COMPAL CONFIDENTIAL

MODEL NAME : *PLM00*

PCB NO : *LA-7161P (DAZ0I800100)*

BOM P/N : *4319AS31L01*
4319AS31L02
4319AS31L03
4319AS31L04
4319AS31L05
4319AS31L06
4319AS31L07
4319AS31L08

Andros MLK

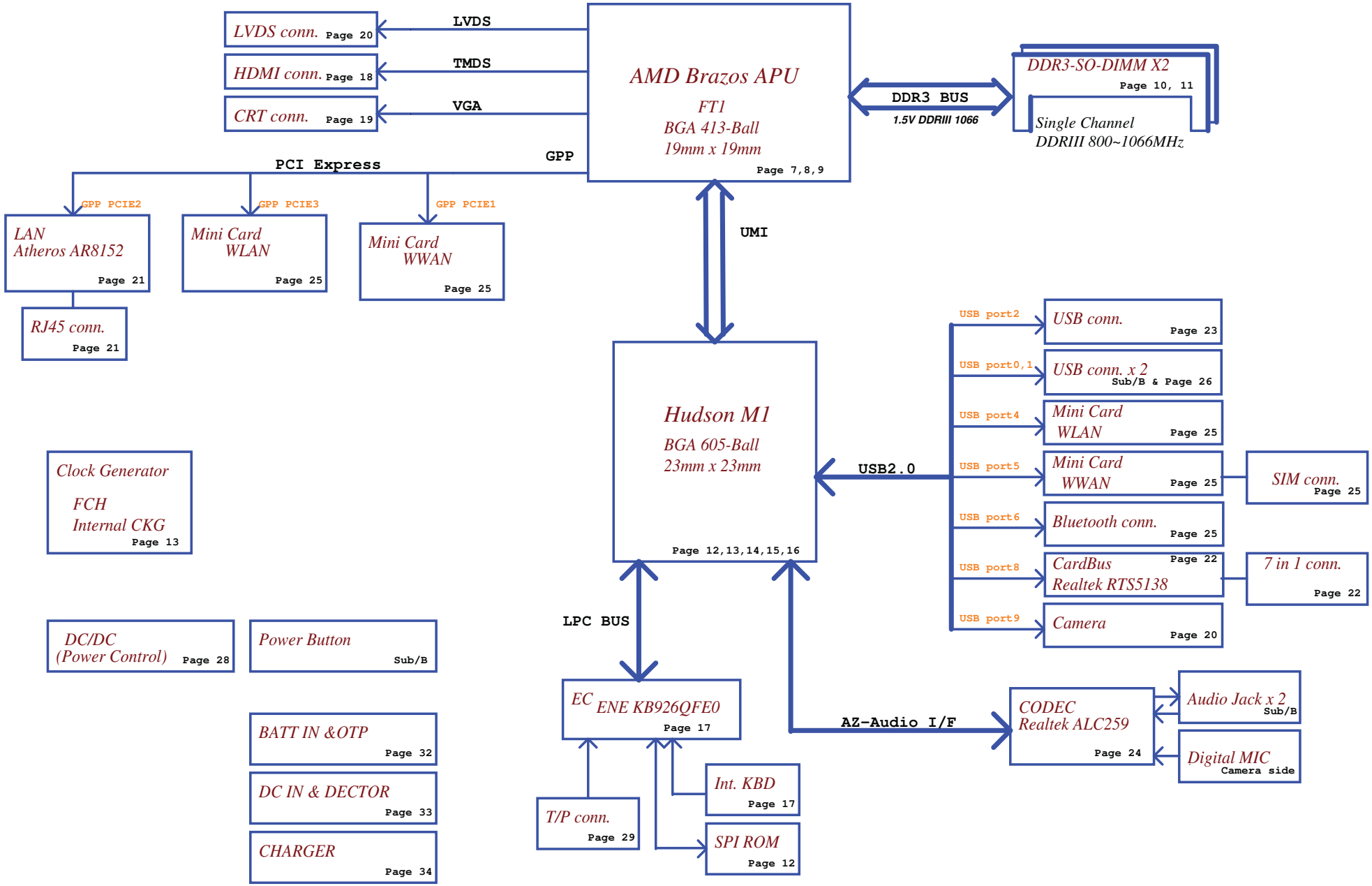
AMD APU (Ontario/Zacate) -FT1 + FCH Hudson-M1

2011-01-05

REV : 1.0(A00)

@ : Nopop Component
WWAN@: WWAN function
CONN@: Connector only
Z@ : Zacate
O@ : Ontario

Compal Electronics, Inc.
Title: Cover Sheet
Size | Document Number: LA-7161P | Rev: 1.0
Date: Wednesday, January 05, 2011 Sheet 1 of 43



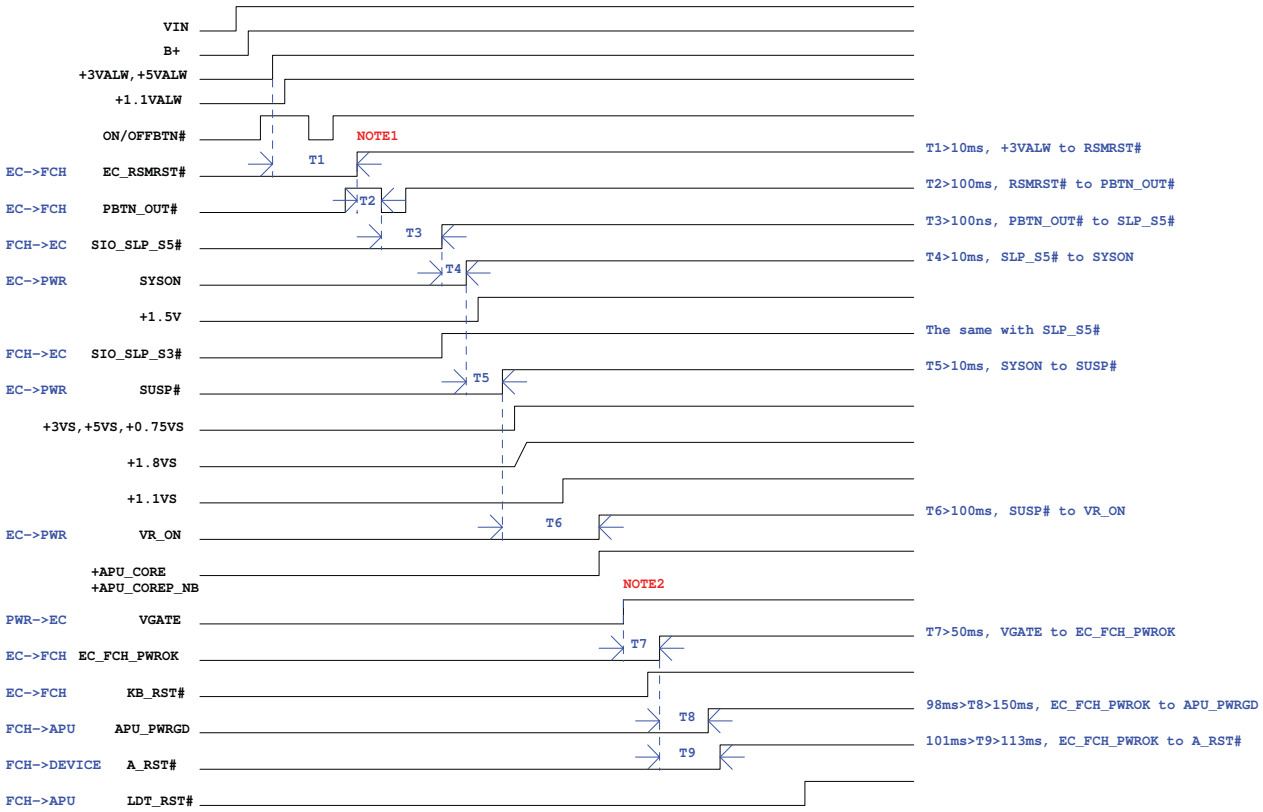
Compal Electronics, Inc.

Title: Block Diagram

Size | Document Number: LA-7161P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 2 of 43

POWER SEQUENCE



NOTE1: RSMRST# rise time(10% to 90%)<50ms
fail time<1ms

NOTE2: EC_FCH_PWROK rise time(10% to 90%)<50ms
fail time<1ms

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

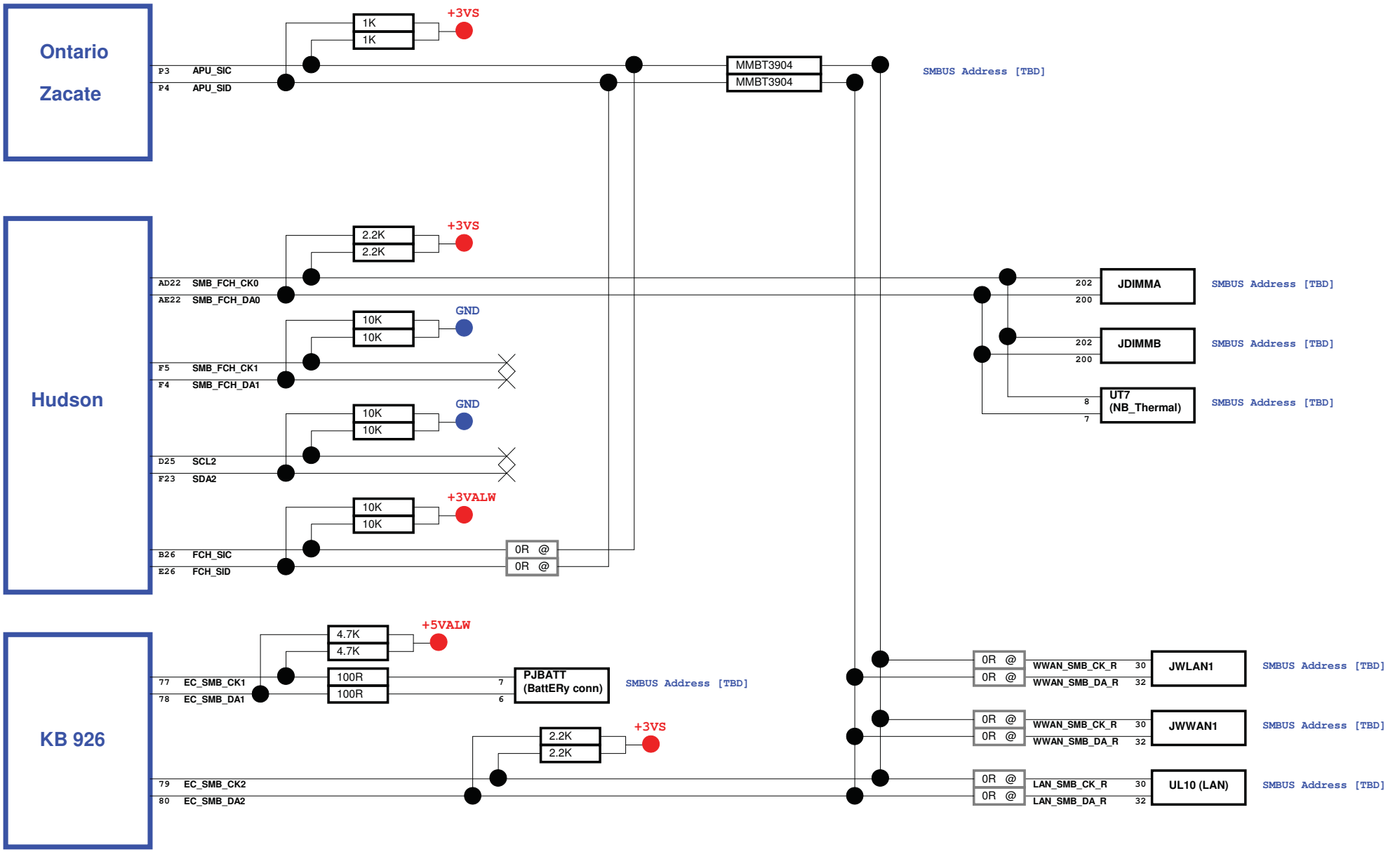
Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

Title: Power Rails		
Size	Document Number: LA-7161P	Rev
Date: Wednesday, January 05, 2011	Sheet 4 of 43	



Compal Electronics, Inc.

Title: SMBus Topology

Size | Document Number: LA-7161P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 5 of 43

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

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1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

SMBUS Control Table

	SOURCE	MIINI1	BATT	MINI2	EXPRESS CARD	SODIMM
EC_SMB_CK1 EC_SMB_DA1	KB926	X	V	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V	X
MEM_SMBCLK MEM_SMBDATA	PCH	X	X	X	X	V

CLKOUT	DESTINATION
PCI0	None
PCI1	PCICLK1
PCI2	PCICLK2
PCI3	PCICLK3
PCI4	PCICLK4

	USB PORT#	DESTINATION
USB	0	USB Port 0 (Sub-board)
	1	USB Port 1 (Sub-board)
	2	USB Port 2
	3	None
	4	MiniCard- WLAN
	5	MiniCard- WWAN
	6	None
	7	None
	8	Card Reader
	9	Camera
	10	None
	11	None
	12	None
	13	None

	DIFFERENTIAL	DESTINATION
CLK	CLKOUT_PCIE0	10/100 LAN
	CLKOUT_PCIE1	MINI CARD- WLAN
	CLKOUT_PCIE2	MINI CARD- WWAN
	CLKOUT_PCIE3	None
	CLKOUT_PCIE4	None
	CLKOUT_PCIE5	None
	CLKOUT_PCIE6	None
	CLKOUT_PCIE7	None
	CLKOUT_PCIE8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

SATA	DESTINATION
SATA0	HDD1
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

APU

PCI EXPRESS	DESTINATION
Port0	None
Port1	WWAN
Port2	10/100
Port3	WLAN

FCH

PCI EXPRESS	DESTINATION
Port0	None
Port1	None
Port2	None
Port3	None

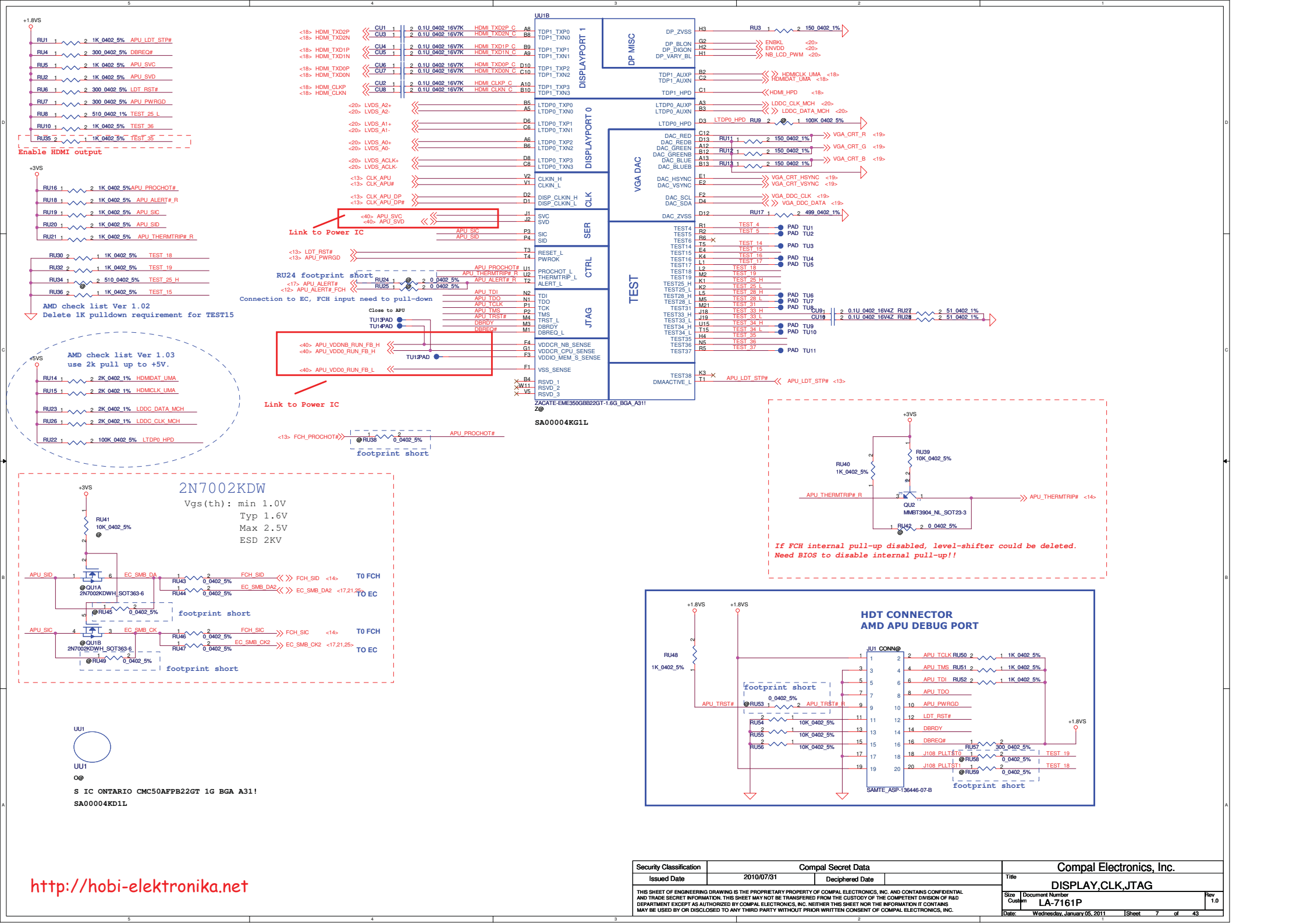
Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: Notes List

Size: Custom | Document Number: LA-7161P | Rev: 1.0

Date: Wednesday, January 05, 2011 | Sheet 6 of 43



http://hobi-elektronika.net

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Issued Date	2010/07/31	Deciphered Date	

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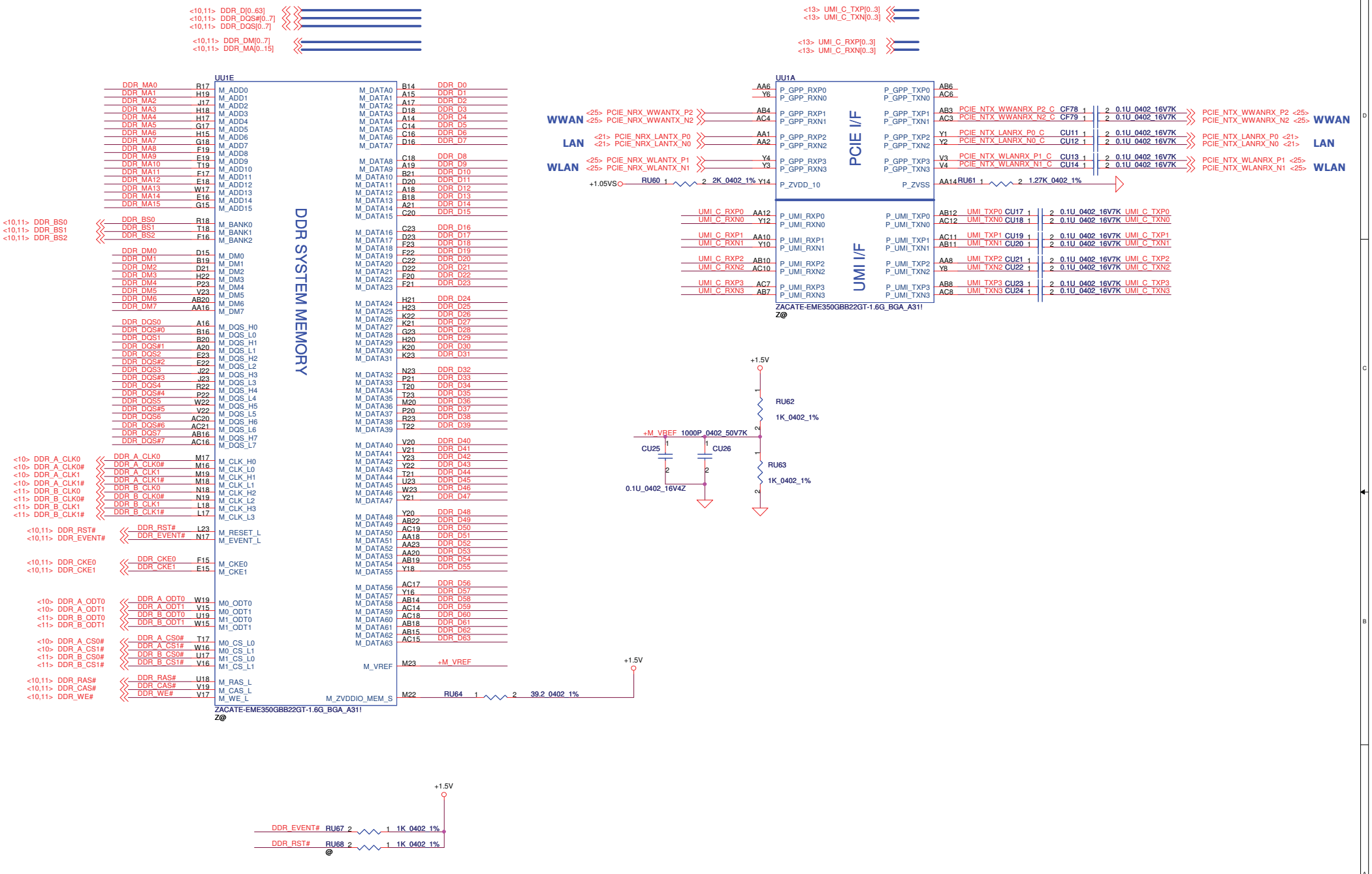
Compal Electronics, Inc.

Title: DISPLAY,CLK,JTAG

Size	Document Number	Rev
Custom	LA-7161P	1.0

Date: Wednesday, January 05, 2011 | Sheet 7 of 43



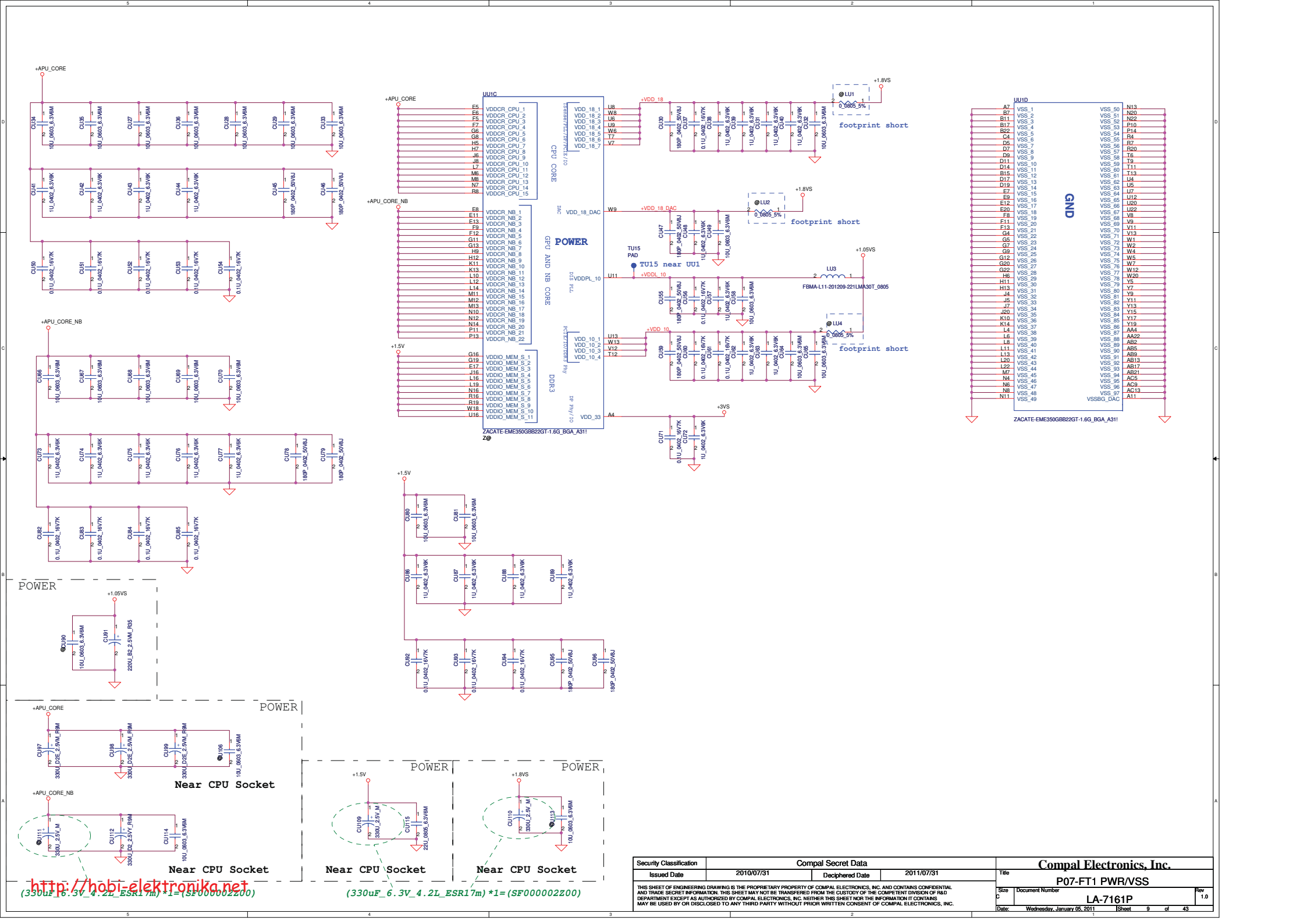
Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	

Compal Electronics, Inc.

Title: DDRIII,UMI

Size	Document Number	Rev
Custom	LA-7161P	1.0

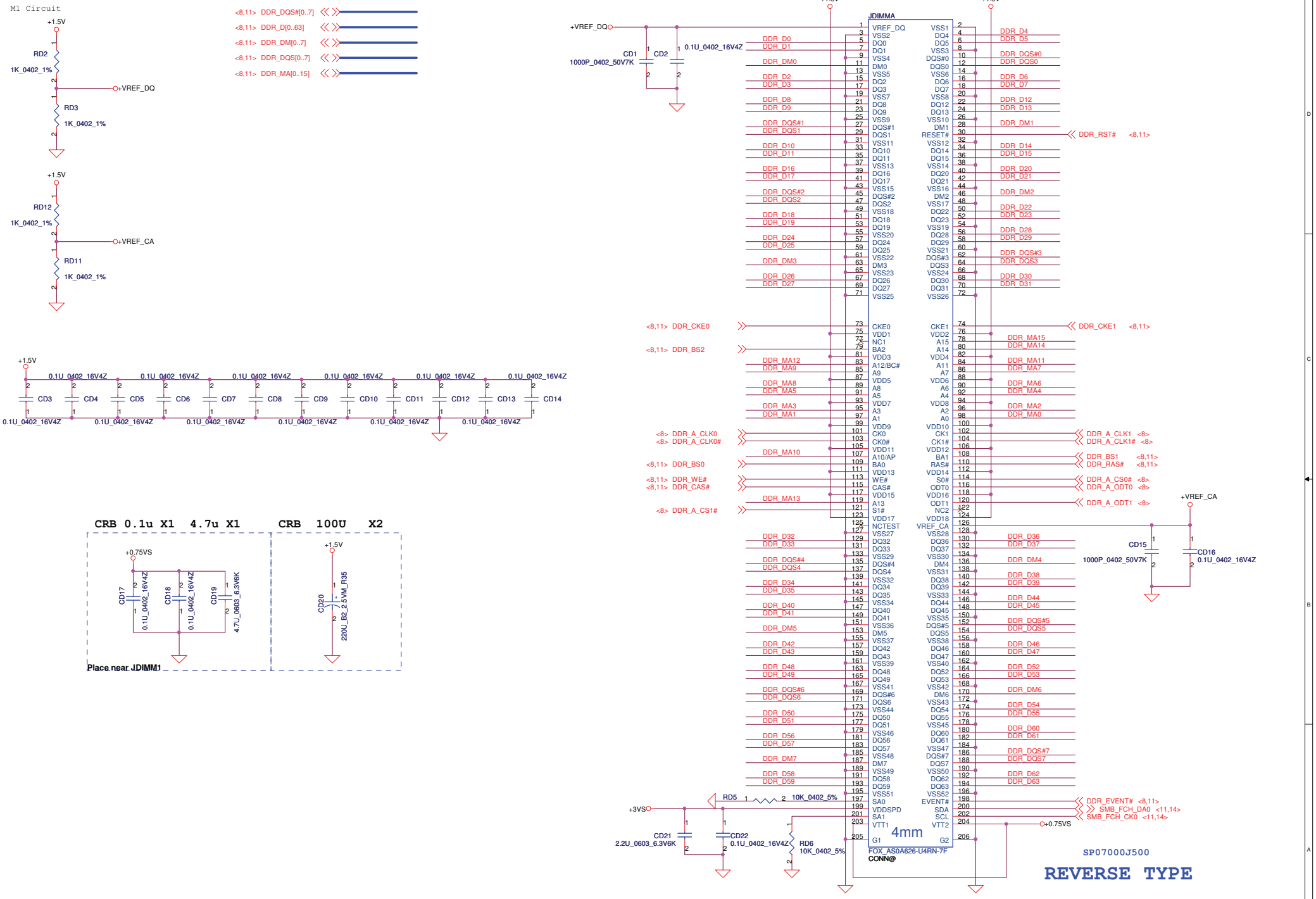
Date: Wednesday, January 05, 2011 | Sheet 8 of 43



Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title	P07-FT1 PWR/VSS	
Size: C	Document Number: LA-7161P	Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 9 of 43	



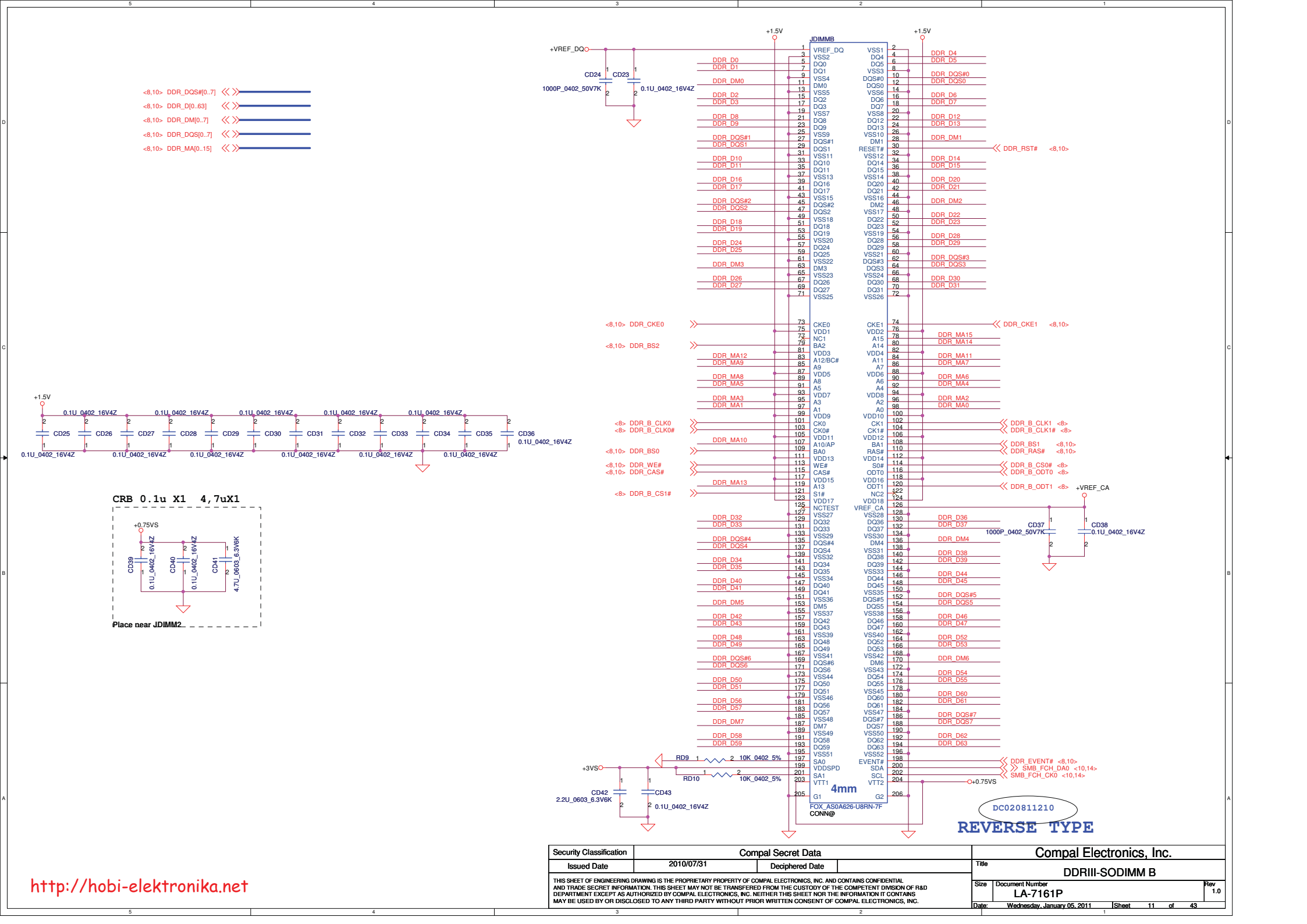
Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

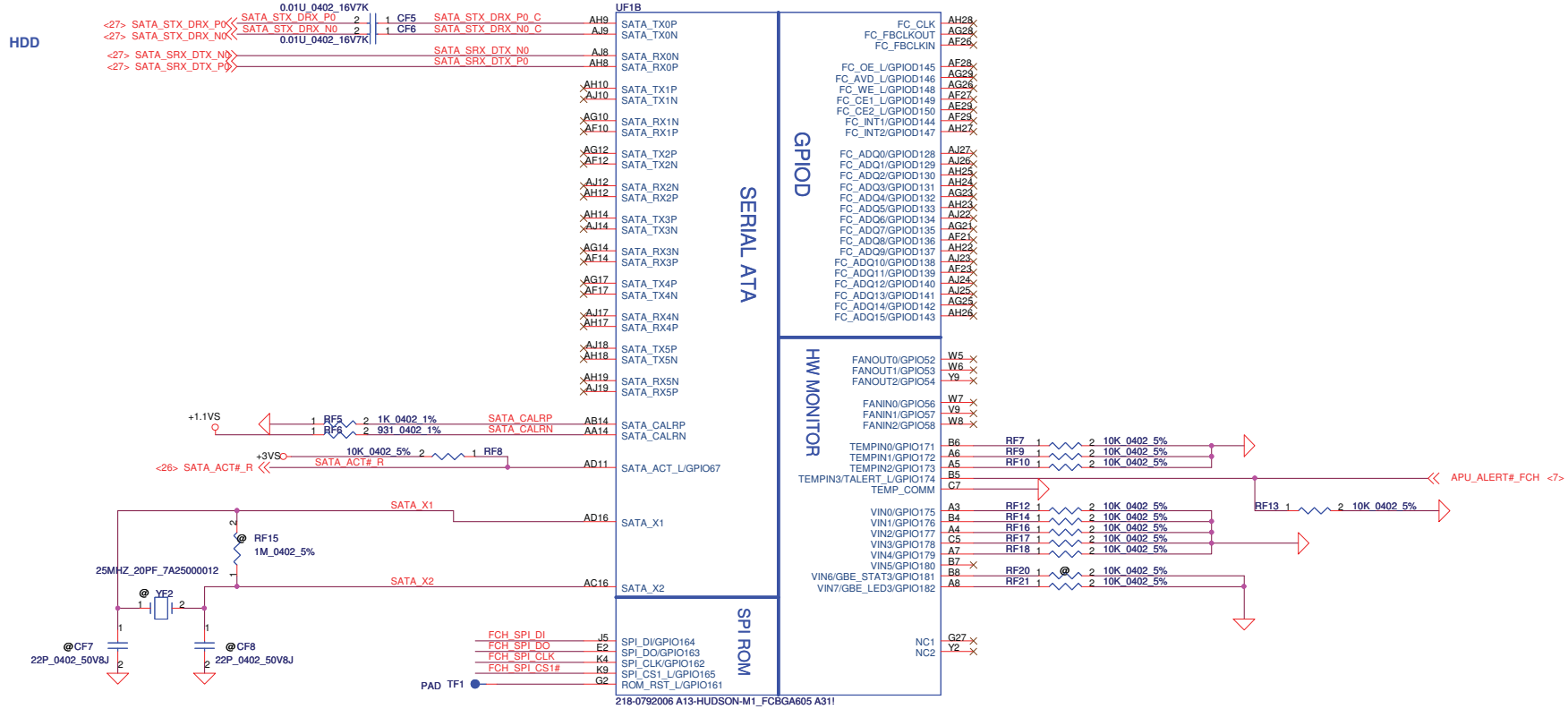
Title: DDRIII-SODIMM A

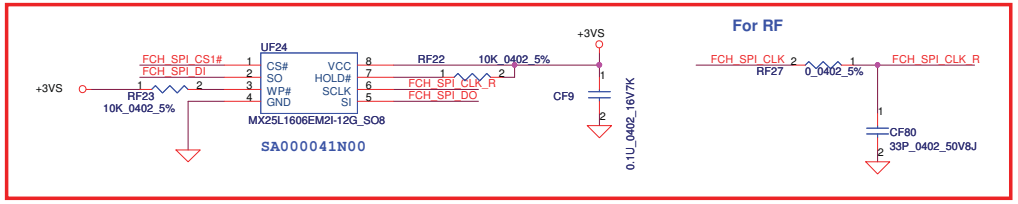
Size	Document Number	Rev
Custom	LA-7161P	1.0

Date: Wednesday, January 05, 2011 Sheet 10 of 43



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/31	Deciphered Date	Title: DDRIII-SODIMM B
Size	Document Number: LA-7161P		Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 11 of 43		





Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	

Compal Electronics, Inc.

Title: SATA,SPI,GPIO

Size	Document Number	Rev
Custom	LA-7161P	1.0

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Need confirm with BIOS

CF77 150P_0402_50V8J
PCIE_RST# RF48 33_0402_5%
PCIE_RST# R

CF10 150P_0402_50V8J
A_RST# RF25 33_0402_5%

UF1E

PCIE_RST_L P1
A_RST_L L1

UMI_C_RXP[0..3] <8>
UMI_C_RXN[0..3] <8>

UMI_C_RXP0 CF16 0.1U_0402_16V7K UMI_RXP0 AD26
UMI_C_RXN0 CF11 0.1U_0402_16V7K UMI_RXN0 AD27
UMI_C_RXP1 CF12 0.1U_0402_16V7K UMI_RXP1 AC28
UMI_C_RXN1 CF17 0.1U_0402_16V7K UMI_RXN1 AC29
UMI_C_RXP2 CF18 0.1U_0402_16V7K UMI_RXP2 AB29
UMI_C_RXN2 CF13 0.1U_0402_16V7K UMI_RXN2 AB28
UMI_C_RXP3 CF14 0.1U_0402_16V7K UMI_RXP3 AB26
UMI_C_RXN3 CF15 0.1U_0402_16V7K UMI_RXN3 AB27

UMI_TX0P
UMI_TX0N
UMI_TX1P
UMI_TX1N
UMI_TX2P
UMI_TX2N
UMI_TX3P
UMI_TX3N

UMI_C_TXP[0..3] <8>
UMI_C_TXN[0..3] <8>

UMI_C_TXP0 AE24
UMI_C_TXN0 AE23
UMI_C_TXP1 AD25
UMI_C_TXN1 AD24
UMI_C_TXP2 AC24
UMI_C_TXN2 AC25
UMI_C_TXP3 AB25
UMI_C_TXN3 AB24

UMI_RX0P
UMI_RX0N
UMI_RX1P
UMI_RX1N
UMI_RX2P
UMI_RX2N
UMI_RX3P
UMI_RX3N

RF26 590_0402_1% PCIE_CALRP AD29
RF28 2K_0402_1% PCIE_CALRN AD28
+1.1VS

PCIE_CALRP
PCIE_CALRN

PCI EXPRESS I/F

GPP_TX0P AA28
GPP_TX0N AA29
GPP_TX1P Y29
GPP_TX1N Y28
GPP_TX2P Y26
GPP_TX2N Y27
GPP_TX3P W28
GPP_TX3N W29

GPP_RX0P AA22
GPP_RX0N Y21
GPP_RX1P AA25
GPP_RX1N AA24
GPP_RX2P W23
GPP_RX2N V24
GPP_RX3P W24
GPP_RX3N W25

PCIE_RCLKP/NB_LNK_CLKP M23
PCIE_RCLKN/NB_LNK_CLKN P23

<7> CLK_APU_DP
<7> CLK_APU_DP#
RF33 0_0402_5% CLK_APU_DP_R U29
RF34 0_0402_5% CLK_APU_DP#_R U28

NB_DISP_CLKP
NB_DISP_CLKN

NB_HT_CLKP T26
NB_HT_CLKN T27

<7> CLK_APU
<7> CLK_APU#
RF35 0_0402_5% CLK_APU_R V21
RF36 0_0402_5% CLK_APU#_R T21

CPU_HT_CLKP
CPU_HT_CLKN

SLT_GFX_CLKP V23
SLT_GFX_CLKN T23

<21> CLK_PCIE_LAN_P
<21> CLK_PCIE_LAN_N
RF37 0_0402_5% CLK_PCIE_LAN_P_R L29
RF38 0_0402_5% CLK_PCIE_LAN_N_R L28

<25> CLK_PCIE_WLAN_P
<25> CLK_PCIE_WLAN_N
RF39 0_0402_5% CLK_PCIE_WLAN_P_R N29
RF40 0_0402_5% CLK_PCIE_WLAN_N_R N28

<25> CLK_PCIE_WWAN_P
<25> CLK_PCIE_WWAN_N
RF41 0_0402_5% CLK_PCIE_WWAN_P_R M29
RF42 0_0402_5% CLK_PCIE_WWAN_N_R M28

GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P T25
GPP_CLK3N V25
GPP_CLK4P L24
GPP_CLK4N L23
GPP_CLK5P P25
GPP_CLK5N M25
GPP_CLK6P P29
GPP_CLK6N P28
GPP_CLK7P N26
GPP_CLK7N N27
GPP_CLK8P T29
GPP_CLK8N T28

CLOCK GENERATOR

Place close to UF1
RF Change to 33PF
CF20 33P_0402_50V8J
RF47 33_0402_5%
<22> CLK_48M
CLK_48M R L25
14M_25M_48M_OSC

CF21 22P_0402_50V8J
CF22 22P_0402_50V8J
YF1 25MHZ_20PF_7A25000012
RF49 1M_0402_5%
XTAL25_IN L26
XTAL25_OUT L27
25M_X1
25M_X2

218-0792006 A13-HUDSON-M1_FCBGA605 A31!

PCICLK0 W2
PCICLK1/GPO36 W1 PAD TF3
PCICLK2/GPO37 W3
PCICLK3/GPO38 W4
PCICLK4/14M_OSC/GPO39 Y1
PCICLK1 <16>
PCICLK2 <16>
PCICLK3 <16>
PCICLK4 <16>
PCIRST_L V2 PAD TF4

PCI CLKS

AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9 PCI_AD23
AD24/GPIO24 AD9 PCI_AD24
AD25/GPIO25 AC11 PCI_AD25
AD26/GPIO26 AF6 PCI_AD26
AD27/GPIO27 AF4 PCI_AD27
AD28/GPIO28 AF3
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3
CBE0_L AA8
CBE1_L AD5
CBE2_L AD8
CBE3_L AA10
FRAME_L AE8
DEVSEL_L AB9
IRDY_L AJ3
TRDY_L AE7
PAR AC5
STOP_L AF5
PERR_L AE6
SERR_L AE4
REQ0_L AE11
REQ1_L/GPIO40 AH5
REQ2_L/CLK_REQ8_L/GPIO41 AH4
REQ3_L/CLK_REQ5_L/GPIO42 AC12 PAD TF12
GNT0_L AD12
GNT1_L/GPO44 AJ5
GNT2_L/GPO45 AH6
GNT3_L/CLK_REQ7_L/GPIO46 AB12 PAD TF13
CLKRUN_L AB11
LOCK_L AD7

PCI_AD23 <16>
PCI_AD24 <16>
PCI_AD25 <16>
PCI_AD26 <16>
PCI_AD27 <16>

PCI I/F

RF11 10K_0402_5%

INTE_L/GPIO32 AJ6
INTF_L/GPIO33 AG6
INTG_L/GPIO34 AG4
INTH_L/GPIO35 AJ4

LPCCLK0 H24
LPCCLK1 H25
LAD0 J27
LAD1 J26
LAD2 H29
LAD3 H28
LFRAME_L G28
LDRQ0_L J25
LDRQ1_L/CLK_REQ6_L/GPIO49 AA18
SERIRQ/GPIO48 AB19

RF43 0_0402_5% LPCCLK0 <16>
RF44 22_0402_5% CLK_PCI_EC <17>
CLK_DEBUG_PORT_R RF45 0_0402_5% CLK_DEBUG_PORT
RF45 footprint short

LPC_LAD0 <17,25>
LPC_LAD1 <17,25>
LPC_LAD2 <17,25>
LPC_LAD3 <17,25>
LPC_LFRAME# <17,25>
IRQ_SERIRQ <17>

LPC

CLK_DEBUG_PORT <16>
CLK_DEBUG_PORT RF46 0_0402_5% CLK_DEBUG_PORT_1 <25>
CLK_DEBUG_PORT_1 <25>

ALLOW_LDTSTP/DMA_ACTIVE_L G21
PROCHOT_L H21
LDT_PG K19
LDT_STP_L G22
LDT_RST_L J24

APU_LDT_STP# <7>
FCH_PROCHOT# <7>
APU_PWRGD <7>
LDT_RST# <7>

CPU

32K_X1 C1 FCH_RTCX1
32K_X2 C2 FCH_RTCX2
RTCCLK D2 SUSCLK <17>
INTRUDER_ALERT_L B2
VDDBT_RTC_G B1 RTCVCC_R
RF50 510_0402_5% +RTCVCC
W=20mils
CF23 1U_0402_6.3V4Z
CMOS1 @ SHORT PADS for Clear CMOS

RTC

+1.8VS
+3VS
RF24 10K_0402_5%
APU_PWRGD 3
APU_PWRGD_CORE <40>
QF2 FDV301N_NL_SOT23-3-D

Link to Power IC

Close to SB
CF24 22P_0402_50V8J
XF1 32.768KHZ_12.5PF_9H03200413
FCH_RTCX1
FCH_RTCX2
RF51 20M_0603_5%
CF25 22P_0402_50V8J

it can be swap if need
CF19 0.1U_0402_16V7K +3VALW
PCIE_RST#
A_RST#
UF25 NC7SZ08P5X_NL_SC70-5
PLT_RST# <17,21,25>
RF31 100K_0402_5%
RF32 0_0402_5%

SUSCLK
@CF83 10P_0402_50V8J
RF reserved

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/07/31	Deciphered Date	Title: UMI,PCIE,CLK,PCI,LPC,RTC,CPU

Size	Document Number	Rev
Custom	LA-7161P	1.0

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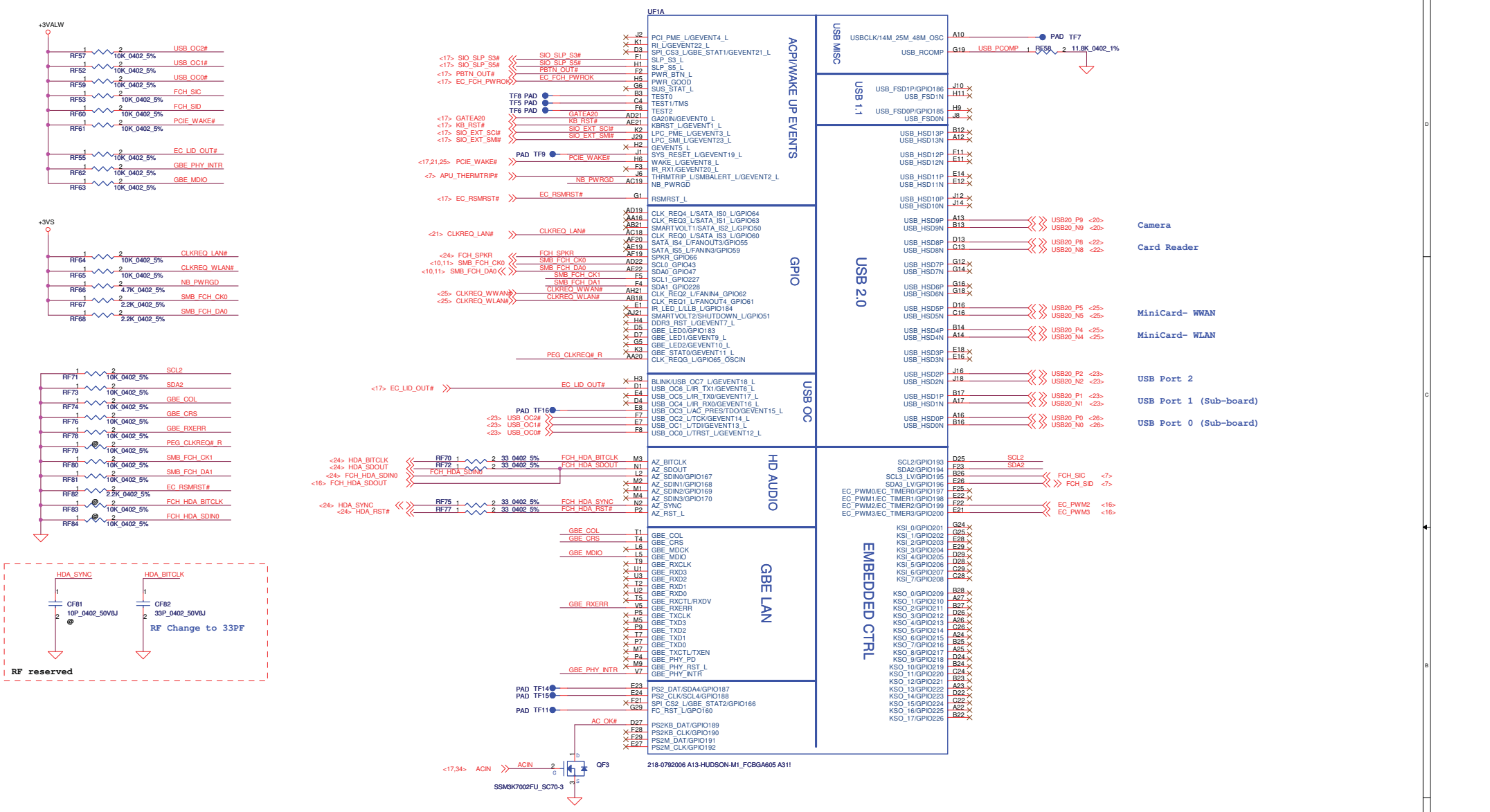

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: USB,GPIO,GLAN,HDA

Size	Document Number	Rev
Custom	LA-7161P	1.0

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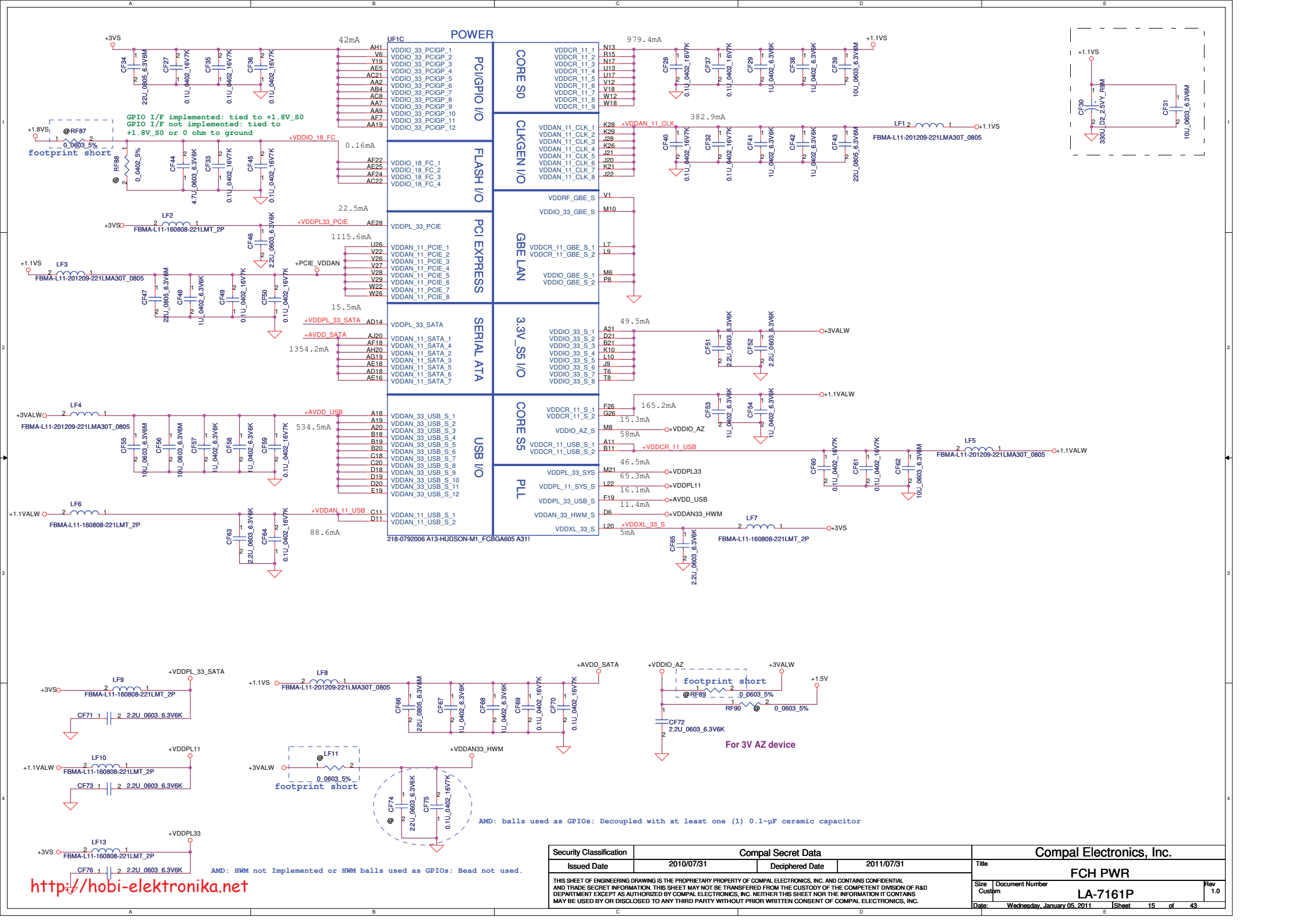

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: LA-7161P | Rev: 1.0

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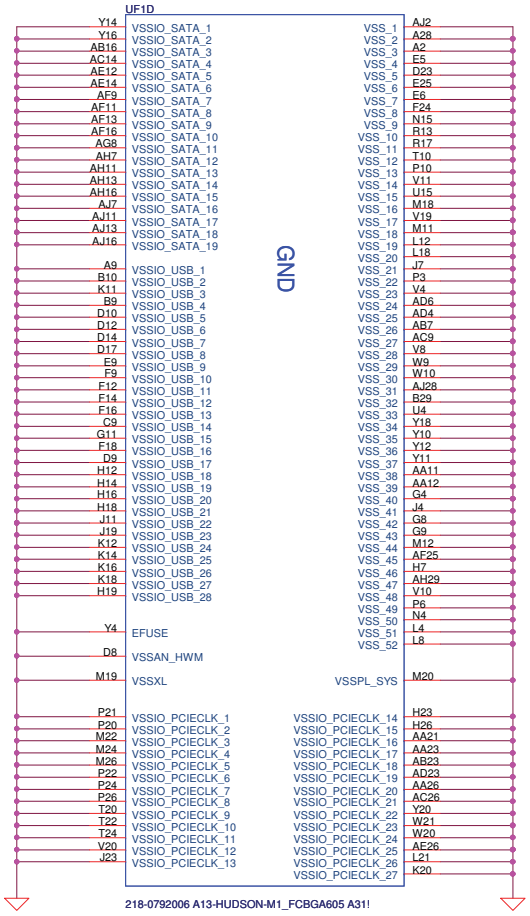
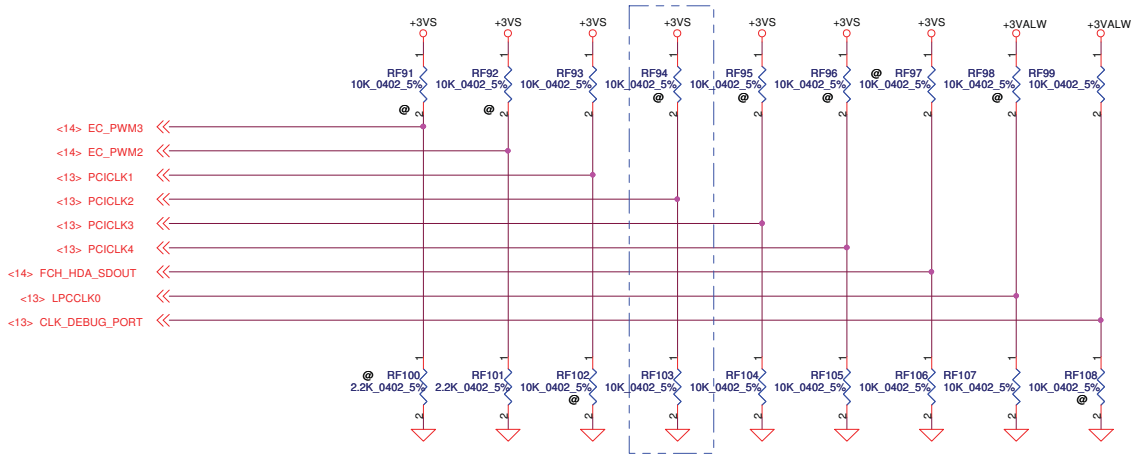
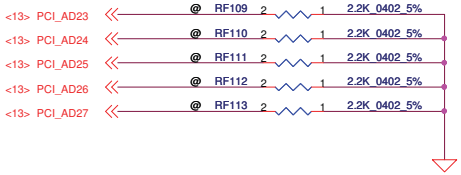




Watchdog timer on NB_PWRGD
enable for pull-up
disable for pull-down
20100527



Net Name	Description
CLK_PCI_EC_R	0 : Integrated Microcontroller (IMC) Disabled * 1 : Integrated Microcontroller (IMC) Enabled
EC_PWM3 *EC_PWM2*	EC_PWM3 / EC_PWM2 / ROM TYPE: x / 0 / SPI ROM * x / x / Reserved 0 / 0 / Reserved 0 / x / LPC ROM
CLK_DEBUG_PORT	0 : External clock mode. 1 : Integrated clock mode. *
PCICLK1	0 : Force PCIe interface at Gen I mode. 1 : PCIe interface is at Gen II mode. *
PCICLK2	0 : Disable the boot fail timer function. * 1 : Enable the boot fail timer function.
PCICLK3	0 : Disable Debug Straps. * 1 : Select external Debug Straps.
PCICLK4	0 : Required setting for integrated clock mode. * 1 : Reserved.
HDA_SDOUT_R	0 : Required setting for integrated clock mode. * 1 : Reserved (Hudson-1 does not support the lower power mode).

Net Name	Description
PCI_AD27	0 : Bypass internal PLL clock 1 : Use internal PLL-generated PLL CLK *
PCI_AD26	0 : ILA auto run enable 1 : ILA auto run disable *
PCI_AD25	0 : Bypass internal FC Clk 1 : Use internal PLL FC Clk * NEED CHECK
PCI_AD24	0 : Getting the value from I2C EPROM 1 : Disable I2C ROM * NEED CHECK
PCI_AD23	0 : Reserved 1 : Required setting (use ROMTYPE straps to determine the ROM type) *

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Compal Electronics, Inc.

Title	GND		
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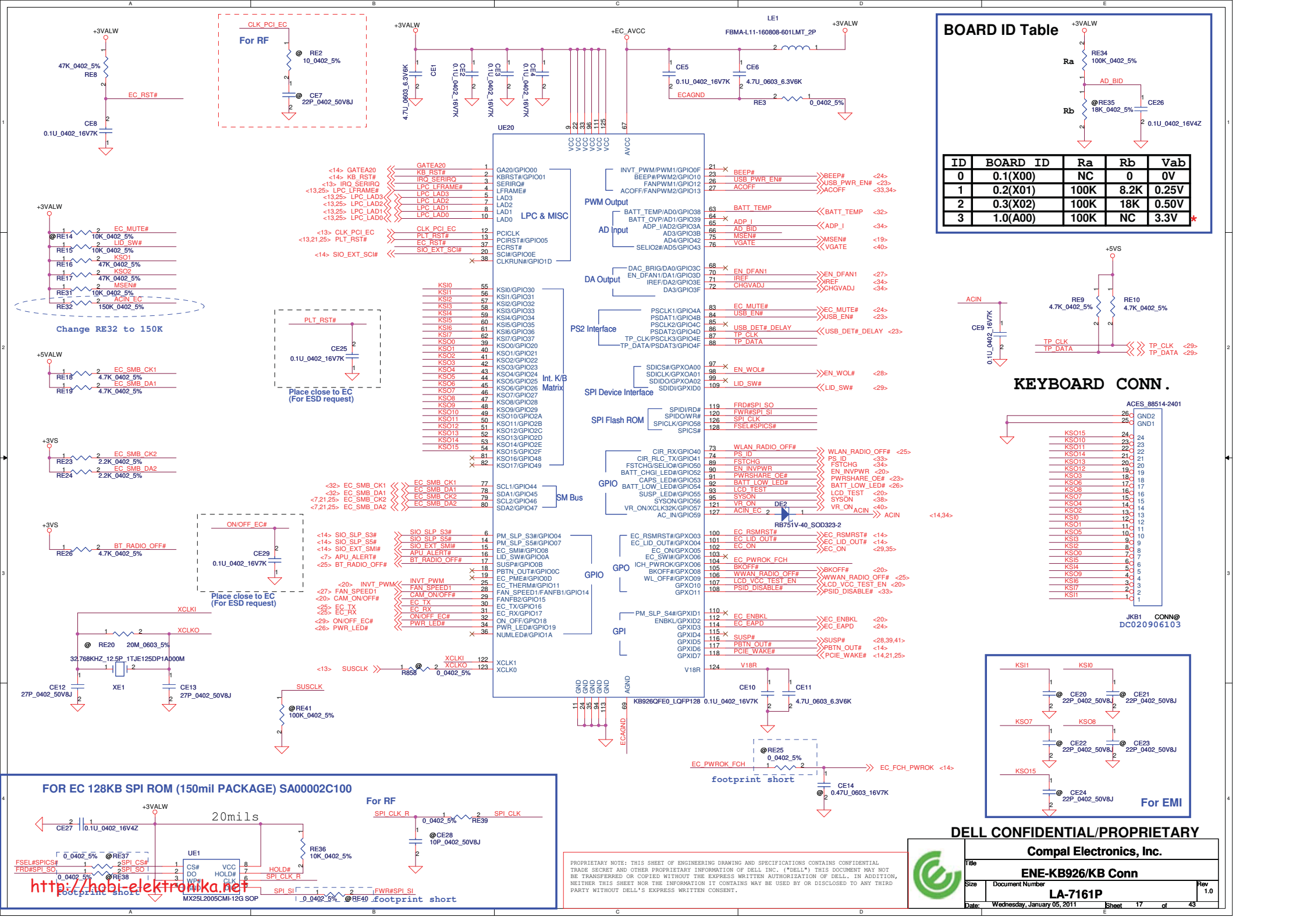
BOARD ID Table
ID | BOARD ID | Ra | Rb | Vab
0 | 0.1(X00) | NC | 0 | 0V
1 | 0.2(X01) | 100K | 8.2K | 0.25V
2 | 0.3(X02) | 100K | 18K | 0.50V
3 | 1.0(A00) | 100K | NC | 3.3V *
KEYBOARD CONN.
ACES_88514-2401
JKB1 CONN@ DC020906103
UE20 KB926QFE0_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
LE1 FBMA-L11-160808-601LMT_2P
Change RE32 to 150K
Place close to EC (For ESD request)
Place close to EC (For ESD request)
For RF
For EMI
FOR EC 128KB SPI ROM (150mil PACKAGE) SA00002C100
UE1 MX25L2005CMI-12G SOP
footprint short
footprint short
footprint short
http://hobi-elektronika.net
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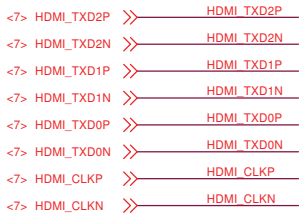
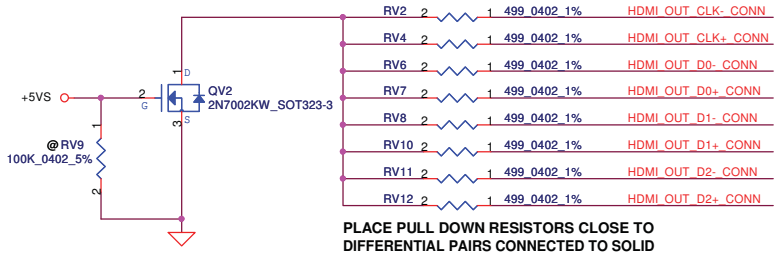
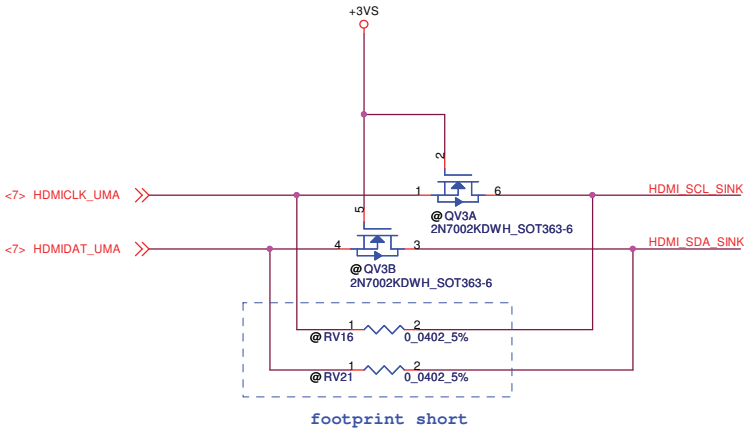
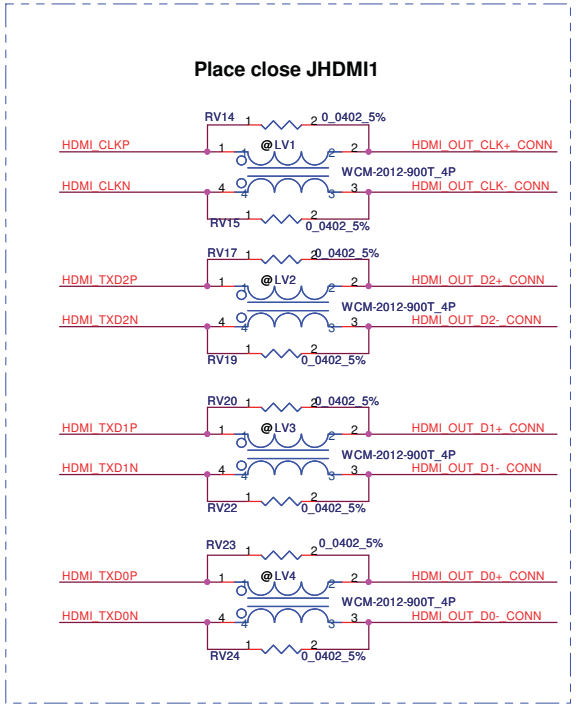
Compal Electronics, Inc.
ENE-KB926/KB Conn
LA-7161P
Wednesday, January 05, 2011

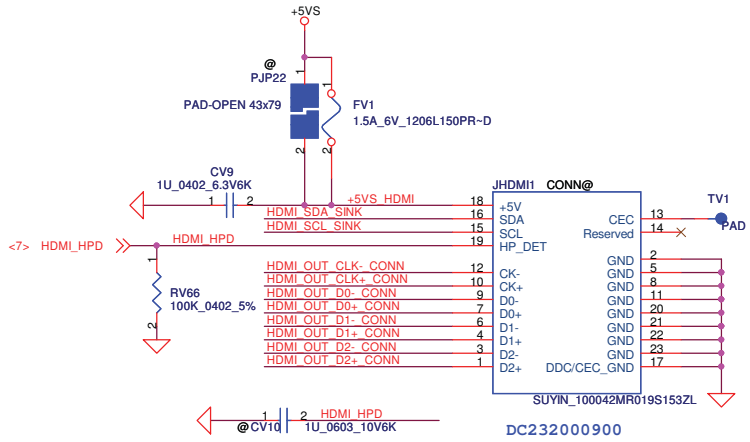




PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES







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Title: HDMI Conn.		
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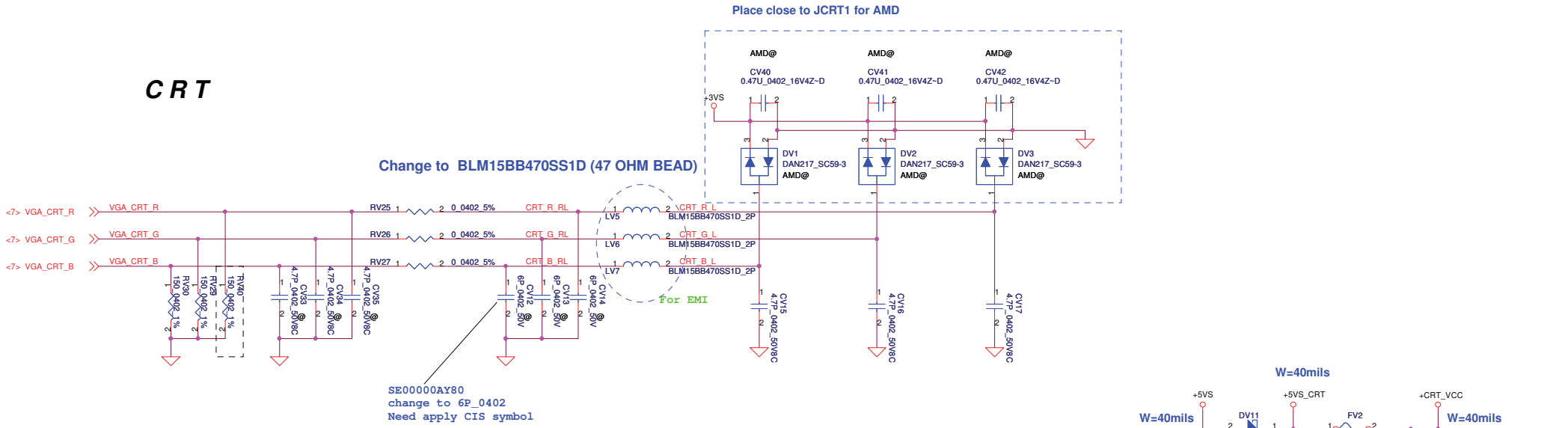
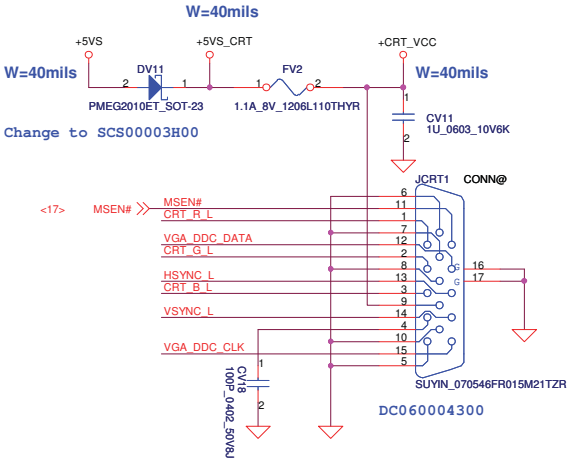
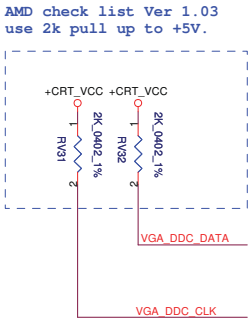
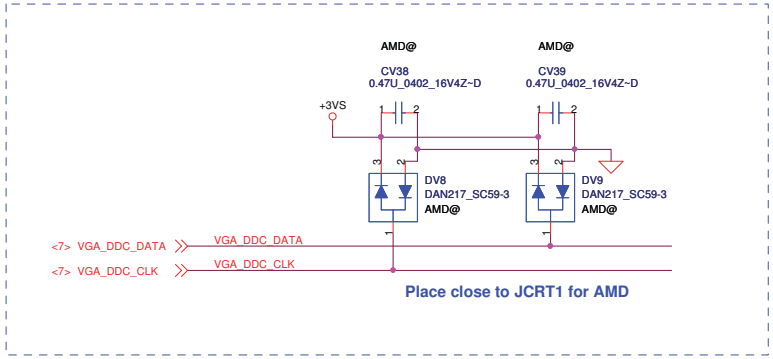
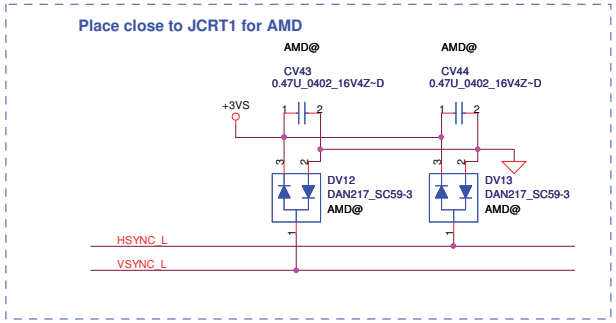
CRT

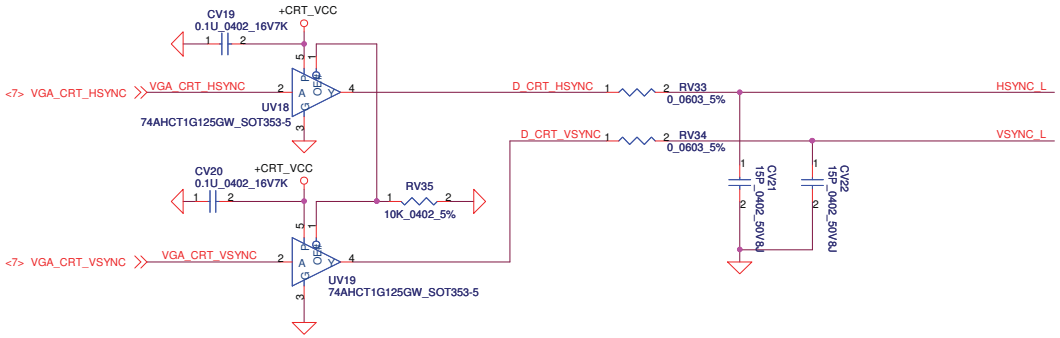












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Compal Electronics, Inc.	
Title	VGA Conn.
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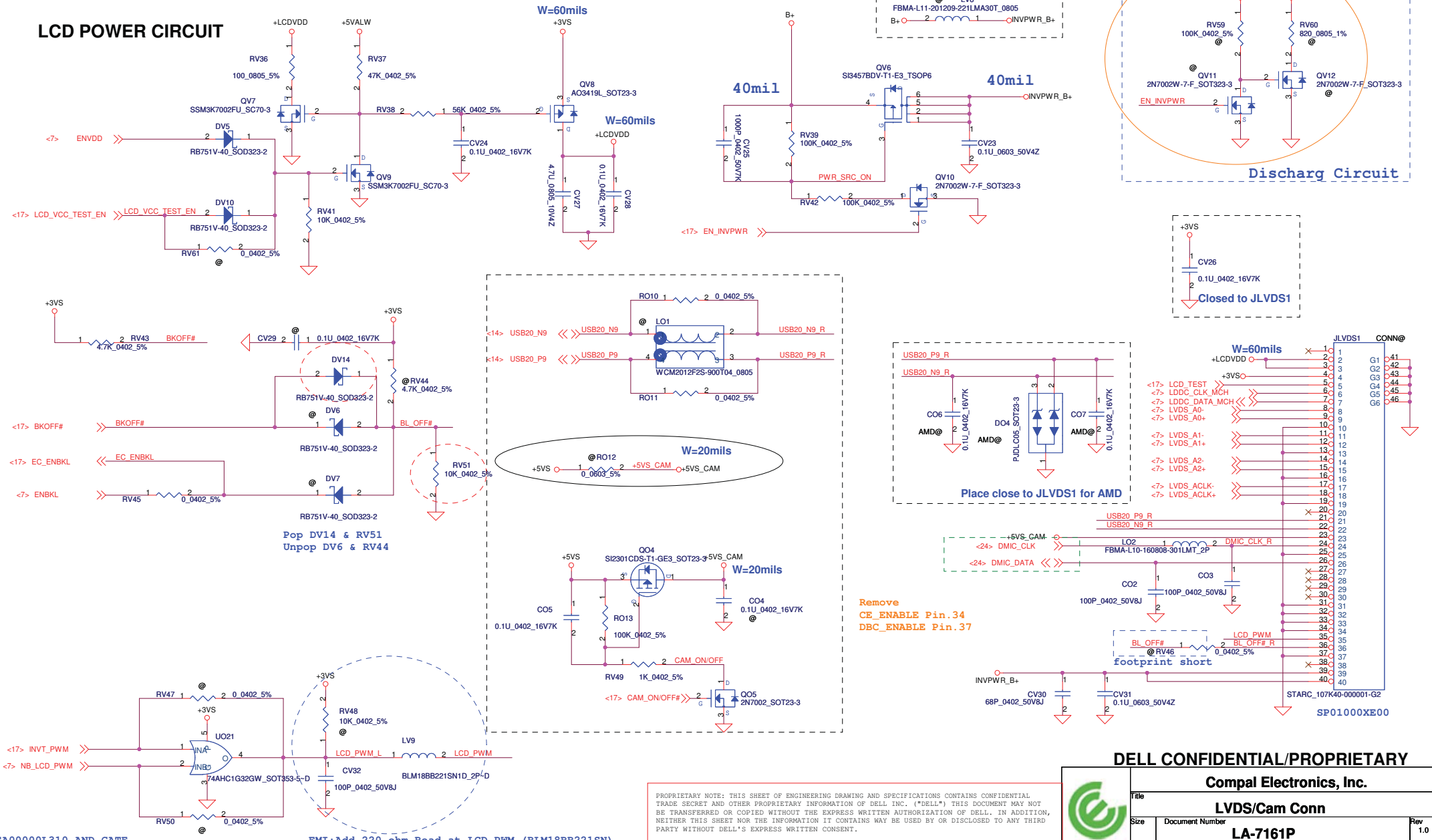
LCD POWER CIRCUIT



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Compal Electronics, Inc.

Title: LVDS/Cam Conn

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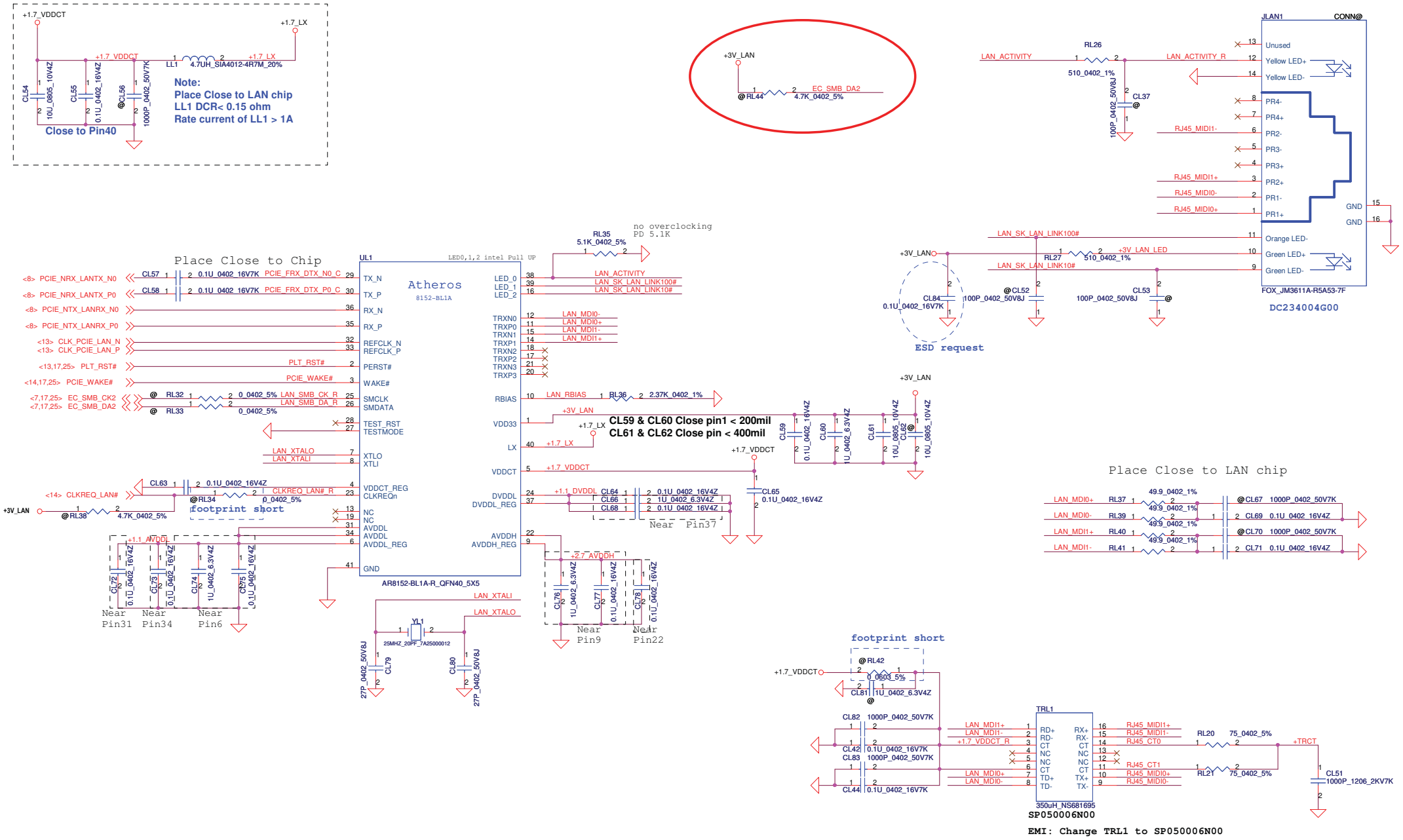

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Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.			
Title	LAN-8152		
Size: Custom	Document Number: LA-7161P		Rev: 1.0
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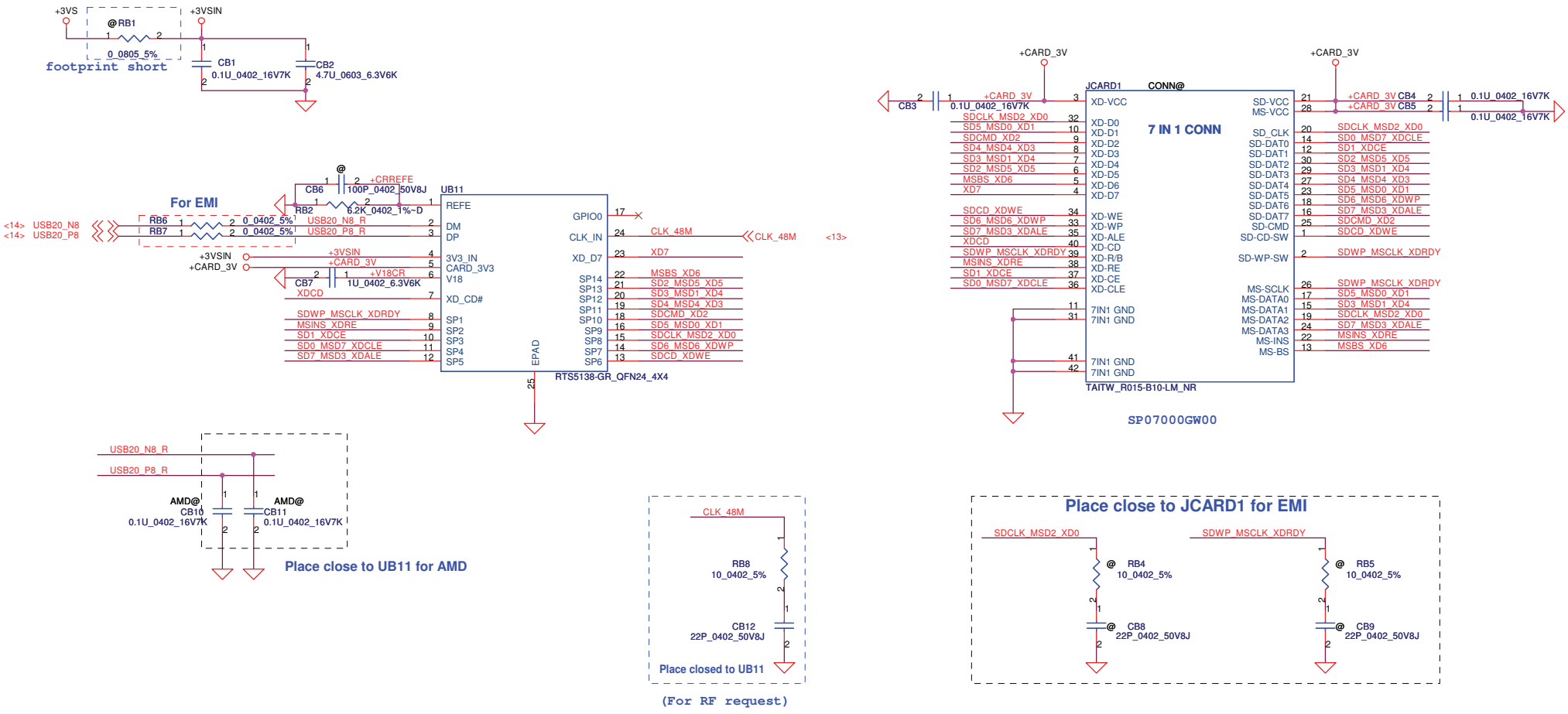

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Title	Card Reader RTS5138
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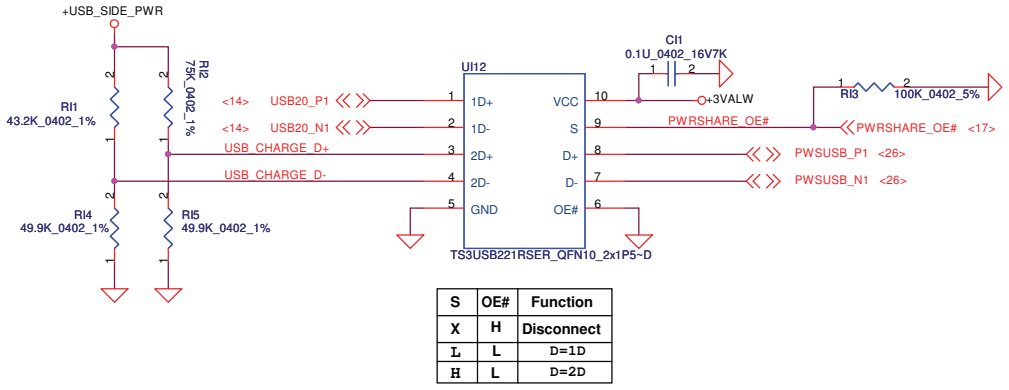
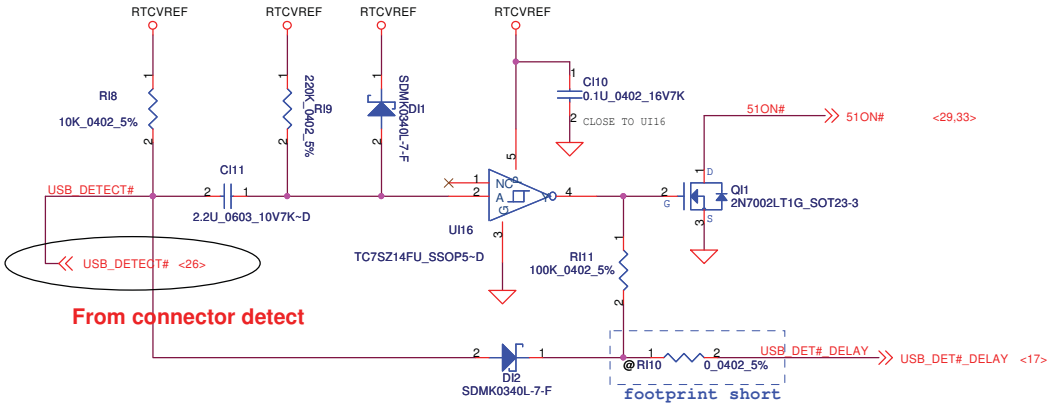
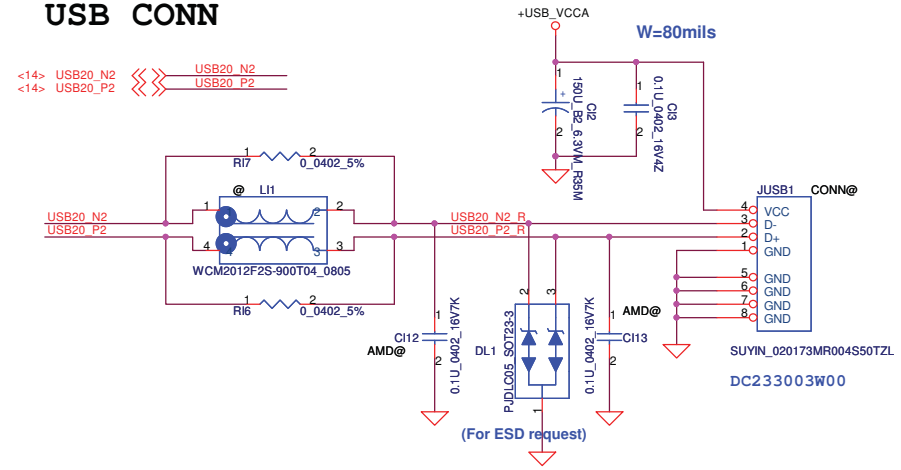


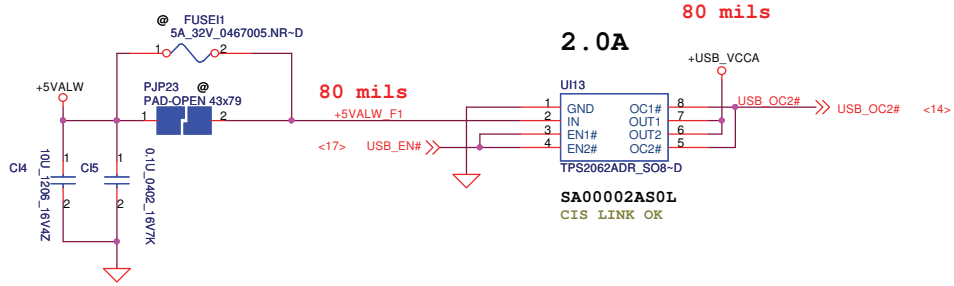
S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

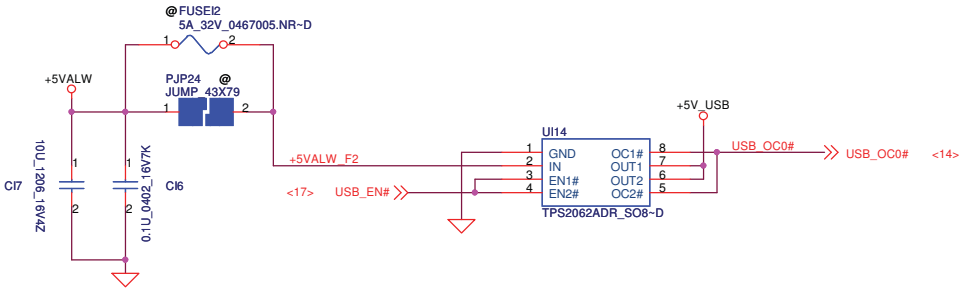


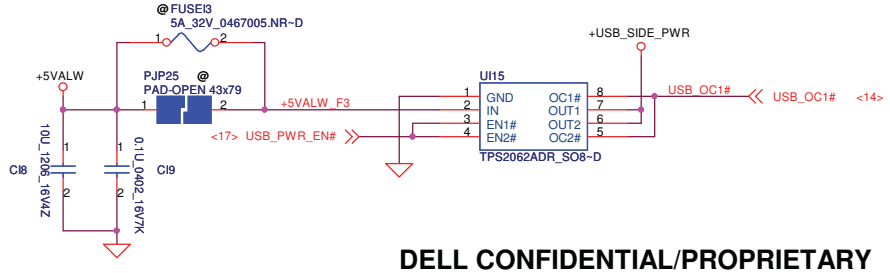
Power share

USB CONN









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Compal Electronics, Inc.	
Title	USB/POWER Share
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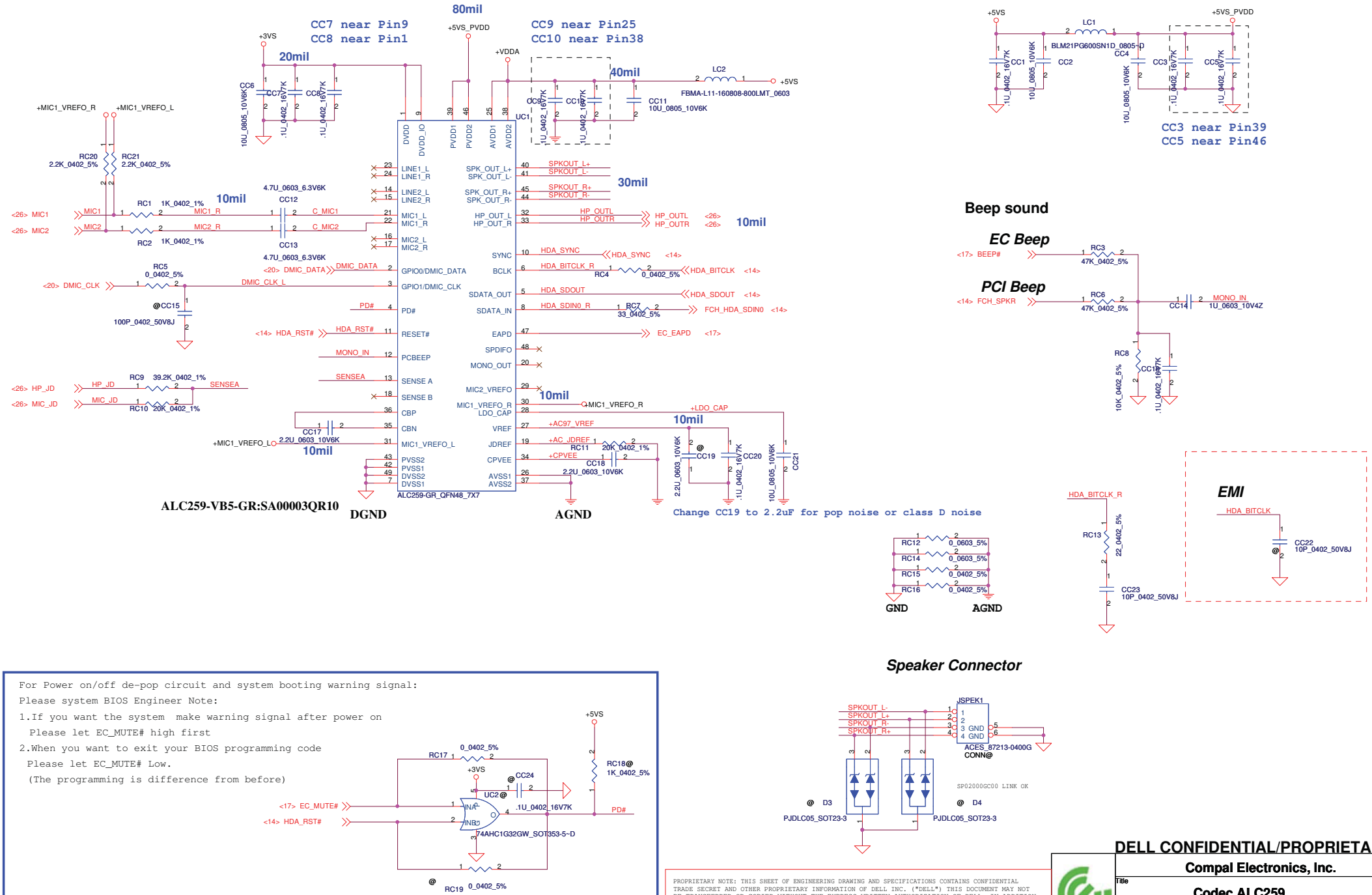
80mil
CC7 near Pin9
CC8 near Pin1
CC9 near Pin25
CC10 near Pin38
20mil
40mil
30mil
10mil
+3VS
+5VS_PVDD
+VDDA
+5VS
+MIC1_VREFO_R
+MIC1_VREFO_L
ALC259-VB5-GR:SA00003QR10
ALC259-GR_QFN48_7X7
DGND
AGND
Change CC19 to 2.2uF for pop noise or class D noise
CC3 near Pin39
CC5 near Pin46
Beep sound
EC Beep
PCI Beep
EMI
Speaker Connector
SP02000GC00 LINK OK
ACES_87213-0400G
CONN@
PJDLC05_SOT23-3
74AHC1G32GW_SOT353-5~D
For Power on/off de-pop circuit and system booting warning signal:
Please system BIOS Engineer Note:
1.If you want the system make warning signal after power on
Please let EC_MUTE# high first
2.When you want to exit your BIOS programming code
Please let EC_MUTE# Low.
(The programming is difference from before)
http://hobi-elektronika.net
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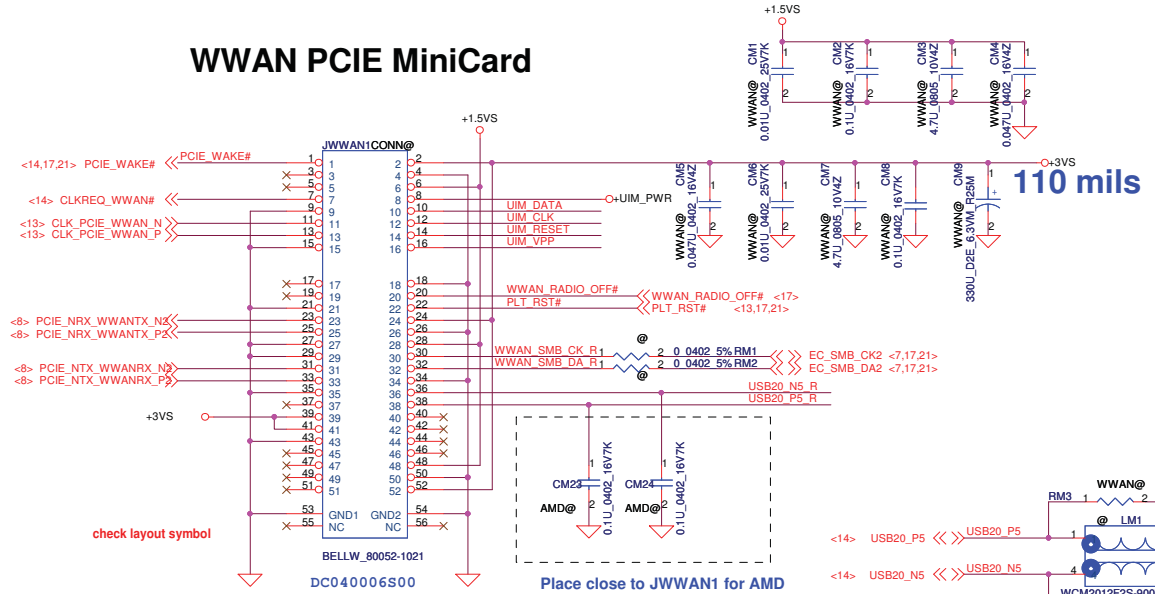
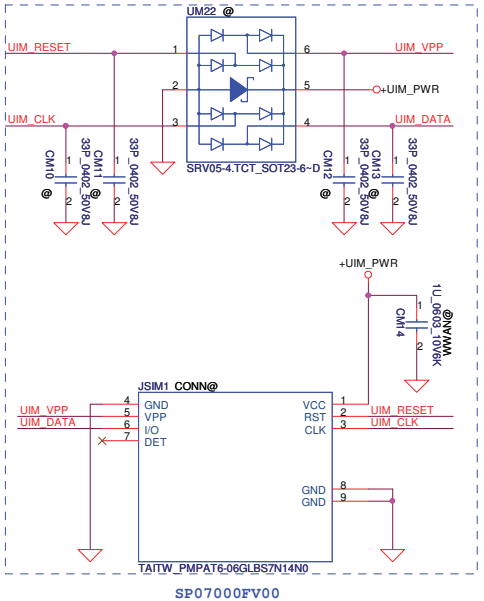
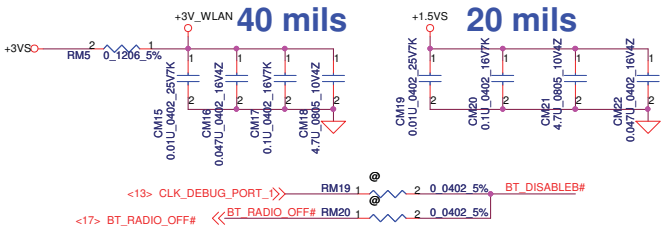
WWAN PCIE MiniCard



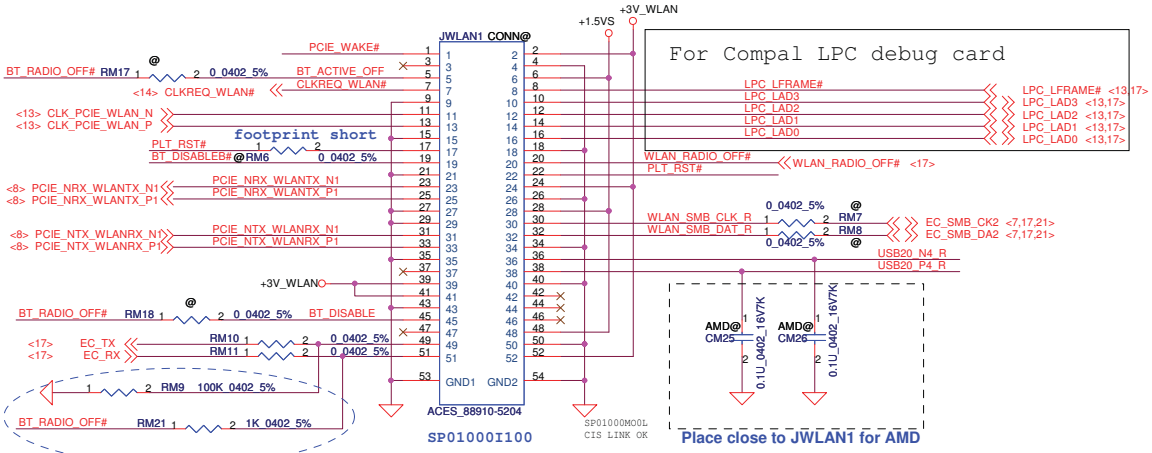
SIM Card

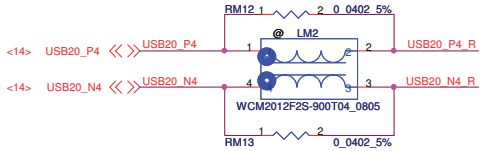


WLAN/WIMAX PCIE Mini Card



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA





RF:Andros MLK will use DW1702 combo card

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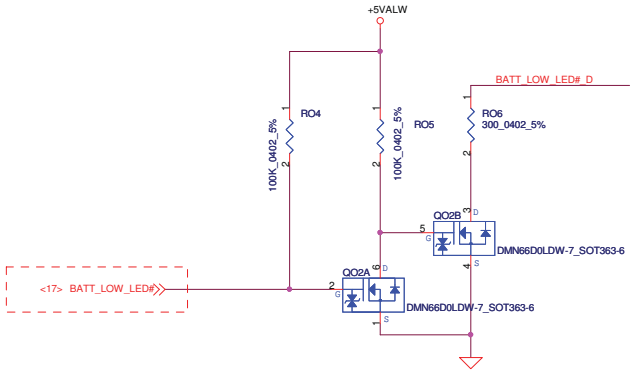
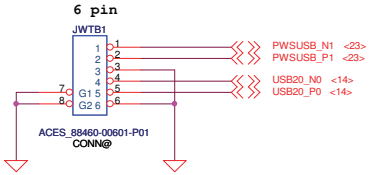
BATT CHARGE

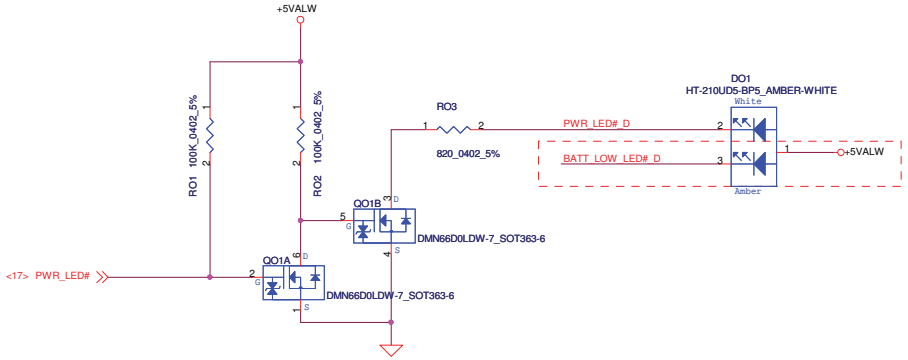


6 pin

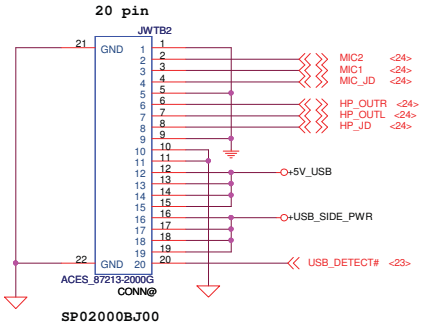


SP010013W00

Power LED

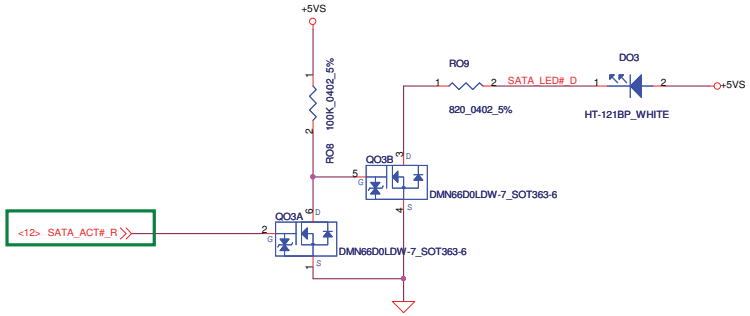


20 pin



SP02000BJ00

HD LED



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Title	WTB Conn/LED
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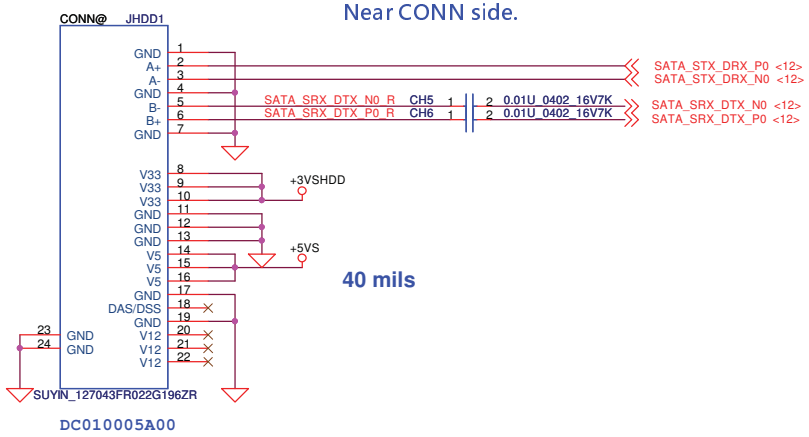
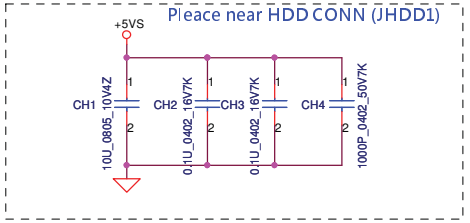
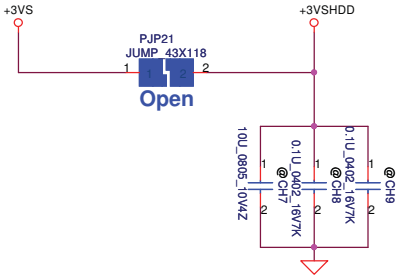
HDD Connector

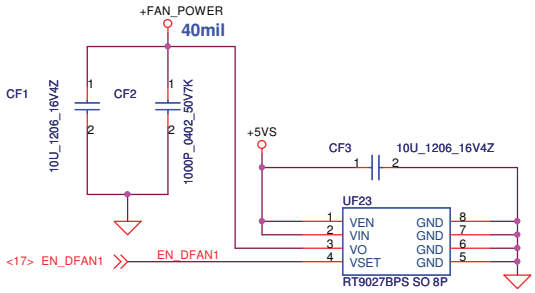


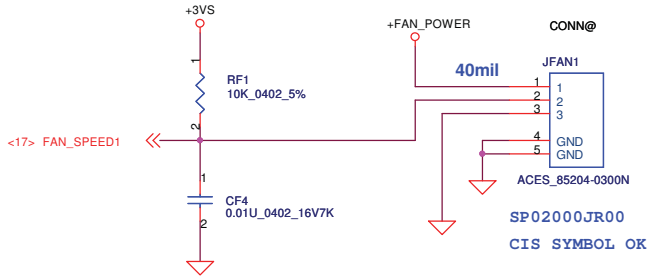
DC010005A00





FAN Control circuit





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Title: FAN/HDD
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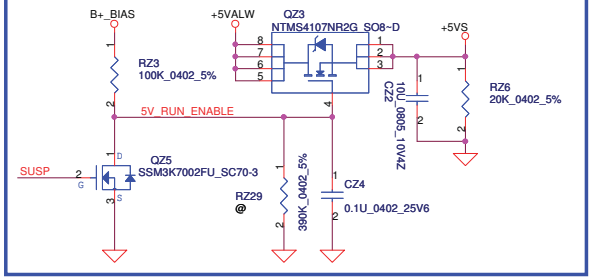
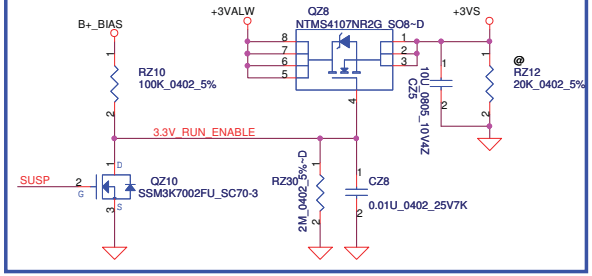
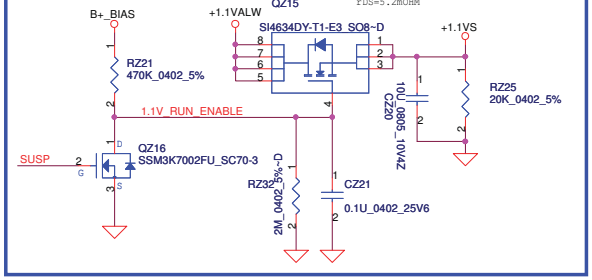
+5VALW to +5VS Transfer



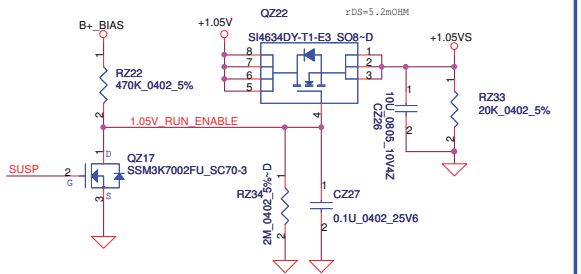
+3VALW to +3VS Transfer



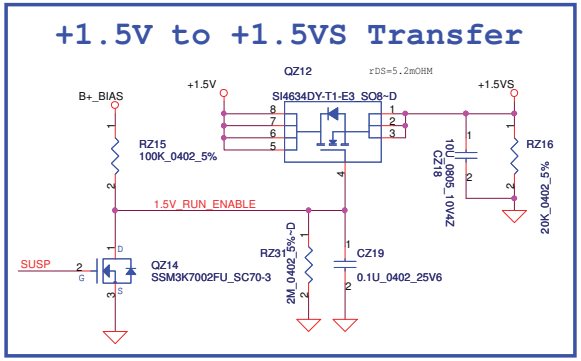
+1.1VALW to +1.1VS Transfer

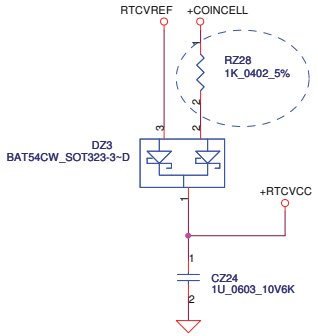


+1.05V to +1.05VS Transfer

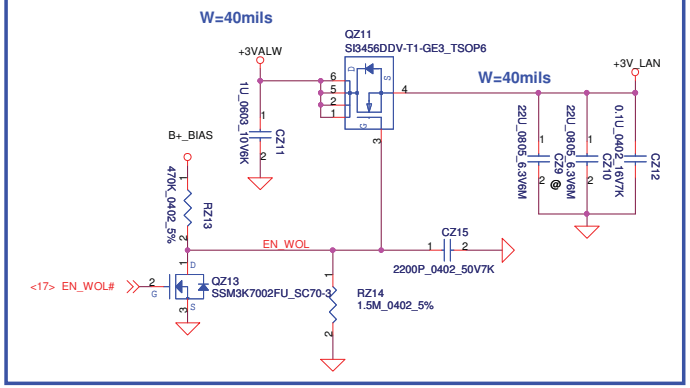


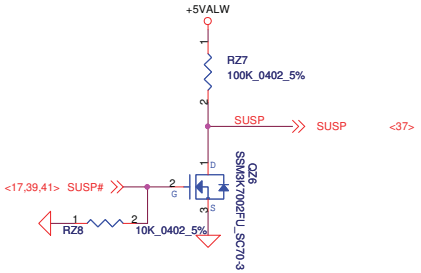
+1.5V to +1.5VS Transfer



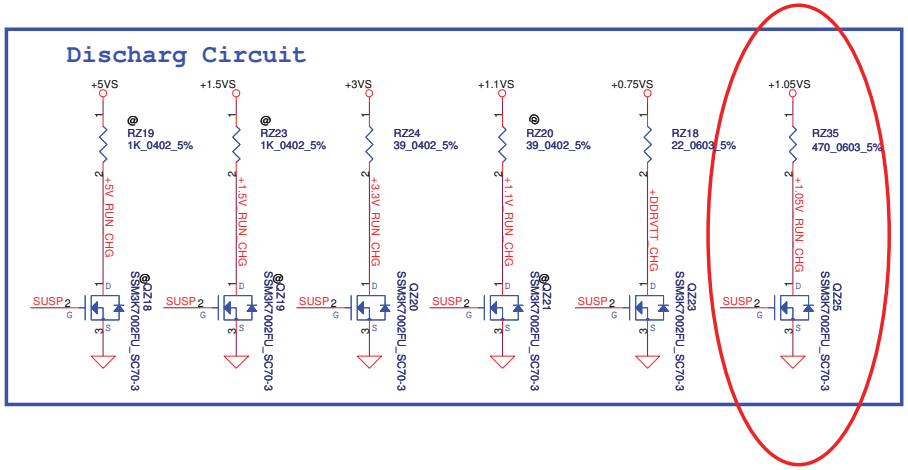


+3VALW to +3V_LAN Transfer





Discharg Circuit



Compal Electronics, Inc.

Title: DC/DC (Power control)

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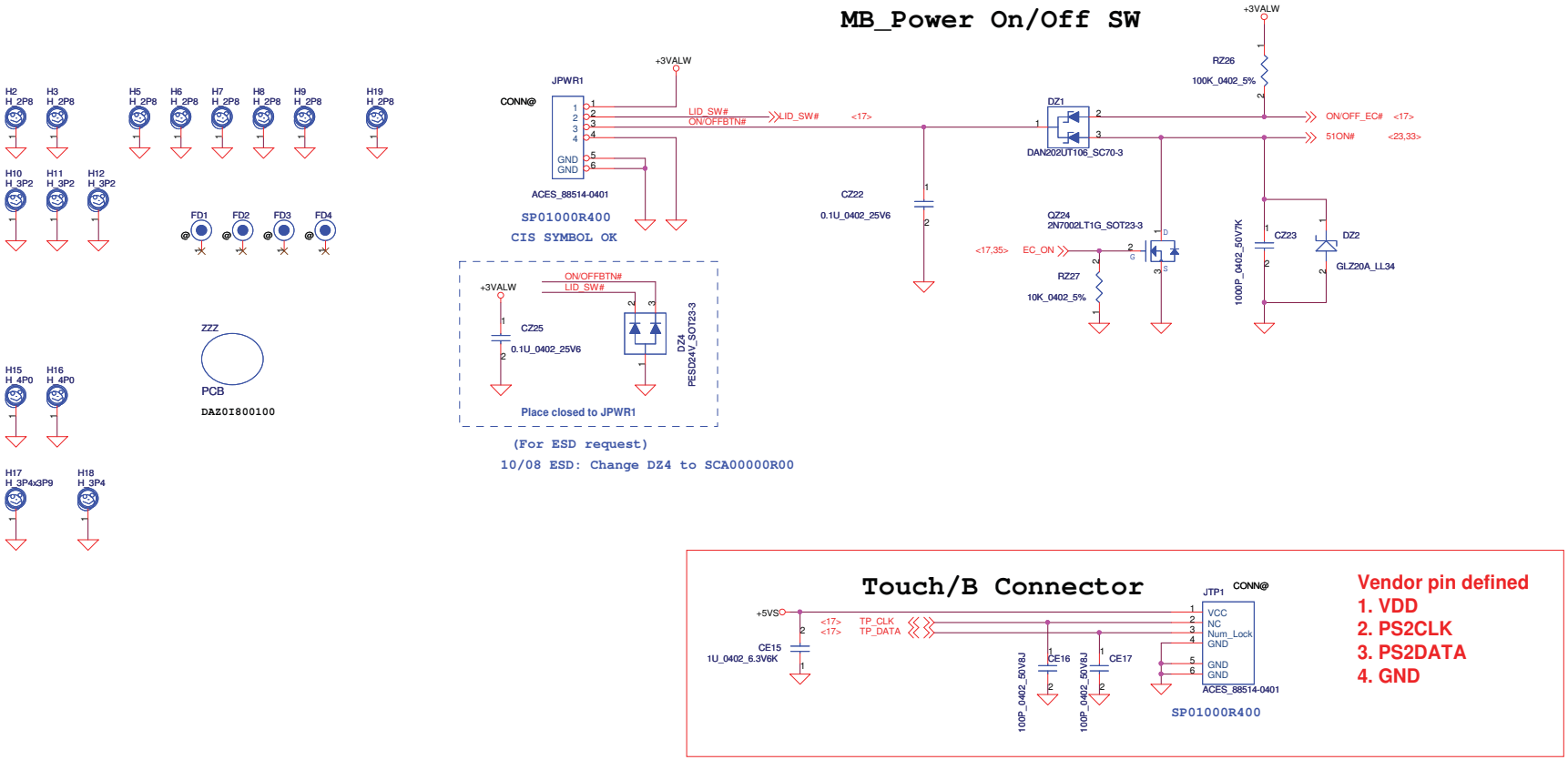

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	SW/TP/PWR/SCREW
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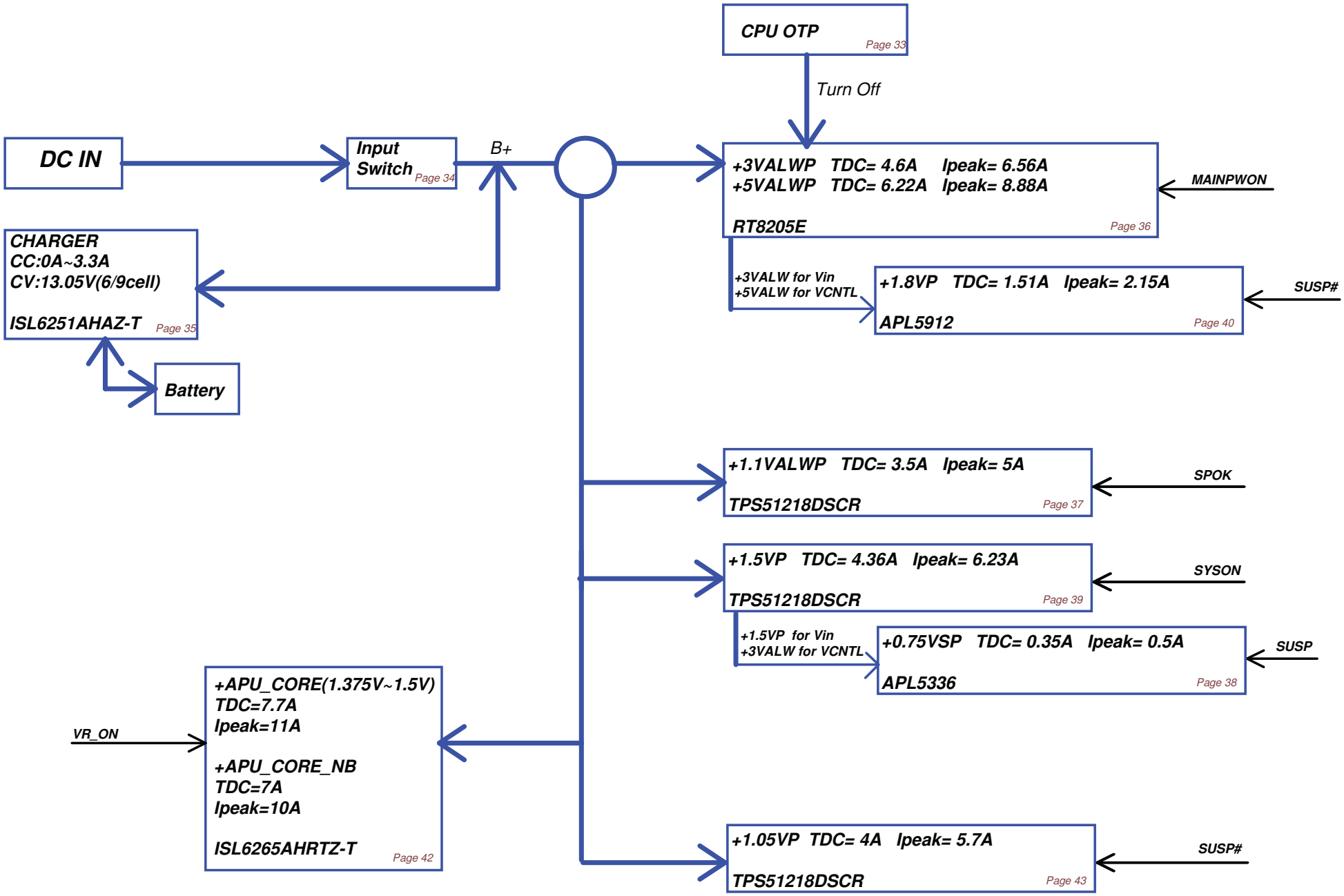
Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	07	LVDS	09/28	EE	LCD Panel display abnormal	Swap LVDS Port	0.2
02	20	LVDS	09/28	EMI	LCD_PWM	Add 220 ohm Bead at LCD_PWM (BLM18BB221SN)	0.2
03	17	Board ID	09/28	EE	Change Board ID to X01	Change RE35 to 8.2K	0.2
04	17	ACIN	09/28	EE	Charge led always light when unplug AC	Change RE32 to150K	0.2
05	29	Power Button ESD	10/08	ESD	Power Button ESD Protection	Change DZ4 to SCA00000R00	0.2
06	19	VGA	10/08	EMI	CRT EMI Noise	Change LV5;LV6;LV7 to SM01000FP00	0.2
07	21	LAN	10/08	EMI	LAN EMI Noise	Change TRL1 to SP050006N00	0.2
08	13;14	FCH	10/11	RF	RF Noise	Add CF20 & CF82 33PF	0.2
09	09	APU PWR	10/14	EE	AMD CRB Rev C update	LU1, LU2, LU4 change to 0_0805	0.2
10	07	LTDP_AUX	11/02	EE	AMD Check list update	RU14,RU15,RU23,RU26 change to 2K ohm pull up to +5VS	0.3
11	07	LTDP0_HPD	11/02	EE	AMD Check list update	Add RU22 100k ohm pull up to +5VS	0.3
12	17	Board ID	11/17	EE	Change Board ID to X02	Change RE35 to 18K	0.3
13	10;11	DDRIII-SODIMM	11/22	EMI	DDR EMI NOISE	POP CD9,CD10,CD11,CD12,CD13,CD14,CD31,CD32,CD33,CD34,CD35,CD36	0.3
14	17	ENE-KB926	11/22	ESD	ESD	Add 0.1uF caps on CE25 & CE29	0.3
15	18	HDMI	11/22	ESD	ESD	Add 0.1uF caps CV36 on +3VS trace of top side layout.	0.3
16	21	LAN	11/22	ESD	ESD	Add 0.1uF caps CL84 on +3V_LAN trace of top side layout.	0.3
17	22	Card Reader	11/23	RF	RF Noise	Mount RB8=10,CB12=22P	0.3
18	12	FCH	11/23	RF	RF Noise	Mount CF80=33P	0.3
19	19	VGA	11/30	EE	AMD Check list update	Change RV31 & RV32 from 4.7K to 2K	0.3
20	17	Board ID	12/10	EE	Change Board ID to A00	Unpop RE35	1.0
21	19	VGA	12/10	Safety	LPS test fail	Delete RV67 . Pop FV2	1.0
22	28	DC/DC	12/16	Safety	Safety RTC battery test fail	Add RZ28 betwwn +COINCELL and DZ3 pin2	1.0
23	20	LVDS	12/23	EE	EC damage	Depop DV6 & RV44 . Pop DV14 & RV51	1.0

Power block



Title	POWER BLOCK DIAGRAM	
Size	Document Number LA7161	Rev
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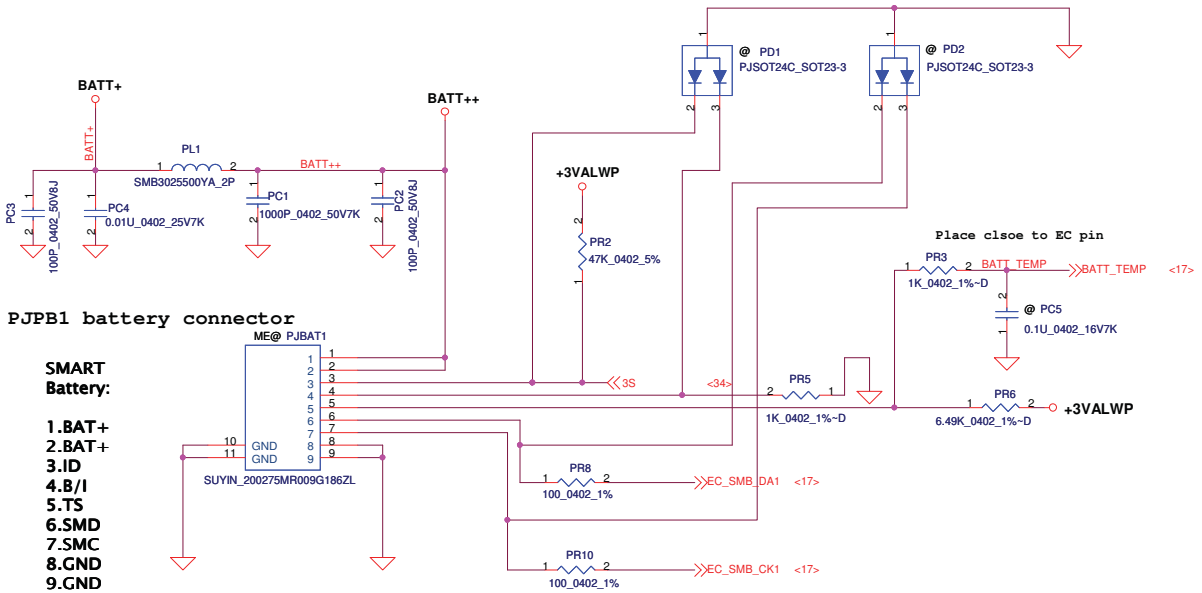
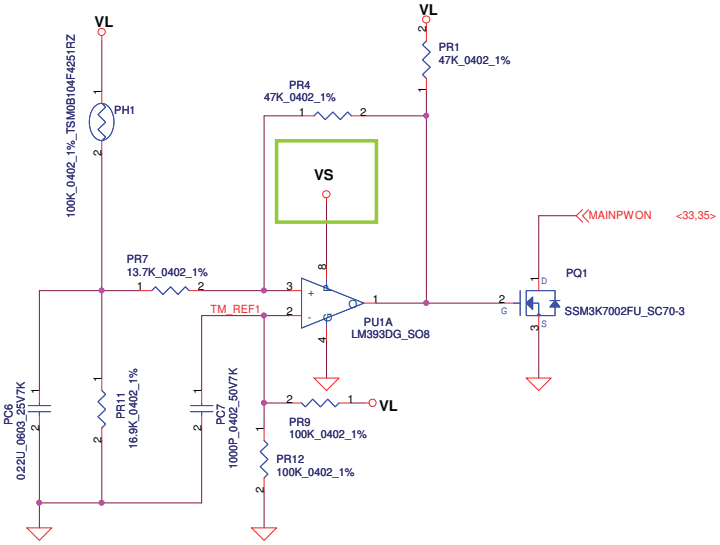
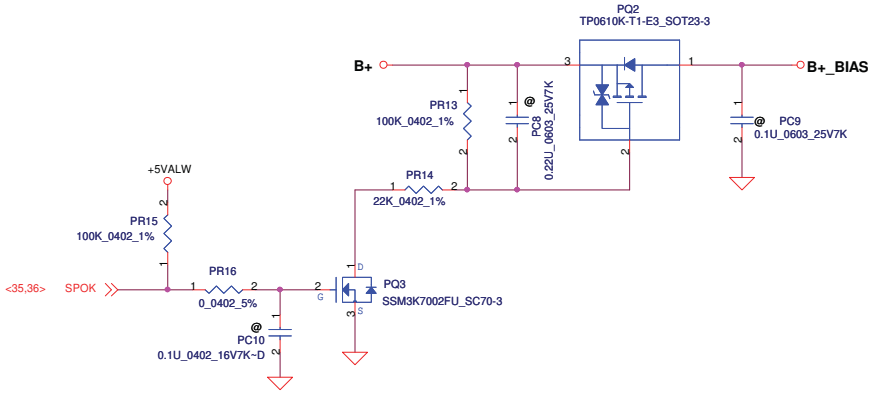


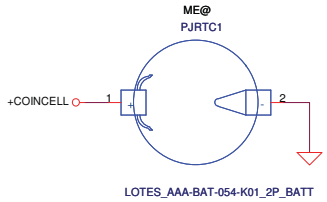
CPU OTP

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C





COIN RTC Battery



Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: BATTERY CONN / OTP / B+_BIAS / RTC

Size	Document Number	Rev
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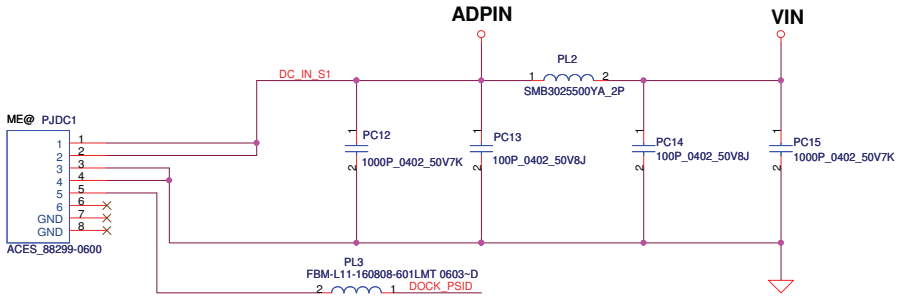
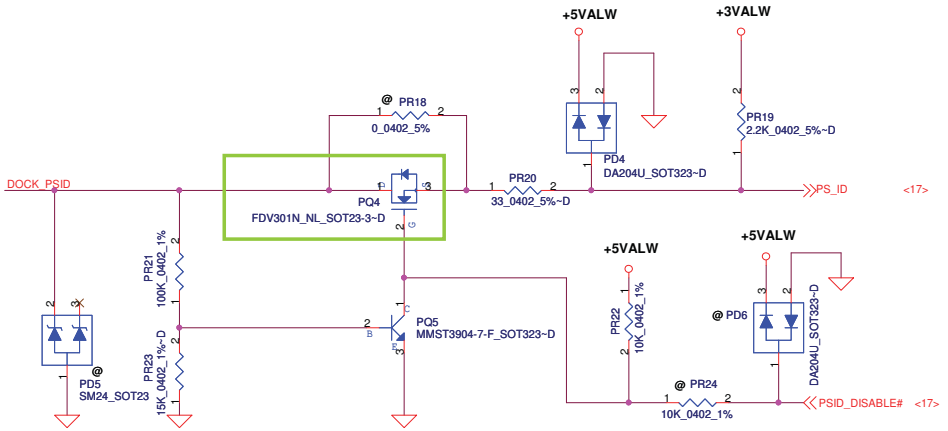
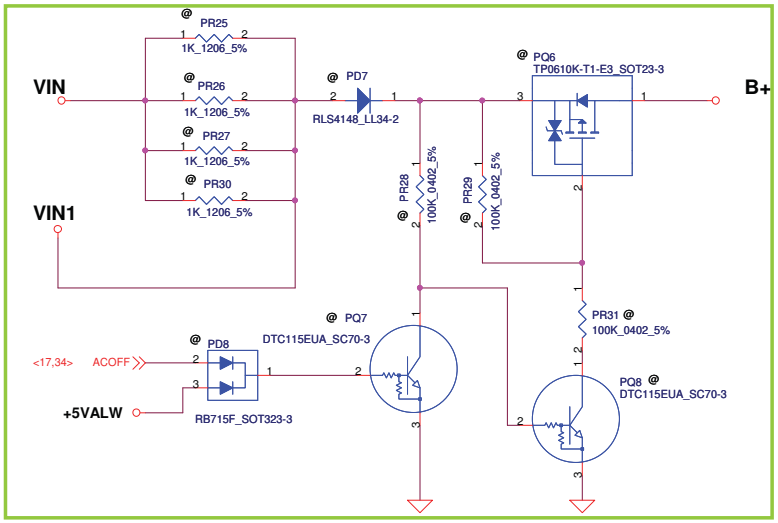




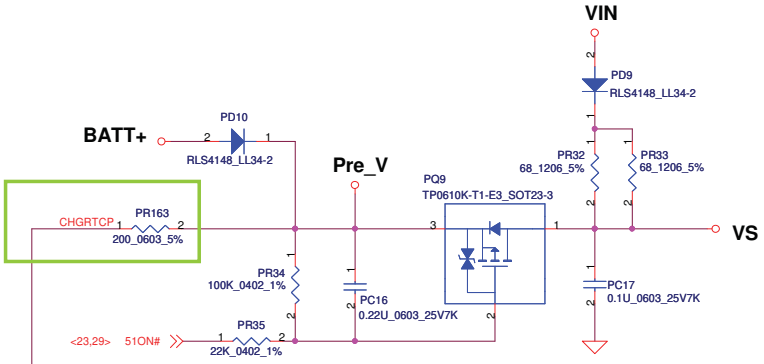


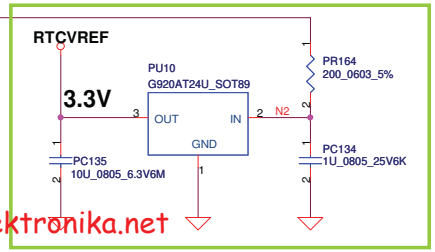
ACIN

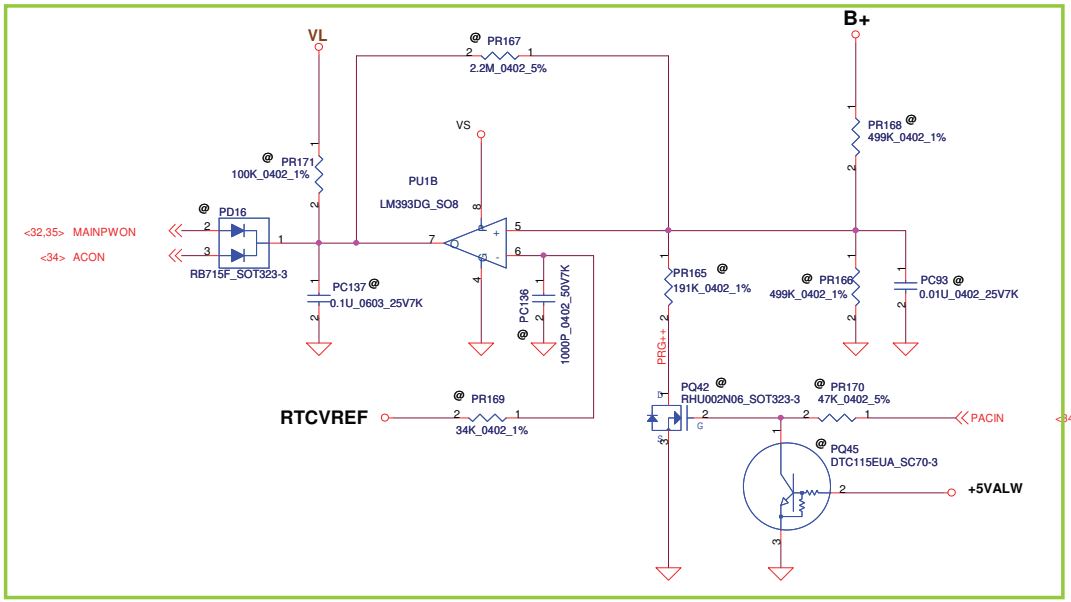
Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V







Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom	LA7161	1.0

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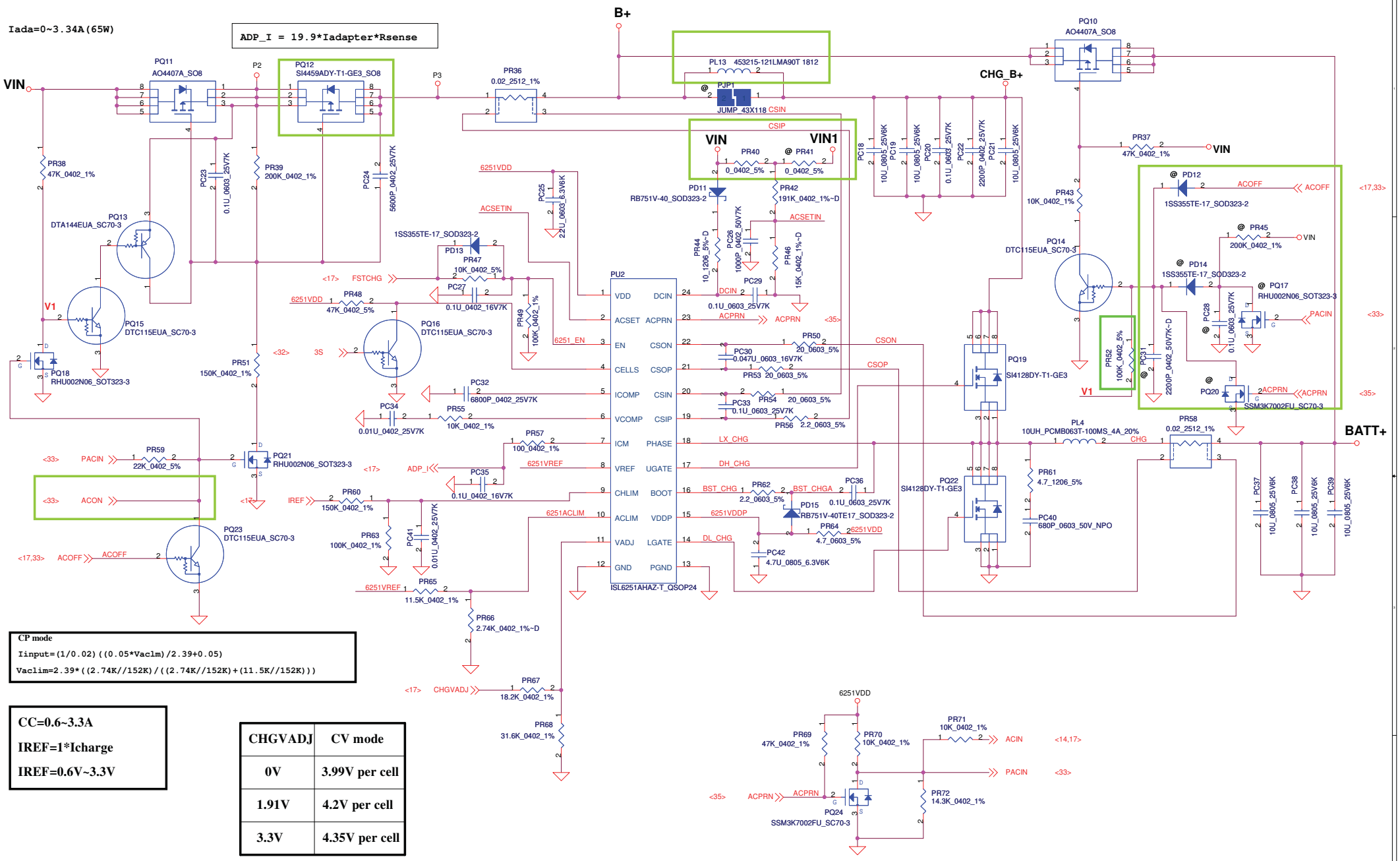

CP mode

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)

Vaclim=2.39*((2.74K//152K)/((2.74K//152K)+(11.5K//152K)))

CC=0.6~3.3A

IREF=1*Icharge

IREF=0.6V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.91V	4.2V per cell
3.3V	4.35V per cell

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: LA7161 | Rev: 1.0

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Note:
Use RT8205E to replace TPS51125 IC can remove RTC refernece LDO
Use RT8205E to replace TPS51427 IC must keep RTC refernece LDO

3.3VALWP
Thermal Design Current=4.6A
Peak Current=6.56A
OCP min=8.53A
H/S RDS(on) 27m ohm(typ),35m ohm(max)
L/S RDS(on) 11.7m ohm(typ),14.2m ohm(max)
FSW 375KHz
Delta_Iin=0.8306A
Delta_Io=2.2154A

5VALWP
Thermal Design Current=6.22A
Peak Current =8.88A
OCP min=11.55A
H/S RDS(on) 27m ohm(typ),35m ohm(max)
L/S RDS(on) 11.7m ohm(typ),14.2m ohm(max)
FSW 300KHz
Delta_Iin=2.4598A
Delta_Io=5.6333A

2VREF_RT8205E
PC43 1U_0603_10V6K~D
+3VALWP
PR73 13K_0402_1%~D
PR74 30K_0402_1%~D
+5VALWP
PR75 20K_0402_1%~D
PR76 20K_0402_1%~D
Typ: 175mA
+3VLP
ENTRIP2
ENTRIP1
PR77 105K_0402_1%
PR78 124K_0402_1%
RT8205E_B+
B+
PJP2 JUMP_43X118
PC44 0.1U_0603_25V7K
PC45 4.7U_0805_25V6K~D
PC46 4.7U_0805_25V6K~D
PC47 2200P_0402_50V7K~D
PC49 4.7U_0805_10V6K~D
PU3
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
ENTRIP2
FB2
TONSEL
REF
FB1
ENTRIP1
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
RT8205EGQW_WQFN24_4X4
VFB=2.0V
PQ25 AO4466_SO8
PQ26 AO4466_SO8
PC50 4.7U_0805_25V6K~D
PC48 4.7U_0805_25V6K~D
PC51 2200P_0402_50V7K~D
PC52 0.1U_0603_25V7K
PC53 4.7U_0805_25V6K~D
PC54 0.1U_0603_25V7K
PR79 0_0603_5%
BST_3V
UG_3V
LX_3V
LG_3V
SPOK
<32,36>
PC55 0.1U_0603_25V7K
PR80 0_0603_5%
BST_5V
UG_5V
LX_5V
LG_5V
PL5 3.3UH_PCMB064T-3R3MS_7A_20%
PL6 2.2UH_PCMC063T-2R2MN_8A_20%
PQ27 AO4710_SO8
PQ28 AO4710_SO8
PR81 4.7_1206_5%
PR82 4.7_1206_5%
PC56 330U_D_6.3VM_R18M~D
PC59 680P_0402_50V7K~D
PC60 680P_0402_50V7K~D
PC57 330U_D_6.3VM_R18M~D
PC58 330U_D_6.3VM_R18M~D
<32,33> MAINPWON
@ PR129 0_0402_5%
@ PR83 499K_0402_1%~D
VL
Typ: 175mA
VS
PR86 499K_0402_1%~D
Pre_V
@ PR87 499K_0402_1%~D
PR84 100K_0402_1%
PC61 1U_0603_10V6K~D
@ PR85 0_0402_5%
PC62 22U_0805_6.3V6M
PC63 0.1U_0603_25V7K
2VREF_RT8205E
PQ29B DMN66D0LDW-7 2N SOT363-6
PQ29A DMN66D0LDW-7 2N SOT363-6
PR88 100K_0402_1%
PR89 0_0402_5%
PR90 100K_0402_1%
PQ30 DTC115EUA_SC70-3
PR91 40.2K_0402_1%~D
PC64 2.2U_0603_16V6K~D
PQ31 RHU002N06_SOT323-3
<34> ACPRN
PR92 100K_0402_1%
<17,29> EC_ON
PQ32 DTC115EUA_SC70-3
PJP3 JUMP_43X118
PJP4 JUMP_43X118
+5VALW
PJP5 JUMP_43X118
PJP6 JUMP_43X118

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
Custom	LA7161	1.0

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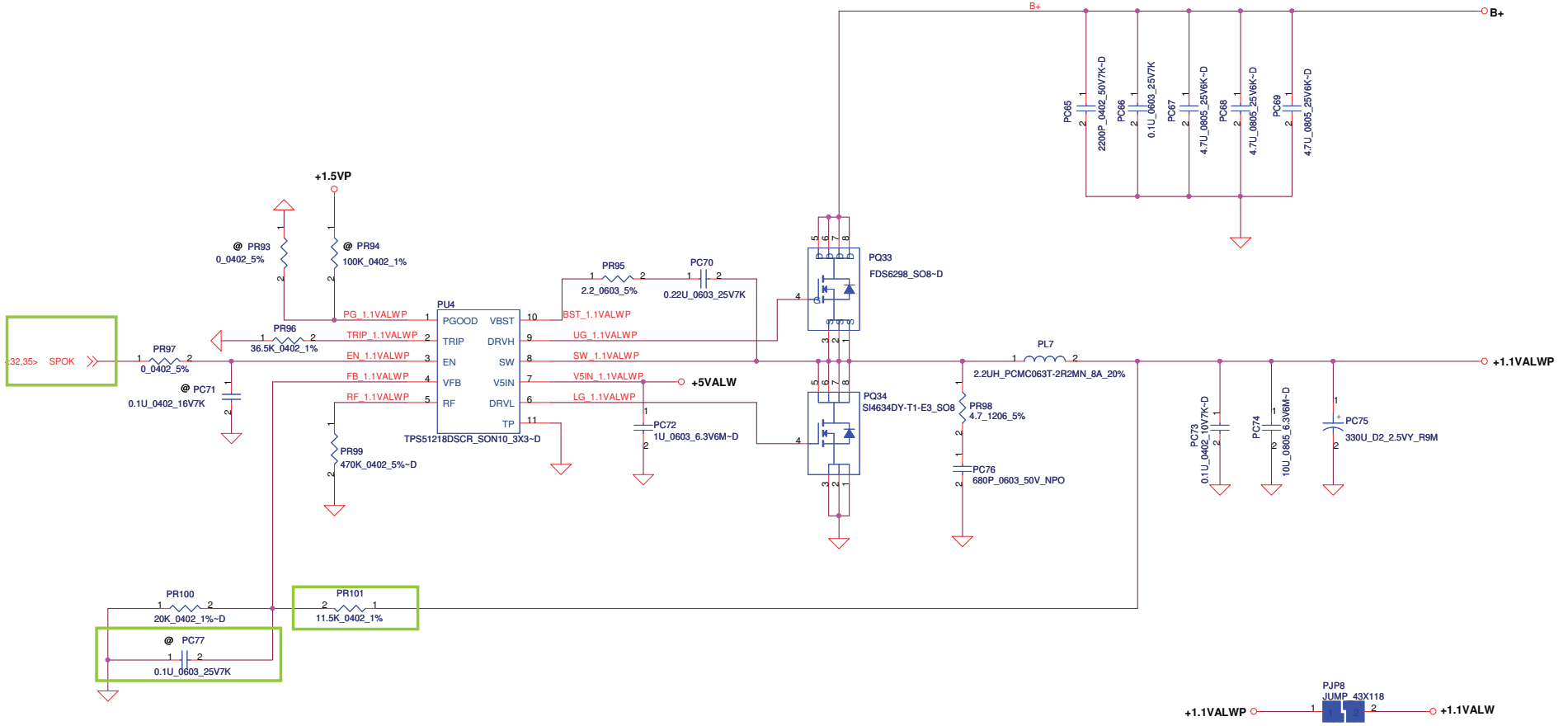


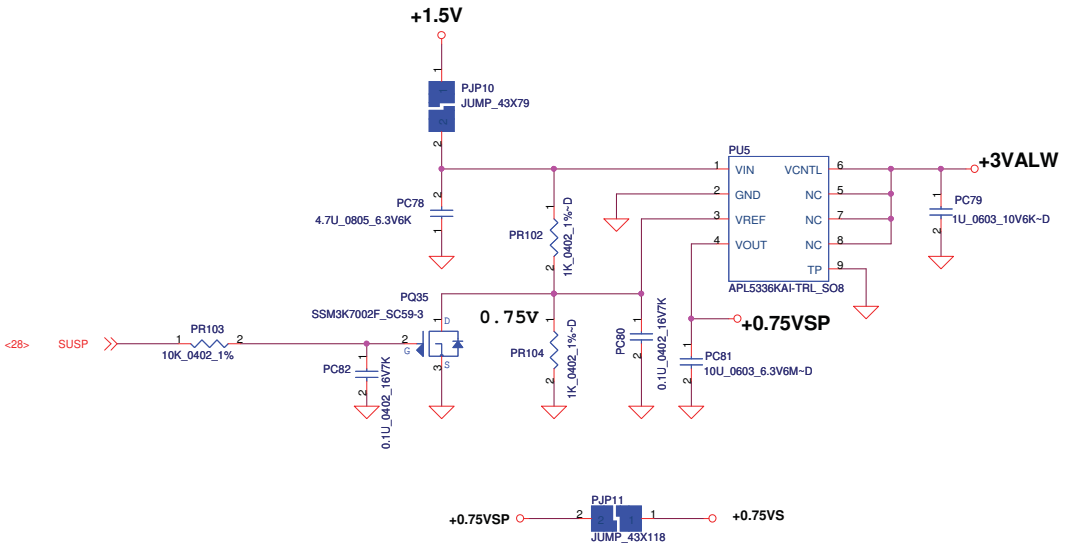
+1.1VALWP
Thermal Design Current=3.5A
Peak Current=5A
OCP min=6.5A
Fsw=290KHZ

Delta I=1.6269A
L/S MOS Rds(on)=5.5m ohm (Typ) ; 6.7m ohm(Max)

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title	+1.1VALWP	
Size: Custom	Document Number: LA7161	Rev: 1.0
Date: Wednesday, January 05, 2011	Sheet 36 of 43	



+0.75VSP
Thermal Design Current=0.35A
Peak Currnet=0.5A
OCP min=0.65A

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title	+0.75VSP	
Size: Custom	Document Number: LA7161	Rev: 1.0
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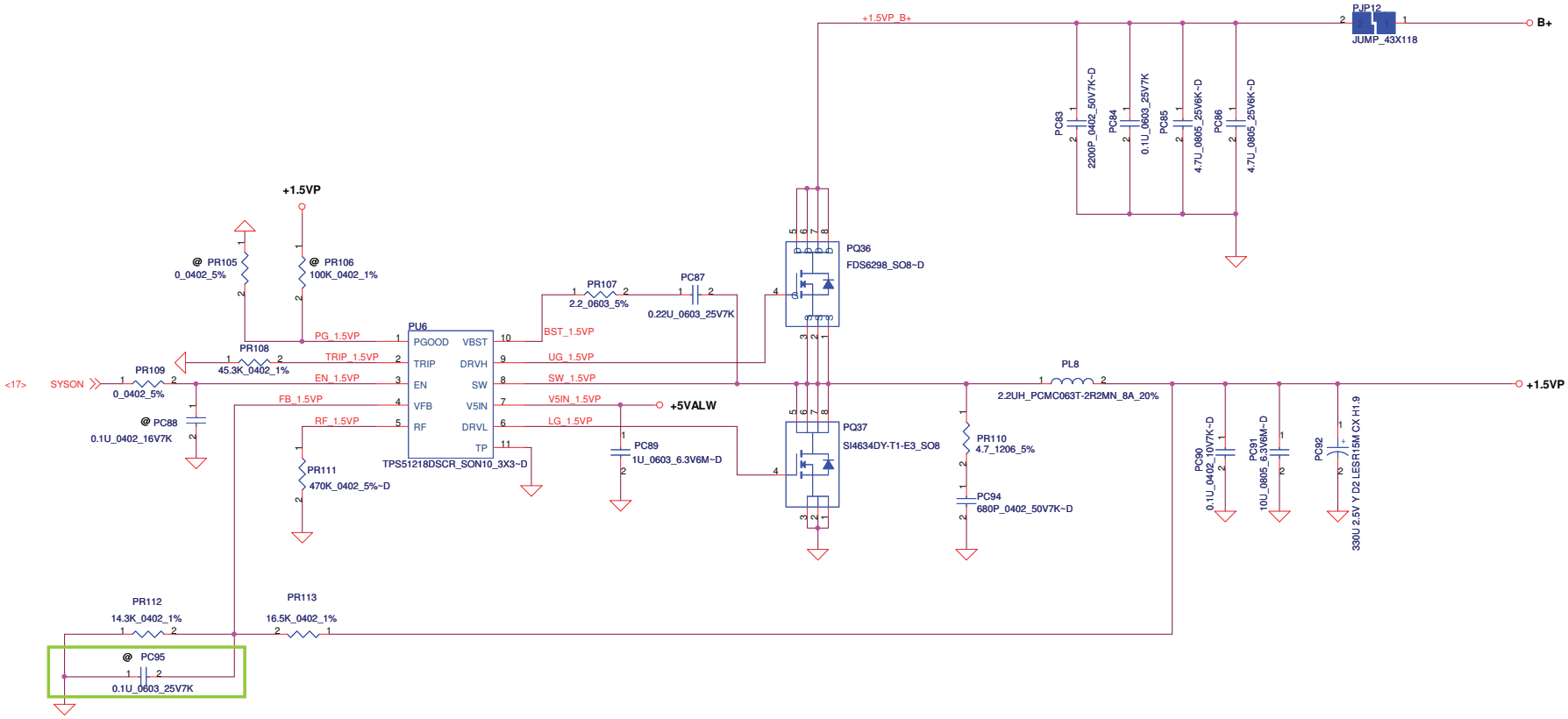

+1.5VP
Thermal Design Current=4.36A
Peak Current=6.23A
OCP min=8.1A
Fsw=290KHZ

Delta I=2.1702A
L/S MOS Rds(on)=5.5m (Typ) ; 6.7m (Max)

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics, Inc.

Title: +1.5VP

Size: Custom | Document Number: LA7161 | Rev:

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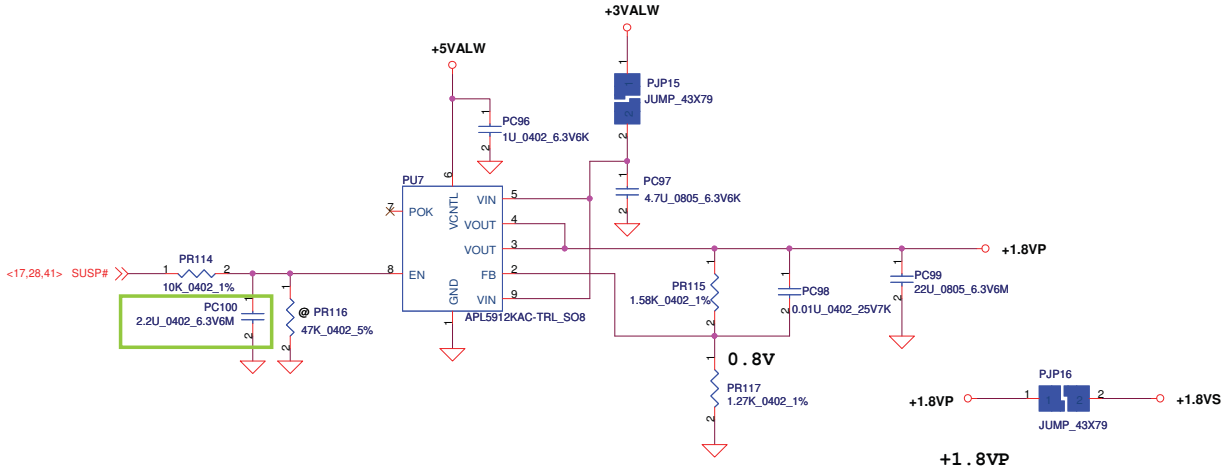

+1.8VP
Thermal Design Current=1.51A
Peak Currnet=2.15A
OCP min=2.8A

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title	+1.8VP	
Size: Custom	Document Number: LA7161	Rev: 1.0
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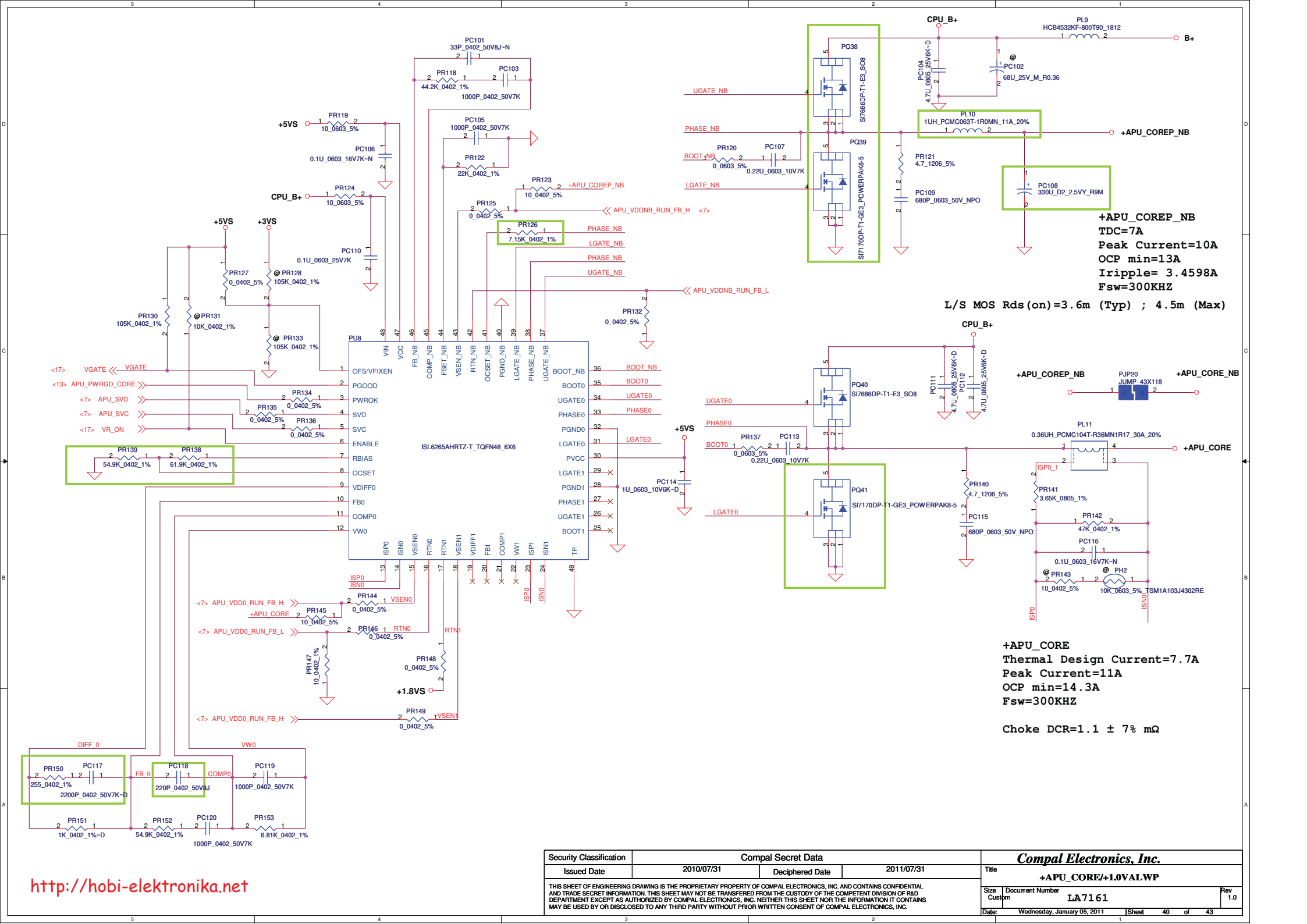
+APU_COREP_NB
TDC=7A
Peak Current=10A
OCP min=13A
Iripple= 3.4598A
Fsw=300KHZ
L/S MOS Rds(on)=3.6m (Typ) ; 4.5m (Max)
+APU_CORE
Thermal Design Current=7.7A
Peak Current=11A
OCP min=14.3A
Fsw=300KHZ
Choke DCR=1.1 ± 7% mΩ
ISL6265AHRTZ-T_TQFN48_6X6
http://hobi-elektronika.net
Compal Electronics, Inc.
+APU_CORE/+1.0VALWP
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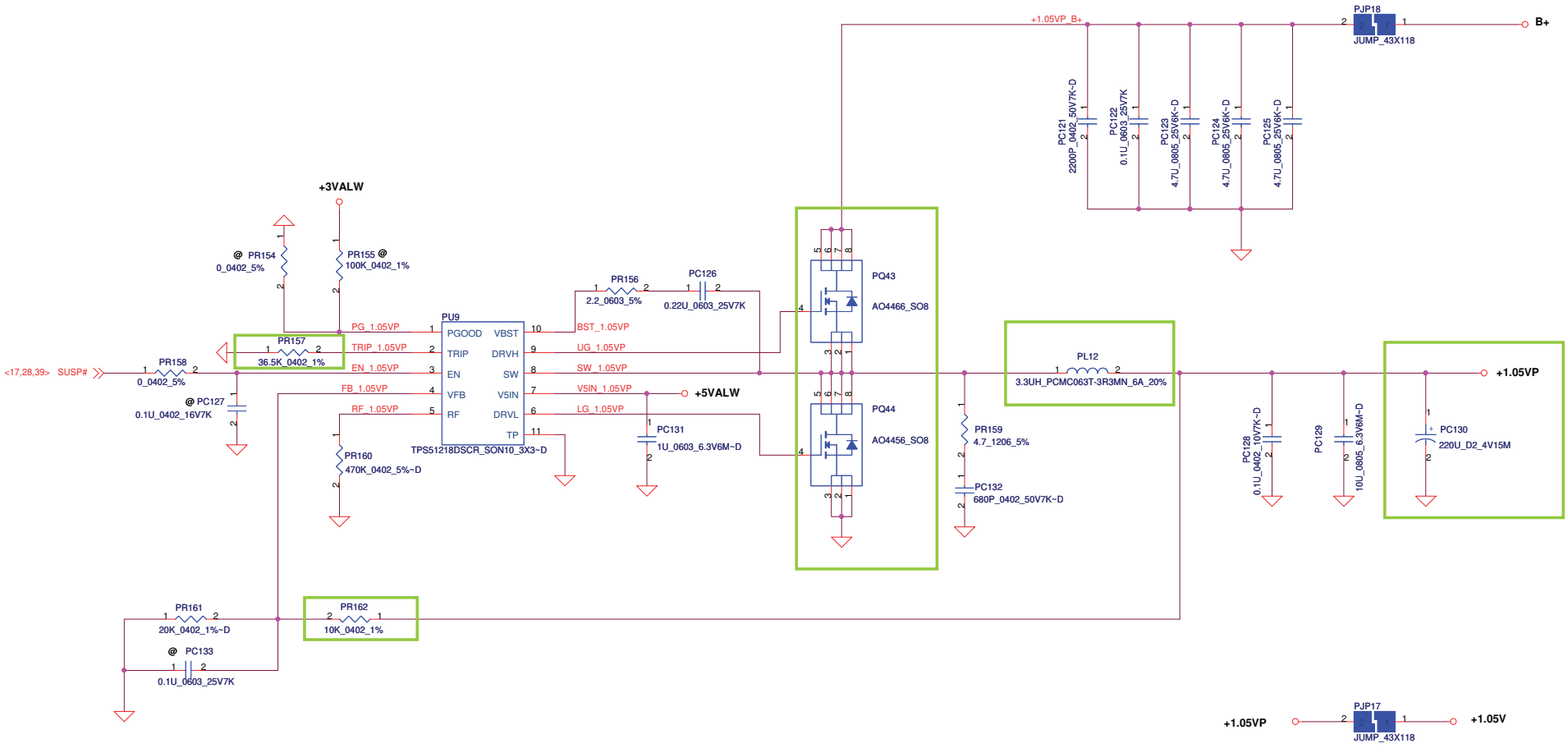

+1.05VP
Thermal Design Current=4A
Peak Current=5.7A
OCP min=7.41A
Fsw=290KHZ

Delta I=1.0381A
L/S MOS Rds(on)=4.5m (Typ) ; 5.6m (Max)

Security Classification	Compal Secret Data		
Issued Date	2010/07/31	Deciphered Date	2011/07/31

Compal Electronics, Inc.

Title	+1.05VP	
Size: Custom	Document Number: LA7161	Rev: 1.0
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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	+APU_CORE/ +APU_COREP_NB	2010/10/04	Compal	PC102(H=5.8mm) will impact ME logic lower	Depop PC102 (P/N : SF000000W00)	X01
2	33 32	DCIN BATTERY CONN /OTP/B+_BIAS	2010/10/12	Compal	HW power share no function when system at S5 ony with battery without AC.	1. Add PR163, PR164 (P/N : SD013200080) (S RES 1/10W 200 +-5% 0603); PU10 (P/N : SA009200010) (S IC G920AT24U SOT89 REG 3.3V); PC134 (P/N : SE000001380) (S CER CAP 1U 25V K X5R 0805 H1.25); PC135 (P/N : SE093106M80) (S CER CAP 10U 6.3V M X5R 0805 H1.25) 2. Modify PD3.pin3 net name, change from +3VLP to RTCVREF 3. Delete PD3, PR17, PC11 =>Cause HW side has alike RTC circuitry (DZ3 and CZ24)	X01
3	32	BATTERY CONN /OTP/B+_BIAS	2010/10/18	Compal	For reduce S5,S4 power leakage when system only with battery	Change PU1A.pin8 net-name from Pre_V to VS	X01
4	32	BATTERY CONN /OTP/B+_BIAS	2010/10/18	Compal	for ME team change RTC battery connector.	Change PJRTC1 P/N from SP02000IA00(with Cable) to SP07000H700(w/o cable)	X01
5	34	CHARGER /DETECTOR	2010/10/18	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	1. Depop PR52 (P/N : SD02810030L), PQ20 (P/N : SB000009610) 2. Pop item: PD12 (P/N: SC1SS355010)S DIO 1SS355TE-17 SOD323 PD14 (P/N: SC1SS355010)S DIO 1SS355TE-17 SOD323 PR45 (P/N: SD034200380)S RES 1/16W 200K +-1% 0402 PC28 (P/N: SE042104K80)S CER CAP .1U 25V K X7R 0603 PQ17 (P/N: SB502060000)S TR RHU002N06 1N SOT323	X01
6	34	CHARGER /DETECTOR	2010/10/22	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	1. Pop PQ20 (P/N: SB000009610) (S TR SSM3K7002FU 1N SC70-3))	X02
7	35	+3VALWP /+5VALWP	2010/11/24	Compal	QAD team highlight BITS issue DF434417: [Rel, PT] OTP (PH1) recovery temperature can't meet spec. The recovery temperature spec is 50 +/- 3degree C.	Add @PR129 (P/N: SD028000080) (S RES 1/16W 0 +-5% 0402)	X03
8	33 34	DCIN CHARGER /DETECTOR	2010/11/24	Compal	follow compal power team new AC-IN, Pre-charge circuits with 連動circuits, need change design to original pre-charge design and ADP/BAT switch circuits.	1. Depop : PD7, PD8, PQ6, PQ7, PQ8, PR25, PR26, PR27, PR28, PR29, PR30, PR31 2. Add @PC93, @PC136, @PC137, @PD16, @PQ42, @PQ45, @PR165, @PR166, @PR167 , @PR168, @PR169, @PR170, @PR171 3. Depop PR41, pop PR40 (P/N: SD028000080) (S RES 1/16W 0 +-5% 0402) 4. Pop PR52 (P/N: SD028100380) (S RES 1/16W 100K +-5% 0402) , depop PC28, PC31, PD12, PD14, PQ17, PQ20, PR45 5. Change PQ21.2 net name to "ACON"	X03

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
9	P35 P36 P38 P40 P41	3VALWP/5VALWP +1.1VALWP +1.5VP +APU_CORE /+APU_COREP_NB +1.05VP	2010/11/24	Compal	for support DFX team and SMT AOI detect: 較容易檢測出是否空焊現象	follow DFX team-Chen. Daniel suggestion: to use the pad length 3.6*2.5mm PCB footprint for the PL6, PL7, PL8, PL10, PL12 material as PL5 . Change PL6 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL7 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL8 footprint from (CYNTE_PCMC063T-2R2MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL10 footprint from (CYNTE_PCMC063T-1R0MN_2P) to (CYNTE_PCMB064T-3R3MS_2P) PL12 footprint from (CYNTE_PCMC063T-3R3MN_2P) to (CYNTE_PCMB064T-3R3MS_2P)	X03
10	34	CHARGER /DETECTOR	2010/11/26	Compal	Support EMC team to reduce nosie	Add @PL13 and lyaout footprint co-layout with PJP1	X03
11	34	CHARGER /DETECTOR	2010/12/14	Compal	Support EMC team to reduce nosie	1. Pop PL13 (P/N: SM01000DJ00) (S SUPPRE_ FBMA-L11-453215-121LMA90T 1812) this bead value= 120 ohm(Current rating=9A) 2. Depop PJP1	A00