PCB STACK UP

8L DIS

V03A DIS/UMA BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

DDRIII-SODIMM1 A 00 PAGE 16 — DDRIII 1333 MT/s
DDRIII-SODIMM2 A 01 PAGE 17 — DDRIII 1333 MT/s

CPU
Sandy Bridge 45W
PGA 989
PAGE 4~8

PCIEx16

Nvidia
N12P-GE (128bit)
29mm X 29mm
BGA 969
PAGE 18~22

DDR3 1GB/2GB
128Mx16bitx8
PG 23,24

HDMI Switch PAGE 26
HDMI CONN PAGE 26

FDI LINK 2.5GT /s
DMI LINK 2.5GT /s

INT HDMI

Re-Driver SN75LVCP412RTJR PAGE 27
E-SATA PAGE 27 — SATA4 300MB /S

SATA -HDD PAGE 28 — SATA0 300MB /S

ODD PAGE 28 — SATA1 300MB /S

3-axis Fall Sensor PAGE 28 — SMBUS

Mobile Intel
Series 6 Chipset
PCH
HM67
Couger Point
BGA 989
25 mm X 25 mm
PAGE 9~15

iGFX Interfaces

INT Dual CHANNEL LVDS

LCD CONN
1600 x 900 (HD) PAGE 25

ESATA+USB2.0 PAGE 27 — USB[0]
Camera PAGE 25 — USB[11]
Card Reader RTS5128-GR PAGE 29 — USB[8]
FP PAGE 35 — USB[10]
Touch Screen PAGE 34 — USB[12]
USB2.0

USB[8]
Express Card
R5538D001 PAGE 02

CRT Board PAGE 03 — IO Board

USB[4] WLAN PAGE 05
USB[5] WiMAX PAGE 04
PCIE[3] USB3.0 Controller PAGE 06
PCIE[1]
PCIE[2] BlueTooth PAGE 05
USB3.0 Ports x2 PAGE 07
PCIE[5] LAN Realtek RTL8111E-VB-GR PAGE 09
USB[6]
USB Port x1 PAGE 08
USB[2]
RJ45 PAGE 10
25MHz

EXP Board
LED Board
PB Board
TP Board
HotKey Board

32.768KHz
Keyboard Conn. PAGE 35
Touch Pad PAGE 35
LED PAGE 36
KBC
ITE 8518
PAGE 30
LPC
PWM FAN &Thermal PAGE 38
SPI ROM 512kB PAGE 34

SPI
SPI ROM 4MB PAGE 34
25MHz
32.768KHz

IHDA
Audio Codec
ALC 269Q-VB6-GR
PAGE 32
Subwoofer MAX9759ETE PAGE 33
Speaker PAGE 32
Jack X2 PAGE 32
Digital-MIC PAGE 32

Charger PAGE 42
3/5V PAGE 43
1.5V_SUS/0.75V_DDR PAGE 44
Batt/DC-IN PAGE 41
1.05V_PCH PAGE 45
VCCSA PAGE 46
DGFX_CORE PAGE 48
CPU_CORE PAGE 47
1.8V_RUN PAGE 45

Quanta Computer Inc.
PROJECT : R03A/V03A

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

Date: Friday, December 31, 2010 Sheet 1 of 50

power / State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+VCHGR +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+5V_SUS +3.3V_SUS +1.5V_SUS +1.5V_CPU +DDR_VTTREF +3.3V_LAN (for R03)	+VCC_CORE +VCC_GFX_CORE +1.05V_PCH +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +VCCSA +0.75V_DDR_VTT +LCDVCC +VCC_DGFX_CORE	
S0	ON	ON	ON	ON	ON	
S1						
S3	ON	ON	ON	ON	OFF	
S4/S5 AC	ON	ON				
S4/S5 DC Only	ON		ON	OFF	OFF	
AC/DC No Exist	ON	OFF	OFF	OFF	OFF	

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	Power Rails	2A

Date: Wednesday, October 27, 2010 Sheet 2 of 50

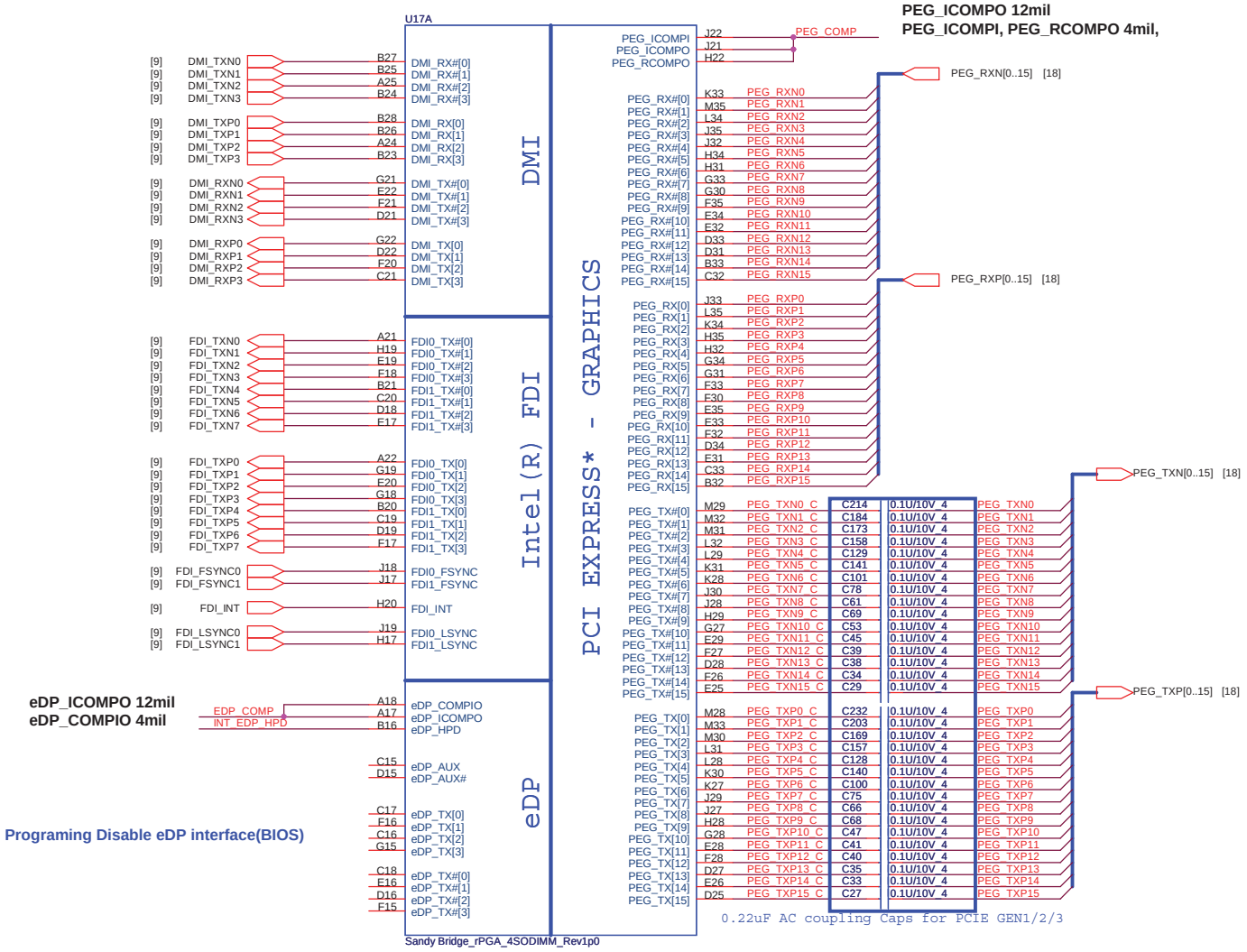
Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	BLANK	2A

Date: Wednesday, October 06, 2010 Sheet 3 of 50

Sandy Bridge Processor (DMI,PEG,FDI)

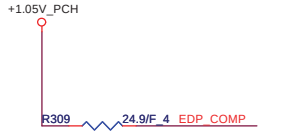


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

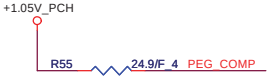
eDP_ICOMPO 12mil
eDP_COMPIO 4mil

Programing Disable eDP interface(BIOS)

DP & PEG Compensation



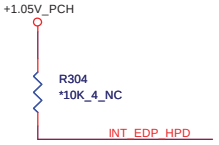
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

Quanta Computer Inc.			
PROJECT : R03A/V03A			
Size	Document Number		Rev
	Sandy Bridge 1/5		2A
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Sandy Bridge Processor (CLK,MISC,JTAG)

U17B

MISC
TP43 C26 PROC_SELECT#
+1.05V_PCH R186 62/F_4 H_PROCHOT#
[30] H_CPUDET# AN34 SKTOCC#

THERMAL
TP34 TP_CATERR# AL33 CATERR#
[30] PECI_EC R445 43/J_4 H_PECI_R AN33 PECI
[30,42,47] H_PROCHOT# R181 56/J_4 H_PROCHOT#_R AL32 PROCHOT#
Over 130 degree C will drive low
[14] PM_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
[9] H_PM_SYNC AM34 PM_SYNC
[14] H_PWRGOOD AP33 UNCOREPWRGOOD
R189 10K/J_4
SM_DRAMPWROK V8 SM_DRAMPWROK
+1.05V_PCH R192 *75/J_4_NC CPU_PLTRST# R193 *43/J_4_NC CPU_PLTRST#_R AR33 RESET#

CLOCKS
BCLK A28 CLK_CPU_BCLKP [13]
BCLK# A27 CLK_CPU_BCLKN [13]
DPLL_REF_CLK A16 CLK_DP_P_R
DPLL_REF_CLK# A15 CLK_DP_N_R
R310 1K_4
R305 *0_4_NC
R306 *0_4_NC
R311 1K_4
+1.05V_PCH
CLK_DP_P [13]
CLK_DP_N [13]

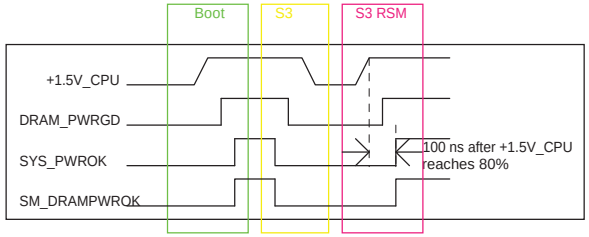
DDR3 MISC
SM_DRAMRST# R8 CPU_DRAMRST#
SM_RCOMP[0] AK1 SM_RCOMP_0 R153 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R312 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R313 200/F_4
SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

JTAG & BPM
PRDY# AP29
PREQ# AP27
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST# R447 51/J_4
TDI AR28 XDP_TDI
TDO AP26 XDP_TDO
DBR# AL35 XDP_DBRST# R443 1K_4
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT30
BPM#[4] AP32
BPM#[5] AR31
BPM#[6] AT31
BPM#[7] AR32
+1.05V_PCH
XDP_TMS R452 51/J_4
XDP_TDI R450 51/J_4
XDP_TDO R201 51/J_4
XDP_TCLK R202 51/J_4
+3.3V_RUN
XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

Sandy Bridge_rPGA_4SODIMM_Rev1p0

IN	OUT
L	L
H	High-Z

+3.3V_SUS
C333 *0.1U/10V/X7R_4_NC
U8
NC VCC 5
IN 2
GND OUT 4
3
*74LVC1G07GW_NC
[12,18,30,31] PLTRST#
CPU_PLTRST#
R556 1.5K 1%
CPU_PLTRST#_R voltage level Ckt.
CPU_PLTRST# R
1%
750
R557



Change OD part same with PDC

Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

+3.3V_SUS
R183 200_4
C301 0.1U/10V/X7R_4
U6
[9] PM_DRAM_PWRGD
[9] SYS_PWROK
74AHC1G09GW
+1.5V_CPU
R170 200/F_4
SM_DRAMPWROK_R
R176 130/F_4 SM_DRAMPWROK
R184 *39_NC
Q14 *2N7002K_NC
PS_S3CNTRL [7,16]

Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration

+1.5V_SUS
R72 1K/F_4
R54 *0_4_NC
Q5 BSS138-7-F
R63 1K/F_4
[16,17] DDR3_DRAMRST#
DDR3_DRAMRST#_R
CPU_DRAMRST#
[13] DDR_HVREF_RST_PCH
C86 0.047U/10V_4
R56 4.99K/F_4

Schematic C/L_v1.0, P56 (PU,PD 1k/J) (Intel and PD3)
Reserve (Intel confirm now)

Quanta Computer Inc.
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	Sandy Bridge 2/5	2A
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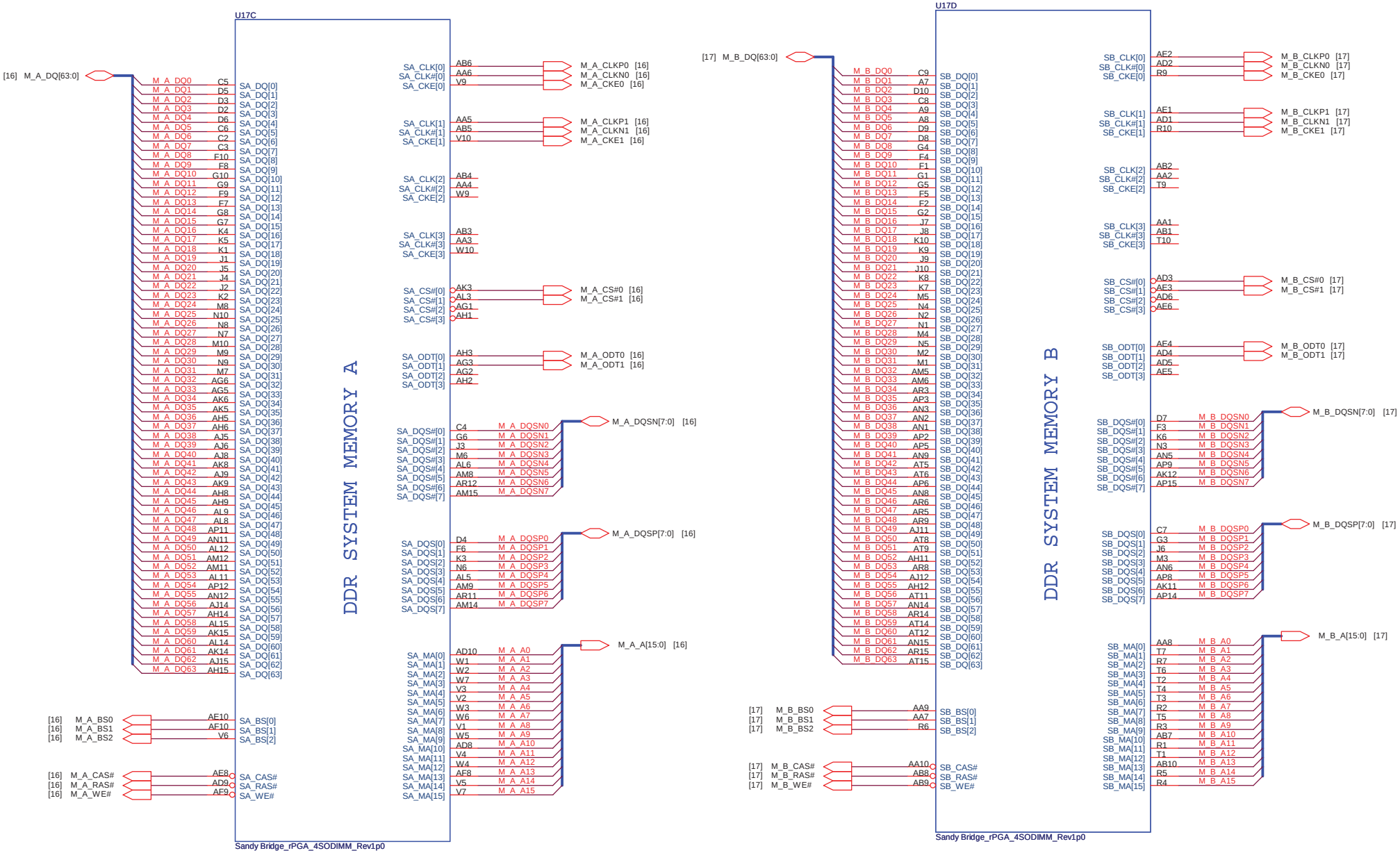
Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : R03A/V03A

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	Sandy Bridge 3/5	2A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:95A
470uF/4mohm x 4
22uF x 16
10uF x 10

CPU VTT
SNB 45W:8.5A
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
1.8V RAIL
DDR3 -1.5V RAILS
SA RAIL
VREF
MISC

22uF (Reserved)

ripple question, check with power, 47uF?

power side low itself

1231 Del C81 for ST interanl notice

S3 Power reduce

Take care Q3509 Vgs(MAX)=2.5

Change R8281,R8285, R8704,R8329 to +/-5%
54.9 ohm has no 5%

Layout note: need routing together and ALERT need between CLK and DATA

Place PU resistor close to CPU

Place PU resistor close to CPU

SVID ALERT

Sandy Bridge_rPGA_4SODIMM_Rev1p0

Quanta Computer Inc.
PROJECT : R03A/V03A
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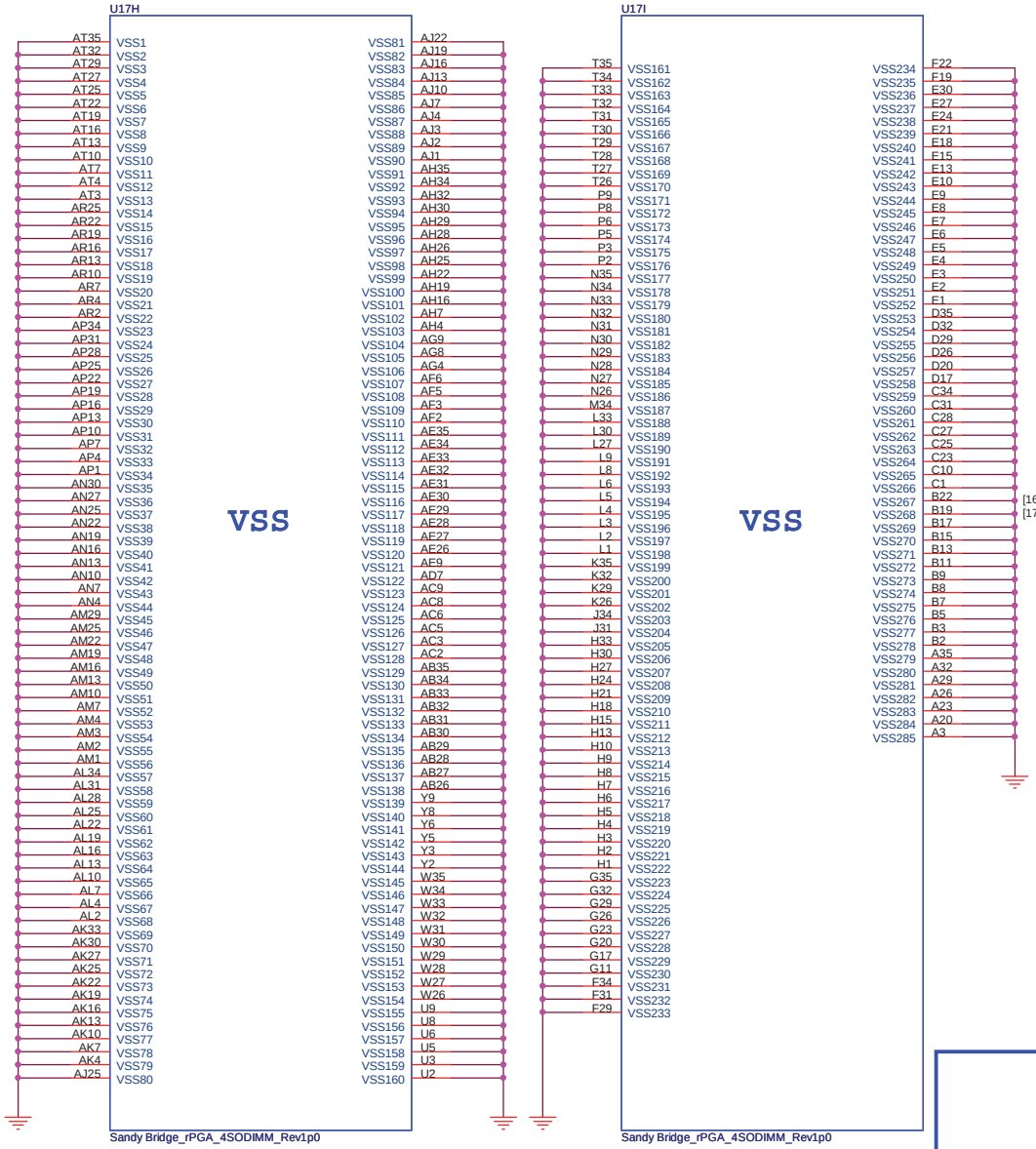
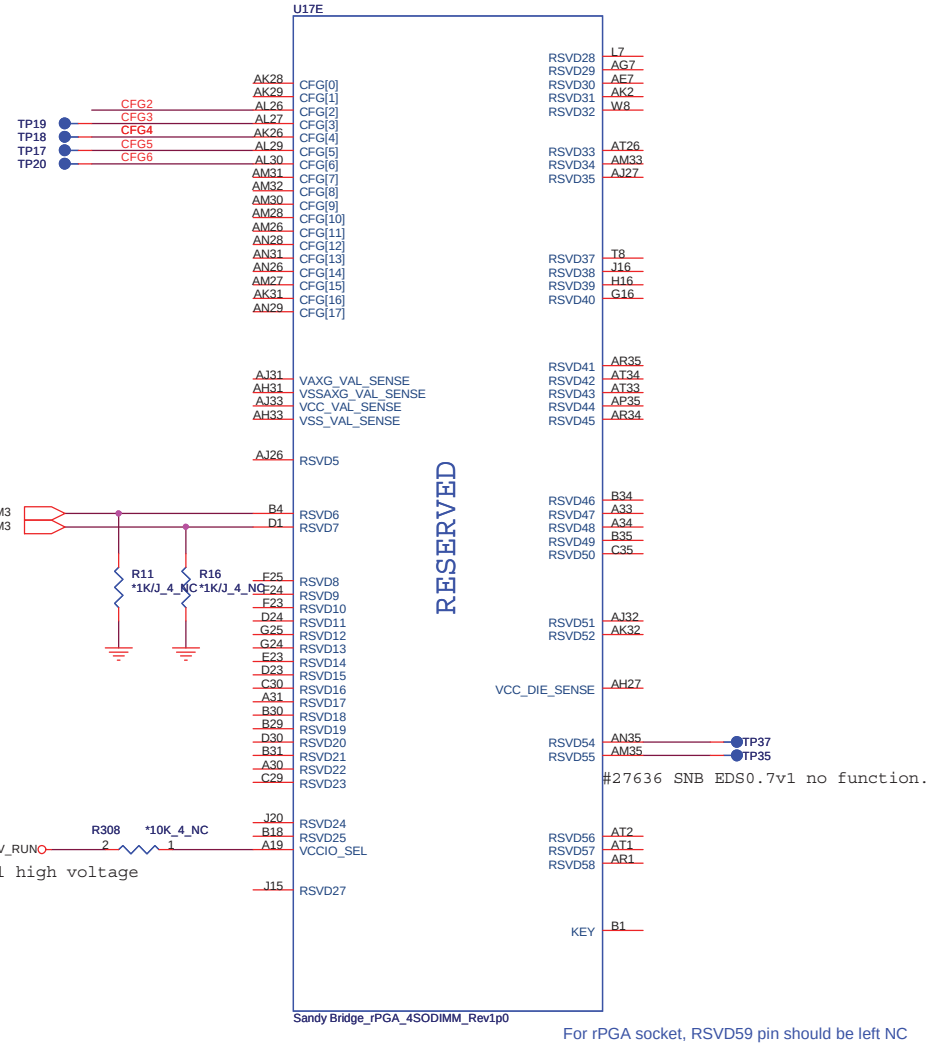
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R199 1K/F_4

Quanta Computer Inc.
PROJECT : R03A/V03A

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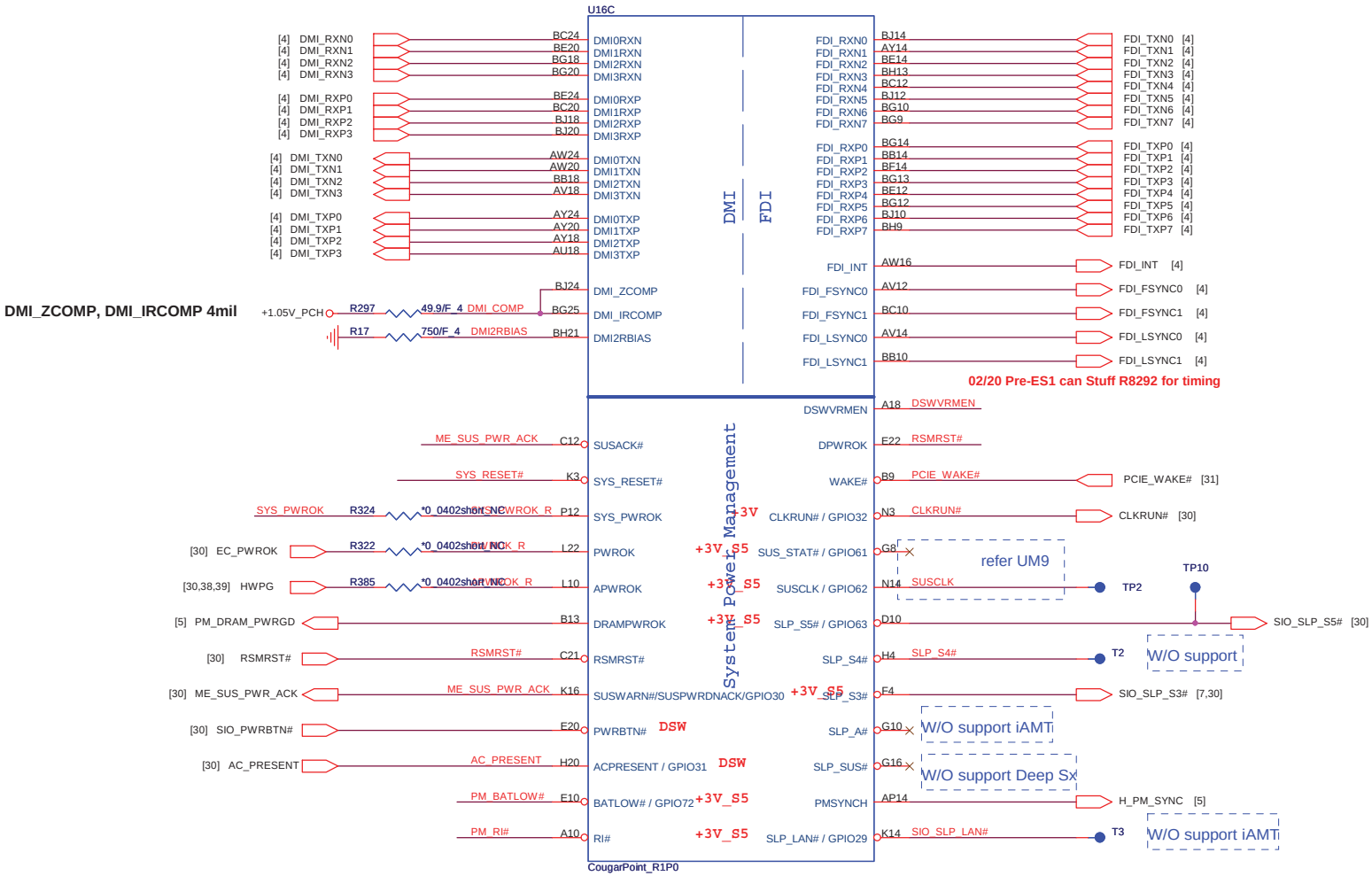
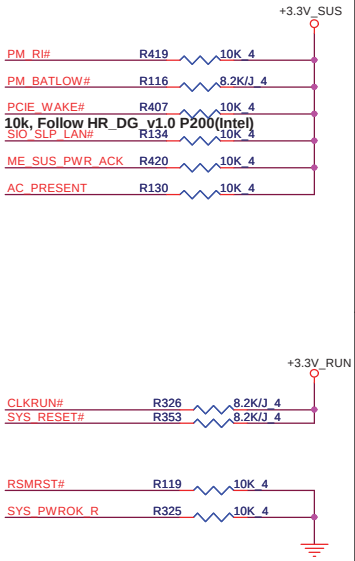
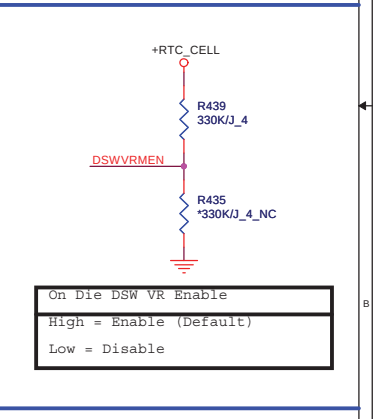
Cougar Point (DMI,FDI,PM)

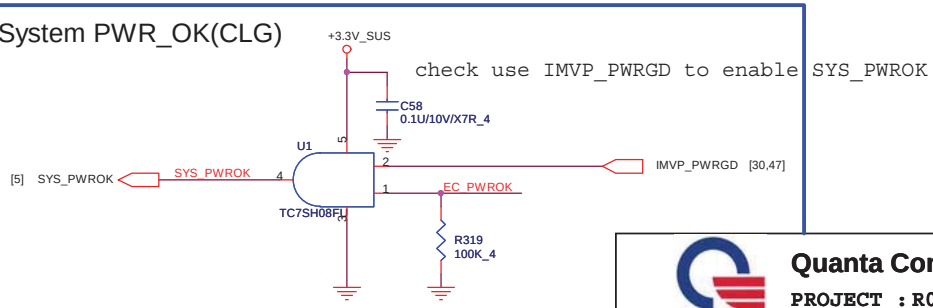


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



Quanta Computer Inc.		
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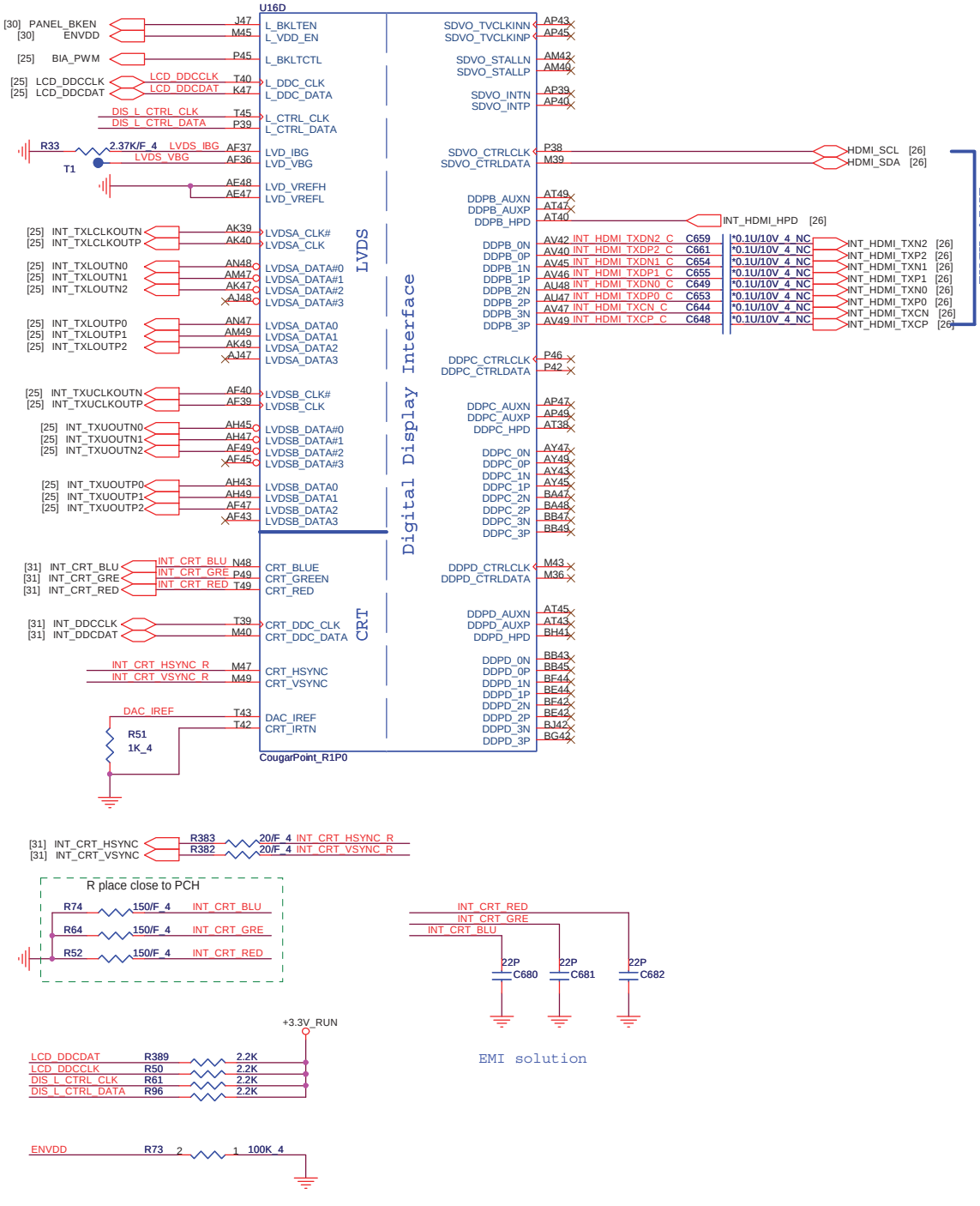
Cougar Point (LVDS,DDI)



Cougar Point (GND)

Quanta Computer Inc.			
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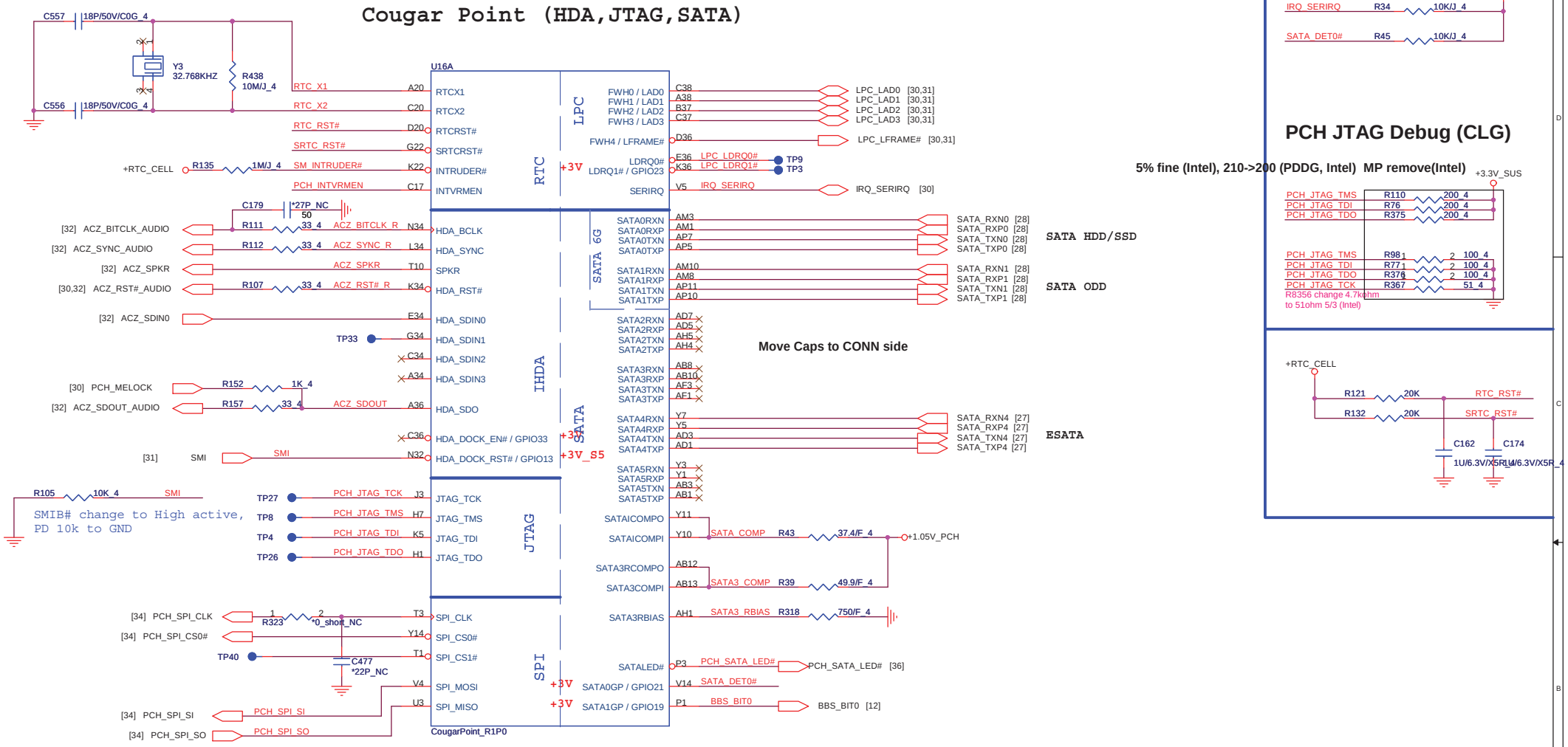

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R41 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R146 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R434 330K/J_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R118 1K_4 ACZ_SYNC_R

Quanta Computer Inc.
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	Cougar Point 3/7	2A

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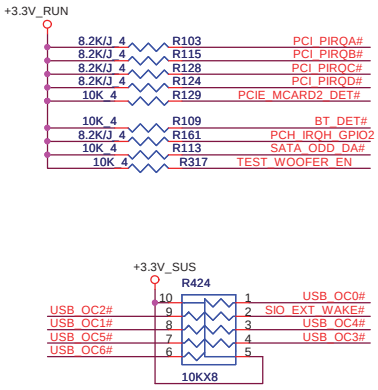
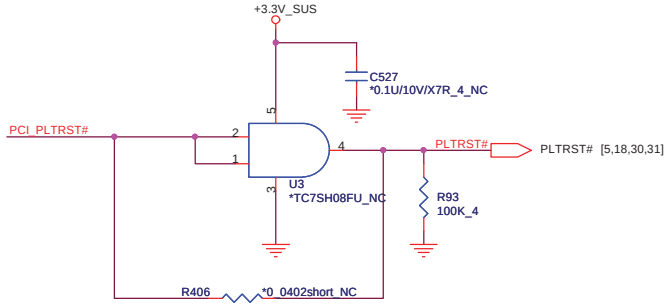
Cougar Point-M (PCI,USB,NVRAM)

PCI/USBOC# Pull-up(CLG)



PLTRST#(CLG)



change SMIB# to SMI

SV_SET_UP
High = Strong (Default)

Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
			Defined in EDS (Intel)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

BBS_BIT1 R102 *1K_4_NC
[11] BBS_BIT0 R327 *1K_4_NC

Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]

CheckList_1.0 p58; HR_v1.0 p450

R314 2.2K +1.8V_RUN
DF_TVS [14]

follow CheckList_1.5, DF_TVS pu-high 2,2k only, Remove R315

Quanta Computer Inc.

PROJECT : R03A/V03A

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Cougar Point-M (PCI-E,SMBUS,CLK)

U16B

WLAN [31] PCIE_RXN1 BG34 PERN1
[31] PCIE_RXP1 BJ34 PERP1
[31] PCIE_TXN1 C31 0.1U/10V/X7R_4 PCIE_TXN1_C AV32 PETN1
[31] PCIE_TXP1 C30 0.1U/10V/X7R_4 PCIE_TXP1_C AU32 PETP1

WWAN [31] PCIE_RXN2 BE34 PERN2
[31] PCIE_RXP2 BF34 PERP2
[31] PCIE_TXN2 C11 0.1U/10V/X7R_4 PCIE_TXN2_C BB32 PETN2
[31] PCIE_TXP2 C12 0.1U/10V/X7R_4 PCIE_TXP2_C AY32 PETP2

USB 3.0 [31] PCIE_RXN3 BG36 PERN3
[31] PCIE_RXP3 BJ36 PERP3
[31] PCIE_TXN3 C16 0.1U/10V/X7R_4 PCIE_TXN3_C AV34 PETN3
[31] PCIE_TXP3 C14 0.1U/10V/X7R_4 PCIE_TXP3_C AU34 PETP3

BF36 PERN4
BE36 PERP4
AY34 PETN4
BB34 PETP4

LAN [31] PCIE_RXN5 BG37 PERN5
[31] PCIE_RXP5 BH37 PERP5
[31] PCIE_TXN5 C24 0.1U/10V/X7R_4 PCIE_TXN5_C AY36 PETN5
[31] PCIE_TXP5 C21 0.1U/10V/X7R_4 PCIE_TXP5_C BB36 PETP5

Express card [31] PCIE_RXN6 BJ38 PERN6
[31] PCIE_RXP6 BG38 PERP6
[31] PCIE_TXN6 C52 0.1U/10V/X7R_4 PCIE_TXN6_LAN_C AU36 PETN6
[31] PCIE_TXP6 C46 0.1U/10V/X7R_4 PCIE_TXP6_LAN_C AV36 PETP6

BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7

BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

PCI-E*

SMBUS
+3V_S5 SMBALERT# / GPIO11 E12 PCH_SMB_ALERT#
SMBCLK H14 SMBCLK SMBCLK [31]
SMBDATA C9 SMBDATA SMBDATA [31]
+3V_S5 SML0ALERT# / GPIO60 A12 1K_4 R421 +3.3V_SUS 10k -> 1k ohm (CRB,Dell) DDR_HVREF_RST_PCH [5]
SML0CLK C8 SML0CLK
SML0DATA G12 SML0DATA
+3V_S5 SML1ALERT# / PCHHOT# / GPIO74 C13 PCH_GPIO74
+3V_S5 SML1CLK / GPIO58 E14 SMB_CLK_ME1
+3V_S5 SML1DATA / GPIO75 M16 SMB_DATA_ME1

Controller Link
CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

CLOCKS
WLAN [31] CLK_PCIE_WLANN Y40 CLKOUT_PCIE0N
[31] CLK_PCIE_WLANP Y39 CLKOUT_PCIE0P
[31] PCIE_CLK_REQ0# PCIE_CLK_REQ0# J2 PCIECLKRQ0# / GPIO73 +3V_S5

WWAN [31] CLK_PCIE_WMAXN AB49 CLKOUT_PCIE1N
[31] CLK_PCIE_WMAXP AB47 CLKOUT_PCIE1P
[31] PCIE_CLK_REQ1# PCIE_CLK_REQ1# M1 PCIECLKRQ1# / GPIO18 +3V

USB3.0 [31] CLK_PCIE_USB30N AA48 CLKOUT_PCIE2N
[31] CLK_PCIE_USB30P AA47 CLKOUT_PCIE2P
[31] PCIE_CLK_REQ2# PCIE_CLK_REQ2# V10 PCIECLKRQ2# / GPIO20 +3V

Y37 CLKOUT_PCIE3N
Y36 CLKOUT_PCIE3P
PCIE_CLK_REQ3# A8 PCIECLKRQ3# / GPIO25 +3V_S5

LAN [31] CLK_PCIE_LANN Y43 CLKOUT_PCIE4N
[31] CLK_PCIE_LANP Y45 CLKOUT_PCIE4P
[31] PCIE_CLK_REQ4# PCIE_CLK_REQ4# L12 PCIECLKRQ4# / GPIO26 +3V_S5

Express card [31] CLK_PCIE_EXPN V45 CLKOUT_PCIE5N
[31] CLK_PCIE_EXPP V46 CLKOUT_PCIE5P
[31] PCIE_CLK_REQ5# PCIE_CLK_REQ5# L14 PCIECLKRQ5# / GPIO44 +3V_S5

AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
PEG_B_CLKRQ# E6 PEG_B_CLKRQ# / GPIO56 +3V_S5

V40 CLKOUT_PCIE6N
V42 CLKOUT_PCIE6P
PCIE_CLK_REQ6# T13 PCIECLKRQ6# / GPIO45 +3V_S5

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
add test point for XDP
PCIE_CLK_REQ7# K12 PCIECLKRQ7# / GPIO46 +3V_S5

XDP CLK_PCIE_XDPN T5 AK14 CLKOUT_ITPXDP_N
CLK_PCIE_XDPP T4 AK13 CLKOUT_ITPXDP_P

PEG_A_CLKRQ# / GPIO47 M10 PEG_A_CLKRQ# PEG_A_CLKRQ# [18]
CLKOUT_PEG_A_N AB37 CLK_PCIE_VGAN [18]
CLKOUT_PEG_A_P AB38 CLK_PCIE_VGAP [18]
CLKOUT_DMI_N AV22 CLK_CPU_BCLKN [5]
CLKOUT_DMI_P AU22 CLK_CPU_BCLKP [5]
CLKOUT_DP_N AM12 CLK_DP_N [5]
CLKOUT_DP_P AM13 CLK_DP_P [5]
CLKIN_DMI_N BF18 CLK_DMIN
CLKIN_DMI_P BE18 CLK_DMIP
CLKIN_GND1_N BJ30 CLK_GND1_N
CLKIN_GND1_P BG30 CLK_GND1_P
CLKIN_DOT_96N G24 CLK_BUF_DREFCLKN
CLKIN_DOT_96P E24 CLK_BUF_DREFCLKP
CLKIN_SATA_N AK7 CLK_BUF_DREFSSCLKN
CLKIN_SATA_P AK5 CLK_BUF_DREFSSCLKP
REFCLK14IN K45 CLK_PCH_14M
CLKIN_PCILOOPBACK H45 CLK_PCI_FB CLK_PCI_FB [12]
XTAL25_IN V47 XTAL25_IN
XTAL25_OUT V49 XTAL25_OUT
C480 27P 50 R368 1M/J_4 Y2 25MHz C493 27P 50
XCLK_RCOMP Y47 XCLK_RCOMP R329 90.9/F_4 +1.05V_PCH

FLEX CLOCKS
+3V CLKOUTFLEX0 / GPIO64 K43 CLK_48M_CARD_R R91 22_4 CLK_48M_CARD [29]
+3V CLKOUTFLEX1 / GPIO65 F47 CLK_VGA_27M_R R405 22_4 CLK_VGA_27M [20]
+3V CLKOUTFLEX2 / GPIO66 H47 CLK_FLEX2 T6
+3V CLKOUTFLEX3 / GPIO67 K49 CLK_VGA_27M_SS_R R79 *22_4_NC CLK_VGA_27M_SS [20]

0727 add 22ohm resistor
C523 *22P_NC
C131 *22P_NC
EMI soultion reserve, please place near PCH

CougarPoint_R1P0

	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

+3.3V_RUN
Q3 2N7002W-7-F R330 2.2K R425 2.2K
SMBCLK WLAN_SCLK [16,17,28,31]
Q33 2N7002W-7-F
SMBDATA WLAN_SDATA [16,17,28,31]
Q4 2N7002W-7-F
SMB_CLK_ME1 SMBCLK1 [30]
+3.3V_SUS Q6 2N7002W-7-F
SMB_DATA_ME1 SMBDAT1 [30]
change direction

CLK_REQ/Strap Pin(CLG)

+3.3V_SUS
PCIE_CLK_REQ0# 10K_4 R89
PCIE_CLK_REQ3# 10K_4 R399
PCIE_CLK_REQ4# 10K_4 R100
PCIE_CLK_REQ5# 10K_4 R123
PCIE_CLK_REQ6# 10K_4 R117
PCIE_CLK_REQ7# 10K_4 R101
PCIE_CLK_REQ2# 10K_4 R42
PEG_B_CLKRQ# 10K_4 R99
+3.3V_RUN
PCIE_CLK_REQ1# 10K_4 R349
+3.3V_SUS
PEG_A_CLKRQ# 10K_4 R94 *10K_4_NC R95
+3.3V_SUS
PCH_GPIO74 10K_4 R422
PCH_SMB_ALERT# 10K_4 R122
SMBCLK R334 2.2K
SMBDATA R411 2.2K
SML0CLK R396 2.2K
SML0DATA R127 2.2K
SMB_CLK_ME1 R351 2.2K
SMB_DATA_ME1 R374 2.2K

Stuff for Integrated CLK Gen Mode

CLK_DMIN R25 10K_4
CLK_DMIP R29 10K_4
CLK_GND1_N
CLK_GND1_P R302 1 2 10K_4
CLK_BUF_DREFCLKN R126 10K_4
CLK_BUF_DREFCLKP R125 10K_4
CLK_BUF_DREFSSCLKN R31 10K_4
CLK_BUF_DREFSSCLKP R30 10K_4
CLK_PCH_14M R78 10K_4

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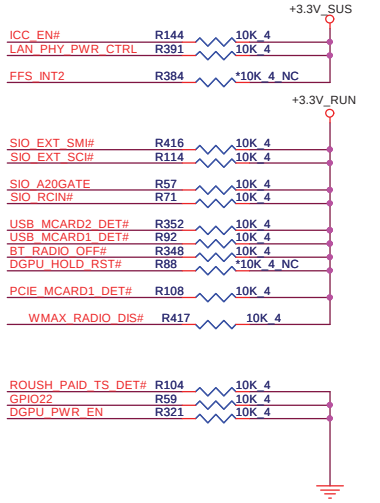
Cougar Point (GPIO,VSS_NCTF,RSVD)

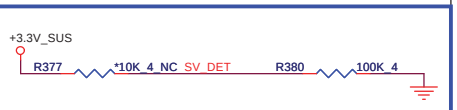
Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

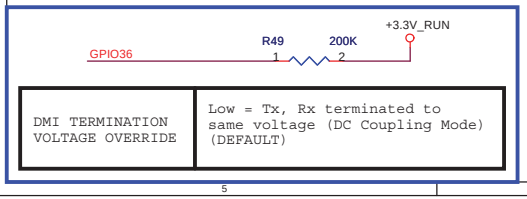
R70 *1K_4_NC PLL_ODVR_EN

GPIO037 follow 14"team need INTEL confirm

GPIO Pull-up/Pull-down(CLG)







SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

MFG-TEST

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COUGAR POINT (POWER)

Cougar Point (POWER)

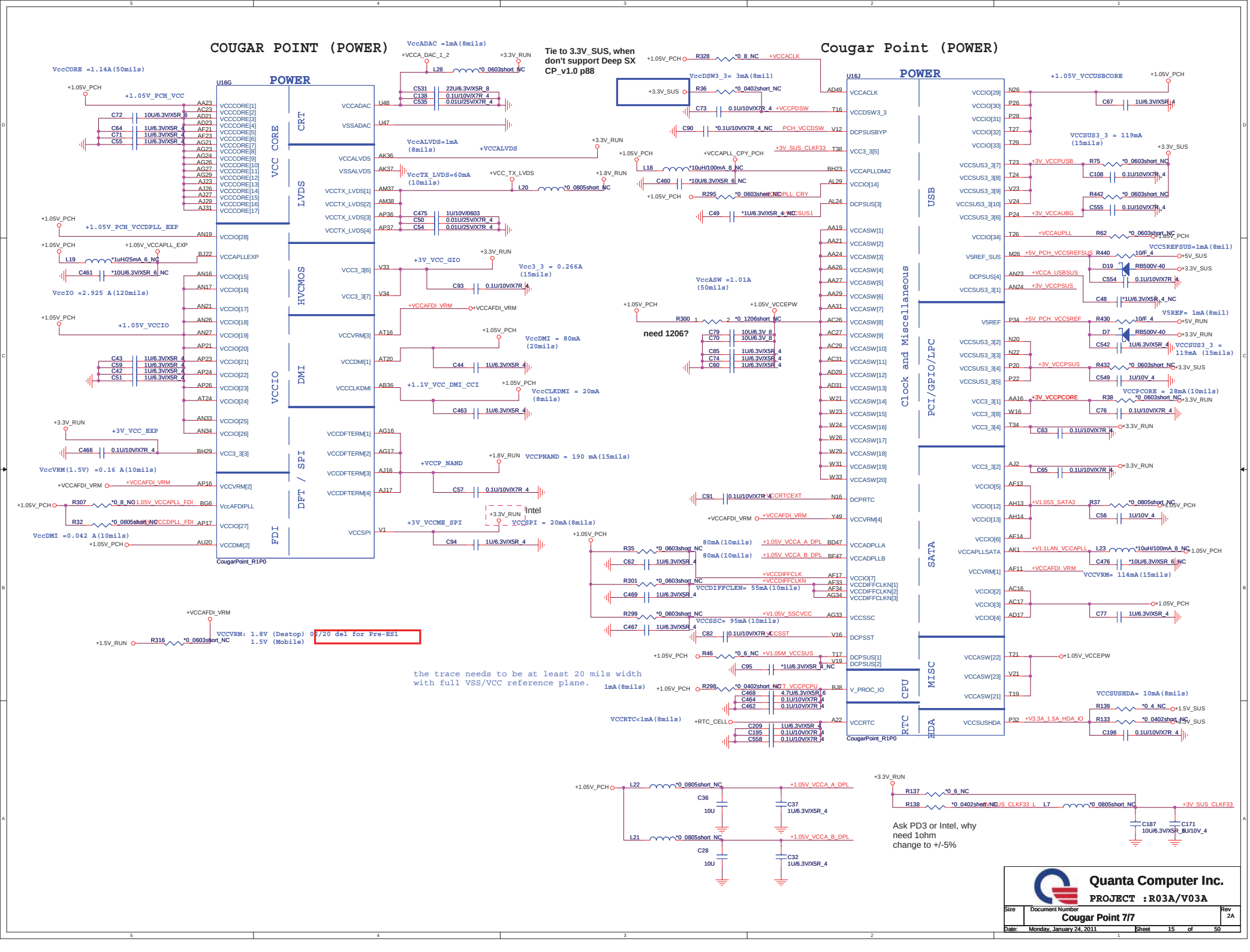
Tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

need 1206?

Intel

the trace needs to be at least 20 mils width with full VSS/VCC reference plane.

Ask PD3 or Intel, why need 1ohm change to +/-5%



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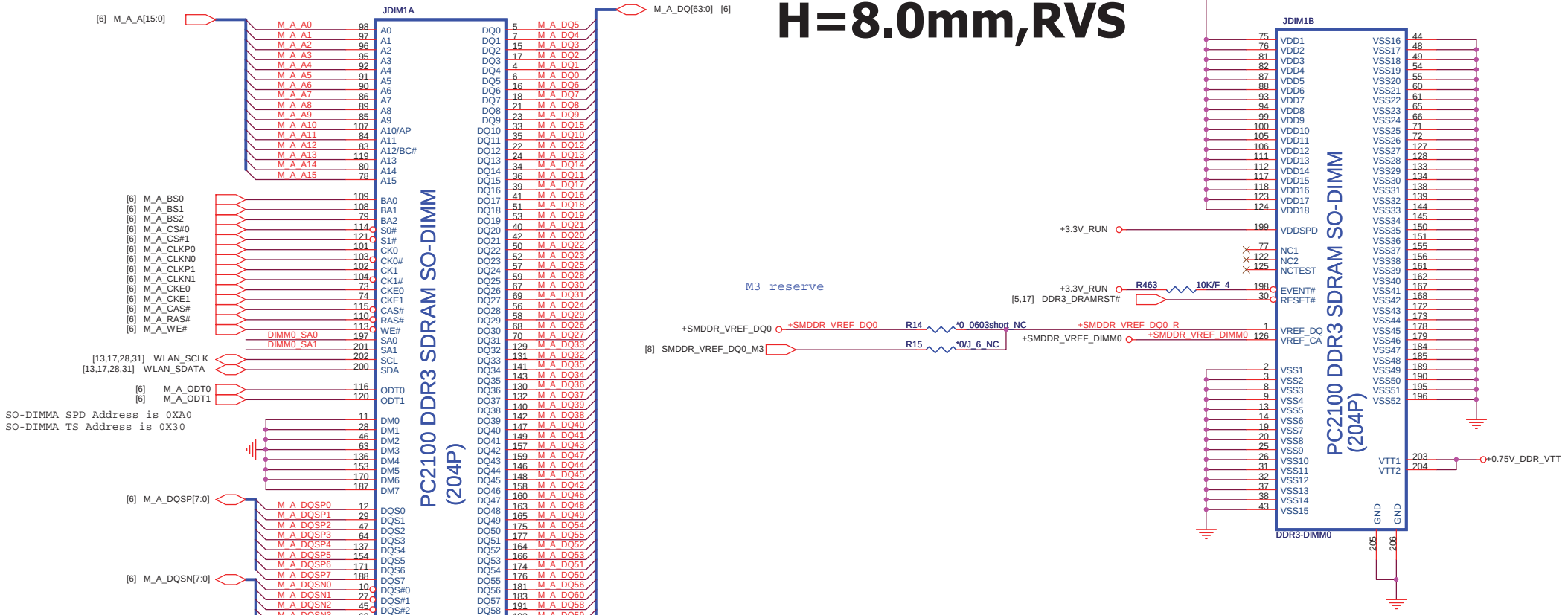
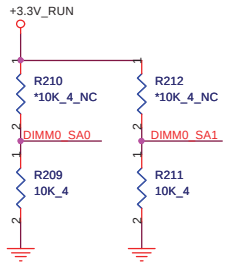
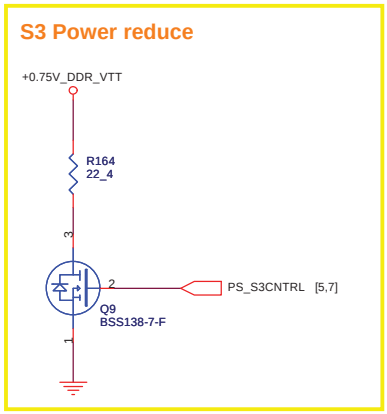
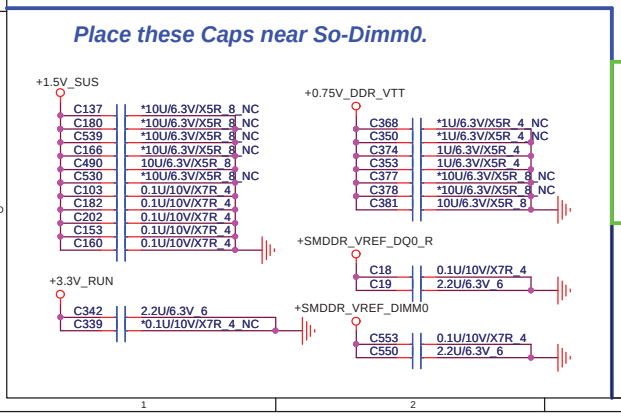
H=8.0mm,RVS

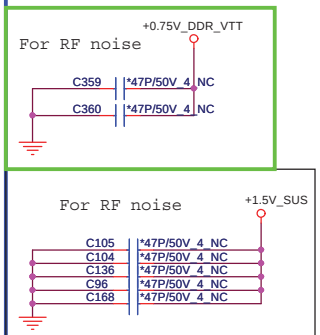


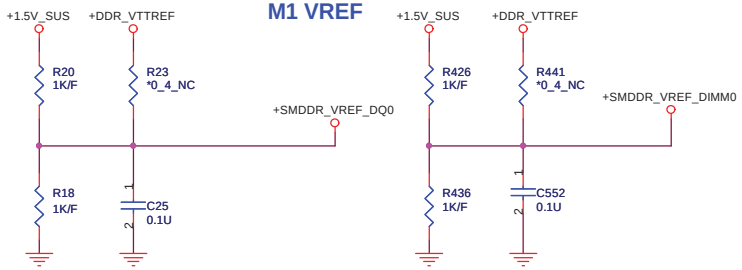


	DIMM0_SA0	DIMM0_SA1
DOMM0	0	0
DOMM1	0	1









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	DDR3 DIMM-0	2A

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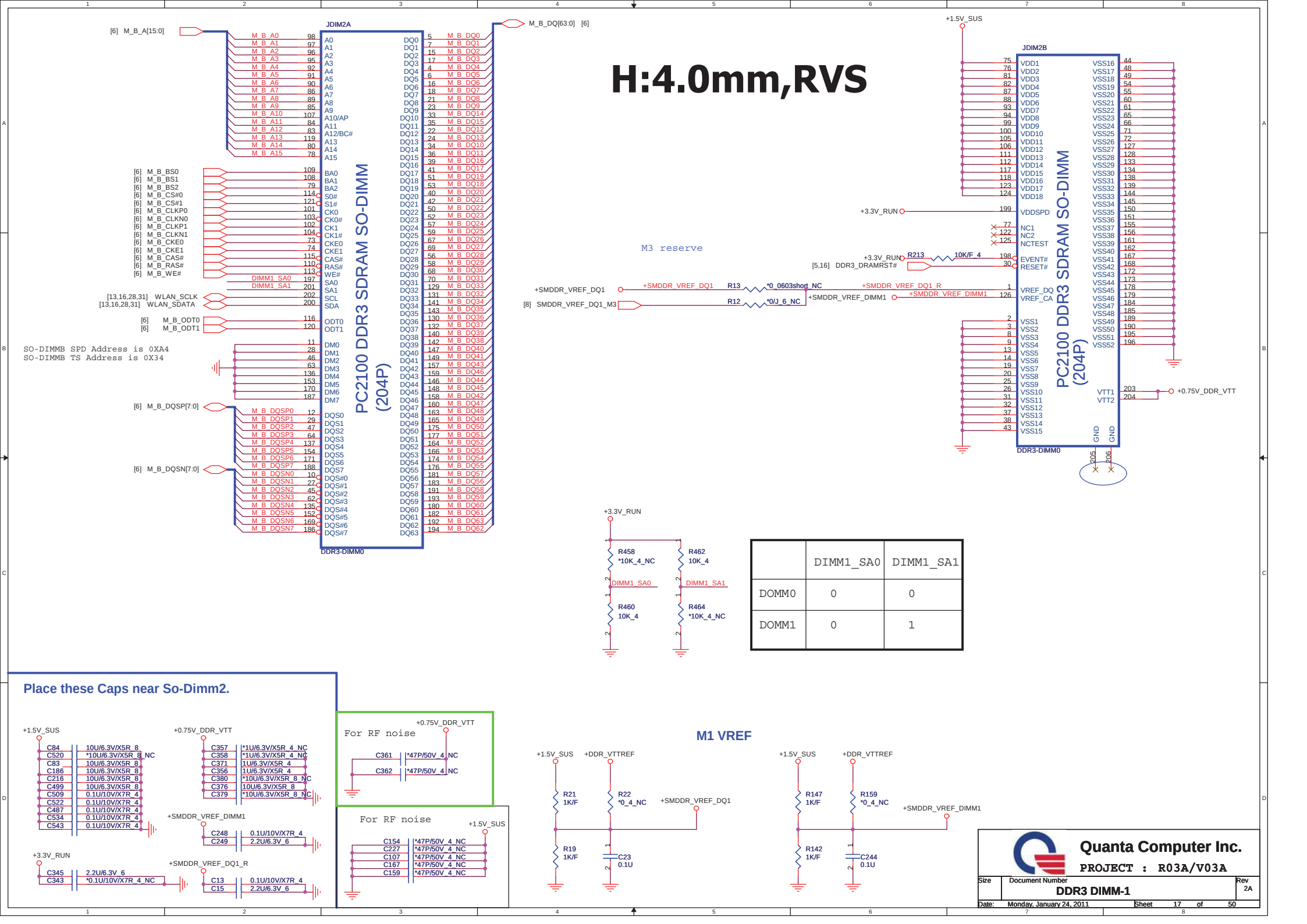
H:4.0mm,RVS



	DIMM1_SA0	DIMM1_SA1
DOMM0	0	0
DOMM1	0	1

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	DDR3 DIMM-1	2A

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PEX_IOVDD+PEX_IOVDDQ >2.2A

~ 500mA

1600mA

0.1u *4 under GPU
Others Near GPU

0.1u under GPU
Others Near GPU

confirm with FAE
should change power rail

12~16 mils width
120mA
0.1u under GPU
Others Near GPU

120mA 12~16 mils width

0.1u under GPU
Others Near GPU
add 1u near GPU as FAE confirm

1211 for Nvidia request
add transition cap

U20A
N12P-GE-A1

PCI EXPRESS

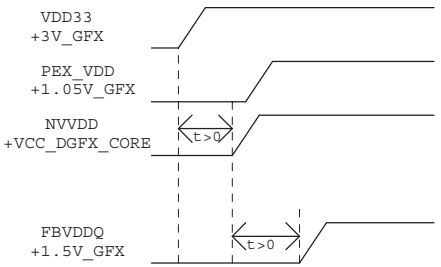
GPU all PWROK

Q84: H(sat), L(cut-off)

10k PU 3V_GFX as FAE's feedback

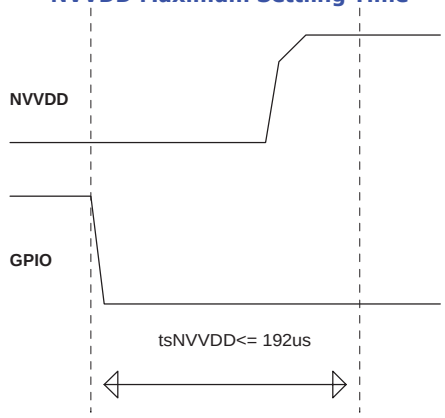
Add MOS for preventing leakage.

Power up sequence

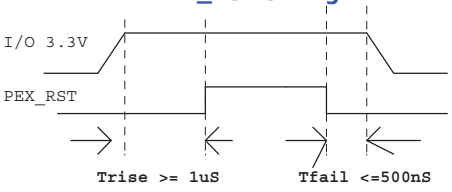


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



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U20B
N12P-GE-A1

U20C
N12P-GE-A1

mode E change to mode D design

Follow Mode D Command Mapping
(ODTX, CKE*, RST)

All need stuff for N11P-GS
N11M-GE2 no VMC_CMD* (64 bits)

MEMORY I/F A

MEMORY I/F C

15mils width

For Debug only

100mA

3050mA

0.1u *8 under GPU
Others Near GPU

All need stuff for N11P

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	N12P-GE (MEMORY I/F) 2/5	2A

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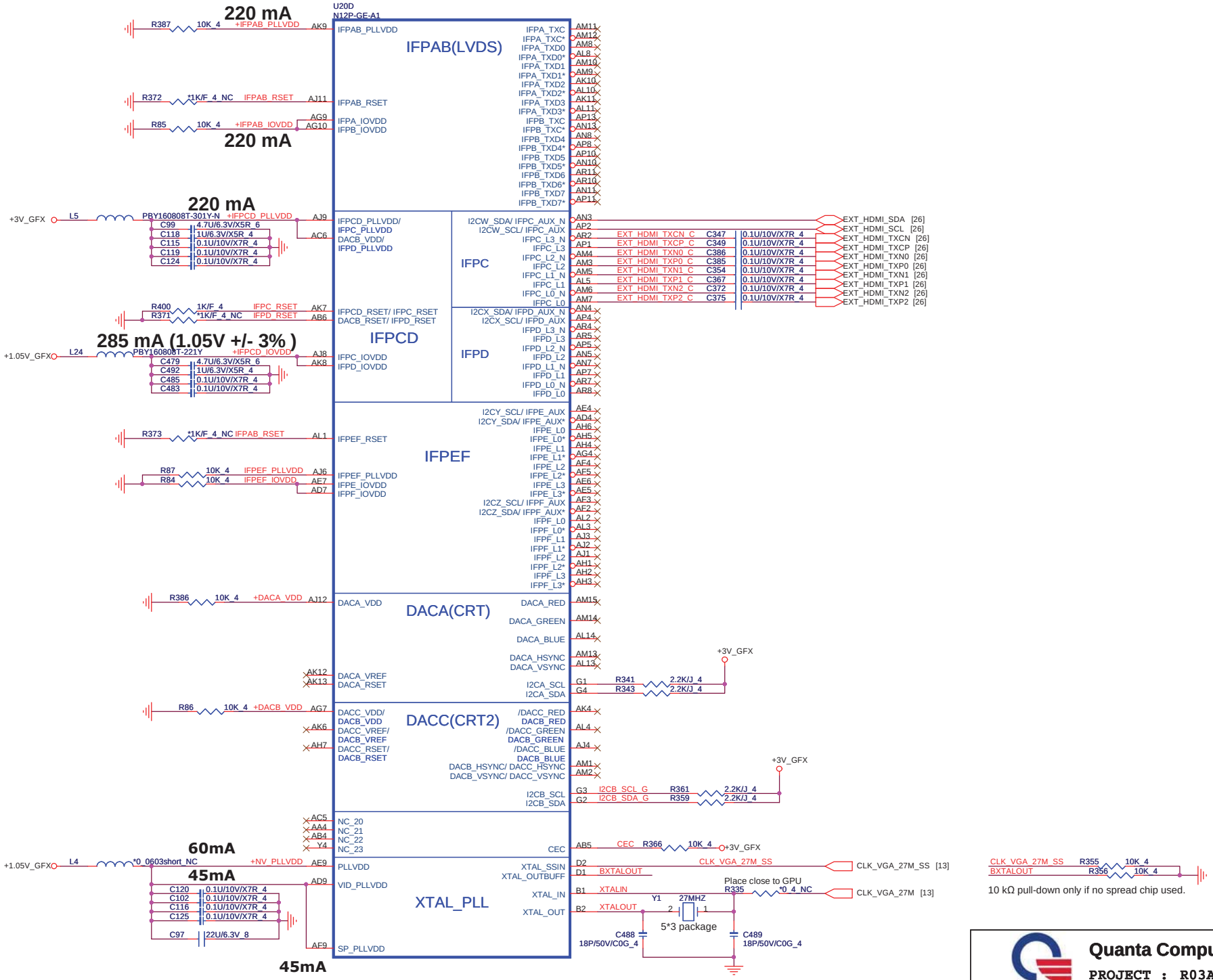

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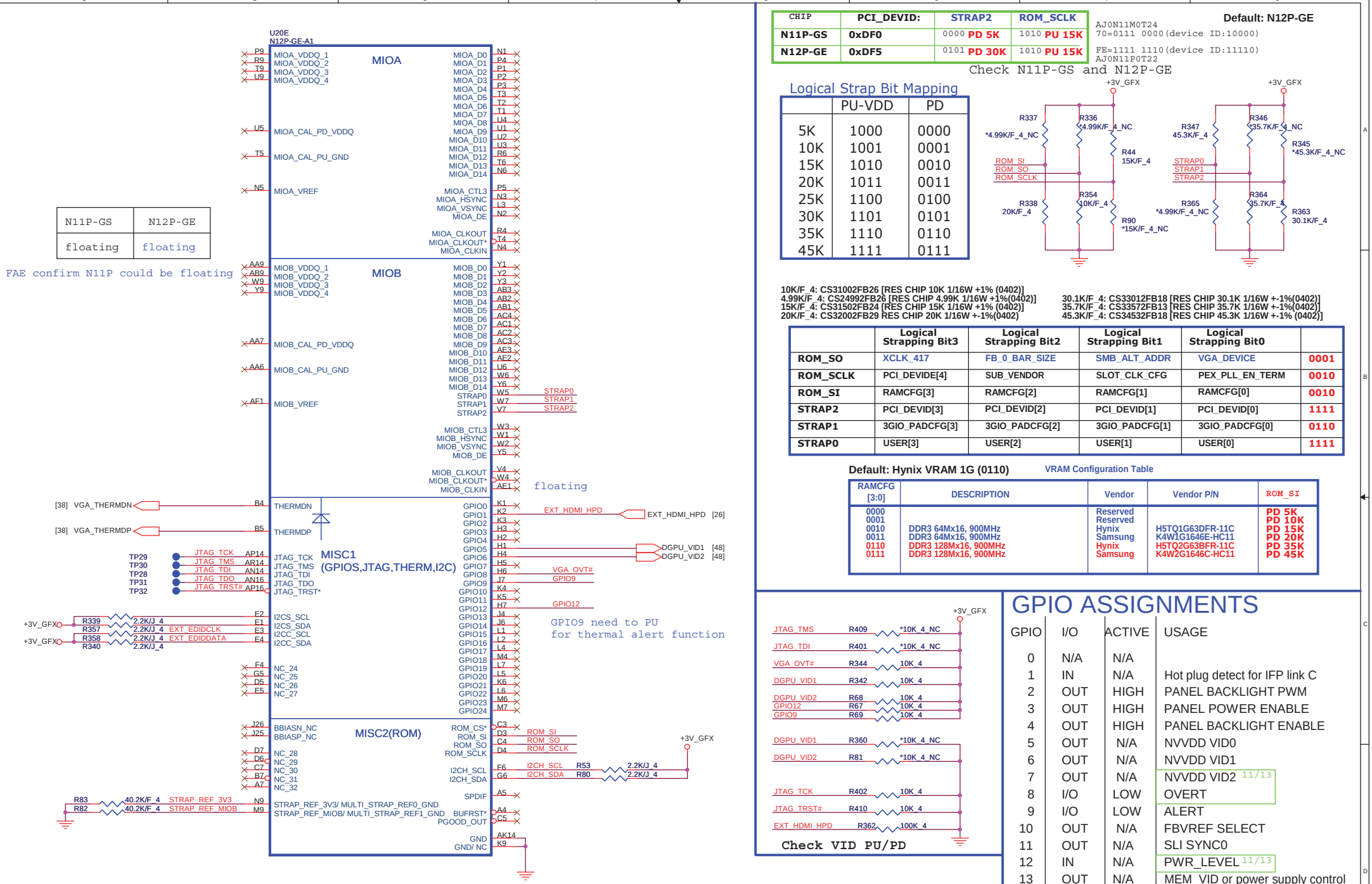

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N11P-GS	0xDF0	0000 PD 5K	1010 PU 15K
N12P-GE	0xDF5	0101 PD 30K	1010 PU 15K

Default: N12P-GE

AJ0N11M0T24
70=0111 0000(device ID:10000)

FE=1111 1110(device ID:11110)
AJ0N11P0T22

Check N11P-GS and N12P-GE

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 1G (0110) VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		PD 5K
0001		Reserved		PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	H5TQ1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz	Samsung	K4W1G1646E-HC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	H5TQ2G63BFR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	K4W2G1646C-HC11	PD 45K

Check VID PU/PD

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

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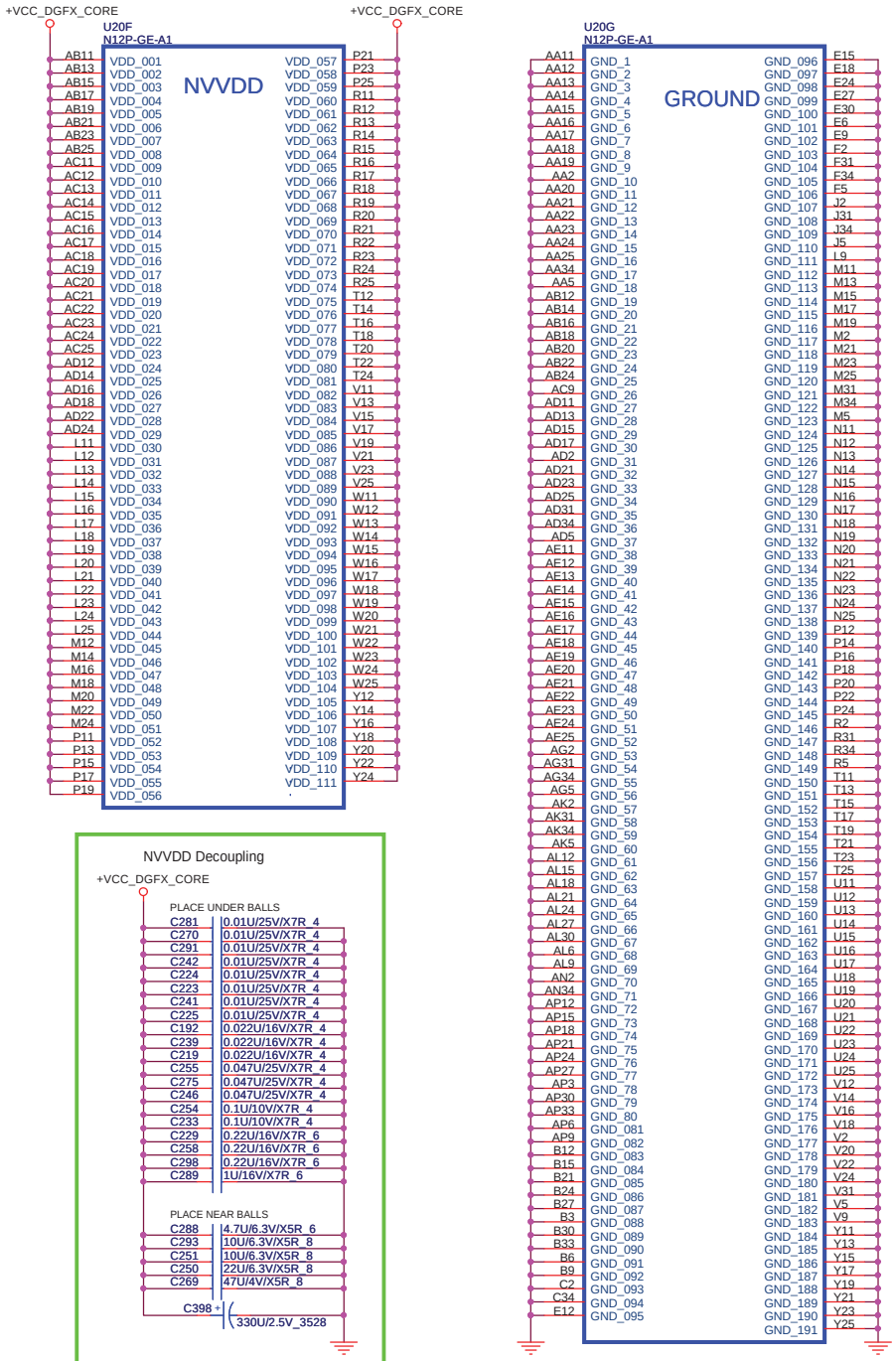

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	N12P-GE (POWER & GND) 5/5	2A

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SWAP CMD NET
modify Mode E to Mode D

[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

change VRAM footprint to hynix 2G(the package is bigger)

U11 / U22 / U12 / U23 — 96-BALL SDRAM DDR3 — K4W1G1646E-HC12

+1.5V_GFX

R257 243/F
R473 243/F
R252 243/F
R490 243/F

R249 162/F
VMA_CLKP0
VMA_CLKN0
Placement has to be close to VRAM

R248 162/F
VMA_CLKP1
VMA_CLKN1
Placement has to be close to VRAM

R477 1.33K/F_4
R480 1.33K/F_4
C584 0.1U/10V/X7R_4
VREFC_VMA1

R487 1.33K/F_4
R486 1.33K/F_4
C586 0.1U/10V/X7R_4
VREFD_VMA1

R484 1.33K/F_4
R479 1.33K/F_4
C585 0.1U/10V/X7R_4
VREFC_VMA3

R476 1.33K/F_4
R474 1.33K/F_4
C579 0.1U/10V/X7R_4
VREFD_VMA3

C397 *330U/2.5V_3528_NC

C403 1U/6.3V/X5R_4
C405 1U/6.3V/X5R_4
C407 0.1U/10V/X5R_4
C404 0.1U/10V/X5R_4
C406 0.1U/10V/X5R_4

C599 1U/6.3V/X5R_4
C598 1U/6.3V/X5R_4
C590 0.1U/10V/X5R_4
C582 0.1U/10V/X5R_4
C595 0.1U/10V/X5R_4

C393 1U/6.3V/X5R_4
C413 1U/6.3V/X5R_4
C409 0.1U/10V/X5R_4
C415 0.1U/10V/X5R_4
C389 0.1U/10V/X5R_4

C604 1U/6.3V/X5R_4
C576 1U/6.3V/X5R_4
C575 0.1U/10V/X5R_4
C603 0.1U/10V/X5R_4
C601 0.1U/10V/X5R_4

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	N12P-GE VRAM-1(DDR3 BGA96)	2A
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SWAP CMD NET
modify Mode E to Mode D

[19] VMC_DQ[63..0]
[19] VMC_DM[7..0]
[19] VMC_WDQS[7..0]
[19] VMC_RDQS[7..0]

CHANNEL B: 512MB/1024MB DDR3

change VRAM footprint to hynix 2G(the package is bigger)

U19 — K4W1G1646E-HC12 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 VREFCA
VREFD_VMC1 H1 VREFDQ

[19] VMC_CMD9 N3 A0
[19] VMC_CMD11 P7 A1
[19] VMC_CMD8 P3 A2
[19] VMC_CMD25 N2 A3
[19] VMC_CMD10 P8 A4
[19] VMC_CMD24 P2 A5
R8 A6
[19] VMC_CMD22 R2 A7
[19] VMC_CMD7 T8 A8
[19] VMC_CMD21 R3 A9
[19] VMC_CMD6 L7 A10/AP
[19] VMC_CMD29 R7 A11
[19] VMC_CMD23 N7 A12/BC
[19] VMC_CMD28 T3 A13
[19] VMC_CMD20 T7 A14
[19] VMC_CMD4 M7 A15
[19] VMC_CMD14

[19] VMC_CMD12 M2 BA0
[19] VMC_CMD27 N8 BA1
[19] VMC_CMD26 M3 BA2

[19] VMC_CLKP0 J7 CK
[19] VMC_CLKN0 K7 CK
[19] VMC_CMD3 K9 CKE

[19] VMC_CMD2 K1 ODT
[19] VMC_CMD0 L2 CS
[19] VMC_CMD30 J3 RAS
[19] VMC_CMD15 K3 CAS
[19] VMC_CMD13 L3 WE

VMC_WDQS2 F3 DQSL
VMC_RDQS2 G3 DQSL

VMC_DM2 E7 DML
VMC_DM0 D3 DMU

VMC_WDQS0 C7 DQSU
VMC_RDQS0 B7 DQSU

[19] VMC_CMD5 T2 RESET

VMC_ZQ1 L8 ZQ

DQL0 E3 VMC_DQ22
DQL1 F7 VMC_DQ21
DQL2 F2 VMC_DQ23
DQL3 F8 VMC_DQ16
DQL4 H3 VMC_DQ20
DQL5 H8 VMC_DQ17
DQL6 G2 VMC_DQ18
DQL7 H7 VMC_DQ19

DQU0 D7 VMC_DQ3
DQU1 C3 VMC_DQ6
DQU2 C8 VMC_DQ0
DQU3 C2 VMC_DQ7
DQU4 A7 VMC_DQ1
DQU5 A2 VMC_DQ5
DQU6 B8 VMC_DQ2
DQU7 A3 VMC_DQ4

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 +1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

R390 243/F

U5 — K4W1G1646E-HC12 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 VREFCA
VREFD_VMC1 H1 VREFDQ

VMC_CMD9 N3 A0
VMC_CMD11 P7 A1
VMC_CMD8 P3 A2
VMC_CMD25 N2 A3
VMC_CMD10 P8 A4
VMC_CMD24 P2 A5
VMC_CMD22 R8 A6
VMC_CMD7 R2 A7
VMC_CMD21 T8 A8
VMC_CMD6 R3 A9
VMC_CMD29 L7 A10/AP
VMC_CMD23 R7 A11
VMC_CMD28 N7 A12/BC
VMC_CMD20 T3 A13
VMC_CMD4 T7 A14
VMC_CMD14 M7 A15

VMC_CMD12 M2 BA0
VMC_CMD27 N8 BA1
VMC_CMD26 M3 BA2

VMC_CLKP0 J7 CK
VMC_CLKN0 K7 CK
VMC_CMD3 K9 CKE

VMC_CMD2 K1 ODT
VMC_CMD0 L2 CS
VMC_CMD30 J3 RAS
VMC_CMD15 K3 CAS
VMC_CMD13 L3 WE

VMC_WDQS3 F3 DQSL
VMC_RDQS3 G3 DQSL

VMC_DM3 E7 DML
VMC_DM1 D3 DMU

VMC_WDQS1 C7 DQSU
VMC_RDQS1 B7 DQSU

VMC_CMD5 T2 RESET

VMC_ZQ2 L8 ZQ

DQL0 E3 VMC_DQ24
DQL1 F7 VMC_DQ30
DQL2 F2 VMC_DQ26
DQL3 F8 VMC_DQ28
DQL4 H3 VMC_DQ25
DQL5 H8 VMC_DQ31
DQL6 G2 VMC_DQ27
DQL7 H7 VMC_DQ29

DQU0 D7 VMC_DQ8
DQU1 C3 VMC_DQ14
DQU2 C8 VMC_DQ9
DQU3 C2 VMC_DQ12
DQU4 A7 VMC_DQ11
DQU5 A2 VMC_DQ13
DQU6 B8 VMC_DQ10
DQU7 A3 VMC_DQ15

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 +1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

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U7 — K4W1G1646E-HC12 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 VREFCA
VREFD_VMC3 H1 VREFDQ

VMC_CMD9 N3 A0
VMC_CMD11 P7 A1
VMC_CMD8 P3 A2
VMC_CMD25 N2 A3
VMC_CMD10 P8 A4
VMC_CMD24 P2 A5
VMC_CMD22 R8 A6
VMC_CMD7 R2 A7
VMC_CMD21 T8 A8
VMC_CMD6 R3 A9
VMC_CMD29 L7 A10/AP
VMC_CMD23 R7 A11
VMC_CMD28 N7 A12/BC
VMC_CMD20 T3 A13
VMC_CMD4 T7 A14
VMC_CMD14 M7 A15

VMC_CMD12 M2 BA0
VMC_CMD27 N8 BA1
VMC_CMD26 M3 BA2

[19] VMC_CLKP1 J7 CK
[19] VMC_CLKN1 K7 CK
[19] VMC_CMD19 K9 CKE

[19] VMC_CMD18 K1 ODT
[19] VMC_CMD16 L2 CS
VMC_CMD30 J3 RAS
VMC_CMD15 K3 CAS
VMC_CMD13 L3 WE

VMC_WDQS4 F3 DQSL
VMC_RDQS4 G3 DQSL

VMC_DM4 E7 DML
VMC_DM5 D3 DMU

VMC_WDQS5 C7 DQSU
VMC_RDQS5 B7 DQSU

VMC_CMD5 T2 RESET

VMC_ZQ3 L8 ZQ

DQL0 E3 VMC_DQ36
DQL1 F7 VMC_DQ34
DQL2 F2 VMC_DQ39
DQL3 F8 VMC_DQ32
DQL4 H3 VMC_DQ37
DQL5 H8 VMC_DQ35
DQL6 G2 VMC_DQ38
DQL7 H7 VMC_DQ33

DQU0 D7 VMC_DQ42
DQU1 C3 VMC_DQ47
DQU2 C8 VMC_DQ41
DQU3 C2 VMC_DQ45
DQU4 A7 VMC_DQ44
DQU5 A2 VMC_DQ43
DQU6 B8 VMC_DQ40
DQU7 A3 VMC_DQ46

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 +1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

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U21 — K4W1G1646E-HC12 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 VREFCA
VREFD_VMC3 H1 VREFDQ

VMC_CMD9 N3 A0
VMC_CMD11 P7 A1
VMC_CMD8 P3 A2
VMC_CMD25 N2 A3
VMC_CMD10 P8 A4
VMC_CMD24 P2 A5
VMC_CMD22 R8 A6
VMC_CMD7 R2 A7
VMC_CMD21 T8 A8
VMC_CMD6 R3 A9
VMC_CMD29 L7 A10/AP
VMC_CMD23 R7 A11
VMC_CMD28 N7 A12/BC
VMC_CMD20 T3 A13
VMC_CMD4 T7 A14
VMC_CMD14 M7 A15

VMC_CMD12 M2 BA0
VMC_CMD27 N8 BA1
VMC_CMD26 M3 BA2

VMC_CLKP1 J7 CK
VMC_CLKN1 K7 CK
VMC_CMD19 K9 CKE

VMC_CMD18 K1 ODT
VMC_CMD16 L2 CS
VMC_CMD30 J3 RAS
VMC_CMD15 K3 CAS
VMC_CMD13 L3 WE

VMC_WDQS6 F3 DQSL
VMC_RDQS6 G3 DQSL

VMC_DM6 E7 DML
VMC_DM7 D3 DMU

VMC_WDQS7 C7 DQSU
VMC_RDQS7 B7 DQSU

VMC_CMD5 T2 RESET

VMC_ZQ4 L8 ZQ

DQL0 E3 VMC_DQ49
DQL1 F7 VMC_DQ48
DQL2 F2 VMC_DQ55
DQL3 F8 VMC_DQ53
DQL4 H3 VMC_DQ52
DQL5 H8 VMC_DQ50
DQL6 G2 VMC_DQ54
DQL7 H7 VMC_DQ51

DQU0 D7 VMC_DQ61
DQU1 C3 VMC_DQ58
DQU2 C8 VMC_DQ62
DQU3 C2 VMC_DQ59
DQU4 A7 VMC_DQ60
DQU5 A2 VMC_DQ56
DQU6 B8 VMC_DQ63
DQU7 A3 VMC_DQ57

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9 +1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

J1 NC#J1
L1 NC#L1
J9 NC#J9
L9 NC#L9

R448 243/F

VMC_CLKP0
R388 162/F
VMC_CLKN0

Placement has to be close to VRAM

+1.5V_GFX
R395 1.33K/F_4
VREFC_VMC1
R148 1.33K/F_4
C519 0.1U/10V/X7R_4

+1.5V_GFX
R106 1.33K/F_4
VREFD_VMC1
R437 1.33K/F_4
C165 0.1U/10V/X7R_4

VMC_CLKP1
R466 162/F
VMC_CLKN1

Placement has to be close to VRAM

+1.5V_GFX
R223 1.33K/F_4
VREFC_VMC3
R226 1.33K/F_4
C369 0.1U/10V/X7R_4

+1.5V_GFX
R468 1.33K/F_4
VREFD_VMC3
R469 1.33K/F_4
C573 0.1U/10V/X7R_4

+1.5V_GFX
C524 1U/6.3V/X5R_4
C548 1U/6.3V/X5R_4
C503 0.1U/10V/X5R_4
C529 0.1U/10V/X5R_4
C505 0.1U/10V/X5R_4

+1.5V_GFX
C228 1U/6.3V/X5R_4
C148 1U/6.3V/X5R_4
C147 0.1U/10V/X5R_4
C146 0.1U/10V/X5R_4
C144 0.1U/10V/X5R_4

+1.5V_GFX
C364 1U/6.3V/X5R_4
C365 1U/6.3V/X5R_4
C366 0.1U/10V/X5R_4
C344 0.1U/10V/X5R_4
C363 0.1U/10V/X5R_4

+1.5V_GFX
C562 1U/6.3V/X5R_4
C568 1U/6.3V/X5R_4
C565 0.1U/10V/X5R_4
C569 0.1U/10V/X5R_4
C572 0.1U/10V/X5R_4

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	N12P-GE VRAM-2(DDR3 BGA96)	2A
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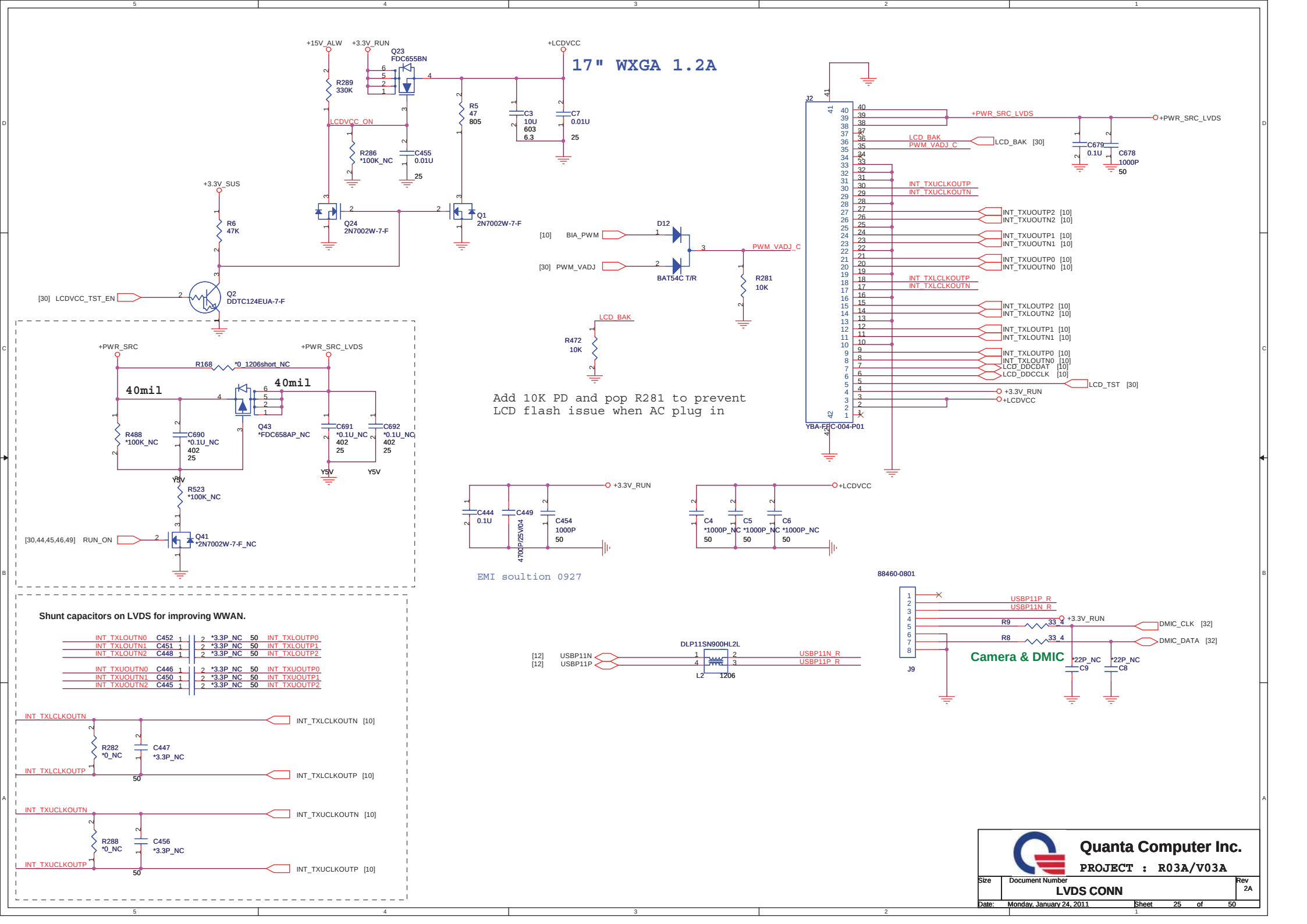
17" WXGA 1.2A
+15V_ALW
+3.3V_RUN
+LCDVCC
Q23
FDC655BN
R289
330K
LCDVCC_ON
R286
*100K_NC
C455
0.01U
25
R5
47
805
C3
10U
603
6.3
C7
0.01U
25
+3.3V_SUS
R6
47K
Q24
2N7002W-7-F
Q1
2N7002W-7-F
[30] LCDVCC_TST_EN
Q2
DDTC124EUA-7-F
[10] BIA_PWM
[30] PWM_VADJ
D12
BAT54C T/R
PWM_VADJ_C
R281
10K
LCD_BAK
R472
10K
Add 10K PD and pop R281 to prevent
LCD flash issue when AC plug in
J2
YBA-FFC-004-P01
+PWR_SRC_LVDS
LCD_BAK
PWM_VADJ_C
LCD_BAK [30]
C679
0.1U
C678
1000P
50
INT_TXUCLKOUTP
INT_TXUCLKOUTN
INT_TXUOUTP2 [10]
INT_TXUOUTN2 [10]
INT_TXUOUTP1 [10]
INT_TXUOUTN1 [10]
INT_TXUOUTP0 [10]
INT_TXUOUTN0 [10]
INT_TXLCLKOUTP
INT_TXLCLKOUTN
INT_TXLOUTP2 [10]
INT_TXLOUTN2 [10]
INT_TXLOUTP1 [10]
INT_TXLOUTN1 [10]
INT_TXLOUTP0 [10]
INT_TXLOUTN0 [10]
LCD_DDCDAT [10]
LCD_DDCCLK [10]
LCD_TST [30]
+3.3V_RUN
+LCDVCC
+PWR_SRC
+PWR_SRC_LVDS
R168
*0_1206short_NC
40mil
40mil
Q43
*FDC658AP_NC
R488
*100K_NC
C690
*0.1U_NC
402
25
C691
*0.1U_NC
402
25
C692
*0.1U_NC
402
25
Y5V
R523
*100K_NC
[30,44,45,46,49] RUN_ON
Q41
*2N7002W-7-F_NC
C444
0.1U
C449
4700P/25V/04
C454
1000P
50
C4
*1000P_NC
50
C5
*1000P_NC
50
C6
*1000P_NC
50
EMI soultion 0927
88460-0801
J9
USBP11P_R
USBP11N_R
R9
33_4
R8
33_4
+3.3V_RUN
DMIC_CLK [32]
DMIC_DATA [32]
Camera & DMIC
*22P_NC
C9
*22P_NC
C8
[12] USBP11N
[12] USBP11P
DLP11SN900HL2L
L2
1206
Shunt capacitors on LVDS for improving WWAN.
INT_TXLOUTN0 C452 *3.3P_NC 50 INT_TXLOUTP0
INT_TXLOUTN1 C451 *3.3P_NC 50 INT_TXLOUTP1
INT_TXLOUTN2 C448 *3.3P_NC 50 INT_TXLOUTP2
INT_TXUOUTN0 C446 *3.3P_NC 50 INT_TXUOUTP0
INT_TXUOUTN1 C450 *3.3P_NC 50 INT_TXUOUTP1
INT_TXUOUTN2 C445 *3.3P_NC 50 INT_TXUOUTP2
INT_TXLCLKOUTN
R282
*0_NC
C447
*3.3P_NC
INT_TXLCLKOUTP
50
INT_TXLCLKOUTN [10]
INT_TXLCLKOUTP [10]
INT_TXUCLKOUTN
R288
*0_NC
C456
*3.3P_NC
INT_TXUCLKOUTP
50
INT_TXUCLKOUTN [10]
INT_TXUCLKOUTP [10]
Quanta Computer Inc.
PROJECT : R03A/V03A
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LVDS CONN
Rev
2A
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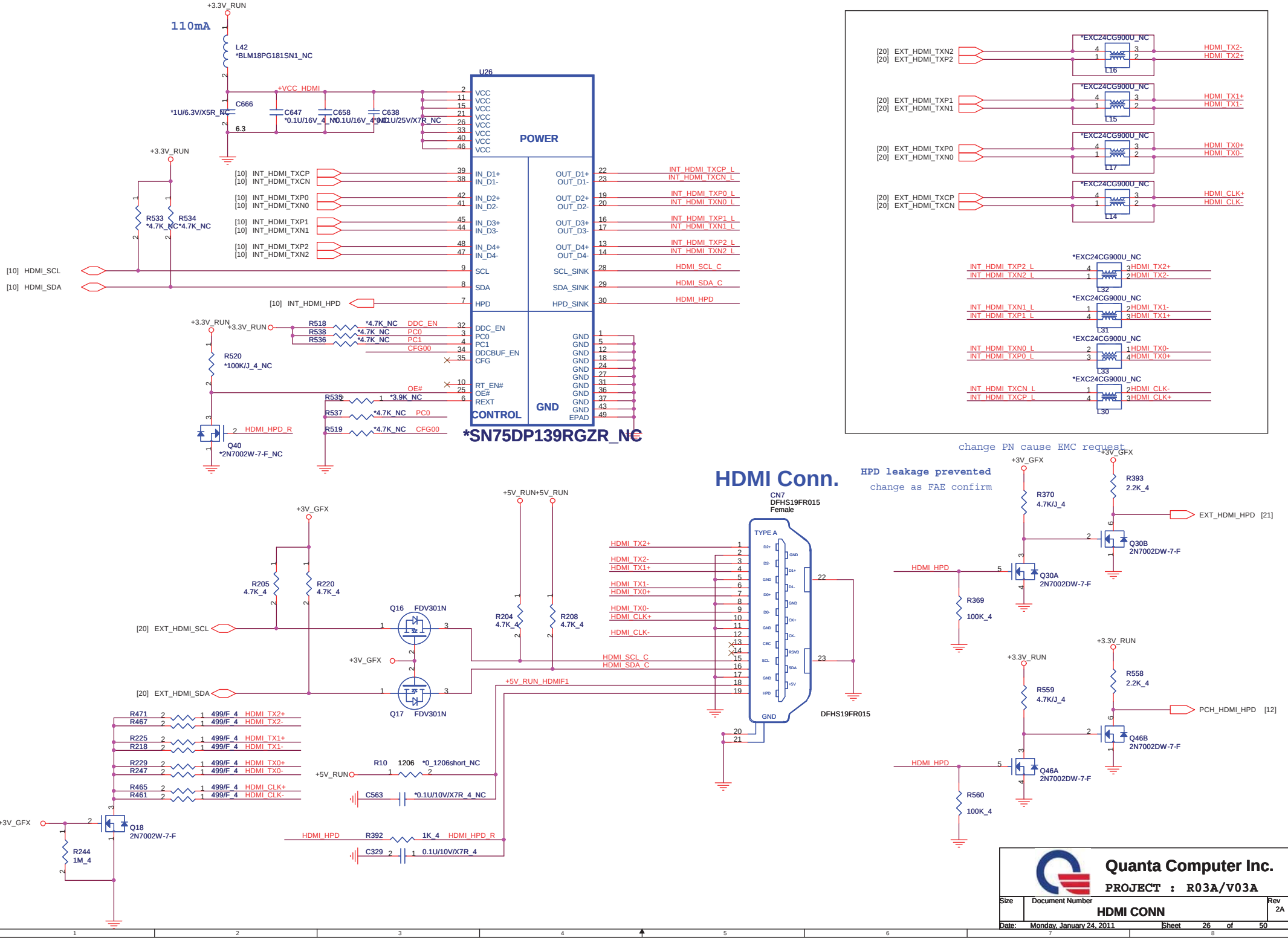
HDMI Conn.



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	HDMI CONN	2A
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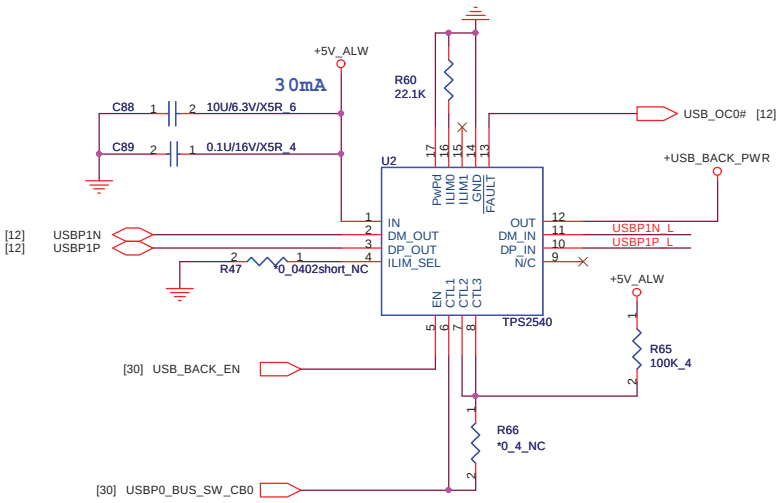
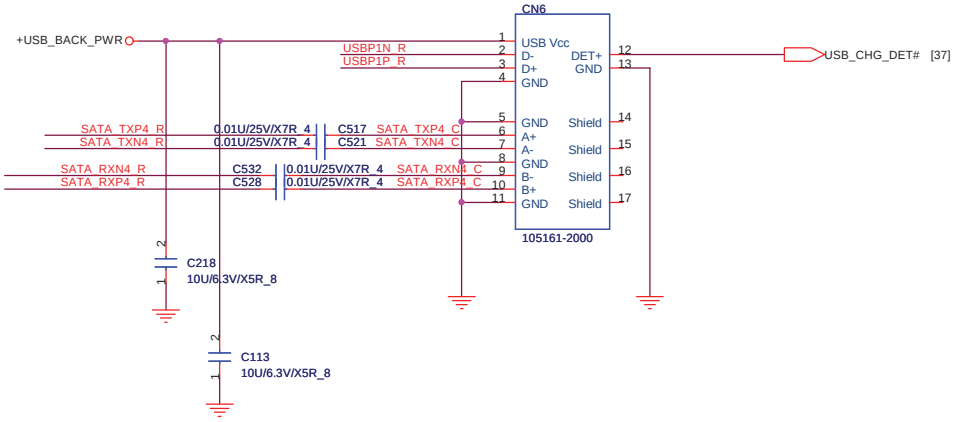
ESATA + USB Conn + Power share

S3/S5 USB charging circuit

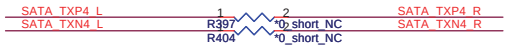


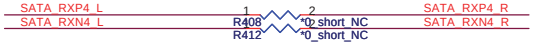


USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

ES(PG1.0): Stuff R66, Remove R65
MP(PG1.1): Remove R66 Stuff R65

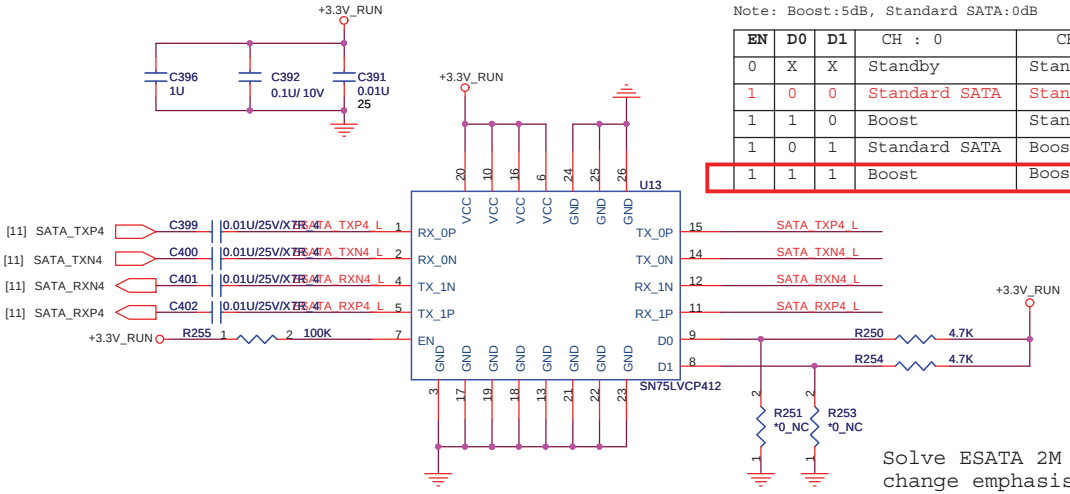
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now





E-SATA Re-driver

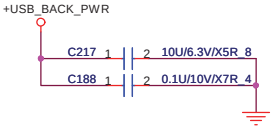
Layout Note: Please put those on the same side of MB PCB

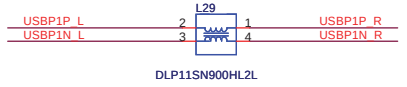


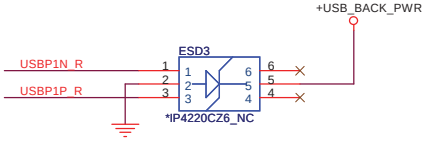
Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Solve ESATA 2M test fail issue, change emphasis setting







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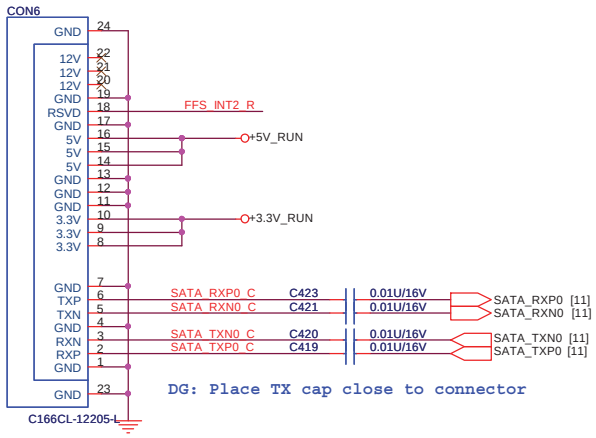
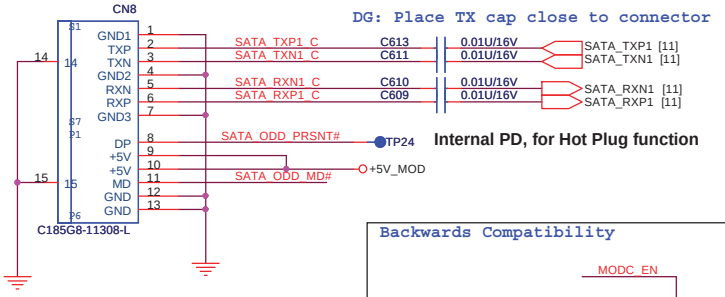
SATA Connector



ODD Connector

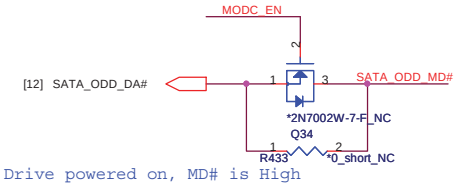
Change connector as ME request



DG: Place TX cap close to connector

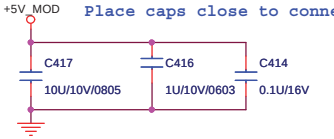
Internal PD, for Hot Plug function

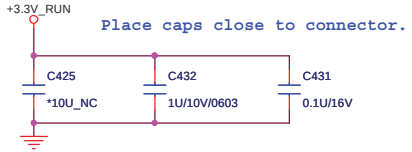
Backwards Compatibility

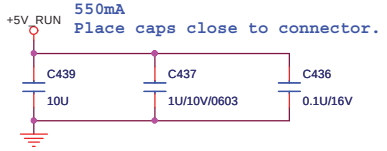


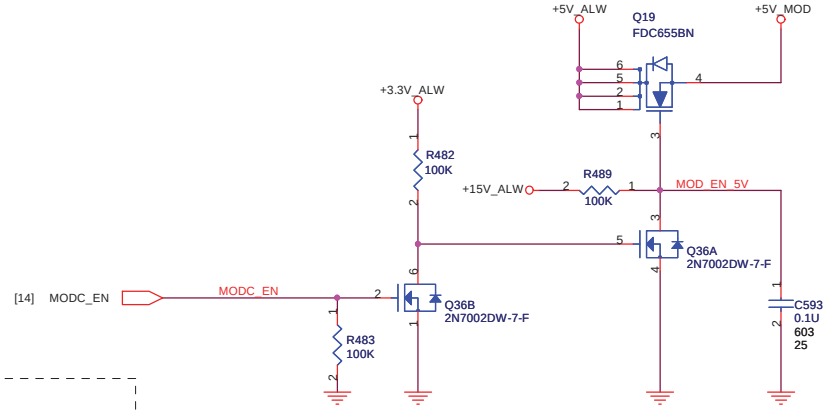
Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

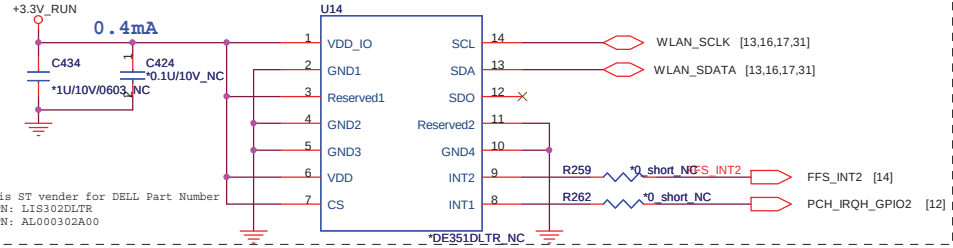




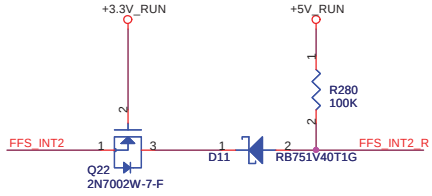




3-axis Fall Sensor (HDD data protector)



DE351DL is ST vender for DELL Part Number
Vender PN: LIS302DLTR
Quanta PN: AL000302A00



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	SATA HDD/ODD	2A

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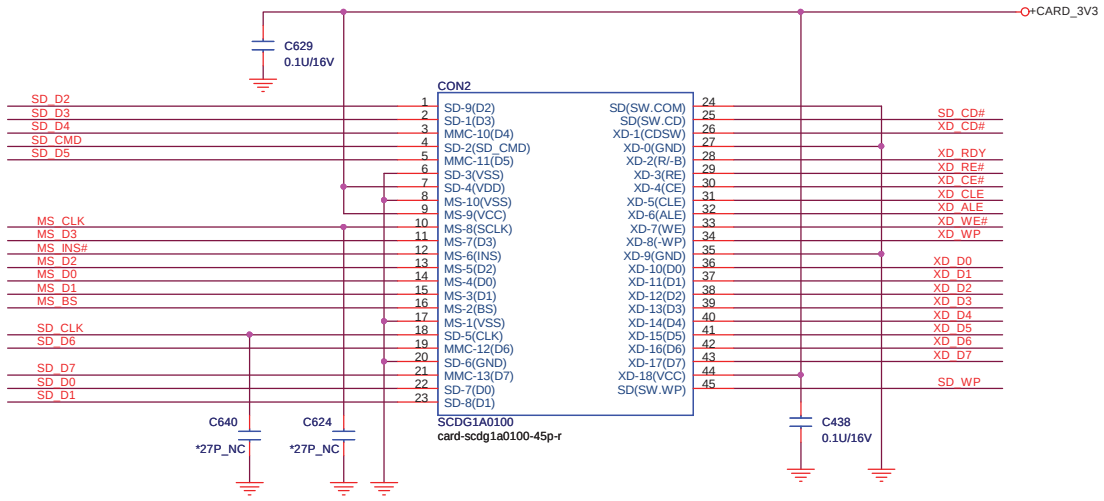
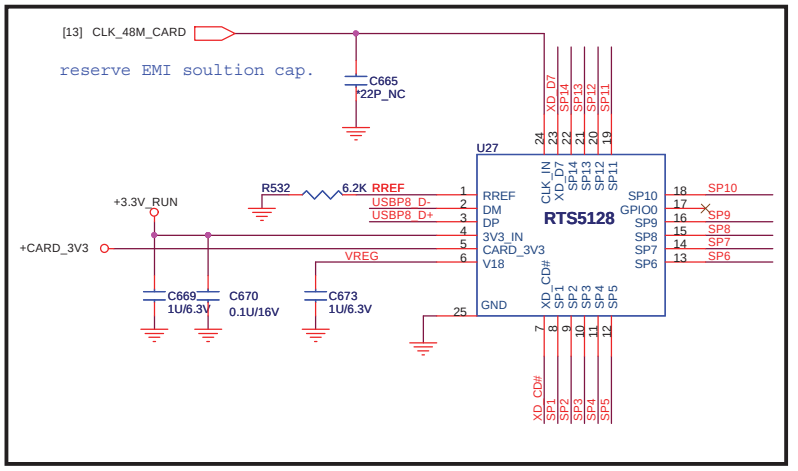
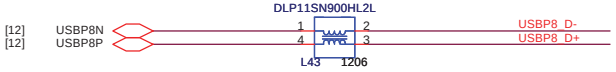
RTS5128-QFN24





SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	Cardreader (RTS5128)	2A

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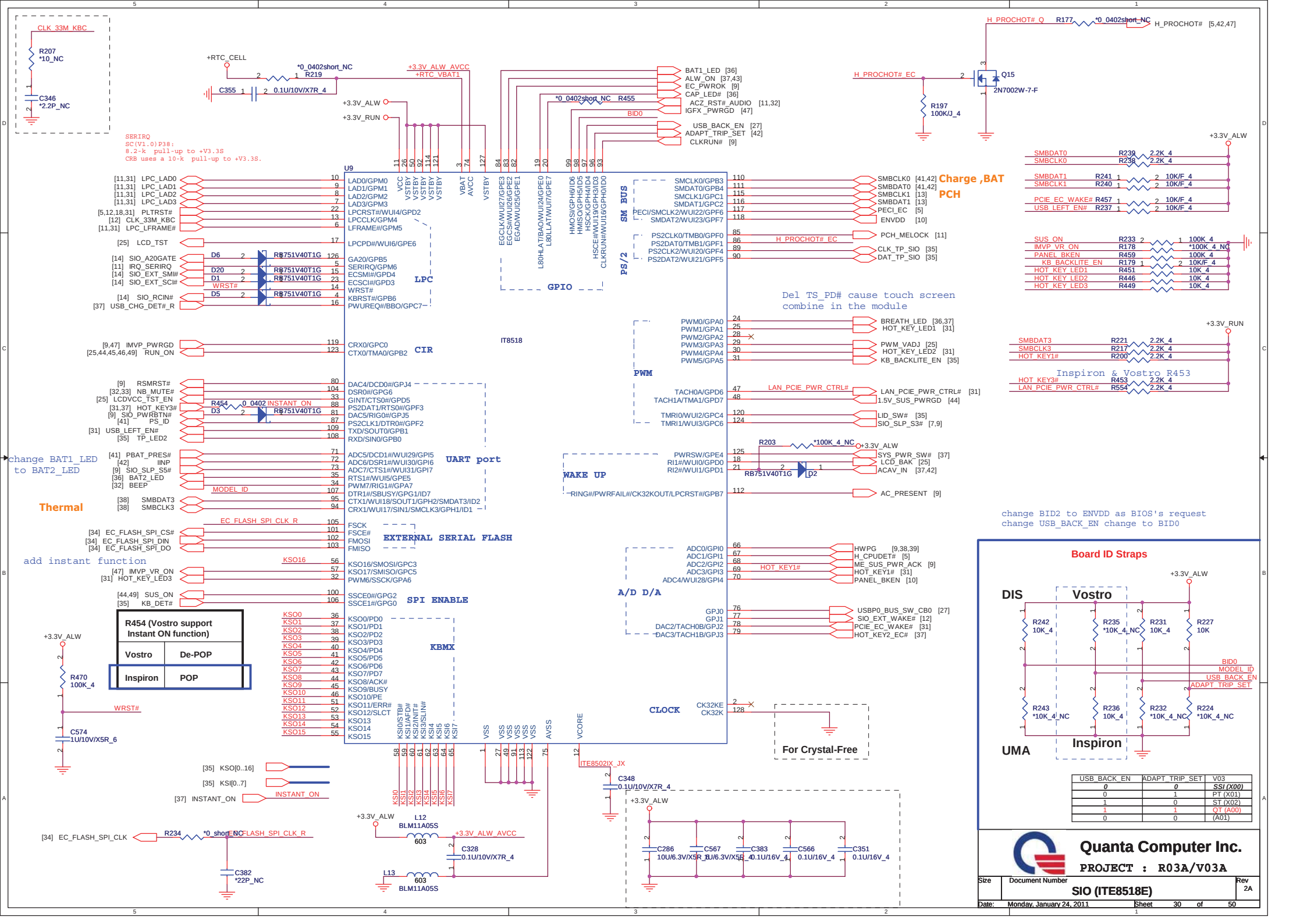
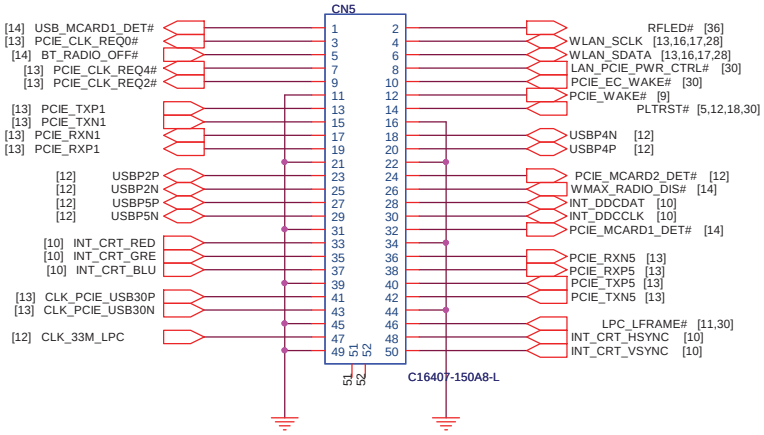
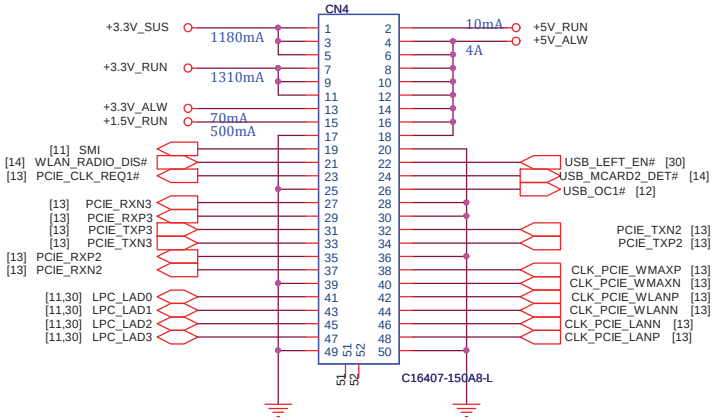
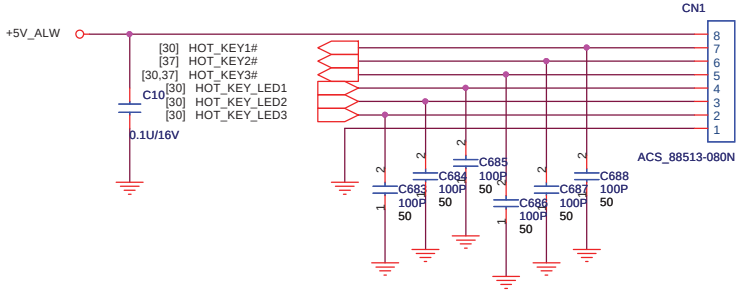

U9
IT8518
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT PCH
Del TS_PD# cause touch screen combine in the module
Inspiron & Vostro R453
change BAT1_LED to BAT2_LED
Thermal
add instant function
change BID2 to ENVDD as BIOS's request
change USB_BACK_EN change to BID0
SERIRQ
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.
R454 (Vostro support Instant ON function)
Vostro De-POP
Inspiron POP
Board ID Straps
DIS
Vostro
UMA
Inspiron
For Crystal-Free
Quanta Computer Inc.
PROJECT : R03A/V03A
SIO (ITE8518E)
Size
Document Number
Rev 2A
Date: Monday, January 24, 2011
Sheet 30 of 50

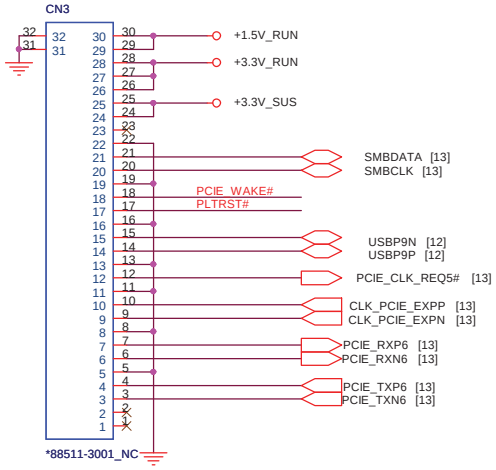




HOTKEY CON



MB to Express Card Board



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	SIO (ITE8518E)	2A

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*NOTE: ALC269_VB type add the LDO circuit in IC
VA type: PIN28 作爲MIC之偏壓
PIN31接A-GND

VB type: PIN31 作爲MIC之偏壓
PIN28接 作爲內部LDO
output 輸出濾波用

AVDD1, AVDD2 TYP=48mA

DVDD & DVDD-IO TYP=50mA

ALC269Q VB6

Analog Plane

Digital Plane

Int. Stereo Speakers
5V / 4 Ohm / 2W

HP JACKN
Normal Open
Pin5 & pin6 short when HP insert

MIC JACK
Normal Open
Pin5 & pin6 short when MIC insert

L34.L35,L36,L37,
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC

PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.

reverse Diode, and remove PD ckt

del 0ohm NC 0928

reserve EMI solution

please close to ALC269 Pin 28

must close to ALC269 Pin12

modify single net GND SIGNAL

Trace width >= 40mil, Trace length < 20cm

Reserve RC for EMI

Digital GND Analog GND
Tied at one point only under the
ALC269 or near the ALC269

Quanta Computer Inc.
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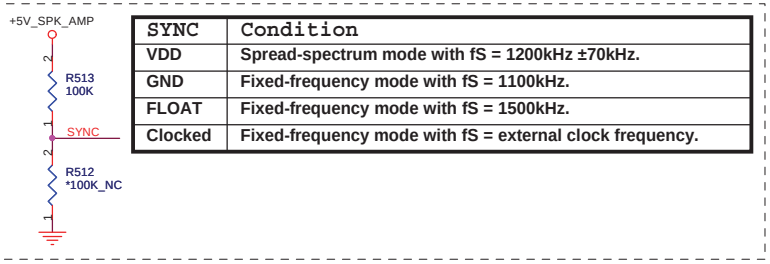
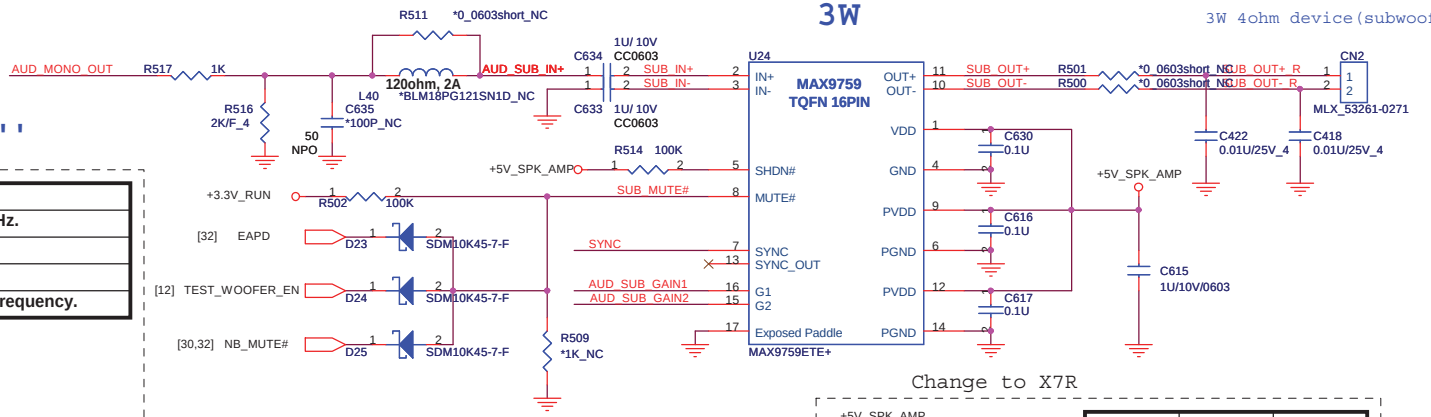
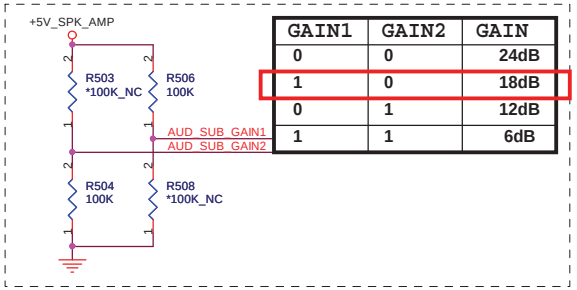
INTERNAL SUBWOOFER AMP Only for 17''

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

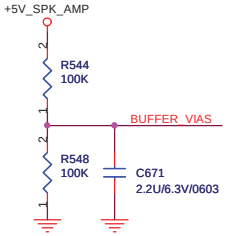


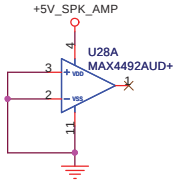


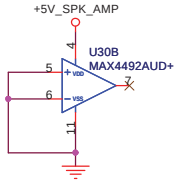
Change to X7R

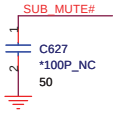


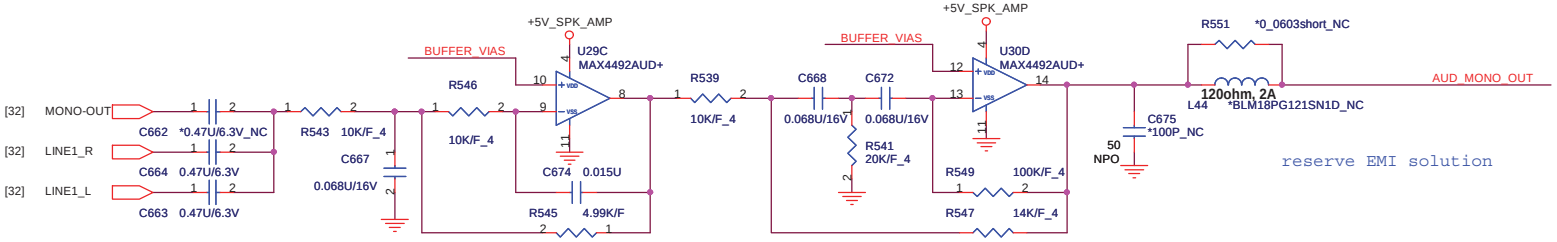
GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB





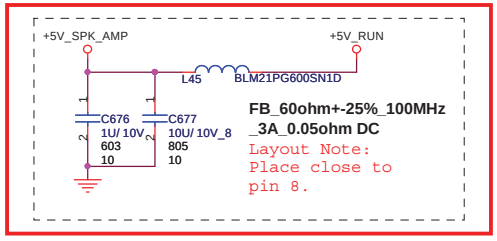






check modify to MONO-OUT PIN

reserve EMI solution



place close to connector side

Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	AUDIO CONN	2A

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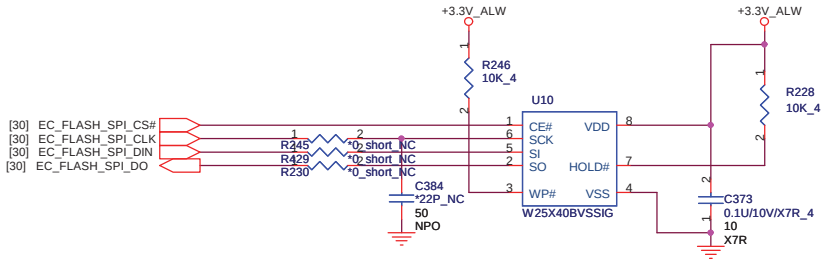
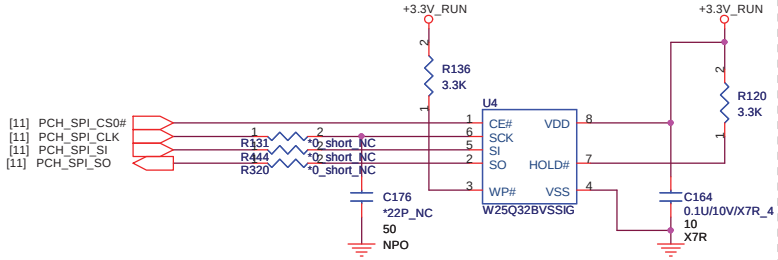
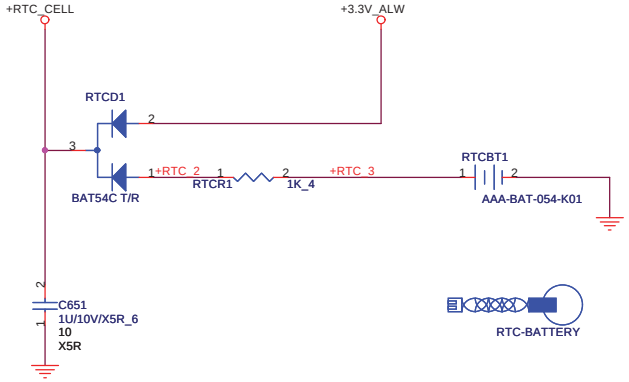
For EC 4Mbit (512K Byte)



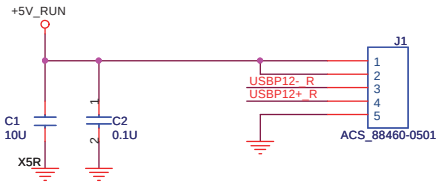
For PCH 32Mbit (4M Byte)



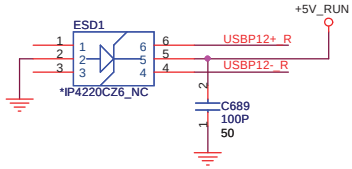
RTC



Touch Screen Module



Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



Quanta Computer Inc.		
PROJECT : R03A/V03A		
Size	Document Number: FLASH / RTC	Rev: 2A
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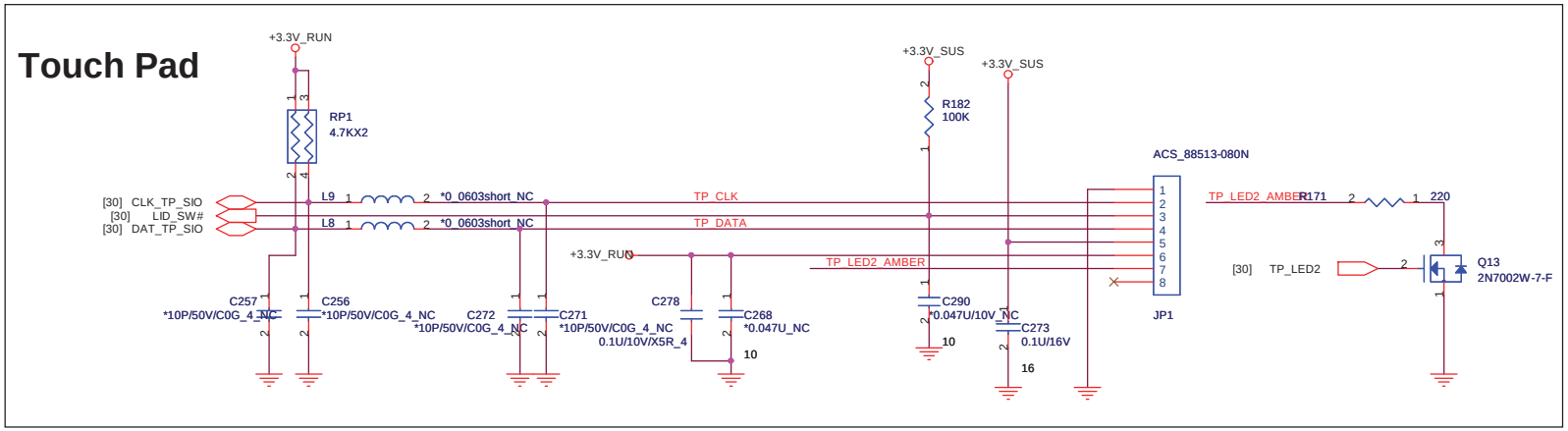
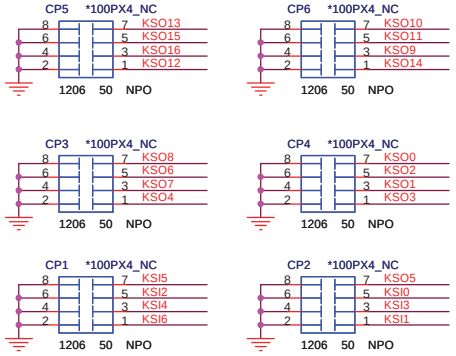
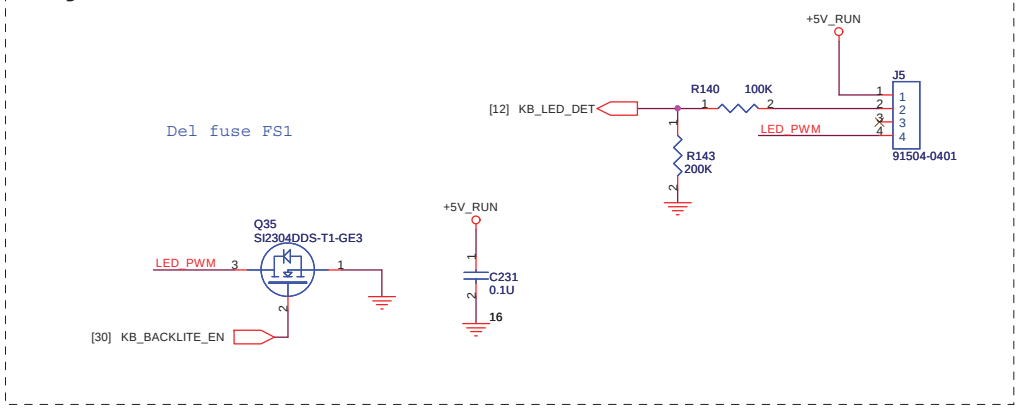
Touch Pad

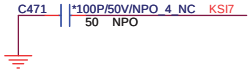




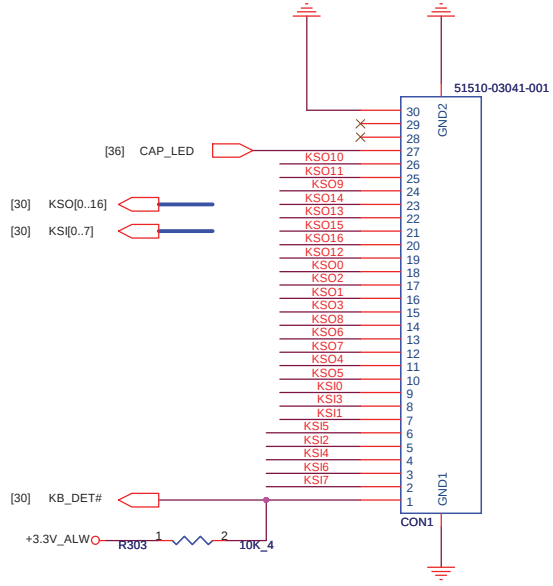
Key board illumination

+KB_LED power trace width >10 mil

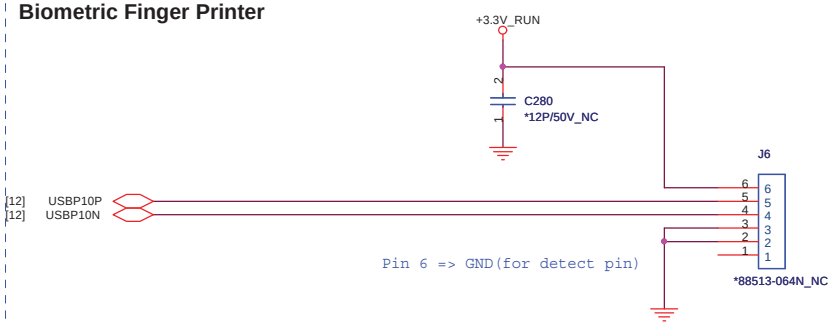




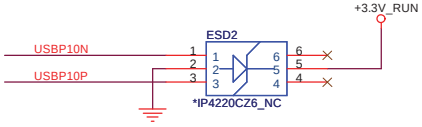
KEYBOARD CONNECTOR



Biometric Finger Printer



ESD by EMC request



Quanta Computer Inc.

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	TP / KB	2A

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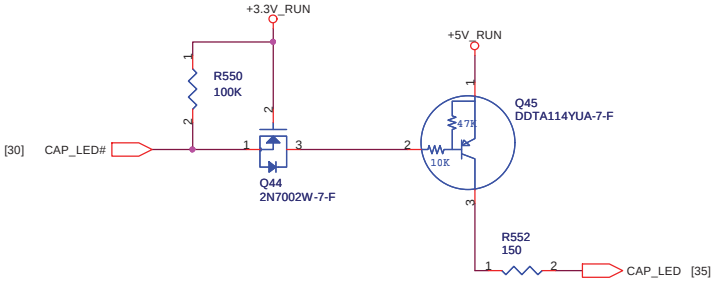
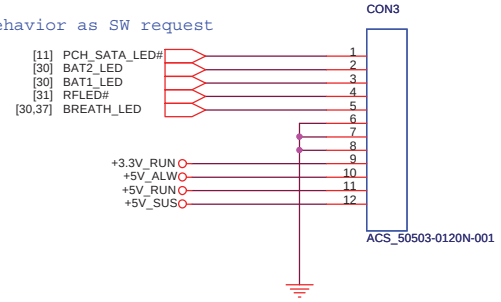
CAP lock LED



Check LED location and type

MB to LED Board conn

correct LED behavior as SW request



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	LED	2A

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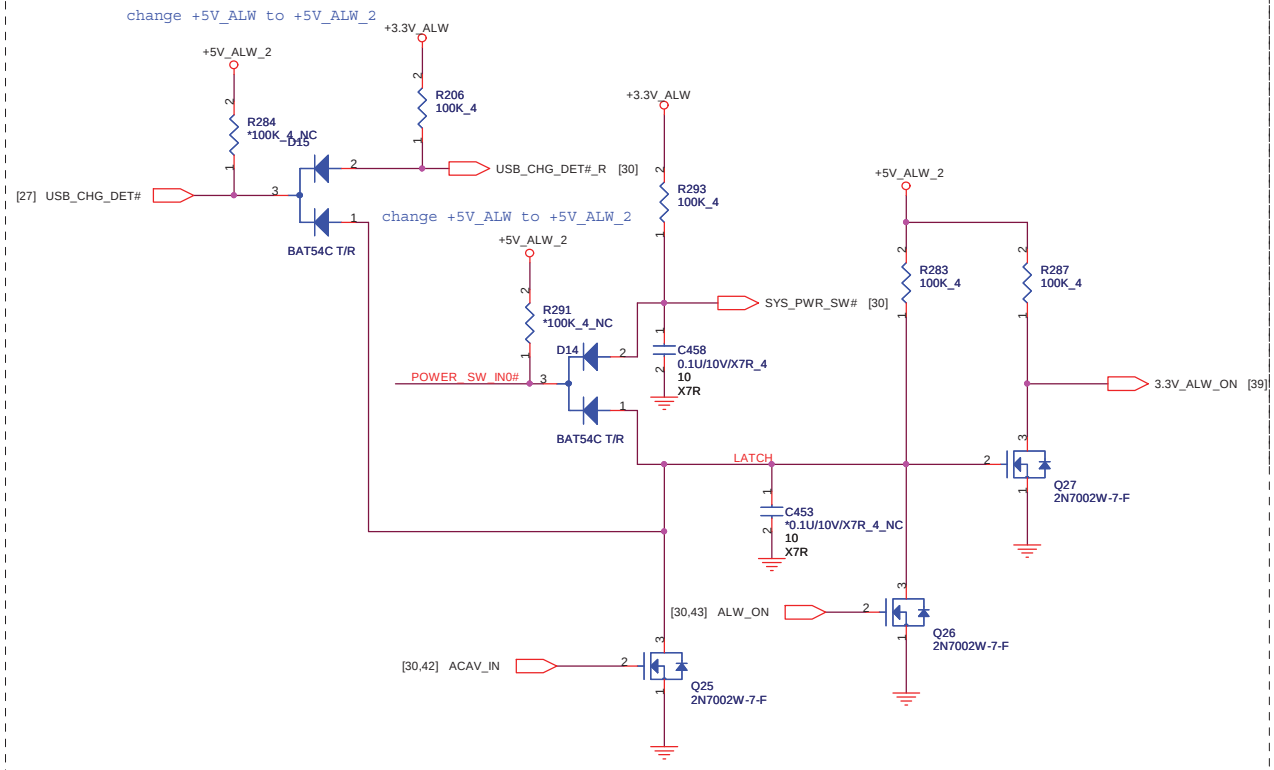
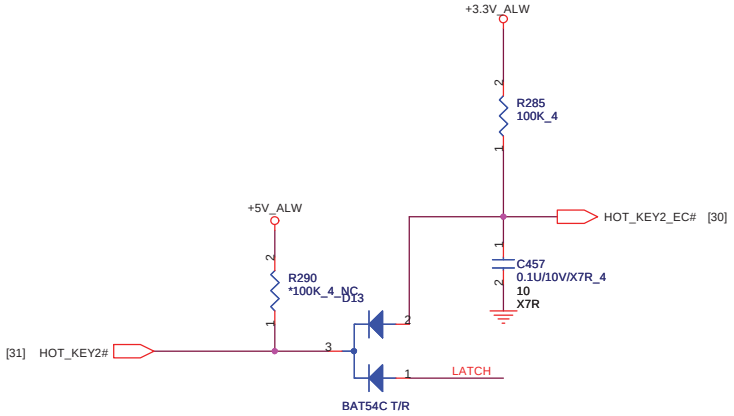
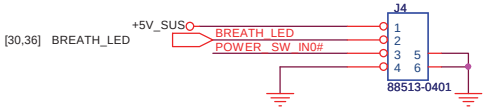
3VALW ON POWER LOGIC

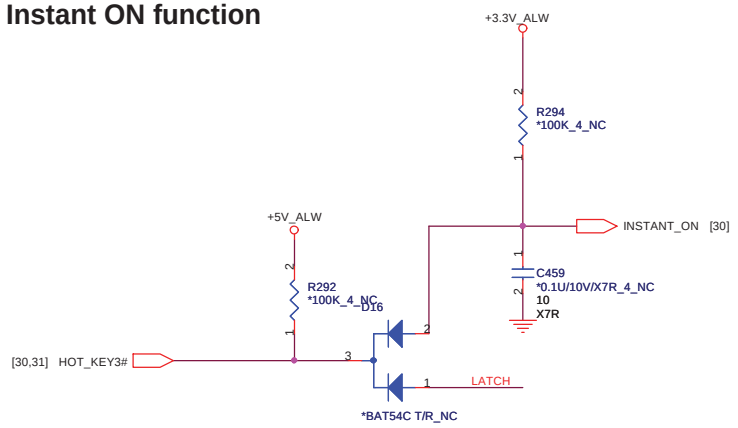




PWR button board form UM7



Instant ON function



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	PWR SW/LED	2A

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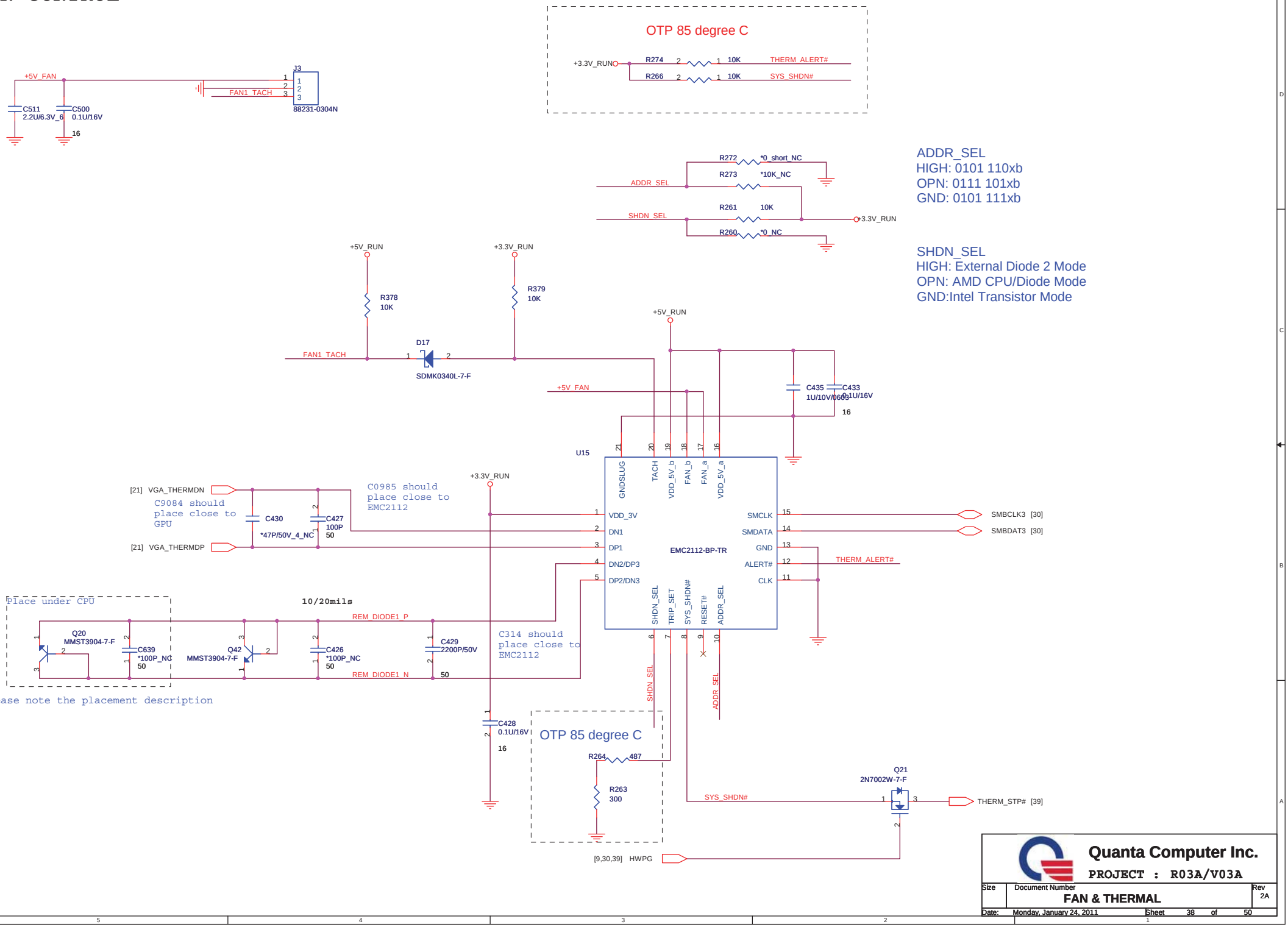
FAN CONTROL



Quanta Computer Inc.		
PROJECT : R03A/V03A		
Size	Document Number: FAN & THERMAL	Rev 2A
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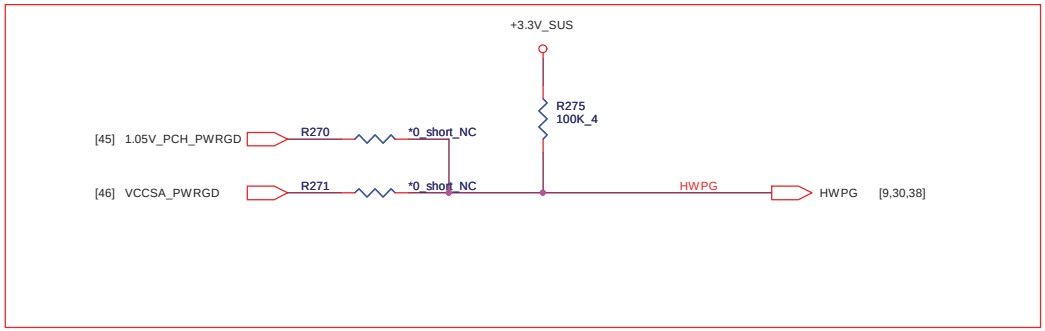

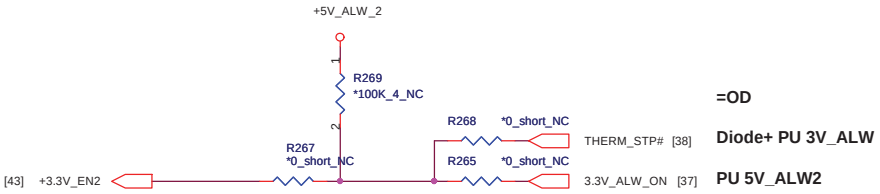

Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	System Reset Circuit	2A

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H2
H-TC236BC197D110P2
H-TC236BC197D110P2

H7
H-TC236BC197D110P2
H-TC236BC197D110P2

H14
h-tc335bc276d126p2
h-tc335bc276d126p2

H5
h-tc335bc276d126p2
h-tc335bc276d126p2

H8
h-c276d177p2
h-c276d177p2

H12
h-c276d126p2
h-c276d126p2

H19
H-C276IN130D110P2
H-C276IN130D110P2

H17
H-C276IN130D110P2
H-C276IN130D110P2

H16
h-c354d126p2
h-c354d126p2

H15
h-tsbc295d126p2
h-tsbc295d126p2

H13
H-C158D158N
H-C158D158N

H9
H-C158D158N
H-C158D158N

H23
h-c276d110pt
h-c276d110pt

add a new hole for layout request

CPU bracket

H10 Intel-cpu-bkt2
Intel-cpu-bkt2

H18
H-C142D142N
H-C142D142N

H20
h-c295d126p2
h-c295d126p2

H6
h-tc236bc197d102p2
h-tc236bc197d102p2

H11
h-tc236bc197d102p2
h-tc236bc197d102p2

H4
H-T236I130B276D110P2
H-T236I130B276D110P2

H24
H-TC276BC236D110P2
H-TC276BC236D110P2

H1
h-c142d142n
h-c142d142n

H3
h-tc335bc276d126p2
h-tc335bc276d126p2

Quanta Computer Inc.
PROJECT : R03A/V03A

Size	Document Number	Rev
	SCREW PAD	2A

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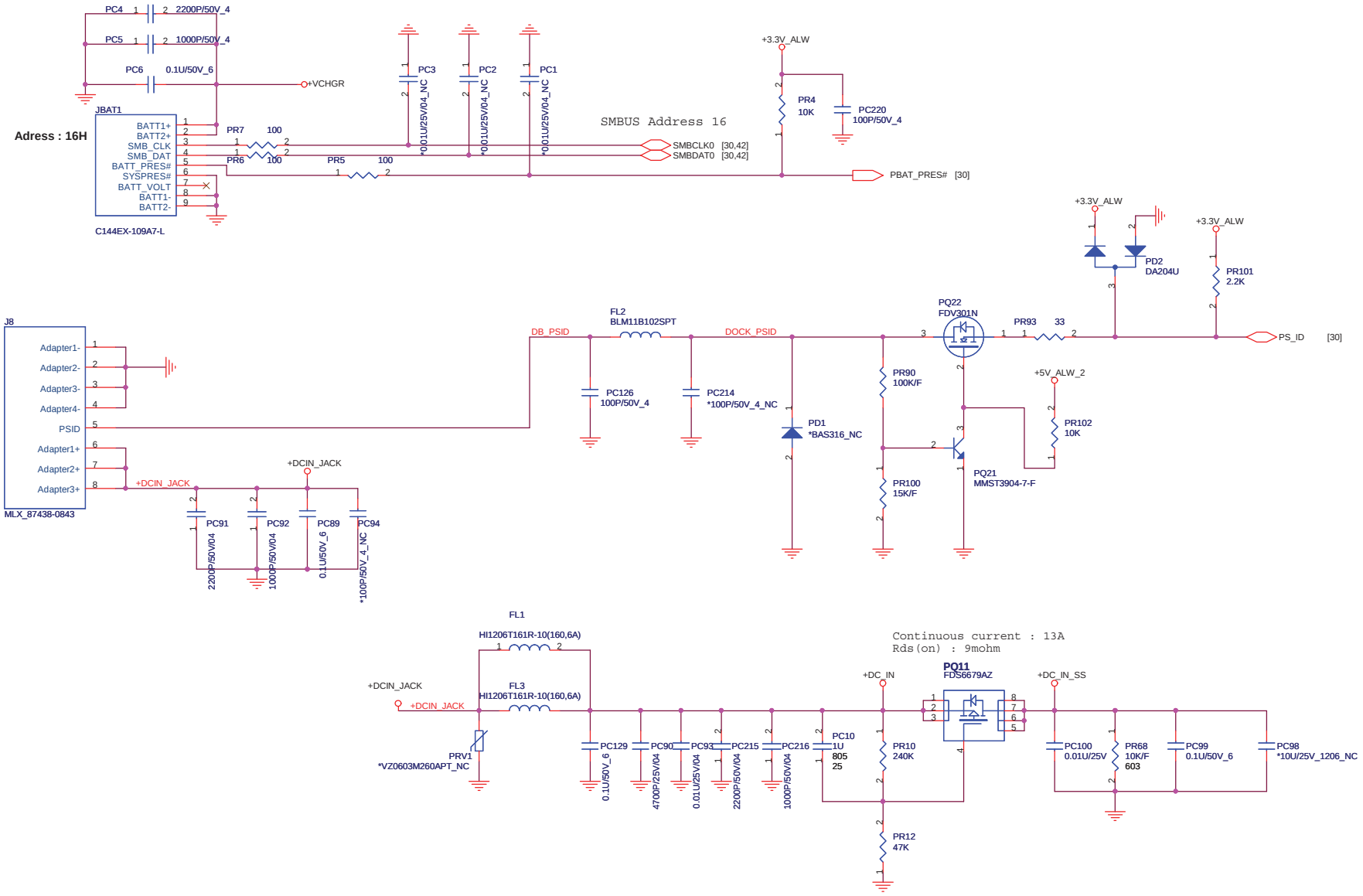
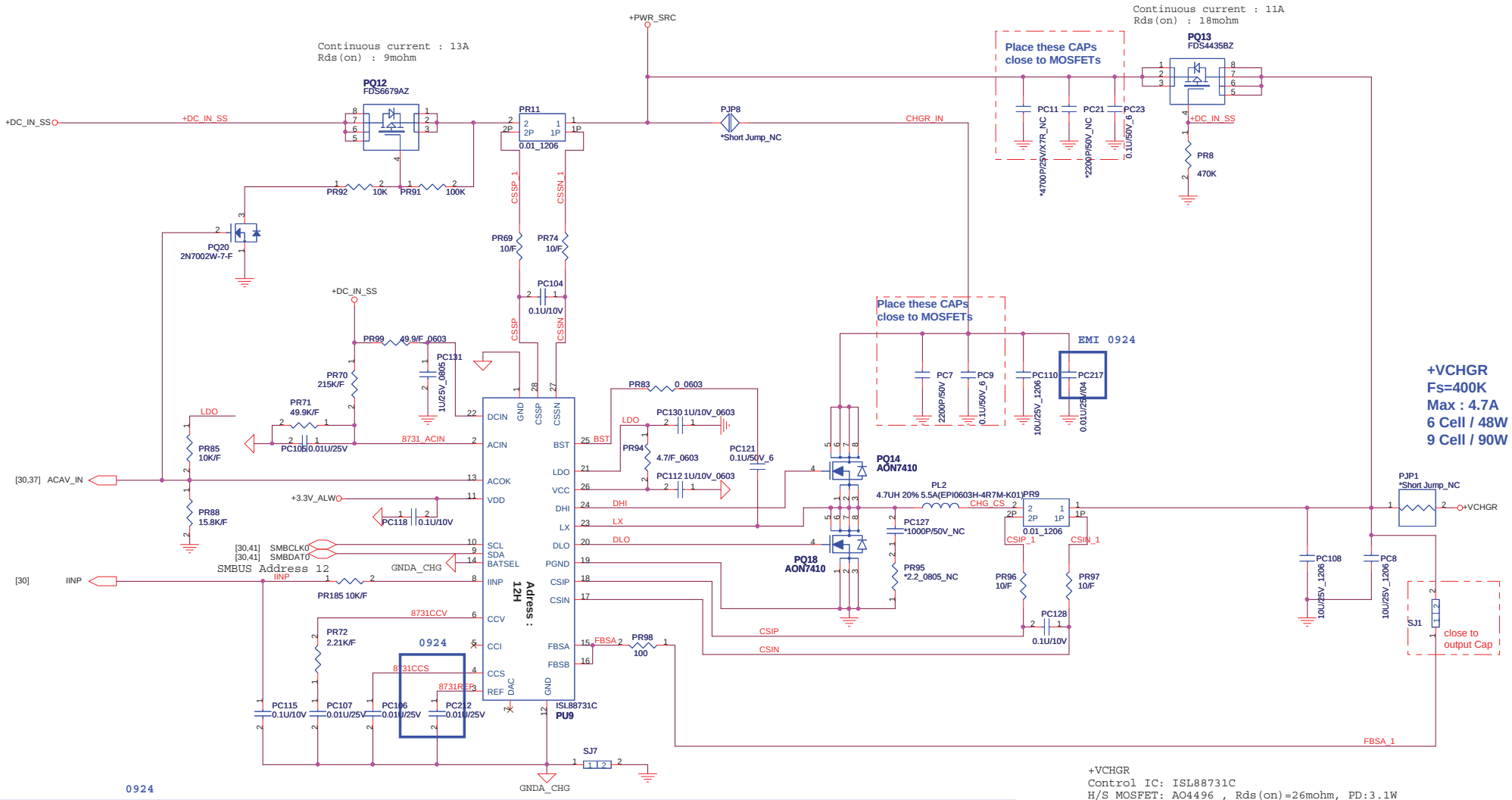
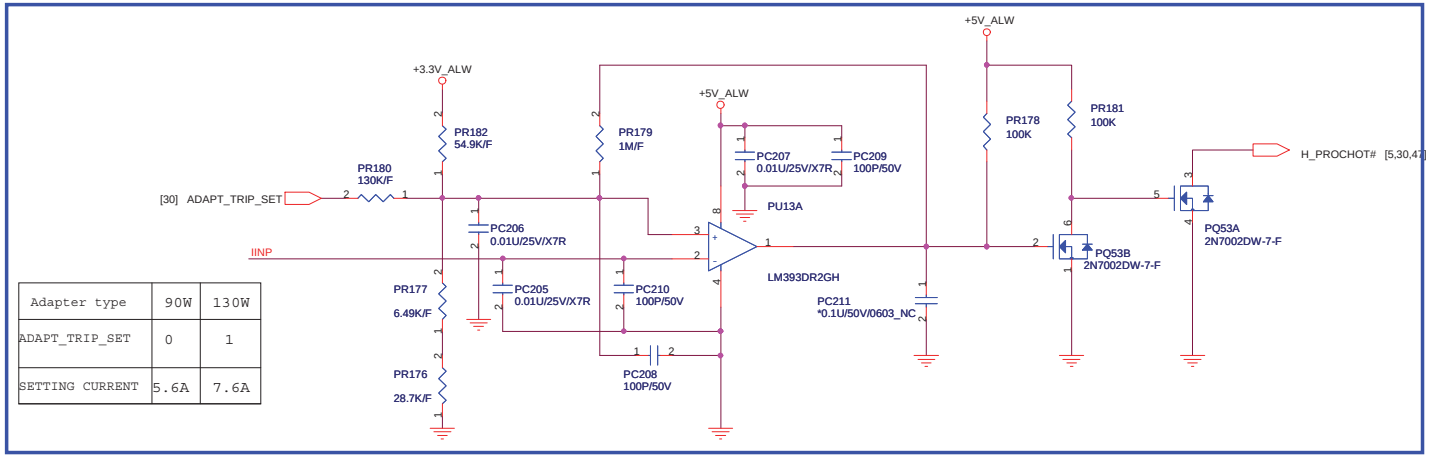


Quanta Computer Inc.		
PROJECT : R03A/V03A		
Size	Document Number	Rev
	DCIN,BATT CONNECTOR	2A
Date: Monday, January 24, 2011	Sheet 41 of 50	



+VCHGR
Control IC: ISL88731C
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 5.8UH +-30% 5.5A SDSL10D40F-5R8Y(TTA), DCR=22mohm
Output Cap: 2*10U 25V(+-10%,X6S,1206)

0924



Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

Quanta Computer Inc.
PROJECT : R03A/V03A

Size	Document Number	Rev
	Charger (ISL88731C)	2A

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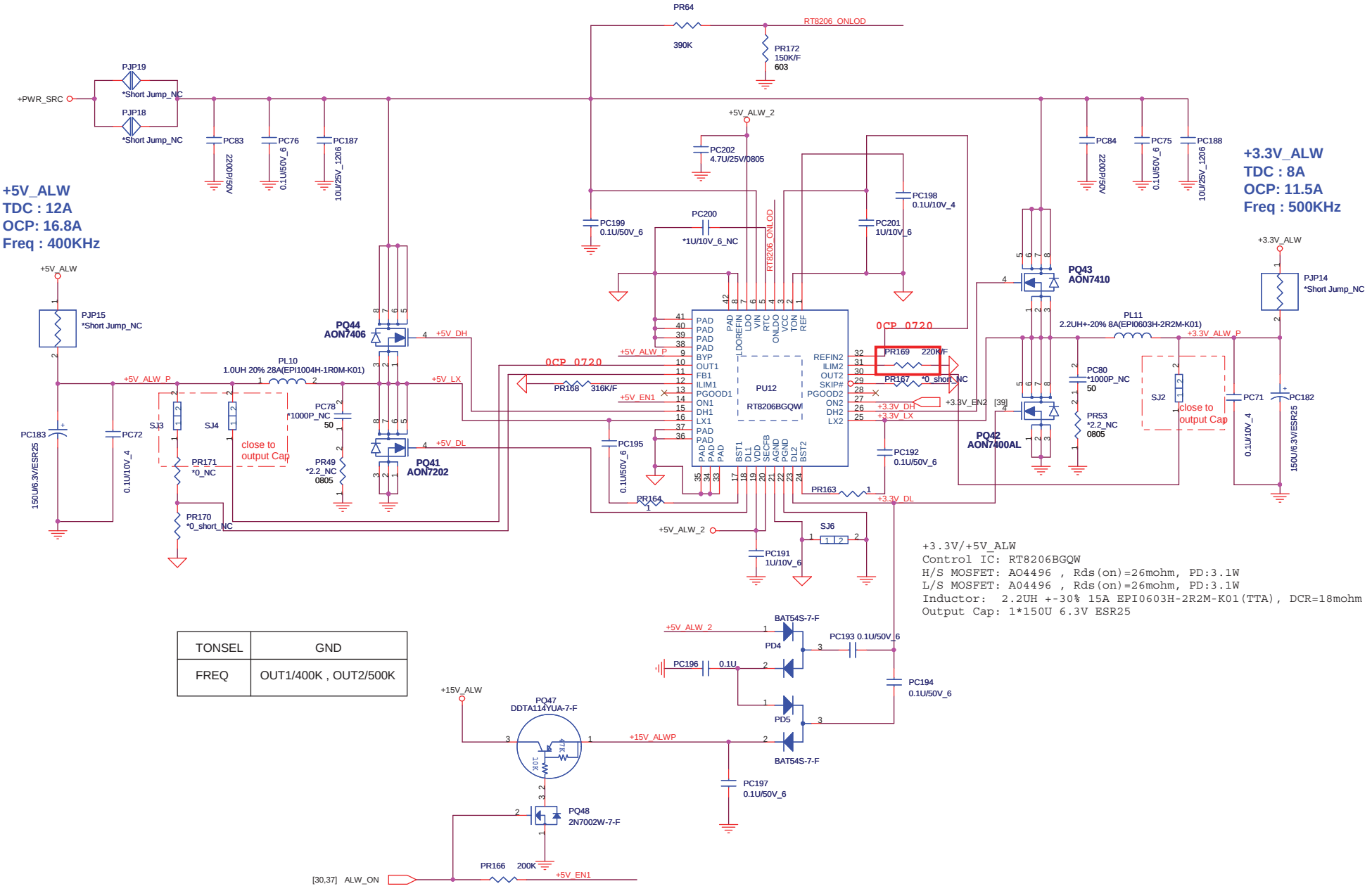
DC/DC +3V_ALW/+5V_ALW /+15V_ALW



TONSEL	GND
FREQ	OUT1/400K , OUT2/500K

Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206BGQW)	2A
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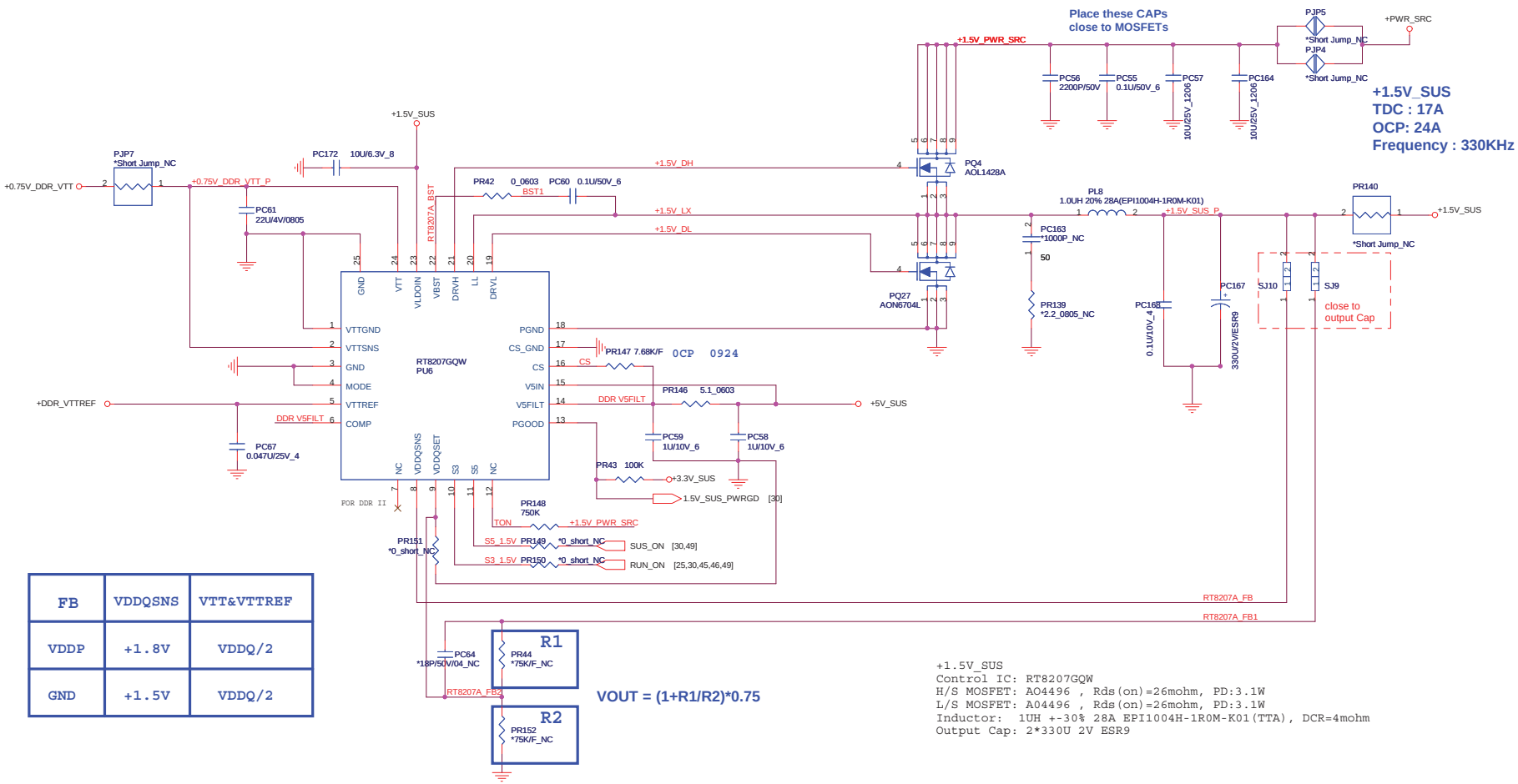

FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207GQW
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 2*330U 2V ESR9

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : R03A/V03A
Size | Document Number: DDR3 +1.5V_SUS(RT8207AGQW) | Rev 2A
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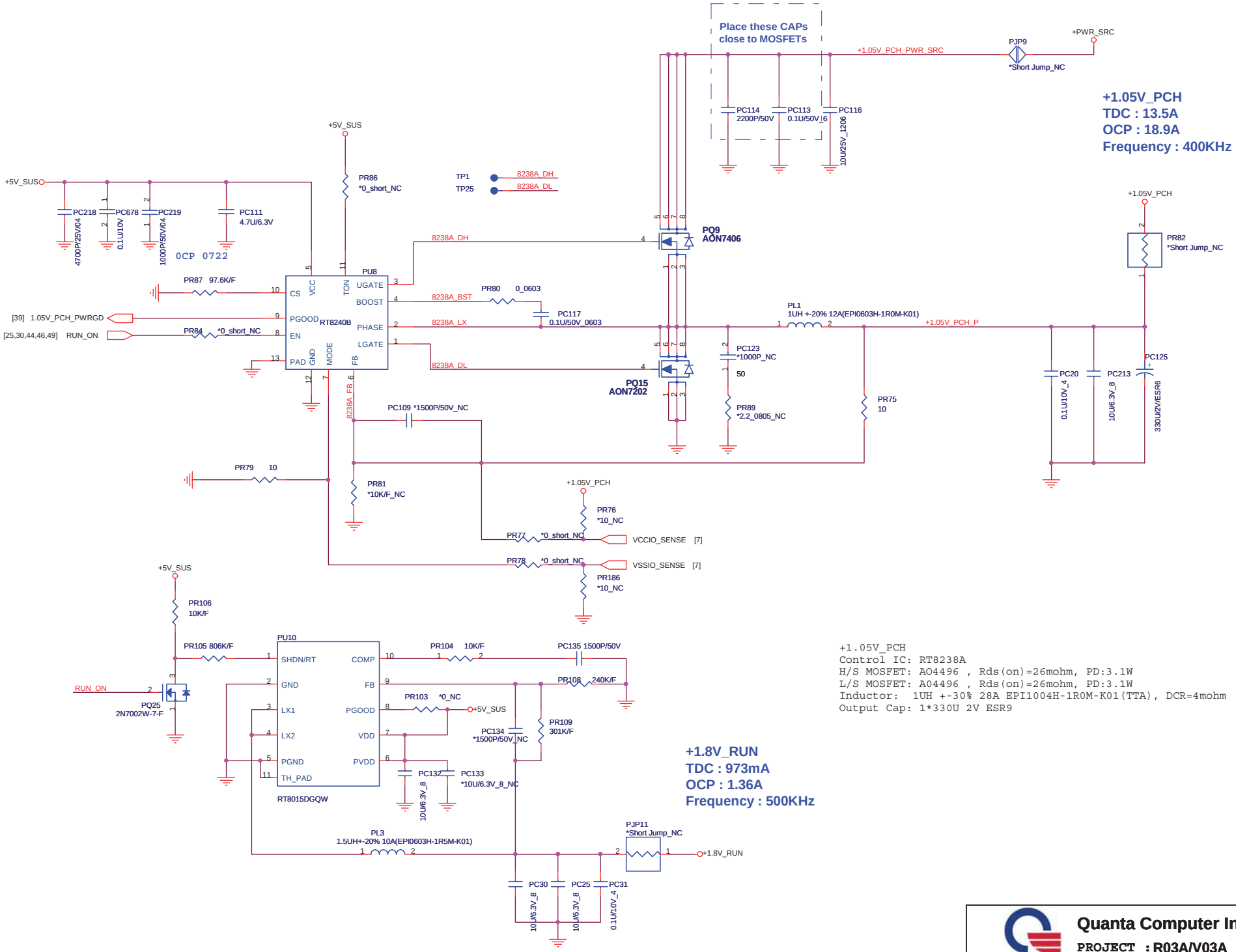
Place these CAPs close to MOSFETs
+1.05V_PCH_PWR_SRC
PJP9
*Short Jump_NC
+PWR_SRC
PC114 2200P/50V
PC113 0.1U/50V_6
PC116 10U/25V_1206
+1.05V_PCH
TDC : 13.5A
OCP : 18.9A
Frequency : 400KHz
+5V_SUS
PR86 *0_short_NC
TP1 8238A_DH
TP25 8238A_DL
PC218 4700P/25V/04
PC678 0.1U/10V
PC219 1000P/50V/04
PC111 4.7U/6.3V
OCP 0722
PU8
RT8240B
PR87 97.6K/F
PR80 0_0603
PC117 0.1U/50V_0603
[39] 1.05V_PCH_PWRGD
[25,30,44,46,49] RUN_ON
PR84 *0_short_NC
PQ9 AON7406
PQ15 AON7202
PL1 1UH +-20% 12A(EPI0603H-1R0M-K01)
+1.05V_PCH_P
PR82 *Short Jump_NC
PC123 *1000P_NC
50
PR89 *2.2_0805_NC
PR75 10
PC20 0.1U/10V_4
PC213 10U/6.3V_8
PC125 330U/2V/ESR6
PC109 *1500P/50V_NC
PR79 10
PR81 *10K/F_NC
PR76 *10_NC
PR77 *0_short_NC
VCCIO_SENSE [7]
PR78 *0_short_NC
VSSIO_SENSE [7]
PR186 *10_NC
PR106 10K/F
PR105 806K/F
PU10
RT8015DGQW
PR104 10K/F
PC135 1500P/50V
PR108 240K/F
RUN_ON
PQ25 2N7002W-7-F
PR103 *0_NC
PC134 *1500P/50V_NC
PR109 301K/F
PC132 10U/6.3V_8
PC133 *10U/6.3V_8_NC
PL3 1.5UH+-20% 10A(EPI0603H-1R5M-K01)
PJP11 *Short Jump_NC
+1.8V_RUN
PC30 10U/6.3V_8
PC25 10U/6.3V_8
PC31 0.1U/10V_4
+1.8V_RUN
TDC : 973mA
OCP : 1.36A
Frequency : 500KHz
+1.05V_PCH
Control IC: RT8238A
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 1*330U 2V ESR9
Quanta Computer Inc.
PROJECT : R03A/V03A
Size
Document Number
+1.05V_PCH(RT8209A)
Rev 2A
Date: Monday, January 24, 2011
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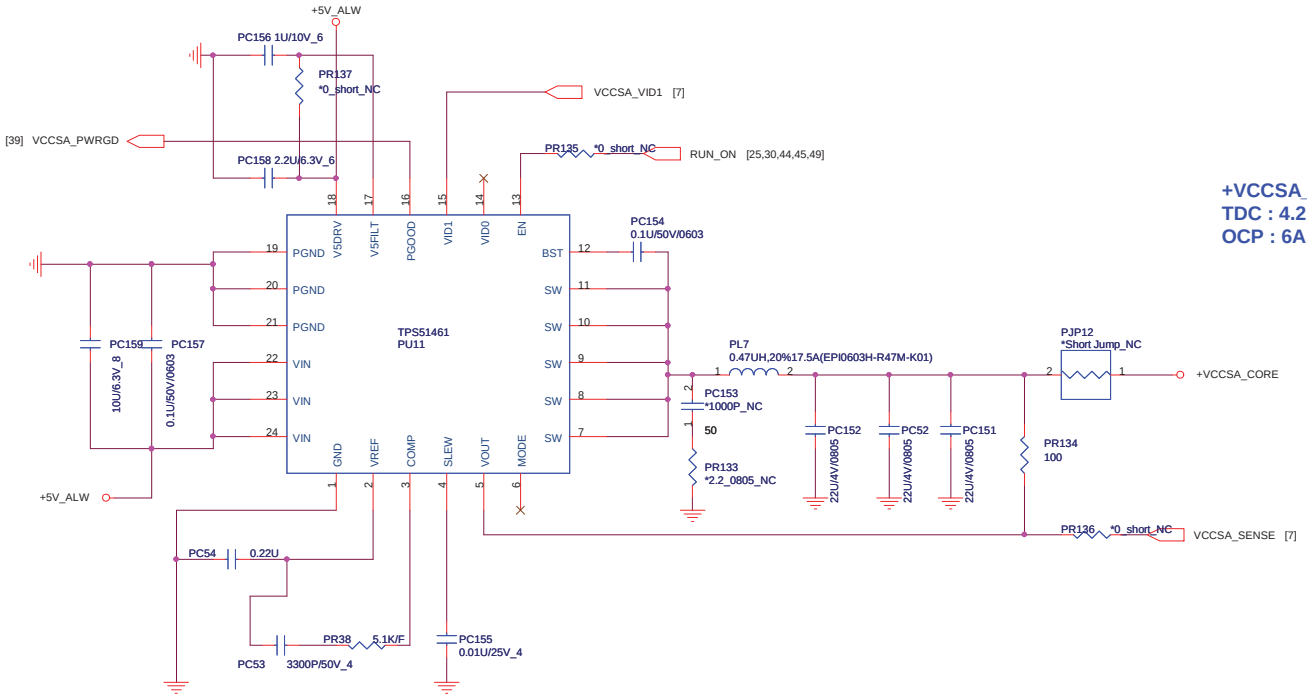

+VCCSA_CORE
TDC : 4.2A
OCP : 6A

+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low

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Size	Document Number	Rev
	VCCSA (TPS51461)	2A

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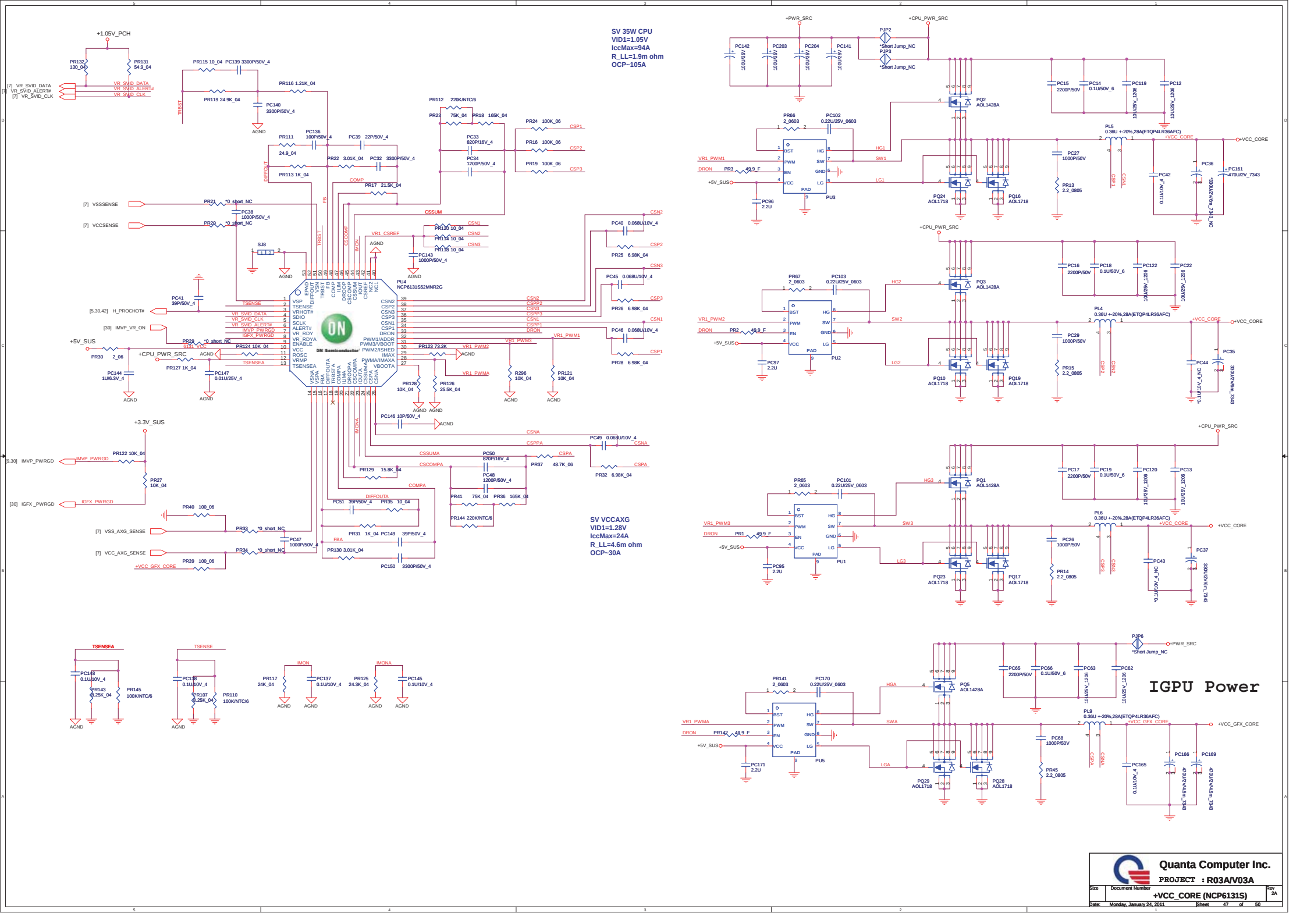
SV 35W CPU
VID1=1.05V
IccMax=94A
R_LL=1.9m ohm
OCP~105A
SV VCCAXG
VID1=1.28V
IccMax=24A
R_LL=4.6m ohm
OCP~30A
IGPU Power
+1.05V_PCH
+3.3V_SUS
+5V_SUS
+CPU_PWR_SRC
+PWR_SRC
+VCC_CORE
+VCC_GFX_CORE
PU4 NCP6131S52MNR2G
PU1 PU2 PU3 PU5
PQ1 PQ2 PQ3 PQ4 PQ5
PL4 PL5 PL6 PL9
TSENSEA
TSENSE
IMON
IMONA
Quanta Computer Inc.
PROJECT : R03A/V03A
+VCC_CORE (NCP6131S)
Monday, January 24, 2011
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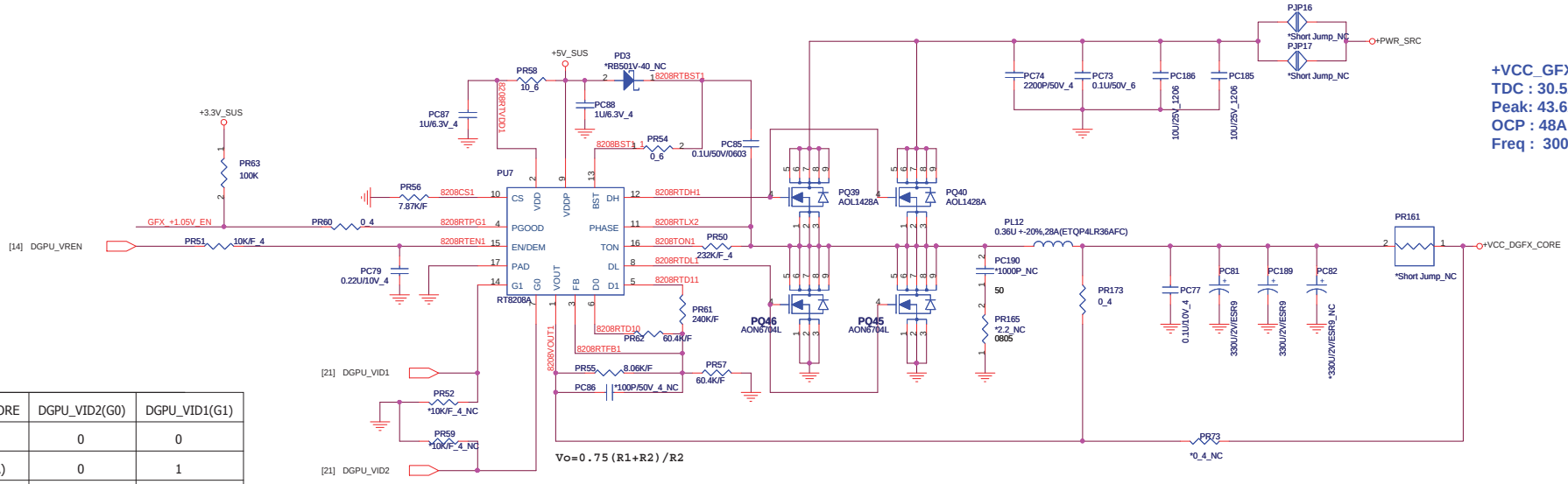
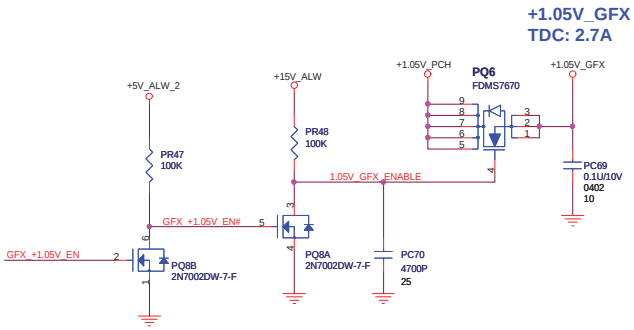
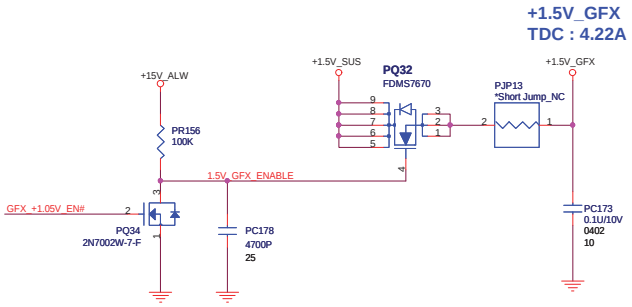
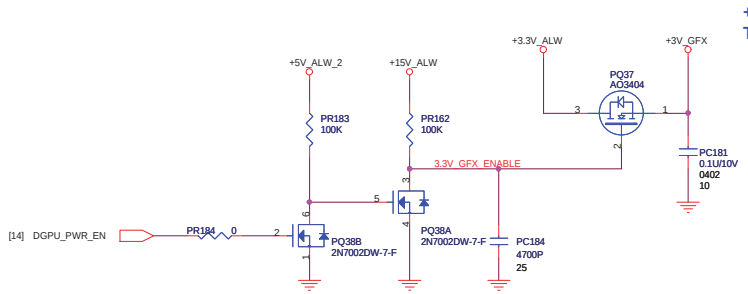


+VCC_DGFX_CORE	DGPU_VID2(G0)	DGPU_VID1(G1)
0.85V	0	0
0.875V(NA)	0	1
0.95 V	1	0
0.975V	1	1

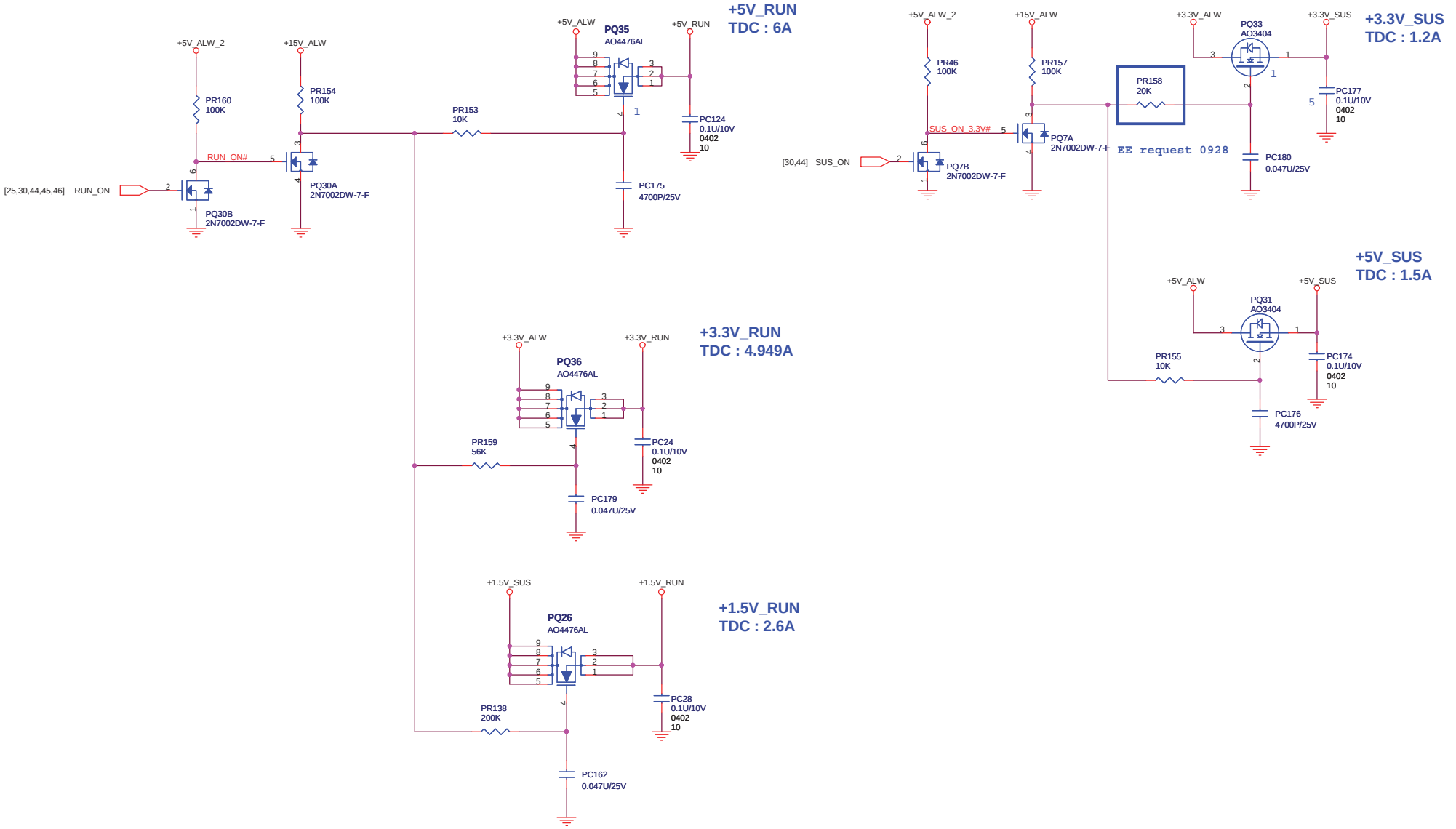
+VCC_GFX_CORE
Control IC: RT8208A
H/S MOSFET: FDMS7692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS0308S(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.36UH 20% 28A(EPI1004H-1R0M-K01)(TTA), DCR=2.8mohm
Output Cap: 2*330U,2.5V(20%,105C,3528),ESR=9mohm







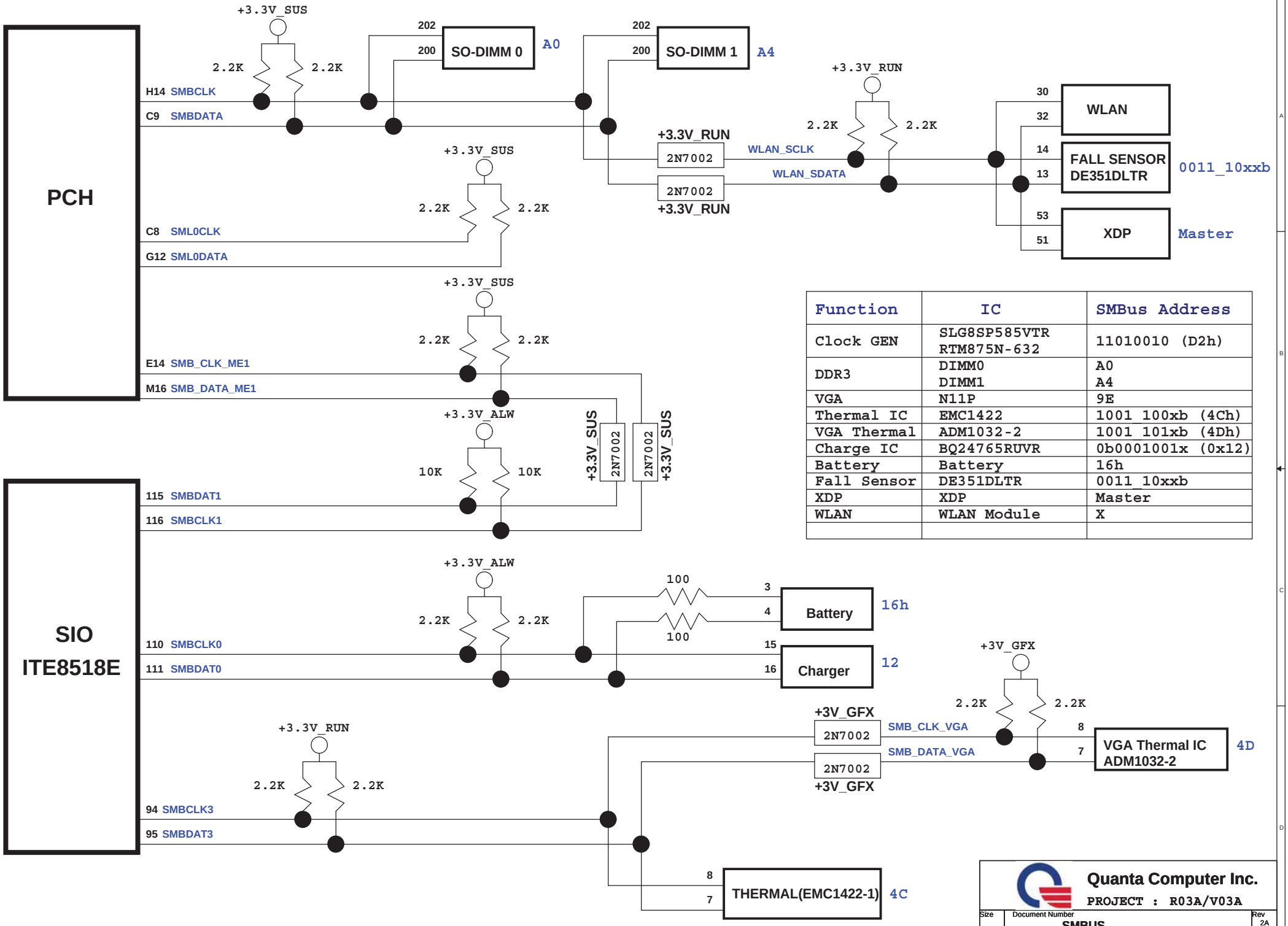
Quanta Computer Inc.
PROJECT : R03A/V03A
Size | Document Number: VGA power (RT8208A) | Rev 2A
Date: Monday, January 24, 2011 | Sheet 48 of 50



Quanta Computer Inc.

PROJECT : R03A/V03A

Size	Document Number	Rev
	RUN / SUS POWER SW	2A
Date: Monday, January 24, 2011	Sheet 49 of 50	



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001 100xb (4Ch)
VGA Thermal	ADM1032-2	1001 101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

Quanta Computer Inc.
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Size	Document Number	Rev
	SMBUS	2A

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