PCB STACK UP

6L DIS

R03/V03 UMA BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : BOT

DDRIII-SODIMM1
A 00 PAGE 16

DDRIII-SODIMM2
A 01 PAGE 17

DDRIII 1333 MT/s

DDRIII 1333 MT/s

CPU
Sandy Bridge 45W
PGA 989
PAGE 4~8

FDI LINK
2.5GT /s

DMI LINK
2.5GT /s

INT HDMI

HDMI Switch PAGE 19

HDMI CONN PAGE 19

INT Dual CHANNEL LVDS

LCD CONN
1600 x 900 (HD) PAGE 18

iGFX Interfaces

Re-Driver
SN75LVCP412RTJR
PAGE 20

E-SATA PAGE 20

SATA4 300MB /S

SATA -HDD PAGE 21

SATA0 300MB /S

ODD PAGE 21

SATA1 300MB /S

3-axis Fall Sensor PAGE 21

SMBUS

Mobile Intel
Series 6 Chipset

PCH

HM67
Couger Point

BGA 989
25 mm X 25 mm

PAGE 9~15

ESATA+USB2.0 PAGE 20

Camera PAGE 18

Card Reader
RTS5128-GR PAGE 22

FP PAGE 28

Touch Screen PAGE 27

USB2.0

USB[0] USB[11] USB[8] USB[10] USB[12]

USB[8]

Express Card
R5538D001 PAGE 02

EXP Board

CRT Board PAGE 03

IO Board

USB[4] USB[5] PCIE[3]

WLAN PAGE 05

WiMAX PAGE 04

USB3.0 Controller PAGE 06

LED Board

PCIE[1] PCIE[2]

PCIE[5]

BlueTooth PAGE 05

USB3.0 Ports x2 PAGE 07

PB Board

LAN
Realtek
RTL8111E-VB-GR
PAGE 09

USB[6]

USB Port x1 PAGE 08

TP Board

RJ45 PAGE 10

USB[2]

HotKey Board

25MHz

32.768KHz

Keyboard Conn. PAGE 28

Touch Pad PAGE 28

LED PAGE 29

KBC
ITE 8518
PAGE 23

LPC

PWM FAN &Thermal PAGE 31

SPI ROM 512kB PAGE 27

SPI

SPI ROM 4MB PAGE 27

25MHz

32.768KHz

IHDA

Audio Codec
ALC 269Q-VB6-GR
PAGE 25

Subwoofer
MAX9759ETE
PAGE 26

Speaker PAGE 25

Jack X2 PAGE 25

Digital-MIC PAGE 25

Charger PAGE 35

3/5V PAGE 36

1.5V_SUS/0.75V_DDR PAGE 37

Batt/DC-IN PAGE 34

1.05V_PCH PAGE 38

VCCSA PAGE 39

CPU_CORE PAGE 40

1.8V_RUN PAGE 38

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	BLOCK DIAGRAM	2A

Date: Wednesday, October 06, 2010 Sheet 1 of 42

power / State	+RTC_CELL	+DC_IN +DC_IN_SS +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+VCHGR +PWR_SRC +5V_ALW_2 +3.3V_ALW +5V_ALW +15V_ALW +3.3V_LAN (for V03)	+5V_SUS +3.3V_SUS +1.5V_SUS +1.5V_CPU +DDR_VTTREF +3.3V_LAN (for R03)	+VCC_CORE +1.05V_PCH +5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +VCCSA +0.75V_DDR_VTT +LCDVCC +VCC_GFX_CORE	
S0	ON	ON	ON	ON	ON	
S1						
S3	ON	ON	ON	ON	OFF	
S4/S5 AC	ON	ON				
S4/S5 DC Only	ON		ON	OFF	OFF	
AC/DC No Exist	ON	OFF	OFF	OFF	OFF	

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Power Rails	2A

Date: Wednesday, October 27, 2010 Sheet 2 of 42

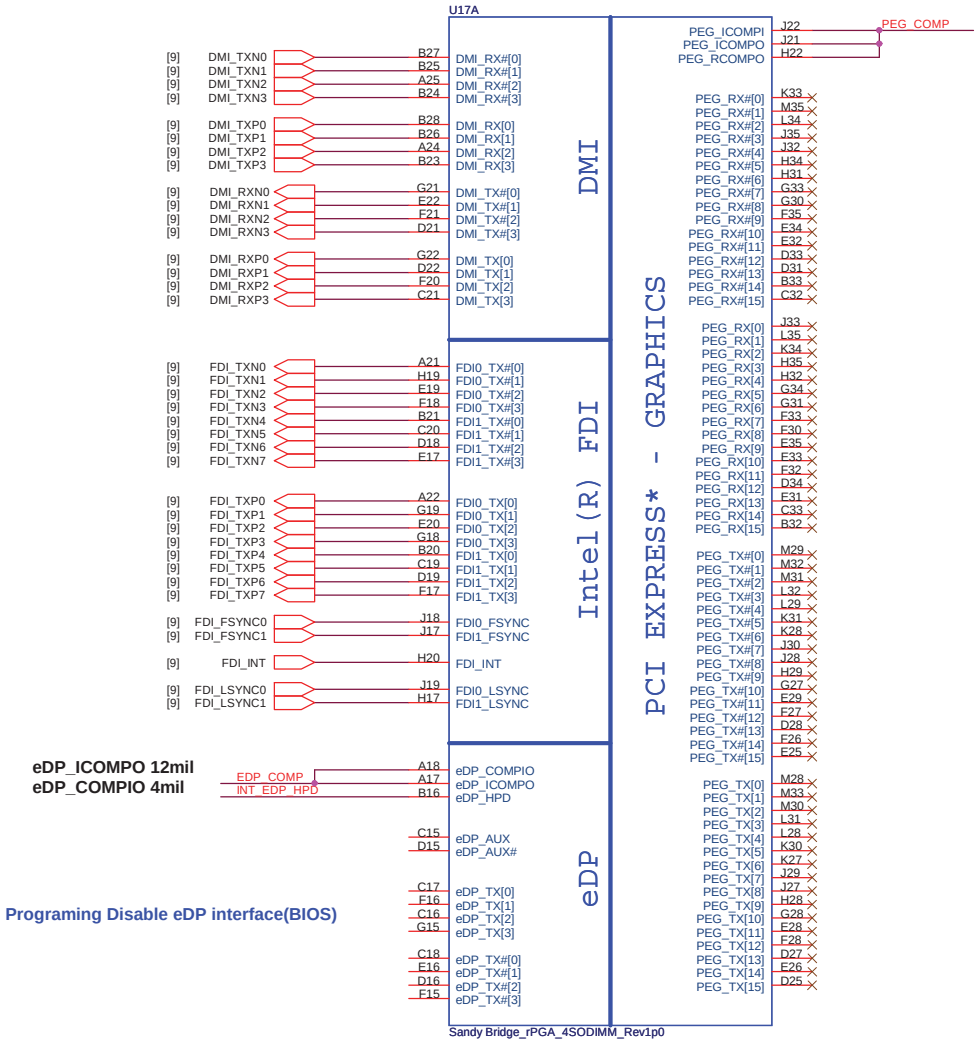
Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	BLANK	2A

Date: Wednesday, October 06, 2010 Sheet 3 of 42

Sandy Bridge Processor (DMI,PEG,FDI)

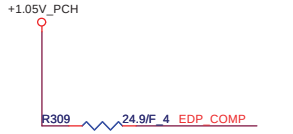


PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,

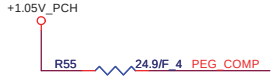
eDP_ICOMPO 12mil
eDP_COMPIO 4mil

Programing Disable eDP interface(BIOS)

DP & PEG Compensation



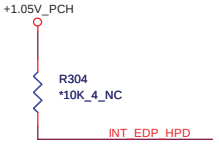
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed within 500 mils



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils

PEG_ICOMPO signals should be routed within 500 mils

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 1/5	2A
Date: Friday, January 07, 2011	Sheet 4 of 42	

Sandy Bridge Processor (CLK,MISC,JTAG)

U17B

follow SS8: SNB_IVB# N.A at SNB EDS #27637 0.7v1

MISC
- TP43 — C26 — PROC_SELECT#
- [23] H_CPUDET# — AN34 — SKTOCC#

THERMAL
- TP34 — TP_CATERR# — AL33 — CATERR#
- [23] PECI_EC — R445 43/J_4 — H_PECI_R — AN33 — PECI
- [23,35,40] H_PROCHOT# — R181 56/J_4 — H_PROCHOT#_R — AL32 — PROCHOT#
- [14] PM_THRMTRIP# — AN32 — THERMTRIP#

Over 130 degree C will drive low

PWR MANAGEMENT
- [9] H_PM_SYNC — AM34 — PM_SYNC
- [14] H_PWRGOOD — AP33 — UNCOREPWRGOOD
  - R189 10K/J_4
- SM_DRAMPWROK — V8 — SM_DRAMPWROK
- +1.05V_PCH — R192 *75/J_4_NC — CPU_PLTRST# — R193 *43/J_4_NC — CPU_PLTRST#_R — AR33 — RESET#

CLOCKS
- BCLK — A28 — CLK_CPU_BCLKP [13]
- BCLK# — A27 — CLK_CPU_BCLKN [13]
- DPLL_REF_CLK — A16 — CLK_DP_P_R — R310 1K_4 — R305 *0_4_NC — CLK_DP_P [13]
- DPLL_REF_CLK# — A15 — CLK_DP_N_R — R306 *0_4_NC — CLK_DP_N [13]
  - R311 1K_4 — +1.05V_PCH

DDR3 MISC
- SM_DRAMRST# — R8 — CPU_DRAMRST#
- SM_RCOMP[0] — AK1 — SM_RCOMP_0 — R153 140/F_4
- SM_RCOMP[1] — A5 — SM_RCOMP_1 — R312 25.5/F_4
- SM_RCOMP[2] — A4 — SM_RCOMP_2 — R313 200/F_4

SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

JTAG & BPM
- PRDY# — AP29
- PREQ# — AP27
- TCK — AR26 — XDP_TCLK
- TMS — AR27 — XDP_TMS
- TRST# — AP30 — XDP_TRST# — R447 51/J_4
- TDI — AR28 — XDP_TDI
- TDO — AP26 — XDP_TDO
- DBR# — AL35 — XDP_DBRST# — R443 1K_4 — +3.3V_RUN
- BPM#[0] — AT28
- BPM#[1] — AR29
- BPM#[2] — AR30
- BPM#[3] — AT30
- BPM#[4] — AP32
- BPM#[5] — AR31
- BPM#[6] — AT31
- BPM#[7] — AR32

+1.05V_PCH
- XDP_TMS — R452 51/J_4
- XDP_TDI — R450 51/J_4
- XDP_TDO — R201 51/J_4
- XDP_TCLK — R202 51/J_4

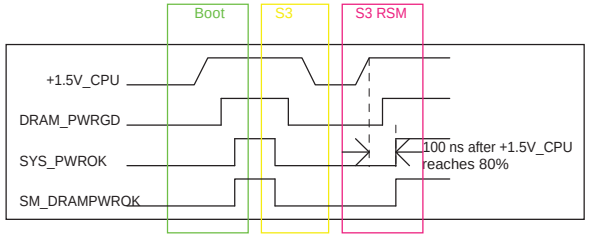
XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor can be removed?
Need to confirm with Intel

Sandy Bridge_rPGA_4SODIMM_Rev1p0

IN	OUT
L	L
H	High-Z

+3.3V_SUS
- U8 NC VCC IN GND OUT — *74LVC1G07GW_NC
- C333 *0.1U/10V/X7R_4_NC
- [12,23,24] PLTRST# — CPU_PLTRST#
- R556 1.5K 1%
- CPU_PLTRST#_R voltage level Ckt.
- CPU_PLTRST# R
- R557 750 1%



Change OD part same with PDC

Copy from PDC

R8239, R8241 change to 5%

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

+3.3V_SUS
- R183 200_4
- C301 0.1U/10V/X7R_4
- U6 74AHC1G09GW
- [9] PM_DRAM_PWRGD
- [9] SYS_PWROK
- SM_DRAMPWROK_R — R184 *39_NC — Q14 *2N7002K_NC — PS_S3CNTRL [7,16]

+1.5V_CPU
- R170 200/F_4
- R176 130/F_4 — SM_DRAMPWROK

Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration

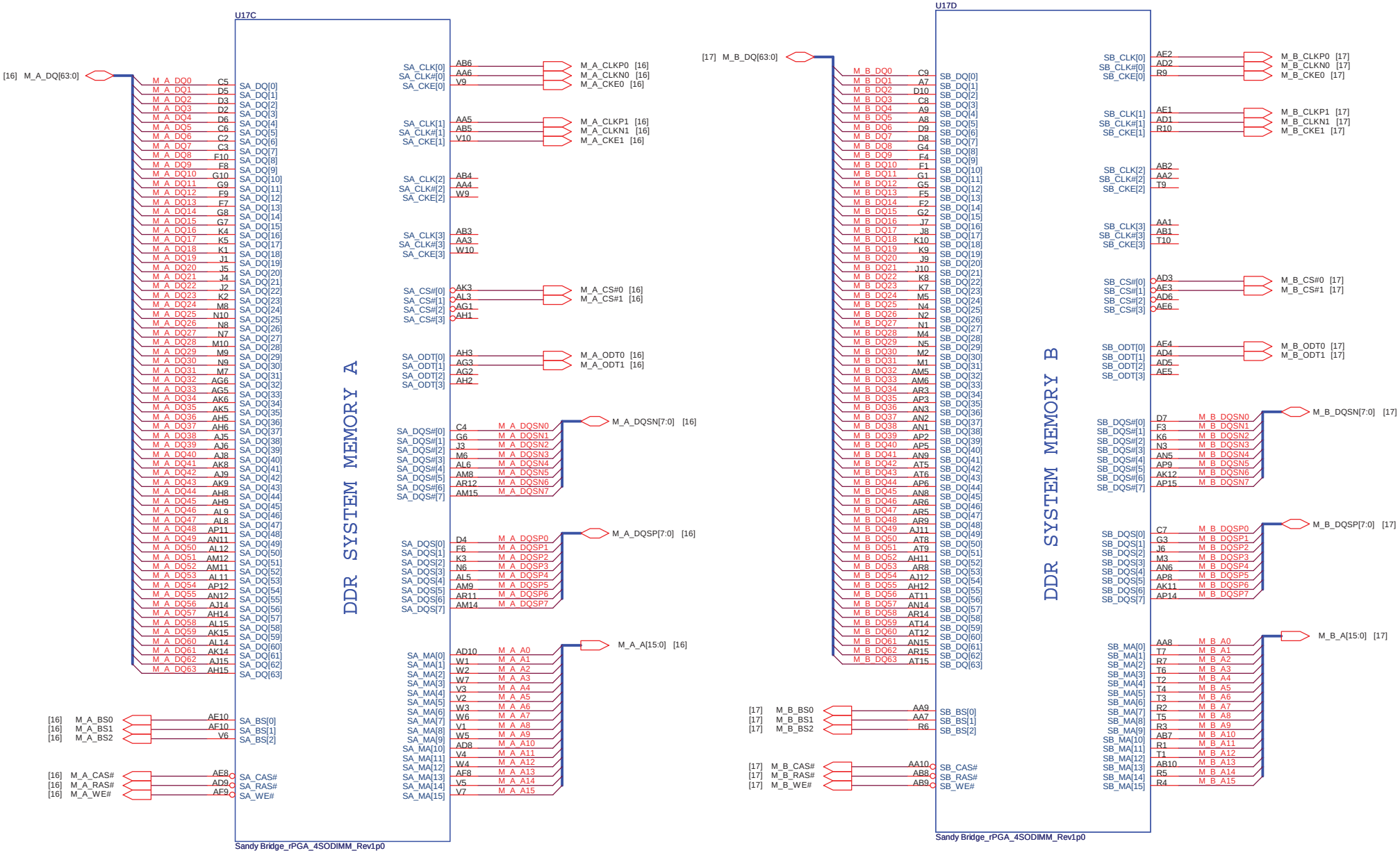
+1.5V_SUS
- R72 1K/F_4
- R54 *0_4_NC
- Q5 BSS138-7-F
- R63 1K/F_4
- [16,17] DDR3_DRAMRST#
- DDR3_DRAMRST#_R
- CPU_DRAMRST#
- [13] DDR_HVREF_RST_PCH
- C86 0.047U/10V_4
- R56 4.99K/F_4

Schematic C/L_v1.0, P56 (PU,PD 1k/J) (Intel and PD3)
Reserve (Intel confirm now)

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 2/5	2A
Date: Monday, January 24, 2011	Sheet 5 of 42	

Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 3/5	2A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU VTT
SNB 45W:8.5A
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

CPU VGT
SNB 45W:22A
22uF x 12

CPU Core Power
SNB 45W:95A
470uF/4mohm x 4
22uF x 16
10uF x 10

CPU MCH
SNB 45W: 5A
330uF/6mohm x 1
10uF x 6

CPU SA
SNB 45W: 6A
330uF/7mohm x 1
10uF x 3

CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2

POWER
CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
VREF

Sandy Bridge_rPGA_4SODIMM_Rev1p0

22uF (Reserved)

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

S3 Power reduce

Take care Q3509 Vgs(MAX)=2.5

Change R8281,R8285, R8704,R8329 to +/-5%
54.9 ohm has no 5%

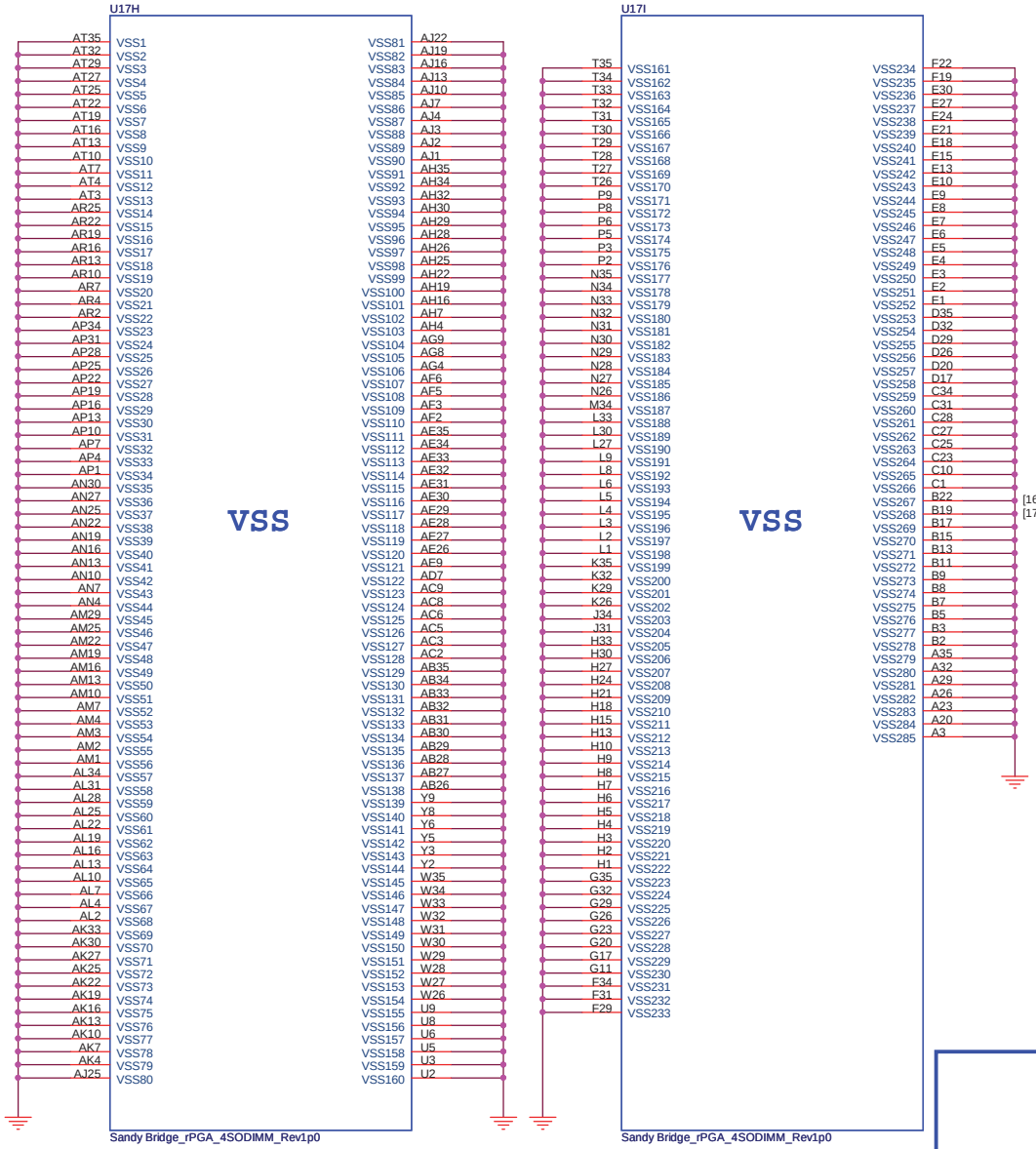
Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
PU Close to VR
Place PU resistor close to CPU
SVID DATA
PU Close to VR
Place PU resistor close to CPU
SVID ALERT

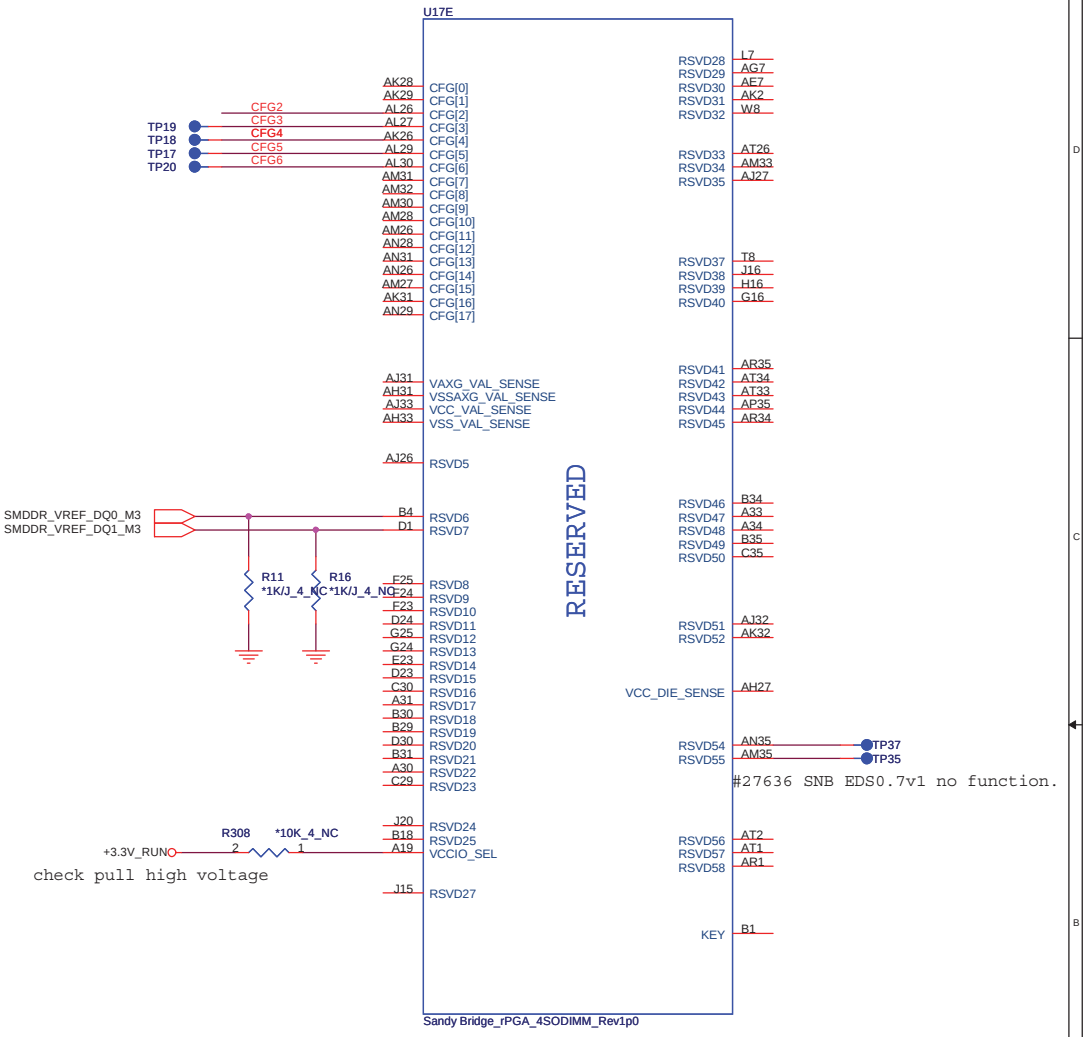
Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 4/5	2A
Date: Monday, January 24, 2011	Sheet 7 of 42	

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R199 1K/F_4

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Sandy Bridge 5/5	2A

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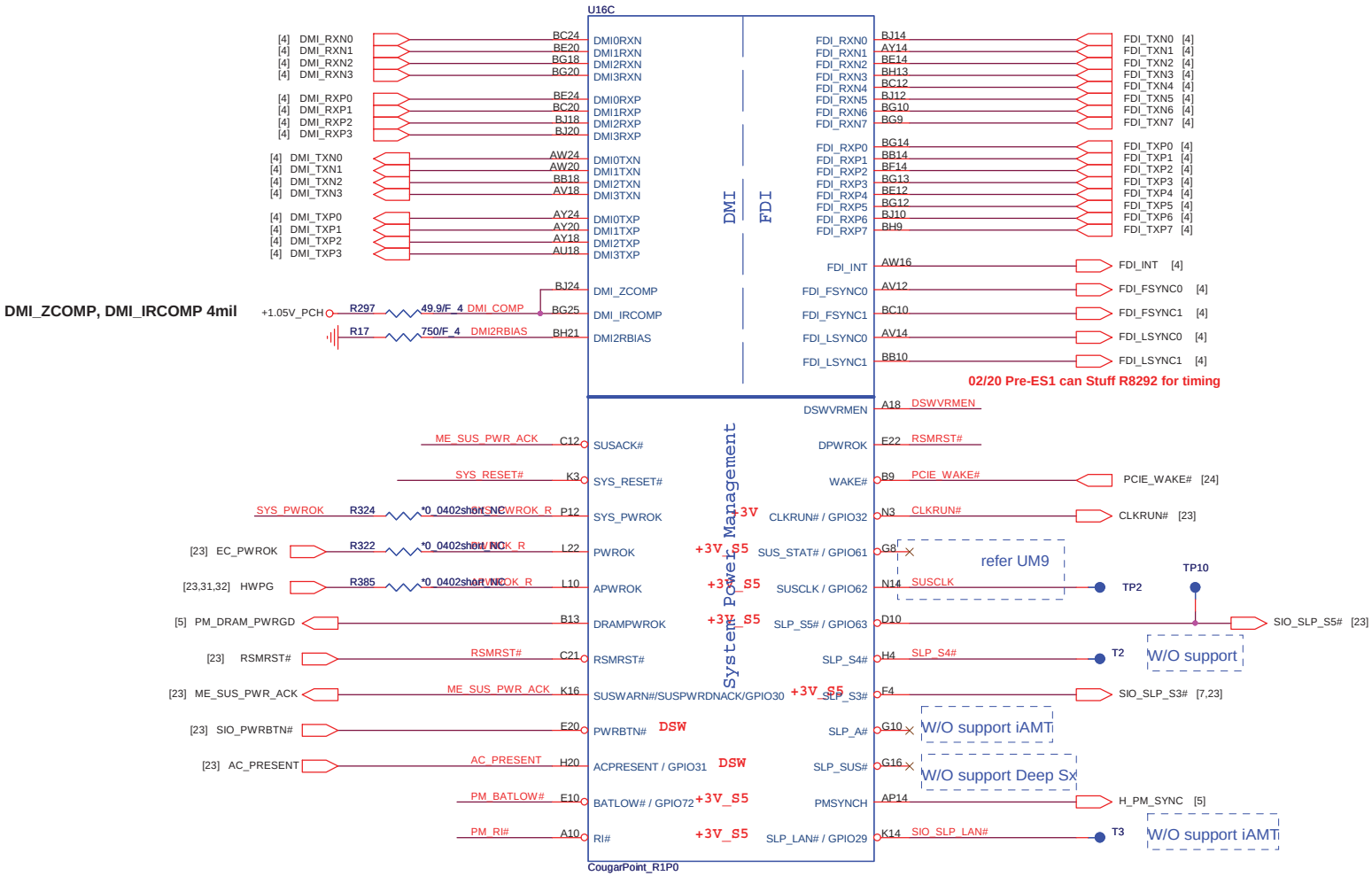
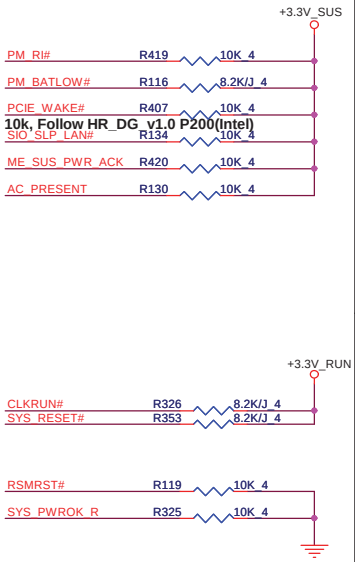
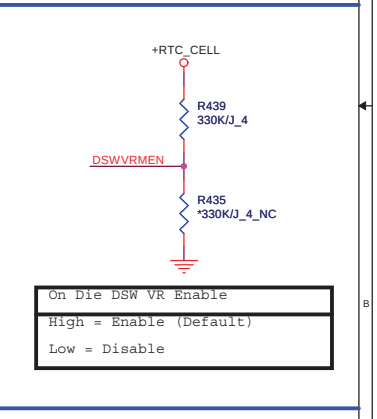
Cougar Point (DMI,FDI,PM)

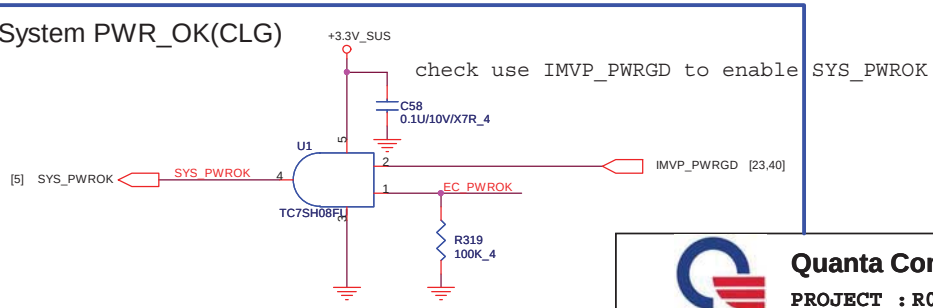


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



Quanta Computer Inc.
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Size	Document Number	Rev
	Cougar Point 1/7	2A
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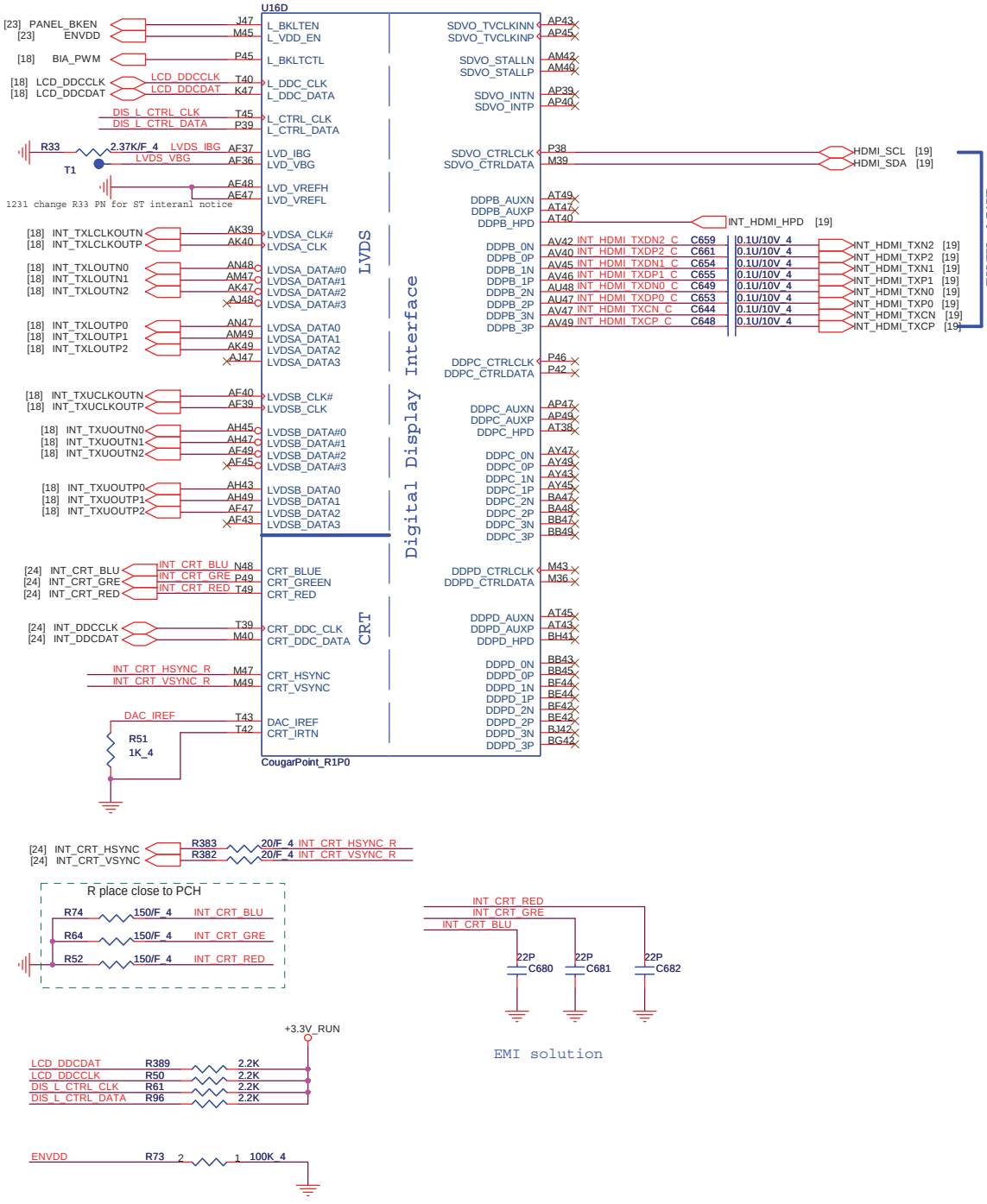
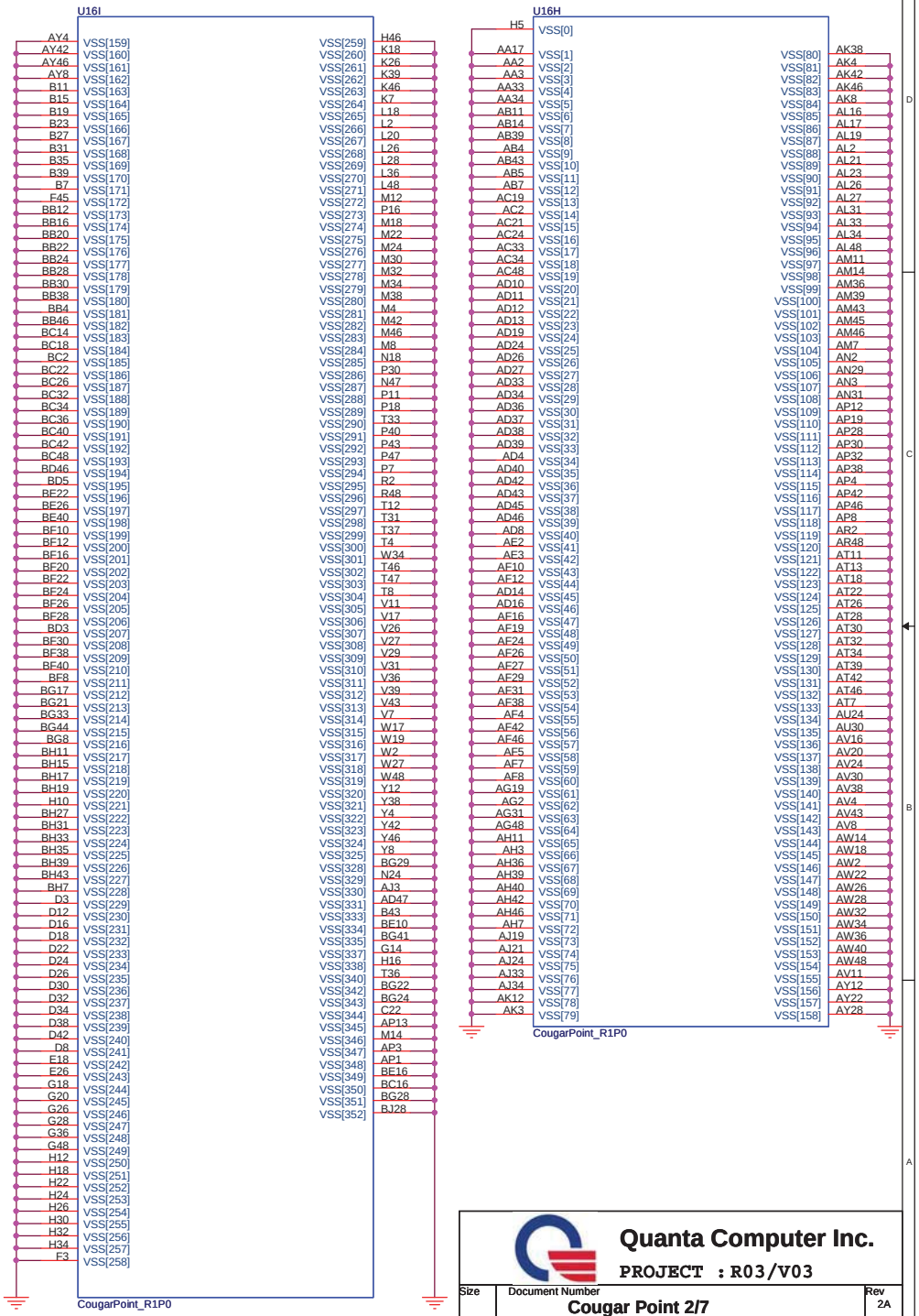
Cougar Point (LVDS,DDI)



Cougar Point (GND)



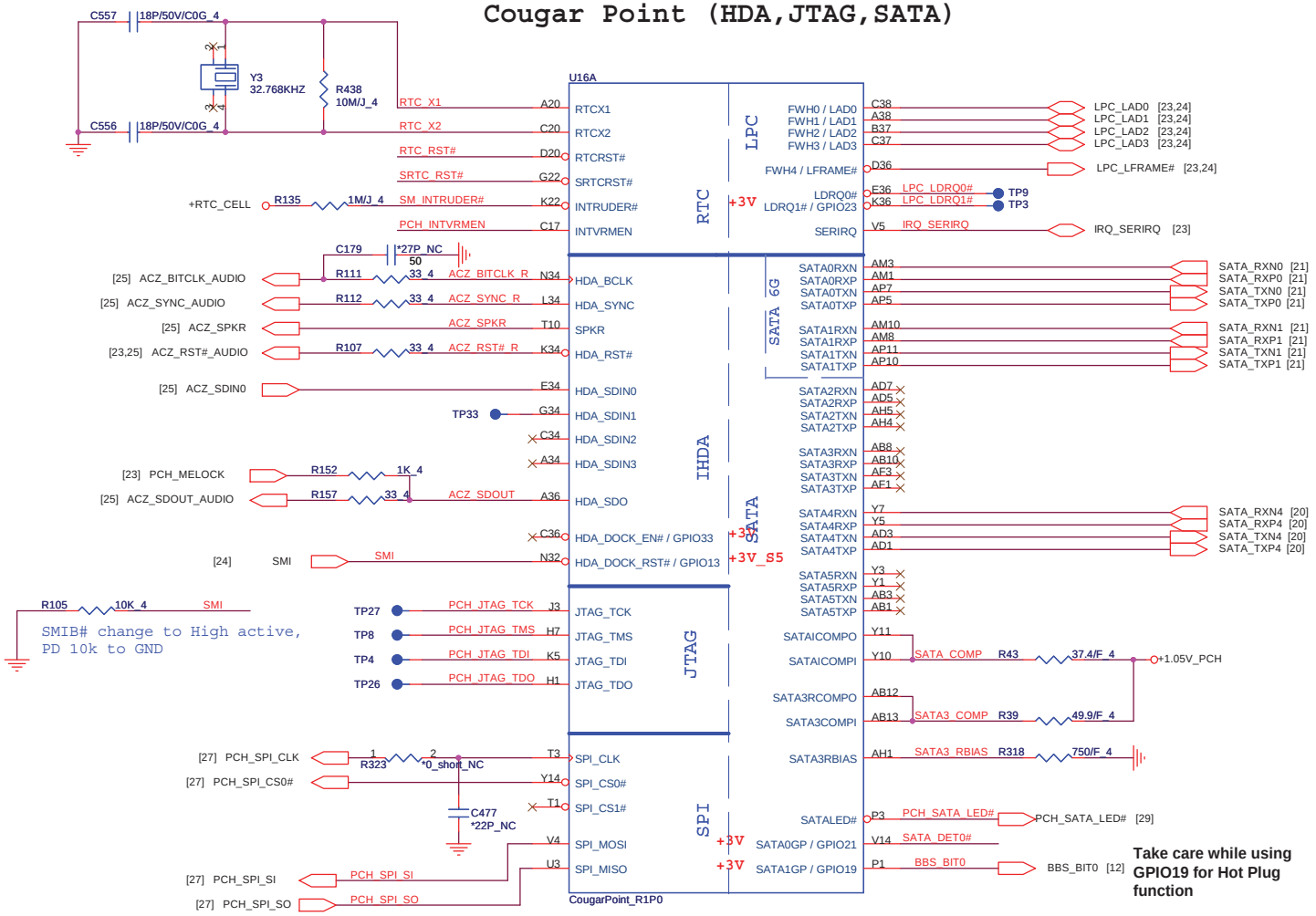
Quanta Computer Inc.

PROJECT : R03/V03

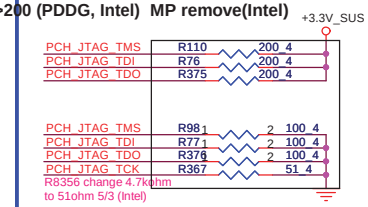
Size	Document Number	Rev
	Cougar Point 2/7	2A

Date: Monday, January 24, 2011 Sheet 10 of 42

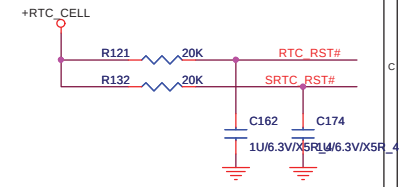
Cougar Point (HDA,JTAG,SATA)



PCH JTAG Debug (CLG)



5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R41 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R146 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R434 330K/J_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R118 1K_4 ACZ_SYNC_R

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 3/7	2A

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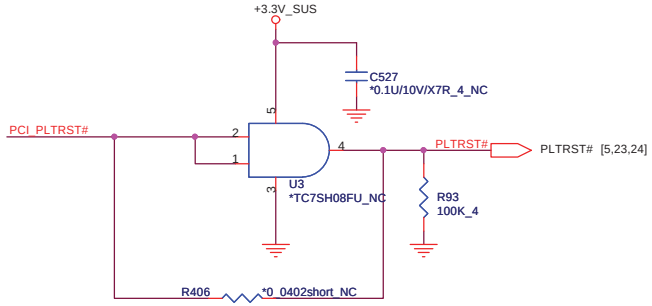
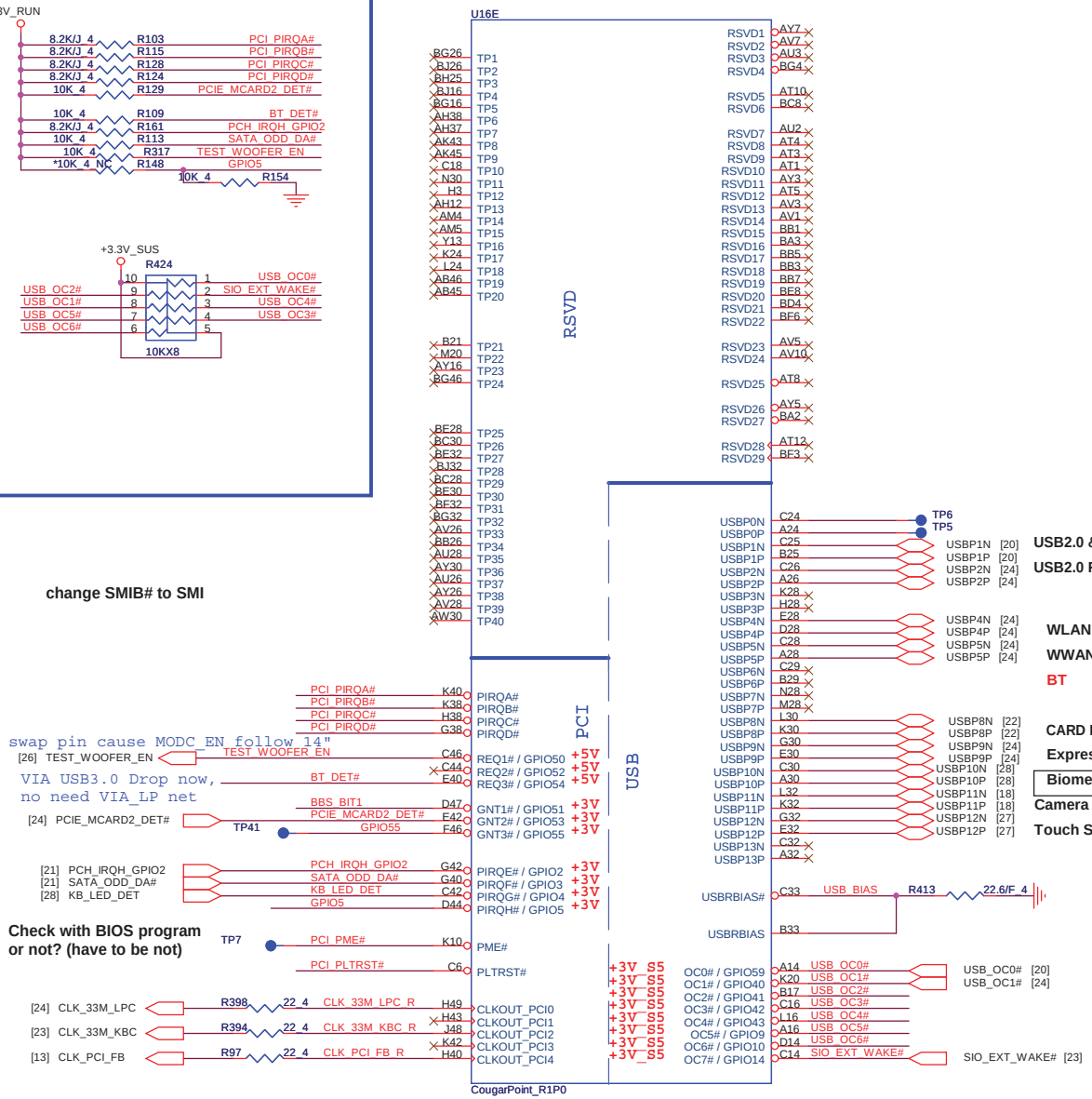
Cougar Point-M (PCI,USB,NVRAM)

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)



change SMIB# to SMI



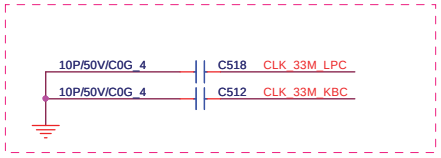
Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
			Defined in EDS (Intel)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
			Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm

CheckList_1.0 p58; HR_v1.0 p450

R314 2.2K +1.8V_RUN
DF_TVS [14]

follow CheckList_1.5, DF_TVS pu-high 2,2k only, Remove R315

SV_SET_UP
High = Strong (Default)



EMI solution pop C518, C512

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Cougar Point 4/7	2A
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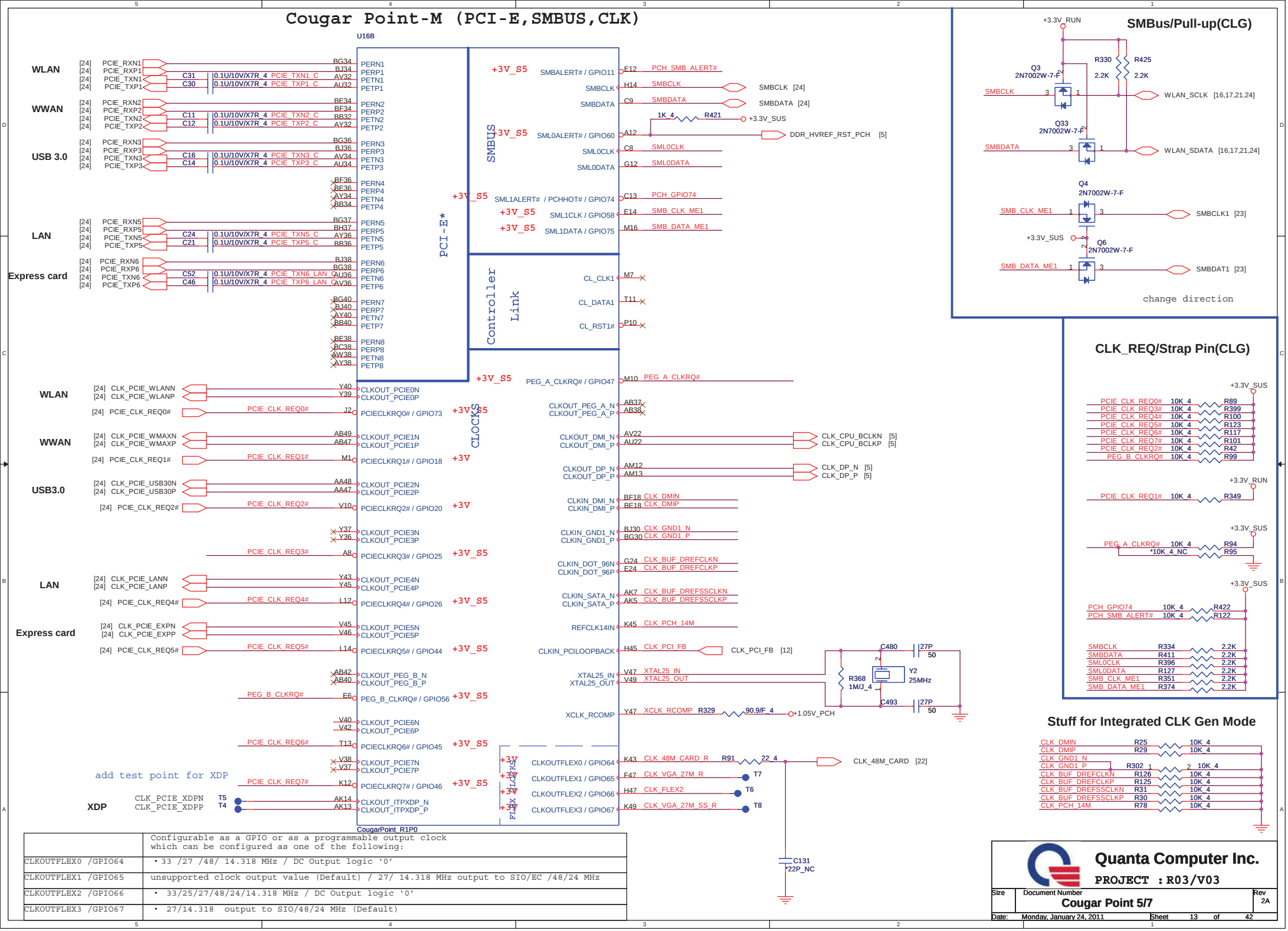
Cougar Point-M (PCI-E,SMBUS,CLK)



	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

Quanta Computer Inc.

PROJECT : R03/V03

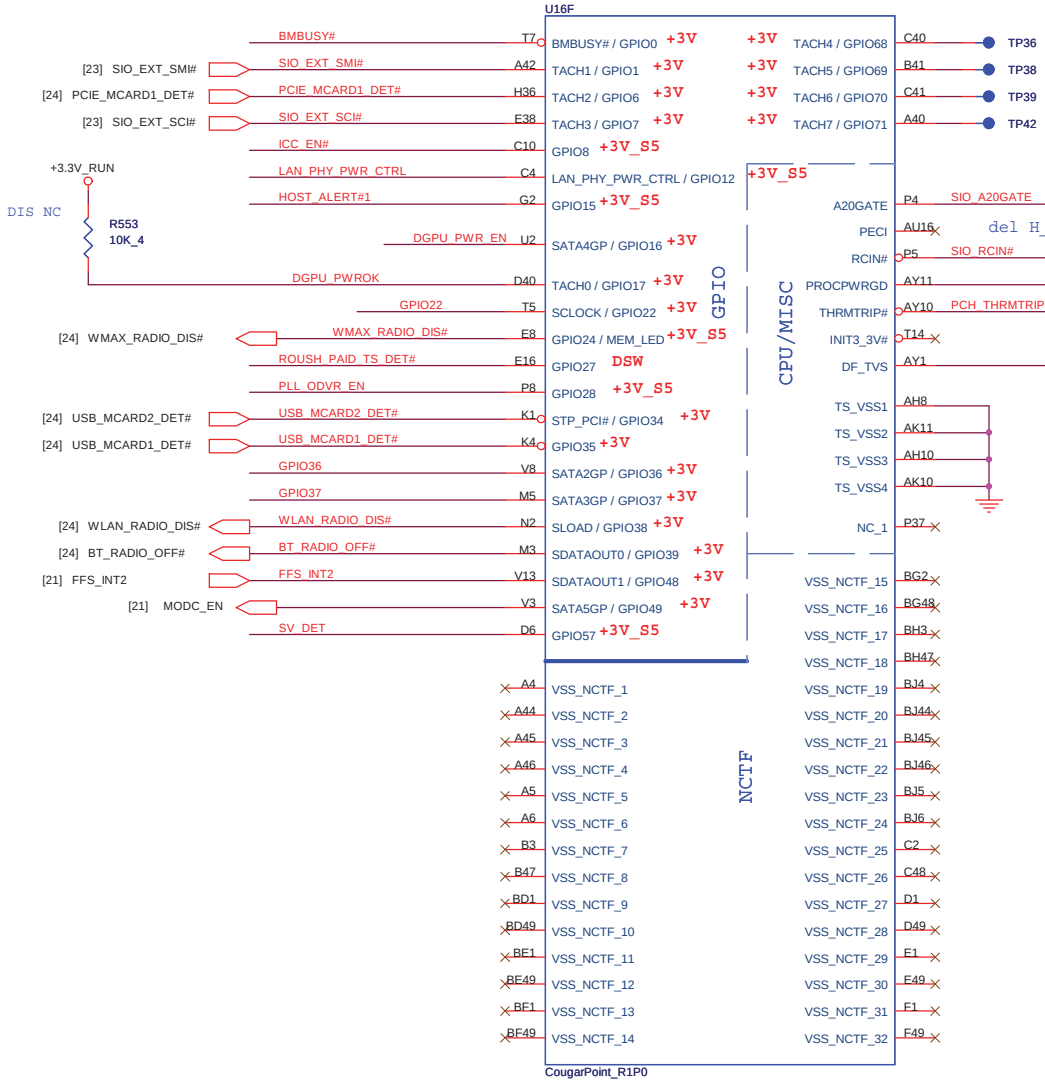
Size	Document Number	Rev
	Cougar Point 5/7	2A

Date: Monday, January 24, 2011 Sheet 13 of 42

Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R70 *1K_4_NC PLL_ODVR_EN

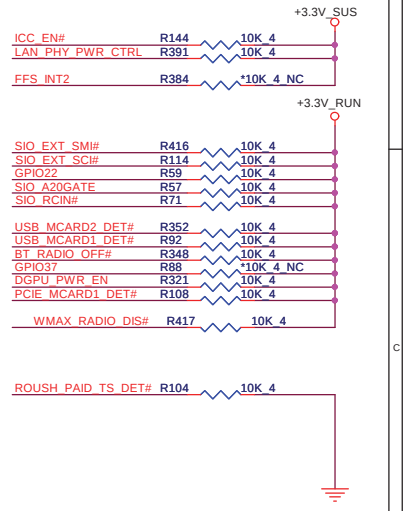


R553 10K_4 DIS NC +3.3V_RUN

Ask Intel, what's the function?

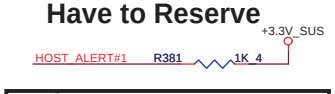
Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)



Can be del

Have to Reserve



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

MFG-TEST Can be del

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COUGAR POINT (POWER)

Cougar Point (POWER)

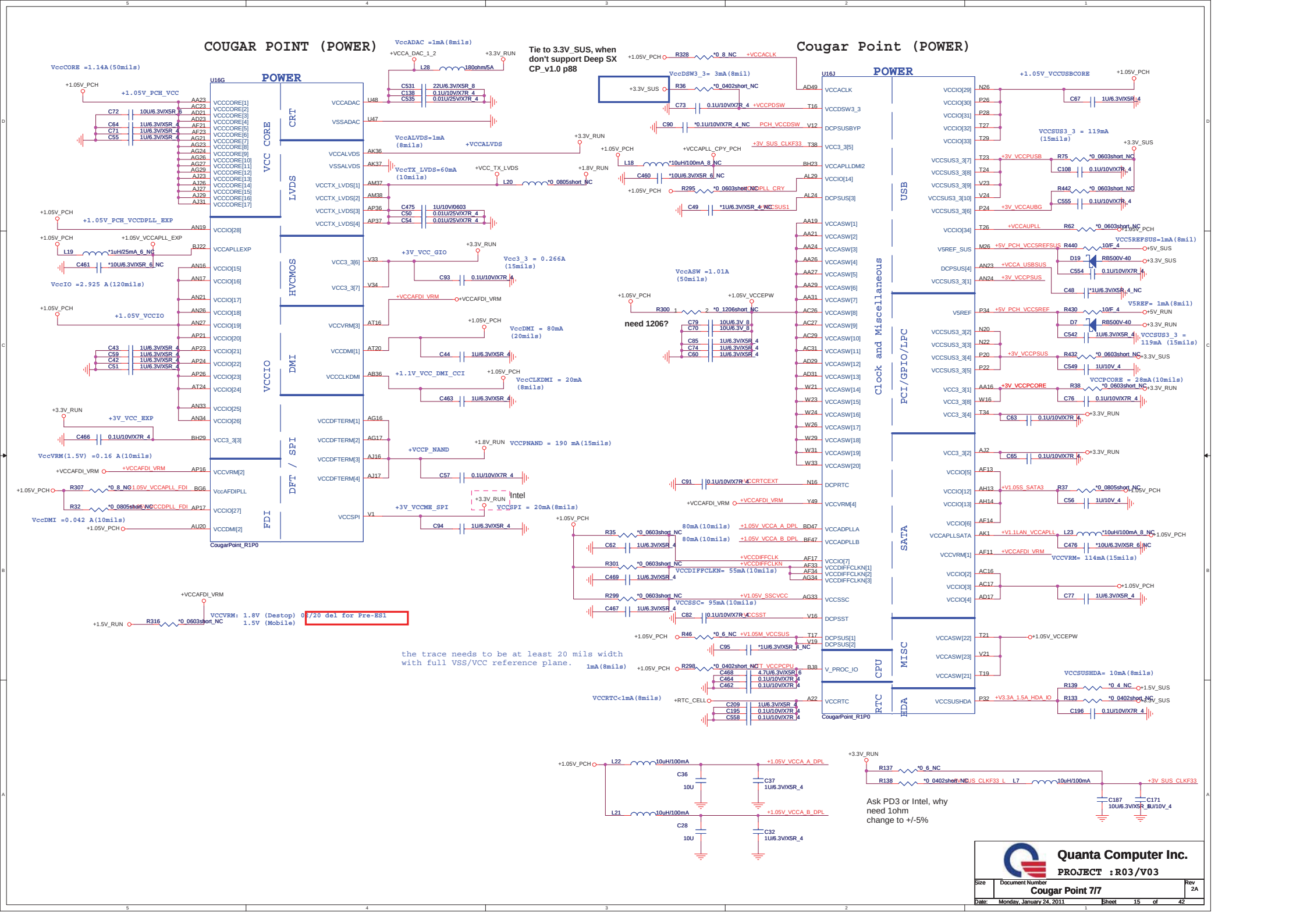
Tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

need 1206?

Intel

the trace needs to be at least 20 mils width with full VSS/VCC reference plane.

Ask PD3 or Intel, why need 1ohm change to +/-5%



Quanta Computer Inc.			
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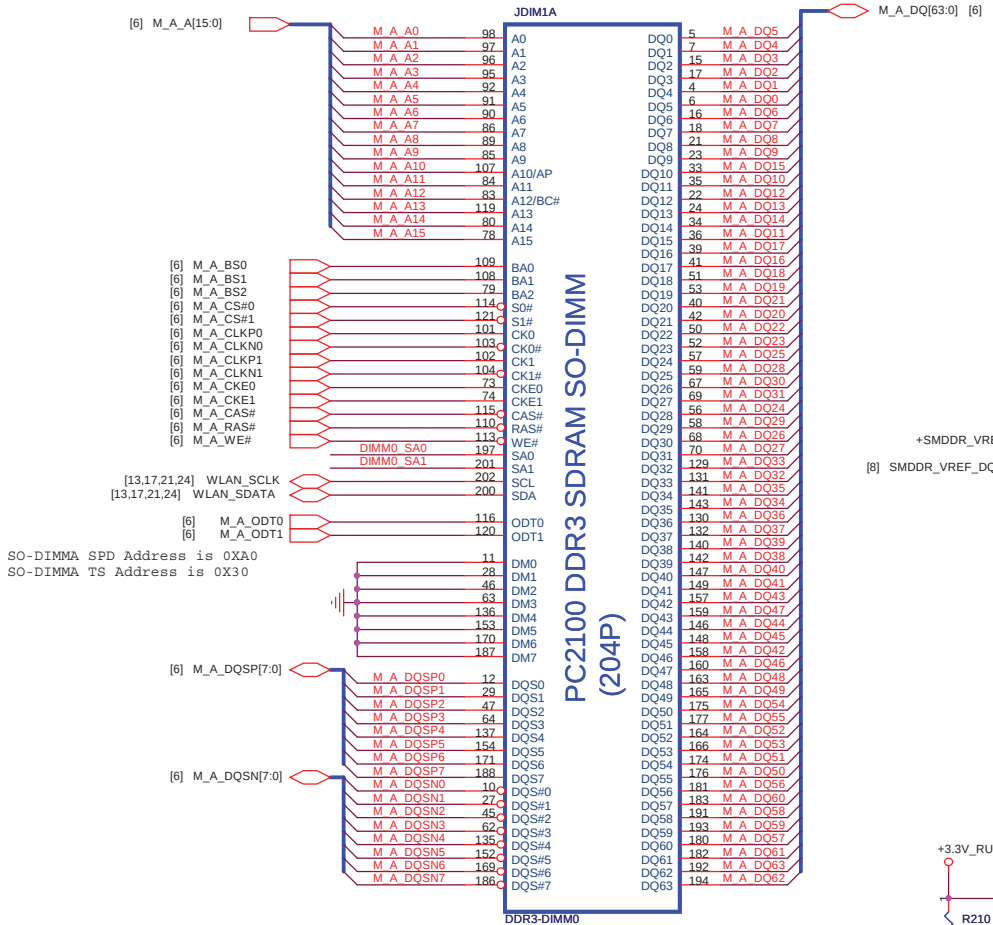
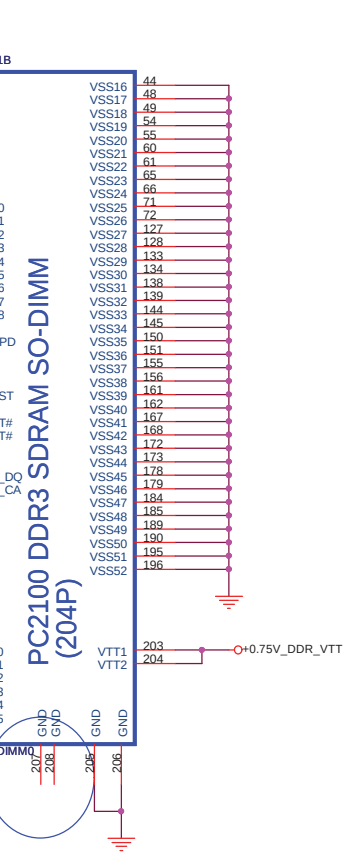
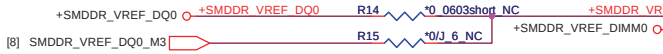
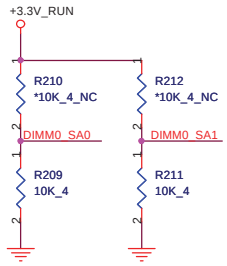
H=8.0mm,RVS





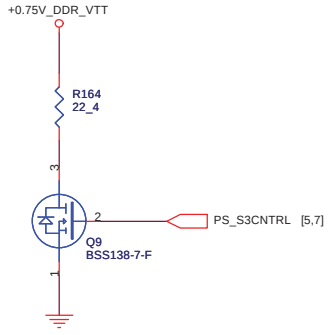
M3 reserve



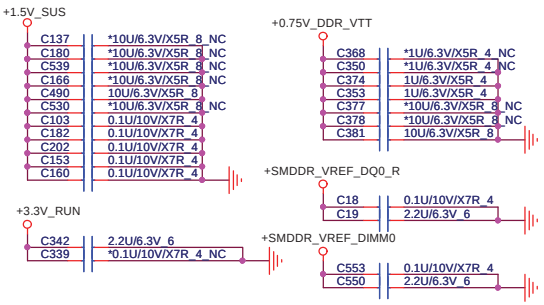


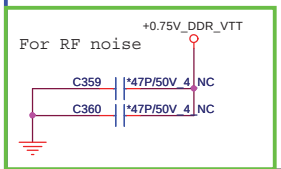
	DIMM0_SA0	DIMM0_SA1
DOMM0	0	0
DOMM1	0	1

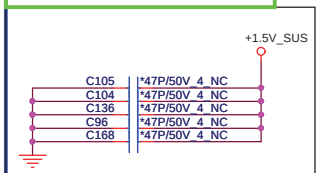
S3 Power reduce



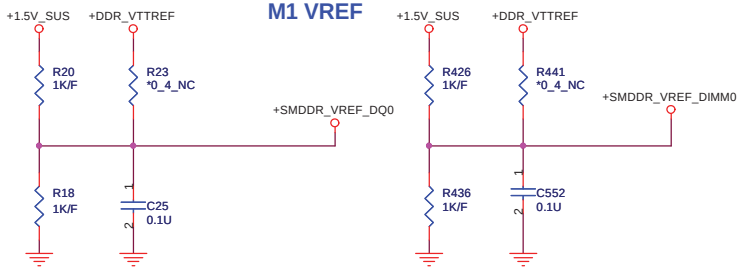
Place these Caps near So-Dimm0.







M1 VREF



Quanta Computer Inc.

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Size	Document Number	Rev
	DDR3 DIMM-0	2A

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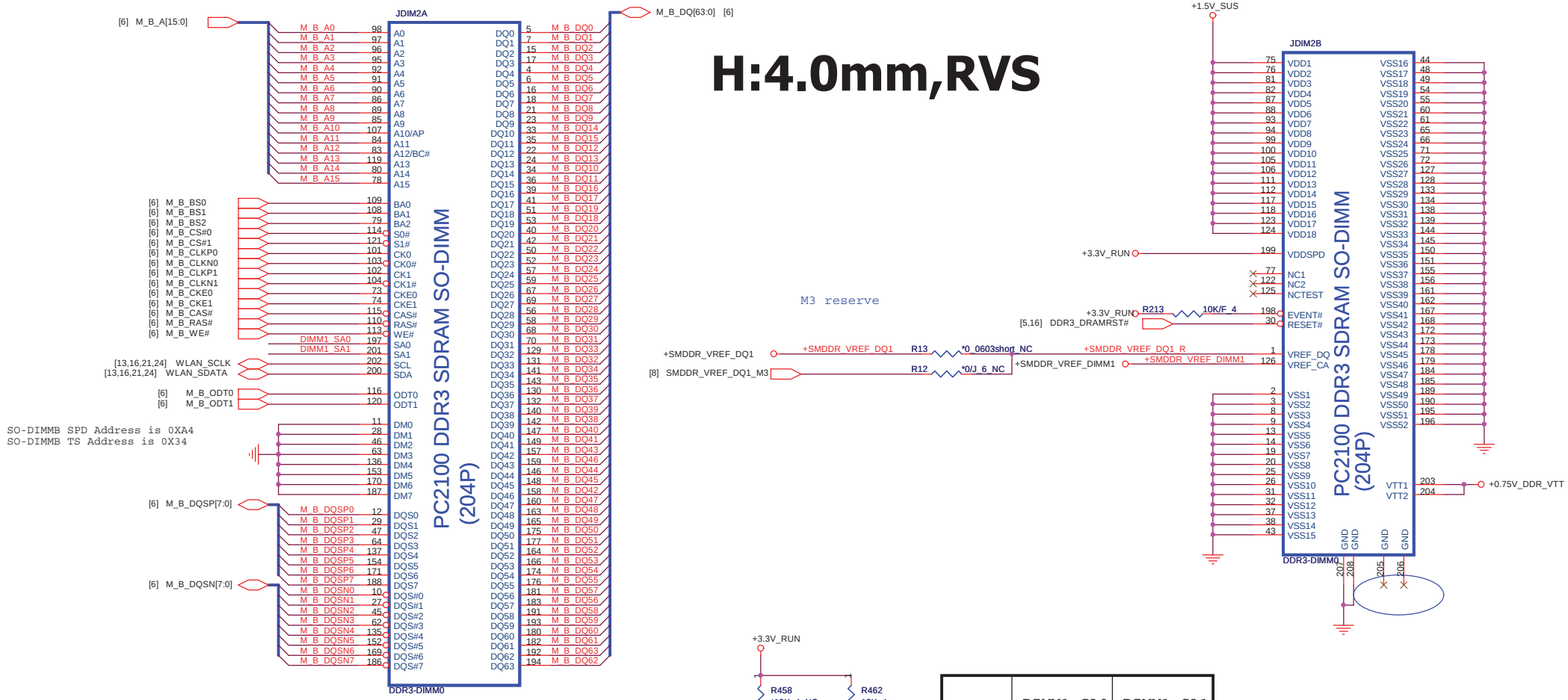
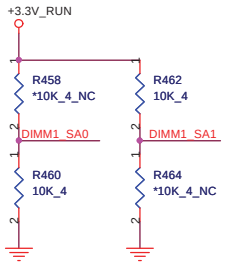
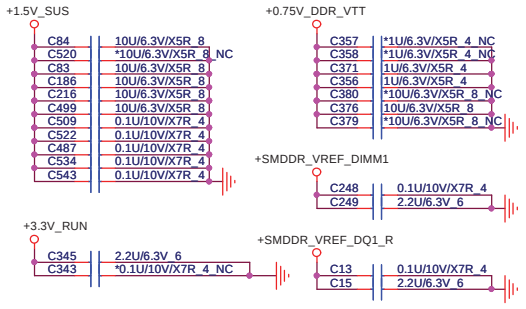
H:4.0mm,RVS

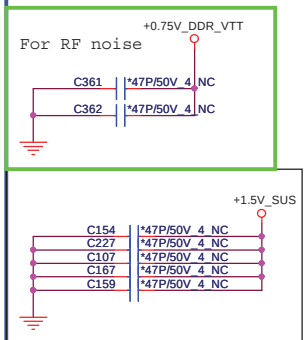




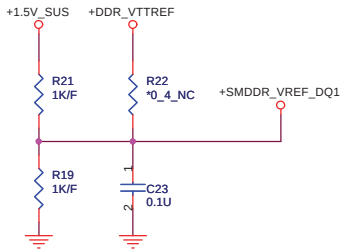
	DIMM1_SA0	DIMM1_SA1
DOMM0	0	0
DOMM1	0	1

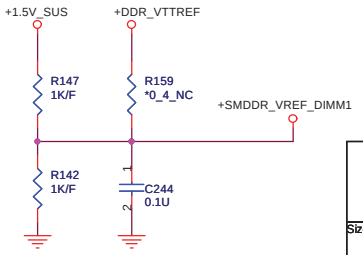
Place these Caps near So-Dimm2.





M1 VREF





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Size	Document Number	Rev
	DDR3 DIMM-1	2A

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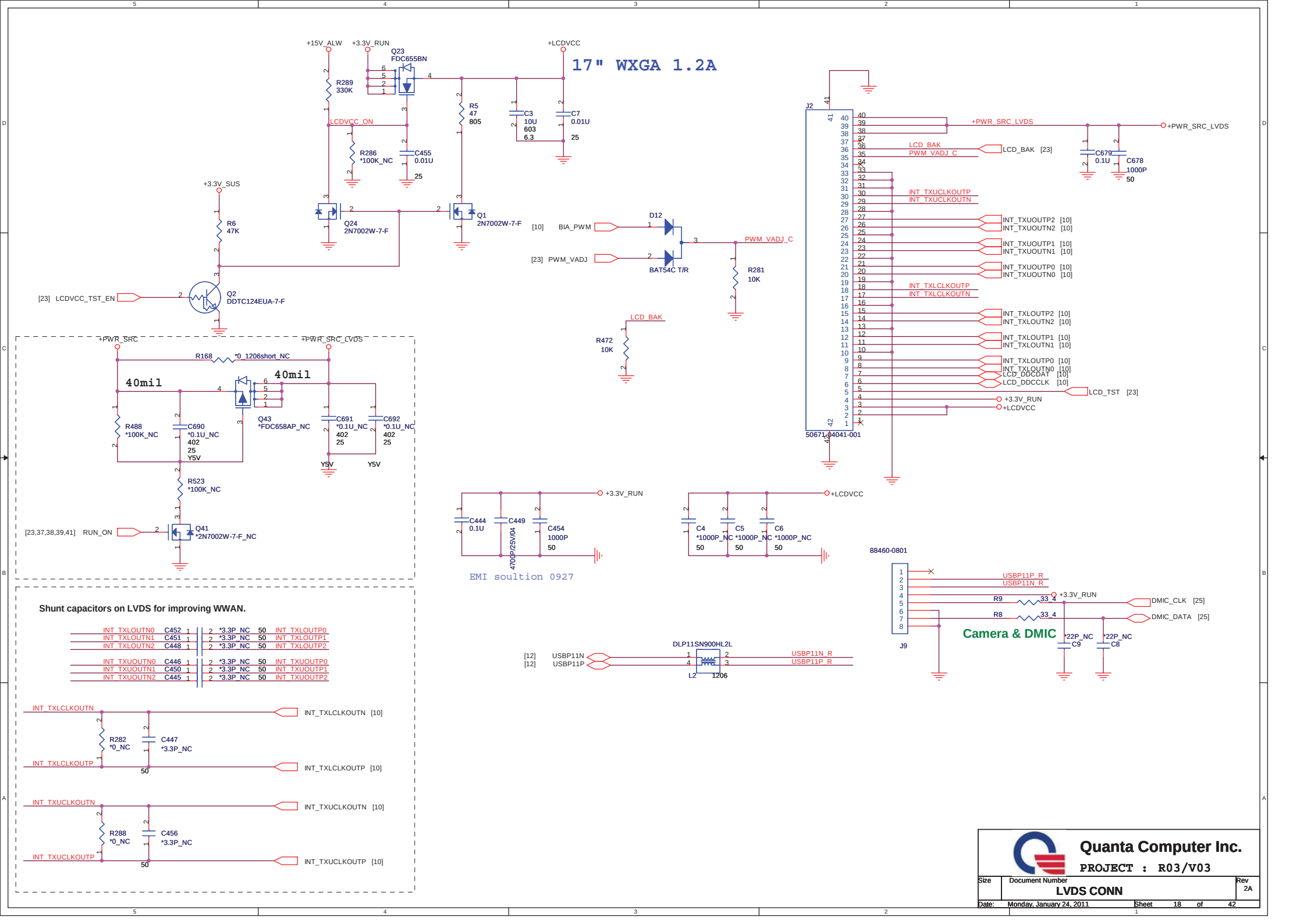
17" WXGA 1.2A
+15V_ALW
+3.3V_RUN
+LCDVCC
Q23
FDC655BN
R289
330K
LCDVCC_ON
R286
*100K_NC
C455
0.01U
25
R5
47
805
C3
10U
603
6.3
C7
0.01U
25
+3.3V_SUS
R6
47K
Q24
2N7002W-7-F
Q1
2N7002W-7-F
[23] LCDVCC_TST_EN
Q2
DDTC124EUA-7-F
[10] BIA_PWM
[23] PWM_VADJ
D12
BAT54C T/R
PWM_VADJ_C
R281
10K
R472
10K
LCD_BAK
J2
+PWR_SRC_LVDS
LCD_BAK
PWM_VADJ_C
LCD_BAK [23]
C679
0.1U
C678
1000P
50
INT_TXUCLKOUTP
INT_TXUCLKOUTN
INT_TXUOUTP2 [10]
INT_TXUOUTN2 [10]
INT_TXUOUTP1 [10]
INT_TXUOUTN1 [10]
INT_TXUOUTP0 [10]
INT_TXUOUTN0 [10]
INT_TXLCLKOUTP
INT_TXLCLKOUTN
INT_TXLOUTP2 [10]
INT_TXLOUTN2 [10]
INT_TXLOUTP1 [10]
INT_TXLOUTN1 [10]
INT_TXLOUTP0 [10]
INT_TXLOUTN0 [10]
LCD_DDCDAT [10]
LCD_DDCCLK [10]
LCD_TST [23]
+3.3V_RUN
+LCDVCC
50671-04041-001
+PWR_SRC
+PWR_SRC_LVDS
R168
*0_1206short_NC
40mil
40mil
R488
*100K_NC
C690
*0.1U_NC
402
25
Y5V
Q43
*FDC658AP_NC
C691
*0.1U_NC
402
25
C692
*0.1U_NC
402
25
R523
*100K_NC
[23,37,38,39,41] RUN_ON
Q41
*2N7002W-7-F_NC
+3.3V_RUN
C444
0.1U
C449
470P/25V/04
C454
1000P
50
EMI soultion 0927
+LCDVCC
C4
*1000P_NC
50
C5
*1000P_NC
50
C6
*1000P_NC
50
88460-0801
USBP11P_R
USBP11N_R
+3.3V_RUN
R9
33_4
R8
33_4
DMIC_CLK [25]
DMIC_DATA [25]
Camera & DMIC
*22P_NC
C9
*22P_NC
C8
J9
DLP11SN900HL2L
[12] USBP11N
[12] USBP11P
L2
1206
Shunt capacitors on LVDS for improving WWAN.
INT_TXLOUTN0 C452 *3.3P_NC 50 INT_TXLOUTP0
INT_TXLOUTN1 C451 *3.3P_NC 50 INT_TXLOUTP1
INT_TXLOUTN2 C448 *3.3P_NC 50 INT_TXLOUTP2
INT_TXUOUTN0 C446 *3.3P_NC 50 INT_TXUOUTP0
INT_TXUOUTN1 C450 *3.3P_NC 50 INT_TXUOUTP1
INT_TXUOUTN2 C445 *3.3P_NC 50 INT_TXUOUTP2
INT_TXLCLKOUTN
R282
*0_NC
C447
*3.3P_NC
INT_TXLCLKOUTP
50
INT_TXLCLKOUTN [10]
INT_TXLCLKOUTP [10]
INT_TXUCLKOUTN
R288
*0_NC
C456
*3.3P_NC
INT_TXUCLKOUTP
50
INT_TXUCLKOUTN [10]
INT_TXUCLKOUTP [10]
Quanta Computer Inc.
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LVDS CONN
Rev
2A
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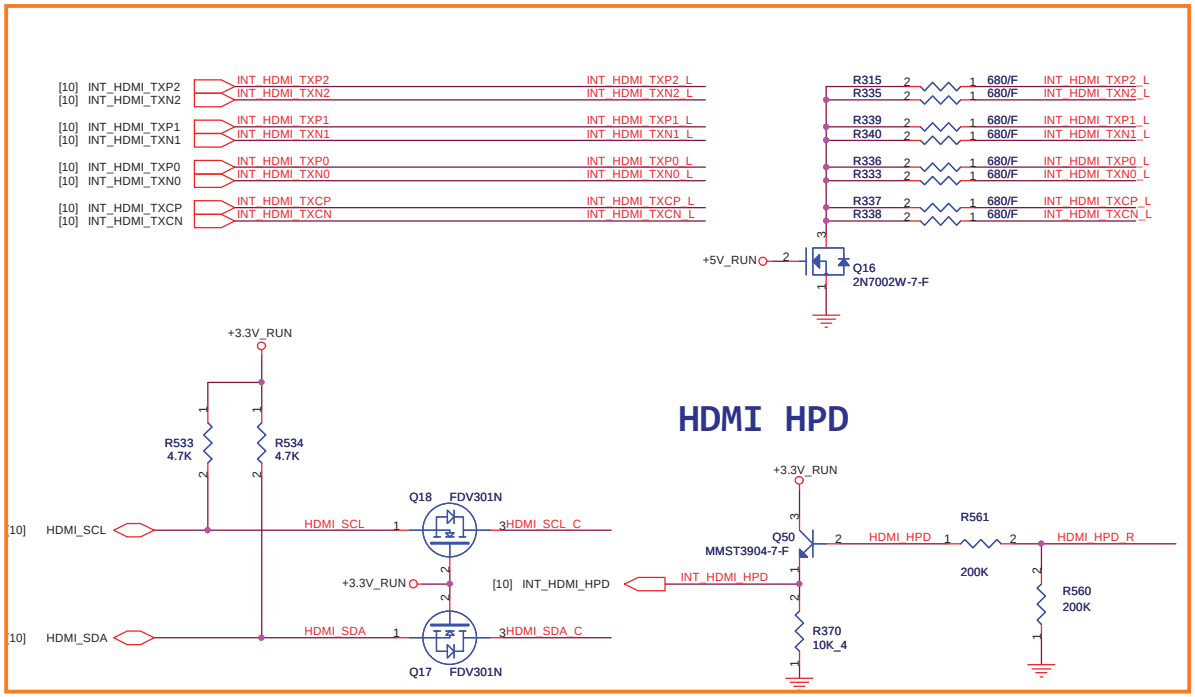

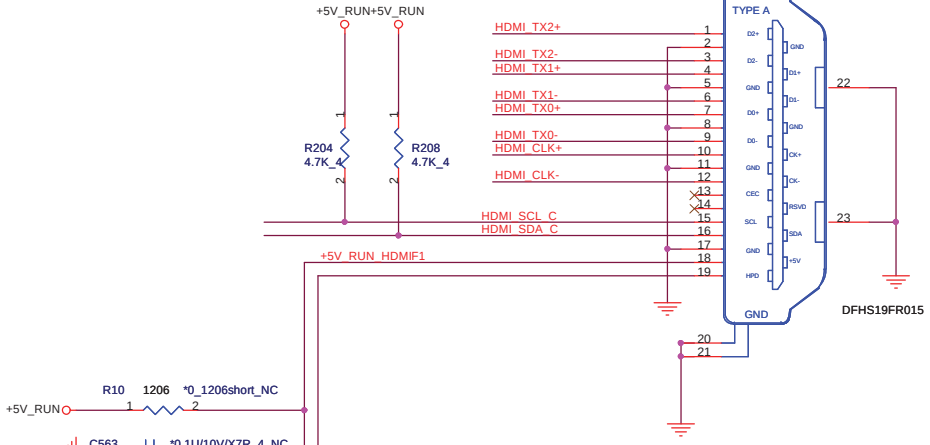

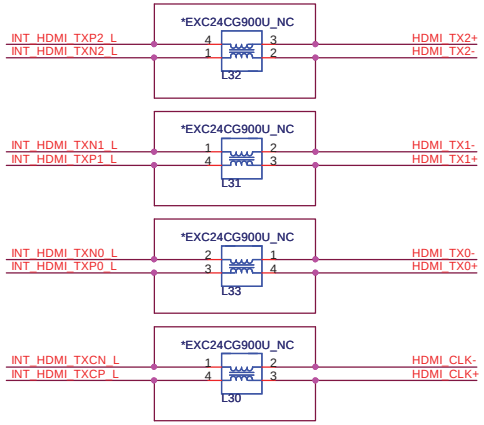

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	HDMI CONN	2A

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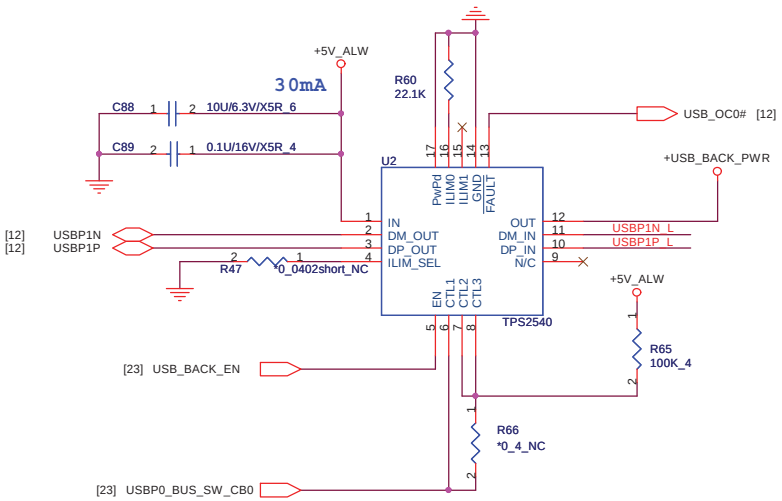
ESATA + USB Conn + Power share

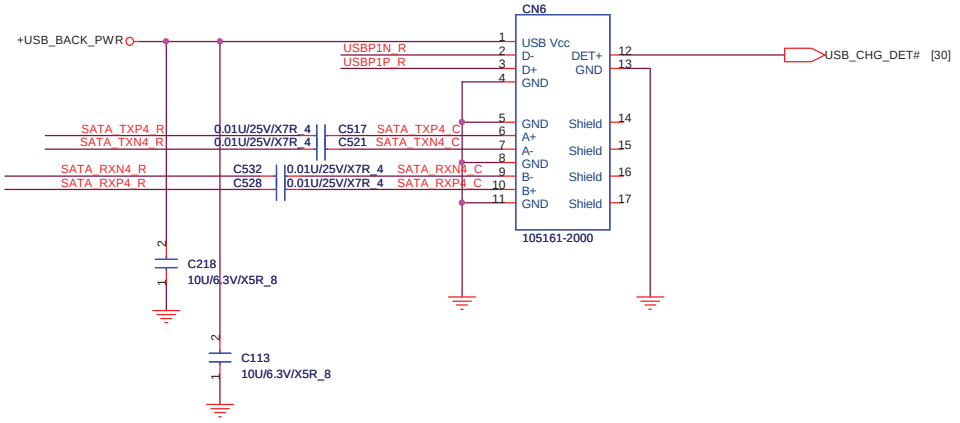
S3/S5 USB charging circuit

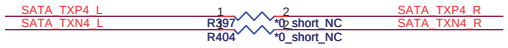


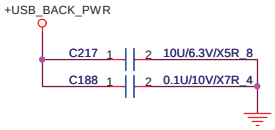
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

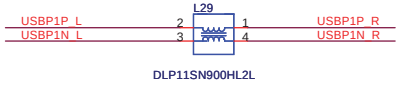
ES(PG1.0): Stuff R66, Remove R65
MP(PG1.1): Remove R66, Stuff R65

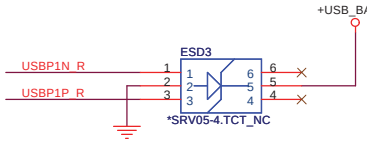
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now





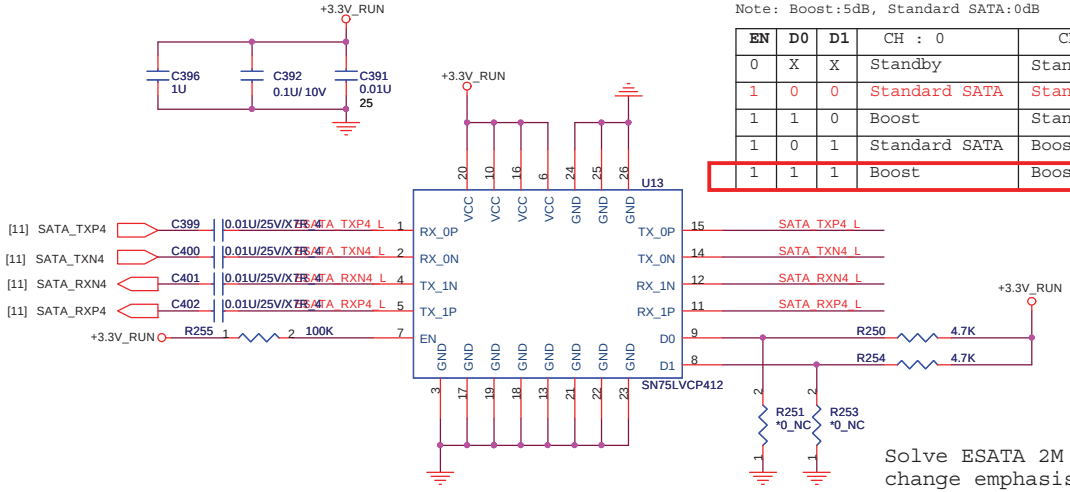






E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Solve ESATA 2M test fail issue, change emphasis setting

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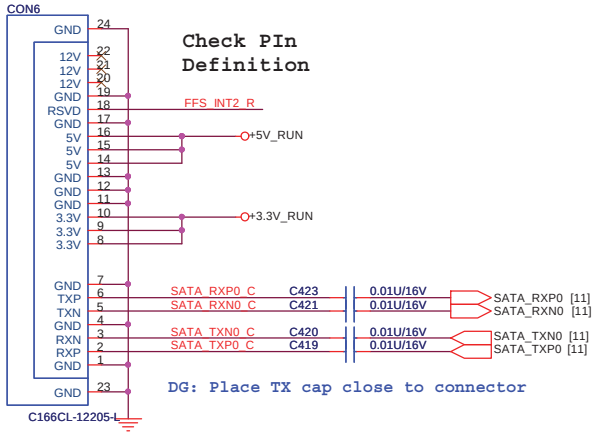
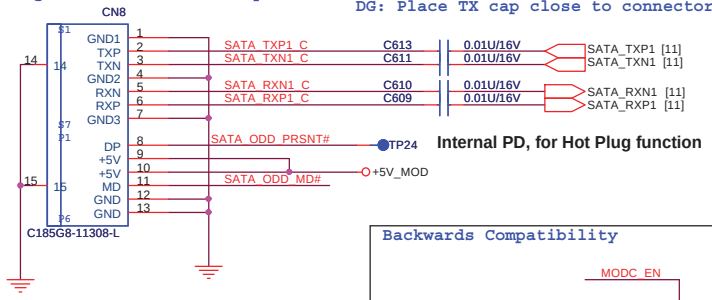
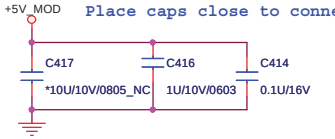
SATA Connector UM8

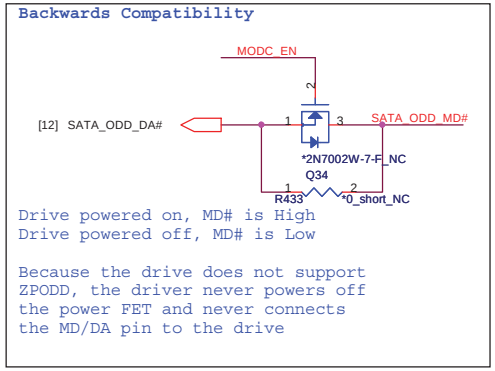


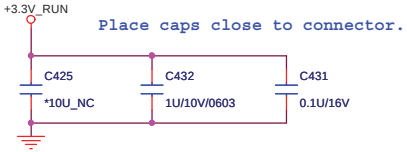
ODD Connector

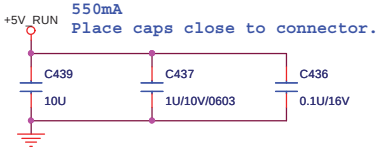
Change connector as ME request



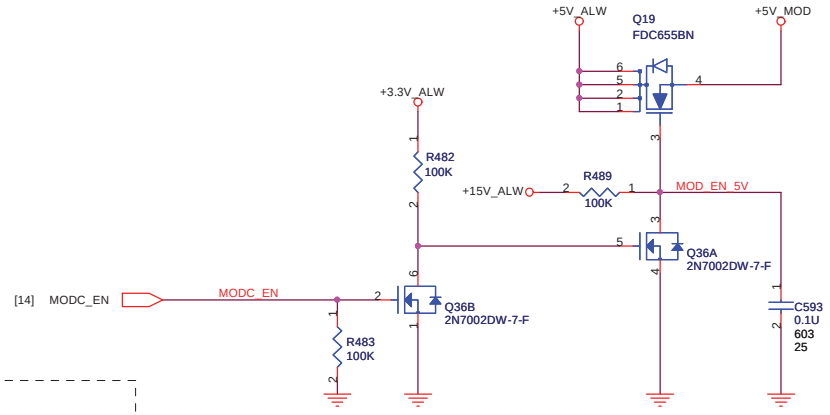


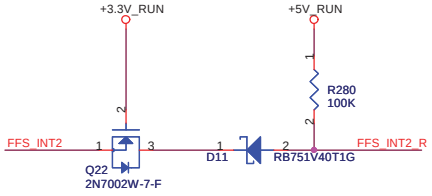


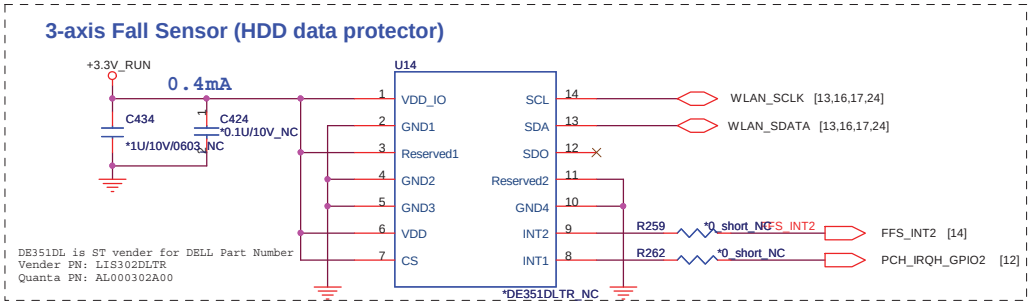




change RUN to ALW, change TRANS MOS for cost down







From FM9

Quanta Computer Inc.
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	SATA HDD/ODD	2A
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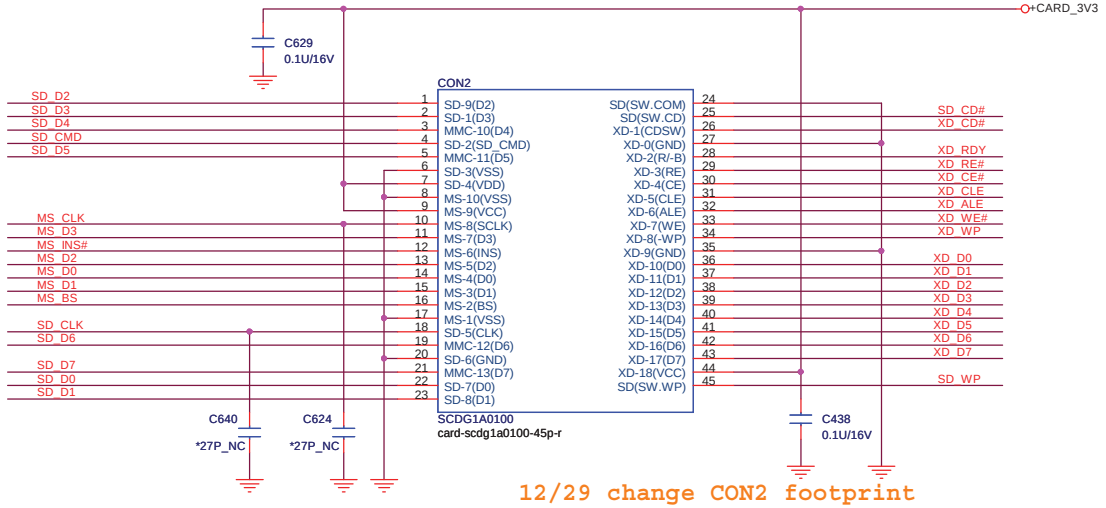
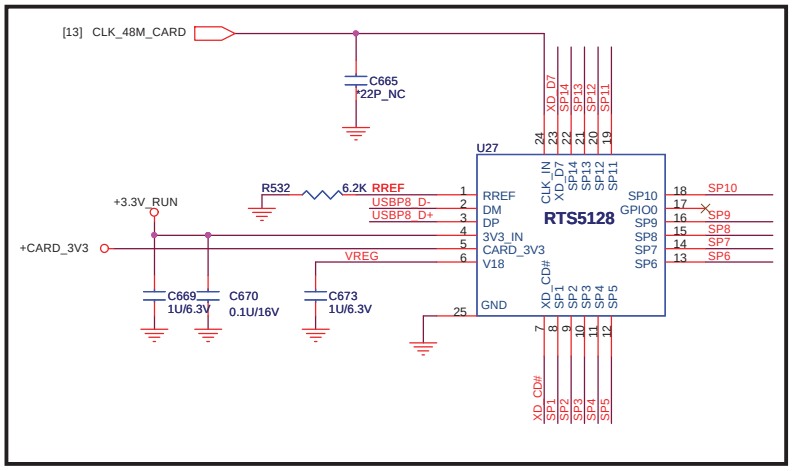
RTS5128-QFN24

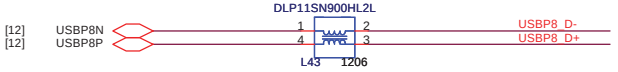


12/29 change CON2 footprint



SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



Quanta Computer Inc.

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Size	Document Number	Rev
	Cardreader (RTS5128)	2A
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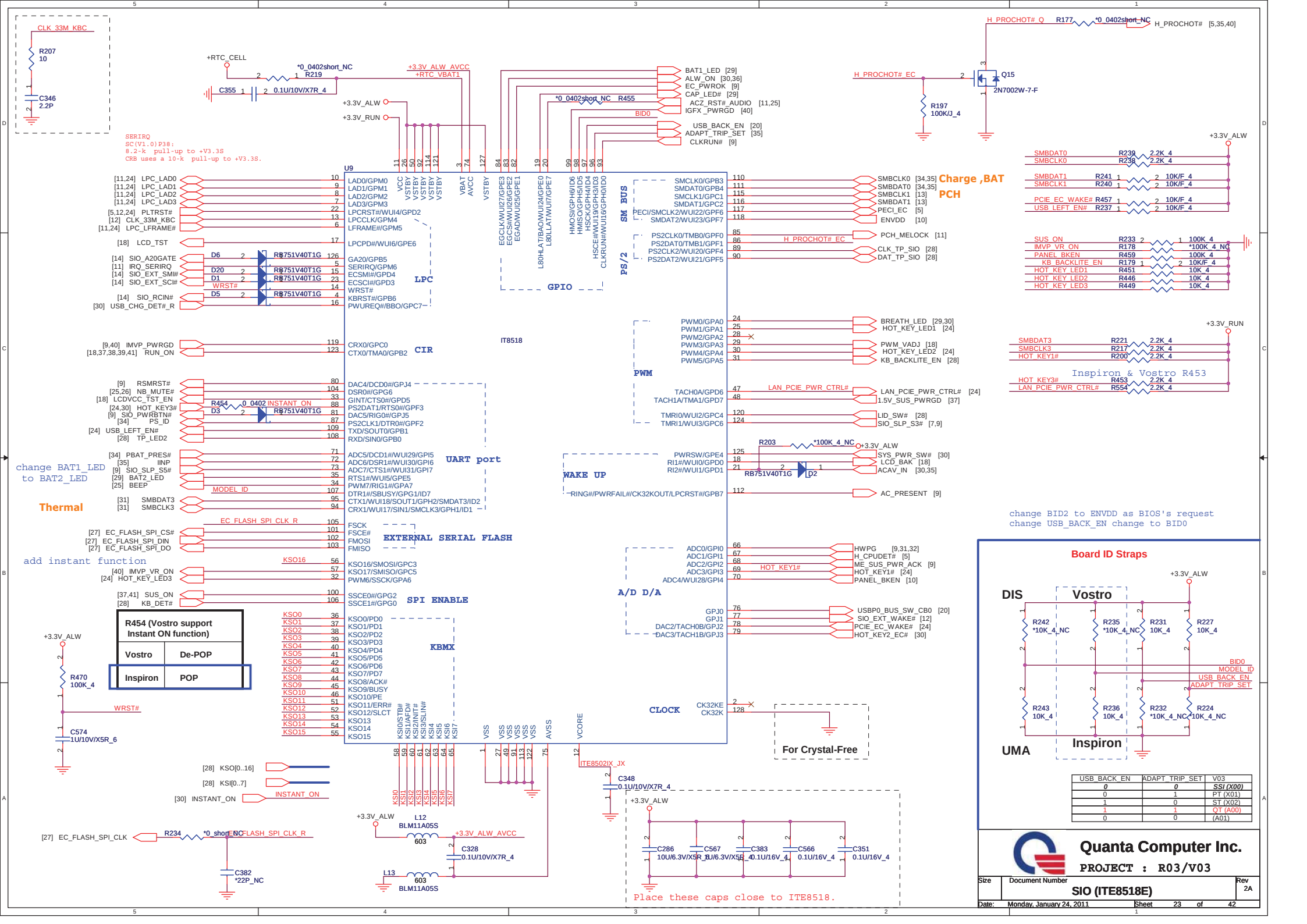
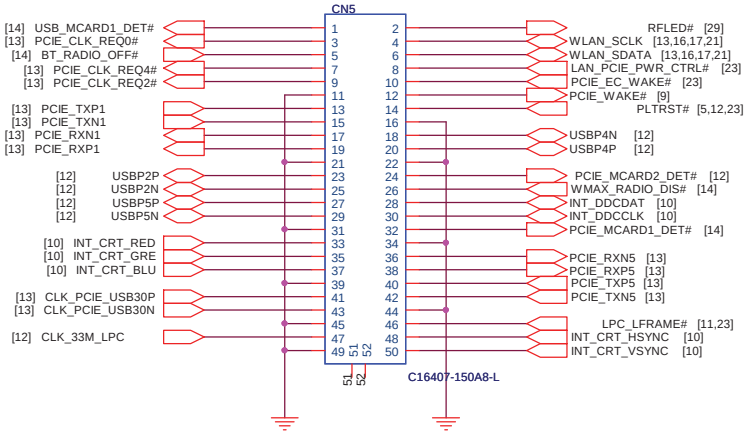
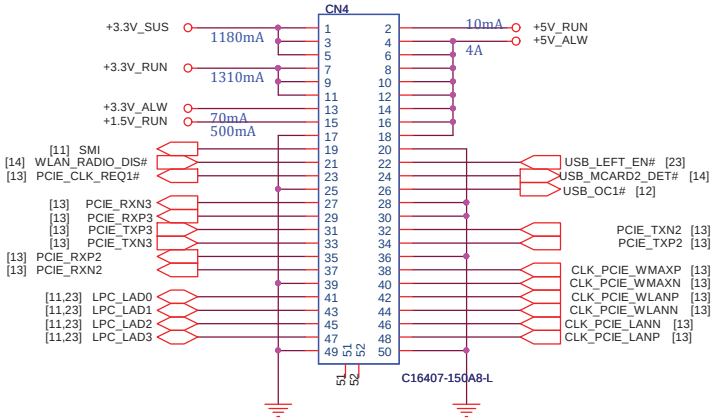
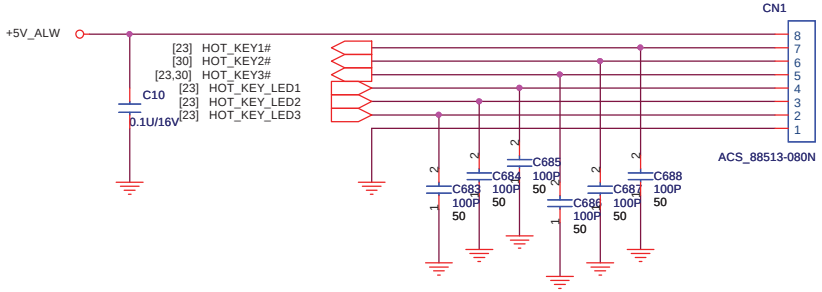

U9
IT8518
LPC
GPIO
SM BUS
PS/2
CIR
UART port
WAKE UP
PWM
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Charge ,BAT
PCH
Thermal
change BAT1_LED
to BAT2_LED
add instant function
change BID2 to ENVDD as BIOS's request
change USB_BACK_EN change to BID0
Inspiron & Vostro R453
Board ID Straps
DIS
Vostro
UMA
Inspiron
R454 (Vostro support Instant ON function)
Vostro
De-POP
Inspiron
POP
For Crystal-Free
Place these caps close to ITE8518.
Quanta Computer Inc.
PROJECT : R03/V03
SIO (ITE8518E)
Monday, January 24, 2011
Sheet 23 of 42



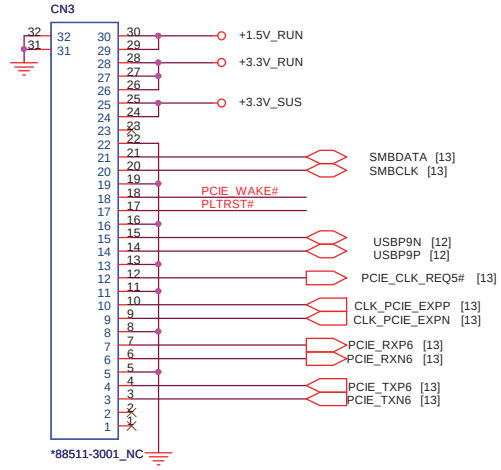


HOTKEY CON



EMI solution

MB to Express Card Board



Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	SIO (ITE8518E)	2A

Date: Monday, January 24, 2011 Sheet 24 of 42

*NOTE: ALC269_VB type add the LDO circuit in IC
VA type: PIN28 作爲MIC之偏壓
PIN31接A-GND

VB type: PIN31 作爲MIC之偏壓
PIN28接CAP作爲內部LDO
output 輸出濾波用

AVDD1, AVDD2 TYP=48mA

AVDD1, AVDD2 TYP=48mA

ALC269Q VB6

ALC269Q-VB6-GR

Analog Plane

Digital Plane

reserve EMI solution

DVDD & DVDD-IO TYP=50mA

del 0ohm NC 0928

PD#=0V : Power down Class D SPK amplifer
PD#=3.3V : Power up Class D SPK amplifer
Internal pulled high.

please close to ALC269 Pin 28

must close to ALC269 Pin12

modify single net GND SIGNAL

Trace width >= 40mil, Trace length < 20cm

Int. Stereo Speakers
5V / 4 Ohm / 2W

L34.L35,L36,L37,
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC

POP noise VB6 fixed,
keep NC first

Reserve RC for EMI

Digital GND Analog GND

AUDIOJACK-SIT_NORMALOPEN_2
Normal Open
HP JACKN

AUDIOJACK-SIT_NORMALOPEN_2
Normal Open
MIC JACK

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	Azelia CODEC	2A
Date: Monday, January 24, 2011	Sheet 25 of 42	

INTERNAL SUBWOOFER AMP Only for 17''

SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz ±70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.

3W

3W 4ohm device(subwoofer)

MAX9759 TQFN 16PIN

MAX9759ETE+

Change to X7R

GAIN1	GAIN2	GAIN
0	0	24dB
1	0	18dB
0	1	12dB
1	1	6dB

MAX4492AUD need to change part?

reserve EMI solution

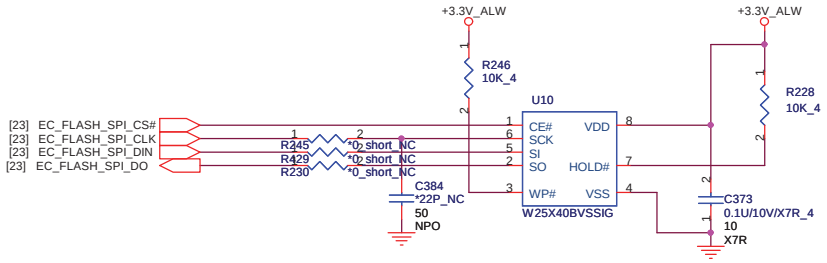
FB_60ohm+-25%_100MHz _3A_0.05ohm DC

Layout Note: Place close to pin 8.

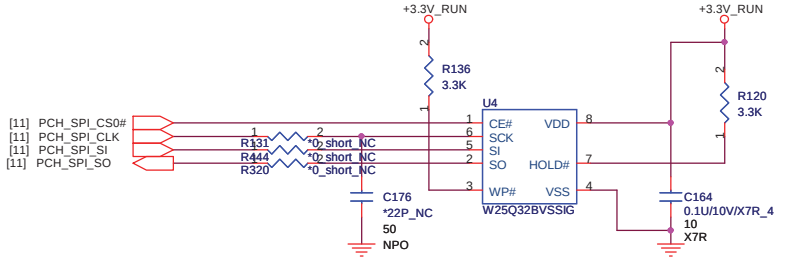
place close to connector side

Quanta Computer Inc.			
PROJECT : R03/V03			
Size	Document Number: AUDIO CONN		Rev 2A
Date: Monday, January 24, 2011	Sheet 26 of 42		

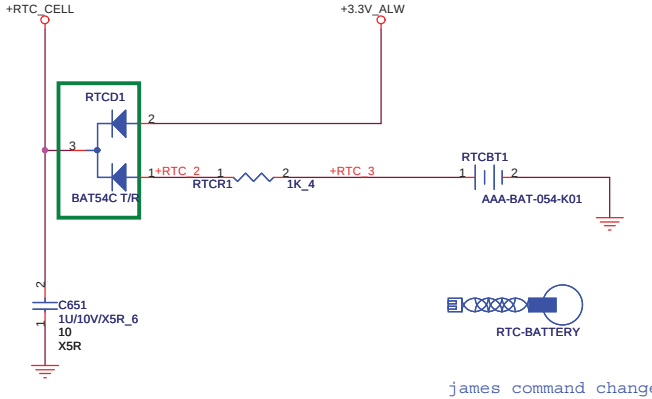
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC

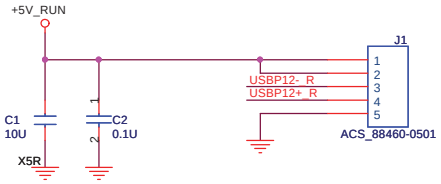


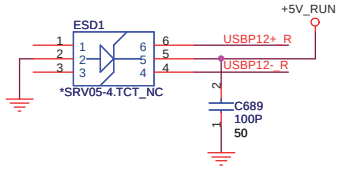
james command change part number

Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Touch Screen Module

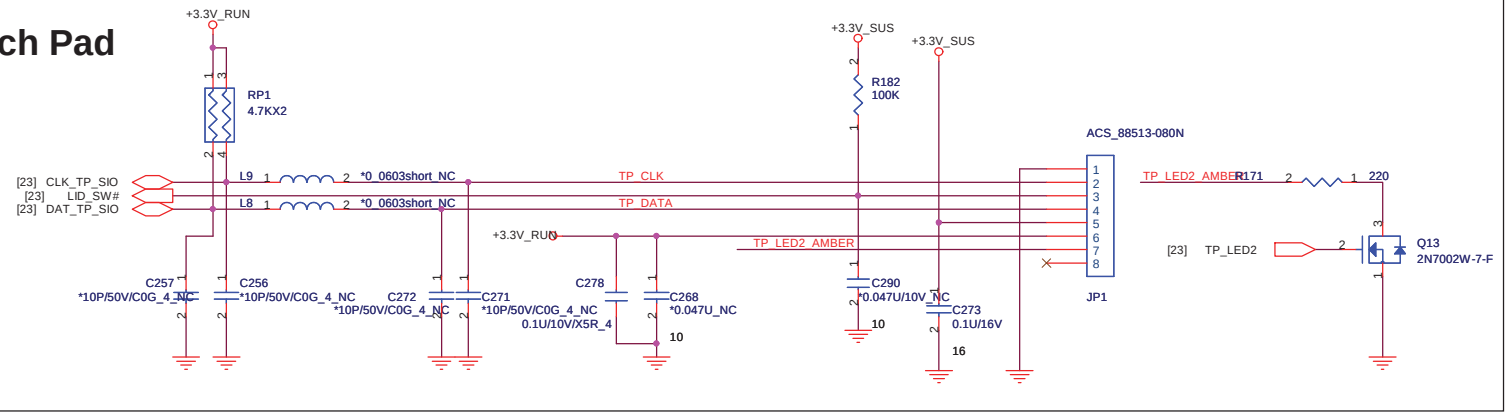
Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
2. Maximum cable resistance on VCC, GND should be 150m ohm.
3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.

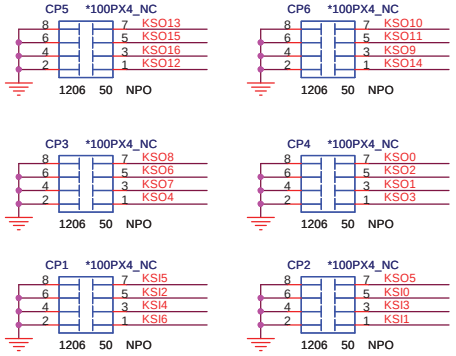




Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: FLASH / RTC	Rev 2A
Date: Monday, January 24, 2011	Sheet 27 of 42	

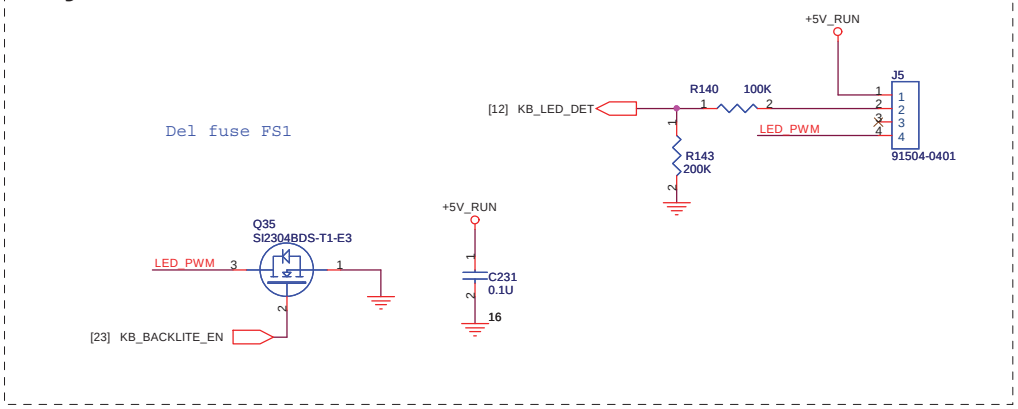
Touch Pad

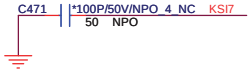




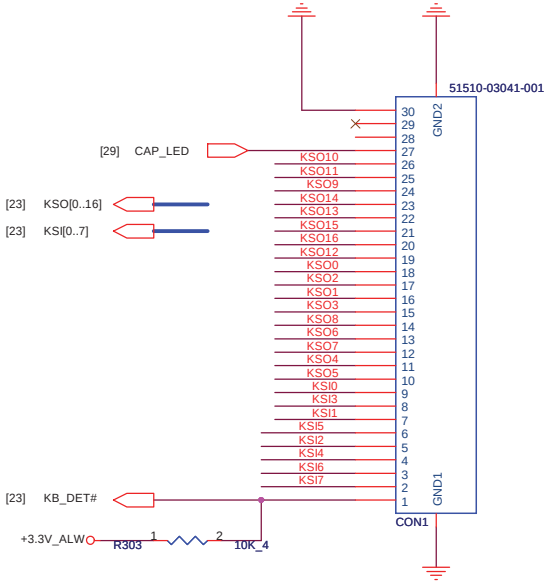
Key board illumination

+KB_LED power trace width >10 mil

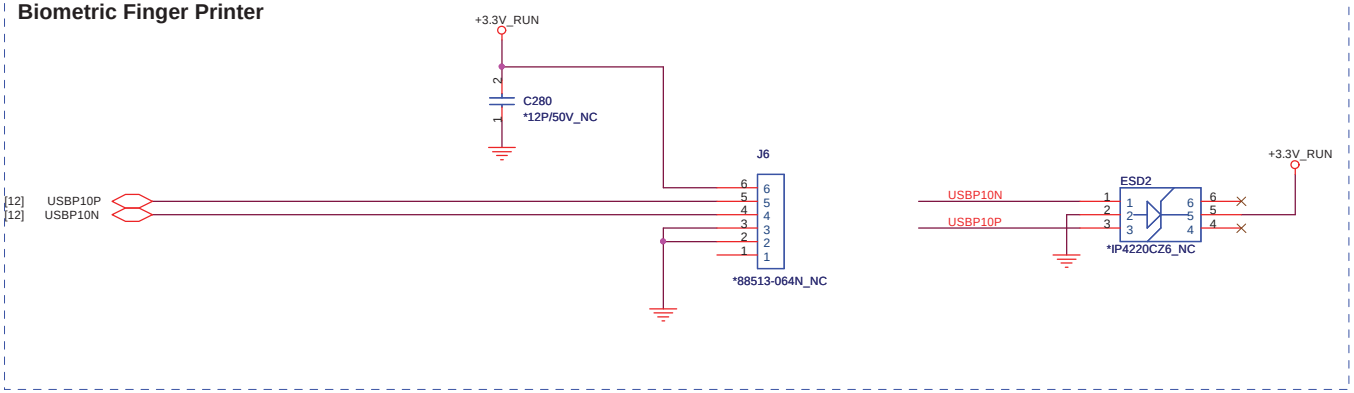




KEYBOARD CONNECTOR

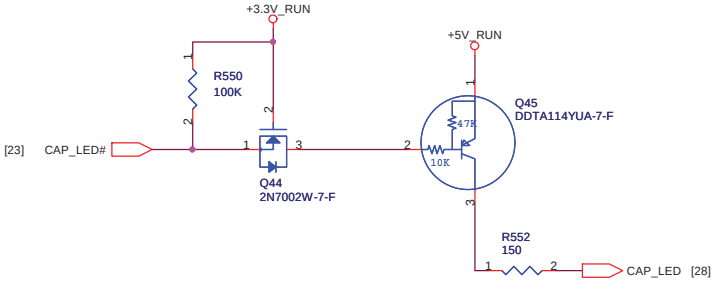


Biometric Finger Printer

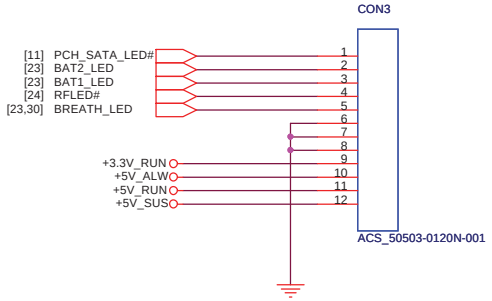


Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: TP / KB	Rev: 2A
Date: Monday, January 24, 2011	Sheet 28 of 42	

CAP lock LED

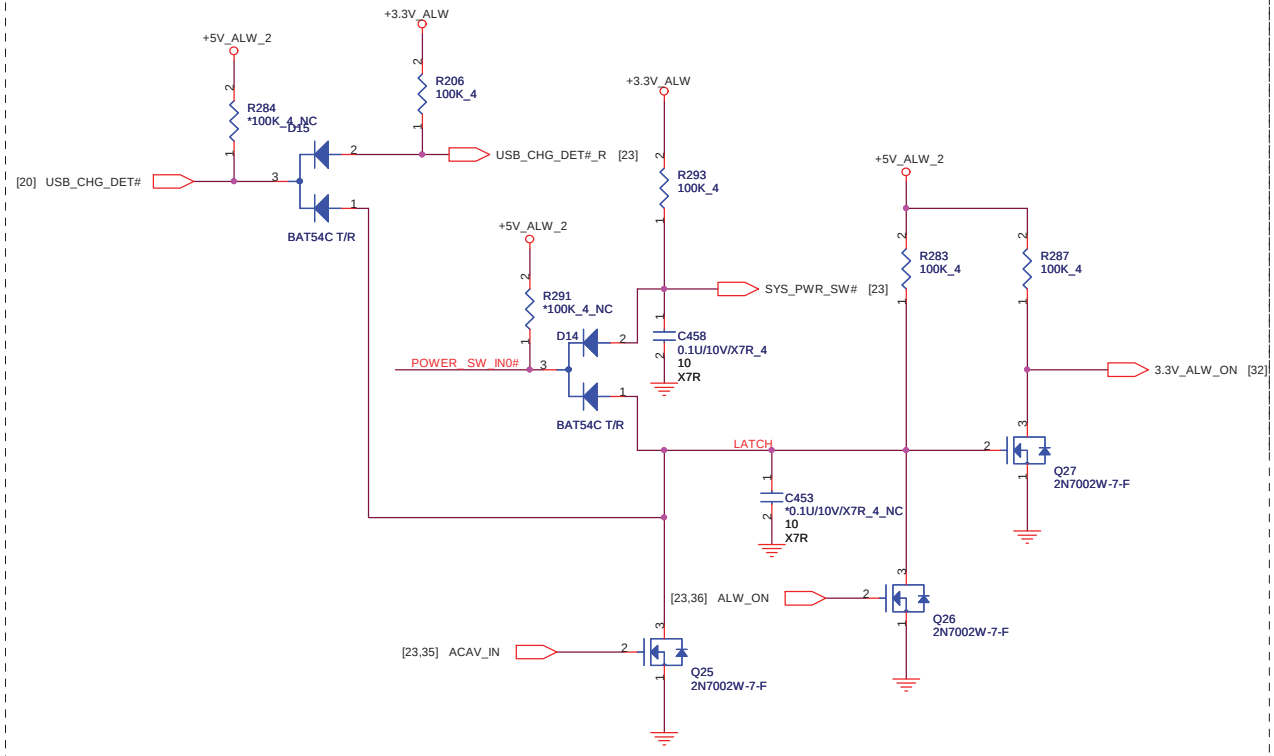


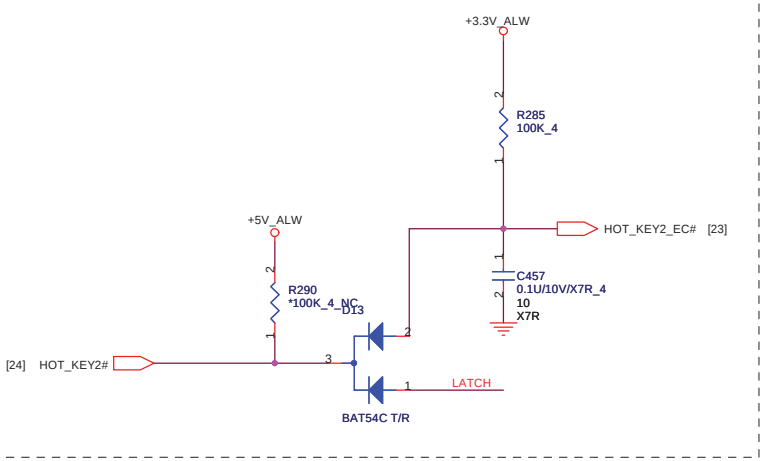
MB to LED Board conn



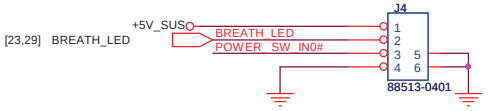
Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: LED	Rev 2A
Date: Monday, January 24, 2011	Sheet 29 of 42	

3VALW ON POWER LOGIC

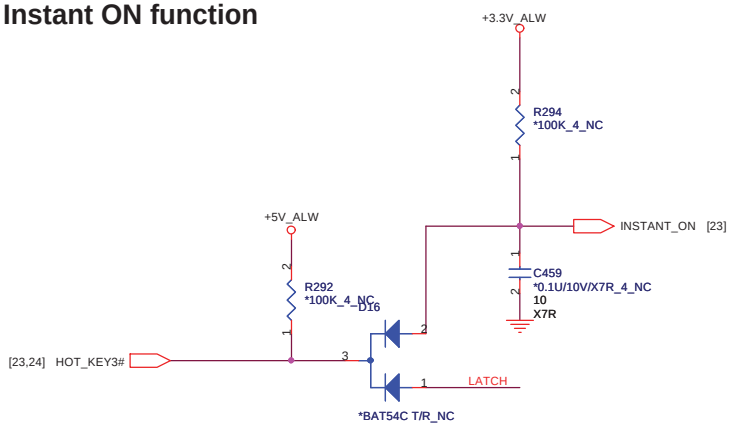




PWR button board form UM7



Instant ON function



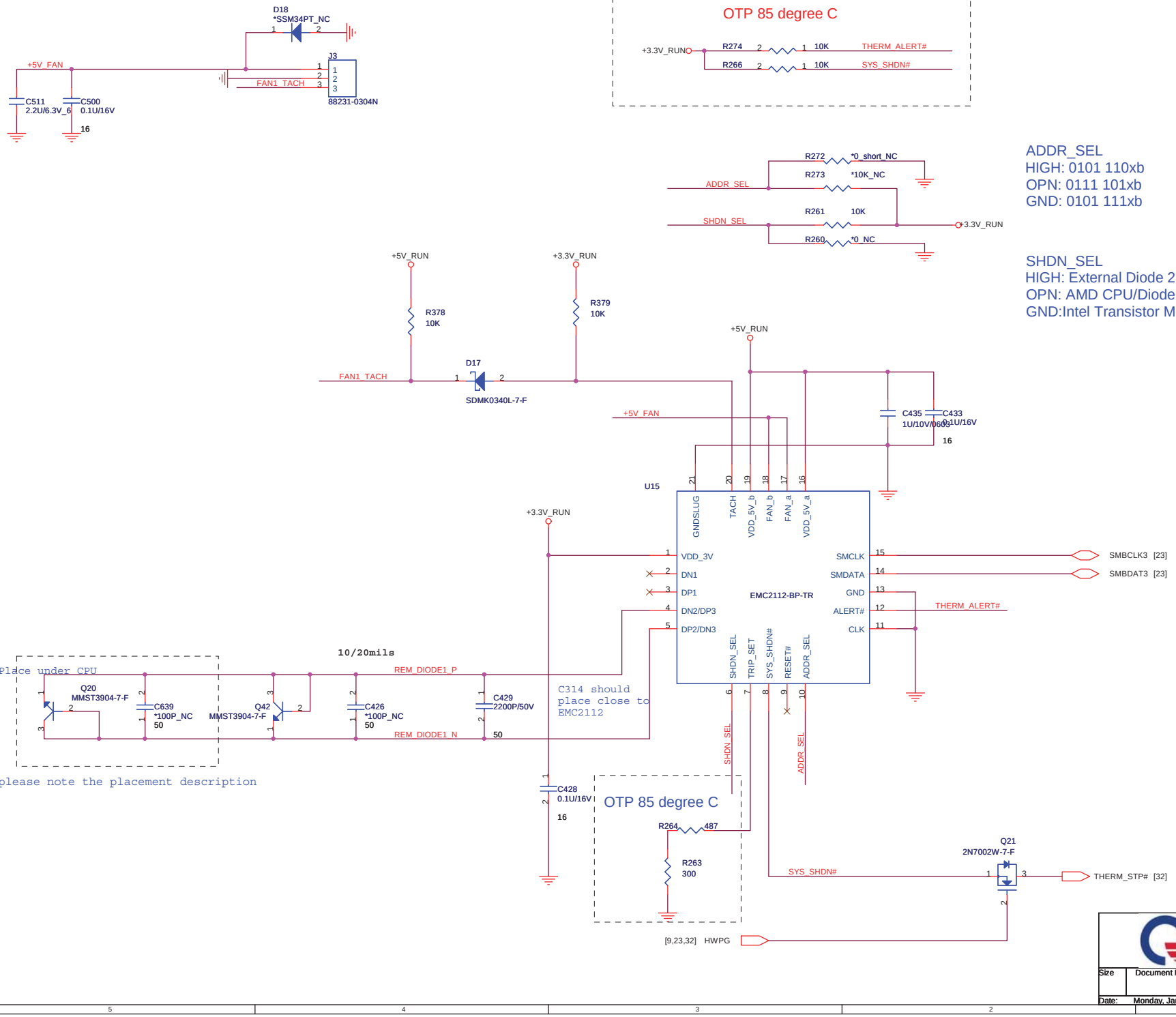
Quanta Computer Inc.

PROJECT : R03/V03

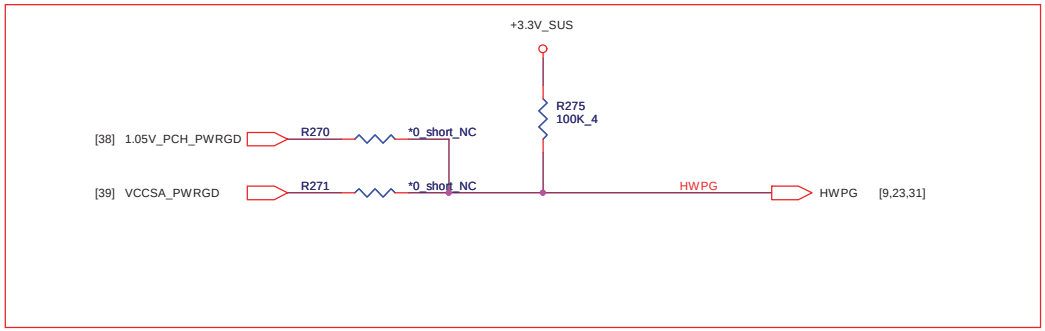
Size	Document Number	Rev
	PWR SW/LED	2A

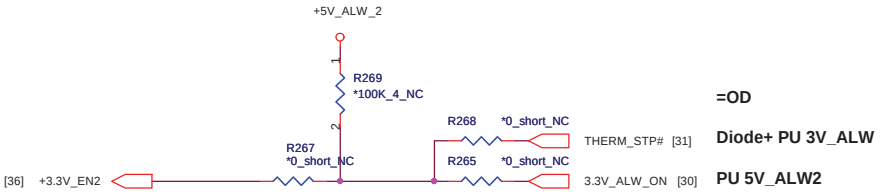
Date: Monday, January 24, 2011 Sheet 30 of 42

FAN CONTROL



Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: FAN & THERMAL	Rev: 2A
Date: Monday, January 24, 2011	Sheet 31 of 42	





Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	System Reset Circuit	2A
Date: Monday, January 24, 2011	Sheet 32 of 42	

H2
H-TC236BC197D110P2
H-TC236BC197D110P2

H7
H-TC236BC197D110P2
H-TC236BC197D110P2

H14
h-tc335bc276d126p2
h-tc335bc276d126p2

H5
h-tc335bc276d126p2
h-tc335bc276d126p2

H8
h-c276d177p2
h-c276d177p2

H12
h-c276d126p2
h-c276d126p2

H19
H-C276IN130D110P2
H-C276IN130D110P2

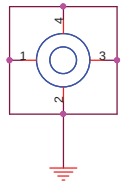
H17
H-C276IN130D110P2
H-C276IN130D110P2

H16
h-c354d126p2
h-c354d126p2

H15
h-t354i130b296d110p2
H-T354I130B296D110P2

CPU bracket

H10 Intel-cpu-bkt2
Intel-cpu-bkt2



H18
H-C142D142N
H-C142D142N

H6, H11 on the button side

H20
h-c295d126p2
h-c295d126p2

H6
h-tc197bc236d102p2
h-tc236bc197d102p2

H11
h-tc197bc236d102p2
h-tc236bc197d102p2

H4
H-T236I130B276D110P2
H-T236I130B276D110P2

H24
H-TC276BC236D110P2
H-TC276BC236D110P2

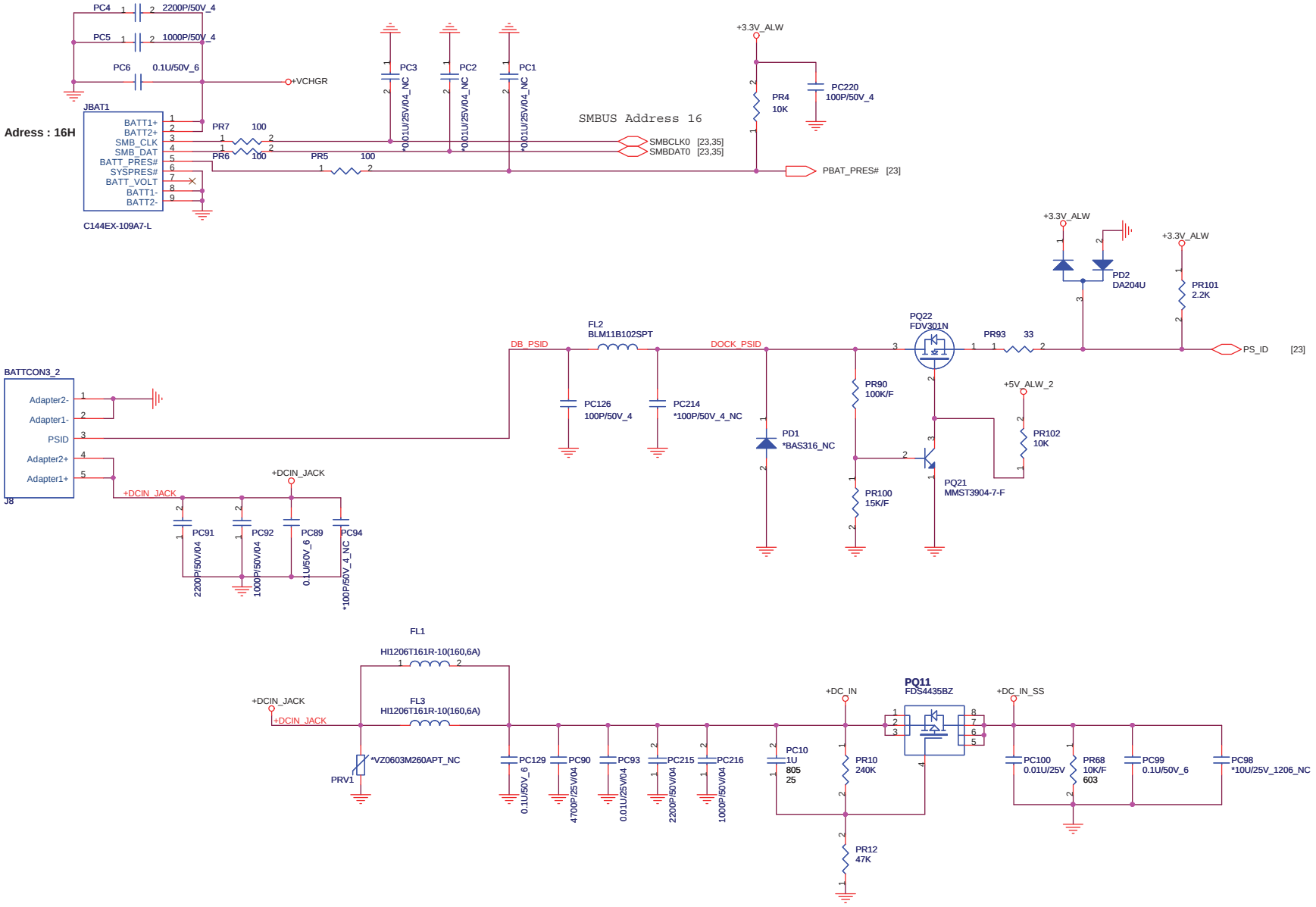
H1
h-c142d142n
h-c142d142n

H3
H-T315I130B276D110P2
H-TC335BC276D126P2

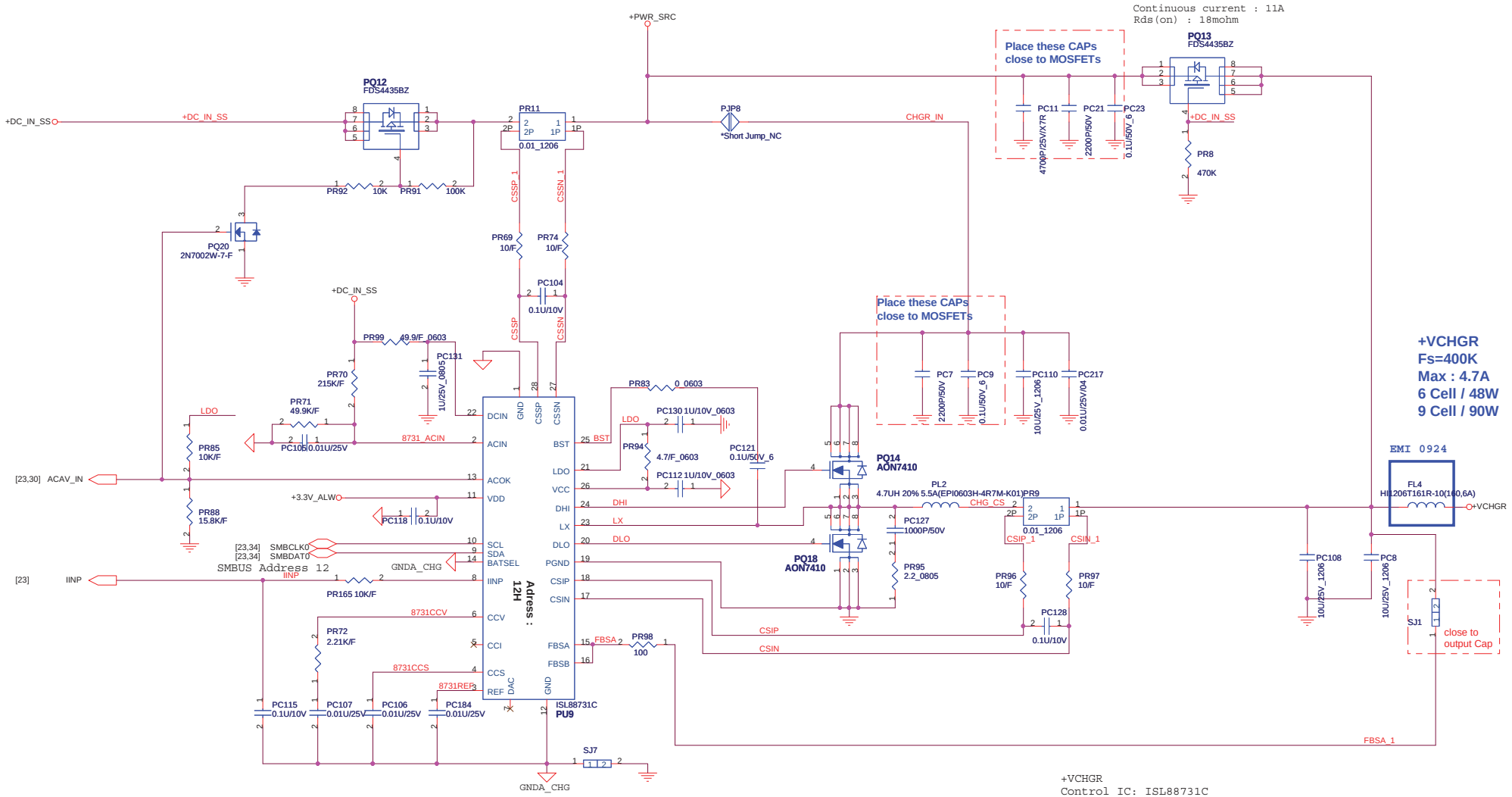
H22
h-c205d91pt
H-C276D110PT

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	SCREW PAD	2A
Date: Monday, January 24, 2011	Sheet 33 of 42	



Quanta Computer Inc.		
PROJECT : R03/V03		
Size	Document Number: DCIN,BATT CONNECTOR	Rev: 2A
Date: Monday, January 24, 2011	Sheet 34 of 42	



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	Charger (ISL88731C)	2A

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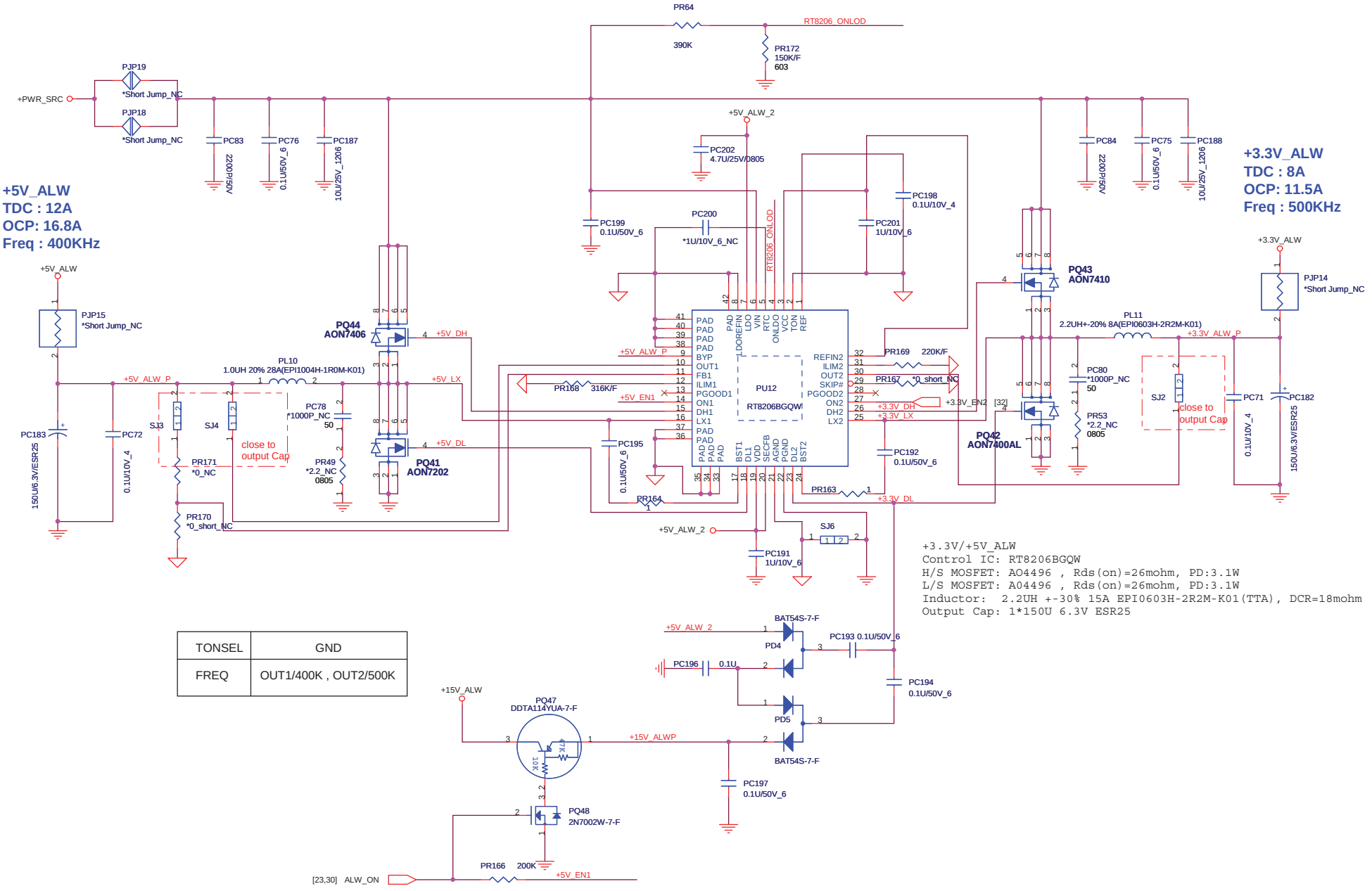
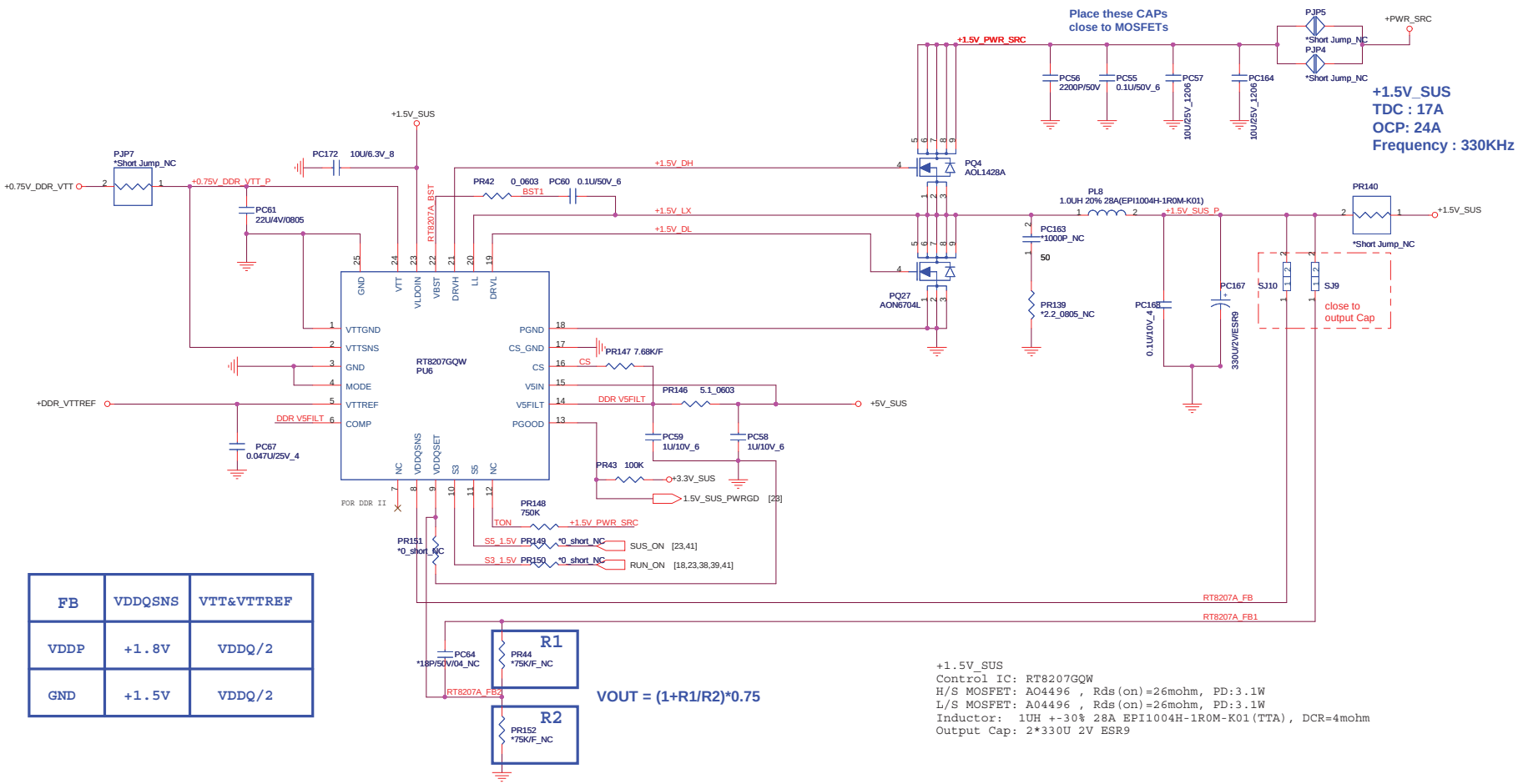
DC/DC +3V_ALW/+5V_ALW /+15V_ALW



TONSEL	GND
FREQ	OUT1/400K , OUT2/500K

Quanta Computer Inc.	
PROJECT : R03/V03	
Size	Document Number: SYSTEM 5V/3V (RT8206BGQW) — Rev 2A
Date: Monday, January 24, 2011	Sheet 36 of 42



FB	VDDQSNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

+1.5V_SUS
Control IC: RT8207GQW
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 2*330U 2V ESR9

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

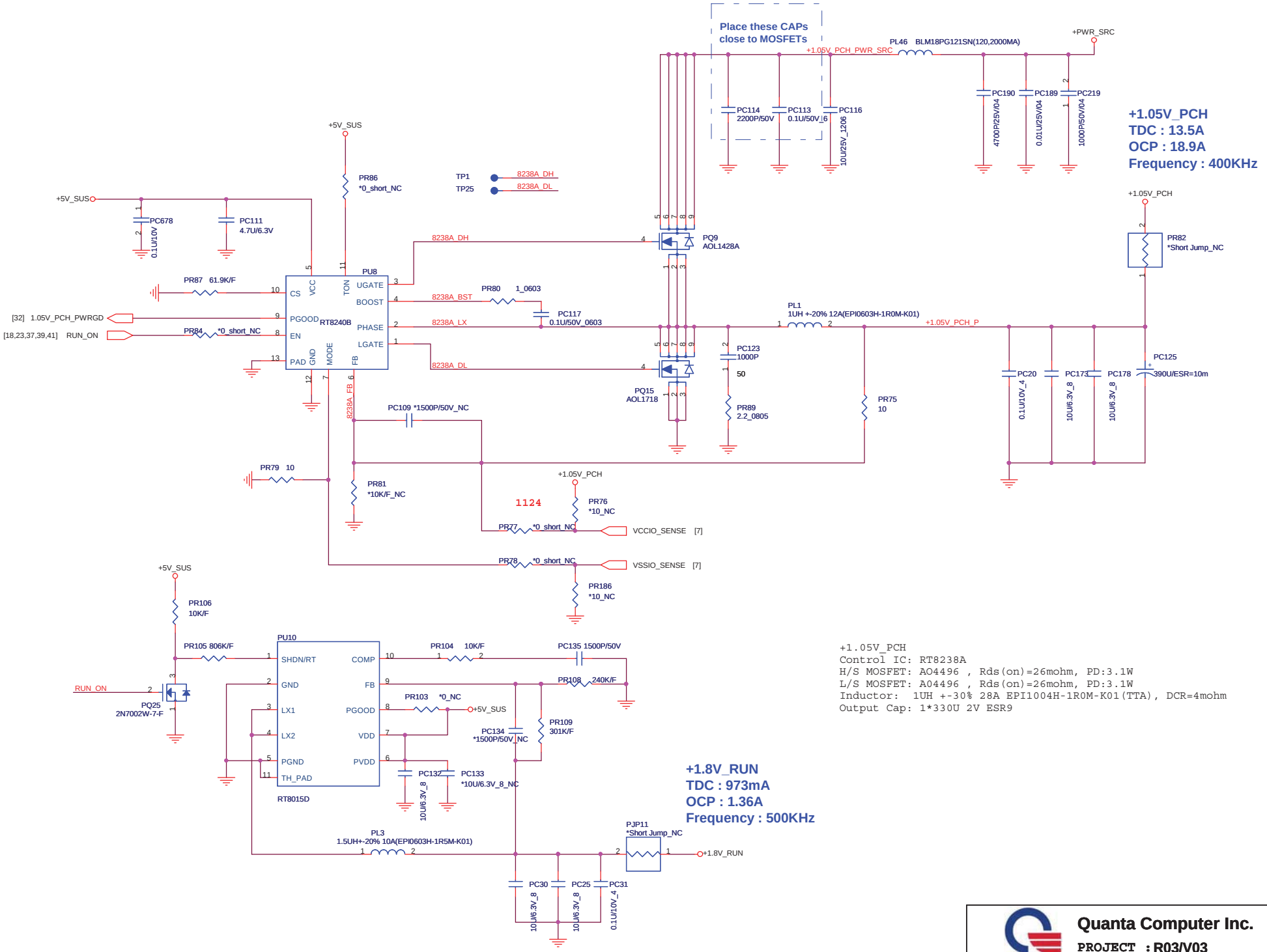
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : R03/V03
Size | Document Number: DDR3 +1.5V_SUS(RT8207AGQW) | Rev 2A
Date: Monday, January 24, 2011 | Sheet 37 of 42


Place these CAPs close to MOSFETs
+1.05V_PCH
TDC : 13.5A
OCP : 18.9A
Frequency : 400KHz
+1.8V_RUN
TDC : 973mA
OCP : 1.36A
Frequency : 500KHz
+1.05V_PCH
Control IC: RT8238A
H/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
L/S MOSFET: AO4496 , Rds(on)=26mohm, PD:3.1W
Inductor: 1UH +-30% 28A EPI1004H-1R0M-K01(TTA), DCR=4mohm
Output Cap: 1*330U 2V ESR9
Quanta Computer Inc.
PROJECT : R03/V03
Size
Document Number
+1.05V_PCH(RT8209A)
Rev 2A
Date: Monday, January 24, 2011
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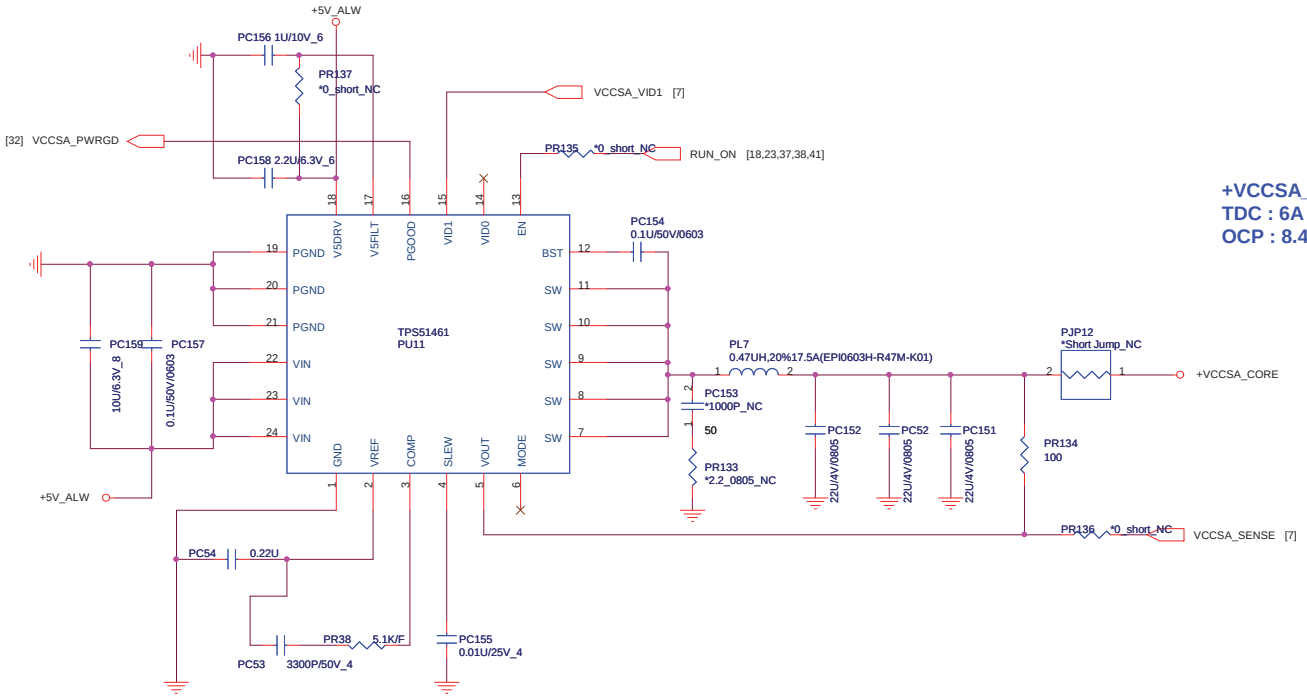
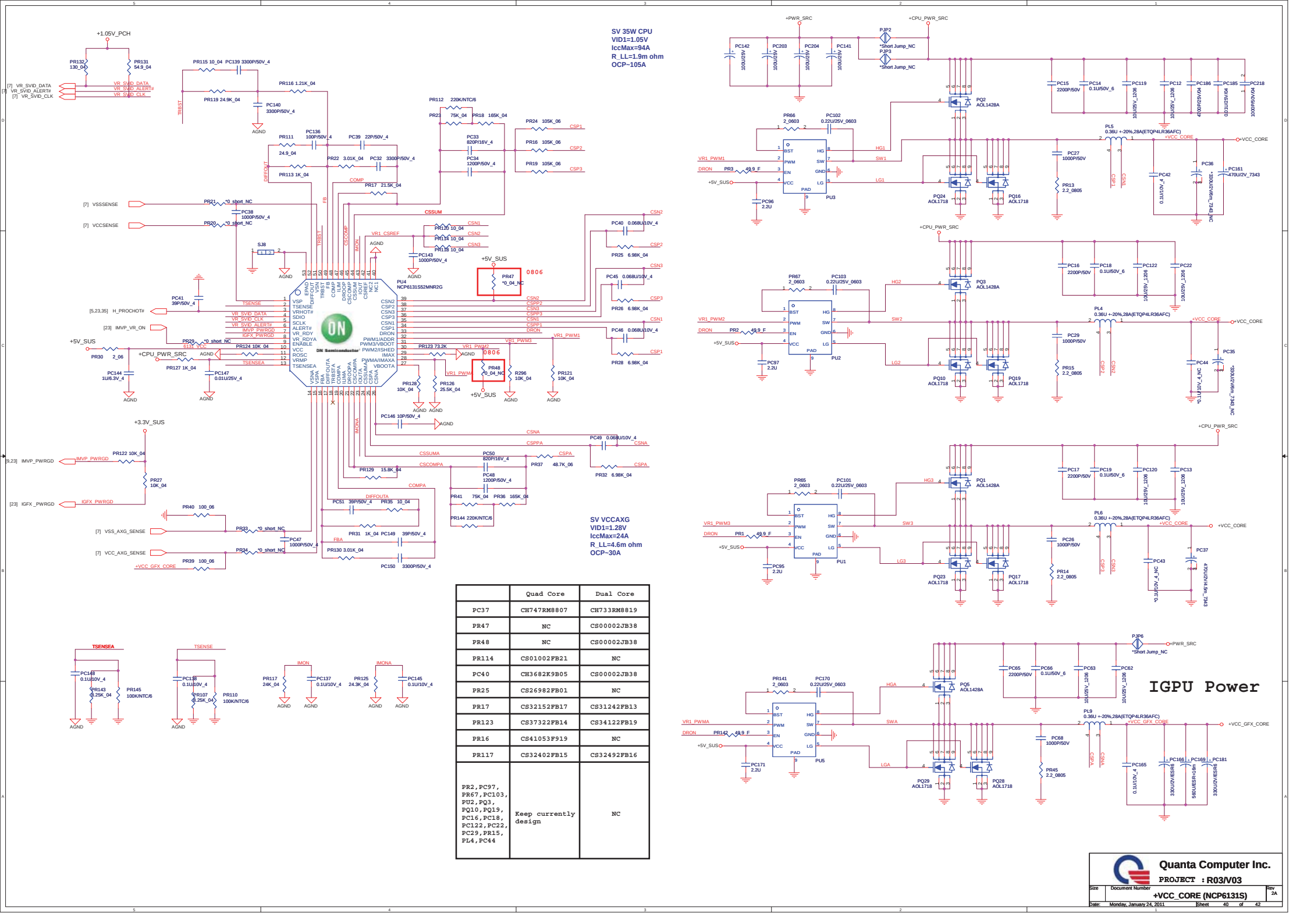


+VCCSA_CORE
TDC : 6A
OCP : 8.4A

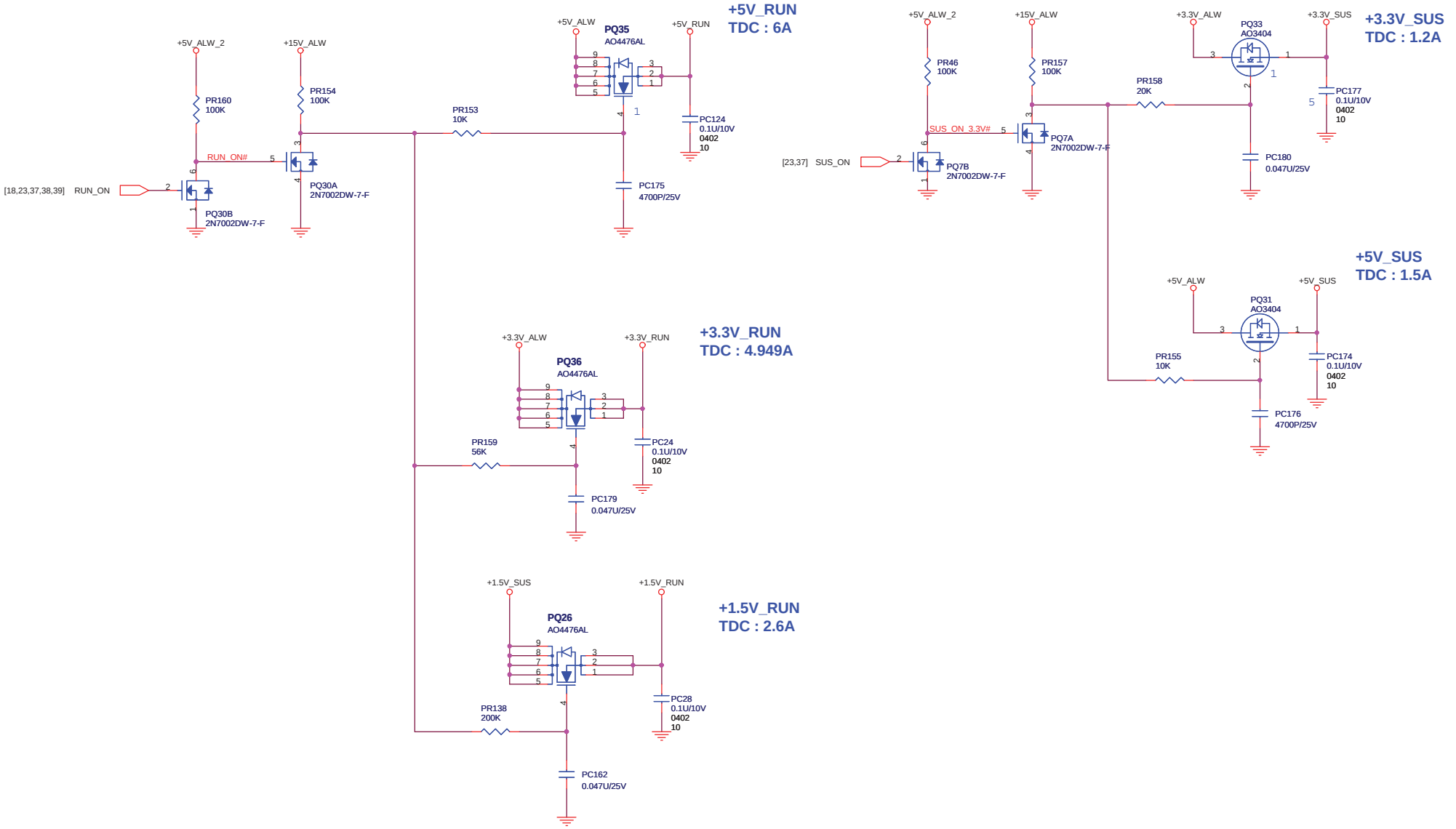
+VCCSA	VCCSA_VID1
0.8V	High
0.9V	Low

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	VCCSA (TPS51461)	2A
Date: Monday, January 24, 2011	Sheet 39 of 42	



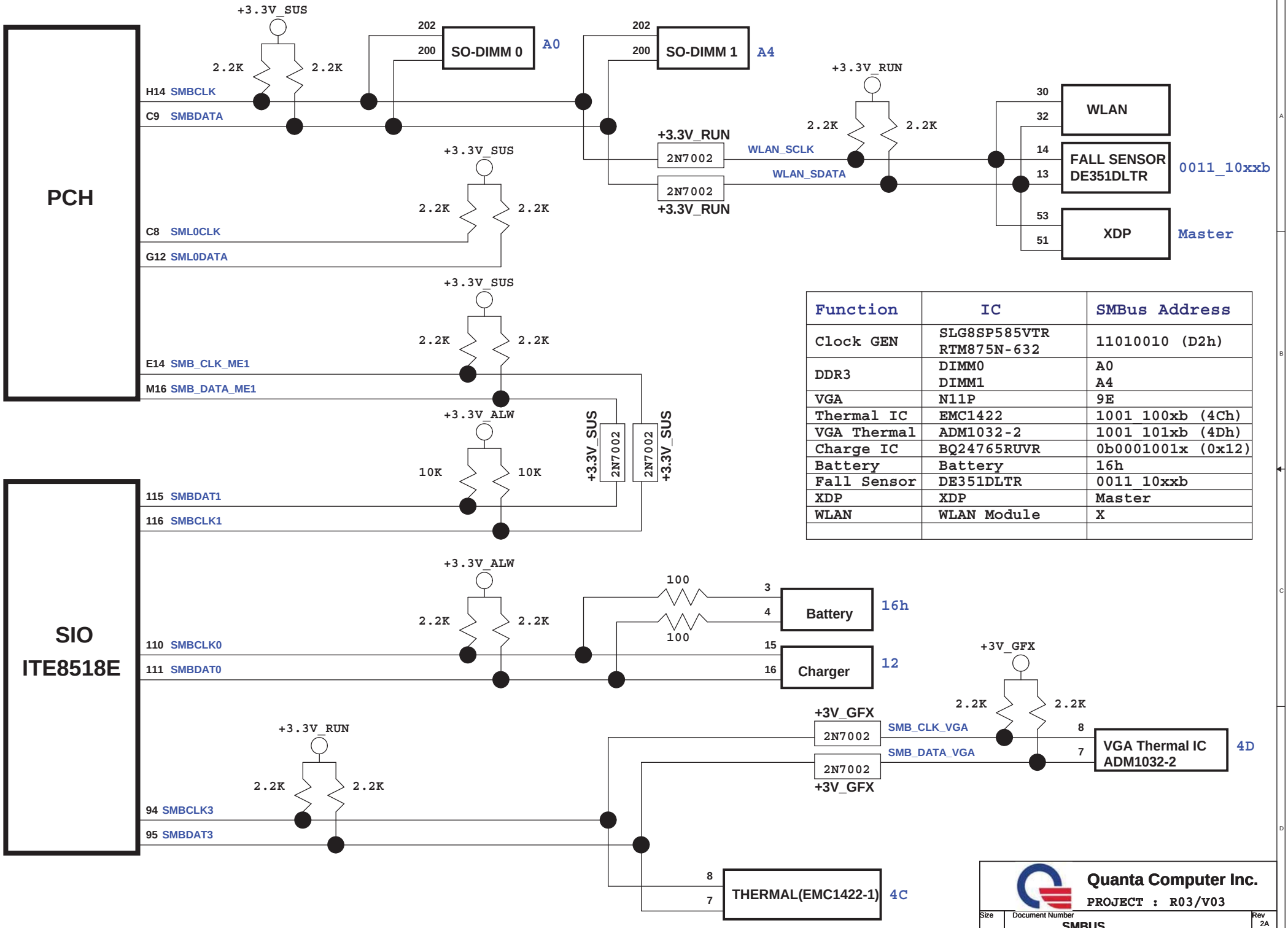
	Quad Core	Dual Core
PC37	CH747RM8807	CH733RM8819
PR47	NC	CS00002JB38
PR48	NC	CS00002JB38
PR114	CS01002FB21	NC
PC40	CH3682K9B05	CS00002JB38
PR25	CS26982FB01	NC
PR17	CS32152FB17	CS31242FB13
PR123	CS37322FB14	CS34122FB19
PR16	CS41053F919	NC
PR117	CS32402FB15	CS32492FB16
PR2,PC97, PR67,PC103, PU2,PQ3, PQ10,PQ19, PC16,PC18, PC122,PC22, PC29,PR15, PL4,PC44	Keep currently design	NC



Quanta Computer Inc.

PROJECT : R03/V03

Size	Document Number	Rev
	RUN / SUS POWER SW	2A
Date: Monday, January 24, 2011	Sheet 41 of 42	



Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001 100xb (4Ch)
VGA Thermal	ADM1032-2	1001 101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

Quanta Computer Inc.
PROJECT : R03/V03

Size	Document Number	Rev
	SMBUS	2A

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