DR2 17.3" Schematics Document

uFCPGA Mobile Penryn

Intel Cantiga-GM + ICH9M

2009-05-18

REV : -1

DY : Nopop Component

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Title: Cover Page

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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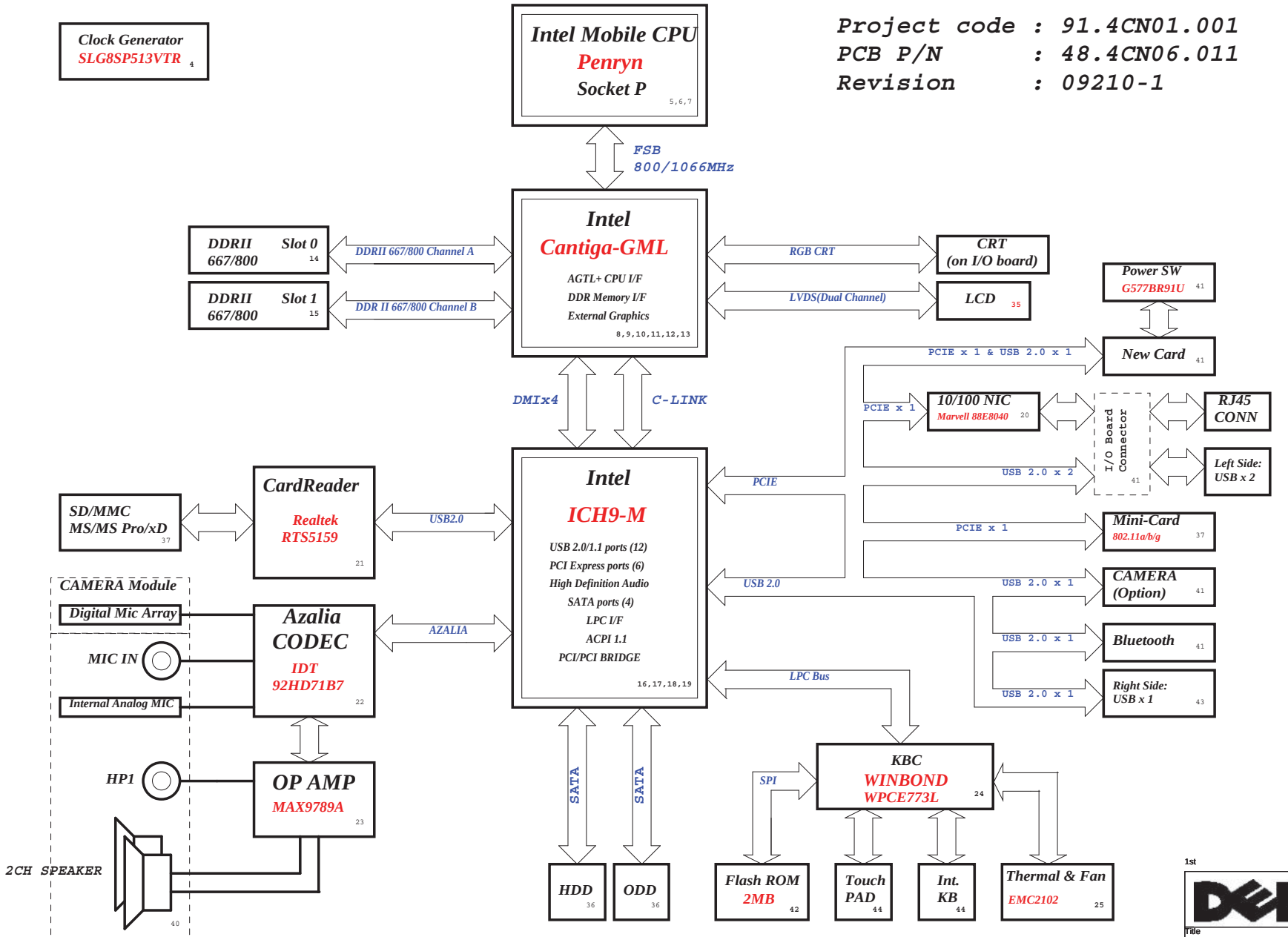
Roberts Block Diagram

Project code : 91.4CN01.001
PCB P/N : 48.4CN06.011
Revision : 09210-1



CPU DC/DC ISL6266A 28,29	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51117 30	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC MAX17020 27	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 31	
INPUTS	OUTPUTS
+PWR_SRC	+1.8V_SUS +0.9V_DDR_VTT +V_DDR_MCH_REF

SYSTEM DC/DC APL5912 32	
INPUTS	OUTPUTS
+1.8V_SUS	+1.5V_RUN

SYSTEM DC/DC LDO 34	
INPUTS	OUTPUTS
+5V_ALW	+5V_RUN
+3.3V_ALW	+3.3V_RUN

MAXIM CHARGER MAX8731A 26	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Title: Block Diagram

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK.	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Cofig Registers: offset 224h). This signal has weak internal pull-down.
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h).
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h).
GPIO20	Reserved.	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK.	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK.	Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8).
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller.
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality(Default)**
CFG9	PCIE Graphics Lane	0 = Reserved Lanes, 15->0, 14->1 ect.. **1 = Normal operation (Default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) **11 = Disabled (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 = Digital display Port and PCIe are operating simulataneously via the PEG port
SDVO _CTRLDATA	SDVO Present	**0 = No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

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Title: Table of Content

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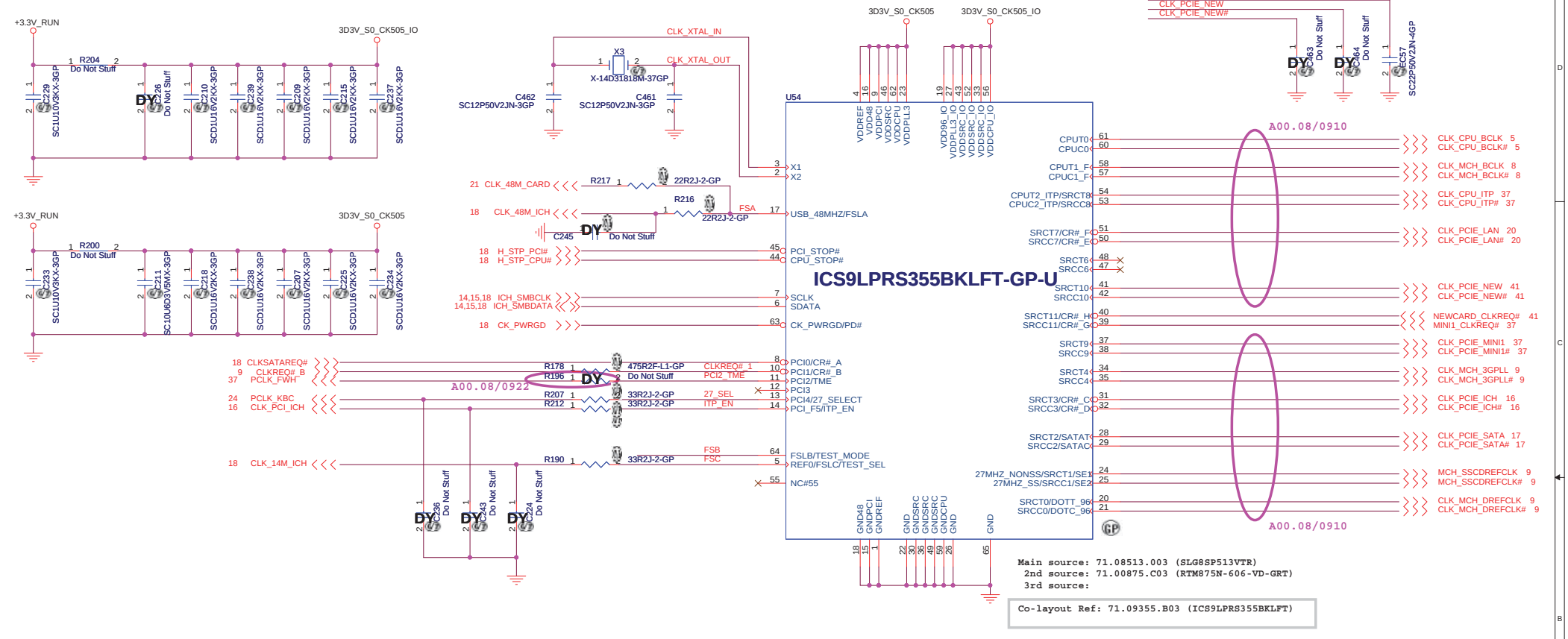
SSID = CLOCK

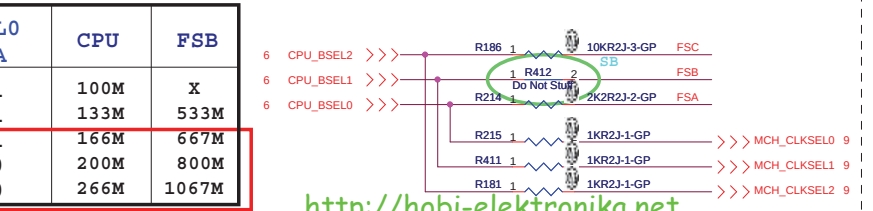


ITP_EN	Output
0	SRC8
1	CPU_ITP

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

27_SEL	PIN 20	PIN 21	
0	DOT96T	DOT96C	GM45
1	SRCT0	SRCC0	PM45

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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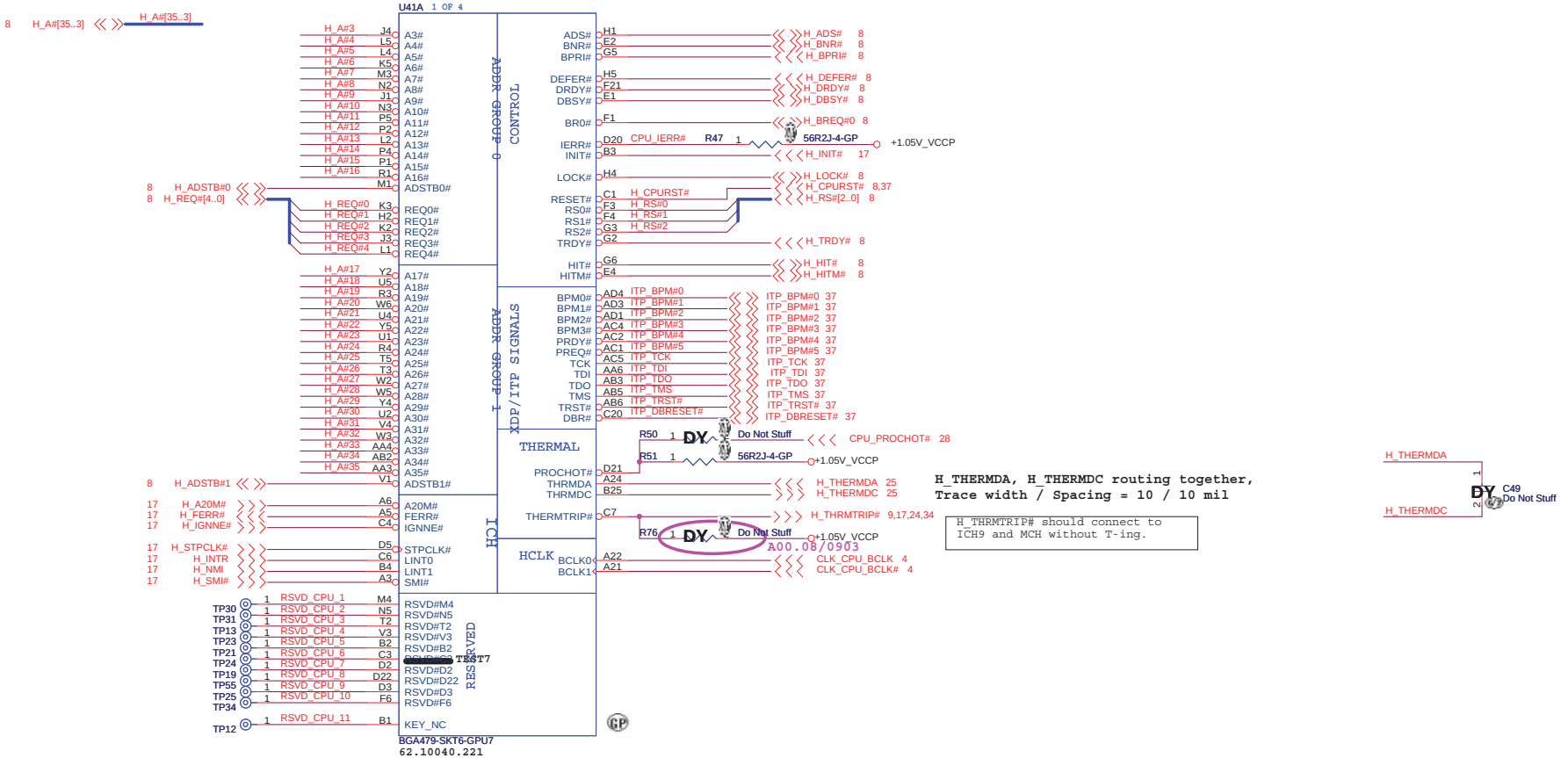
Title: Clock Generator SLG8SP513VTR
Size: Custom | Document Number: DR2 17" UMA | Rev: -1
Date: Monday, May 18, 2009 | Sheet 4 of 59

SSID = CPU



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect to ICH9 and MCH without T-ing.

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Title: CPU-FSB(1/3)

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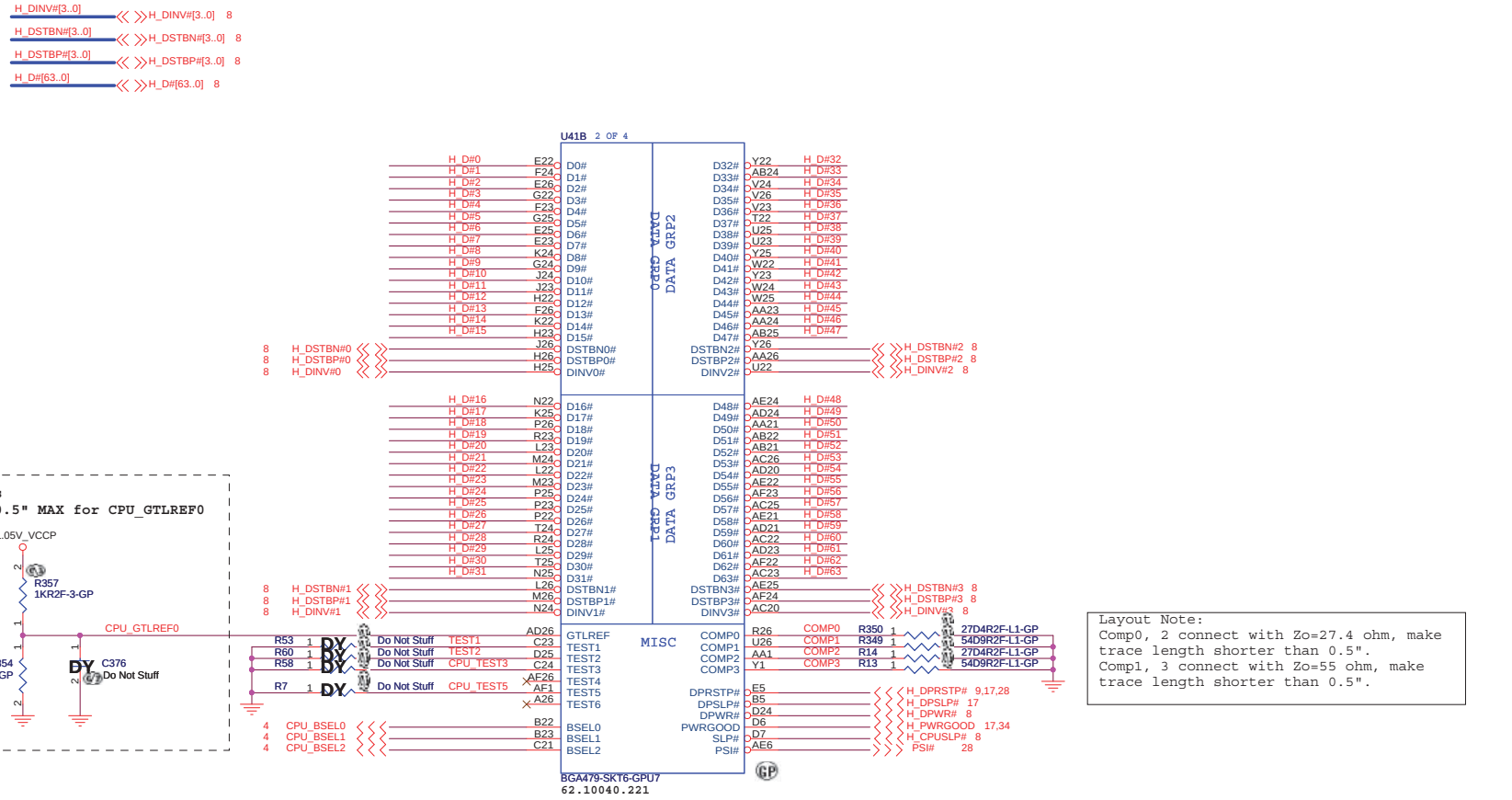
SSID = CPU



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Title: CPU-FSB(2/3)

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SSID = CPU

+VCC_CORE

+VCC_CORE

U41C 3 OF 4

BGA479-SKT6-GPU7
62.10040.221

+VCC_CORE

C10 SC22U6D3V5MX-2GP

+VCC_CORE

C24 SC22U6D3V5MX-2GP

+VCC_CORE

C336 SC22U6D3V5MX-2GP

+1.05V_VCCP

C8 SCD1U10V2KX-4GP

layout note: "+1.5V_VCCA" as short as possible

+1.5V_VCCA

+1.5V_RUN

R356 Do Not Stuff

C374 SCD01U16V2KX-3GP

C377 SC10U6D3V5MX-3GP

Layout Note:
Place as close as possible to the CPU VCCA pin.

CPU_VID[6..0] 28

R311 100R2F-L1-GP-U

+VCC_CORE

VCC_SENSE 28

R302 100R2F-L1-GP-U

VSS_SENSE 28

VCC_SENSE and VSS_SENSE lines should be of equal length.

U41D 4 OF 4

BGA479-SKT6-GPU7
62.10040.221

NCTF

TP10

TP224

TP20

TP56

http://hobi-elektronika.net

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Title: CPU-Power(3/3)

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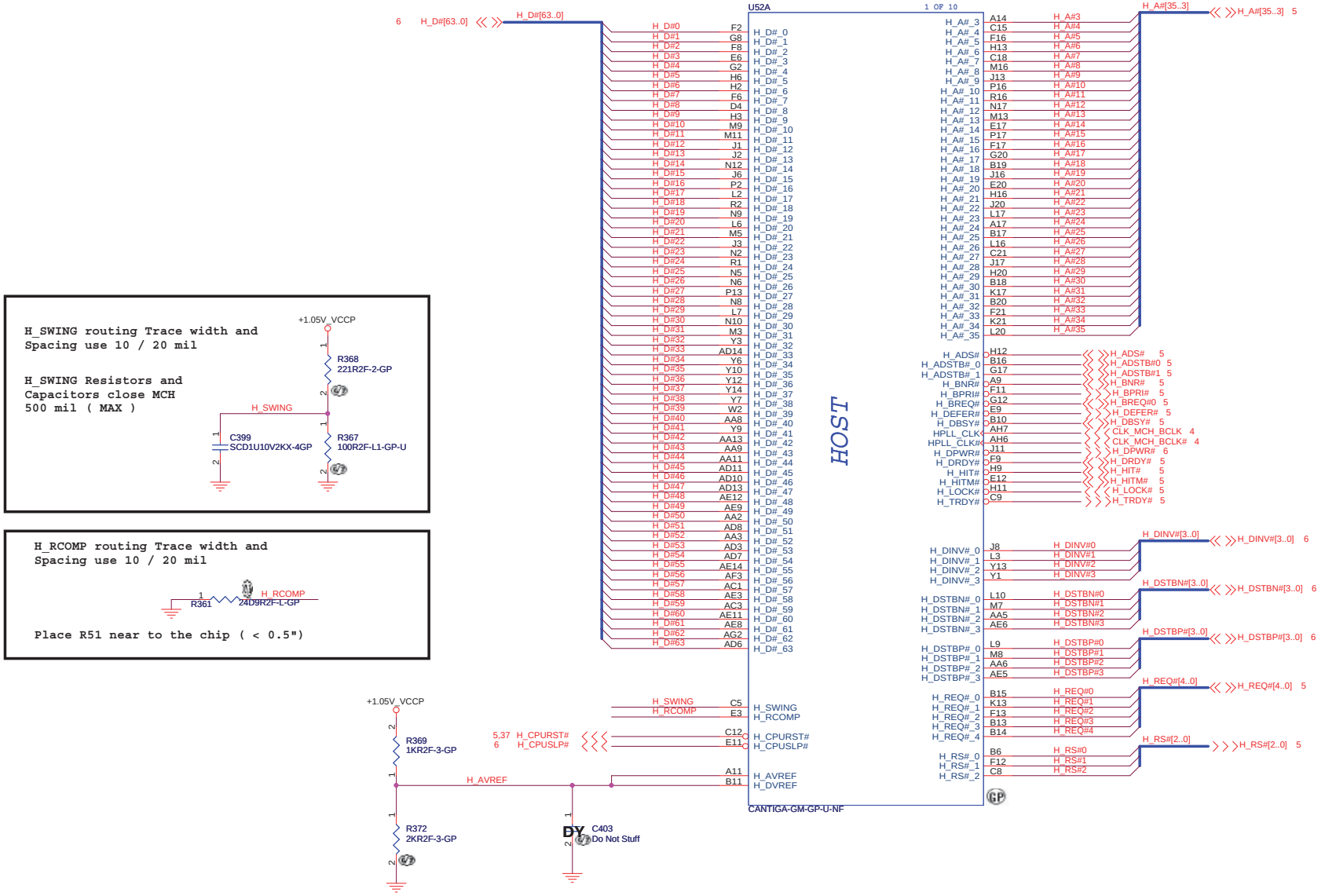
SSID = MCH



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Title: Cantiga-HOST(1/6)

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SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

U52B — 2 OF 10

RESERVED#M36 RESERVED#N36 RESERVED#R33 RESERVED#T33 RESERVED#AH9 RESERVED#AH10 RESERVED#AH12 RESERVED#AH13 RESERVED#K12 RESERVED#AL34 RESERVED#AK34 RESERVED#AN35 RESERVED#AM35 RESERVED#T24 RESERVED#B31 RESERVED#B2 RESERVED#M1 RESERVED#AY21 RESERVED#BG23 RESERVED#BF23 RESERVED#BH18 RESERVED#BF18

RSVD

SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#

DDR CLK/ CONTROL/COMPENSATION

DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#

CLK

DMI_RXN_0..3 DMI_RXP_0..3 DMI_TXN_0..3 DMI_TXP_0..3

DMI

CFG_0..20

CFG

GFX_VID_0..4 GFX_VR_EN

GRAPHICS VID

PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

PM

CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

ME

DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#

MISC

HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

HDA

NC#BG48 NC#BF48 NC#BD48 NC#BC48 NC#BH47 NC#BG47 NC#BE47 NC#BH46 NC#BF46 NC#BG45 NC#BH44 NC#BH43 NC#BH6 NC#BH5 NC#BG4 NC#BH3 NC#BF3 NC#BH2 NC#BG2 NC#BE2 NC#BG1 NC#BF1 NC#BD1 NC#BC1 NC#F1 NC#A47

NC

CANTIGA-GM-GP-U-NF

M_CLK_DDR0..3 14/15 — M_CKE0..3 14/15 — M_CS0#..M_CS3# 14/15 — M_ODT0..3 14/15 — M_RCOMPP M_RCOMPN — SM_RCOMP_VOH SM_RCOMP_VOL — SM_REXT R374 499R2F-2-GP — CLK_MCH_DREFCLK CLK_MCH_DREFCLK# MCH_SSCDREFCLK MCH_SSCDREFCLK# — CLK_MCH_3GPLL CLK_MCH_3GPLL# — DMI_TXN0..3 16 — DMI_TXP0..3 16 — DMI_RXN0..3 16 — DMI_RXP0..3 16 — GFX_VID_0..4 — CL_CLK0 18 CL_DATA0 18 M_PWROK 18 CL_RST#0 18 MCH_CLVREF — CLKREQ#_B 4 MCH_ICH_SYNC# 18 TSATN#

+1.8V_SUS

R380 80D6R2F-L-GP — R377 80D6R2F-L-GP — R122 1KR2F-3-GP — R116 3K01R2F-3-GP — R119 1KR2F-3-GP — C159 SCD01U16V2KX-3GP SC2D2U10V3KX-1GP — C162 SCD01U16V2KX-3GP — C145 SCD01U16V2KX-3GP SC2D2U10V3KX-1GP — C151 SCD01U16V2KX-3GP

+V_DDR_MCH_REF — R142 Do Not Stuff — R145 Do Not Stuff

+1.05V_VCCP — R370 56R2J-4-GP — R126 1KR2F-3-GP — R130 499R2F-2-GP — C175 SCD1U10V2KX-4GP

+3.3V_RUN — R371 Do Not Stuff — Q19 Do Not Stuff — TSATN#_KBC — TSATN#_KBC 24

R131 10KR2J-3-GP — CLKREQ#_B

MCH_CLVREF ~= 0.35V

+3.3V_RUN

R104 R128 R117 R121 R383 R112 R111 R102 R382 R375 R101 R105 R103 — Do Not Stuff — CFG11 CFG18 CFG19 CFG20 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG12 CFG13 CFG16

RN20 SRN10KJ-5-GP — PM_EXTTS#0 PM_EXTTS#1

FSB setting

MCH_CLKSEL0 MCH_CLKSEL1 MCH_CLKSEL2

TP86 TP88 TP84 TP85 TP87

CFG3 CFG4 CFG5 CFG6 CFG7 CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15 CFG16 CFG17 CFG18 CFG19 CFG20

18 PM_SYNC# 6,17,28 H_DPRSTP# 14 PM_EXTTS#0 15 PM_EXTTS#1

18,24,25 PM_PWROK — RSTIN#

16,20,21,24,37,41 PLT_RST# — R94 100R2F-L1-GP-U — C94 Do Not Stuff

5,17,24,34 H_THRMTRIP# 18,28 DPRSLPVR

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Title: Cantiga-DMI/CFG(2/6)

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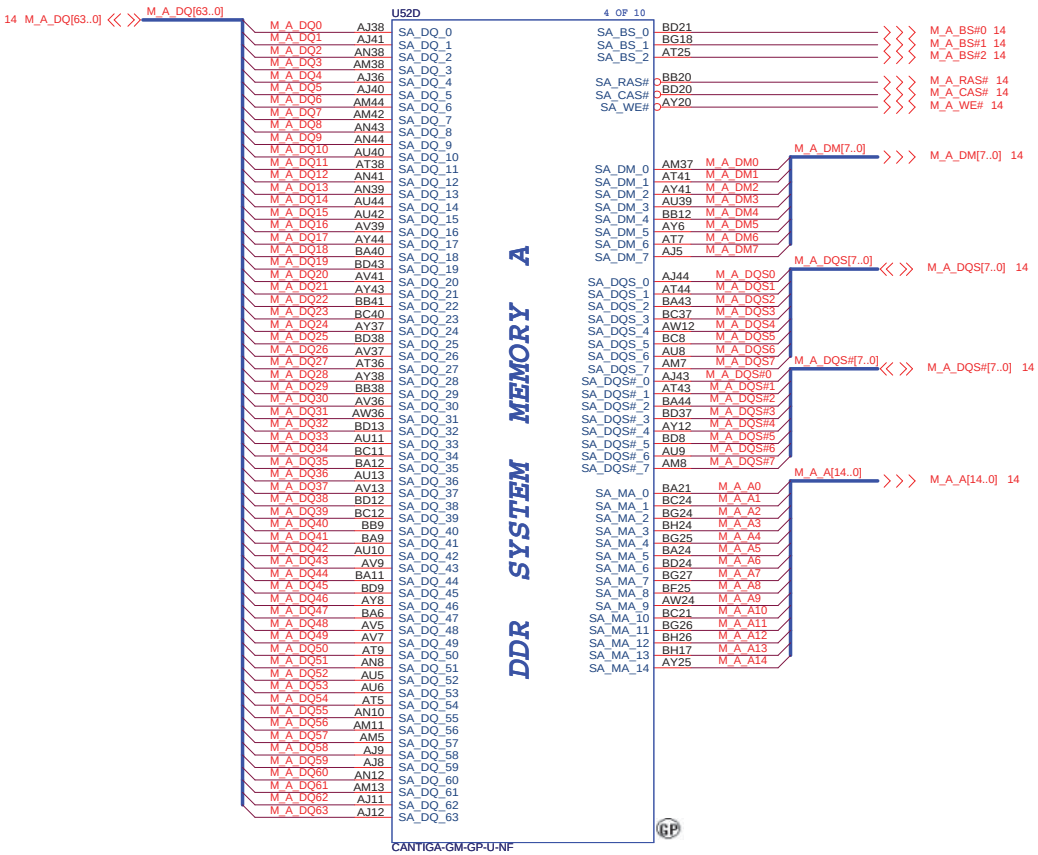
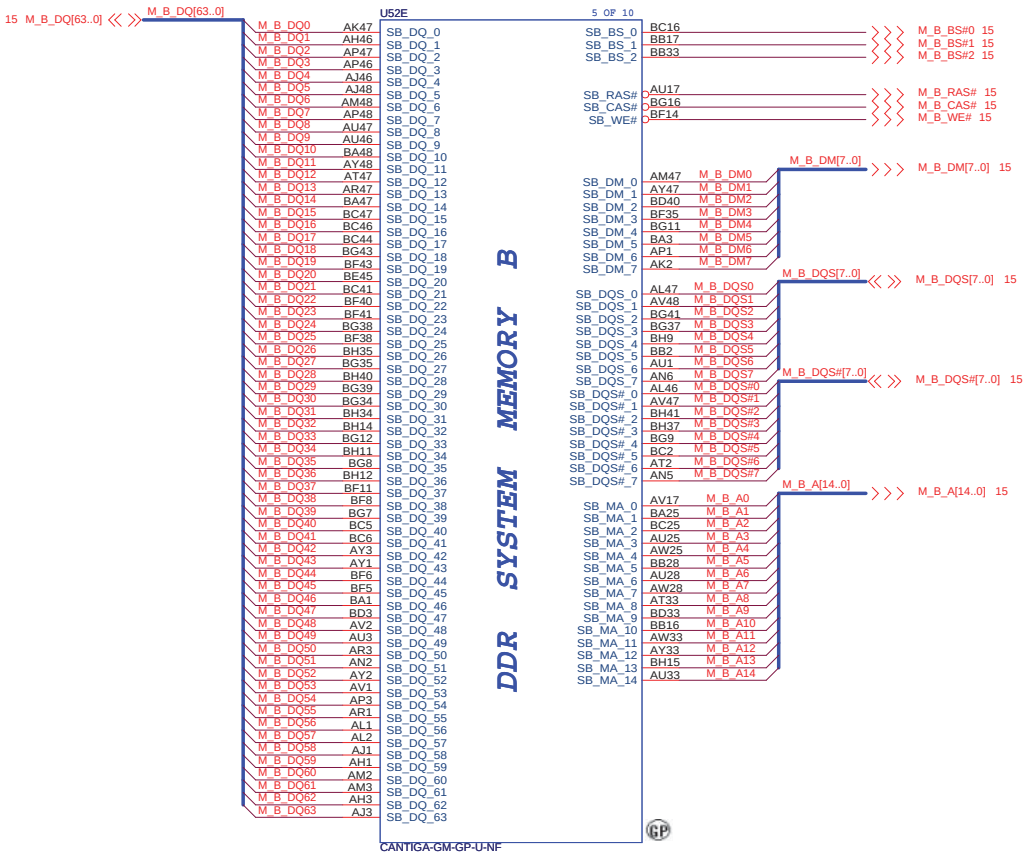
SSID = MCH





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Size	Document Number	Rev
Custom	DR2 17" UMA	-1

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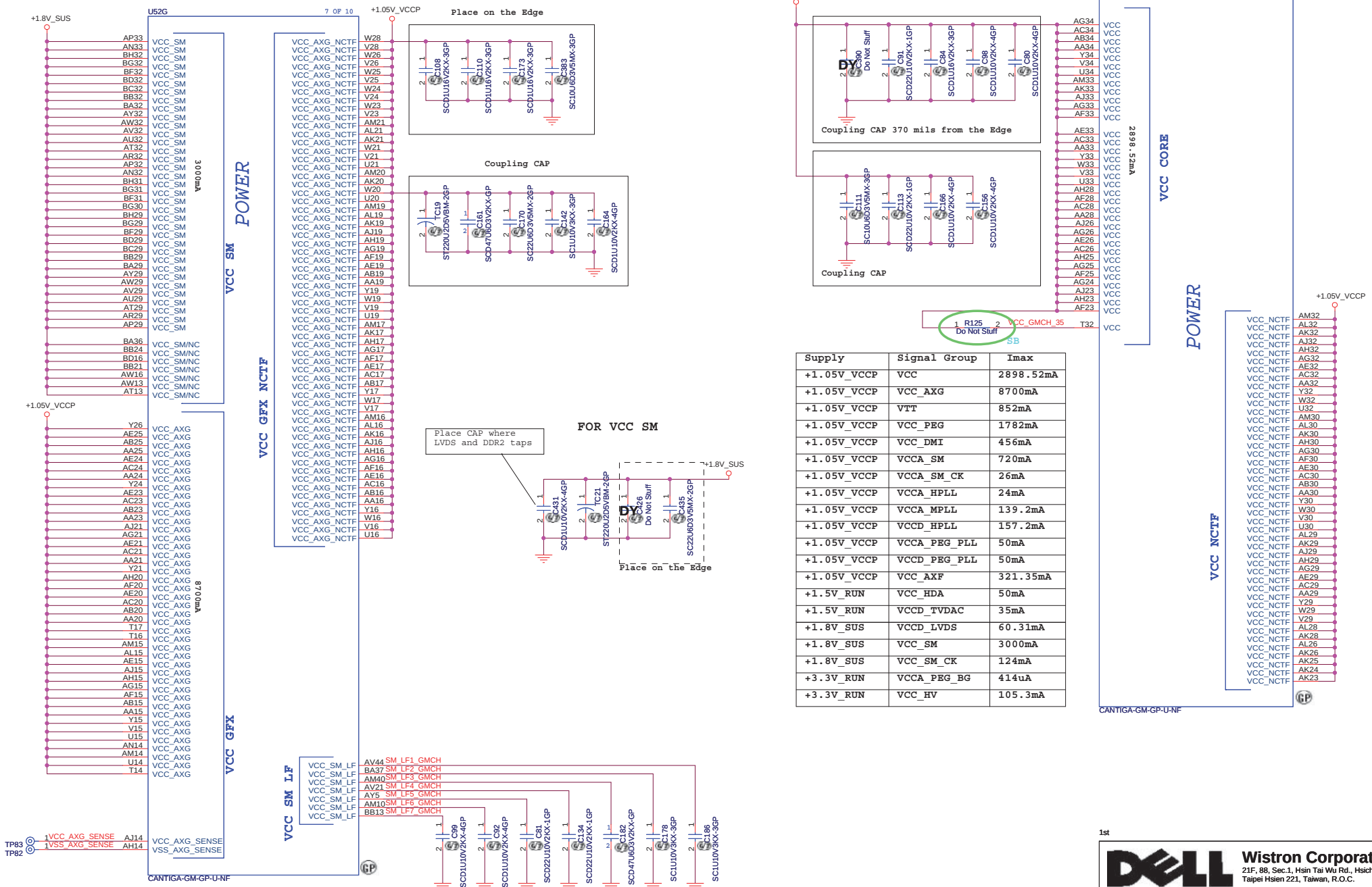
SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	2898.52mA
+1.05V_VCCP	VCC_AXG	8700mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCC_HDA	50mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCCD_LVDS	60.31mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+3.3V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

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Title: Cantiga-Power(4/6)

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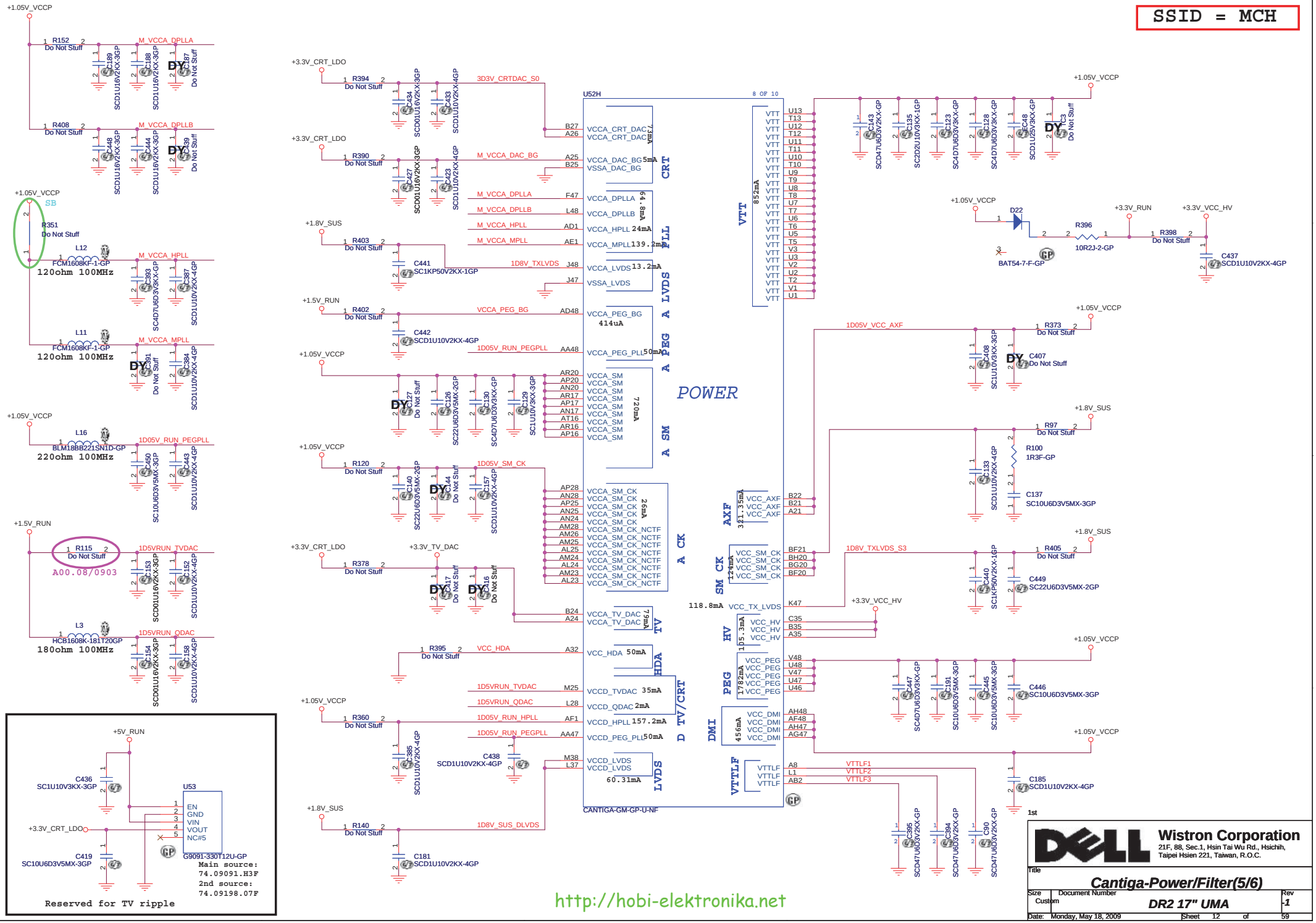
SSID = MCH



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Title: Cantiga-Power/Filter(5/6)
Size: Custom | Document Number: DR2 17" UMA | Rev: -1
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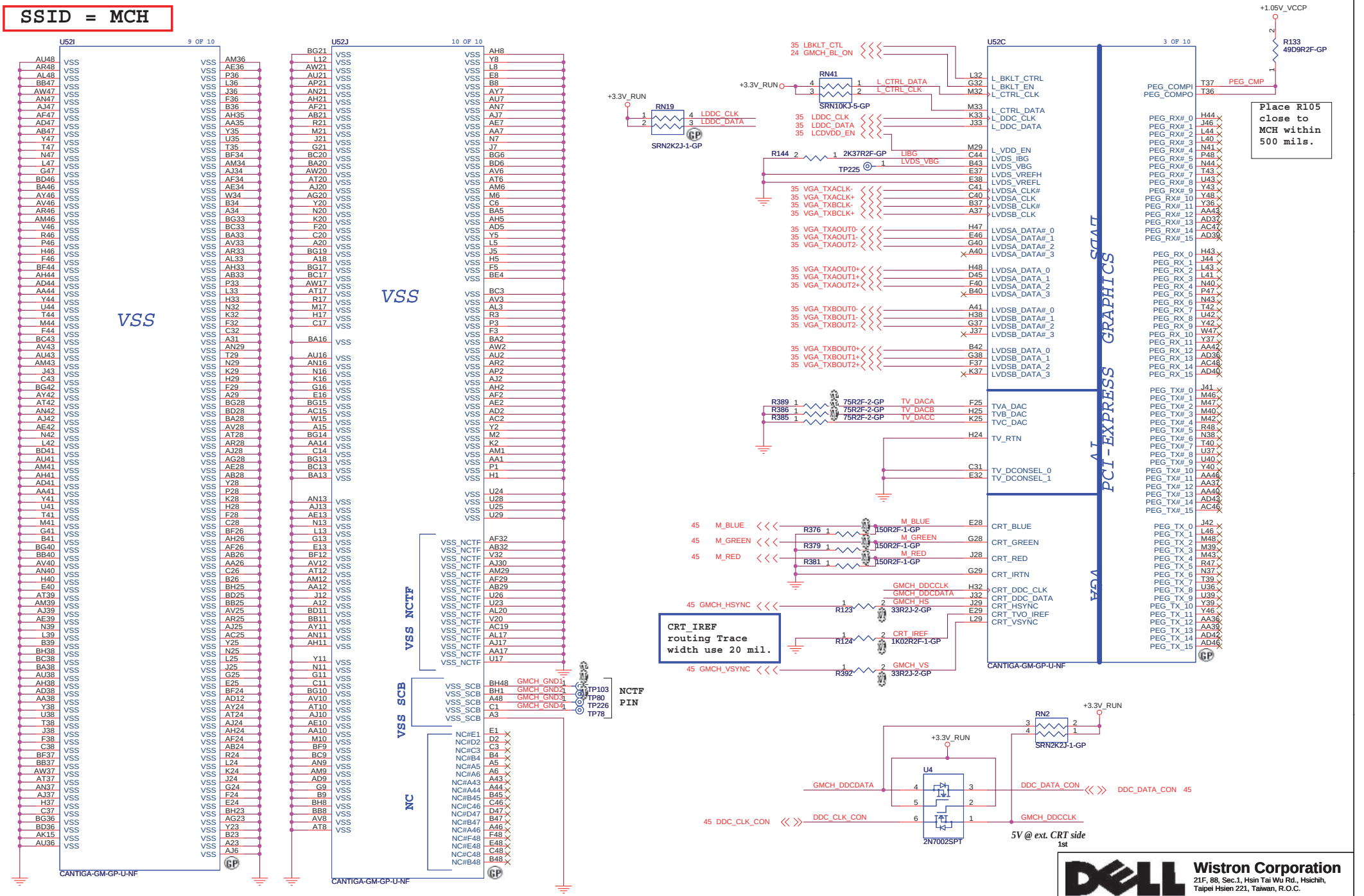
1st

SSID = MCH



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Cantiga-GND/LVDS/VGA(6/6)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 13 of 59

SSID = MEMORY

10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[14..0]

DM2

M_A_A0	102	A0	RAS#	108	M_A_RAS# 10
M_A_A1	101	A1	WE#	109	M_A_WE# 10
M_A_A2	100	A2	CAS#	113	M_A_CAS# 10
M_A_A3	99	A3			
M_A_A4	98	A4	CS0#	110	M_CS0# 9
M_A_A5	97	A5	CS1#	115	M_CS1# 9
M_A_A6	94	A6			
M_A_A7	92	A7	CKE0	79	M_CKE0 9
M_A_A8	93	A8	CKE1	80	M_CKE1 9
M_A_A9	91	A9			
M_A_A10	105	A10/AP	CK0	30	M_CLK_DDR0 9
M_A_A11	90	A11	CK0#	32	M_CLK_DDR#0 9
M_A_A12	89	A12			
M_A_A13	116	A13	CK1	164	M_CLK_DDR1 9
M_A_A14	86	A14	CK1#	166	M_CLK_DDR#1 9
	84	A15			
M_A_BS#2	85	A16/BA2	DM0	10	M_A_DM0
			DM1	26	M_A_DM1
M_A_BS#0	107	BA0	DM2	52	M_A_DM2
M_A_BS#1	106	BA1	DM3	67	M_A_DM3
			DM4	130	M_A_DM4
M_A_DQ0	5	DQ0	DM5	147	M_A_DM5
M_A_DQ1	7	DQ1	DM6	170	M_A_DM6
M_A_DQ2	17	DQ2	DM7	185	M_A_DM7
M_A_DQ3	19	DQ3			
M_A_DQ4	4	DQ4	SDA	195	ICH_SMBDATA
M_A_DQ5	6	DQ5	SCL	197	ICH_SMBCLK
M_A_DQ6	14	DQ6			
M_A_DQ7	16	DQ7	VDDSPD	199	+3.3V_RUN
M_A_DQ8	23	DQ8			
M_A_DQ9	25	DQ9	SA0	198	R55 2 0R0402-PAD
M_A_DQ10	35	DQ10	SA1	200	R56 2 0R0402-PAD
M_A_DQ11	37	DQ11			
M_A_DQ12	20	DQ12	NC#50	50	
M_A_DQ13	22	DQ13	NC#69	69	
M_A_DQ14	36	DQ14	NC#83	83	
M_A_DQ15	38	DQ15	NC#120	120	
M_A_DQ16	43	DQ16	NC#163/TEST	163	
M_A_DQ17	45	DQ17			
M_A_DQ18	55	DQ18			
M_A_DQ19	57	DQ19	VDD	81	
M_A_DQ20	44	DQ20	VDD	82	
M_A_DQ21	46	DQ21	VDD	87	
M_A_DQ22	56	DQ22	VDD	88	
M_A_DQ23	58	DQ23	VDD	95	
M_A_DQ24	61	DQ24	VDD	96	
M_A_DQ25	63	DQ25	VDD	103	
M_A_DQ26	73	DQ26	VDD	104	
M_A_DQ27	75	DQ27	VDD	111	
M_A_DQ28	62	DQ28	VDD	112	
M_A_DQ29	64	DQ29	VDD	117	
M_A_DQ30	74	DQ30	VDD	118	
M_A_DQ31	76	DQ31			
M_A_DQ32	123	DQ32	VSS	3	
M_A_DQ33	125	DQ33	VSS	8	
M_A_DQ34	135	DQ34	VSS	9	
M_A_DQ35	137	DQ35	VSS	12	
M_A_DQ36	124	DQ36	VSS	15	
M_A_DQ37	126	DQ37	VSS	18	
M_A_DQ38	134	DQ38	VSS	21	
M_A_DQ39	136	DQ39	VSS	24	
M_A_DQ40	141	DQ40	VSS	27	
M_A_DQ41	143	DQ41	VSS	28	
M_A_DQ42	151	DQ42	VSS	33	
M_A_DQ43	153	DQ43	VSS	34	
M_A_DQ44	140	DQ44	VSS	39	
M_A_DQ45	142	DQ45	VSS	40	
M_A_DQ46	152	DQ46	VSS	41	
M_A_DQ47	154	DQ47	VSS	42	
M_A_DQ48	157	DQ48	VSS	47	
M_A_DQ49	159	DQ49	VSS	48	
M_A_DQ50	173	DQ50	VSS	53	
M_A_DQ51	175	DQ51	VSS	54	
M_A_DQ52	158	DQ52	VSS	59	
M_A_DQ53	160	DQ53	VSS	60	
M_A_DQ54	174	DQ54	VSS	65	
M_A_DQ55	176	DQ55	VSS	66	
M_A_DQ56	179	DQ56	VSS	71	
M_A_DQ57	181	DQ57	VSS	72	
M_A_DQ58	189	DQ58	VSS	77	
M_A_DQ59	191	DQ59	VSS	78	
M_A_DQ60	180	DQ60	VSS	121	
M_A_DQ61	182	DQ61	VSS	122	
M_A_DQ62	192	DQ62	VSS	127	
M_A_DQ63	194	DQ63	VSS	128	
			VSS	132	
M_A_DQS#0	11	DQS0#	VSS	133	
M_A_DQS#1	29	DQS1#	VSS	138	
M_A_DQS#2	49	DQS2#	VSS	139	
M_A_DQS#3	68	DQS3#	VSS	144	
M_A_DQS#4	129	DQS4#	VSS	145	
M_A_DQS#5	146	DQS5#	VSS	149	
M_A_DQS#6	167	DQS6#	VSS	150	
M_A_DQS#7	186	DQS7#	VSS	155	
			VSS	156	
M_A_DQS0	13	DQS0	VSS	161	
M_A_DQS1	31	DQS1	VSS	162	
M_A_DQS2	51	DQS2	VSS	165	
M_A_DQS3	70	DQS3	VSS	168	
M_A_DQS4	131	DQS4	VSS	171	
M_A_DQS5	148	DQS5	VSS	172	
M_A_DQS6	169	DQS6	VSS	177	
M_A_DQS7	188	DQS7	VSS	178	
			VSS	183	
M_ODT0	114	OTD0	VSS	184	
M_ODT1	119	OTD1	VSS	187	
			VSS	190	
	1	VREF	VSS	193	
	2	VSS	VSS	196	
	202	GND	GND	201	
MH1		MH1	MH2		MH2

SKT-SODIMM200-37GP

62.10017.E21

-1

put near connector
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C72 Do Not Stuff
C74 Do Not Stuff
C192 Do Not Stuff
C195 Do Not Stuff

Layout Note:
Place near DM1
+1.8V_SUS
C132 SC2D2U10V3KX-1GP
C122 SC2D2U10V3KX-1GP
C60 Do Not Stuff
C138 Do Not Stuff
C116 SC2D2U10V3KX-1GP
C93 Do Not Stuff
C109 SCD1U16V2KX-3GP
C100 SCD1U16V2KX-3GP
C106 SCD1U16V2KX-3GP
C8 Do Not Stuff

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
C101 Do Not Stuff
C409 SCD1U16V2KX-3GP
C103 Do Not Stuff
C96 SCD1U16V2KX-3GP
C83 Do Not Stuff
C132 Do Not Stuff
C97 SCD1U16V2KX-3GP
C114 Do Not Stuff
C118 Do Not Stuff
C119 SCD1U16V2KX-3GP
C115 SCD1U16V2KX-3GP
C428 SCD1U16V2KX-3GP
C420 SCD1U16V2KX-3GP

+V_DDR_MCH_REF
C203 SCD1U16V2KX-3GP
C202 Do Not Stuff

+3.3V_RUN
C54 SCD1U16V2KX-3GP
C53 Do Not Stuff

Layout Note:
Place these resistors close to DM1,
all trace length Max=1.5".
+0.9V_DDR_VTT

RN37	M_A_A9 / M_A_A12	RN6	M_A_A13
RN31	M_A_A10 / M_A_BS#0	RN35	M_A_A5 / M_A_A8
RN4	M_ODT0 / M_CS0#	RN10	M_A_A6 / M_A_A2
RN12	M_CKE1 / M_A_A14	RN33	M_A_A1 / M_A_A3
RN29	M_A_WE# / M_A_CAS#	RN39	M_CKE0 / M_A_BS#2
RN28	M_CS1# / M_ODT1	RN8	M_A_BS#1 / M_A_RAS#
RN11	M_A_A11 / M_A_A7	RN17	M_A_A0 / M_A_A4

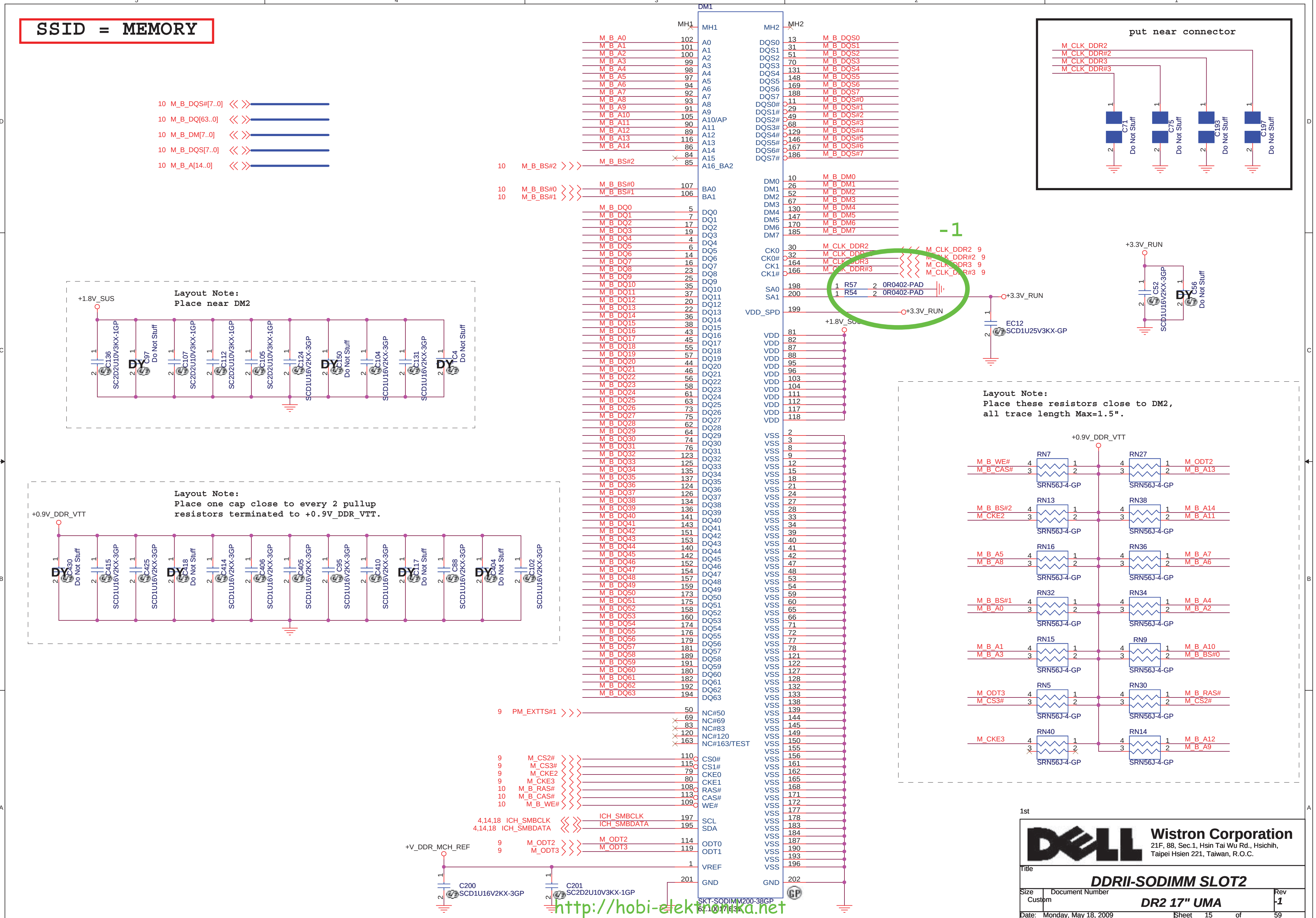
All: SRN56J-4-GP

1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT1
Size: Custom | Document Number: DR2 17" UMA | Rev: -1
Date: Monday, May 18, 2009 | Sheet 14 of 59

SSID = MEMORY



put near connector
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C71 Do Not Stuff
C75 Do Not Stuff
C193 Do Not Stuff
C197 Do Not Stuff
10 M_B_DQS#[7..0]
10 M_B_DQ[63..0]
10 M_B_DM[7..0]
10 M_B_DQS[7..0]
10 M_B_A[14..0]
DM1
SKT-SODIMM200-38GP
Layout Note:
Place near DM2
+1.8V_SUS
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT.
+0.9V_DDR_VTT
Layout Note:
Place these resistors close to DM2,
all trace length Max=1.5".
SRN56J-4-GP
+3.3V_RUN
0R0402-PAD
SCD1U25V3KX-GP
-1
PM_EXTTS#1
ICH_SMBCLK
ICH_SMBDATA
+V_DDR_MCH_REF
SCD1U16V2KX-3GP
SC2D2U10V3KX-1GP

1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRII-SODIMM SLOT2

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 15 of 59

SSID = ICH

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U25E

ICH9M-GP-NF

+3.3V_RUN

U32

DY

Do Not Stuff

PLT_RST#

PCI_PLTRST#

R262

2 OF 6

U25B

PCI

Interrupt I/F

ICH9M-GP-NF

PCI_REQ0#
PCI_GNT0#
PCI_REQ1#
PCI_GNT1#
PCI_REQ2#
PCI_GNT2#
PCI_REQ3#
PCI_GNT3#

TP179
TP261
TP135
TP138

PCI_IRDY#
PCIRST1#
PCI_DEVSEL#
PCI_PERR#
PCI_PLOCK#
PCI_SERR#
PCI_STOP#
PCI_TRDY#
PCI_FRAME#
PCI_PLTRST#
CLK_PCI_ICH
ICH_PME#

PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
PCI_PIRQE#
PCI_PIRQF#
PCI_PIRQG#
PCI_PIRQH#

RN57
RN25
RN26
RN58
RN56

SRN8K2J-4-GP

R245
R240
C315

U27

SPI_WP#
SPI_MOSO
SPI_CS#0
SPI_MOSI
SPI_CLK
SPI_HOLD#

RP1

SRN10KJ-L3-GP

RN55

SRN8K2J-4-GP

USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
USB_OC#10
USB_OC#11

+3.3V_ALW

R442
R443
R441

PCI_GNT0#
SPI_CS#1
PCI_GNT3#

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

4 OF 6

U25D

PCI-Express Direct Media Interface

SPI

USB

Mini Card

LAN

New Card

PCIE_RXN2
PCIE_RXP2
PCIE_TXN2
PCIE_TXP2
PCIE_C_TXN2
PCIE_C_TXP2

PCIE_RXN3
PCIE_RXP3
PCIE_TXN3
PCIE_TXP3
PCIE_C_TXN3
PCIE_C_TXP3

PCIE_RXN5
PCIE_RXP5
PCIE_TXN5
PCIE_TXP5
PCIE_C_TXN5
PCIE_C_TXP5

C500
C497
C506
C510
C518
C517

SCD1U16V2KX-3GP

DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP

DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3

DMI_CLKN
DMI_CLKP
CLK_PCIE_ICH#
CLK_PCIE_ICH

DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R

R429
24D9R2F-L-GP

+1.5V_RUN

PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP

SPI_CLK
SPI_CS0#
SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI
SPI_MISO

SPI_CLK_R
SPI_CS#0_R
SPI_MOSI_R
SPI_MOSO_R

R233
R241
R230
R237

USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBP10N
USBP10P
USBP11N
USBP11P

USB_PN0
USB_PP0
USB_PN1
USB_PP1
USB_PN2
USB_PP2
USB_PN3
USB_PP3
USB_PN4
USB_PP4
USB_PN5
USB_PP5
USB_PN6
USB_PP6
USB_PN7
USB_PP7
USB_PN8
USB_PP8
USB_PN9
USB_PP9
USB_PN10
USB_PP10
USB_PN11
USB_PP11

TP246
TP247
TP250
TP251
TP248
TP249
TP252
TP253

OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#/GPIO44
OC9#/GPIO45
OC10#/GPIO46
OC11#/GPIO47

USBRBIAS
USBRBIAS#

R208
22R2F-1-GP

USB1
USB2
USB3
BlUETOOTH
New Card
Card Reader
CAMERA

USB Pair	Device
0	USB1
1	USB2
2	USB3
3	RESERVED
4	MINI CARD
5	RESERVED
6	BLUETOOTH
7	NEW CARD
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

NCTF PIN

ICH_GND1
ICH_GND2
ICH_GND3
ICH_GND4

TP177
TP178
TP125
TP127

1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-PCI/PCIE/DMI/USB/GND(1/4)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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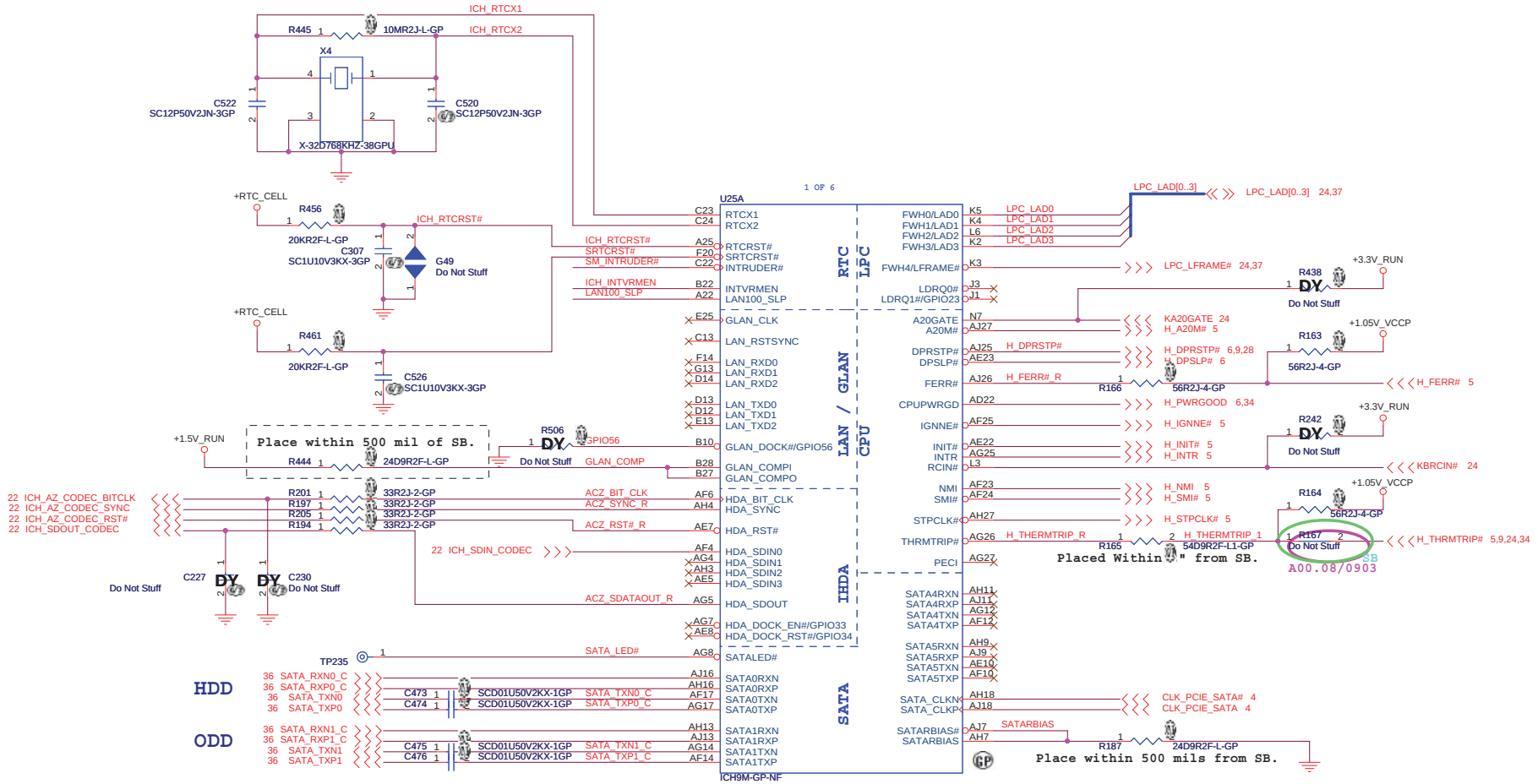
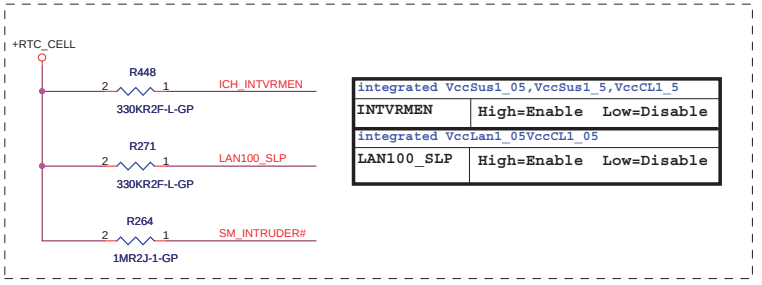
SSID = ICH





integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

1st

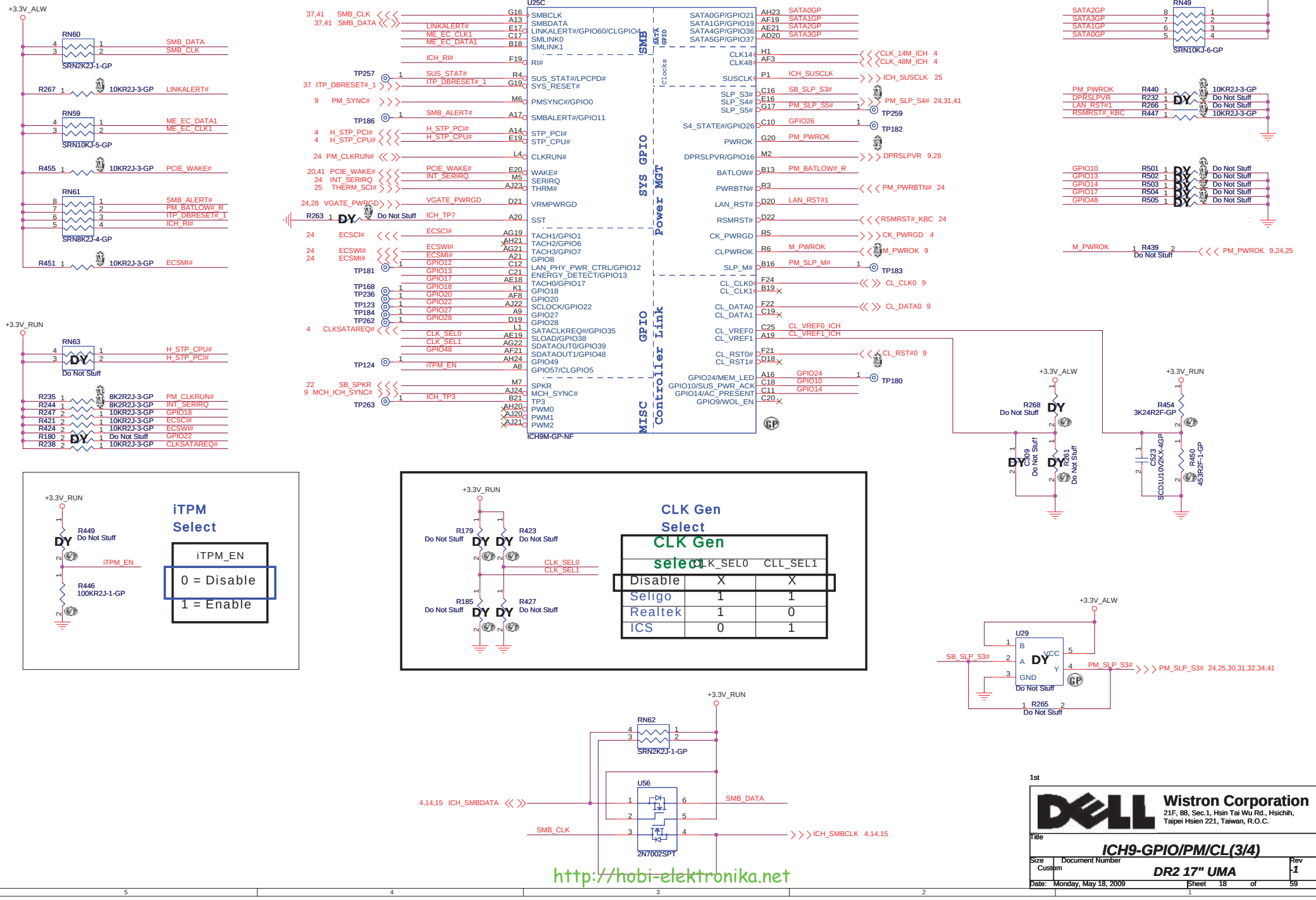
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(2/4)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 17 of 59

SSID = ICH


+3.3V_ALW
RN60
SMB_DATA
SMB_CLK
SRN2K2J-1-GP
R267 10KR2J-3-GP LINKALERT#
RN59
ME_EC_DATA1
ME_EC_CLK1
SRN10KJ-5-GP
R455 10KR2J-3-GP PCIE_WAKE#
RN61
SMB_ALERT#
PM_BATLOW#_R
ITP_DBRESET#_1
ICH_RI#
SRN8K2J-4-GP
R451 10KR2J-3-GP ECSMI#
+3.3V_RUN
RN63
H_STP_CPU#
H_STP_PCI#
Do Not Stuff
R235 8K2R2J-3-GP PM_CLKRUN#
R244 8K2R2J-3-GP INT_SERIRQ
R247 10KR2J-3-GP GPIO18
R421 10KR2J-3-GP ECSCI#
R424 10KR2J-3-GP ECSWI#
R180 Do Not Stuff GPIO22
R238 10KR2J-3-GP CLKSATAREQ#
3 OF 6
U25C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SMB
GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
ICH9M-GP-NF
TP257
TP186
TP181
TP168
TP236
TP123
TP184
TP262
TP124
TP263
TP259
TP182
TP183
TP180
R263 Do Not Stuff
+3.3V_RUN
RN49
SRN10KJ-6-GP
R440 10KR2J-3-GP
R232 Do Not Stuff
R266 Do Not Stuff
R447 10KR2J-3-GP
R501 Do Not Stuff
R502 Do Not Stuff
R503 Do Not Stuff
R504 Do Not Stuff
R505 Do Not Stuff
R439 Do Not Stuff
+3.3V_ALW
R268 Do Not Stuff
R309 Do Not Stuff
R261 Do Not Stuff
+3.3V_RUN
R454 3K24R2F-GP
C523 SCD1U10V2KX-4GP
R450 453R2F-1-GP
+3.3V_RUN
R449 Do Not Stuff
iTPM_EN
R446 100KR2J-1-GP
iTPM Select
iTPM_EN
0 = Disable
1 = Enable
+3.3V_RUN
R179 Do Not Stuff
R423 Do Not Stuff
R185 Do Not Stuff
R427 Do Not Stuff
CLK_SEL0
CLK_SEL1
CLK Gen Select
CLK Gen select
CLL_SEL0
CLL_SEL1
Disable X X
Seligo 1 1
Realtek 1 0
ICS 0 1
+3.3V_ALW
U29
SB_SLP_S3#
PM_SLP_S3#
PM_SLP_S3# 24,25,30,31,32,34,41
R265 Do Not Stuff
+3.3V_RUN
RN62
SRN2K2J-1-GP
U56
2N7002SPT
4,14,15 ICH_SMBDATA
SMB_DATA
SMB_CLK
ICH_SMBCLK 4,14,15
http://hobi-elektronika.net
1st
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-GPIO/PM/CL(3/4)
Size Custom
Document Number
DR2 17" UMA
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Date: Monday, May 18, 2009
Sheet 18 of 59

SSID = ICH

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

U25F

6 OF 6

ICH9M-GP NF

+RTC_CELL

+1.05V_VCCP

+1.5V_RUN

+3.3V_RUN

+3.3V_ALW

+VCCSATAPLL

VCC_GLAN_PLL

VCCLAN1D05

1D5V_USB_S0

1D5V_DMIPLL_ICH_S0

SB_V_CPU_IO

SB_VCC_3_3_C

SB_VCCHDA

SB_VCCSUS3_3

SB_VCCLAN3_3

SB_VCCCL3_3

3D3V_VCCPCORE_ICH_S0

PCI_VCCP_CORE_S0

VCCDMI

V5REF_S0

V5REF_S5

A00.08/0909

Do Not Stuff

http://hobi-elektronika.net

Wistron Corporation
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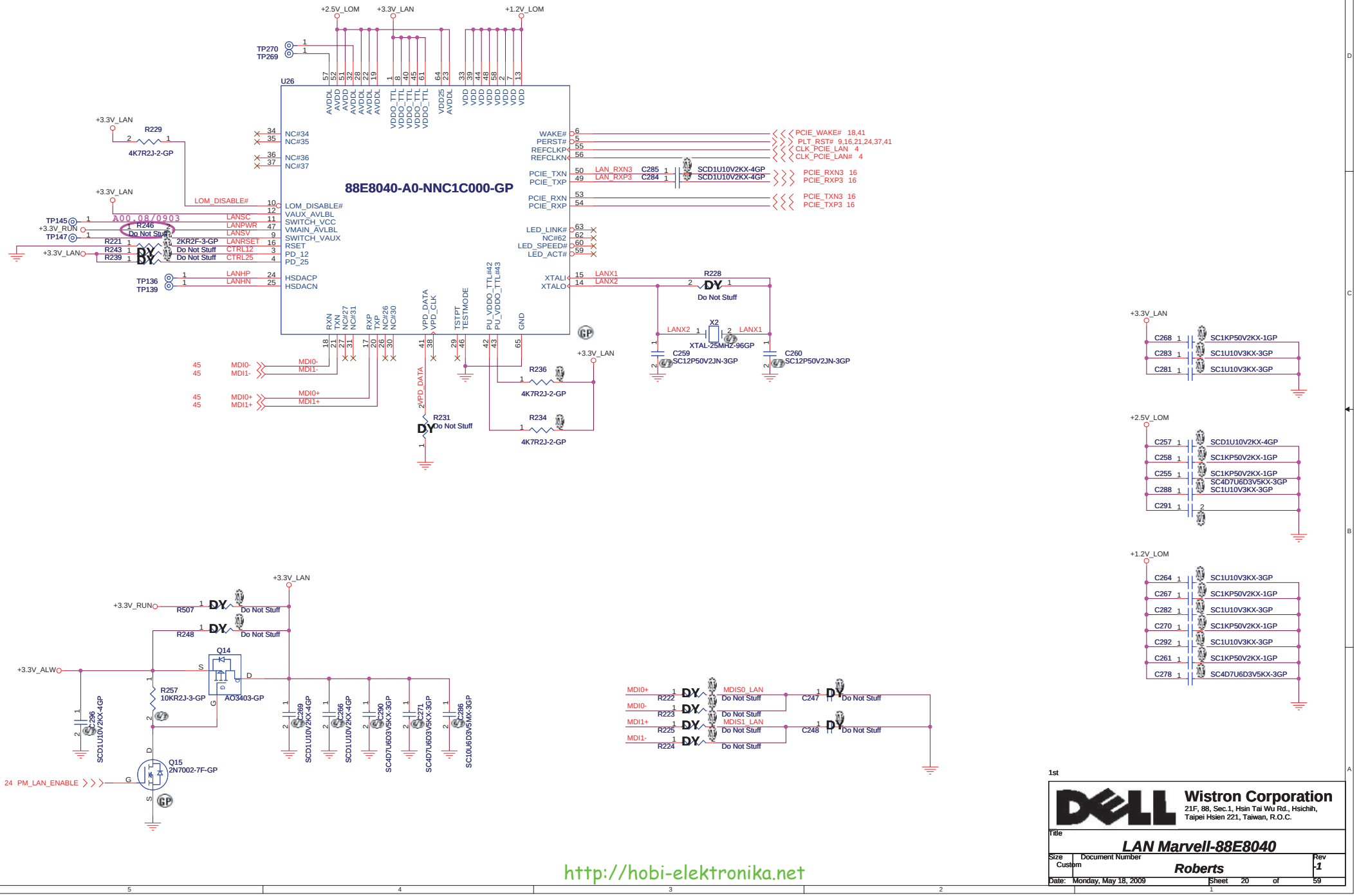
Title: ICH9-POWER(4/4)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 19 of 59

SSID = LOM



http://hobi-elektronika.net

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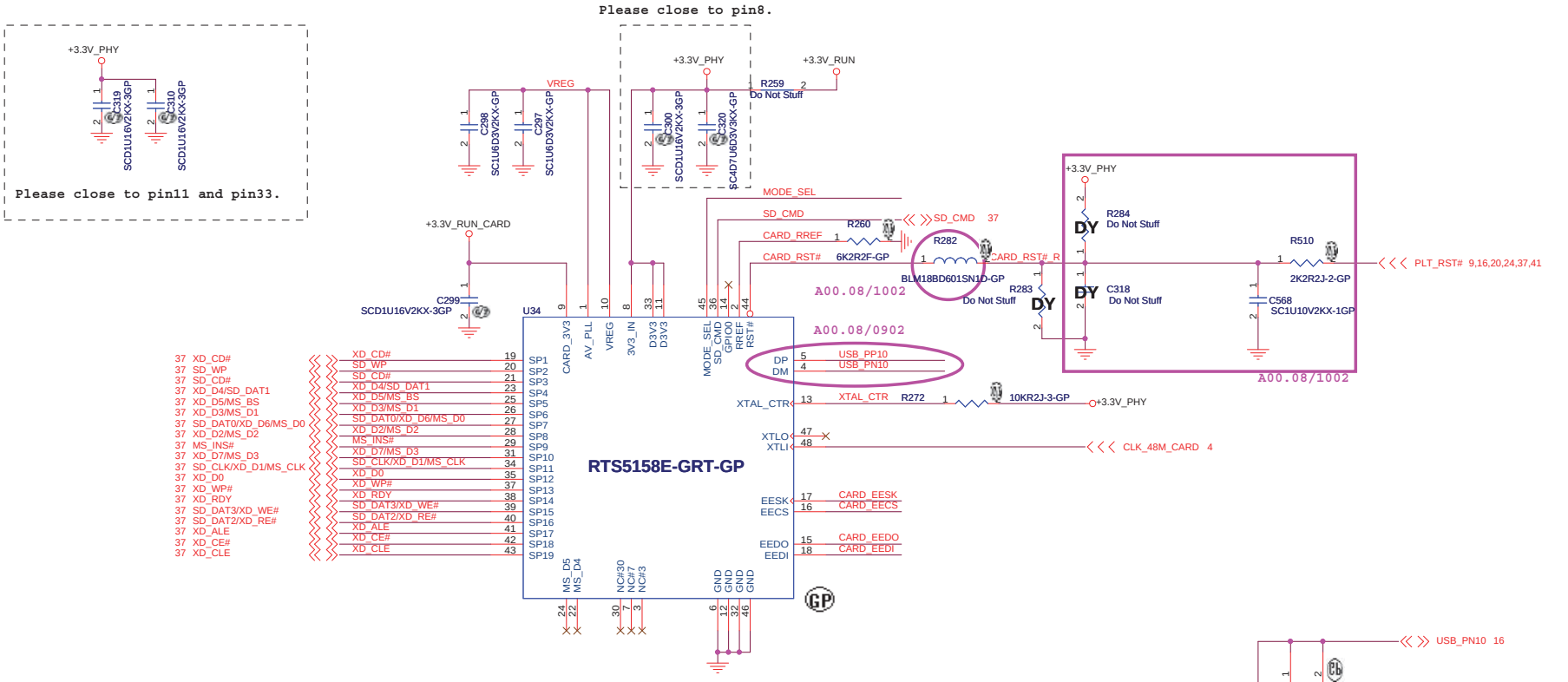
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Marvell-88E8040

Size	Document Number	Rev
Custom	Roberts	-1

Date: Monday, May 18, 2009 Sheet 20 of 59

SSID = SDIO



1st

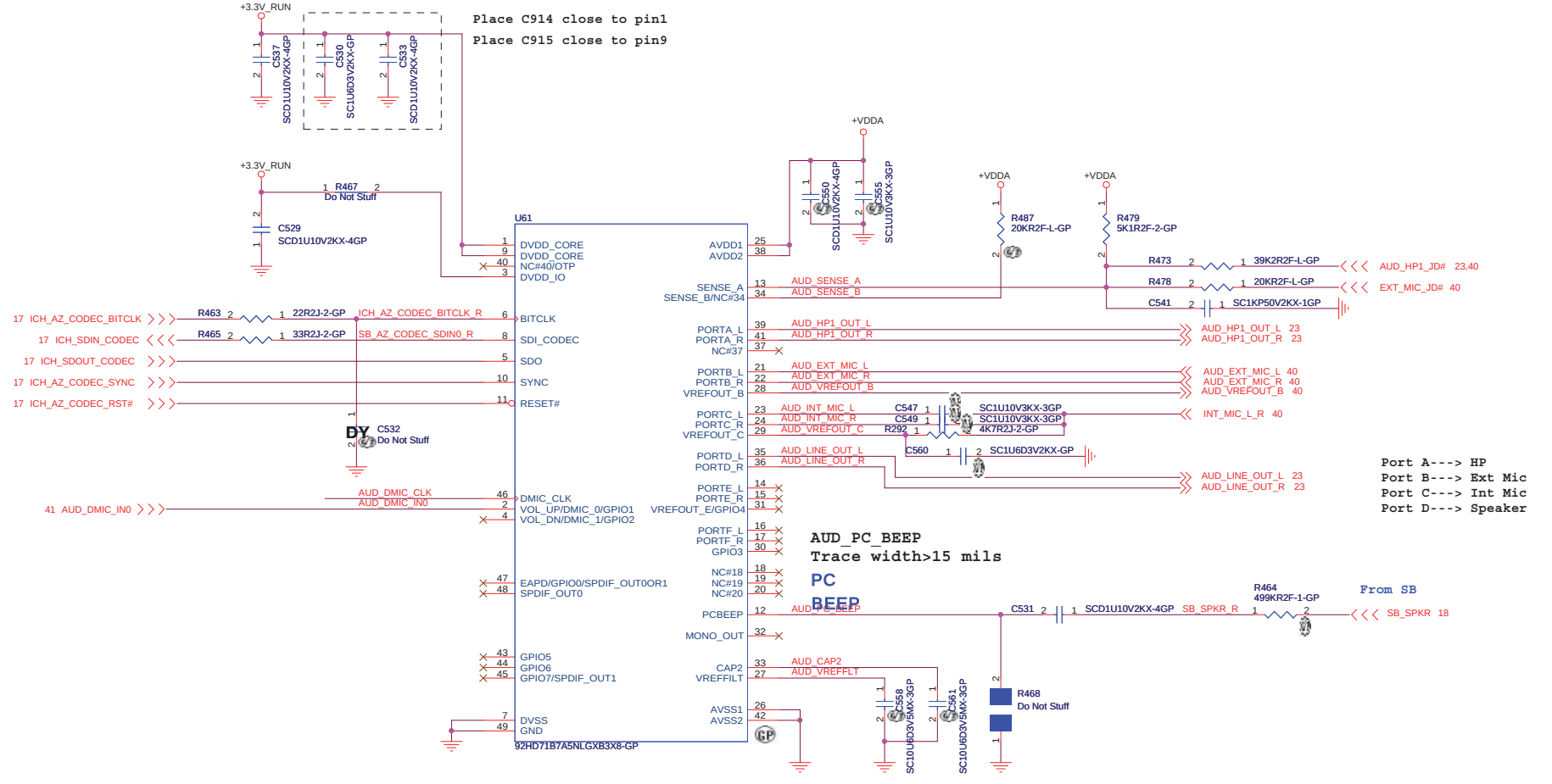
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5158E

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

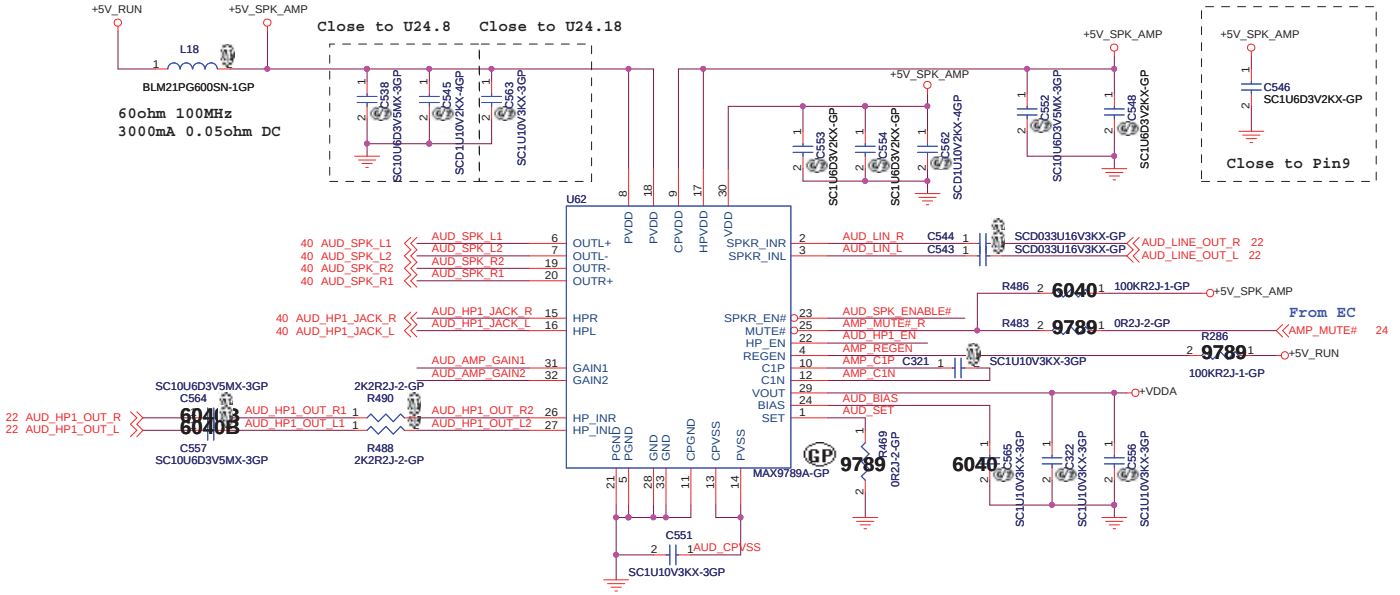
Date: Monday, May 18, 2009 | Sheet 21 of 59

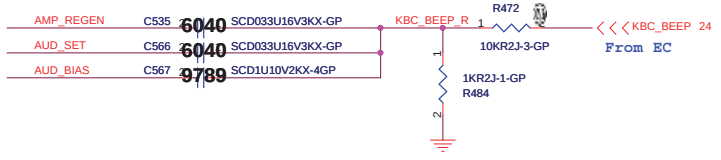
SSID = AUDIO



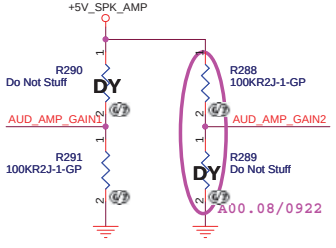
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO CODEC 92HD71B7
Size: Custom	Document Number: DR2 17" UMA
Rev: -1	
Date: Monday, May 18, 2009	Sheet 22 of 59

SSID = AUDIO



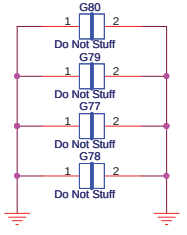


GAIN SETTING

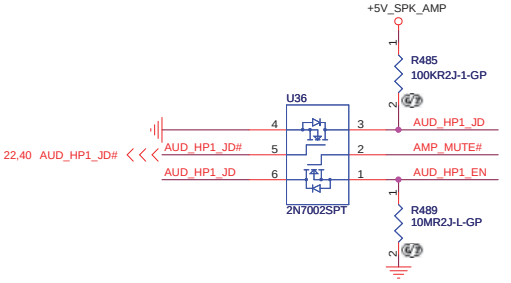


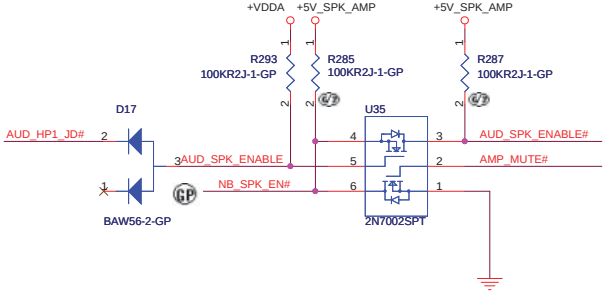
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

	Main source	Second source
	TPA6040A (74.06040.013)	MAX9789A (74.09789.013)
R486	100K	No ASM
R483	No ASM	0 Ohm
R469	No ASM	0 Ohm
R286	No ASM	100K
C535	0.033uF	No ASM
C566	0.033uF	No ASM
C565	1uF	No ASM
C567	No ASM	0.1uF
C564	10uF	2.2uF
C557	10uF	2.2uF



Signal inverter for speaker shutdown





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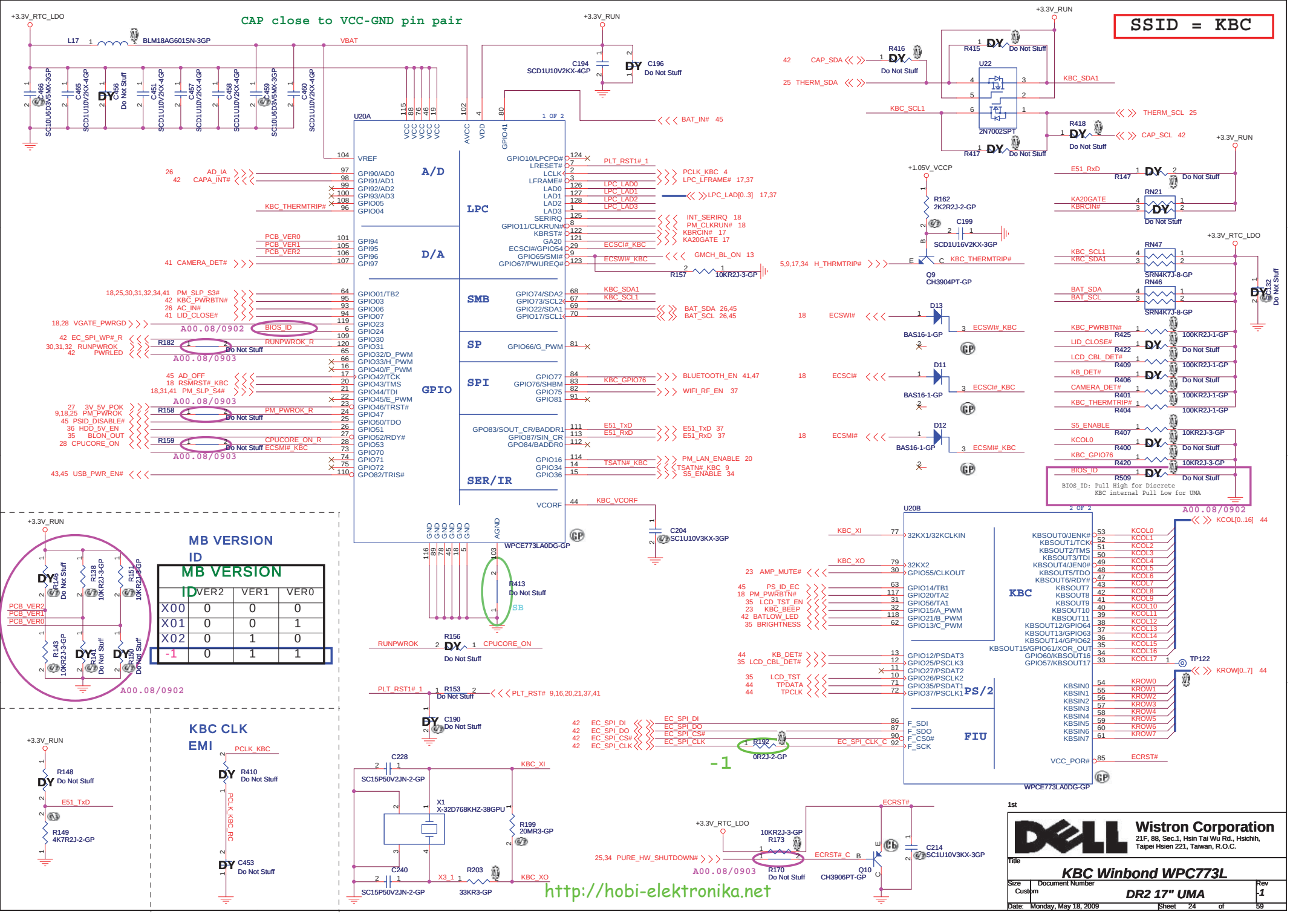
Title: AUDIO AMP/SPEAKER

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 23 of 59


SSID = KBC
CAP close to VCC-GND pin pair
MB VERSION ID
MB VERSION ID
VER2 VER1 VER0
X00 0 0 0
X01 0 0 1
X02 0 1 0
-1 0 1 1
KBC CLK EMI
U20A
1 OF 2
A/D
LPC
D/A
SMB
SP
GPIO
SPI
SER/IR
U20B
2 OF 2
KBC
PS/2
FIU
WPCE773LA0DG-GP
BIOS_ID: Pull High for Discrete KBC internal Pull Low for UMA
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Winbond WPC773L
DR2 17" UMA
Monday, May 18, 2009
Sheet 24 of 59

SSID = Thermal

+5V_RUN
+3.3V_RUN
+3.3V_RTC_LDO
+3.3V_ALW

C386 SC4D7U6D3V5KX-3GP
C389 SCD1U16V2KX-3GP
R63 10KR2J-3-GP
R66 DY Do Not Stuff
R348 DY Do Not Stuff
D6 RB551V30-GP
EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 36
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE 36
RN3 SRN4K7J-8-GP
THERM_SCL 24
THERM_SDA 24
R346 DY Do Not Stuff
R340 49D9R2F-GP
EMC2102_VDD_3D3
C60 SCD1U16V2KX-3GP

1.For CPU Sensor

5 H_THERMDC
5 H_THERMDA
C50 SC470P50V3JN-2GP
Layout notice : Both H_THERMDA and THERMDC routing 10 mil trace width and 10 mil spacing.
Layout notice : Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing.

C388 must be near Q18
Q18 MMBT3904-3-GP
C388 DY Do Not Stuff
C61 SC470P50V3JN-2GP
C61 must be near EMC2102

2.System Sensor, Put between CPU and NB.

C37 must be near Q1
Q1 MMBT3904-3-GP
C37 DY Do Not Stuff
C63 SC470P50V3JN-2GP
C63 must be near EMC2102

3.HW T8 sensor

U8 EMC2102-DZK-GP
GND VDD_3V DN1 DP1 DN2 DP2 DN3 DP3
TACH VDD_5Va FANa FANb VDD_5Vb SMCLK SMDATA
NC#21 GND ALERT# CLK_IN CLK_SEL RESET# NC#15
NC#8 SHDN_SEL FAN_MODE TRIP_SET SYS_SHDN# THERMTRIP# POWER_OK#
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
ALERT# R87 DY Do Not Stuff
CLK_32K
EMC2102_CLK_SEL R88 10KR2J-3-GP
EM2102_RESET#
R89 8K2R2J-3-GP
THERM_SCI# 18

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

R67 DY Do Not Stuff EMC2102_SHDN
R68 DY Do Not Stuff EMC2102_FAN_mode
R71 10KR2J-3-GP
R85 10KR2J-3-GP
R84 10KR2J-3-GP

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

R362 10KR2J-3-GP
R347 10KR2J-3-GP
Q17 2N7002-7F-GP
PURE_HW_SHUTDOWN# 24,34

TP223
TP72
EMC2102_FAN_TACH_1
EMC2102_FAN_DRIVE

A00.08/0922
C78 SCD1U16V2KX-3GP
R82 10KR2F-2-GP
C70 SCD1U16V2KX-3GP
R78 2K37R2F-GP
V_DEGREE

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

T8 shutdown is set 88 deg-C.

32K suspend clock output

18 ICH_SUSCLK
Q13 2N7002-7F-GP
CLK_32K_R
R219 10R2J-2-GP
CLK_32K
C249 DY Do Not Stuff
RUN_POWER_ON

U10
EM2102_RESET#
18,24,30,31,32,34,41 PM_SLP_S3#
C82 DY Do Not Stuff
PM_PWROK 9,18,24

1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom
Document Number: DR2 17" UMA
Rev: -1
Date: Monday, May 18, 2009
Sheet 25 of 59

SSID = Charger

Adaptor In Soft-Start Circuit

Id=-8A
Qg=17~24nC
Rdson=15~20mohm

Layout Trace 250mil

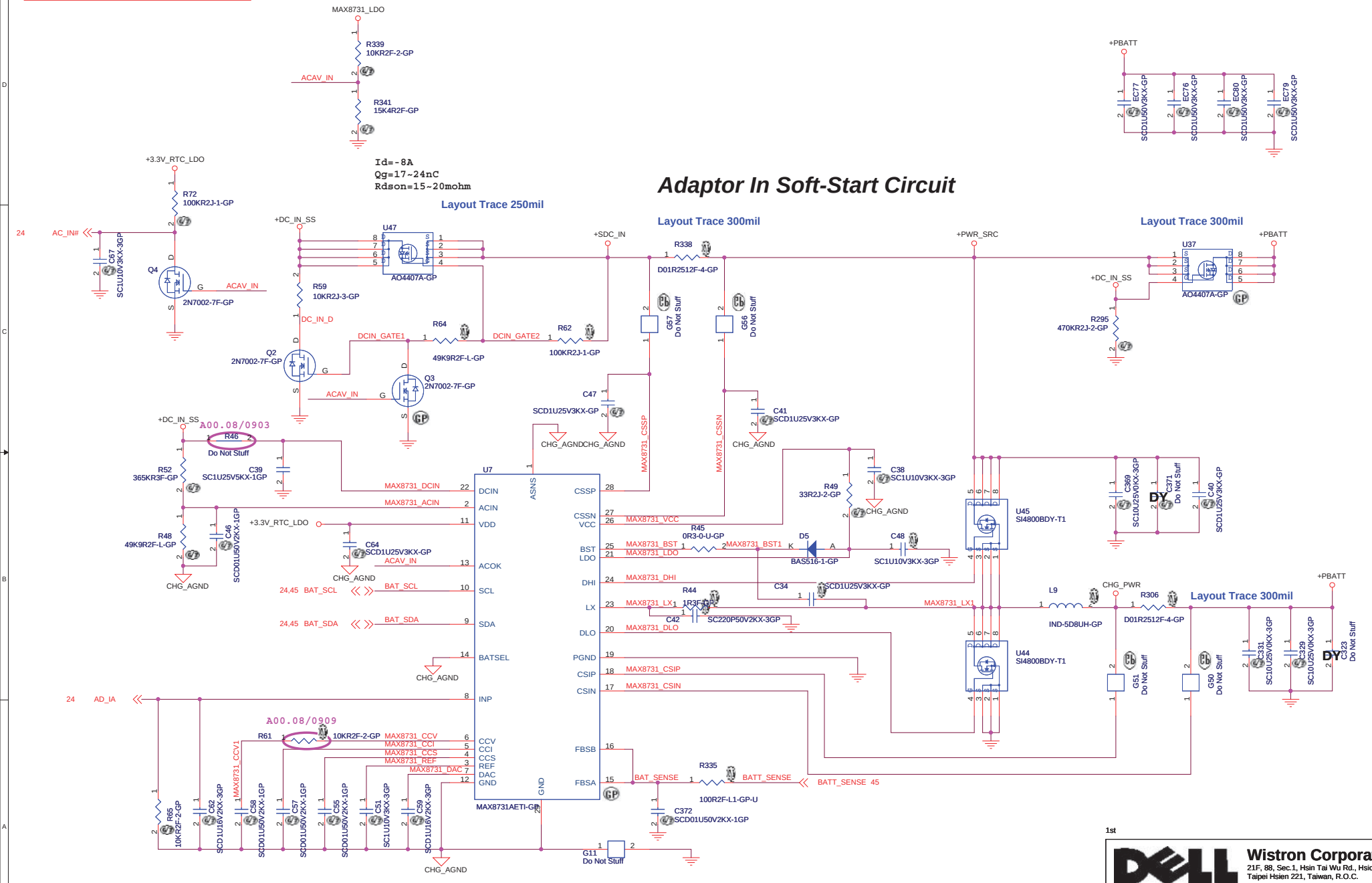
Layout Trace 300mil

Layout Trace 300mil

Layout Trace 300mil

A00.08/0903

A00.08/0909



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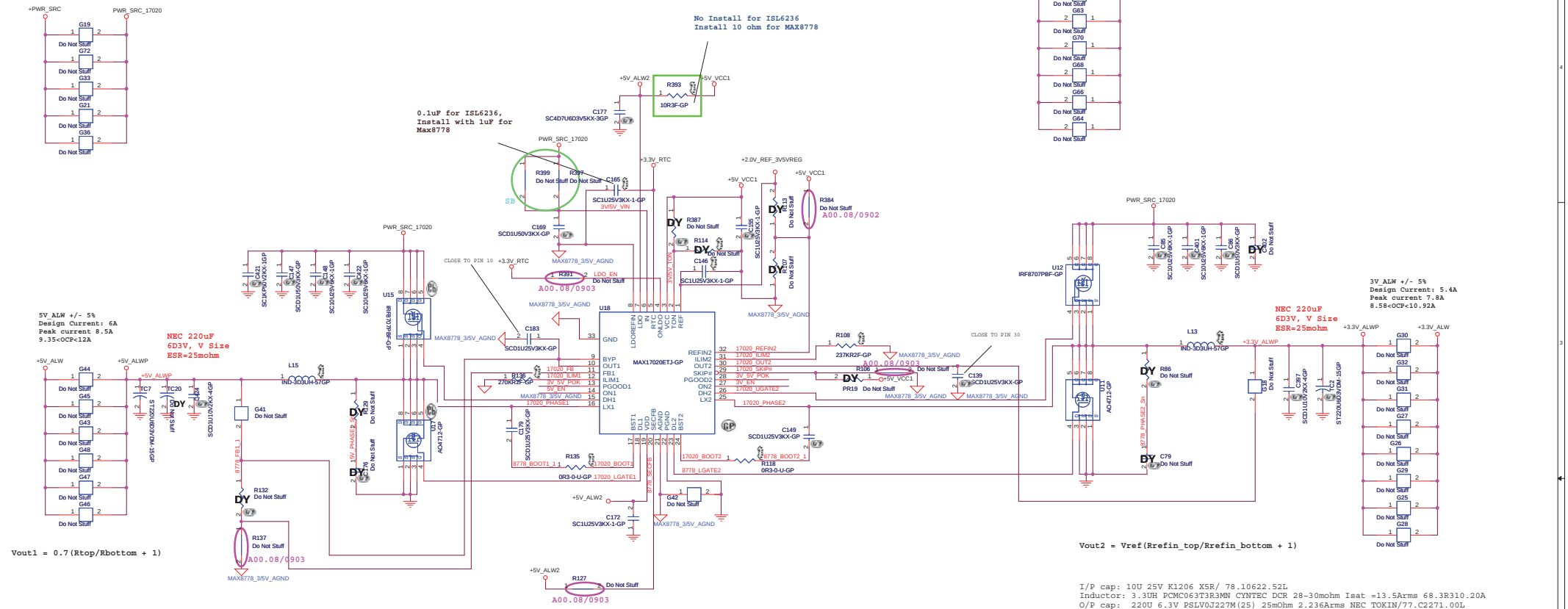
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8731

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 26 of 59

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMC063T3R3MN CYNTEC DCR 28~30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 150U 6.3V PSLB20J157M(45) 45mOhm 1.374rms NEC_TOKIN/77.C1571.09L
H/S: IRF8707 SO-8/ 14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS4712 SO-8/ 15mohm/18mOhm@4.5Vgs/ 84.04712.037

SKIPSEL	GND	Open/REF (2V)	High (VCC or 3.3V)
Operating Mode	pulse-skipping mode	ultrasonic mode	forced-PWM operation

TONSEL	GND	Open (REF)	High (VCC)
CH1 Freq	400kHz	400kHz	200kHz
CH2 Freq	500kHz	300kHz	300kHz

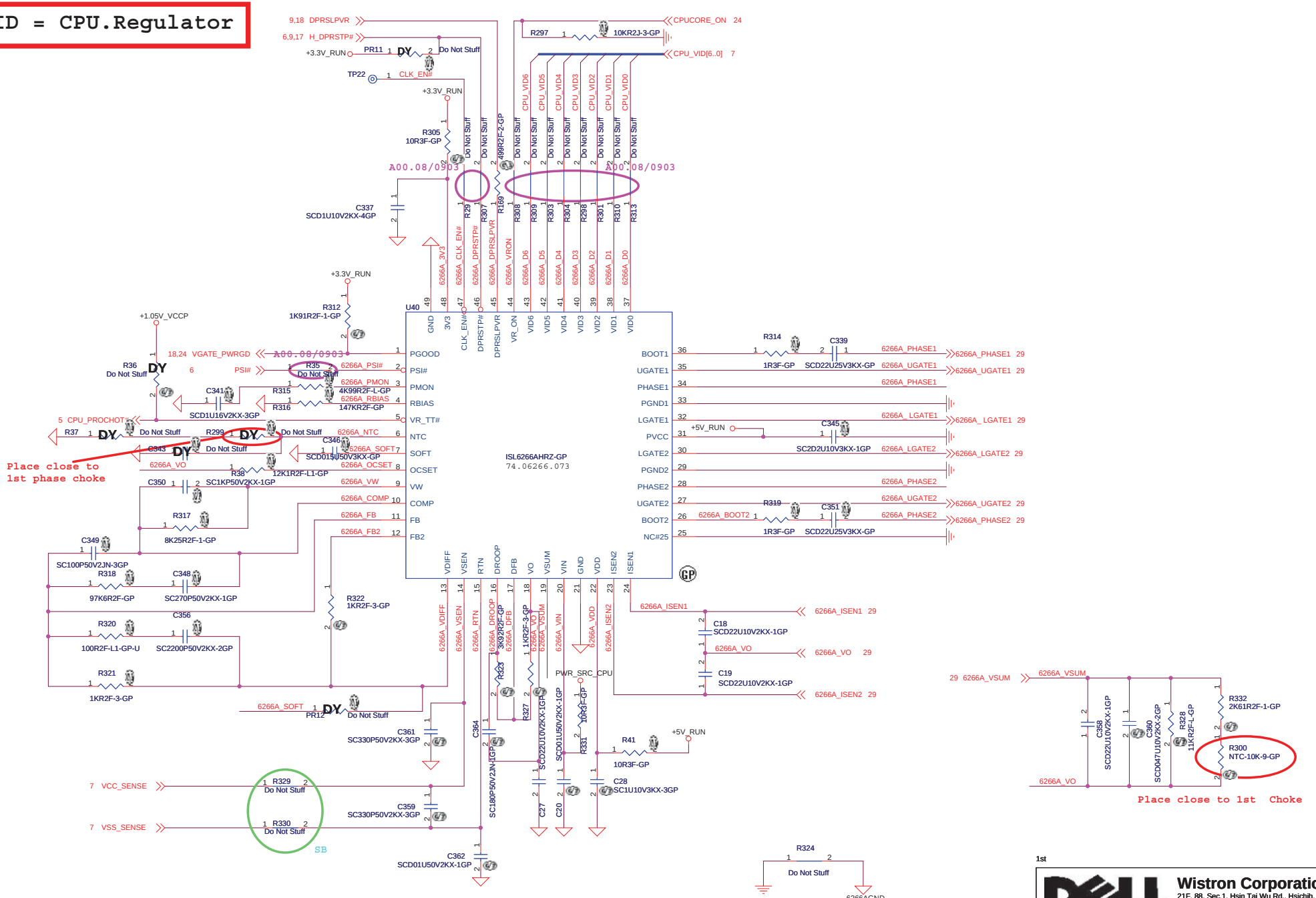
LDOREFIN	GND	VCC	VLDOREFIN = 0.5V
Operating Mode	4.90/5.0/5.10	3.23/3.3/3.37	0.96/1.0/1.04

FB1	GND	VCC	
Operating Mode	4.925/5.00/5.075	1.482/1.50/1.518	

REFIN2	5V	RTC (3.3V)	
Operating Mode	3.255/3.3/3.345	3.038/3.050/3.062	

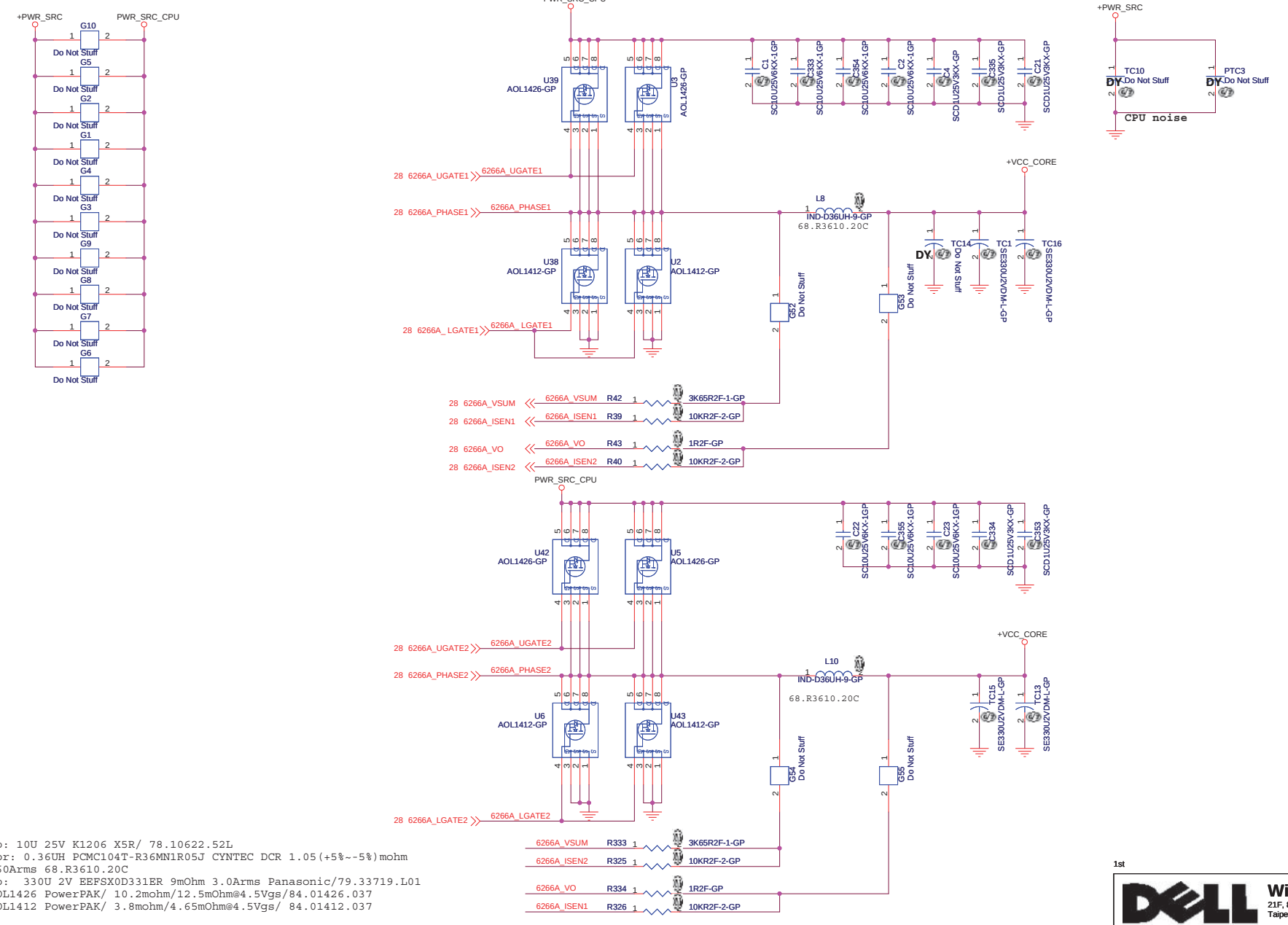
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC to DC 3.3V/5V			
Size: A2	Document Number: DR2 17" UMA		Rev: -1
Date: Monday, May 18, 2009	Sheet 27 of 59		

SSID = CPU.Regulator



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU VCORE POWER(1/2)
Size: Custom	Document Number: DR2 17" UMA
Rev: -1	
Date: Monday, May 18, 2009	Sheet 28 of 59

SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
Isat =60Arms 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
H/S: AOL1426 PowerPAK/ 10.2mohm/12.5mOhm@4.5Vgs/84.01426.037
L/S: AOL1412 PowerPAK/ 3.8mohm/4.65mOhm@4.5Vgs/ 84.01412.037

1st

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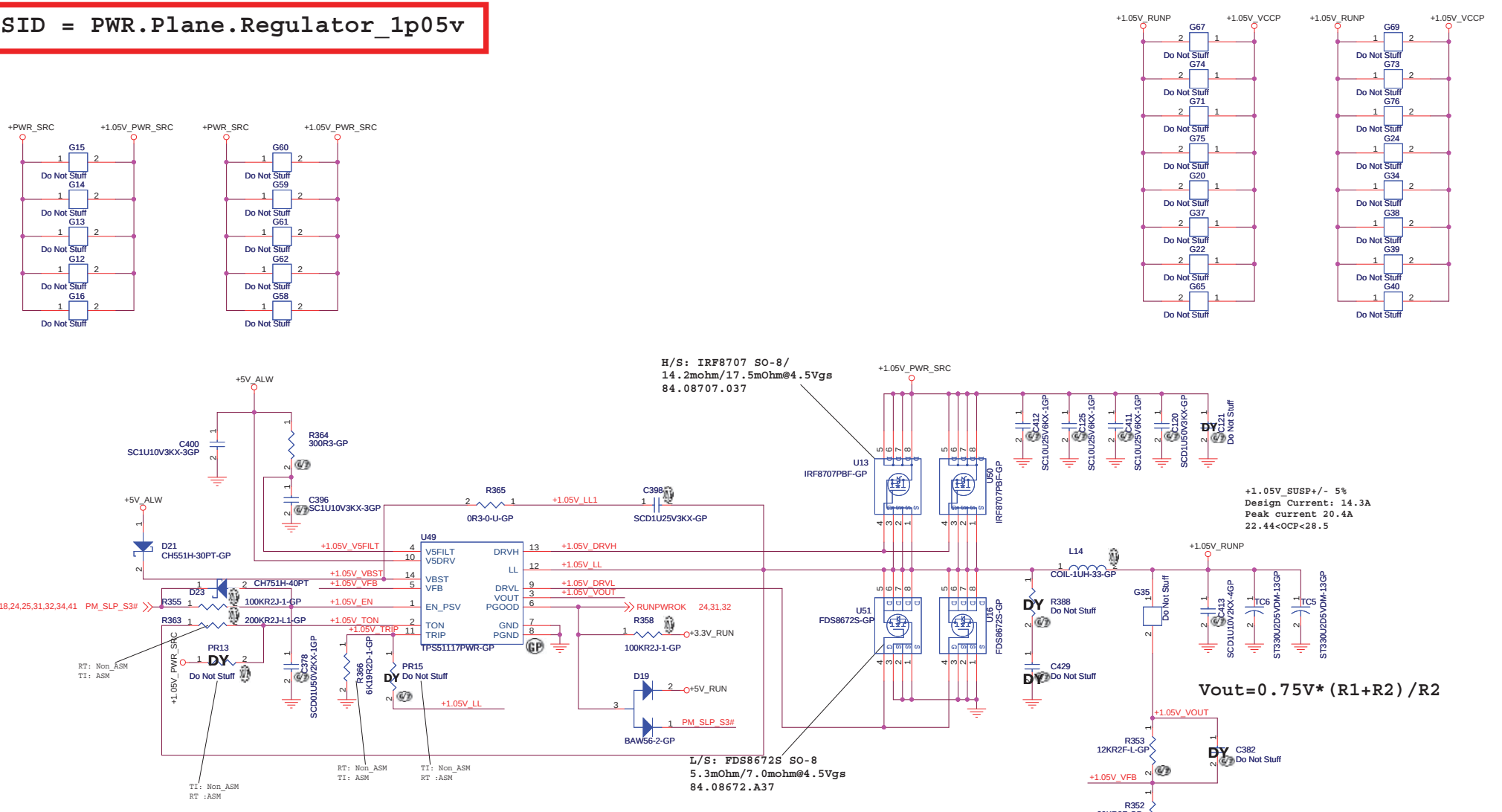
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER(2/2)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 29 of 59

SSID = PWR.Plane.Regulator_1p05v



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0UH PCMC104T1R0MN Cyntec DCR:3.0 ~3.5mohm Isat =40Arms 68.1R01A.20A
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: IRF8707 SO-8/14.2mohm/17.5mOhm@4.5Vgs/ 84.08707.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->350KHz

1st

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Taipei Hsien 221, Taiwan, R.O.C.

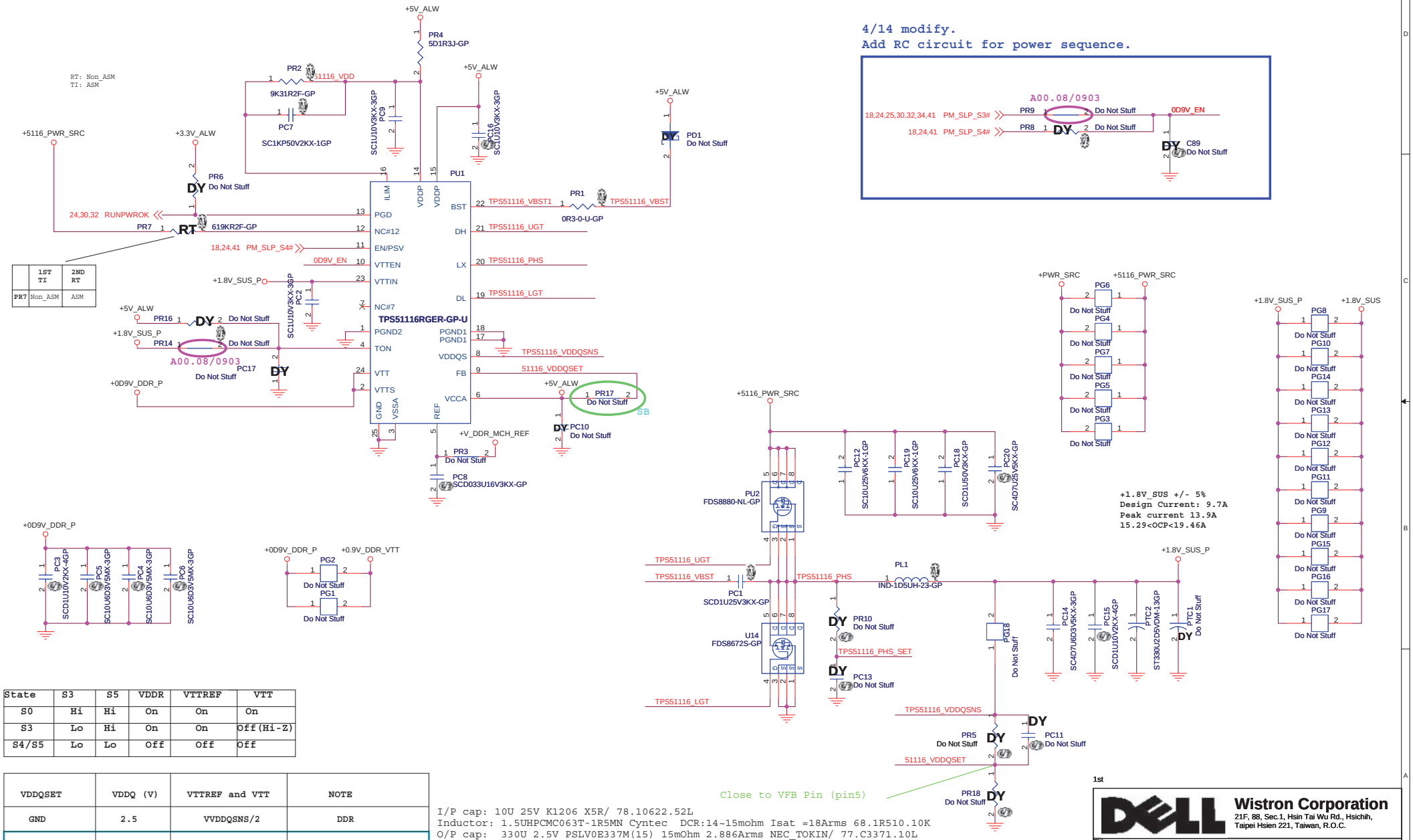
Title: DC to DC 1.05V

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 30 of 59

SSID = PWR.Plane.Regulator_1p8v0p9v

TI TPS51116 for 1.8V and 0.9V



4/14 modify.
Add RC circuit for power sequence.

+1.8V_SUS +/- 5%
Design Current: 9.7A
Peak current 13.9A
15.29<OCP<19.46A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

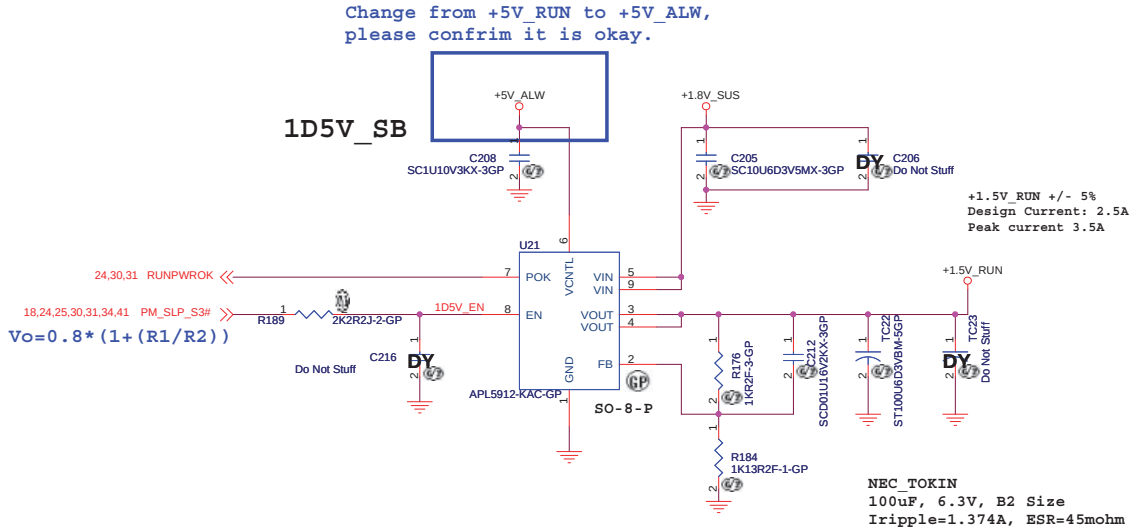
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UHPCMC063T-1R5MN Cyntec DCR:14~15mohm Isat =18Arms 68.1R510.10K
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.8V/0.9V
Size: Custom | Document Number: DR2 17" UMA | Rev: -1
Date: Monday, May 18, 2009 | Sheet 31 of 59

SSID = PWR.Plane.Regulator_1p5v



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Title: DC to DC 1.5V

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 32 of 59

(Blanking)

1st

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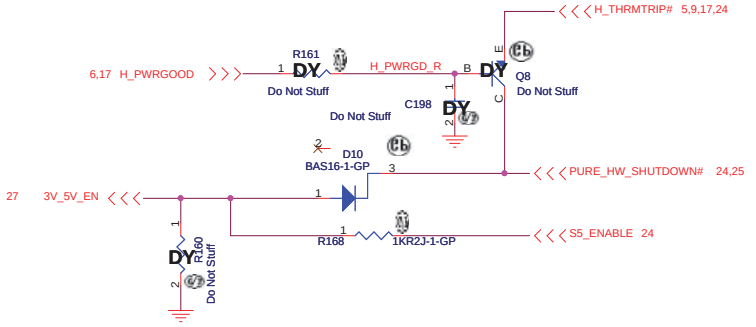
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA Power

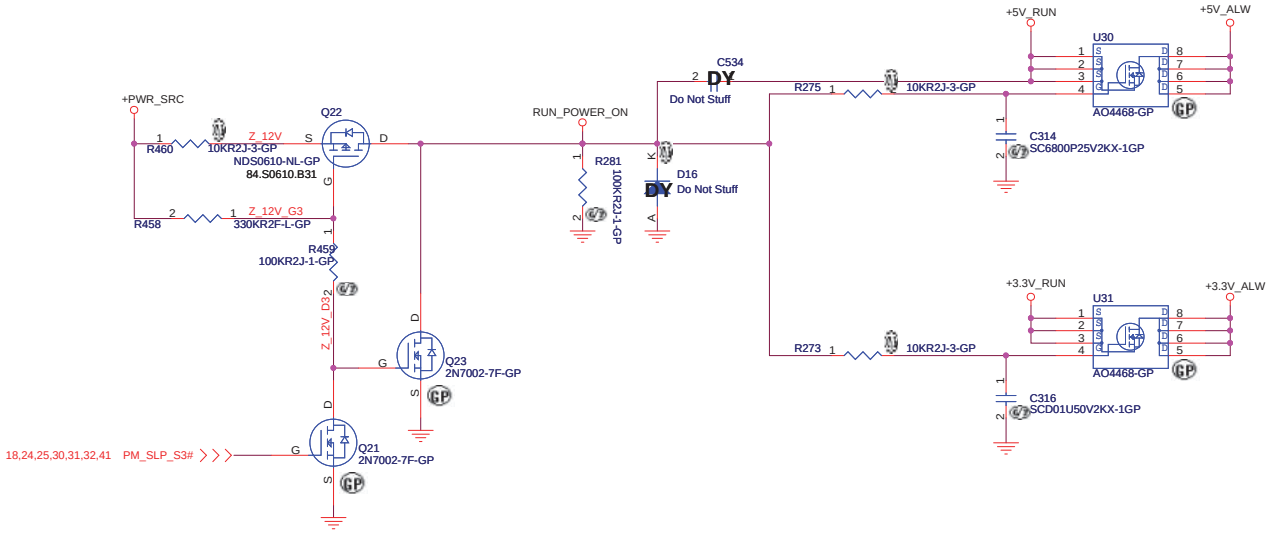
Size: Custom | Document Number: DR2 17" UMA | Rev: -1

Date: Monday, May 18, 2009 | Sheet 33 of 59

SSID = Reset.Suspend



Run Power



1st

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

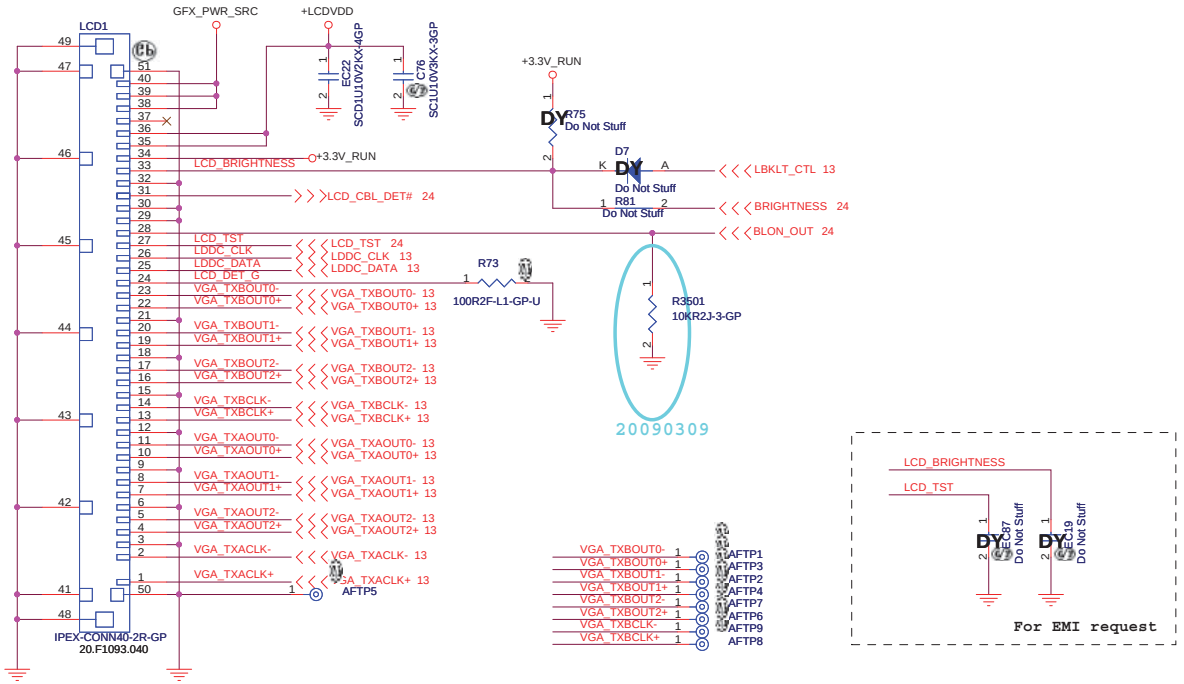
Title: Power Plane Enable

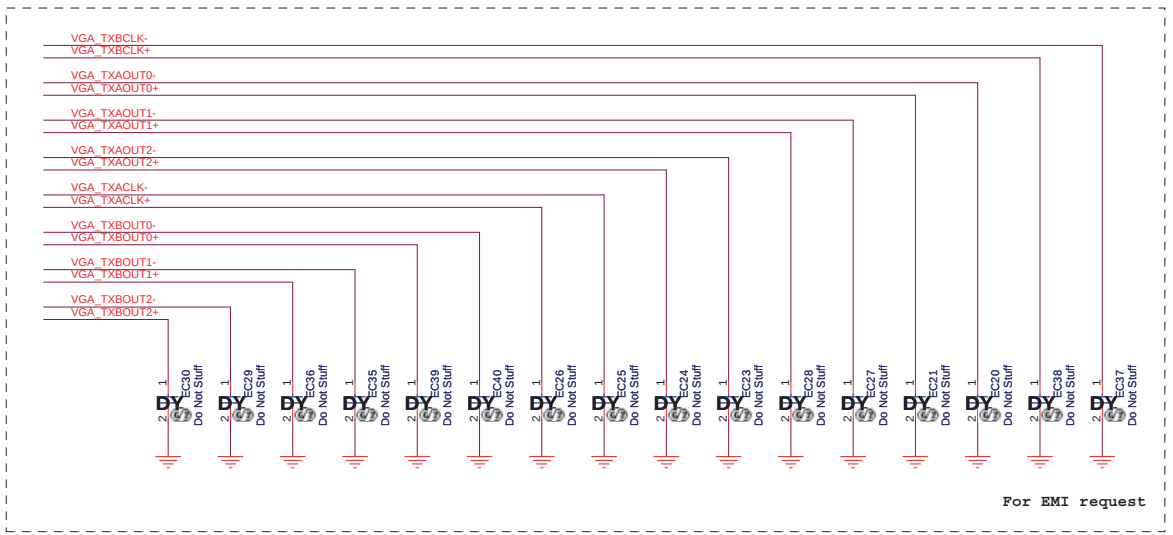
Size	Document Number	Rev
Custom	DR2 17" UMA	-1

Date: Monday, May 18, 2009 Sheet 34 of 59

SSID = VIDEO

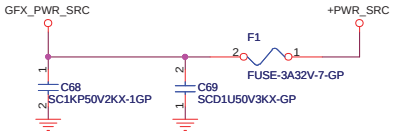
LVDS CONNECTOR





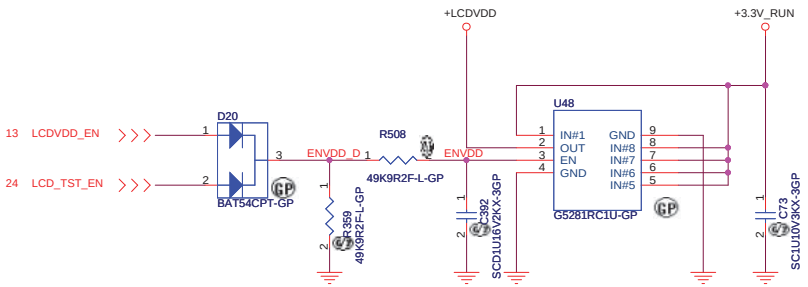
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



1st

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Taipei Hsien 221, Taiwan, R.O.C.

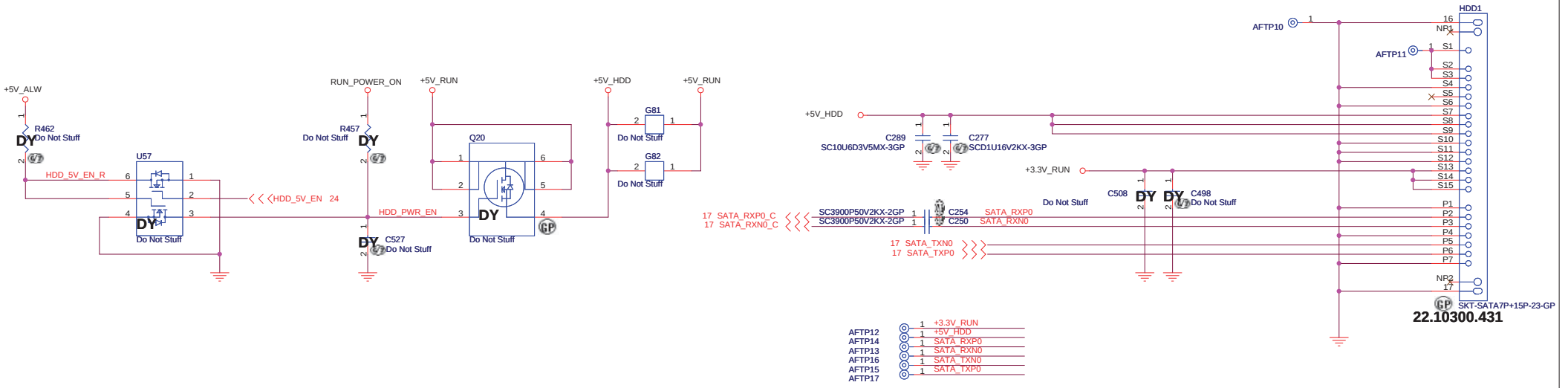
Title: *LCD/Inverter Connector*

Size	Document Number	Rev
Custom	*DR2 17" UMA*	-1

Date: Monday, May 18, 2009 Sheet 35 of 59

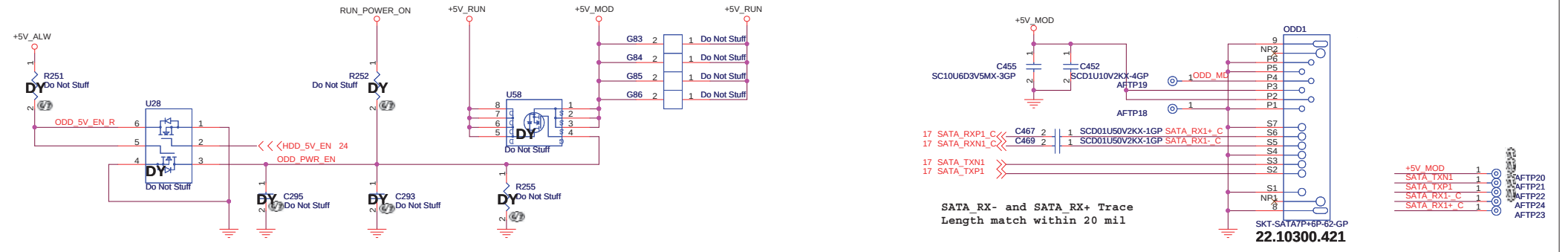
SSID = SATA

SATA HDD Connector



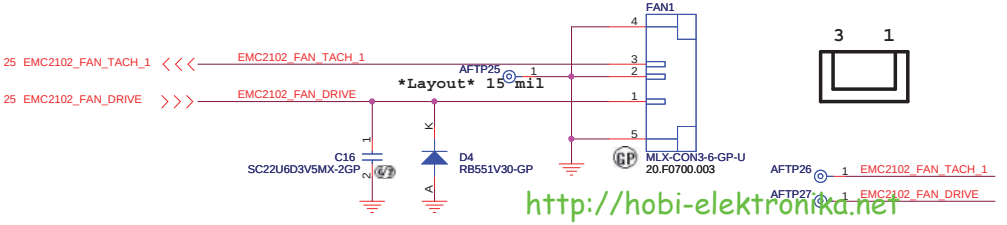
SSID = SATA

ODD Connector



SSID = Thermal

Fan Connector



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Title	HDD/ODD/FAN	
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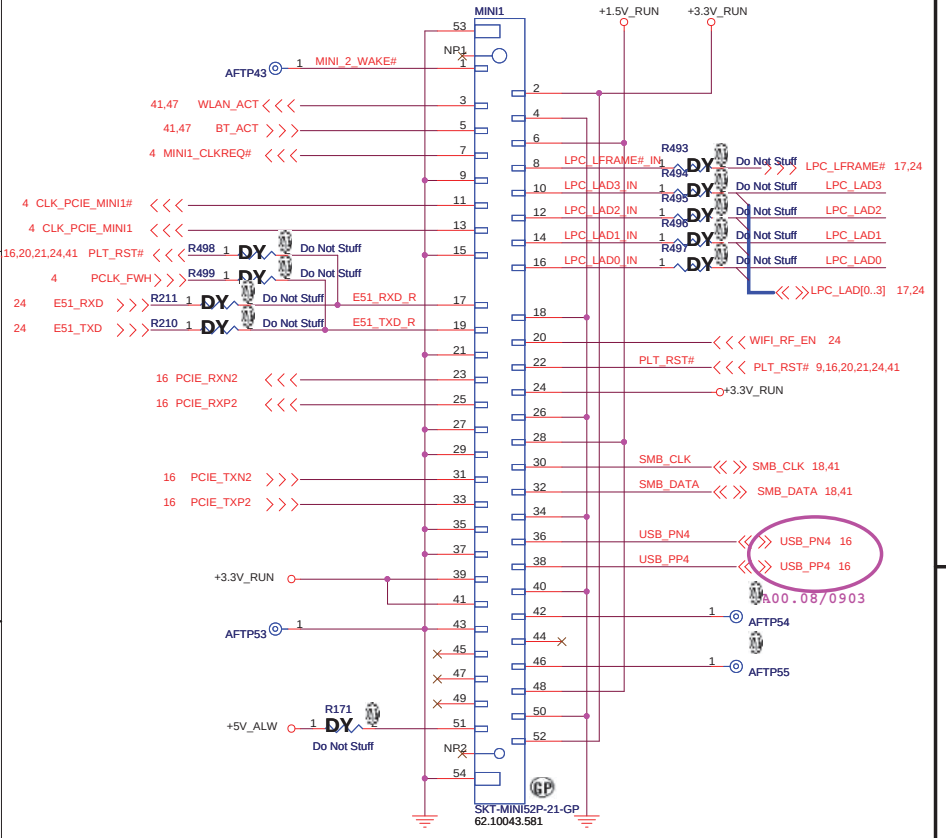
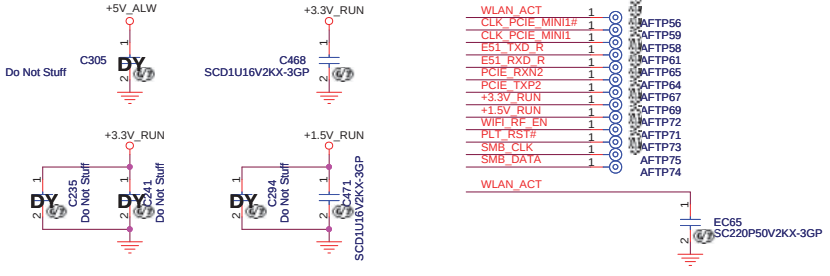
SSID = Wireless

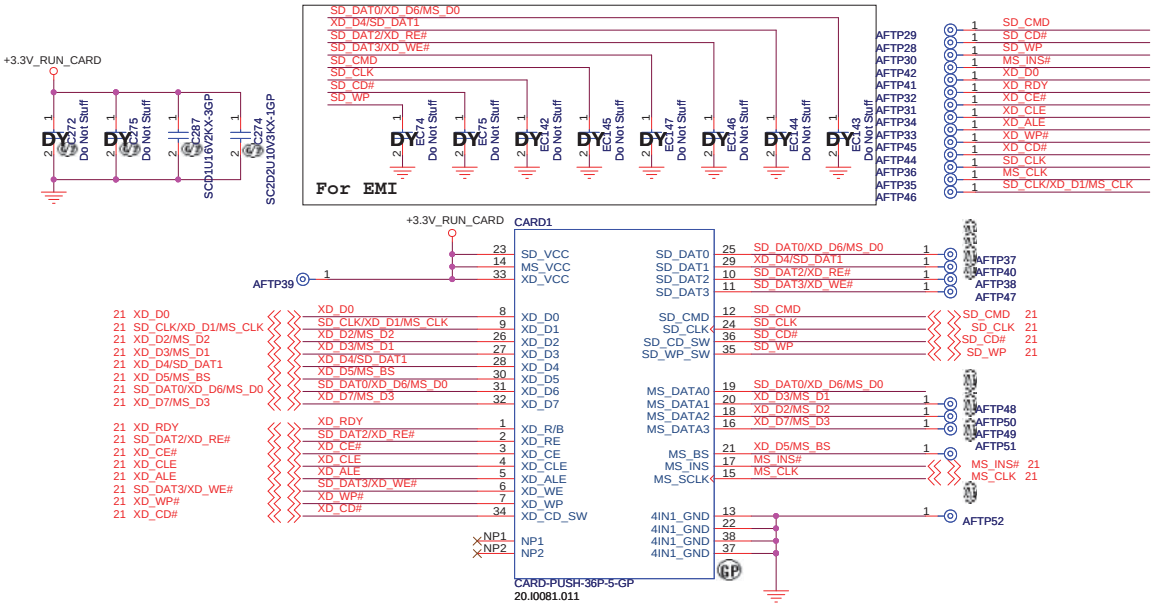
Mini Card Connector(802.11a/b/g)





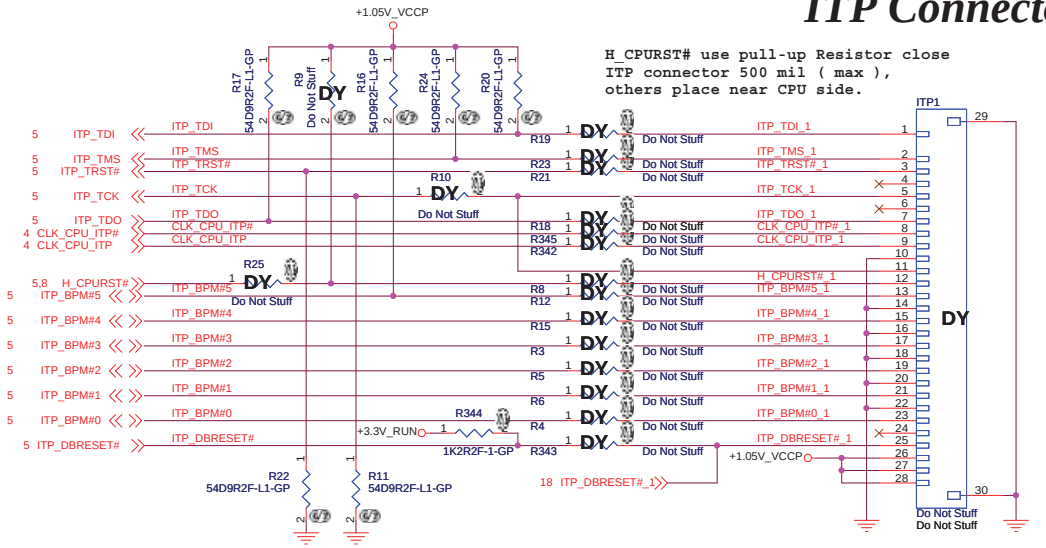
SSID = SDIO

SD/XD/MS Card Reader



SSID = User.Interface

ITP Connector



+1.05V_VCCP use Decoupling Capacitor close ITP connector 100 mil (max)

CPU

TCK(PIN AC5)

ITP Connector

TCK(PIN 5)

FBO(PIN 11)

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Title: MINICARD(WLAN)/SD/ITP CONN

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(Blanking)

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Title: MINICARD(WWAN)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WPAN)

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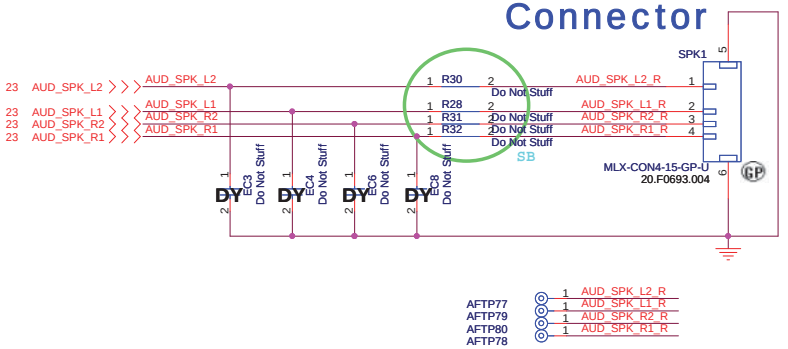
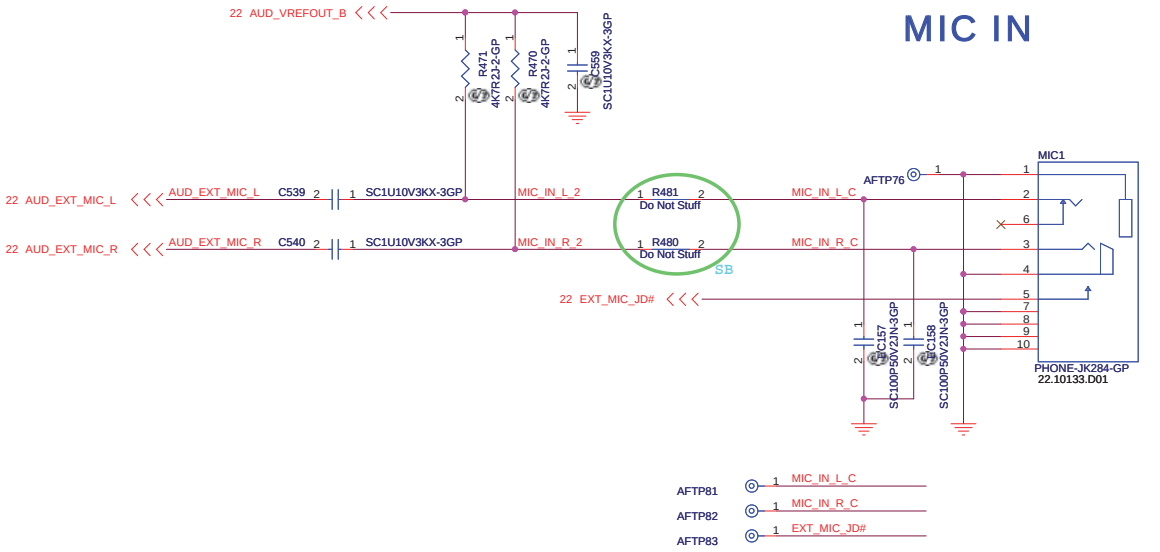
SSID = AUDIO

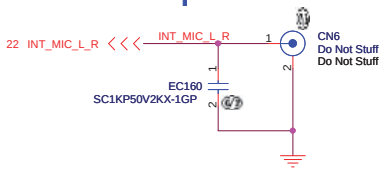
Speaker Connector



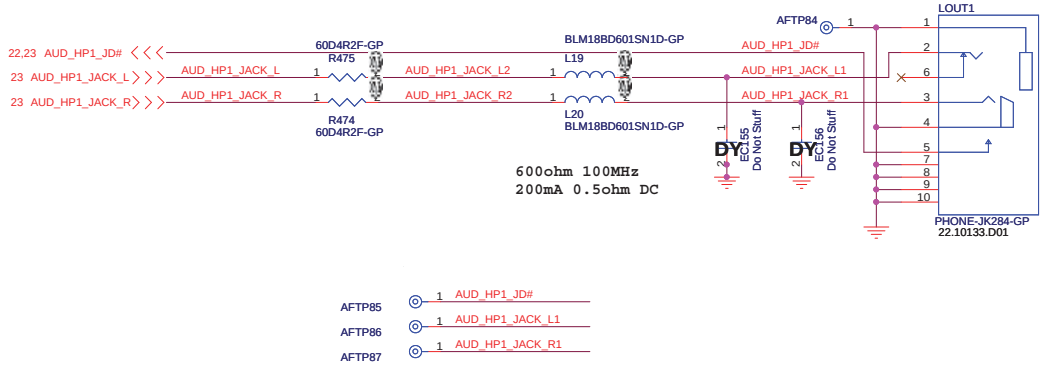
MIC IN



Internal Microphone



LINE1 OUT



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Title: Audio Jack

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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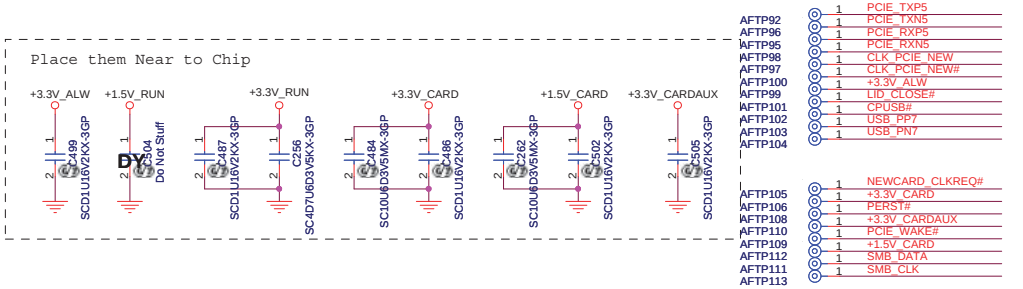
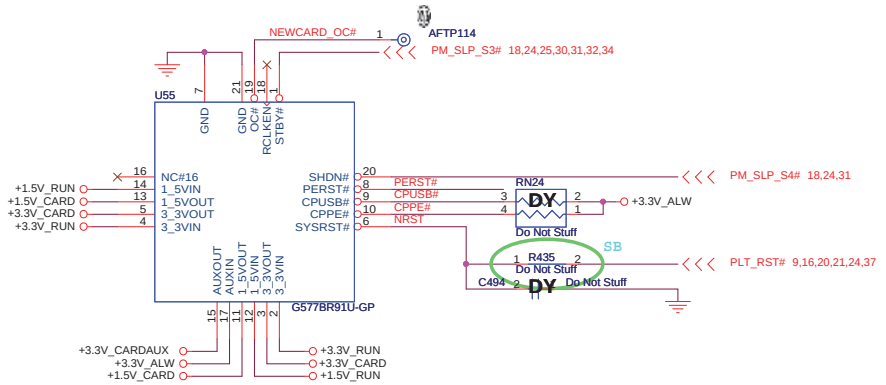
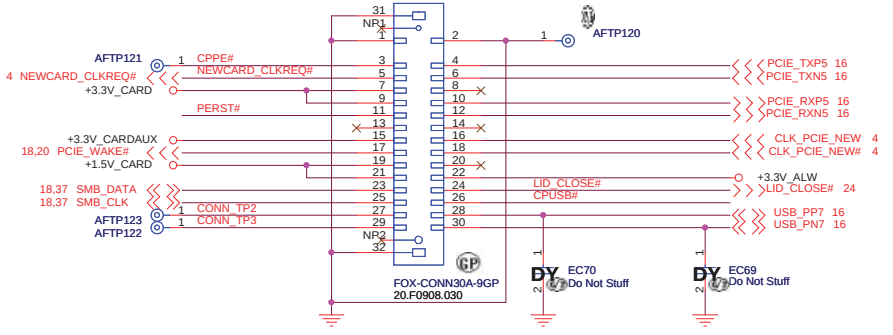
SSID = ExpressCard





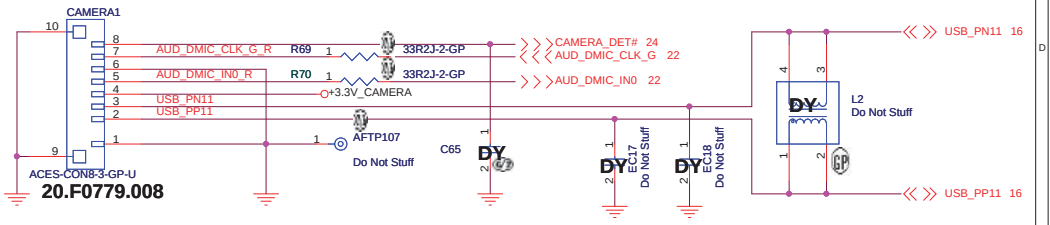
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

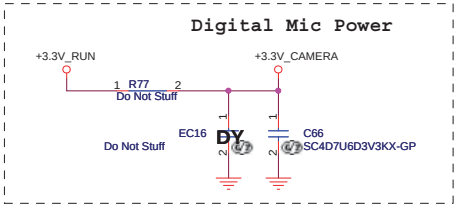
New Card Connector

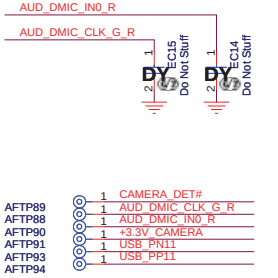


SSID = User.Interface

Camera Connector

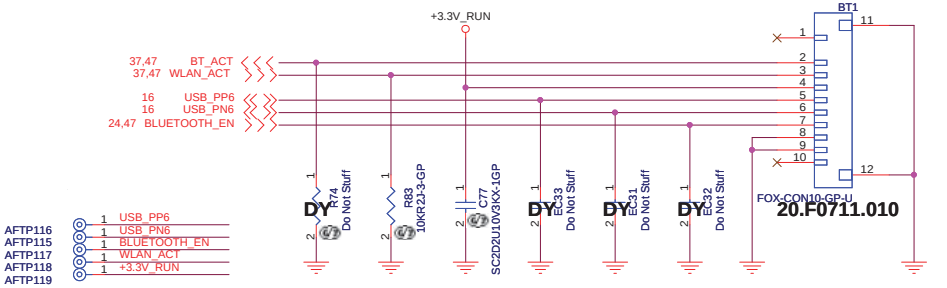






SSID = User.Interface

Bluetooth Module conn.



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Title: **Bluetooth/CAM/New Card**

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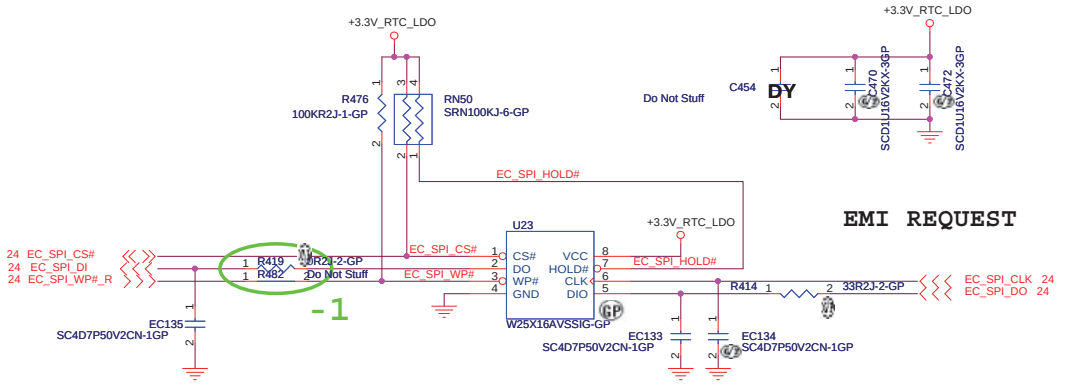
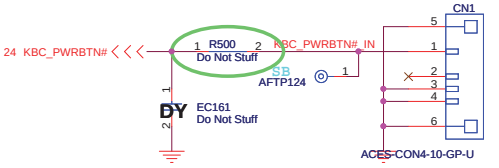
SPI FLASH ROM (16M bits)

SSID = Flash.ROM



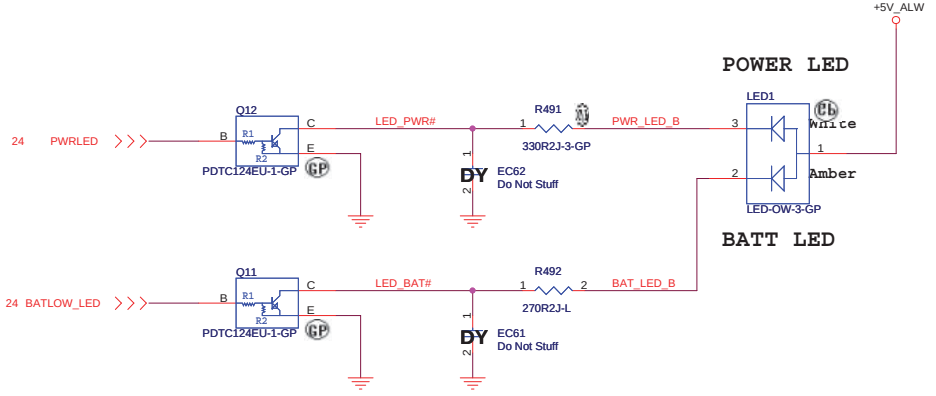
SSID = User.Interface

Power Dash Board to Board CONN



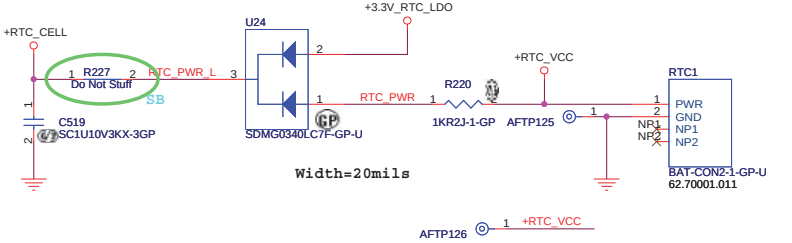
SSID = User.Interface

Power/Battery LED



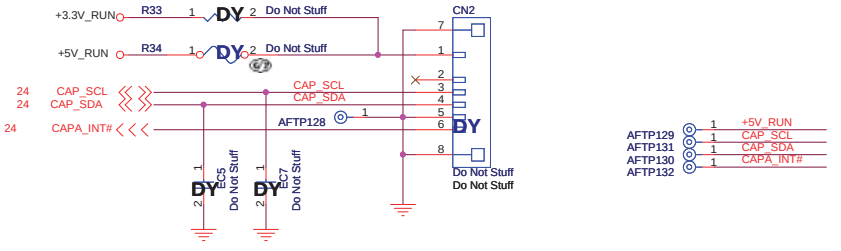
SSID = RBATT

RTC Connector



SSID = User.Interface

Capacitive Button



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Title: FWH/LED/Power Dash/RTC/Cap

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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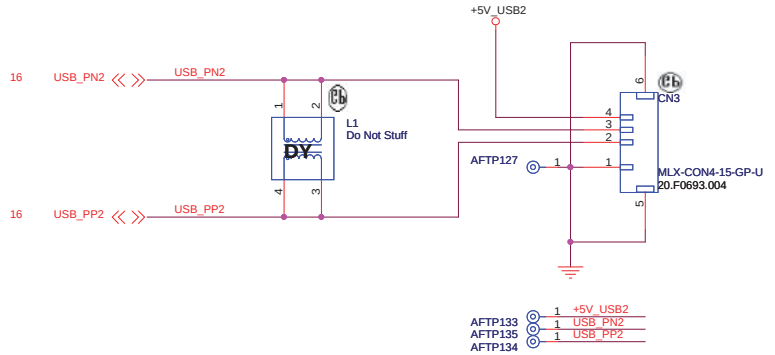
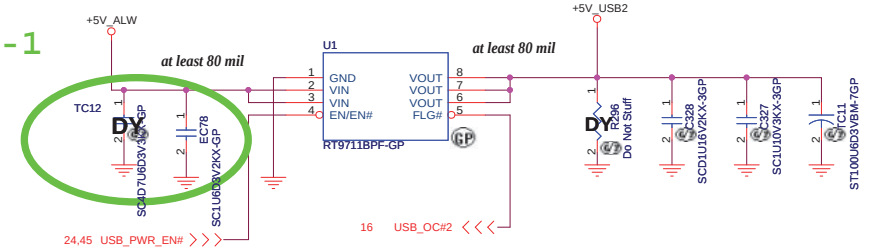
SSID = USB

Right USB Port CONN





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Title: USB

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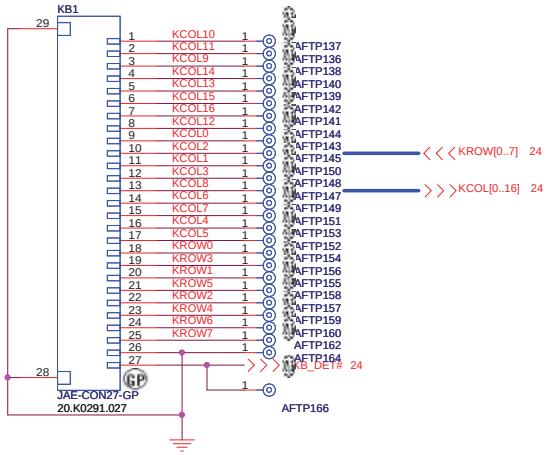
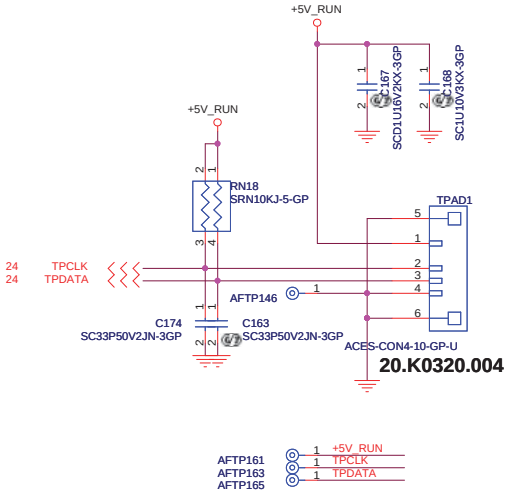
SSID = KBC

Internal KeyBoard Connector

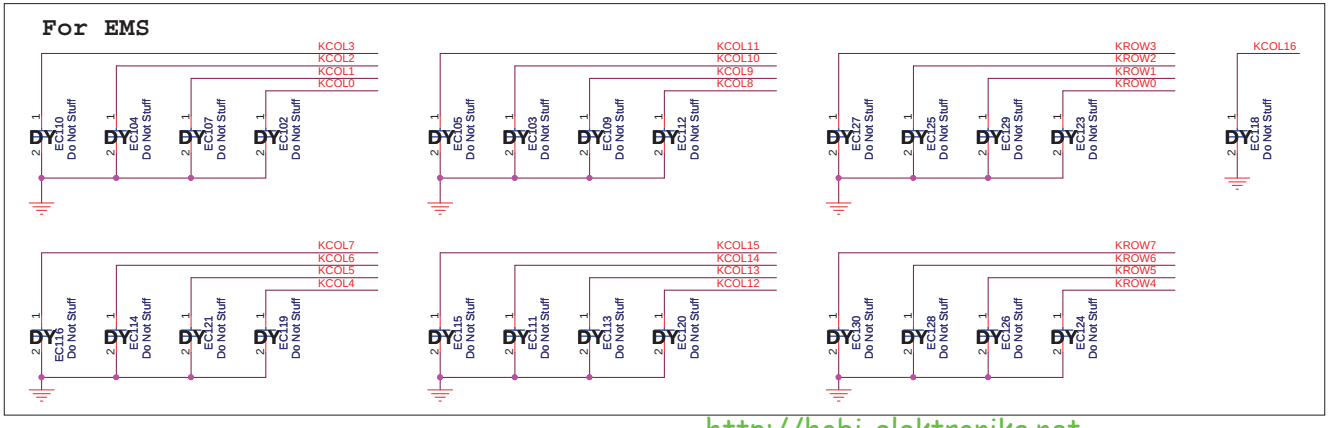


SSID = Touch.Pad

TouchPad Connector



For EMS



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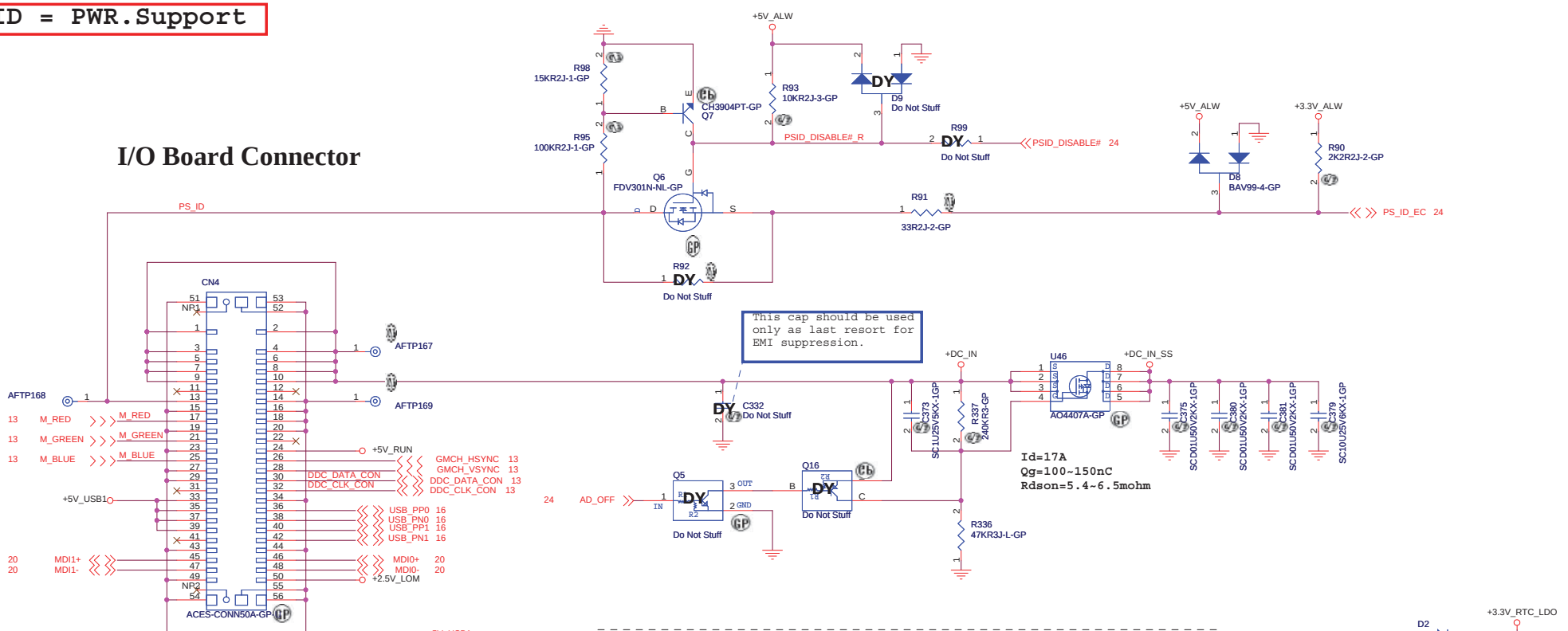
Title: KeyBoard/Touch Pad

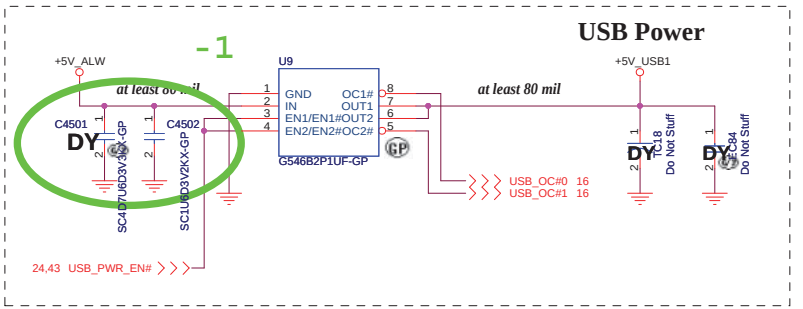
Size: Custom | Document Number: DR2 17" UMA | Rev: -1

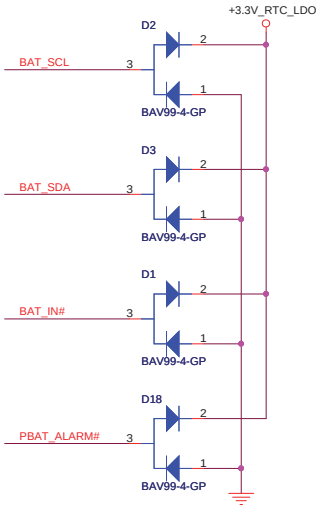
Date: Monday, May 18, 2009 | Sheet 44 of 59

SSID = PWR.Support

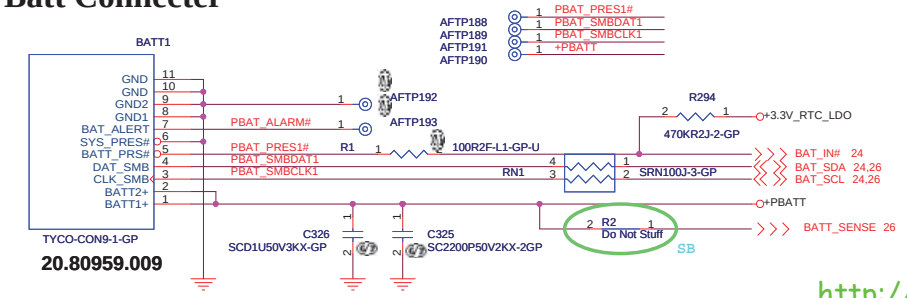
I/O Board Connector

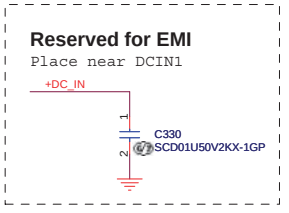






Batt Connecter





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Title: LEFT IO/DCIN/BATT CONN

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SSID = LOM

SSID = VIDEO

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Title: LAN CONNECTOR / CRT

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SSID = Mechanical

+3.3V_RTC_LDO

EC54 Do Not Stuff
EC151 Do Not Stuff
EC91 SCD1U16V2KX-3GP
EC88 Do Not Stuff

+3.3V_RUN

EC93 SC47P50V2JN-3GP
EC9 Do Not Stuff
EC71 Do Not Stuff
EC122 Do Not Stuff
EC108 Do Not Stuff

+5V_ALW

EC60 Do Not Stuff
EC53 Do Not Stuff
EC96 Do Not Stuff
EC99 SC47P50V2JN-3GP

+DC_IN_SS

EC92 Do Not Stuff
EC324 SCD1U50V3KX-GP

+PWR_SRC

EC97 Do Not Stuff
EC13 Do Not Stuff
EC1 SCD1U50V3KX-GP
EC94 Do Not Stuff

+1.05V_VCCP

EC49 Do Not Stuff
EC138 Do Not Stuff
EC51 Do Not Stuff
EC89 Do Not Stuff
EC2 Do Not Stuff
EC131 Do Not Stuff

24,41 BLUETOOTH_EN
37,41 WLAN_ACT
37,41 BT_ACT

EC162 Do Not Stuff
EC163 Do Not Stuff
EC164 Do Not Stuff

+5V_MOD

EC165 Do Not Stuff
EC166 Do Not Stuff

+5V_ALW +3.3V_ALW

EC167 Do Not Stuff
EC168 Do Not Stuff
EC169 Do Not Stuff

+0.9V_DDR_VTT

EC41 Do Not Stuff
EC34 Do Not Stuff
EC43 Do Not Stuff

+1.8V_SUS

EC45 Do Not Stuff
EC44 Do Not Stuff
EC47 Do Not Stuff
EC46 Do Not Stuff
EC55 Do Not Stuff
EC98 Do Not Stuff
EC106 Do Not Stuff
EC117 Do Not Stuff

+3.3V_RUN

EC91 Do Not Stuff

H18 Do Not Stuff
H11 Do Not Stuff
H5 Do Not Stuff
H13 Do Not Stuff
H15 Do Not Stuff
H12 Do Not Stuff
H9 Do Not Stuff
H10 Do Not Stuff
H4 Do Not Stuff
H17 Do Not Stuff
H20 Do Not Stuff

For TP button holder touch.

H3 Do Not Stuff
H2 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff
H1 Do Not Stuff
H6 Do Not Stuff

H14 HOLE
H16 HOLE
H19 HOLE

34.4W005.001 Mini Card BOSS
34.4W004.001 New Card BOSS
34.4W001.001 NB Thermal BOSS

BOSS Placement

+5V_RUN

EC85 Do Not Stuff
EC101 Do Not Stuff
EC82 Do Not Stuff

+5V_RUN

EC90 Do Not Stuff
EC11 Do Not Stuff
EC50 Do Not Stuff
EC68 Do Not Stuff
EC153 Do Not Stuff
EC152 Do Not Stuff
EC148 Do Not Stuff
EC67 Do Not Stuff
EC59 Do Not Stuff
EC52 Do Not Stuff
EC100 Do Not Stuff
EC95 SCD1U16V2KX-3GP

+3.3V_RUN

EC83 Do Not Stuff
EC137 Do Not Stuff
EC150 Do Not Stuff
EC159 Do Not Stuff

+3.3V_RUN

EC58 Do Not Stuff
EC10 Do Not Stuff
EC86 Do Not Stuff
EC64 Do Not Stuff
EC141 Do Not Stuff
EC149 Do Not Stuff
EC136 Do Not Stuff
EC72 Do Not Stuff
EC63 Do Not Stuff
EC42 Do Not Stuff
EC66 Do Not Stuff
EC73 SCD1U16V2KX-3GP

+PWR_SRC

EC173 Do Not Stuff
EC171 Do Not Stuff
EC172 Do Not Stuff
EC170 Do Not Stuff
EC174 Do Not Stuff

SPR2 SPRING-24-GP 34.45T31.001
SPR3 SPRING-24-GP 34.45T31.001
SPR5 SPRING-58-GP 34.4B312.002
SPR4 SPRING-24-GP 34.45T31.001
SPR1 SPRING-24-GP 34.45T31.001
SW1 SPRING-24-GP
Spring

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Title: MISC

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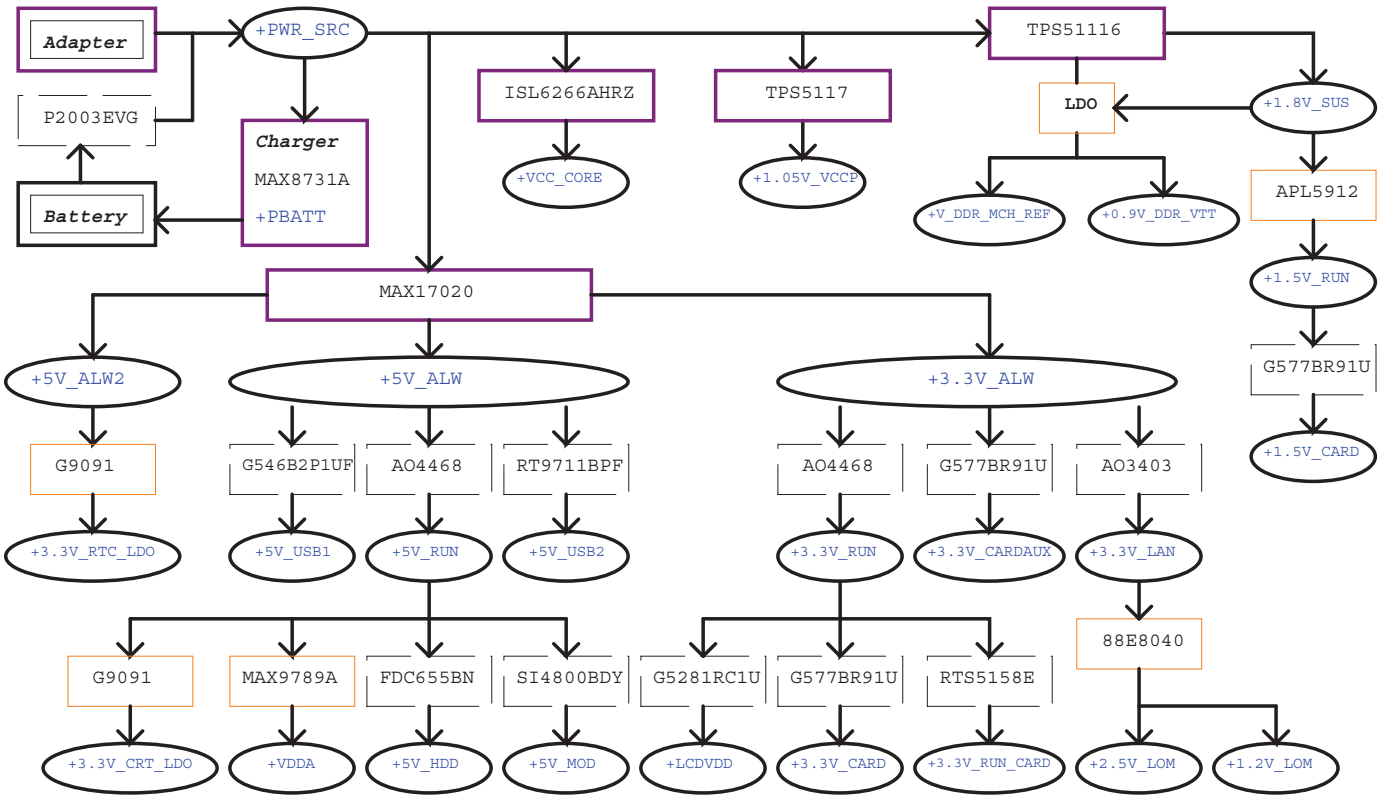

Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

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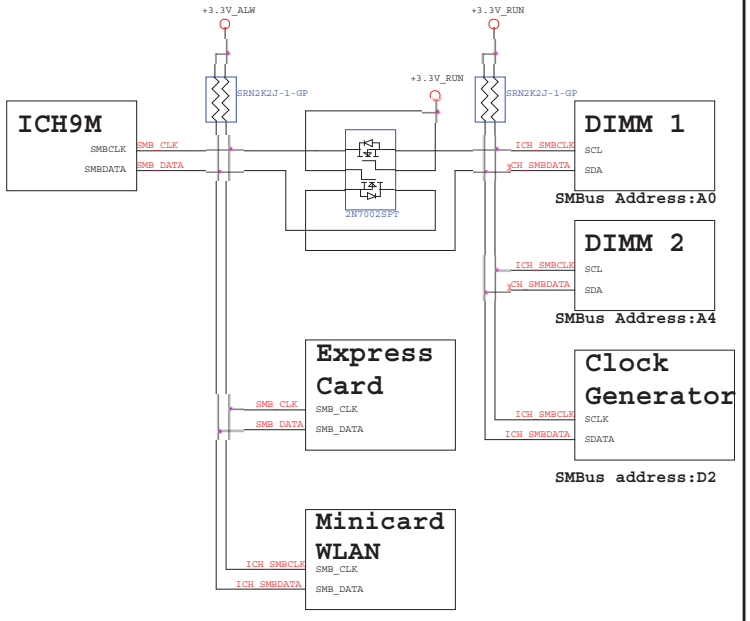
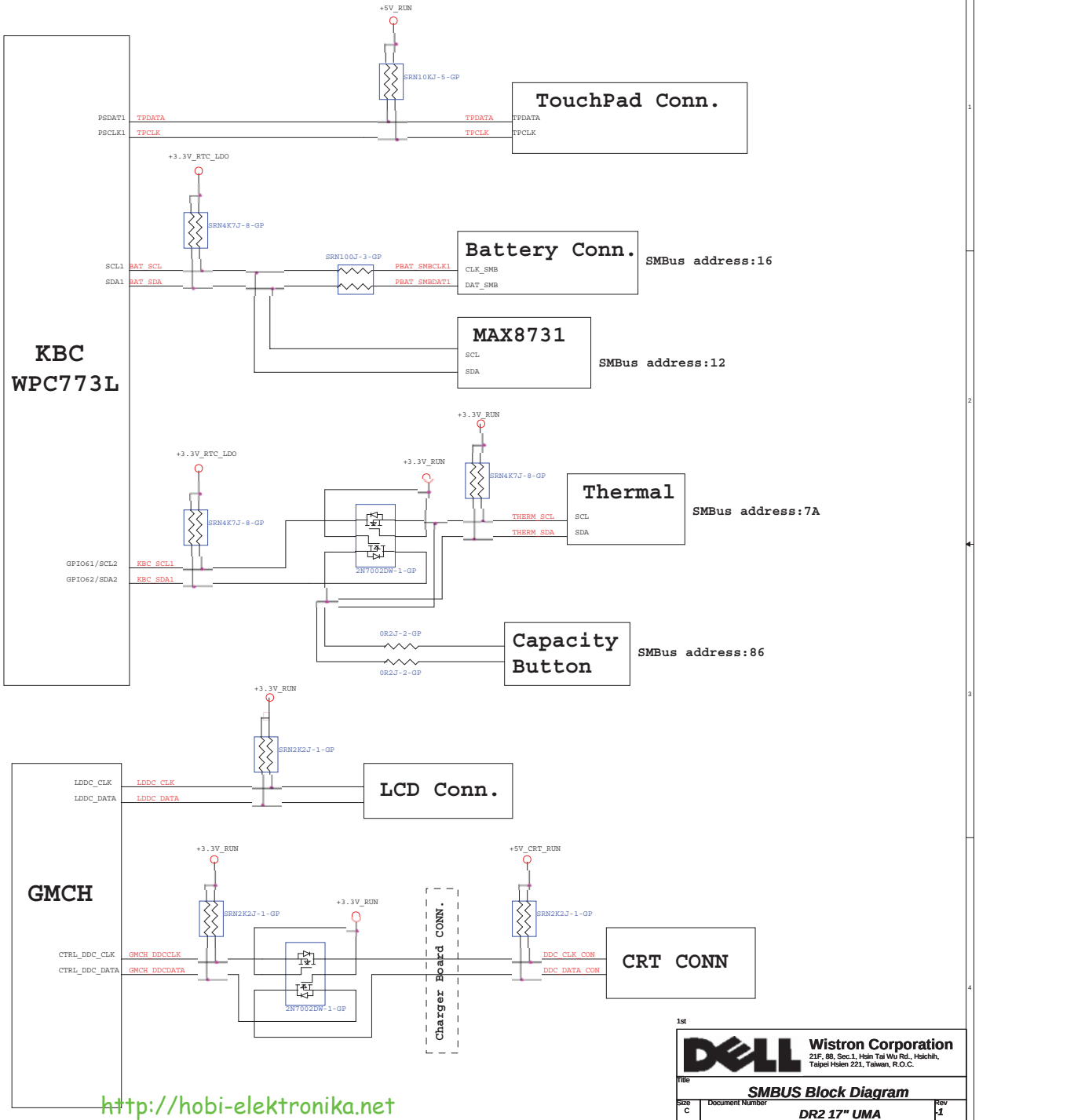
ICH9M SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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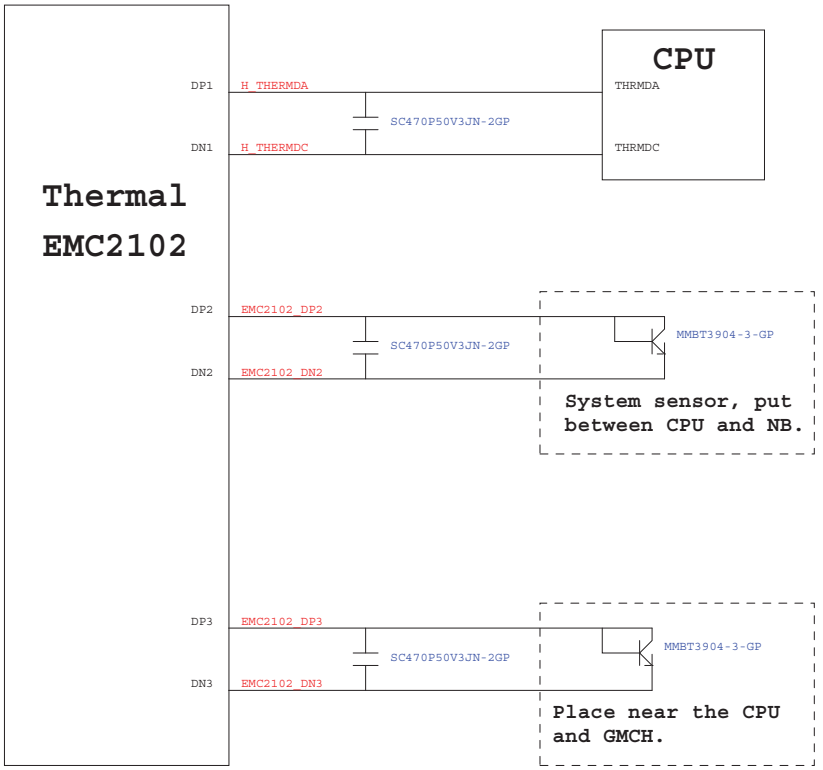
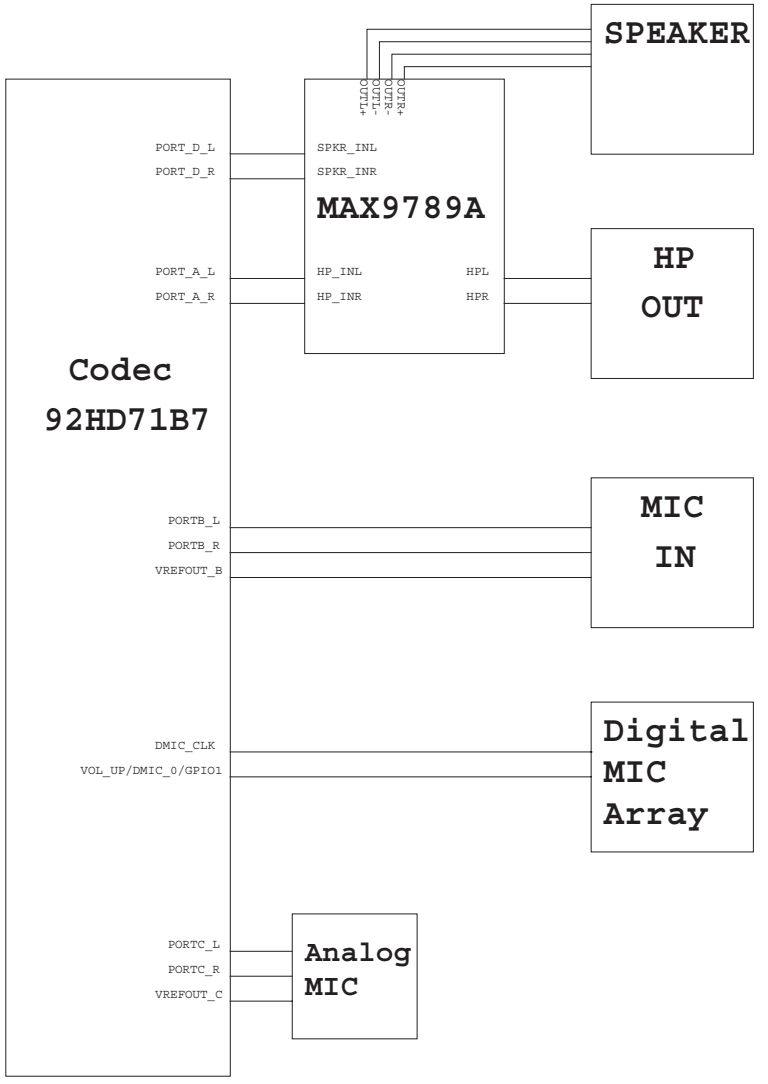
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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Title: VGA-PCIE(1/4)

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Title: VGA-VRAM(2/4)

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Title: VGA-HDMI/STRAP(3/4)

Size: Custom | Document Number: DR2 17" UMA | Rev: -1

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Title: VGA-LVDS/TV/CRT/(4/4)

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Title: VRAM

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	45	CN4 Pin.51 from +DC_IN change to GND.	CN4 Pin.51 should be ground.	EE
		2	24	Dummy R422	LID SW is push-pull type, no need pull high.	EE
		3	41	CAMERA1 conn reduce from 10 to 8 pin.	Follow camera design.	EE
		4	42	RTC1 CONN change p/n: 22.70031.001 to 62.70001.011.	Qty issue to change another.	EE
		5	46	Exchange H14 and H6 names.	Correction. H14 for mini card boss ; H6 is hole.	EE
06/05		6	42	Reverse LED1.	Correction. Amber for BAT_LED_B ; White for PWR_LED_B.	EE
		7	37,41	Remove CN5 and related circuit in page.41. Add dummy R: R493, R494, R495, R496, R497, R498, R499	Remove debug board connector. For debug mini card, change LPC Bus to mini card base. Set dummy res to avoid damaging MB or additional mini card.	EE
		8	37	Dummy R210, R211	For debug mini card. Set dummy res to avoid damaging MB or additional mini card.	EE
06/06		9	24	Dummy R150. Staff R151.	PCB Version for SB.	EE
		10	42	CN1 Pin.2 set to NC. Add R500 and dummy EC161.	Avoid shorting between KBC_PWRBTN# and GND. New R and C are for EMC pre-location.	EE
		11	24	Dummy R406. Change R425, R422, R409, R406, R401, R404 to 100K ohm.	Dummy R406 for no keyboard detect function. R change to 100k for save power.	EE
06/10		12	36	Update HDD symbol.	Update symbol and footprint for only SATA HDD. (no co-layout)	EE
		13	35~45	Change All TP near connectors to AFTP (ZZ.AFT30.101).	For AFTE test pad.	EE
		14	04	Change C461 and C462 from 15pF to 12pF.	For X3 cap choice by report suggestion.	EE
		15	17	Change C520 and C522 from 15pF to 12pF.	For X4 cap choice by report suggestion.	EE
06/12		16	24,42	Add 0 ohm R482 on EC_SPI_WP# and link to KBC/GPIO30. Change RN50 to 100k and Add R476 for EC_SPI_WP#.	KBC can control WP# of Flash ROM. R change to 100k for save power.	EE
		17	40	Change L19 and L20 to 68.00082.531.	For EMI.	EE
		18	45	Change M_RED to CN4 Pin.17 ; M_GREEN to CN4 Pin.21 ; M_BLUE to CN4 Pin.25. CN4 Pin.23 and Pin.27 to GND.	Avoiding noise to impact CRT signals.	EE
		19	47	Add H20.	Add square GND for TP button holder touch.	EE
06/16		20	42	Dummy CN2, R34.	Cap. button function is disable.	EE
		21	47	Add dummy EC162, EC163, EC164. Add dummy EC165, EC166. Add dummy EC167, EC168, EC169.	For EMI.	EE
06/17		22	04	Change R216 to 22 ohm.	The same clock dirve to U25 and U34.	EE
06/18		23	44	Dummy EC110, EC104, EC107, EC102, EC105, EC103, EC109, EC112, EC127, EC125, EC129, EC123, EC118, EC116, EC114, EC121, EC119, EC115, EC111, EC113, EC120, EC130, EC128, EC126, EC124.	For EMI.	EE
06/19		24	43	Short R26, R27.	No need 0 ohm R.	EE
		25	47	Add SW1.	ME request.	EE
		26	35	LCD1.38 link to GFX_PWR_SRC ; LCD1.37 set NC ; LCD1.35 link to +LCDVDD ; LCD1.34 link to +3.3V_RUN ; LCD1.33 link to LCD_BRIGHTNESS ; LCD1.32 to GND ; LCD1.31 link to LCD_CBL_DET#.	For LED backlight panel.	EE
		27	18	Dummy R179, R423.	SW check vender ID by SMBus.	EE
		28	24	Dummy R416, R418.	Cap. button function is disable.	EE
		29	40	Change LOUT1 and MIC1 to 22.10133.D01.	Change jack source.	EE
		30	17,18	Dummy U25.B10 link R506 to GND; U25.C18 link R501 to GND; Dummy U25.C21 link R502 to GND; U25.C11 link R503 to GND; Dummy U25.AE18 link R504 to GND; U25.AF21 link R505 to GND. Dummy R421, R424.	Avoiding abnormal action in U25(ICH9-M).	EE
06/23		31	25	Change R82 to 20K 1% ; Change R78 to 10K 1%.	For T8 shutdown is set 88 deg-C.	EE
		32	47	Add dummy EC170, EC171, EC172, EC173, EC174.	For EMI.	EE
06/27		33	42	Change U23 to 72.25X16.A01.	Better performance.	EE

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Title: Change List - EE (1/3)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
07/30	X02	34	18	Staff R421, R424. (PT build cut-in)	Avoiding always issue interrupt event.	EE
		35	23	Dummy R290 ; Staff R291. (PT build cut-in)	Adjust audio amp. gain value.	EE
		36	20	Add dummy R507.	Add RUN power for LAN.	EE
		37	21	Short R253, R254.	No need 0 ohm R.	EE
		38	24	Staff R138, R150 ; Dummy R141, R151.	PCB Version for SC.	EE
		39	35	Add R508 ; Change R359 to 49.9k ohm.	For LCD power sequence.	EE
		40	22,23	Move C535 (Change 0.033uF), R472 to page.23. Remove C536 (Change 0.033uF), C542. Add R484 to gnd ; Add C566 for AUD_SET, C567 for AUD_BIAS. C565 for 6040 only.	For PC beep.	EE
		41	36	Material change: HDD1	ME request.	EE
		42	37	Material change: CARD1	ME request.	EE
		43	47	Material change: SPR4	ME request.	EE
		44	09	Add TP271 for U52/ SDVO_CTRLDATA.	TP.	EE
08/06		45	41	Short R79, R80.	No need 0 ohm R.	EE
		46	04	Symbol change: U54.	For clock generator co-layout.	EE
		47	-	Change to close line: R204, R200, R356, R139, R152, R408, R394, R390, R403, R402, R96, R120, R378, R360, R140, R373, R97, R405, R155, R154, R262, R266, R439, R265, R226, R269, R174, R175, R183, R432, R433, R434, R430, R431, R437, R191, R177, R270, R188, R436, R452, R259, R282, R250, R249, R467, R153, R81, R77.	No need 0 ohm R.	EE
		48	24,32	Move R182 to page.24.	Movement.	EE
		49	37	Short R428, R426 ; Add DY L21.	Pre-location for Minicard USB trace.	EE
08/07		50	-	Short R139, R96 , R155, R154, R226, R174, R175, R432, R433.	No need 0 ohm R.	EE
		51	19	Staff C488.	For DMI.	EE
08/11		52	23	Use 2.2uF C564 and C557 for Maxim U62 IC.	For improving bobo sound.	EE
		53	32	Material change: TC23. (DY)	Material issue.	EE
08/15		54	11	Material change: TC19, TC21.	Material issue.	EE
09/02	A00	55	21	USB_PP10 for U34.5 ; USB_PN10 for U34.4. (ST build cut-in)	Schematic modification.	EE
		56	24	Staff R151 ; Dummy R150.	PCB Version for -1(Xbuild).	EE
		57	24	Add dummy R509 to gnd for KBC GPIO24. (09/10 update)	For GM45.	EE
09/03		58	05,17	Dummy R76 ; Staff R167	For H_THRMTRIP# to SB.	EE
		59	12,20,24	Change to close line: R115, R246, R182, R158, R159, R170.	No need 0 ohm R.	EE
09/09		60	37	Remove L21.	No need L21.	EE
		61	19	Staff R453, C511 ; DY C521.	Follow Intel DG 2.0.	EE
09/10		62	04	Short RN42, RN43, RN44, RN45, RN48, RN22, RN23, RN54, RN53, RN52, RN51.	No need 0 ohm R.	EE
		63	21	Add dummy R510 and C568. Staff R282 0 ohm.	For U34 power bounce issue.	EE
09/22		64	04	Dummy R196.	For debug. Normally, no need it.	EE
		65	25	R82 change to 10k ; R78 change to 2.37k.	For T8 thermal shutdown setting.	EE
		66	23	Staff R288 ; Dummy R289.	For Audio amp. gain.	EE
10/02		67	21	Dummy R284, C318. Staff R282 to Bead 68.00082.531. Staff R510 to 2.2K ; Staff C568.	For U34 power bounce issue.	EE

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Title: Change List - EE (2/3)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
05/18	-1	1	43	EC78 change to 1u	follow u1 spec design	EE
		2	43	TC12 change to 4.7u	follow u1 spec design	EE
		3	45	add c4501 and c4502	follow u1 spec design	EE
		4	24	change R192 from short pad to 0ohm		EE
		5	42	change R419 from short pad to 0ohm		EE
		6	14/15	change R57 R54 R55 R56 from 0ohm to short pad		EE

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Title: Change List - EE (3/3)

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DATE	VERSON	NO	PAGE	Modified List	Issue Description	OWNER
06/03	X01	1	32	R189 change to 2.2K ohm, C216 dummy.	For +1.5V_RUN sequence.	Power EE
		2	30	C378 change to 0.01uF.	For +1.05V_VCCP sequence.	Power EE
		3	34	C316 change from 4.7nF to 0.01uF.	For +3.3V_RUN sequence and improve +3.3V_ALW voltage drop due to SW(U31) turn on quickly (higher loading).	Power EE
		4	34	Staff C314 and change from 4.7nF to 6.8nF.	For +5V_RUN sequence and improve +5V_ALW voltage drop due to SW(U30) turn on quickly (higher loading).	Power EE
06/05		5	36	Dummy Q20, U57, R462, R457, C527 and U58, U28, R251, R252, C293, C295 Change R258, R256 to G81, G82 Change R278, R279, R277, R276 to G83, G84, G85, G86	No sniffer function, no control HDD & ODD power.	Power EE
06/06		6	27	R136 change to 270k and R108 change to 237k	For 5V/3.3V OCP	Power EE
		7	28	R38 change to 12.1k R323 change to 3.92k , C360 change to 0.047 uF 10V X7R	R38 for VCORE OCP R323 and C360 for transient and load line.	Power EE
		8	31	PC9 to GND.	PC9 to GND otherwise DC-DC IC can not obtain power to generate 1.8V/0.9V output.	Power EE
		9	31	PR2 change to 9.31k ohm.	For 1.8V OCP.	Power EE
		10	30	Add D23.	For power sequence.	Power EE
06/10		11	18,24	Remove U60, R482, R476 and change trace name VRMPWRGD to VGATE_PWRGD.	For power sequence.	Power EE
06/18		12	31	PR7.1 link to +5116_PWR_SRC.	Reserve for other source.	Power EE
06/23		13	30	Rename "+1.05V_SUSP" to "+1.05V_RUNP"	Correct naming.	Power EE
		14	26,45	Material change: U37, U46, U47.	NIKO-SEM P2003EVG component has some risk.	Power EE
07/30	X02	15	31	Change PR7 value from 622k to 619k ohm.	For 2nd source.	Power EE
08/11		16	26,45	Material change: U37, U46, U47.	Power team request.	Power EE
09/03	A00	17	26,27, 28,31	Change to close line: R46 ,R137 ,R127,R106 ,R384 ,R391 ,R35 ,R29 ,R307 ,R308 ,R309 ,R303 ,R304 , R298 ,R301 ,R310 ,R313 ,PR14.	No need 0 ohm R.	Power EE
		18	26	R61 change 4.7k to 10k.	Power team request.	Power EE
xx		19				
xx		20				
		21				
		22				
xx		23	x	x	x	Power EE
xx		24	x	x	x	Power EE
		25	x	x	x	Power EE

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Title: ***Change List - Power***

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