

FM7 Hepburn Intel Discrete GFX

VER : D3B

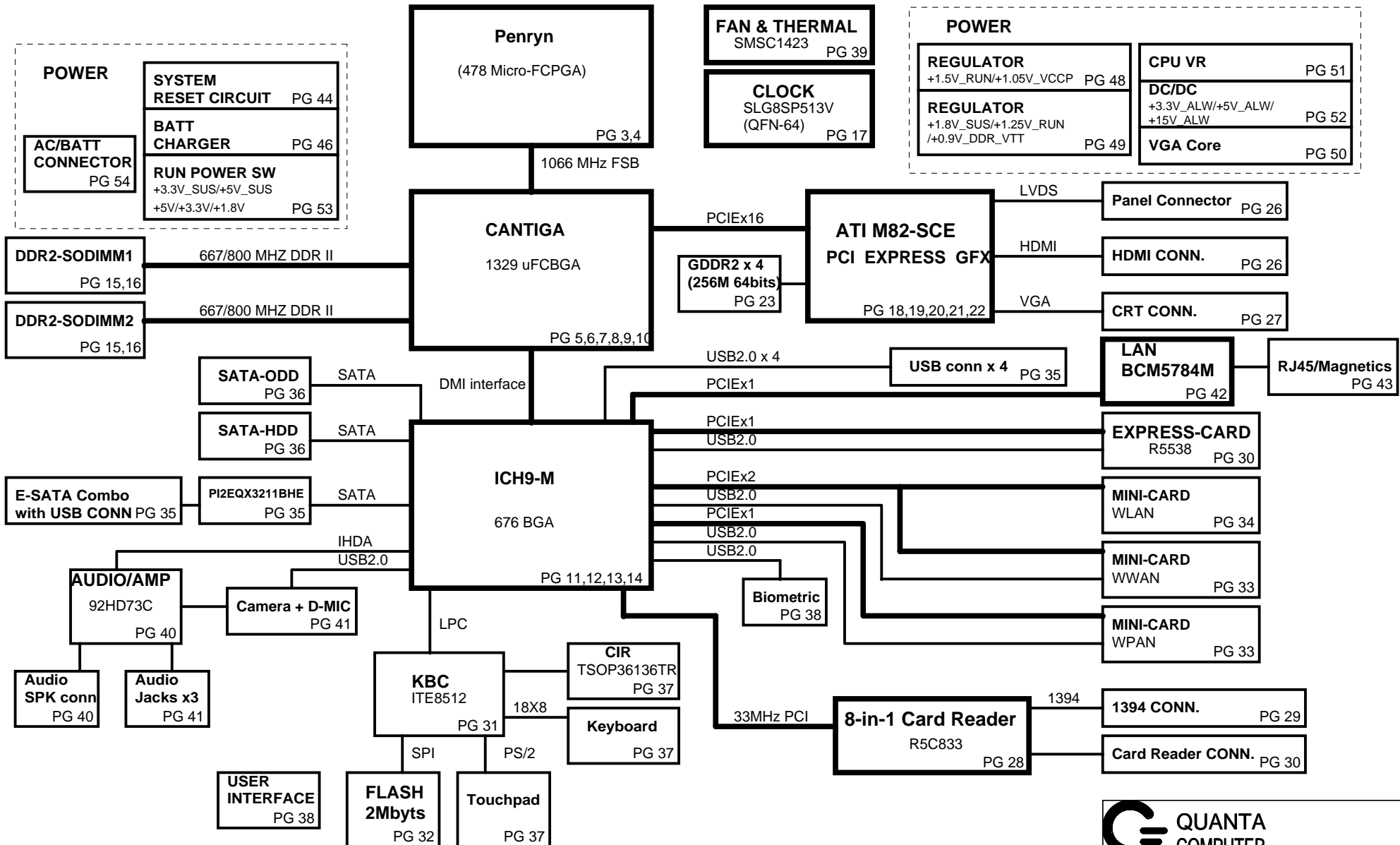









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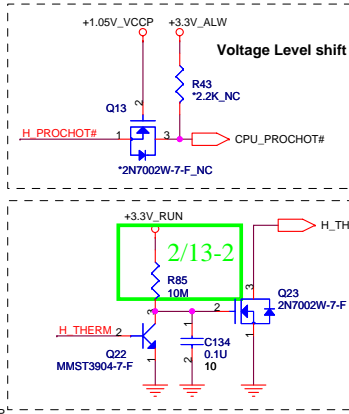
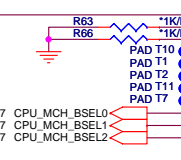
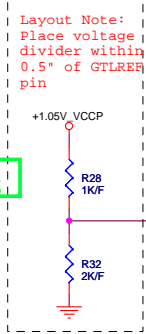
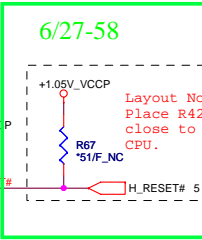
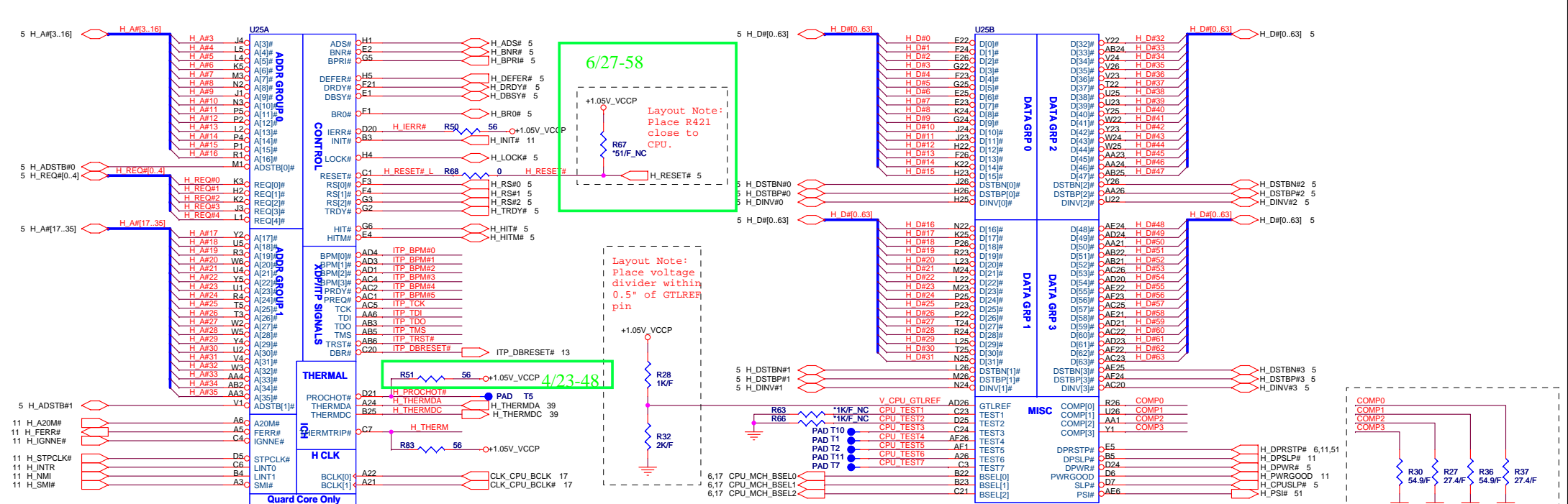
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25	BLANK PAGE
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27	CRT CONN
28	5C833/PCI
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32	FLASH / RTC
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34	MINI-Card (WLAN)
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36	SATA (HDD & CD_ROM)
37	TP / KEYBOARD
38	SWITCH / LED
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55	PAD & SCREW
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58	Power Block Diagram

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52,56	MAIN POWER		S0-S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0-S5
+3.3V_ALW	+3.3V	3,13,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0-S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0-S5
+5V_ALW2	+5V	37,38,52,53	LARGE POWER	+5V_ALW	S0-S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,26,27,36,37,38,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,26,27,28,30,31,33,34,36,38,39,40,41,42,53,56	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,53,56	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.2V_LOM	+1.25V	42	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48,56	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51,56	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	

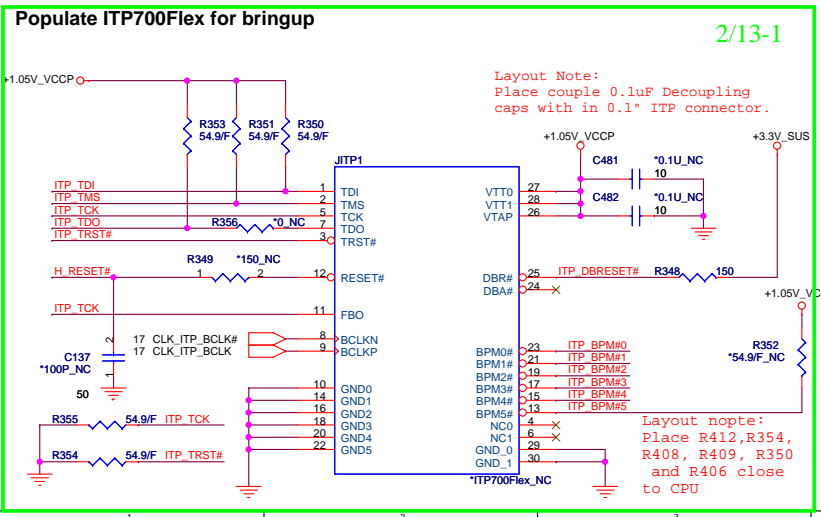
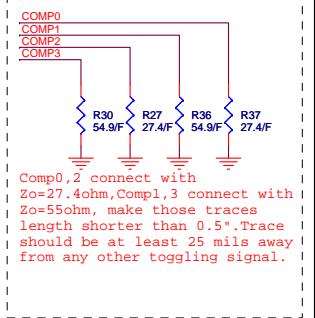
GND PLANE	PAGE	DESCRIPTION
 8731AGND	46	
 AGND_0.9V	49	
 AGND_DC/DC	52	
 AGND_DC2	48	
 AGND_DDR	49	
 AGND_ISL6260	51	
 GND	ALL	



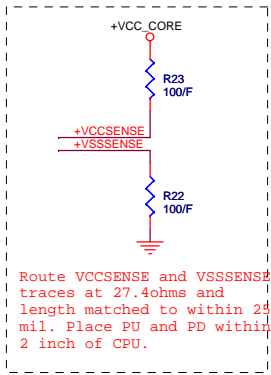
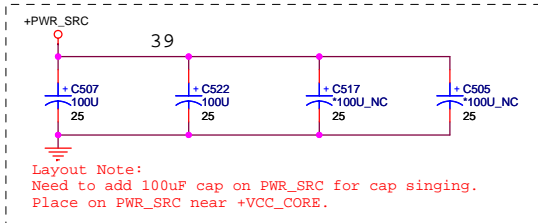
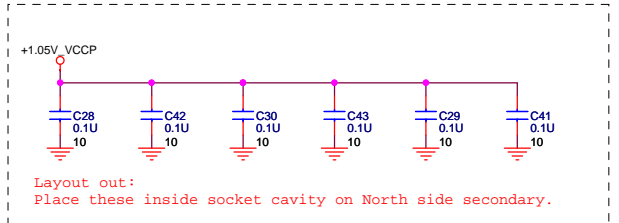
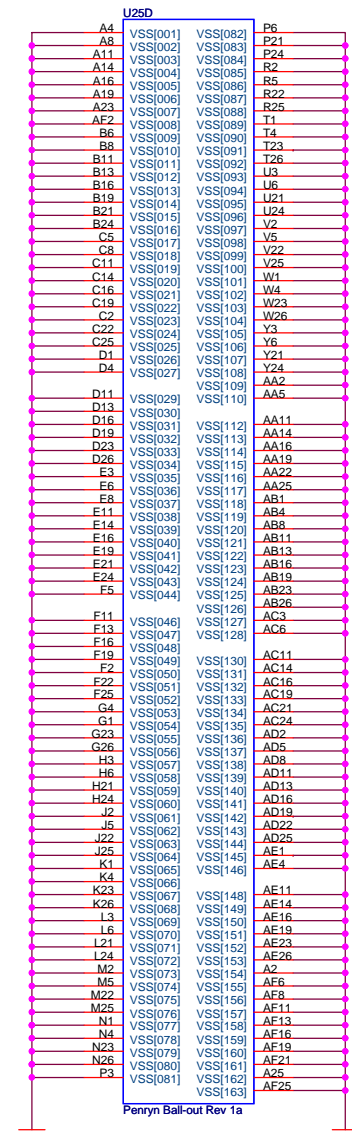
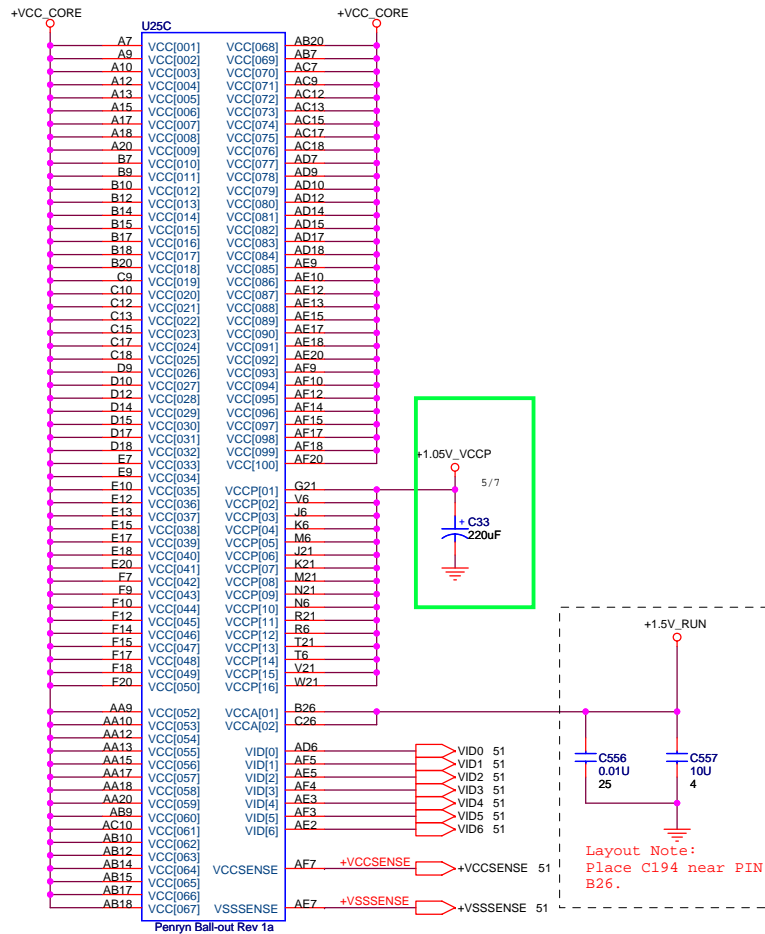
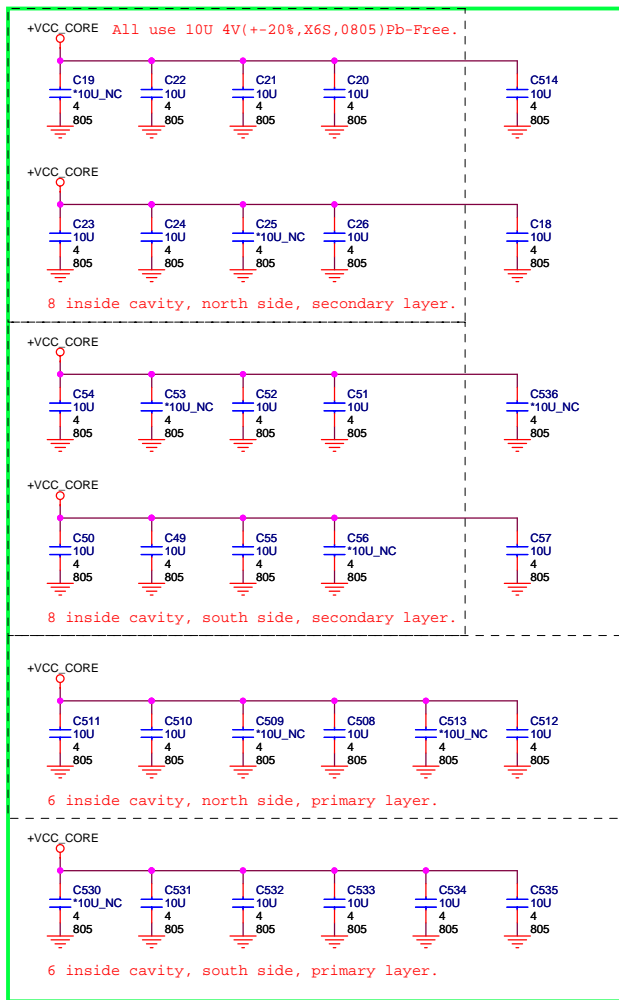


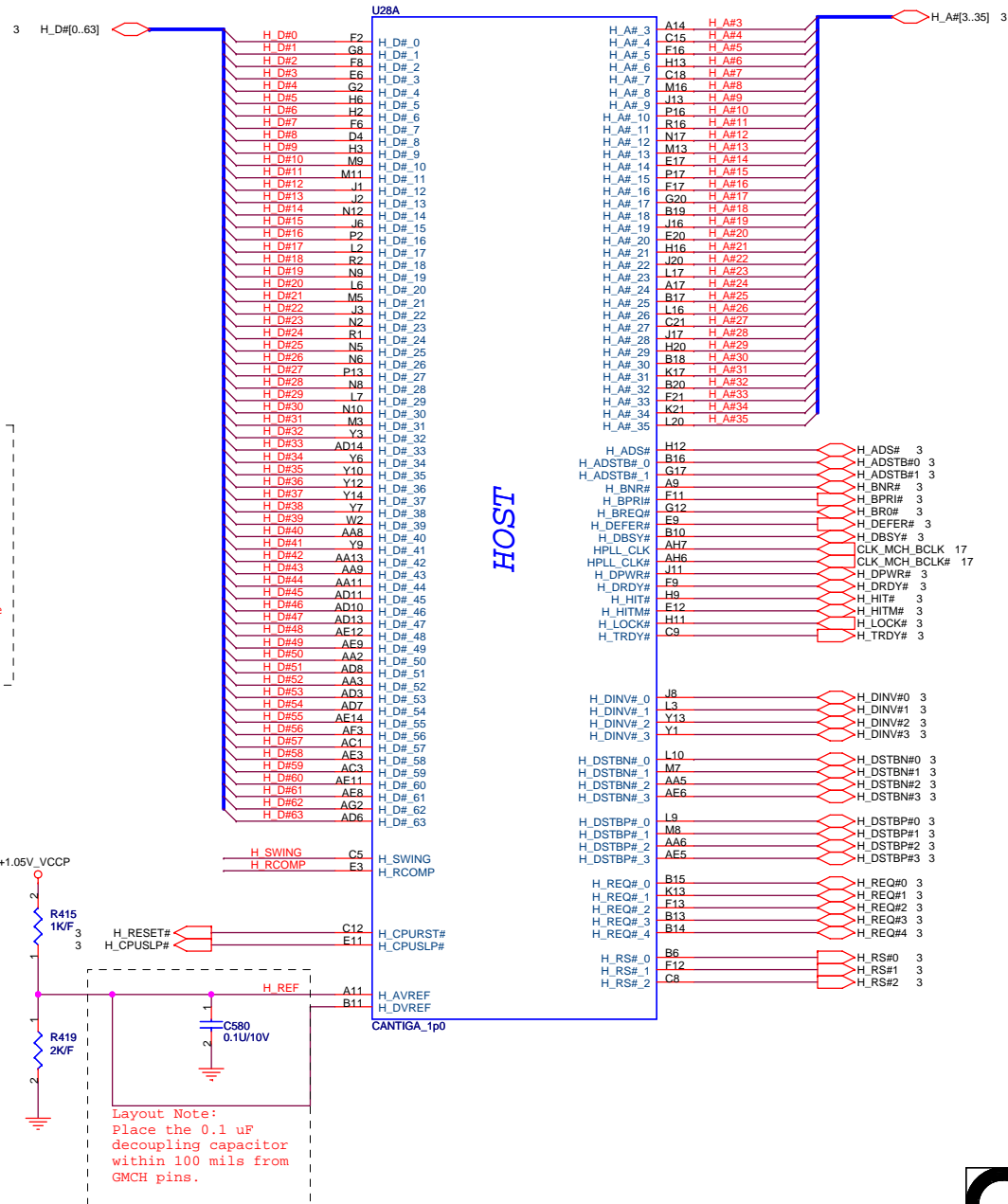
ITP disable guidelines

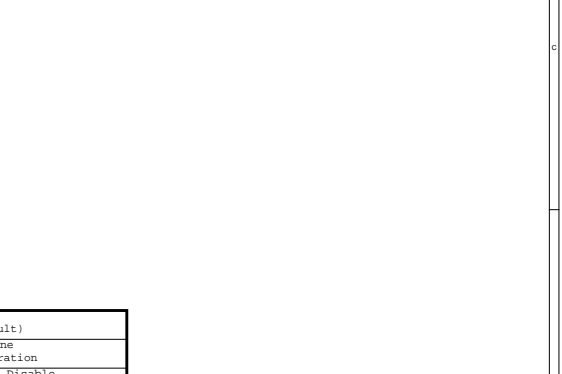
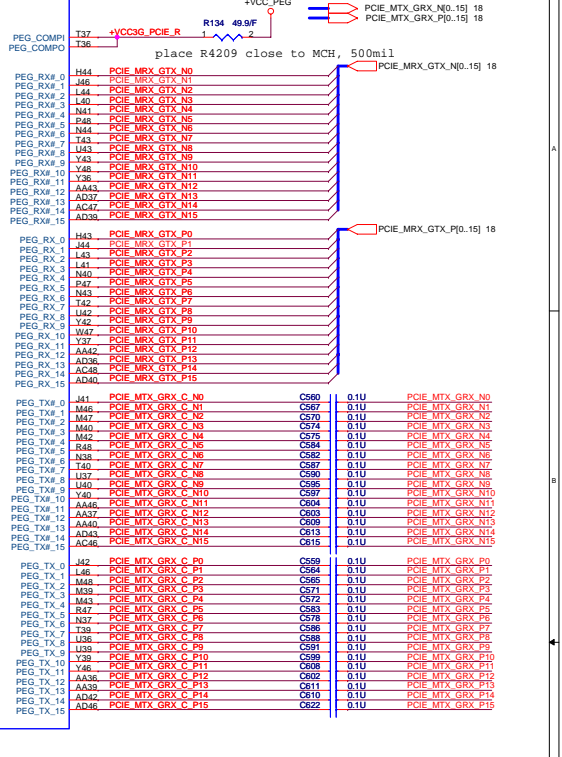
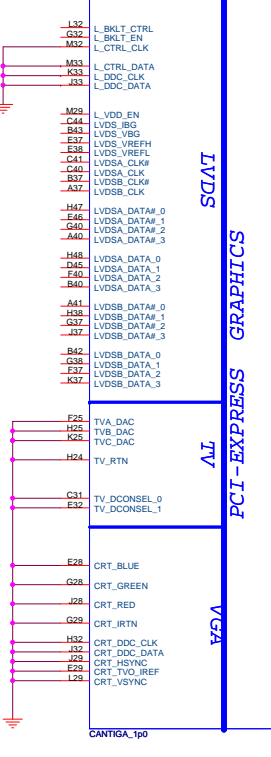
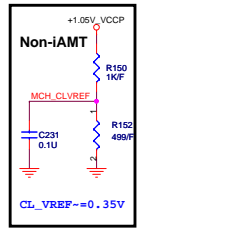
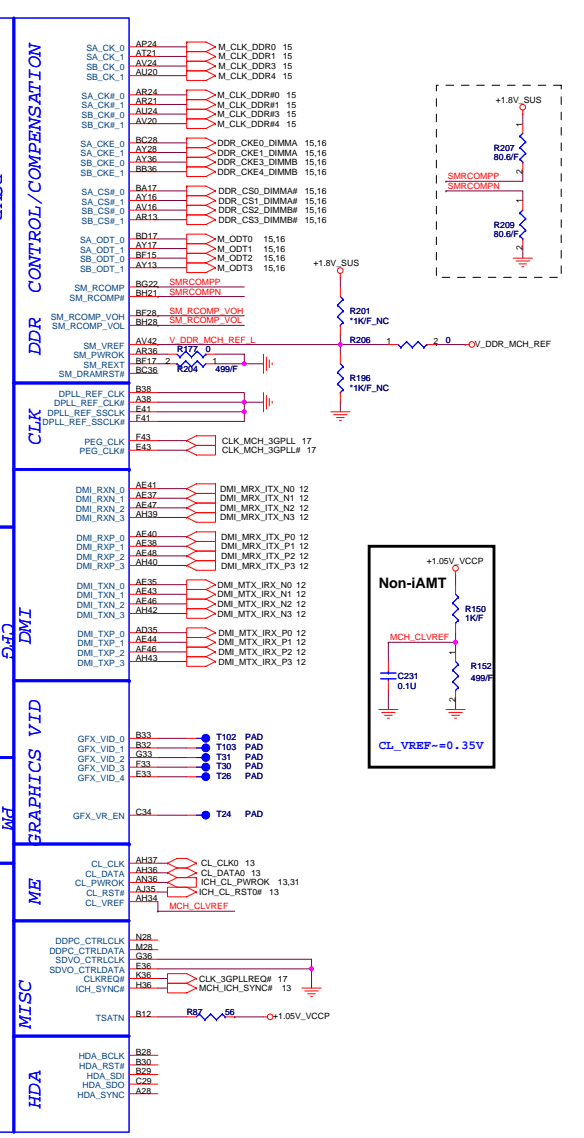
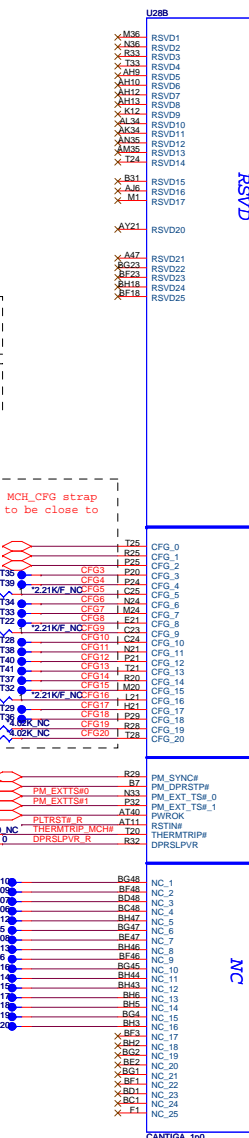
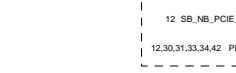
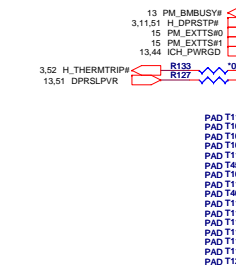
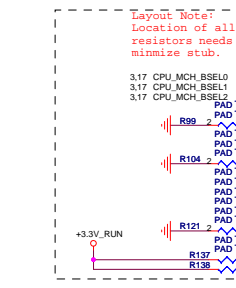
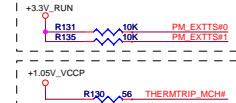
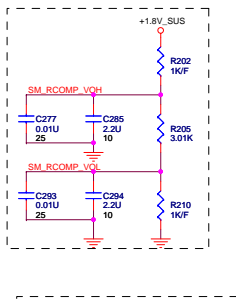
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VIT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VIT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VIT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0







CFG5	DMI X2 Select	Low=DMiX2 High=DMiX4(Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (default) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

QUANTA COMPUTER

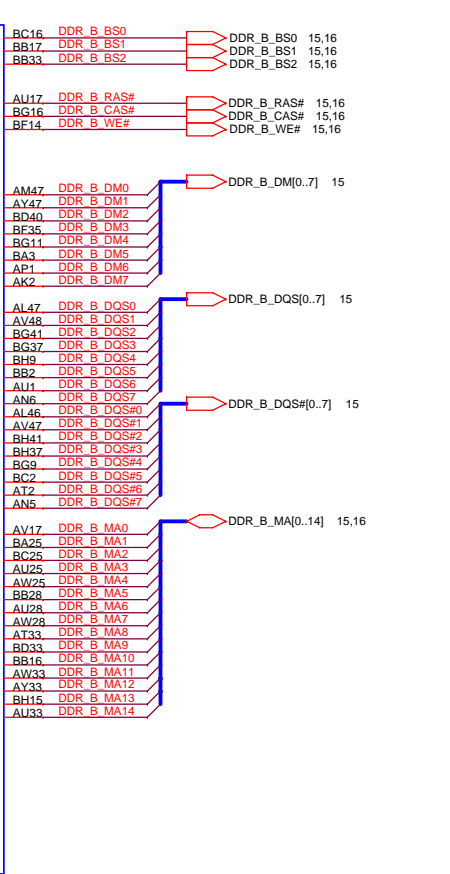
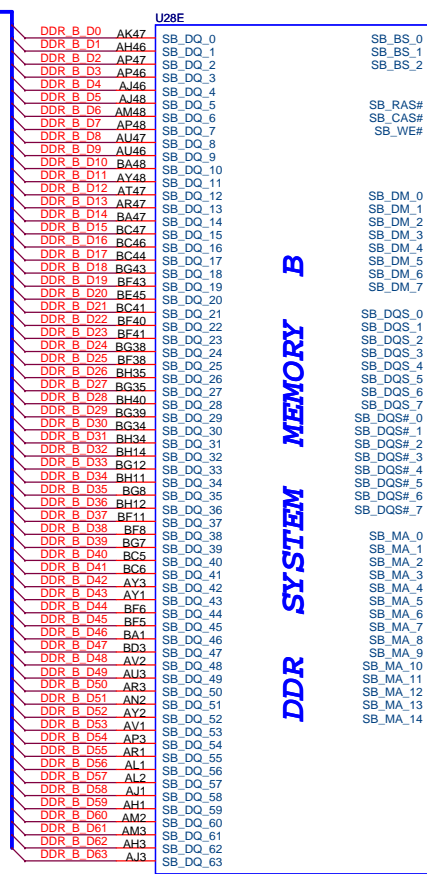
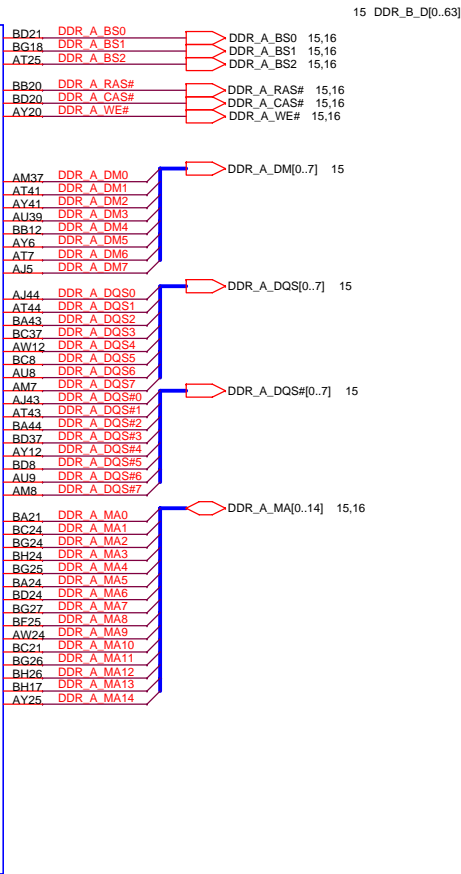
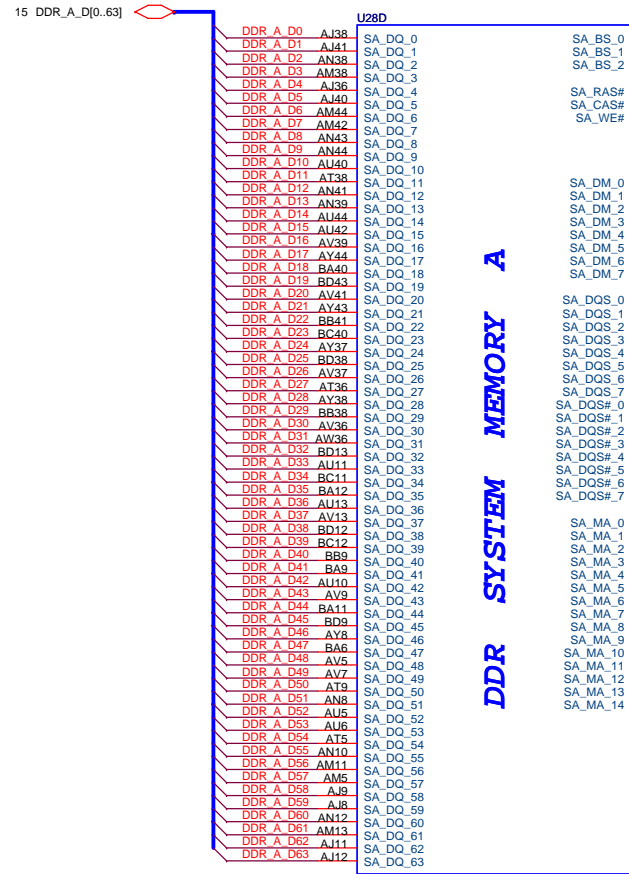
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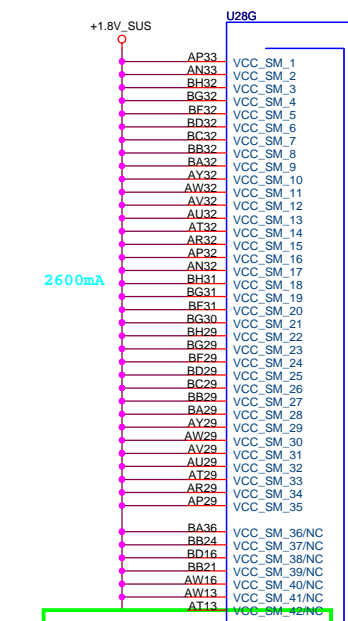
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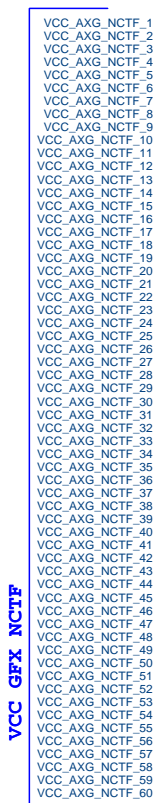
Rev: 1A



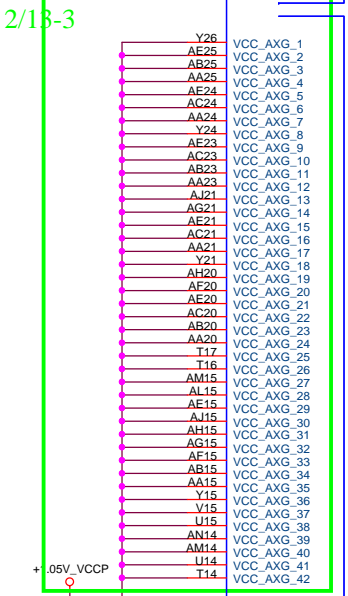


POWER

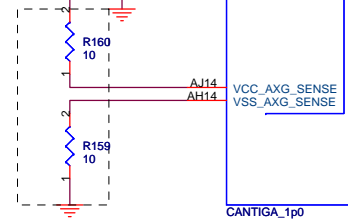
VCC SM



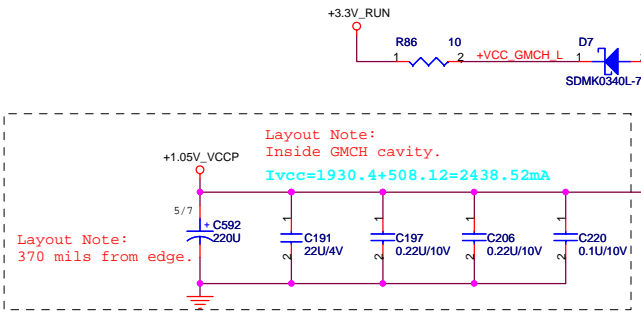
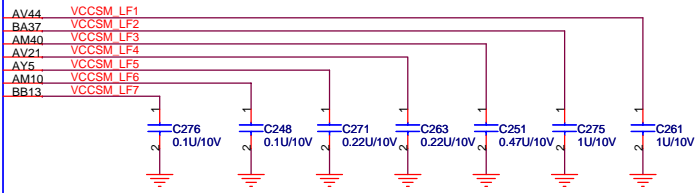
VCC GFX NCTF



VCC GFX

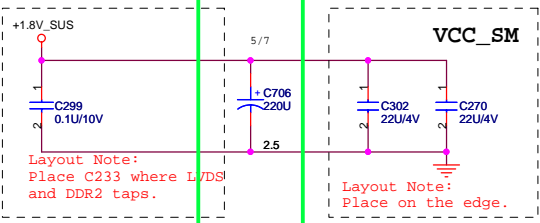


VCC SM LF



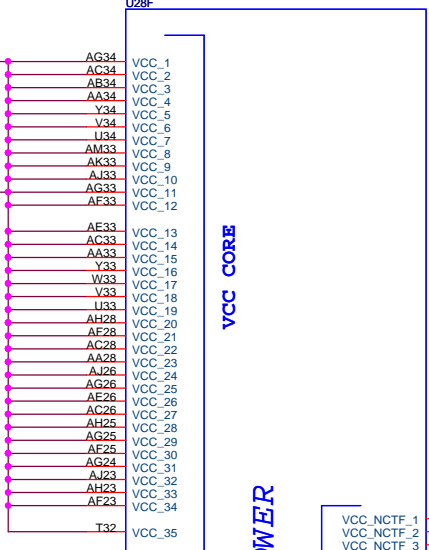
Layout Note:
370 mils from edge.

Layout Note:
Inside GMCH cavity.
 $I_{vcc}=1930.4+508.12=2438.52mA$



Layout Note:
Place C233 where L/D/S and DDR2 taps.

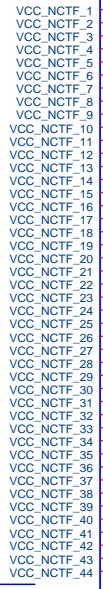
Layout Note:
Place on the edge.



VCC CORE

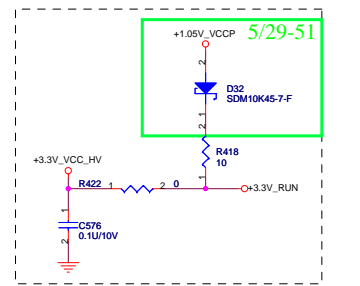
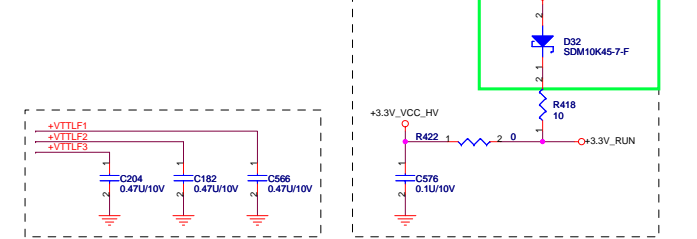
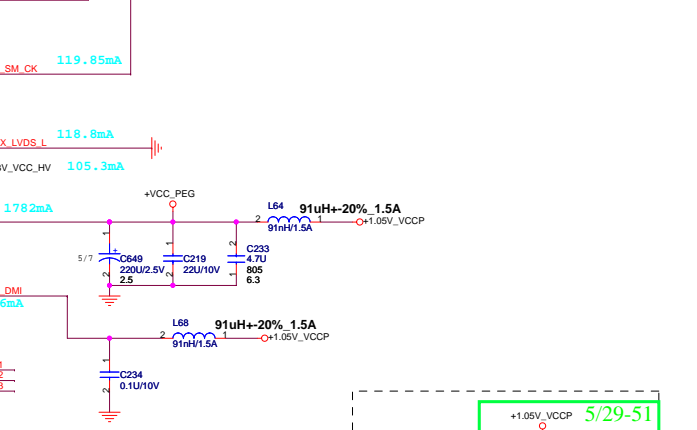
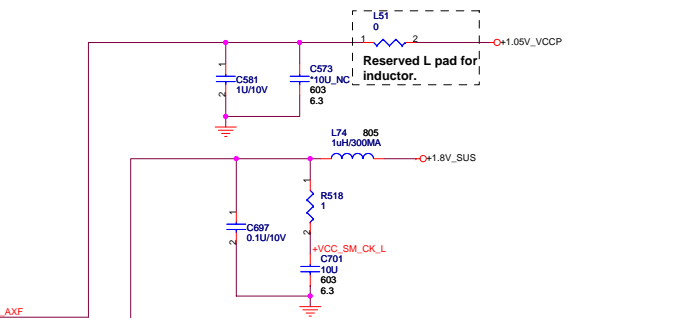
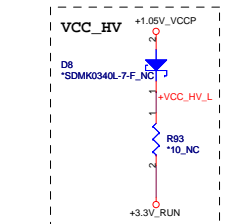
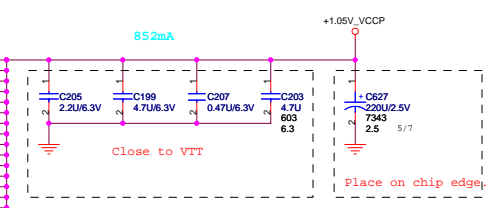
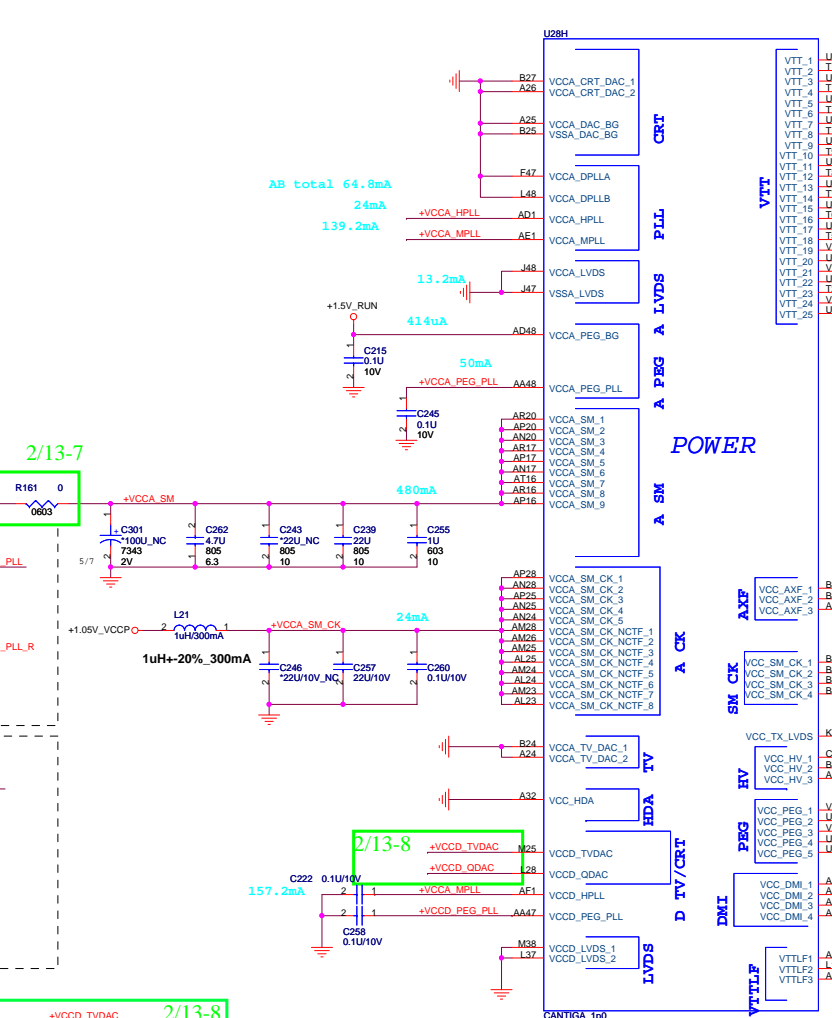
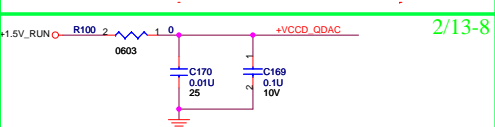
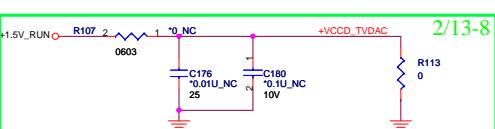
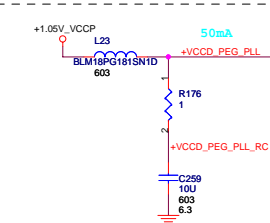
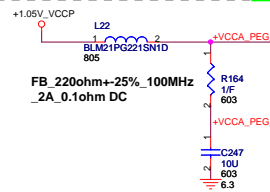
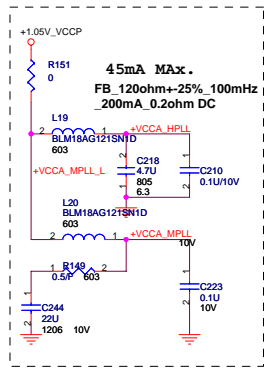
POWER

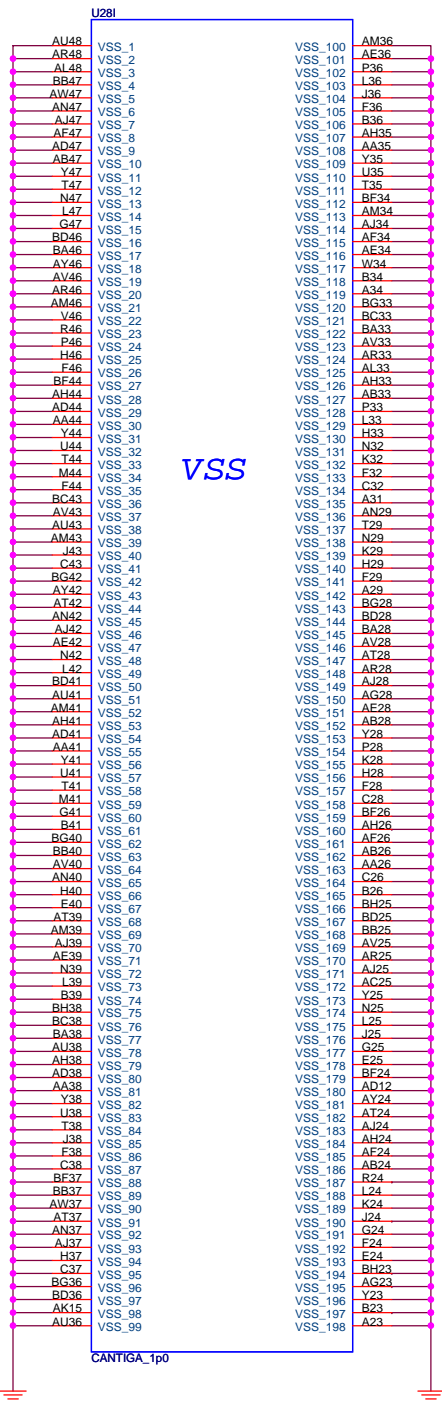
VCC NCTF



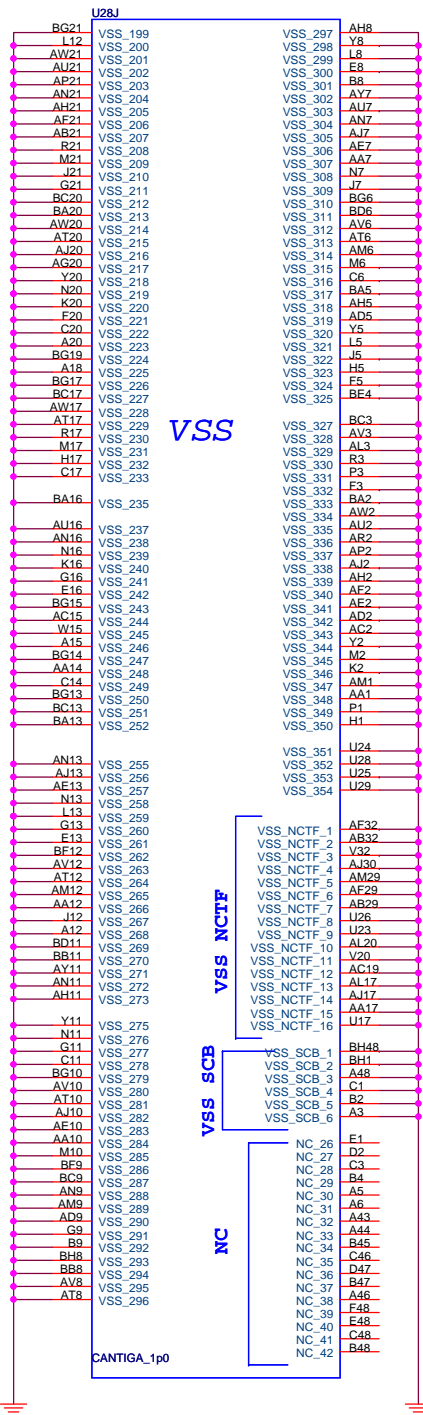
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UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.





VSS



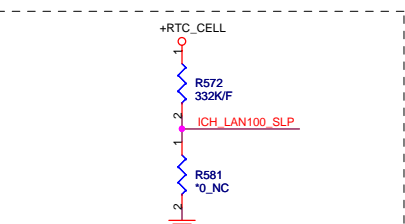
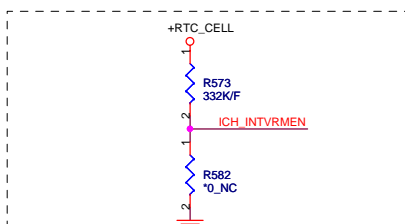
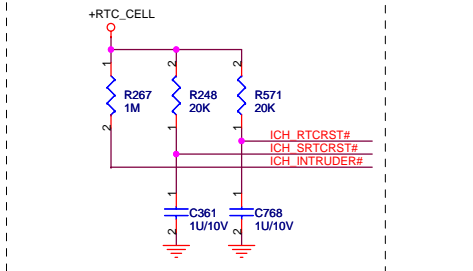
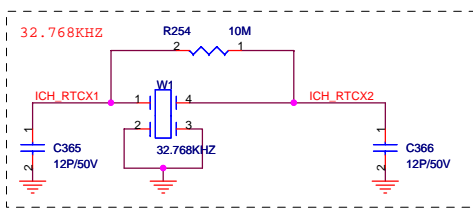
VSS

VSS NCTF

VSS SCB

NC



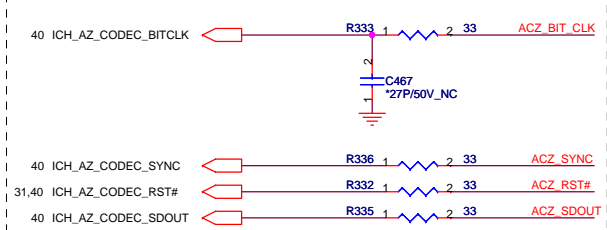


ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

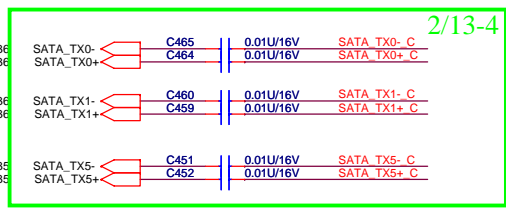
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
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ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

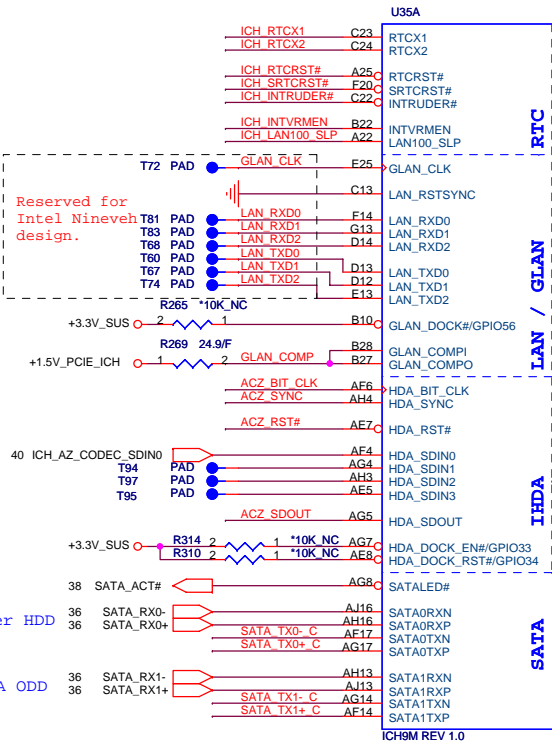
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)
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Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respectively. Basically, keep the same distance from T for all series termination resistors.

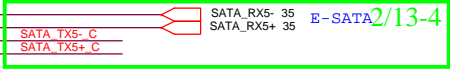
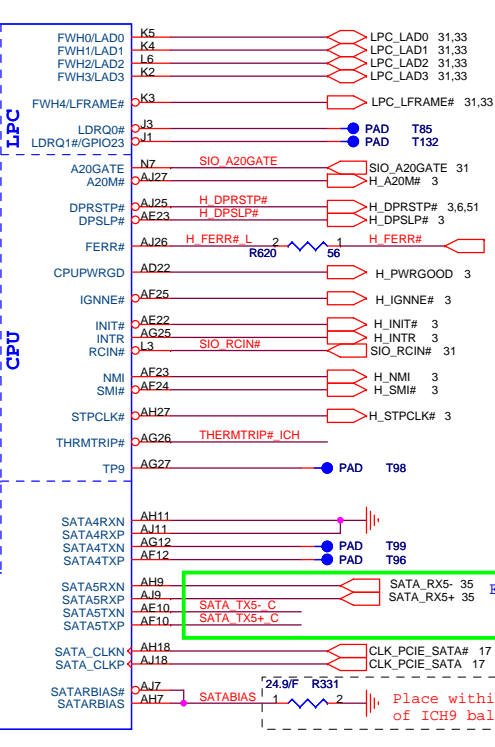


Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

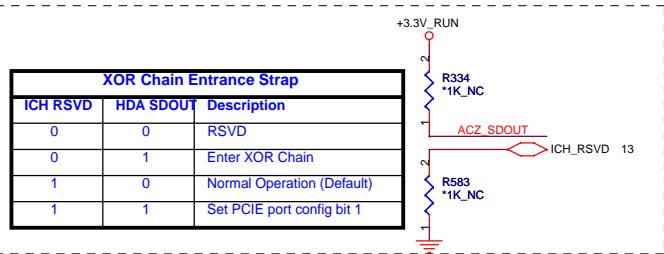
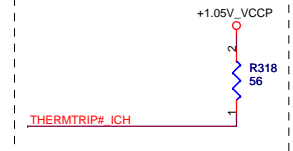
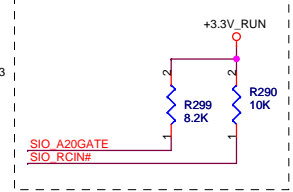
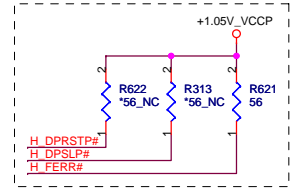


Reserved for Intel Nineveh design.

Master HDD
SATA ODD



Place within 500mils of ICH9 ball



Place TX DC blocking caps close ICH8.

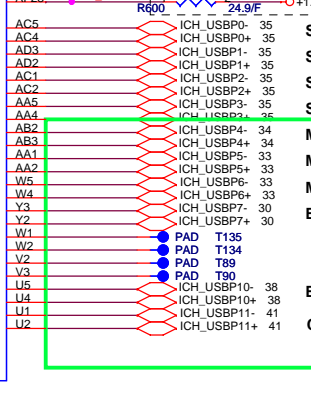
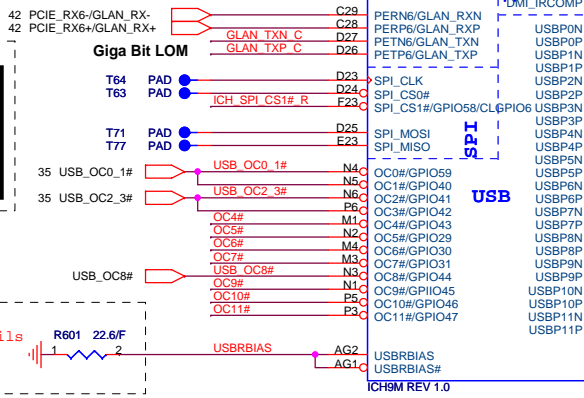
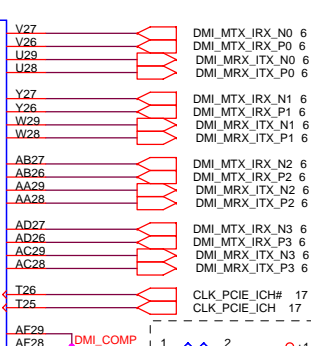
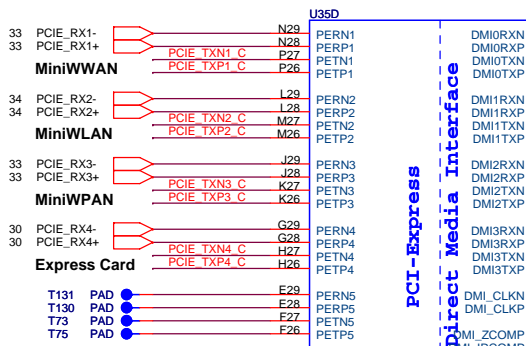
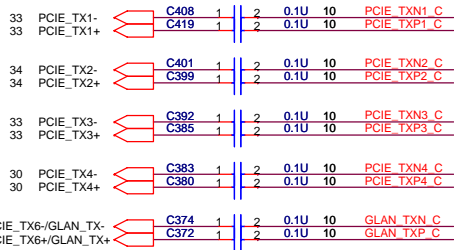
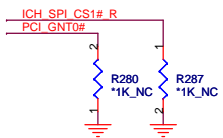
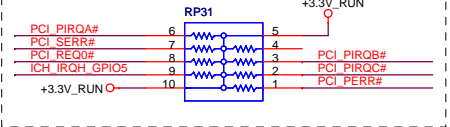
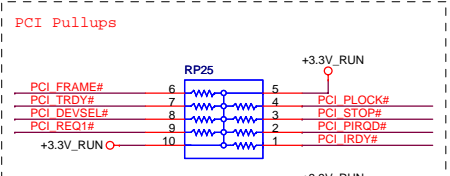
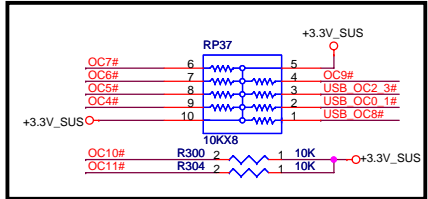
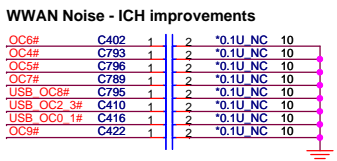


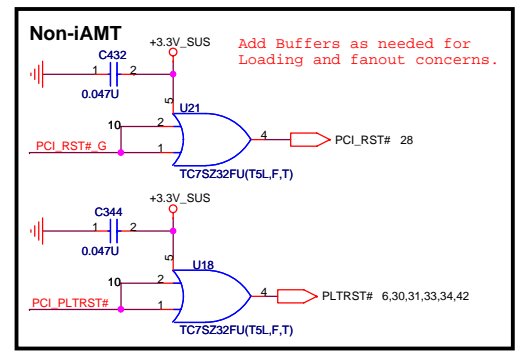
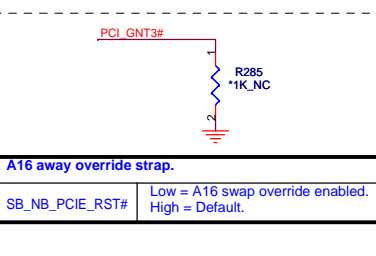
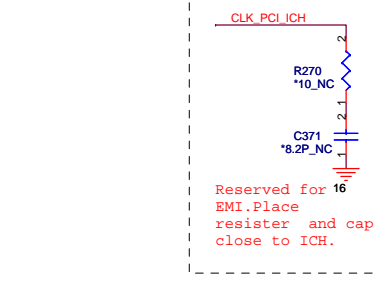
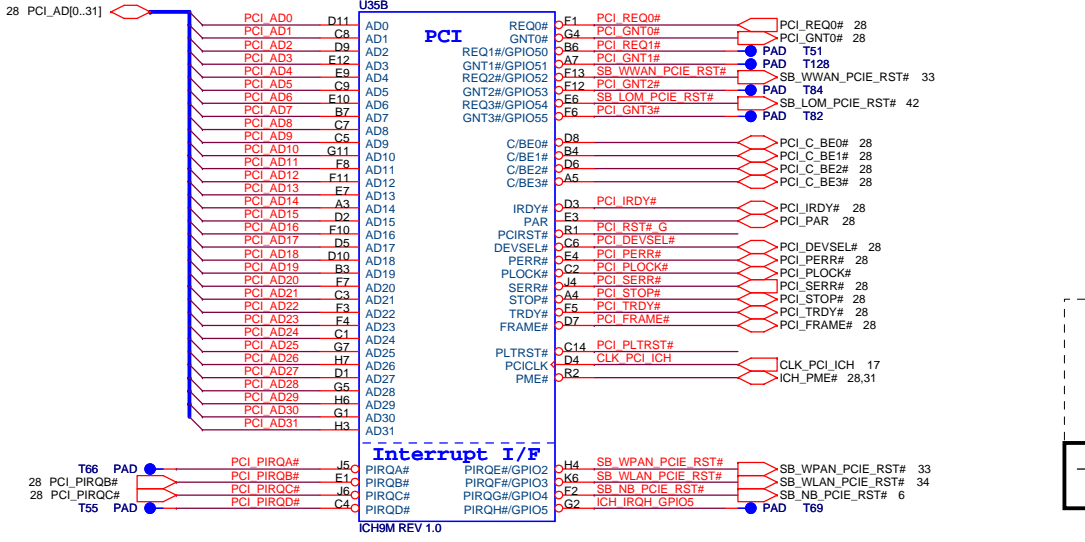
Table for Boot BIOS Strap with columns for LPC, PCI, SPI and rows for GNT0#, SPI_CS1#.



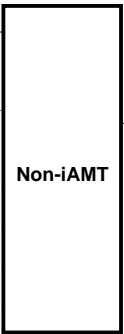
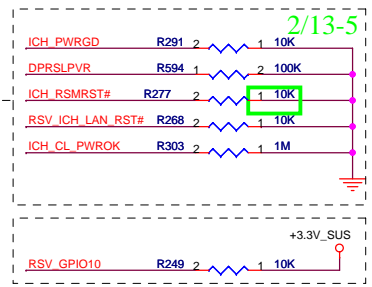
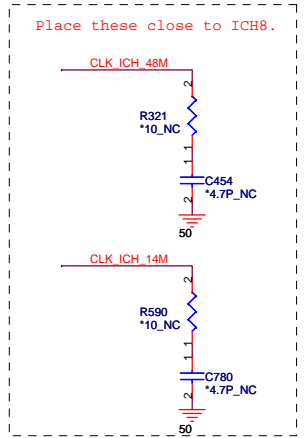
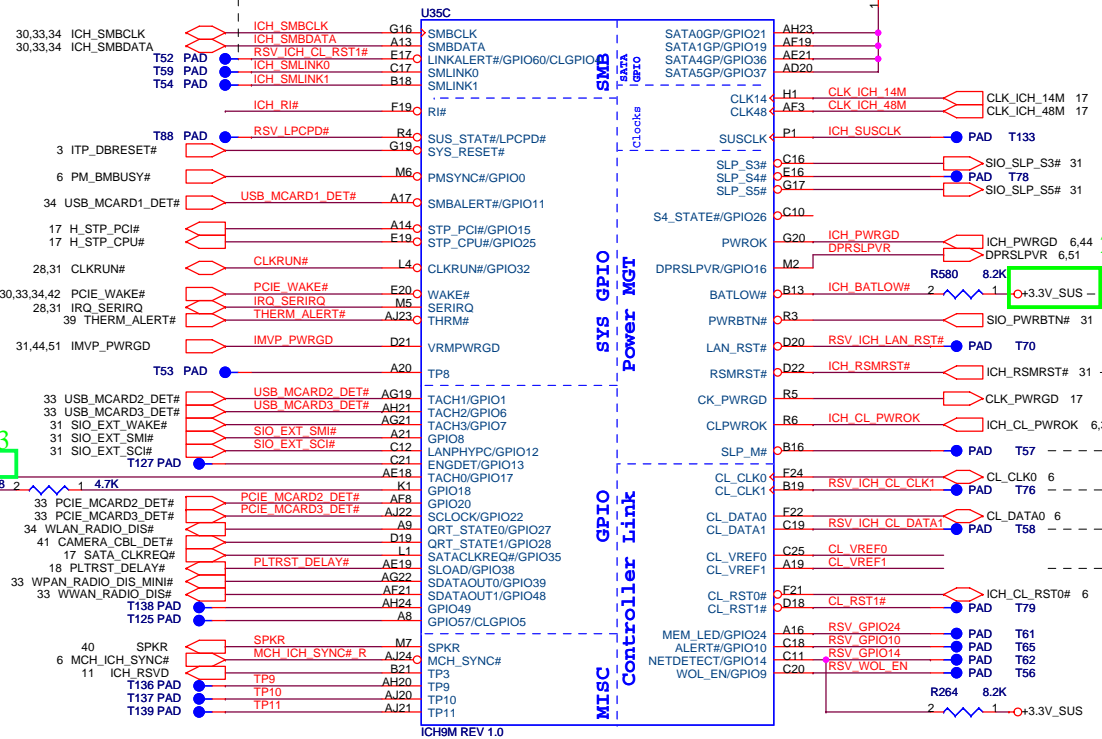
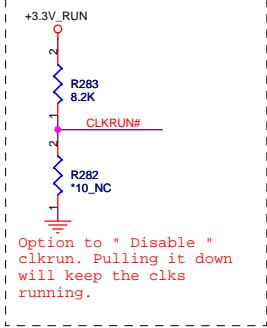
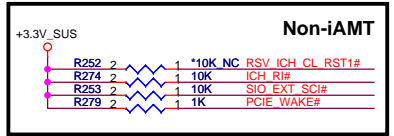
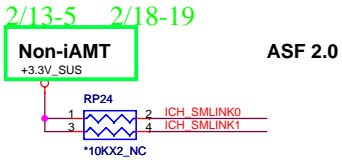
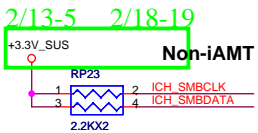
Places within 500 mils of the ICH9



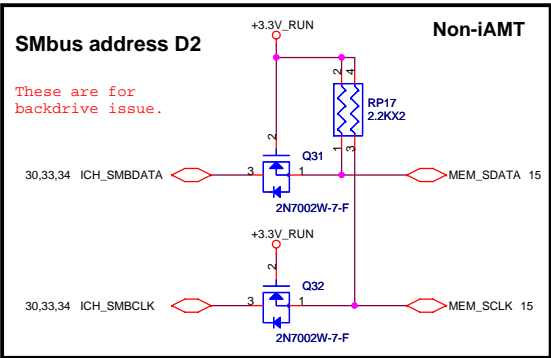
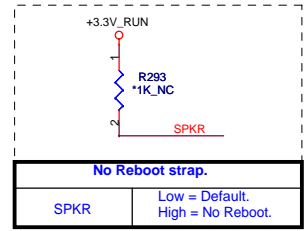
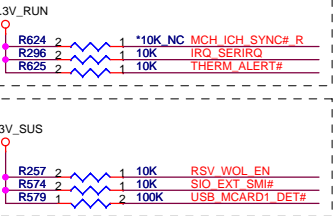
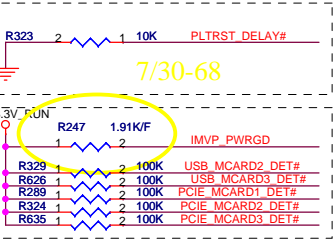
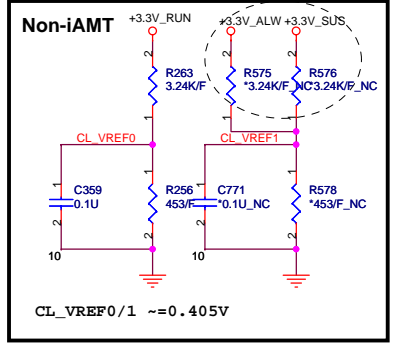
BIOS should not enable the internal GPIO pull up resistor.

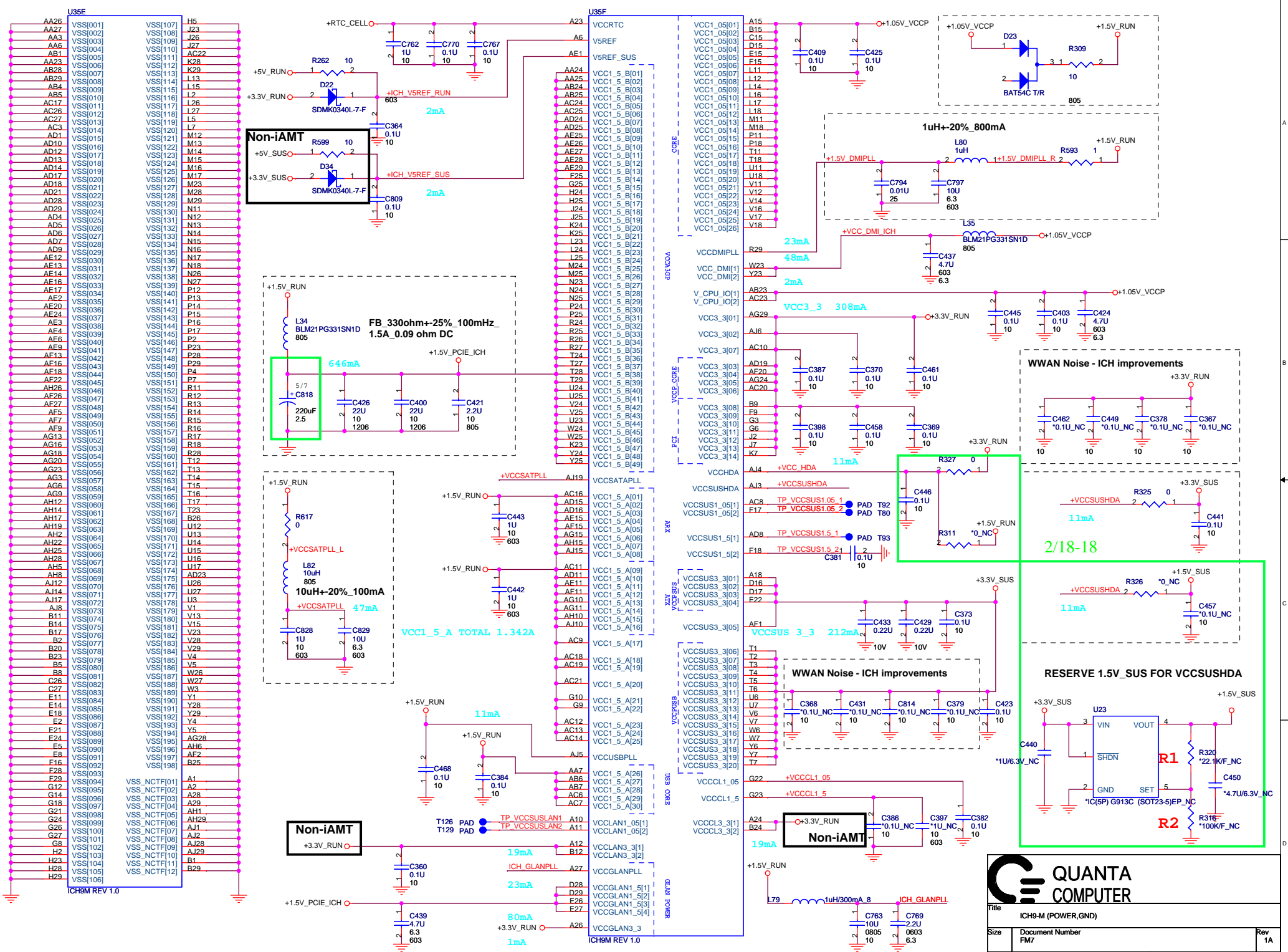


QUANTA COMPUTER logo and document information including Title, Size, Document Number, Date, Sheet, and Rev.



DIS:ALW
UMA:SUS (19)



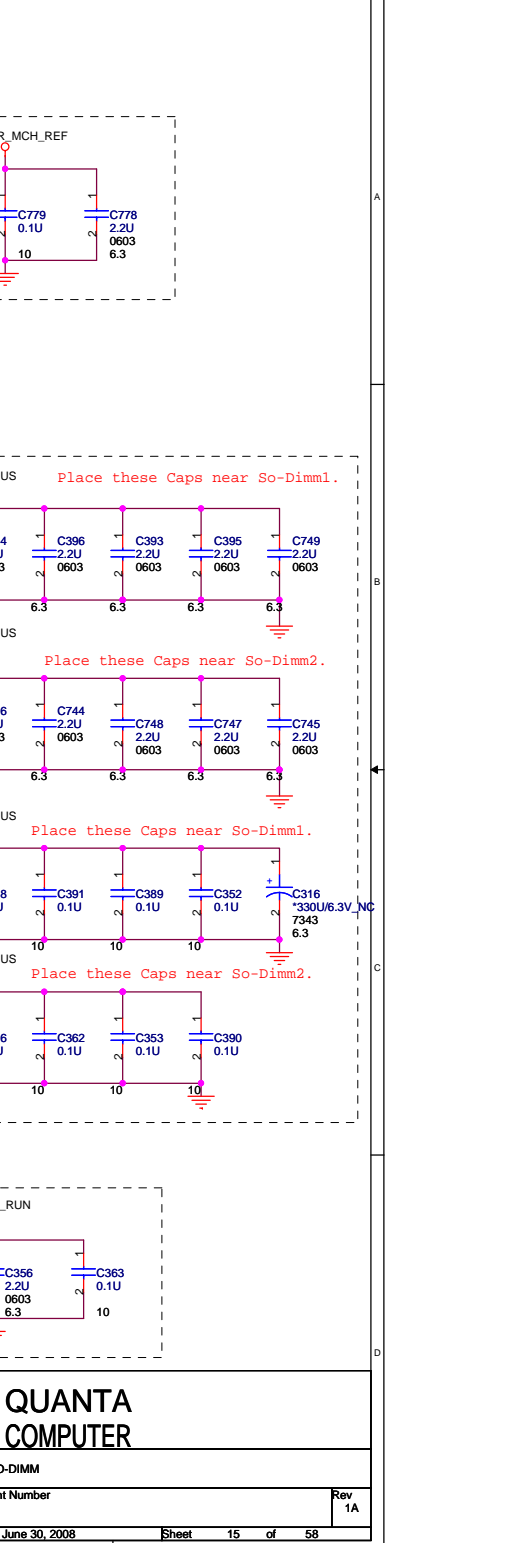
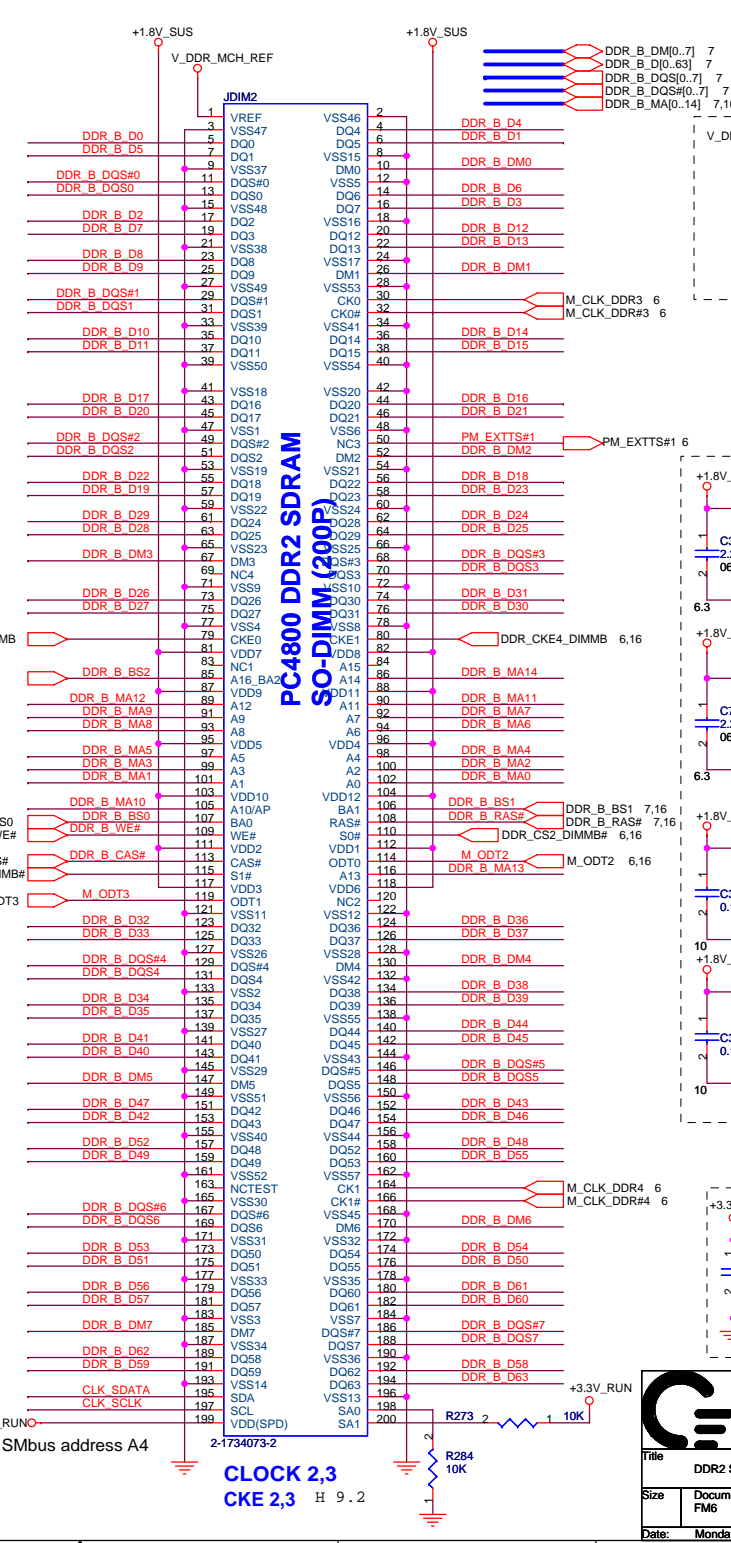
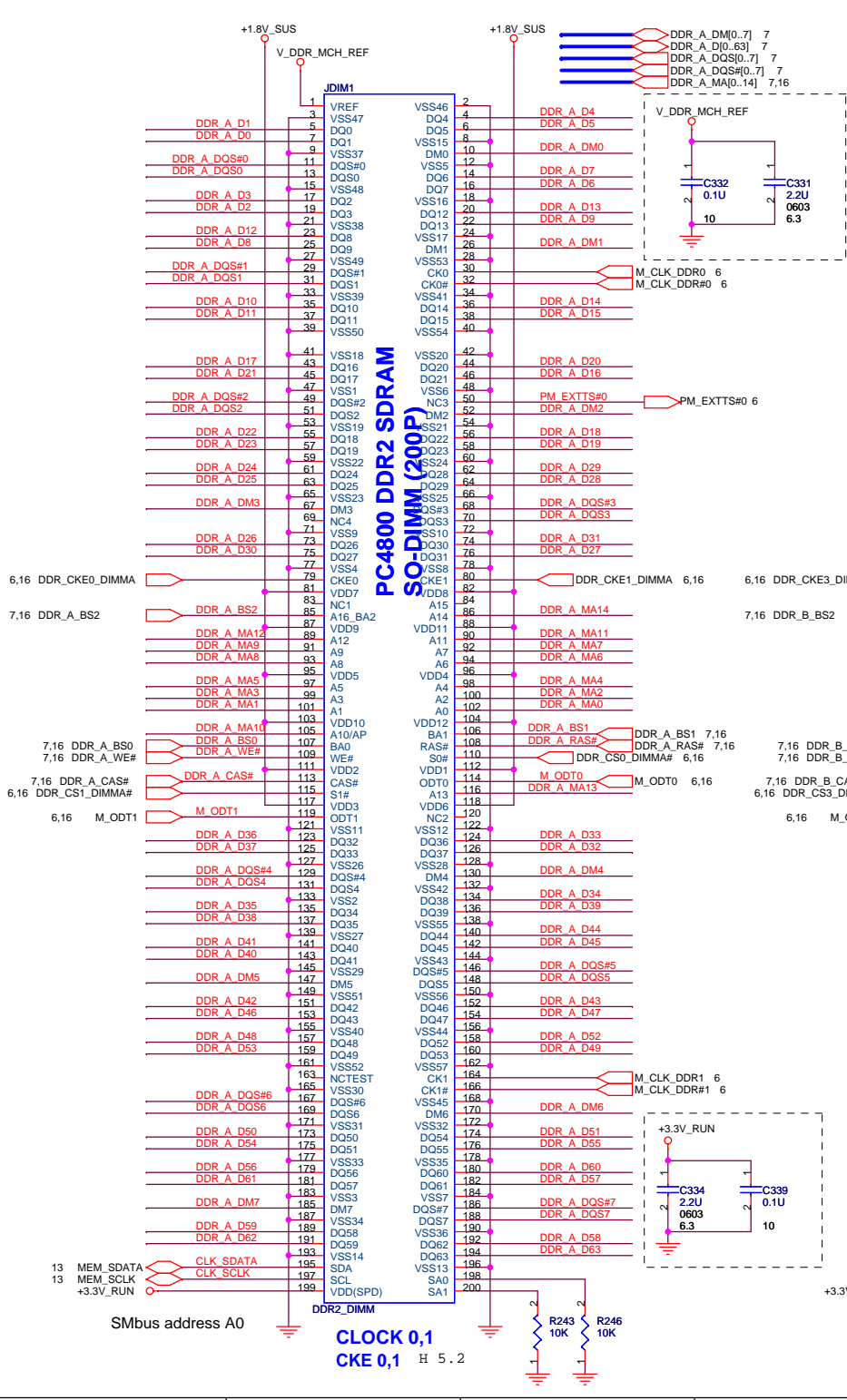


QUANTA COMPUTER

Title: ICH9-M (POWER, GND)

Size	Document Number	Rev
	FM7	1A

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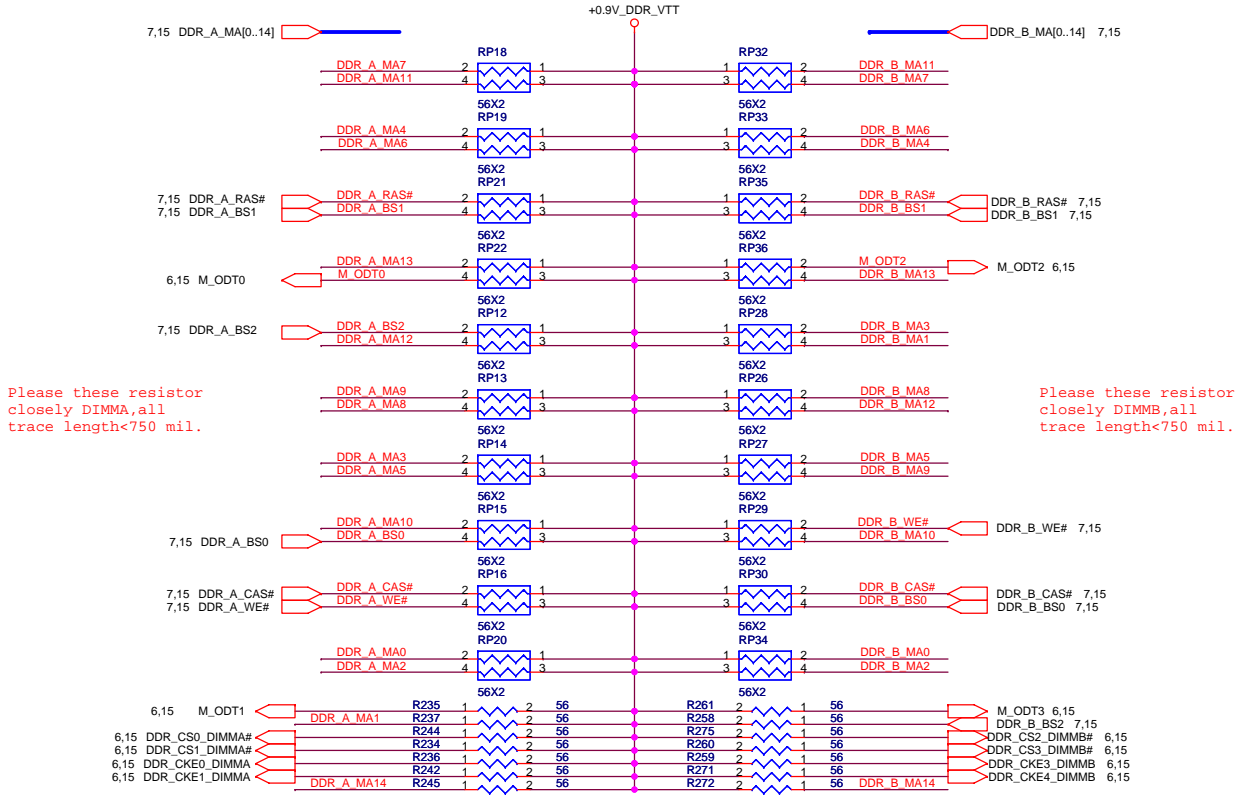
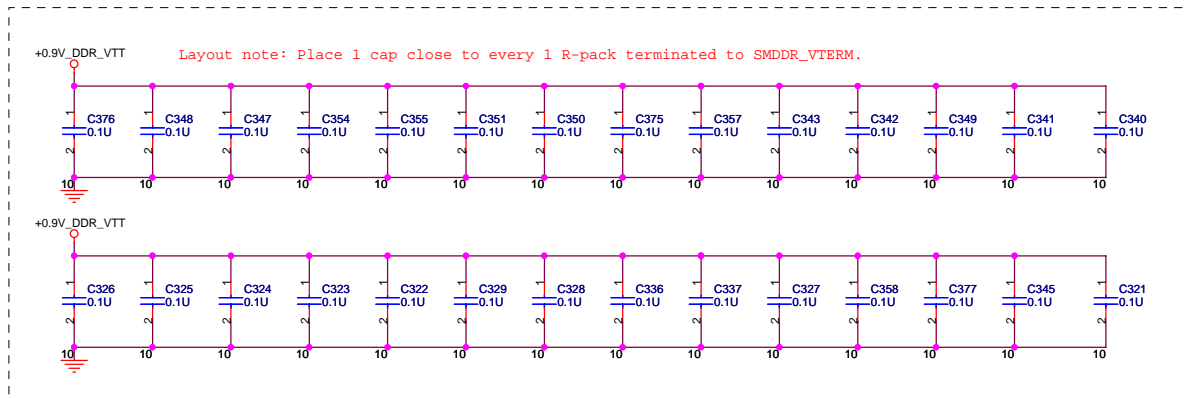


QUANTA COMPUTER

Title: DDR2 SO-DIMM

Size: FM6	Document Number: 1A	Rev: 1A
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Date: Monday, June 30, 2008 Sheet 15 of 58



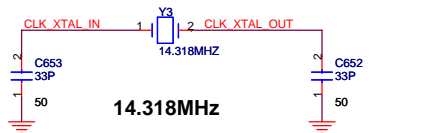
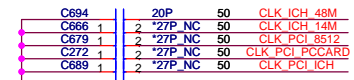
**QUANTA
COMPUTER**

Title: DDR2 RES. ARRAY

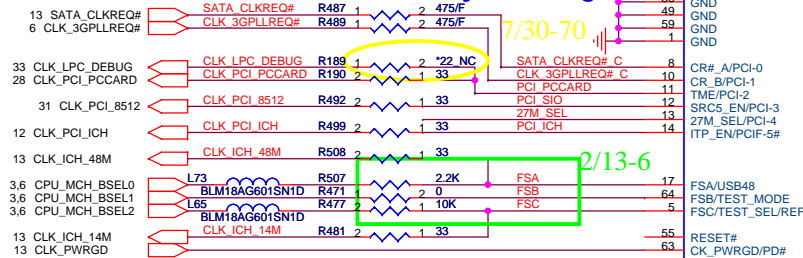
Size: Document Number FM6 Rev 1A

Date: Monday, June 30, 2008 Sheet 16 of 58

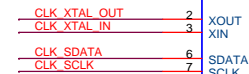
Add capacitor pads for improving WWAN.



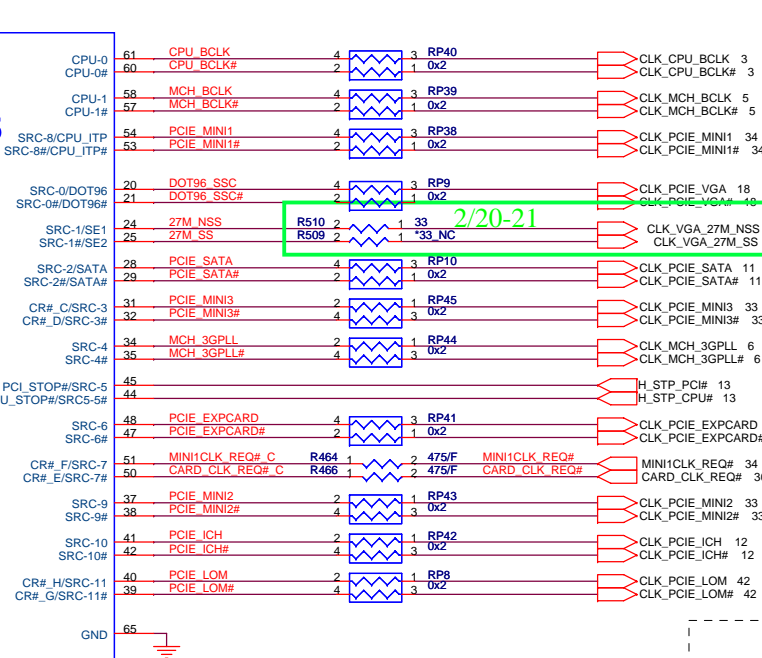
Only for debug



2/13-6

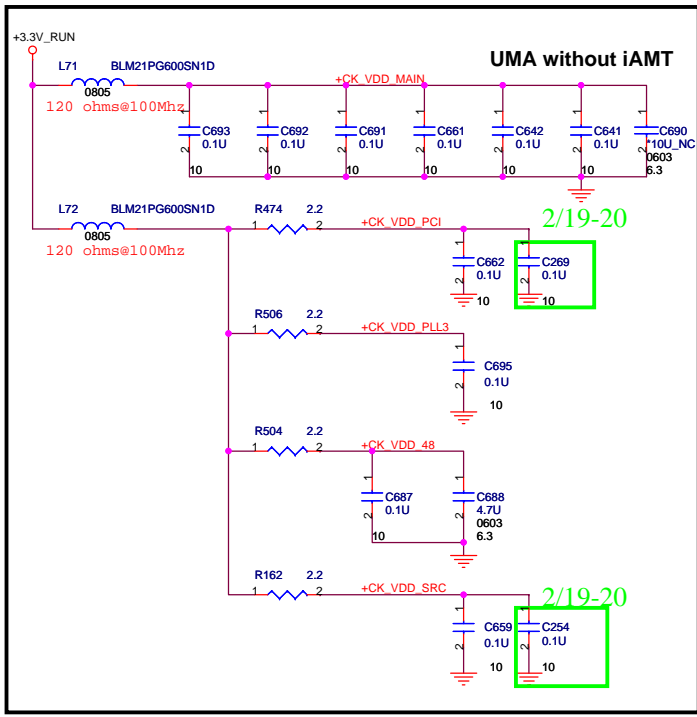
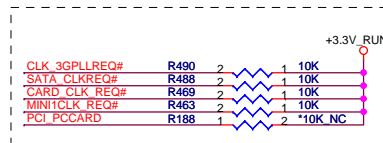


CK505 QFN64



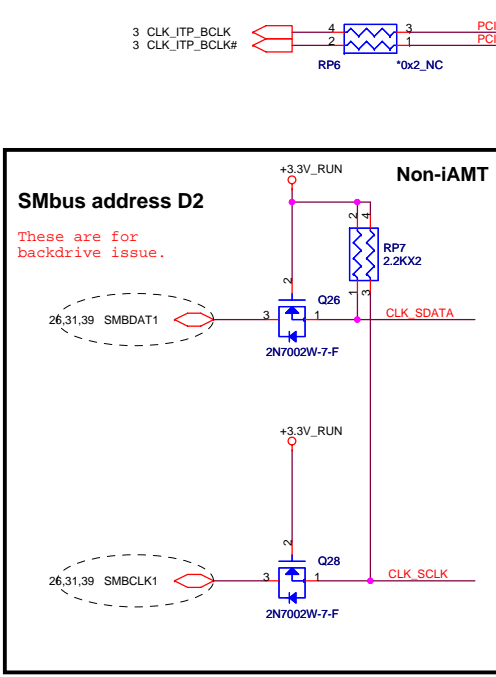
2/21-24

2/20-21



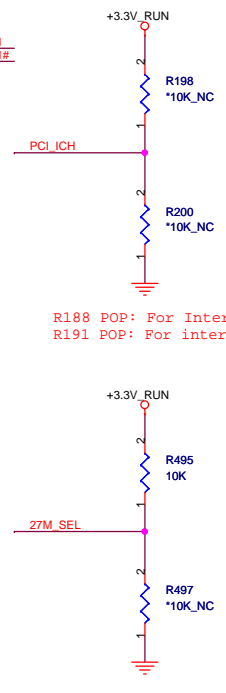
2/19-20

2/19-20



Smbus address D2

These are for backdrive issue.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

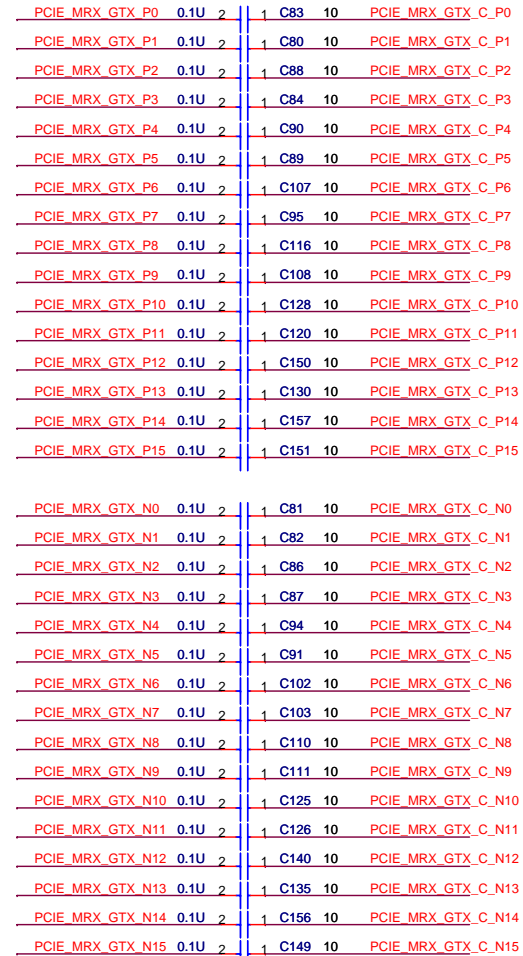
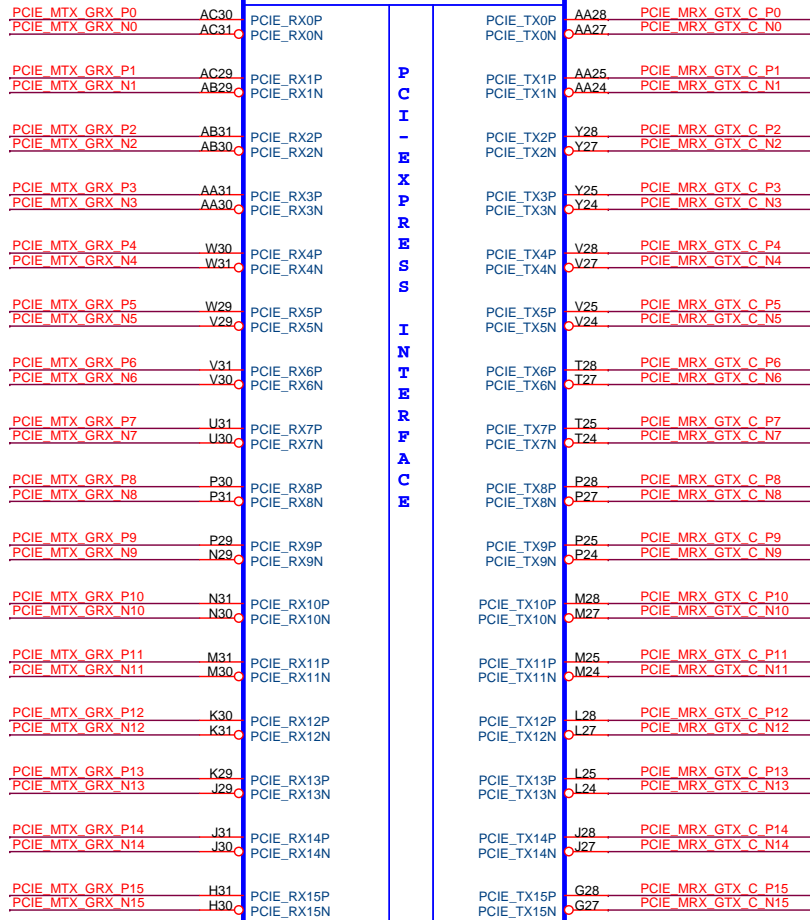
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



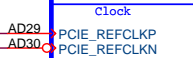
6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]

6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]

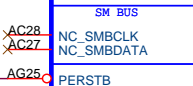
U27A
PART 1 OF 6



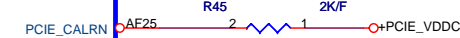
17 CLK_PCIE_VGA
17 CLK_PCIE_VGA#



13 PLTRST_DELAY#



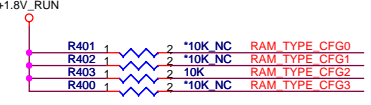
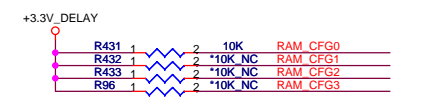
Calibration



Title			VGA-M82-S (PCIe)
Size	Document Number	Rev	
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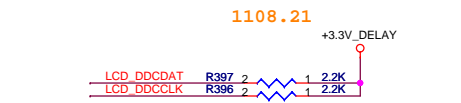
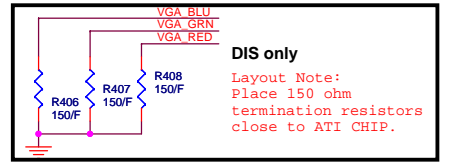
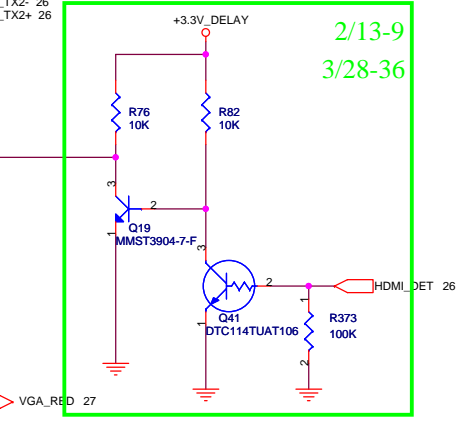
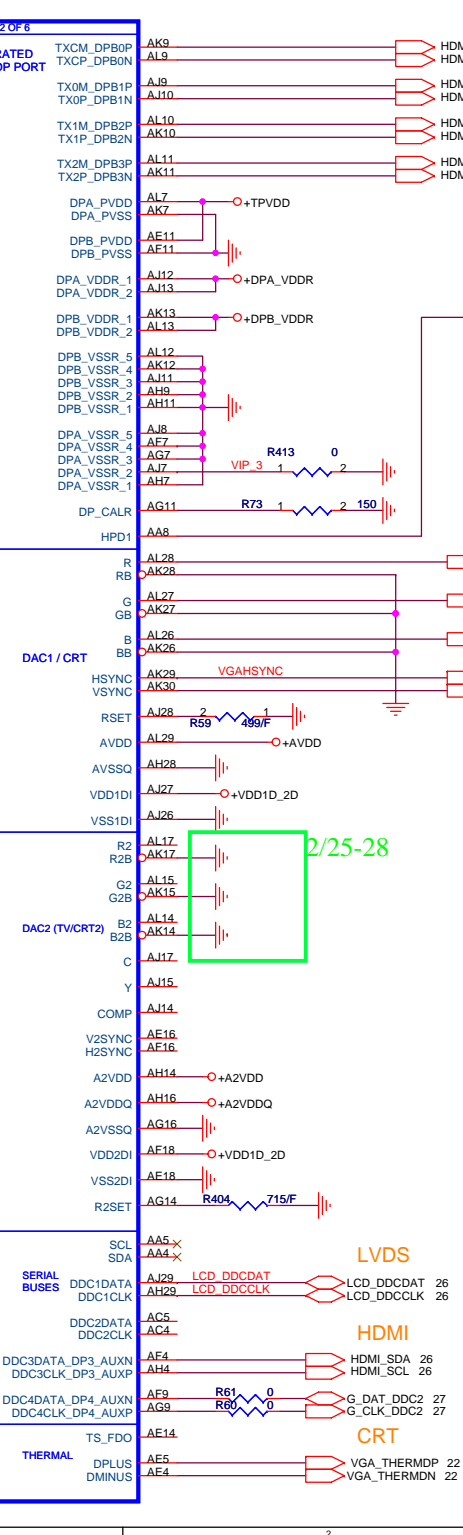
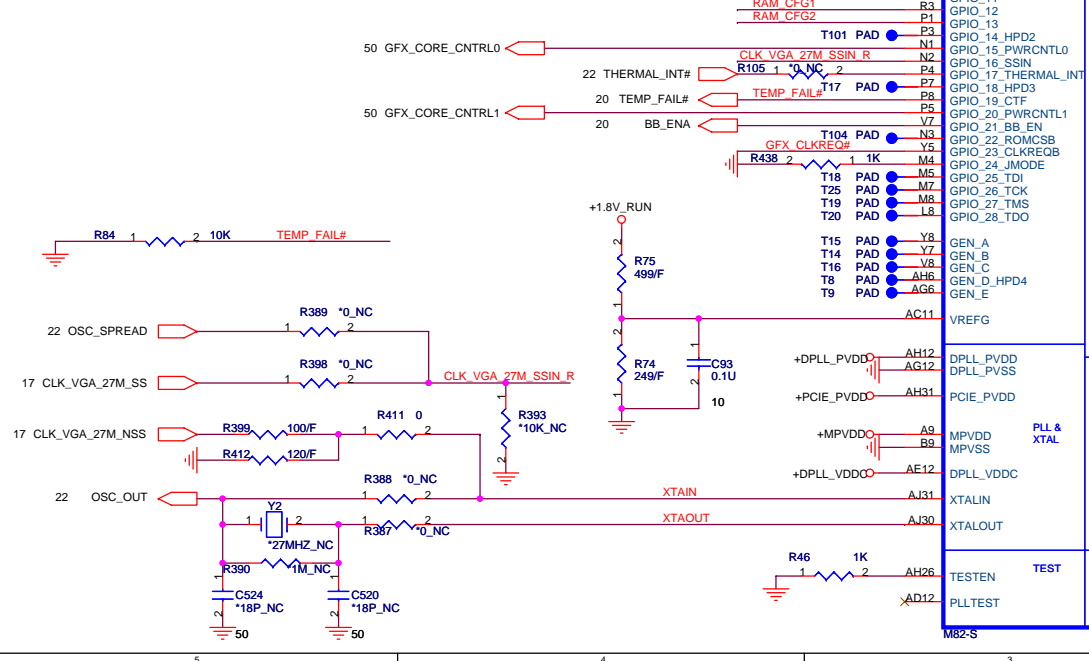
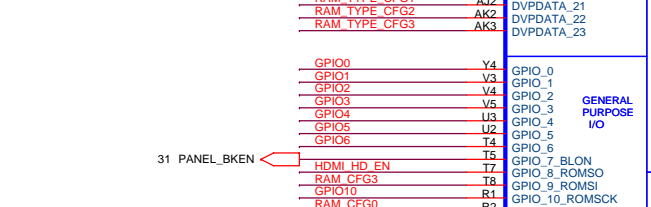
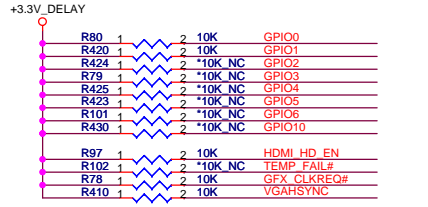
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

Memory Straps	RAM_TYPE CFG3	RAM_TYPE CFG2	RAM_TYPE CFG1	RAM_TYPE CFG0
400MHz 256MB(32M*16) Samsung	0	0	1	0
400MHz 256MB(32M*16) Hynix	0	0	1	1
500MHz 256MB(32M*16) Samsung	0	1	1	0
500MHz 256MB(32M*16) Qimonda	0	1	0	0



GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIe FULL TX OUTPUT SWING	X	1
GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.	0	0

ATI Usage recommended settings: 0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)

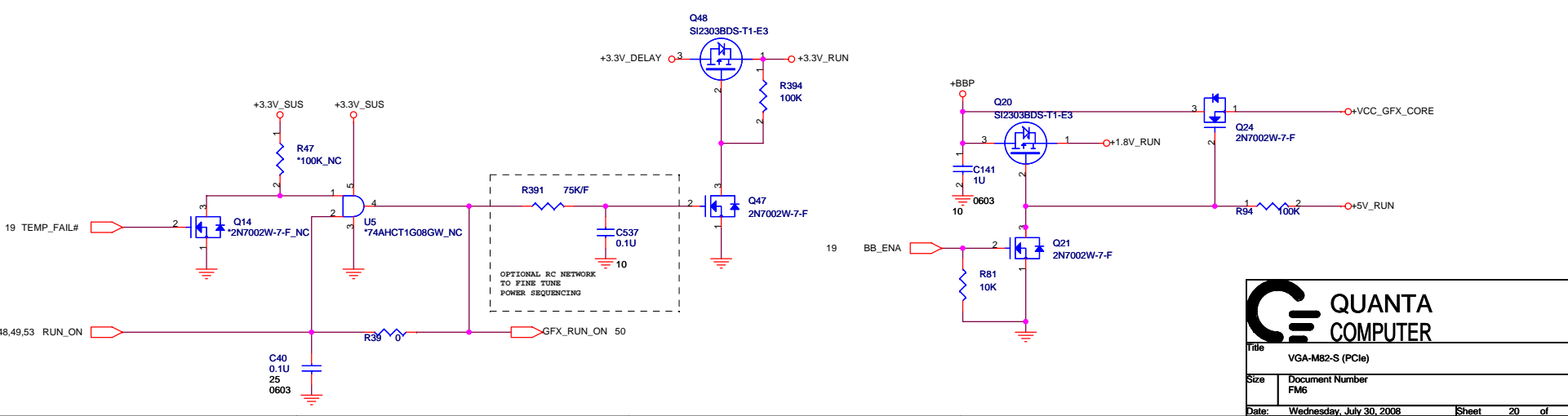
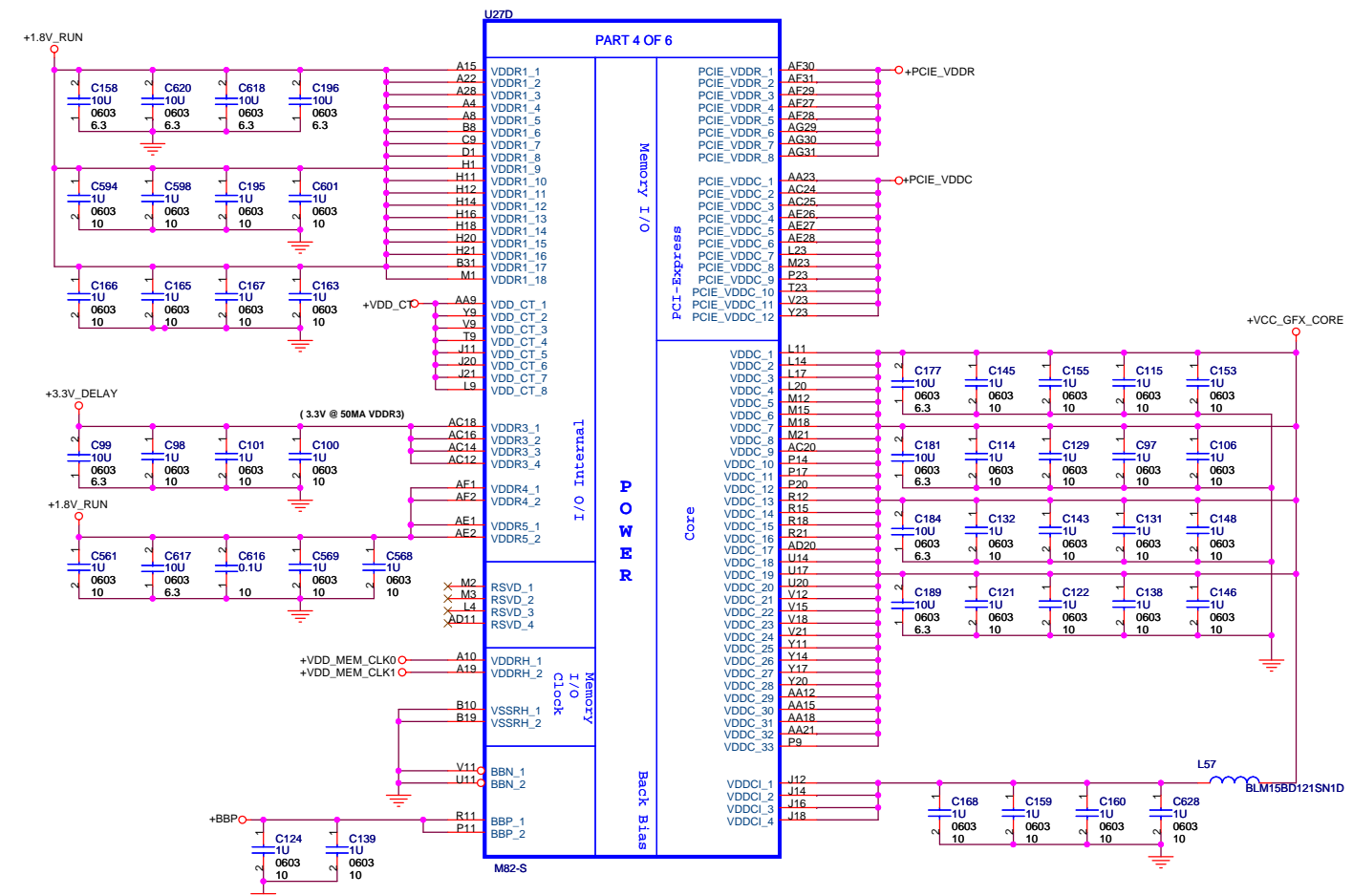
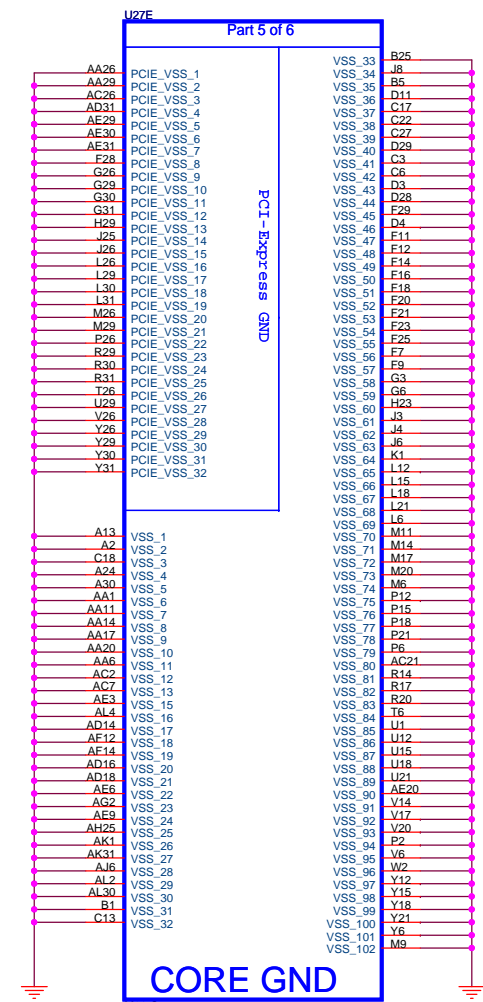


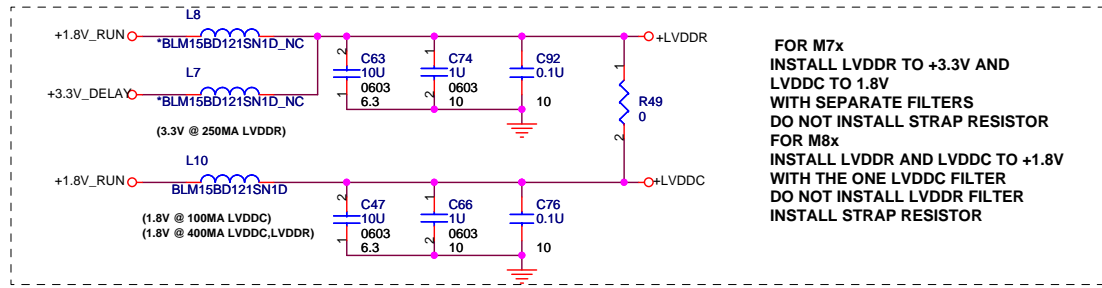
QUANTA COMPUTER

Title: VGA-G86GLM (VIDEO)

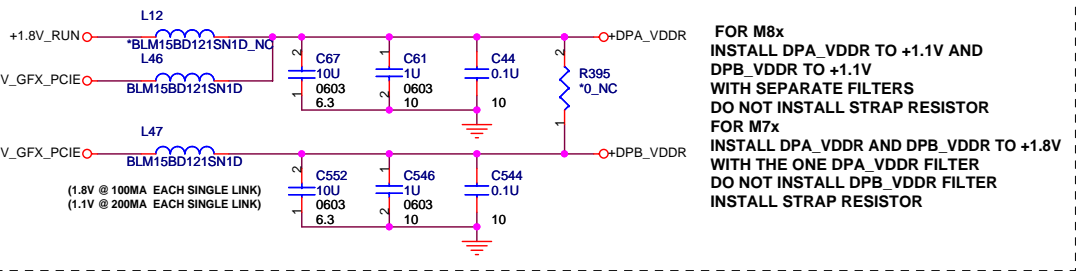
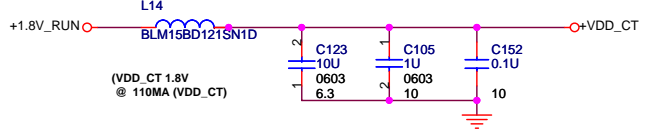
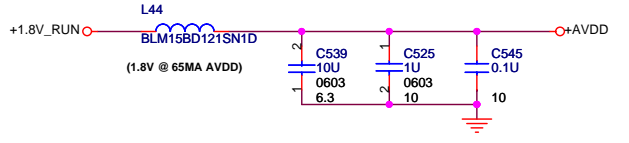
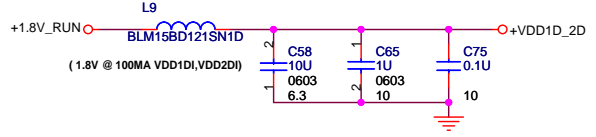
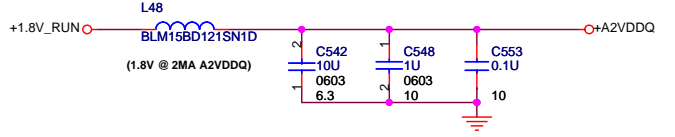
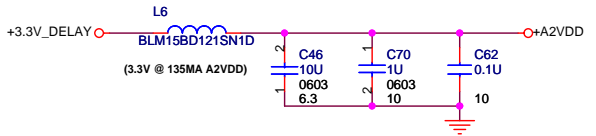
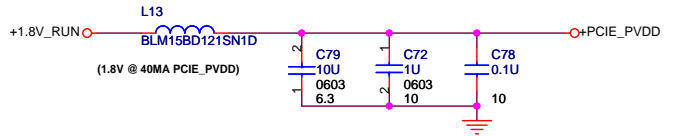
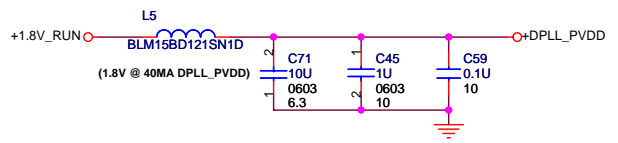
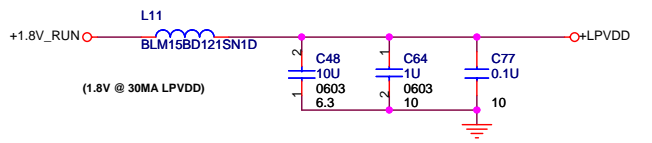
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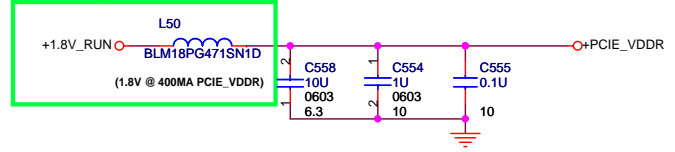
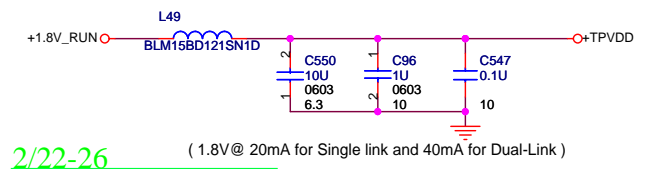
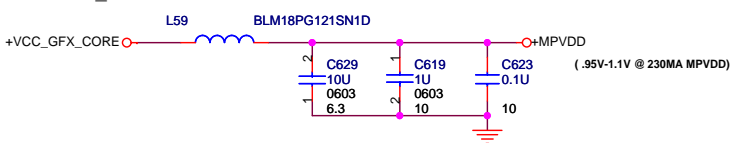
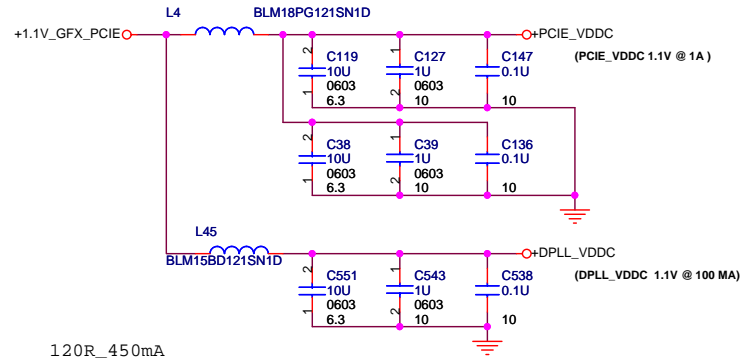
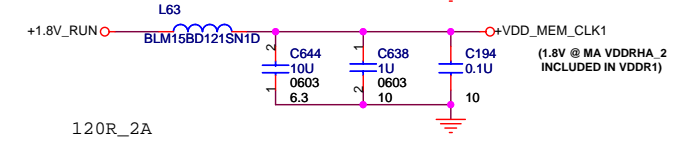
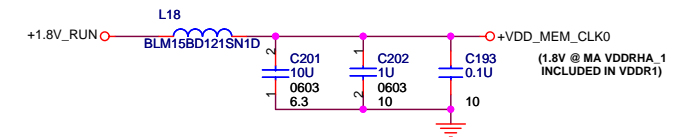




FOR M7x
INSTALL LVDDR TO +3.3V AND
LVDDC TO 1.8V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR



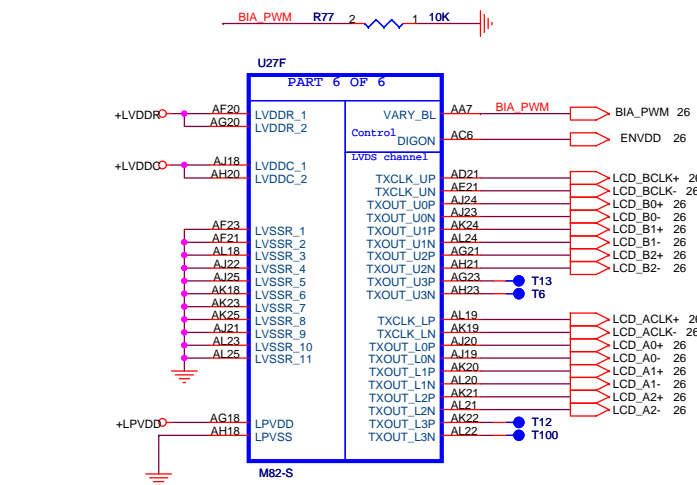
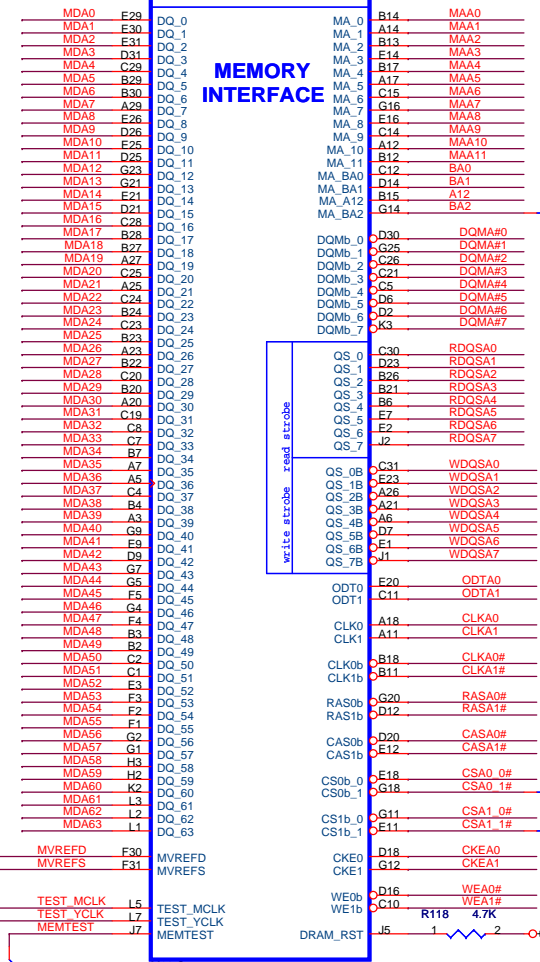
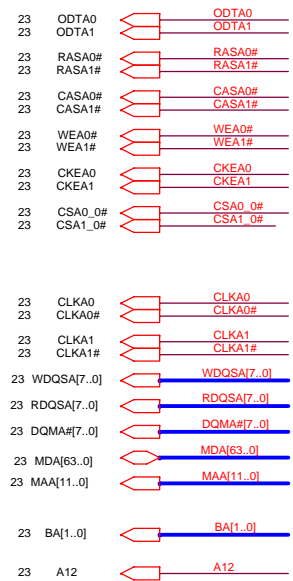
FOR M8x
INSTALL DPA_VDDR TO +1.1V AND
DPB_VDDR TO +1.1V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M7x
INSTALL DPA_VDDR AND DPB_VDDR TO +1.8V
WITH THE ONE DPA_VDDR FILTER
DO NOT INSTALL DPB_VDDR FILTER
INSTALL STRAP RESISTOR



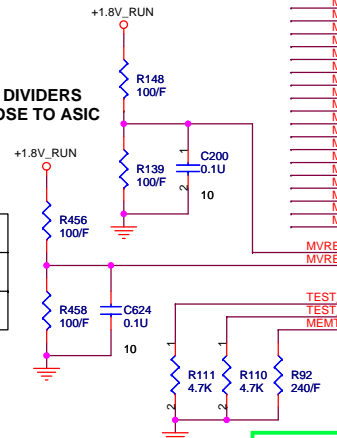
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE



Title			VGA-M82-S (PCIe)
Size	Document Number	Rev	
	FM6	1A	
Date:	Monday, June 30, 2008	Sheet	21 of 58

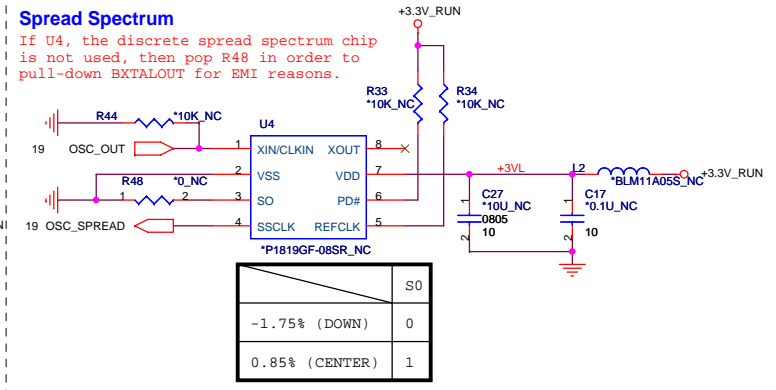


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



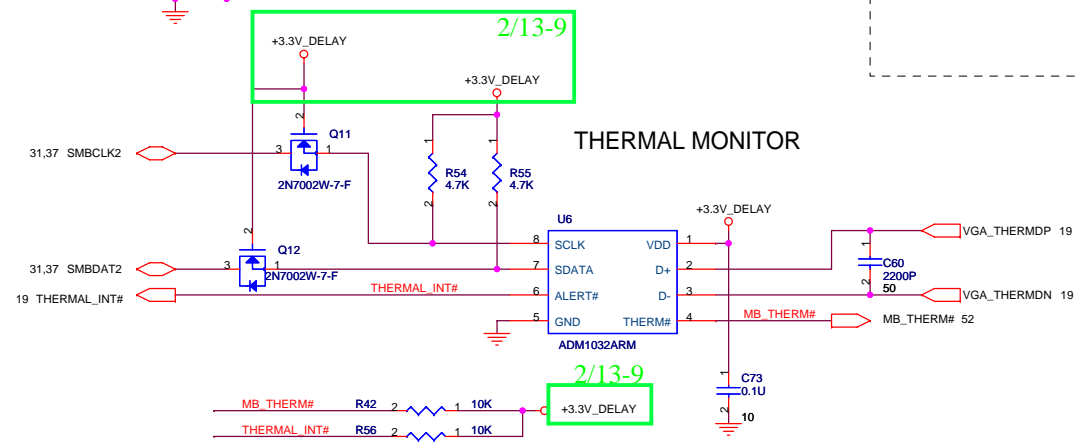
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

Spread Spectrum
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down BXTALOUT for EMI reasons.

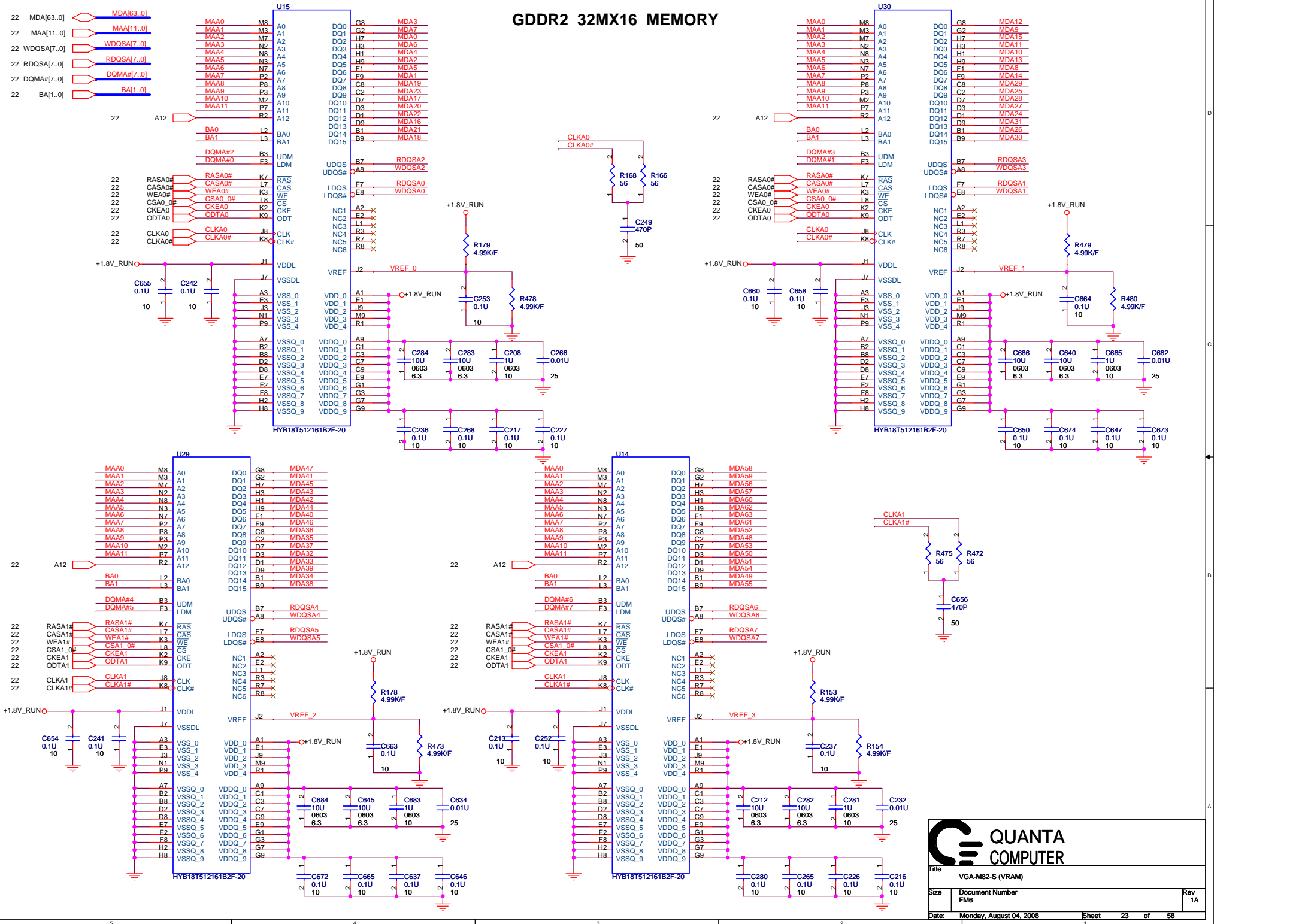


Remove MEM_RST

THERMAL MONITOR



GDDR2 32MX16 MEMORY



File: VGA-M82-S (VRAM)		
Size: FM6	Document Number: FM6	Rev: 1A
Date: Monday, August 04, 2008	Sheet: 23	of 58

GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	ATI Usage	FM6 Usage
GPIO0	PCIE FULL TX OUTPUT SWING	X	1
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	1
GPIO2	ATI reserved configuration straps.	RSVD	0
GPIO3	ATI reserved configuration straps.	RSVD	0
GPIO4	DEBUG SIGNALS MUXED OUT	0	0
GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
GPIO6	ATI Internal use only	0	0
GPIO10	Serial ROM clock to ROM.		0
ATI Usage recommended settings	0= DO NOT INSTALL RESISTOR, X = DESIGN DEPENDANT, RSVD = ATI RESERVED (DO NOT INSTALL)		

5

4

3

2

1

D

D

C

C

B

B

A

A



QUANTA
COMPUTER

Title		VGA-M82-S (PCIe)	
Size	Document Number	Rev	
	FM6	1A	
Date:	Monday, June 30, 2008	Sheet	25 of 58

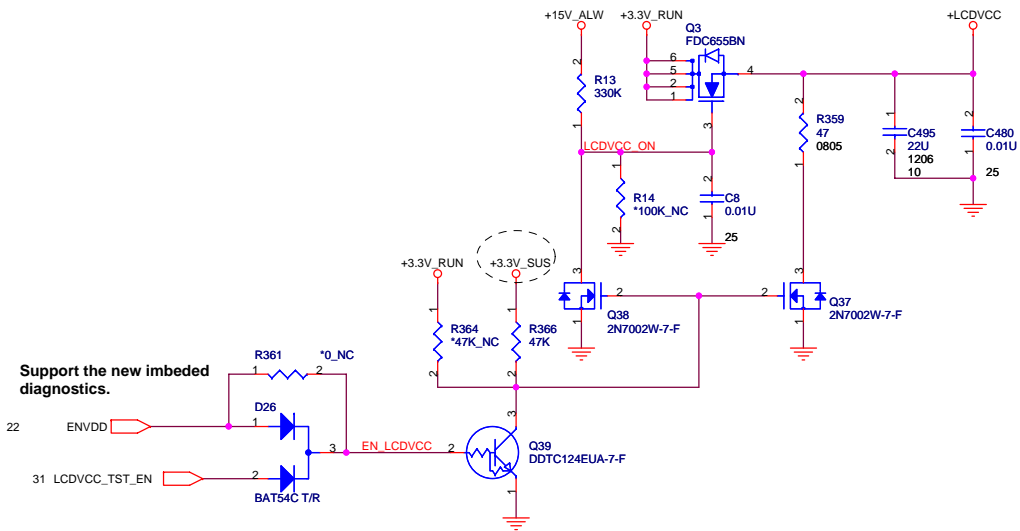
5

4

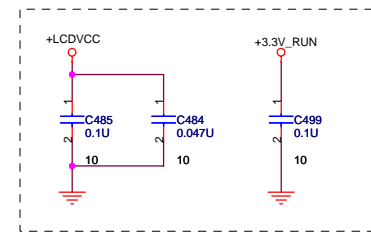
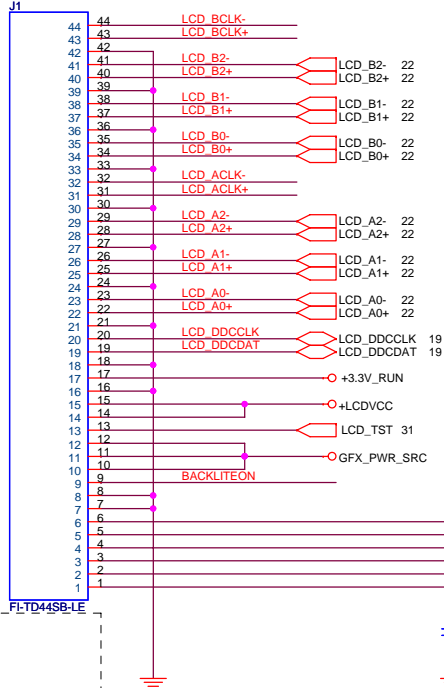
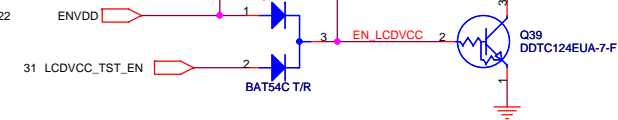
3

2

1

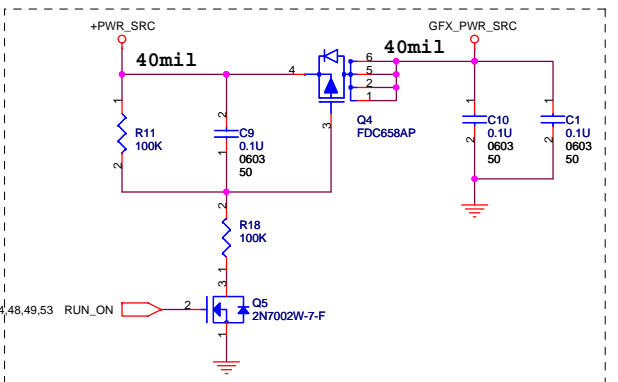


Support the new imbedded diagnostics.

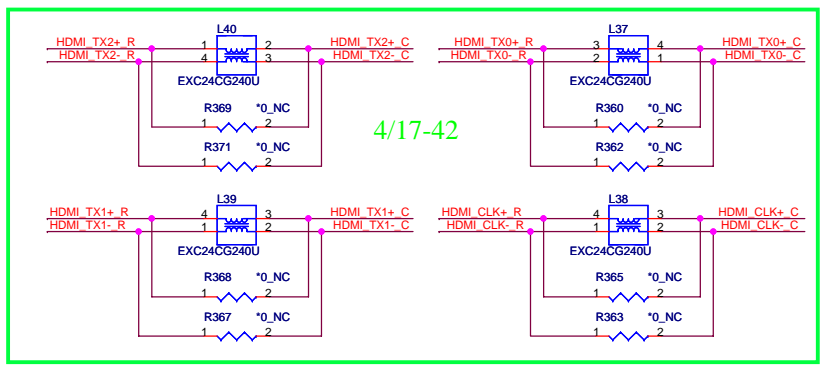
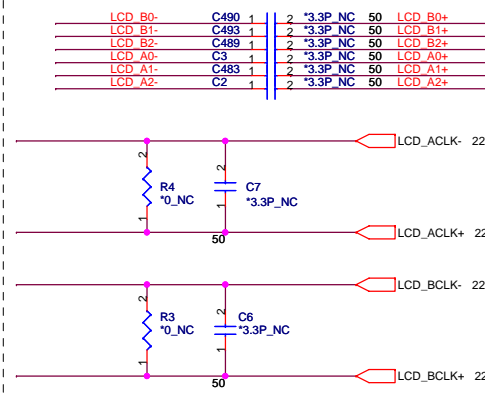


Address : A9H --Contrast
AAH --Backlight

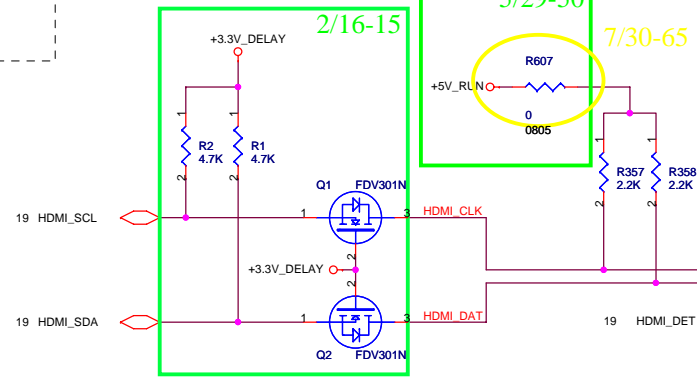
UMA
Populate R355 for DPST implementation only.
Populate R353 for platform without DPST support. No Stuff for Discrete DPST support due to back up plan.



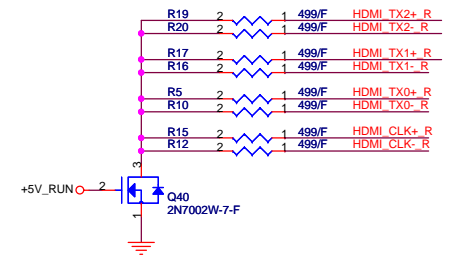
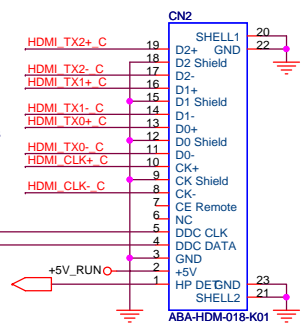
Shunt capacitors on LVDS for improving WWAN.



19	HDMI_TX2+	C502	0.1U/10V/X7R	HDMI_TX2+ R
19	HDMI_TX2-	C503	0.1U/10V/X7R	HDMI_TX2- R
19	HDMI_TX1+	C501	0.1U/10V/X7R	HDMI_TX1+ R
19	HDMI_TX1-	C500	0.1U/10V/X7R	HDMI_TX1- R
19	HDMI_TX0+	C491	0.1U/10V/X7R	HDMI_TX0+ R
19	HDMI_TX0-	C494	0.1U/10V/X7R	HDMI_TX0- R
19	HDMI_CLK+	C498	0.1U/10V/X7R	HDMI_CLK+ R
19	HDMI_CLK-	C497	0.1U/10V/X7R	HDMI_CLK- R



HDMI

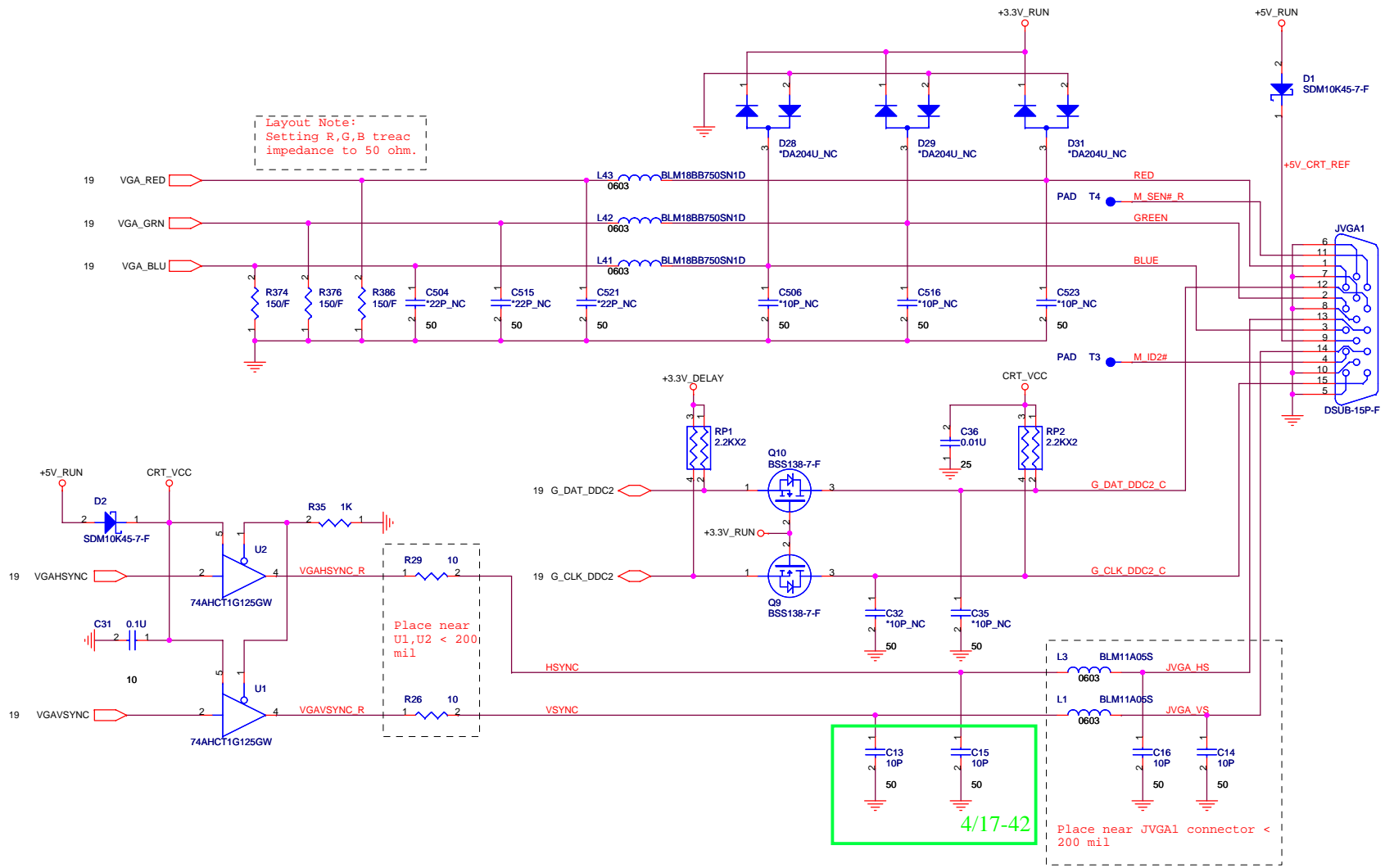


QUANTA COMPUTER

Title: LCD CONN & CK-SSCD

Size: Document Number FM6 Rev 2A

Date: Wednesday, July 30, 2008 Sheet 26 of 58



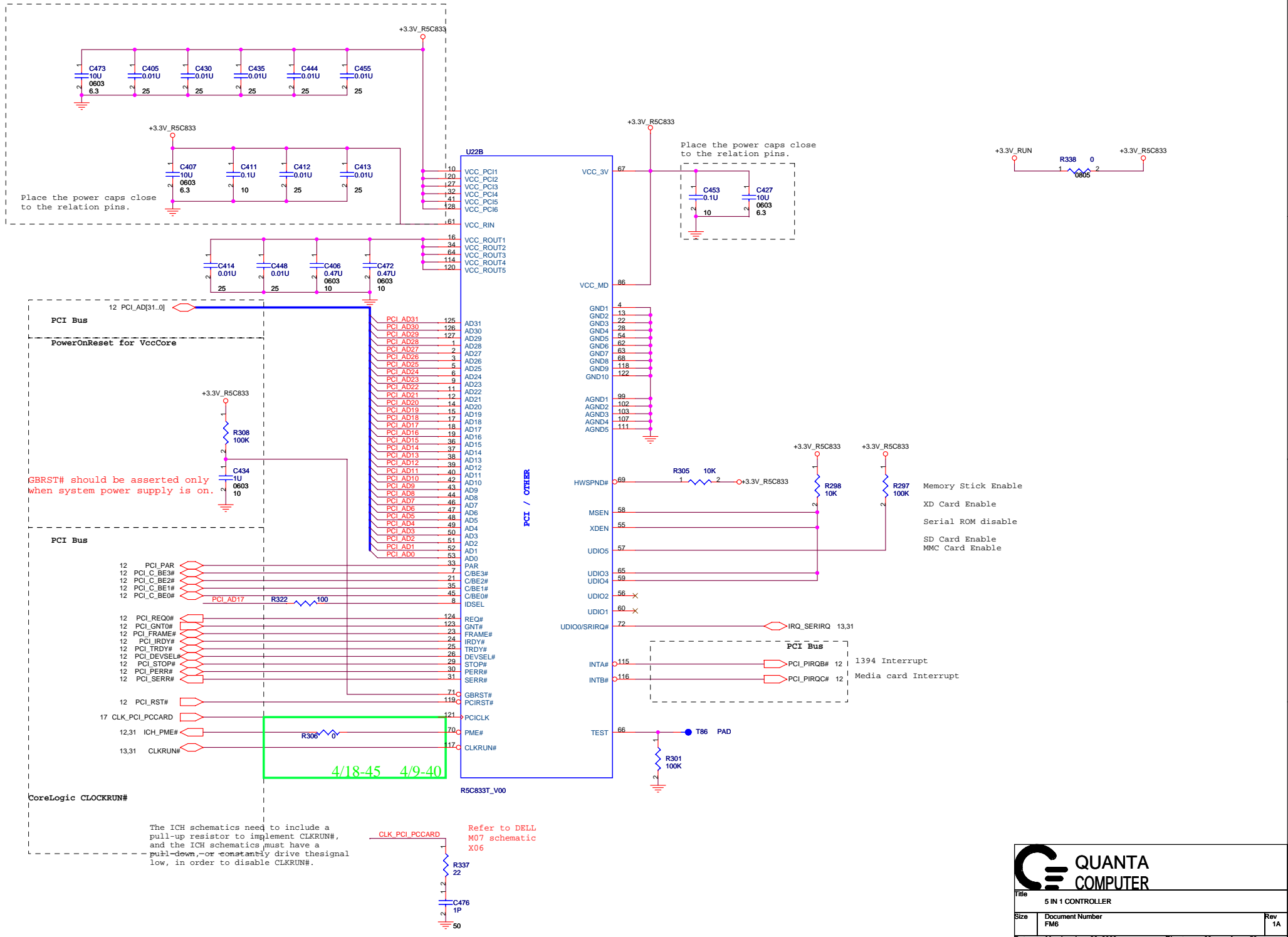
Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

Place near
U1,U2 < 200
mil

4/17-42

Place near JVGA1 connector <
200 mil





Place the power caps close to the relation pins.

Place the power caps close to the relation pins.

GBRST# should be asserted only when system power supply is on.

The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.

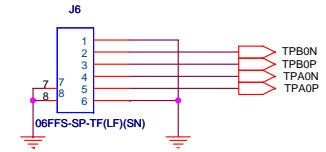
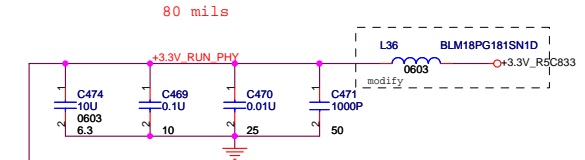
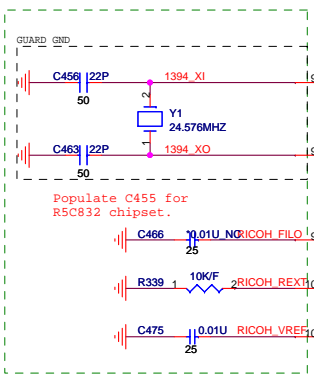
Refer to DELL M07 schematic X06

QUANTA COMPUTER

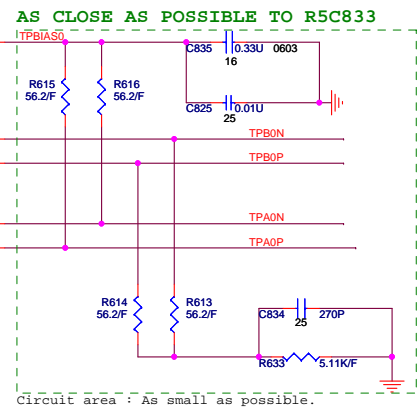
Title: 5 IN 1 CONTROLLER

Size	Document Number	Rev
FM6		1A

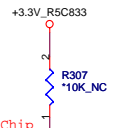
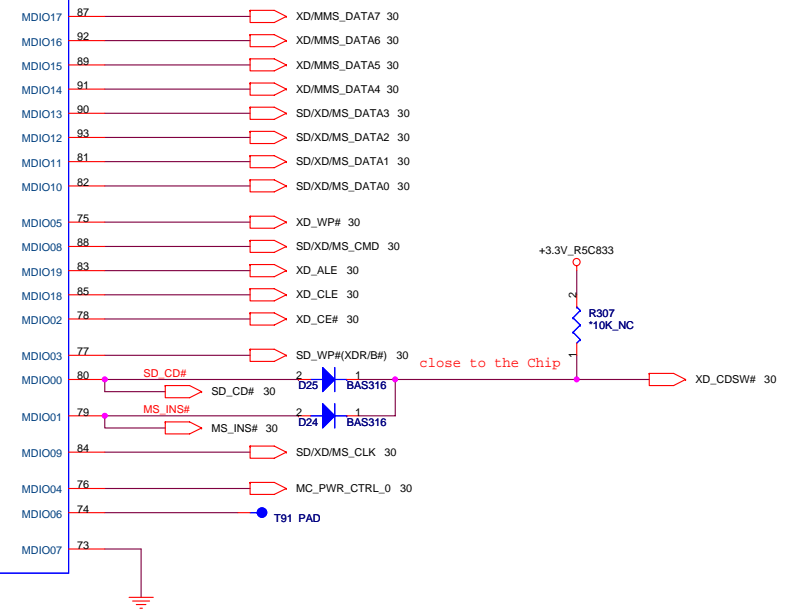
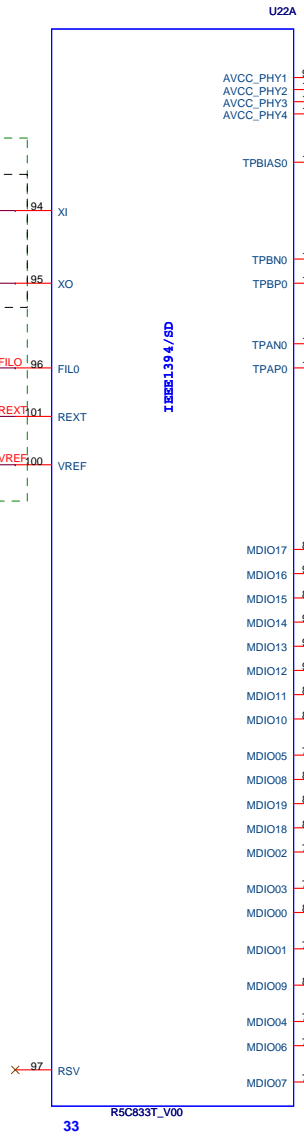
Date: Monday, June 30, 2008 Sheet 28 of 58



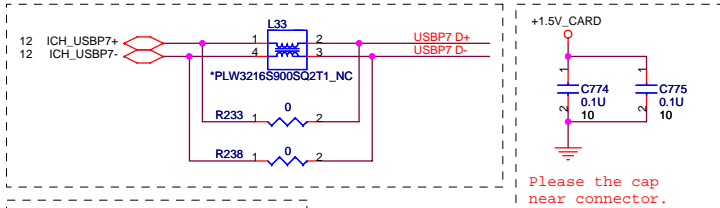
Place these caps as close to the U26 as possible.



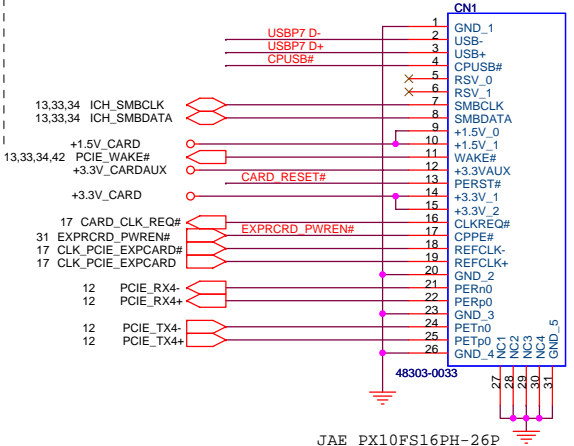
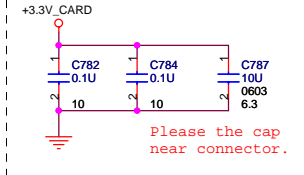
- *TPA0P/TPA0N, TPB0P/TPB0N pair trace : As close as possible.
- *TPA0P/TPA0N, TPB0P/TPB0N pair trace : Same length electrically.
- *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



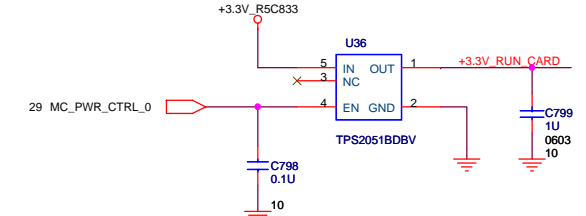
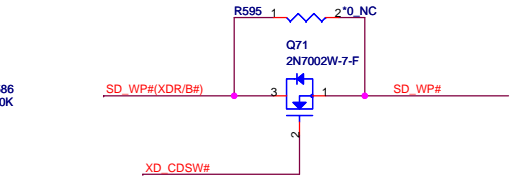
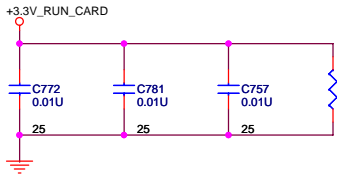
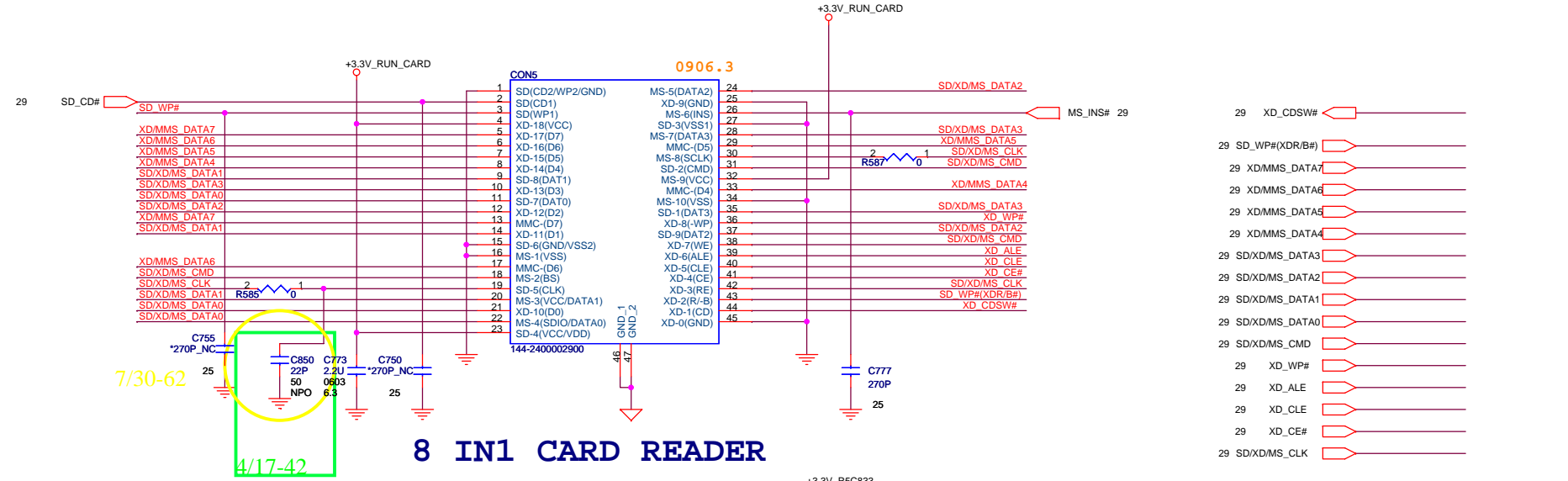
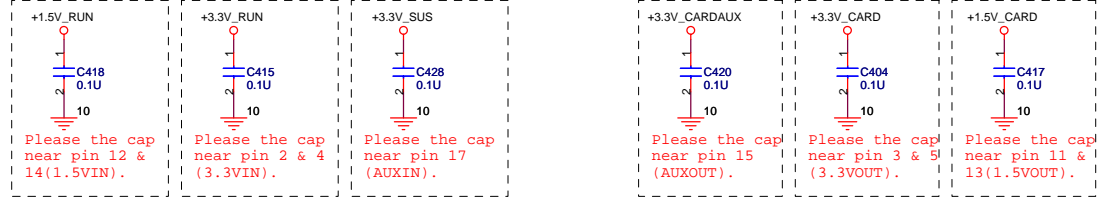
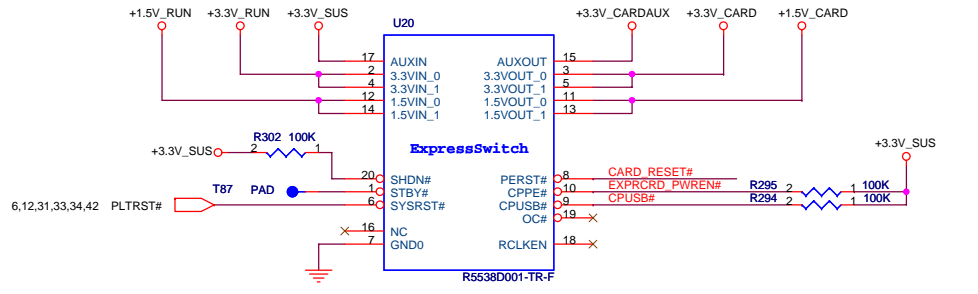
Express Card



Please the cap near connector.



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

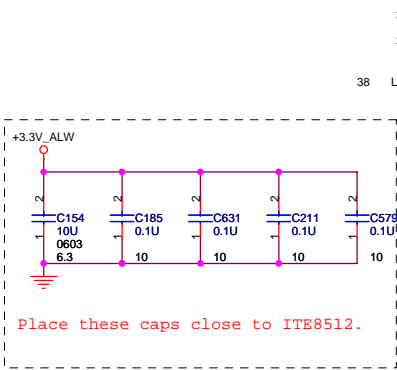


QUANTA COMPUTER

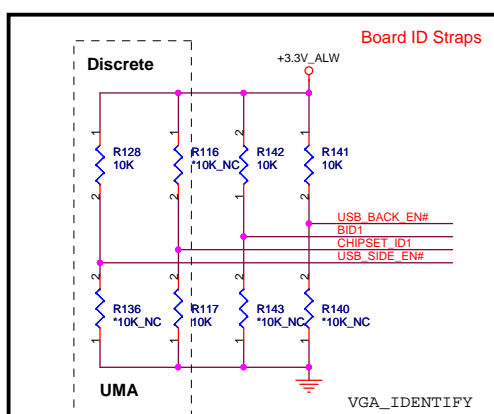
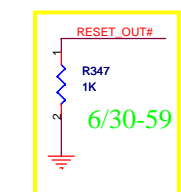
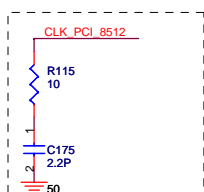
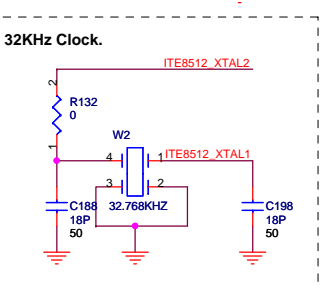
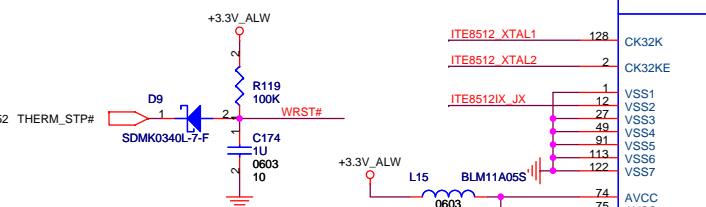
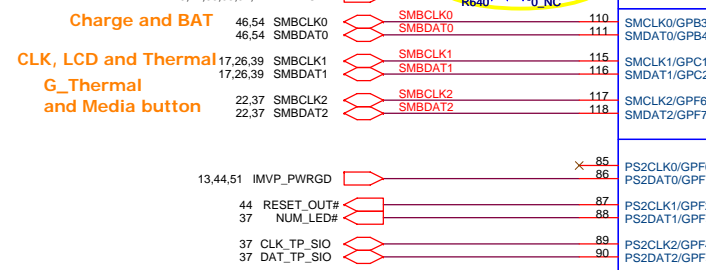
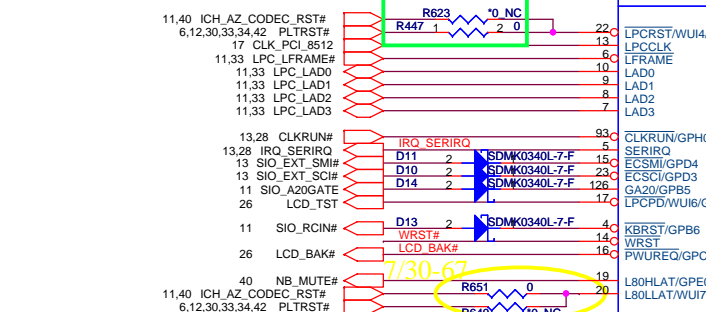
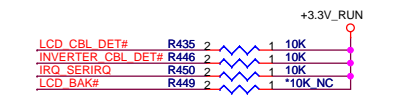
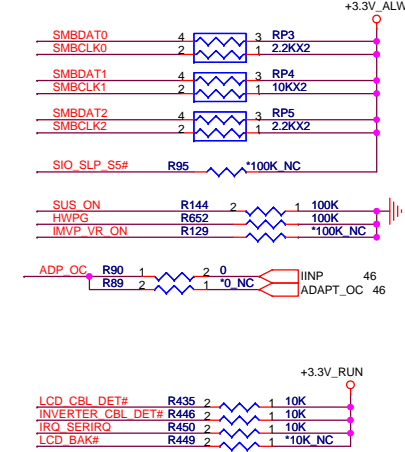
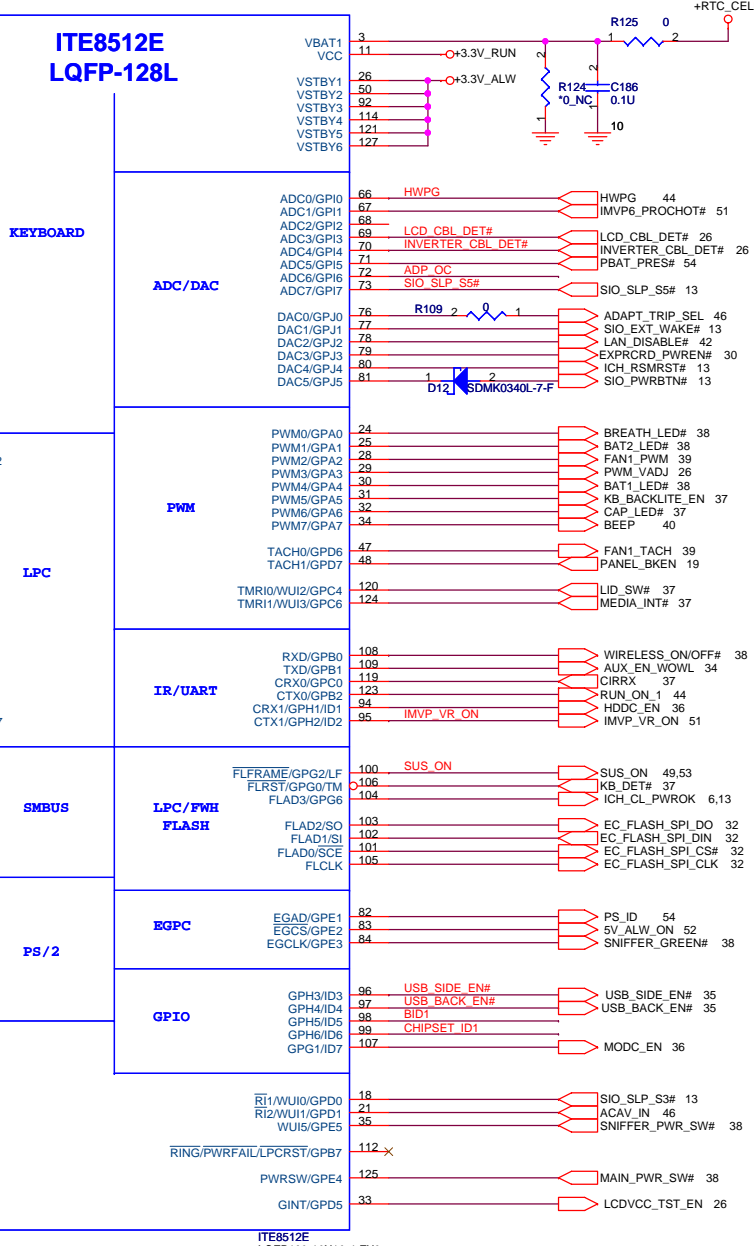
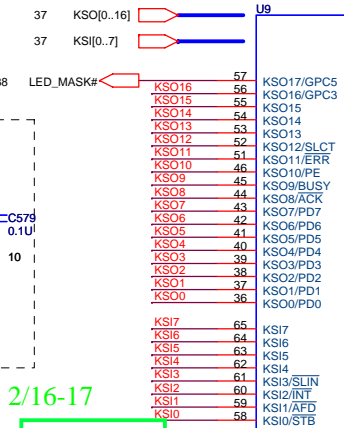
Title: ExpressCard/SmartCard

Size: FM6	Document Number	Rev: 2A
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Date: Wednesday, July 30, 2008 Sheet 30 of 58



Place these caps close to ITE8512.



VGA_IDENTIFY

USB_SIDE_EN#
1 = Discrete Gfx.
0 = UMA.

CHIPSET ID1	BID1	USB BACK EN#	FM6B(UMA)	FM6(Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	GT (A00)	GT (A00)
0	0	0	(A01)	(A01)
0	0	1		

QUANTA COMPUTER

Title: Ultra I/O Controller ECE5028

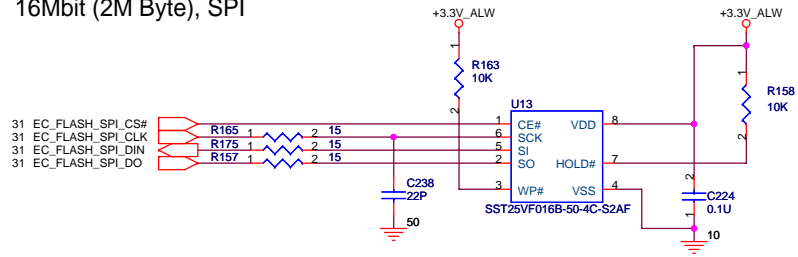
Size: Document Number FM6

Date: Monday, August 04, 2008

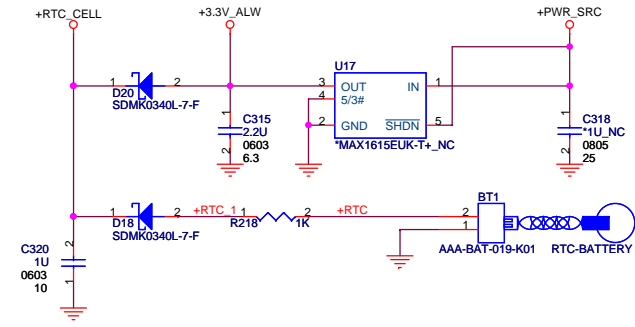
Sheet: 31 of 58

Rev: 3A

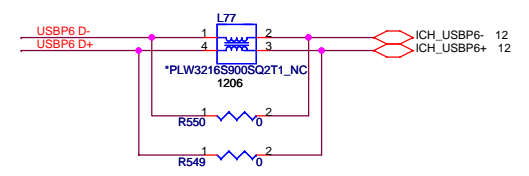
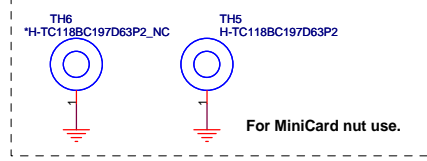
16Mbit (2M Byte), SPI



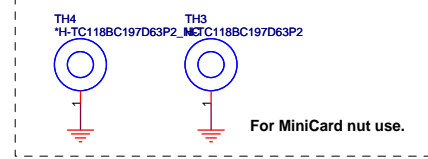
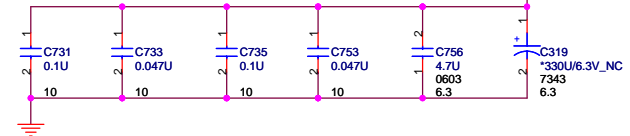
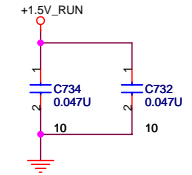
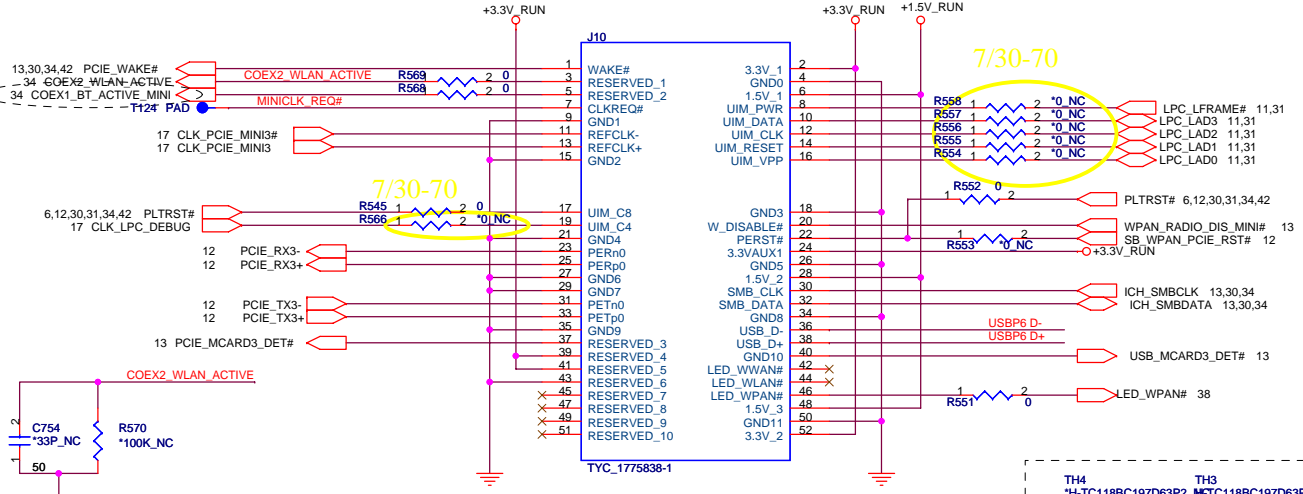
RTC BATTERY



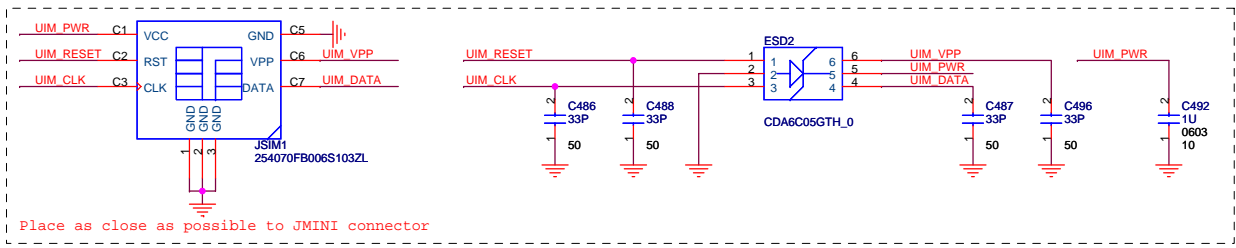
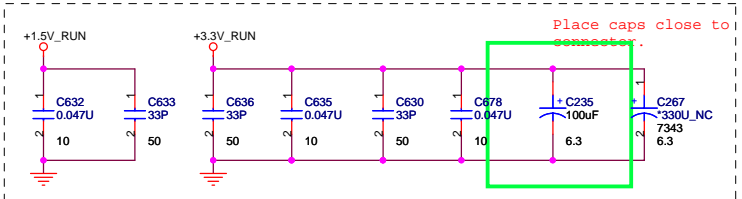
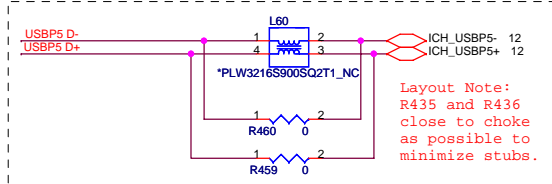
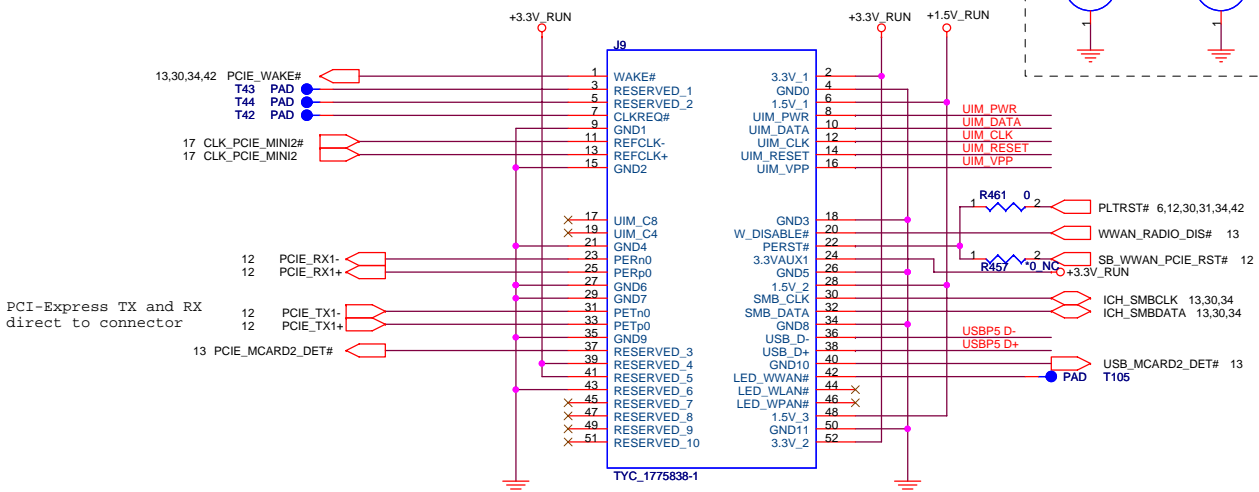
Title		
Ultra I/O Controller ECE5028		
Size	Document Number	Rev
	FM6	3A
Date:	Monday, June 30, 2008	Sheet 32 of 58



MiniCard Robson, BT. UWB connector



MiniCard WWAN connector



QUANTA COMPUTER

Title: MINI-PCI

Size: FM6	Document Number: FM6	Rev: 2A
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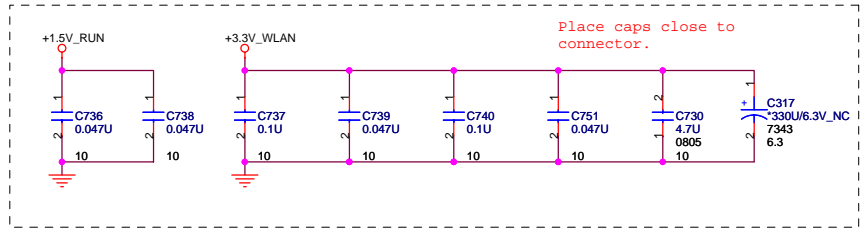
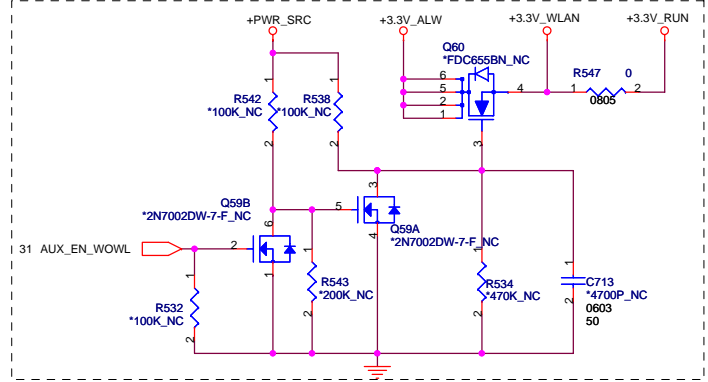
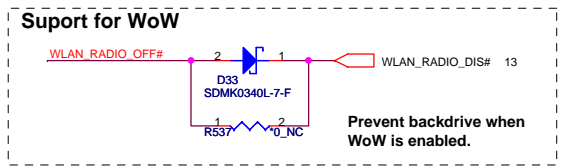
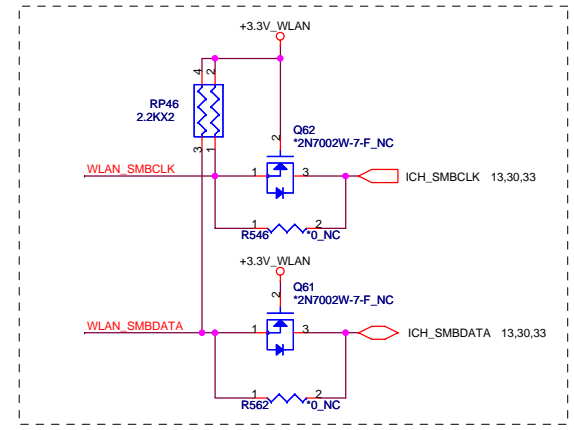
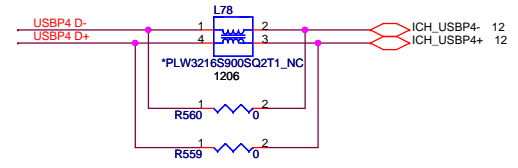
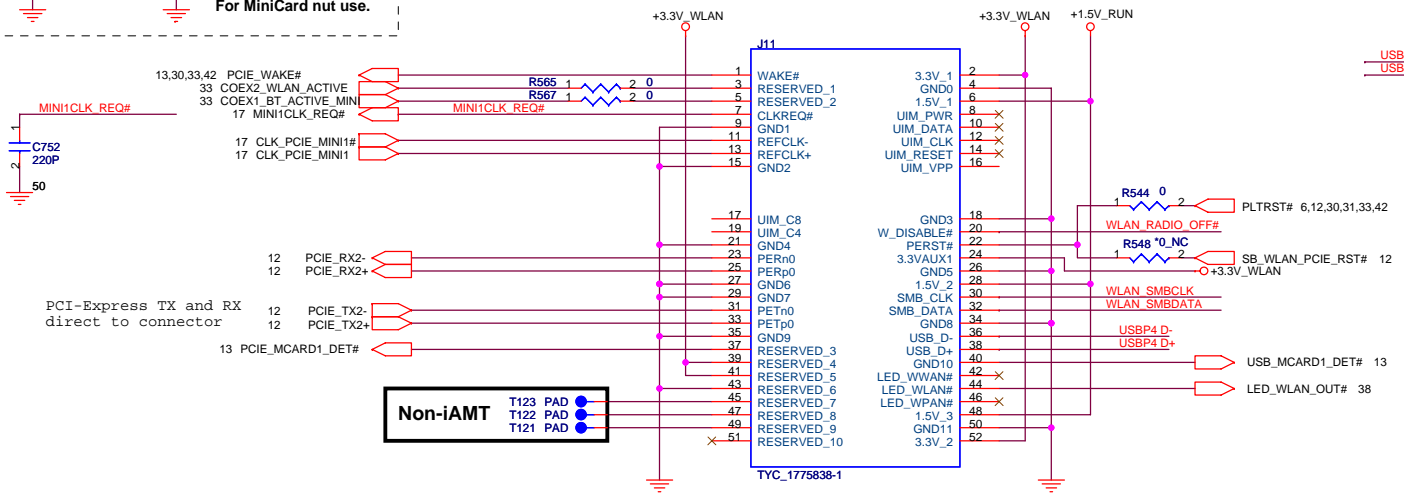
Date: Friday, August 01, 2008 Sheet: 33 of 58

TH2 TH1
 "H-TC177BC197D83P2_NCH-TC177BC197D83P2

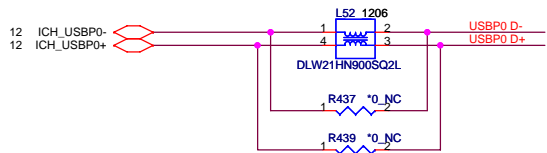


For MiniCard nut use.

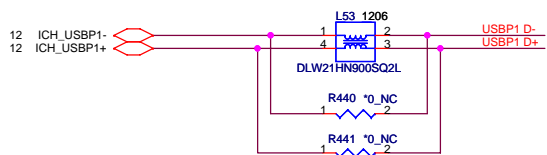
MiniCard WLAN connector



External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



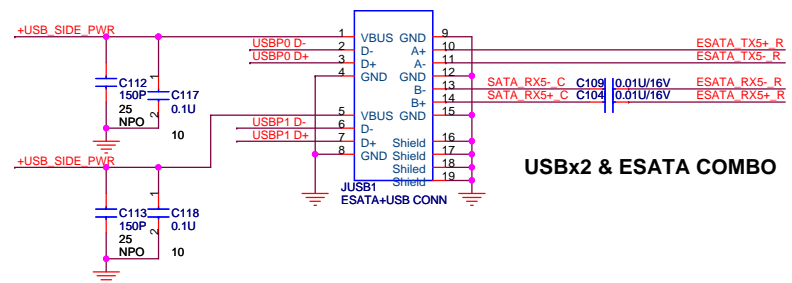
2/22-25
4/17-42



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Side External USBX2

2/13-4

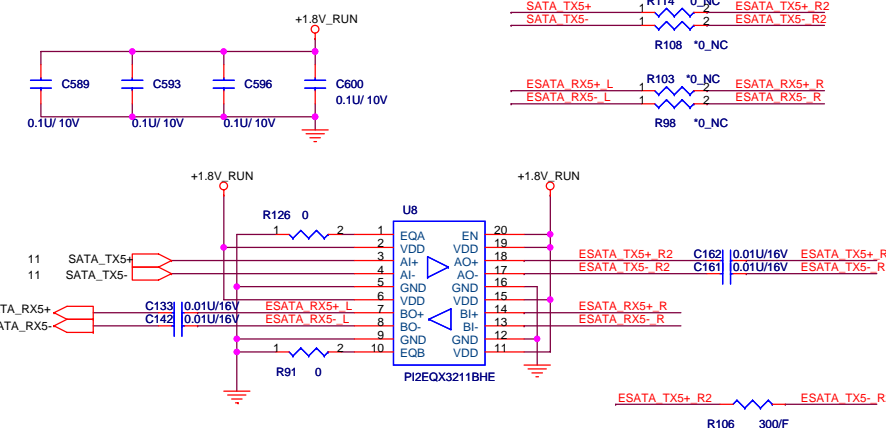


USBx2 & ESATA COMBO

5/29-52

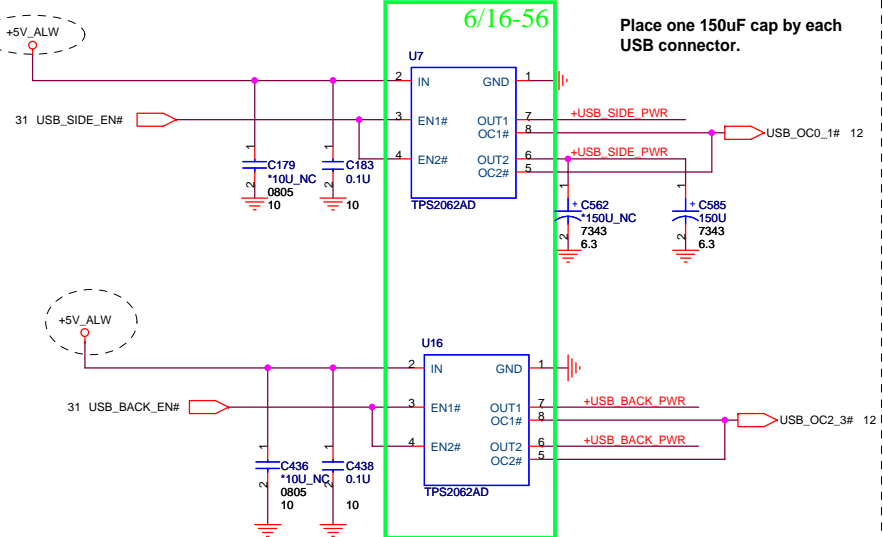
2/20-22

E-SATA Re-driver



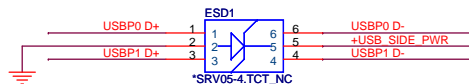
6/16-56

Place one 150uF cap by each USB connector.

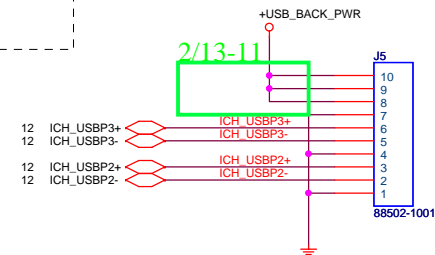


Each channel is 1A

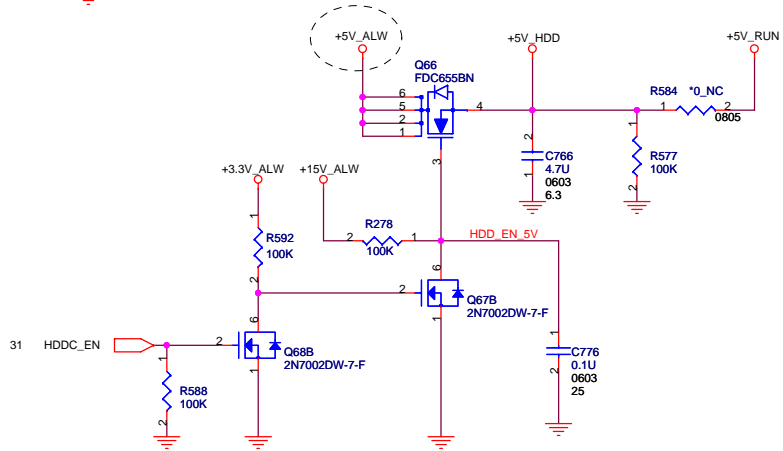
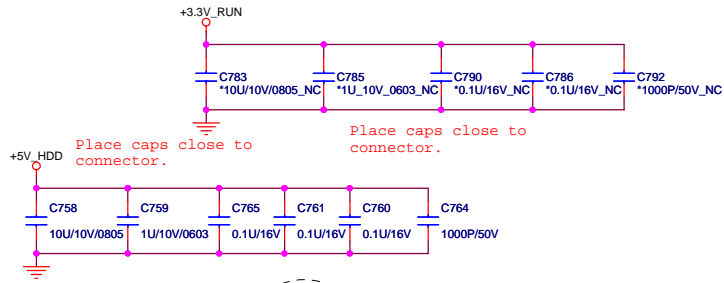
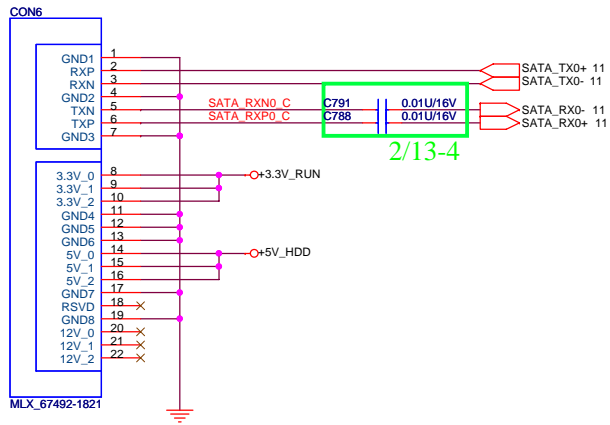
Place ESD diodes as close as USB connector.



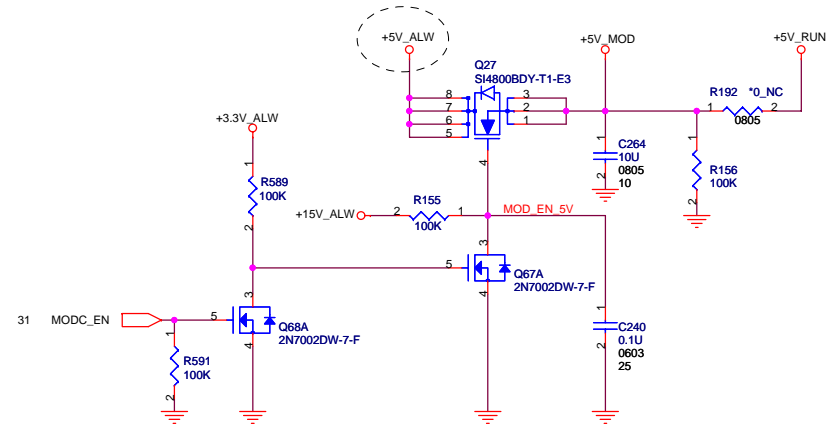
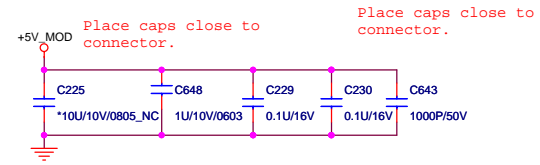
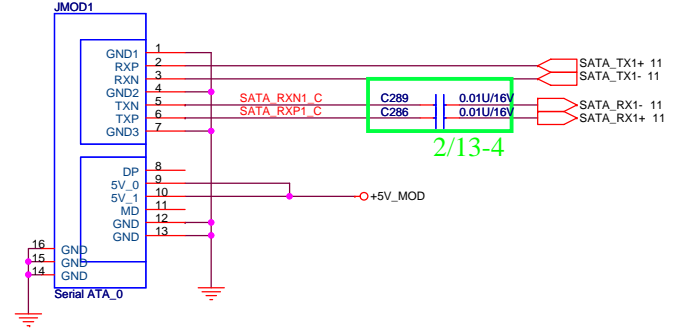
MB side



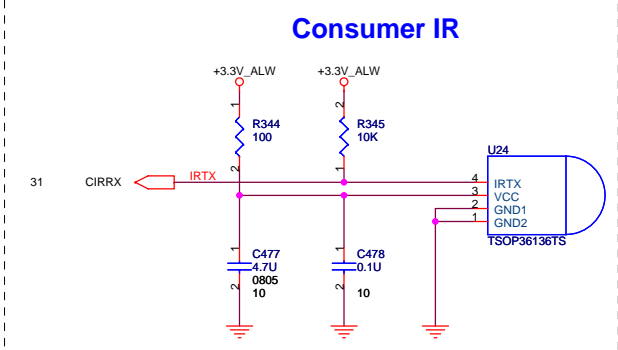
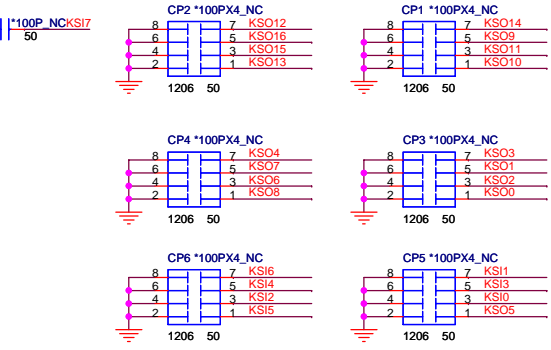
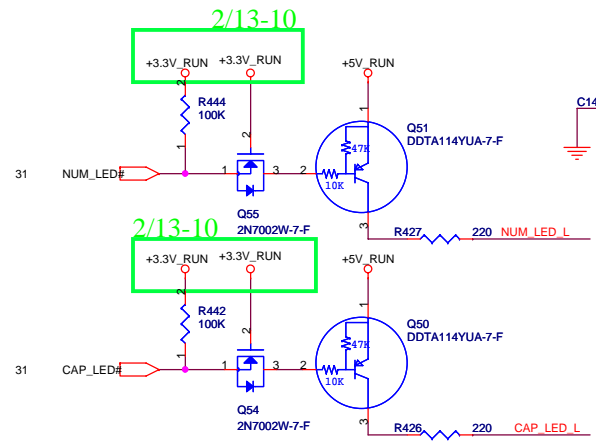
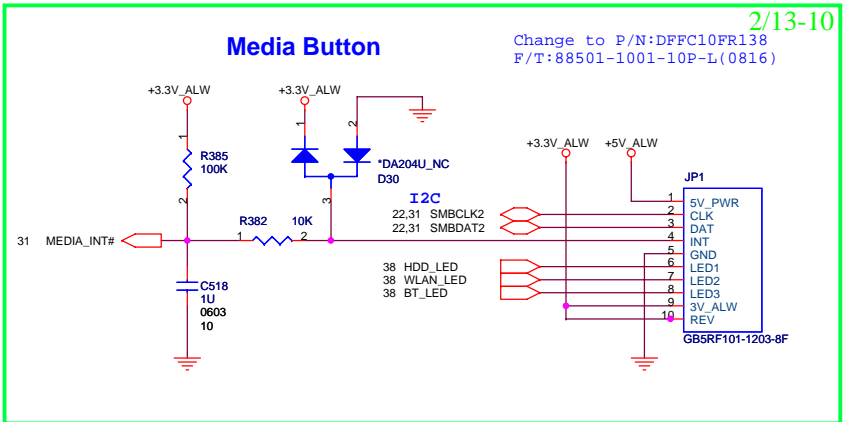
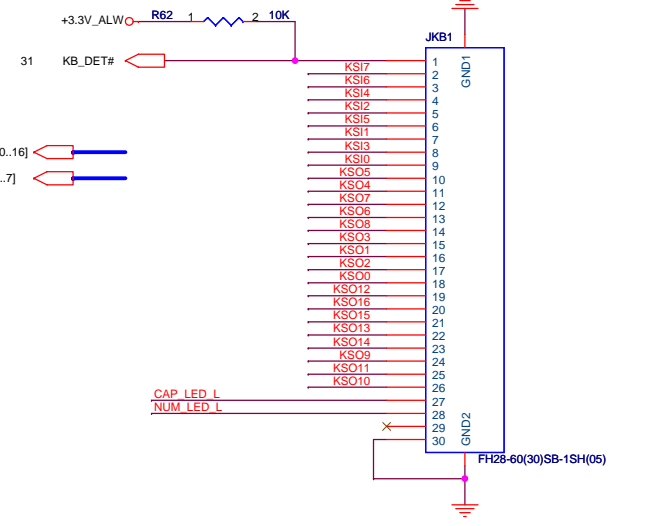
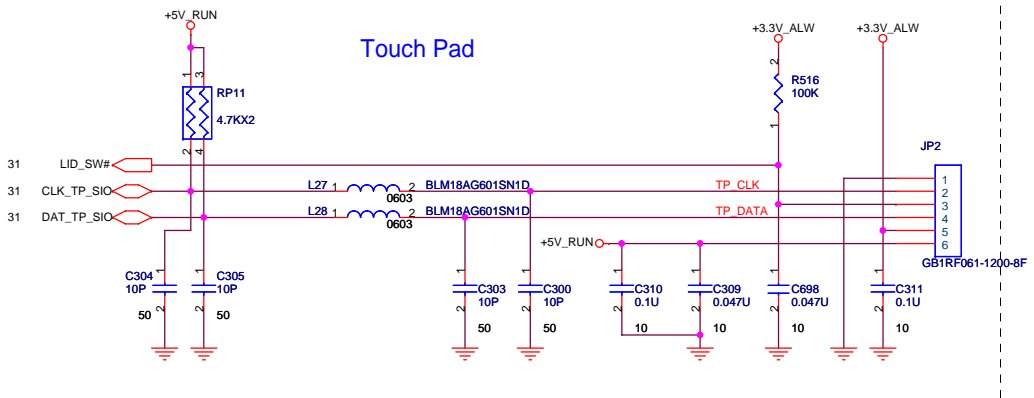
SATA Connector.



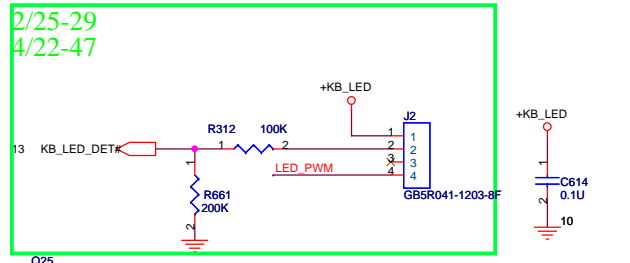
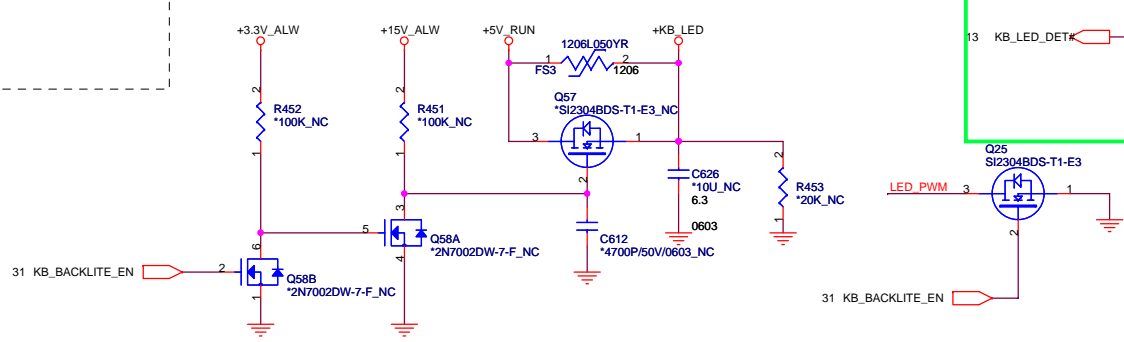
ODD Connector



KEYBOARD CONNECTOR



Key board Illumination

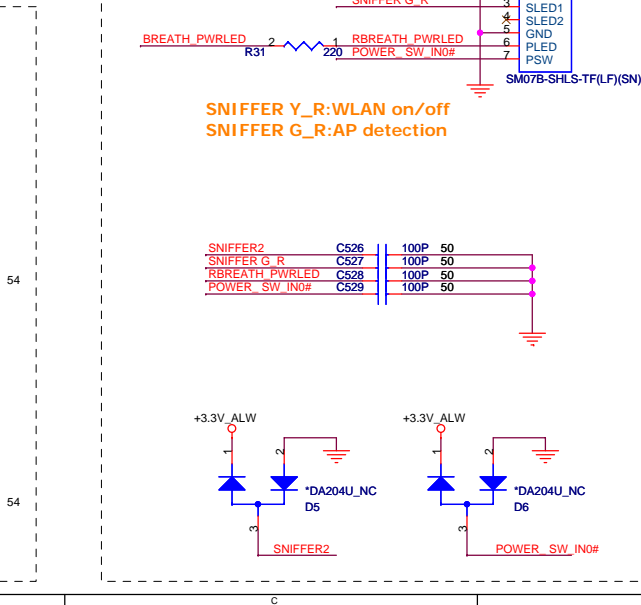
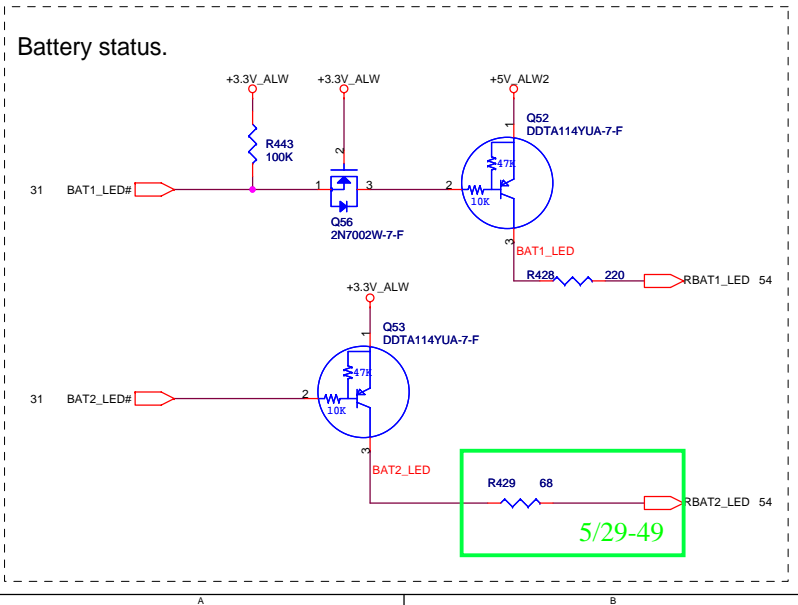
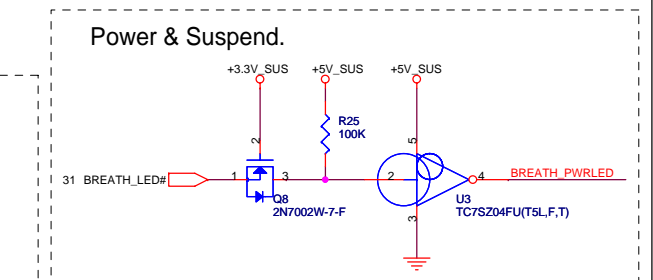
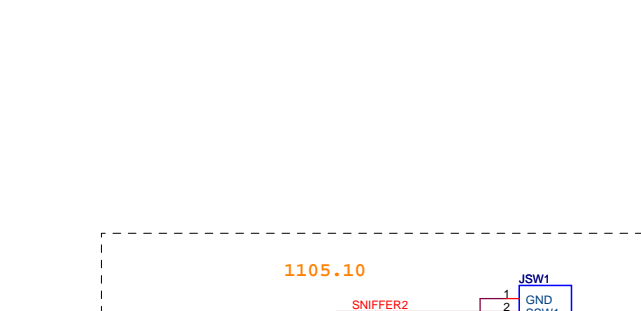
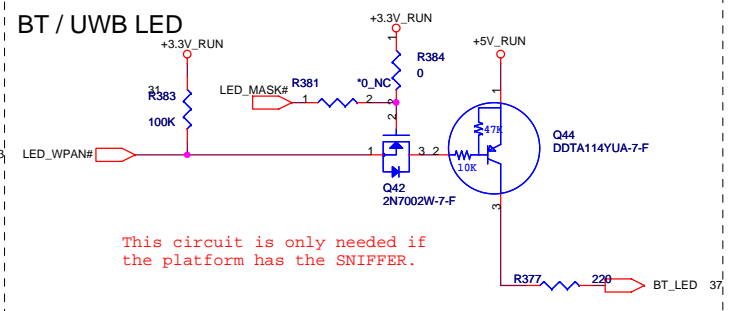
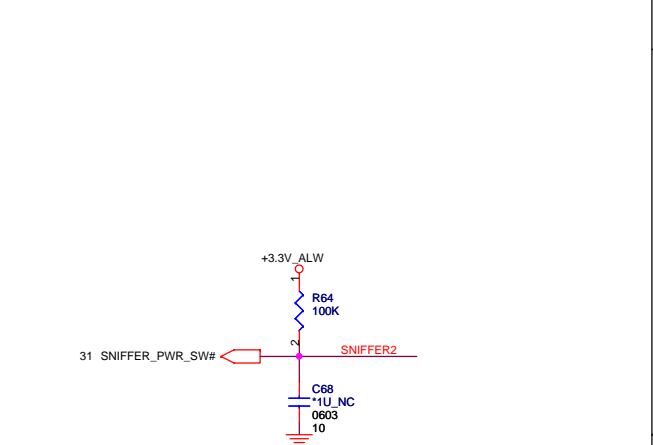
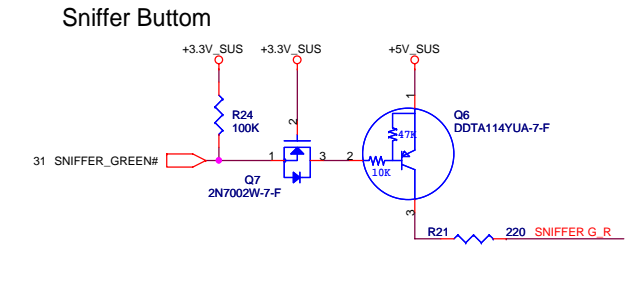
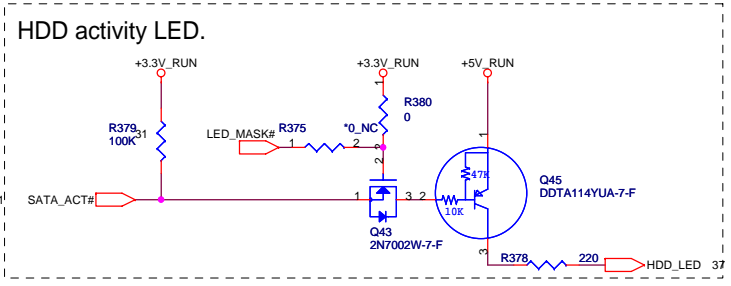
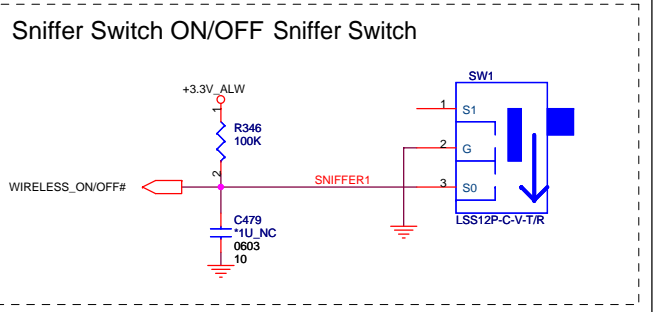
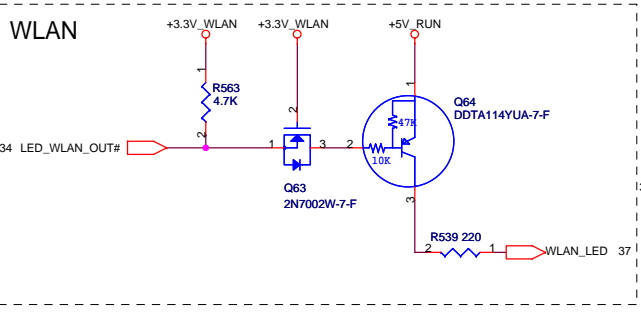
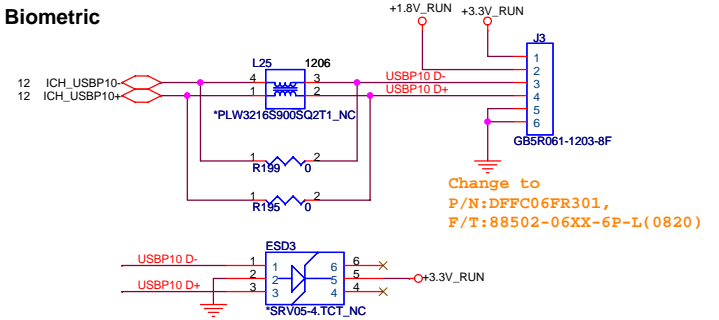


QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

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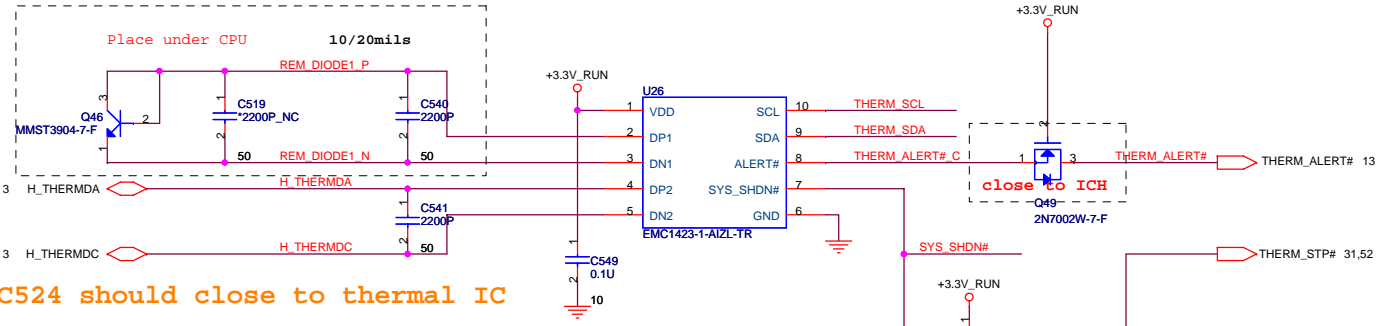
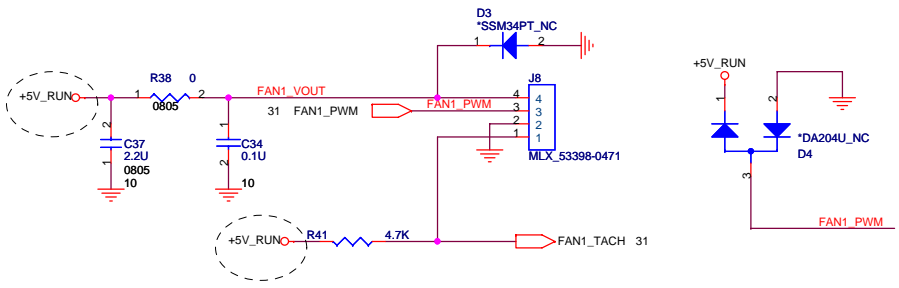


QUANTA
COMPUTER

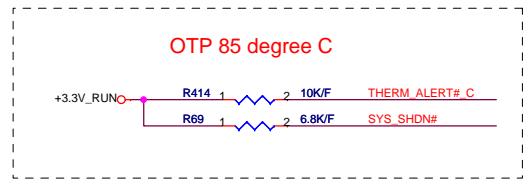
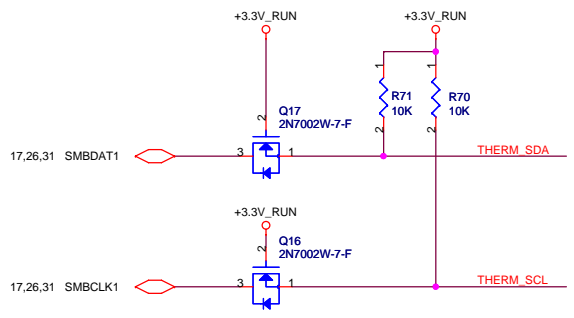
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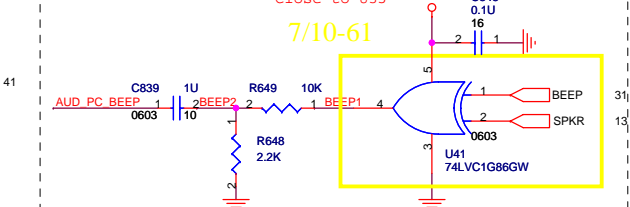
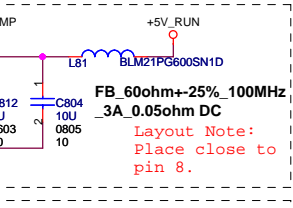
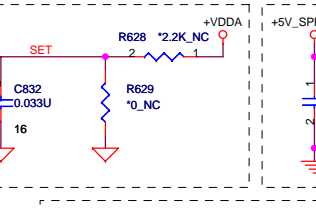
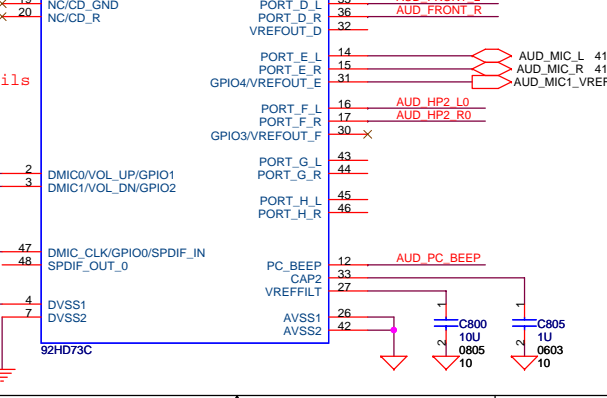
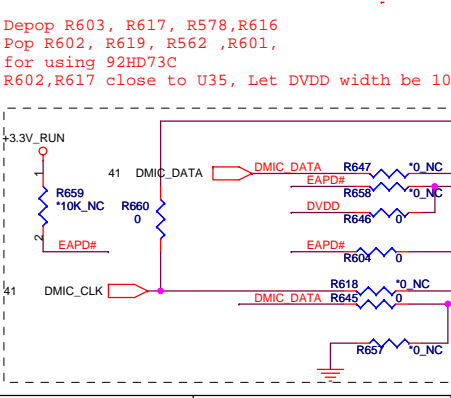
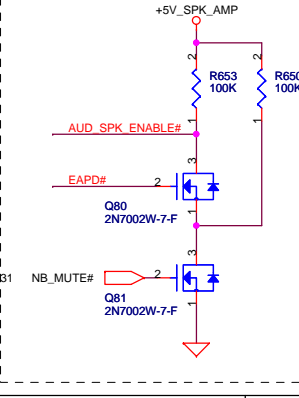
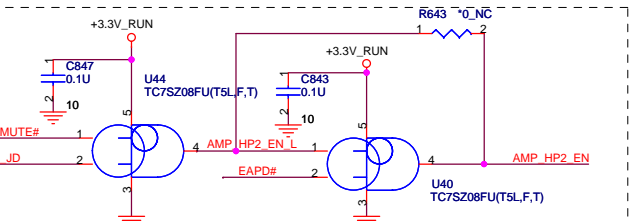
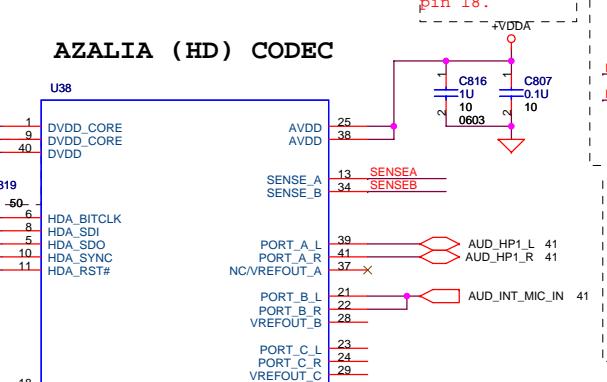
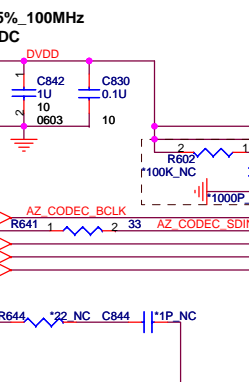
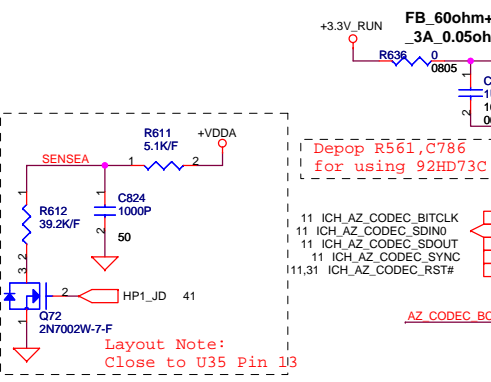
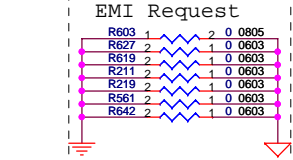
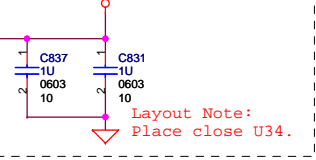
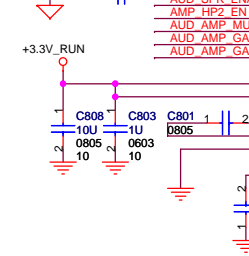
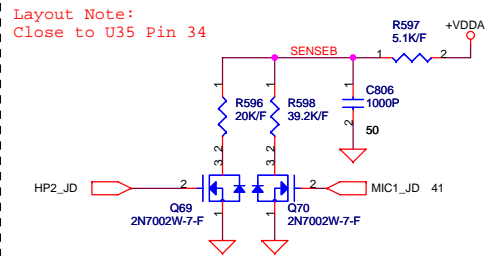
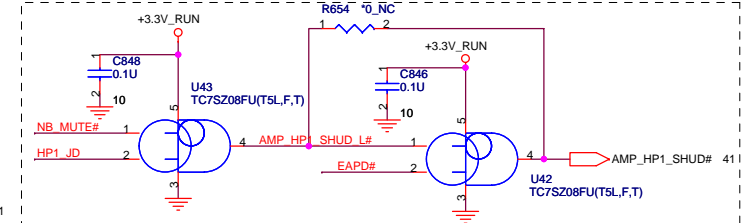
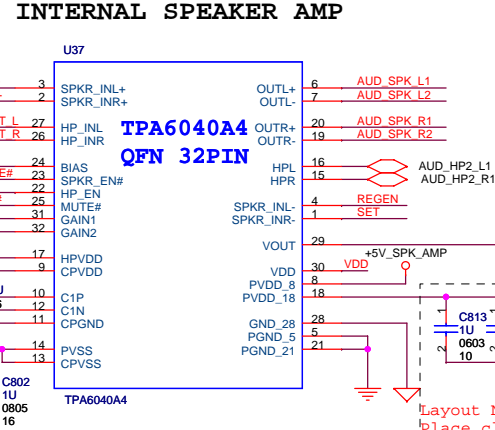
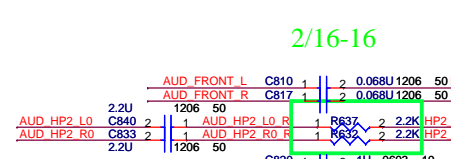
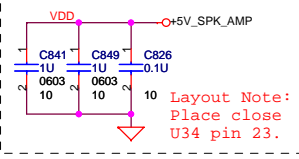
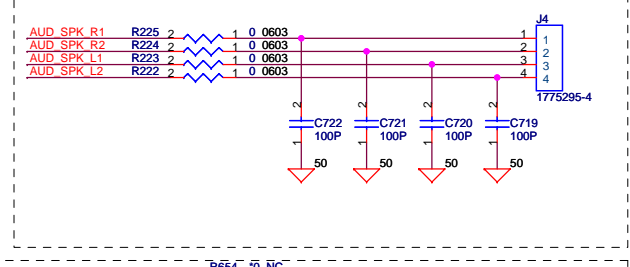
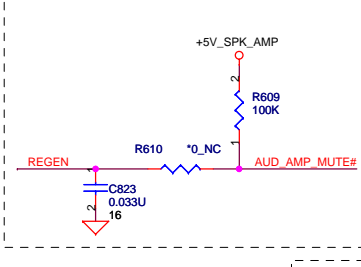
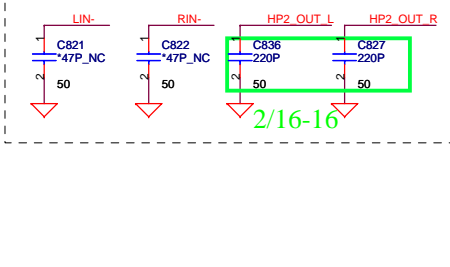
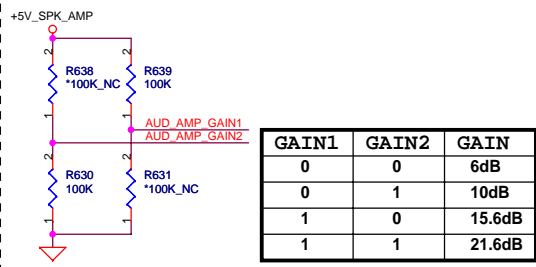
Size: FM6	Document Number: Rev 3A
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C523, C524 should close to thermal IC





QUANTA COMPUTER

Title: Azelia CODEC

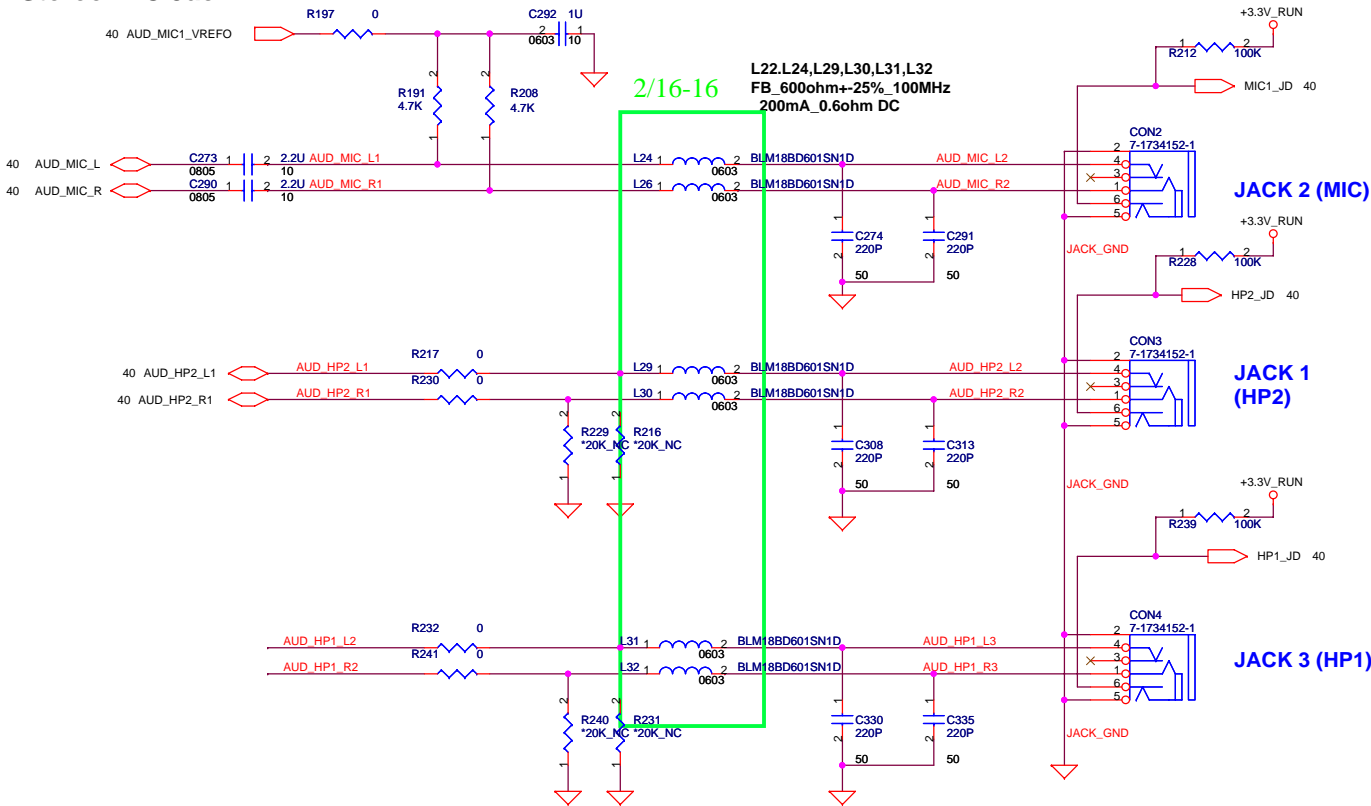
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Date: Wednesday, July 30, 2008

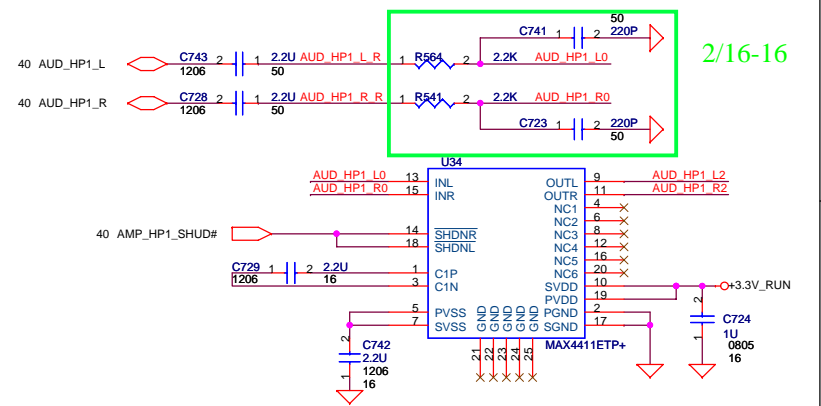
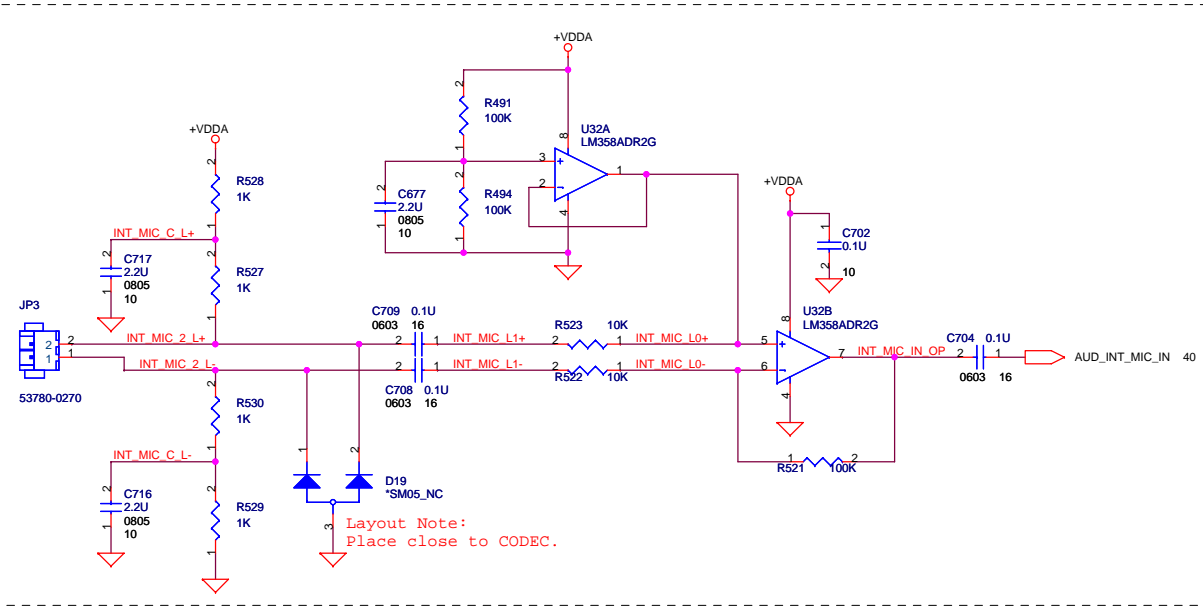
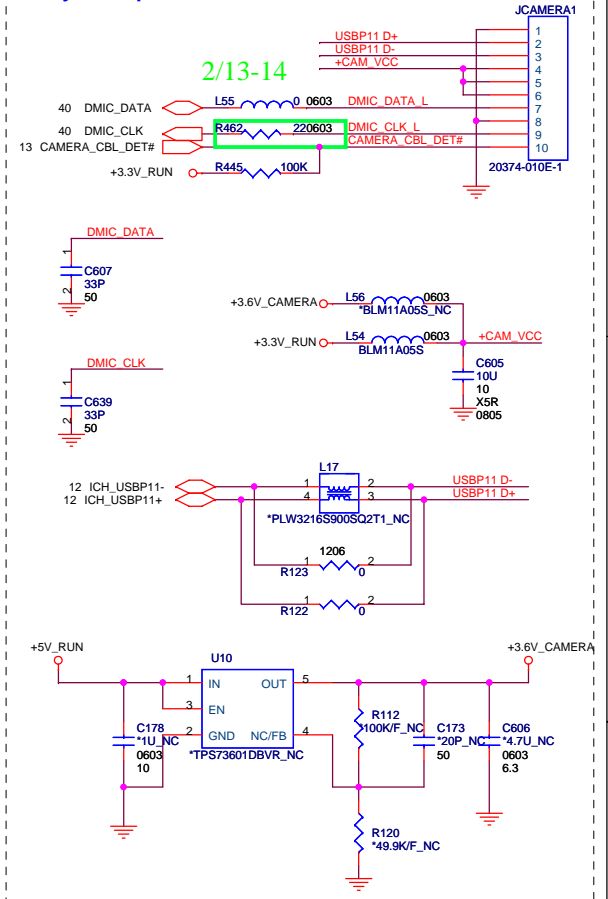
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Rev: 2A

Headphone Jack Stereo MIC Jack



Array Microphone & Camera



QUANTA COMPUTER

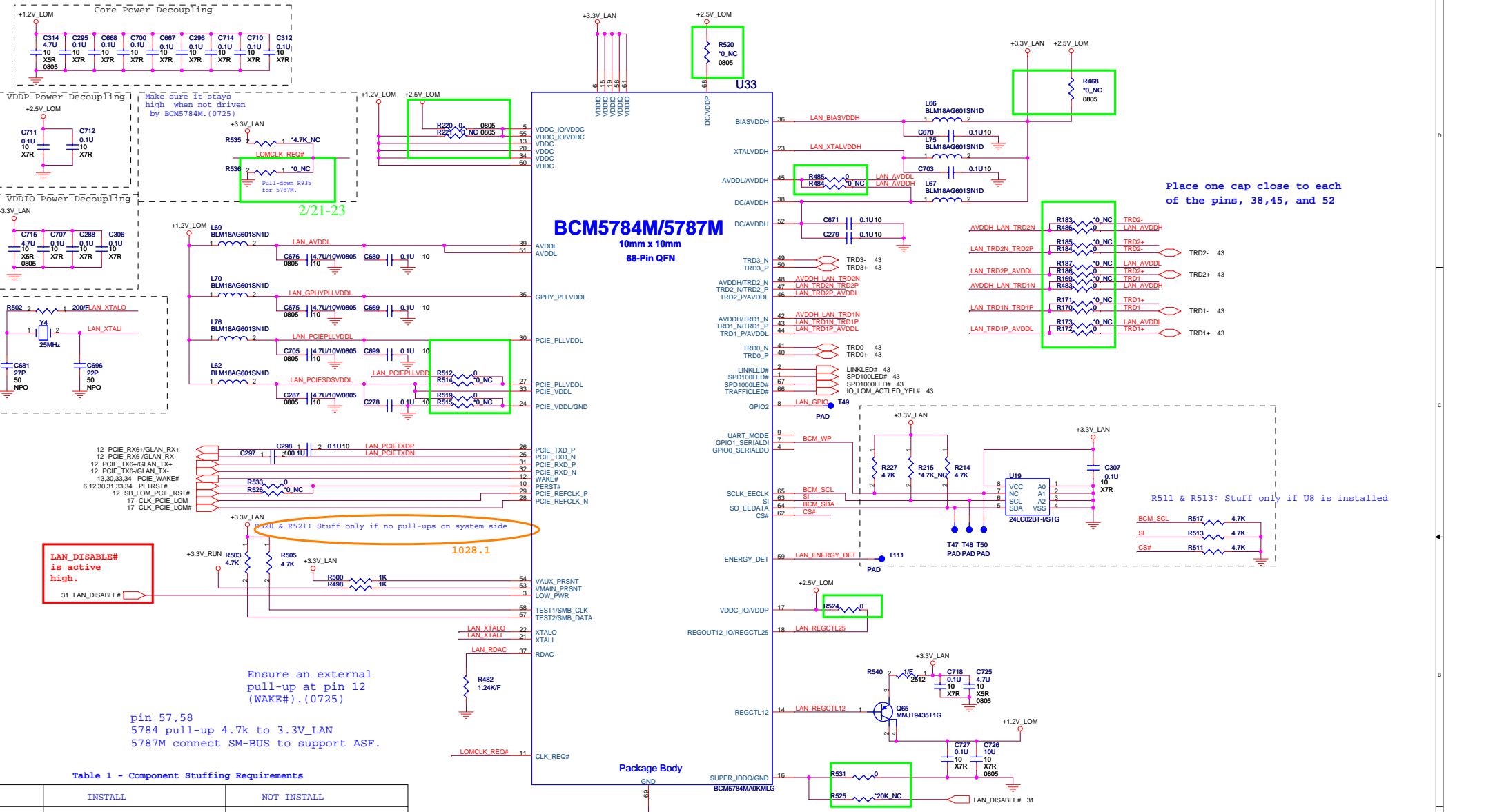
Title: **AUDIO CONN**

Size: **Document Number FM6**

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Sheet: **41** of **58**



BCM5784M/5787M 10mm x 10mm 68-Pin QFN

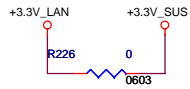
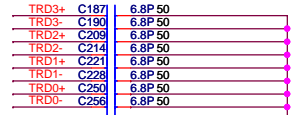
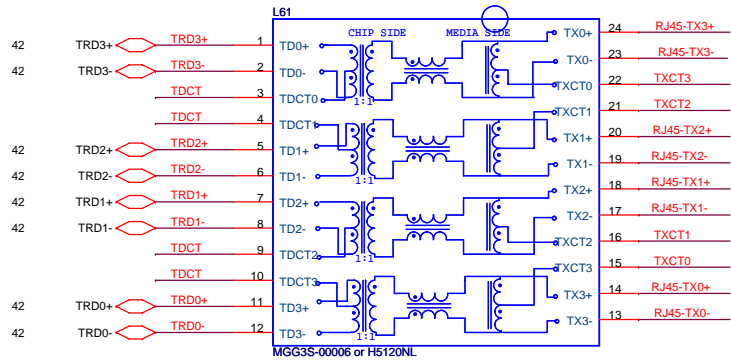
Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R221, R487, R488, Q55, C671, C672, C686, C687, R174, R176, R178, R169, R171, R173, R459, R443, R492	R209, R485, R491, R496, R461, R175, R177, R458, R170, R172, R460, R451
5784	R209, R485, R491, R496, R461, R175, R177, R458, R170, R172, R460, R451	R221, R487, R488, Q55, C671, C672, C686, C687, R174, R176, R178, R169, R171, R173, R459, R443, R492

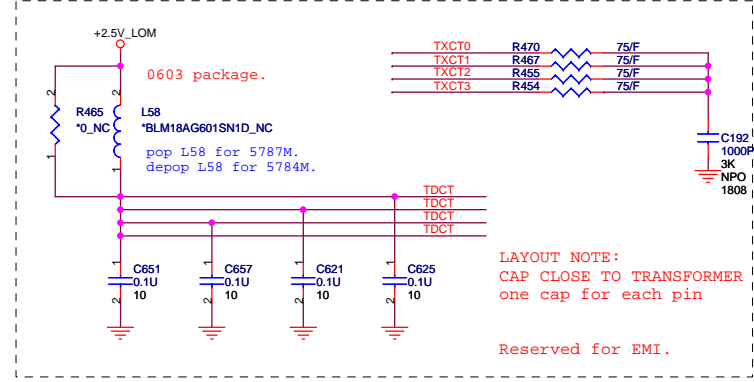
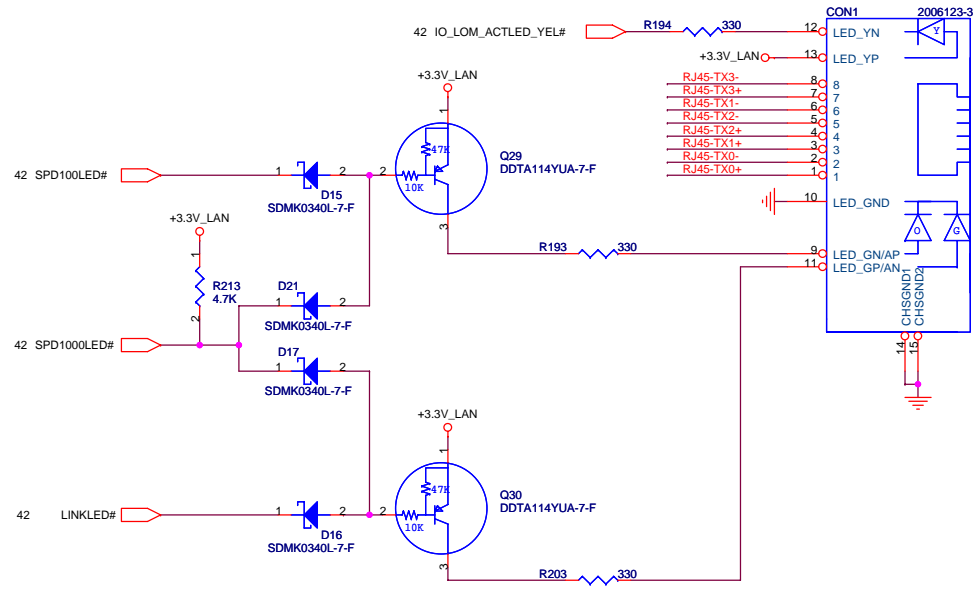
	5784M	5787M
R503	39k	0
R497	20k	*20k_NC

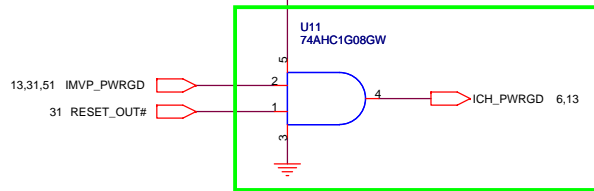
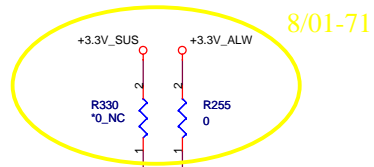
Note:thermal pad

TRANSFORM TRANSFORM



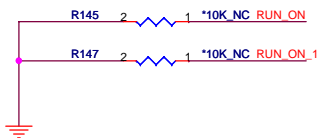
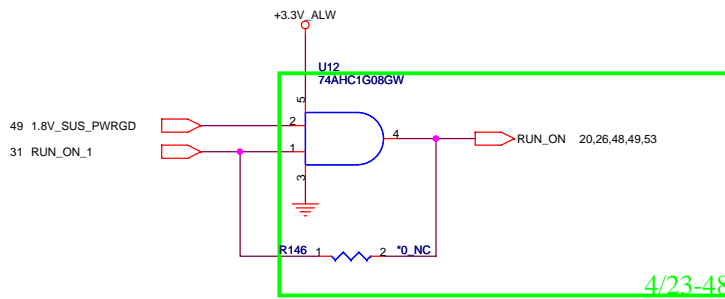
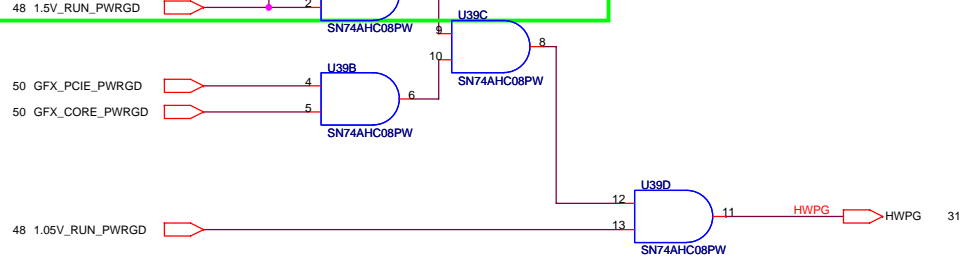
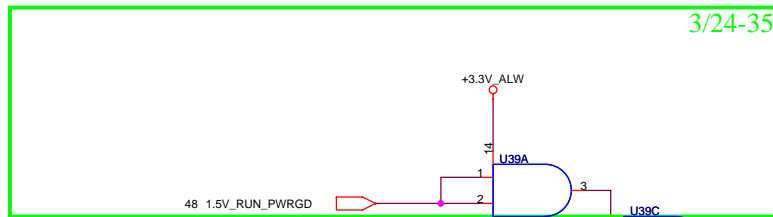
RJ-45 Connector





4/23-48

Keep Away from high speed buses



1

2

3

4

5

A

A

B


B

C

C

D

D

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Title Battery Selector			
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1

2

3

4

5

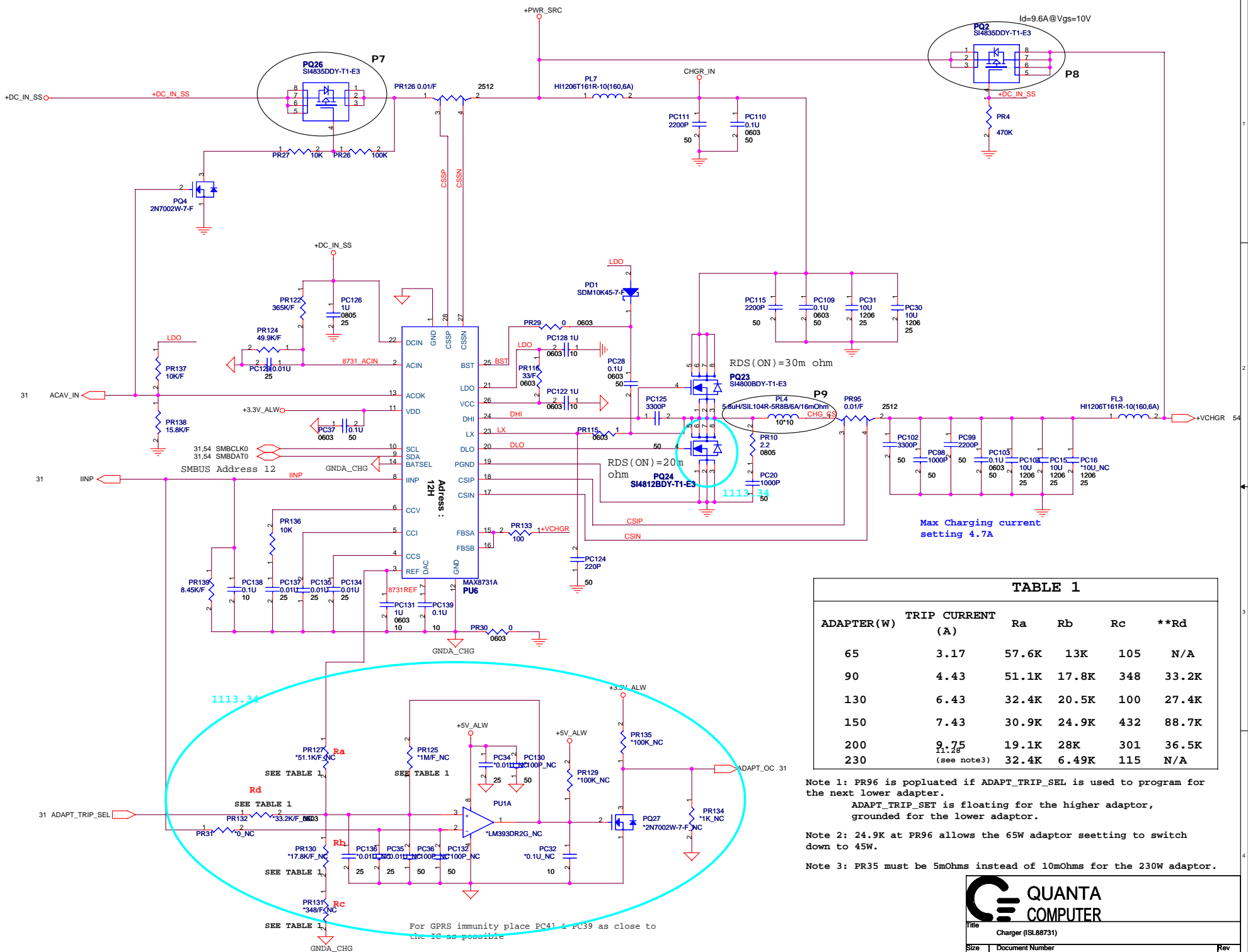


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.


Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

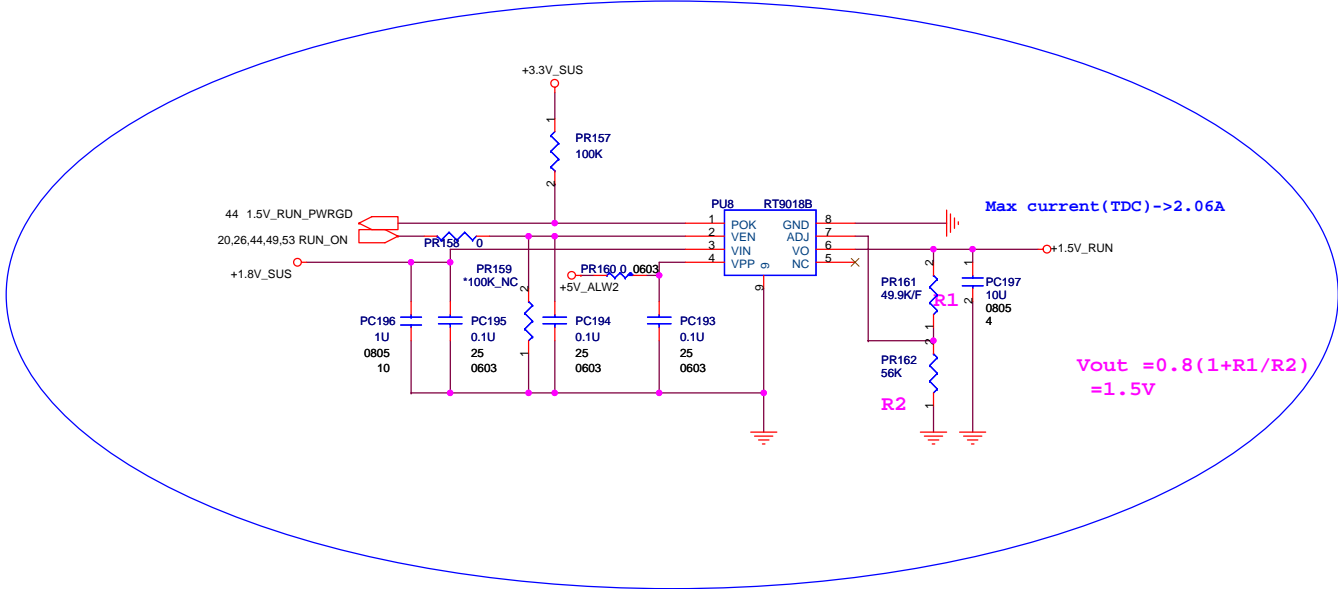
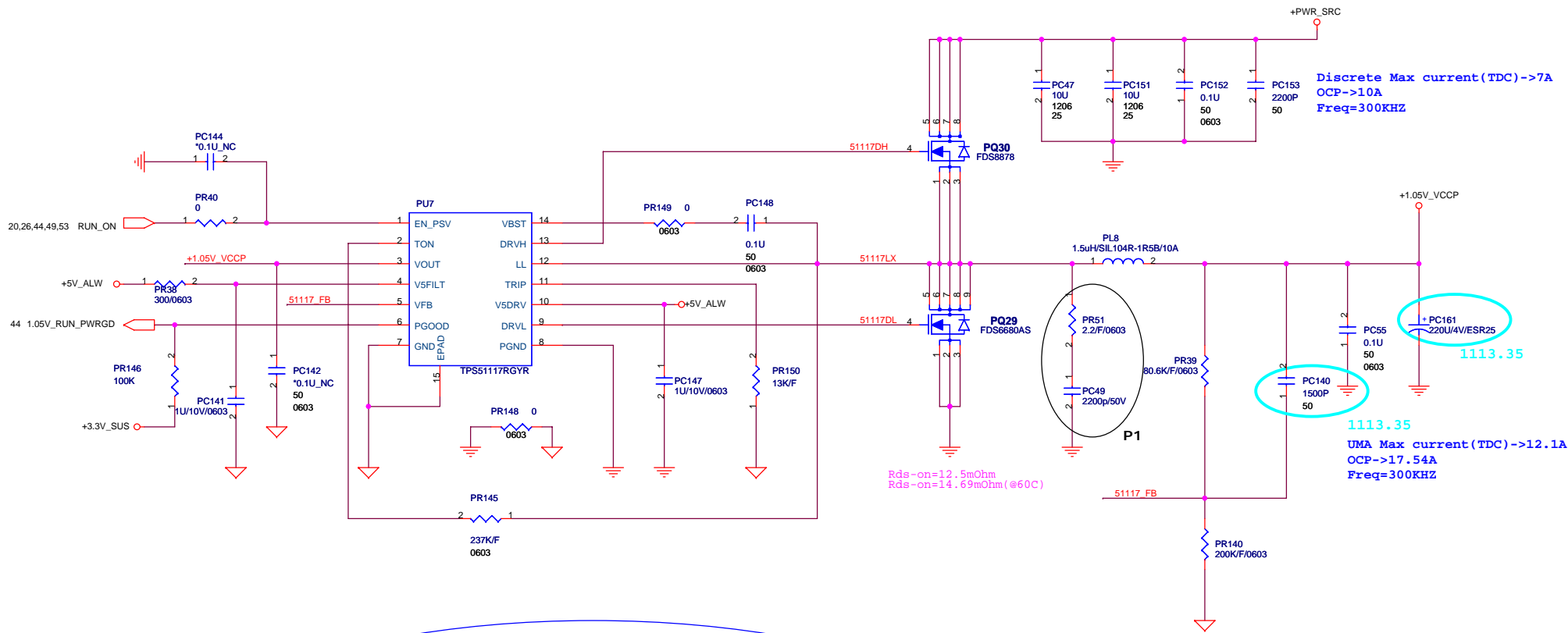
For GPRS immunity place PC41 & PC39 as close to the IC as possible

QUANTA COMPUTER

Title Charger (ISL88731)		
Size FM7	Document Number FM7	Rev 1A
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Title		
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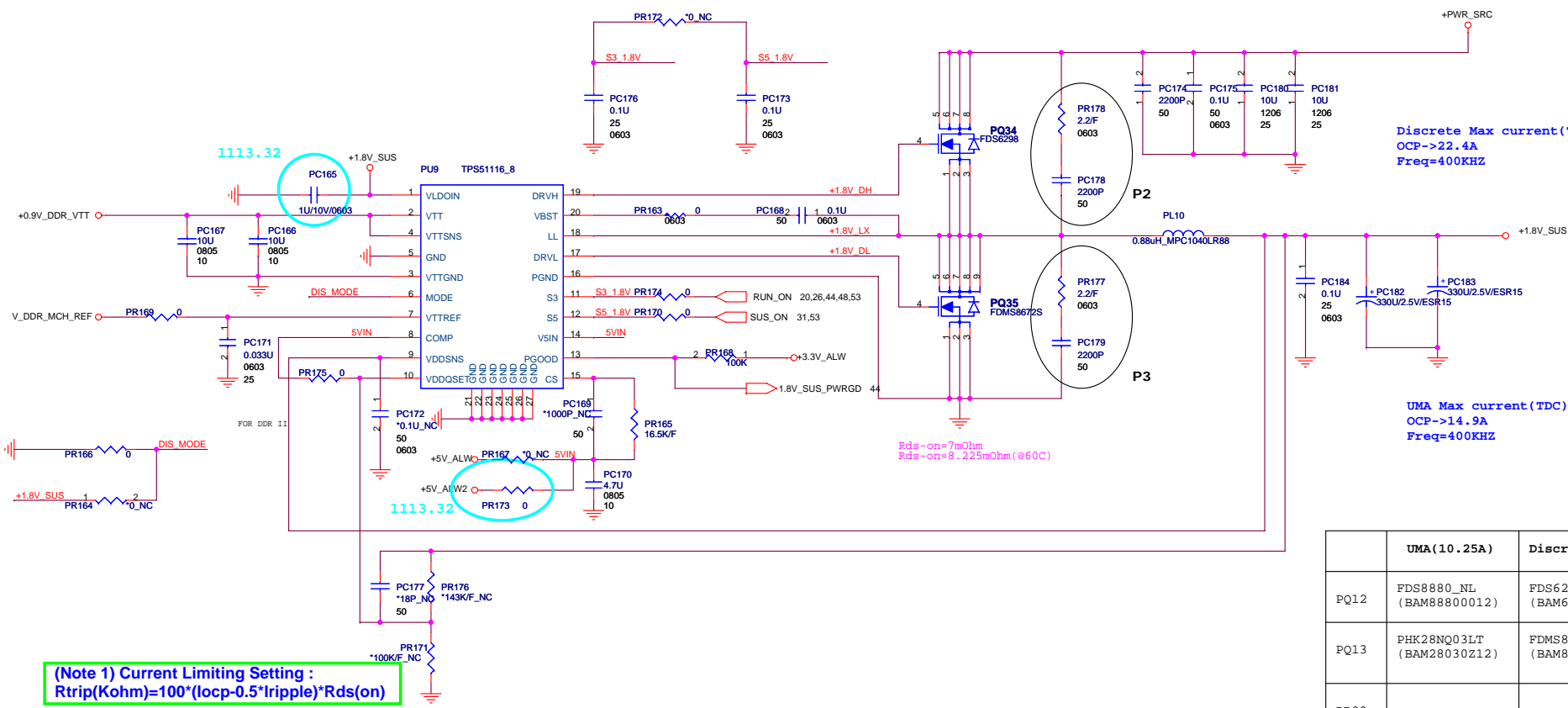
	UMA (12.1A)	Discrete (7A)
PQ22	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ25	FDS6676AS_NL (BAM66760026)	FDS6680AS (BAM66800061)
PL25	SIL105RA-1R5-R (CV-15F0M208)	SIL104R-1R5PF (DC-15A00010)
PR452	9.09K/F (CS29092FB27)	10K/F (CS31002FB26)

QUANTA COMPUTER

Title: 1.05_VCCP & 1.5V_RUN

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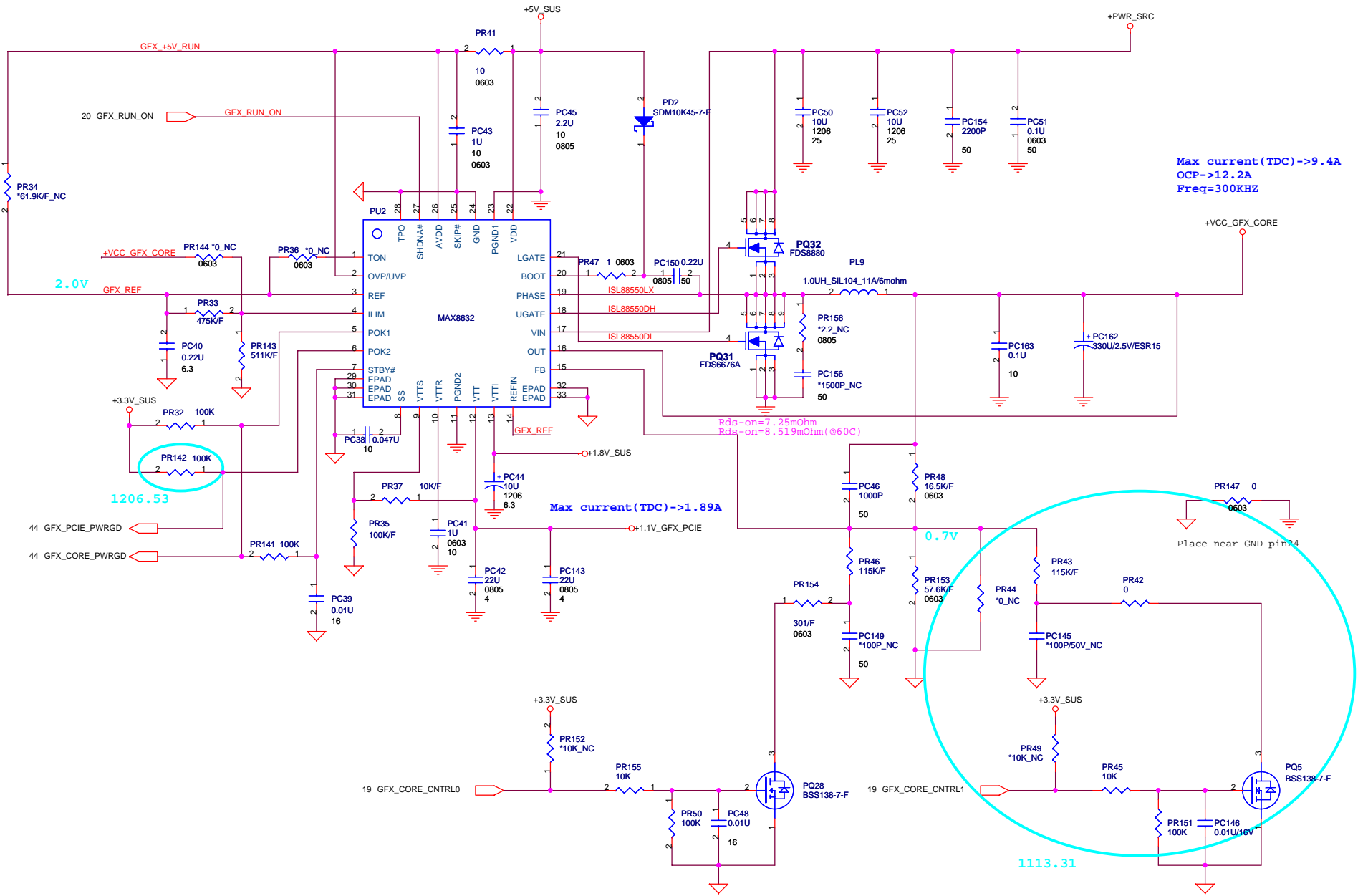


Discrete Max current (TDC)->15.6A
 OCP->22.4A
 Freq=400KHZ

UMA Max current (TDC)->10.25A
 OCP->14.9A
 Freq=400KHZ

(Note 1) Current Limiting Setting :
 $R_{trip}(Kohm)=100*(I_{ocp}-0.5*I_{ripple})*R_{ds(on)}$

	UMA (10.25A)	Discrete (15.6A)
PQ12	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ13	PHK28NQ03LT (BAM28030212)	FDMS8672S (BAM86720000)
PR83		



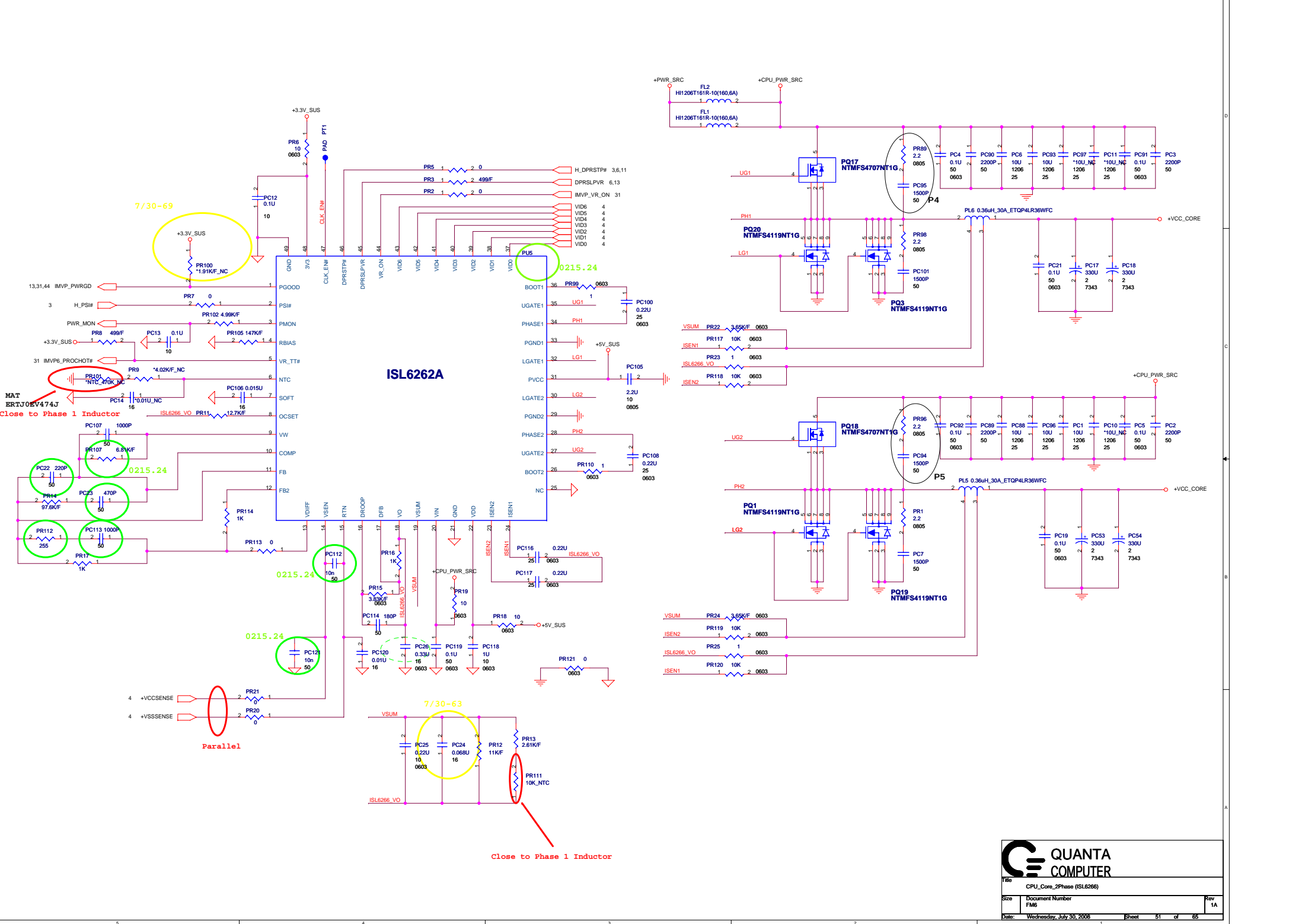
Max current (TDC) -> 9.4A
 OCP -> 12.2A
 Freq=300KHZ

Max current (TDC) -> 1.89A

1113.31

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9
HIGH	LOW	1.0V
HIGH	HIGH	1.1V





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Close to Phase 1 Inductor

0215.24

0215.24

0215.24

Parallel

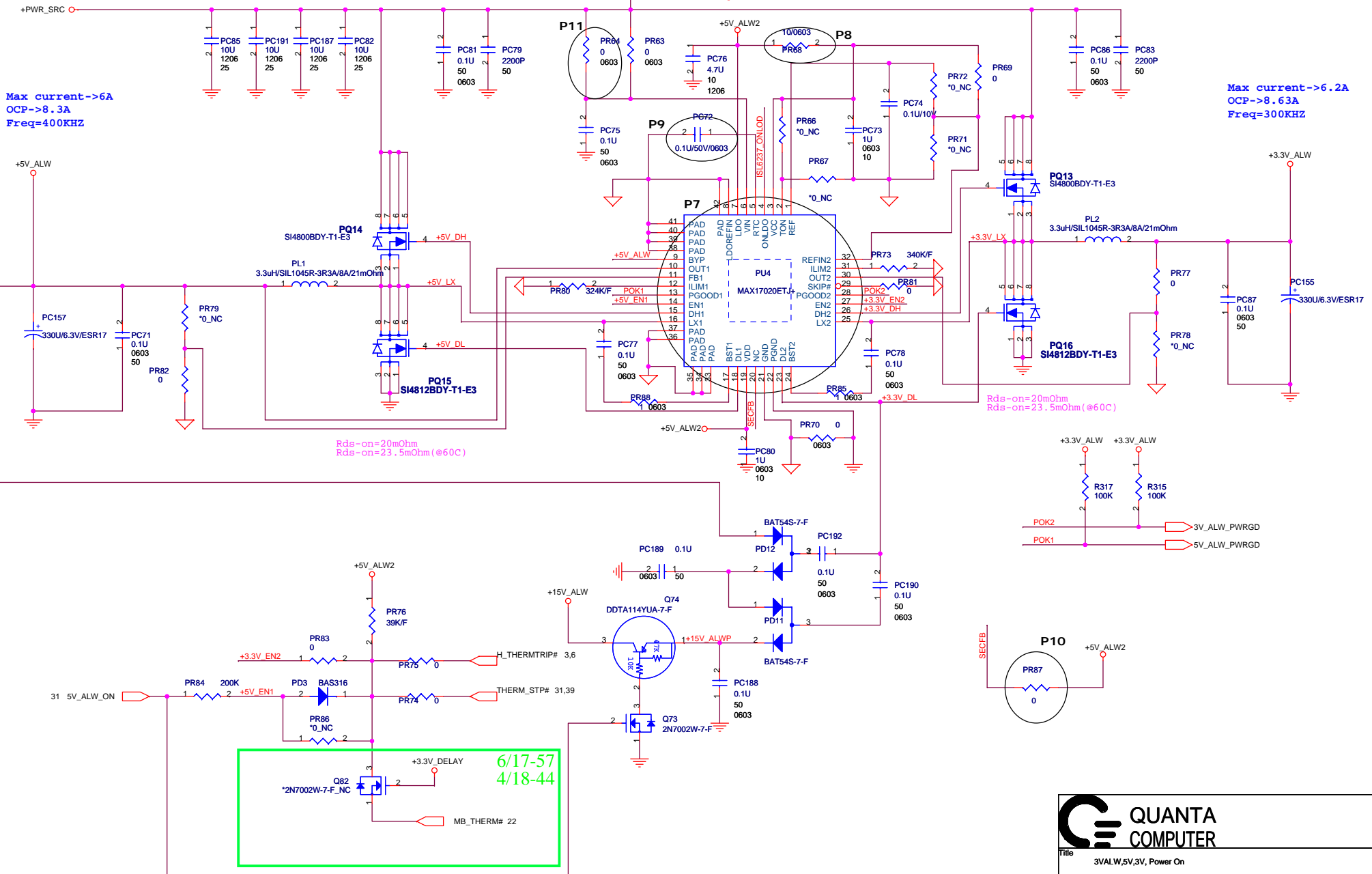
7/30-63

Close to Phase 1 Inductor

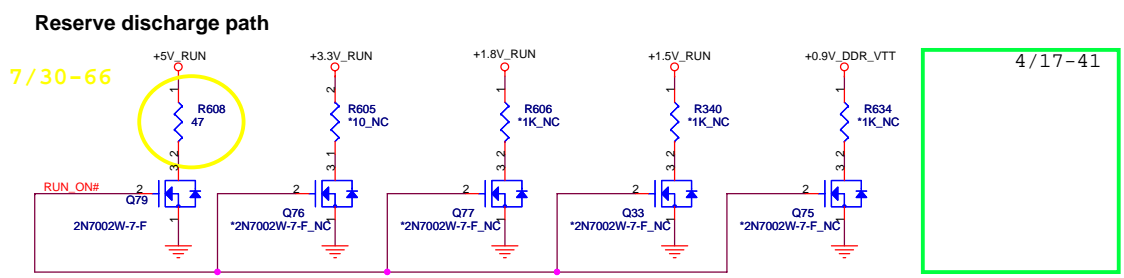
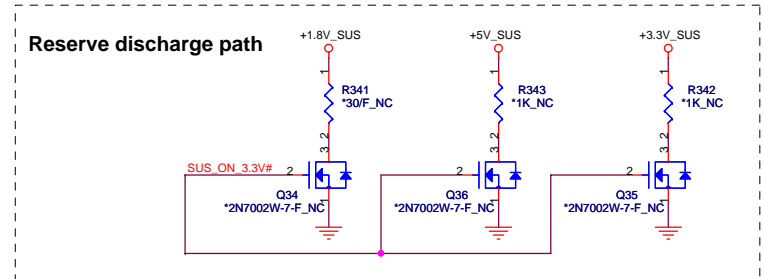
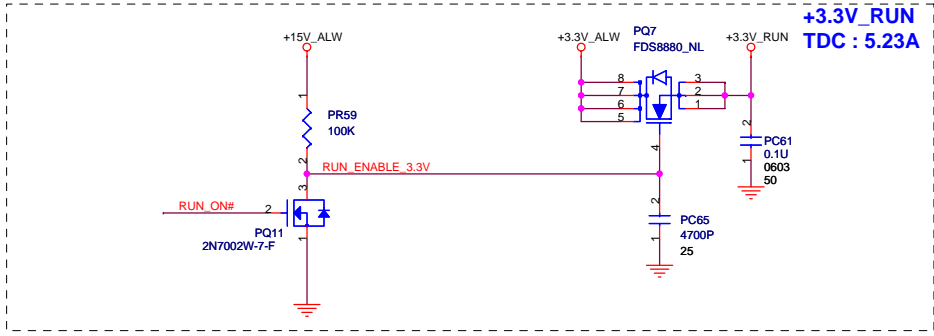
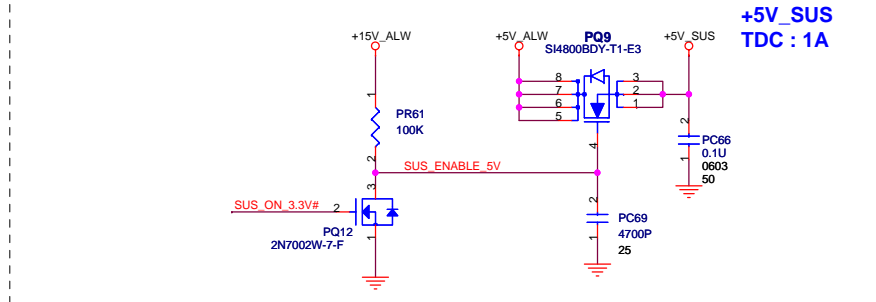
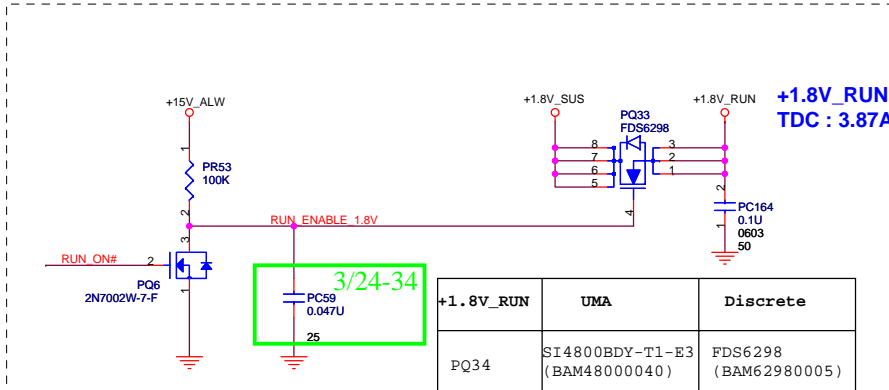
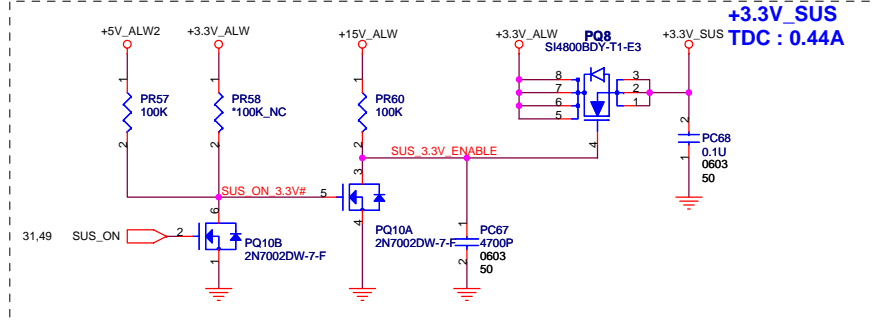
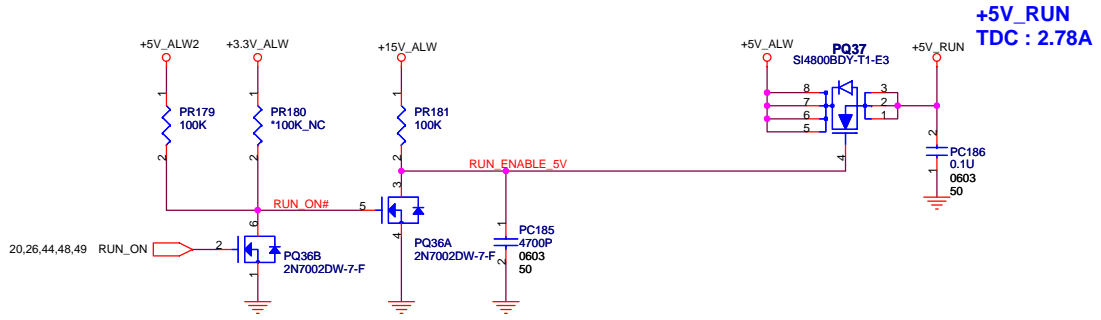
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs



Title		
3VALW.5V.3V, Power On		
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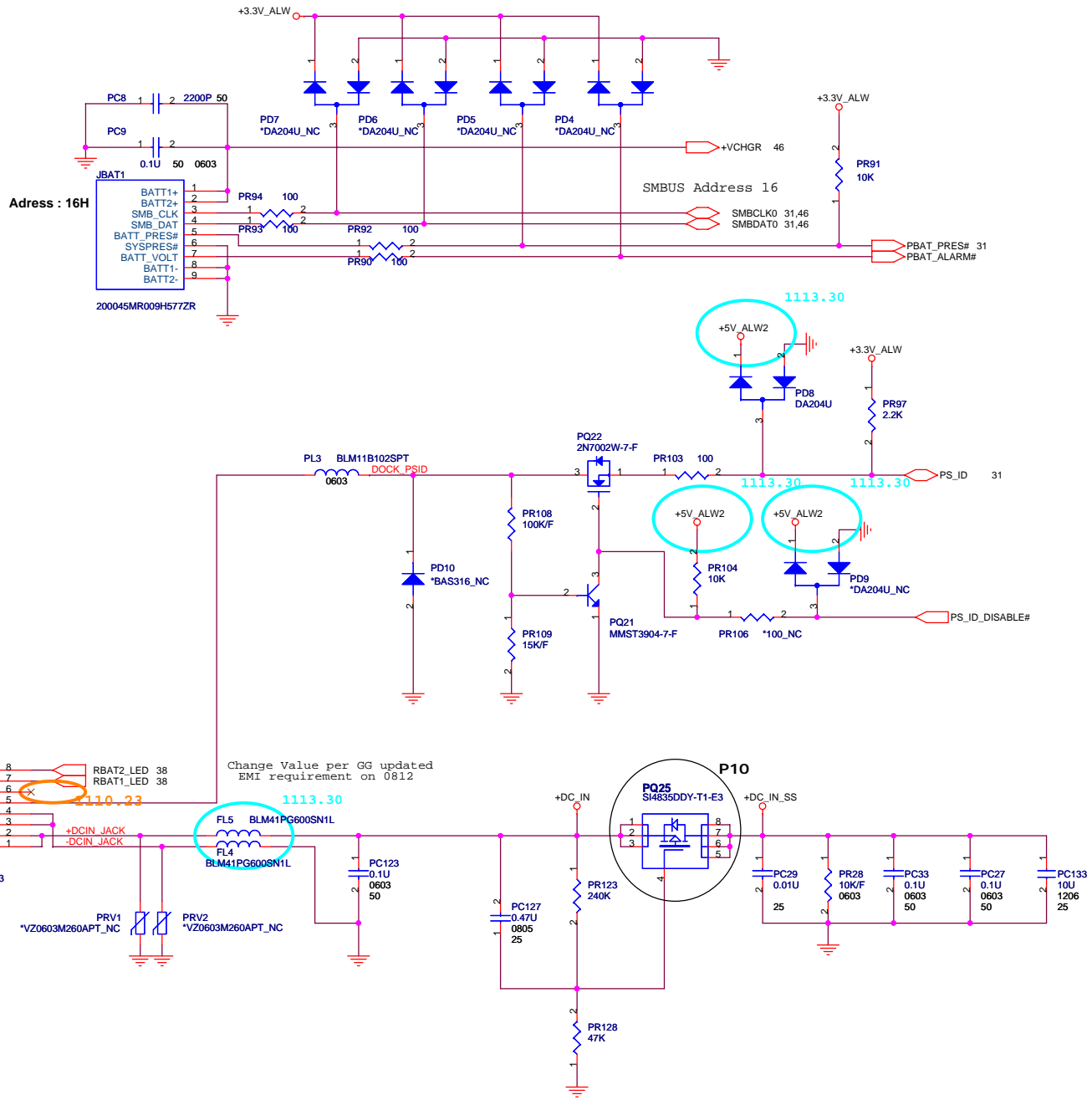


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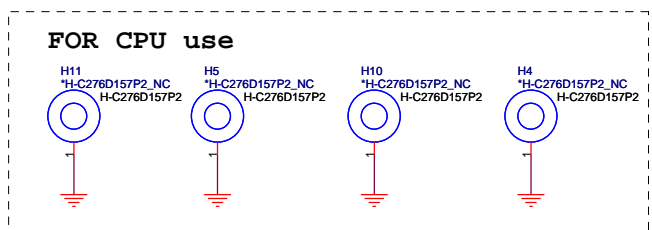
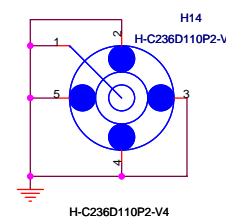
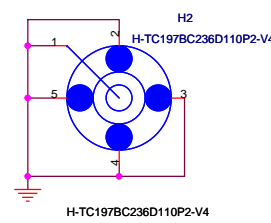
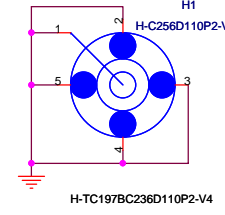
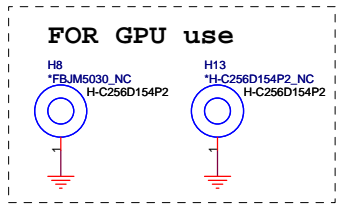
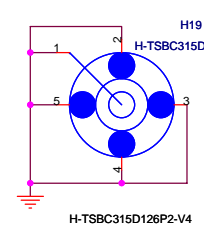
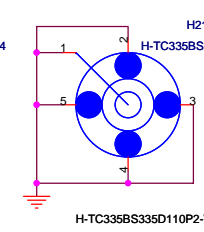
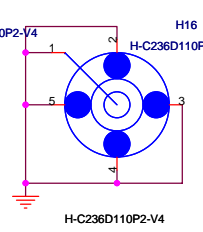
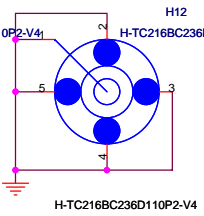
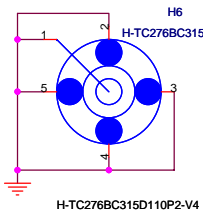
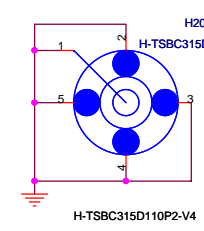
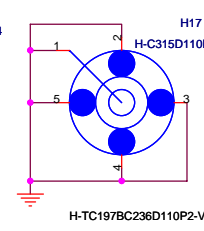
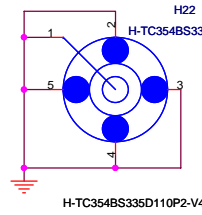
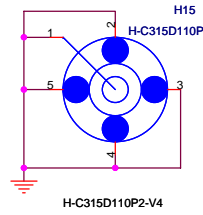
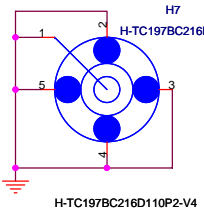
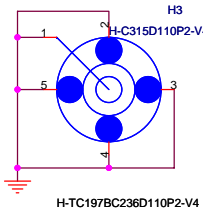
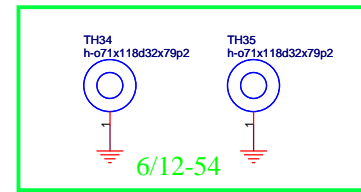
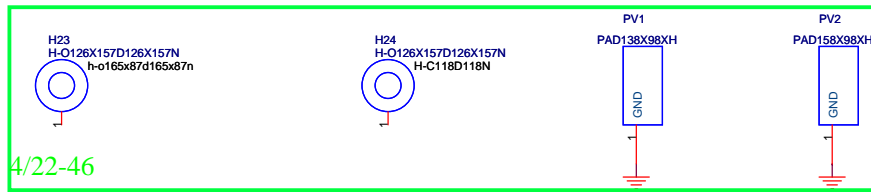
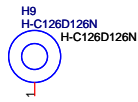
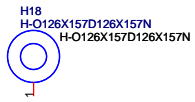
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Title DCIN, BATT CONNECTOR		
Size FMT	Document Number FMT	Rev 1A
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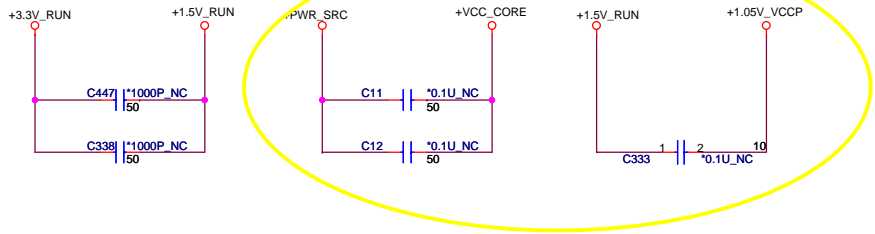
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Reserved for EMI.

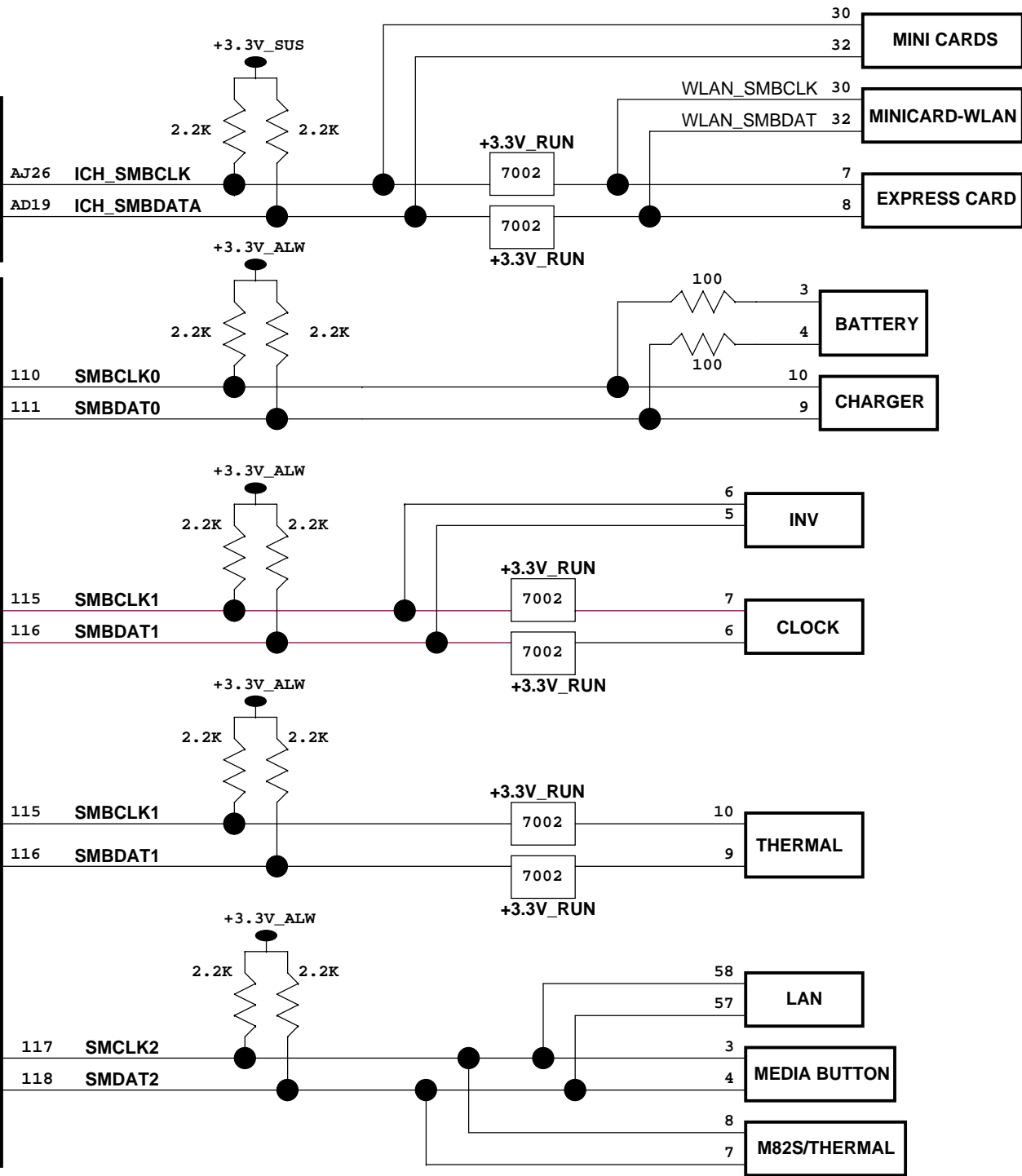
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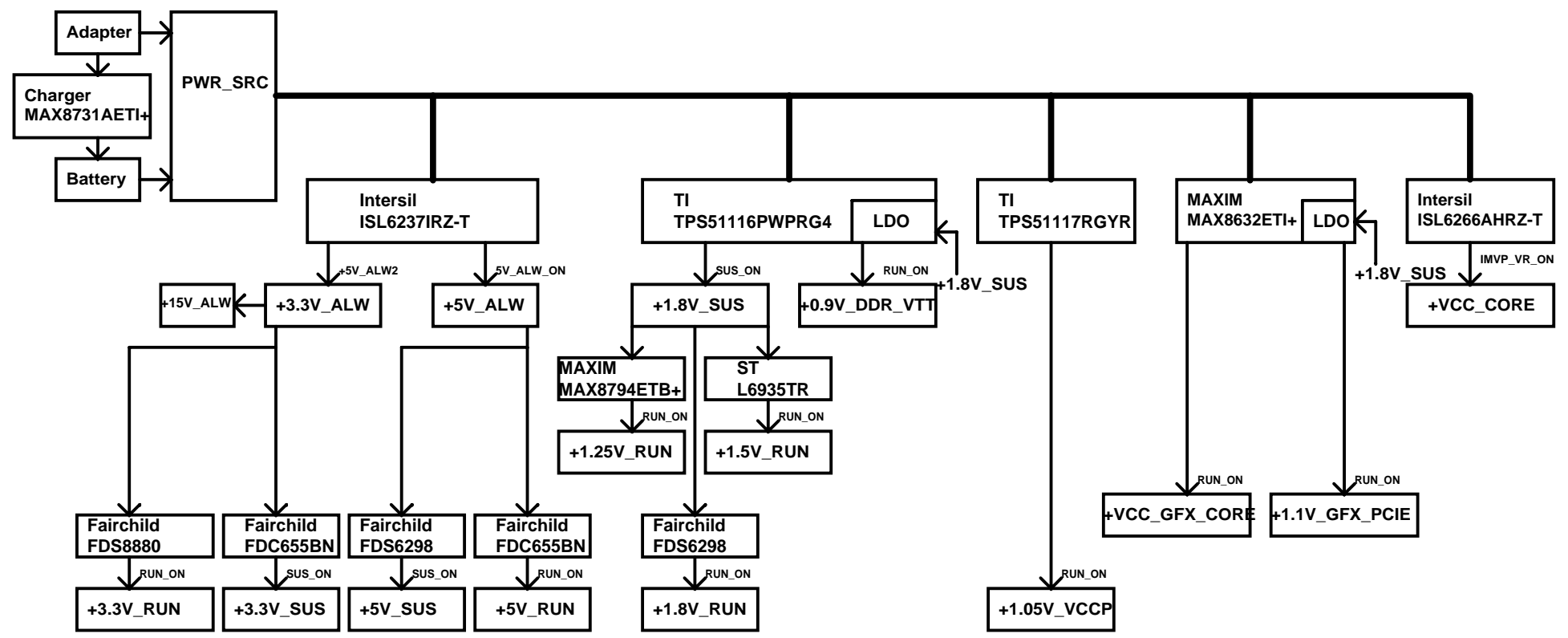


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Title: EMI CAP		
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ICH8-M

**SIO
ITE8512**





Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	1	3	2-13-08				Debug port needs to be updated for MV	Change the BOM, and add a pull high circuit on ITP_BPM#5
	2	3	2-13-08				H_THERM circuit has risk	Change the BOM in order to make it same with FM6
	3	8	2-13-08				VCC_AXG and VCC_AXG_NCTF are different with MV DG	Change VCC_AXG, and VCC_AXG_NCTF to ground
	4	11, 35	2-13-08				Add E-SATA function	Refer to page 11 and 35
	5	13	2-13-08				Some power rails don't mach with DG	Refer to page 13
	6	17	2-13-08				BSEL0, BSEL1, and BSEL2's seris resistors don't mach with DG	Refer to page 17
	7	9	2-13-08				VCCA_SM doesn't mach with DG	Add 0-ohm in order to make it same with other project
	8	9	2-13-08				VCCD_TVDAC and VCCD_QDAC are different with DG	Grond VCCD_TVDAC and update another circuit for VCCD_QDAC
	9	19,22	2-13-08				Change the power rail for avoiding leakage during power up	Change +3.3V_RUN to +3.3V_DELAY
	10	37	2-13-08				MMB vender changed it's F/W to fix the LED flash issue. Change Num/Cap LED circuit for avoiding leakage voltage	Change the circuit, refer to page 37
	11	35	2-13-08				Fulfill reliability's request	Add one more power pin on connector
	12	31	2-13-08				New chip version for ITE	Change the circuit
	13	40,42	2-13-08				Change chip version for Codec and LOM	Done
	14	41	2-13-08				Approve DMIC'S performance according to IDT's recommendation	Change o-ohm to 22-ohm
	15	26	2-16-08				DDC BUS for HDMI Certificate	Add Level Shift on DDC BUS of HDMI
	16	40,41	2-16-08				Need to meet WLP4.0	Refer to page 40 and 41
	17	31	2-16-08				Add audio solution for PO noise issue when loading driver	Connect ICH_AZ_CODEC_RST# to SIO.22
	18	14	2-18-08				Reserve +1.5V_SUS for VCCSUSHDA	Add a LDO and reserve 0-ohm for +1.5V_SUS
	19	13	2-18-08				Avoid leakage voltage	Follow the SR FM6 design
	20	17	2-19-08				After FAE review, modify circuit in order to let wave form smooth	Add two 0.1u cap
	21	17	2-20-08				After FAE review, modify circuit for single end nets	change 0-ohm to 33-ohm, add pull high resistor
	22	35	2-20-08				Add E-SATA redriver function	Refer to page 35
	23	42	2-21-08				According to FAE, stub a resister	Refer to page 42
	24	17	2-21-08				In order to meet spec, we need to swap two signals	Refer to page 17
	25	35	2-22-08				Co-work with GM3 team and decide to take USB charger function off	Refer to page 35
	26	21	2-22-08				According to realiability team request, change BOM	Change L51
	27	12	2-25-08				Need to meet Dell USB port requirement	Refer to page 12
	28	19	2-25-08				FAE's suggestion is add ground	Refer to page 19
	29	13,37	2-25-08				Add one pin for LCD inverter det	Refer to pages
	30	30	3-03-08				Footprint is wrong for express card	Refer to FM6 footprint
	31	32 35	3-24-08				Change locations for USB and Coin Battery for safty requirement	Refer to those pages
	32	26 35	3-24-08				Change BOM for HDMI and E-sata	Refer to those pages
	33	49	3-24-08				Del 1.25V power rail	Refer to page 49
	34	53	3-24-08				Change BOM for correcting power sequence	Refer to page 53



Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	35	44	3-24-08				Change system reset circuit	Refer to page 44
	36	19	3-28-08				Change HDMI detect circuit	Refer to page 19
	37	26	3-28-08				In order to pass HDMI 7-13 item	Change diode, which has only 2pF internal capacitance
	38	31	3-28-08				ITE EC hardware issue	Del a cap
	39	1,31	4-03-08				Get schematic ready for PT build	Change block diagram and Board ID strap pin
	40	28	4-09-08				Leakage voltage issue	Change 0-ohm to diode
	41	53	4-17-08				1.25V_RUN discharge voltage is no need	Remove it
	42	30,35 26 27	4-17-08				EMI Issue	Refer to pages
	P1	48	4-17-08				For EMI suggested	populate 2.2ohm in PR56 and 1500pf in PC49
	P2	49	4-17-08				For EMI suggested	populate 2.2ohm in PR178 and 1500pf in PC178
	P3	49	4-17-08				For EMI suggested	populate 2.2ohm in PR177 and 1500pf in PC179
	P4	51	4-17-08				For EMI suggested	populate 2.2ohm in PR89 and 1500pf in PC95
	P5	51	4-17-08				For EMI suggested	populate 2.2ohm in PR96 and 1500pf in PC94
	P6	48	4-17-08				LDO cost issue	Change one LDO to another vender
	43		4-18-08				Change connectors PN due to connector list changes J2,JP1,JP2,J3,JSIM1,J5,J6,BT1., AND JDIM2	Refer to locations
	44	52	4-18-08				ATI OTP circuit redesigned	Refer to page 52
	45	28	4-18-08				the leakage voltage can be solved by EC	Change diode back to resister
	46	55	4-22-08				Layout team request two hole footprints and EMI spring	Refer to page 55
47	37	4-22-08				K/B B/L circuit change to high active	Refer to page 37	
48	3 44	4-23-08				BOM change for CPU and system reset circuit	Change Resister value to 56 ohm for proshot pin and AND gate PN	

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
FM7	49	38	5-29-08				The brightness is not light enough	Change R432 from 220 ohm to 68 ohm
	50	26	5-29-08				Secound sources team ask to change the diode PN.	Change D27 to another PN, which use on the other pages
	51	9	5-29-08				The diode PN is not on DELL PSL	Change PN
	52	35	5-29-08				Remove E-sata redriver	Refer to page 35
	53	13	6-11-08				Dell asks us to support KB_DET function	Add 0-ohm, which make the schematic work
	54	55	6-12-08				EMI request to change EMI spring PN and location Factory asks us to have a housing for CIR	Rerer to page 55
	55	40	6-16-08				Audio codec has new version	Change PN
	56	35	6-16-08				USB power IC is going to pass UL, so we will need to change it to new one	Change PN
	57	52	6-17-08				DELL's request on thermal detect pin	Refer to page 52
	58	3	6-27-08				Follow INTEL CRB and schematic checl list 2.0	De-pop H_RESET# PU resistor

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