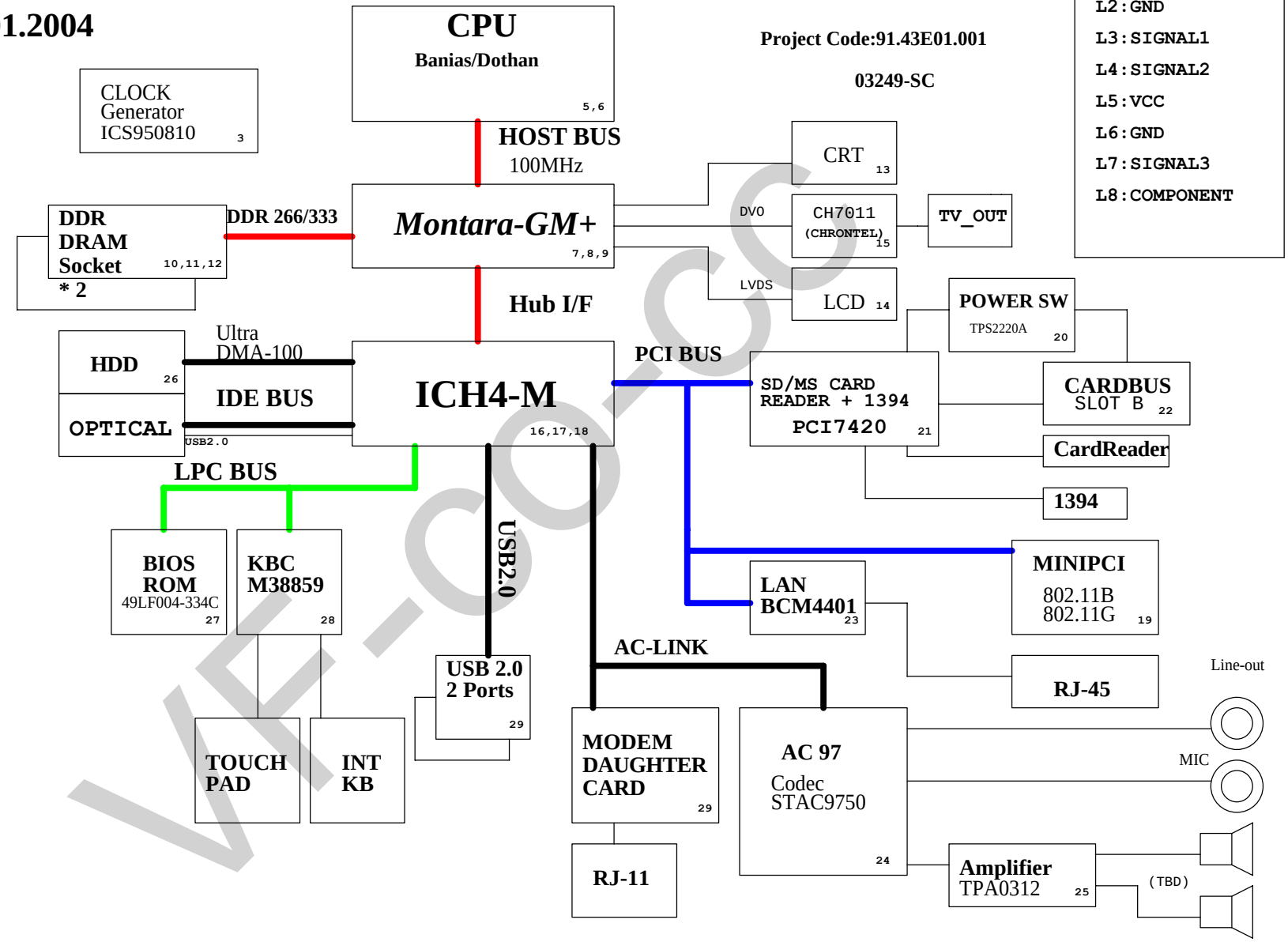
MOLOKAI Block Diagram

SPR.01.2004

Project Code:91.43E01.001

03249-SC



DC/DC IMVP4
Switching Power
ISL6218 32

INPUTS	OUTPUT
DCBATOUT	VCC_CORE

SYSTEM DC/DC
MAX1715 34

INPUTS	OUTPUTS
DCBATOUT	1D35V_S0 2D5V_S3

DC/DC&CHARGER
MAX1645 35

INPUTS	OUTPUTS
AD+	BT+

DC/DC
MAX1999 33

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

G913C/APL1085
APL5331kAC/G1211X 38

INPUTS	OUTPUTS
3D3V_S0	1D8V_VCCA_S0
3D3V_S5	1D5V_S5
3D3V_S0	1D5V_S0
2D5V_S3	1D25V_S0
1D35V_S0	VCC_IO_S0

PCB LAYER

L1:COMPONENT
L2:GND
L3:SIGNAL1
L4:SIGNAL2
L5:VCC
L6:GND
L7:SIGNAL3
L8:COMPONENT

Wistron Confidential

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Monday, April 05, 2004	Sheet 1 of 39	

S5

5V_S5 — 5V_S5 18,33,34,36
3D3V_S5 — 3D3V_S5 4,16,17,18,28,30,31,33,36,38,39
1D5V_S5 — 1D5V_S5 18,38
VCC_RTC_S5 — VCC_RTC_S5 17

S3

3D3V_S3 — 3D3V_S3 14,25,28,30,34,36,39
2D5V_S3 — 2D5V_S3 7,9,10,11,34,38,39
1D25V_DDRVREF_S3 — 1D25V_DDRVREF_S3 7,10,34

S0

5V_S0 — 5V_S0 13,14,17,18,19,20,24,26,28,30,32,34,36,38,39
3D3V_S0 — 3D3V_S0 3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,30,31,32,36,38,39
1D5V_S0 — 1D5V_S0 7,8,9,15,16,18,27,38,39
1D25V_S0 — 1D25V_S0 11,12,38
1D35V_S0 — 1D35V_S0 7,9,34,38,39
VCC_CORE_S0 — VCC_CORE_S0 6,32,39
VCC_IO_S0 — VCC_IO_S0 4,5,6,7,9,17,18,32,38,39
1D8V_VCCA_S0 — 1D8V_VCCA_S0 5,38

AC-IN / BAT.-IN

AD+ — AD+ 35,37,39
DCBATOUT — DCBATOUT 14,32,33,34,35,36,38,39

LAN-AC

3D3V_LAN_S5AC — 3D3V_LAN_S5AC 23,29,36,37

5VA_AUD_S3 — 5VA_AUD_S3 24 → AUDIO

3D3V_LCD_S0 — 3D3V_LCD_S0 14 → LCD

CRT_VCC_S0 — CRT_VCC_S0 13 → CRT

TV3D3V1_S0 — TV3D3V1_S0 15
TV3D3VA_S0 — TV3D3VA_S0 15
TV3D3V2_S0 — TV3D3V2_S0 15
TV1D5V_S0 — TV1D5V_S0 15
→ TV-OUT

OTHERS

5V_AUX — 5V_AUX 30,31,33,35,37,38,39
3D3V_AUX — 3D3V_AUX 14,17,33

3D3V_RTC — 3D3V_RTC 17,28
ICH_VBIAS — ICH_VBIAS 17
MAX1999_REF — MAX1999_REF 33,38

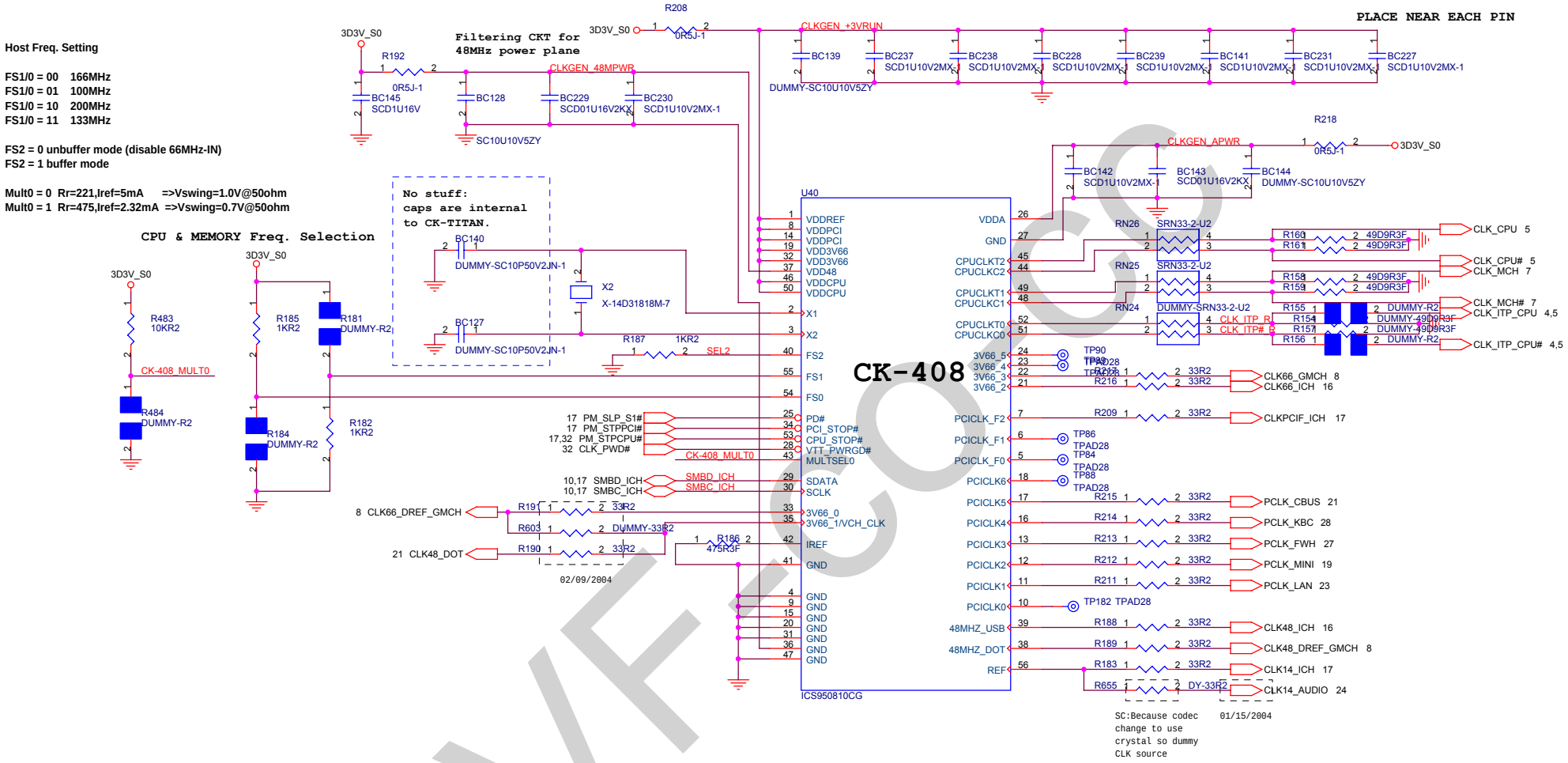
MAX1999_VCC — MAX1999_VCC 33

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
SD/MS CARD READER+1394 PCI7420	AD20	PIRQB# PIRQC# PIRQF#	REQ#1 / GNT#1
MINI PCI 802.11B/G	AD17	PIRQE# PIRQG#	REQ#0 / GNT#0
LAN BCM4401	AD21	PIRQD#	REQ#4 / GNT#4

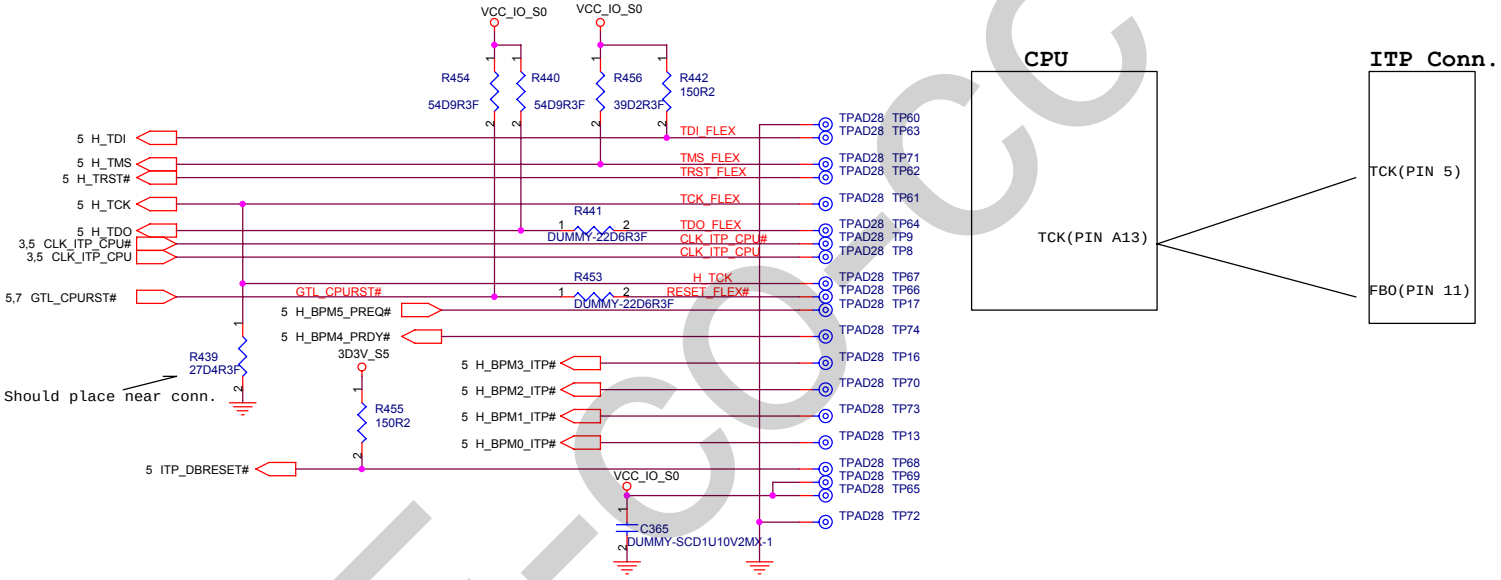
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content
Size: A3 | Document Number: MOLOKAI | Rev: SC
Date: Saturday, April 17, 2004 | Sheet 2 of 39



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Clock GEN.		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 3 of 39	

ITP Debug Pad



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 4 of 39	

CPU VCCA POWER:

At Dothan CPU application, POWER is 1.5V or 1.8V.

For CPU VCCA[0:3] PLL place one 0.01u & 10u for each VCCA pin

1D8V_VCCA_S0

BC87 DY-SC10U6D3V5MX
BC75 SC10U6D3V5MX
BC108 DY-SC10U6D3V5MX
BC104 DY-SC10U6D3V5MX
BC106 SCD01U16V2KX
BC105 SCD01U16V2KX
BC86 SCD01U16V2KX
BC90 SCD01U16V2KX

U68D

3 CLK_CPU
3 CLK_CPU#
3,4 CLK_ITP_CPU
3,4 CLK_ITP_CPU#
BCLK0
BCLK1
ITP_CLK0
ITP_CLK1

17 CC_A20M#
17 CC_FERR#
17 CC_IGNNE#
CC_FERR#
A20M#
FERR#
IGNNE#

17 CC_INTR
17 CC_NMI
LINT0
LINT1

17 CC_SMI#
17 CC_STPCLK#
SMI#
STPCLK#

1D8V_VCCA_S0
VCCA3 120mA
VCCA2
VCCA1
VCCA0

RSVD
TP_CLK0
TP_CLK1
TEST3
TP19
TPAD28

17 CC_CPUSLP#
4 H_TCK
H_TCK
SLP#
TCK

4 H_TDI
4 H_TDO
H_TDI
H_TDO
TDI
TDO

TP12
TPAD28
VCCSENSE
VSSSENSE

32 H_VID[5:0]
H_VID5
H_VID4
H_VID3
H_VID2
H_VID1
H_VID0
VID5
VID4
VID3
VID2
VID1
VID0

R131 DUMMY-54D9R3F
R132 DUMMY-54D9R3F

BGA479-SKT-2-U

Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
COMP1 and COMP3 should be routed asx Zo=54.9ohm, traces shorter than 0.5".

BPM3# H_BPM3_ITP# H_BPM3_ITP# 4
BPM2# H_BPM2_ITP# H_BPM2_ITP# 4
BPM1# H_BPM1_ITP# H_BPM1_ITP# 4
BPM0# H_BPM0_ITP# H_BPM0_ITP# 4

COMP3 AB1 27D4-3 R135 54D9R3F
COMP2 AB2 27D4-1 R136 27D4R3F
COMP1 P26 27D4-4 R110 54D9R3F
COMP0 P25 27D4-2 R109 27D4R3F

DPSLP# B7 CC_DPSLP# 7,17

GTLREF3 AC1
GTLREF2 G1
GTLREF1 E26
GTLREF0 AD26

VCC_IO_S0
R108 1KR2F
SC: Change to 1KR2F for GTLREF pass
Voltage divider placed within 0.5" of CPU pin via a Zo=55ohm trace.
H_GTLREF_0
2/3 RATIO
R107 2KR3F
C134 DUMMY-SCD01U16V

PROCHOT# B17 CC_PROCHOT#
PWRGOOD E4 CC_CPUPWRGD CC_CPUPWRGD 7,17

TEST1 C5 TEST1 TP6 TPAD28
TEST2 F23 TEST2 TP15 TPAD28
THERMDA B18 TPAD28
THERMDC A18
THERMTRIP# C17
THERMDP1 30
C165 SC1000P50V
THERMDN 30
PM_THERMTRIP# 17
TMS C11 H_TMS H_TMS 4
TRST# B13 H_TRST# 4
R115 680R2

VCC_IO_S0
GTL_IERR# R450 56R2J
CC_CPUPWRGD R133 330R2
CC_PROCHOT# R114 56R2J

VCC_IO_S0
R116 150R2
H_TDI
R113 DUMMY-1KR2

U68C

7 GTL_D#[15..0]
GTL_D#15 C25 D15#
GTL_D#14 E23 D14#
GTL_D#13 B23 D13#
GTL_D#12 C26 D12#
GTL_D#11 E24 D11#
GTL_D#10 D24 D10#
GTL_D#9 B24 D9#
GTL_D#8 C20 D8#
GTL_D#7 B20 D7#
GTL_D#6 A21 D6#
GTL_D#5 B26 D5#
GTL_D#4 A24 D4#
GTL_D#3 B21 D3#
GTL_D#2 A22 D2#
GTL_D#1 A25 D1#
GTL_D#0 A19 D0#

D47# Y25 GTL_D#47
D46# AA26 GTL_D#46
D45# Y23 GTL_D#45
D44# V26 GTL_D#44
D43# U25 GTL_D#43
D42# V24 GTL_D#42
D41# U26 GTL_D#41
D40# AA23 GTL_D#40
D39# R23 GTL_D#39
D38# R26 GTL_D#38
D37# R24 GTL_D#37
D36# V23 GTL_D#36
D35# U23 GTL_D#35
D34# T25 GTL_D#34
D33# AA24 GTL_D#33
D32# Y26 GTL_D#32
GTL_D#[47..32] 7

7 GTL_DINV#0 D25 DINV0#
7 GTL_DSTBN#0 C23 DSTBN0#
7 GTL_DSTBP#0 C22 DSTBP0#
DINV2# T24 GTL_DINV#2 7
DSTBN2# W25 GTL_DSTBN#2 7
DSTBP2# W24 GTL_DSTBP#2 7

7 GTL_D#[31..16]
GTL_D#31 K25 D31#
GTL_D#30 N25 D30#
GTL_D#29 H26 D29#
GTL_D#28 M25 D28#
GTL_D#27 N24 D27#
GTL_D#26 L26 D26#
GTL_D#25 J25 D25#
GTL_D#24 M23 D24#
GTL_D#23 J23 D23#
GTL_D#22 G24 D22#
GTL_D#21 F25 D21#
GTL_D#20 H24 D20#
GTL_D#19 M26 D19#
GTL_D#18 L23 D18#
GTL_D#17 G25 D17#
GTL_D#16 H23 D16#

D63# AF26 GTL_D#63
D62# AF22 GTL_D#62
D61# AF25 GTL_D#61
D60# AD21 GTL_D#60
D59# AF21 GTL_D#59
D58# AF20 GTL_D#58
D57# AD24 GTL_D#57
D56# AF23 GTL_D#56
D55# AE22 GTL_D#55
D54# AD23 GTL_D#54
D53# AC25 GTL_D#53
D52# AC22 GTL_D#52
D51# AC20 GTL_D#51
D50# AB24 GTL_D#50
D49# AC23 GTL_D#49
D48# AB25 GTL_D#48
GTL_D#[63..48] 7

7 GTL_DINV#1 J26 DINV1#
7 GTL_DSTBN#1 K24 DSTBN1#
7 GTL_DSTBP#1 L24 DSTBP1#
DINV3# AD20 GTL_DINV#3 7
DSTBN3# AE24 GTL_DSTBN#3 7
DSTBP3# AE25 GTL_DSTBP#3 7

BGA479-SKT-2-U

U68B

7 GTL_A#[16..3]
GTL_A#16 AA2 A16#
GTL_A#15 Y3 A15#
GTL_A#14 AA3 A14#
GTL_A#13 U1 A13#
GTL_A#12 Y1 A12#
GTL_A#11 Y4 A11#
GTL_A#10 W2 A10#
GTL_A#9 T4 A9#
GTL_A#8 W1 A8#
GTL_A#7 V2 A7#
GTL_A#6 R3 A6#
GTL_A#5 V3 A5#
GTL_A#4 U4 A4#
GTL_A#3 P4 A3#

7 GTL_ADSTB#0 U3 ADSTB0#

7 GTL_A#[31..17]
GTL_A#31 AF1 A31#
GTL_A#30 AE1 A30#
GTL_A#29 AF3 A29#
GTL_A#28 AD6 A28#
GTL_A#27 AE2 A27#
GTL_A#26 AD5 A26#
GTL_A#25 AC6 A25#
GTL_A#24 AB4 A24#
GTL_A#23 AD2 A23#
GTL_A#22 AE4 A22#
GTL_A#21 AD3 A21#
GTL_A#20 AC3 A20#
GTL_A#19 AC7 A19#
GTL_A#18 AC4 A18#
GTL_A#17 AF4 A17#

7 GTL_ADSTB#1 AE5 ADSTB1#

BGA479-SKT-2-U

TP18 TPAD28

ADS# N2 GTL_ADS# 7
BNR# L1 GTL_BNR# 7
BPRI# J3 GTL_BPRI# 7
BR0# N4 GTL_BR0# 7
DBR# A7 ITP_DBRESET# 4
DBSY# M2 GTL_DBSY# 7
DEFER# L4 GTL_DEFER# 7
DRDY# H2 GTL_DRDY# 7
HIT# K3 GTL_HIT# 7
HITM# K4 GTL_HITM# 7
IERR# A4 GTL_IERR#
INIT# B5 CC_INIT# 17,27
LOCK# J2 GTL_LOCK# 7
PRDY# A10 H_BPM4_PRDY# 4
PREQ# B10 H_BPM5_PREQ# 4
RESET# B11 GTL_CPURST# 4,7

TRDY# M3 GTL_TRDY# 7

RS2# L2 GTL_RS#2 7
RS1# K1 GTL_RS#1 7
RS0# H1 GTL_RS#0 7

DPWR# C19 GTL_DPWR# 7

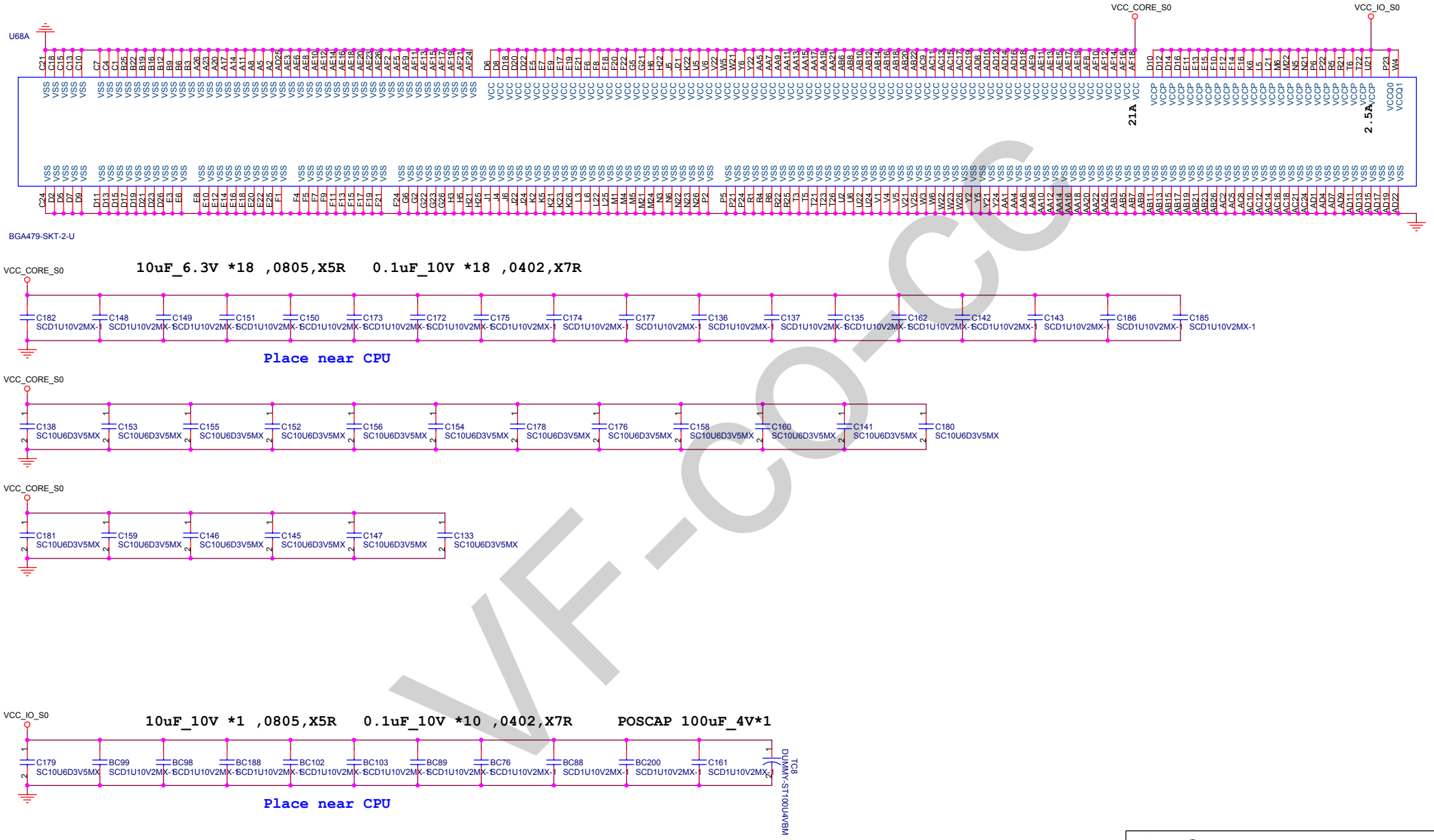
GTL_REQ#[0..4] 7
REQ4# T1 GTL_REQ#4
REQ3# P1 GTL_REQ#3
REQ2# T2 GTL_REQ#2
REQ1# P3 GTL_REQ#1
REQ0# R2 GTL_REQ#0

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Banias CPU (1 of 2)

Size: A3 | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 5 of 39

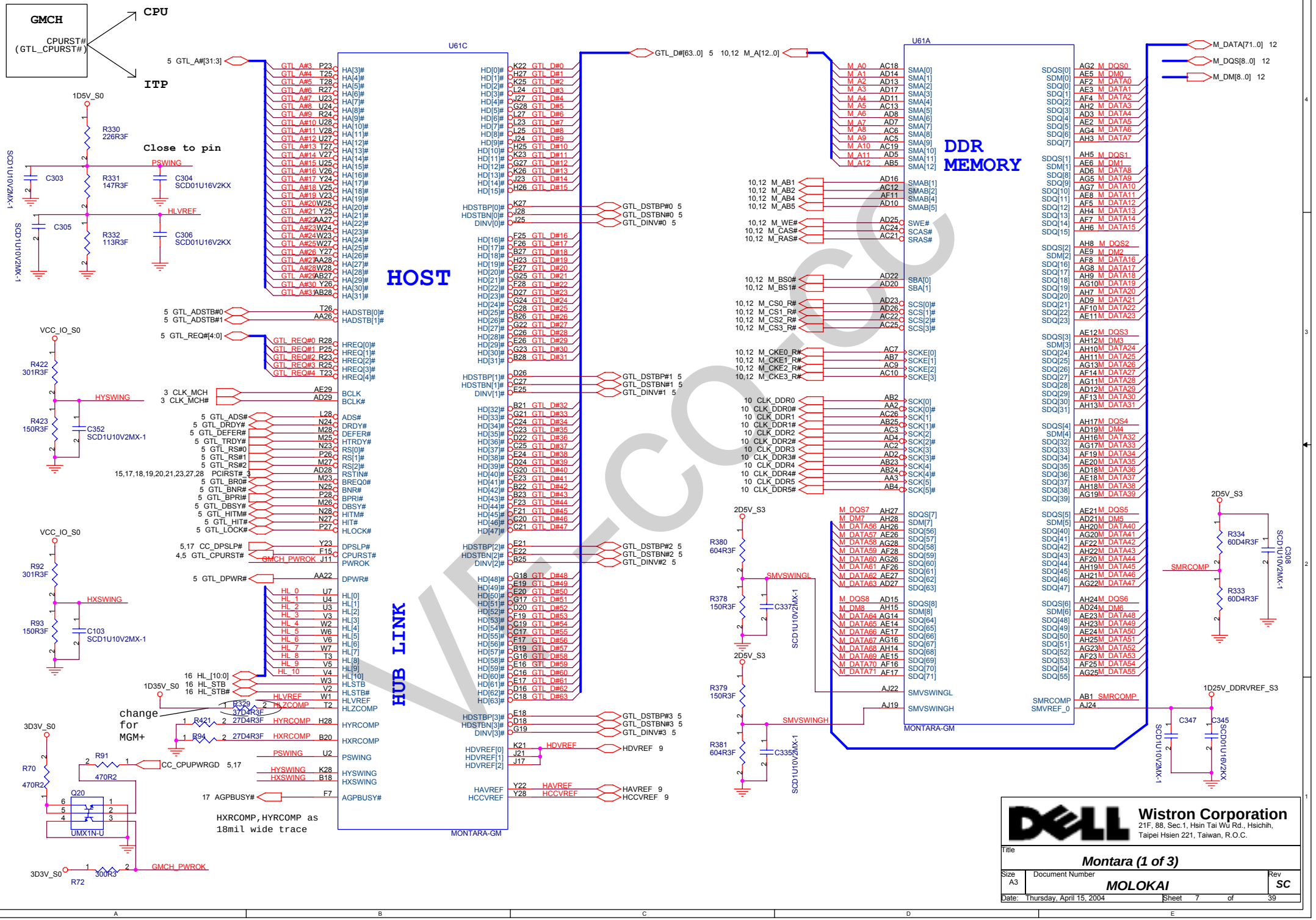


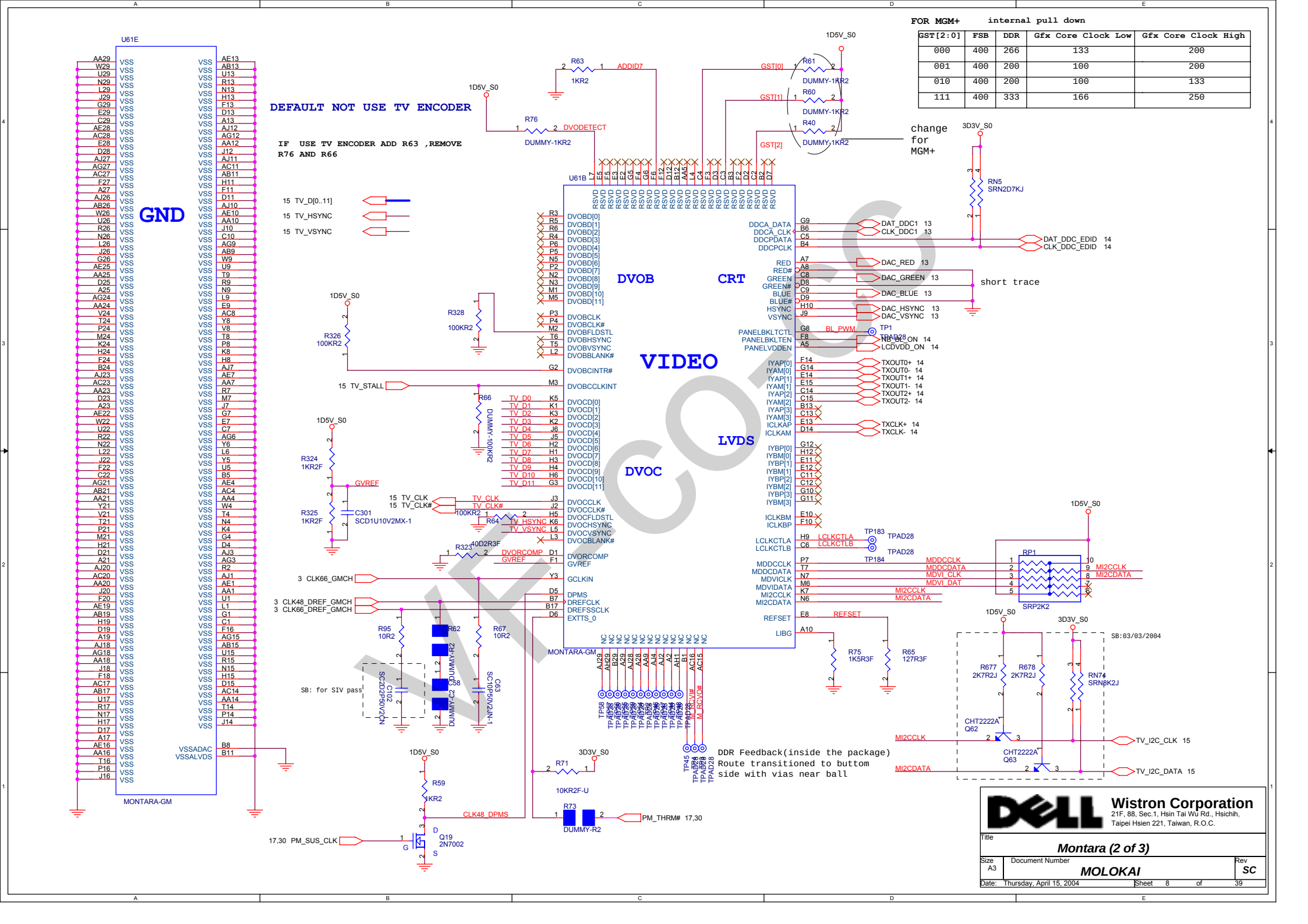
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

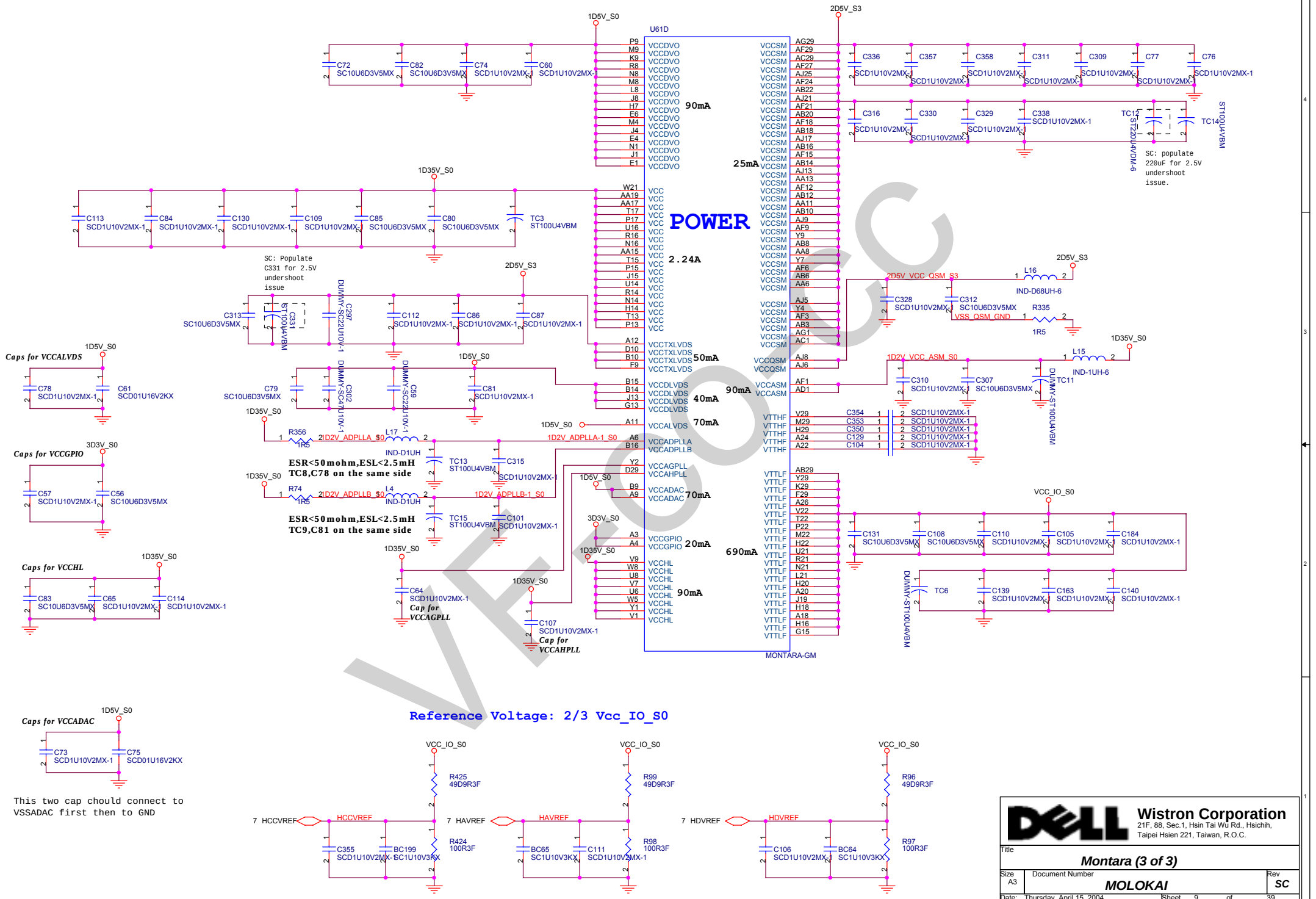
Title: *Banias CPU (2 of 2)*

Size: A3 | Document Number: *MOLOKAI* | Rev: *SC*

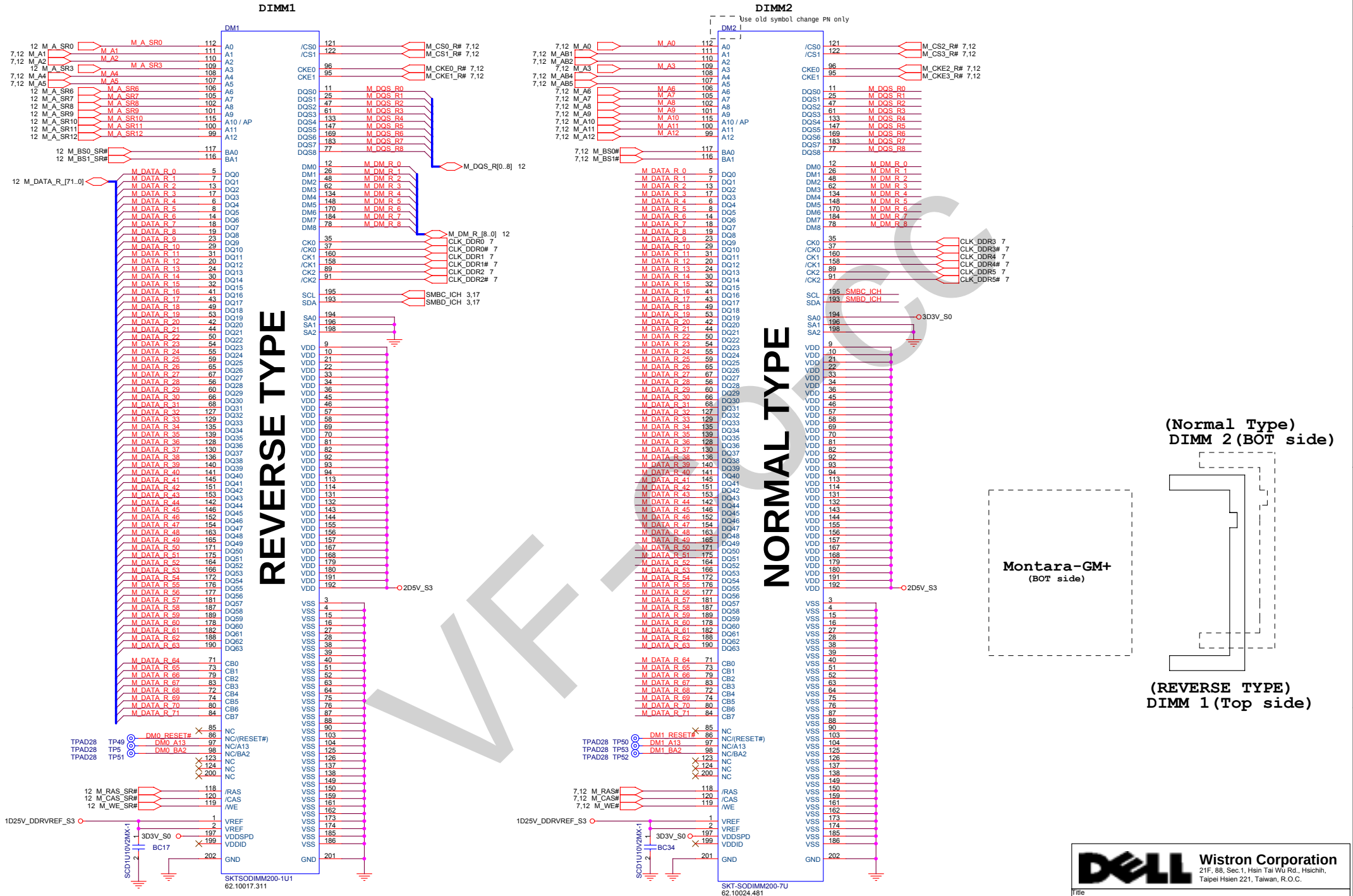
Date: Thursday, April 15, 2004 | Sheet 6 of 39




FOR MGM+ internal pull down
GST[2:0] | FSB | DDR | Gfx Core Clock Low | Gfx Core Clock High
000 | 400 | 266 | 133 | 200
001 | 400 | 200 | 100 | 200
010 | 400 | 200 | 100 | 133
111 | 400 | 333 | 166 | 250
DEFAULT NOT USE TV ENCODER
IF USE TV ENCODER ADD R63 ,REMOVE R76 AND R66
change for MGM+
short trace
DDR Feedback(inside the package) Route transitioned to buttom side with vias near ball
SB: for SIV pass
SB:03/03/2004
GND
VIDEO
DVOB
DVOC
CRT
LVDS
U61E
U61B
MONTARA-GM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Montara (2 of 3)
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 8 of 39



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *Montara (3 of 3)*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
Date: Thursday, April 15, 2004	Sheet 9 of 39	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Socket

Size: Custom | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 10 of 39

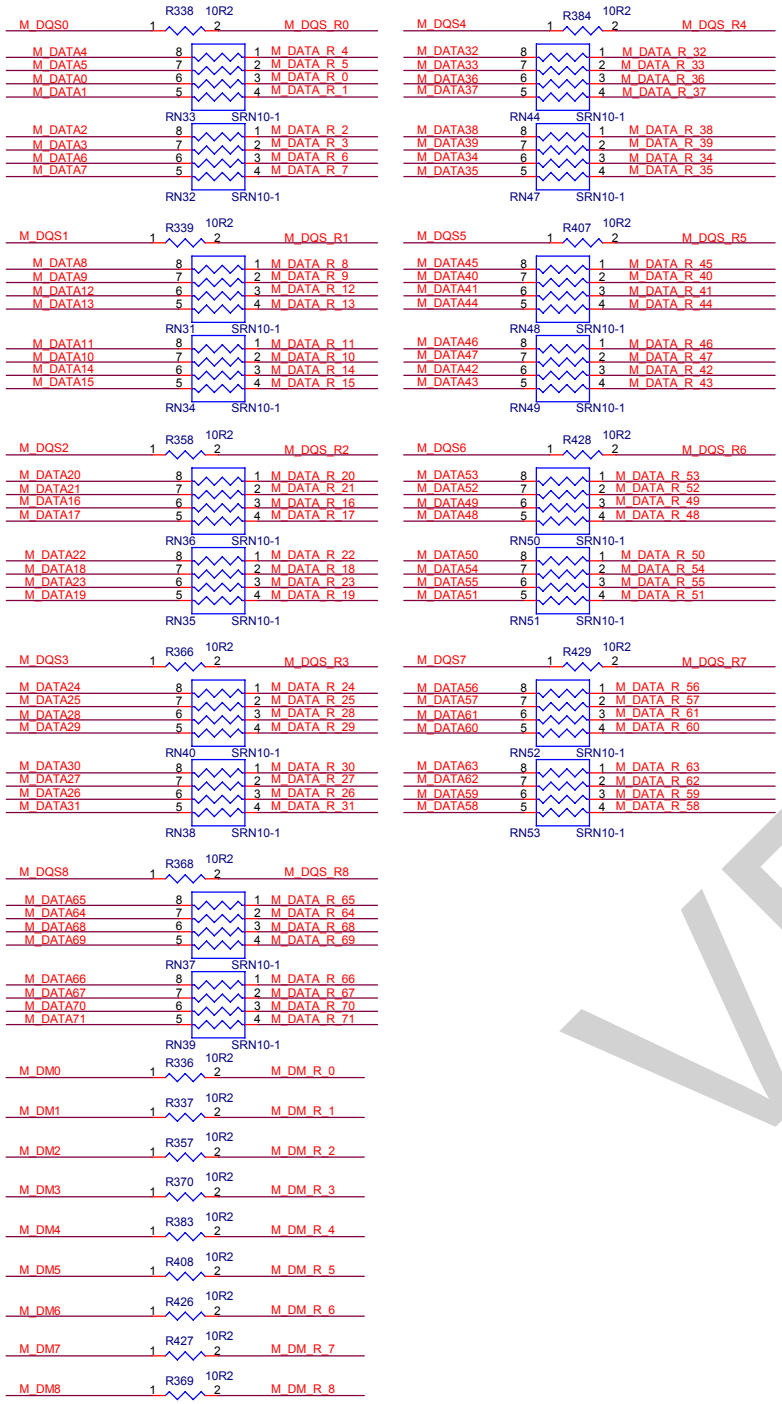
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Decoupling CPA

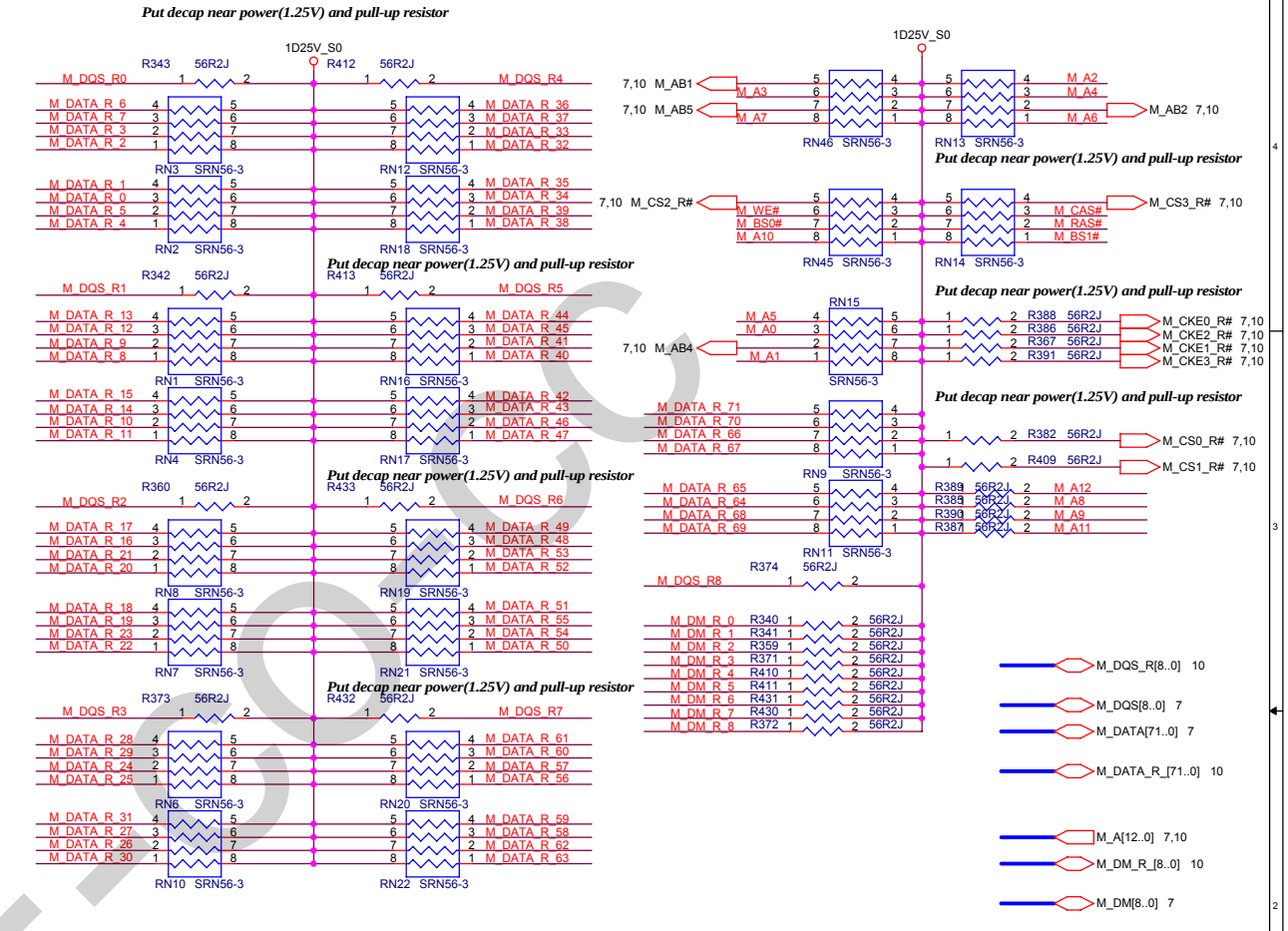
Size: A3 | Document Number: MOLOKAI | Rev: SC

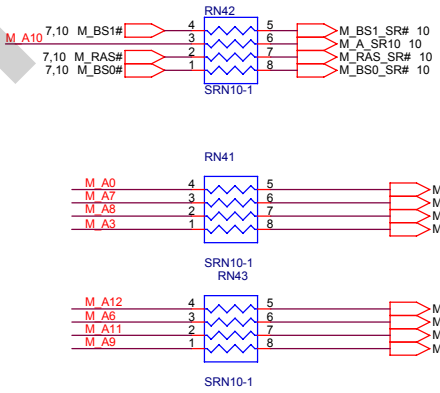
Date: Thursday, April 15, 2004 | Sheet 11 of 39

SERIES DAMPING

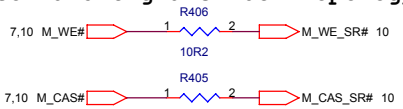


PARALLEL TERMINATION





Command Signals USE Topology 2



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR Serial/Terminator Resistor*

Size: A3 | Document Number: *MOLOKAI* | Rev: *SC*

Date: Thursday, April 15, 2004 | Sheet 12 of 39

CRT

Ferrite bead impedance:
75ohm@100MHz

8 DAC_RED
8 DAC_GREEN
8 DAC_BLUE
L18 MLB-160808-10
L19 MLB-160808-10
L20 MLB-160808-10
CRT_R
CRT_G
CRT_B
C85 SC15P50V2JN
C89 SC15P50V2JN
C90 SC15P50V2JN
SB: for SIV pass
R79 75R2F
R80 75R2F
R81 75R2F
5V_S0
D44
D45
D46
BAV99-2
BAV99-2
BAV99-2
5V_S0
BC63 SCD1U10V2MX-1
U25A
8 DAC_HSYNC
R78 33R2
TSAHCT125
HSYNC_5
8 DAC_VSYNC
R100 33R2
U25B
TSAHCT125
VSYNC_5
L5 33R2
L6 33R2
JVGA_HS
JVGA_VS
5V_S0
D20 SSM5817SL
CRT_VCC_1_S0
F9 FUSE-1A6V
CRT_VCC_S0
BC189 SCD01U16V2KX
R415 3K3R2
R414 3K3R2
CRT_R
CRT_G
CRT_B
DAT_DDC1_5
CLK_DDC1_5
C481 SC47P50V2JN
C482 SC47P50V2JN
JVGA_HS
JVGA_VS
CRT1
MH1
MH2
FOX-CONN15-2-U
20.20305.015
C116 DUMMY-SC3D3P50V
C117 DUMMY-SC3D3P50V
CLOSE TO CRT CONN

Layout Note:
Must be a ground return path for CRT_R,CRT_G,CRT_B

DDC_CLK & DATE LEVEL SHIFT

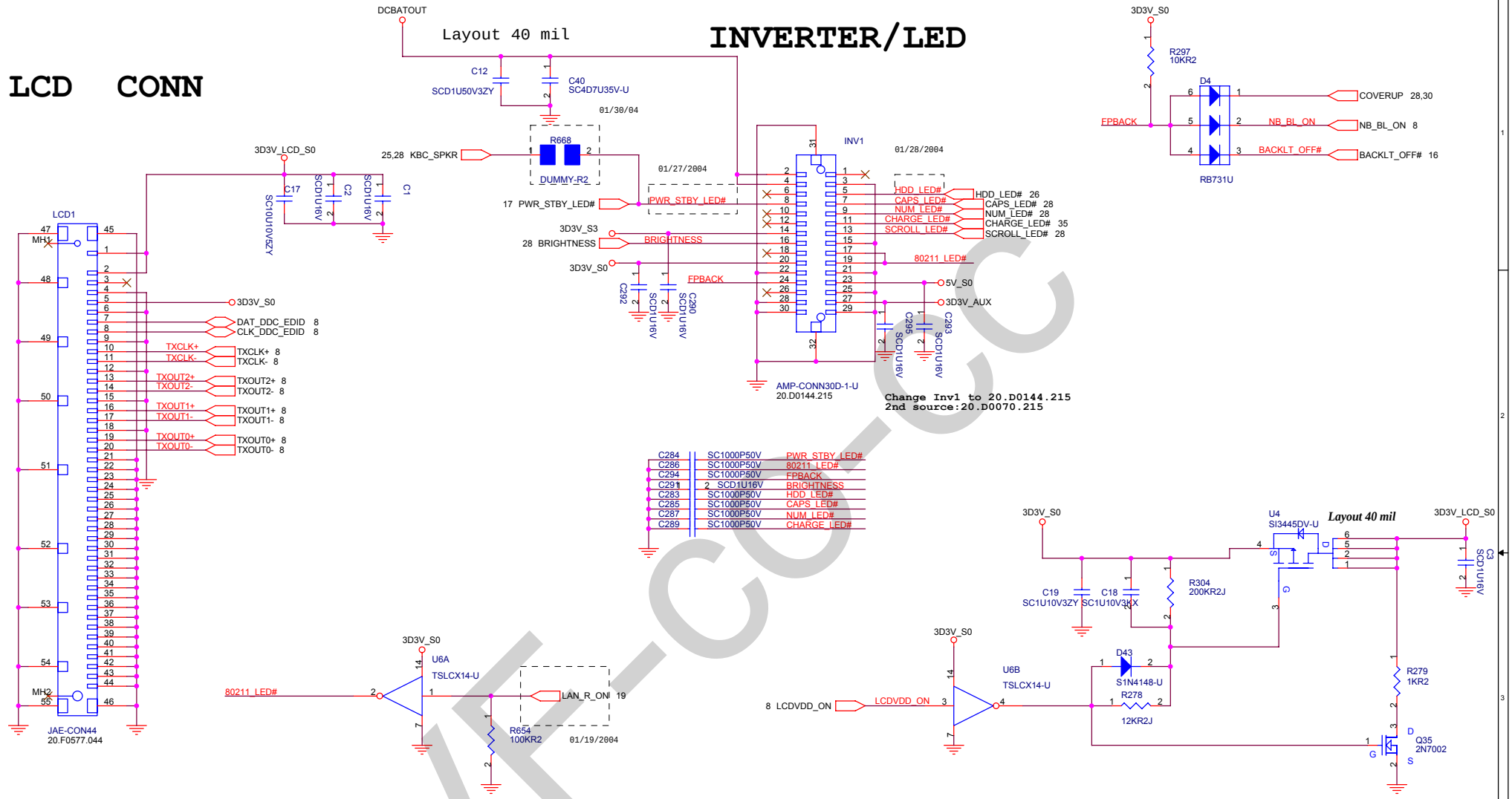
3D3V_S0
3D3V_S0
R435 2K2R3
R434 2K2R3
R416 10KR2
Q40 2N7002
8 DAT_DDC1
DAT_DDC1_5
Q41 2N7002
8 CLK_DDC1
CLK_DDC1_5

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT CONN.	
Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 13 of 39	

LCD CONN

INVERTER/LED



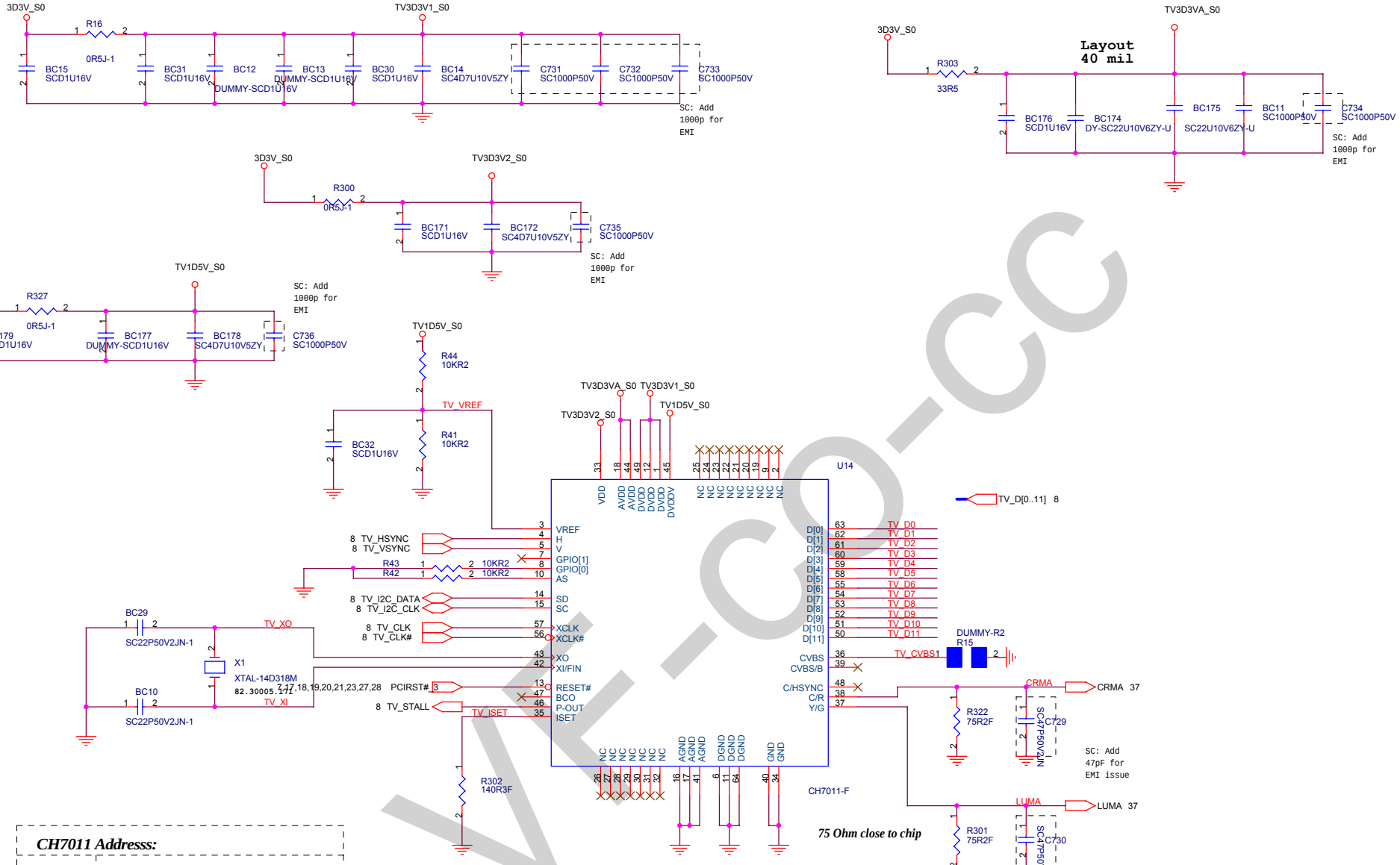
	S0/S1	S3	S4	S5	Functions	when LID is closed
Power On / Battery Low LED (PWR_LED#)	LOW	HIGH	HIGH	HIGH		readable
Sleep / Waking LED (STDBY_LED#)	HIGH	LOW	HIGH	HIGH	(Don't flash during waking)	readable
Disk Media (MEDIA_LED#)					HDD,ODD access indicator	not readable
Charging LED (CHARGE_LED#)					On when charging. Flashing when charging error is occured.	not readable
Wireless LED (80211_LED#)					On when wireless is On	not readable
NUM Lock (NUM_LED#)					On when Number key is locked	not readable
CAPS Lock (MEDIA_LED#)					On when Caps lock is On	not readable

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & INVERTER

Size: A3 | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 14 of 39



CH7011 Addresss:		
0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

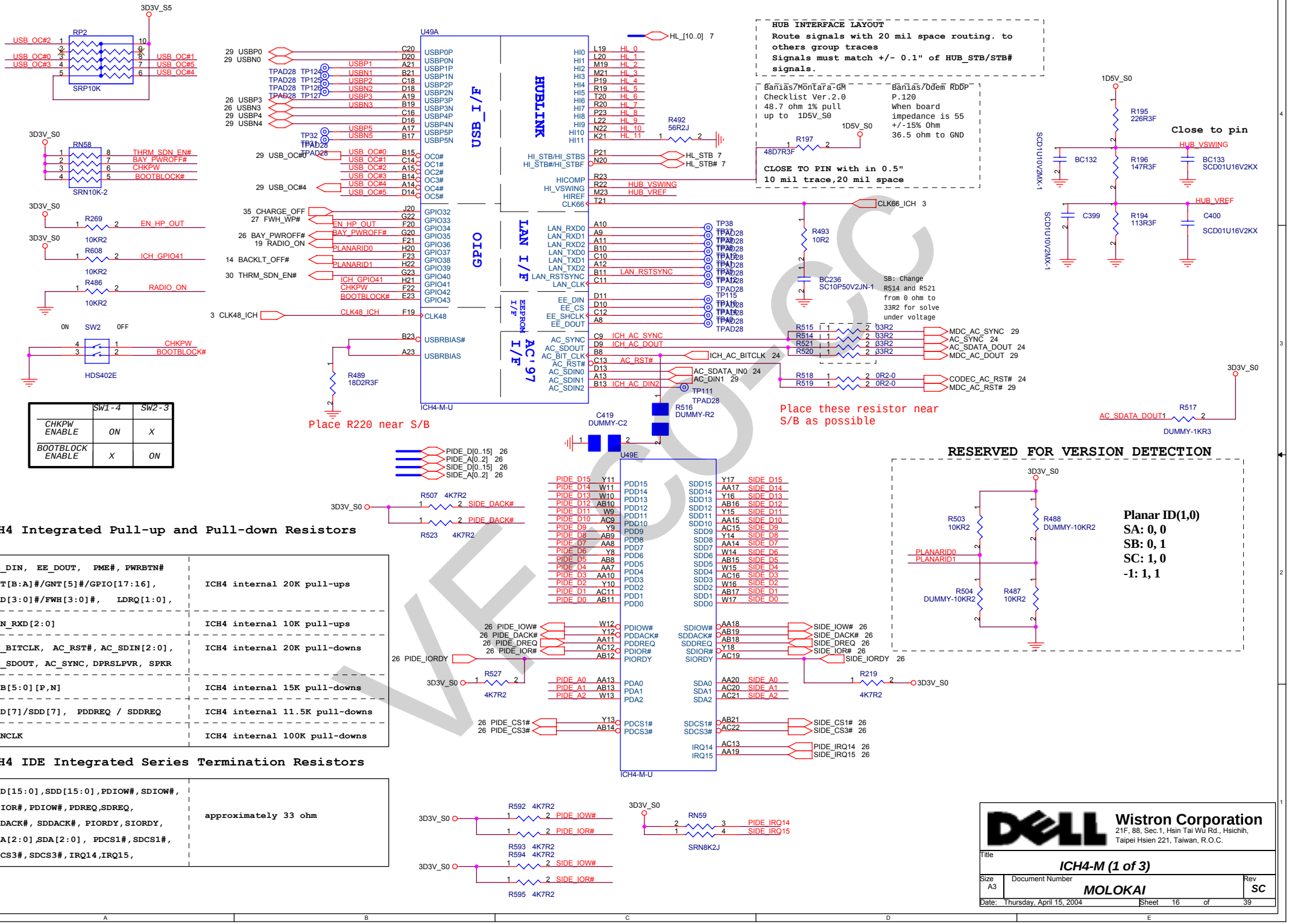
Power up default:		
NTSC	GPIO0 pull-down	
PAL	GPIO0 pull-up	(int. pull-up)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TV_ENCODER

Size: A3 | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 15 of 39



	SW1-4	SW2-3
CHKPW ENABLE	ON	X
BOOTBLOCK ENABLE	X	ON

ICH4 Integrated Pull-up and Pull-down Resistors

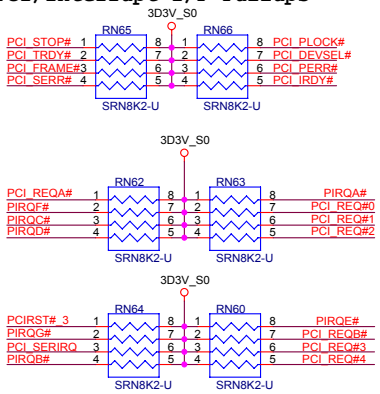
EE_DIN, EE_DOUT, PME#, PWRBTN# GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	ICH4 internal 20K pull-ups
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

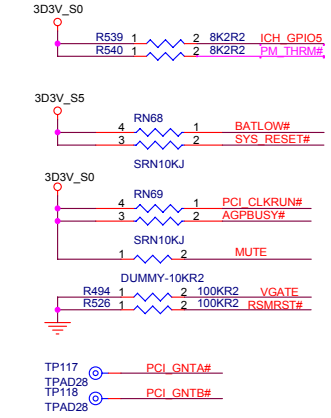
ICH4 IDE Integrated Series Termination Resistors

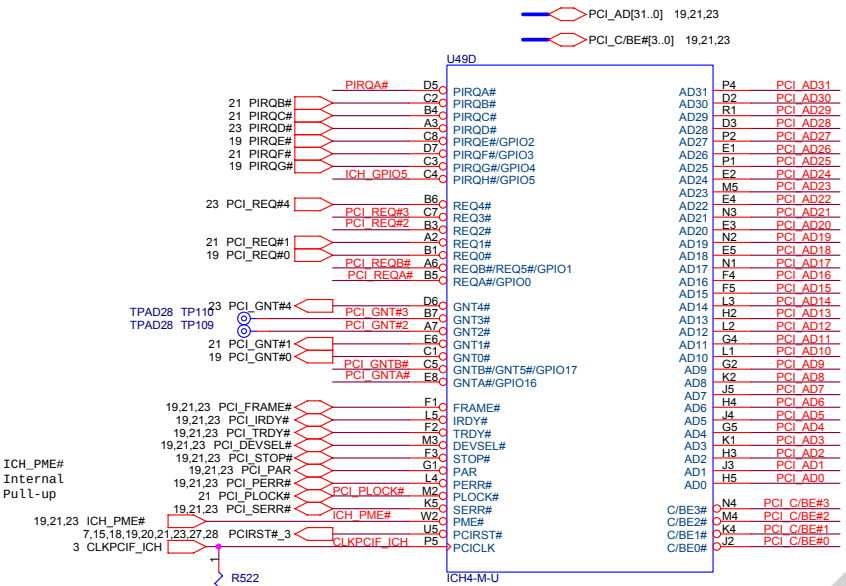
PDD[15:0],SDD[15:0],PDIOW#,SDIOW#, PDIOR#,PDIOW#,PDREQ,SDREQ, PDDACK#, SDDACK#, PIORDY,SIORDY, PDA[2:0],SDA[2:0], PDCS1#,SDCS1#, PDCS3#,SDCS3#,IRQ14,IRQ15,	approximately 33 ohm

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ICH4-M (1 of 3)		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 16 of 39	

PCI/Interrupt I/F Pullups





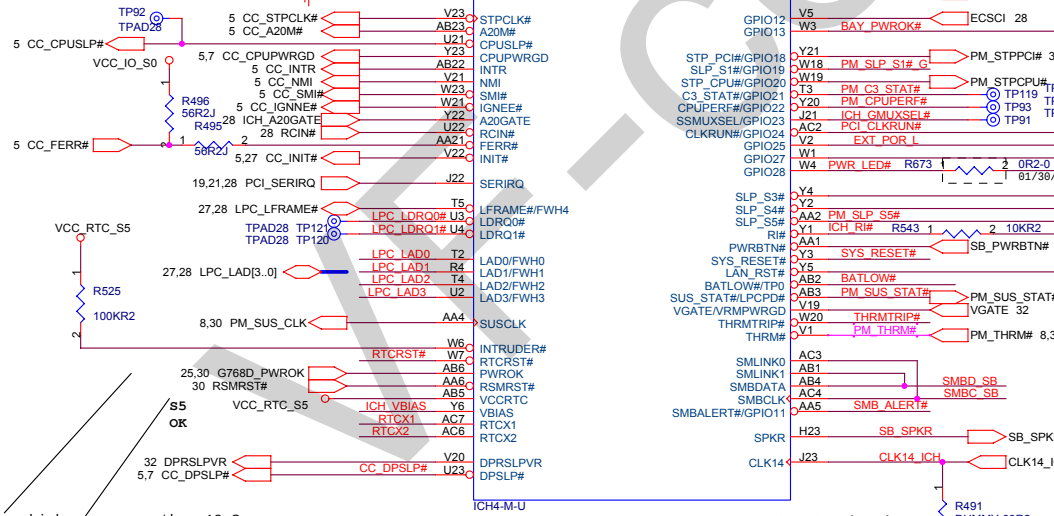


ICH_PME#
Internal
Pull-up

R522 10R2

SC10P50V2JN-1

BC264

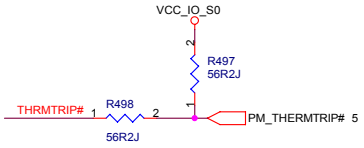


Should go high no sooner than 10mS
after both +3VRUN and +1.5VRUN
have reach their nominal voltage

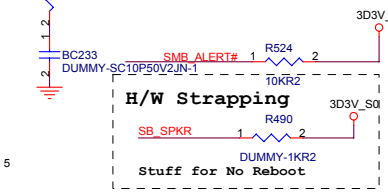
Should go high no sooner than 10mS
after both +3VSUS and +1.5VSUS
have reach their nominal voltage

S5
OK

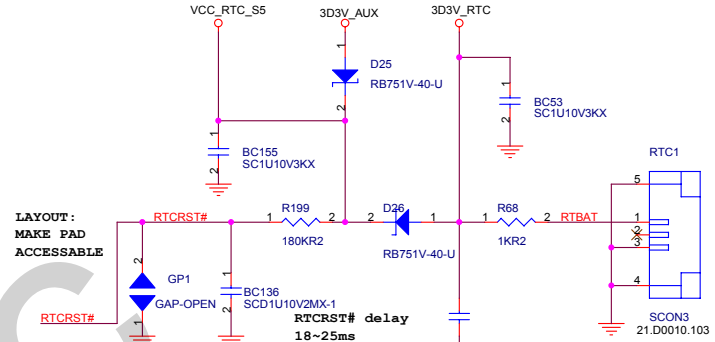
If ICH-4 LAN not used,10K ohm
PD
or connect directly to
----RSMRST#(SUSPWROK)
But in Bon conncet to
PWROK(DELAY_IMVP_PWRGD)

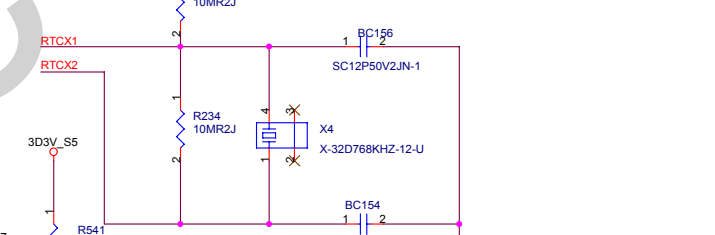


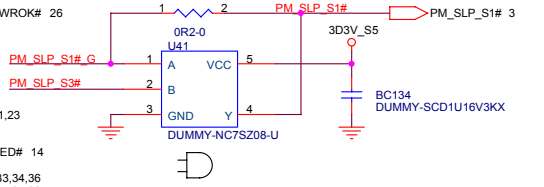
CLK termination
close to ICH4

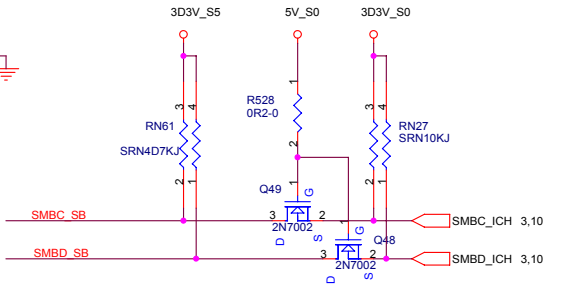


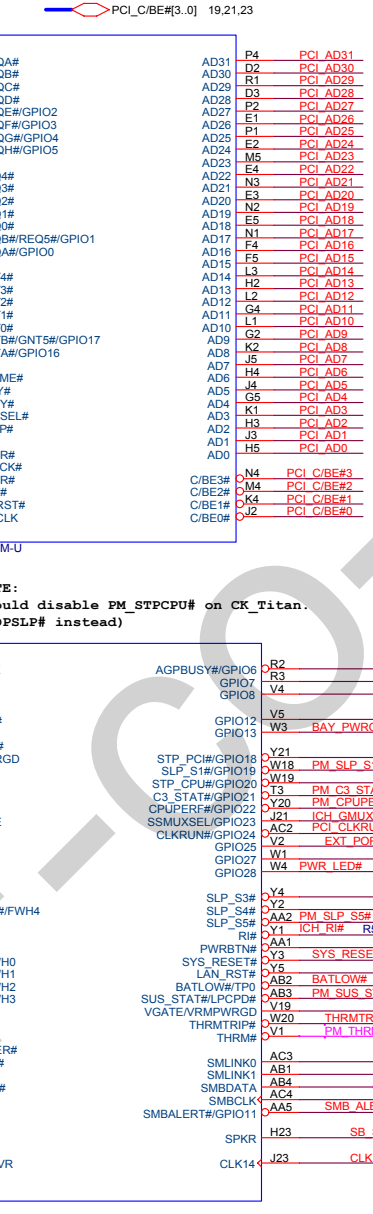
RTC Circuitry







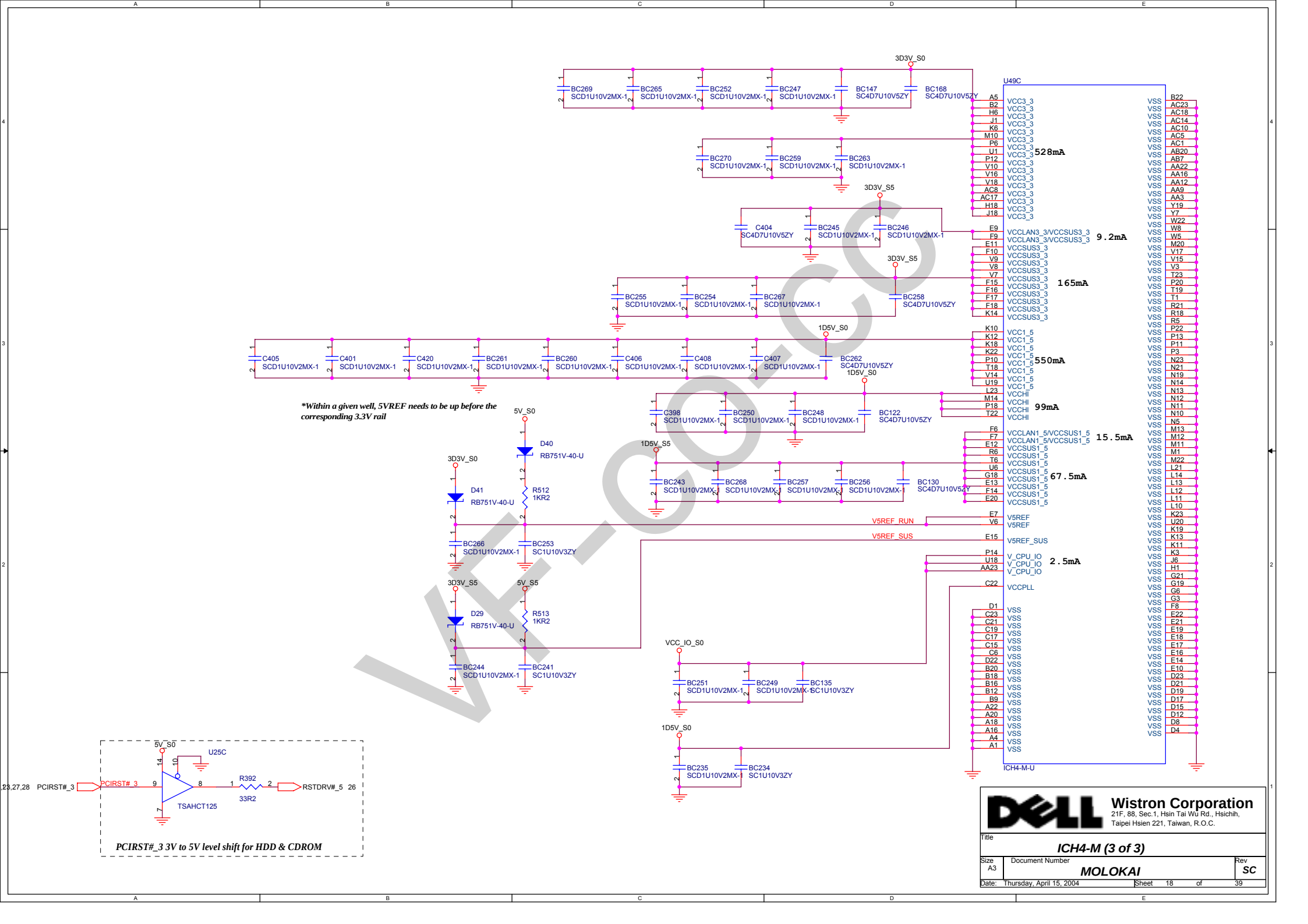




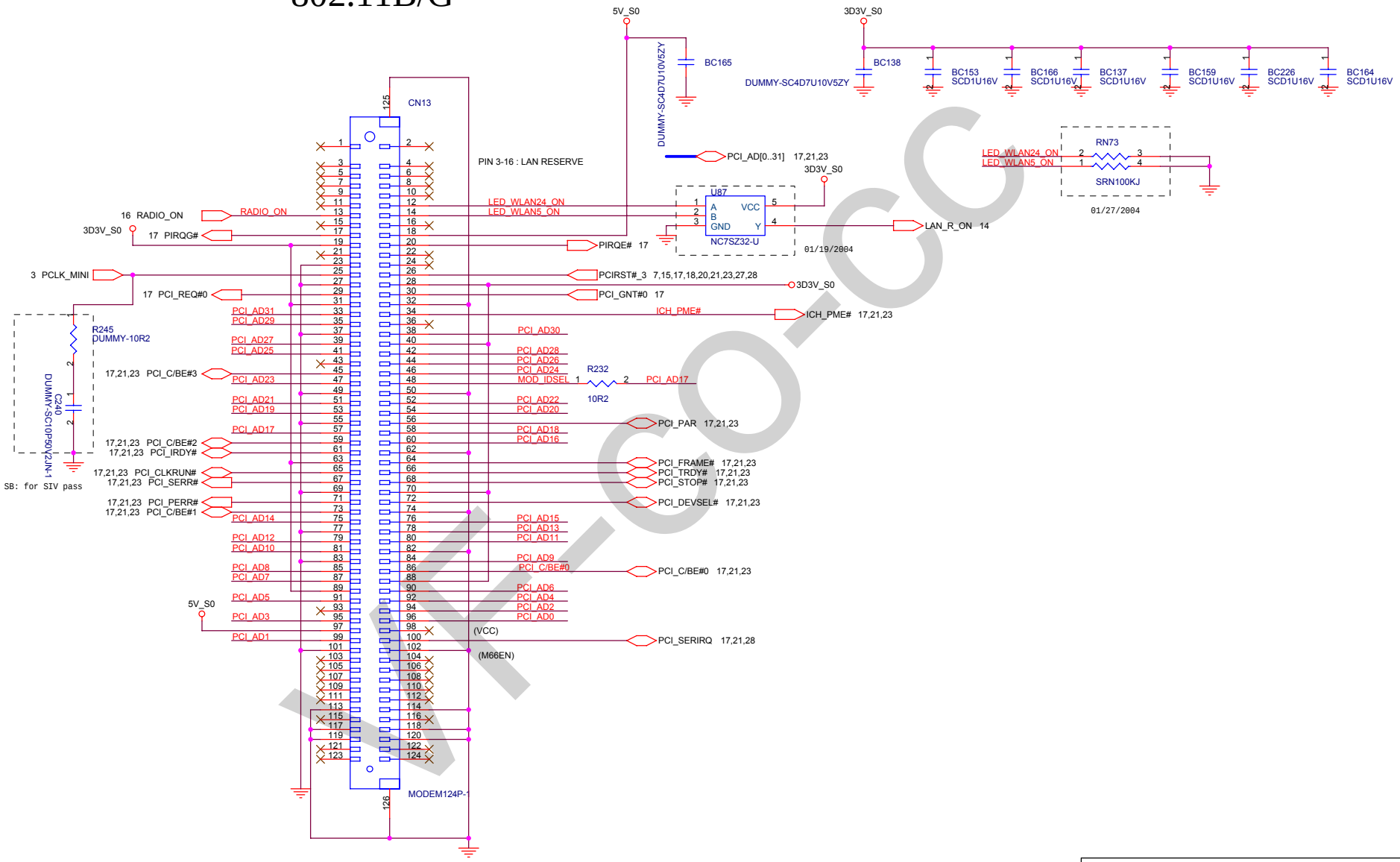
Title: ICH4-M (2 of 3)

Size: Custom | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 17 of 39

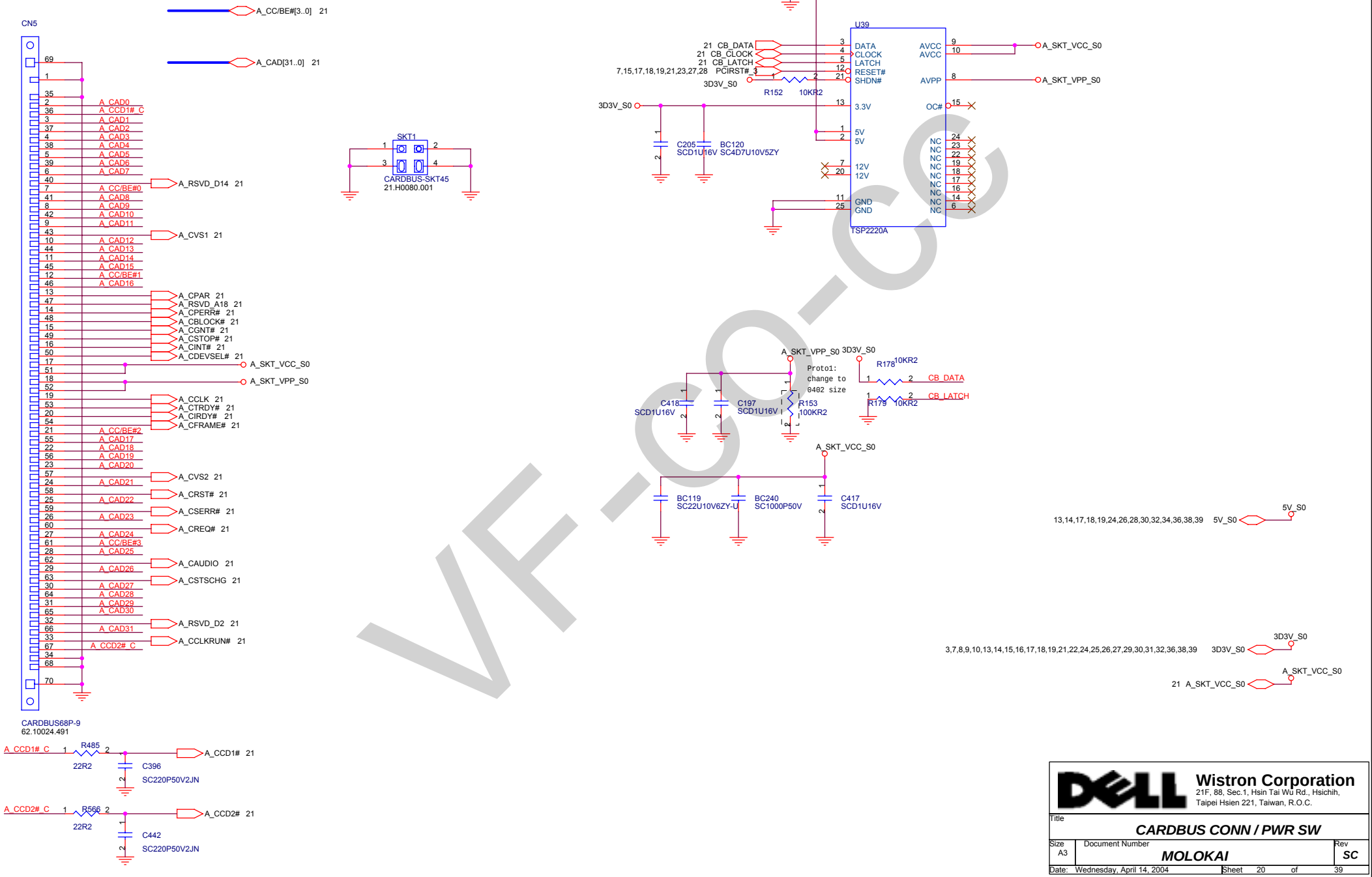

U49C
3D3V_S0
1D5V_S0
3D3V_S5
1D5V_S5
5V_S0
5V_S5
VCC_IO_S0
V5REF_RUN
V5REF_SUS
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
528mA
9.2mA
165mA
550mA
99mA
15.5mA
67.5mA
2.5mA
ICH4-M-U
U25C
TSAHCT125
PCIRST#_3 3
RSTDRV#_5 26
PCIRST#_3 3V to 5V level shift for HDD & CDROM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4-M (3 of 3)
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 18 of 39

Mini PCI
802.11B/G

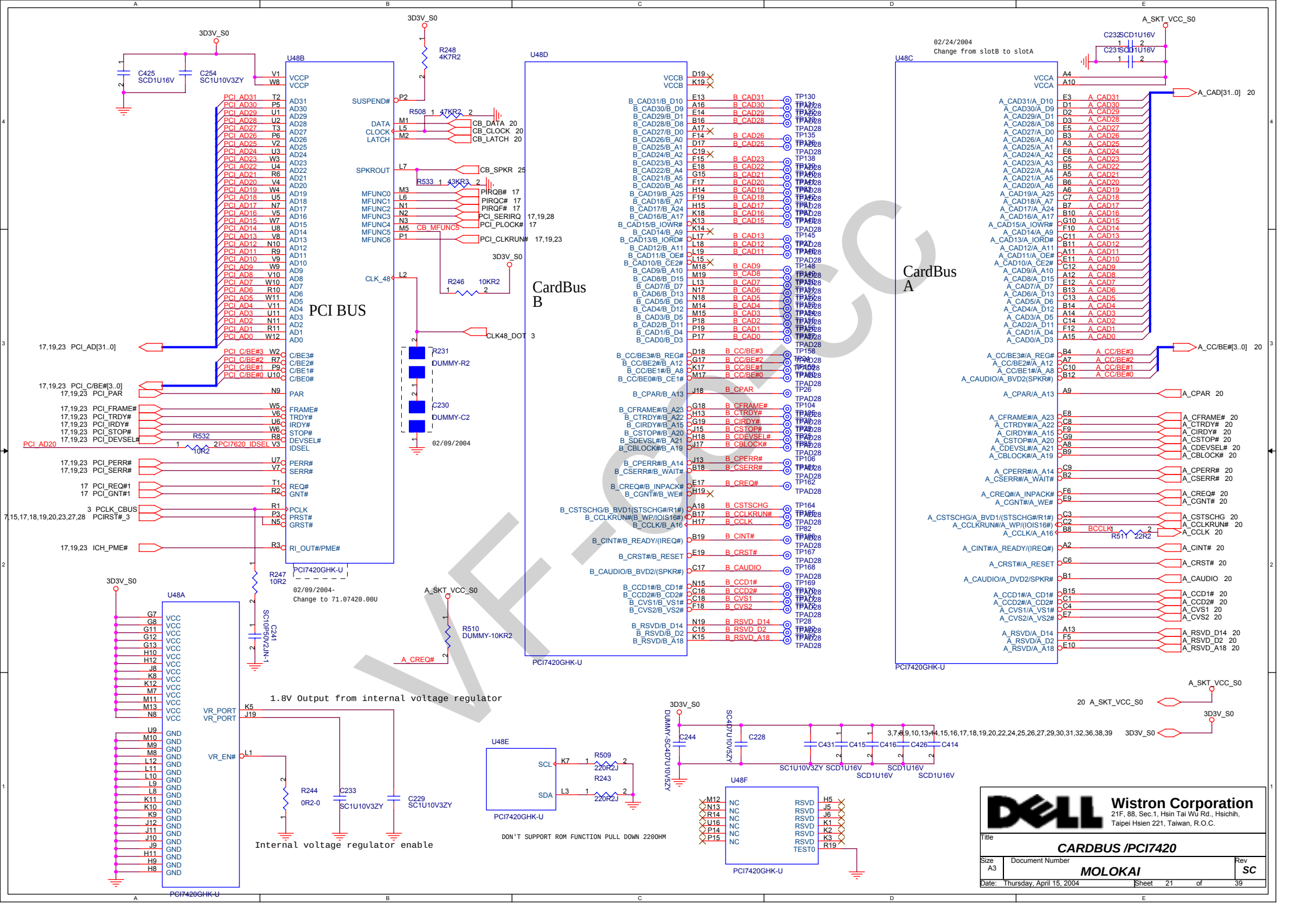


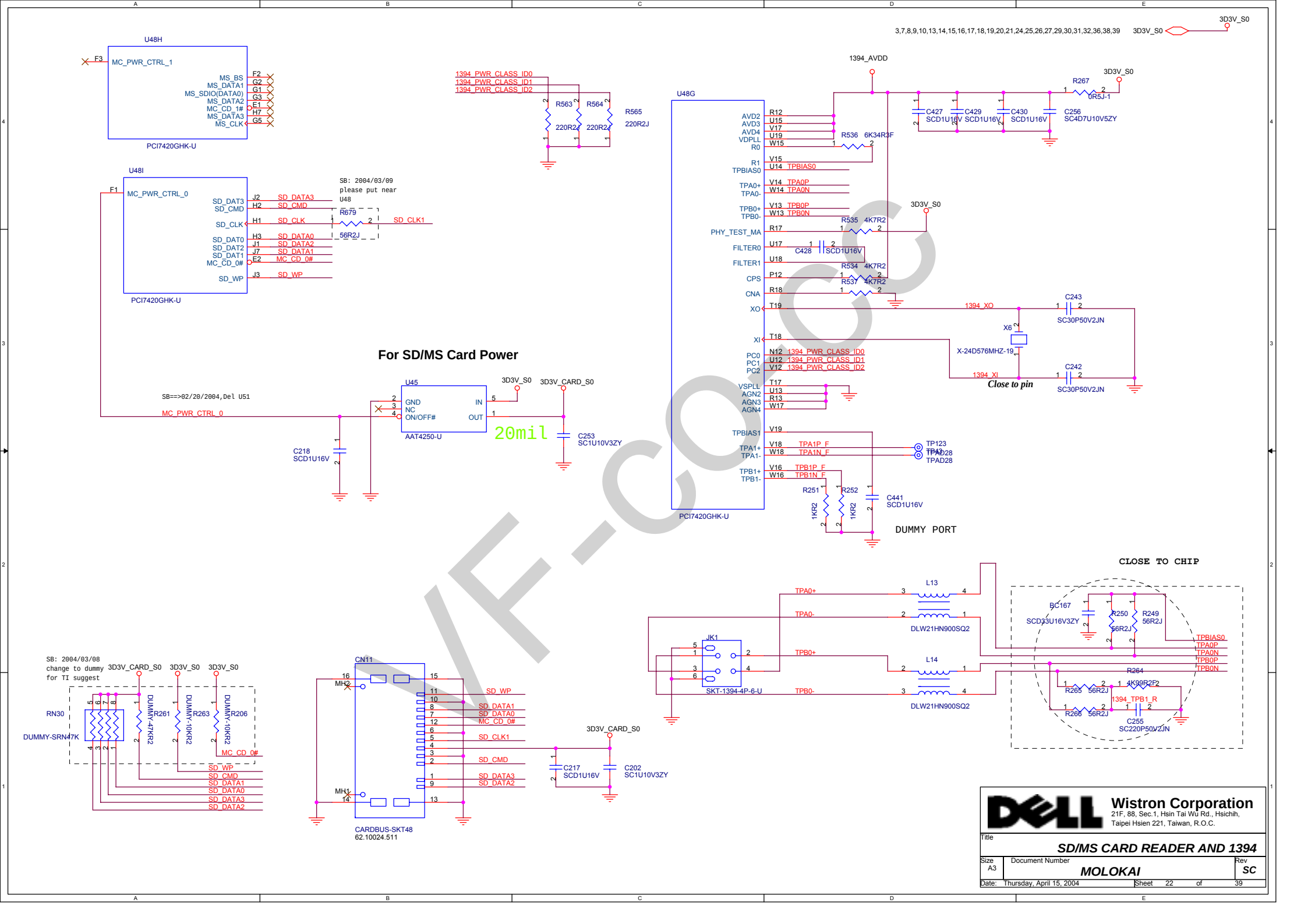
DELL	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Mini PCI Socket***	
Size: A3	Document Number: ***MOLOKAI***	Rev: ***SC***
Date: Thursday, April 15, 2004	Sheet 19 of 39	

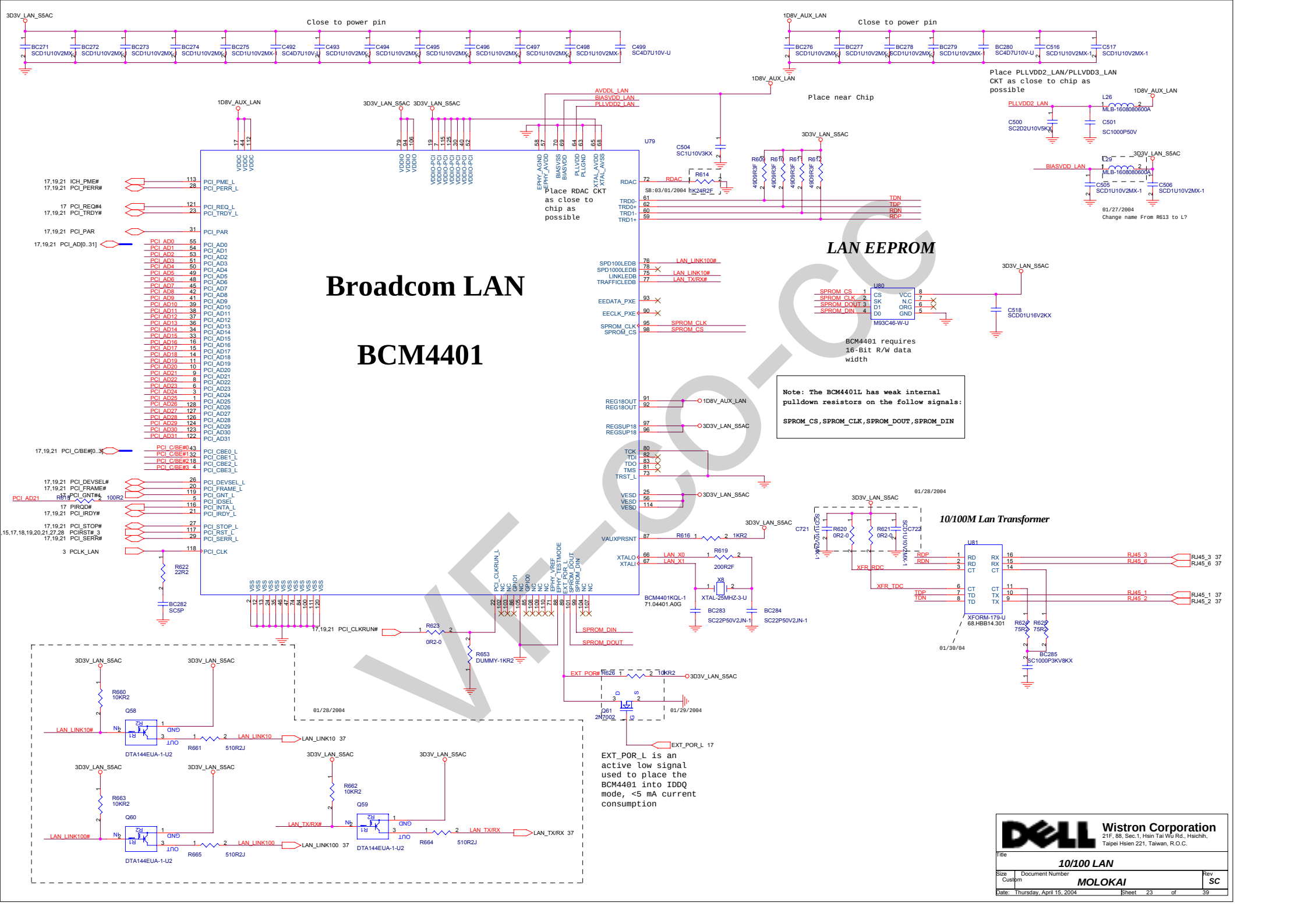
PCMCIA socket

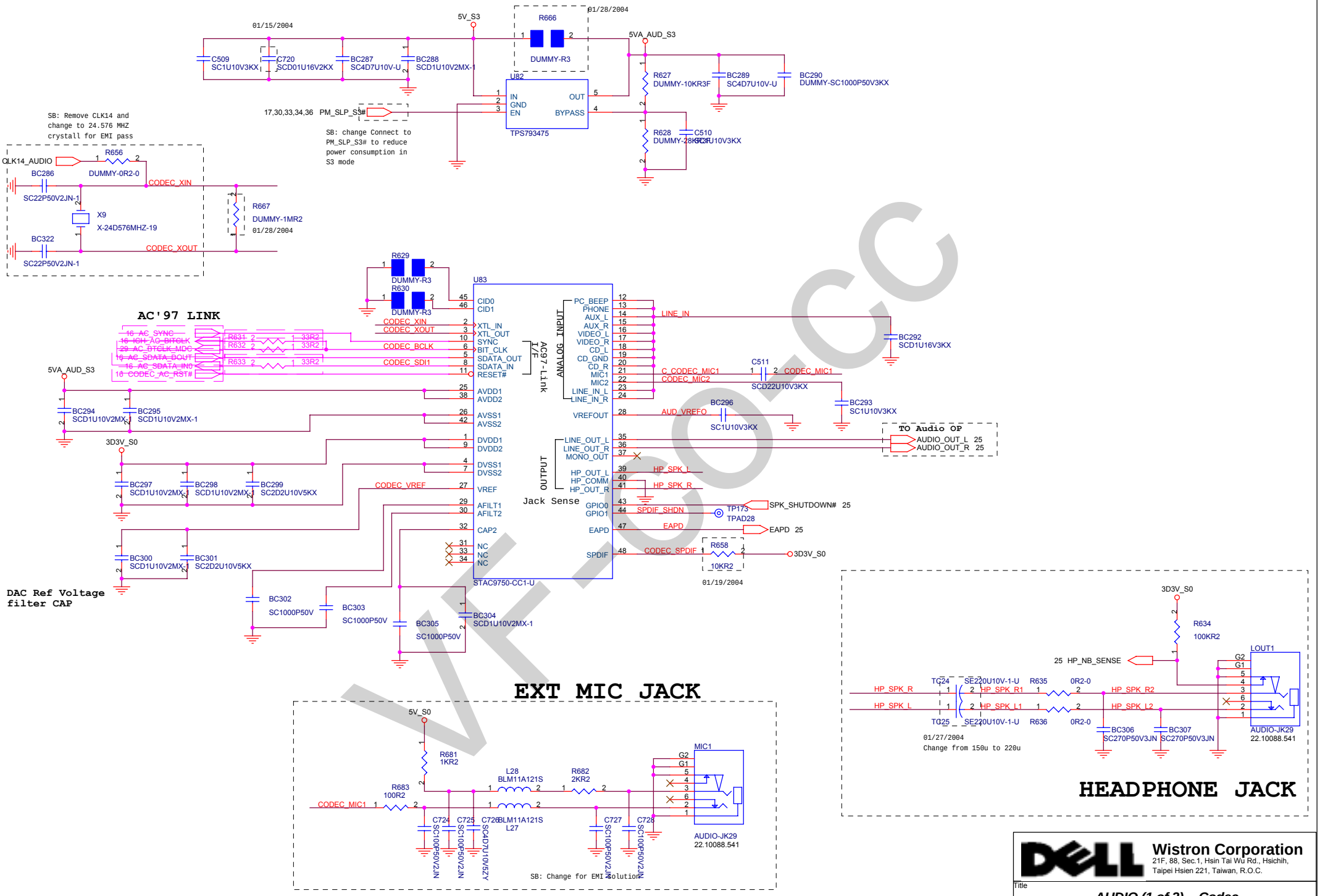


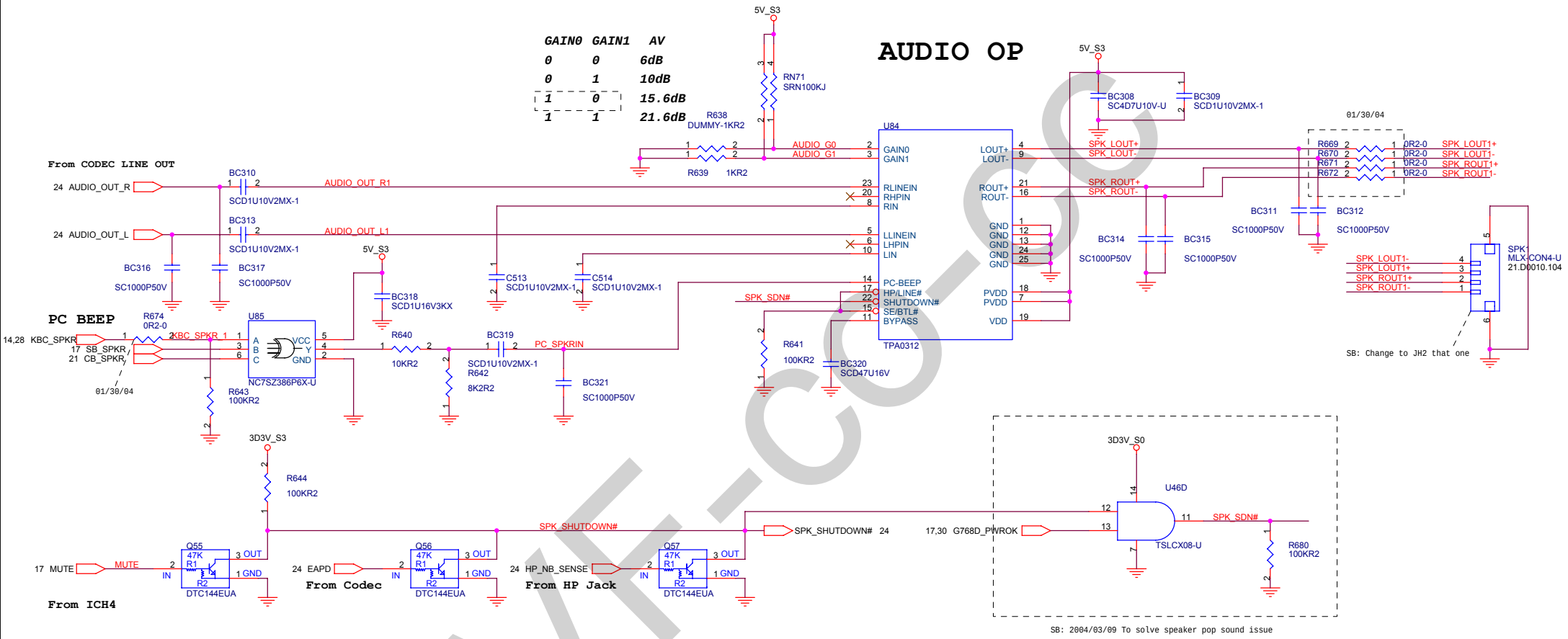
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CARDBUS CONN / PWR SW
Size A3 / Document Number	MOLOKAI / Rev SC
Date: Wednesday, April 14, 2004	Sheet 20 of 39


U48B
PCI BUS
PCI7420GHK-U
U48D
CardBus B
PCI7420GHK-U
U48C
CardBus A
PCI7420GHK-U
02/24/2004
Change from slotB to slotA
U48A
PCI7420GHK-U
1.8V Output from internal voltage regulator
Internal voltage regulator enable
U48E
PCI7420GHK-U
DON'T SUPPORT ROM FUNCTION PULL DOWN 220OHM
U48F
PCI7420GHK-U
02/09/2004-
Change to 71.07420.00U
02/09/2004
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CARDBUS /PCI7420
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 21 of 39

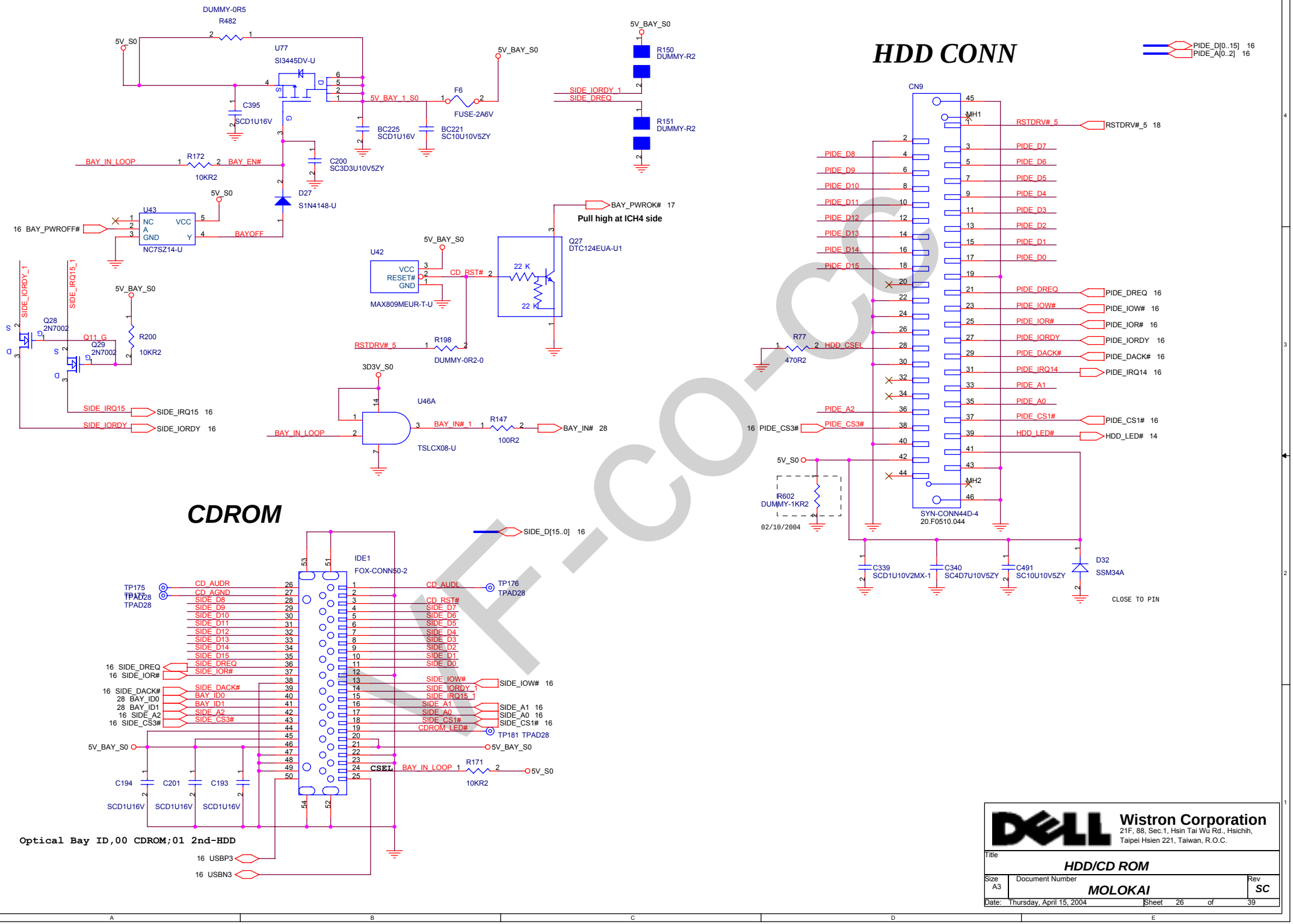

3,7,8,9,10,13,14,15,16,17,18,19,20,21,24,25,26,27,29,30,31,32,36,38,39
3D3V_S0
U48H
F3
MC_PWR_CTRL_1
MS_BS F2
MS_DATA1 G2
MS_SDIO(DATA0) G1
MS_DATA2 G3
MC_CD_1# E1
MS_DATA3 H7
MS_CLK G5
PCI7420GHK-U
U48I
F1
MC_PWR_CTRL_0
SD_DAT3 J2 SD_DATA3
SD_CMD H2 SD_CMD
SD_CLK H1 SD_CLK
SD_DAT0 H3 SD_DATA0
SD_DAT2 J1 SD_DATA2
SD_DAT1 J7 SD_DATA1
MC_CD_0# E2 MC_CD_0#
SD_WP J3 SD_WP
SB: 2004/03/09
please put near
U48
R679
56R2J
SD_CLK1
PCI7420GHK-U
1394_PWR_CLASS_ID0
1394_PWR_CLASS_ID1
1394_PWR_CLASS_ID2
R563 220R2J
R564 220R2J
R565 220R2J
U48G
1394_AVDD
AVD2 R12
AVD3 U15
AVD4 V17
VDPLL U19
R0 W15
R536 6K34R3F
R1 V15
TPBIAS0 U14 TPBIAS0
TPA0+ V14 TPA0P
TPA0- W14 TPA0N
TPB0+ V13 TPB0P
TPB0- W13 TPB0N
PHY_TEST_MA R17
R535 4K7R2
FILTER0 U17
C428 SCD1U16V
FILTER1 U18
CPS P12
R534 4K7R2
R537 4K7R2
CNA R18
XO T19
XI T18
PC0 N12 1394_PWR_CLASS_ID0
PC1 U12 1394_PWR_CLASS_ID1
PC2 V12 1394_PWR_CLASS_ID2
VSPLL T17
AGN2 U13
AGN3 R13
AGN4 W17
TPBIAS1 V19
TPA1+ V18 TPA1P_F
TPA1- W18 TPA1N_F
TPB1+ V16 TPB1P_F
TPB1- W16 TPB1N_F
R251 1KR2
R252 1KR2
C441 SCD1U16V
PCI7420GHK-U
R267 0R5J-1
C427 SCD1U16V
C429 SCD1U16V
C430 SCD1U16V
C256 SC4D7U10V5ZY
C243 SC30P50V2JN
X6
X-24D576MHZ-19
1394_XO
1394_XI
C242 SC30P50V2JN
Close to pin
TP123 TPAD28
TP43 TPAD28
DUMMY PORT
For SD/MS Card Power
SB==>02/20/2004,Del U51
MC_PWR_CTRL_0
U45
GND
NC
ON/OFF#
IN
OUT
AAT4250-U
3D3V_S0
3D3V_CARD_S0
20mil
C218 SCD1U16V
C253 SC1U10V3ZY
CLOSE TO CHIP
TPA0+
TPA0-
TPB0+
TPB0-
JK1
SKT-1394-4P-6-U
L13
L14
DLW21HN900SQ2
DLW21HN900SQ2
BC167 SCD33U16V3ZY
R250 56R2J
R249 56R2J
R264 4K99R2F2
R265 56R2J
R266 56R2J
1394_TPB1_R
C255 SC220P50V2JN
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
SB: 2004/03/08
change to dummy
for TI suggest
3D3V_CARD_S0
3D3V_S0
3D3V_S0
RN30
DUMMY-SRN47K
DUMMY-47KR2
DUMMY-10KR2
DUMMY-10KR2
MC_CD_0#
SD_WP
SD_CMD
SD_DATA1
SD_DATA0
SD_DATA3
SD_DATA2
CN11
MH2
MH1
CARDBUS-SKT48
62.10024.511
SD_WP
SD_DATA1
SD_DATA0
MC_CD_0#
SD_CLK1
SD_CMD
SD_DATA3
SD_DATA2
3D3V_CARD_S0
C217 SCD1U16V
C202 SC1U10V3ZY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SD/MS CARD READER AND 1394
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 22 of 39


Broadcom LAN
BCM4401
LAN EEPROM
10/100M Lan Transformer
Close to power pin
Place near Chip
Place RDAC CKT as close to chip as possible
Place PLLVDD2_LAN/PLLVDD3_LAN CKT as close to chip as possible
BCM4401 requires 16-Bit R/W data width
Note: The BCM4401L has weak internal pulldown resistors on the follow signals:
SPROM_CS,SPROM_CLK,SPROM_DOUT,SPROM_DIN
EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption
Change name From R613 to L?
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
10/100 LAN
Size Custom
Document Number MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 23 of 39


01/15/2004
5V_S3
R666
01/28/2004
DUMMY-R3
5VA_AUD_S3
C509 SC1U10V3KX
C720 SCD01U16V2KX
BC287 SC4D7U10V-U
BC288 SCD1U10V2MX-1
U82
IN
GND
EN
OUT
BYPASS
TPS793475
R627 DUMMY-10KR3F
BC289 SC4D7U10V-U
BC290 DUMMY-SC1000P50V3KX
17,30,33,34,36 PM_SLP_S3#
SB: change Connect to PM_SLP_S3# to reduce power consumption in S3 mode
R628 DUMMY-28KR3F
C510 SC1U10V3KX
SB: Remove CLK14 and change to 24.576 MHZ crystall for EMI pass
3 CLK14_AUDIO
R656 DUMMY-0R2-0
BC286 SC22P50V2JN-1
CODEC_XIN
X9 X-24D576MHZ-19
R667 DUMMY-1MR2
01/28/2004
BC322 SC22P50V2JN-1
CODEC_XOUT
R629 DUMMY-R3
R630 DUMMY-R3
U83
AC'97 LINK
16_AC_SYNC
16_IGH_AC_BITCLK
29_AC_BTCLK_MDC
16_AC_SDATA_BOUT
16_AC_SDATA_IN0
16_CODEC_AC_RST#
R631 33R2
R632 33R2
R633 33R2
CODEC_BCLK
CODEC_SDI1
CODEC_XIN
CODEC_XOUT
CID0
CID1
XTL_IN
XTL_OUT
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
AC97-LINK
ANALOG_INPUT
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
LINE_IN
C_CODEC_MIC1
CODEC_MIC2
C511 SCD22U10V3KX
CODEC_MIC1
BC292 SCD1U16V3KX
BC293 SC1U10V3KX
VREFOUT
AUD_VREFO
BC296 SC1U10V3KX
OUTPUT
LINE_OUT_L
LINE_OUT_R
MONO_OUT
HP_OUT_L
HP_COMM
HP_OUT_R
HP_SPK_L
HP_SPK_R
TO Audio OP
AUDIO_OUT_L 25
AUDIO_OUT_R 25
AVDD1
AVDD2
AVSS1
AVSS2
DVDD1
DVDD2
DVSS1
DVSS2
VREF
AFILT1
AFILT2
CAP2
NC
NC
NC
GPIO0
GPIO1
EAPD
SPDIF
SPDIF_SHDN
TP173 TPAD28
SPK_SHUTDOWN# 25
EAPD
EAPD 25
CODEC_SPDIF
R658 10KR2
3D3V_S0
Jack Sense
STAC9750-CC1-U
01/19/2004
5VA_AUD_S3
BC294 SCD1U10V2MX-1
BC295 SCD1U10V2MX-1
3D3V_S0
BC297 SCD1U10V2MX-1
BC298 SCD1U10V2MX-1
BC299 SC2D2U10V5KX
CODEC_VREF
BC300 SCD1U10V2MX-1
BC301 SC2D2U10V5KX
DAC Ref Voltage filter CAP
BC302 SC1000P50V
BC303 SC1000P50V
BC305 SC1000P50V
BC304 SCD1U10V2MX-1
EXT MIC JACK
5V_S0
R681 1KR2
R683 100R2
CODEC_MIC1
L28 BLM11A121S
L27 BLM11A121S
R682 2KR2
C724 SC100P50V2JN
C725 SC100P50V2JN
C726 SC4D7U10V5ZY
C727 SC100P50V2JN
C728 SC100P50V2JN
MIC1
AUDIO-JK29 22.10088.541
SB: Change for EMI solution
3D3V_S0
R634 100KR2
25 HP_NB_SENSE
LOUT1
HP_SPK_R
HP_SPK_L
TC24
TC25
SE220U10V-1-U
HP_SPK_R1
HP_SPK_L1
R635 0R2-0
R636 0R2-0
HP_SPK_R2
HP_SPK_L2
BC306 SC270P50V3JN
BC307 SC270P50V3JN
AUDIO-JK29 22.10088.541
01/27/2004
Change from 150u to 220u
HEADPHONE JACK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1 of 2) -- Codec
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 24 of 39



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO (2 of 2) --Phone Jack
Size A3	Document Number MOLOKAI
Rev	SC
Date: Thursday, April 15, 2004	Sheet 25 of 39


HDD CONN
CDROM
DUMMY-0R5
R482
U77
SI3445DV-U
C395
SCD1U16V
BC225
SCD1U16V
BC221
SC10U10V5ZY
F6
FUSE-2A6V
C200
SC3D3U10V5ZY
R172
10KR2
D27
S1N4148-U
U43
NC7SZ14-U
Q28
2N7002
Q29
2N7002
R200
10KR2
U42
MAX809MEUR-T-U
Q27
DTC124EUA-U1
22 K
R198
DUMMY-0R2-0
U46A
TSLCX08-U
R147
100R2
R150
DUMMY-R2
R151
DUMMY-R2
Pull high at ICH4 side
CN9
SYN-CONN44D-4
20.F0510.044
R77
470R2
R602
DUMMY-1KR2
02/10/2004
C339
SCD1U10V2MX-1
C340
SC4D7U10V5ZY
C491
SC10U10V5ZY
D32
SSM34A
CLOSE TO PIN
IDE1
FOX-CONN50-2
R171
10KR2
C194
C201
C193
SCD1U16V
Optical Bay ID,00 CDROM;01 2nd-HDD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDD/CD ROM
Size
A3
Document Number
MOLOKAI
Rev
SC
Date: Thursday, April 15, 2004
Sheet 26 of 39

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

Unused FGPI pins must not be float

RN29
SELECT_FWH
FWH_FGPI4
SRN10K-2

RN28
FWH_FGPI3
FWH_FGPI2
FWH_FGPI1
FWH_FGPI0
SRN10K-2

7,15,17,18,19,20,21,23,28 PCIRST#_3

R585
68R2

SB: Because new add R684
is 330 ohm so need change
R260 from 1K to 4.7K to
make FWH_INIT# low level
be correct

3D3V_S0
1D5V_S0
R260
4K7R2
R259
1K5R2
Q33
FWH_INT_Q
MMBT3904-1-U
84.03904.B11

CC_INIT1#
R684
330R2
CC_INIT# 5,17
SB: for SIV pass

U55
NC
VSS
IC
A10/FGPI4
R/C#(CLK)
VDD
RST#
A9(FGPI3)
A8(FGPI2)
A7(FGPI1)
A6(FGPI0)
A5(WP#)
A4(TBL#)
OE#/INIT#
WE#/FWH4
DQ7/RES
DQ6/RES
DQ5/RES
DQ4/RES
DQ3/LAD3
VSS
DQ2/LAD2
DQ1/LAD1
DQ0/LAD0
A0/ID0
A1/ID1
A2/ID2
A3/ID3
49LF004A-33

FWH_INIT#
LPC_LFRAME# 17,28
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
LPC_LAD[3..0] 17,28

3 PCLK_FWH
R262
10R2
R240
10KR2
63.10334.1D1
PCLK_FWH_2
16 FWH_WP#
BC163
SC10P50V2JN-1

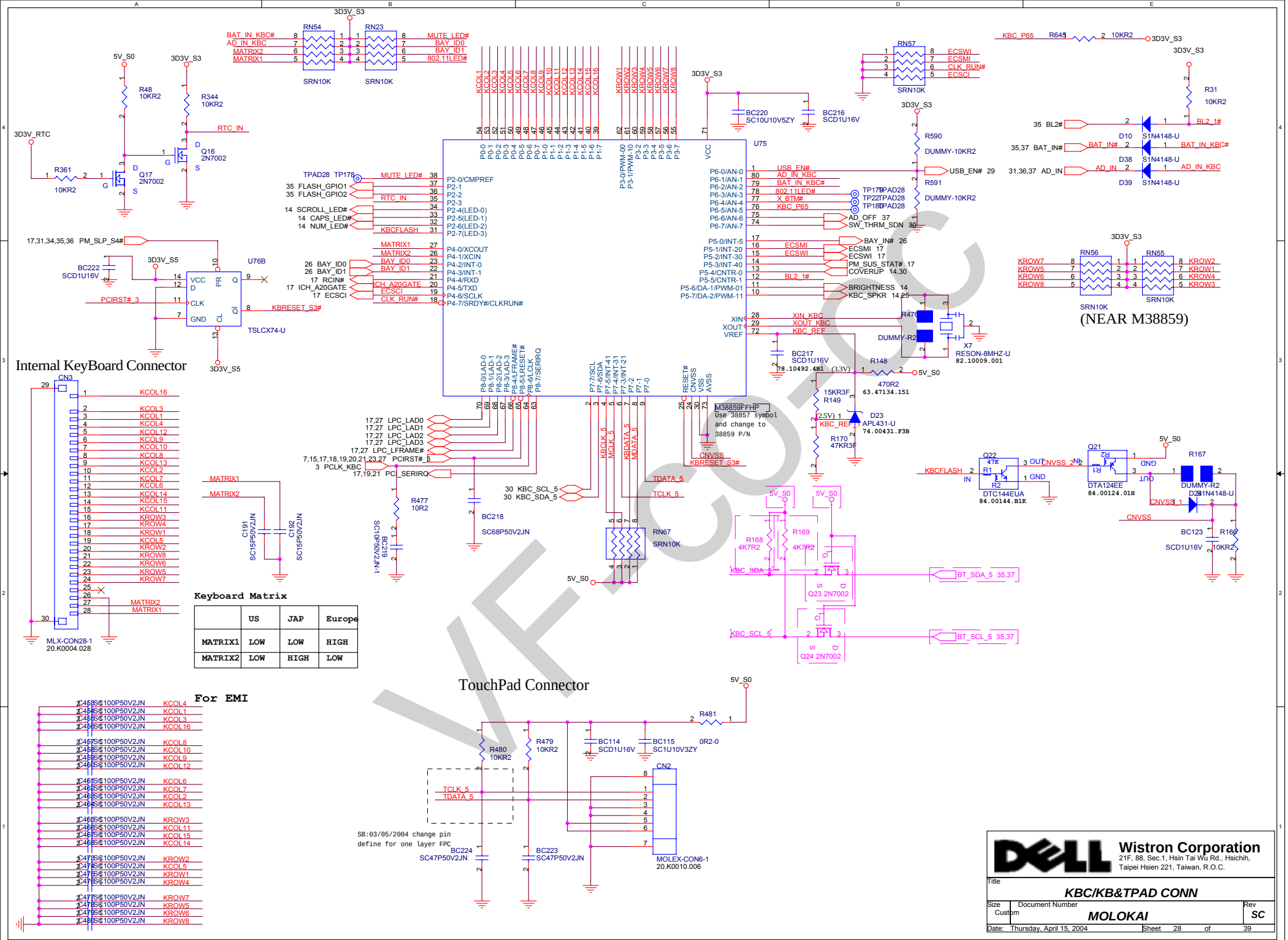
3D3V_S0

BC162
DUMMY-SC10U10V5ZY
BC149
BC158
BC157
BC150
SCD1U10V2MX-1
78.10492.4B1

3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,29,30,31,32,36,38,39 3D3V_S0
5V_S0
13,14,17,18,19,20,24,26,28,30,32,34,36,38,39 5V_S0
1D5V_S0
7,8,9,15,16,18,38,39 1D5V_S0

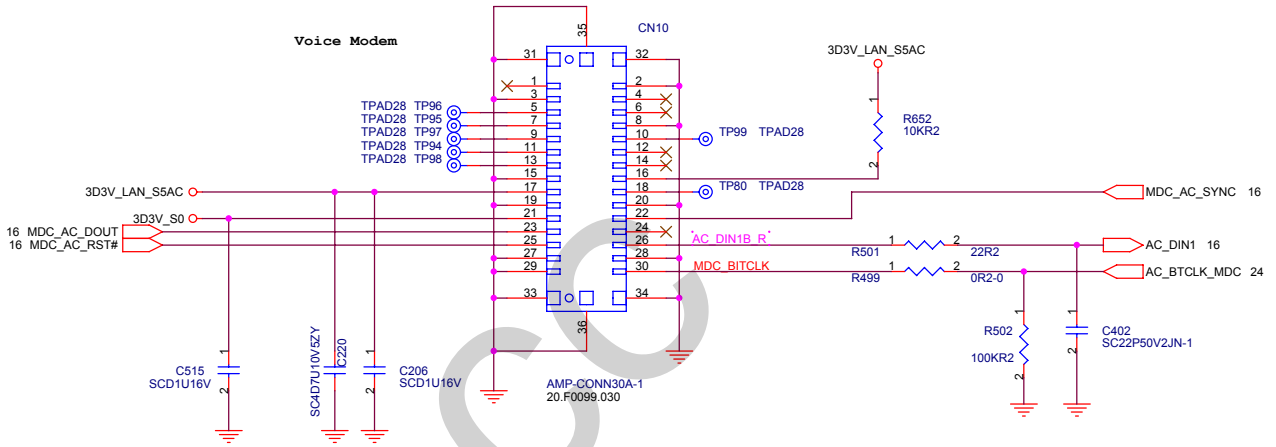
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH/Debug Port
Size: A3
Document Number: MOLOKAI
Rev: SC
Date: Thursday, April 15, 2004
Sheet 27 of 39

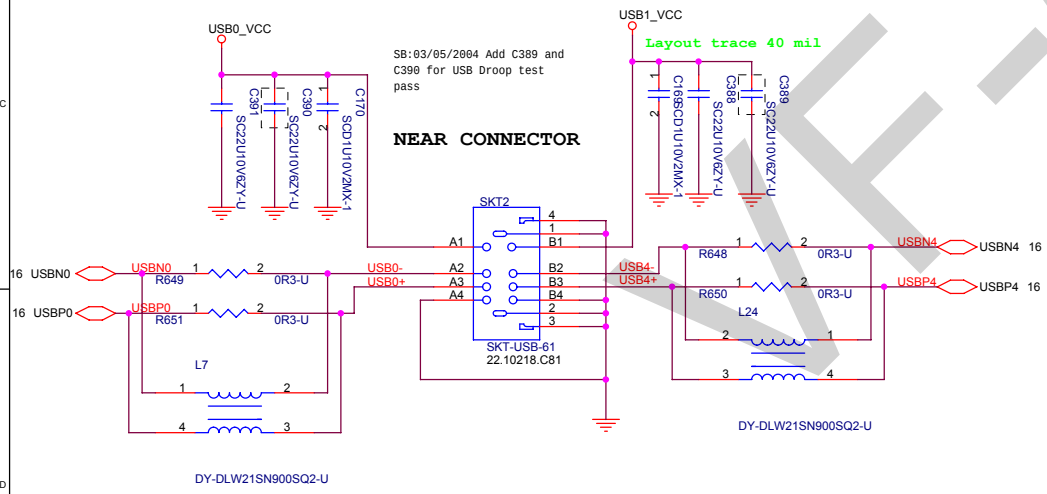


	US	JAP	Europe
MATRIX1	LOW	LOW	HIGH
MATRIX2	LOW	HIGH	LOW

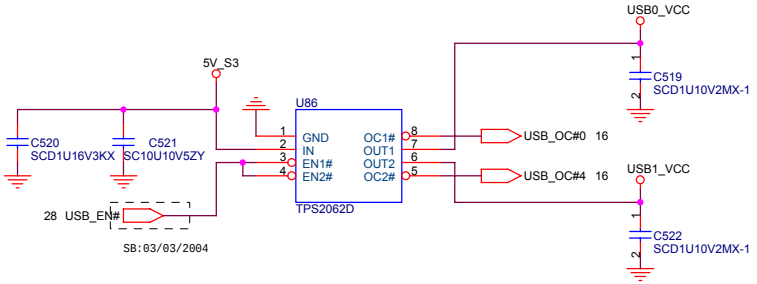
MDC CONN



USB PORT



Dual USB switch



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	MDC CONN & USB CONN	
Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 29 of 39	

240 ms after VCC_G768 > 4.38v

Check default setting, default enable is preferred

FAN Conn.

THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768D

SYSTEM SENSOR

put together

32K suspend clock output

SC:change TEMP setting from 85 to 105 degree.

HW thermal shut down tempature setting 105 degree . Put Near vent out .

COVER SWITCH

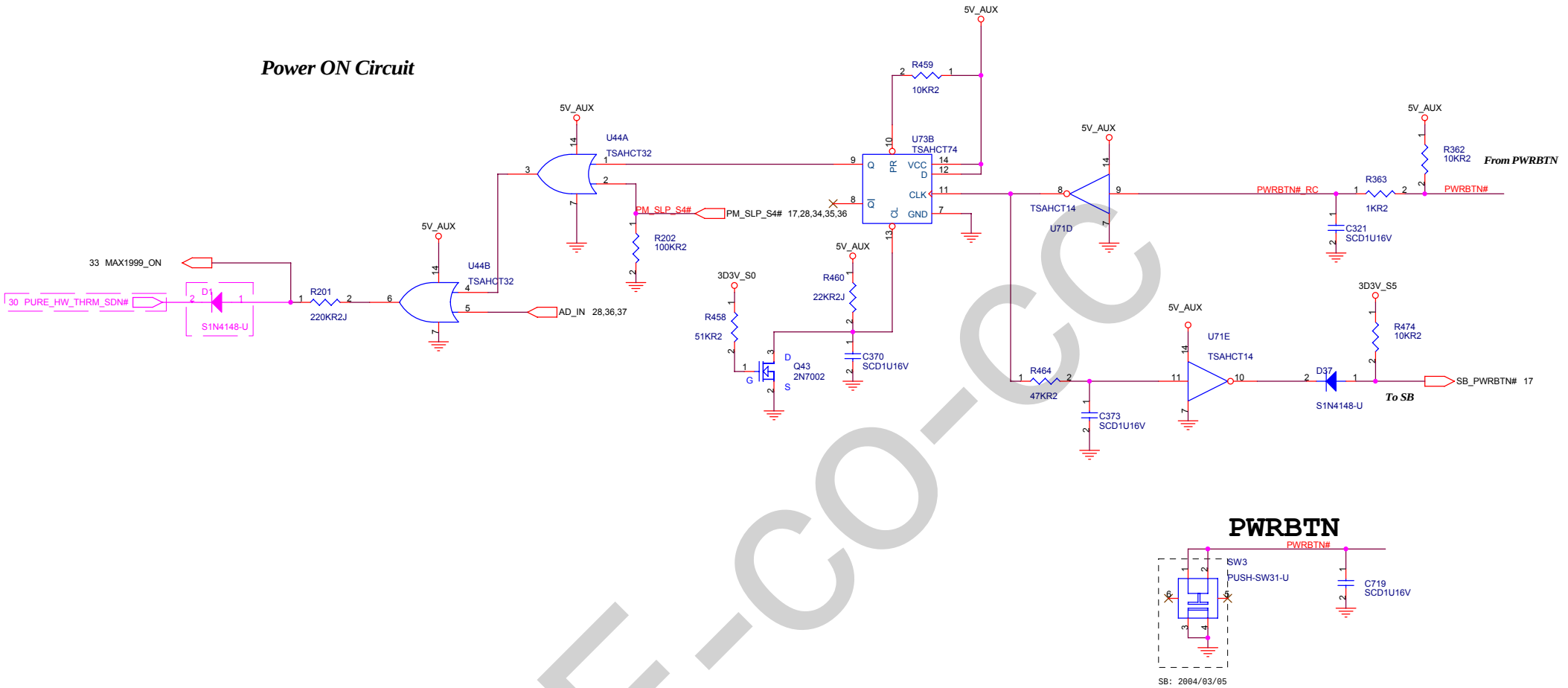
TO KBC

RESUME RESET

TO SB

RSMRST# is RTC power plane

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G768D		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 30 of 39	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON CIRCUIT

Size	Document Number	Rev
A3	MOLOKAI	SC

Date: Thursday, April 15, 2004 Sheet 31 of 39

Deep Sleep
100k/(100k+1.21k)=98.79%
OffSet= 1.21%

	Active	Deep	Deeper
DPRSLPVR	0	0	1
STP_CPU#	1	0	0

IFL=(RISEN*32uA*n) / Rds(on)=
1.96k*32uA*2 / 5mR =25.157A
FDS7088N3 Rds(on)=5mR

MAX=14A

MAX=21A
Vf=0.7V

PWRCH Low ==> One Phase

ISL6218

ISL6218CV-T

IMVP IV
Load Line Slope :3mR
32A=> 96mV
Rdroop = 96mV /
32uA

V_OCSET = 1.75V
V_DRSV = 0.75716V
V_BOOT =1.2611V
I_OCSET = 12.5uA =>
OCP =125% ~ 175%

For Banias/ULV CPU:

Active Mode:
1.Highest Frequency:
VID=1.484V/1.00V
2.Lowest Frequency:
VID=0.956V/0.85V

Deep Sleep Mode:
1.Highest Frequency: VID=1.484V,Offset=-1.2%->VID=1.466
2.Lowest Frequency: VID=0.956V,Offset=-1.2%->VID=0.945

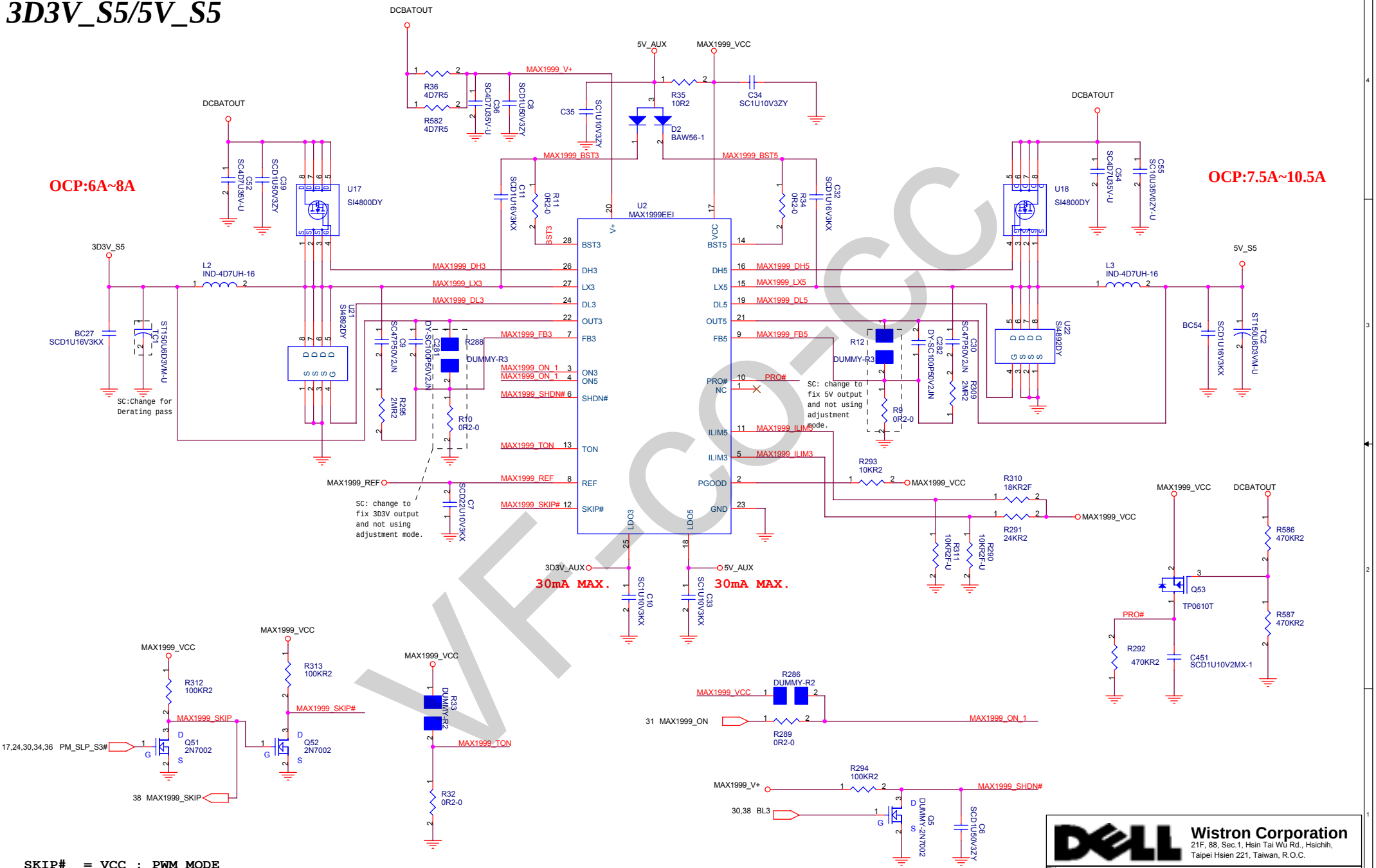
Deeper Sleep Mode:
VID=0.748V

VCC_IO_S0-->Delay 3 mS-->CPUCORDE_ON_DELAY

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *IMVP IV-CPU POWER-ISL6218*
Size: A3 | Document Number: *MOLOKAI* | Rev: *SC*
Date: Thursday, April 15, 2004 | Sheet 32 of 39

SYSTEM DC/DC
3D3V_S5/5V_S5

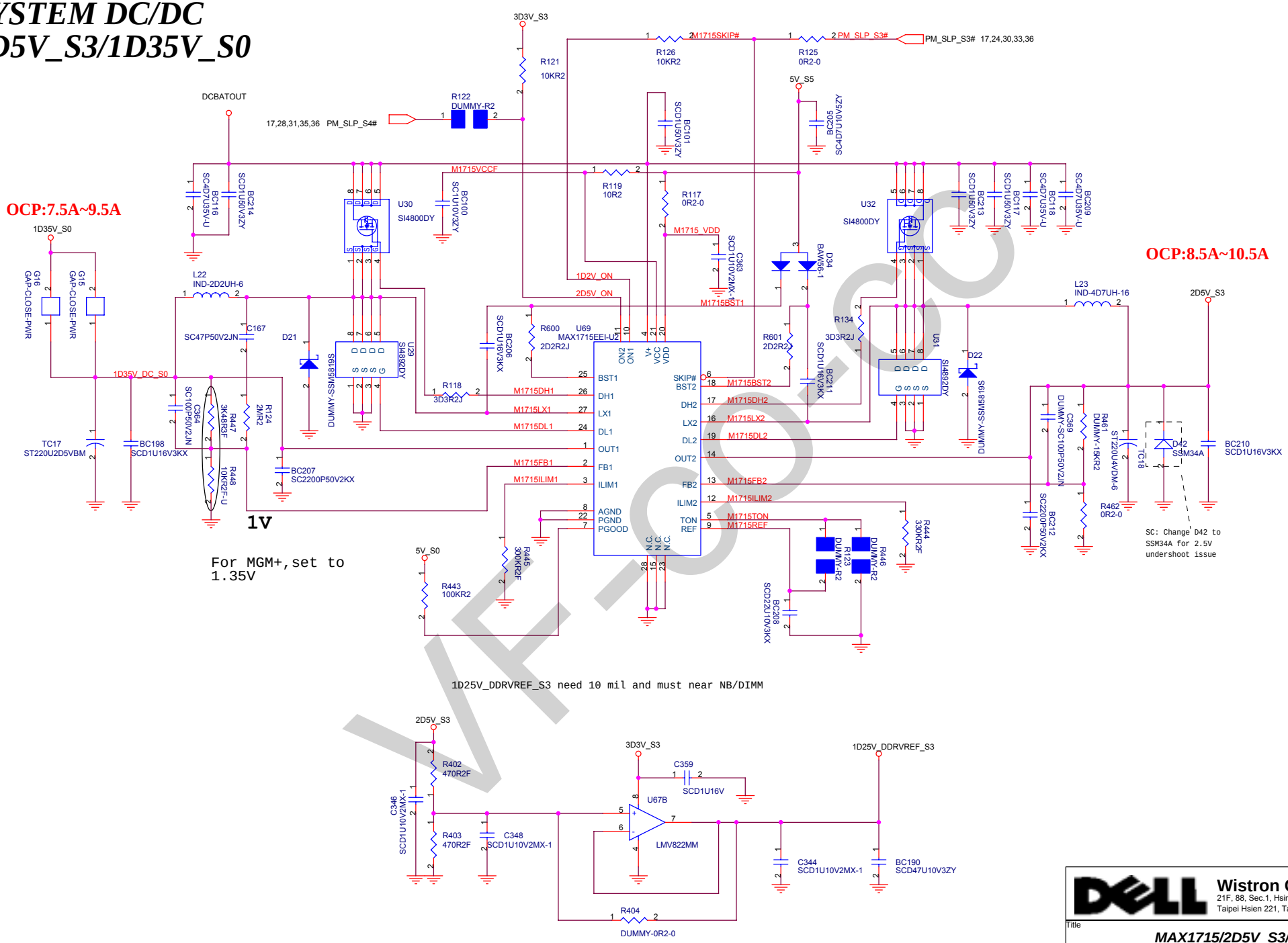


SKIP# = VCC : PWM MODE
SKIP# = GND : SKIP MODE
SKIP# = REF/FloatING : Ultrasonic MODE (25KHz min)

Ton = VCC : 200KHz/300KHz
Ton = GND : 400KHz/500KHz (5V/3D3V)

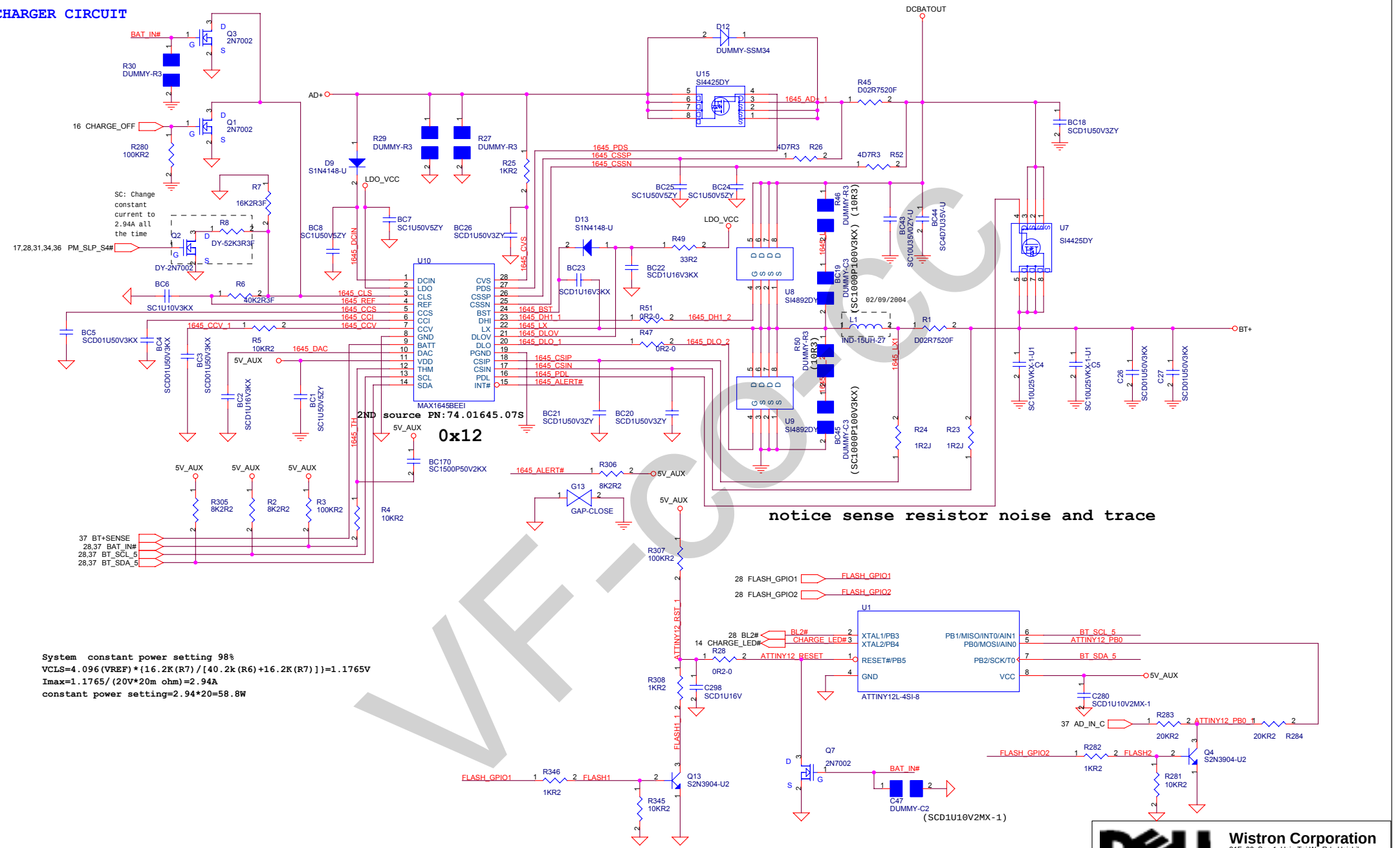
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MAX1999/3D3V_S5/5V_S5		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 33 of 39	

SYSTEM DC/DC
2D5V_S3/1D35V_S0



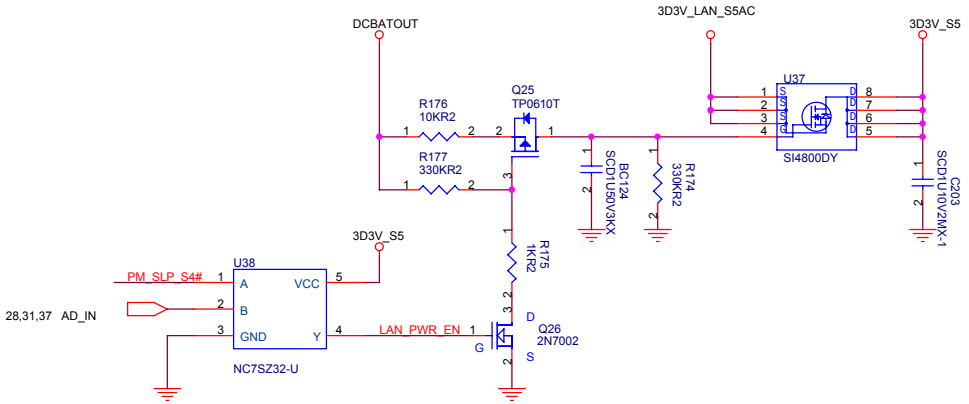
Wistron Corporation	Title	MAX1715/2D5V_S3/1D35V_S0	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	Size A3	Document Number MOLOKAI	Rev SC
	Date: Thursday, April 15, 2004	Sheet 34 of 39	

CHARGER CIRCUIT

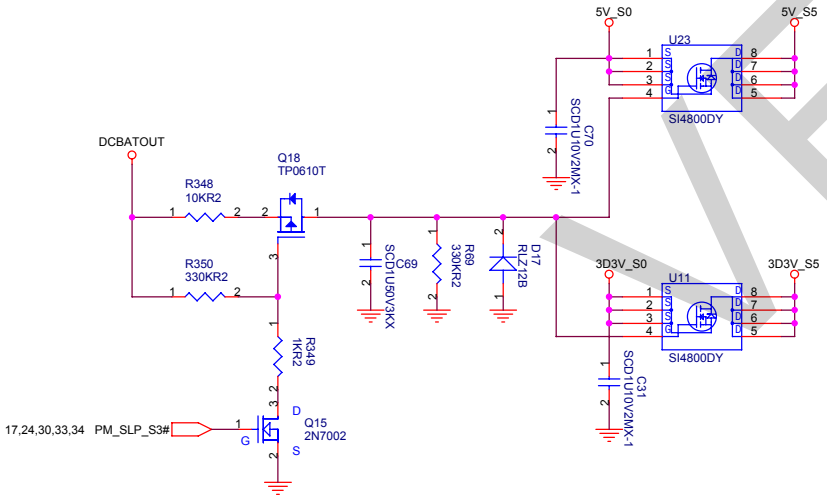


Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CHARGER&MicroP		
Size: Custom	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 35 of 39	

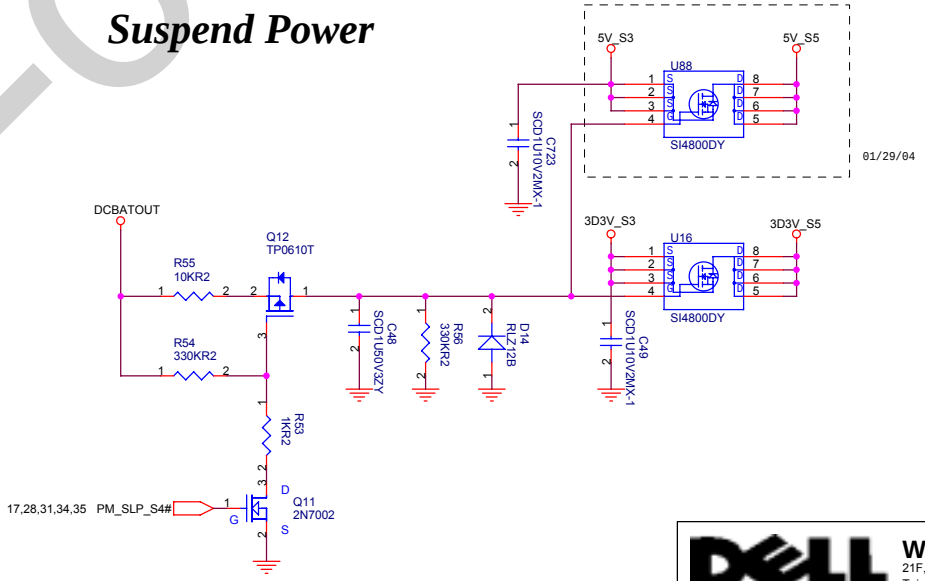
LAN Power



Run Power

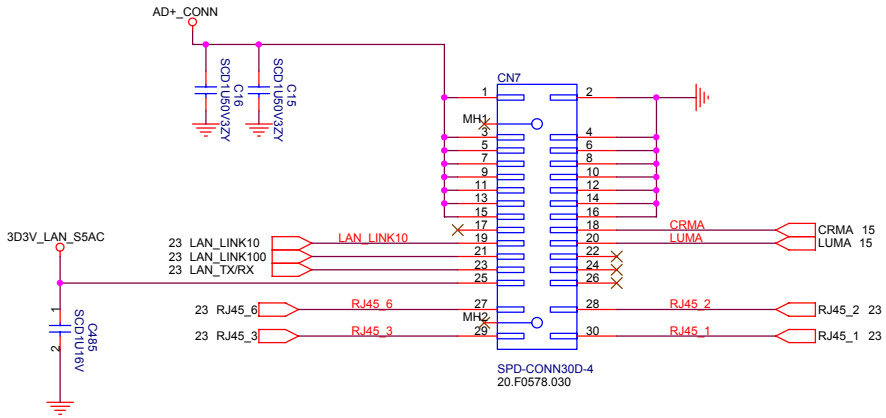


Suspend Power

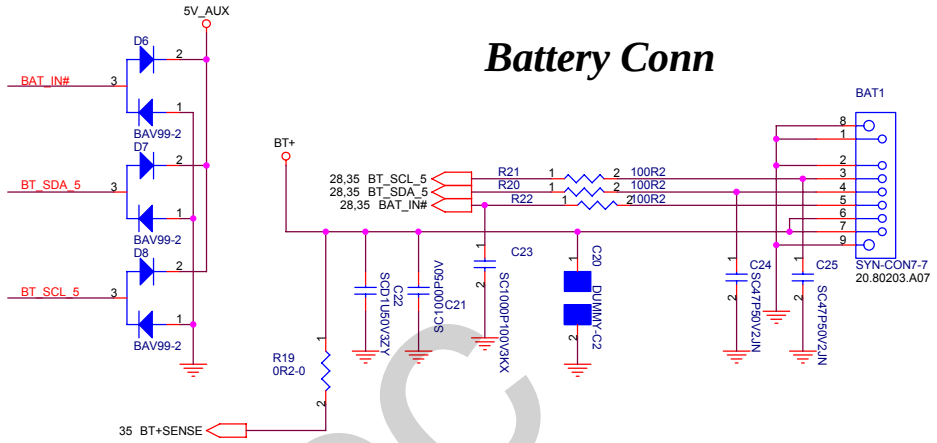


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWR Plane SW / VCC_IO_S0		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 36 of 39	

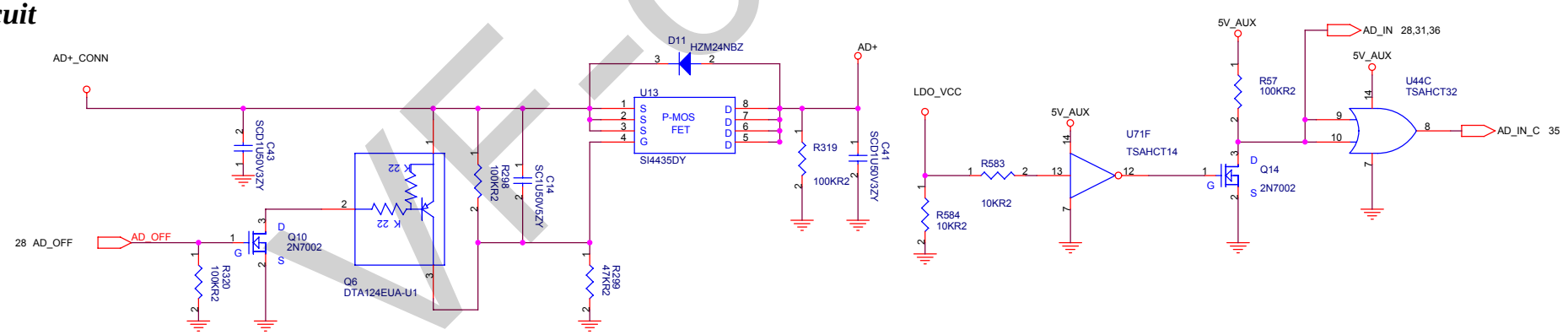
TV BD Conn



Battery Conn

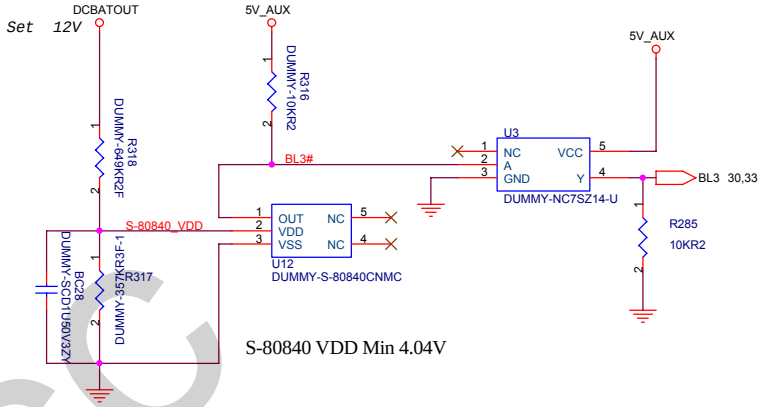


Adaptor In Circuit



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Battery Conn/TV BD Conn/Adaptor In Circuit
Size A3	Document Number MOLOKAI
Rev	SC
Date: Thursday, April 15, 2004	Sheet 37 of 39

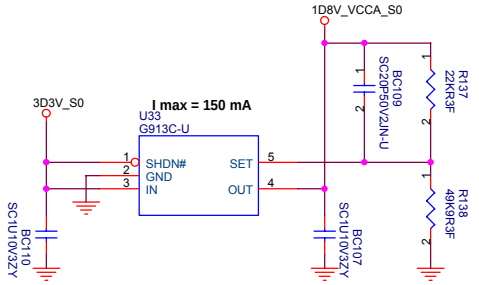
BATRERY LOW3 DETECTOR



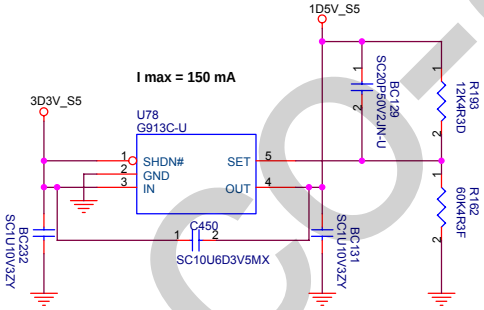
S-80840 VDD Min 4.04V

At Dothan CPU application, POWER is 1.5V or 1.8V.

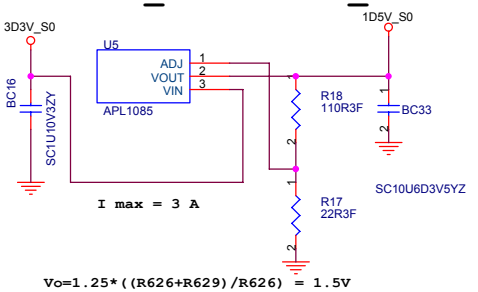
3D3V_S0 --> 1D8V_VCCA_S0 (For CPU VCCA)



3D3V_S5 --> 1D5V_S5

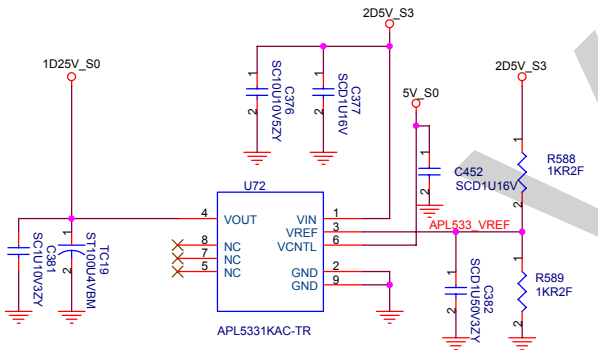


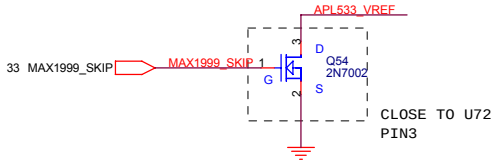
3D3V_S0 → 1D5V_S0



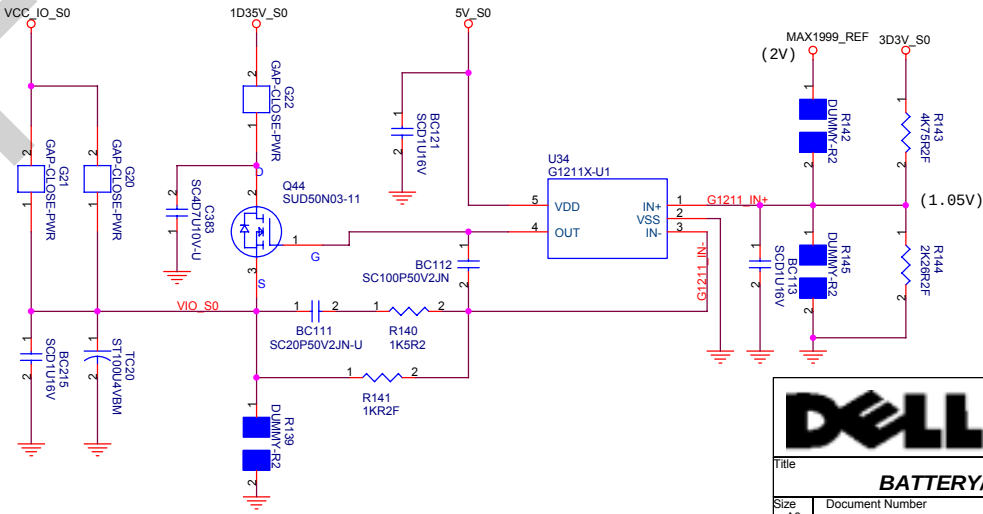
Vo=1.25*((R626+R629)/R626) = 1.5V

2D5V_S3 → 1D25V_S0

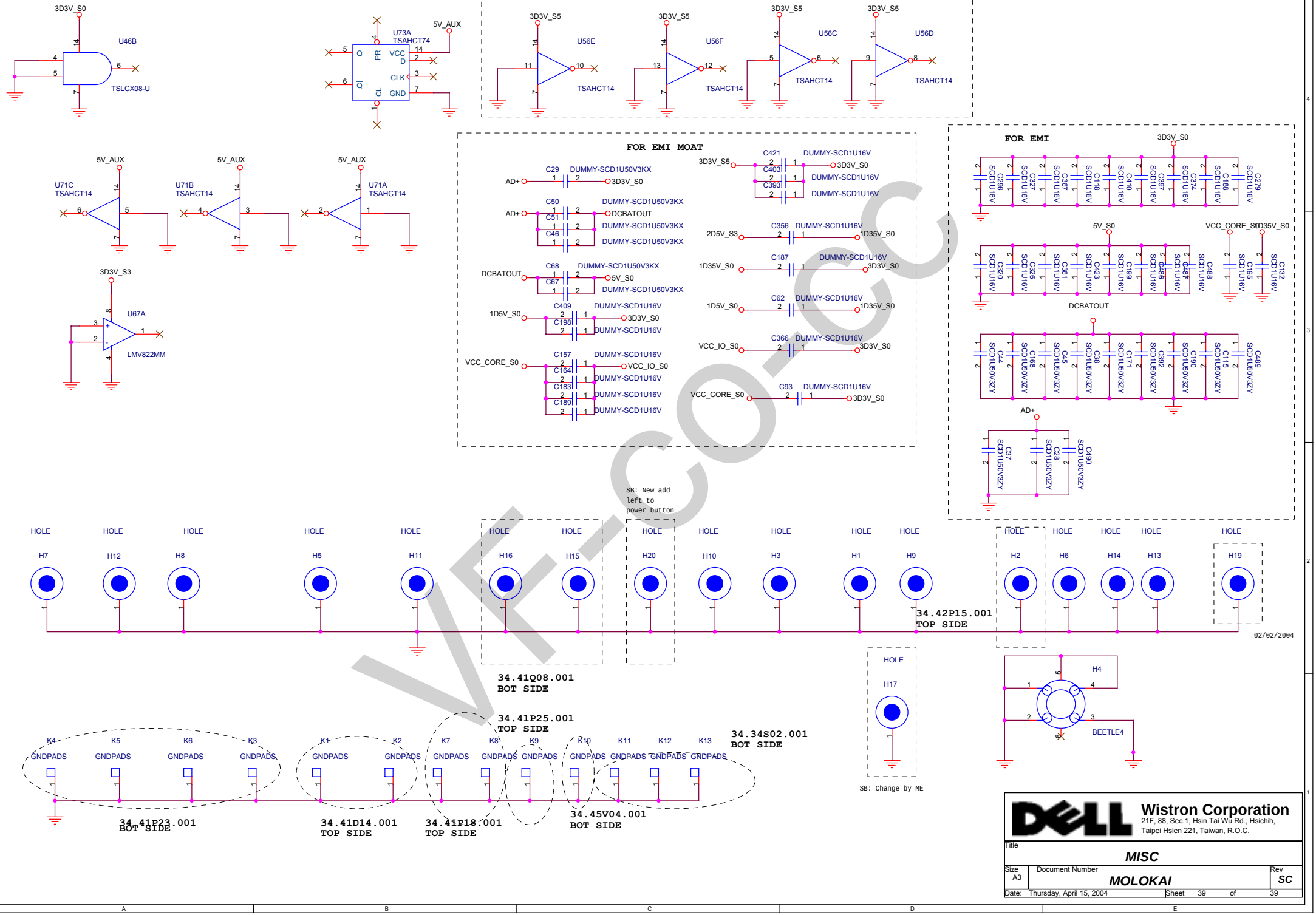




1D35V_S0 → VCC_IO_S0(1.05V)



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATTERY/LDO/Adaptor In		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 38 of 39	



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MISC	
Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 39 of 39	