Parker Block Diagram

Project code:91.4S701.001
PCB P/N :48.4S701.001
REVISION :06240-1

CPU
- U1400 FW289
- U1500 UP954
- U7500 JW620
- U7600 FW418

Clock Generator ICS 951463 4

Intel Mobile CPU
Yonah / Merom ULV
FSB:533Mhz
5,6

HOST BUS | FSB 533MHz

12.1WXGA 17 — LVDS

RS600ME
DUAL DDR2 CHANNEL
INTEGRATED GRAPHICS
PCI-EXPRESS(4)
LVDS
7,8,9,10,11

DDRII 533/667MHz — ON-BOARD RAM 1G CELL X 8 12,13,14
DDRII 533/667MHz — UNBUFFERED DDR2 SODIMM Socket 15

200-PIN DDR2 SODIMM
Support Aero Glass

SDVO

CRT Port 16 — RGB CRT

CRT

PCI Express (4)
- Power Switch 31
  - Express Card Slot 54mm PORT6 PCIE3 31
  - Mini-Card WWAN PORT9 PCIE1 32 — SIM CONN 32
  - Mini-Card 802.11a/g/n PCIE2 32
  - Biometric PORT5 17
  - Bluetooth PORT7 31
  - USB*2 PORT0.1 P-USB*1 PORT2 34
  - Digi Tizer PORT3 17
  - BCM5756ME Giga LAN — RJ45 CONN 28
  - TPM 1.2 PCIE0 27

ALINK x4

Thermal Sensor EMC4001 23

PATA HDD 33 — IDE

ATI SB600
USB 2.0/1.1 ports (10)
High Definition Audio
ATA 66/ 100/133
SATA2 (4)
LPC I/F
PCI/PCI BRIDGE
ACPI 2.0
SPI
18,19,20,21,22

1394 CONN 26 — 1394
SD card 26 — 8 in1
TI 7402 Card reader 1394 2 port 24,25 — PCI BUS

USB2.0 (10)

AZALIA

MIC IN
Digital MIC Array
Azalia CODEC STAC 9205 29

LINE OUT
INT.SPKR
Speaker AMP. Headphone AMP. TI TPA6040A4 30

SPI

LPC

BIOS SPI FLASH 2MB 33 — SPI
EC SMSC MEC5025 35
SIO Expander SMSC ECE5021 36

SMBus

Touch Pad 37
KBC SMSC ECE1077 37
Int. KB 37

DVI CRT | S/PDIF | SMBus | USB 2.0 PORT8 | RJ45

Media-Slice 38

Battery Charger ISL88731 39,40

INPUTS	OUTPUTS
+PWR_SRC	+PBATT

CPU DC/DC ADP3207 42

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

System DC/DC ISL6236/MAX8778 43

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO +5V_ALW +3.3V_ALW

LDO MAX8794 44

+1.8V_SUS	+1.5V_RUN

LDO TPS51100 44

+1.8V_SUS	+0.9V_DDR_VTT V_DDR_NB_REF

System DC/DC ISL6236/MAX8778 45

+PWR_SRC	+1.8V_SUS +1.05V_VCCP

System DC/DC ISL6236/MAX8778 46

+PWR_SRC	+NB_VCORE +1.2V_SUS

PCB LAYER

L1:TOP
L2:Signal
L3:GND
L4:Signal
L5:GND
L6:VCC
L7:Signal
L8:GND
L9:Signal
L10:BOTTON

08/14/2007

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Parker | Rev: -1
Date: Tuesday, August 14, 2007 | Sheet 1 of 53

CLK-GEN ICS951463

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CLKREQA# B# C# MAP

CLKREQA#	CLKSRC 7 NB ALINK
	CLKSRC 5 EXPRESS CARD
	CLKSRC 6 SB ALINK
CLKREQB#	CLKSRC 2 WLAN
	CLKSRC 4 LOM
CLKREQC#	CLKSRC 0 WWAN
	ATIGCLK 1 NB-PCIEX16
	ATIGCLK 2 NO -USED

ATI NB-RS600ME STRAP PIN

Strap name	LOW 0	HIGH 1
NB_VSYNC (DAC_VSYNC: STRAP_MOBILE_GFX)	DESKTOP GRAPHICS DEVICE	MOBILE GRAPHICS DEVICE ★
NB_HSYNC (DAC_HSYNC: STRP_INTGFX_DISABLE)	ENABLE ★	DISABLE
NB_SDVO_CTRLDATA (DDC_DATA: STRAP_MEMVMODE)	DDR3	DDR2 ★
STRP_DATA (STRP_DATA: STRP_MEMSTRAPS)	SELECT MEMORY CHA A AS DEBUG BUS	NORMAL MODE ★

SR600ME PCIE route

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD

ATI SB-SB600 STRAP PIN

Strap name	LOW 0	HIGH 1
AC_SDOUT SB_AC_SDOUT	IGNORE DEBUG STRAPS ★	DEBUG STRAPS Default
RTC_CLK SB_RTCCLK	EXTERNAL RTC	INTERNAL RTC ★ Default
PCI_CLK4 CLK_SB_PCI4	EXTERNAL 48MHZ ★ Default	INTERNAL PLL48
PCI_CLK6 CLK_SB_PCI6	INTEL CPU ★ Default	AMD CPU

PCI_CLK0 CLK_SB_PCI0	PCI_CLK1 CLK_SB_PCI1	ROM TYPE
0	0	FWH
0	1	LPC Default
1	0	SPI
1	1	PCI

USB TABLE

USB0	Ext Side 1
USB1	Ext Side 2
USB2	POWER USB
USB3	Digi Tizer
USB4	
USB5	Biometric
USB6	Express Card
USB7	BLUETOOTH
USB8	Media Slice
USB9	MiniCard WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MEDIACARD	AD17	G H	1	1

PCI-CLK route

PCICLK 2	MEC5025
PCICLK 5	BCM5756ME
PCICLK 6	TI7402

TABLE OF CONTENTS

SMBUS TABLE

SMBUS TABLE

SOURCE	SIGNAL NAME	LINKED DEVICES
RS600ME	I2C_CLK/DAC_SDA	CRT/SLICE CRT
	I2C_CLK/I2C_DATA	LVDS
	I2C_CLK/DDC_SDA	DVI
SB600	SCL1/SDA1	LAN / WLAN / WWAN / EXPRESS CARD/SO-DIMM
MEC5025	AB1A_CLK/AB1A_DATA	SLICE CONN.
	AB1B_CLK/AB1B_DATA	INVERTER / LIGHT SENSOR
	AB1C_CLK/AB1C_DATA	BATTERY CONN.
	AB1D_CLK/AB1D_DATA	BATTERY-SLICE CONN.
	AB1E_CLK/AB1E_DATA	P-USB / CHARGER / THERMAL
	AB1H_CLK/AB1H_DATA	CLK-GEN
	IMCLK/IMDAA	TOUCH PAD

EMC4001 Thermal sensor mapping

D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

<Variant Name>

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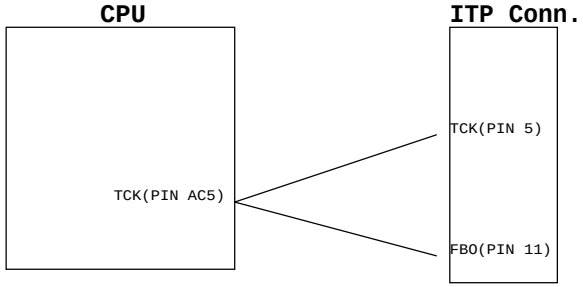
Title: Table Contsnt

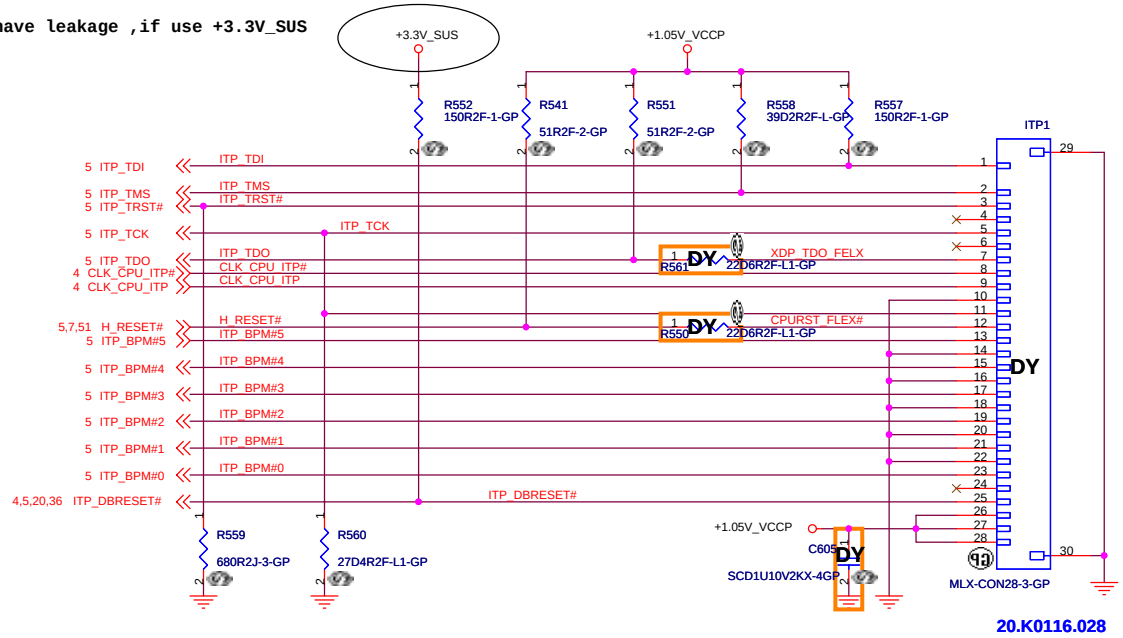
Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 2 of 53

SSID = CPU



clk-gen may have leakage ,if use +3.3V_SUS



H_CPURST# use pull-up Resistor close ITP connector 500 mil (max)

+1.05VRUN use Decoupling Capacitor close ITP connector 100 mil (max)

ITP Debug Conn.

<Variant Name>

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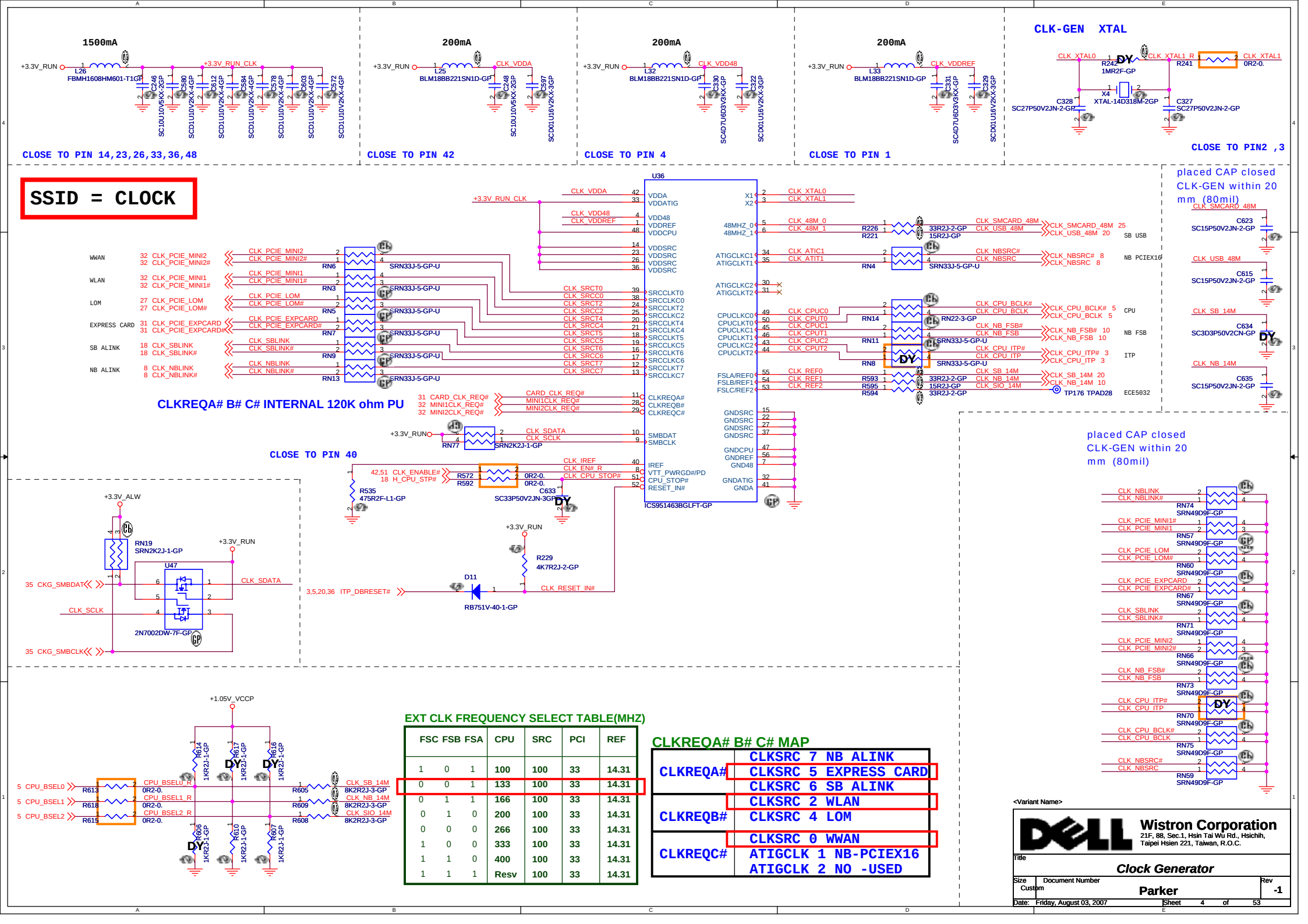
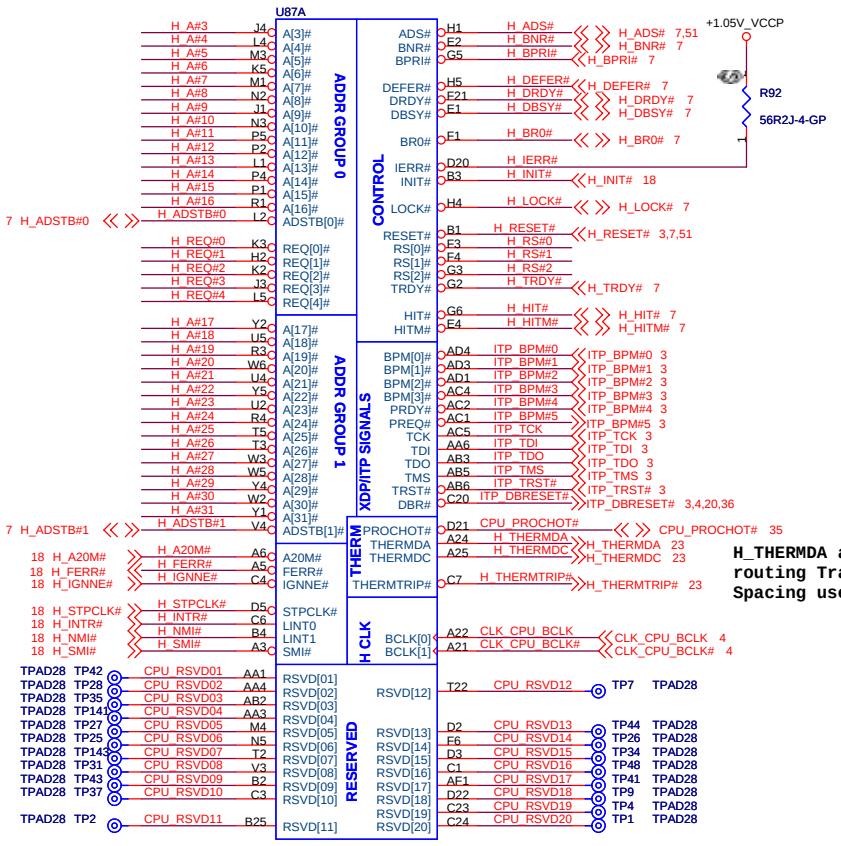
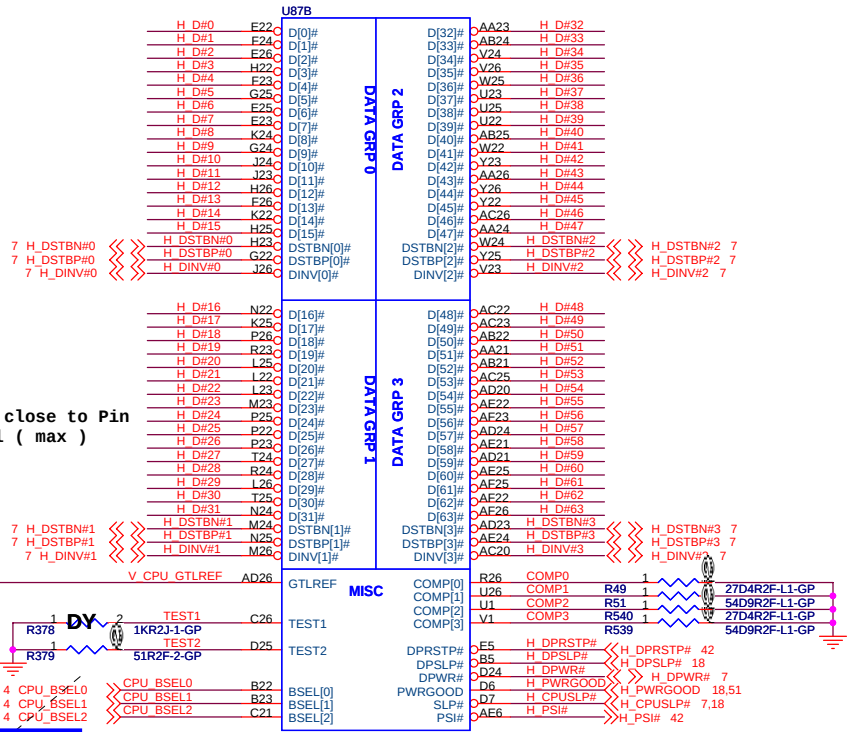
Title	*ITP Debug*	
Size A3	Document Number: Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 3 of 53	

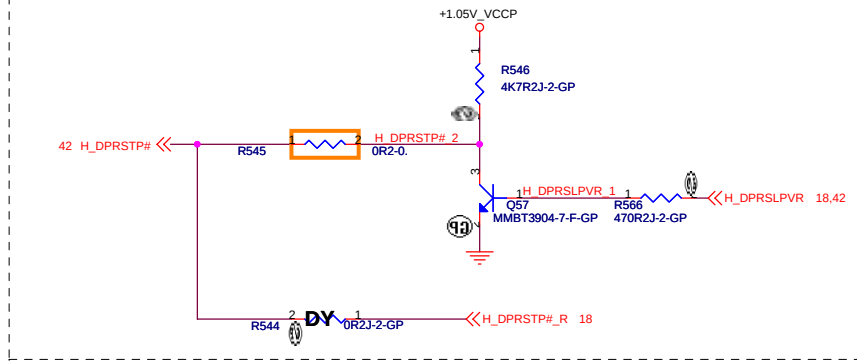

1500mA
+3.3V_RUN
L26
FBMH1608HM601-T1GP
+3.3V_RUN_CLK
C246
SC10U10V5KX-2GP
C580
C612
C584
C578
C603
C572
SCD1U10V2KX-4GP
CLOSE TO PIN 14,23,26,33,36,48
200mA
+3.3V_RUN
L25
BLM18BB221SN1D-GP
CLK_VDDA
C248
C597
SC10U10V5KX-2GP
SCD01U16V2KX-3GP
CLOSE TO PIN 42
200mA
+3.3V_RUN
L32
BLM18BB221SN1D-GP
CLK_VDD48
C330
C322
SC47U6D3V3KX-GP
SCD01U16V2KX-3GP
CLOSE TO PIN 4
200mA
+3.3V_RUN
L33
BLM18BB221SN1D-GP
CLK_VDDREF
C331
C329
SC47U6D3V3KX-GP
SCD01U16V2KX-3GP
CLOSE TO PIN 1
CLK-GEN XTAL
CLK_XTAL0
R242
1MR2F-GP
DY
CLK_XTAL1_R
R241
0R2-0.
CLK_XTAL1
X4
XTAL-14D318M-2GP
C328
SC27P50V2JN-2-GP
C327
SC27P50V2JN-2-GP
CLOSE TO PIN2 ,3
SSID = CLOCK
U36
ICS951463BGLFT-GP
VDDA
VDDATIG
VDD48
VDDREF
VDDCPU
VDDSRC
SRCCLKT0
SRCCLKC0
SRCCLKT2
SRCCLKC2
SRCCLKT4
SRCCLKC4
SRCCLKT5
SRCCLKC5
SRCCLKT6
SRCCLKC6
SRCCLKT7
SRCCLKC7
CLKREQA#
CLKREQB#
CLKREQC#
SMBDAT
SMBCLK
IREF
VTT_PWRGD#/PD
CPU_STOP#
RESET_IN#
GNDSRC
GNDCPU
GNDREF
GND48
GNDATIG
GNDA
X1
X2
48MHZ_0
48MHZ_1
ATIGCLKC1
ATIGCLKT1
ATIGCLKC2
ATIGCLKT2
CPUCLKC0
CPUCLKT0
CPUCLKC1
CPUCLKT1
CPUCLKC2
CPUCLKT2
FSLA/REF0
FSLB/REF1
FSLC/REF2
CLK_XTAL0
CLK_XTAL1
CLK_48M_0
CLK_48M_1
CLK_ATIC1
CLK_ATIT1
CLK_CPUC0
CLK_CPUT0
CLK_CPUC1
CLK_CPUT1
CLK_CPUC2
CLK_CPUT2
CLK_REF0
CLK_REF1
CLK_REF2
WWAN
WLAN
LOM
EXPRESS CARD
SB ALINK
NB ALINK
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_LOM
CLK_PCIE_LOM#
CLK_PCIE_EXPCARD
CLK_PCIE_EXPCARD#
CLK_SBLINK
CLK_SBLINK#
CLK_NBLINK
CLK_NBLINK#
SRN33J-5-GP-U
RN6
RN3
RN5
RN7
RN9
RN13
CLK_SRCT0
CLK_SRCC0
CLK_SRCT2
CLK_SRCC2
CLK_SRCT4
CLK_SRCC4
CLK_SRCT5
CLK_SRCC5
CLK_SRCT6
CLK_SRCC6
CLK_SRCT7
CLK_SRCC7
CLK_SMCARD_48M
CLK_USB_48M
33R2J-2-GP
15R2J-GP
R226
R221
SB USB
CLK_NBSRC#
CLK_NBSRC
RN4
NB PCIEX16
CLK_CPU_BCLK#
CLK_CPU_BCLK
RN14
RN22-3-GP
CPU
CLK_NB_FSB#
CLK_NB_FSB
RN11
NB FSB
CLK_CPU_ITP#
CLK_CPU_ITP
RN8
ITP
CLK_SB_14M
CLK_NB_14M
CLK_SIO_14M
R593
R595
R594
TP176 TPAD28
ECE5032
placed CAP closed
CLK-GEN within 20
mm (80mil)
C623
SC15P50V2JN-2-GP
C615
SC15P50V2JN-2-GP
C634
SC3D3P50V2CN-GP
C635
SC15P50V2JN-2-GP
CLKREQA# B# C# INTERNAL 120K ohm PU
31 CARD_CLK_REQ#
32 MINI1CLK_REQ#
32 MINI2CLK_REQ#
CARD_CLK_REQ#
MINI1CLK_REQ#
MINI2CLK_REQ#
+3.3V_RUN
RN77
CLK_SDATA
CLK_SCLK
SRN2K2J-1-GP
CLOSE TO PIN 40
42,51 CLK_ENABLE#
18 H_CPU_STP#
R572
R592
0R2-0.
CLK_IREF
CLK_EN#_R
CLK_CPU_STOP#
R535
475R2F-L1-GP
C633
SC33P50V2JN-3GP
DY
+3.3V_ALW
RN19
SRN2K2J-1-GP
+3.3V_RUN
U47
2N7002DW-7F-GP
35 CKG_SMBDAT
CLK_SDATA
CLK_SCLK
35 CKG_SMBCLK
+3.3V_RUN
R229
4K7R2J-2-GP
D11
RB751V-40-1-GP
3,5,20,36 ITP_DBRESET#
CLK_RESET_IN#
placed CAP closed
CLK-GEN within 20
mm (80mil)
CLK_NBLINK
CLK_NBLINK#
RN74
SRN49D9F-GP
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
RN57
CLK_PCIE_LOM
CLK_PCIE_LOM#
RN60
CLK_PCIE_EXPCARD
CLK_PCIE_EXPCARD#
RN67
CLK_SBLINK
CLK_SBLINK#
RN71
CLK_PCIE_MINI2
CLK_PCIE_MINI2#
RN66
CLK_NB_FSB#
CLK_NB_FSB
RN73
CLK_CPU_ITP#
CLK_CPU_ITP
RN70
CLK_CPU_BCLK#
CLK_CPU_BCLK
RN75
CLK_NBSRC#
CLK_NBSRC
RN59
+1.05V_VCCP
5 CPU_BSEL0
5 CPU_BSEL1
5 CPU_BSEL2
R613
R618
R615
CPU_BSEL0_R
CPU_BSEL1_R
CPU_BSEL2_R
0R2-0.
1KR2J-1-GP
R614
R617
R616
R606
R610
R607
R605
R609
R608
CLK_SB_14M
CLK_NB_14M
CLK_SIO_14M
8K2R2J-3-GP
EXT CLK FREQUENCY SELECT TABLE(MHZ)
FSC FSB FSA CPU SRC PCI REF
1 0 1 100 100 33 14.31
0 0 1 133 100 33 14.31
0 1 1 166 100 33 14.31
0 1 0 200 100 33 14.31
0 0 0 266 100 33 14.31
1 0 0 333 100 33 14.31
1 1 0 400 100 33 14.31
1 1 1 Resv 100 33 14.31
CLKREQA# B# C# MAP
CLKREQA# CLKSRC 7 NB ALINK
CLKSRC 5 EXPRESS CARD
CLKREQB# CLKSRC 6 SB ALINK
CLKSRC 2 WLAN
CLKSRC 4 LOM
CLKREQC# CLKSRC 0 WWAN
ATIGCLK 1 NB-PCIEX16
ATIGCLK 2 NO -USED
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator
Size
Custom
Document Number
Parker
Rev
-1
Date: Friday, August 03, 2007
Sheet 4 of 53

SSID = CPU

IC CPU YONAH U1500 1.33G BGA--P/N:UP954
IC CPU MEROM U7500 1.06G BGA--P/N:JW602
IC CPU YONAH U1400 1.2G BGA--P/N:FW289



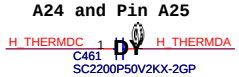


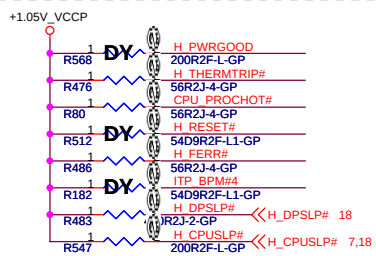


H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

CPU_GTLREF0 close to Pin AD26 500 mil (max)

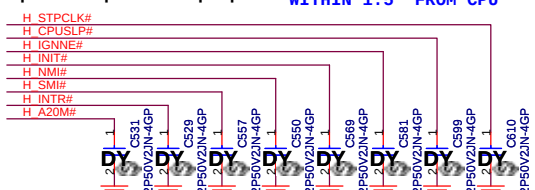
C126 close to Pin A24 and Pin A25





place cap close cpu pin

THESE CAPS PLACE WITHIN 1.5" FROM CPU



Yonah support

Change R846 to 51 ohm and Populate R843 for Yonah B0 Forward

Parker will use B0 version or later version

This resistor is needed for Yonah but not for Meorm.

CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.Trace should be No Longer than 500 mils

<Variant Name>

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Title: CPU - 01 - Yonah - FSB

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 5 of 53

SSID = CPU

Merom (Dual Core)

All Pop

Yahon (Signal Core)

De-pop C91, 93, 123, 127, 166, 169, 191 and 193

22uF 0805 X5R -> 85 degree C ,
Or better such As X6S and X7R

Please these inside socket cavity on L8 (North side Secondary)

Place R50 and R51 near CPU
Routing VCC_SENSE and VSS_SENSE at
27.4 ohms,50 mils spacing,1 inch.

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - 02 - Yonah - POWER

Size: A3 | Document Number: Parker | Rev: -1

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SSID = N.B

+1.8V_RUN_NB_IOPLLVDD18

200mA

+1.8V_RUN — L20 BLM18BB221SN1D-GP — +1.8V_RUN_NB_IOPLLVDD18 — C168 SC2D2U6D3V3MX-1-GP

Place close pin AA35

+1.2V_RUN_NB_IOPLLVDD12

200mA

+1.2V_RUN — L13 BLM18BB221SN1D-GP — +1.2V_RUN_NB_IOPLLVDD12 — C133 SC2D2U6D3V3MX-1-GP

Place close pin V35

+1.05V_VCCP_NB_CPU_VREF

+1.05V_VCCP — R84 61D9R2F-GP — +1.05V_VCCP_NB_CPU_VREF — R76 127R2F-GP — C43 SC1U6D3V2KX-GP — C44 SC220P50V2JN-3GP

width/space: 10/10

Place close pin A32

NB_TEST_MODE

+3.3V_RUN_NB — R52 4K7R2J-2-GP (DY) — NB_TEST_MODE — R56 4K7R2J-2-GP

TESTMODE	RS600MODE
HIGH	TEST MODE
LOW	NORMAL MODE

NB THERMAL DIODE

CAP close to NB pin

NB_THERMDP — C239 SC2200P50V2KX-2GP (DY) — NB_THERMDN

H_RS#[2..0] — H_RS#[2..0] 5
H_D#[63..0] — H_D#[63..0] 5
H_A#[31..3] — H_A#[31..3] 5
H_REQ#[4..0] — H_REQ#[4..0] 5

U91A 1 OF 7

ADDR GROUP 0: H_A#3 M42, H_A#4 K42, H_A#5 M44, H_A#6 T39, H_A#7 M38, H_A#8 P42, H_A#9 T43, H_A#10 P38, H_A#11 P44, H_A#12 P36, H_A#13 W39, H_A#14 V40, H_A#15 W42, H_A#16 V42, H_REQ#0 P39, H_REQ#1 M39, H_REQ#2 K44, H_REQ#3 H42, H_REQ#4 K40, H_ADSTB#0 T42 — 5 H_ADSTB#0

ADDR GROUP 1: H_A#17 AC39, H_A#18 W43, H_A#19 V44, H_A#20 V36, H_A#21 AA40, H_A#22 AC43, H_A#23 V38, H_A#24 AA42, H_A#25 AA38, H_A#26 AC42, H_A#27 AD36, H_A#28 AD38, H_A#29 AA36, H_A#30 AD42, H_A#31 AD40, H_A#32 AD44, H_A#33 AD43, H_ADSTB#1 AA44 — 5 H_ADSTB#1; TPAD28 TP20, TPAD28 TP21

CONTROL: H_ADS# R46, H_BNR# M47, H_BPRI# H44, H_DEFER# K46, H_DRDY# P45, H_DBSY# M46, H_LOCK# M45, H_RESET# K25, H_RS#2 L45, H_RS#1 R47, H_RS#0 L47, H_BR0# T45, H_TRDY# R45, H_HIT# K47, H_HITM# P46, H_DPWR# T47 — 5,51 H_ADS#; 5 H_BNR#; 5 H_BPRI#; 5 H_DEFER#; 5 H_DRDY#; 5 H_DBSY#; 5 H_LOCK#; 3,5,51 H_RESET#; 5 H_BR0#; 5 H_TRDY#; 5 H_HIT#; 5 H_HITM#; 5 H_DPWR#

MISC: SUS_STAT# AT9, SYSRESET# D10, POWERGOOD F10, CPU_COMP_P B32, CPU_COMP_N A31, THERMALDIODE_P AT5, THERMALDIODE_N AT4, IOPLLVDD18 AA35, IOPLLVDD12 V35, IOPLLVSS W35, CPU_SLP# C17, CPU_VREF A32, TESTMODE A20

P-4 AGTL+I/F

DATA GROUP 0: CPU_D0 H46, CPU_D1 G47, CPU_D2 K45, CPU_D3 G45, CPU_D4 H45, CPU_D5 G46, CPU_D6 F45, CPU_D7 F47, CPU_D8 C46, CPU_D9 A44, CPU_D10 D46, CPU_D11 C45, CPU_D12 D47, CPU_D13 B44, CPU_D14 A43, CPU_D15 B45, CPU_DBI0 E47, CPU_DSTB0N E46, CPU_DSTB0P E45 — H_D#0..H_D#15, H_DINV#0, H_DSTBN#0, H_DSTBP#0

DATA GROUP 1: CPU_D16 E40, CPU_D17 F44, CPU_D18 E42, CPU_D19 F40, CPU_D20 H40, CPU_D21 D44, CPU_D22 D42, CPU_D23 D40, CPU_D24 E38, CPU_D25 F36, CPU_D26 E36, CPU_D27 J34, CPU_D28 F34, CPU_D29 H38, CPU_D30 D32, CPU_D31 E34, CPU_DBI1 K36, CPU_DSTB1N J38, CPU_DSTB1P J36 — H_D#16..H_D#31, H_DINV#1, H_DSTBN#1, H_DSTBP#1

DATA GROUP 2: CPU_D32 J32, CPU_D33 F32, CPU_D34 K32, CPU_D35 D29, CPU_D36 M29, CPU_D37 K30, CPU_D38 F30, CPU_D39 E30, CPU_D40 M27, CPU_D41 F27, CPU_D42 K27, CPU_D43 D25, CPU_D44 E27, CPU_D45 J27, CPU_D46 J25, CPU_D47 F25, CPU_DBI2 J30, CPU_DSTB2N H29, CPU_DSTB2P F29 — H_D#32..H_D#47, H_DINV#2, H_DSTBN#2, H_DSTBP#2

DATA GROUP 3: CPU_D48 C37, CPU_D49 B40, CPU_D50 B43, CPU_D51 C42, CPU_D52 C43, CPU_D53 A42, CPU_D54 B38, CPU_D55 A41, CPU_D56 C40, CPU_D57 A38, CPU_D58 C36, CPU_D59 B36, CPU_D60 A37, CPU_D61 C38, CPU_D62 B34, CPU_D63 C34, CPU_DBI3 A36, CPU_DSTB3N B41, CPU_DSTB3P C41 — H_D#48..H_D#63, H_DINV#3, H_DSTBN#3, H_DSTBP#3

RS600ME-GP

+1.8V_SUS — R170 4K7R2J-2-GP (DY)

+1.8V_RUN — Q18 2N7002-7-FP-GP — R96 1KR2J-1-GP — R99 0R2J-2-GP (DY) — 35,48,51 NB_PWRGD

20 PM_SUS_STAT# — 18,27,31,32,35,45,46,51 PLTRST# — R405 0R2-0. — PM_SUS_STAT# / PLTRST#_NB / NB_POWERGOOD

+1.05V_VCCP — R81 53D6R3F-2-GP — NB_CPU_COMP_P; R65 21R3F-GP — NB_CPU_COMP_N

23 NB_THERMDP — NB_THERMDP; 23 NB_THERMDN — NB_THERMDN

+1.8V_RUN_NB_IOPLLVDD18; +1.2V_RUN_NB_IOPLLVDD12; NB_H_CPUSLP#; +1.05V_VCCP_NB_CPU_VREF; NB_TEST_MODE

+3.3V_RUN_NB — R82 20KR2J-L2-GP

+1.05V_VCCP — R108 4K7R2J-2-GP — NB_H_CPUSLP#_1 — Q11 MMBT3904-7-F-GP

5,18 H_CPUSLP# — Q10 MMBT3904-7-F-GP

+1.05V_VCCP — R93 2K2R2J-2-GP — NB_H_CPUSLP#_2

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

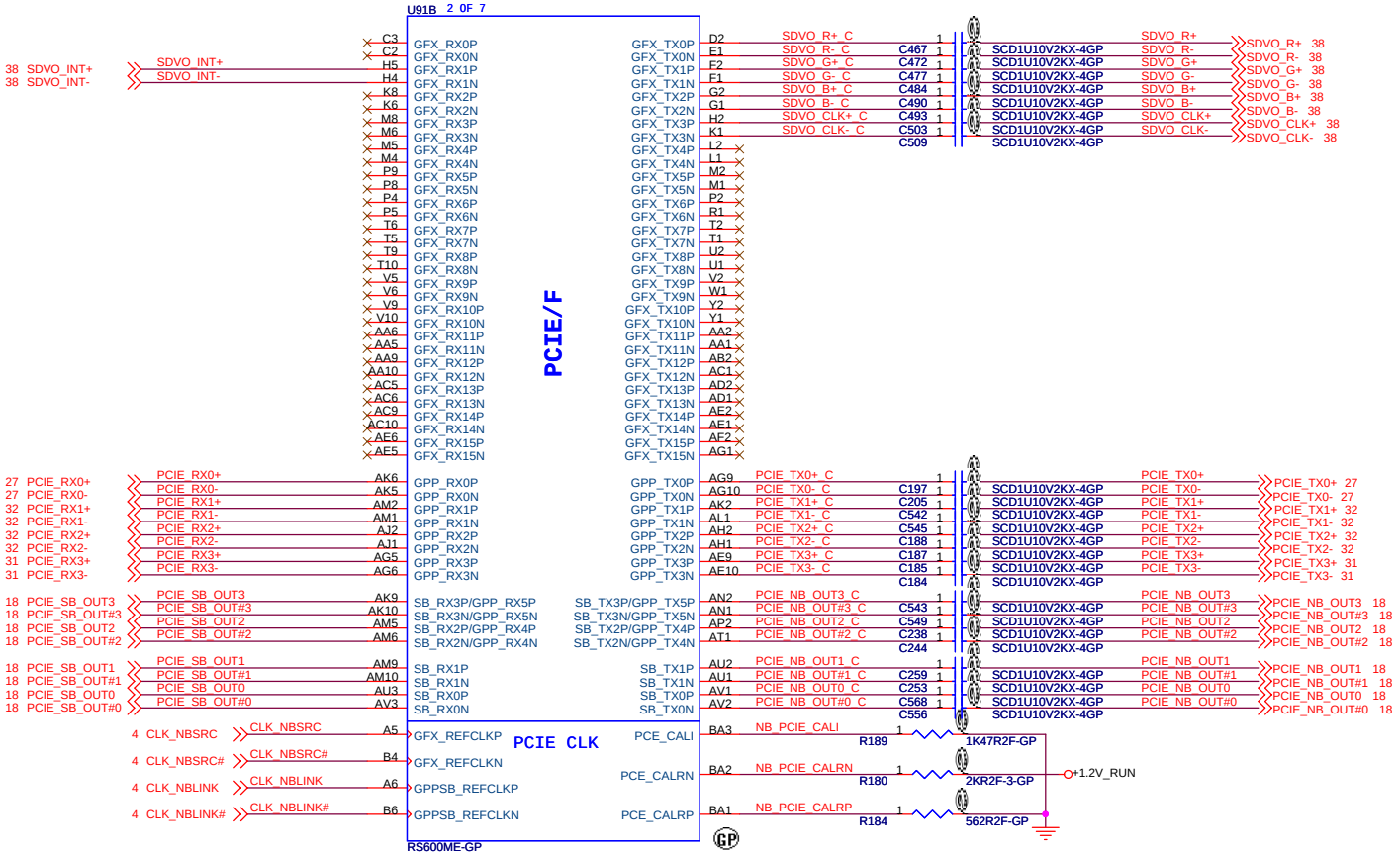
Title: RS600ME-AGTL(1/5)

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 7 of 53

SSID = N.B

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD



<Variant Name>

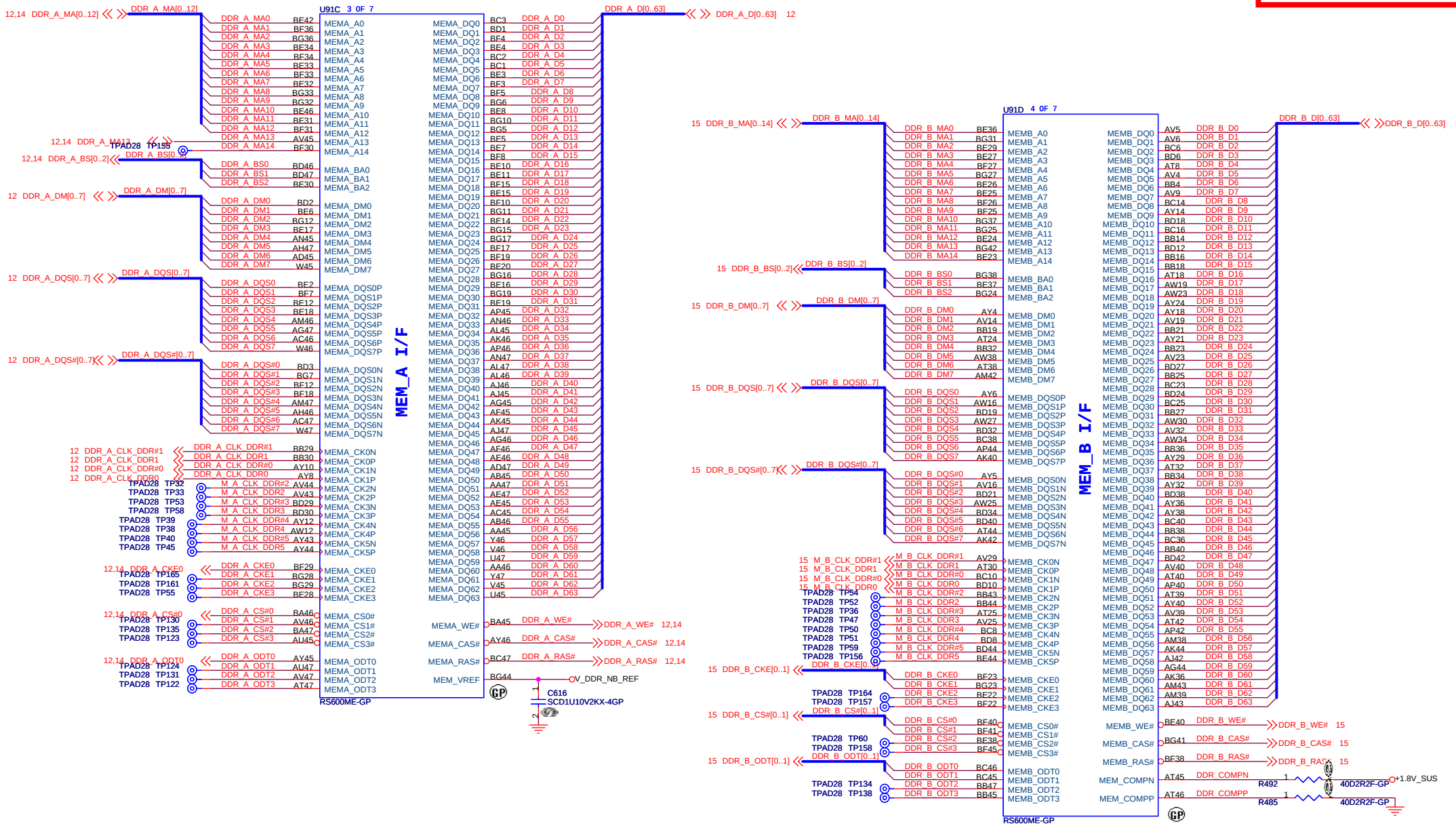
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS600ME-ALINK/PCIE-2(2/5)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 8 of 53

SSID = N.B



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS600ME-MEMORY I/F (3/5)

Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 Sheet 9 of 53

SSID = N.B

NB 3.3V are independent

PUT AT LEAST TWO VIAS
CLOSE TO VDDR3 TWO BALLS
FOR POWER DELIVERY

placed CAP closed
NB within 20 mm
(80mil)

use 24 bit or 18bit

FROM DVI CONN.
hot-plug detect.
need used it or detect
by KBC

Place close to NB

Use to control NB core power 1~1.2V

ONLY FOR NB 3.3V POWER

DAC_VSYNC: STRAP_MOBILE_GFX
DEFAULT: 1
0: DESKTOP GRAPHICS DEVICE
1: MOBILE GRAPHICS DEVICE

DAC_HSYNC: STRP_INTGFX_DISABLE
DEFAULT: 0
0: ENABLE
1: DISABLE

STRP_DATA: STRP_MEMSTRAPS
DEFAULT: 1
0: SELECT MEMORY CHA A AS DEBUG BUS
1: NORMAL MODE

DDC_DATA: STRAP_MEMVMODE
DEFAULT: 1
0: DDR3
1: DDR2

<Variant Name>

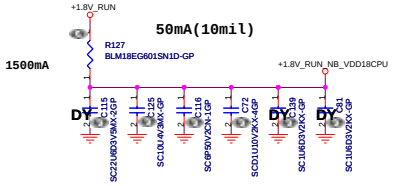
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RS600ME-4(4/5)

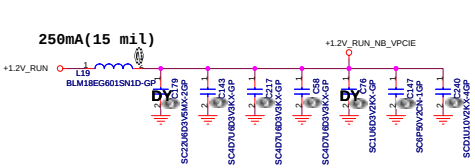
Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 10 of 53

NB-VDD18_CPU DE-COUPLING

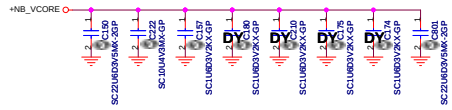


NB-VDD_PCIE DE-COUPLING

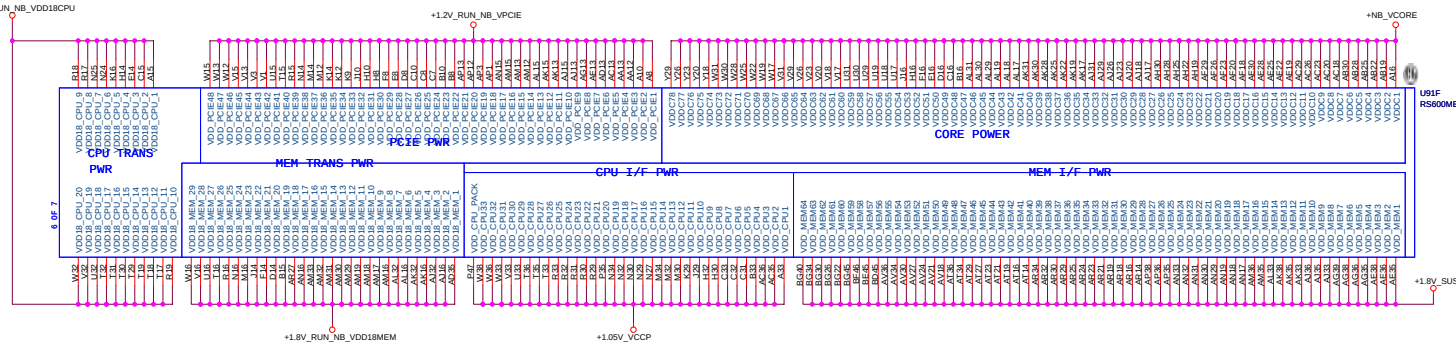


NB-VDDC DE-COUPLING

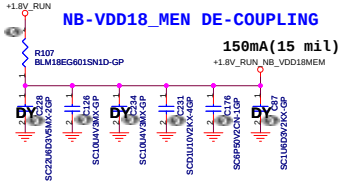
POWER 1V~1.2V 6A(240 mil)



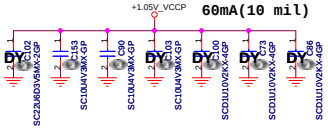
SSID = N.B



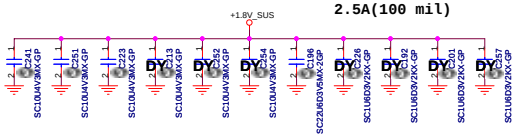
NB-VDD18_MEN DE-COUPLING



NB-VDD_CPU DE-COUPLING

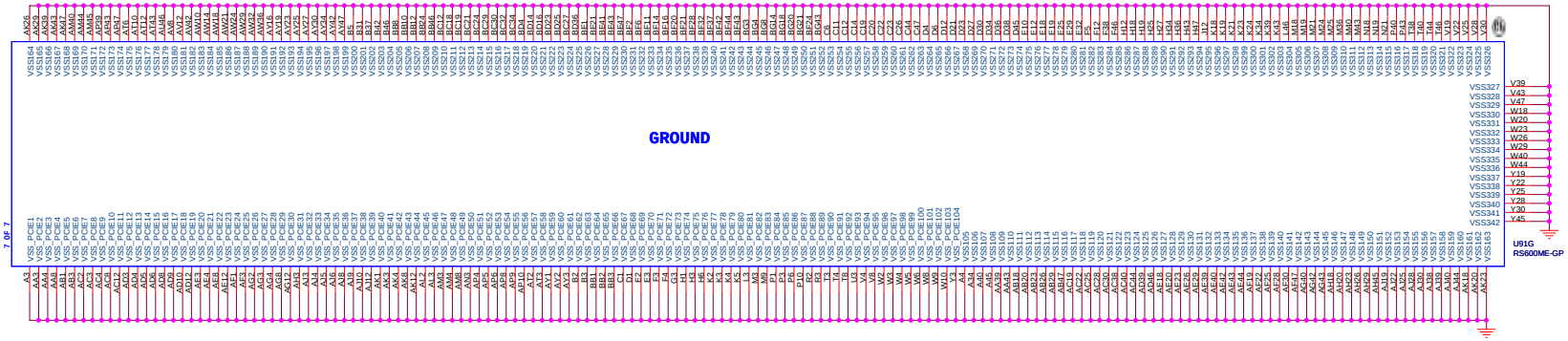


NB-VDD_MEN DE-COUPLING



THE CAPS HAVE TO BE PLACED UNDER NB. ALL CAPS' GND USE COPPER FLOOD TOGETHER, AND POWER ALSO LIKE THIS WAY.

GROUND



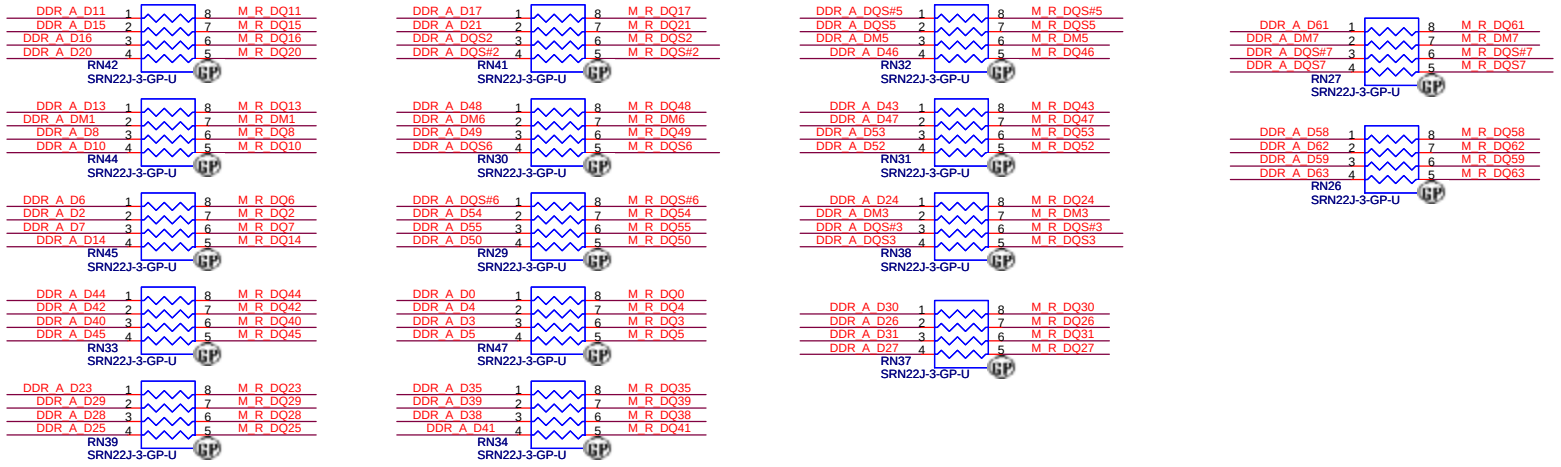
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

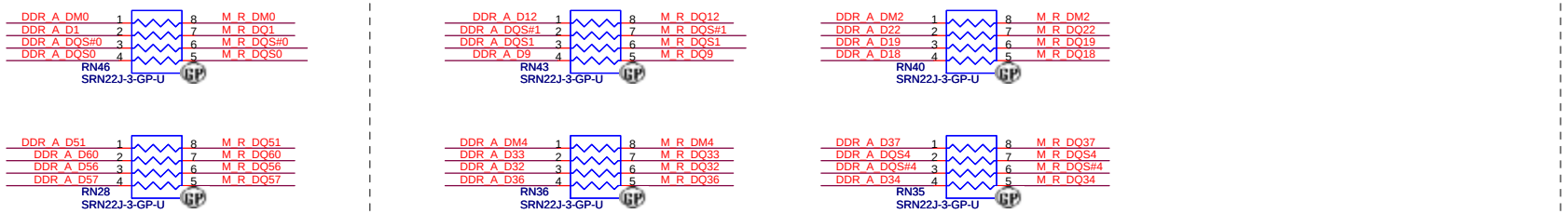
Title: RS600ME-5(5/5)

Size: A2 | Document Number: Parker | Rev: -1

Date: Thursday, August 09, 2007 | Sheet 11 of 53



series resistor 22 ohm CHANNEL A DATA



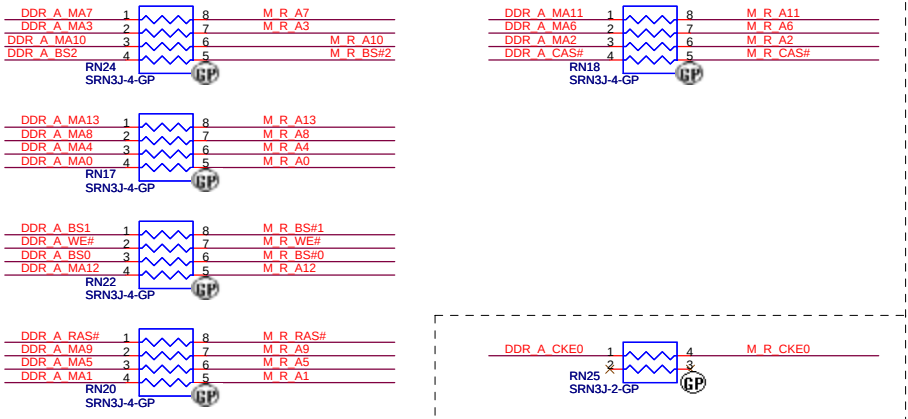
CHANNEL A DATA-MASK
series resistor 22 ohm

series resistor 22 ohm CHANNEL A DATA-STROBE

CHANNEL A ADDRESS

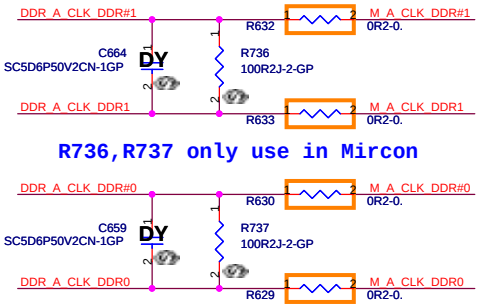
CHANNEL A COMMAND
RAM CELL ADDRESS 13

CHANNEL A BANK SELECT



series resistor 3 ohm

series resistor 3 ohm



FROM NB

DDR_A_D[0..63] DDR_A_D[0..63] 9
DDR_A_DM[0..7] DDR_A_DM[0..7] 9
DDR_A_DQS[0..7] DDR_A_DQS[0..7] 9
DDR_A_DQS#[0..7] DDR_A_DQS#[0..7] 9
DDR_A_MA[0..12] DDR_A_MA[0..12] 9,14
DDR_A_BS[0..2] DDR_A_BS[0..2] 9,14

DDR_A_CS#0 DDR_A_CS#0 9,14
DDR_A_RAS# DDR_A_RAS# 9,14
DDR_A_CAS# DDR_A_CAS# 9,14
DDR_A_WE# DDR_A_WE# 9,14
DDR_A_CKE0 DDR_A_CKE0 9,14
DDR_A_ODT0 DDR_A_ODT0 9,14
DDR_A_MA13 DDR_A_MA13 9,14

DDR_A_CLK_DDR#1 DDR_A_CLK_DDR#1 9
DDR_A_CLK_DDR1 DDR_A_CLK_DDR1 9
DDR_A_CLK_DDR#0 DDR_A_CLK_DDR#0 9
DDR_A_CLK_DDR0 DDR_A_CLK_DDR0 9

TO DIMM

M_R_DQ[63..0] M_R_DQ[63..0] 13
M_R_DM[7..0] M_R_DM[7..0] 13
M_R_DQS[7..0] M_R_DQS[7..0] 13
M_R_DQS#[7..0] M_R_DQS#[7..0] 13
M_R_A[12..0] M_R_A[12..0] 13
M_R_BS#[2..0] M_R_BS#[2..0] 13

M_R_CS#0 M_R_CS#0 13
M_R_CAS# M_R_CAS# 13
M_R_RAS# M_R_RAS# 13
M_R_ODT0 M_R_ODT0 13
M_R_CKE0 M_R_CKE0 13
M_R_WE# M_R_WE# 13
M_R_A13 M_R_A13 13

M_A_CLK_DDR#1 M_A_CLK_DDR#1 13
M_A_CLK_DDR1 M_A_CLK_DDR1 13
M_A_CLK_DDR#0 M_A_CLK_DDR#0 13
M_A_CLK_DDR0 M_A_CLK_DDR0 13

SSID = MEMORY

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

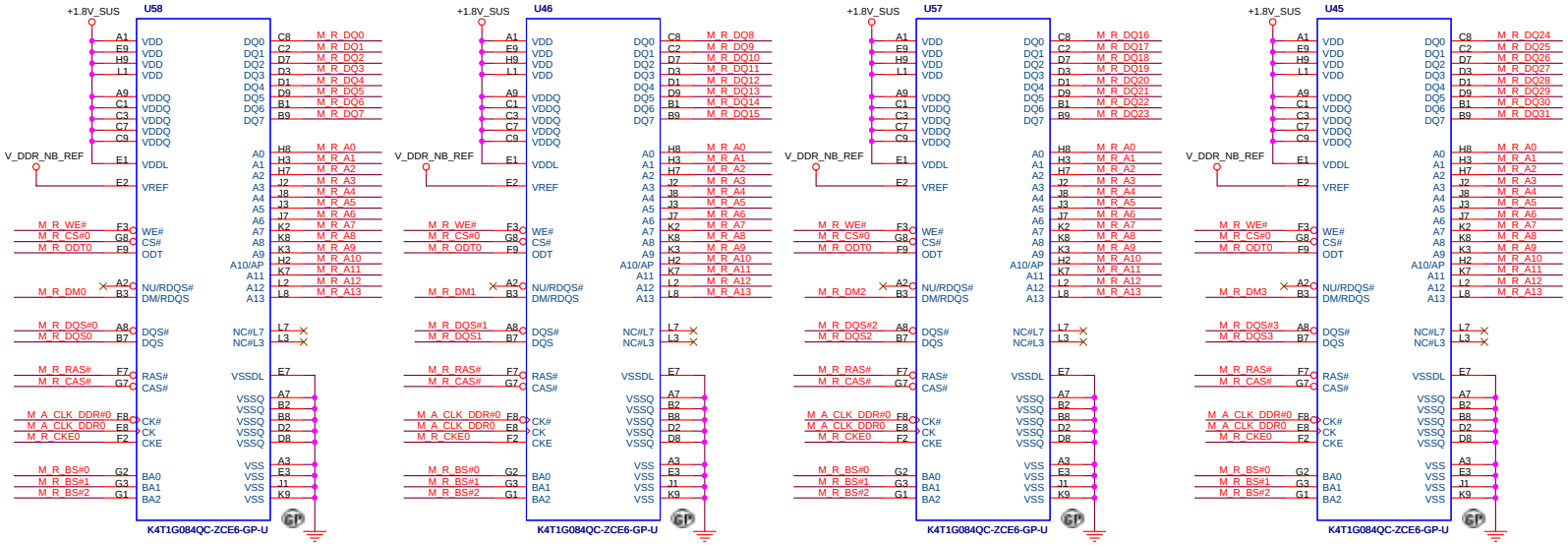
Title: CHANNEL A RESISTORS

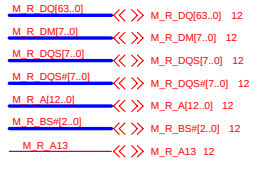
Size	Document Number	Rev
A3	Parker	-1

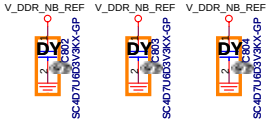
Date: Friday, August 03, 2007 Sheet 12 of 53

On-board DDR2 Memory

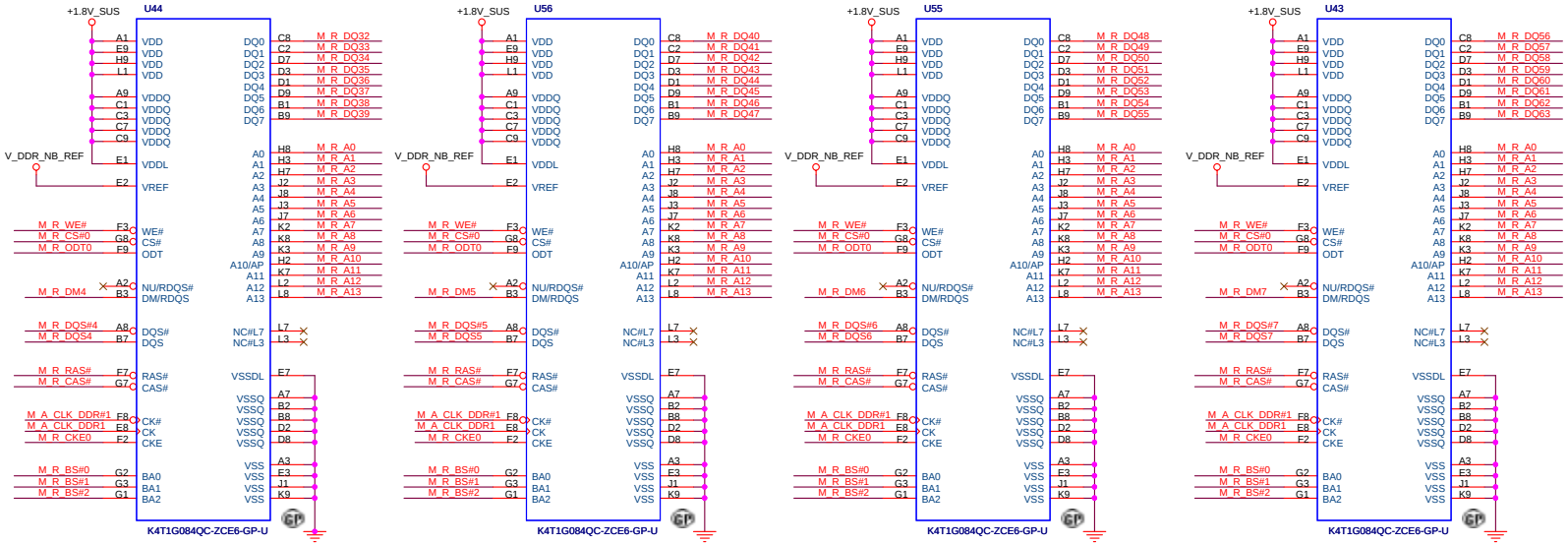
samsung

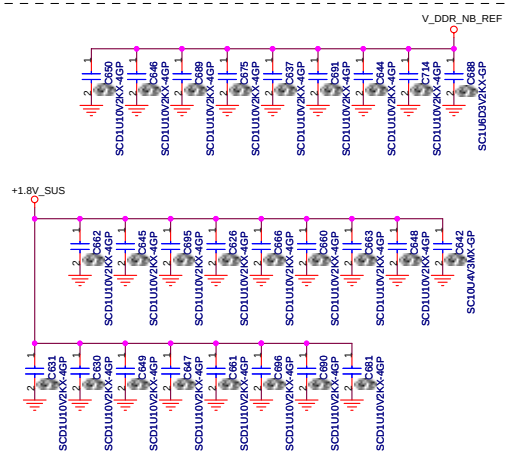






SSID = MEMORY





Place around the DDR2 chips

<Variant Name>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ON BOARD MEMORY**

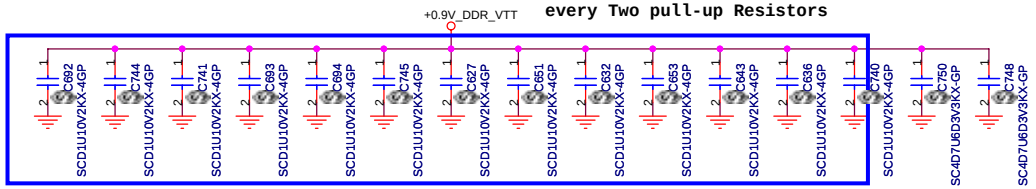
Size	Document Number	Rev
Custom	Parker	-1

Date: Friday, August 03, 2007 Sheet 13 of 53

SSID = MEMORY

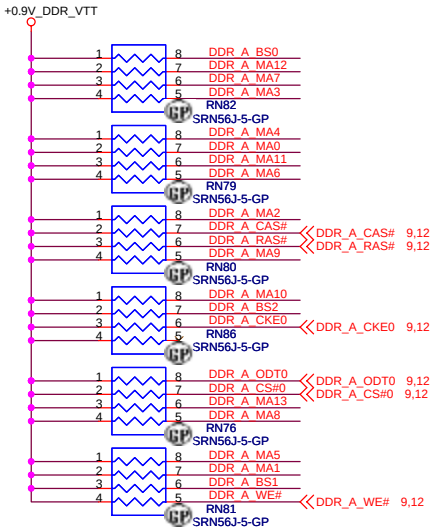
DIMMA-DDR +0.9V_DDR_VTT DE-COUPLING

Please use One Capacitor close to every Two pull-up Resistors



DDR_A_BS[0..2] DDR_A_BS[0..2] 9,12
DDR_A_MA[0..12] DDR_A_MA[0..12] 9,12
DDR_A_MA13 DDR_A_MA13 9,12

ON-BOARD MEMORY TERMINATION



<Variant Name>

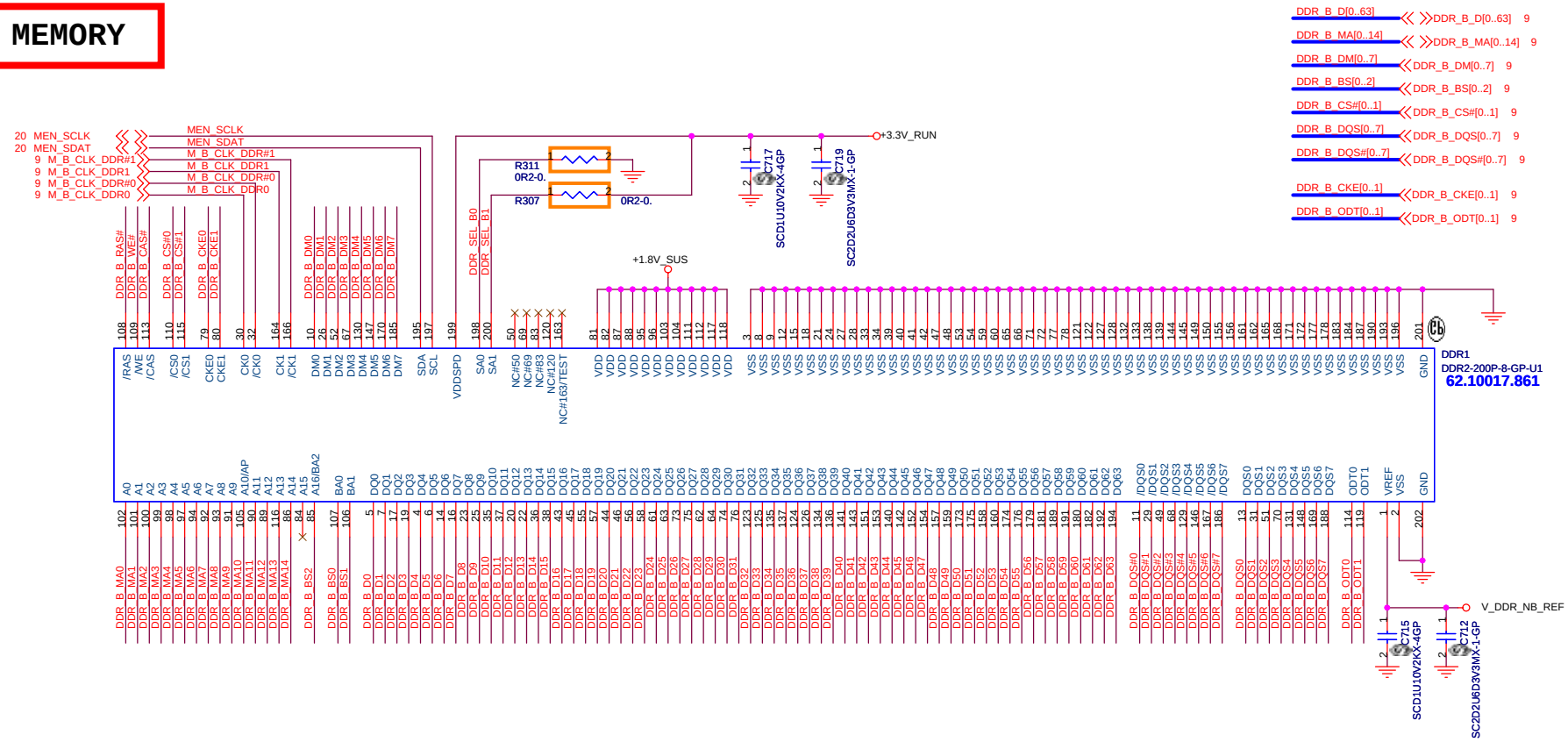
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ON-BOARD MEMORY TERMINATION

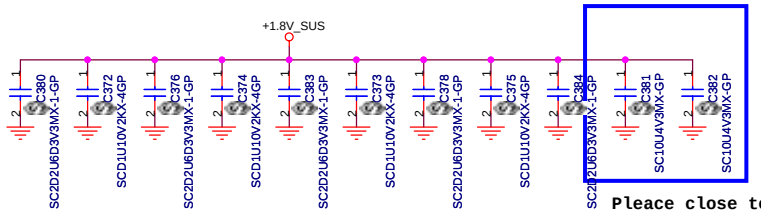
Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 14 of 53

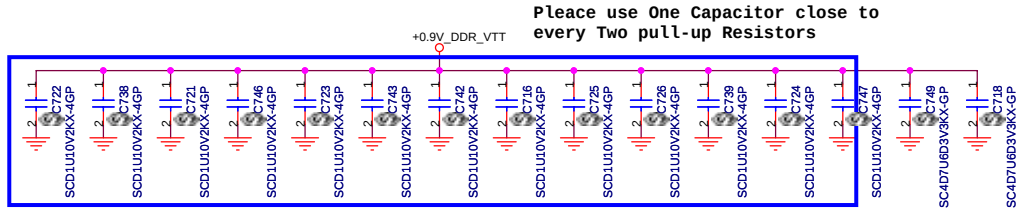
SSID = MEMORY

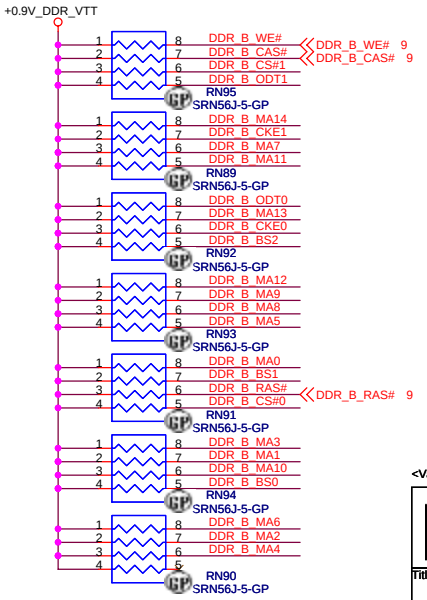


DIMMB-DDR +1.8V_SUS DE-COUPLING



DIMMB-DDR +0.9V_DDR_VTT DE-COUPLING





<Variant Name>

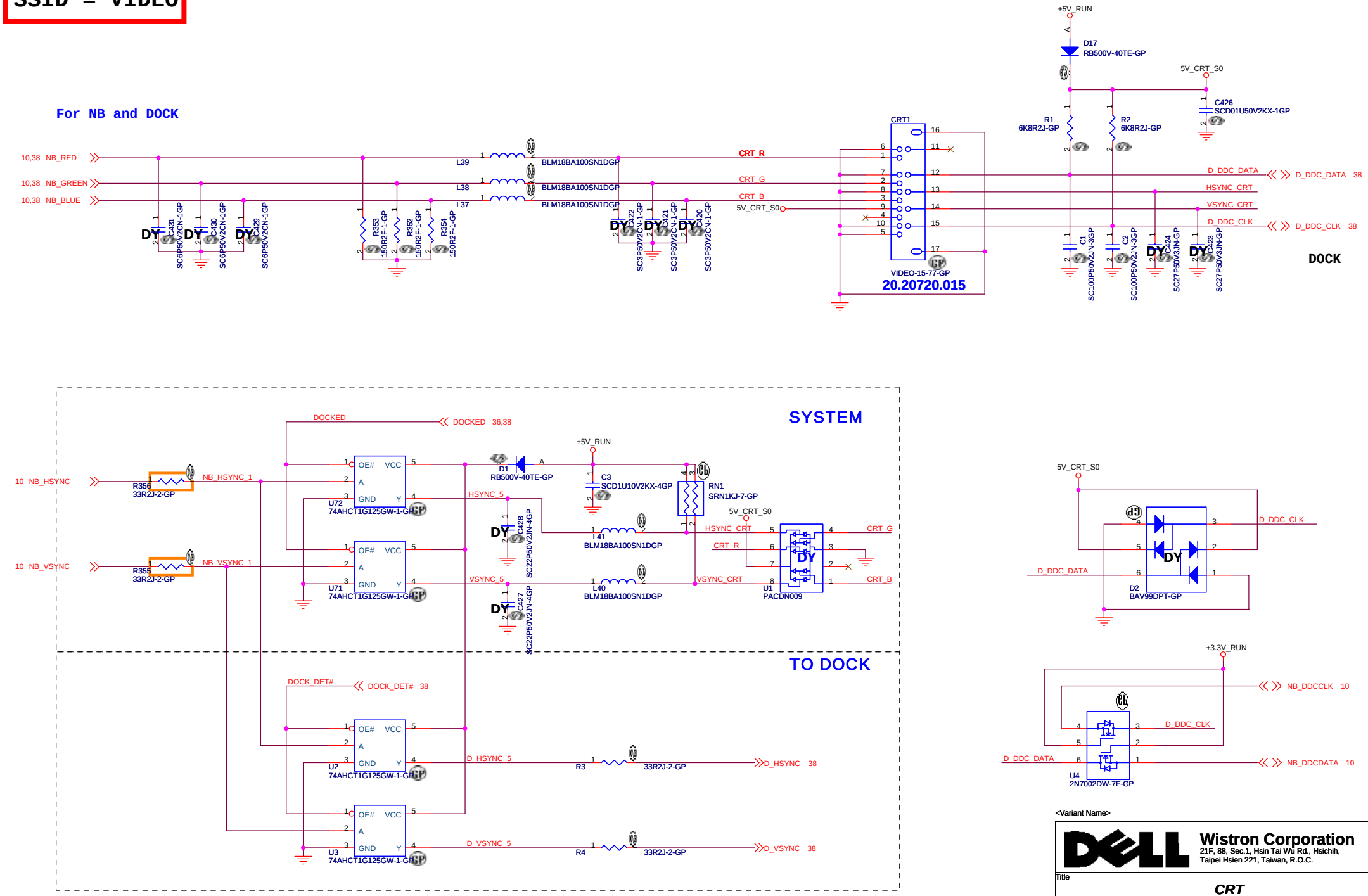
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR-B***

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 15 of 53

SSID = VIDEO

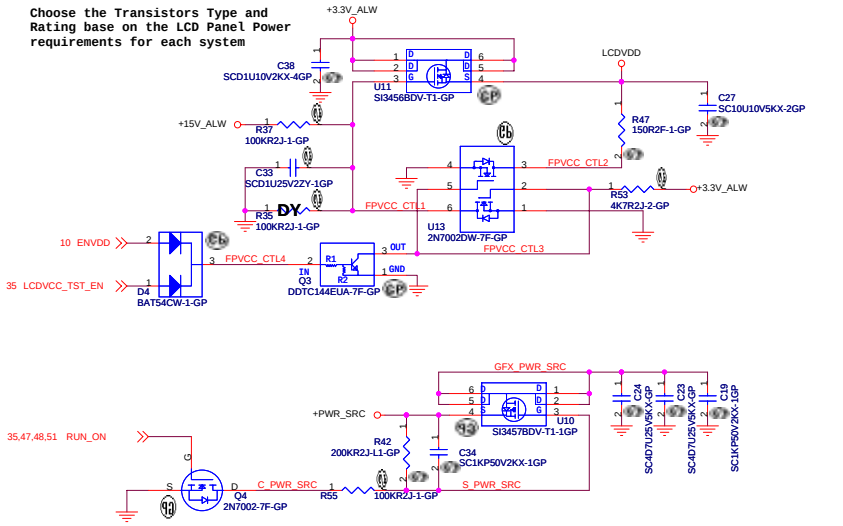


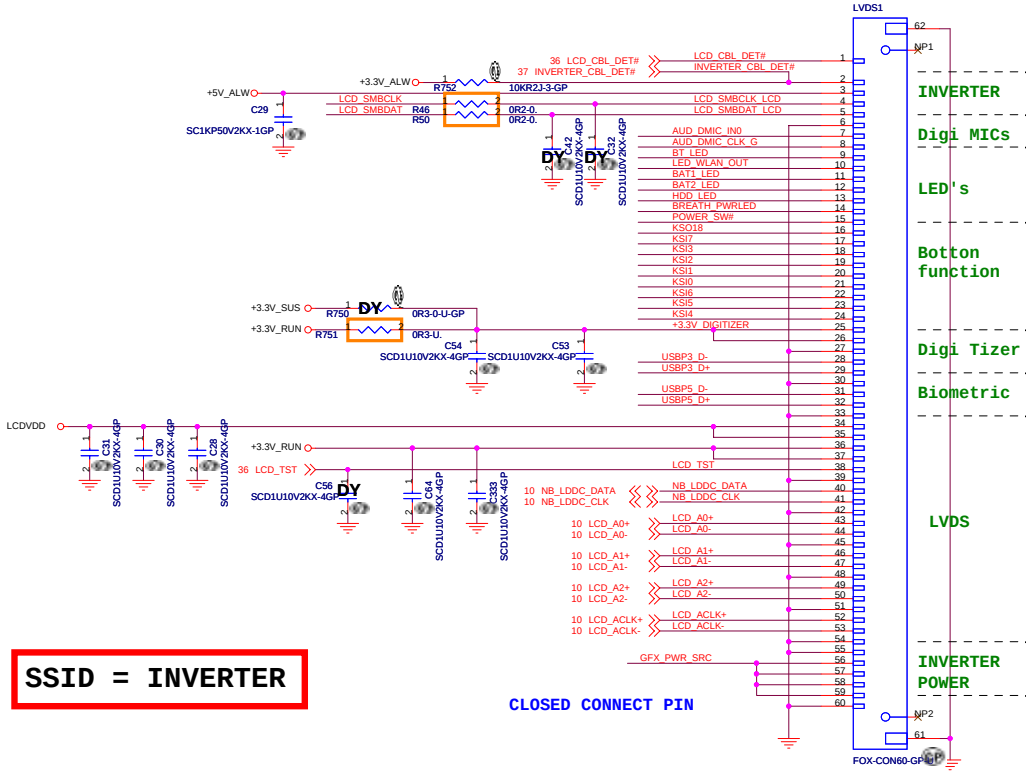
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 16 of 53	

Choose the Transistors Type and Rating base on the LCD Panel Power requirements for each system





Digi MICs 750uA **3 PIN**

+3.3V_RUN PLANE

29 AUD_DMIC_CLK_G — AUD_DMIC_CLK_G
29 AUD_DMIC_IN0 — AUD_DMIC_IN0

Light Sensor **2 PIN**

+3.3V_RUN PLANE

35 LCD_SMBCLK — LCD_SMBCLK
35 LCD_SMBDAT — LCD_SMBDAT

maybe use the same SMBUS

Digi Tizer **2 PIN**

+3.3V_RUN PLANE

20 SB600_USBP3- — R75 0R2-0. — USBP3_D-

20 SB600_USBP3+ — R74 0R2-0. — USBP3_D+

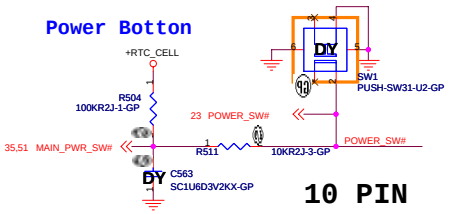
Biometric **2 PIN**

+3.3V_RUN PLANE

20 SB600_USBP5- — R73 0R2-0. — USBP5_D-

20 SB600_USBP5+ — R72 0R2-0. — USBP5_D+

Power Botton



10 PIN

Ctrl+Del+Alt Botton

37 KSI0 — KSI0

Mobility Center Botton

37 KSI1 — KSI1

User-Programmable Botton

37 KSI2 — KSI2

Screen Rotation Botton

37 KSI3 — KSI3

37 KSO18 — KSO18

Toggle Switch

37 KSI4 — KSI4 — R

37 KSI5 — KSI5 — L

37 KSI6 — KSI6

Forward Botton

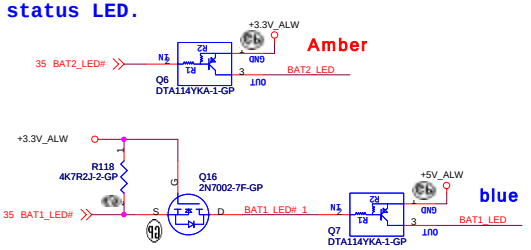
37 KSI7 — KSI7

SSID = INVERTER

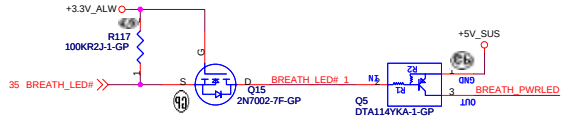
CLOSED CONNECT PIN

20.F1015.060

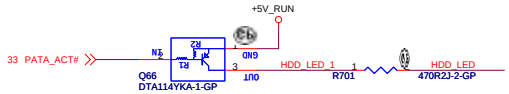
Battery status LED.



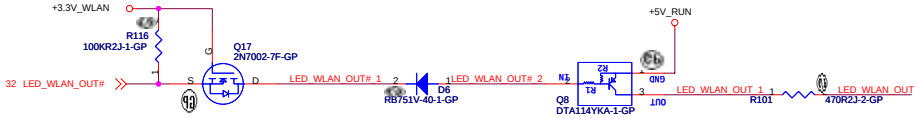
Power & Suspend LED.



HDD activity LED.

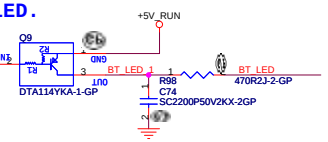


WLAN LED.



6 PIN

Bluetooth LED.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 17 of 53

SSID = S.B

Place R160,R155,R156 Close to pin E29,E28,E27<100 mil

U35A 1 of 4

SB600-GP

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

LPC

XTAL

CPU

RTC

PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	G H	1	1

SSID =RBATT

SB_RTC

SB_Xtal

Place Close to pin D2,C1

AND Gate

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-CPU&LPC&PCI&PCIE(1/5)

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 18 of 53

<Variant Name> 20.F0693.003

SSID = S.B

If SATA I/F no used SATA_X1 directly to GND
AVDD_SATA directly to GND
PLLVDD_SATA directly to GND
XTLVDD_SATA directly to GND

U35B 2 of 4

SERIAL ATA

SATA_TX0+ AH21
SATA_TX0- AJ21
SATA_RX0- AH20
SATA_RX0+ AJ20
SATA_TX1+ AH18
SATA_TX1- AJ18
SATA_RX1- AH17
SATA_RX1+ AJ17
SATA_TX2+ AH13
SATA_TX2- AH14
SATA_RX2- AH16
SATA_RX2+ AJ16
SATA_TX3+ AJ11
SATA_TX3- AH11
SATA_RX3- AH12
SATA_RX3+ AJ13
SATA_CAL AF12
SATA_X1 AD16
SATA_X2 AD18
SATA_ACT#/GPIO67 AC12

R602 DY 1KR2F-3-GP
SATA_CAL
SATA_XTAL1
SATA_XTAL2

SERIAL ATA POWER

PLLVDD_SATA AD14
PLLVDD_SATA AJ10
XTLVDD_SATA AC16
AVDD_SATA AE14
AVDD_SATA AE16
AVDD_SATA AE18
AVDD_SATA AE19
AVDD_SATA AF19
AVDD_SATA AF21
AVDD_SATA AG22
AVDD_SATA AG23
AVDD_SATA AH22
AVDD_SATA AH23
AVDD_SATA AJ12
AVDD_SATA AJ14
AVDD_SATA AJ19
AVDD_SATA AJ22
AVDD_SATA AJ23
AVSS_SATA AB14
AVSS_SATA AB16
AVSS_SATA AB18
AVSS_SATA AC14
AVSS_SATA AC18
AVSS_SATA AC19
AVSS_SATA AD12
AVSS_SATA AD19
AVSS_SATA AD21
AVSS_SATA AE12
AVSS_SATA AE21
AVSS_SATA AF11
AVSS_SATA AF14
AVSS_SATA AF16
AVSS_SATA AF18
AVSS_SATA AG11
AVSS_SATA AG12
AVSS_SATA AG13
AVSS_SATA AG14
AVSS_SATA AG16
AVSS_SATA AG17
AVSS_SATA AG18
AVSS_SATA AG19
AVSS_SATA AG20
AVSS_SATA AG21
AVSS_SATA AH10
AVSS_SATA AH19

SB600-GP

ATA 66/100

IDE_IORDY AB29 — IDE_IORDY 33
IDE_IRQ AA28 — INT_IRQ14 33
IDE_A0 AA29 — IDE_A0 33
IDE_A1 AB27 — IDE_A1 33
IDE_A2 Y28 — IDE_A2 33
IDE_DACK# AB28 — IDE_DACK# 33
IDE_DRQ AC27 — IDE_DREQ 33
IDE_IOR# AC29 — IDE_IOR# 33
IDE_IOW# AC28 — IDE_IOW# 33
IDE_CS1# W28 — IDE_CS1# 33
IDE_CS3# W27 — IDE_CS3# 33
IDE_D[0..15] 33

IDE_D0/GPIO15 AD28 — IDE_D0
IDE_D1/GPIO16 AD26 — IDE_D1
IDE_D2/GPIO17 AE29 — IDE_D2
IDE_D3/GPIO18 AF27 — IDE_D3
IDE_D4/GPIO19 AG29 — IDE_D4
IDE_D5/GPIO20 AH28 — IDE_D5
IDE_D6/GPIO21 AJ28 — IDE_D6
IDE_D7/GPIO22 AJ27 — IDE_D7
IDE_D8/GPIO23 AH27 — IDE_D8
IDE_D9/GPIO24 AG27 — IDE_D9
IDE_D10/GPIO25 AG28 — IDE_D10
IDE_D11/GPIO26 AF28 — IDE_D11
IDE_D12/GPIO27 AF29 — IDE_D12
IDE_D13/GPIO28 AF28 — IDE_D13
IDE_D14/GPIO29 AD25 — IDE_D14
IDE_D15/GPIO30 AD29 — IDE_D15

SB_EC_SPI_DIN_R — C776 DY SC22P50V2JN-4GP

SPI ROM

SPI_DI/GPIO12 J3 — SB_EC_SPI_DIN_R — R518 0R2-0. — SB_EC_SPI_DIN 35
SPI_DO/GPIO11 J6 — SB_EC_SPI_DO_R — R529 47R2J-2-GP — SB_EC_SPI_DO 35
SPI_CLK/GPIO47 G3 — SB_EC_SPI_CLK_R — R514 47R2J-2-GP — SB_EC_SPI_CLK 35
SPI_HOLD#/GPIO31 G2 — SB_SPI_HOLD# R — R509 0R2J-2-GP — SB_SPI_HOLD# 33
SPI_CS#/GPIO32 G6 — SB_SPI_CS#

LAN_RST#/GPIO13 C23 — SB_LAN_RST# — TP126 TPAD28
ROM_RST#/GPIO14 G5 — SB_ROM_RST# — TP132 TPAD28

FANOUT0/GPIO3 M4
FANOUT1/GPIO48 T3 — PCIE_WLAN_DET# — PCIE_WLAN_DET# 32
FANOUT2/GPIO49 V4 — USB_WLAN_DET# — USB_WLAN_DET# 32

WLAN

FANIN0/GPIO50 N3 — PCIE_WWAN_DET# — PCIE_WWAN_DET# 32
FANIN1/GPIO51 P2 — USB_WWAN_DET# — USB_WWAN_DET# 32
FANIN2/GPIO52 W4

WWAN

HW MONITOR

TEMP_COMM P5 — SB_TEMP_COMM — TP151 TPAD28
TEMPIN0/GPIO61 P7
TEMPIN1/GPIO62 P8 — AUD_SPK_DET# — AUD_SPK_DET# 30
TEMPIN2/GPIO63 T8 — RTC_BAT_DET# 18
TEMPIN3/TALERT#/GPIO64 T7 — MINI3_CLK_REQ# — R543 10KR2J-3-GP — +3.3V_RUN

VIN0/GPIO53 V5 — SB_WWAN_PCIE_RST# 32
VIN1/GPIO54 L7 — SB_WLAN_PCIE_RST# 32
VIN2/GPIO55 M8 — SB_LOM_PCIE_RST# 27
VIN3/GPIO56 V6 — NC_GPIO56
VIN4/GPIO57 M6 — MEM_VEND_ID1 — MEM_VEND_ID1 36
VIN5/GPIO58 P4 — LBF_ID1 — TP148 TPAD28
VIN6/GPIO59 M7 — LBF_ID2 — TP145 TPAD28
VIN7/GPIO60 V7 — ALT_TP_DET# — R563 10KR2J-3-GP — +3.3V_RUN

R585 20KR2J-L2-GP
R533 20KR2J-L2-GP
R522 20KR2J-L2-GP
R589 20KR2J-L2-GP

BIOS should not enable the internal GPIO pull up resistor

+3.3V_RUN_HW
AVDD N1 — L27 200mA BLM18BB221SN1D-GP — +3.3V_RUN
AVSS M1
C276 SCD1U10V2KX-4GP
C275 SC2D2U6D3V3MX-1-GP
R186 0R3-U.
HW_AGND

Place R175 close to SB600
HWM AGND trace at least 10 mil wide

VCC_SATA_PLL
VCC_RUN_SB — L35 200mA BLM18BB221SN1D-GP — VCC_SATA_PLL
C628 SC1U6D3V2KX-GP
R738 0R2-0.

VCC_SATA_XTL
+3.3V_RUN — L34 200mA BLM18BB221SN1D-GP — VCC_SATA_XTL
R739 0R2-0.

VCC_SATA_SB
VCC_RUN_SB — L36 1500mA BLM18PG181SN-3GP — VCC_SATA_SB
C634 SC22U6D3V5MX-2GP
C638 SC1U6D3V2KX-GP
C640 SC1U6D3V2KX-GP
R740 0R2-0.

SATA_Xtal

SATA_XTAL3 — R247 0R2J-2-GP — SATA_XTAL1
R244 10MR2J-L-GP — SATA_XTAL2
X3 XTAL-25MHZ-72GP
C332 SC10P50V2JN-4GP
C323 SC10P50V2JN-4GP

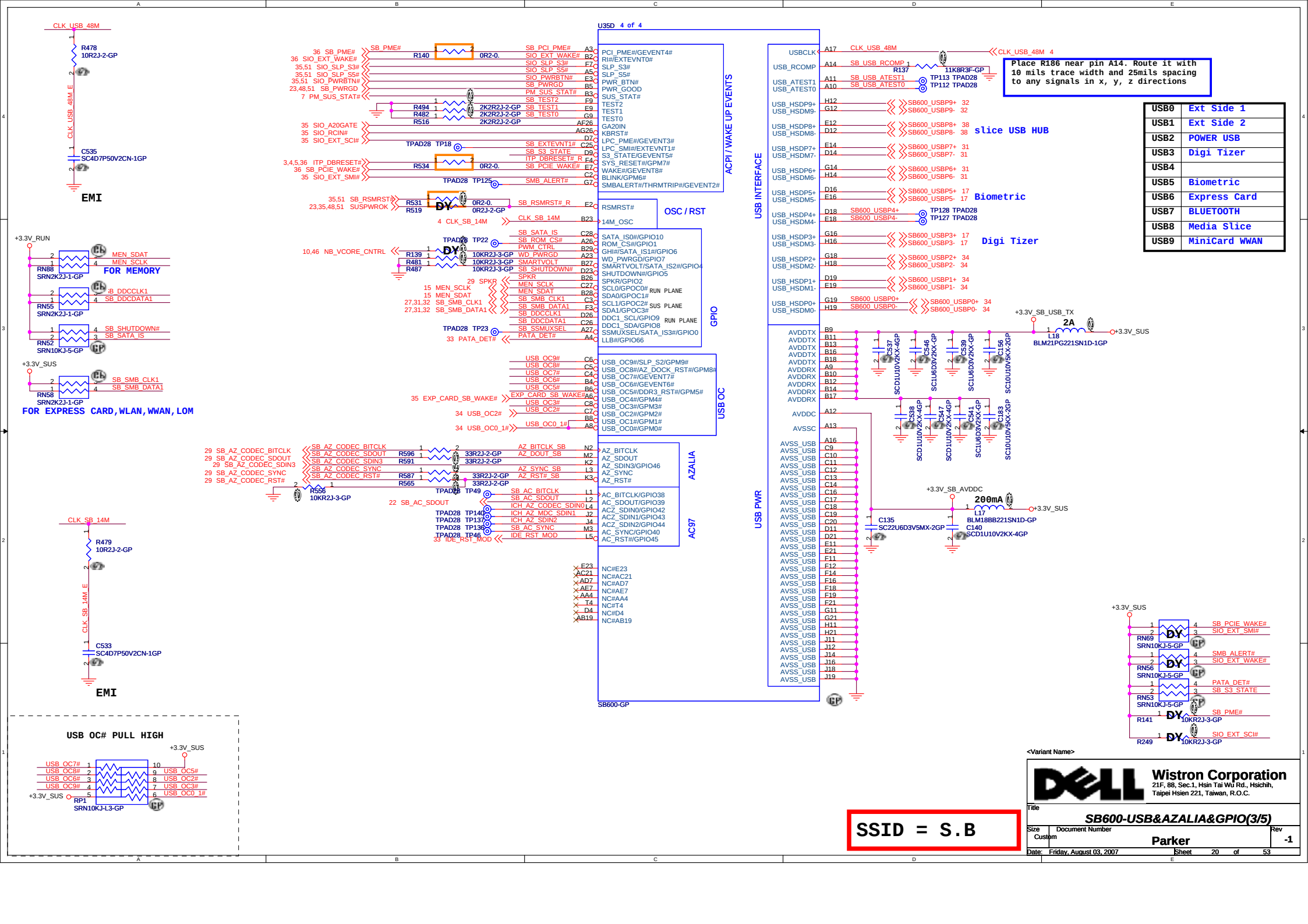
AND Gate

+3.3V_SUS
R484 1KR2J-1-GP
SB_SPI_CS#
35 SIO_SPI_CS#
R445 47R2J-2-GP
+3.3V_ALW
C499 SCD1U10V2KX-4GP
U84 74AHC1G08GW-GP-U
SPI_CS# R
R436 15R2J-GP
SPI_CS# 33

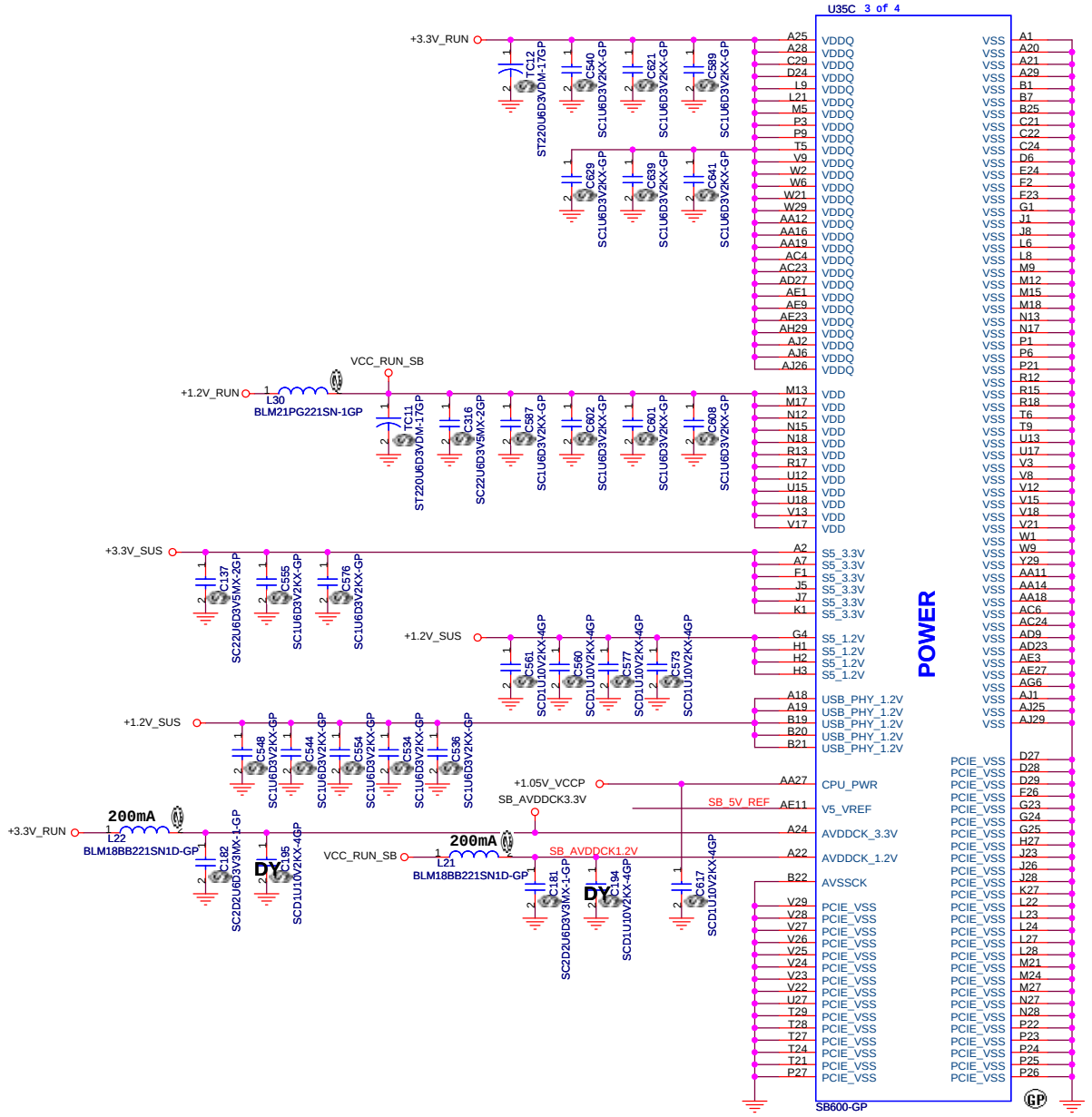
<Variant Name>

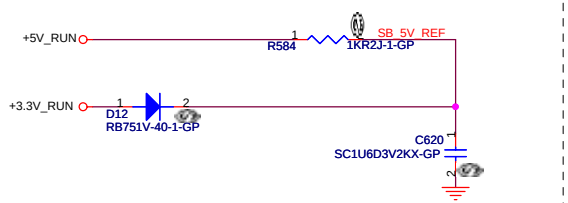
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-IDE&SATA$SPI(2/5)
Size: A3 | Document Number: Parker | Rev: -1
Date: Tuesday, August 14, 2007 | Sheet 19 of 53


CLK_USB_48M
R478
10R2J-2-GP
CLK_USB_48M_E
C535
SC4D7P50V2CN-1GP
EMI
+3.3V_RUN
MEM_SDAT
MEM_SCLK
RN88
SRN2K2J-1-GP
FOR MEMORY
SB_DDCCLK1
SB_DDCDATA1
RN55
SRN2K2J-1-GP
SB_SHUTDOWN#
SB_SATA_IS
RN52
SRN10KJ-5-GP
+3.3V_SUS
SB_SMB_CLK1
SB_SMB_DATA1
RN58
SRN2K2J-1-GP
FOR EXPRESS CARD,WLAN,WWAN,LOM
CLK_SB_14M
R479
10R2J-2-GP
CLK_SB_14M_E
C533
SC4D7P50V2CN-1GP
EMI
USB OC# PULL HIGH
+3.3V_SUS
USB_OC7#
USB_OC8#
USB_OC6#
USB_OC9#
USB_OC5#
USB_OC2#
USB_OC3#
USB_OC0_1#
RP1
SRN10KJ-L3-GP
U35D 4 of 4
SB_PME#
R140
0R2-0.
SB_PCI_PME#
SIO_EXT_WAKE#
SIO_SLP_S3#
SIO_SLP_S5#
SIO_PWRBTN#
SB_PWRGD
PM_SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0
R494
R482
R516
2K2R2J-2-GP
SIO_A20GATE
SIO_RCIN#
SIO_EXT_SCI#
TPAD28 TP18
SB_EXTEVNT1#
SB_S3_STATE
ITP_DBRESET#_R
R534
SB_PCIE_WAKE#
TPAD28 TP125
SMB_ALERT#
SB_RSMRST#
SUSPWROK
R531
R519
DY
SB_RSMRST#_R
CLK_SB_14M
TPAD28 TP22
SB_SATA_IS
SB_ROM_CS#
PWM_CTRL
NB_VCORE_CNTRL
R139
R481
R487
10KR2J-3-GP
WD_PWRGD
SMARTVOLT
SB_SHUTDOWN#
SPKR
MEN_SCLK
MEN_SDAT
SB_SMB_CLK1
SB_SMB_DATA1
SB_DDCCLK1
SB_DDCDATA1
SB_SSMUXSEL
TPAD28 TP23
PATA_DET#
USB_OC9#
USB_OC8#
USB_OC7#
USB_OC6#
USB_OC5#
EXP_CARD_SB_WAKE#
USB_OC3#
USB_OC2#
USB_OC0_1#
SB_AZ_CODEC_BITCLK
SB_AZ_CODEC_SDOUT
SB_AZ_CODEC_SDIN3
SB_AZ_CODEC_SYNC
SB_AZ_CODEC_RST#
R596
R591
R587
R565
R556
10KR2J-3-GP
33R2J-2-GP
AZ_BITCLK_SB
AZ_DOUT_SB
AZ_SYNC_SB
AZ_RST#_SB
TPAD28 TP49
SB_AC_BITCLK
SB_AC_SDOUT
ICH_AZ_CODEC_SDIN0
ICH_AZ_MDC_SDIN1
ICH_AZ_SDIN2
SB_AC_SYNC
IDE_RST_MOD
TPAD28 TP140
TPAD28 TP137
TPAD28 TP138
TPAD28 TP146
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
ACPI / WAKE UP EVENTS
RSMRST#
14M_OSC
OSC / RST
SATA_IS0#/GPIO10
ROM_CS#/GPIO1
GHI#/SATA_IS1#/GPIO6
WD_PWRGD/GPIO7
SMARTVOLT/SATA_IS2#/GPIO4
SHUTDOWN#/GPIO5
SPKR/GPIO2
SCL0/GPOC0# RUN PLANE
SDA0/GPOC1#
SCL1/GPOC2# SUS PLANE
SDA1/GPOC3#
DDC1_SCL/GPIO9 RUN PLANE
DDC1_SDA/GPIO8
SSMUXSEL/SATA_IS3#/GPIO0
LLB#/GPIO66
GPIO
USB_OC9#/SLP_S2/GPM9#
USB_OC8#/AZ_DOCK_RST#/GPM8#
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/DDR3_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZALIA
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
AC97
USB PWR
NC#E23
NC#AC21
NC#AD7
NC#AE7
NC#AA4
NC#T4
NC#D4
NC#AB19
SB600-GP
USB INTERFACE
USBCLK
CLK_USB_48M
USB_RCOMP
R137
11K8R3F-GP
USB_ATEST1
USB_ATEST0
SB_USB_RCOMP
SB_USB_ATEST1
SB_USB_ATEST0
TP113 TPAD28
TP112 TPAD28
Place R186 near pin A14. Route it with 10 mils trace width and 25mils spacing to any signals in x, y, z directions
USB_HSDP9+
USB_HSDM9-
USB_HSDP8+
USB_HSDM8-
USB_HSDP7+
USB_HSDM7-
USB_HSDP6+
USB_HSDM6-
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USB_HSDP1+
USB_HSDM1-
USB_HSDP0+
USB_HSDM0-
SB600_USBP9+
SB600_USBP9-
SB600_USBP8+
SB600_USBP8-
SB600_USBP7+
SB600_USBP7-
SB600_USBP6+
SB600_USBP6-
SB600_USBP5+
SB600_USBP5-
SB600_USBP4+
SB600_USBP4-
SB600_USBP3+
SB600_USBP3-
SB600_USBP2+
SB600_USBP2-
SB600_USBP1+
SB600_USBP1-
SB600_USBP0+
SB600_USBP0-
slice USB HUB
Biometric
Digi Tizer
USB0 Ext Side 1
USB1 Ext Side 2
USB2 POWER USB
USB3 Digi Tizer
USB4
USB5 Biometric
USB6 Express Card
USB7 BLUETOOTH
USB8 Media Slice
USB9 MiniCard WWAN
AVDDTX
AVDDRX
AVDDC
AVSSC
AVSS_USB
+3.3V_SB_USB_TX
2A
L18
BLM21PG221SN1D-1GP
+3.3V_SUS
SCD1U10V2KX-4GP
SC1U6D3V2KX-GP
SC1U6D3V2KX-4GP
SC1U6D3V2KX-2GP
SC10U10V5KX-2GP
+3.3V_SB_AVDDC
200mA
L17
BLM18BB221SN1D-GP
C135
SC22U6D3V5MX-2GP
C140
SCD1U10V2KX-4GP
+3.3V_SUS
SB_PCIE_WAKE#
SIO_EXT_SMI#
RN69
SRN10KJ-5-GP
SMB_ALERT#
SIO_EXT_WAKE#
RN56
SRN10KJ-5-GP
PATA_DET#
SB_S3_STATE
RN53
SRN10KJ-5-GP
SB_PME#
R141
10KR2J-3-GP
SIO_EXT_SCI#
R249
10KR2J-3-GP
SSID = S.B
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600-USB&AZALIA&GPIO(3/5)
Size Custom
Document Number
Parker
Rev -1
Date: Friday, August 03, 2007
Sheet 20 of 53

SSID = S.B





<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-Power(4/5)

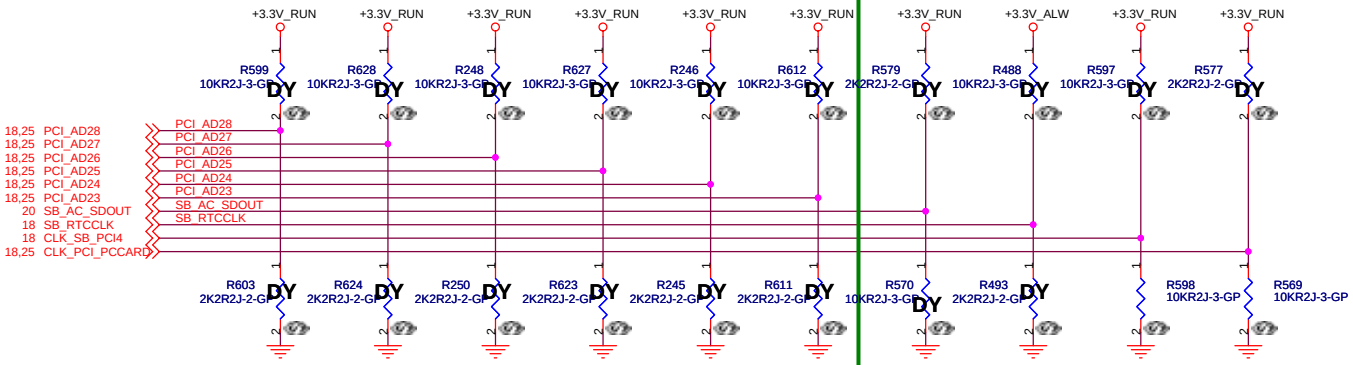
Size	Document Number	Rev
A3	Parker	-1

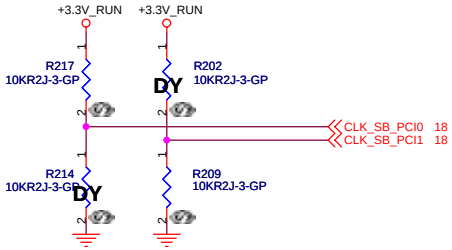
Date: Friday, August 03, 2007 Sheet 21 of 53

Debug Straps

SSID = S.B

Standard Straps





CLK_SB_PCI4

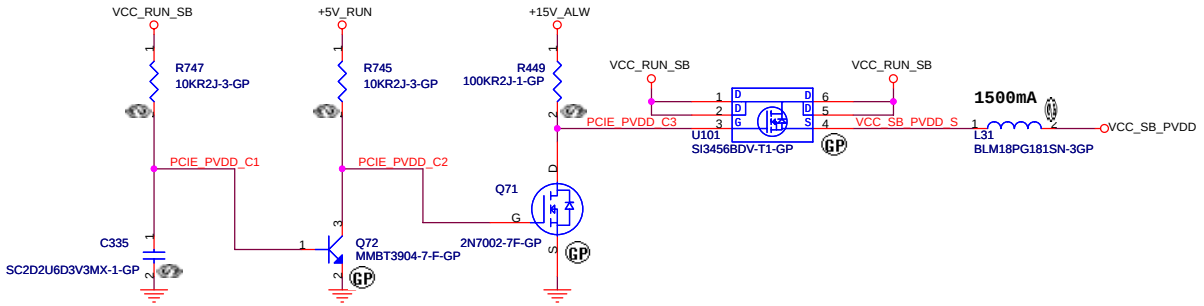
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6
HIGH	LONG RESET Default	PCI PLL Default	ACPI BCLK Default	IDE PLL Default	DEFAULT PCIE STRAPS Default	BOOTFAIL TIMER DISABLED Default	DEBUG STRAPS	INTERNAL RTC Default	INTERNAL PLL48	AMD CPU
LOW	SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED	IGNORE DEBUG STRAPS Default	EXTERNAL RTC	EXTERNAL 48MHZ Default	INTEL CPU Default

CLK_PCI_PCCARD

CLK_SB_PCI0

PCI_CLK0	PCI_CLK1	ROM TYPE
0	0	FWH
0	1	LPC
1	0	SPI Default
1	1	PCI

CLK_SB_PCI1



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *SB600-Strapping Pin(5/5)*

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 22 of 53

SSID = THERMAL

Note :

VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

EMC4001's GPIO1-6 are 3.3V tolerant only

Placement should be near the WWAN minicard connector just under the inserted minicard.

Thermistor

R443 = R526*((VOUT/1.22)-1)
VOUT=1.5V,R443=0.229*R526

Thermal sensor for CPU D1

REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil

Locate C350 near Guardian

place on the backside of the motherboard under CPU

Thermal sensor for SODIMM D3

REM_DIODE3_N and REM_DIODE3_P routing Trace width and Spacing use 10 / 10 mil

Locate C351 near Guardian

Please near the bottom SODIMM CONN

Thermal sensor for RS600ME D5

NB_THERMDA and NB_THERMDC routing Trace width and Spacing use 10 / 10 mil

Locate C368 near Guardian

Reserve area near NB for a cap between DP4/DN4

Thermal sensor for CPU DIODE D2

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

Locate C352 near Guardian

Thermal sensor for skin temp D4

REM_DIODE4_N and REM_DIODE4_P routing Trace width and Spacing use 10 / 10 mil

Locate C355 near Guardian

Thermal sensor mapping

D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

FAN

3V_PWROK#

CPU THERMALTRIP

<Variant Name>

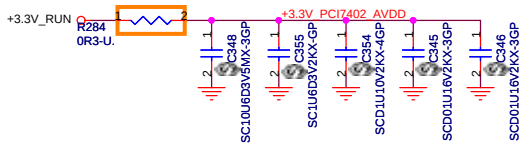
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN, EMC4001

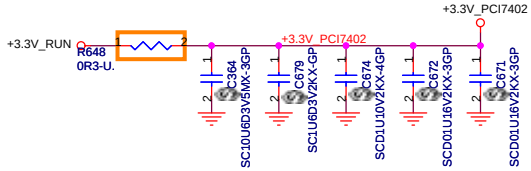
Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 23 of 53

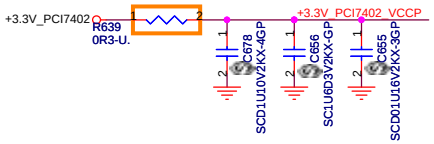
PCI7402_AVDD_33



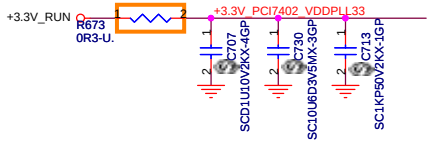
PCI7402_VCC



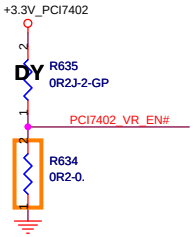
PCI7402_VCCP



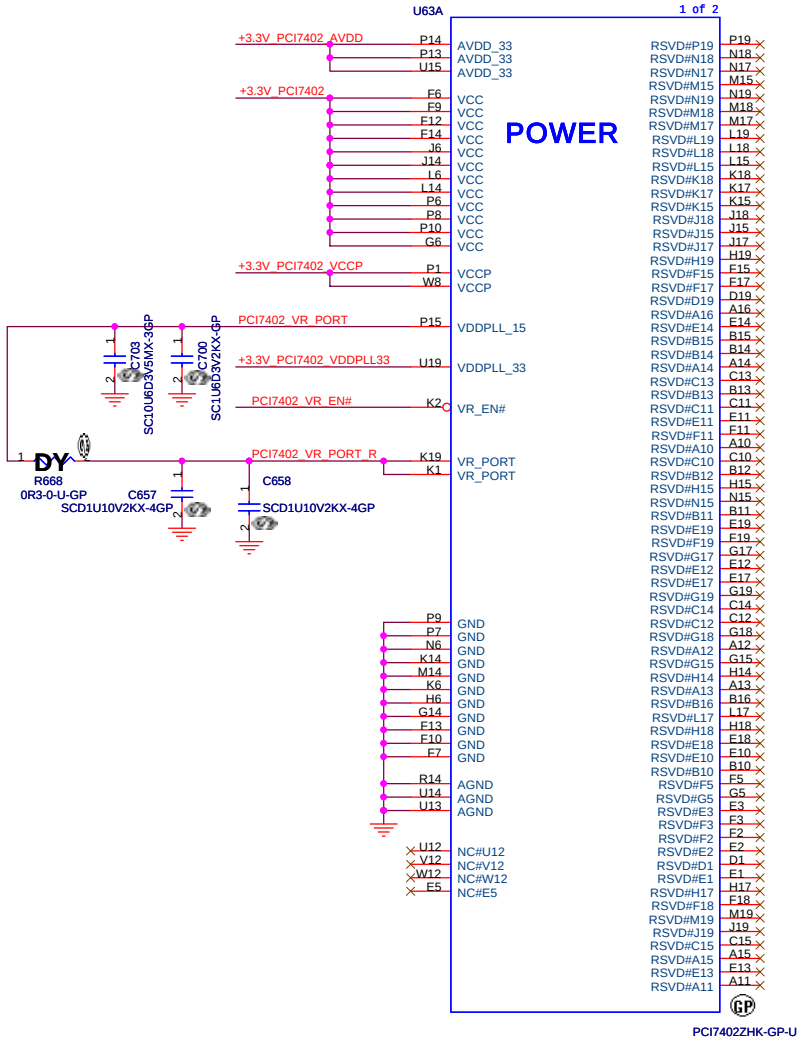
PCI7402_VDDPLL33



PCI7402_VR_EN#



SSID = 1394



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCI7402-1***

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 24 of 53

SSID = 1394

U63B — 2 of 2

PCI AD[0..31] — PCI / IEEE 1394

SD/MMC/MS/MS-PRO/SM/XD

Miscellaneous

PCI7402ZHK-GP-U

if want to use internal 1.5V regulator, must be use 0.1uF cap placed between pin T18 and R17

1394 Xtal

1394_X1 — R326 0R2-0. — 1394_X2 — X5 X-24D576MHZ-46GP

C386 SC12P50V2JN-3GP — C385 SC12P50V2JN-3GP

PCI-CLK EMI

CLOSE TO PIN L1

CLK_PCI_PCCARD — R631 22R2J-2-GP — PCLK_CBUS_E — C654 SC10P50V2JN-4GP — EMI

CLK 48M EMI

CLOSE TO PIN F1

CLK_SMCARD_48M — R636 10R2J-2-GP — CLK_CARD_48M_E — C667 SC4D7P50V2CN-1GP — EMI

MEDIA SLICE 1394

CLOSE TO PIN V16,W16,V15,W15

CHOCK put on MEDIA SLICE side

TO MEDIA SLICE

PHY_TEST_MA

+3.3V_PCI7402 — R674 330R2J-3-GP — PCI7402_PHY_TEST_MA — R671 330R2J-3-GP — DY

CLOSE TO PIN P17

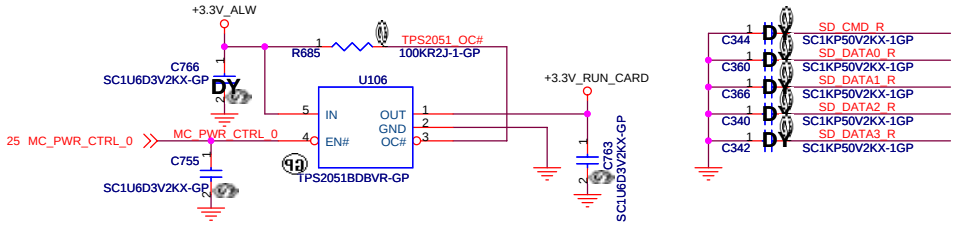
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

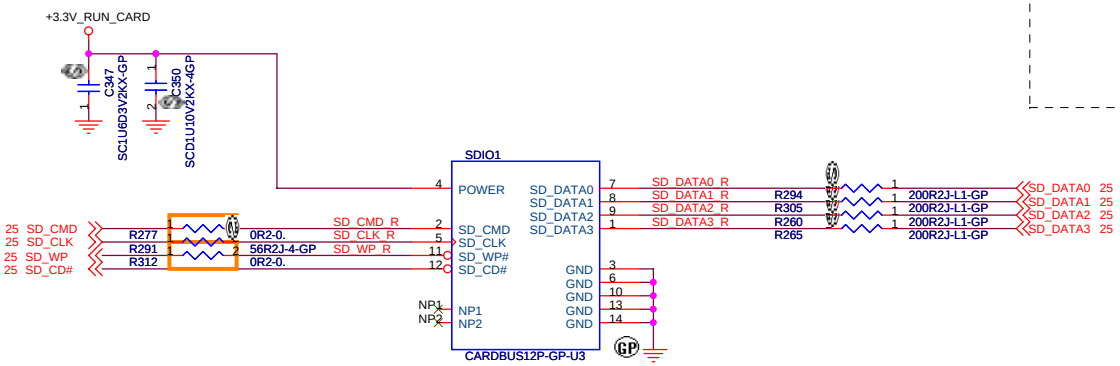
Title	PCI7402-2	
Size A3	Document Number: Parker	Rev: -1
Date: Tuesday, August 14, 2007	Sheet 25 of 53	

SD POWER-SWITCH

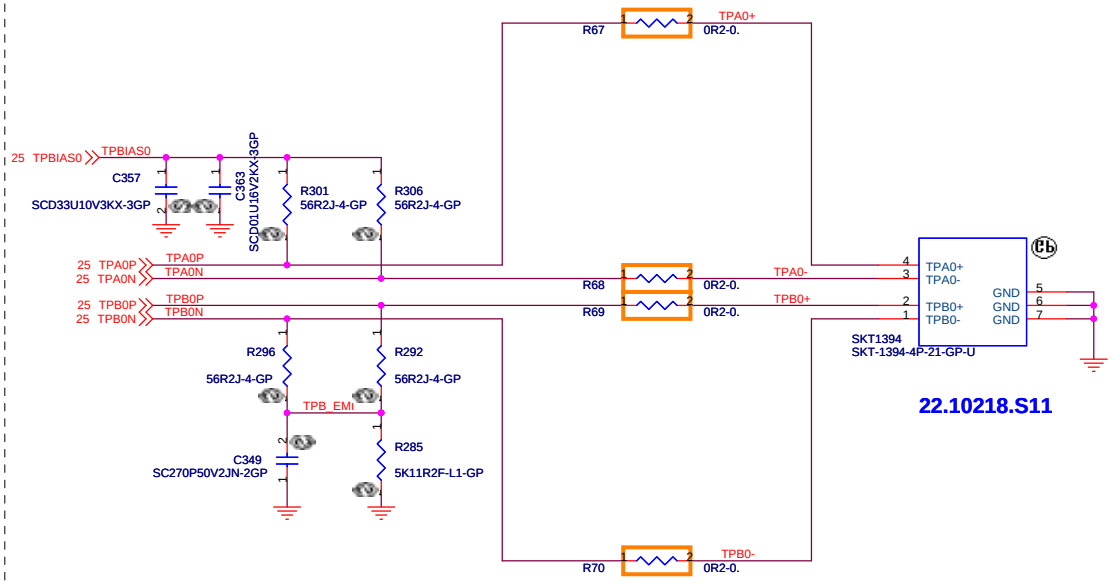
SSID = 1394



SD SOCKET



M/B 1394



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMART CARD/SD/1394(3/3)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 26 of 53

SSID = LOM

Closed to pin E4, J3, D6, G8

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Monitor GPHY PLL Clk

Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

Place resister as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.

Populate resister for debug

Place crystal less than 0.75" (~1.9cm) from LAN Controller

DOCKED
SEL 0:RJ45.
SEL 1:Dock.

Logic High Voltage must be 0.7V to 2.75V

LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.

Reserve for EMI

Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for bath footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.

	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

VDDIOPower Decoupling

Core Power Decoupling

VDDP Power Decoupling

place C937 near U91 pin L11

Place high-fregency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side ofthe cap to the ground via should also be minimized.

<Variant Name>

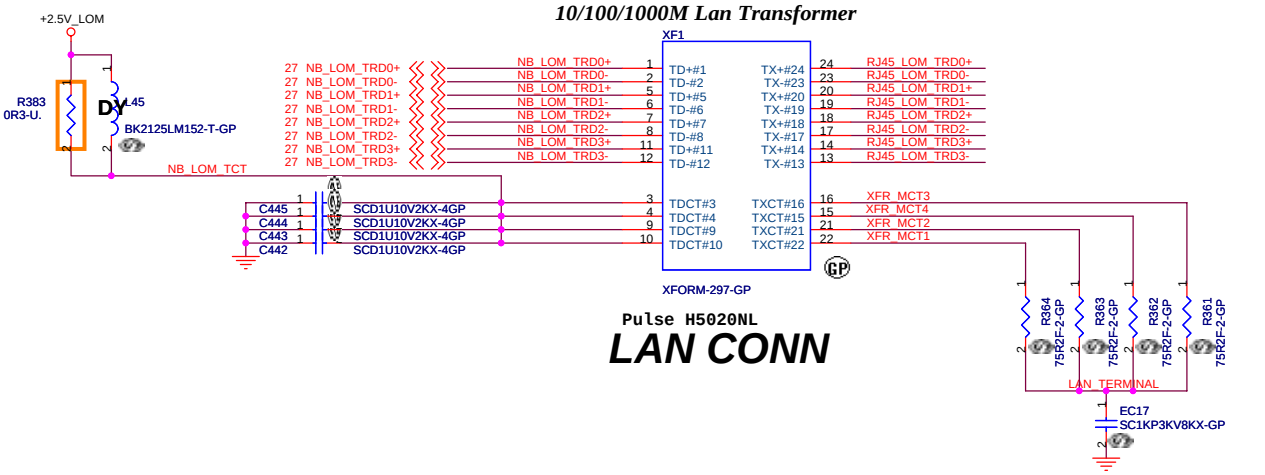
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

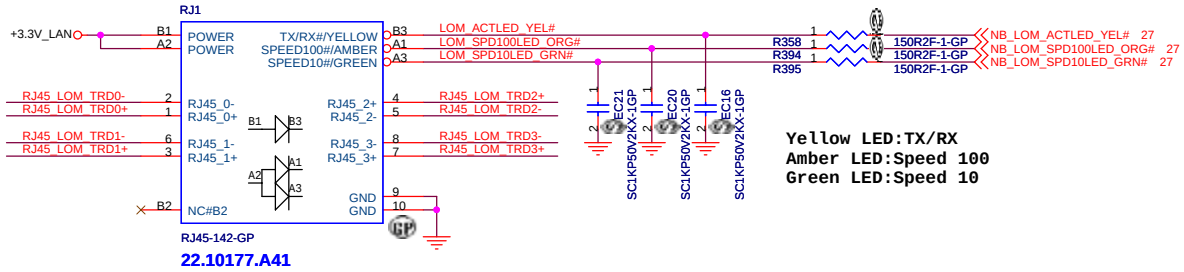
Title: LAN BCM5756ME

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 27 of 53

SSID = LOM





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

<Variant Name>

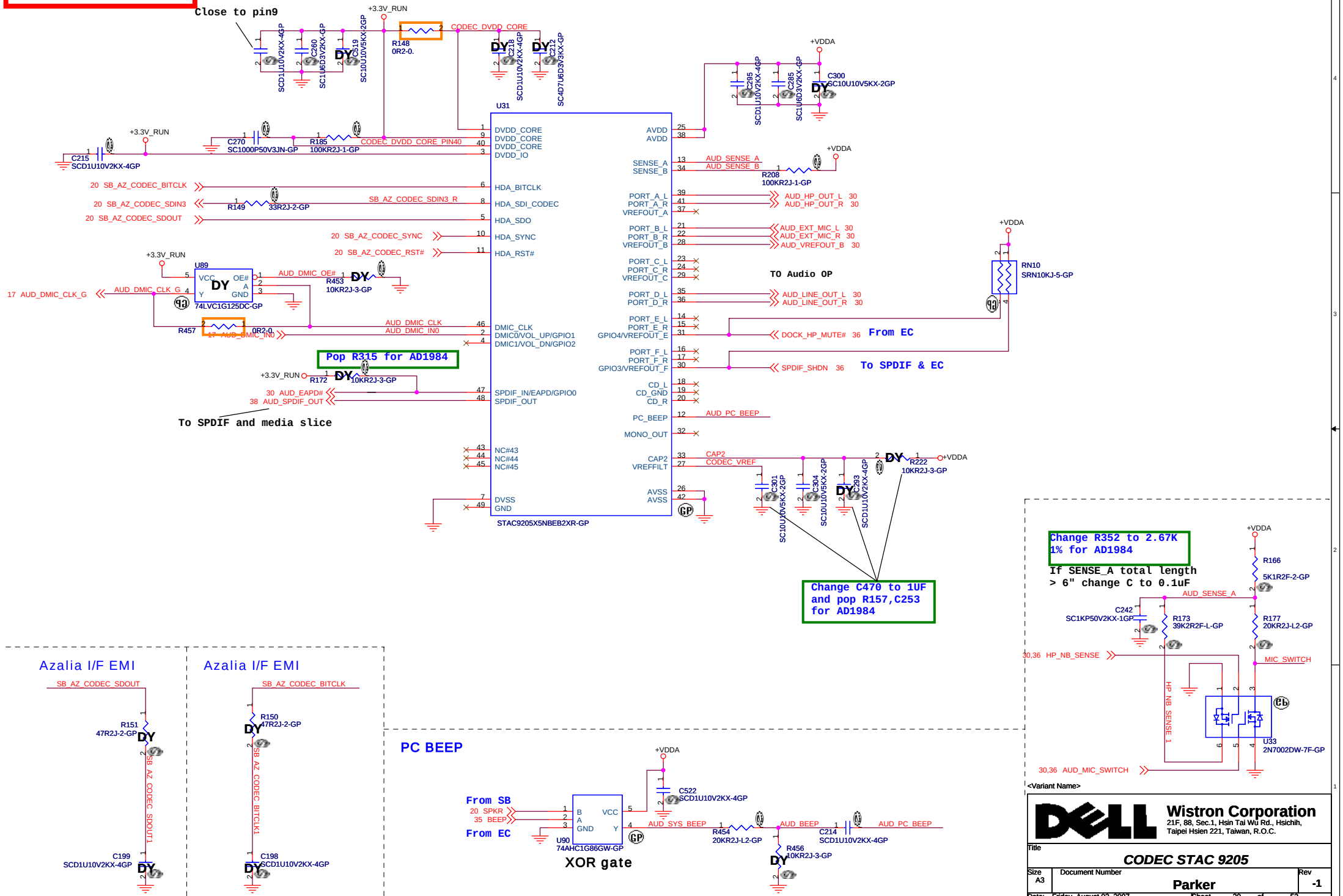
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LAN Connector*

Size: A3 | Document Number: Parker | Rev: -1

Date: Thursday, August 09, 2007 | Sheet 28 of 53

SSID = AUDIO



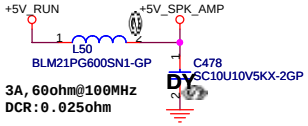
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

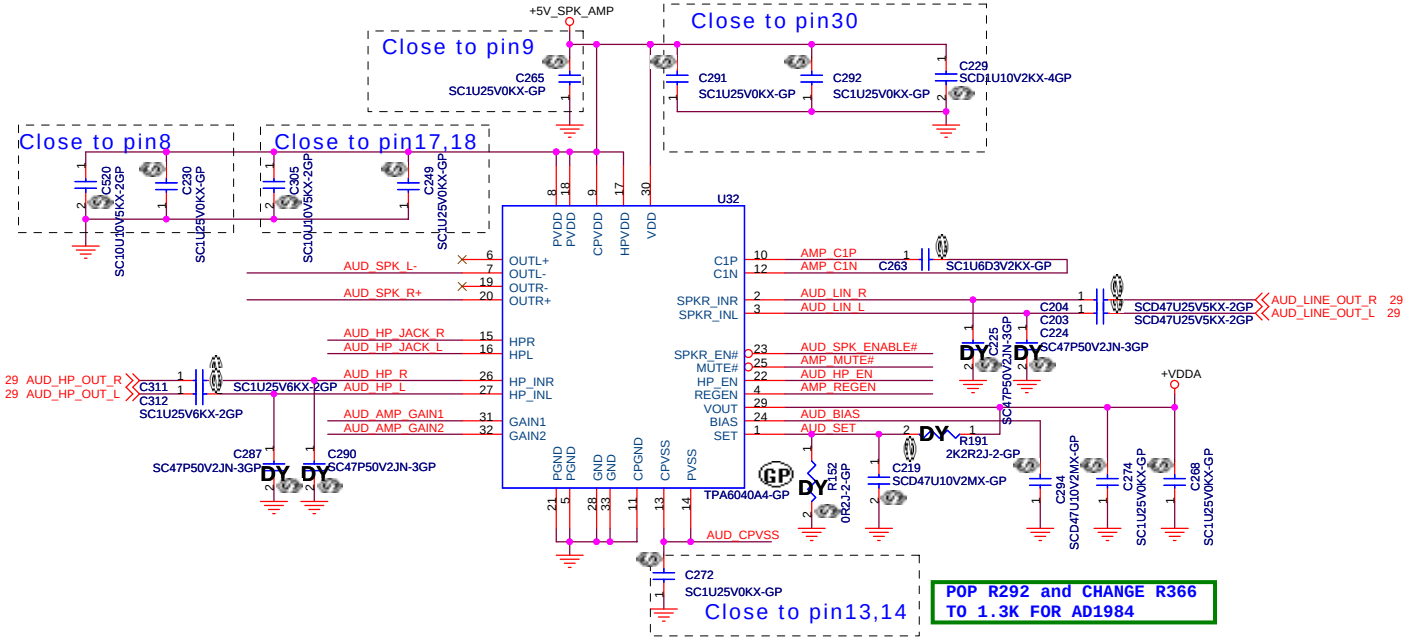
Title: CODEC STAC 9205

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 29 of 53

SSID = AUDIO

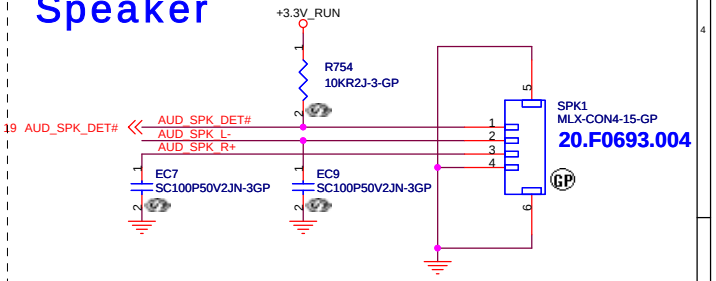




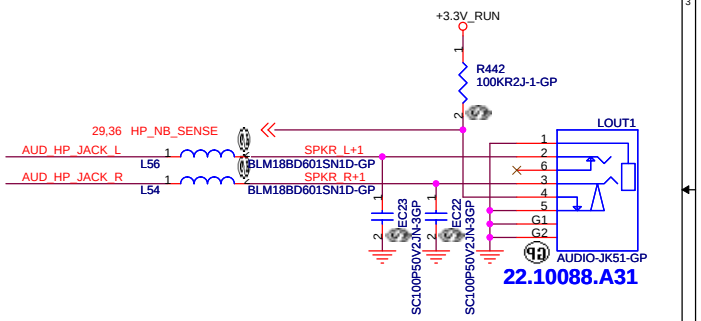
POP R292 and CHANGE R366 TO 1.3K FOR AD1984

U32 for TPA6040A4
Pop R746,C219,C220, Depop R152,R153,R210, Change C203,C204,C294 to 0.47UF
U32 for MAX9789A
Pop R152,R153,R210, Depop R746,C219,C220, Change C203,C204,C294 to 0.033UF

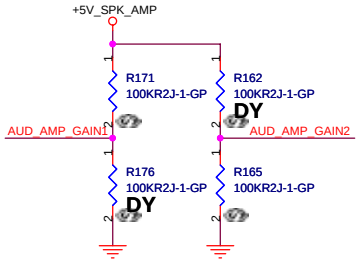
Speaker



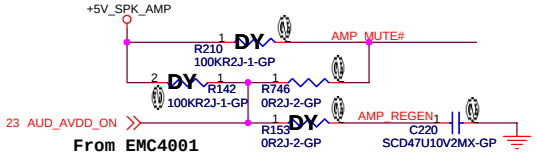
LINE OUT



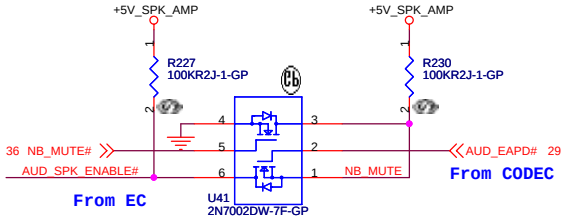
GAIN SETTING

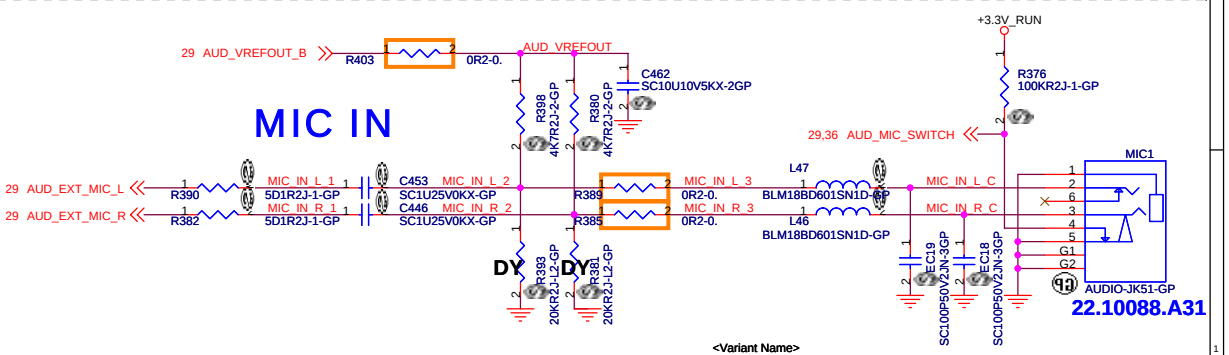


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

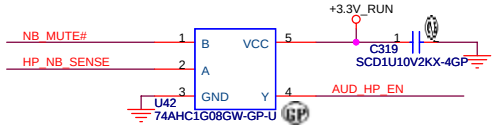


Signal inverter for speaker shutdown





AND Gate



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

Size	Document Number	Rev
A3	Parker	-1

Date: Thursday, August 09, 2007 Sheet 30 of 53

EXPRESS CARD POWER SWITCH

SSID = ExpressCard

Please Near the U32

+3.3V_SUS: C762 SCD1U10V2KX-4GP
+3.3V_RUN: C391 SCD1U10V2KX-4GP
+1.5V_RUN: C402 SCD1U10V2KX-4GP
+3.3V_CARDSUS: C403 SCD1U10V2KX-4GP
+3.3V_CARD: C390 SCD1U10V2KX-4GP
+1.5V_CARD: C765 SCD1U10V2KX-4GP

STBY# — R703 DY 0R2J-2-GP — EXPRCRD_STDBY# — EXPRCRD_STDBY# 36

EC5018

U65 TPS2231RGP-GP

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

+1.5V_RUN, +1.5V_CARD, +3.3V_CARD, +3.3V_RUN
NC#16, NC#14, NC#13, NC#5, NC#4
+1.5VIN, +1.5VOUT, +3VOUT, +3VIN
GND, THERMAL_PAD, OC#, RCLKEN, STBY#
AUXOUT, AUXIN, 1.5VOUT, 1.5VIN, 3.3VOUT, 3.3VIN

SHDN# — R704 100KR2J-1-GP — +3.3V_SUS
CARD_RESET#
CPUSB#
EXPRCRD_PWREN# — R705 100KR2J-1-GP
PERST#
CPPE#
NRST — R702 100KR2J-1-GP
SYSRST# — R680 0R2-0. — PLTRST# — PLTRST# 7,18,27,32,35,45,46,51

Test circuit
Use Card and No Card

+3.3V_CARDSUS, +3.3V_SUS, +1.5V_CARD, +3.3V_RUN, +3.3V_CARD, +1.5V_RUN

20 SB600_USBP6+ — R657 0R2-0. — USBP6D+
20 SB600_USBP6- — R658 0R2-0. — USBP6D-

Close EPR1

Geometry : 1759714-1
ERPSKT1
NP1
CARDBUS-SKT92-GP-U2
For Newcard socket

EXPRESS CARD
USB-PORT6

ERP1
CARDBUS26P-9GP-U
62.10024.891

8 PCIE_TX3+ — PCIE_TX3+
8 PCIE_TX3- — PCIE_TX3-
8 PCIE_RX3+ — PCIE_RX3+
8 PCIE_RX3- — PCIE_RX3-
4 CLK_PCIE_EXPCARD — CLK_PCIE_EXPCARD
4 CLK_PCIE_EXPCARD# — CLK_PCIE_EXPCARD#
36 EXPRCRD_PWREN# — EXPRCRD_PWREN#
4 CARD_CLK_REQ# — CARD_CLK_REQ#
+3.3V_CARD — CARD_RESET#
+3.3V_CARDSUS — PCIE_WAKE#_C
27,32,36 PCIE_WAKE# — PCIE_WAKE# — R649 0R2-0.
+1.5V_CARD
20,27,32 SB_SMB_DATA1 — SB_SMB_DATA1
20,27,32 SB_SMB_CLK1 — SB_SMB_CLK1
CPUSB#
USBP6D+
USBP6D-

EXPRESS PIN	
26	GND
25	PCIE_TXP4
24	PCIE_TXN4
23	GND
22	PCIE_RXP4
21	PCIE_RXN4
20	GND
19	CLK_PCIE_NEW
18	CLK_PCIE_NEW#
17	CPPE#
16	CONN_CLKREQ#
15	+3VRUN_NEW
14	+3VRUN_NEW
13	PERST#
12	+3VAUX_NEW
11	PCIE_WAKE#
10	+1.5VRUN_NEW
9	+1.5VRUN_NEW
8	SMB_DATA
7	SMB_CLK
6	TP1
5	TP2
4	CPUSTB#
3	USB+
2	USB-
1	GND

+3.3V_CARD: C668 SC10U10V5KX-2GP
+3.3V_CARD: C665 SCD1U10V2KX-4GP
+1.5V_CARD: C697 SC10U10V5KX-2GP
+1.5V_CARD: C680 SCD1U10V2KX-4GP

Please Near the EPR1

USB-PORT7

SSID = User.interface

Bluetooth Module conn.

BT1 MLX-CON10-7-GP
20.D0183.110

20 SB600_USBP7+
20 SB600_USBP7-
32 COEX1_BT_ACTIVE
36 BT_RADIO_DIS#
32 COEX2_WLAN_ACTIVE
BT_ACTIVITY

+3.3V_RUN
C756 SCD1U10V2KX-4GP
C760 SC4D7U6D3V3KX-GP
R679 10KR2J-3-GP

Note:Place R310 near CN13.

This circuit is only needed if the platform has the SNIFFER

+5V_RUN
R707 10KR2J-3-GP
33,36 LED_MASK#
17 BT_ACTIVE# — BT_ACTIVE#
Q65 2N7002-7F-GP
R697 DY 0R2J-2-GP
BT_ACTIVITY 1# — BT_ACTIVITY 1# 32
Q64 MMBT3904-7-F-GP

Sniffer LED.

yellow
35 SNIFFER_YELLOW# — Q35 DTA114YKA-1-GP — SNIFFER_Y
+3.3V_SUS

+3.3V_SUS — R297 100KR2J-1-GP
35 SNIFFER_BLUE# — Q34 2N7002-7F-GP — SNIFFER_BLUE# 1
Q33 DTA114YKA-1-GP — SNIFFER_B
+5V_SUS

blue

R308 470R2J-2-GP
R309 470R2J-2-GP
26 SNIFFER_DET# — SNIFFER_DET#
RSNIFFER_Y
RSNIFFER_B

SNIFFER1 HRS-CON6-3-GP
20.K0267.006

SSID = User.interface

Sniffer Switch

+3.3V_RUN
R313 100KR2J-1-GP
36 WIRELESS_ON/OFF# — R318 0R2-0. — SNIFFER1
DY C367 SC1U6D3V2KX-GP

SNIFFER2

+RTC_CELL
R317 100KR2J-1-GP
35 SNIFFER_PWR_SW# — R319 0R2-0.
DY C371 SC1U6D3V2KX-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXPRESS CARD/BT/SNIFFER
Size: A3 | Document Number: Parker | Rev: -1
Date: Friday, August 03, 2007 | Sheet 31 of 53

SSID = WWAN

MiniCard WWAN connector

USB-PORT9

Close MINICARD2(WWAN)

C593 Please Near the MINICARD2/Pin24

Place caps closest to the SIM connector

Layout Note: Place resistors close to choke as possible to minimize stubs.

62.10024.841

62.10043.481

62.10043.491

SSID = WLAN

MiniCard WLAN connector

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

C587 Please Near the MINICARD1/Pin24

Prevent backdrive when WoW is enabled.

For Debug card used only.

62.10043.481

62.10043.491

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN/WWAN

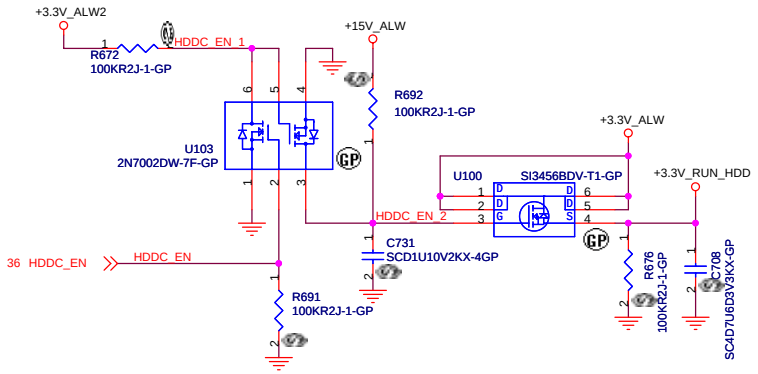
Size: Custom | Document Number: Parker | Rev: -1

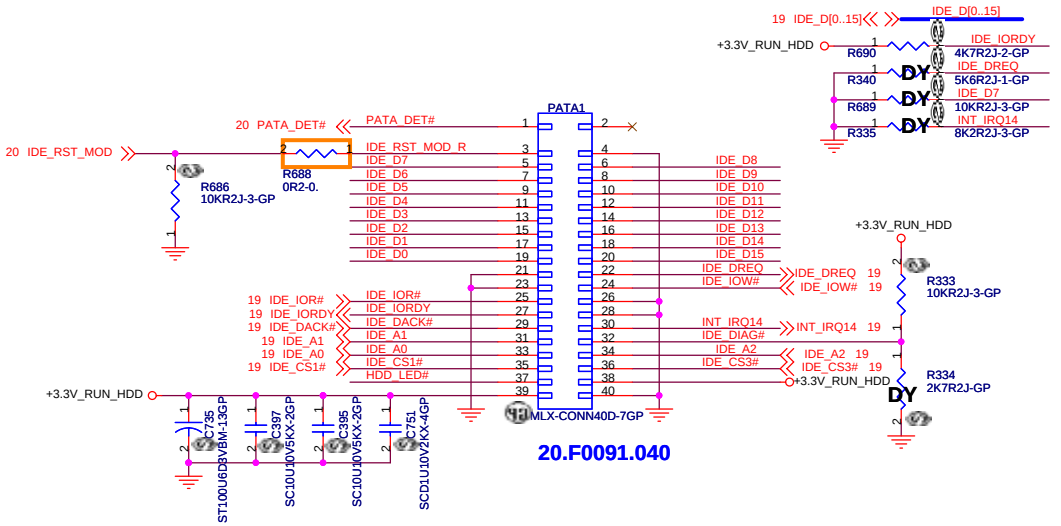
Date: Friday, August 03, 2007 | Sheet 32 of 53

SSID = PATA

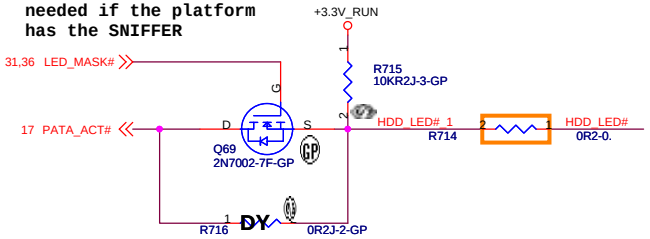
PATA HDD conn.

SSID = PATA





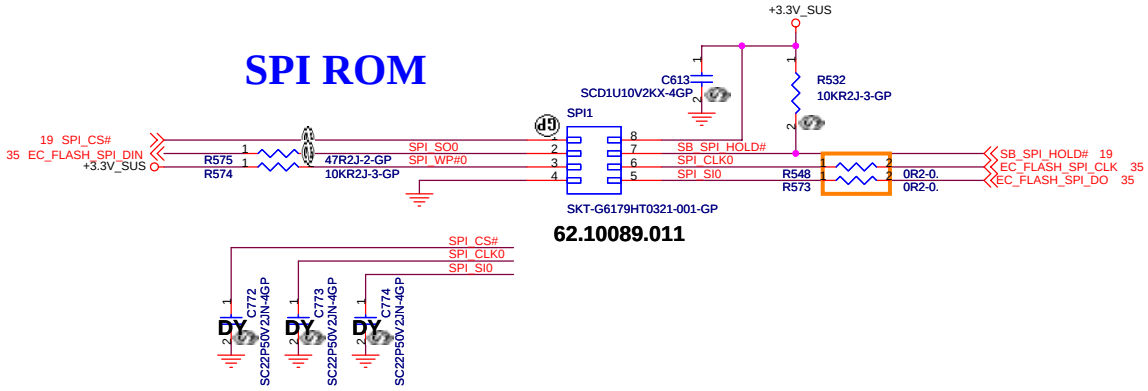
This circuit is only needed if the platform has the SNIFFER



SSID = Flash.ROM

SPI BIOS :SST FEROM 25VF016B
P/N:72.25016.A01
SPI BIOS socket :62.10076.011

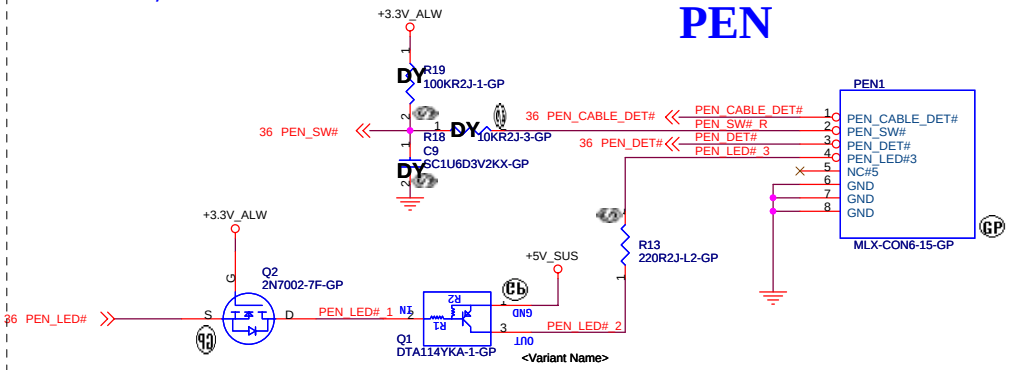
SPI ROM



SSID = User.interface

JUST SUPPORT S3 WAKE UP,CHANGE TO SUS POWER

PEN



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/SPI ROM/PEN

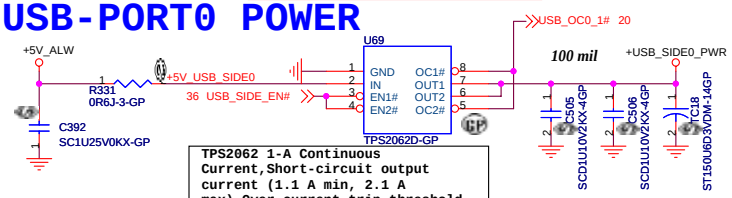
Size	Document Number	Rev
A3	Parker	-1

Date: Thursday, August 09, 2007 Sheet 33 of 53

USB POWER

SSID = USB

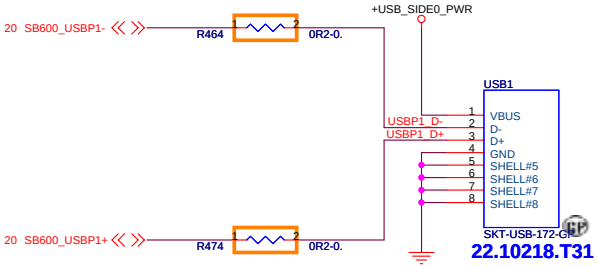
USB-PORT0 POWER

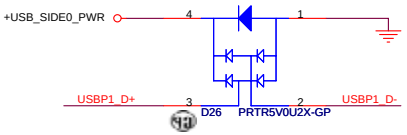


TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.

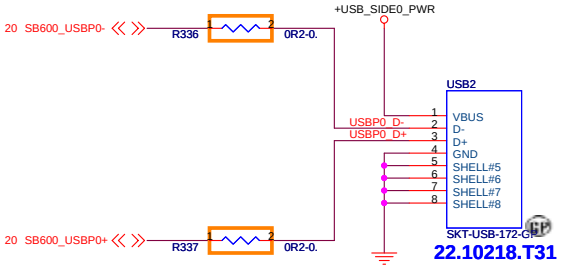
ESD Cap must near USB connector

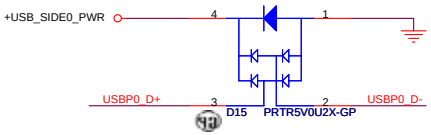
USB-PORT1





USB-PORT0

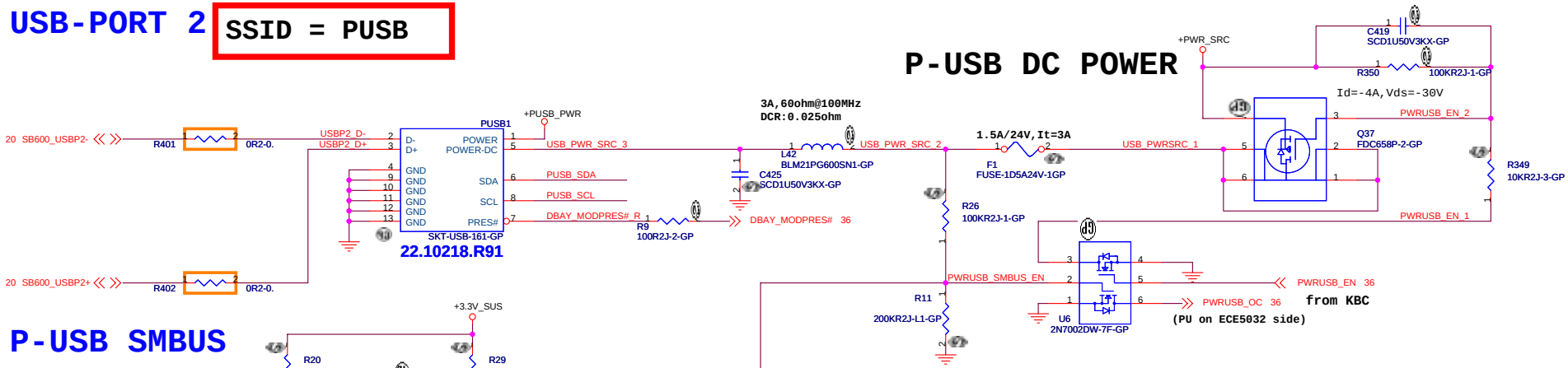




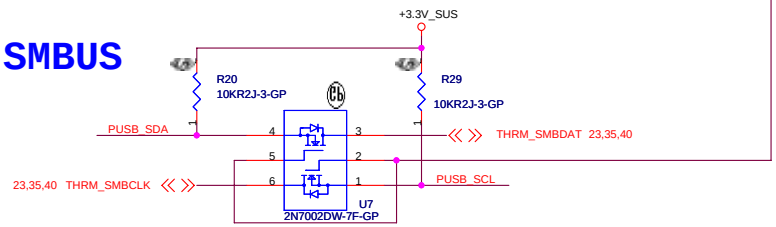
USB-PORT 2

SSID = PUSB

P-USB DC POWER

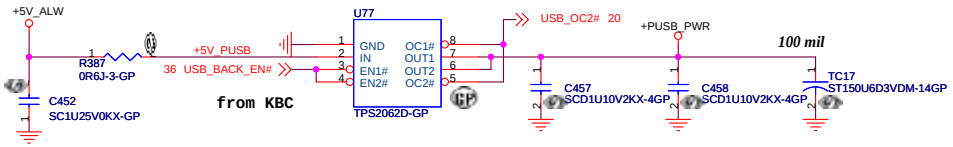


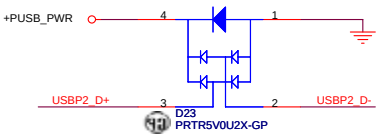
P-USB SMBUS



P-USB POWER

TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: P-USB/USB

Size: Custom | Document Number: Parker | Rev: -1

Date: Thursday, August 09, 2007 | Sheet 34 of 53

SSID = KBC

ATI versus Intel chipset to allow power sequence differences.
ATI is Logic High.
Intel is Logic Low.

Place cap close to pin 121

Place these caps close to MEC5025.

Note: MEC5025 KSO3/GPIOC3 pin 29 was 3V_5V_SUS_PWRGD, M08 platforms already had 3V_5V_SUS_PWRGD from the discrete component.

ECE1077 BC bus

ECE5021 BC bus

TP

Flash Recovery.
1=Enabled
0=Disabled

Low=
Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

Not Stuff R921 0 ohm when doing Flash recovery.

Debug Serial Port
Flash Recovery port.

To KBC 5025

U30 MEC5025-NU-1-GP

U52 74AHCT1G125GW-1-GP

Q45 2N7002-7F-GP

Q47 MMBT3904-7-F-GP

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

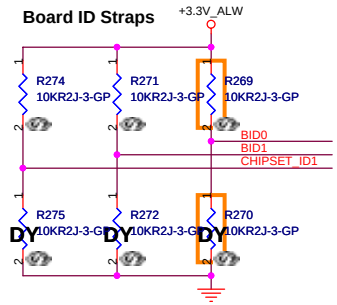
Title: KBC MEC5025

Size: A3 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 35 of 53

SSID = SIO

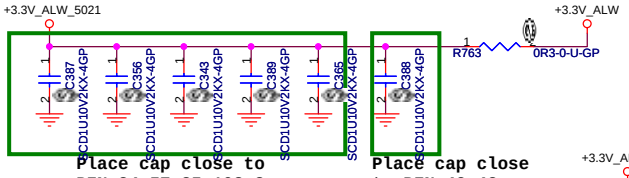
Board ID Straps

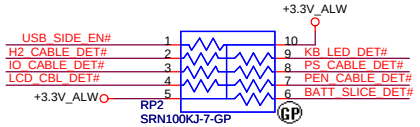


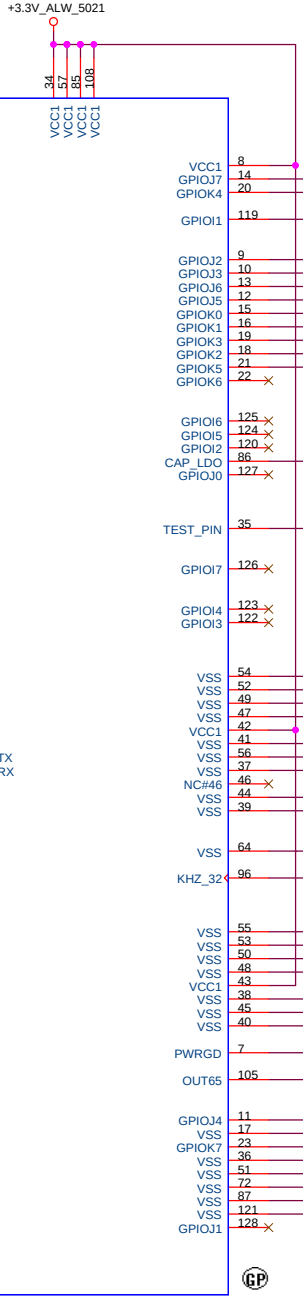
BID1	BID0	Board Rev.
0	0	SST(X00)
0	1	PT(X01)
1	0	ST(X02)
1	1	X-B(A00)

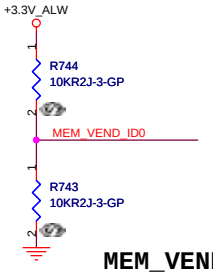
CHIPSET_ID1

This resistor strapping will not change and is used to identify parker chipset as ATI



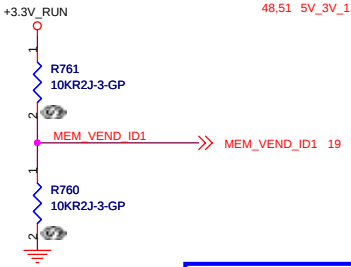






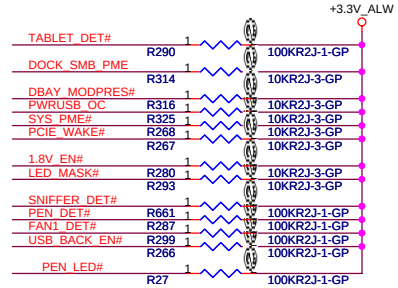
MEM_VEND_ID support

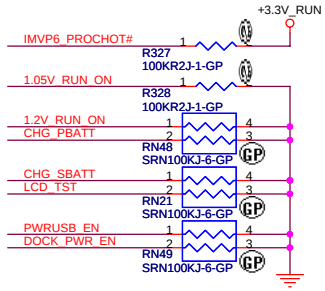
	MEM_VEND_ID1	MEM_VEND_ID0
Sansung	H	L
Hynix	L	H
Mircon	L	L

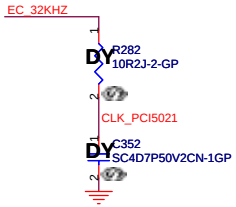


VGA_IDENTIFY
Low=UMA, High=Discrete

1105







Parker

Wistron Corporation
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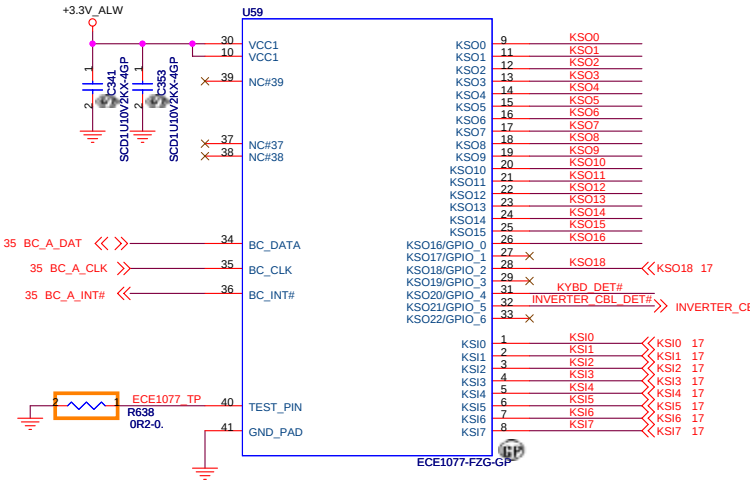
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SIO ECE5021		
Size: A3	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 36 of 53	

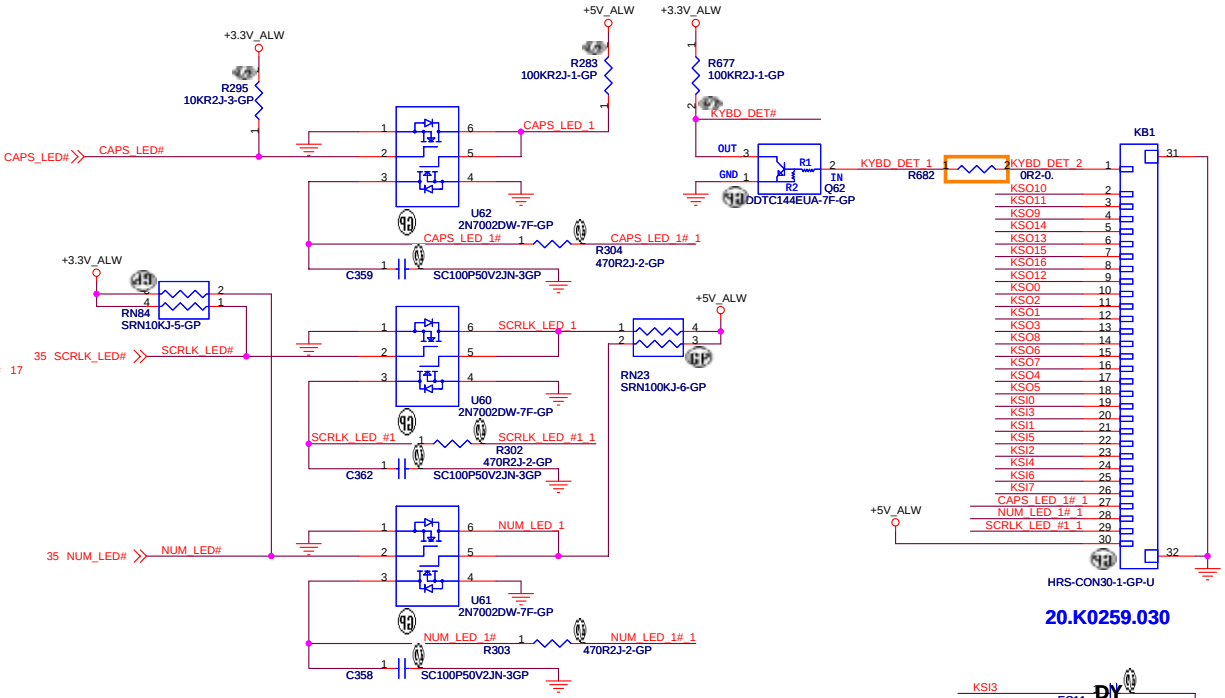
K/B CONN.

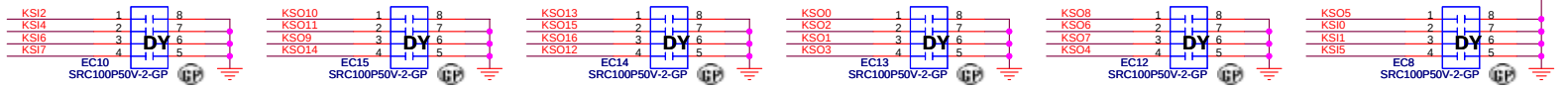
SSID = User.interface



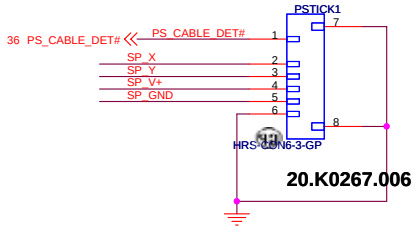
PLACE HOLDER

KB LEDs

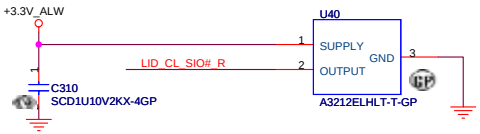


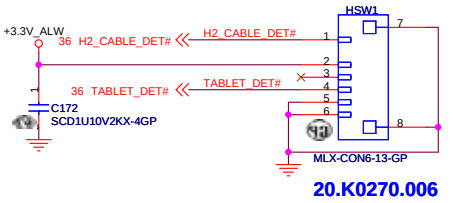


POINT-STICK CONN.

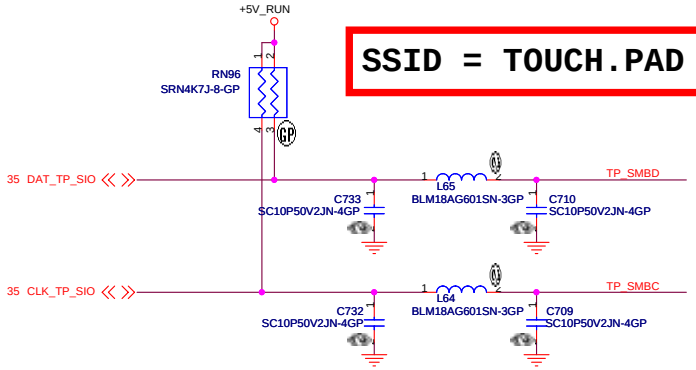


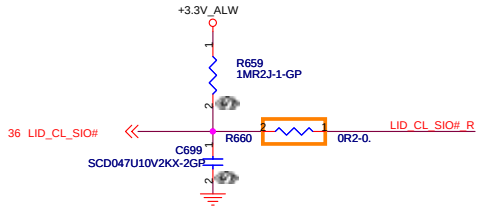
hall switch



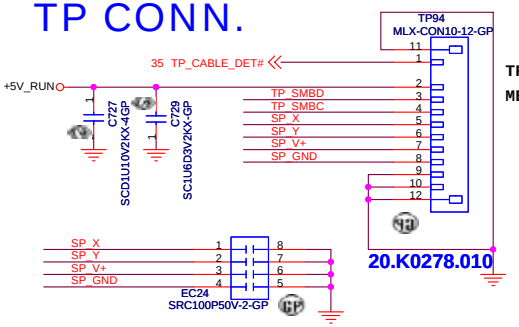


SSID = TOUCH.PAD





TP CONN.



TP AND POWER MEC5025 CONNECT

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ECE1077

Size: Custom | Document Number: Parker | Rev: -1

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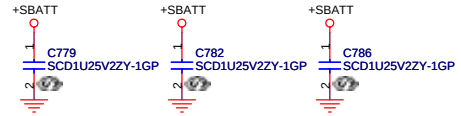
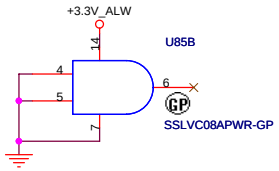
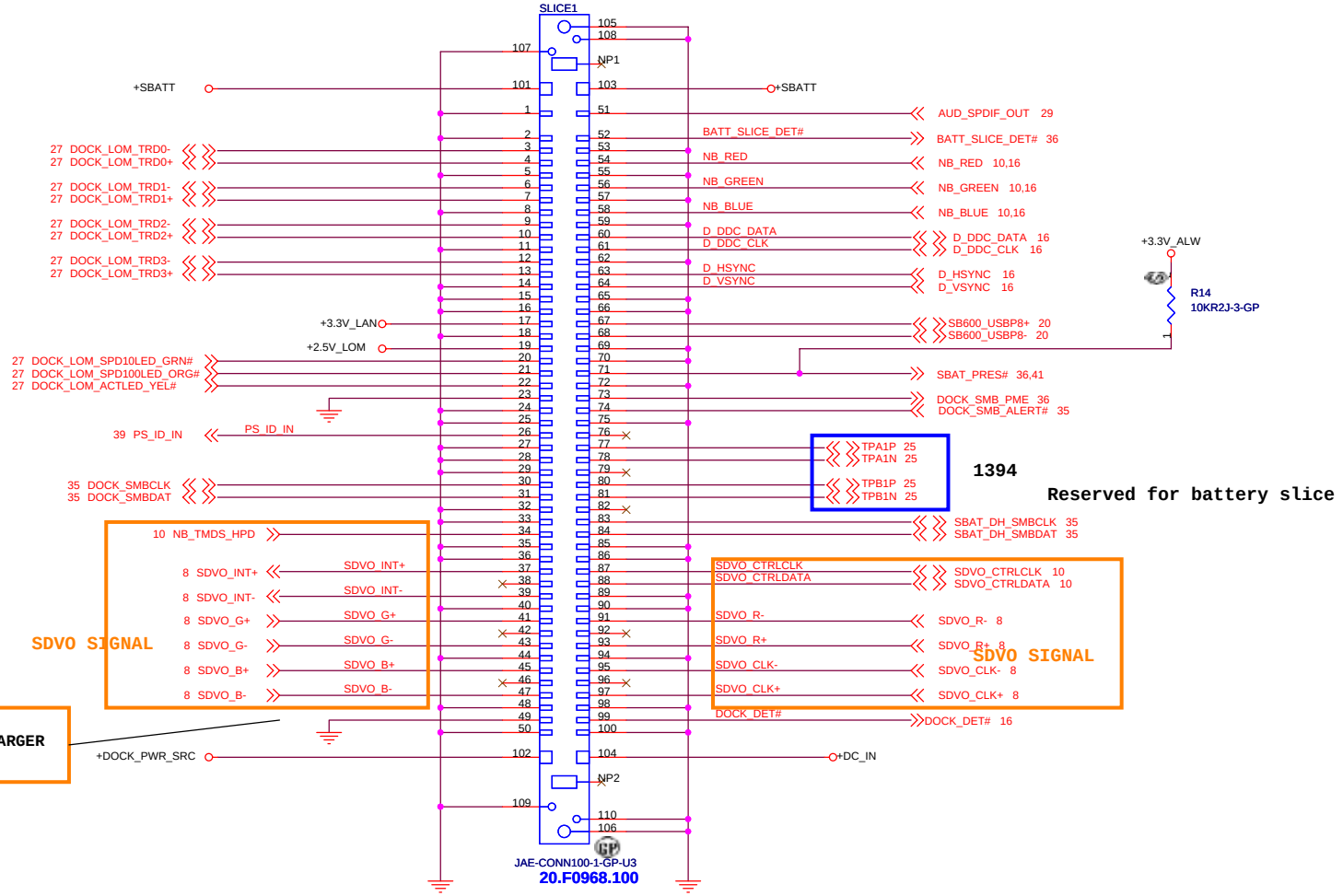
SSID = MEDIA SLICE

The green frame are used to battery_slice

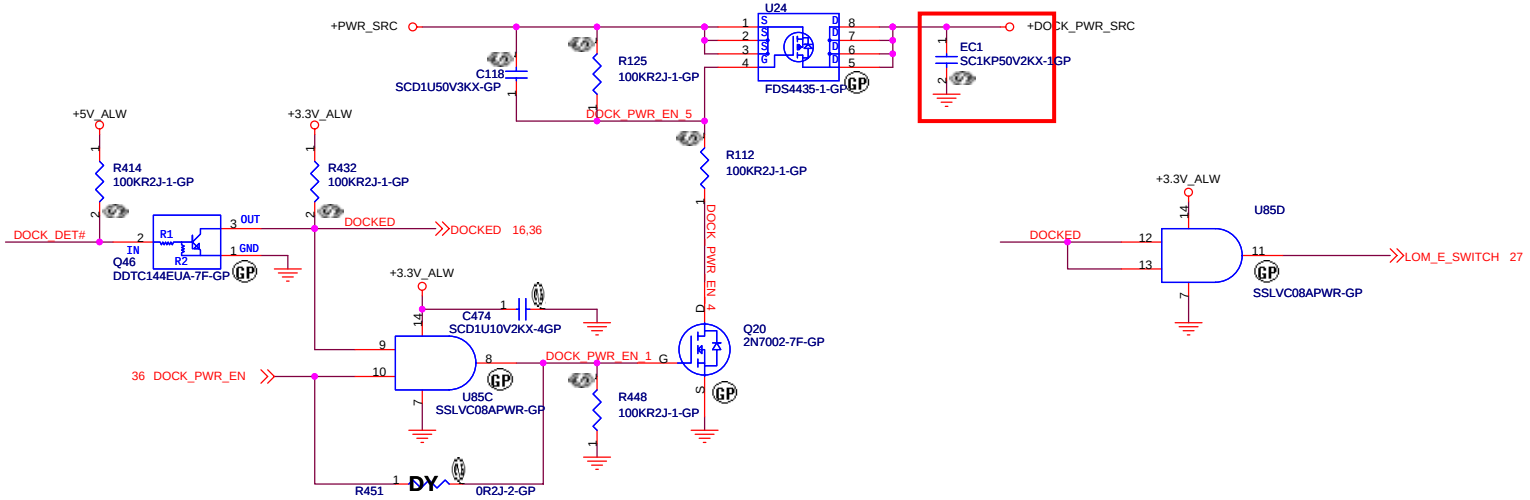






USE TO BATT_SLICE_DET# GND

USE TO BATT_SLICE GND ON/OFF CHARGER (battery slice side SYS_PRES#)



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MEDIA SLICE***

Size	Document Number	Rev
A3	Parker	-1

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SSID = PWR.Support

Adapter In

DC_IN CONN	
PIN 1,2	DC_IN+
PIN 4,8	DC_IN-
PIN 5	ID
PIN 3,6,7,9	GND

22.10140.321

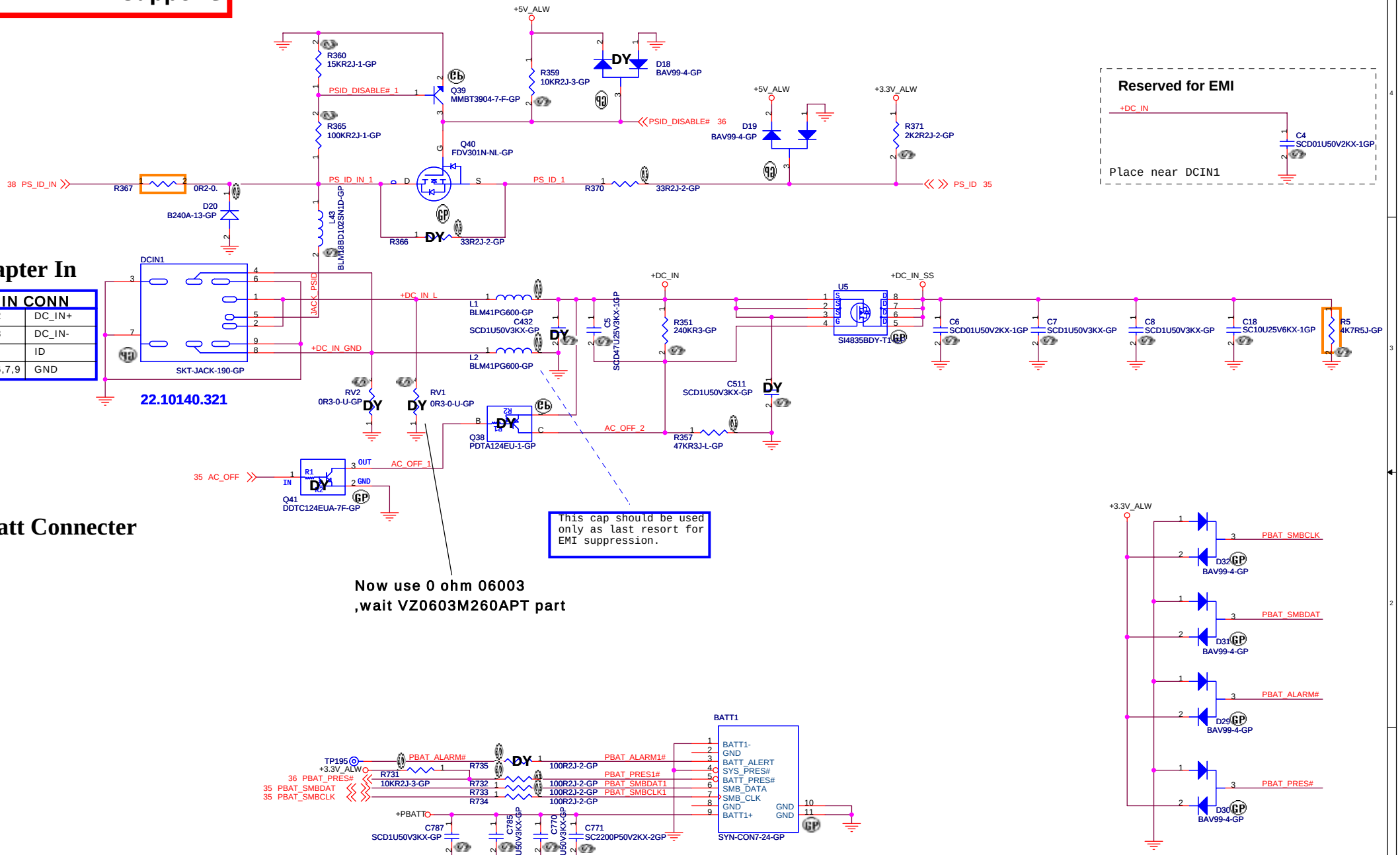
Batt Connecter

Now use 0 ohm 06003
,wait VZ0603M260APT part

This cap should be used only as last resort for EMI suppression.

Reserved for EMI

Place near DCIN1



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN / BATT CONN.

Size: A3 | Document Number: Parker | Rev: -1

Date: Tuesday, August 14, 2007 | Sheet 39 of 53

SSID = CHARGER

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

Adapter (W)	Trip Current (A)	R1620	R1621	R1622	R1623
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R23 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.

This Resistor must be 1% tolerance.

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

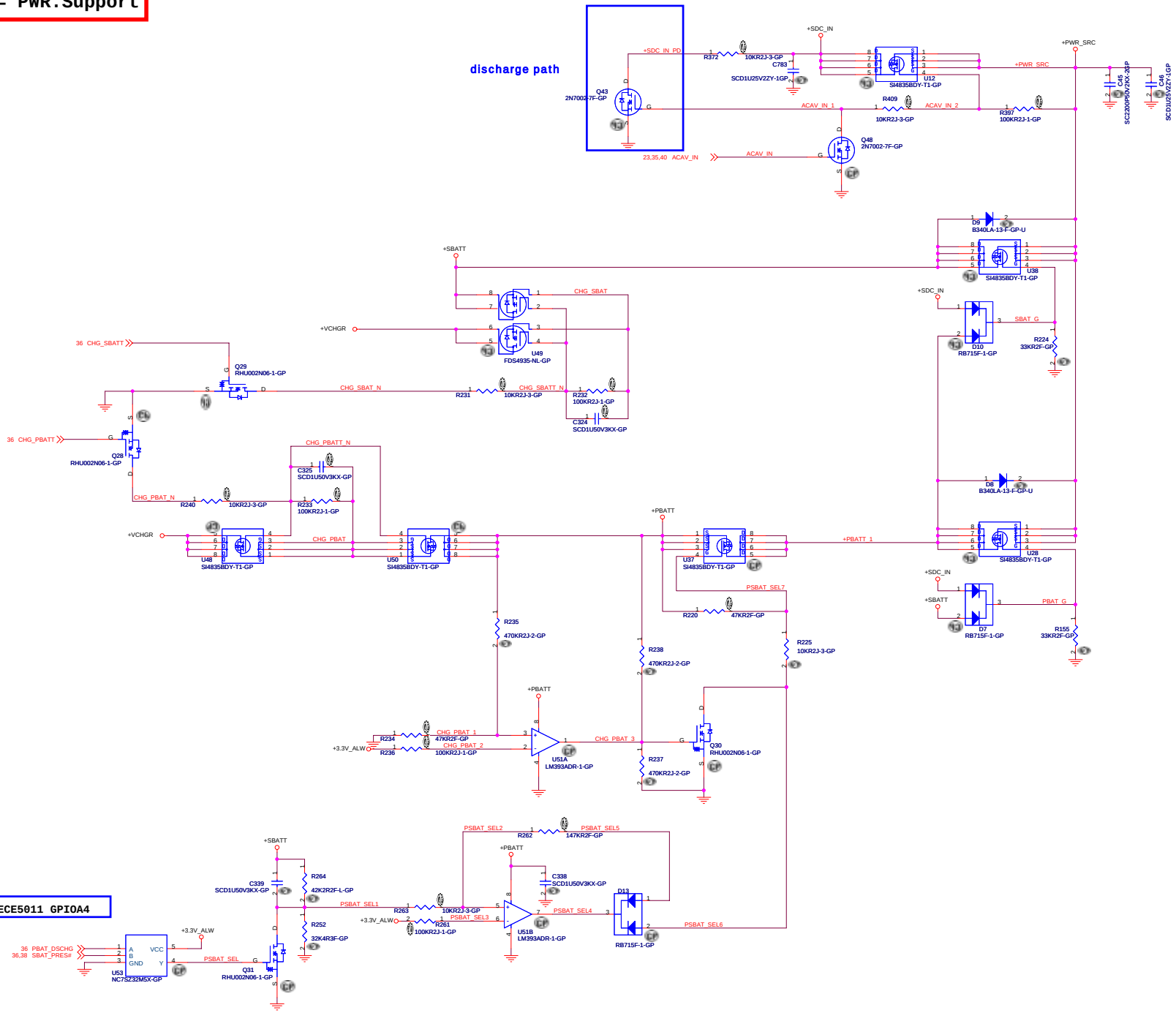
REF DES	MAXIM	INTERSIL
R1610	8.45K 1%	DUMMY
C1412	0.01uF	0.1uF
C1404	0.1uF 10V	DUMMY
C1408	1uF 10V	DUMMY
R1602	365K 1%	215K 1%
R1609	0 5%	10 5%
R1601	0 5%	10 5%
C1402	DUMMY	0.22uF
C1388	DUMMY	0.22uF
C1406	0.01uF	DUMMY
C1409	0.1uF 10V	DUMMY
C1399	220pF 50V	DUMMY
D36	RB751V-40	DUMMY
C1398	3.3nF	DUMMY
R1607	1 1%	0 5%
R1612	100 5%	0 5%
R1759	0 5%	8.45K 1%
R1611	10K 5%	2.2K 5%
C1405	0.01uF	0.01uF
C1407	0.01uF	0.01uF
R1606	1K 5%	DUMMY
D35	ISS355	DUMMY

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger
Size: Custom | Document Number: Parker | Rev: -1
Date: Thursday, August 09, 2007 | Sheet 40 of 53

SSID = PWR.Support



In M07,use ECE5011 GPIOA4

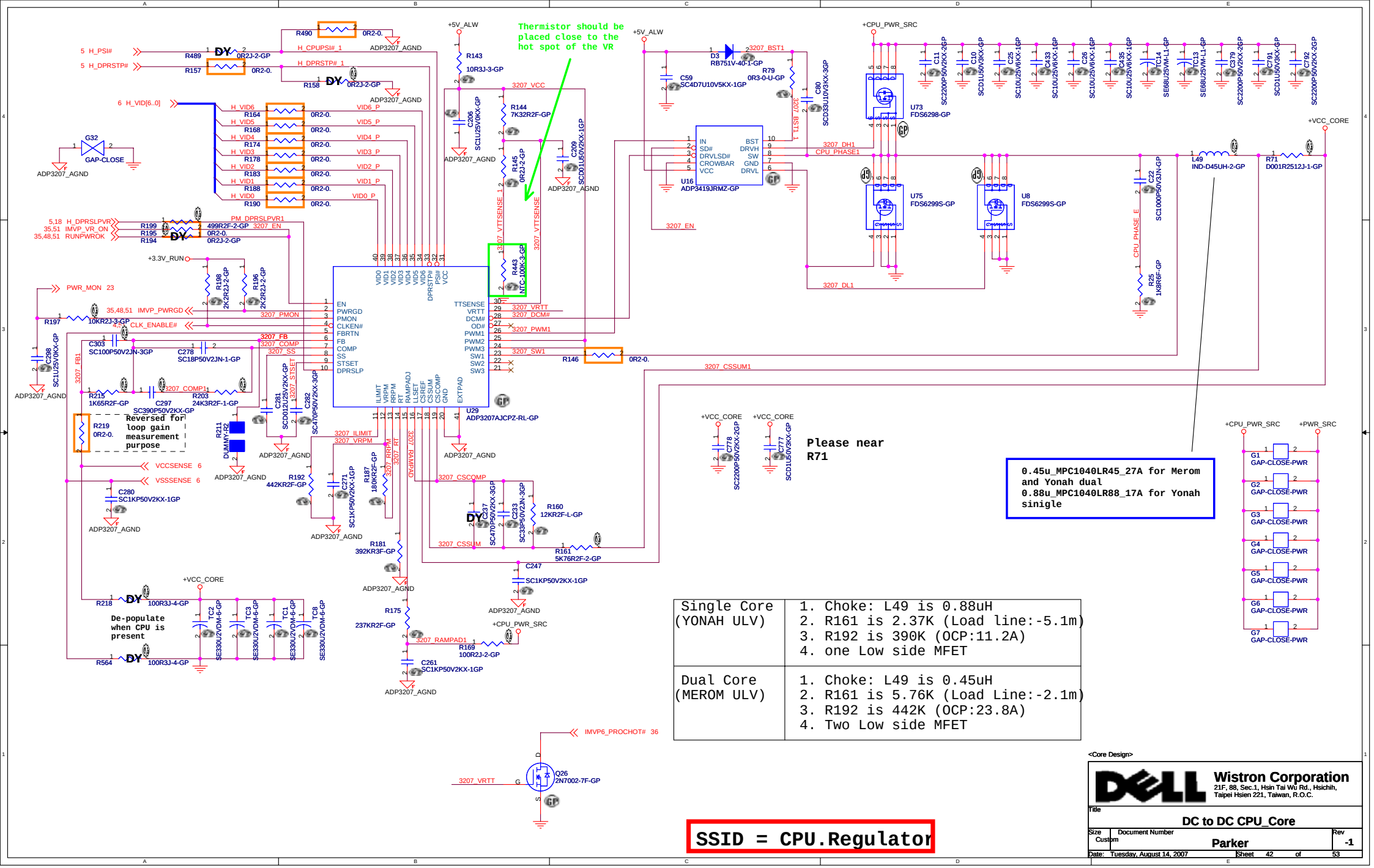
<Variant Name>

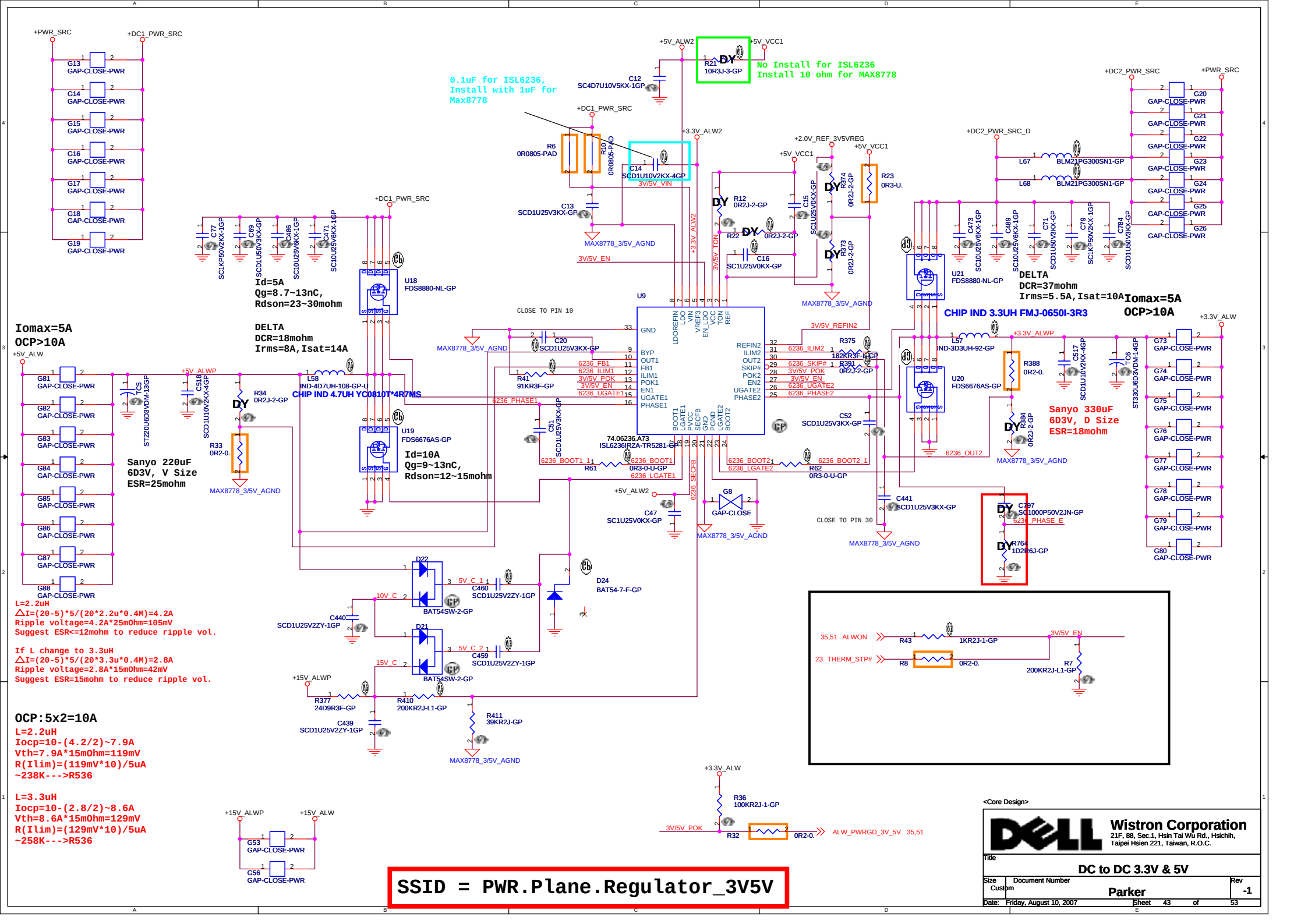
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATTERY SELECT**

Size	Document Number	Rev
A2	Parker	-1

Date: Friday, August 03, 2007 Sheet 41 of 53


Thermistor should be placed close to the hot spot of the VR
U29 ADP3207AJCPZ-RL-GP
U16 ADP3419JRMZ-GP
U73 FDS6298-GP
U75 FDS6299S-GP
U8 FDS6299S-GP
Q26 2N7002-7F-GP
D3 RB751V-40-1-GP
L49 IND-D45UH-2-GP
R71 D001R2512J-1-GP
R146 0R2-0.
R143 10R3J-3-GP
R144 7K32R2F-GP
R145 0R2J-2-GP
R443 NTC-100K-3-GP
R79 0R3-0-U-GP
R25 1K8R6F-GP
R192 442KR2F-GP
R187 180KR2F-GP
R160 12KR2F-L-GP
R161 5K76R2F-2-GP
R181 392KR3F-GP
R175 237KR2F-GP
R169 100R2J-2-GP
R211 DUMMY-R2
R219 0R2-0.
Reversed for loop gain measurement purpose
De-populate when CPU is present
Please near R71
0.45u_MPC1040LR45_27A for Merom and Yonah dual
0.88u_MPC1040LR88_17A for Yonah sinigle
+5V_ALW
+3.3V_RUN
+VCC_CORE
+CPU_PWR_SRC
+PWR_SRC
ADP3207_AGND
3207_VCC
3207_VTTSENSE
3207_VTTSENSE_1
3207_DH1
3207_BST1
3207_BST1_1
CPU_PHASE1
3207_DL1
3207_EN
3207_CSSUM1
3207_FB
3207_COMP
3207_SS
3207_STSET
3207_COMP1
3207_ILIMIT
3207_VRPM
3207_RRPM
3207_RT
3207_RAMPAD
3207_RAMPAD1
3207_CSCOMP
3207_CSSUM
3207_VRTT
3207_DCM#
3207_PWM1
3207_SW1
PM_DPRSLPVR1
PWR_MON 23
VCCSENSE 6
VSSSENSE 6
IMVP6_PROCHOT# 36
5 H_PSI#
5 H_DPRSTP#
6 H_VID[6..0]
5,18 H_DPRSLPVR
35,51 IMVP_VR_ON
35,48,51 RUNPWROK
35,48,51 IMVP_PWRGD
4,5 CLK_ENABLE#
Single Core (YONAH ULV)
1. Choke: L49 is 0.88uH
2. R161 is 2.37K (Load line:-5.1m)
3. R192 is 390K (OCP:11.2A)
4. one Low side MFET
Dual Core (MEROM ULV)
1. Choke: L49 is 0.45uH
2. R161 is 5.76K (Load Line:-2.1m)
3. R192 is 442K (OCP:23.8A)
4. Two Low side MFET
SSID = CPU.Regulator
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC to DC CPU_Core
Size Custom
Document Number
Parker
Rev -1
Date: Tuesday, August 14, 2007
Sheet 42 of 53


+PWR_SRC
+DC1_PWR_SRC
G13 GAP-CLOSE-PWR
G14 GAP-CLOSE-PWR
G15 GAP-CLOSE-PWR
G16 GAP-CLOSE-PWR
G17 GAP-CLOSE-PWR
G18 GAP-CLOSE-PWR
G19 GAP-CLOSE-PWR
+5V_ALW2
+5V_VCC1
R21 10R3J-3-GP
No Install for ISL6236
Install 10 ohm for MAX8778
0.1uF for ISL6236,
Install with 1uF for
Max8778
C12 SC4D7U10V5KX-1GP
+3.3V_ALW2
+2.0V_REF_3V5VREG
R6 0R0805-PAD
R10 0R0805-PAD
C14 SCD1U10V2KX-4GP
3V/5V_VIN
C13 SCD1U25V3KX-GP
MAX8778_3/5V_AGND
3V/5V_EN
R12 0R2J-2-GP
R22 0R2J-2-GP
C16 SC1U25V0KX-GP
C15 SC1U25V0KX-GP
R374 0R2J-2-GP
R373 0R2J-2-GP
R23 0R3-U.
+DC2_PWR_SRC
+DC2_PWR_SRC_D
L67 BLM21PG300SN1-GP
L68 BLM21PG300SN1-GP
G20 GAP-CLOSE-PWR
G21 GAP-CLOSE-PWR
G22 GAP-CLOSE-PWR
G23 GAP-CLOSE-PWR
G24 GAP-CLOSE-PWR
G25 GAP-CLOSE-PWR
G26 GAP-CLOSE-PWR
C77 SC1K50V2KX-1GP
C69 SCD1U50V3KX-GP
C486 SC10U25V6KX-1GP
C471 SC10U25V6KX-1GP
Id=5A
Qg=8.7~13nC,
Rdson=23~30mohm
DELTA
DCR=18mohm
Irms=8A,Isat=14A
U18 FDS8880-NL-GP
U21 FDS8880-NL-GP
C473 SC10U25V6KX-1GP
C489 SC10U25V6KX-1GP
C71 SCD1U50V3KX-GP
C79 SC1K50V2KX-1GP
C784 SCD1U50V3KX-GP
DELTA
DCR=37mohm
Irms=5.5A,Isat=10A
Iomax=5A
OCP>10A
CHIP IND 3.3UH FMJ-0650I-3R3
U9
CLOSE TO PIN 10
GND
BYP
OUT1
FB1
ILIM1
POK1
EN1
UGATE1
PHASE1
LDOREFIN
LDO
VIN
VREF3
EN_LDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
POK2
EN2
UGATE2
PHASE2
BOOT1
LGATE1
PVCC
SECFB
GND
PGND
LGATE2
BOOT2
3V/5V_REFIN2
C20 SCD1U25V3KX-GP
R41 91KR3F-GP
6236_FB1
6236_ILIM1
3V/5V_POK
3V/5V_EN
6236_UGATE1
6236_PHASE1
C51 SCD1U25V3KX-GP
74.06236.A73
ISL6236IRZA-TR5281-GP
6236_BOOT1_1
R61 0R3-0-U-GP
6236_BOOT1
6236_LGATE1
6236_SECFB
6236_ILIM2
6236_SKIP#
6236_UGATE2
6236_PHASE2
R375 182KR3F-GP
R391 0R2J-2-GP
C52 SCD1U25V3KX-GP
6236_BOOT2_1
R62 0R3-0-U-GP
6236_BOOT2
6236_LGATE2
6236_OUT2
L57 IND-3D3UH-92-GP
U20 FDS6676AS-GP
R388 0R2-0.
R384 0R2J-2-GP
MAX8778_3/5V_AGND
Sanyo 330uF
6D3V, D Size
ESR=18mohm
ST330U6D3VDM-14GP
C517 SCD1U10V2KX-4GP
+3.3V_ALWP
+3.3V_ALW
G73 GAP-CLOSE-PWR
G74 GAP-CLOSE-PWR
G75 GAP-CLOSE-PWR
G76 GAP-CLOSE-PWR
G77 GAP-CLOSE-PWR
G78 GAP-CLOSE-PWR
G79 GAP-CLOSE-PWR
G80 GAP-CLOSE-PWR
Iomax=5A
OCP>10A
+5V_ALW
G81 GAP-CLOSE-PWR
G82 GAP-CLOSE-PWR
G83 GAP-CLOSE-PWR
G84 GAP-CLOSE-PWR
G85 GAP-CLOSE-PWR
G86 GAP-CLOSE-PWR
G87 GAP-CLOSE-PWR
G88 GAP-CLOSE-PWR
C5 ST220U6D3VDM-13GP
C518 SCD1U10V2KX-4GP
+5V_ALWP
R34 0R2J-2-GP
R33 0R2-0.
L58 IND-4D7UH-108-GP-U
CHIP IND 4.7UH YC0810T*4R7MS
Sanyo 220uF
6D3V, V Size
ESR=25mohm
U19 FDS6676AS-GP
Id=10A
Qg=9~13nC,
Rdson=12~15mohm
MAX8778_3/5V_AGND
C47 SC1U25V0KX-GP
G8 GAP-CLOSE
C441 SCD1U25V3KX-GP
CLOSE TO PIN 30
C797 SC1000P50V2JN-GP
6236_PHASE_E
R764 1D2R6J-GP
D22 BAT54SW-2-GP
D21 BAT54SW-2-GP
D24 BAT54-7-F-GP
5V_C_1
5V_C_2
10V_C
15V_C
C460 SCD1U25V2ZY-1GP
C459 SCD1U25V2ZY-1GP
C440 SCD1U25V2ZY-1GP
C439 SCD1U25V2ZY-1GP
+15V_ALWP
+15V_ALW
R377 24D9R3F-GP
R410 200KR2J-L1-GP
R411 39KR2J-GP
L=2.2uH
△I=(20-5)*5/(20*2.2u*0.4M)=4.2A
Ripple voltage=4.2A*25mOhm=105mV
Suggest ESR<=12mohm to reduce ripple vol.
If L change to 3.3uH
△I=(20-5)*5/(20*3.3u*0.4M)=2.8A
Ripple voltage=2.8A*15mOhm=42mV
Suggest ESR=15mohm to reduce ripple vol.
OCP:5x2=10A
L=2.2uH
Iocp=10-(4.2/2)~7.9A
Vth=7.9A*15mOhm=119mV
R(Ilim)=(119mV*10)/5uA
~238K--->R536
L=3.3uH
Iocp=10-(2.8/2)~6.6A
Vth=8.6A*15mOhm=129mV
R(Ilim)=(129mV*10)/5uA
~258K--->R536
35,51 ALWON
23 THERM_STP#
R43 1KR2J-1-GP
R8 0R2-0.
R7 200KR2J-L1-GP
3V/5V_EN
+3.3V_ALW
R36 100KR2J-1-GP
3V/5V_POK
R32 0R2-0.
ALW_PWRGD_3V_5V 35,51
G53 GAP-CLOSE-PWR
G56 GAP-CLOSE-PWR
SSID = PWR.Plane.Regulator_3V5V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC to DC 3.3V & 5V
Size Custom
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Parker
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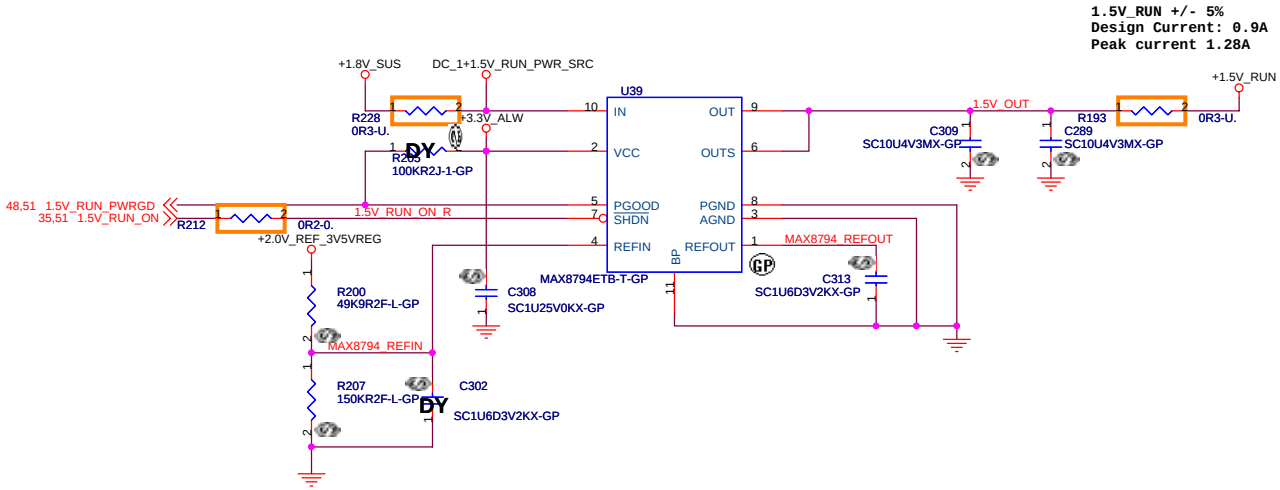
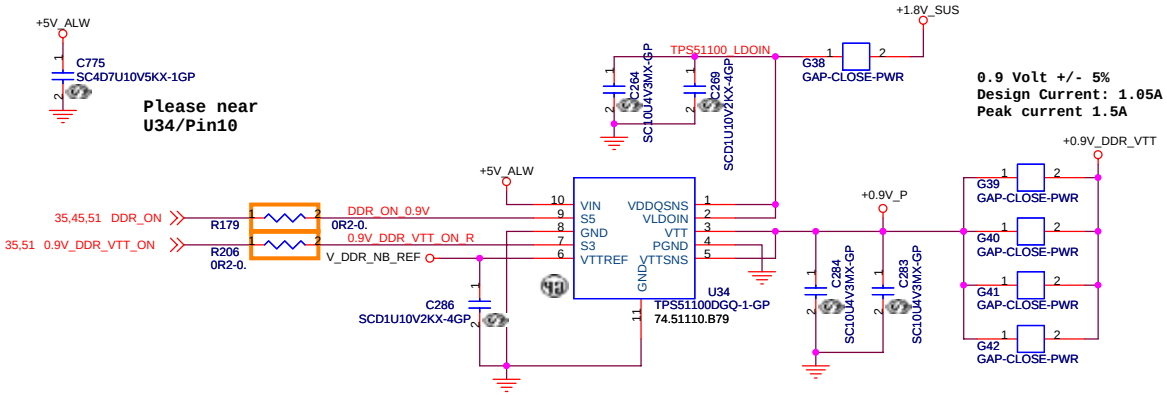
SSID = PWR.Plane.Regulator_1.5V



SSID = PWR.Plane.Regulator_0.9V



<Core Design>

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Title: DC to DC 1D5V / 0D9V

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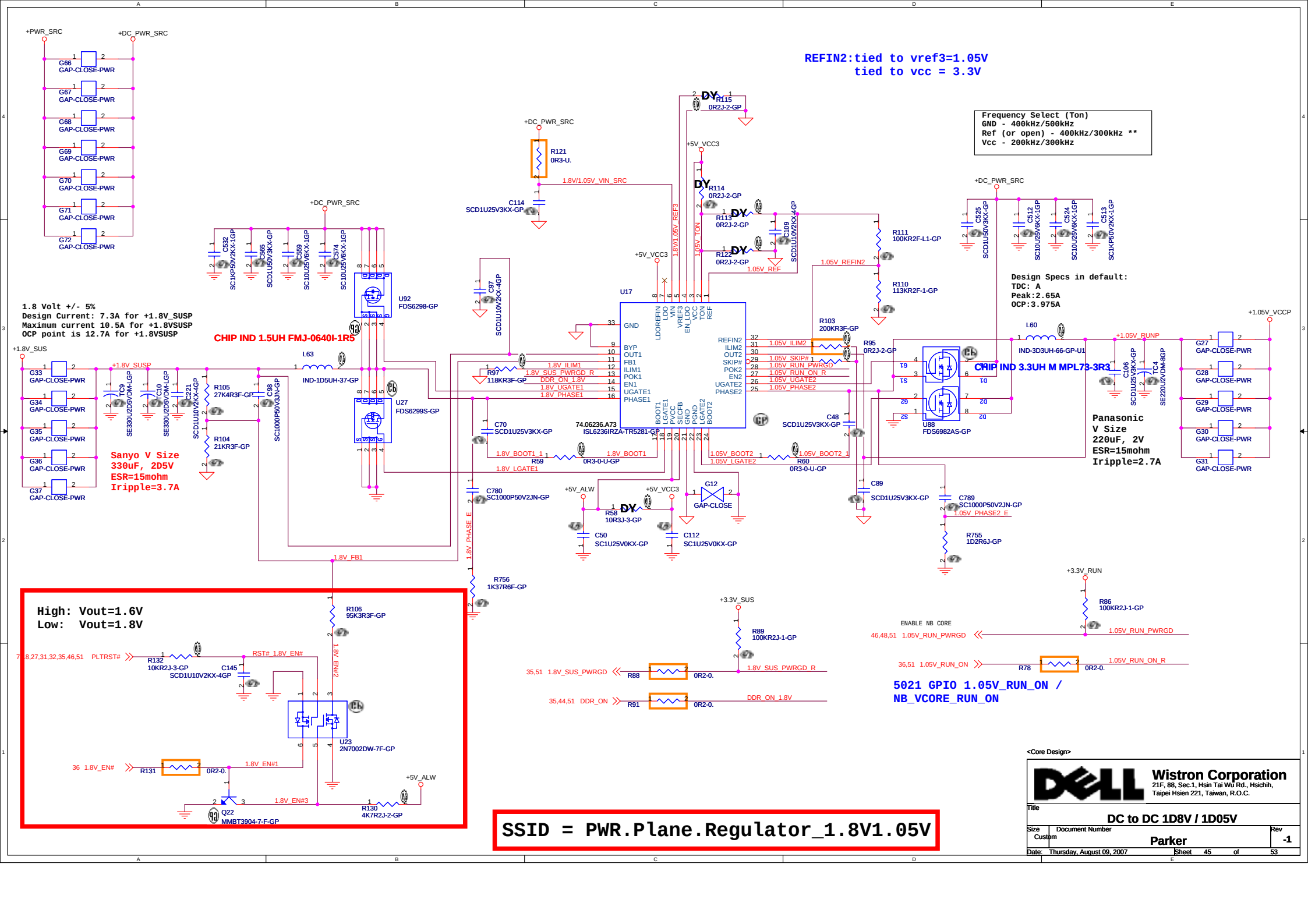
REFIN2:tied to vref3=1.05V
tied to vcc = 3.3V
Frequency Select (Ton)
GND - 400kHz/500kHz
Ref (or open) - 400kHz/300kHz **
Vcc - 200kHz/300kHz
1.8 Volt +/- 5%
Design Current: 7.3A for +1.8V_SUSP
Maximum current 10.5A for +1.8VSUSP
OCP point is 12.7A for +1.8VSUSP
CHIP IND 1.5UH FMJ-0640I-1R5
Sanyo V Size
330uF, 2D5V
ESR=15mohm
Iripple=3.7A
CHIP IND 3.3UH M MPL73-3R3
Panasonic
V Size
220uF, 2V
ESR=15mohm
Iripple=2.7A
Design Specs in default:
TDC: A
Peak:2.65A
OCP:3.975A
High: Vout=1.6V
Low: Vout=1.8V
5021 GPIO 1.05V_RUN_ON /
NB_VCORE_RUN_ON
SSID = PWR.Plane.Regulator_1.8V1.05V
Wistron Corporation
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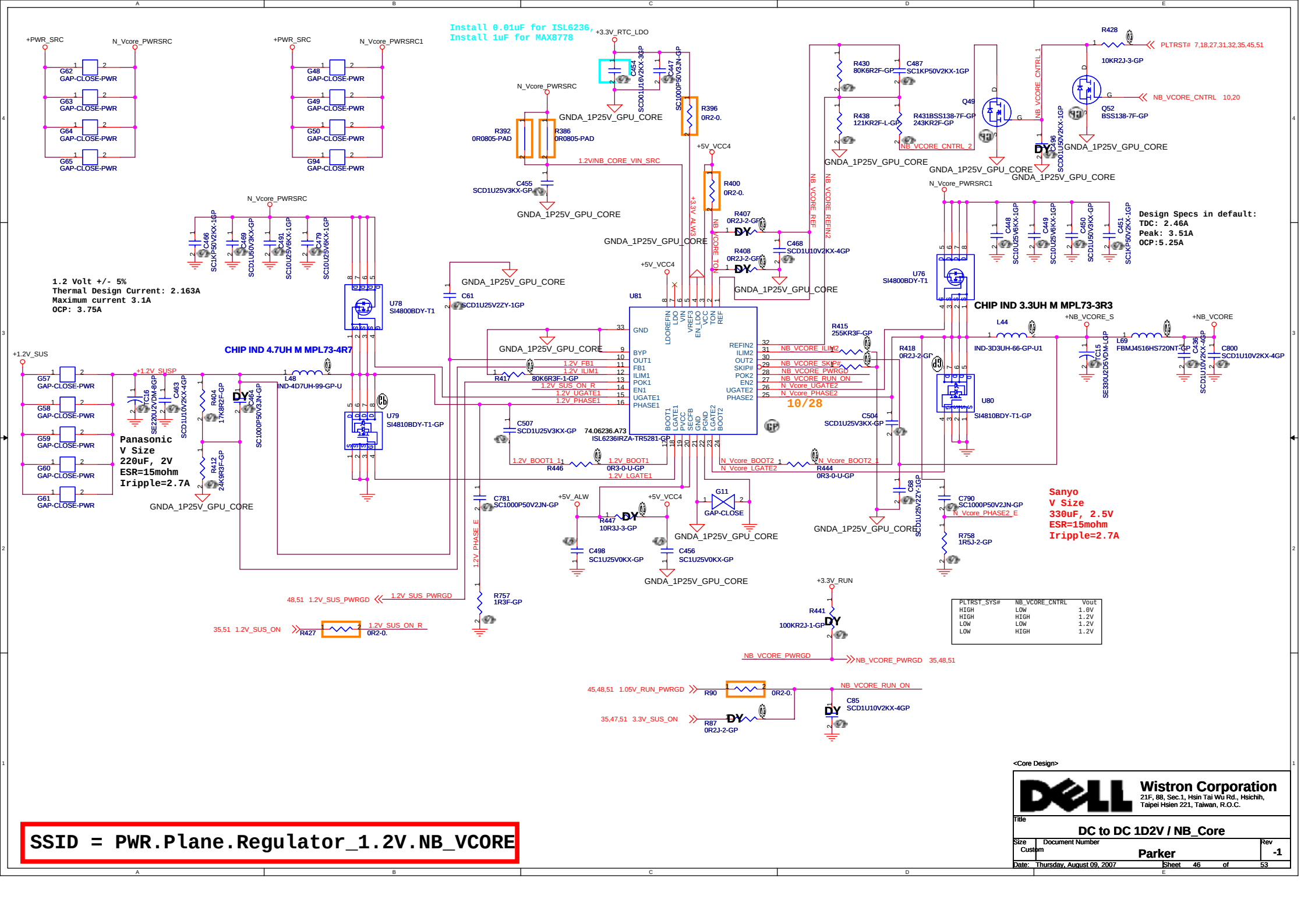
Taipei Hsien 221, Taiwan, R.O.C.
DC to DC 1D8V / 1D05V
Parker
Thursday, August 09, 2007


Install 0.01uF for ISL6236,
Install 1uF for MAX8778
1.2 Volt +/- 5%
Thermal Design Current: 2.163A
Maximum current 3.1A
OCP: 3.75A
CHIP IND 4.7UH M MPL73-4R7
CHIP IND 3.3UH M MPL73-3R3
Panasonic
V Size
220uF, 2V
ESR=15mohm
Iripple=2.7A
Sanyo
V Size
330uF, 2.5V
ESR=15mohm
Iripple=2.7A
Design Specs in default:
TDC: 2.46A
Peak: 3.51A
OCP:5.25A
10/28
PLTRST_SYS# NB_VCORE_CNTRL Vout
HIGH LOW 1.0V
HIGH HIGH 1.2V
LOW LOW 1.2V
LOW HIGH 1.2V
SSID = PWR.Plane.Regulator_1.2V.NB_VCORE
Wistron Corporation
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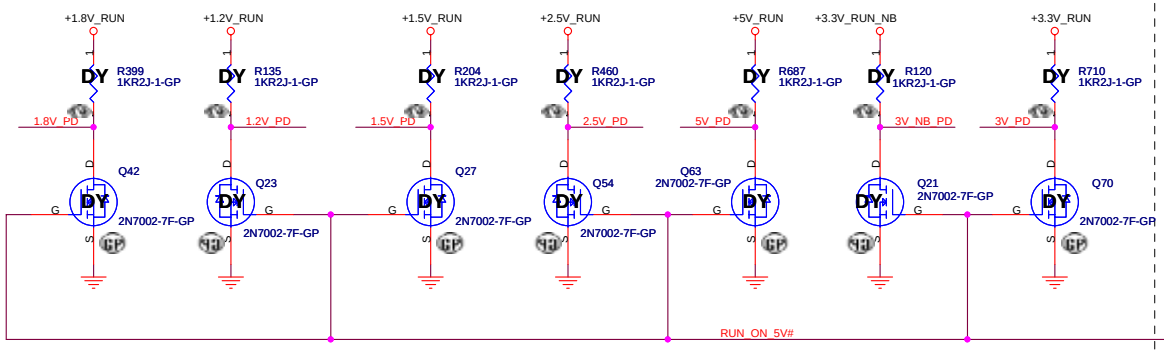
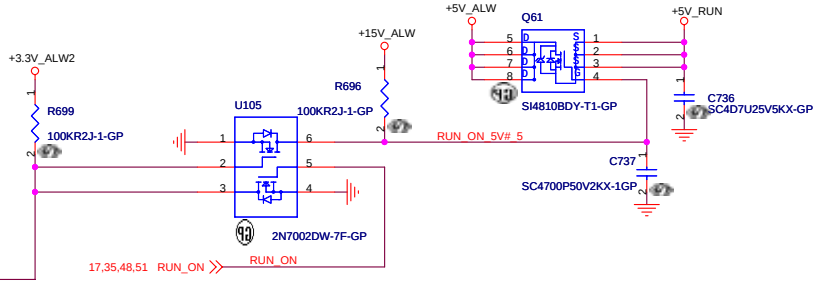
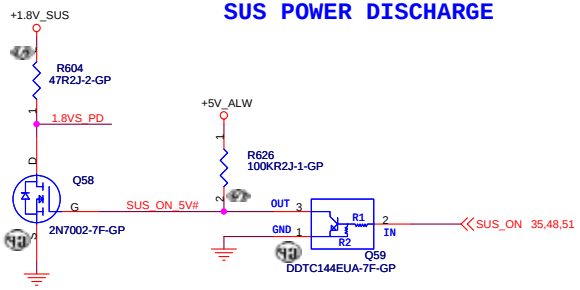
Taipei Hsien 221, Taiwan, R.O.C.
DC to DC 1D2V / NB_Core
Parker
Thursday, August 09, 2007

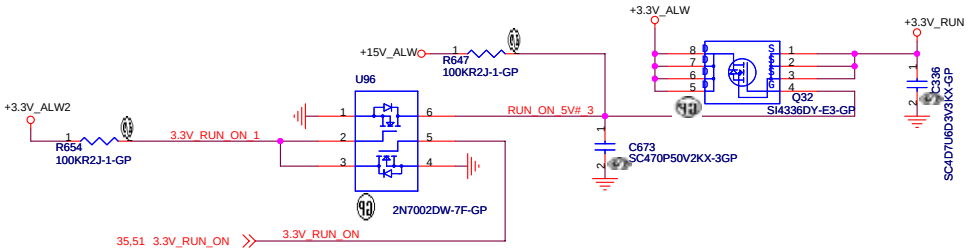
RUN POWER DISCHARGE



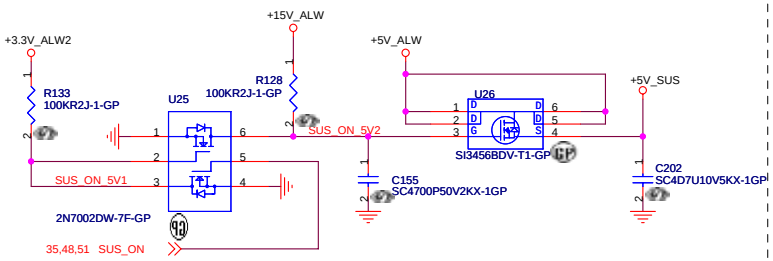


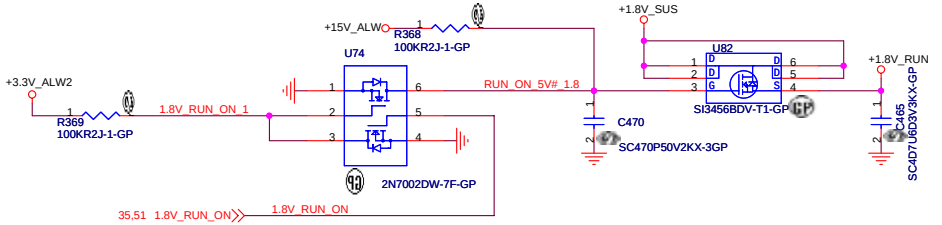
SUS POWER DISCHARGE



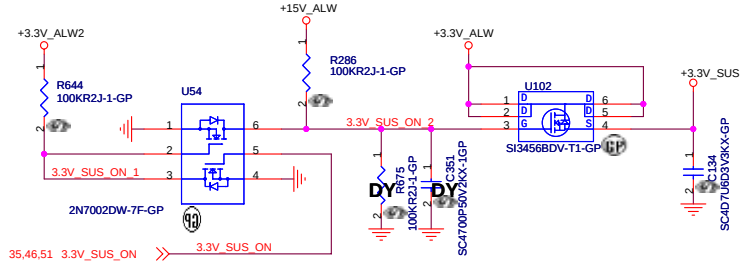


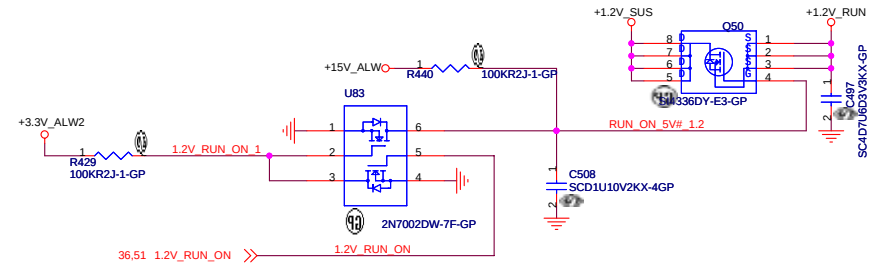
+5V_SUS POWER ENABLE





+3.3V_SUS POWER ENABLE





SSID = Reset.Suspend

<Variant Name>

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Title: POWER ENABLE

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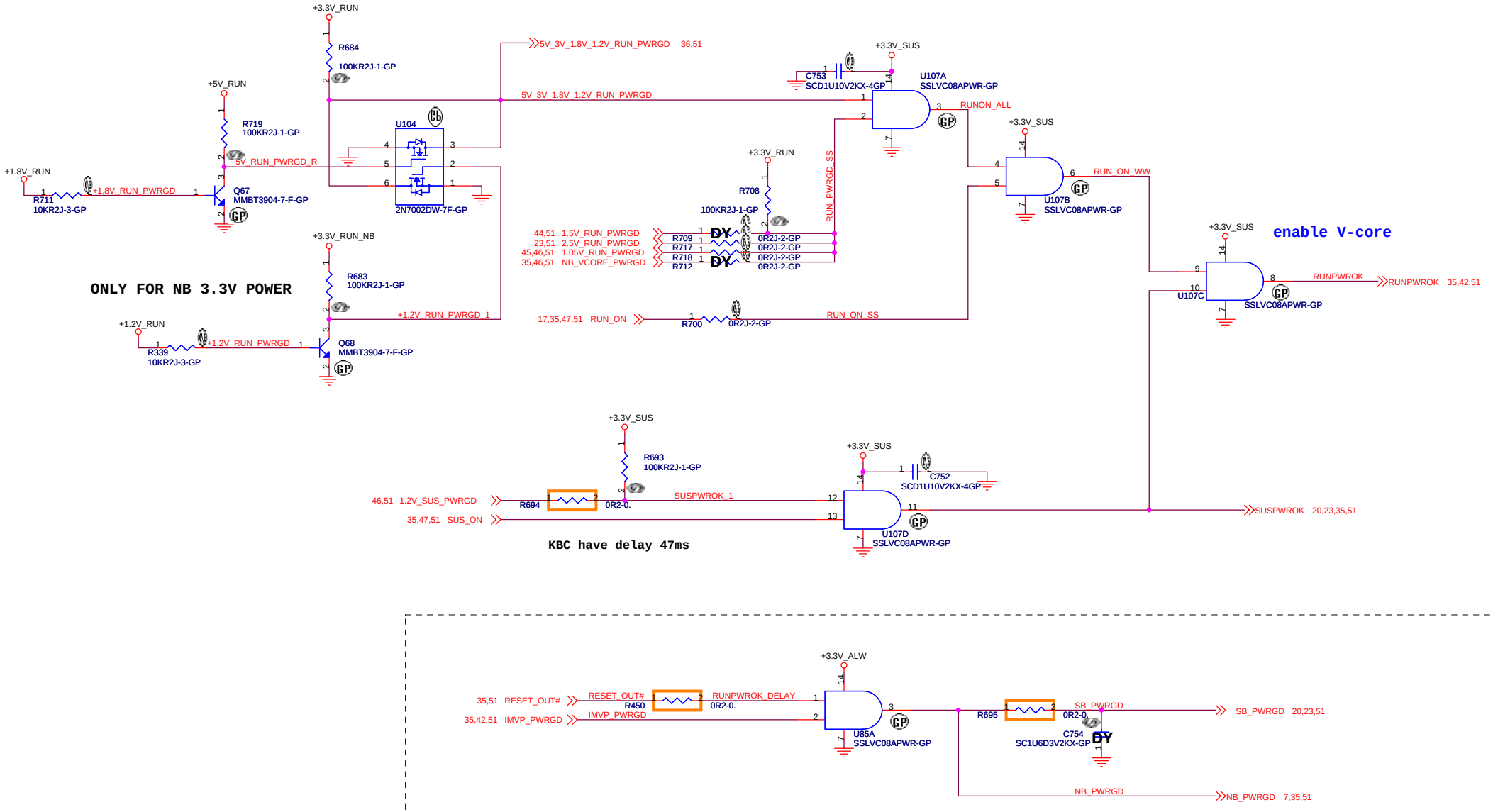

SSID = Reset.Suspend

<Variant Name>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON LOGIC***

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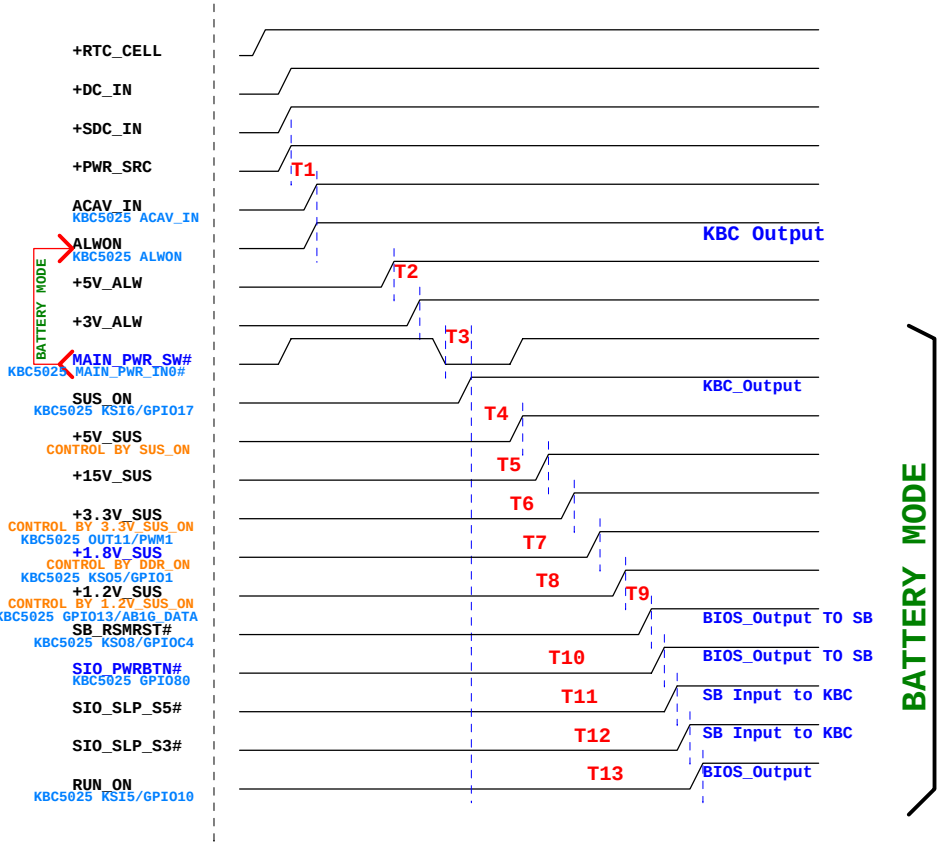
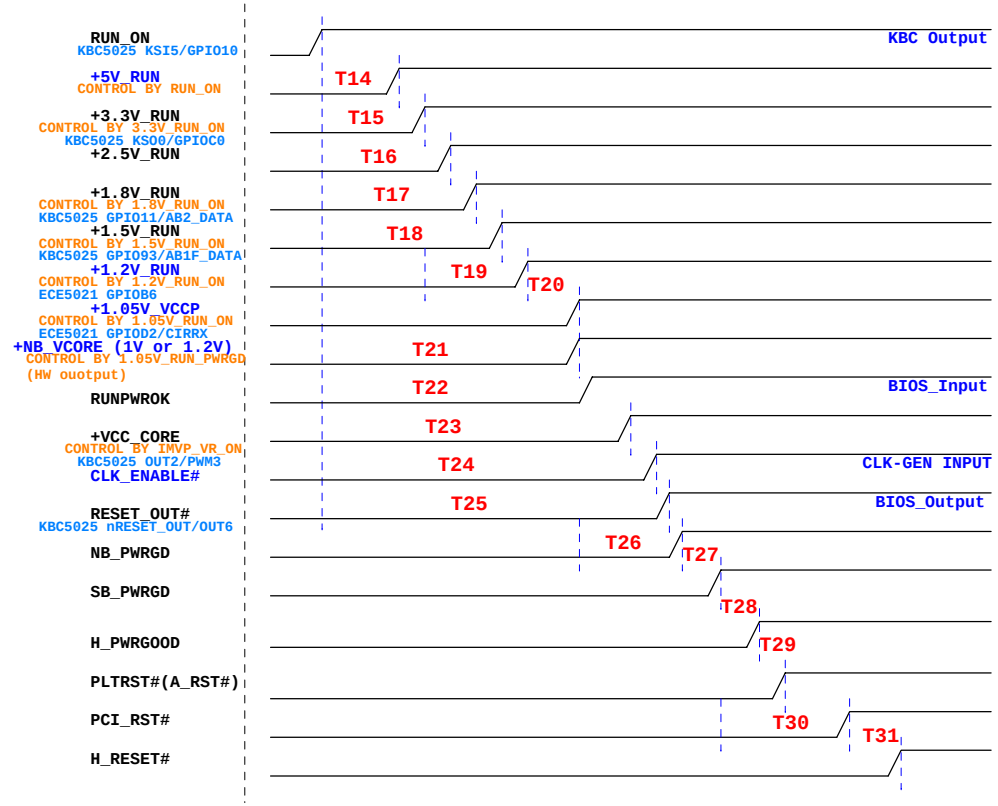
DP2 PLATFORMS POWER UP

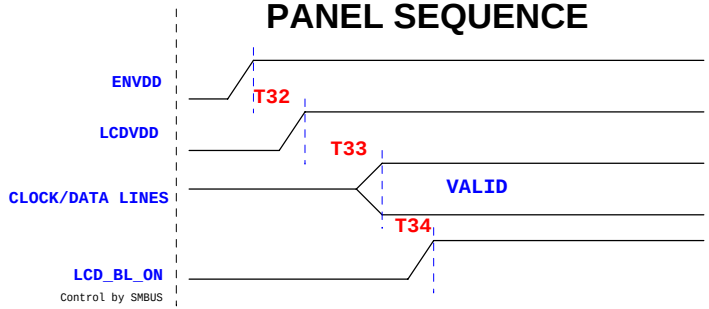
AC MODE



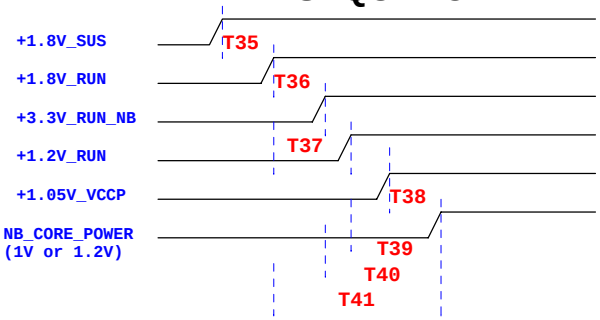
BATTERY MODE



PANEL SEQUENCE



NB SEQUENCE



<Variant Name>

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Title: POWER ON SEQUENCE

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Power

Signal Name	Test Position	Signal Name	Test Position
+DC_IN	U5.1;Page 39	GFX_PWR_SRC	U10.1;Page 17
+DC_IN_SS	U5.8;Page 39	+RTC_CELL	C266.1;Page 18
+SDC_IN	U12.8;Page 41	VCC_RUN_SB	L31.1;Page 18
+VCHGR	U48.8;Page 41	VCC_SB_PVDD	C315.1;Page 18
+PBATT	U37.1;Page 41	VCC_SB_VDDR	C245.1;Page 18
+SBATT	U38.8;Page 41	SB_AVDDCK1.2	C181.1;Page 21
+DOCK_PWR_SRC	U24.8;Page 38	+3.3V_RUN_HW	C275.1;Page 19
+PWR_SRC	U12.1;Page 41	+3.3V_SB_USB_TX	C156.1;Page 20
+VCC_CORE	TC2.1;Page 42	+3.3V_SB_USB_RX	C183.1;Page 20
+15V_ALW	R696.1;Page 47	+3.3V_SB_AVDDC	C135.1;Page 20
+5V_ALW	R413.1;Page 18	+SB_AVDDCK3.3	C182.1;Page 21
+3.3V_ALW	U11.1;Page 17	SB_5V_REF	C620.1;Page 21
+3.3V_ALW2	C14.2;Page 43	+2.5V_RUN	C552.1;Page 23
+1.5V_RUN	R193.2;Page 44	THERMAL_LDO_IN	C553.1;Page 23
+0.9V_DDR_VTT	C718.1;Page 15	+3.3V_PCI7402_AVDD	C348.1;Page 24
+1.8V_SUS	R170.1;Page 7	+3.3V_PCI7402	C364.1;Page 24
+1.05V_VCCP	C102.1;Page 11	+3.3V_PCI7402_VCCP	C656.1;Page 24
+1.2V_SUS	Q50.8;Page 47	+3.3V_PCI7402_VDDPLL33	C730.1;Page 24
+NB_VCORE	U26.6;Page 47	PCI7402_VR_PORT	C703.1;Page 24
+5V_SUS	U26.6;Page 47	+3.3V_RUN_CARD	C763.1;Page 26
+3.3V_SUS	U102.6;Page 47	+3.3V_LAN	U93.4;Page 27
+5V_RUN	Q61.1;Page 41	+2.5V_LOM	C62.1;Page 27
+3.3V_RUN	Q32.1;Page 47	+2.5V_BIASVDD	L51.1;Page 27
+1.8V_RUN	U82.6;Page 47	+2.5V_XTALVDD	L53.1;Page 27
+1.2V_RUN	Q50.1;Page 47	+2.5V_AVDD	L59.1;Page 27
CLK_VDDREF	C331.1;Page 4	+1.2V_LOM	C492.1;Page 27
CLK_VDD48	C330.1;Page 4	+1.2V_AVDDL	L55.2;Page 27
CLK_VDDA	C248.1;Page 4	+1.2V_GPHY_PLLVDD	L52.2;Page 27
+3.3V_RUN_CLK	C246.1;Page 4	+1.2V_PCIE_PLLVDD	L61.2;Page 27
V_CPU_GTLREF	R54.1;Page 5	+1.2V_PCIE_SDVDD	L16.2;Page 27
+1.05V_VCCP_NB_CPU_VREF	C43.1;Page 7	CODEC_DVDD_CORE	U31.1;Page 29
V_DDR_NB_REF	C616.1;Page 9	CODEC_DVDD_CORE_PIN40	U31.40;Page 29
+1.8V_RUN_NB_IOPLLVDD18	C168.1;Page 7	+5V_SPK_AMP	L50.2;Page 30
+1.2V_RUN_NB_IOPLLVDD12	C133.1;Page 7	+VDDA	C268.1;Page 30
+1.8V_RUN_NB_PLLVDD18	C35.1;Page 10	+3.3V_CARDSUS	C403.1;Page 31
+1.2V_RUN_NB_PLLVDD12	C55.1;Page 10	+1.5V_CARD	C765.1;Page 31
+1.2V_NB_VDDPLL_PCIE	C124.1;Page 10	+3.3V_CARD	C390.1;Page 31
+1.8V_RUN_NB_AVDDD	C88.1;Page 10	+3.3V_WLAN	U98.6;Page 32
+1.8V_RUN_NB_AVDDQ	C49.1;Page 10	+3.3V_RUN_HDD	U100.6;Page 33
+1.8V_RUN_NB_VDDLT18	C129.1;Page 10		
+1.8V_RUN_NB_LTP18VDD	C21.1;Page 10		
+3.3V_RUN_NB_AVDD	C65.1;Page 10		
+3.3V_RUN_NB_VDDR33	C66.1;Page 10		
+3.3V_RUN_NB_VDDLT33	C130.1;Page 10		
+3.3V_RUN_NB	U22.6;Page 10		
+1.8V_RUN_NB_VDD18CPU	C115.1;Page 11		
+1.8V_RUN_NB_VDD18MEN	C228.1;Page 11		
+1.2V_RUN_NB_VPCIE	C179.1;Page 11		
5V_CRT_S0	C426.1;Page 16		
LCDVDD	U11.4;Page 17		

Power Sequence

Signal Name	Test Position	Signal Name	Test Position
+RTC_CELL	C258/1 ; Page 18	+NB_VCORE	C150/1 ; Page 11
+DC_IN	U5/1 ; Page 41	RUNPWROK	U107/8 ; Page 48
+SDC_IN	U12/8 ; Page 41	+VCC_CORE	TC2/1 ; Page 42
+PWR_SRC	U12/1 ; Page 41	CLK_ENABLE#	R572/1 ; Page 4
ACAV_IN	R329/2 ; Page 40	RESET_OUT#	U30/53 ; Page 35
ALWON	R43/1 ; Page 43	NB_PWRGD	R695/1 ; Page 48
+3.3V_ALW	C314/1 ; Page 35	SB_PWRGD	R695/2 ; Page 48
+5V_ALW	Q61/5 ; Page 47	H_PWRGOOD	R568/2 ; Page 5
MAIN_PWR_SW#	R511/2 ; Page 17	PLTRST#	R664/1 ; Page 18
SUS_ON	U30/34 ; Page 35	PCI_RST#	R621/2 ; Page 18
+5V_SUS	U26/4 ; Page 47	H_RESET#	R512/2 ; Page 5
+15V_ALWP	R377/1 ; Page 43	ENVDD	D4/2 ; Page 17
+3.3V_SUS	RN50/3 ; Page 35	LCDVDD	U11/4 ; Page 17
+1.8V_SUS	U82/1 ; Page 47		
+1.2V_SUS	Q50/8 ; Page 47		
SB_RSMRST#	U30/23 ; Page 35		
SIO_PWRBTN#	U30/109 ; Page 35		
SIO_SLP_S5#	U30/31 ; Page 35		
SIO_SLP_S3#	U30/30 ; Page 35		
RUN_ON	U30/35 ; Page 35		
+5V_RUN	Q61/1 ; Page 47		
+3.3V_RUN	Q32/1 ; Page 47		
+2.5V_RUN	R460/1 ; Page 47		
+1.8V_RUN	U82/4 ; Page 47		
+1.5V_RUN	R193/2 ; Page 44		
+1.2V_RUN	Q50/1 ; Page 47		
+1.05V_VCCP	R108/2 ; Page 7		

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON TIMING

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SSID=EMI

SPR2 SPRING-24-GP 34.45T31.001
SPR1 SPRING-24-GP 34.45T31.001
SPR6 SPRING-24-GP 34.45T31.001
SPR4 SPRING-24-GP 34.45T31.001
SPR3 SPRING-24-GP 34.45T31.001
SPR5 SPRING-24-GP 34.45T31.001
SPR8 SPRING-48-GP 34.43G01.002
SPR7 SPRING-48-GP 34.43G01.002
SW3 SPRING-17 34.45V09.001
SW2 SPRING-17 34.45V09.001
SW4 SPRING-17 34.45V09.001

SSID=Mechanical

H5 HOLE ZZ.0HOLE.XXX
H7 HOLE ZZ.0HOLE.XXX
H11 HOLE ZZ.0HOLE.XXX
H3 HOLE ZZ.0HOLE.XXX
H14 HOLE ZZ.0HOLE.XXX
H16 HOLE ZZ.0HOLE.XXX
H8 HOLE ZZ.0HOLE.XXX
H7,BOSS 34.4S701.001
H1 HOLE ZZ.0HOLE.XXX
H18 HOLE ZZ.0HOLE.XXX
H12 HOLE ZZ.0HOLE.XXX
H17 HOLE ZZ.0HOLE.XXX
H2 HOLE ZZ.0HOLE.XXX
H19 HOLE ZZ.0HOLE.XXX

CLK-GEN Shading BOX

H13 ACES-CON5-7-GP-U
H6 HOLE ZZ.0HOLE.XXX
H15 HOLE ZZ.0HOLE.XXX

CLK-GEN Shading-Lock
34.4S712.001
34.4S713.001

LAN Shading BOX

H20 MLX-CON2-7-GP
H10 HOLE ZZ.0HOLE.XXX
H9 HOLE ZZ.0HOLE.XXX

LAN Shading-Lock
34.4S710.001
34.4S711.001

35,43	ALWON	ALWON	TP29 TPAD28
17,35	MAIN_PWR_SW#	MAIN_PWR_SW#	TP120 TPAD28
35,43	ALW_PWRGD_3V_5V	ALW_PWRGD_3V_5V	TP17 TPAD28
35,47,48	SUS_ON	SUS_ON	TP99 TPAD28
35,46,47	3.3V_SUS_ON	3.3V_SUS_ON	TP80 TPAD28
35,44,45	DDR_ON	DDR_ON	TP129 TPAD28
35,45	1.8V_SUS_PWRGD	1.8V_SUS_PWRGD	TP8 TPAD28
35,46	1.2V_SUS_ON	1.2V_SUS_ON	TP110 TPAD28
46,48	1.2V_SUS_PWRGD	1.2V_SUS_PWRGD	TP186 TPAD28
20,23,35,48	SUSPWROK	SUSPWROK	TP191 TPAD28
20,35	SB_RSMRST#	SB_RSMRST#	TP139 TPAD28
20,35	SIO_PWRBTN#	SIO_PWRBTN#	TP119 TPAD28
20,35	SIO_SLP_S5#	SIO_SLP_S5#	TP16 TPAD28
20,35	SIO_SLP_S3#	SIO_SLP_S3#	TP14 TPAD28
17,35,47,48	RUN_ON	RUN_ON	TP190 TPAD28
35,47	3.3V_RUN_ON	3.3V_RUN_ON	TP177 TPAD28
23,48	2.5V_RUN_PWRGD	2.5V_RUN_PWRGD	TP98 TPAD28
35,47	1.8V_RUN_ON	1.8V_RUN_ON	TP175 TPAD28
35,44	0.9V_DDR_VTT_ON	0.9V_DDR_VTT_ON	TP56 TPAD28
35,44	1.5V_RUN_ON	1.5V_RUN_ON	TP150 TPAD28
44,48	1.5V_RUN_PWRGD	1.5V_RUN_PWRGD	TP192 TPAD28

36,47	1.2V_RUN_ON	1.2V_RUN_ON	TP111 TPAD28
36,48	5V_3V_1.8V_1.2V_RUN_PWRGD	5V_3V_1.8V_1.2V_RUN_PWRGD	TP97 TPAD28
36,45	1.05V_RUN_ON	1.05V_RUN_ON	TP6 TPAD28
45,46,48	1.05V_RUN_PWRGD	1.05V_RUN_PWRGD	TP194 TPAD28
35,46,48	NB_VCORE_PWRGD	NB_VCORE_PWRGD	TP193 TPAD28
35,42,48	RUNPWROK	RUNPWROK	TP189 TPAD28
35,42	IMVP_VR_ON	IMVP_VR_ON	TP149 TPAD28
4,42	CLK_ENABLE#	CLK_ENABLE#	TP160 TPAD28
35,42,48	IMVP_PWRGD	IMVP_PWRGD	TP118 TPAD28
35,48	RESET_OUT#	RESET_OUT#	TP144 TPAD28
7,35,48	NB_PWRGD	NB_PWRGD	TP187 TPAD28
20,23,48	SB_PWRGD	SB_PWRGD	TP188 TPAD28
5,18	H_PWRGOOD	H_PWRGOOD	TP169 TPAD28
7,18,27,31,32,35,45,46	PLTRST#	PLTRST#	TP185 TPAD28
18,25	PCI_RST#	PCI_RST#	TP5 TPAD28
3,5,7	H_RESET#	H_RESET#	TP12 TPAD28
5,7	H_ADS#	H_ADS#	TP13 TPAD28

<Variant Name>

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Title: EMI/HOLE

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/11/03	X00	1	18	REMOVE DVI CHIP TO MEDIA SLICE SIDE	Change SPEC	EE
		2	3	Dummy ITP1		EE
		3	4	Add R616,R617, Dummy R607,R610	Ext Clock Frequency select to 133MHz	EE , SW
		4	4	Change R221,R595 to 15 ohm , RN14 to 22 ohm	EA report fail issues	EE
		5	8	Change PCI-E GPP_TX	PCI-E GPP error	EE
		6	10	Add R742 10K ohm in NB_TMDS_HPD_R	BIT issues	EE
		7	11	Change +1.8V_RUN_NB_VDD18MEN TO +1.8V_RUN_NB_VDD18MEM	BIT issues	EE
		8	12	Change R629,R630,R632,R633 to 0 ohm and Add R736,R737 100 ohm	DDR clock driver issues	EE
		9	13	Change Onboard memory to Hynix and Mircon	Sansung memory can't support issues	EE
		10	16	Change L37, L38, L39, L40, L41 to BLM18BA100SN1D	EA report fail issues	EE
		11	17	Change R47 to 150 ohm	EA report fail issues	EE
		12	17	Change LVDS1 Power circuit	LCD Power issues	EE
		13	19	Add R738,R739,R740 0 ohm connect SATA power and GND	No support SATA HDD issues	EE
		14	19	Add C776 22pF De-pop and Change R445,R514,R529 to 47 ohm	SPI ROM issues	RF
		15	20	Change Memory SMBus support to SB SMBus 0 and Del U101,RN58	Memory controller issues	SW
		16	20	Del L23 and Change AVDDRX power to +3.3V_SB_USB_TX	ATI Desgin check issues	EE
		17	25	Change signal IRQ_SERIRQ to U63/Pin H1;Change U63/Pin H2 to signal MFUNC2	TI multi function setting issues	EE , SW
		18	25	Change C385,C386 to 12PF	Crytal result issues	EE
		19	26	Change R260,R265,R294,R305 to 200 ohm , R291 to 75 ohm	SDIO Rise time fall issues	EE
		20	27	Change C510 to 33PF	Crytal result issues	EE
		21	27	Change R420 to 1.18K ohm	LOM Driver issues	EE
		22	29	Change U31/Pin 4 AUD_SPK_DET signal to U35/Pin P8	Audio detect issues	SW
		23	30	Change U32 to TI TPA6040A4 and setting	AMP Main source change issues	EE
		24	30	Change U40/Pin 5 Power to +3.3V_RUN	BIT issues	EE
2007/03/21	X01	25	30	Change C446, C453 to 1uF 25V 0603	Audio issues	EE
		26	32	Swap ESD1 and De-pop C369, C377	WWAN's SIM error	EE
		27	32	Change U98 to Vishay SI3424DV	WLAN Power issues	Power
		28	33	Change R548,R573 to 0 ohm , R575 to 47 ohm and Add C772,C773, C774 22pF De-pop	SPI ROM issues	EE
		29	35	Dummy DBG1, DBG2		EE
		30	35	Change R641 to 1M ohm	BIT issues	EE
		31	35	Change RN54,RN61,RN65,RN78 to 2.2K ohm	SUS and RUN power open two time issues	EE , SW
		32	35	Change C173 to 12PF ,C200 to 15PF	Crytal result issues	EE
		33	35	De-pop R321	BIT issues	EE
		34	35	Add R749 10K ohm to +RTL_CELL	Pen switch issues	EE , SW
		35	36	Add R269 10K ohm, Dummy R270	Board ID issues	EE , SW
		36	36	Add MEM_VEND_I Detect in U64 Pin 1	Memory controller for SPD issues	SW
		37	36	Change U64 Pin 7 signal connect GND	BIT issues	EE
		38	36	Add PEN_SW# connector to U64/Pin 119	Pen switch issues	EE , SW
		39	37	Change KB1 signal	Keyboard issues	EE , KBC
		40	37	Change LID_CL_SIO#_R to U40/Pin 2 , TABLET_DET# to HSW1/Pin 4	Hall switch support change issues	ME
		41	38	Change U85 power source to +3.3V_ALW	BIT issues	EE
		42	38	Add DOCKED signal use U85 to LOM and Change U86/Pin E3 signal to LOM_E_SWITCH	LOM Docking switch issues	EE
		43	40	Add 1K8 ohm 1206 De-pop in +VCHGR to GND	BIT issues	EE
		44	43	Change TC5 to 220U6D3V	BIT issues	EE
		45	44	Add C775 near U34/Pin 10	BIT issues	EE
		46	45	Change L63 to IND-1D5UH , TC9,TC10 to SE330U2D5VVD , R97 to 118K , R103 to 93.1K	Power issues	Power
		47	46	Change R417 to 80.6K ohm , R415 to 255K ohm , TC15 to 330U2D5V	Power issues	Power
		48	48	Change R695 to 0 ohm , Del R666, C730	Power sequence issues	Power
		49		Change Power use Gap to Clise Gap		Power

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	4	Del C570,582,585,592,595,604,606,609,611,622	RF noise issues	RF
		2	4	Change C615,623,635 to 15pF	RF noise issues	RF
		3	11	Change C116,147,176 to 6pF, C72,231,240 to 0.1uF and ADD C801 22uF	RF noise issues	RF
		4	13	Add C802,803,804 to 4.7uF	+1.8_SUS, +0.9V_DDR_VTT, V_DDR_NB_REF ripple issues	EE
		5	17	Change C563 to Dummy	Power switch issues	EE
		6	17	Add R752 10K ohm	Cable detect setting issues	SW
		7	17	Change LCD Lunch Board Power support	Digitizer Power support	EE
		8	17	Change R98,101,701 to 470 ohm	Battery life issues	EE
		9	18	Add R753 10K ohm	Cable detect setting issues	SW
		10	19	Change Net LBF_ID0 to MEM_VEND_ID1	Onboard memory vendor support issues	EE,SW
		11	20	Change R478,479 to 10 ohm, C533,535 to 4.7pF	EMI issues	EMI
		12	22	Add SB power delay circuit	ATI power issues	EE
		13	25	Change R631 to 22 ohm, R636 to 10 ohm, C654 to 10pF and C667 to 4.7pF	EMI issues	EMI
		14	27	Add R485 0 ohm	Cable detect setting issues	SW
		15	27	Change R462 to 22 ohm and C527 to 4.7pF	EMI issues	EMI
		16	28	Change R383 to 0 ohm and L45 to Dummy	EMI issues	EMI
		17	30	Add R754 10K ohm	Cable detect setting issues	SW
		18	31	Change R308,309 to 470 ohm	Battery life issues	EE
		19	32	Add +1.5V_RUN_WLAN switching circuit	Power switch issues	EE
		20	33	Change R18,19 and C9 to Dummy	Pen detect setting issues	SW
		21	34	Add C793,794,795,796 EMI Capacitor Pad and D15,23,26 EMI Diode	EMI issues	EMI
		22	35	Add R762 0 ohm	RF noise issues	RF
		23	35	Change Net AC_OFF ti pull down	AC_OFF setting issues	EE,SW
		24	35	Change R223 to 22 ohm and C321 to 10pF	EMI issues	EMI
2007/06/25	X02	25	36	Change Board ID to X02	Board ID setting issues	SW
		26	36	Add R763 0 ohm	RF noise issues	RF
		27	37	Change R302,303 and 304 to 470 ohm	Battery life issues	EE
		28	37	Change R682 to 0 ohm	Cable detect setting issues	SW
		29	38	Add C779,782 and 786 0.1uF	RF noise issues	RF
		30	39	Add C511,785 and 787 0.1uF	RF noise issues	RF
		31	40	Change L66 part to SIL104R	Charge issues	POWER
		32	40	Add C788 to 0.1uF	RF noise issues	RF
		33	40	Add ACAV_IN detect circuit	ACAV_IN setting issues	SW
		34	42	Change C297 to 390pF, R203 to 24.3K ohm, R192 to 442K ohm, R175 to 237K ohm and C233 to 33pF	CPU power issues	POWER
		35	42	Add C777,791 0.1uF, C22,379,778,792 2200pF and R25 1 ohm	RF noise issues	RF
		36	43	Change C77,79 to 1000pF and Add C784 0.1uF	RF noise issues	RF
		37	43	Add L67,68 30 ohm Bead	RF noise issues	RF
		38	45	Change C513,532 to 1000pF and Add C780,789 1000pF, R755,756 1.2 ohm	RF noise issues	RF RF
		39	46	Add L69 60 ohm	RF noise issues	RF
		40	46	Change C451,466 to 1000pF and Add C781,790 1000pF, R757,758 1 ohm	RF noise issues	RF
		41				
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Title: *HISTORY2*

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