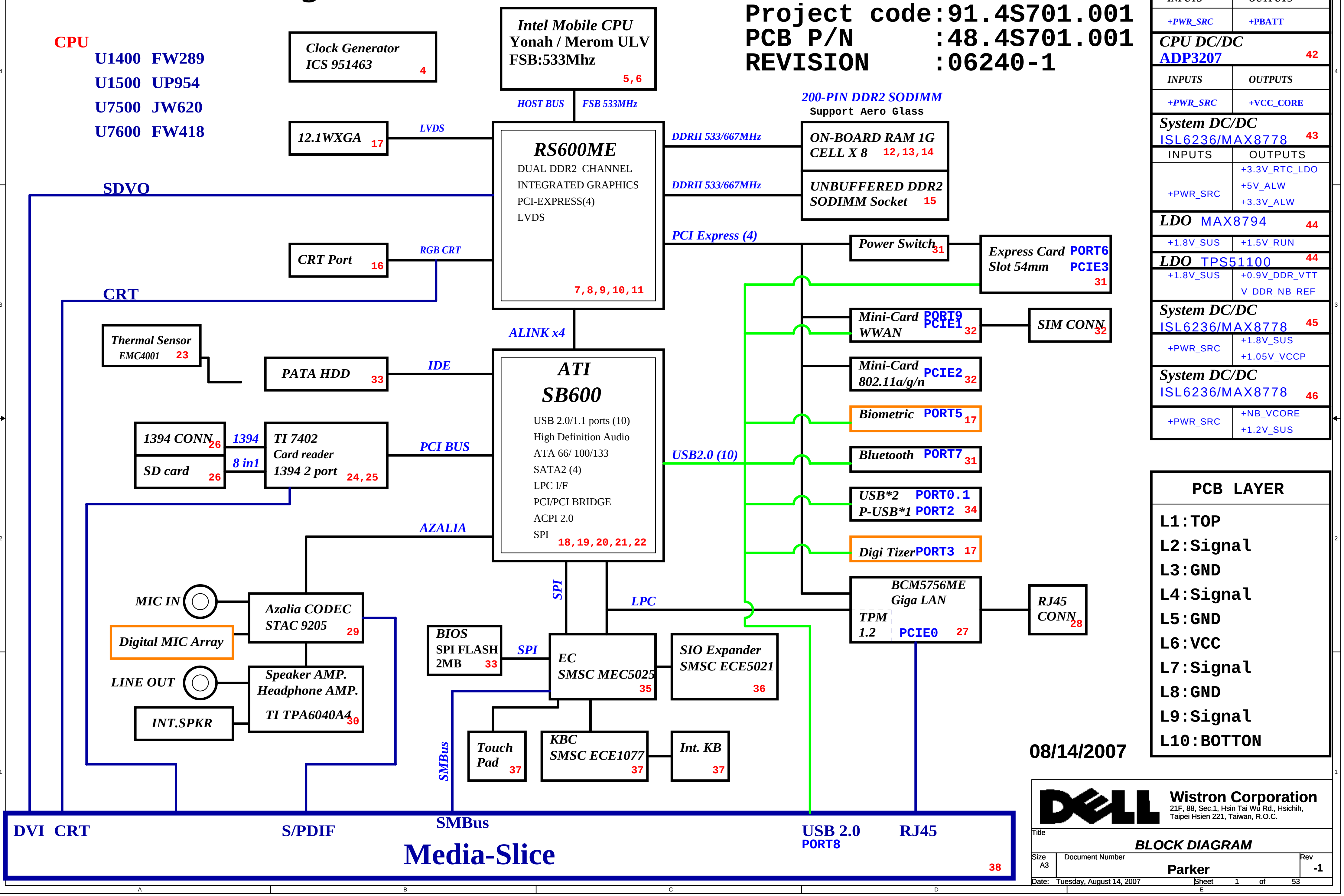
Parker Block Diagram



CLK-GEN ICS951463

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CLKREQA# B# C# MAP

CLKREQA#	CLKSRC 7 NB ALINK
	CLKSRC 5 EXPRESS CARD
	CLKSRC 6 SB ALINK
CLKREQB#	CLKSRC 2 WLAN
	CLKSRC 4 LOM
CLKREQC#	CLKSRC 0 WWAN
	ATIGCLK 1 NB-PCIEX16
	ATIGCLK 2 NO -USED

ATI NB-RS600ME STRAP PIN

Strap name	LOW 0	HIGH 1
NB_VSYNC (DAC_VSYNC: STRAP_MOBILE_GFX)	DESKTOP GRAPHICS DEVICE	MOBILE GRAPHICS DEVICE ★
NB_HSYNC (DAC_HSYNC: STRP_INTGFX_DISABLE)	ENABLE ★	DISABLE
NB_SDVO_CTRLDATA (DDC_DATA: STRAP_MEMVMODE)	DDR3	DDR2 ★
STRP_DATA (STRP_DATA: STRP_MEMSTRAPS)	SELECT MEMORY CHA A AS DEBUG BUS	NORMAL MODE ★

SR600ME PCIE route

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD

ATI SB-SB600 STRAP PIN

Strap name		LOW 0	HIGH 1
AC_SDOUT	SB_AC_SDOUT	IGNORE DEBUG STRAPS ★	DEBUG STRAPS Default
RTC_CLK	SB_RTCCLK	EXTERNAL RTC	INTERNAL RTC ★ Default
PCI_CLK4	CLK_SB_PCI4	EXTERNAL 48MHZ ★ Default	INTERNAL PLL48
PCI_CLK6	CLK_SB_PCI6	INTEL CPU ★ Default	AMD CPU

PCI_CLK0 CLK_SB_PCI0	PCI_CLK1 CLK_SB_PCI1	ROM TYPE
0	0	FWH
0	1	LPC Default
1	0	SPI
1	1	PCI

USB TABLE

USB0	Ext Side 1
USB1	Ext Side 2
USB2	POWER USB
USB3	Digi Tizer
USB4	
USB5	Biometric
USB6	Express Card
USB7	BLUETOOTH
USB8	Media Slice
USB9	MiniCard WWAN

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MEDIACARD	AD17	G H	1	1

PCI-CLK route

PCICLK 2	MEC5025
PCICLK 5	BCM5756ME
PCICLK 6	TI7402

TABLE OF CONTENTS

SMBUS TABLE

SMBUS TABLE

SOURCE	SIGNAL NAME	LINKED DEVICES
RS600ME	I2C_CLK/DAC_SDA	CRT/SLICE CRT
	I2C_CLK/I2C_DATA	LVDS
	I2C_CLK/DDC_SDA	DVI
SB600	SCL1/SDA1	LAN / WLAN / WWAN / EXPRESS CARD/SO-DIMM
MEC5025	AB1A_CLK/AB1A_DATA	SLICE CONN.
	AB1B_CLK/AB1B_DATA	INVERTER / LIGHT SENSOR
	AB1C_CLK/AB1C_DATA	BATTERY CONN.
	AB1D_CLK/AB1D_DATA	BATTERY-SLICE CONN.
	AB1E_CLK/AB1E_DATA	P-USB / CHARGER / THERMAL
	AB1H_CLK/AB1H_DATA	CLK-GEN
	IMCLK/IMDAA	TOUCH PAD

EMC4001 Thermal sensor mapping

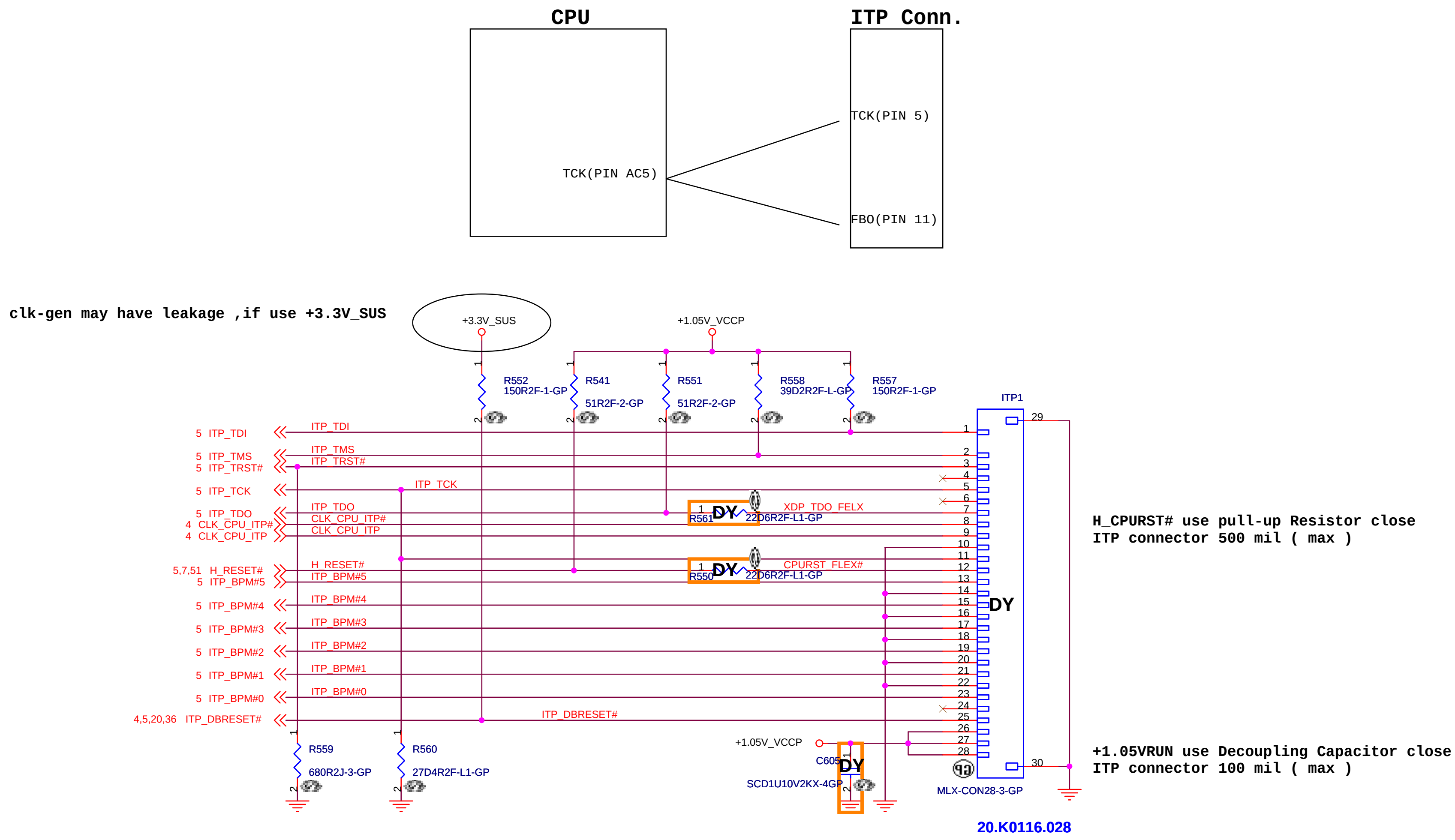
D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Table Contsnt		
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 2 of 53	

SSID = CPU

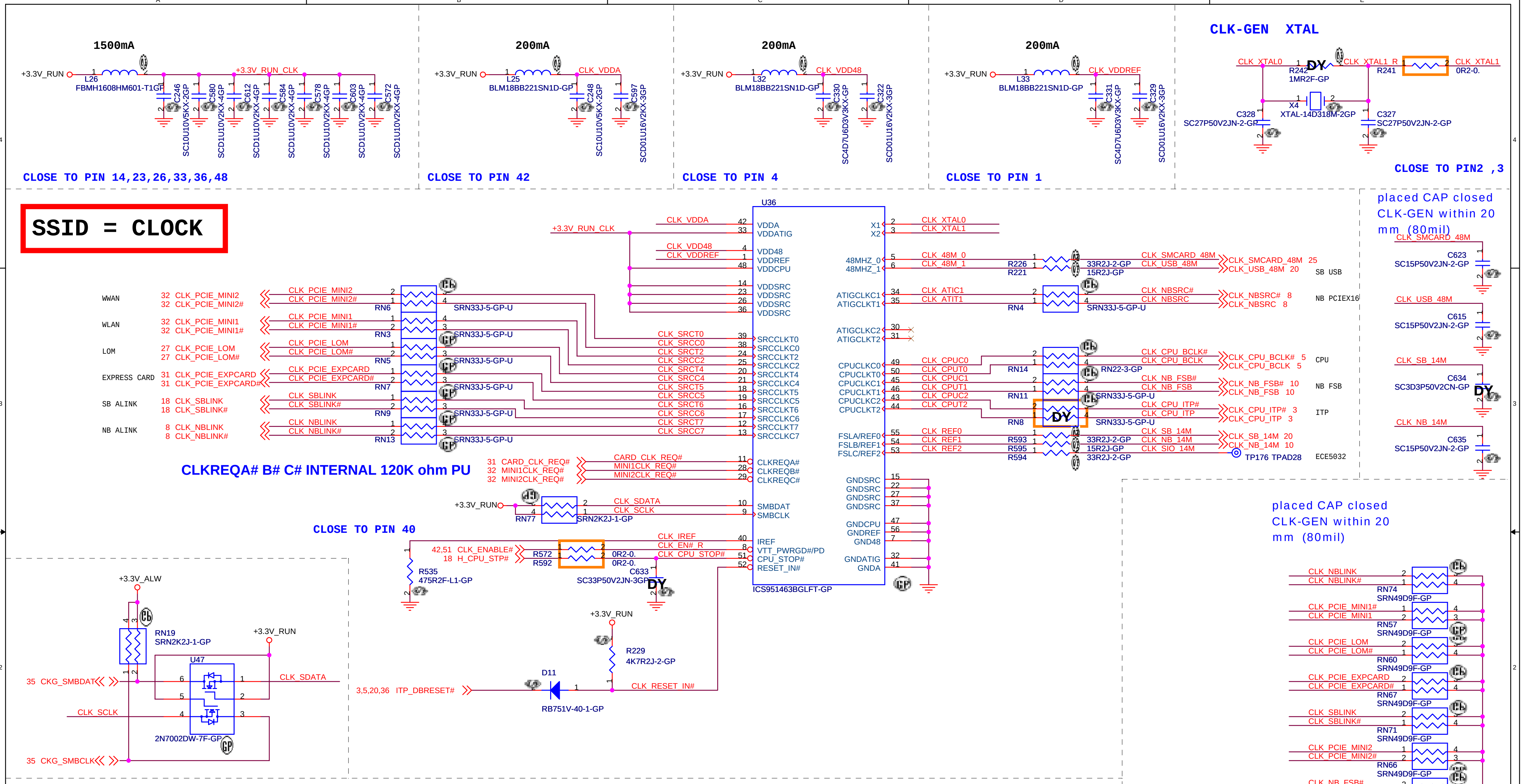


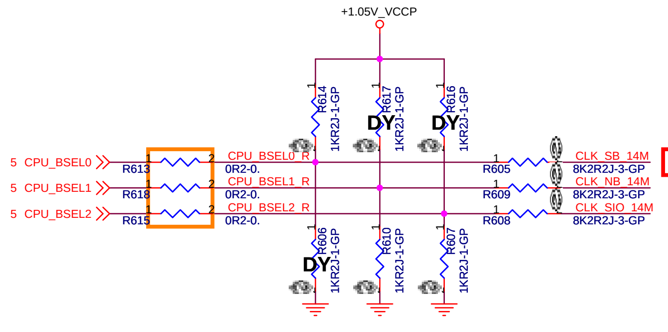
ITP Debug Conn.

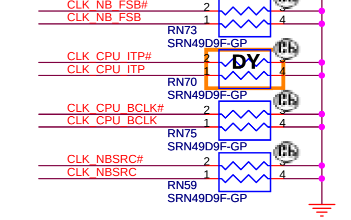
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ITP Debug	
Size A3	Document Number: Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 3 of 53	







EXT CLK FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

CLKREQA# B# C# MAP

CLKREQA#	CLKSRC 7 NB ALINK CLKSRC 5 EXPRESS CARD CLKSRC 6 SB ALINK
CLKREQB#	CLKSRC 2 WLAN CLKSRC 4 LOM
CLKREQC#	CLKSRC 0 WWAN ATIGCLK 1 NB-PCIEX16 ATIGCLK 2 NO -USED

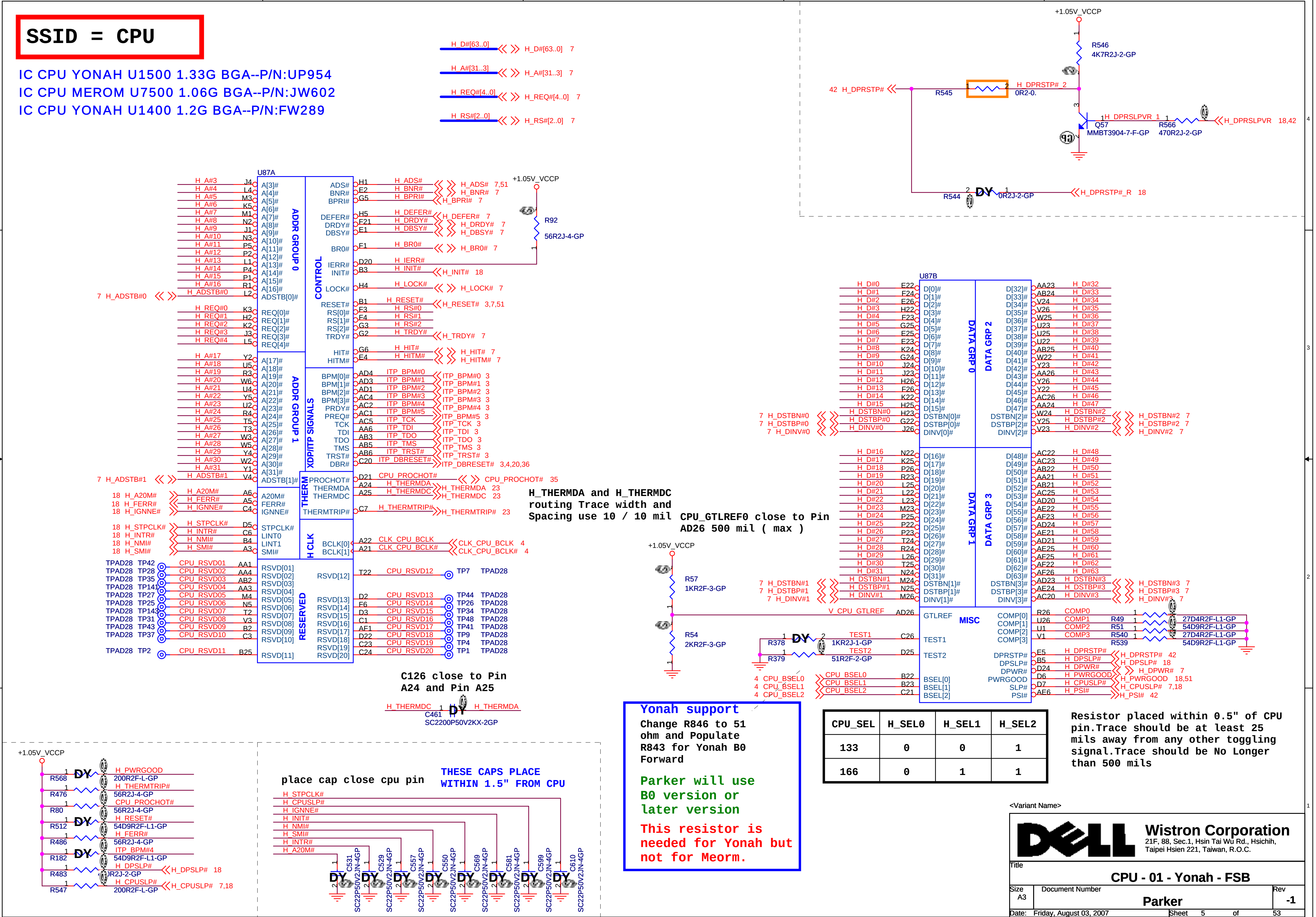
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Clock Generator	
Size: Custom	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 4 of 53	

SSID = CPU

IC CPU YONAH U1500 1.33G BGA--P/N:UP954
IC CPU MEROM U7500 1.06G BGA--P/N:JW602
IC CPU YONAH U1400 1.2G BGA--P/N:FW289



H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

CPU_GTLREF0 close to Pin AD26 500 mil (max)

C126 close to Pin A24 and Pin A25

place cap close cpu pin

THESE CAPS PLACE WITHIN 1.5" FROM CPU

Yonah support

Change R846 to 51 ohm and Populate R843 for Yonah B0 Forward

Parker will use B0 version or later version

This resistor is needed for Yonah but not for Meorm.

CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.Trace should be No Longer than 500 mils

<Variant Name>

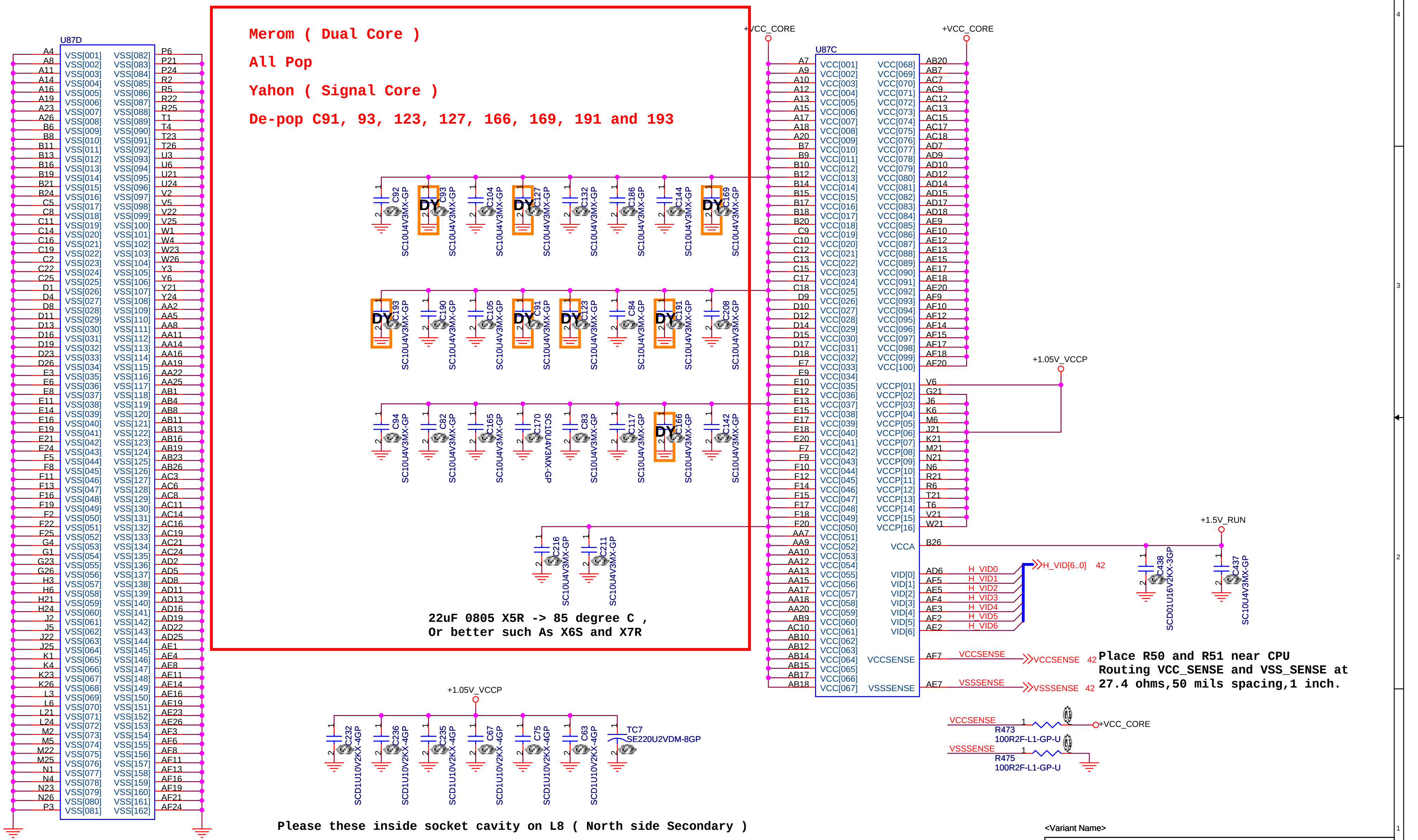
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - 01 - Yonah - FSB

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 5 of 53

SSID = CPU



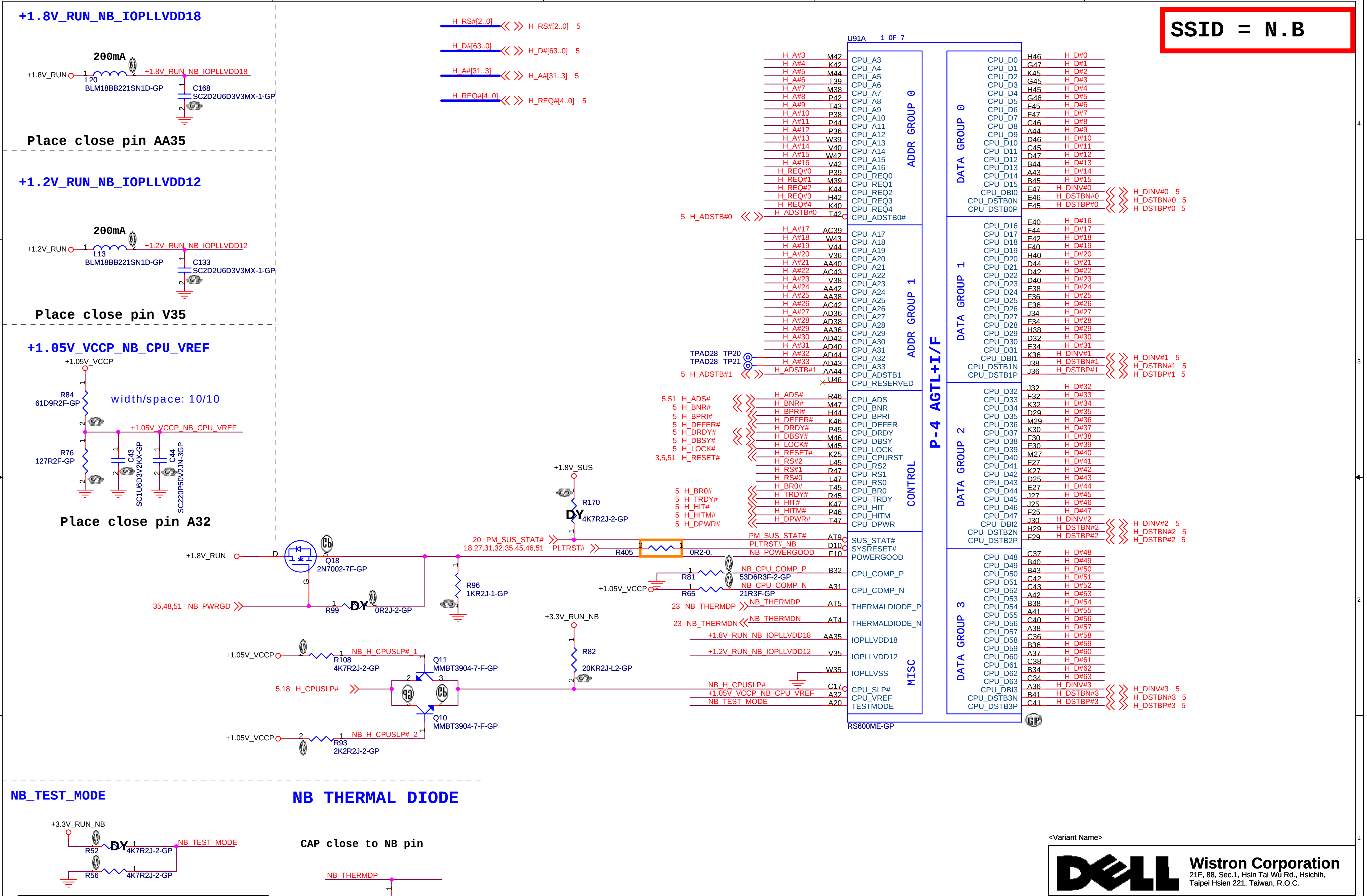
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU - 02 - Yonah - POWER**

Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 Sheet 6 of 53



TESTMODE	RS600MODE
HIGH	TEST MODE
LOW	NORMAL MODE

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

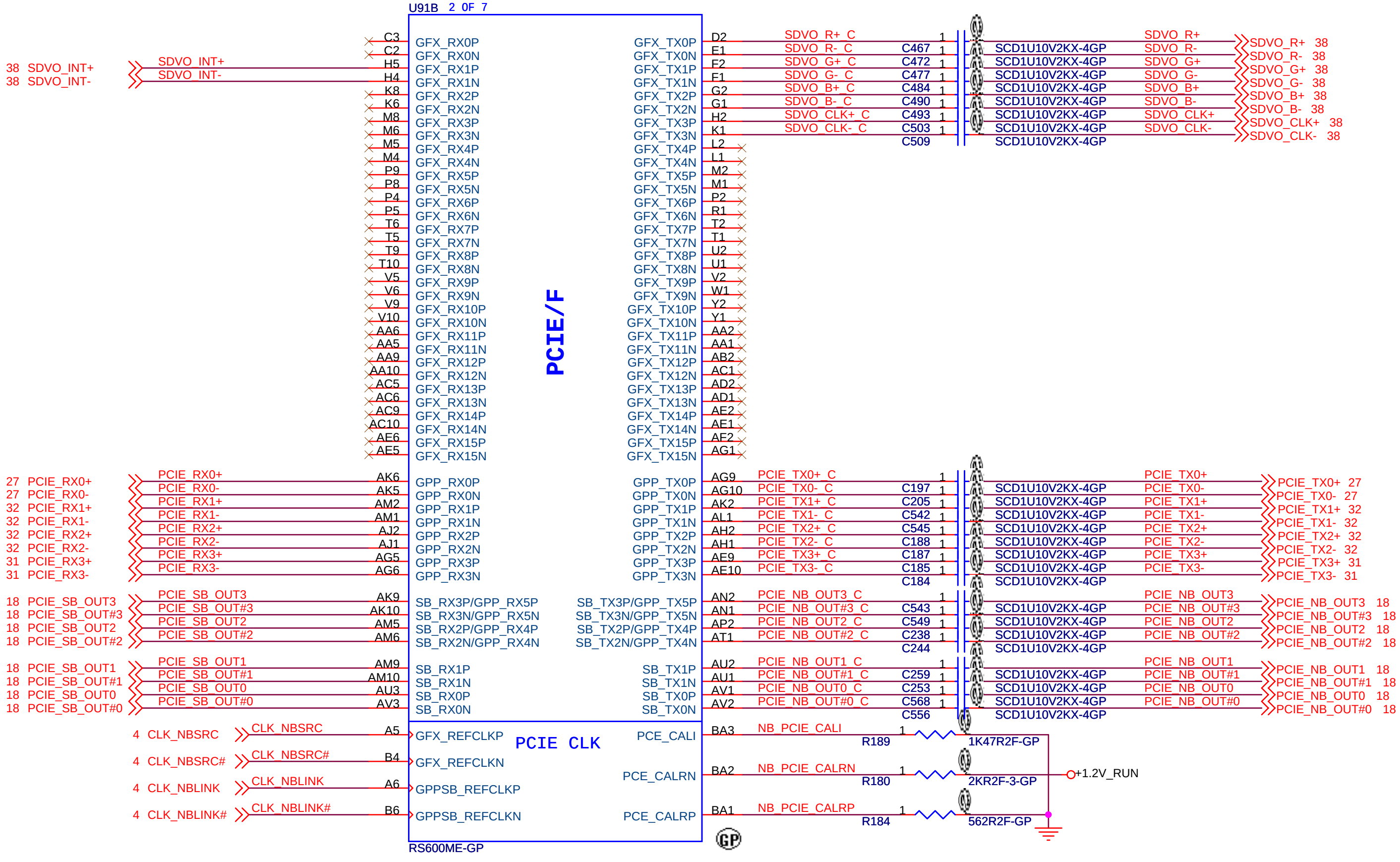
Title: RS600ME-AGTL(1/5)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 7 of 53

SSID = N.B

PCIE 0	LOM BCM5756ME
PCIE 1	MINI WWAN
PCIE 2	MINI WLAN
PCIE 3	EXPRESS CARD



<Variant Name>

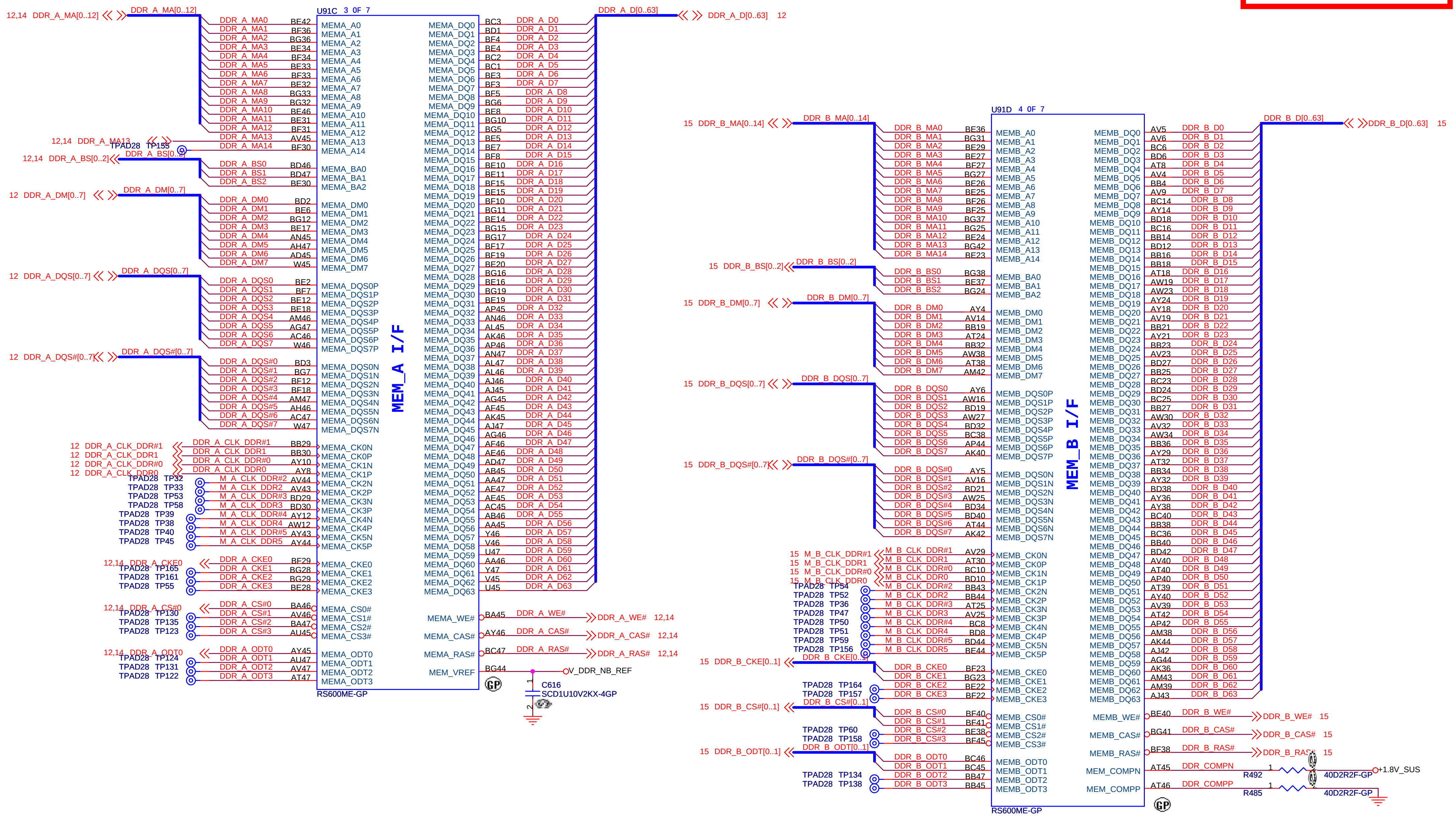
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
RS600ME-ALINK/PCIE-2(2/5)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 8 of 53

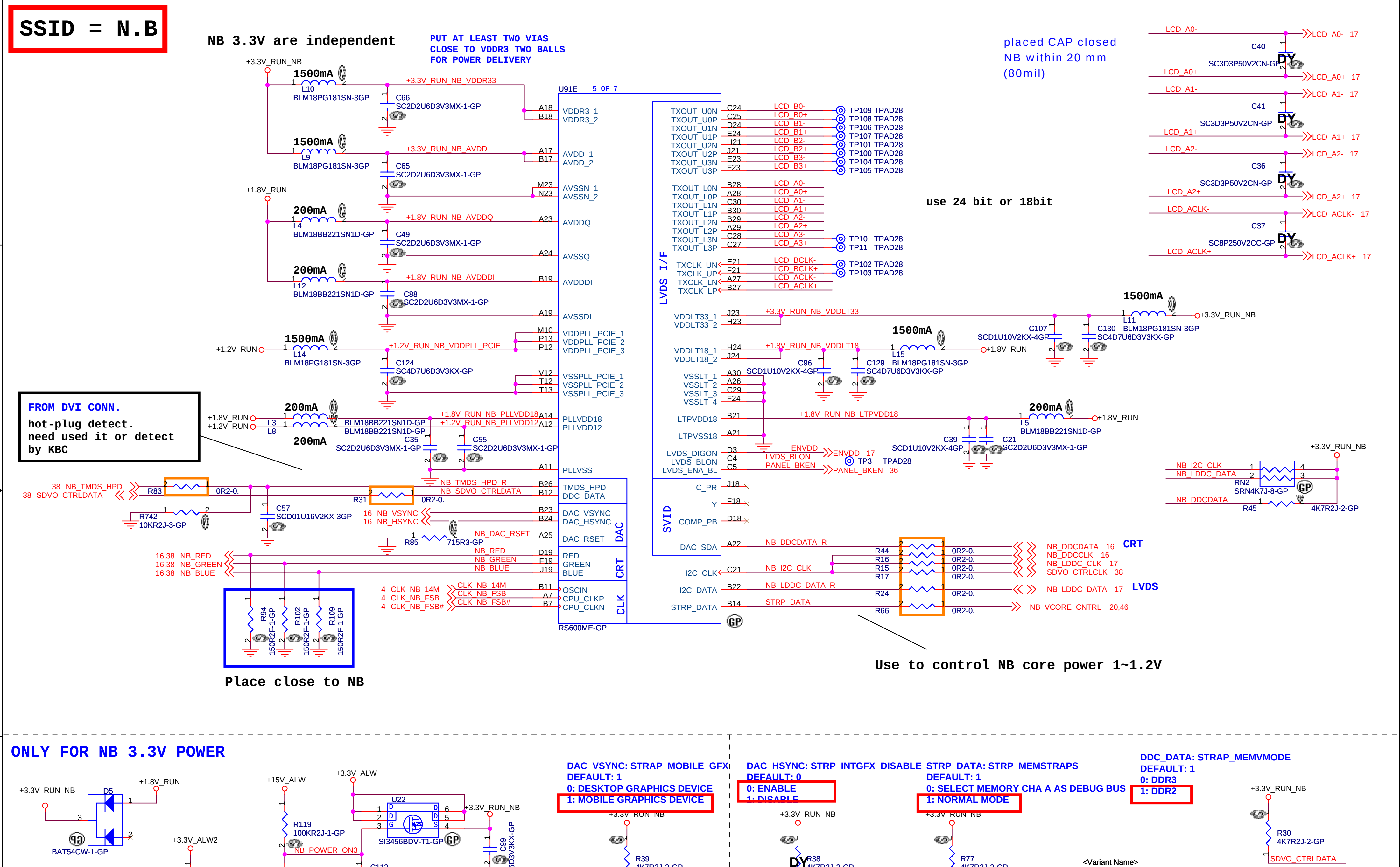
SSID = N.B



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

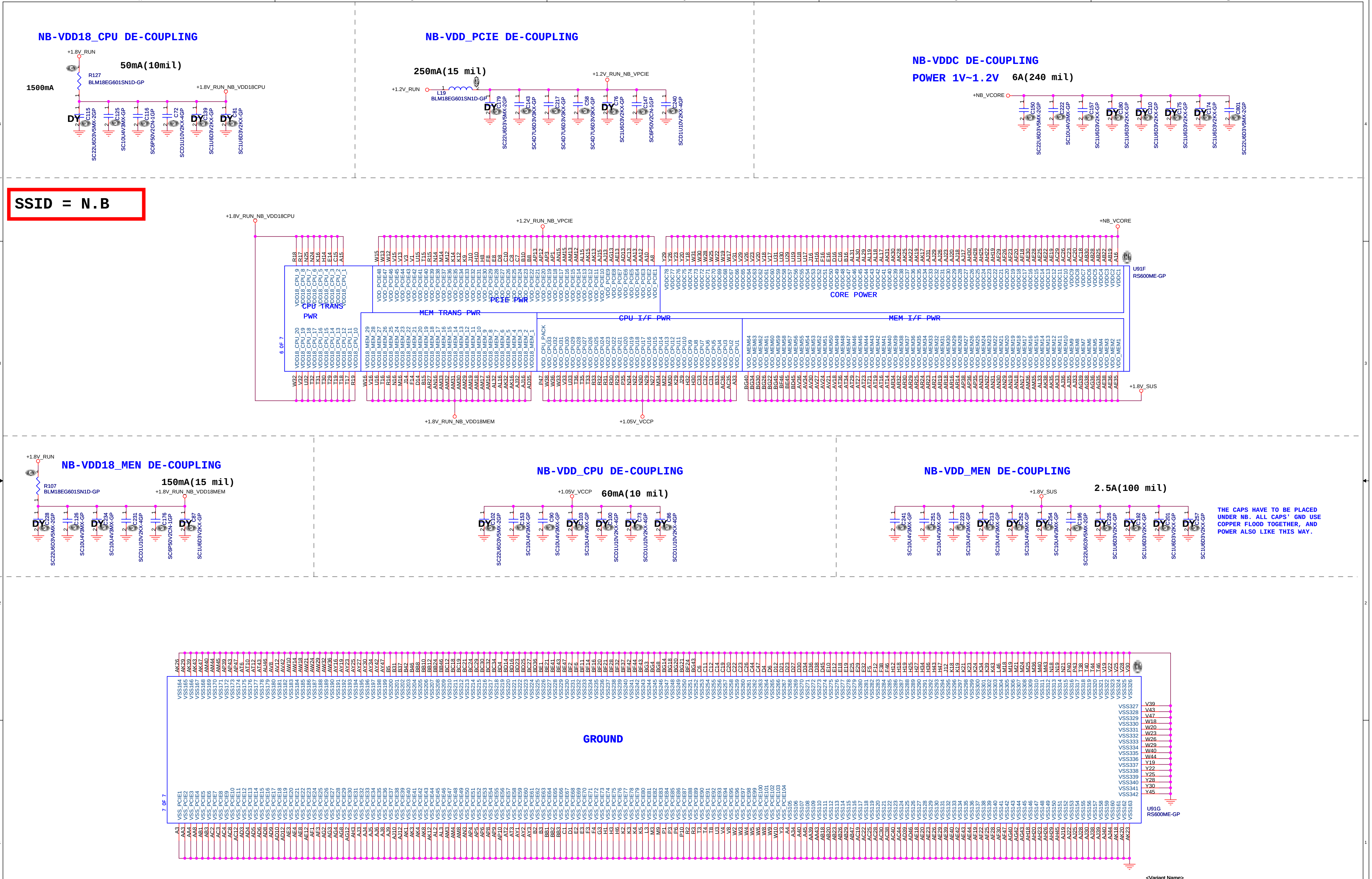
Title		
RS600ME-MEMORY I/F (3/5)		
Size: A3	Document Number: Parker	Rev: -1
Date: Tuesday, August 14, 2007	Sheet 9 of 53	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RS600ME-4(4/5)	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 10 of 53	

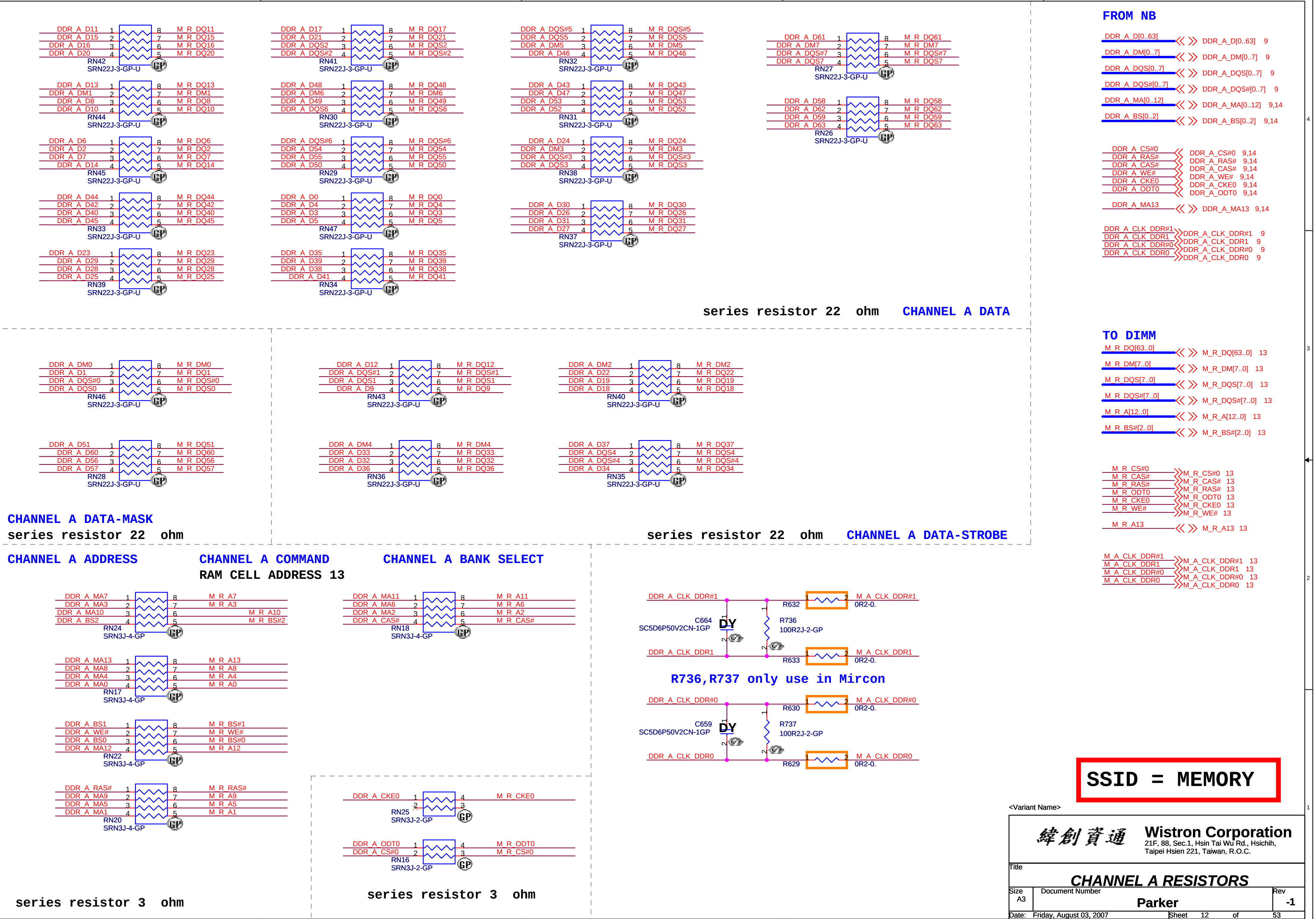


<Variant Name>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RS600ME-5(5/5)	
Size A2	Document Number: Parker	Rev -1
Date: Thursday, August 09, 2007	Sheet 11 of 53	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHANNEL A RESISTORS**

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 12 of 53

On-board DDR2 Memory

samsung

Place around the DDR2 chips

<Variant Name>

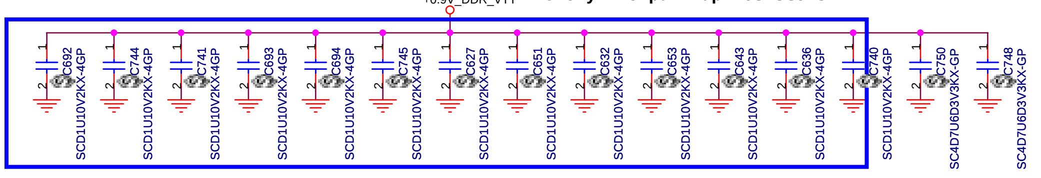
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ON BOARD MEMORY	
Size: Custom	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 13 of 53	

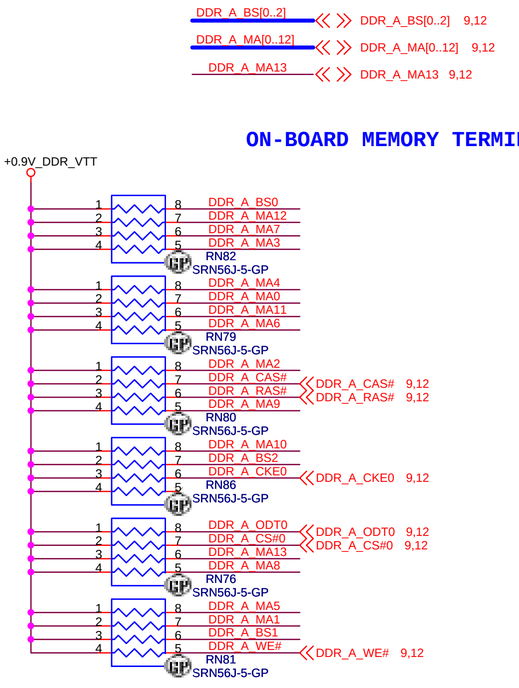
SSID = MEMORY

DIMMA-DDR +0.9V_DDR_VTT DE-COUPLING

Pleace use One Capacitor close to every Two pull-up Resistors



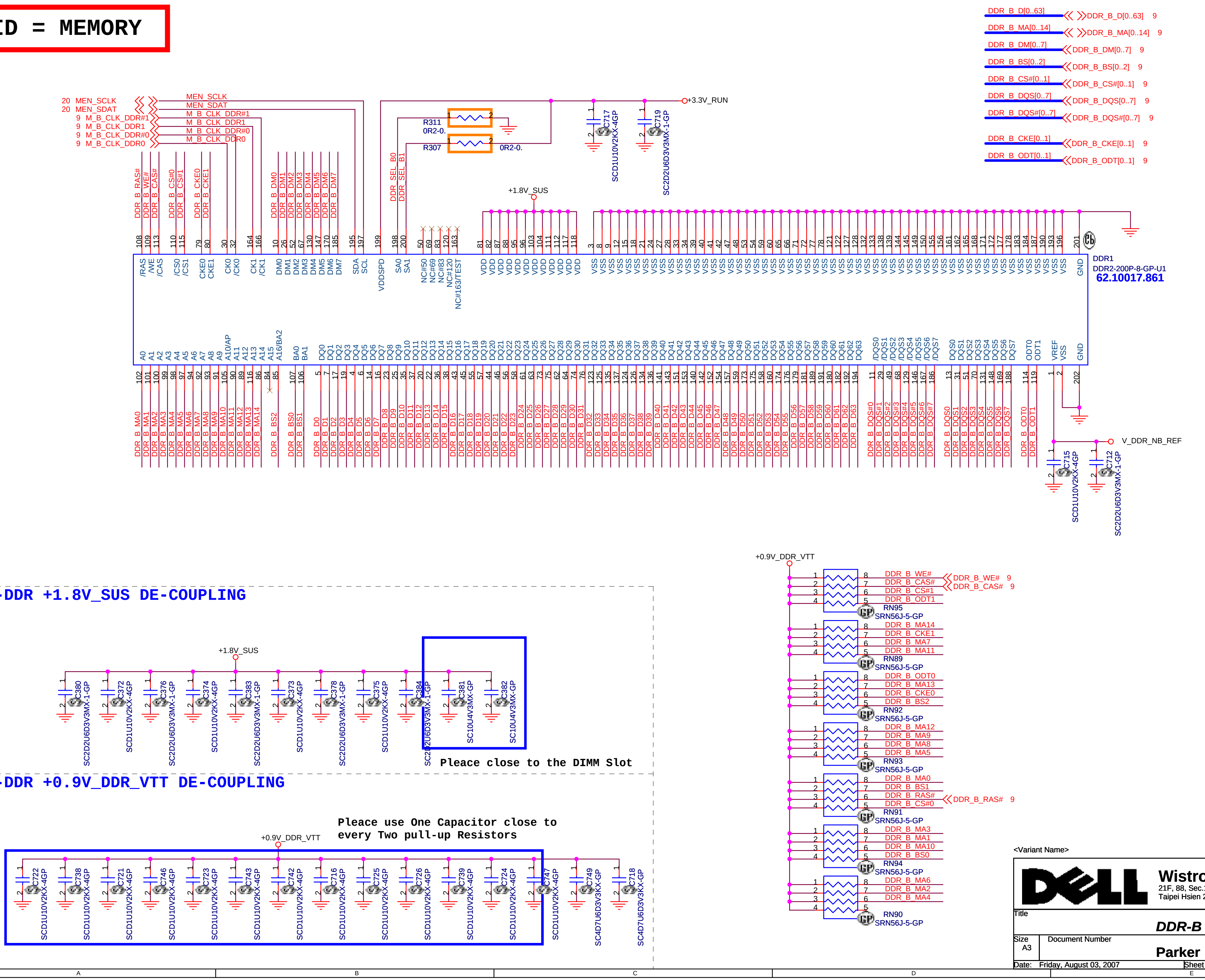
ON-BOARD MEMORY TERMINATION



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ON-BOARD MEMORY TERMINATION***	
Size A3	Document Number **Parker**	Rev -1
Date: Friday, August 03, 2007	Sheet 14 of 53	

SSID = MEMORY

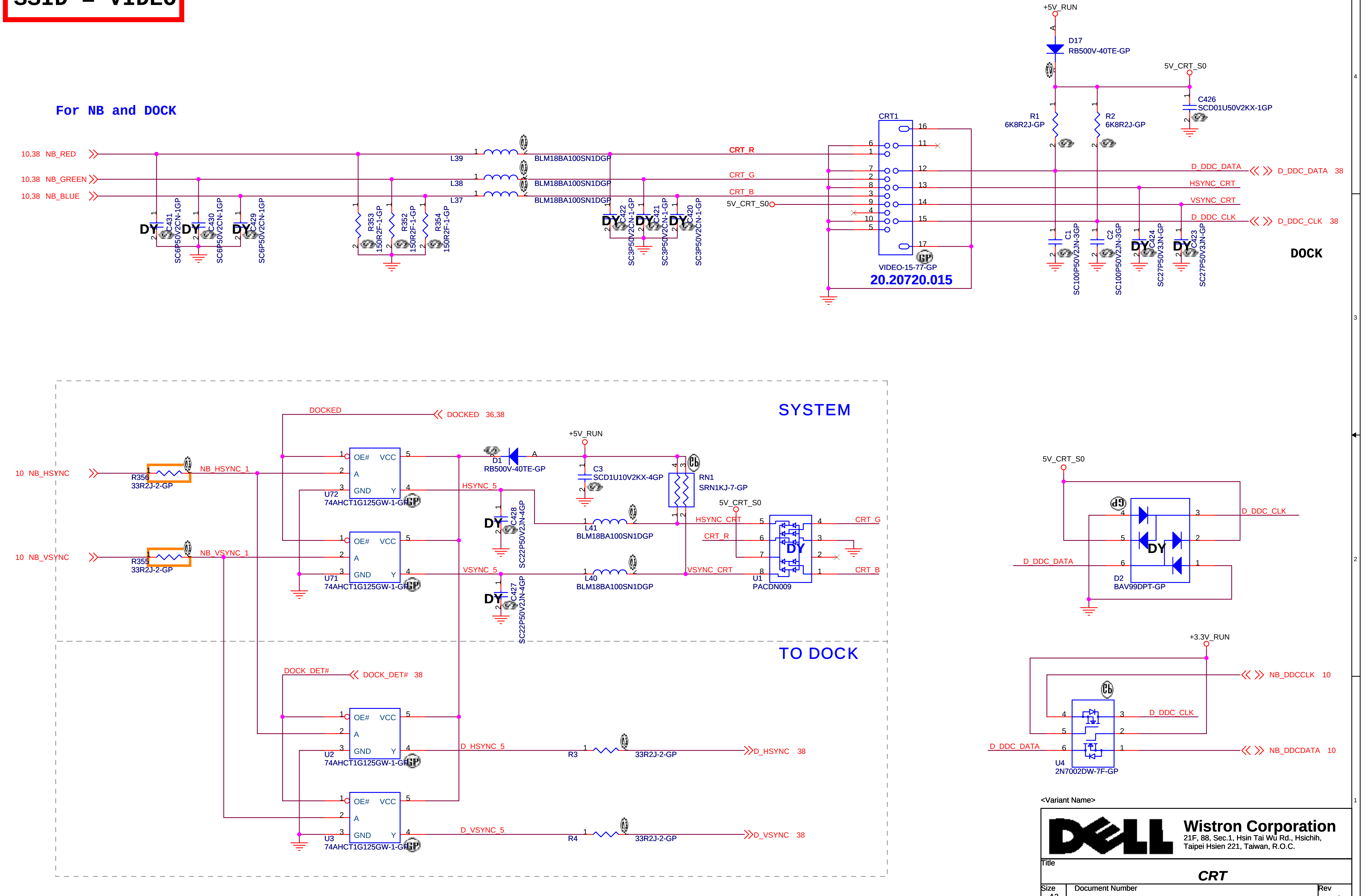


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR-B	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 15 of 53	

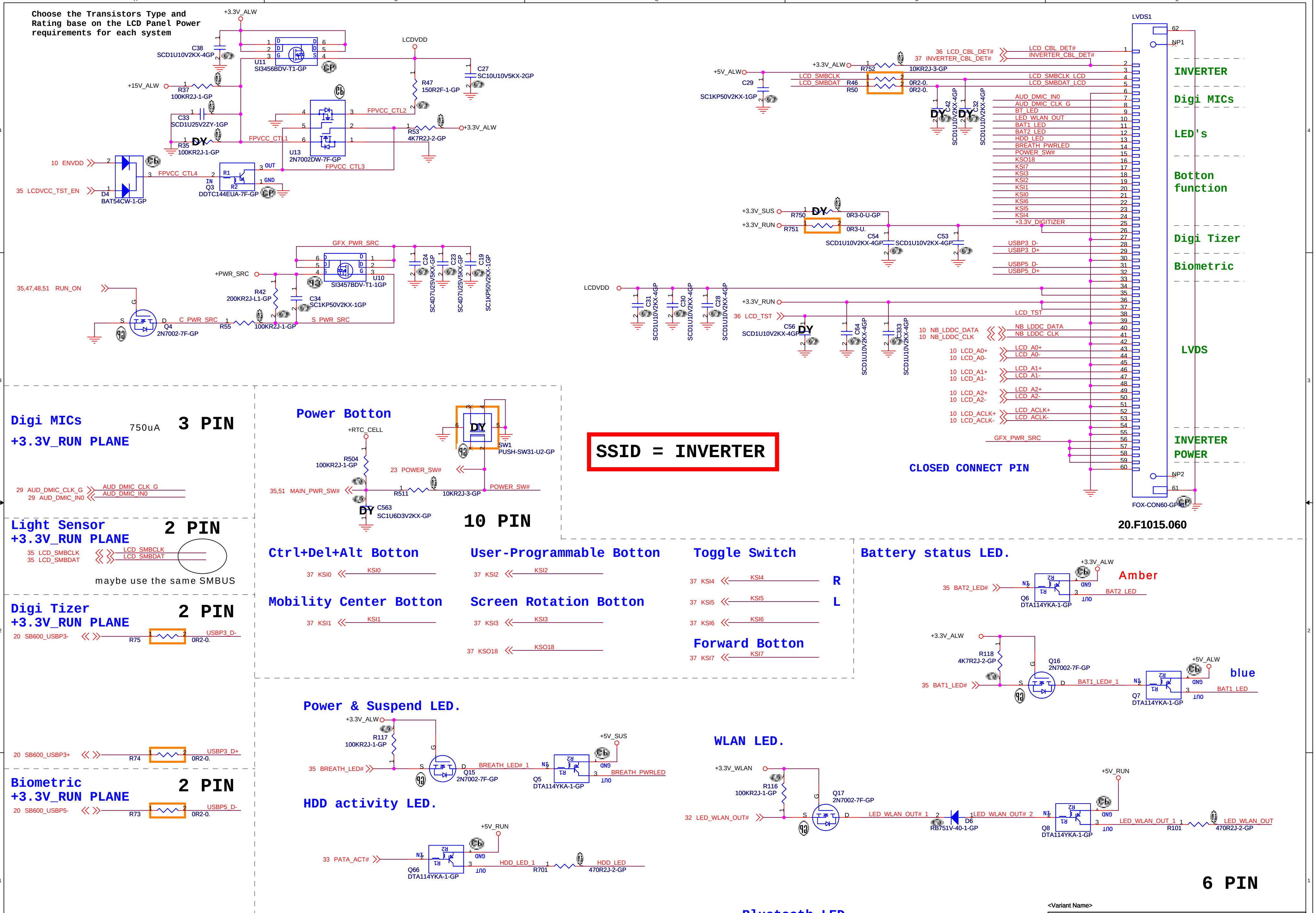
SSID = VIDEO



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

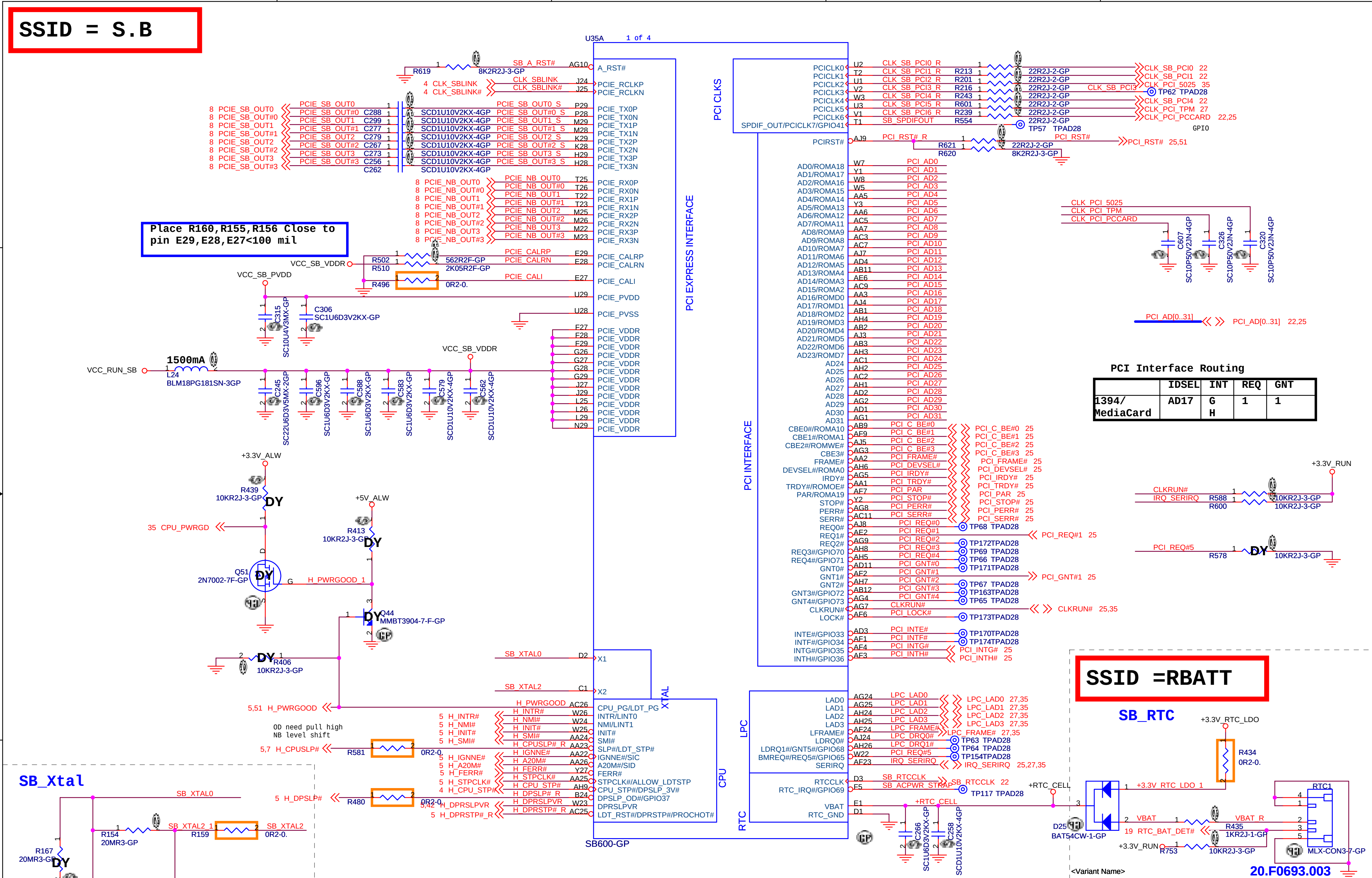
Title	CRT		
Size A3	Document Number: Parker		Rev -1
Date: Friday, August 03, 2007		Sheet 16 of 53	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LVDS	
Size: Custom	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 17 of 53	



PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	G H	1	1

<Variant Name>

20.F0693.003

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

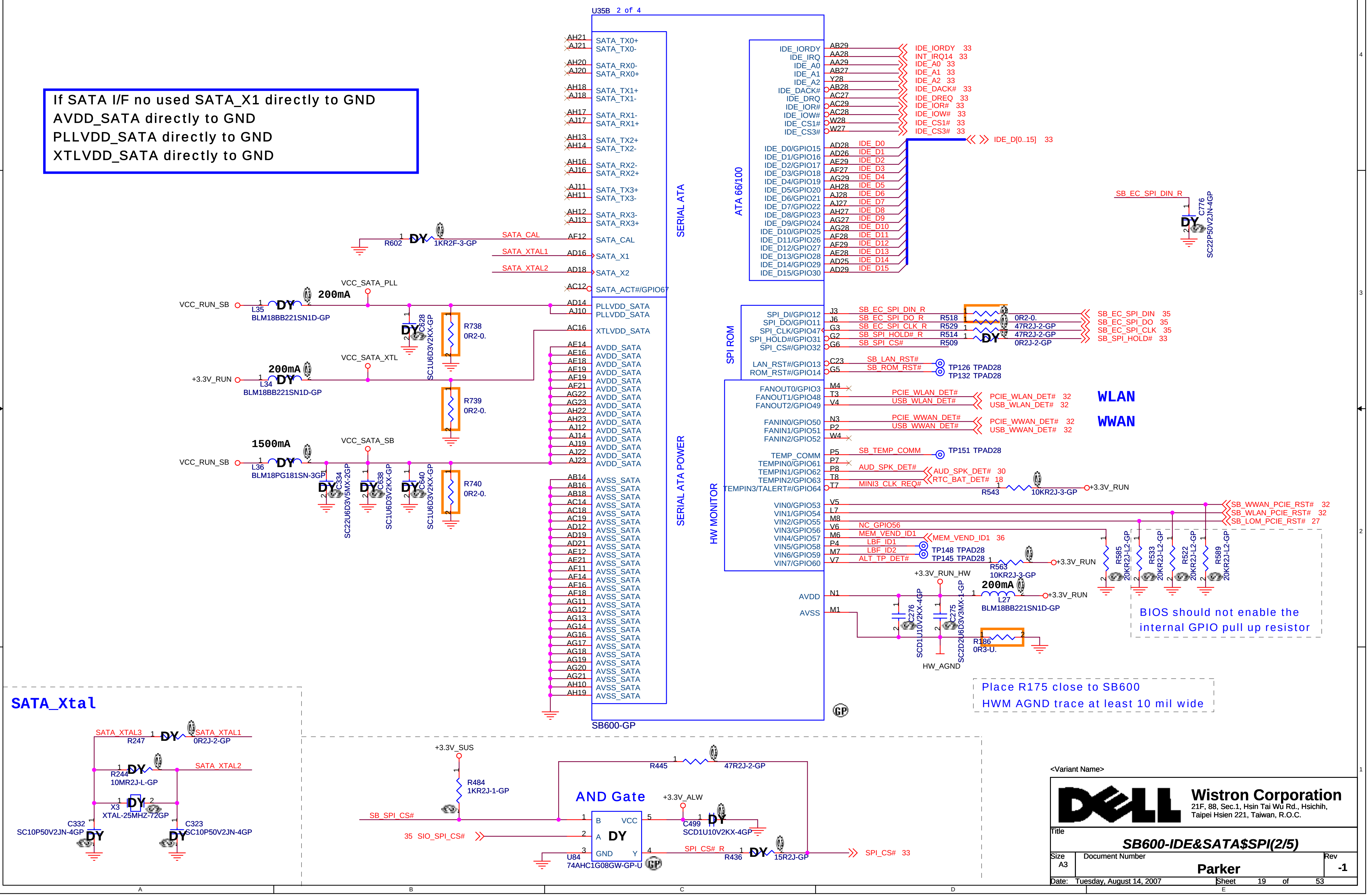
Title: SB600-CPU&LPC&PCI&PCIE(1/5)

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 18 of 53

SSID = S.B

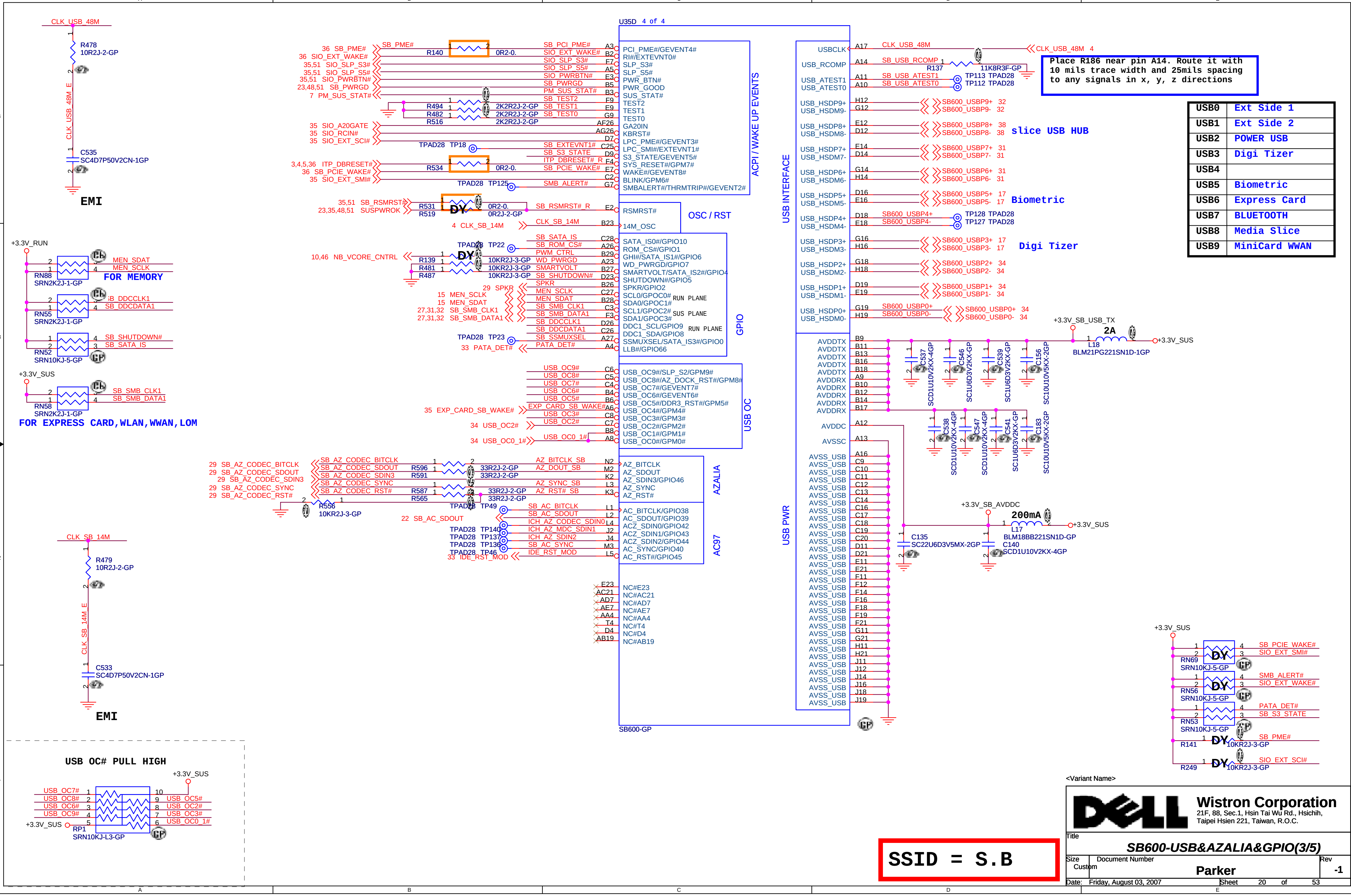
If SATA I/F no used SATA_X1 directly to GND
AVDD_SATA directly to GND
PLLVDD_SATA directly to GND
XTLVDD_SATA directly to GND



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SB600-IDE&SATA$SPI(2/5)	
Size A3	Document Number Parker	Rev -1
Date: Tuesday, August 14, 2007	Sheet 19 of 53	



USB0	Ext Side 1
USB1	Ext Side 2
USB2	POWER USB
USB3	Digi Tizer
USB4	
USB5	Biometric
USB6	Express Card
USB7	BLUETOOTH
USB8	Media Slice
USB9	MiniCard WWAN

SSID = S.B

<Variant Name>

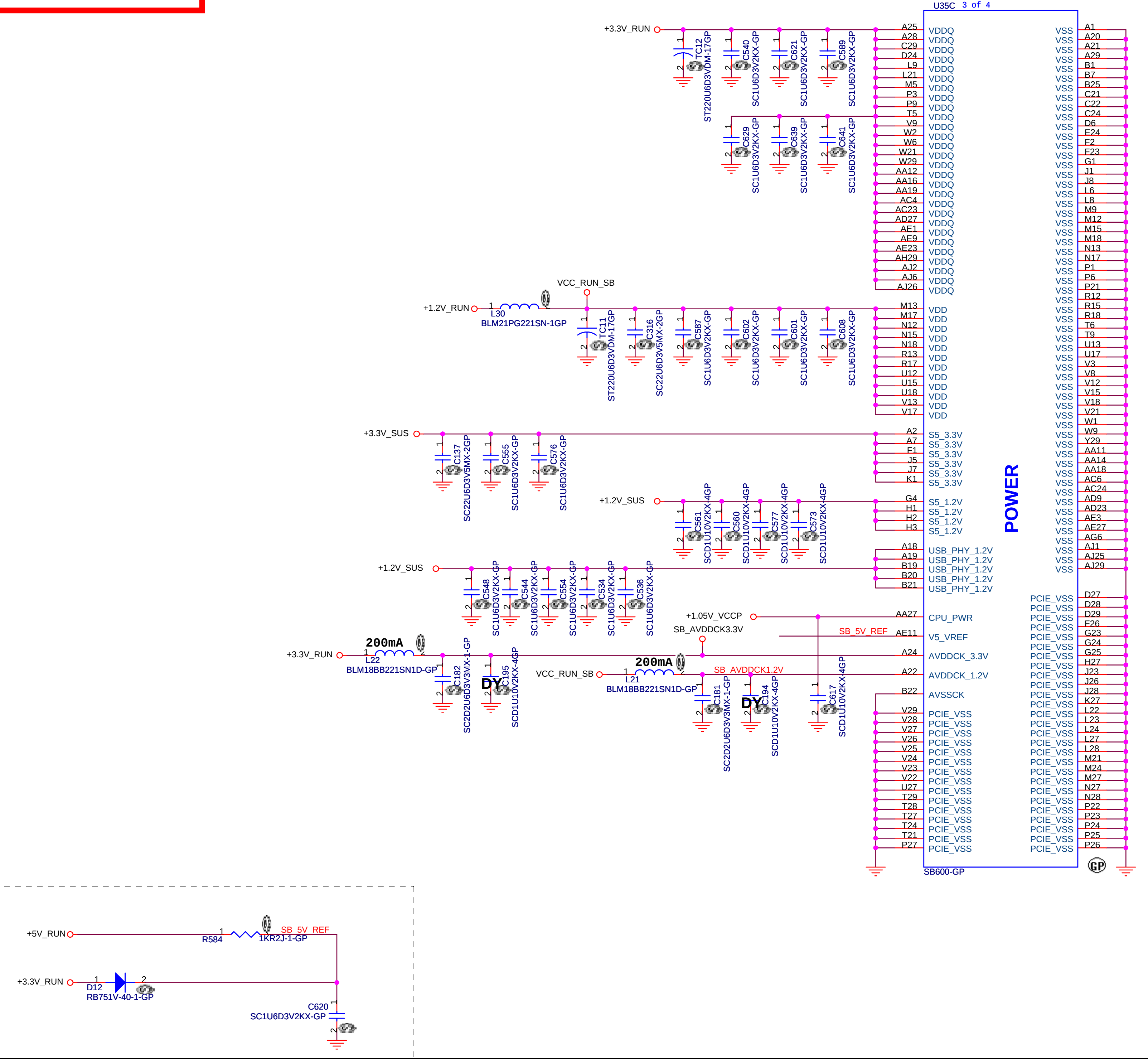
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600-USB&AZALIA&GPIO(3/5)

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 20 of 53

SSID = S.B



<Variant Name>

DELL

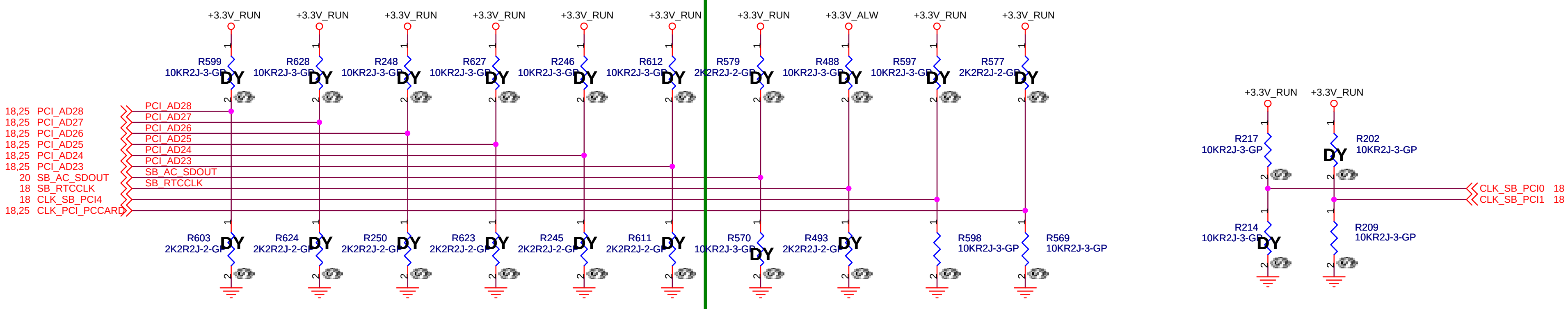
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
SB600-Power(4/5)		
Size: A3	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 21 of 53	

Debug Straps

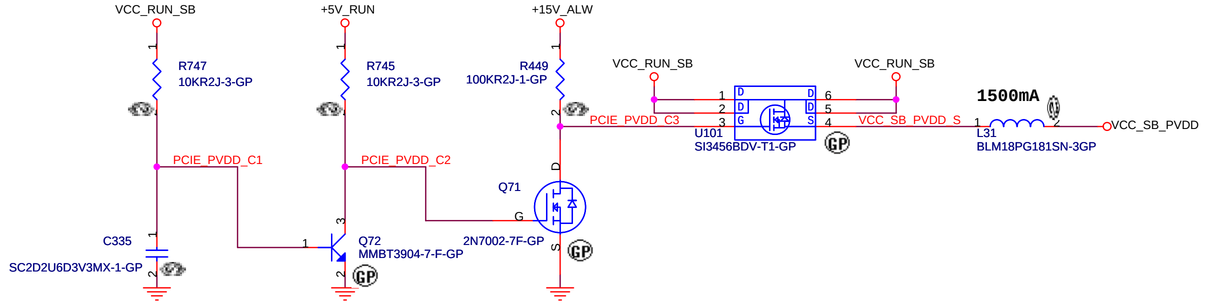
SSID = S.B

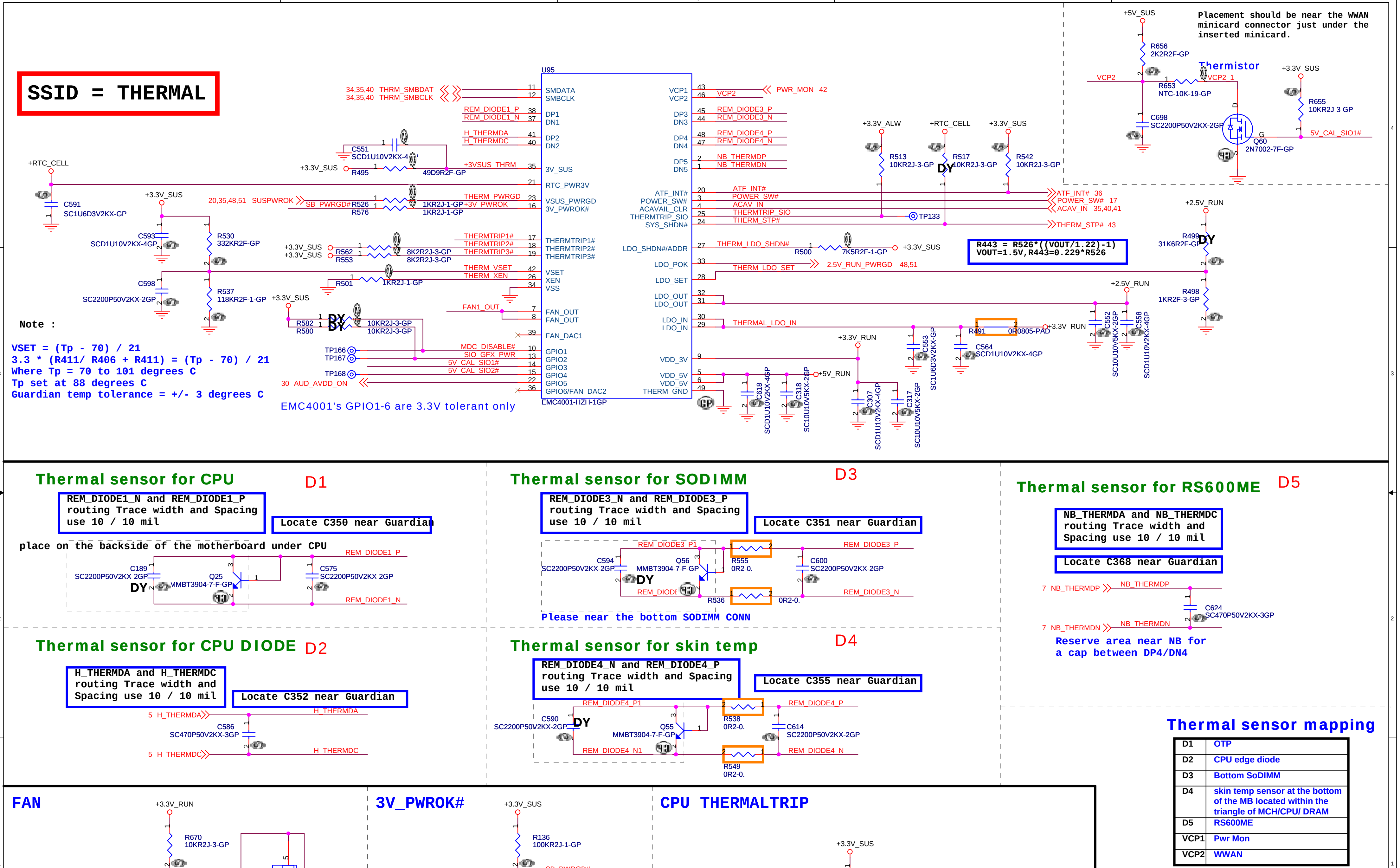
Standard Straps



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	AC_SDOUT	RTC_CLK	PCI_CLK4 (CLK_SB_PCI4)	PCI_CLK6 (CLK_PCI_PCCARD)
HIGH	LONG RESET **Default**	PCI PLL **Default**	ACPI BCLK **Default**	IDE PLL **Default**	DEFAULT PCIE STRAPS **Default**	BOOTFAIL TIMER DISABLED **Default**	DEBUG STRAPS	INTERNAL RTC **Default**	INTERNAL PLL48	AMD CPU
LOW	SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	EEPROM PCIE STRAPS	BOOTFAIL TIMER ENABLED	IGNORE DEBUG STRAPS **Default**	EXTERNAL RTC	EXTERNAL 48MHZ **Default**	INTEL CPU **Default**

PCI_CLK0 (CLK_SB_PCI0)	PCI_CLK1 (CLK_SB_PCI1)	ROM TYPE	
0	0	FWH	
0	1	LPC	
1	0	SPI	**Default**
1	1	PCI	





Thermal sensor mapping

D1	OTP
D2	CPU edge diode
D3	Bottom SoDIMM
D4	skin temp sensor at the bottom of the MB located within the triangle of MCH/CPU/ DRAM
D5	RS600ME
VCP1	Pwr Mon
VCP2	WWAN

<Variant Name>

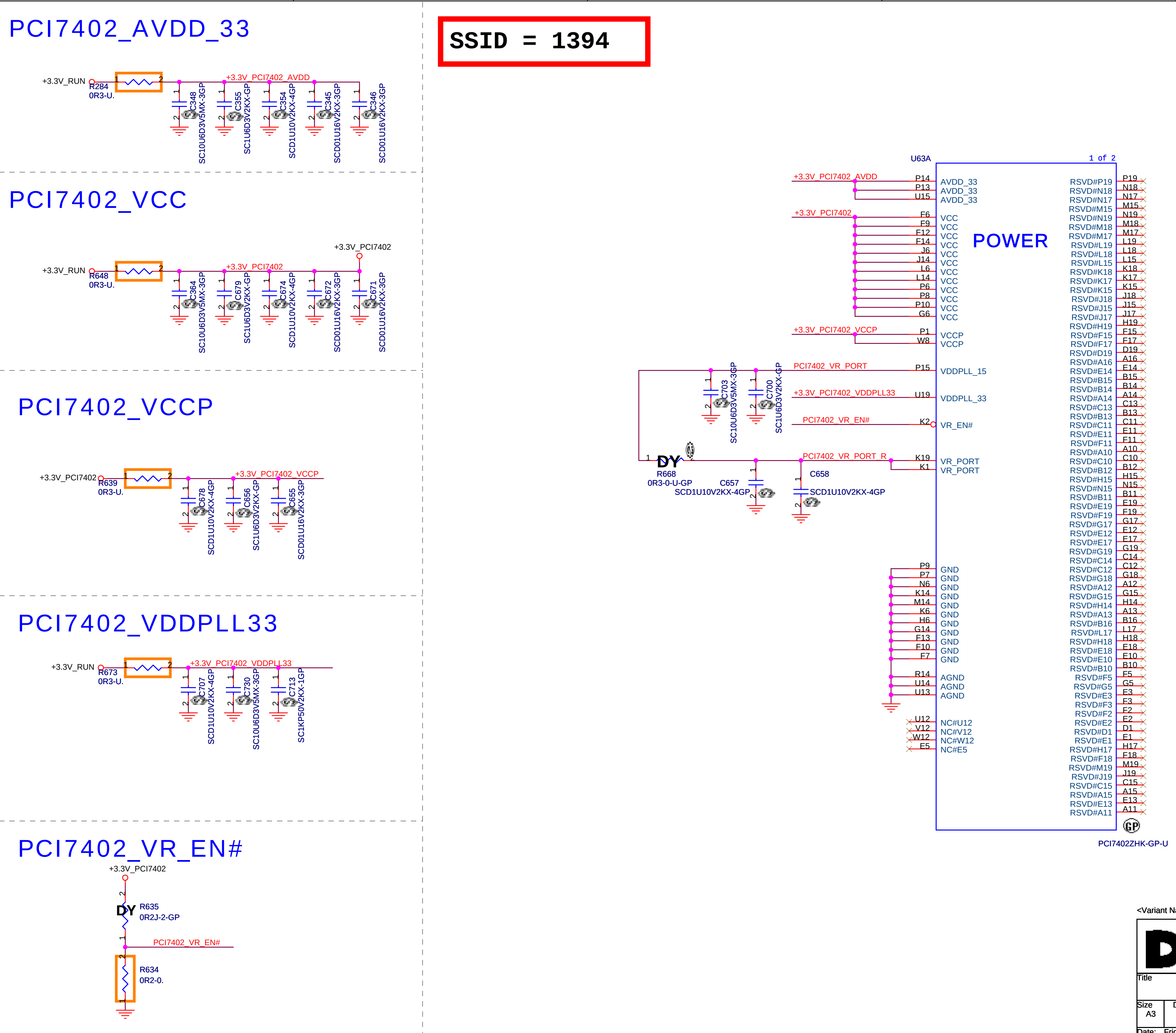
DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **FAN, EMC4001**

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 23 of 53



SSID = 1394

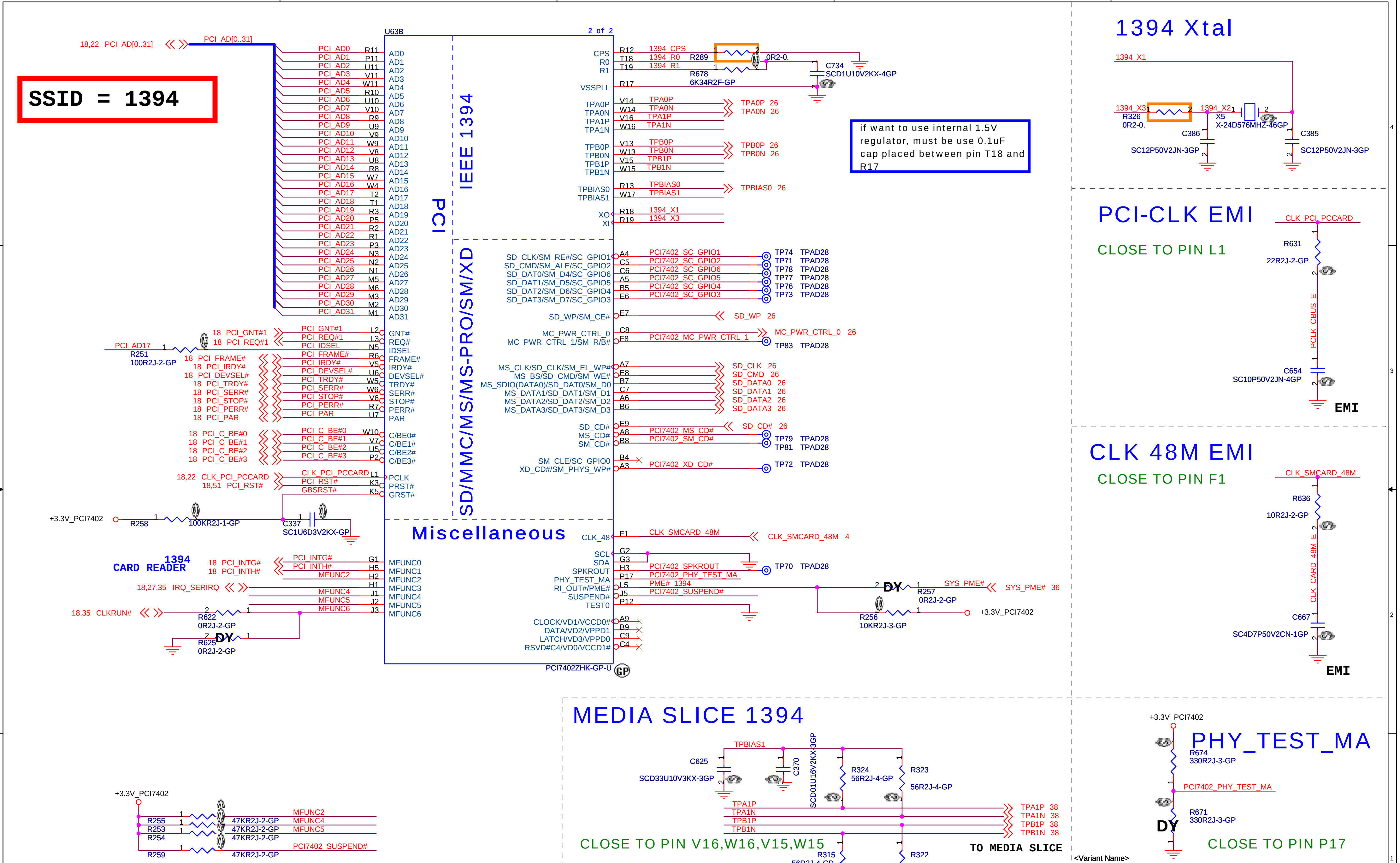
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCI7402-1

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 24 of 53



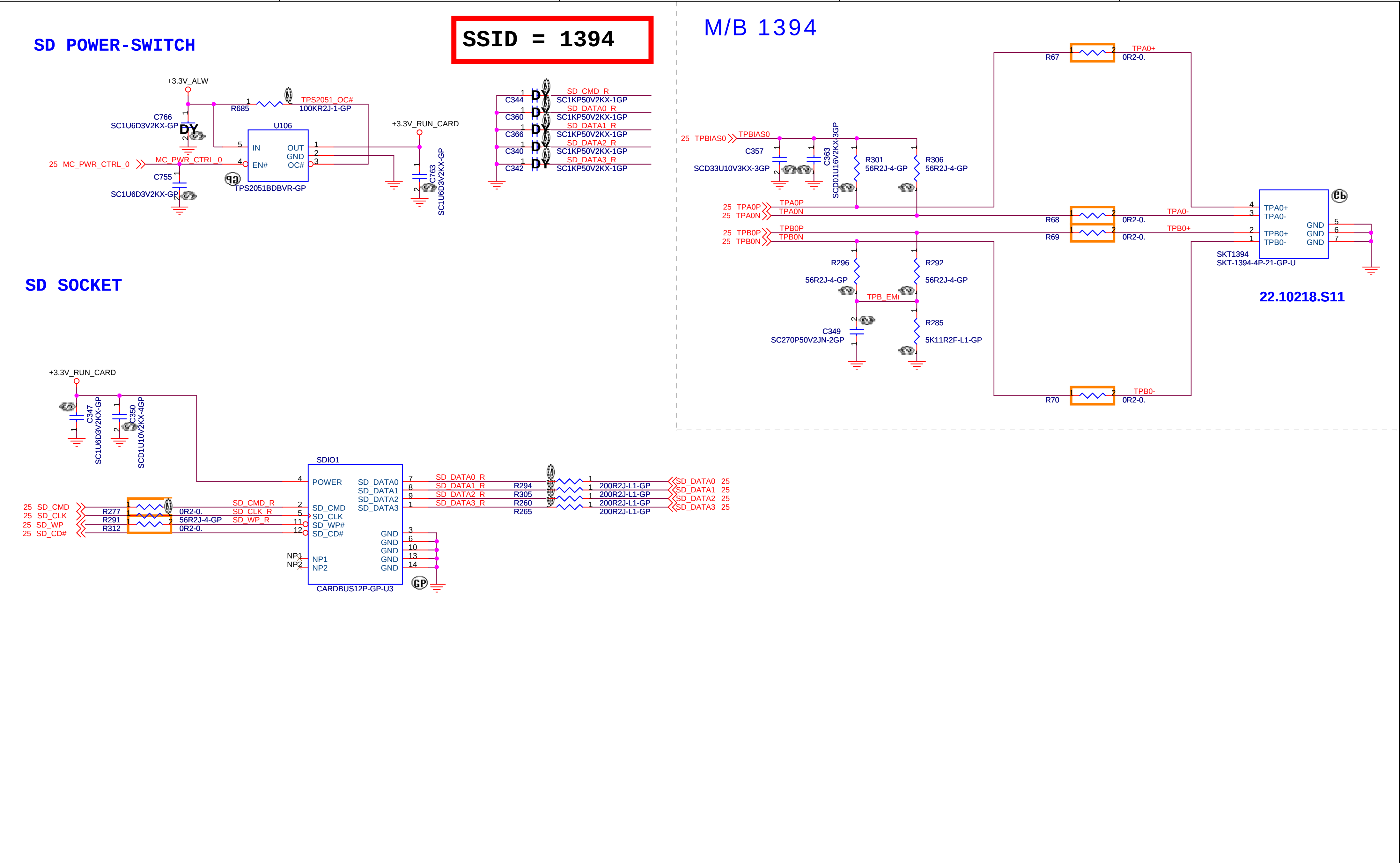
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCI7402-2**

Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 | Sheet 25 of 53



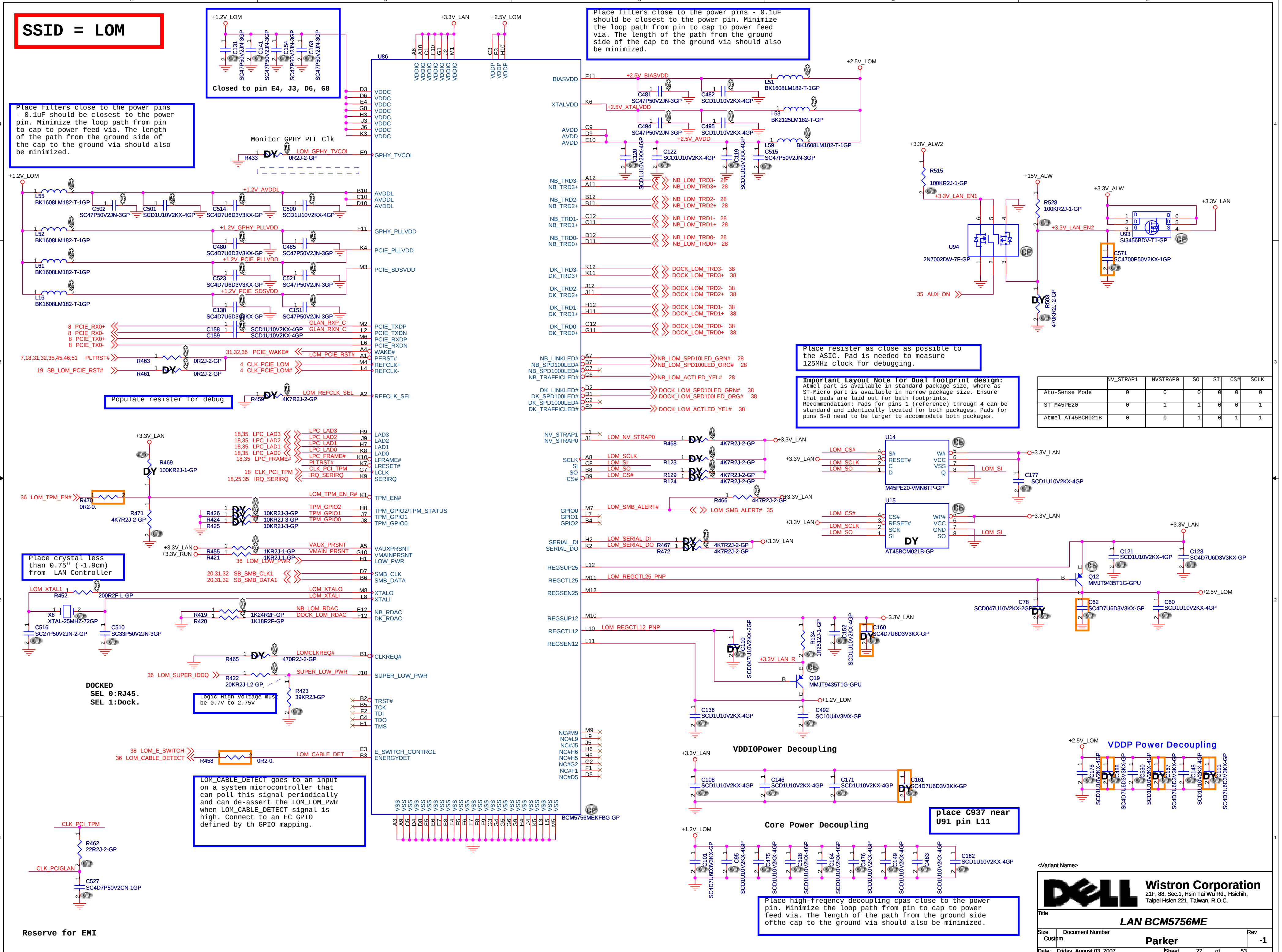
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
SMART CARD/SD/1394(3/3)

Size	Document Number	Rev
A3	Parker	-1

Date: Friday, August 03, 2007 Sheet 26 of 53



	NV_STRAP1	NVSTRAP0	SO	SI	CS#	SCLK
Ato-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

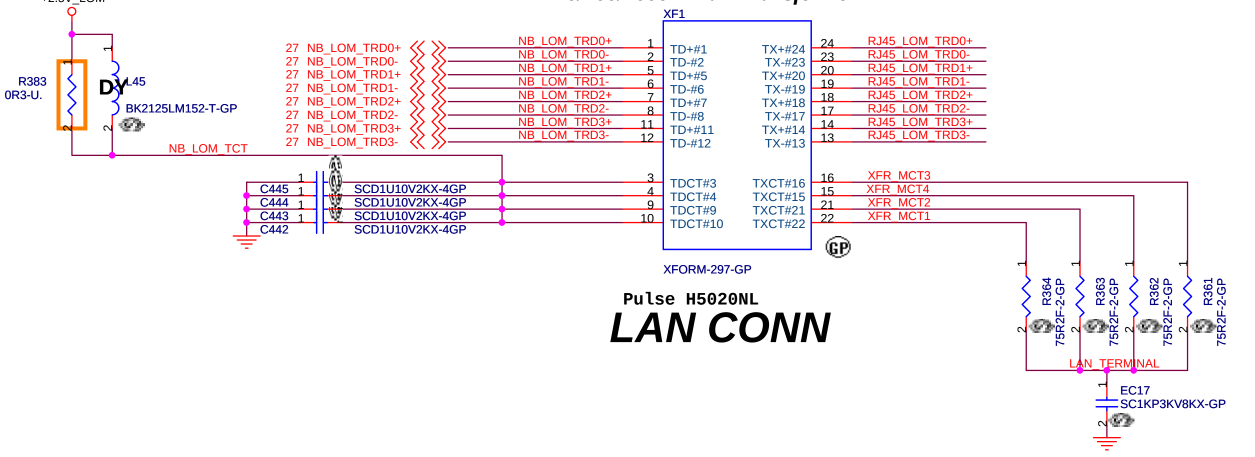
Title: LAN BCM5756ME

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 27 of 53

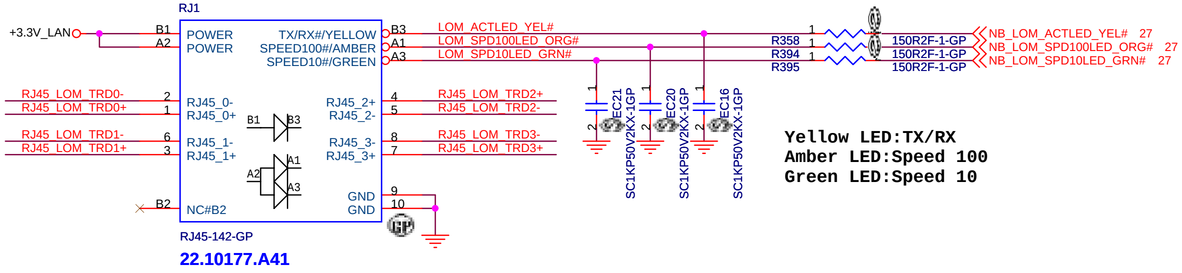
SSID = LOM

10/100/1000M Lan Transformer



Pulse H5020NL

LAN CONN



Yellow LED:TX/RX
Amber LED:Speed 100
Green LED:Speed 10

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

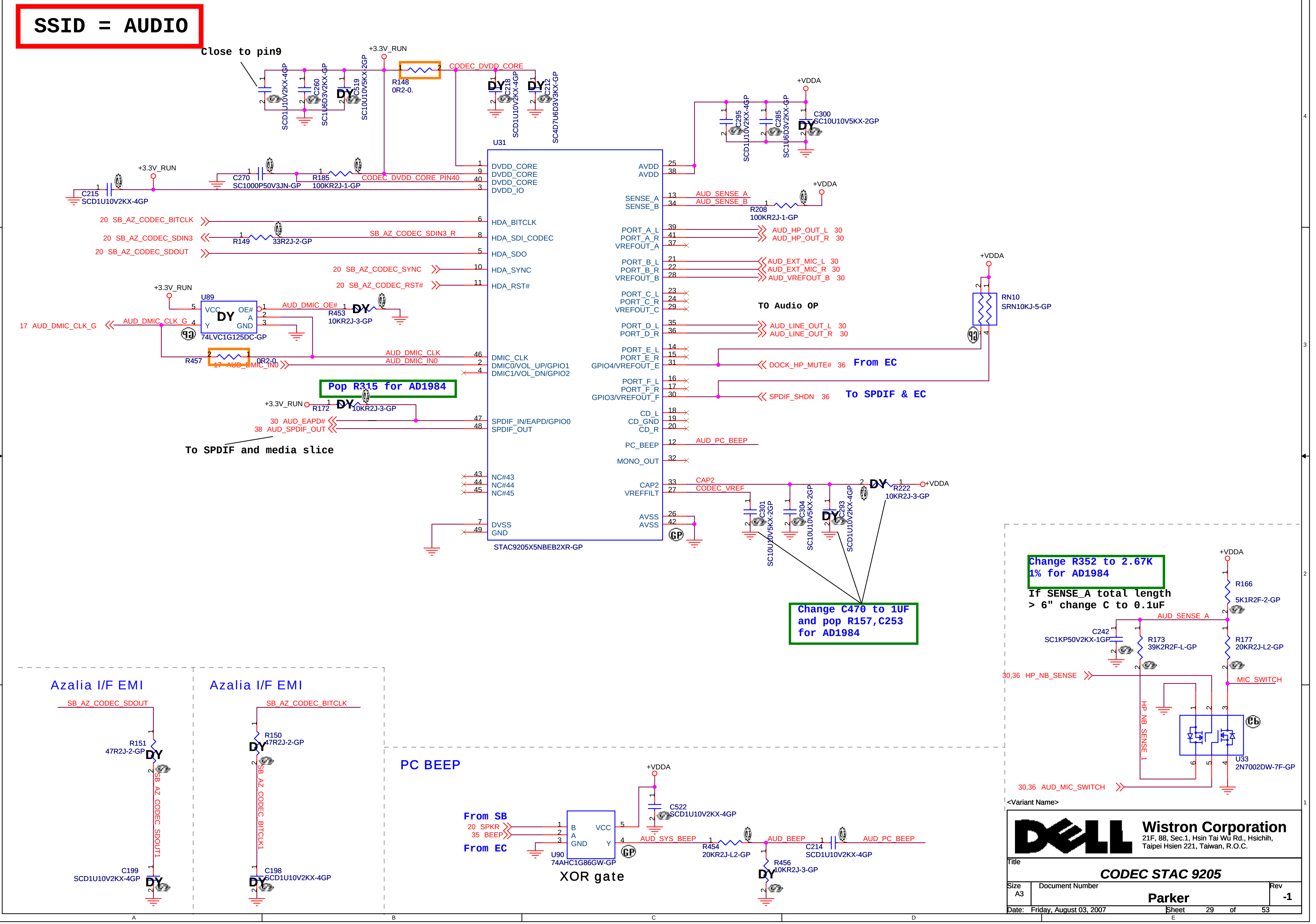
Hipot layout guide line update space > 50mil

Rj11 layout guide line update > 100mil

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

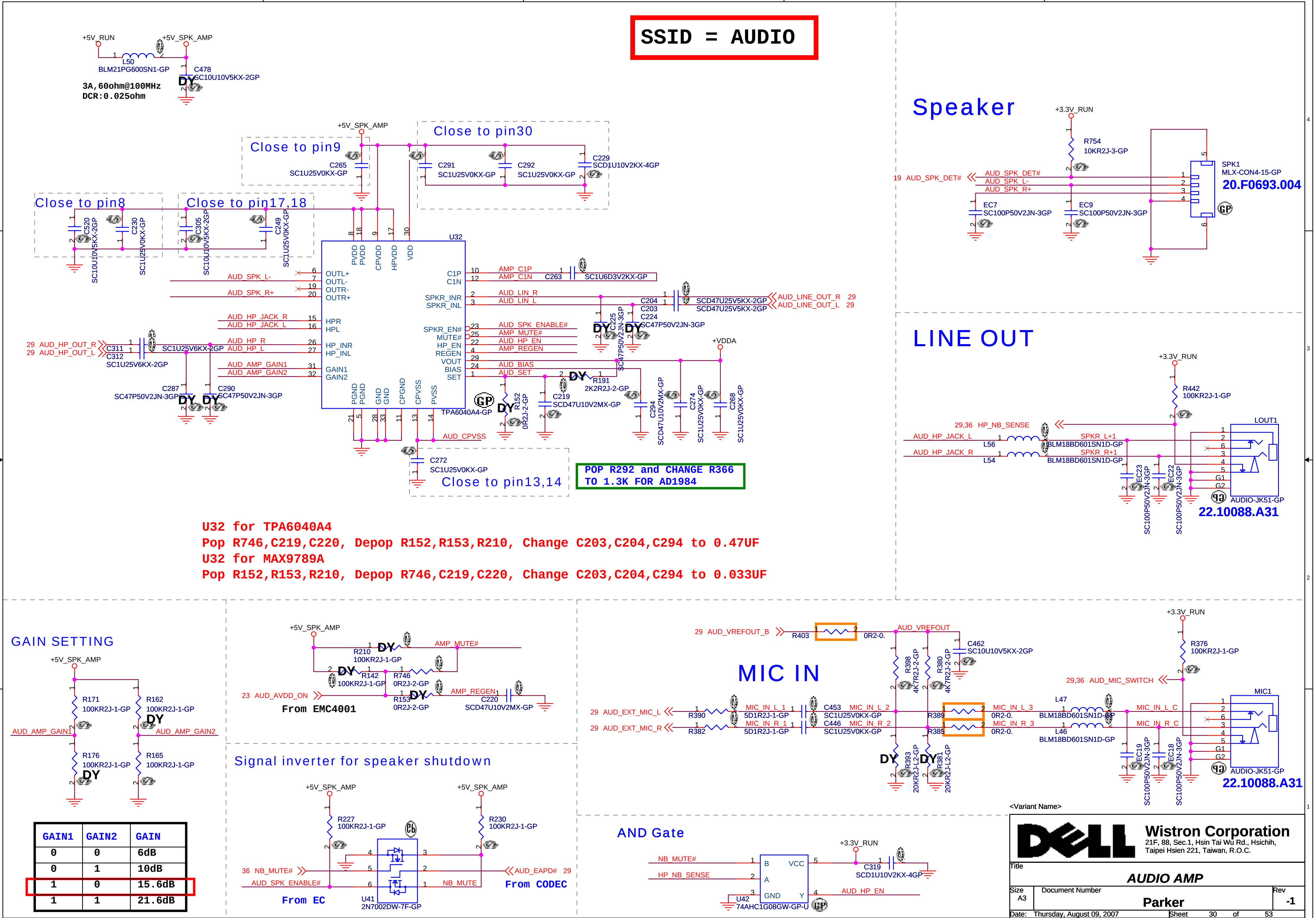
Title		
LAN Connector		
Size: A3	Document Number: Parker	Rev: -1
Date: Thursday, August 09, 2007	Sheet 28 of 53	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CODEC STAC 9205		
Size A3	Document Number: Parker		Rev -1
Date: Friday, August 03, 2007		Sheet 29 of 53	



GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

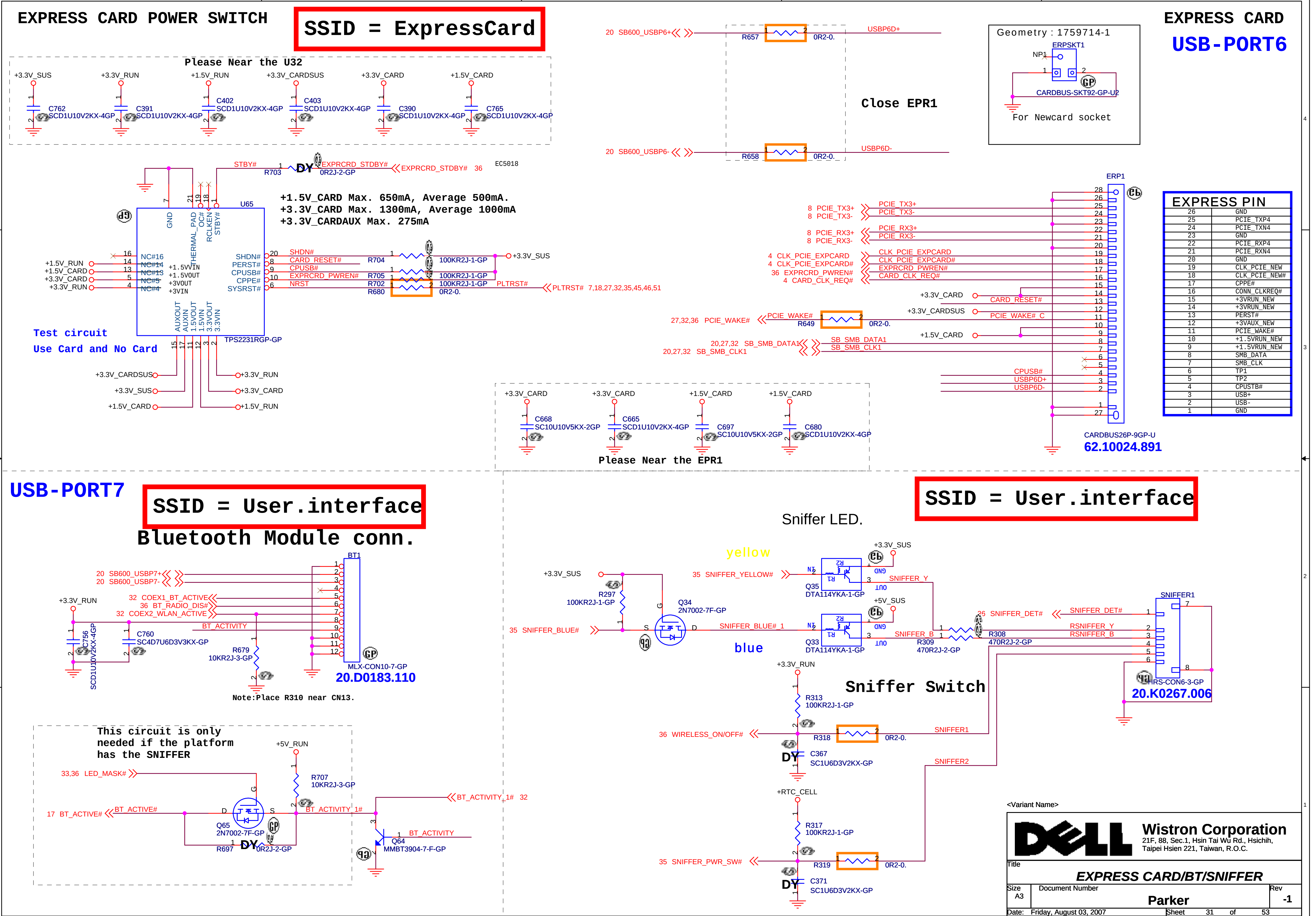
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP

Size: A3 | Document Number: Parker | Rev: -1

Date: Thursday, August 09, 2007 | Sheet 30 of 53



EXPRESS PIN

26	GND
25	PCIE_TXP4
24	PCIE_TXN4
23	GND
22	PCIE_RXP4
21	PCIE_RXN4
20	GND
19	CLK_PCIE_NEW
18	CLK_PCIE_NEW#
17	CPPE#
16	CONN_CLKREQ#
15	+3VRUN_NEW
14	+3VRUN_NEW
13	PERST#
12	+3VAUX_NEW
11	PCIE_WAKE#
10	+1.5VRUN_NEW
9	+1.5VRUN_NEW
8	SMB_DATA
7	SMB_CLK
6	TP1
5	TP2
4	CPUSTB#
3	USB+
2	USB-
1	GND

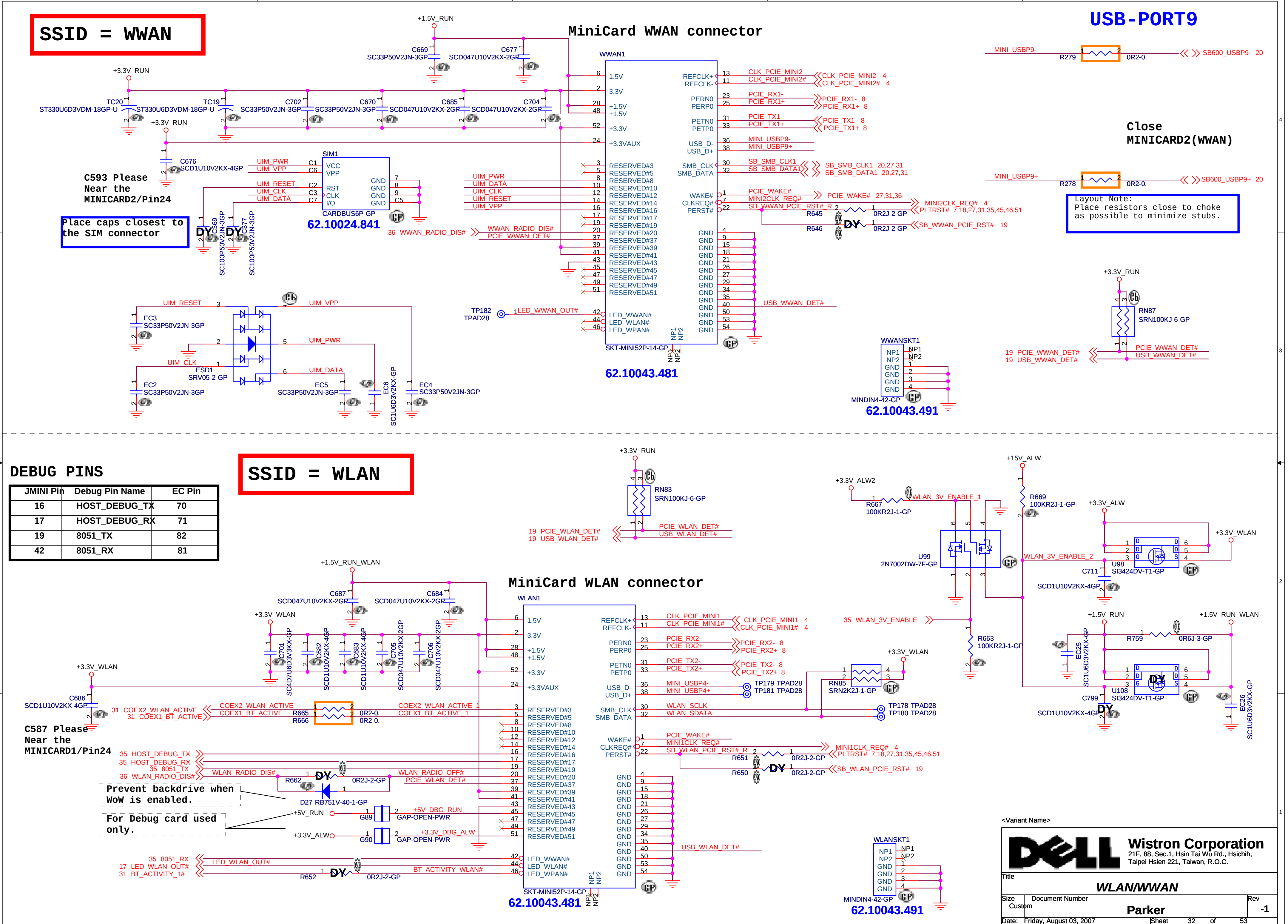
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXPRESS CARD/BT/SNIFFER

Size: A3 | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 31 of 53



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

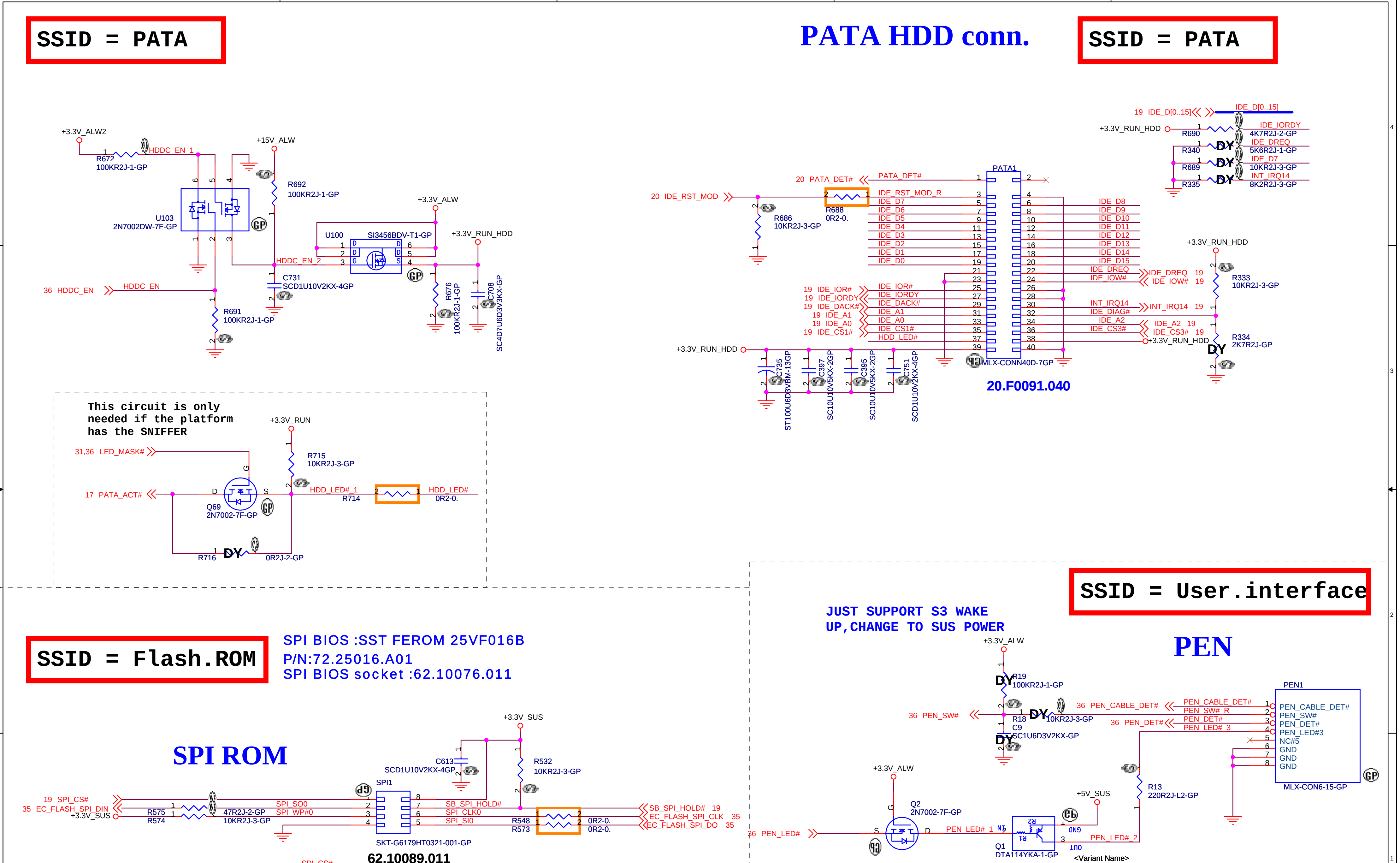
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN/WWAN

Size: Custom | Document Number: Parker | Rev: -1

Date: Friday, August 03, 2007 | Sheet 32 of 53



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	HDD/SPI ROM/PEN		
Size A3	Document Number	Parker	Rev -1
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USB POWER

SSID = USB

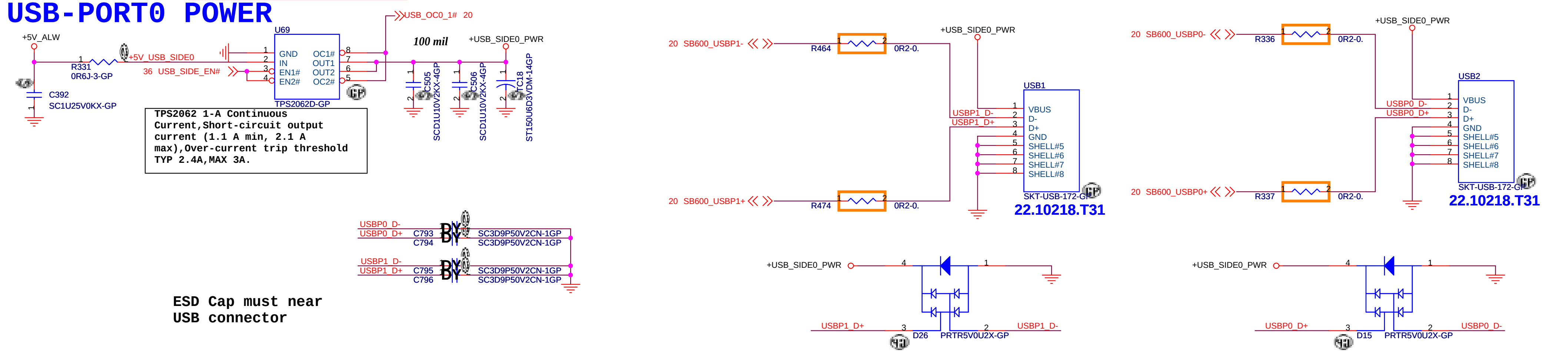
USB-PORT0 POWER

TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.

USB-PORT1

USB-PORT0

ESD Cap must near USB connector



USB-PORT 2

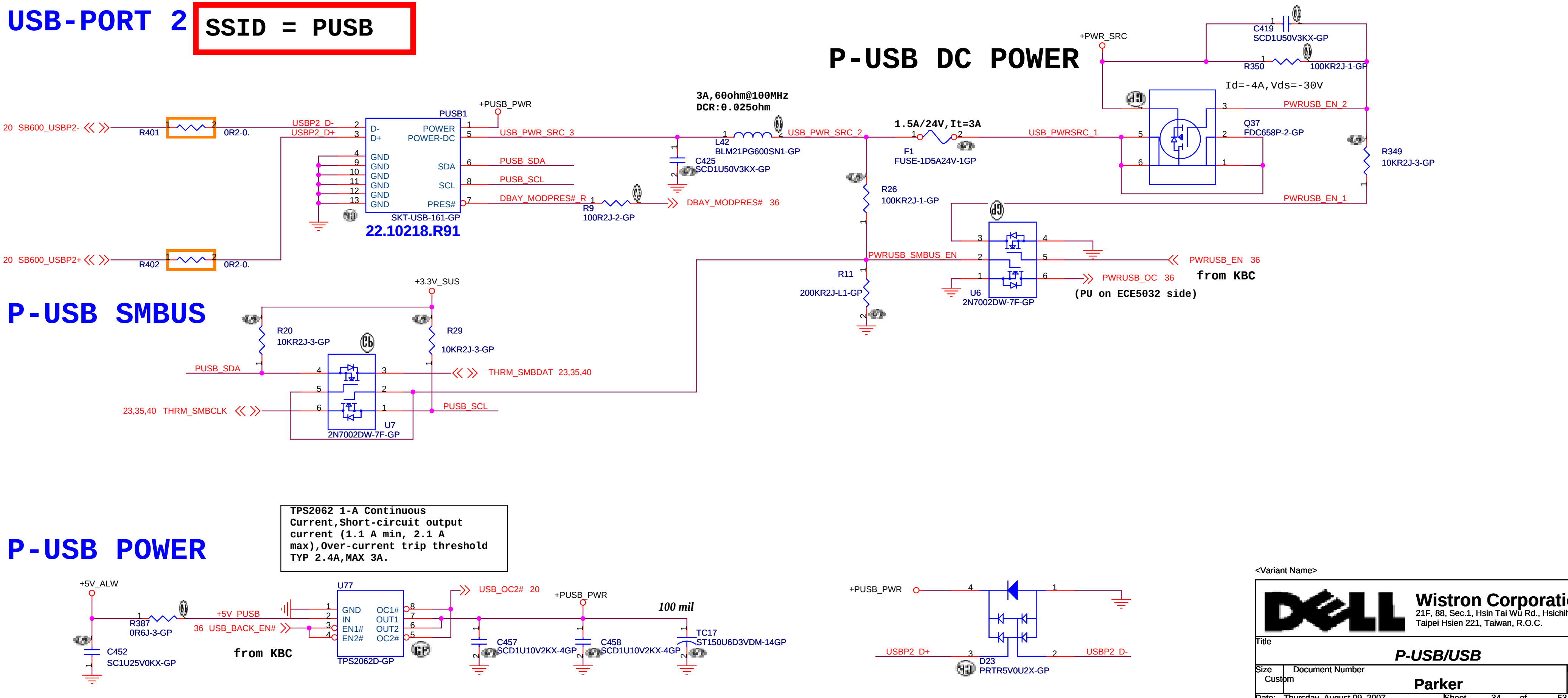
SSID = PUSB

P-USB DC POWER

P-USB SMBUS

P-USB POWER

TPS2062 1-A Continuous Current,Short-circuit output current (1.1 A min, 2.1 A max),Over-current trip threshold TYP 2.4A,MAX 3A.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	P-USB/USB		
Size: Custom	Document Number: Parker		Rev: -1
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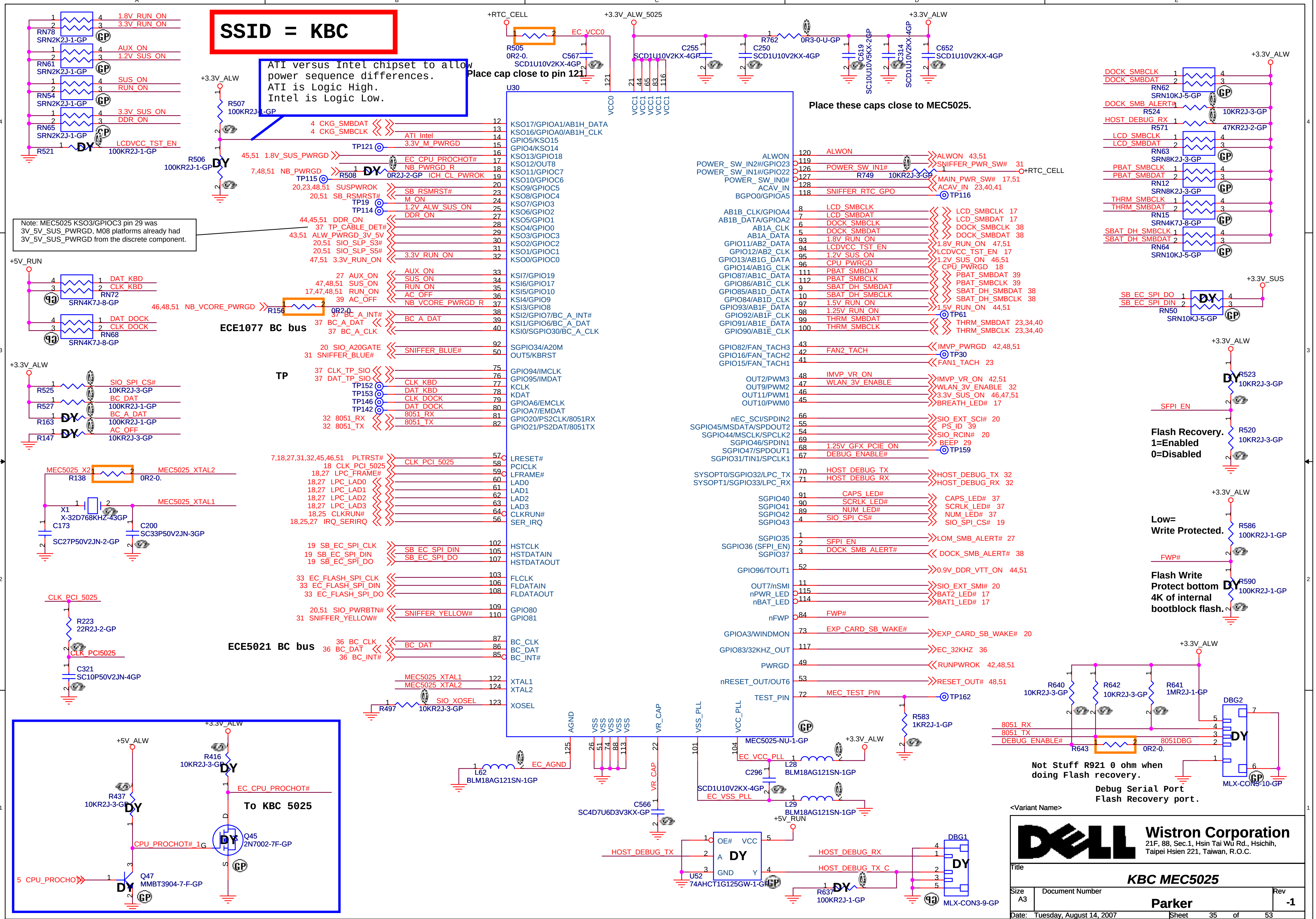


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: *KBC MEC5025*

Size	Document Number	Rev
A3	Parker	-1

Date: Tuesday, August 14, 2007 | Sheet 35 of 53

SSID = SIO

Board ID Straps

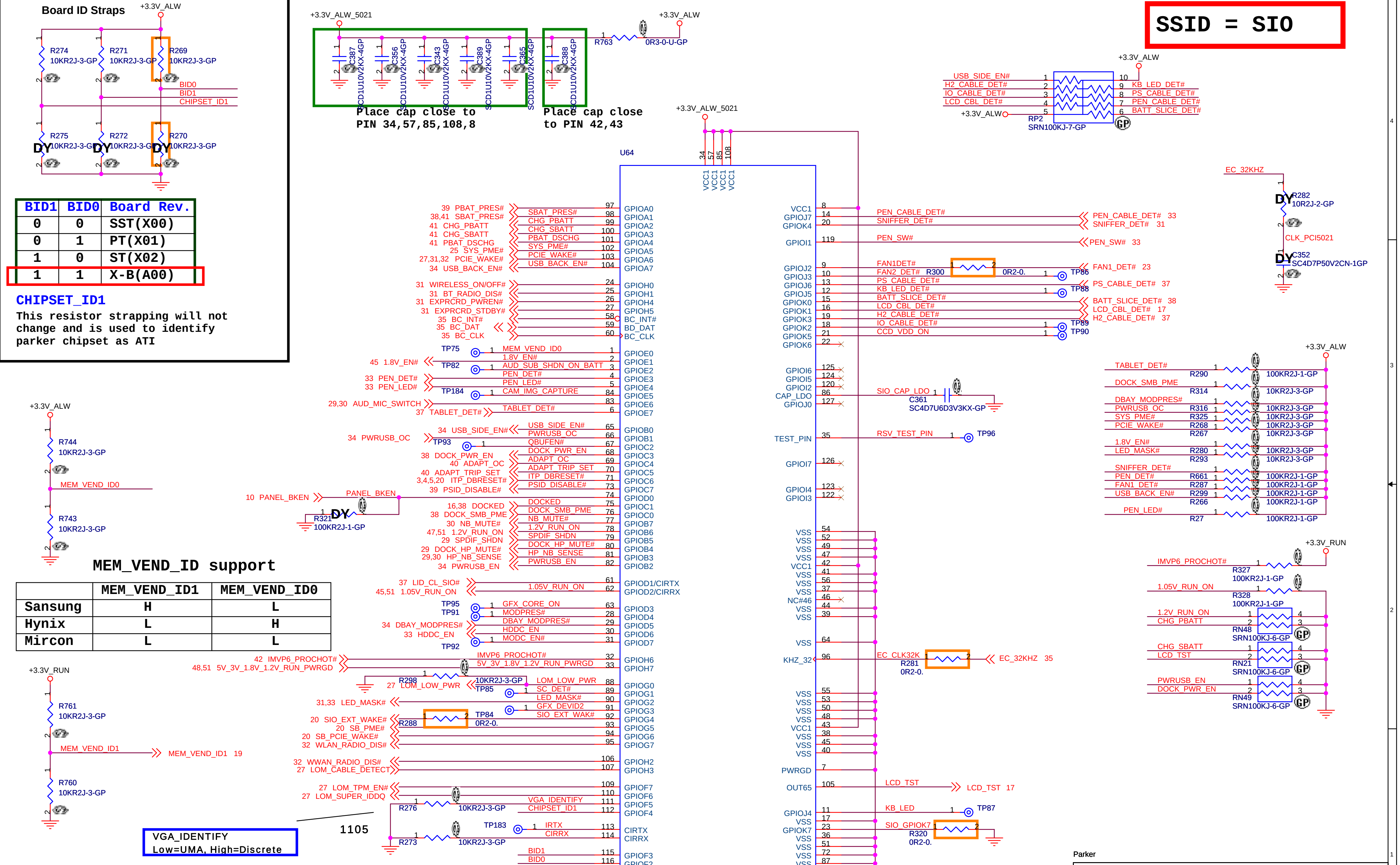
BID1	BID0	Board Rev.
0	0	SST(X00)
0	1	PT(X01)
1	0	ST(X02)
1	1	X-B(A00)

CHIPSET_ID1

This resistor strapping will not change and is used to identify parker chipset as ATI

MEM_VEND_ID support

	MEM_VEND_ID1	MEM_VEND_ID0
Sansung	H	L
Hynix	L	H
Mircon	L	L



Parker

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
SIO ECE5021		
Size A3	Document Number Parker	Rev -1
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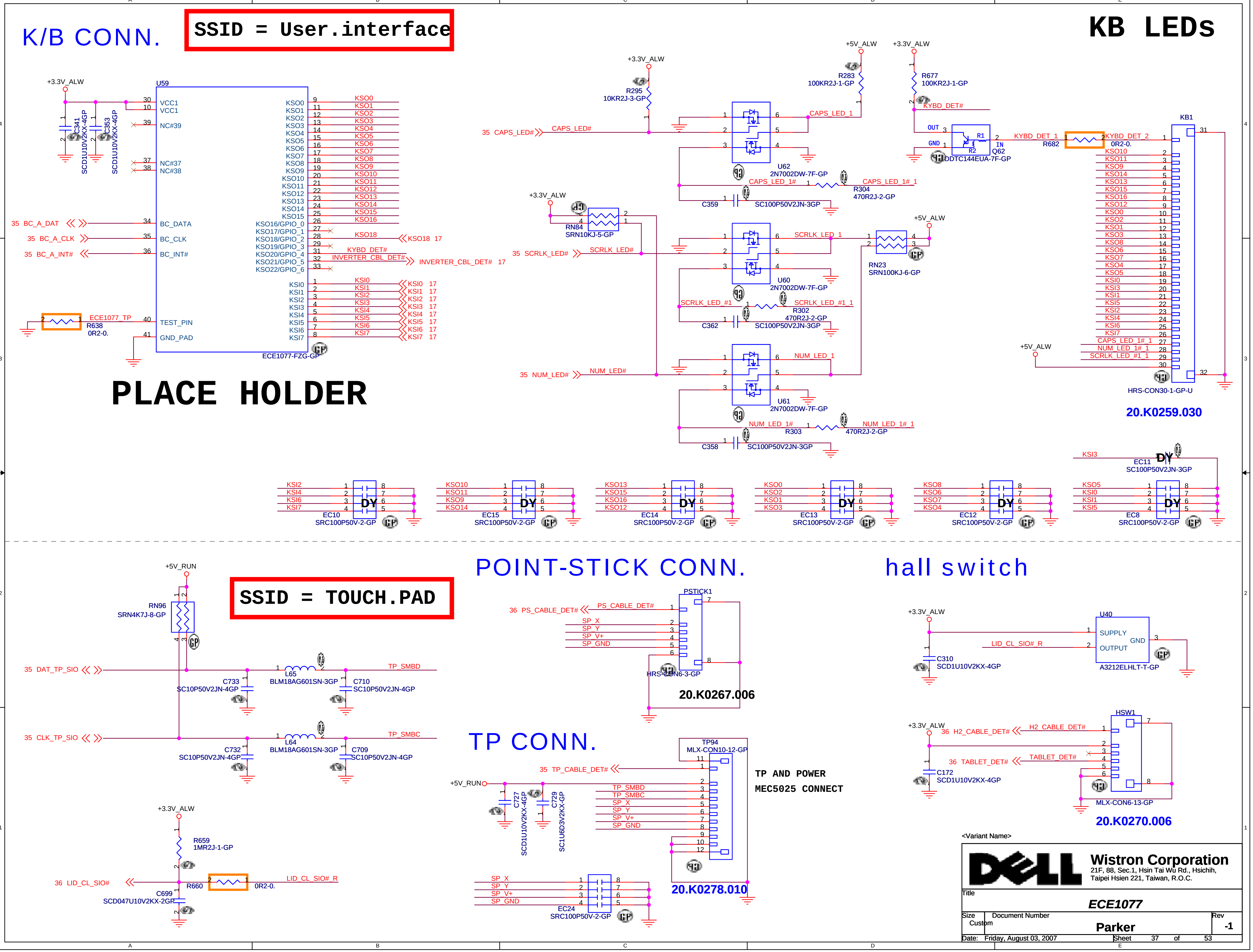

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ECE1077

Size: Custom | Document Number: Parker | Rev: -1

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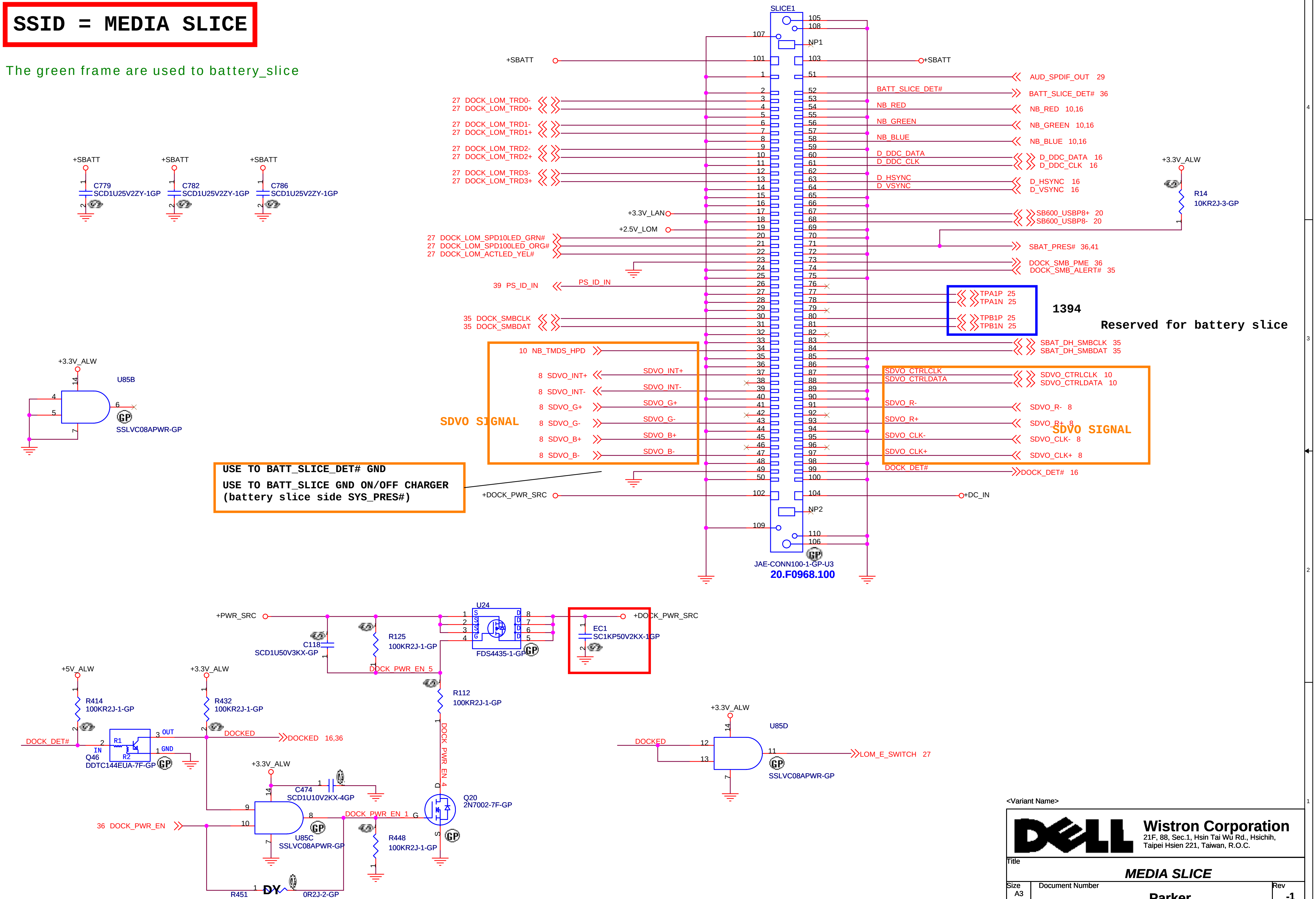
SSID = MEDIA SLICE

The green frame are used to battery_slice



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	MEDIA SLICE	
Size A3	Document Number Parker	Rev -1
Date: Friday, August 03, 2007	Sheet 38 of 53	

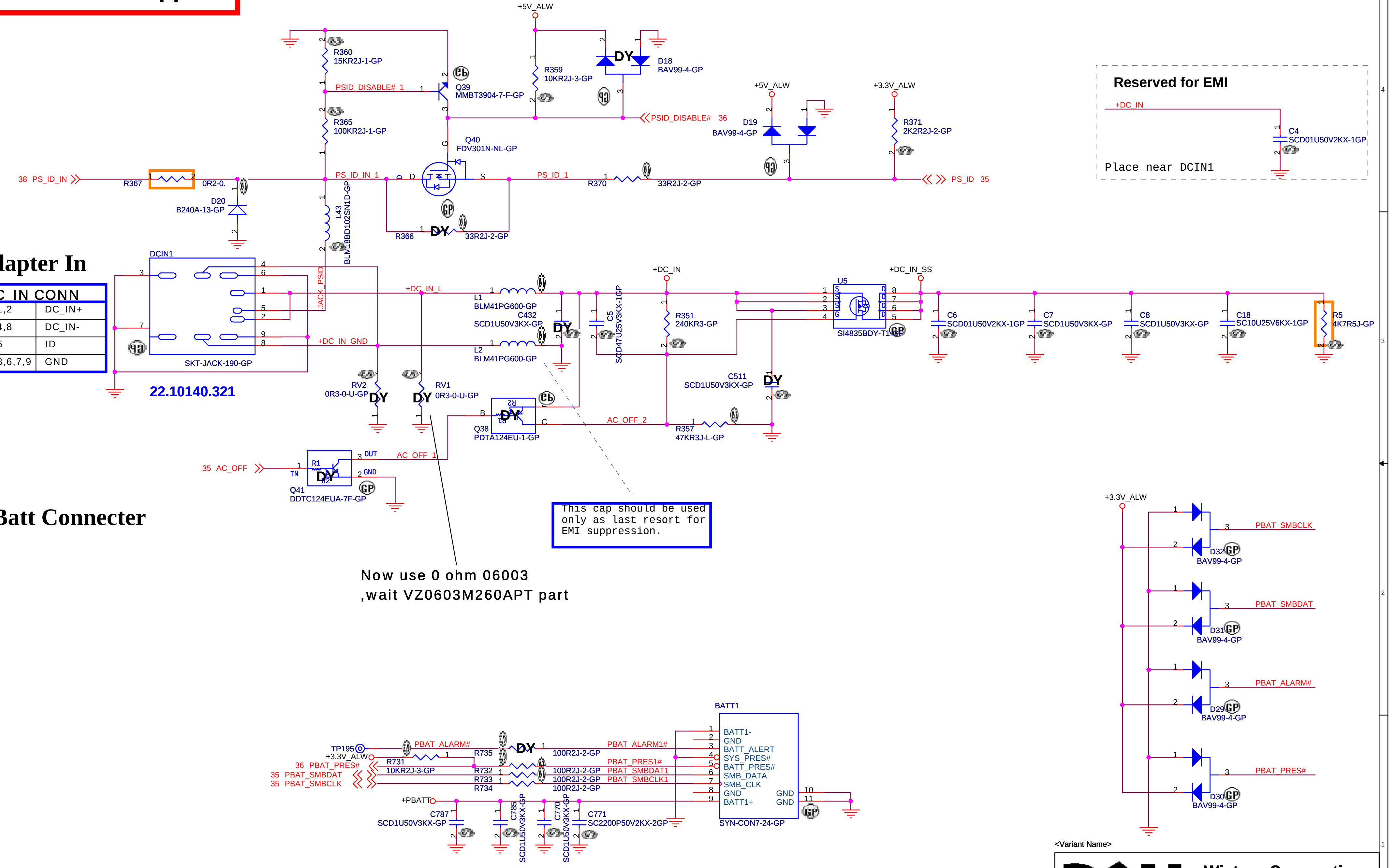
SSID = PWR.Support

Adapter In

DC IN CONN	
PIN 1,2	DC_IN+
PIN 4,8	DC_IN-
PIN 5	ID
PIN 3,6,7,9	GND

22.10140.321

Batt Connecter



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			
DCIN / BATT CONN.			
Size: A3	Document Number: Parker		Rev: -1
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SSID = CHARGER

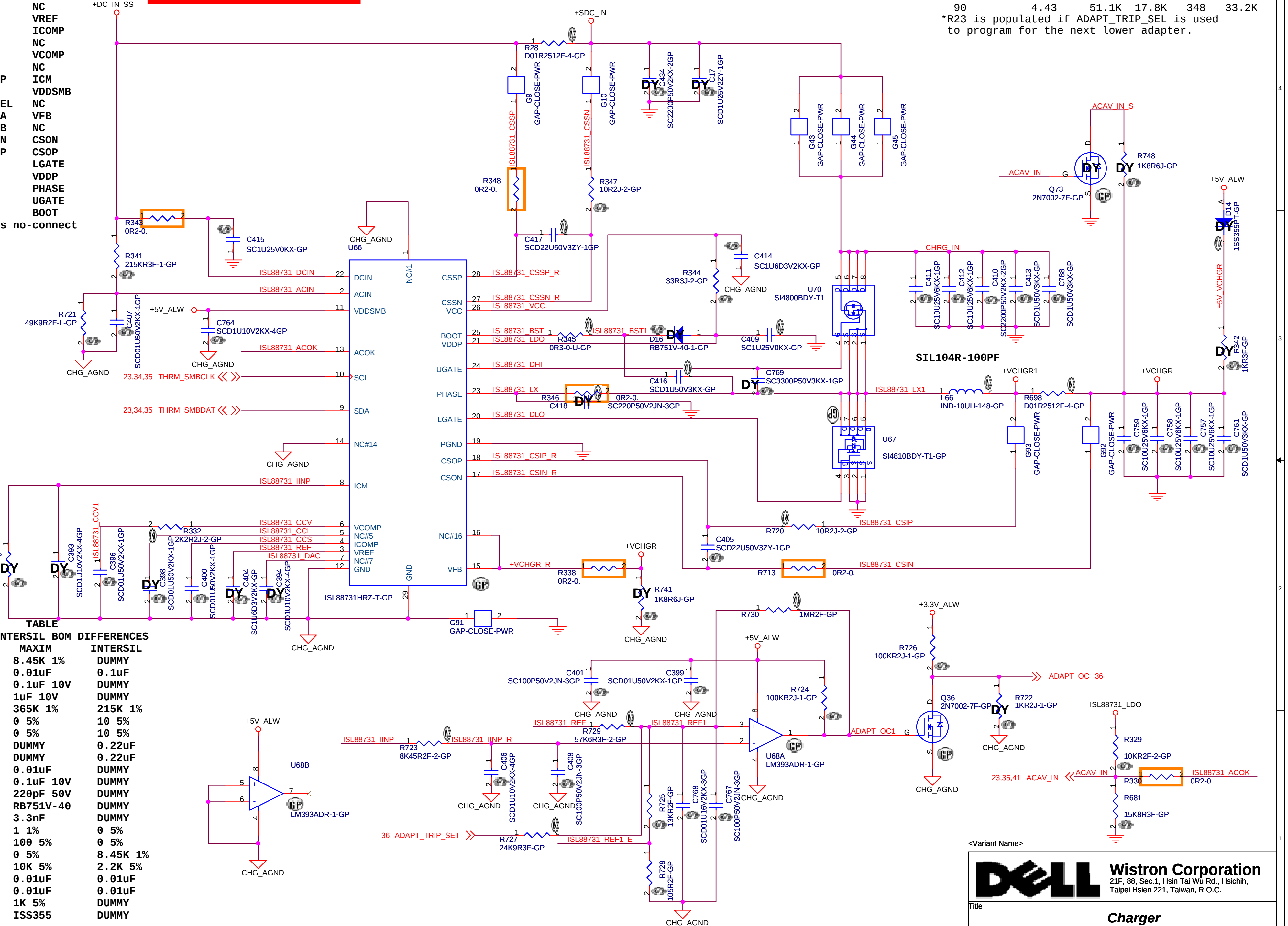
PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

Adapter (W)	Trip Current (A)	R1620	R1621	R1622	R1623
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R23 is populated if ADAPT_TRIP_SEL is used to program for the next lower adapter.



This Resistor must be 1% tolerance.

TABLE

MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL
R1610	8.45K 1%	DUMMY
C1412	0.01uF	0.1uF
C1404	0.1uF 10V	DUMMY
C1408	1uF 10V	DUMMY
R1602	365K 1%	215K 1%
R1609	0 5%	10 5%
R1601	0 5%	10 5%
C1402	DUMMY	0.22uF
C1388	DUMMY	0.22uF
C1406	0.01uF	DUMMY
C1409	0.1uF 10V	DUMMY
C1399	220pF 50V	DUMMY
D36	RB751V-40	DUMMY
C1398	3.3nF	DUMMY
R1607	1 1%	0 5%
R1612	100 5%	0 5%
R1759	0 5%	8.45K 1%
R1611	10K 5%	2.2K 5%
C1405	0.01uF	0.01uF
C1407	0.01uF	0.01uF
R1606	1K 5%	DUMMY
D35	ISS355	DUMMY

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger

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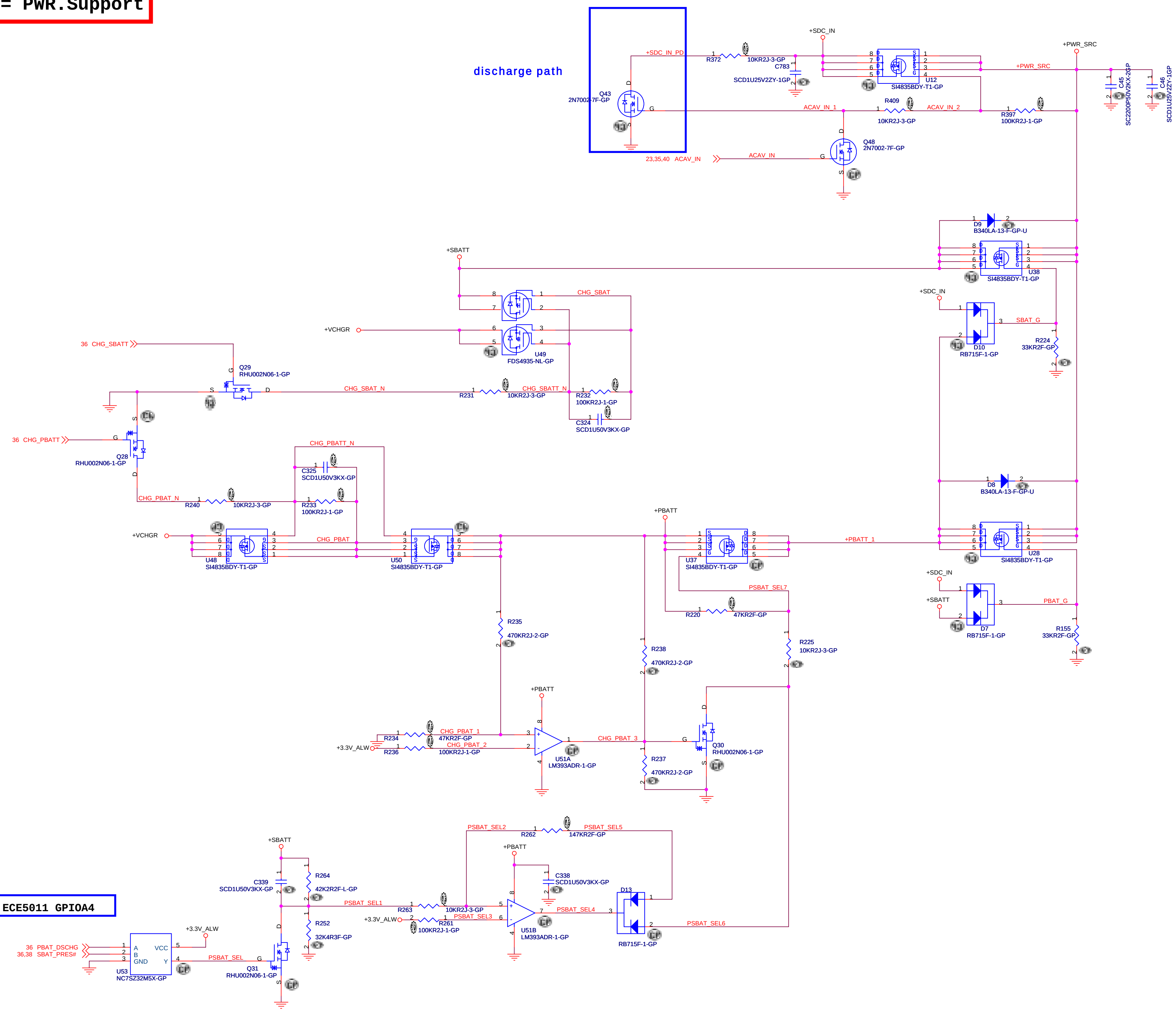
SSID = PWR.Support



In M07,use ECE5011 GPIOA4

<Variant Name>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BATTERY SELECT		
Size: A2	Document Number: Parker	Rev: -1
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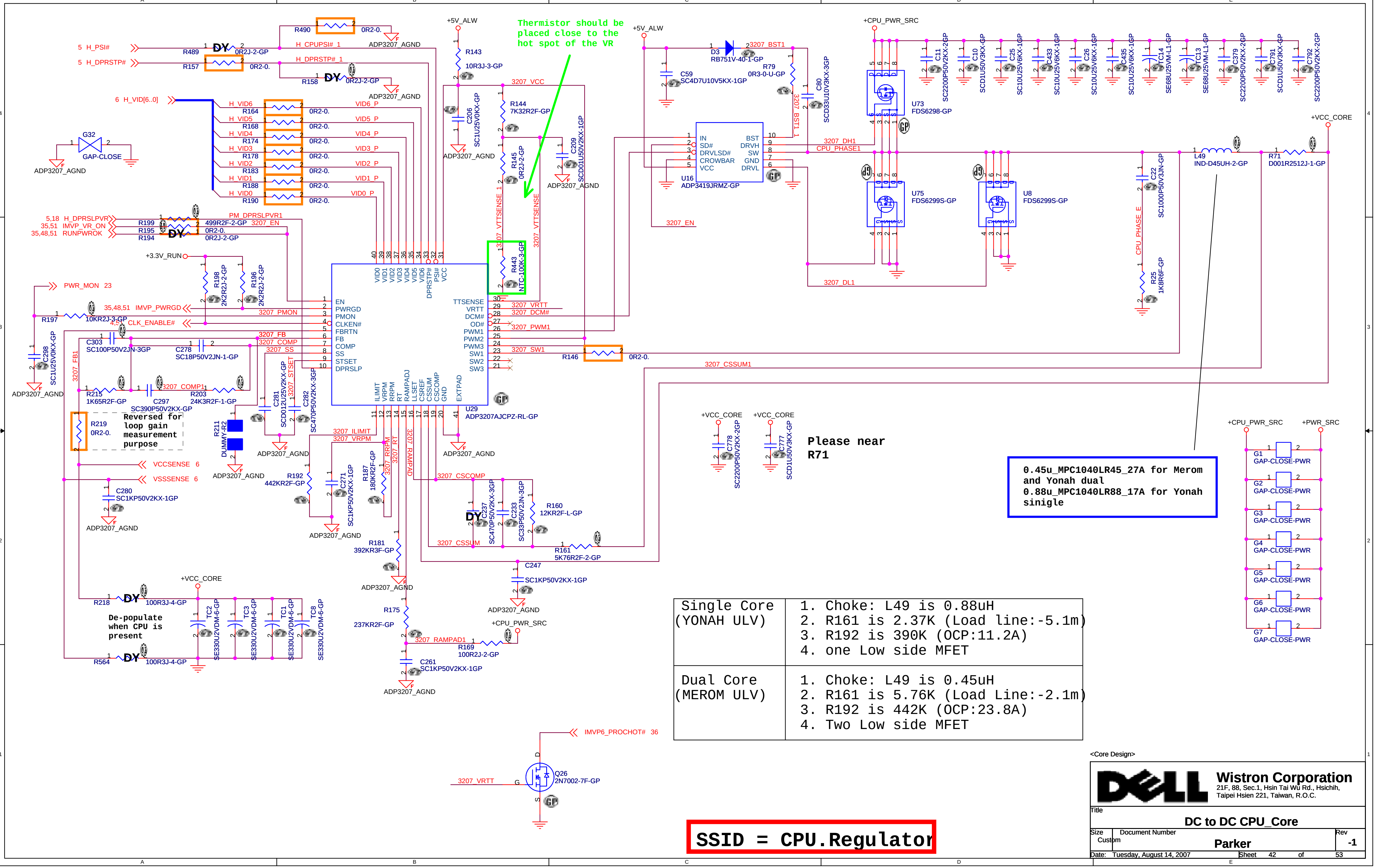

Single Core (YONAH ULV)	1. Choke: L49 is 0.88uH 2. R161 is 2.37K (Load line:-5.1m) 3. R192 is 390K (OCP:11.2A) 4. one Low side MFET
Dual Core (MEROM ULV)	1. Choke: L49 is 0.45uH 2. R161 is 5.76K (Load Line:-2.1m) 3. R192 is 442K (OCP:23.8A) 4. Two Low side MFET

SSID = CPU.Regulator

<Core Design>

Wistron Corporation
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Title: DC to DC CPU_Core

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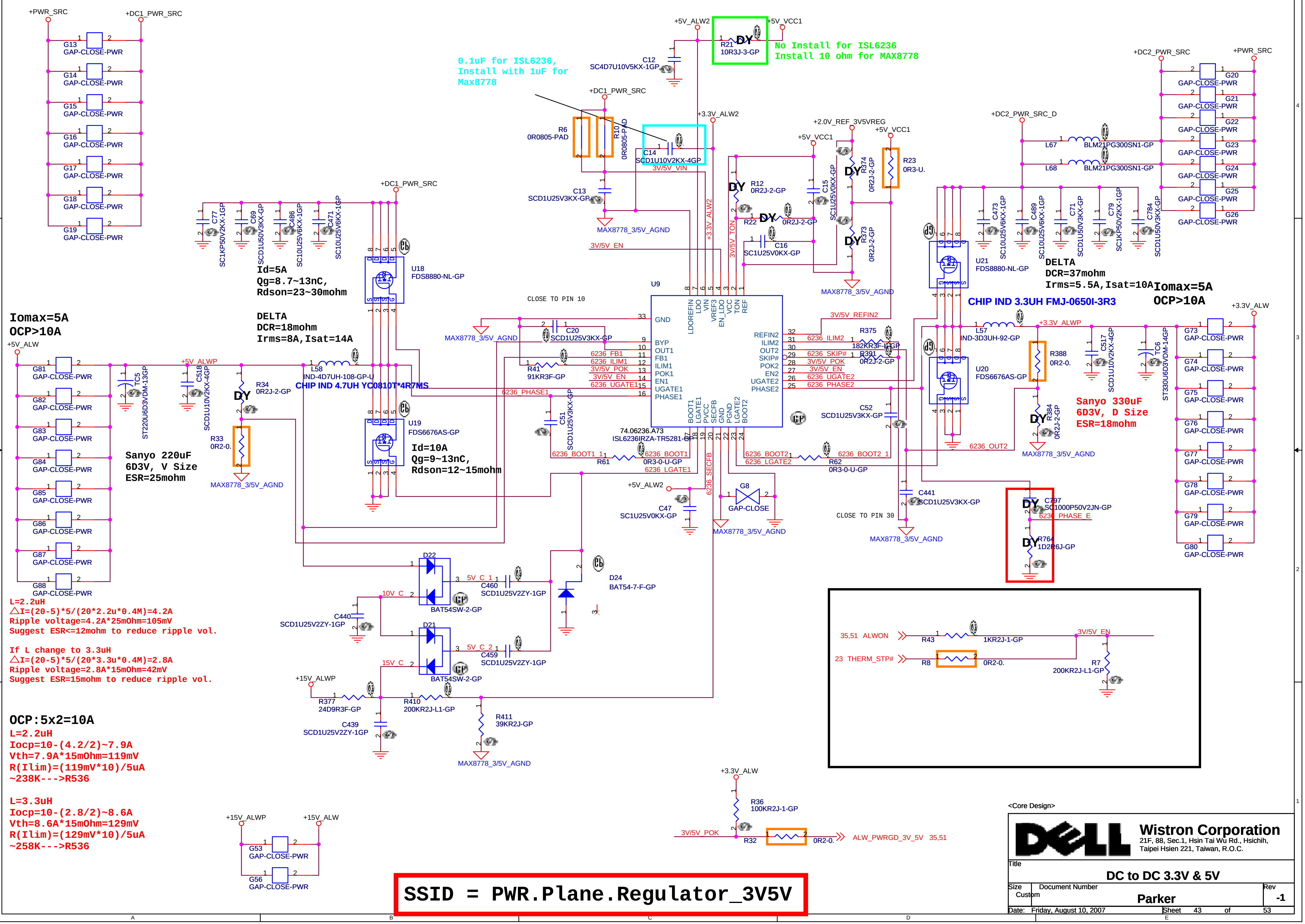

L=2.2uH
△I=(20-5)*5/(20*2.2u*0.4M)=4.2A
Ripple voltage=4.2A*25mOhm=105mV
Suggest ESR<=12mohm to reduce ripple vol.

If L change to 3.3uH
△I=(20-5)*5/(20*3.3u*0.4M)=2.8A
Ripple voltage=2.8A*15mOhm=42mV
Suggest ESR=15mohm to reduce ripple vol.

OCP:5x2=10A
L=2.2uH
Iocp=10-(4.2/2)~7.9A
Vth=7.9A*15mOhm=119mV
R(Ilim)=(119mV*10)/5uA
~238K--->R536

L=3.3uH
Iocp=10-(2.8/2)~8.6A
Vth=8.6A*15mOhm=129mV
R(Ilim)=(129mV*10)/5uA
~258K--->R536

SSID = PWR.Plane.Regulator_3V5V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 3.3V & 5V

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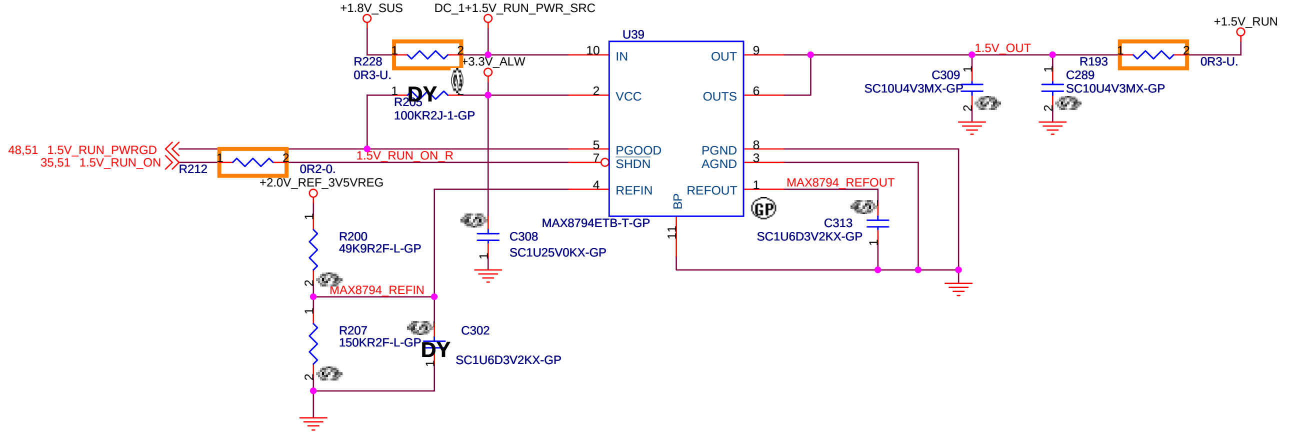
SSID = PWR.Plane.Regulator_1.5V

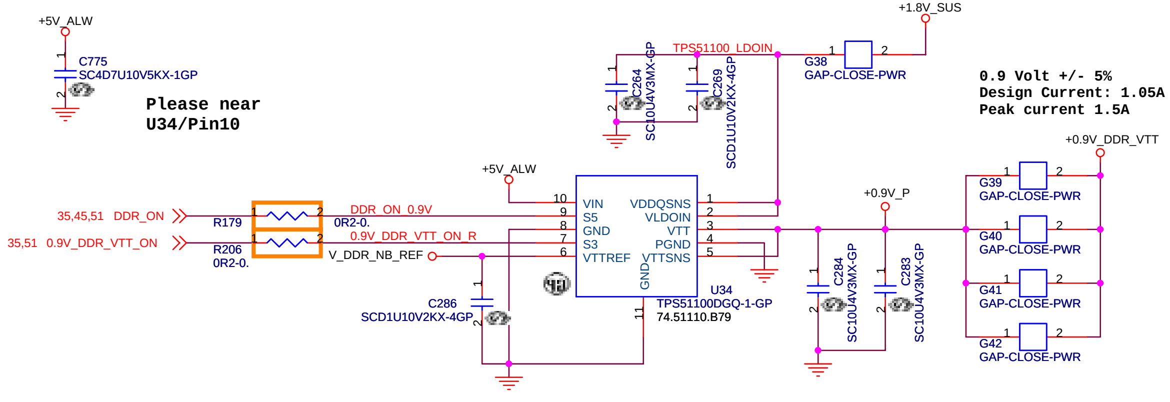
1.5V_RUN +/- 5%
Design Current: 0.9A
Peak current 1.28A



SSID = PWR.Plane.Regulator_0.9V

Please near U34/Pin10

0.9 Volt +/- 5%
Design Current: 1.05A
Peak current 1.5A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	DC to DC 1D5V / 0D9V	
Size: A3	Document Number: Parker	Rev: -1
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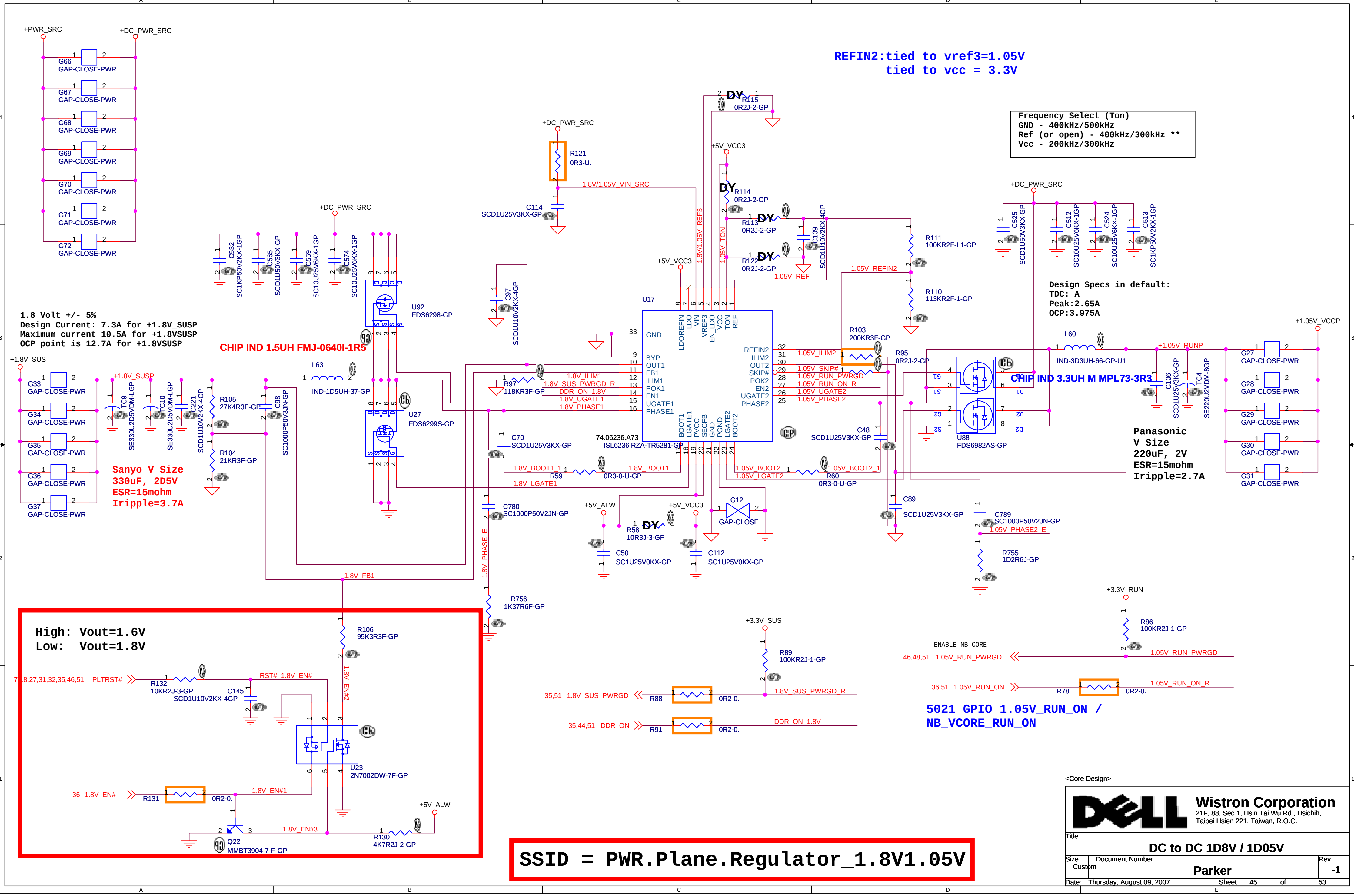
REFIN2:tied to vref3=1.05V
tied to vcc = 3.3V
Frequency Select (Ton)
GND - 400kHz/500kHz
Ref (or open) - 400kHz/300kHz **
Vcc - 200kHz/300kHz
1.8 Volt +/- 5%
Design Current: 7.3A for +1.8V_SUSP
Maximum current 10.5A for +1.8VSUSP
OCP point is 12.7A for +1.8VSUSP
CHIP IND 1.5UH FMJ-0640I-1R5
Design Specs in default:
TDC: A
Peak:2.65A
OCP:3.975A
CHIP IND 3.3UH M MPL73-3R3
Sanyo V Size
330uF, 2D5V
ESR=15mohm
Iripple=3.7A
Panasonic
V Size
220uF, 2V
ESR=15mohm
Iripple=2.7A
U17
74.06236.A73
ISL6236IRZA-TR5281-GP
U92 FDS6298-GP
U27 FDS6299S-GP
U88 FDS6982AS-GP
U23 2N7002DW-7F-GP
Q22 MMBT3904-7-F-GP
L63 IND-1D5UH-37-GP
L60 IND-3D3UH-66-GP-U1
+PWR_SRC
+DC_PWR_SRC
+1.8V_SUS
+1.05V_VCCP
+5V_VCC3
+5V_ALW
+3.3V_SUS
+3.3V_RUN
High: Vout=1.6V
Low: Vout=1.8V
7,18,27,31,32,35,46,51 PLTRST#
36 1.8V_EN#
35,51 1.8V_SUS_PWRGD
35,44,51 DDR_ON
46,48,51 1.05V_RUN_PWRGD
36,51 1.05V_RUN_ON
ENABLE NB CORE
5021 GPIO 1.05V_RUN_ON /
NB_VCORE_RUN_ON
SSID = PWR.Plane.Regulator_1.8V1.05V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC to DC 1D8V / 1D05V
Size Custom
Document Number
Parker
Rev -1
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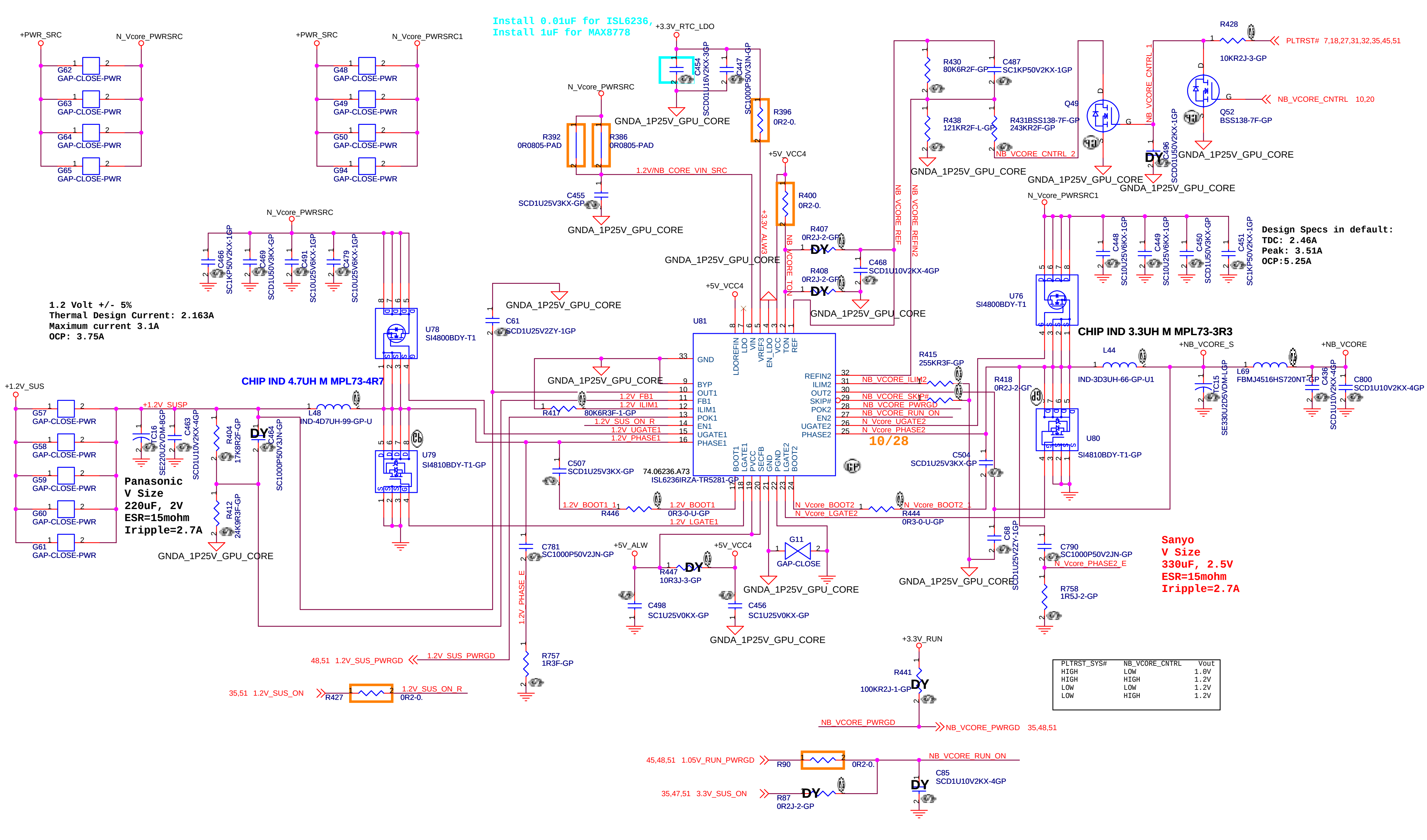

PLTRST_SYS#	NB_VCORE_CNTRL	Vout
HIGH	LOW	1.0V
HIGH	HIGH	1.2V
LOW	LOW	1.2V
LOW	HIGH	1.2V

SSID = PWR.Plane.Regulator_1.2V.NB_VCORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D2V / NB_Core

Size: Custom | Document Number: Parker | Rev: -1

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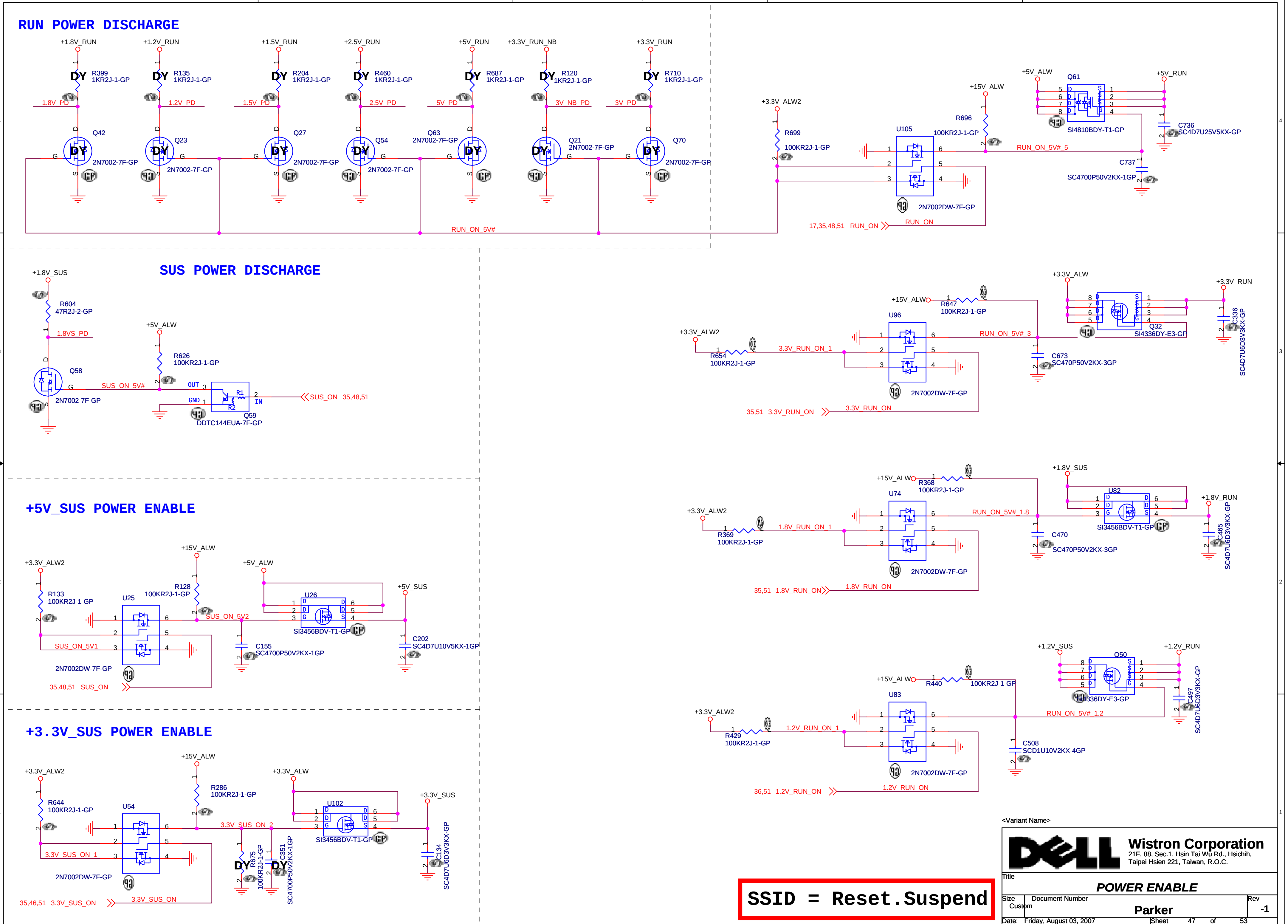

SSID = Reset.Suspend

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER ENABLE	
Size Custom	Document Number Parker	Rev -1
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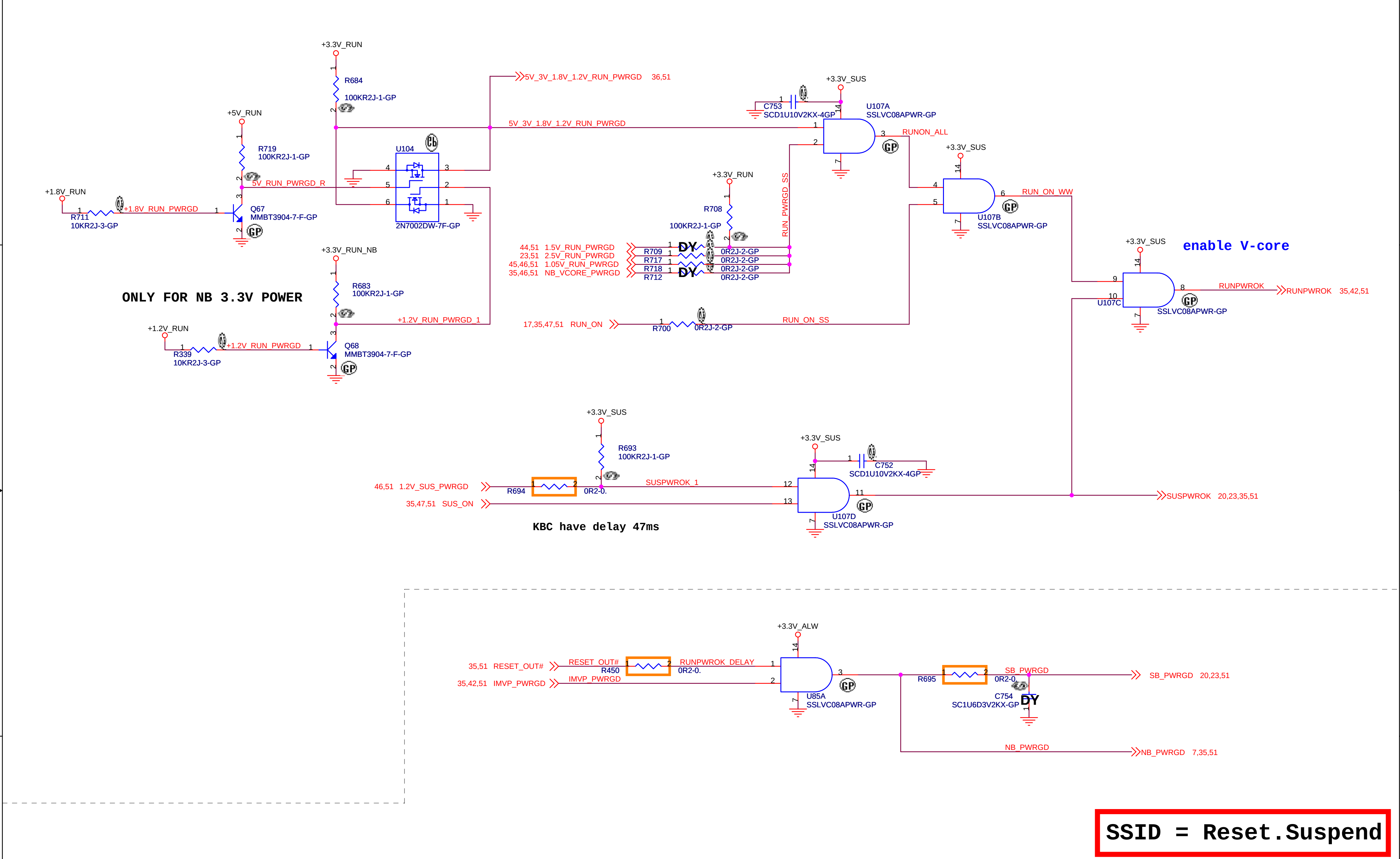

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
POWER ON LOGIC

Size	Document Number	Rev
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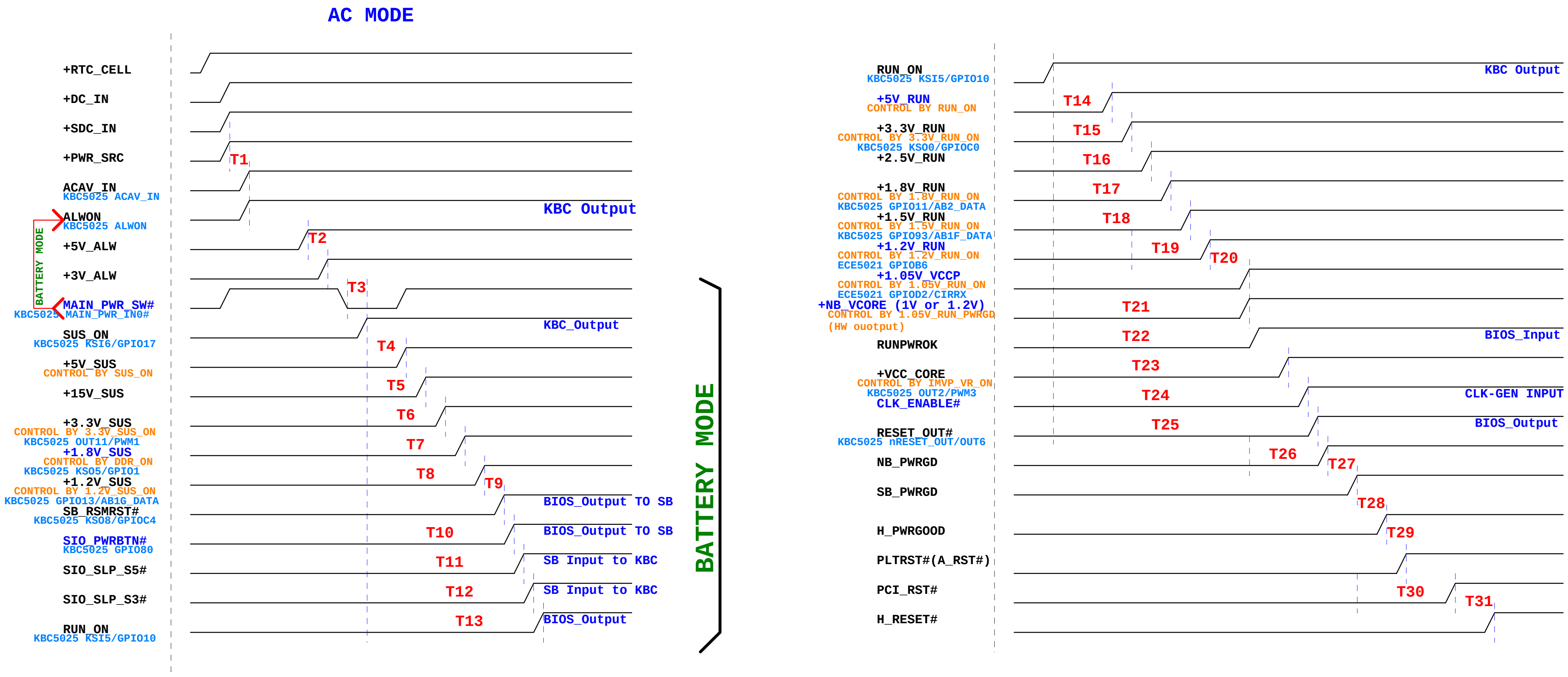
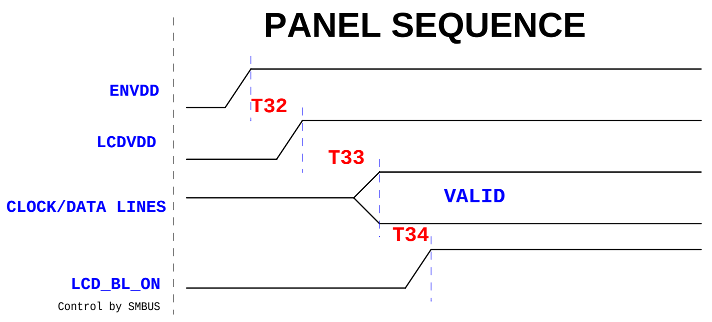
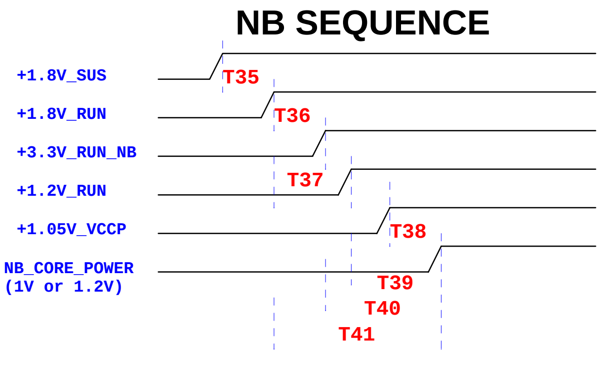
DP2 PLATFORMS POWER UP







<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
POWER ON SEQUENCE		
Size: Custom	Document Number: Parker	Rev: -1
Date: Friday, August 03, 2007	Sheet 49 of 53	

Power

Signal Name	Test Position	Signal Name	Test Position
+DC_IN	U5.1;Page 39	GFX_PWR_SRC	U10.1;Page 17
+DC_IN_SS	U5.8;Page 39	+RTC_CELL	C266.1;Page 18
+SDC_IN	U12.8;Page 41	VCC_RUN_SB	L31.1;Page 18
+VCHGR	U48.8;Page 41	VCC_SB_PVDD	C315.1;Page 18
+PBATT	U37.1;Page 41	VCC_SB_VDDR	C245.1;Page 18
+SBATT	U38.8;Page 41	SB_AVDDCK1.2	C181.1;Page 21
+DOCK_PWR_SRC	U24.8;Page 38	+3.3V_RUN_HW	C275.1;Page 19
+PWR_SRC	U12.1;Page 41	+3.3V_SB_USB_TX	C156.1;Page 20
+VCC_CORE	TC2.1;Page 42	+3.3V_SB_USB_RX	C183.1;Page 20
+15V_ALW	R696.1;Page 47	+3.3V_SB_AVDDC	C135.1;Page 20
+5V_ALW	R413.1;Page 18	+SB_AVDDCK3.3	C182.1;Page 21
+3.3V_ALW	U11.1;Page 17	SB_5V_REF	C620.1;Page 21
+3.3V_ALW2	C14.2;Page 43	+2.5V_RUN	C552.1;Page 23
+1.5V_RUN	R193.2;Page 44	THERMAL_LDO_IN	C553.1;Page 23
+0.9V_DDR_VTT	C718.1;Page 15	+3.3V_PCI7402_AVDD	C348.1;Page 24
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+1.8V_RUN	U82.6;Page 47	+2.5V_XTALVDD	L53.1;Page 27
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+1.8V_RUN_NB_AVDDD	C88.1;Page 10	+3.3V_WLAN	U98.6;Page 32
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+3.3V_RUN_NB_VDDR33	C66.1;Page 10		
+3.3V_RUN_NB_VDDLT33	C130.1;Page 10		
+3.3V_RUN_NB	U22.6;Page 10		
+1.8V_RUN_NB_VDD18CPU	C115.1;Page 11		
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Power Sequence

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+DC_IN	U5/1 ; Page 41	RUNPWROK	U107/8 ; Page 48
+SDC_IN	U12/8 ; Page 41	+VCC_CORE	TC2/1 ; Page 42
+PWR_SRC	U12/1 ; Page 41	CLK_ENABLE#	R572/1 ; Page 4
ACAV_IN	R329/2 ; Page 40	RESET_OUT#	U30/53 ; Page 35
ALWON	R43/1 ; Page 43	NB_PWRGD	R695/1 ; Page 48
+3.3V_ALW	C314/1 ; Page 35	SB_PWRGD	R695/2 ; Page 48
+5V_ALW	Q61/5 ; Page 47	H_PWRGOOD	R568/2 ; Page 5
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SUS_ON	U30/34 ; Page 35	PCI_RST#	R621/2 ; Page 18
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+3.3V_RUN	Q32/1 ; Page 47		
+2.5V_RUN	R460/1 ; Page 47		
+1.8V_RUN	U82/4 ; Page 47		
+1.5V_RUN	R193/2 ; Page 44		
+1.2V_RUN	Q50/1 ; Page 47		
+1.05V_VCCP	R108/2 ; Page 7		

<Variant Name>

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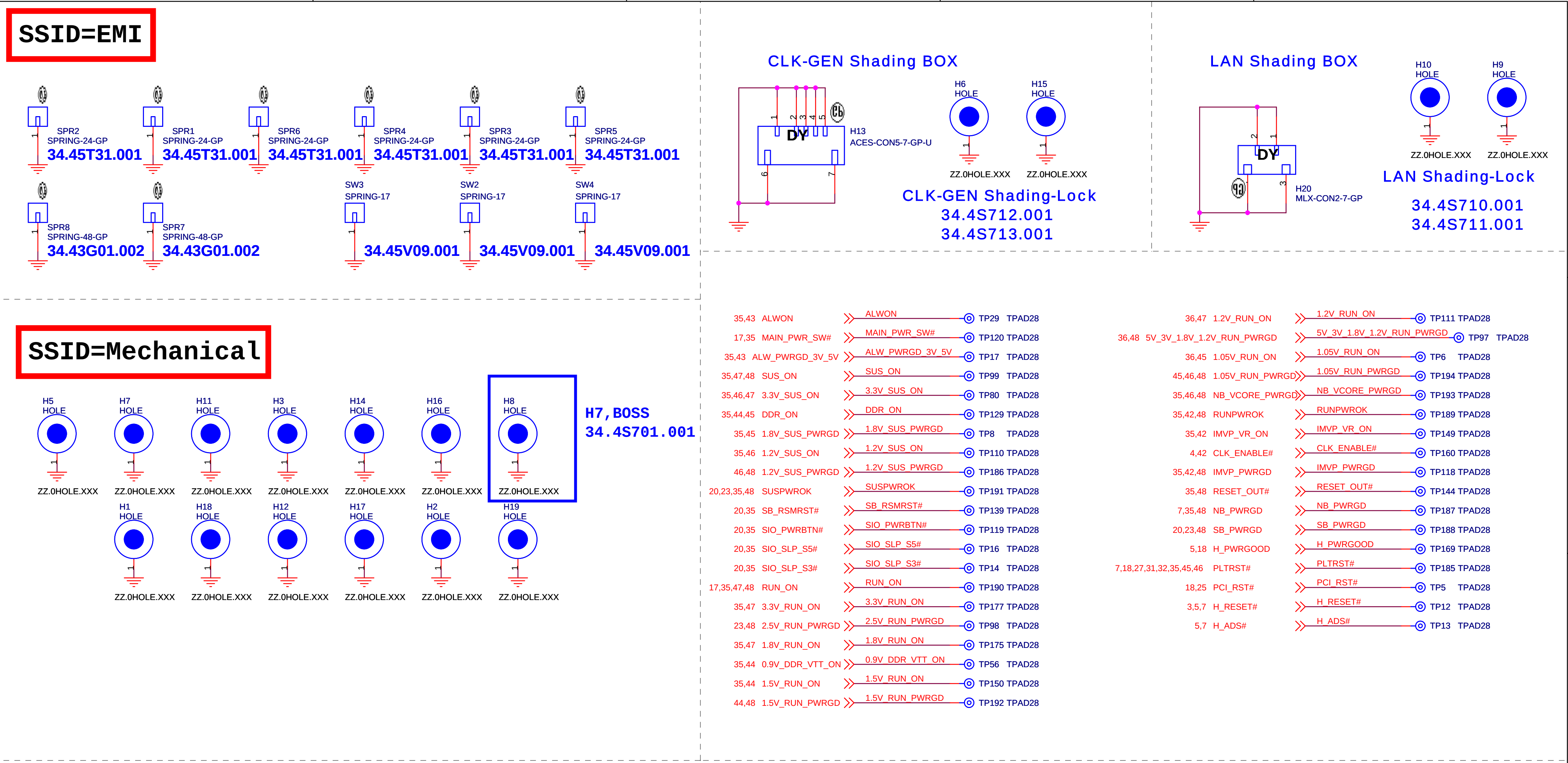

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/11/03	X00	1	18	REMOVE DVI CHIP TO MEDIA SLICE SIDE	Change SPEC	EE
2007/03/21	X01	2	3	Dummy ITP1		EE
		3	4	Add R616,R617, Dummy R607,R610	Ext Clock Frequency select to 133MHz	EE , SW
		4	4	Change R221,R595 to 15 ohm , RN14 to 22 ohm	EA report fail issues	EE
		5	8	Change PCI-E GPP_TX	PCI-E GPP error	EE
		6	10	Add R742 10K ohm in NB_TMDS_HPD_R	BIT issues	EE
		7	11	Change +1.8V_RUN_NB_VDD18MEN TO +1.8V_RUN_NB_VDD18MEM	BIT issues	EE
		8	12	Change R629,R630,R632,R633 to 0 ohm and Add R736,R737 100 ohm	DDR clock driver issues	EE
		9	13	Change Onboard memory to Hynix and Mircon	Sansung memory can't support issues	EE
		10	16	Change L37, L38, L39, L40, L41 to BLM18BA100SN1D	EA report fail issues	EE
		11	17	Change R47 to 150 ohm	EA report fail issues	EE
		12	17	Change LVDS1 Power circuit	LCD Power issues	EE
		13	19	Add R738,R739,R740 0 ohm connect SATA power and GND	No support SATA HDD issues	EE
		14	19	Add C776 22pF De-pop and Change R445,R514,R529 to 47 ohm	SPI ROM issues	RF
		15	20	Change Memory SMBus support to SB SMBus 0 and Del U101,RN58	Memory controller issues	SW
		16	20	Del L23 and Change AVDDRX power to +3.3V_SB_USB_TX	ATI Desgin check issues	EE
		17	25	Change signal IRQ_SERIRQ to U63/Pin H1;Change U63/Pin H2 to signal MFUNC2	TI multi function setting issues	EE , SW
		18	25	Change C385,C386 to 12PF	Crytal result issues	EE
		19	26	Change R260,R265,R294,R305 to 200 ohm , R291 to 75 ohm	SDIO Rise time fall issues	EE
		20	27	Change C510 to 33PF	Crytal result issues	EE
		21	27	Change R420 to 1.18K ohm	LOM Driver issues	EE
		22	29	Change U31/Pin 4 AUD_SPK_DET signal to U35/Pin P8	Audio detect issues	SW
		23	30	Change U32 to TI TPA6040A4 and setting	AMP Main source change issues	EE
		24	30	Change U40/Pin 5 Power to +3.3V_RUN	BIT issues	EE
		25	30	Change C446, C453 to 1uF 25V 0603	Audio issues	EE
		26	32	Swap ESD1 and De-pop C369, C377	WWAN's SIM error	EE
		27	32	Change U98 to Vishay SI3424DV	WLAN Power issues	Power
		28	33	Change R548,R573 to 0 ohm , R575 to 47 ohm and Add C772,C773, C774 22pF De-pop	SPI ROM issues	EE
		29	35	Dummy DBG1, DBG2		EE
		30	35	Change R641 to 1M ohm	BIT issues	EE
		31	35	Change RN54,RN61,RN65,RN78 to 2.2K ohm	SUS and RUN power open two time issues	EE , SW
		32	35	Change C173 to 12PF ,C200 to 15PF	Crytal result issues	EE
		33	35	De-pop R321	BIT issues	EE
		34	35	Add R749 10K ohm to +RTL_CELL	Pen switch issues	EE , SW
		35	36	Add R269 10K ohm, Dummy R270	Board ID issues	EE , SW
		36	36	Add MEM_VEND_I Detect in U64 Pin 1	Memory controller for SPD issues	SW
		37	36	Change U64 Pin 7 signal connect GND	BIT issues	EE
		38	36	Add PEN_SW# connector to U64/Pin 119	Pen switch issues	EE , SW
		39	37	Change KB1 signal	Keyboard issues	EE , KBC
		40	37	Change LID_CL_SIO#_R to U40/Pin 2 , TABLET_DET# to HSW1/Pin 4	Hall switch support change issues	ME
		41	38	Change U85 power source to +3.3V_ALW	BIT issues	EE
		42	38	Add DOCKED signal use U85 to LOM and Change U86/Pin E3 signal to LOM_E_SWITCH	LOM Docking switch issues	EE
		43	40	Add 1K8 ohm 1206 De-pop in +VCHGR to GND	BIT issues	EE
		44	43	Change TC5 to 220U6D3V	BIT issues	EE
		45	44	Add C775 near U34/Pin 10	BIT issues	EE
		46	45	Change L63 to IND-1D5UH , TC9,TC10 to SE330U2D5VVD , R97 to 118K , R103 to 93.1K	Power issues	Power
		47	46	Change R417 to 80.6K ohm , R415 to 255K ohm , TC15 to 330U2D5V	Power issues	Power
		48	48	Change R695 to 0 ohm , Del R666, C730	Power sequence issues	Power
		49		Change Power use Gap to Clise Gap		Power

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/06/25	X02	1	4	Del C570,582,585,592,595,604,606,609,611,622	RF noise issues	RF
		2	4	Change C615,623,635 to 15pF	RF noise issues	RF
		3	11	Change C116,147,176 to 6pF, C72,231,240 to 0.1uF and ADD C801 22uF	RF noise issues	RF
		4	13	Add C802,803,804 to 4.7uF	+1.8_SUS, +0.9V_DDR_VTT, V_DDR_NB_REF ripple issues	EE
		5	17	Change C563 to Dummy	Power switch issues	EE
		6	17	Add R752 10K ohm	Cable detect setting issues	SW
		7	17	Change LCD Lunch Board Power support	Digitizer Power support	EE
		8	17	Change R98,101,701 to 470 ohm	Battery life issues	EE
		9	18	Add R753 10K ohm	Cable detect setting issues	SW
		10	19	Change Net LBF_ID0 to MEM_VEND_ID1	Onboard memory vendor support issues	EE,SW
		11	20	Change R478,479 to 10 ohm, C533,535 to 4.7pF	EMI issues	EMI
		12	22	Add SB power delay circuit	ATI power issues	EE
		13	25	Change R631 to 22 ohm, R636 to 10 ohm, C654 to 10pF and C667 to 4.7pF	EMI issues	EMI
		14	27	Add R485 0 ohm	Cable detect setting issues	SW
		15	27	Change R462 to 22 ohm and C527 to 4.7pF	EMI issues	EMI
		16	28	Change R383 to 0 ohm and L45 to Dummy	EMI issues	EMI
		17	30	Add R754 10K ohm	Cable detect setting issues	SW
		18	31	Change R308,309 to 470 ohm	Battery life issues	EE
		19	32	Add +1.5V_RUN_WLAN switching circuit	Power switch issues	EE
		20	33	Change R18,19 and C9 to Dummy	Pen detect setting issues	SW
		21	34	Add C793,794,795,796 EMI Capacitor Pad and D15,23,26 EMI Diode	EMI issues	EMI
		22	35	Add R762 0 ohm	RF noise issues	RF
		23	35	Change Net AC_OFF ti pull down	AC_OFF setting issues	EE,SW
		24	35	Change R223 to 22 ohm and C321 to 10pF	EMI issues	EMI
		25	36	Change Board ID to X02	Board ID setting issues	SW
		26	36	Add R763 0 ohm	RF noise issues	RF
		27	37	Change R302,303 and 304 to 470 ohm	Battery life issues	EE
		28	37	Change R682 to 0 ohm	Cable detect setting issues	SW
		29	38	Add C779,782 and 786 0.1uF	RF noise issues	RF
		30	39	Add C511,785 and 787 0.1uF	RF noise issues	RF
		31	40	Change L66 part to SIL104R	Charge issues	POWER
		32	40	Add C788 to 0.1uF	RF noise issues	RF
		33	40	Add ACAV_IN detect circuit	ACAV_IN setting issues	SW
		34	42	Change C297 to 390pF, R203 to 24.3K ohm, R192 to 442K ohm, R175 to 237K ohm and C233 to 33pF	CPU power issues	POWER
		35	42	Add C777,791 0.1uF, C22,379,778,792 2200pF and R25 1 ohm	RF noise issues	RF
		36	43	Change C77,79 to 1000pF and Add C784 0.1uF	RF noise issues	RF
		37	43	Add L67,68 30 ohm Bead	RF noise issues	RF
		38	45	Change C513,532 to 1000pF and Add C780,789 1000pF, R755,756 1.2 ohm	RF noise issues	RF RF
		39	46	Add L69 60 ohm	RF noise issues	RF
		40	46	Change C451,466 to 1000pF and Add C781,790 1000pF, R757,758 1 ohm	RF noise issues	RF
		41				
		42				
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