

Berry Discrete/UMA Schematics Document

AMD Danube CPU S1g4

AMD GPU Madison-LP/M96-LP M2

RS880M + SB820M

2010-03-08

REV : A00

DY : Nopop Component

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A4

Document Number

Berry AMD Discrete/UMA

Rev

A00

Date: Monday, March 08, 2010

Sheet

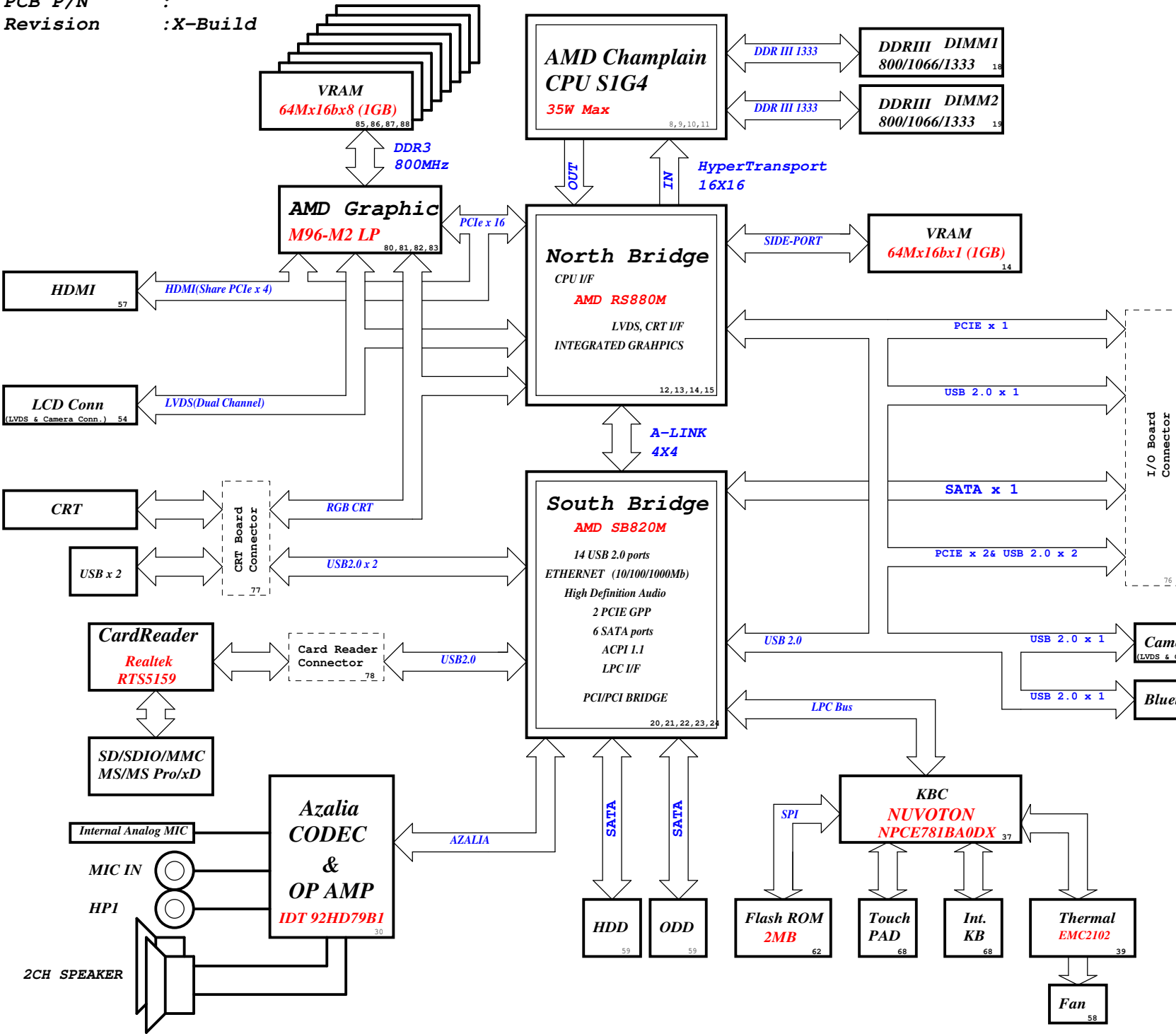
1

of

95

Berry DG15 Discrete/UMA Block Diagram

Project code : 91.4HH01.001
 PCB P/N :
 Revision : X-Build



CHARGER	
BQ24745	45
INPUTS	OUTPUTS
+DC_IN_SS	+PWR_SRC
+VCHGR	
SYSTEM DC/DC	
RT8205B	
46	
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_RTC_LDO
	+5V_ALW
	+3.3V_ALW
CPU VDDR	
RT9025	
48	
INPUTS	OUTPUTS
+1.5V_SUS	+CPU_VDDR
CPU CORE	
ISL6265AHRZ-T-GP	
47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
	+VDDNB
AMD RS880M CORE	
RT8209	
50	
INPUTS	OUTPUTS
+PWR_SRC	+NB_VDDC
AMD SB820M S5 POWER	
RT9025	
48	
INPUTS	OUTPUTS
+3.3V_ALW	+1.1V_ALW
DDR III SUS&VTT	
RT8207	
49	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS
DDR III SUS&VTT	
RT8207	
49	
INPUTS	OUTPUTS
+PWR_SRC	+0.75V_DDR_VTT
AMD GPU CORE	
RT8208B	
89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE
PCB LAYER	
L1: Top	
L2: VCC	
L3: Signal	
L4: Signal	
L5: GND	
L6: Bottom	

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Title: **Block Diagram**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet 2 of 95	

mailto:kevin.f@hotmail.com

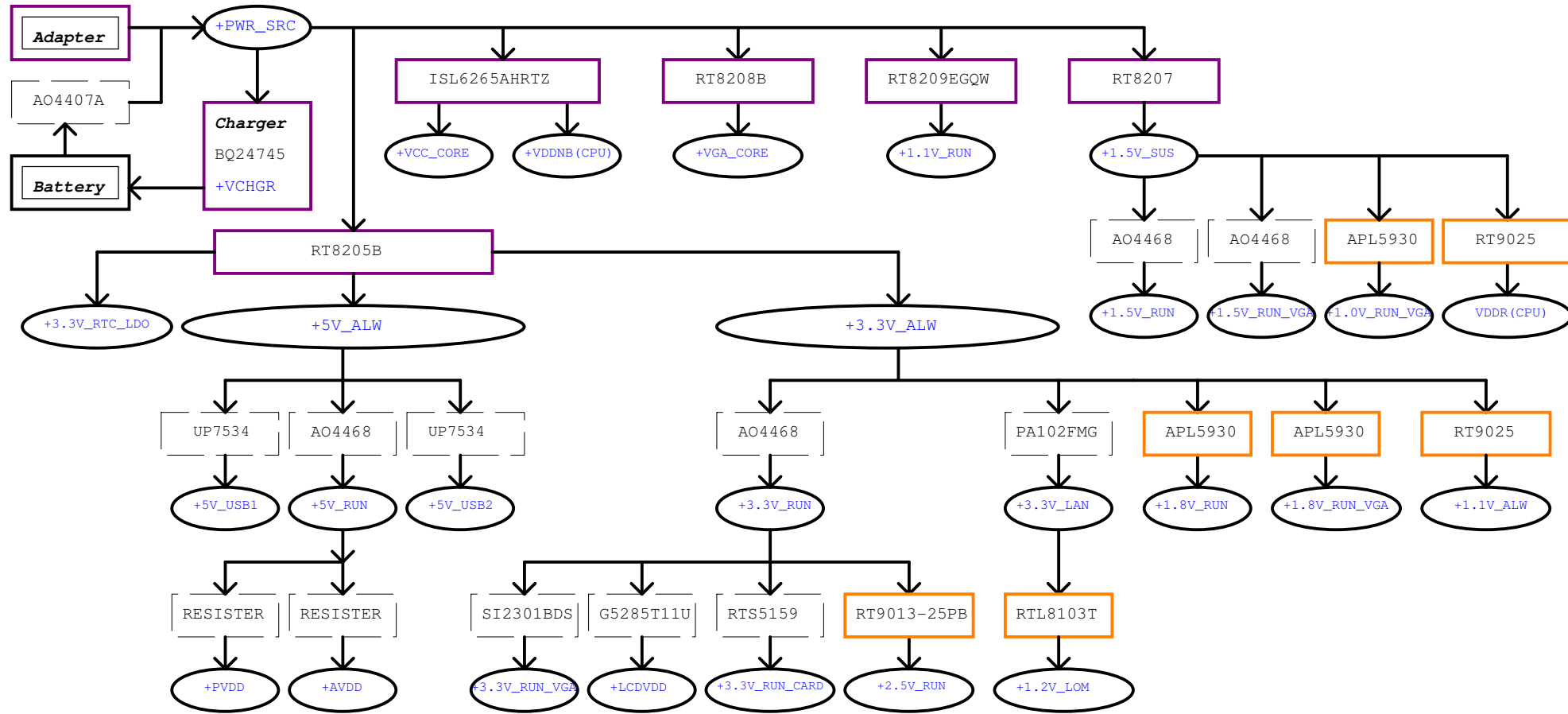
Power Block Diagram

Power Shape

Regulator

LDO

Switch

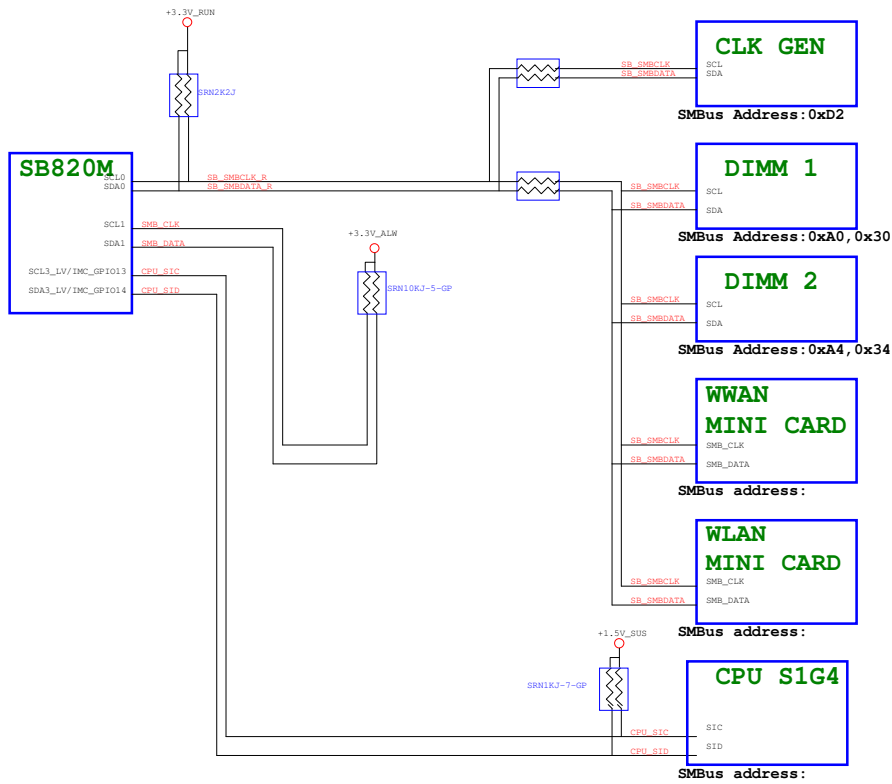


<Core Design>

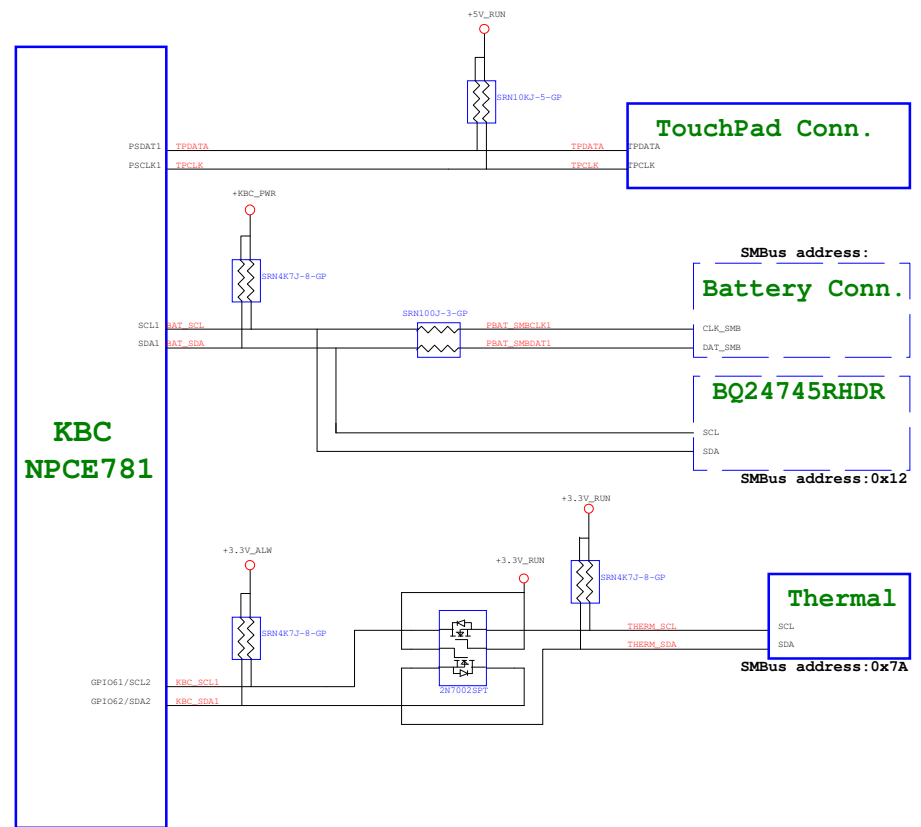


Title			Power Block Diagram
Size	Document Number	Rev	
A3	Berry AMD Discrete/UMA	A00	
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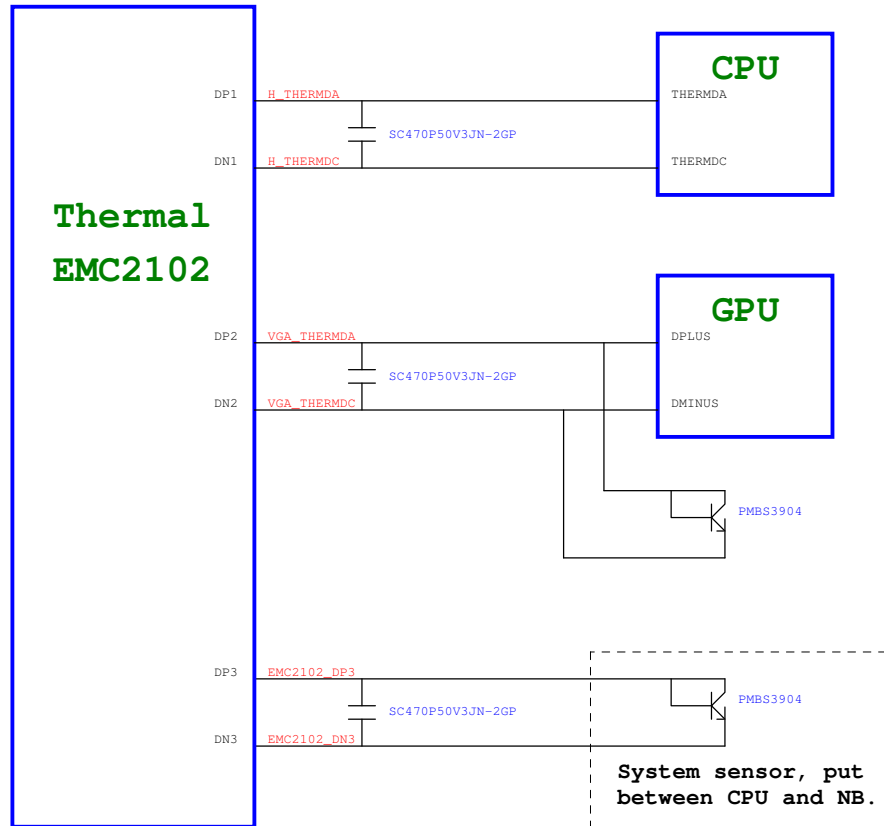
SB820M SMBus Block Diagram



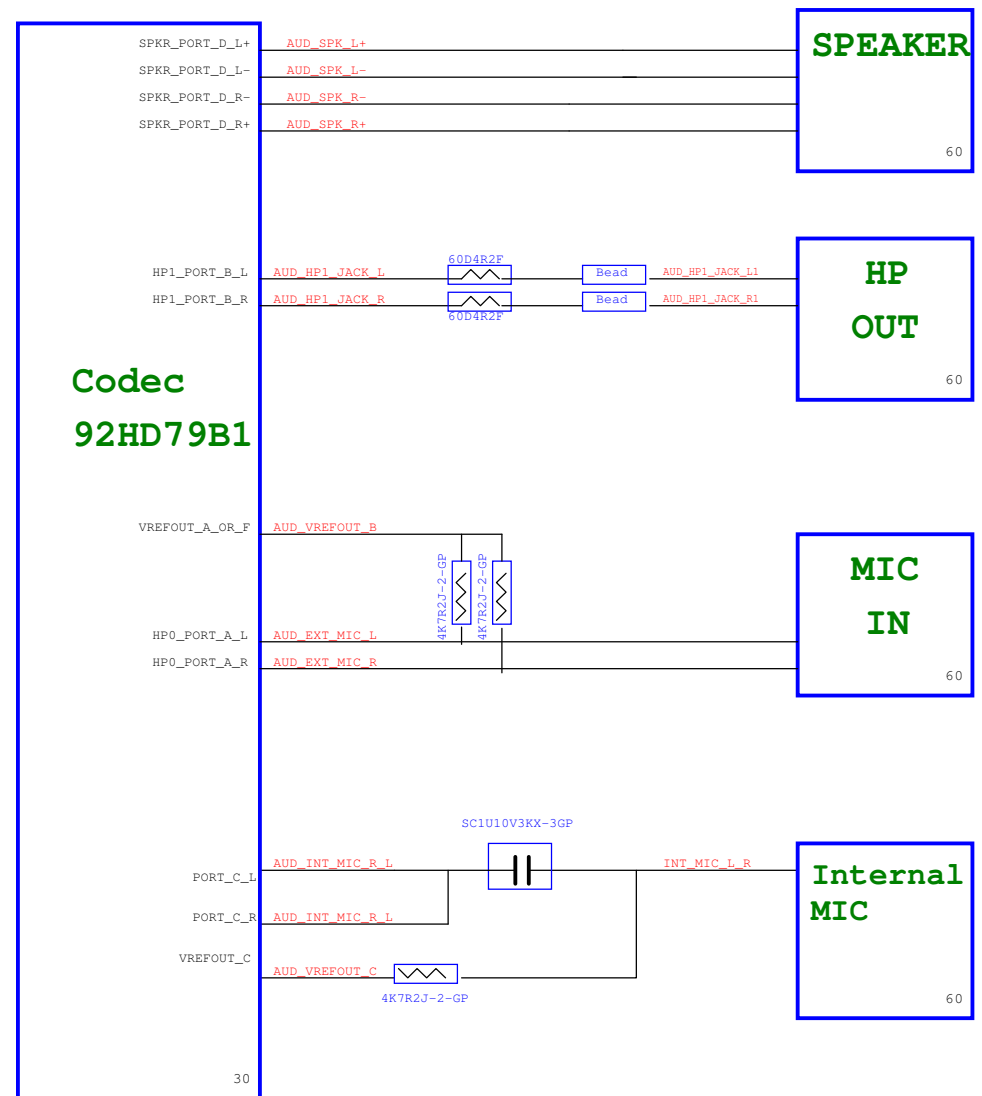
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



<Core Design>

SB820M Strapping

Capture from 45484 Rev. 1.02 AMD SB8xx-Series Southbridge Design Guide

Name	Strap Name	Schematic Note															
LPCCLK0	ECEnableStrap	Embedded Controller (EC) * 0 V - Disabled 3.3 V - Enabled															
EC_PWM3 EC_PWM2	{ROMTYPE_1, ROMTYPE_0 }	<table border="1"> <thead> <tr> <th>ROMTYPE_1</th> <th>ROMTYPE_0</th> <th>ROM TYPE</th> </tr> </thead> <tbody> <tr> <td>3.3V</td> <td>0V</td> <td>SPI ROM</td> </tr> <tr> <td>3.3V</td> <td>3.3V</td> <td>Reserved</td> </tr> <tr> <td>0V</td> <td>0V</td> <td>Firmware Hub</td> </tr> <tr> <td>0V</td> <td>3.3V</td> <td>LPC ROM (supports both LPC and PMC ROM types)</td> </tr> </tbody> </table> *	ROMTYPE_1	ROMTYPE_0	ROM TYPE	3.3V	0V	SPI ROM	3.3V	3.3V	Reserved	0V	0V	Firmware Hub	0V	3.3V	LPC ROM (supports both LPC and PMC ROM types)
ROMTYPE_1	ROMTYPE_0	ROM TYPE															
3.3V	0V	SPI ROM															
3.3V	3.3V	Reserved															
0V	0V	Firmware Hub															
0V	3.3V	LPC ROM (supports both LPC and PMC ROM types)															
LPCCLK1	CLKGEN	Defines clock generator * 0V - External clock mode: Use 100-MHz PCIeR clock as reference clock and generate internal clocks only. 3.3V- Integrated clock mode: Use 25-MHz crystal clock and generate both internal and external clocks															
PCICLK1	BIF_GEN2_COMPLIANCE_Strap	Set PCIe to Gen II mode 0V- Force PCIe interface at Gen I mode * 3.3V- PCIe interface is at Gen II mode Not Applicable to SB820M but provision for pull-down is required.															
PCICLK2	BootFailTmrEn	Watchdog function * 0V- Disable the boot fail timer function 3.3V- Enable the boot fail timer function															
PCICLK3	DefaultStrapMode	Default Debug Straps * 0V- Disable Debug Straps. 3.3V- Select external Debug Straps															
PCICLK4	CPUClkSel	CPU/NB HT Clock Selection * 0V- Reserved. 3.3V- Required setting for integrated clock mode. This strap is not used if the strap CLKGEN is configured for external clock generator mode.															
AZ_SDOUT	CoreSpeedMode	Slow down core clock for low power platform. * 0V- Performance mode 3.3V- Low Power mode															

RS880M Strapping

Capture from 46113_rs880m_ds_nda_1.03

Name	Strap Function	Schematic Note
DAC_VSYNC	STRAP_DEBUG_BUS_GPIO_ENABLE#	Enables debug bus access through memory I/O pads and GPIOs. 0: Enable * 1: Disable
DAC_HSYNC	SIDE_PORT_EN#	Indicates if memory side-port is available or not 0: Available(UMA) 1: Not available(Discrete)
SUS_STAT#	LOAD_EEPROM_STRAPS#	Selects loading of strap values from EEPROM. 0: I2C master can load strap values from EEPROM if connected, or use default values if EEPROM is not connected. Please refer to RS880M's reference schematics for system level implementation details. * 1: Use default values

USB Table

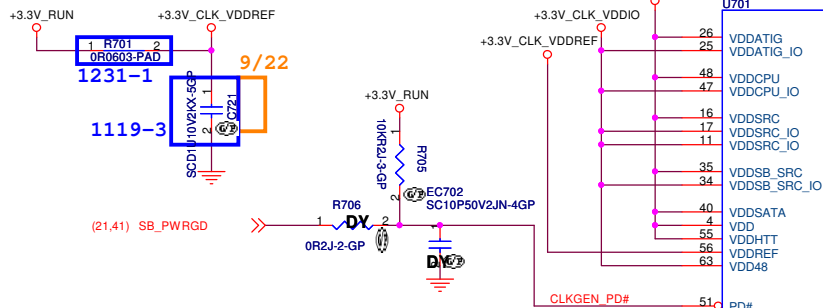
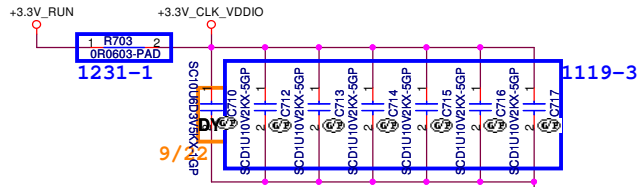
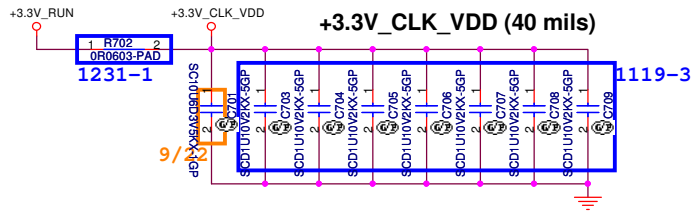
USB	
Pair	Device
0	USB0 (I/O Board/ESATA)
1	USB1 (I/O Board)
2	USB2 (CRT Board)
3	USB3 (CRT Board)
4	WLAN USB
5	WWAN USB
6	RESERVED
7	RESERVED
8	RESERVED
9	BLUETOOTH
10	CARD READER
11	CAMERA (LVDS CONN)
12	RESERVED
13	RESERVED

PCIE Routing

RS880M	
LANE0	MiniCard WLAN
LANE1	LAN
LANE2	MiniCard WWAN

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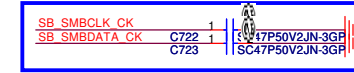
DELL		Wistron Corporation	
		21F, 8th, Sec. 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.	
Table of Content			
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CLKREQ# MAP

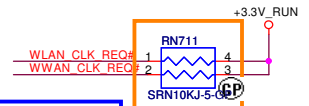
CLKREQ0#	No use
CLKREQ1#	CLKSRC1 WLAN
CLKREQ2#	CLKSRC2 WWAN
CLKREQ3#	CLKSRC3 LAN
CLKREQ4#	No use

0107-1

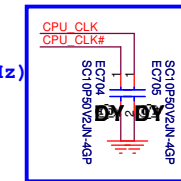


VGA (100MHz)

Need External PU Resistor

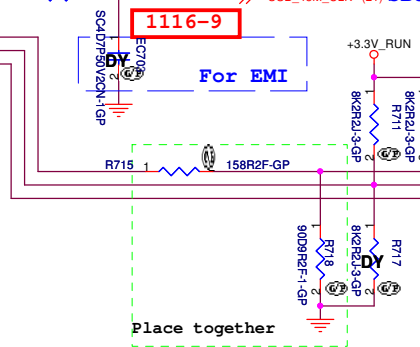


CPU_CLK (200MHz)

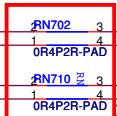


SB820M_USB (48MHz)

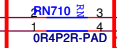
SB OSCIN (14MHz)



WLAN (100MHz)



WWAN (100MHz)



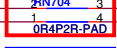
LAN (100MHz)



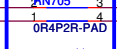
VGA (27MHz)



NB (100MHz)



SB (100MHz)



- TP701 1 TP_CLK_SRC6
- TP702 1 TP_CLK_SRC6#
- TP703 1 TP_CLKREQ0#
- TP704 1 TP_CLKREQ3#
- TP705 1 TP_CLKREQ4#
- TP706 1 TP_CLK_SRC4
- TP707 1 TP_CLK_SRC4#
- TP709 1 R_NB_GPP_CLK
- TP708 1 R_NB_GPP_CLK#

NB ALINK (100MHz)
SB PCIE (100MHz)
VGA Madison (27MHz)

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
SEL_SATA FS1	0*	100 MHz differential HTT clock
SEL_27MHz FS2	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock

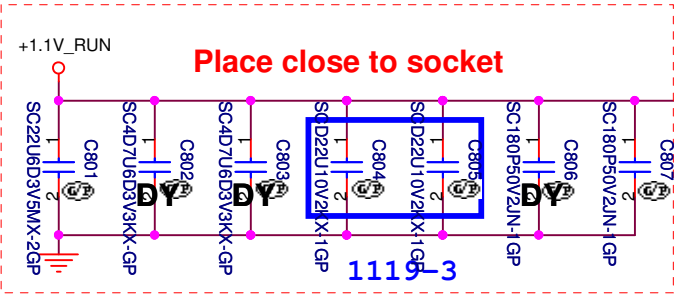
<Core Design>



Clock Generator ICS9LPR480

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A3				
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SSID = CPU



1.1V(1.5A) for VLDT



(12) HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0 (12)
(12) HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0 (12)
(12) HT_NB_CPU_CAD_H1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1 (12)
(12) HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1 (12)
(12) HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2 (12)
(12) HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2 (12)
(12) HT_NB_CPU_CAD_H3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3 (12)
(12) HT_NB_CPU_CAD_L3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_CPU_NB_CAD_L3 (12)
(12) HT_NB_CPU_CAD_H4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_CPU_NB_CAD_H4 (12)
(12) HT_NB_CPU_CAD_L4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4 (12)
(12) HT_NB_CPU_CAD_H5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5 (12)
(12) HT_NB_CPU_CAD_L5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5 (12)
(12) HT_NB_CPU_CAD_H6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6 (12)
(12) HT_NB_CPU_CAD_L6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_CPU_NB_CAD_L6 (12)
(12) HT_NB_CPU_CAD_H7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_CPU_NB_CAD_H7 (12)
(12) HT_NB_CPU_CAD_L7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_CPU_NB_CAD_L7 (12)
(12) HT_NB_CPU_CAD_H8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_CPU_NB_CAD_H8 (12)
(12) HT_NB_CPU_CAD_L8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_CPU_NB_CAD_L8 (12)
(12) HT_NB_CPU_CAD_H9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_CPU_NB_CAD_H9 (12)
(12) HT_NB_CPU_CAD_L9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_CPU_NB_CAD_L9 (12)
(12) HT_NB_CPU_CAD_H10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_CPU_NB_CAD_H10 (12)
(12) HT_NB_CPU_CAD_L10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_CPU_NB_CAD_L10 (12)
(12) HT_NB_CPU_CAD_H11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_CPU_NB_CAD_H11 (12)
(12) HT_NB_CPU_CAD_L11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_CPU_NB_CAD_L11 (12)
(12) HT_NB_CPU_CAD_H12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_CPU_NB_CAD_H12 (12)
(12) HT_NB_CPU_CAD_L12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_CPU_NB_CAD_L12 (12)
(12) HT_NB_CPU_CAD_H13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_CPU_NB_CAD_H13 (12)
(12) HT_NB_CPU_CAD_L13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_CPU_NB_CAD_L13 (12)
(12) HT_NB_CPU_CAD_H14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_CPU_NB_CAD_H14 (12)
(12) HT_NB_CPU_CAD_L14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_CPU_NB_CAD_L14 (12)
(12) HT_NB_CPU_CAD_H15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_CPU_NB_CAD_H15 (12)
(12) HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15 (12)
(12) HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0 (12)
(12) HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0 (12)
(12) HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1 (12)
(12) HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1 (12)
(12) HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0 (12)
(12) HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0 (12)
(12) HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1 (12)
(12) HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1 (12)

SKT-BGA638H176

1'nd 62.10055.111
2'nd 62.10055.171

<Core Design>



Title CPU_HT_LINK I/F_(1/4)		
Size A4	Document Number Berry AMD Discrete/UMA	Rev A00
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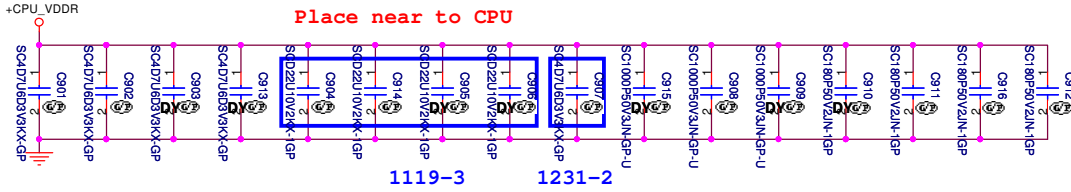
SSID = CPU

1231-2

Set empty: C905, C906, C903, C909, C913, C910, C915

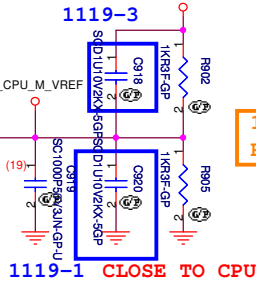
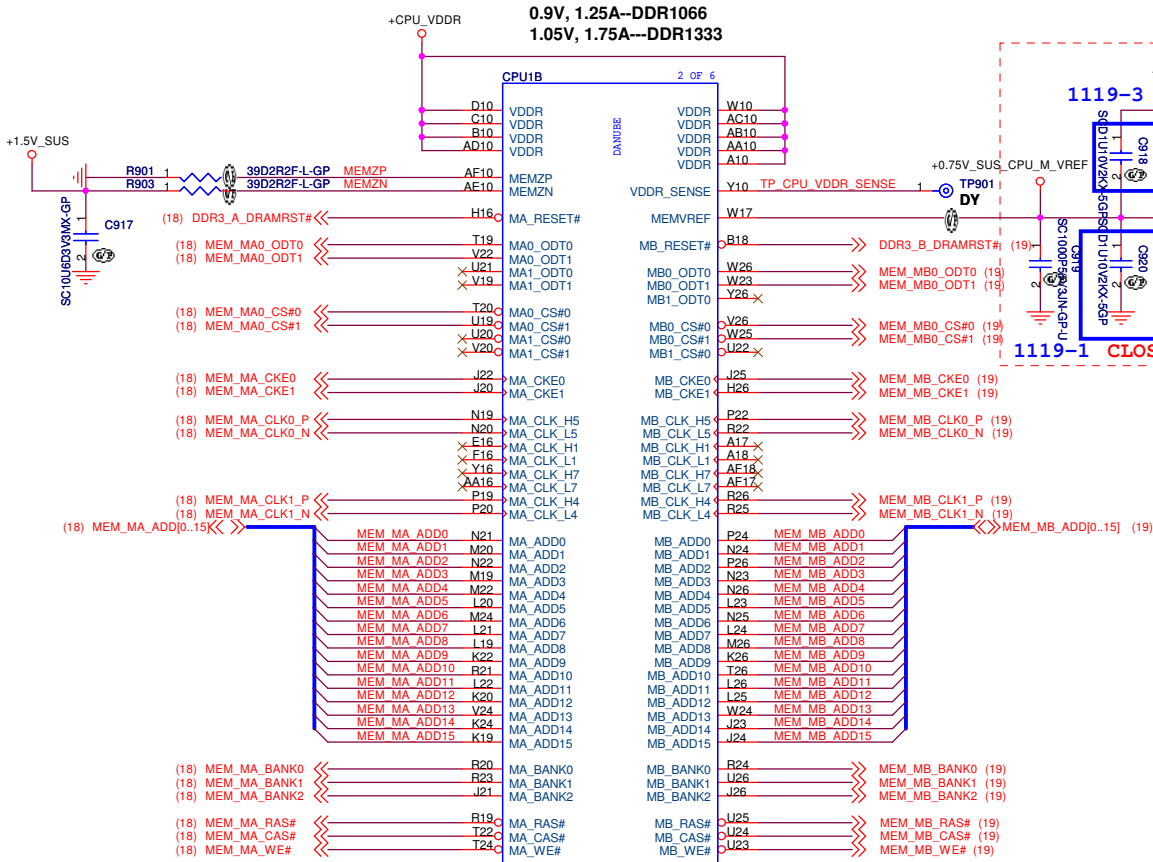
4.7UF*4
0.22UF*4
100PF*4
180PF*4

Place near to CPU



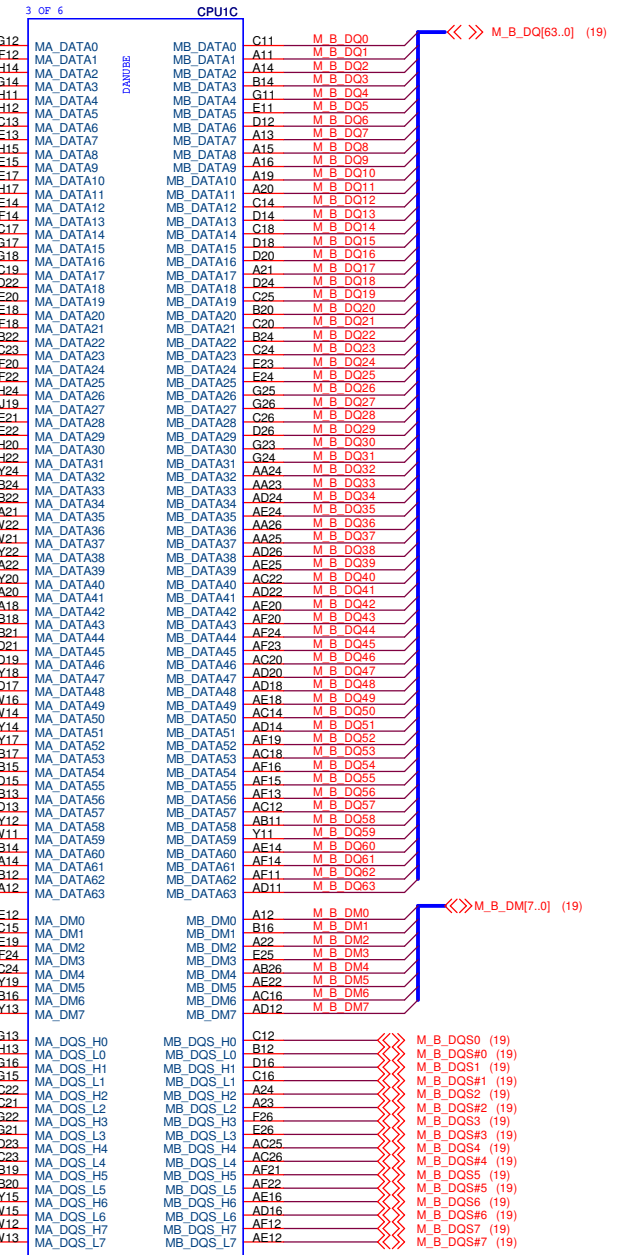
1119-3 1231-2

0.9V, 1.25A--DDR1066
1.05V, 1.75A--DDR1333



1117-8 Remove

1119-1 CLOSE TO CPU



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DELL

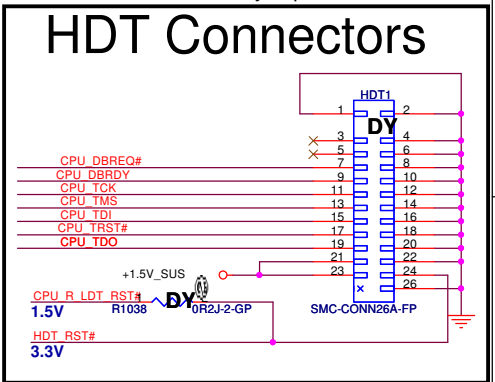
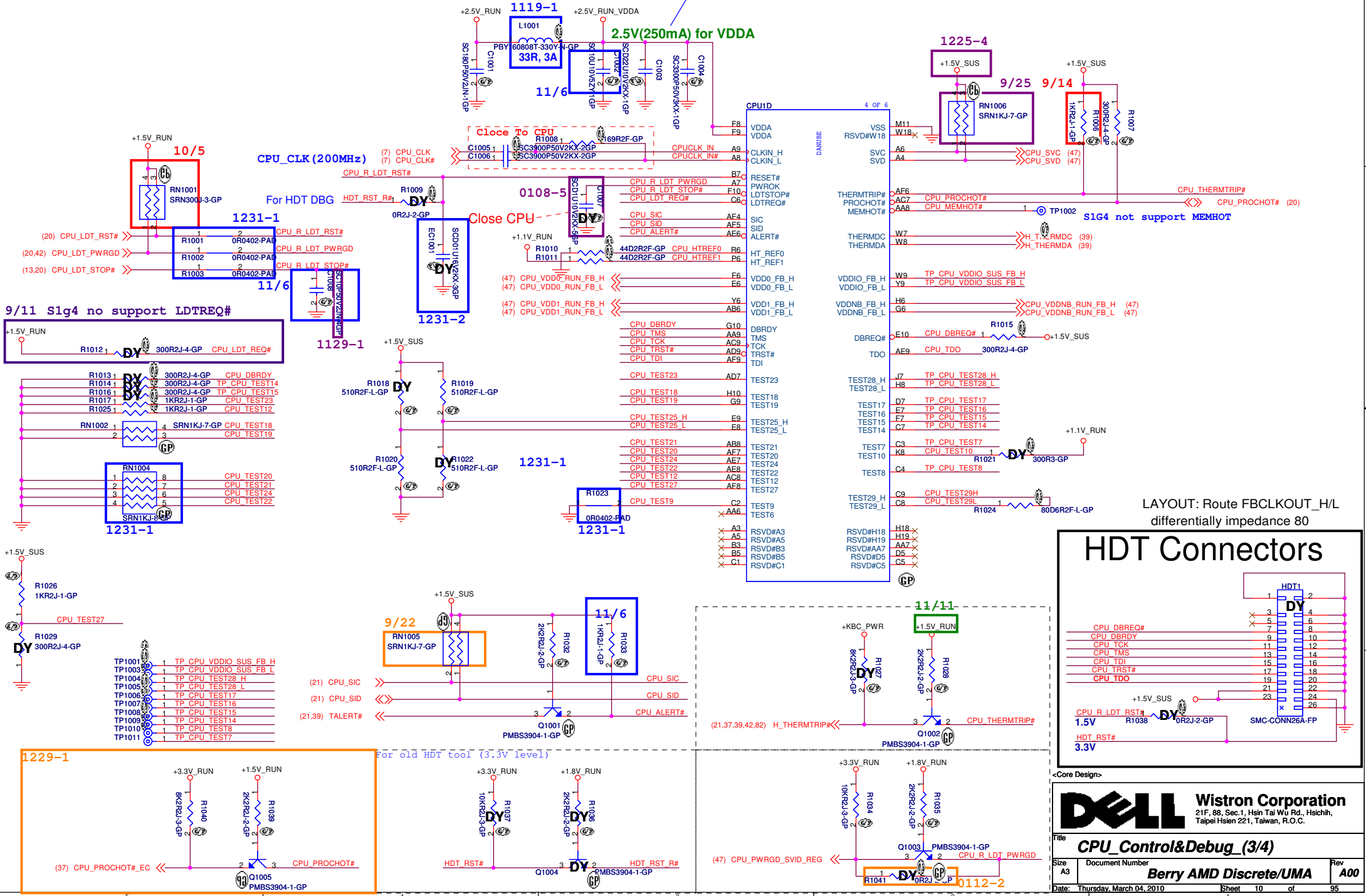
Title: **CPU_DDR (2/4)**

Size: A3 Document Number: **Berry AMD Discrete/UMA** Rev: **A00**

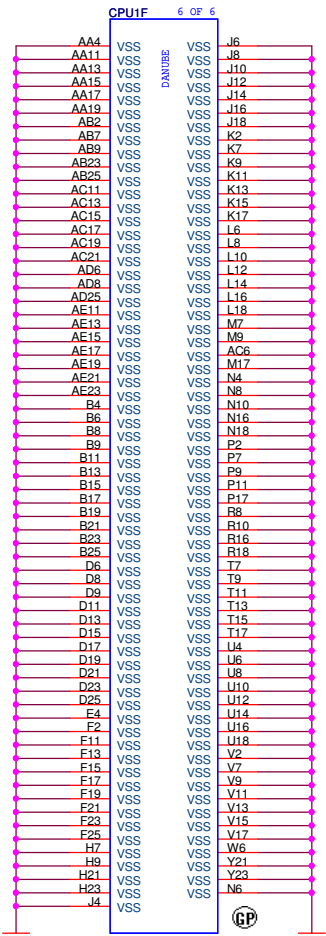
Date: Thursday, March 04, 2010 Sheet 9 of 95

SSID = CPU

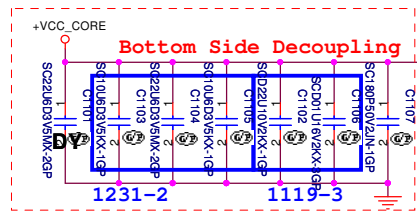
LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



SSID = CPU

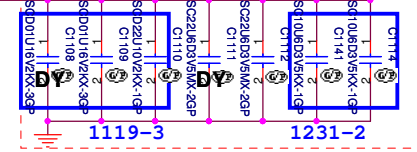


(36A) for 35W S1G4 VDD



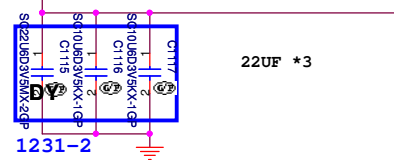
- 22uF *2
- 10uF *2
- 0.22uF *1
- 0.01uF *1
- 180pF *1

Bottom Side Decoupling



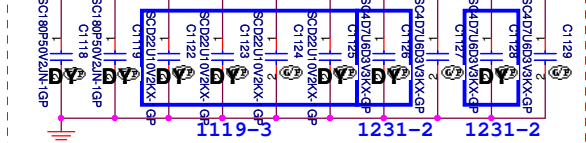
- 22uF *2
- 10uF *2
- 0.22uF *1
- 0.01uF *1
- 180pF *1

0.9V(4A) for VDDNB

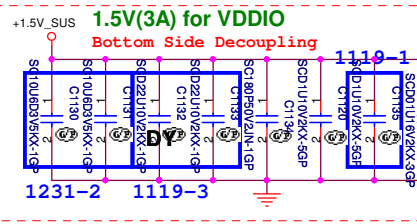


22uF *3

Place near to CPU



- 0.01uF *1
- 0.1uF *2
- 0.22uF *4
- 4.7uF *4
- 180PF *2



- 10uF *2
- 0.22uF *2
- 180PF *1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_Power_(4/4)**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
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SSID = N.B

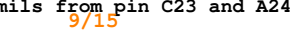
RS880M : 71.RS880.M05

Table listing pin numbers and signal names for HT_CPU_NB_CAD_H0 through HT_CPU_NB_CLK_L1.

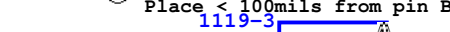
Table listing pin numbers and signal names for HT_RXCAD0P through HT_RXCALN.

Table listing pin numbers and signal names for HT_TXCAD0P through HT_TXCALN.

Table listing pin numbers and signal names for HT_NB_CPU_CAD_H0 through HT_NB_CPU_CLK_L1.



Place < 100mils from pin C23 and A24



Place < 100mils from pin B25 and B24

Table listing pin numbers and signal names for PCIE_NRX_GTX_P15 through PCIE_NRX_GTX_N0.

Table listing pin numbers and signal names for GFX_RX0P through GFX_RX15N.

Table listing pin numbers and signal names for PCIE_NTX_GRX_C_P15 through PCIE_NTX_GRX_C_N0.

Table listing pin numbers and signal names for SCD1U10V2KX-5GP through SCD1U10V2KX-5GP.

Table listing pin numbers and signal names for PCIE_NTX_GRX_P15 through PCIE_NTX_GRX_N0.

Table listing signal names and pin numbers for WLAN, LAN, and WWAN.

Table listing signal names and pin numbers for PCIE_I/F_GPP.

Table listing signal names and pin numbers for PCIE_I/F_GPP.

Table listing signal names and pin numbers for PCIE_I/F_GPP.

Table listing signal names and pin numbers for WLAN, LAN, and WWAN.

Table listing signal names and pin numbers for A-LINK.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for A-LINK.

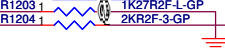
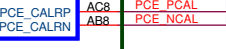
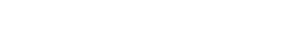
Table listing signal names and pin numbers for A-LINK.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for PCIE_I/F_SB.

Table listing signal names and pin numbers for A-LINK.



Place < 100mils from pin AC8 and AB8

PCIE_NTX_GRX_P[12..15] >> PCIE_NTX_GRX_P[12..15] (57)

PCIE_NTX_GRX_N[12..15] >> PCIE_NTX_GRX_N[12..15] (57)

PCIE_NTX_GRX_P[0..11] >> PCIE_NTX_GRX_P[0..11] (80)

PCIE_NTX_GRX_N[0..11] >> PCIE_NTX_GRX_N[0..11] (80)

PCIE_NRX_GTX_P[0..15] << PCIE_NRX_GTX_P[0..15] (80)

PCIE_NRX_GTX_N[0..15] << PCIE_NRX_GTX_N[0..15] (80)

A-LINK

Dell Wistron Corporation logo and address information.

SSID = N.B

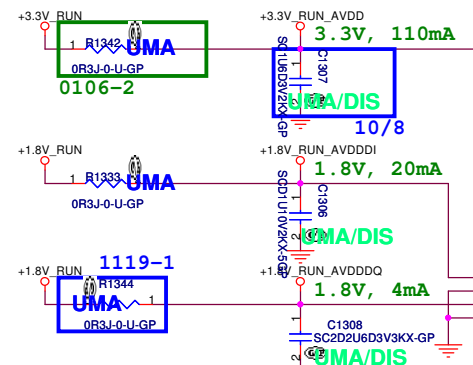
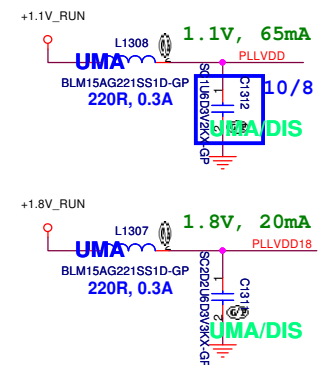
RS880M : 71.RS880.M05

UMA DAC Signal: GREEN/BLUE: Connected to GND through two separate 150- 1% resistors.

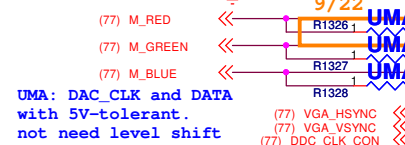
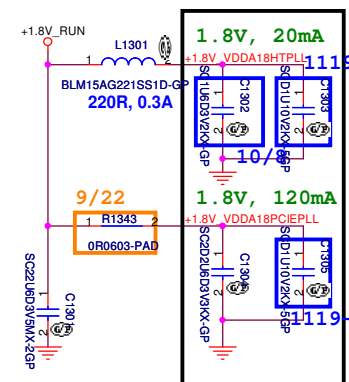
RED: Connected to GND through two separate 133- 1% resistors. (For match resistor on CRT/B 150- 1%)

STRAP_DEBUG_BUS_GPIO_ENABLE# (RS880M use DAC_VSYNC) Enables debug bus access through memory I/O pads and GPIOs. *1 : Disable 0 : Enable

*DEFAULT

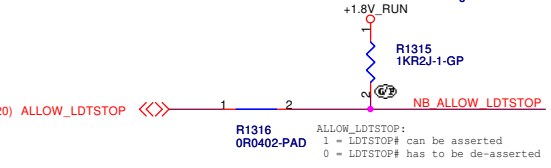
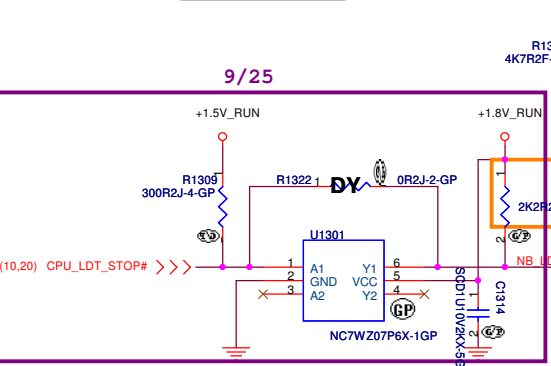


Layout Note Trace at least 15 mil

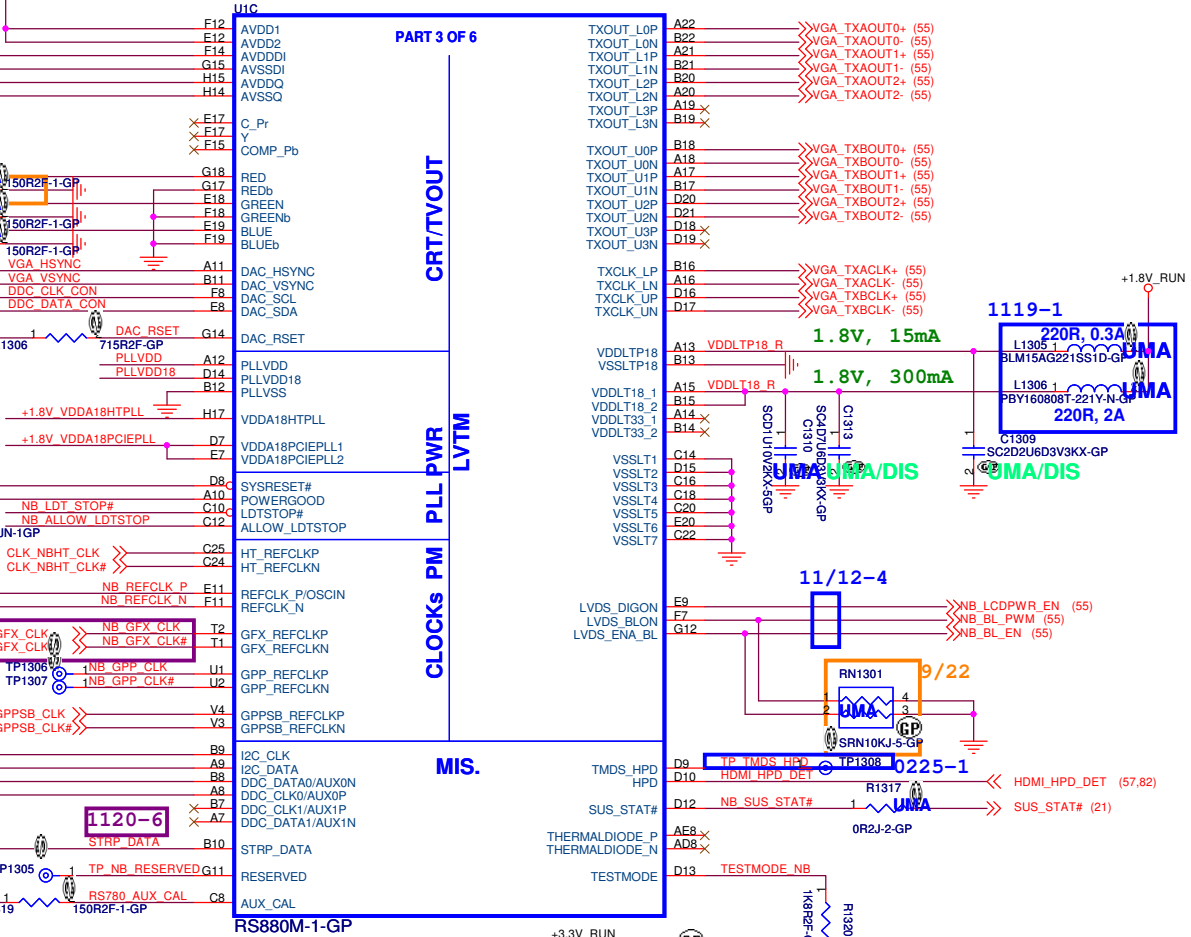
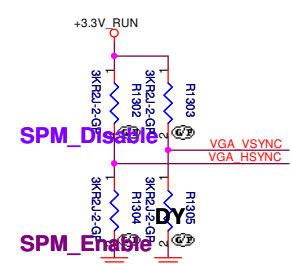


UMA: DAC_CLK and DATA with 5V-tolerant. not need level shift

Trace at least 10 mil



ALLOW_LDTSTOP: 1 = LDTSTOP# can be asserted 0 = LDTSTOP# has to be de-asserted



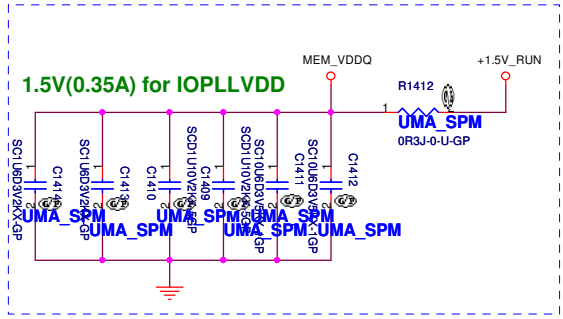
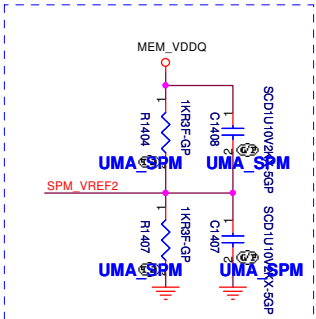
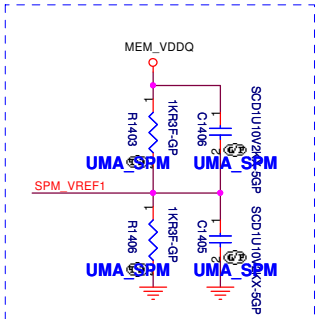
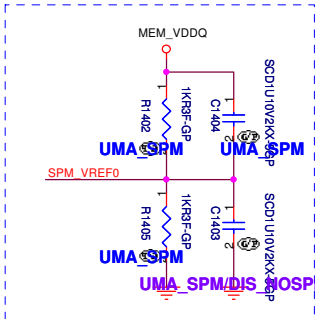
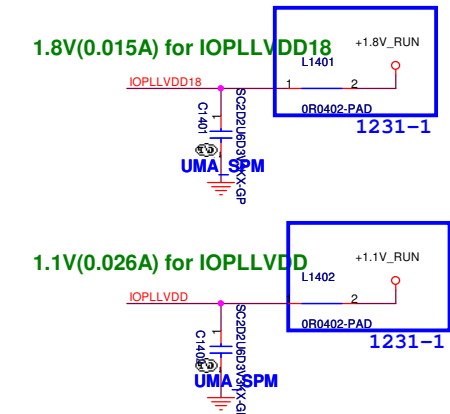
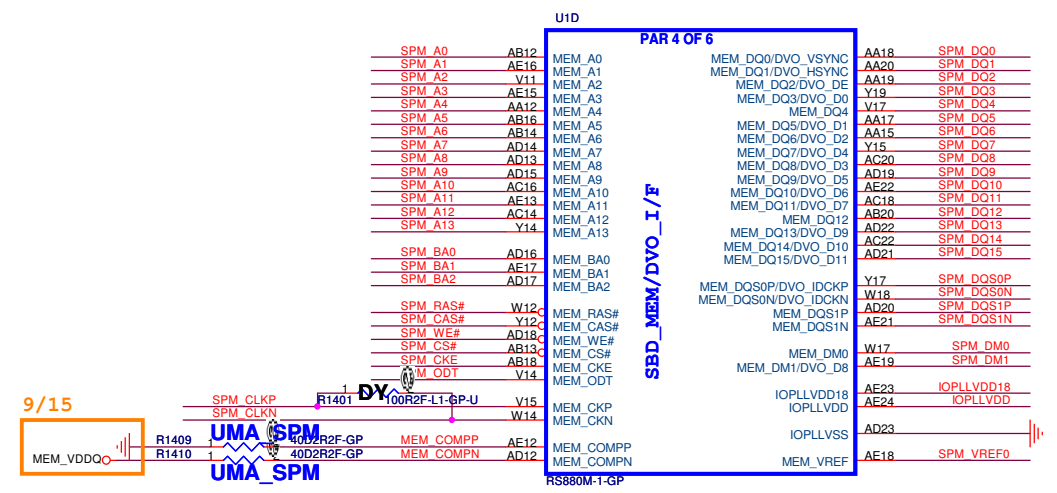
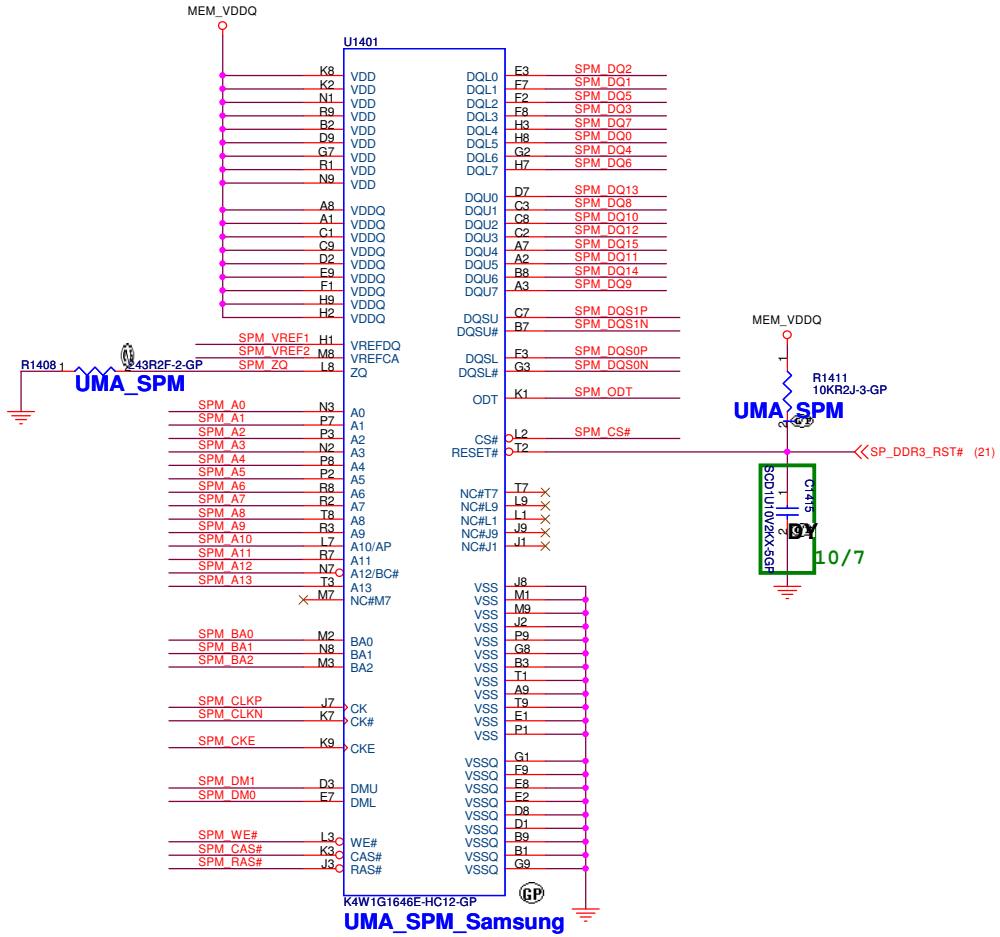
CRIT/OUT

CLOCKS PM PLL PWR LVTM

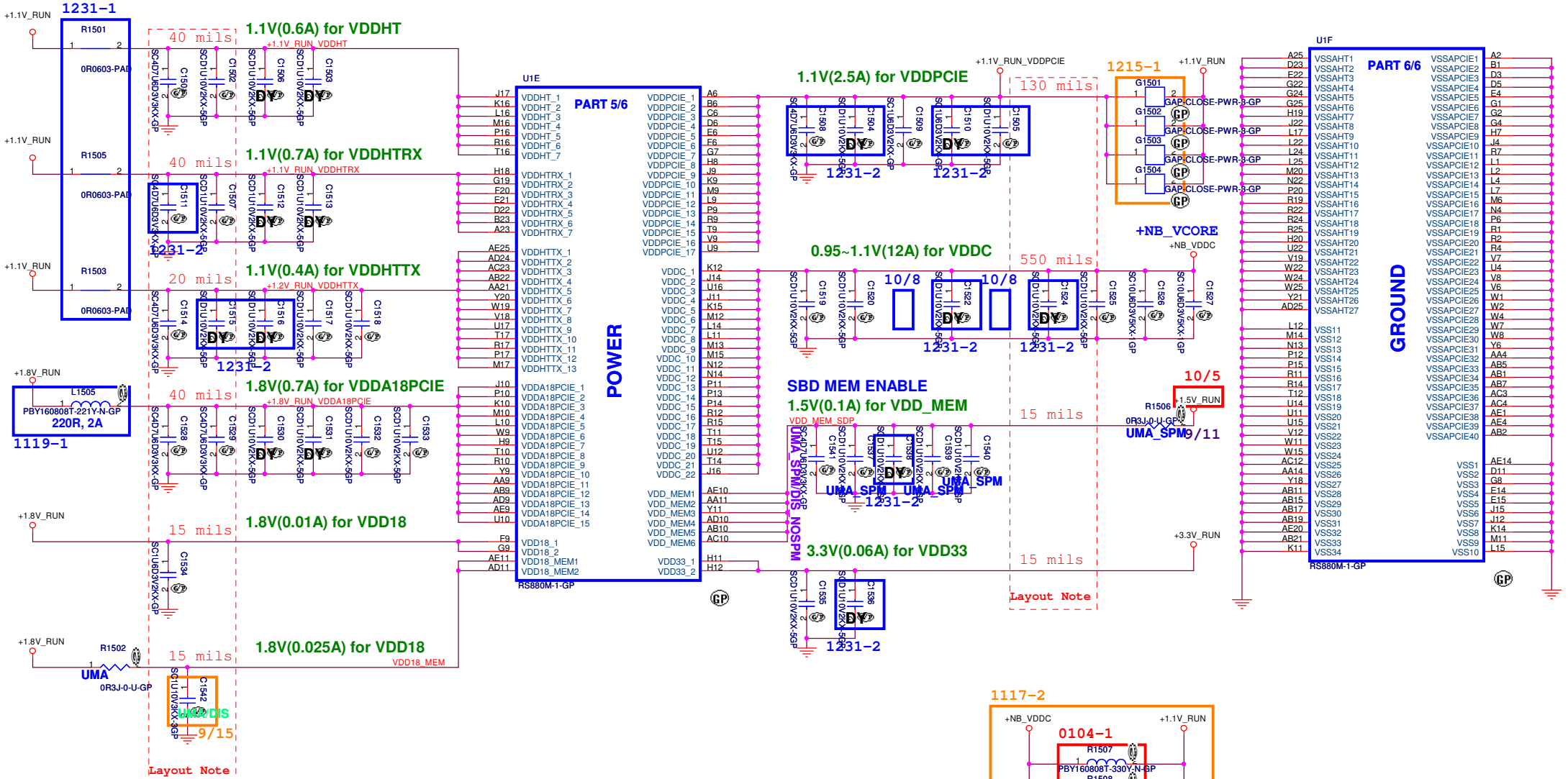
MIS.

Dell Wistron Corporation logo and title block. Title: AMD-RS880M_LVDS&CRT_(2/4). Document Number: Berry AMD Discrete/UMA. Date: Thursday, March 04, 2010. Sheet 13 of 95.

SSID = N.B

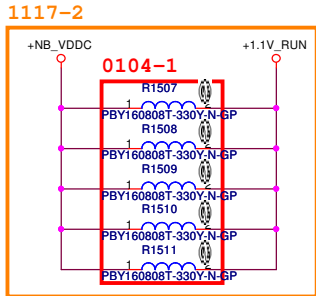


SSID = N.B



Layout Note

Layout Note



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Title **AMD-RS880M_PWR&GD_(4/4)**

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(Blanking)

<Core Design>

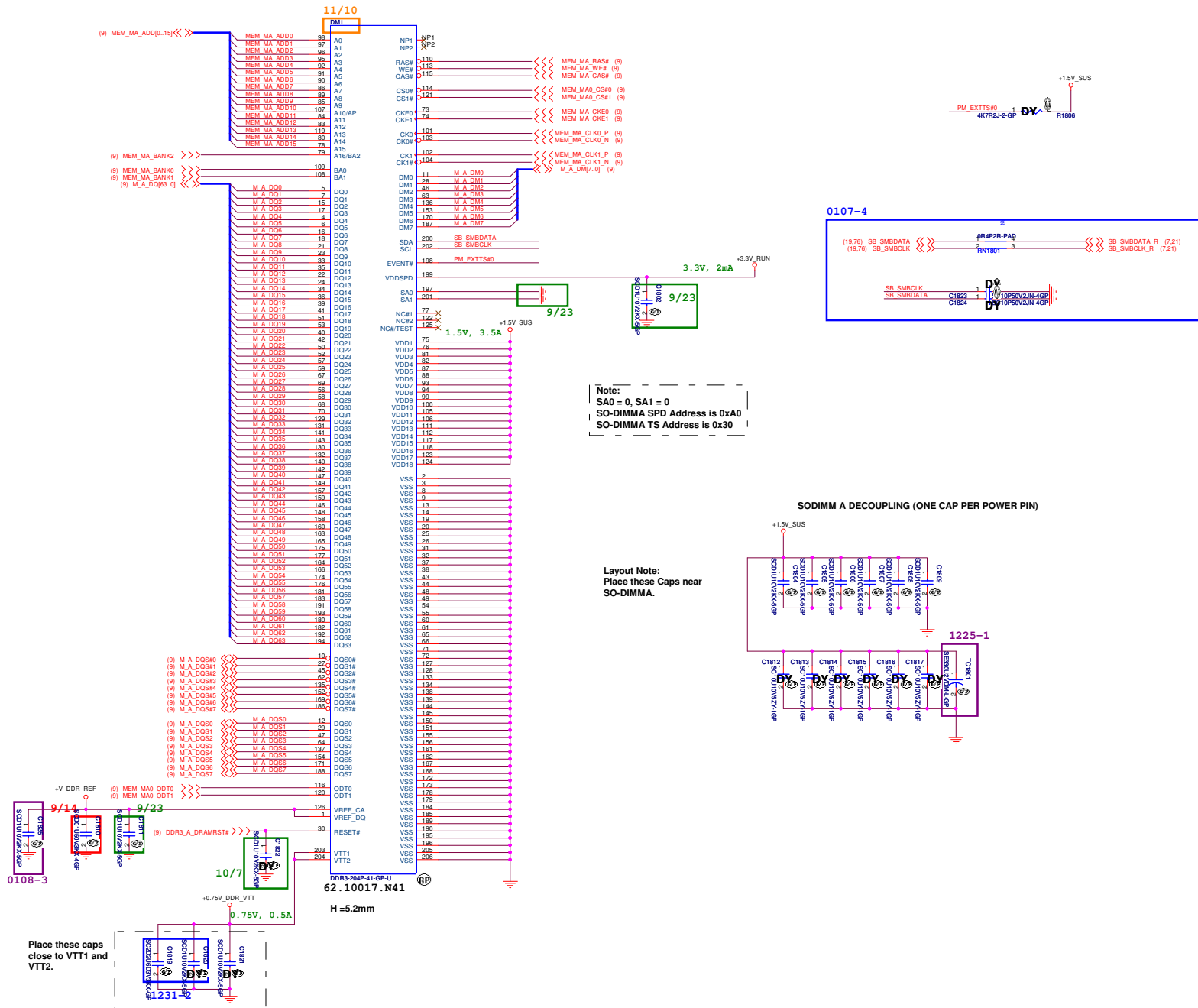
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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<Core Design>

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SSID = MEMORY



Note:
SA0 = 0, SA1 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

Layout Note:
Place these Caps near
SO-DIMMA.

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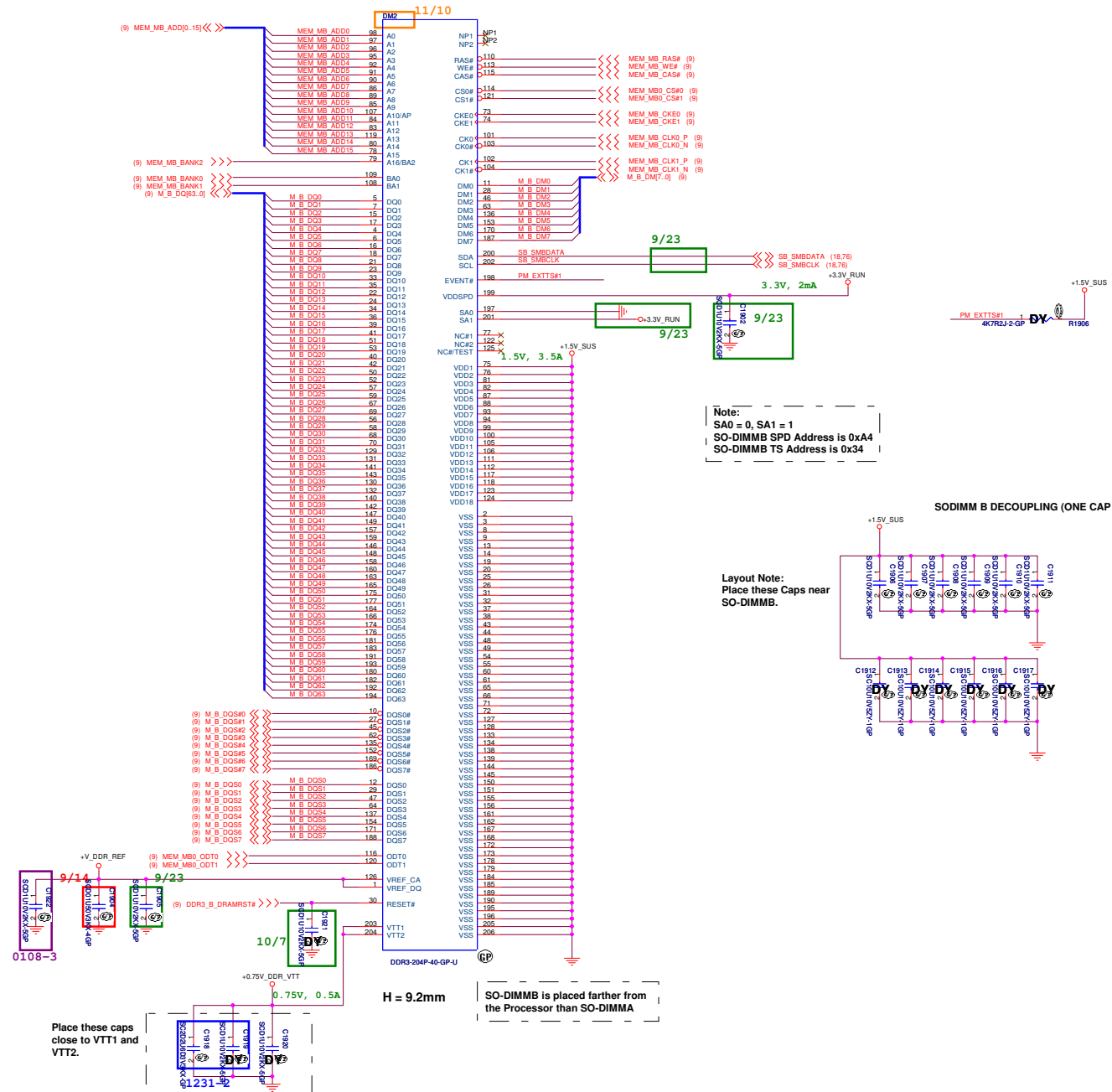
File: **DDR3-SODIMM1**

Size: Document Number Rev: **A00**

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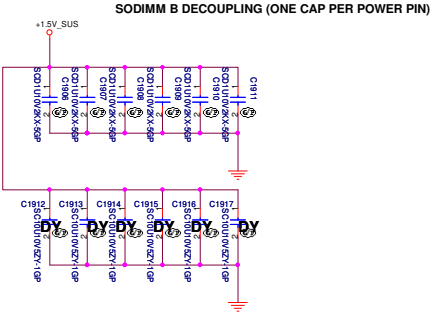
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SSID = MEMORY

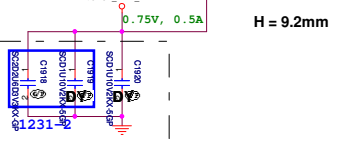


Note:
SA0 = 0, SA1 = 1
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

Layout Note:
Place these Caps near
SO-DIMMB.



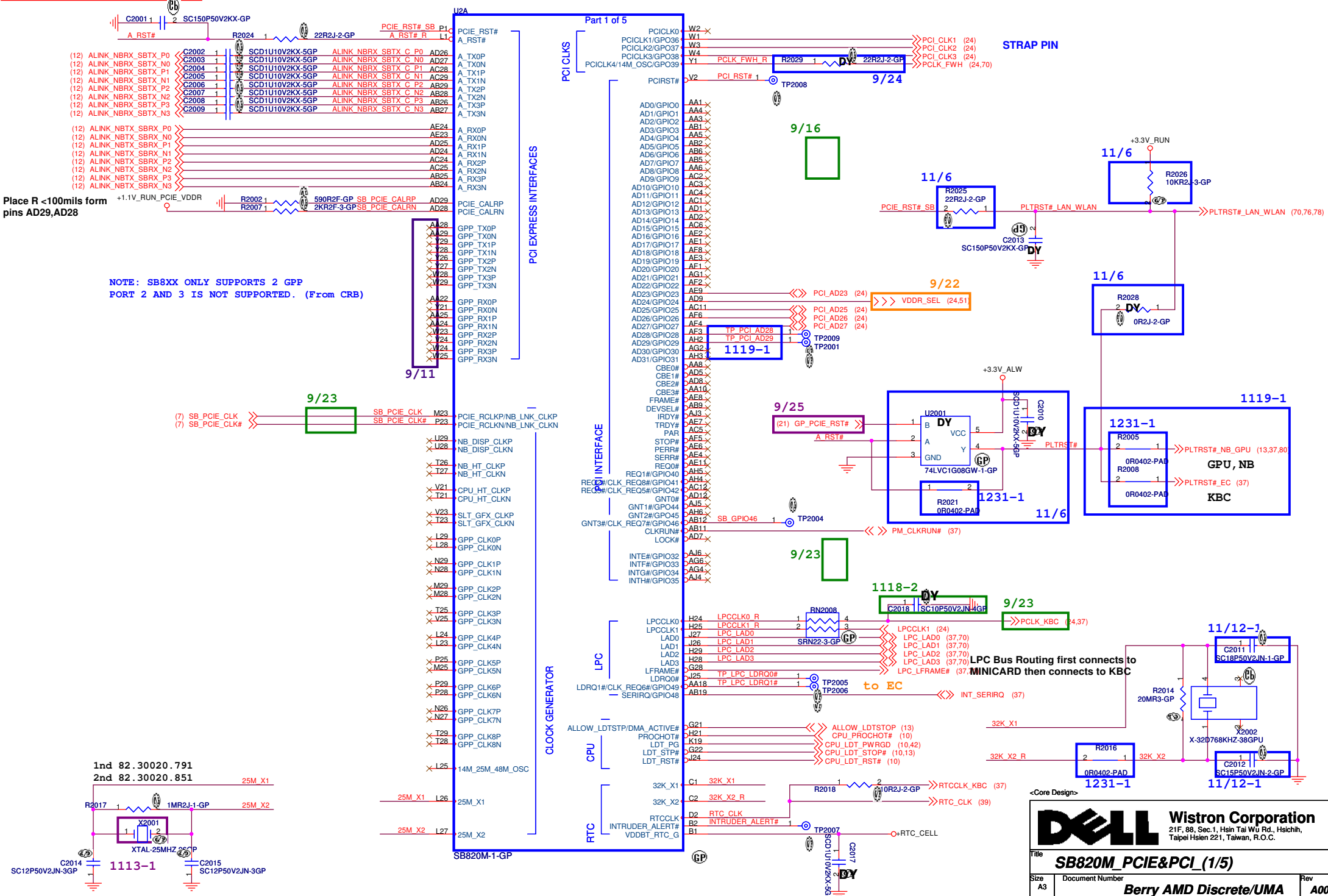
Place these caps
close to VTT1 and
VTT2.



H = 9.2mm
SO-DIMMB is placed farther from
the Processor than SO-DIMMA

SSID = S.B

SB820M : 71.SB820.M02



NOTE: SB8XX ONLY SUPPORTS 2 GPP PORT 2 AND 3 IS NOT SUPPORTED. (From CRB)

Place R <100mils form pins AD29,AD28

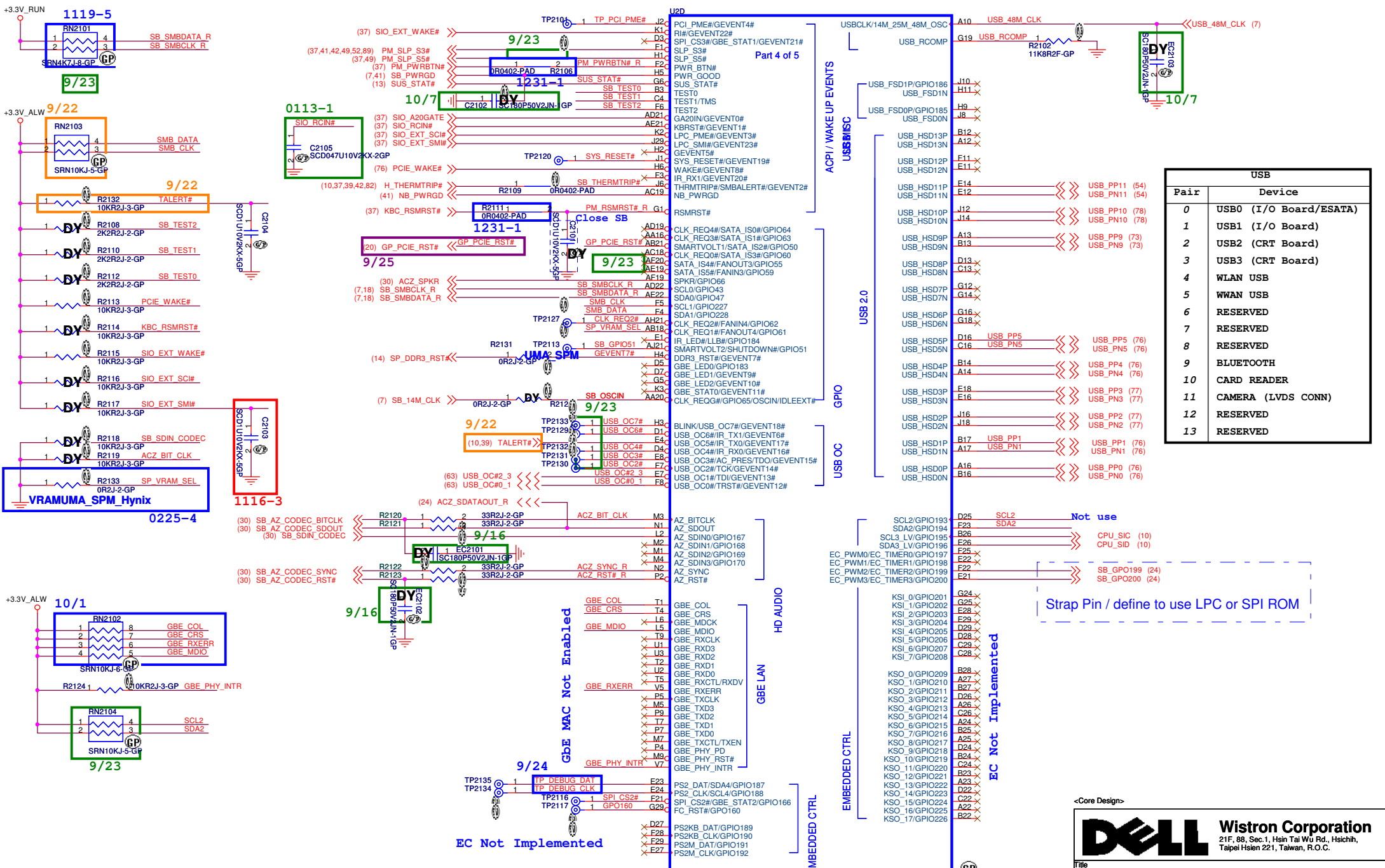
STRAP PIN

LPC Bus Routing first connects to MINICARD then connects to KBC

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Title		SB820M_PCIE&PCI_(1/5)	
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SSID = S.B



USB		
Pair	Device	
0	USB0 (I/O Board/ESATA)	
1	USB1 (I/O Board)	
2	USB2 (CRT Board)	
3	USB3 (CRT Board)	
4	WLAN USB	
5	WWAN USB	
6	RESERVED	
7	RESERVED	
8	RESERVED	
9	BLUETOOTH	
10	CARD READER	
11	CAMERA (LVDS CONN)	
12	RESERVED	
13	RESERVED	

Strap Pin / define to use LPC or SPI ROM

EC Not Implemented

EC Not Implemented

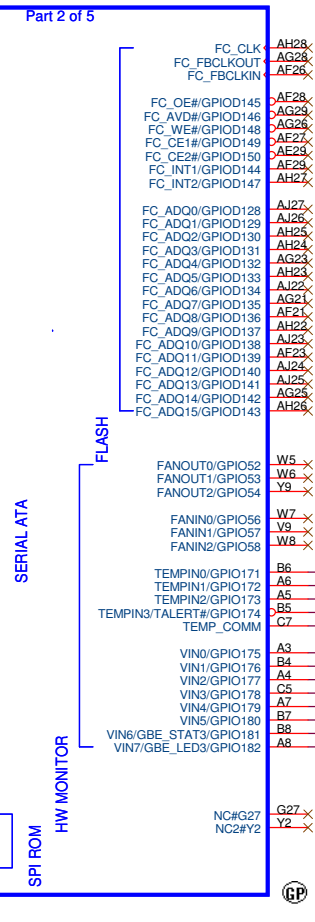
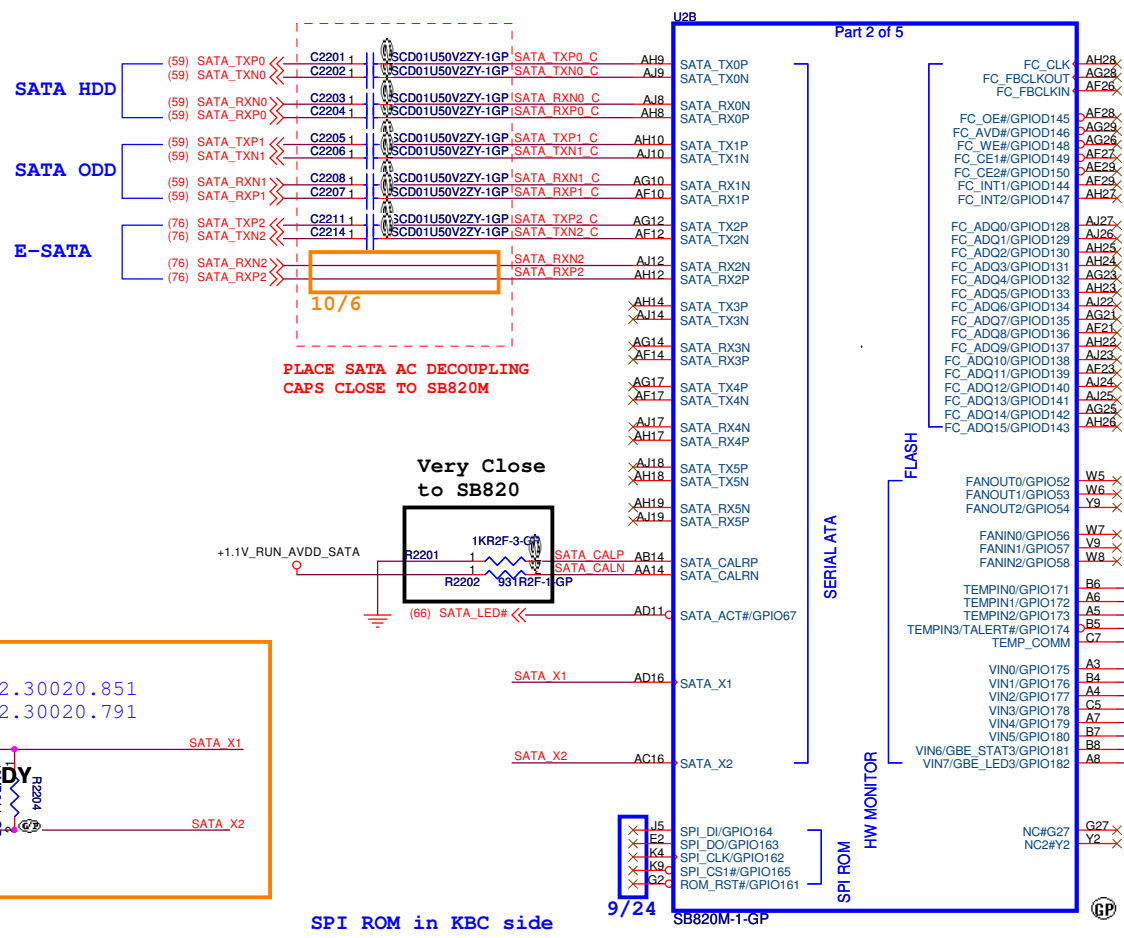
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File: **SB820M_USB&GPIO_(2/5)**

Size: A3 Document Number: **Berry AMD Discrete/UMA** Rev: **A00**

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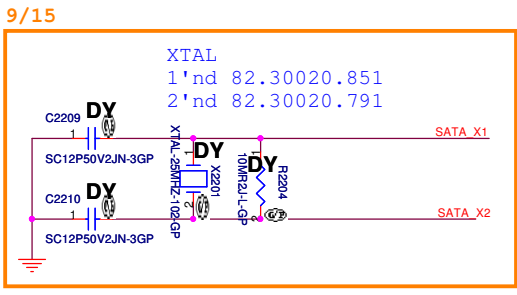
SSID = S.B



GPIO[150:128] are open drain GPIO pins where as GPO160 is an open drain GPO pin. These pins are not programmed to GPIO mode by default.

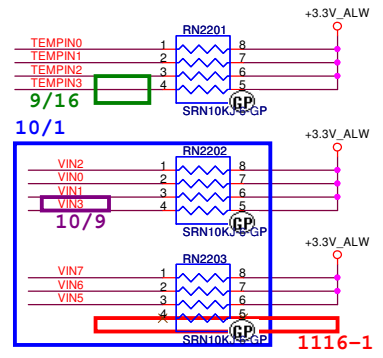
If use as GPIO, need to pull up to 1.8V_RUN

1119-1
Move to P.51



9/22

10/9
MEM1_1V5 >> MEM_1V5 (51)



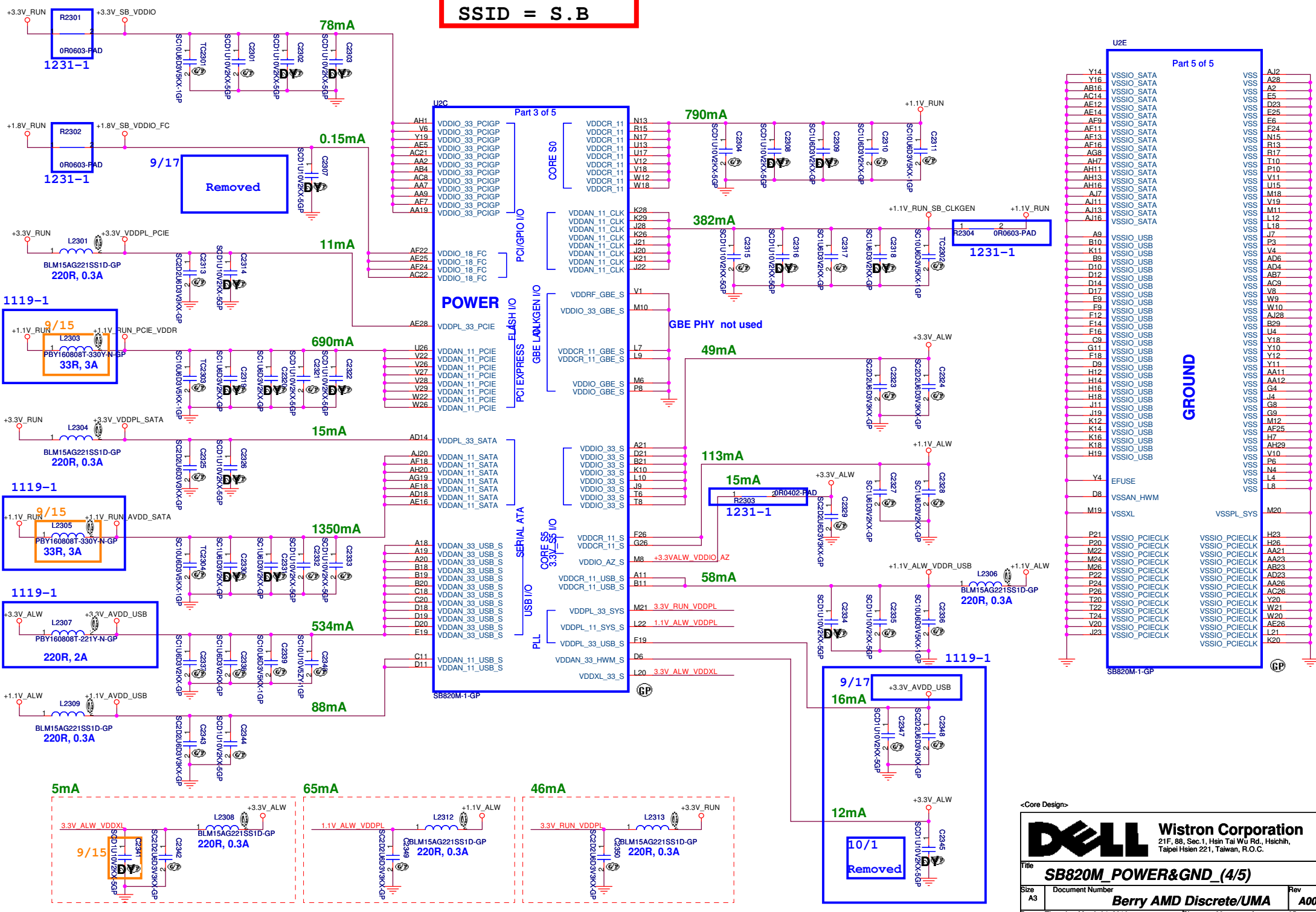
<Core Design>

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File: **SB820M_SATA-IDE_(3/5)**

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SSID = S.B



<Core Design>

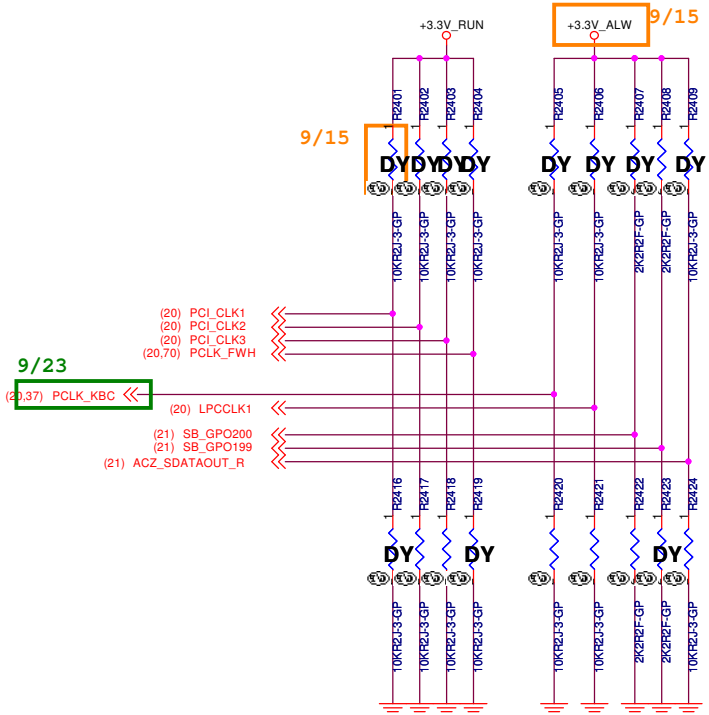
Wistron Corporation
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Title: **SB820M_POWER&GND_(4/5)**

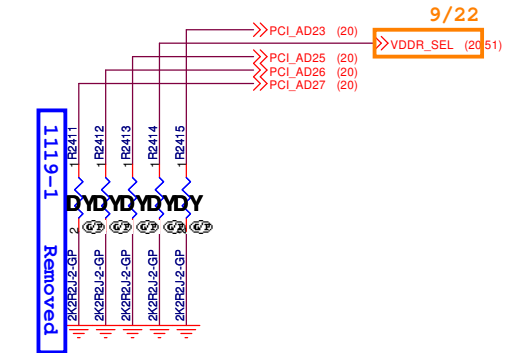
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SSID = S.B

REQUIRED STRAPS



DEBUG STRAPS



REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	AZ_SDOUT#	PCI_CLK1	PCI_CLK2	PCLK_KBC (PCI_CLK3)	PCLK_FWH (PCI_CLK4)	LPCCLK0	LPCCLK1	SB_GPO200 , SB_GPO199 ROM TYPE:
PULL HIGH	LOW POWER MODE	Allow PCIE GEN2 DEFAULT	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	non_Fusion CLOCK mode DEFAULT	ENABLE EC	CLKGEN ENABLED (Use Internal)	H, H = Reserved H, L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	Force PCIE GEN1	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode	DISABLE EC DEFAULT	DEFAULT CLKGEN DISABLED (Use External)	L, H = LPC ROM DEFAULT L, L = FWH ROM

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: SB820M has 15K internal PU FOR PCI_AD[27:23]

<Core Design>

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Title: **SB820M_STRAPPING_(5/5)**

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<Core Design>

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Reserved		
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(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size	Document Number	Rev
	Berry AMD Discrete/UMA	A00
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(Blanking)

<Core Design>

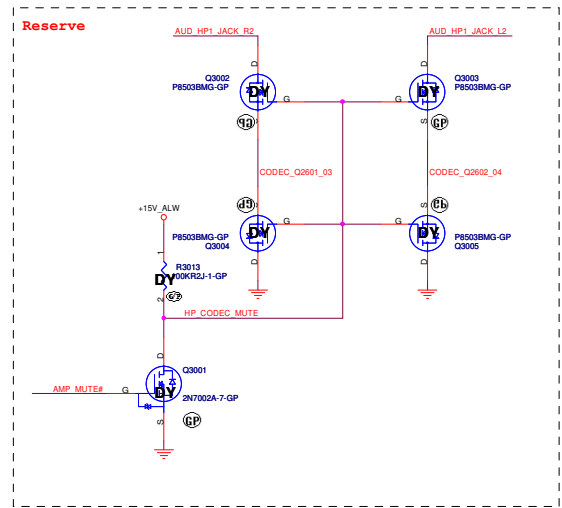
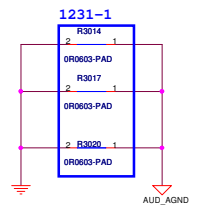
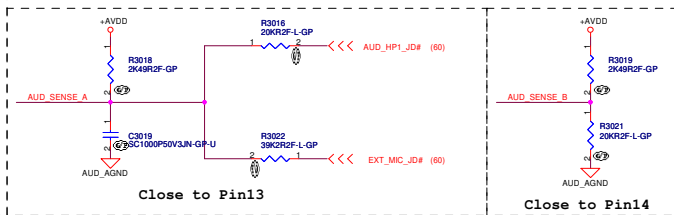
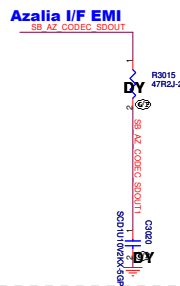
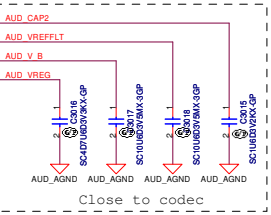
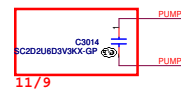
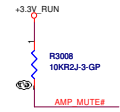
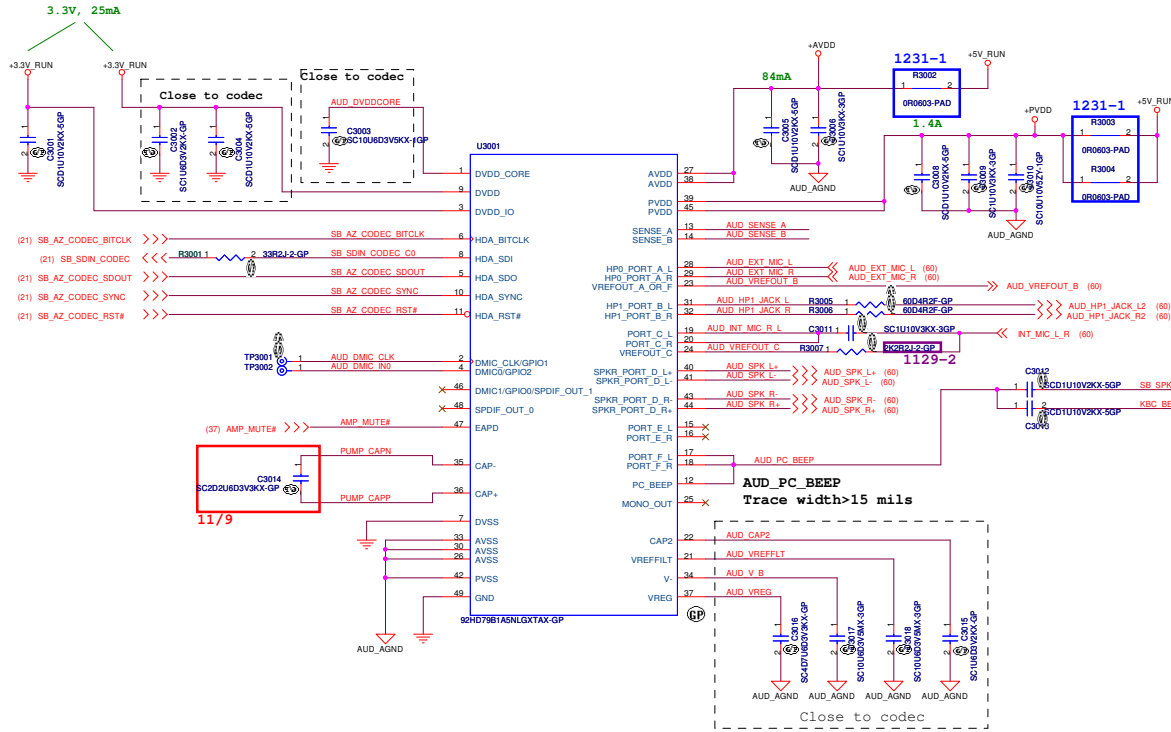
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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<Core Design>


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Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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(Blanking)

<Core Design>



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A4

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(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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(Blanking)

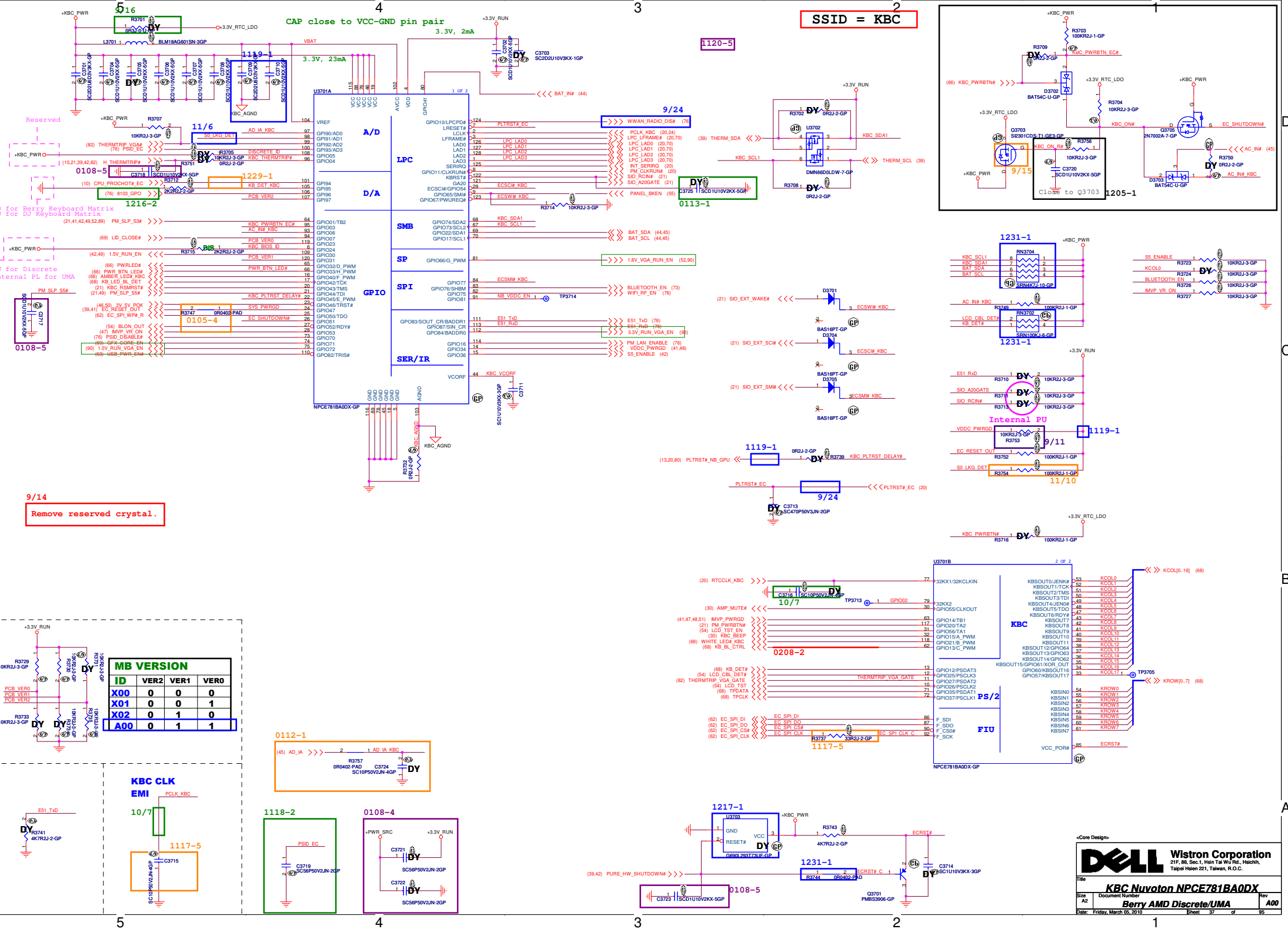
<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
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(Blanking)

<Core Design>

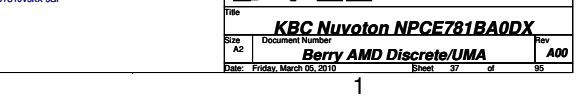
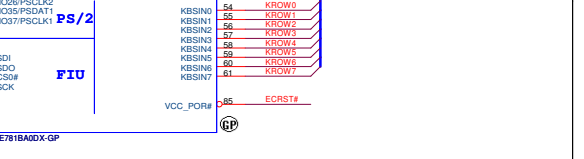
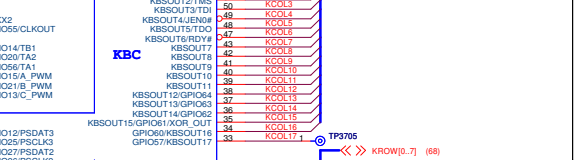
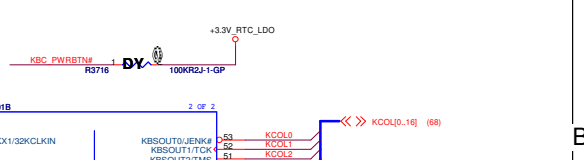
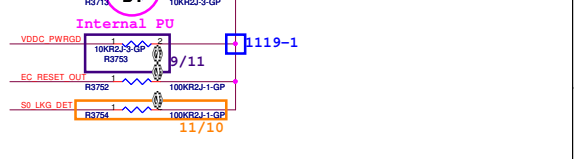
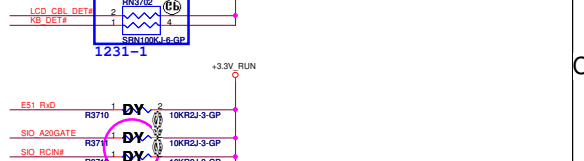
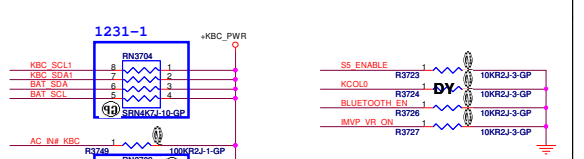
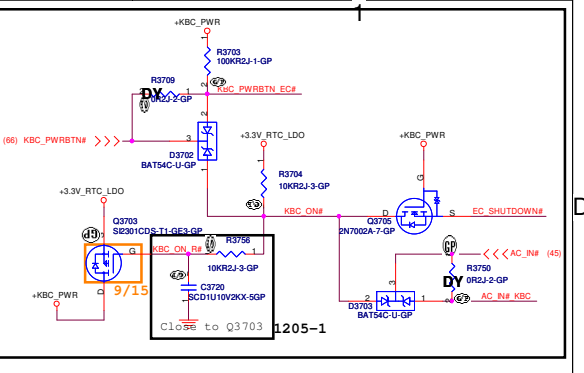
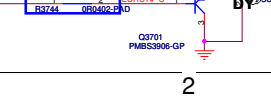
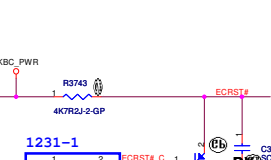
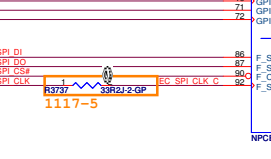
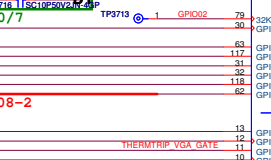
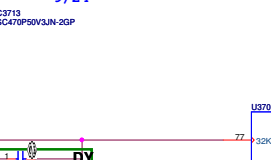
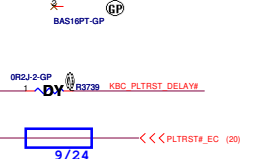
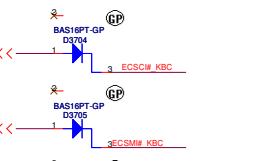
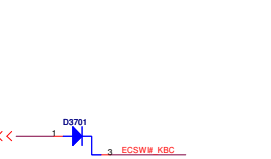
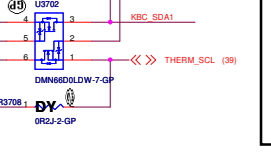
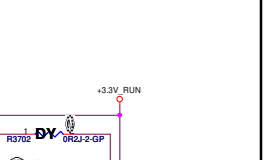
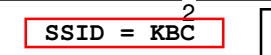
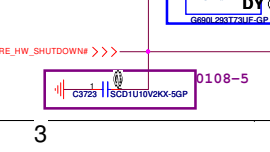
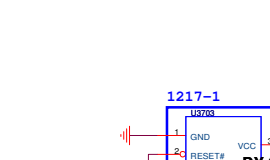
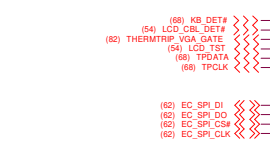
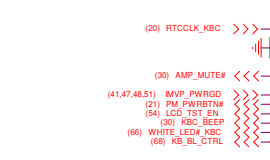
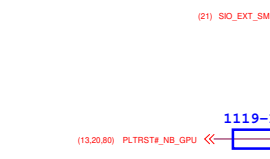
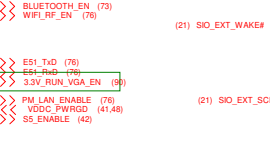
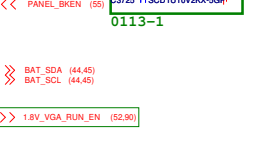
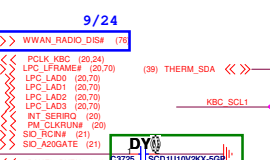
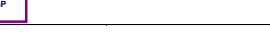
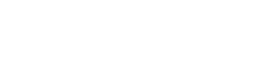
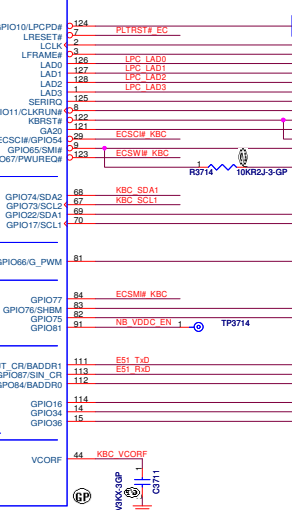
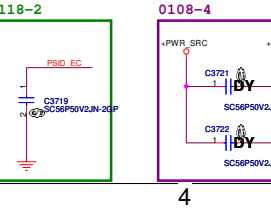
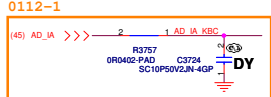
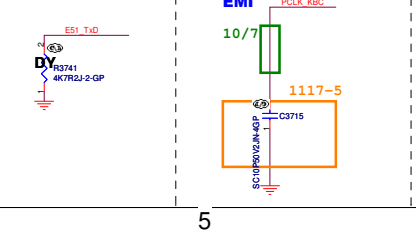
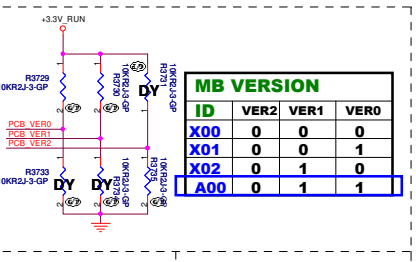
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 36 of 95



PD for Berry Keyboard Matrix for BJ Keyboard Matrix

PU for Discrete Internal PL for UMA

9/14 Remove reserved crystal.



Core Design

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File: **KBC Nuvoton NPC781BA0DX**
 Size: **A2**
 Date: Friday, March 05, 2010

Documen Number: **Berry AMD Discrete/UMA**
 Sheet: 37 of 95

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Berry AMD Discrete/UMA A00

Rev

Date: Thursday, March 04, 2010

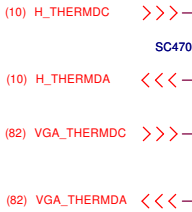
Sheet 38 of 95

SSID = Thermal

Please near to CPU side

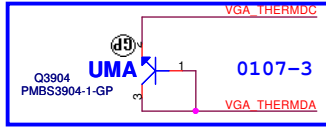
1. For CPU Sensor

Layout notice:
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing



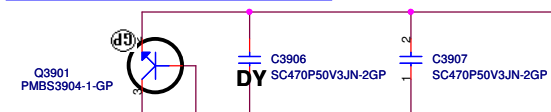
2. VGA Sensor

Layout notice:
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing



3. HW T8 sensor

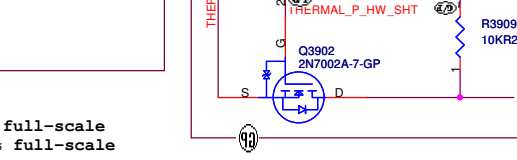
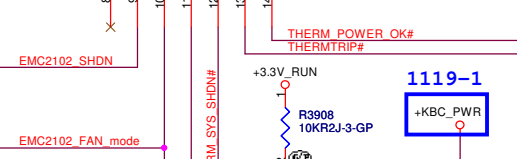
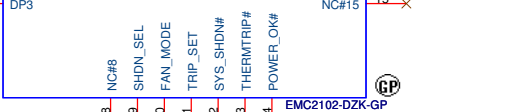
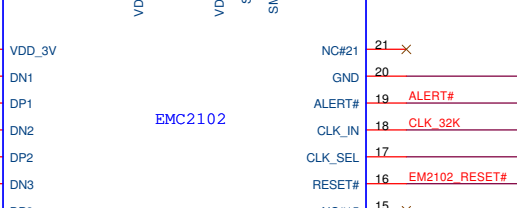
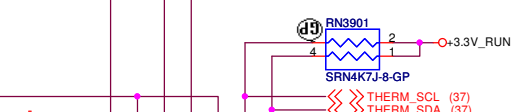
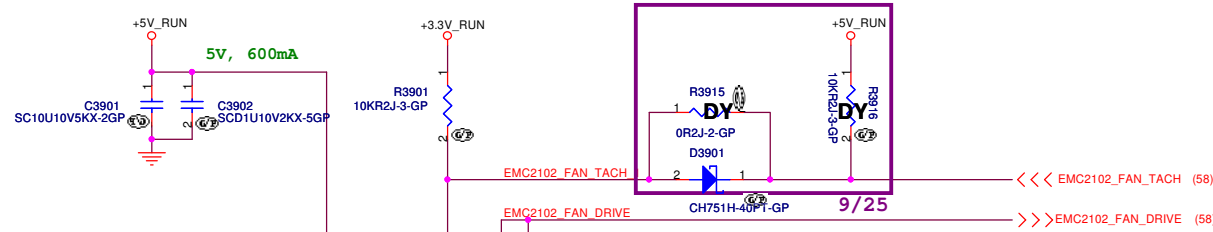
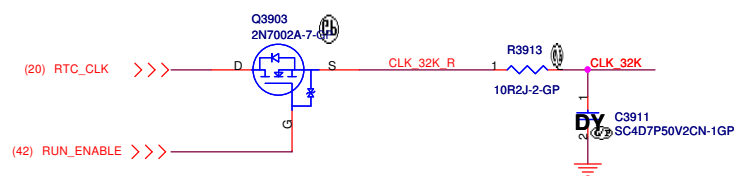
Layout notice:
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.



GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

32K suspend clock output



GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$
T8 shutdown is 88 deg-C.

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.


Title: **Thermal/Fan Controller EMC2102**

Size A3	Document Number	Rev
	Berry AMD Discrete/UMA	A00

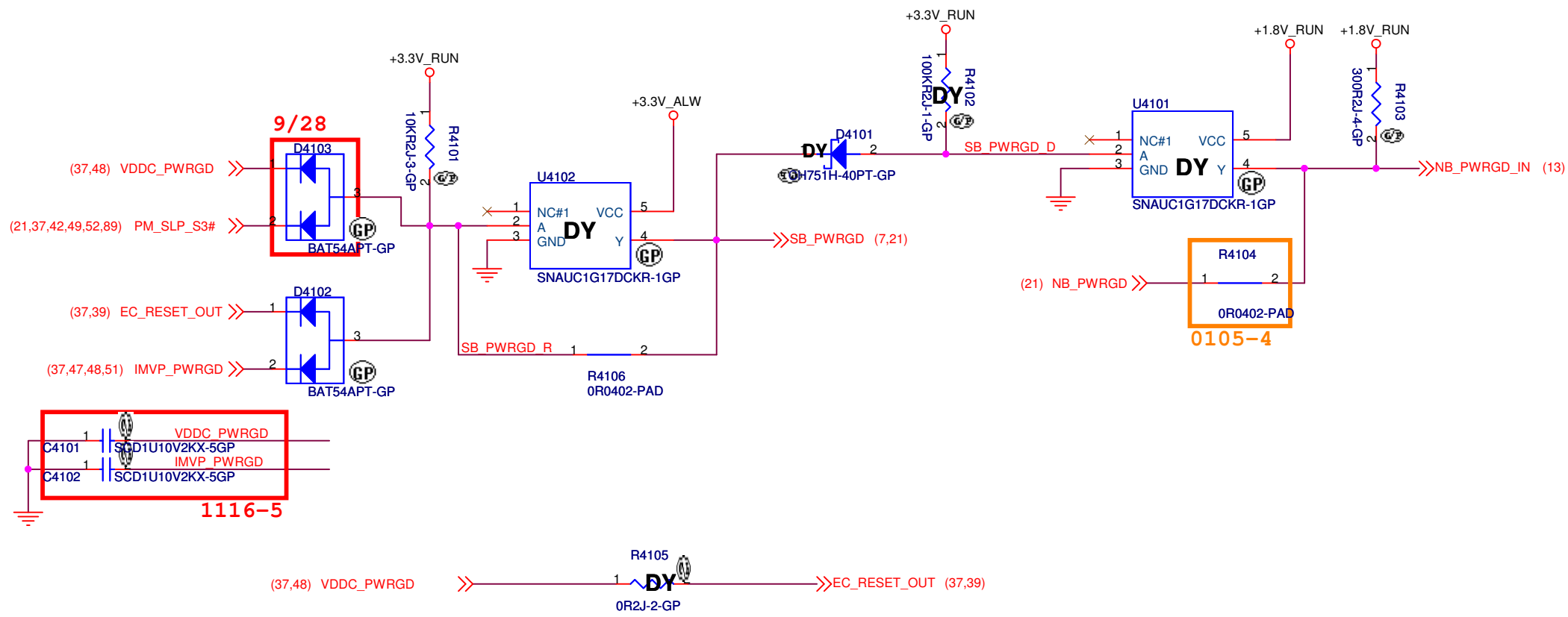
Date: Thursday, March 04, 2010 Sheet 39 of 95

(Blanking)


<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 40	of 95

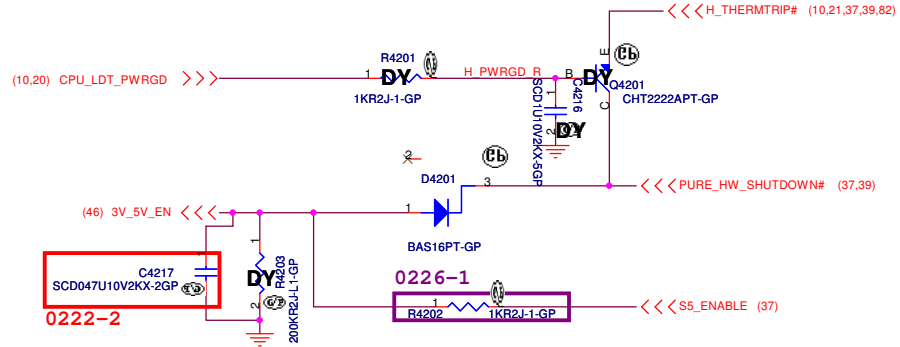
SSID = Reset.Suspend



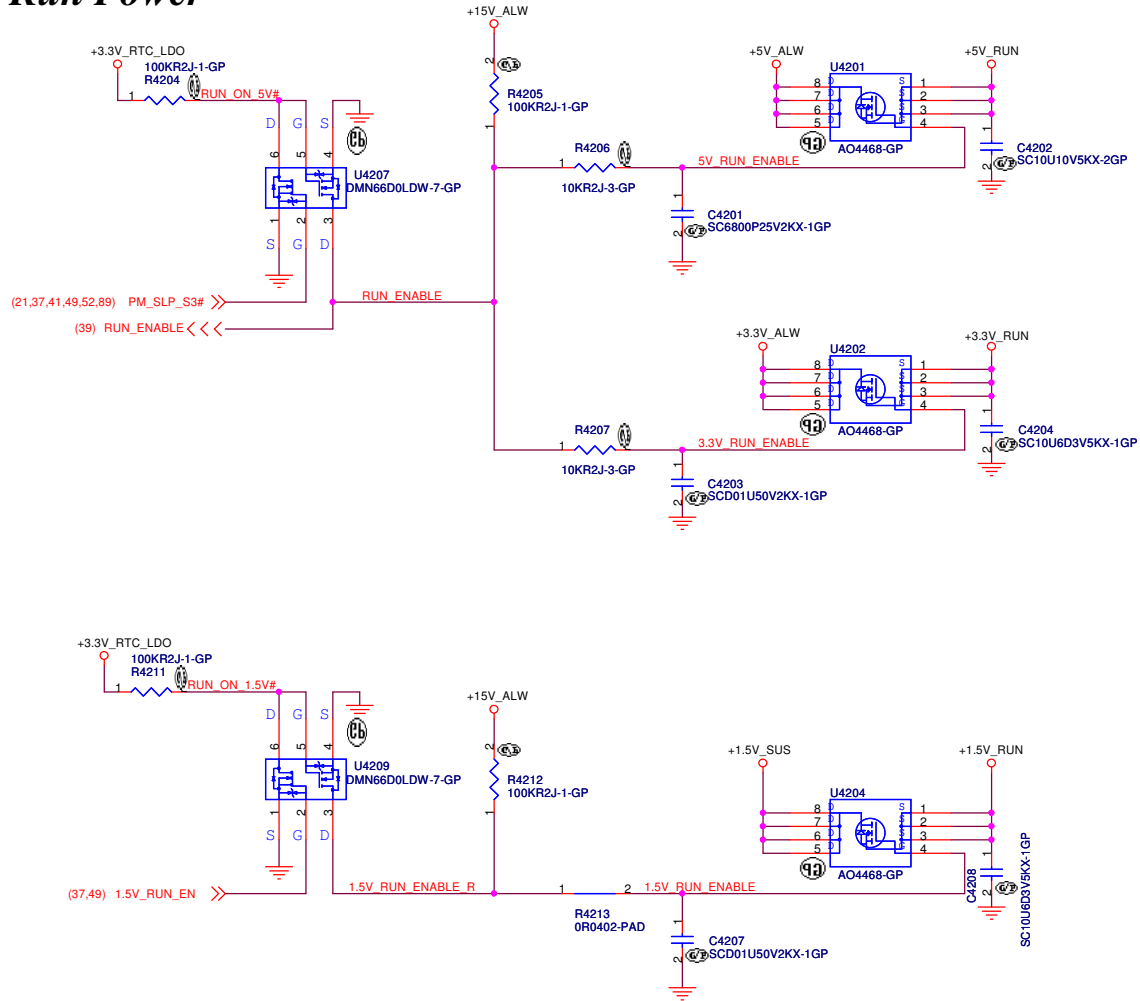
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Power On Logic	
Size A4	Document Number Berry AMD Discrete/UMA	Rev A00	
Date: Thursday, March 04, 2010		Sheet 41 of 95	

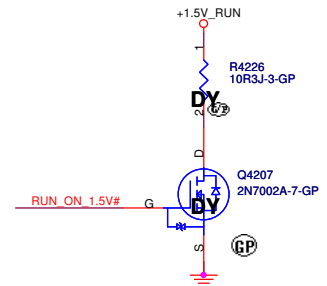
SSID = Reset . Suspend



Run Power



1117-2
Remove



<Core Design>


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Title: **Power Plane Enable**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 42 of 95	

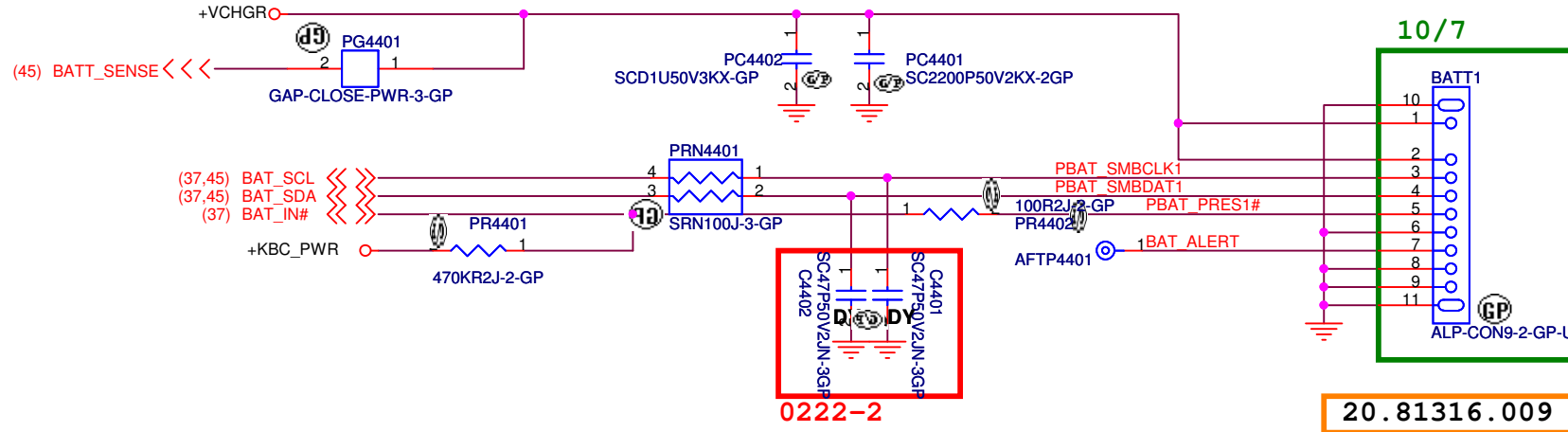
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 43	of 95

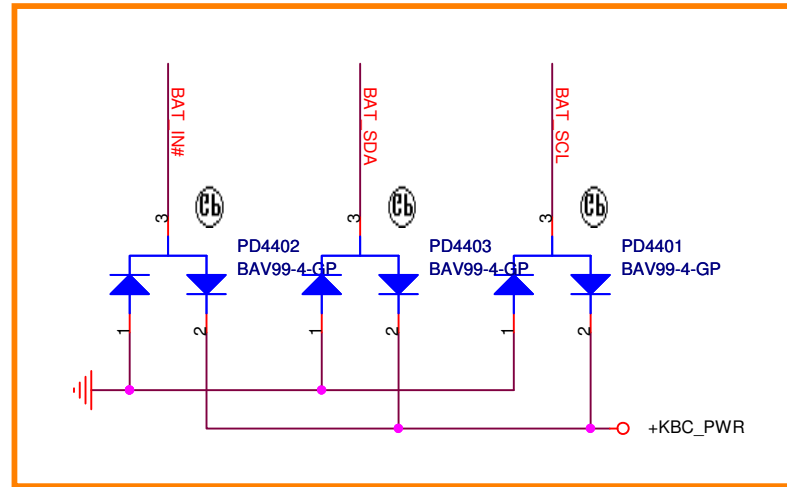
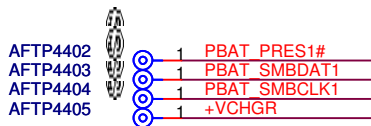
SSID = BATT CONN

Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector

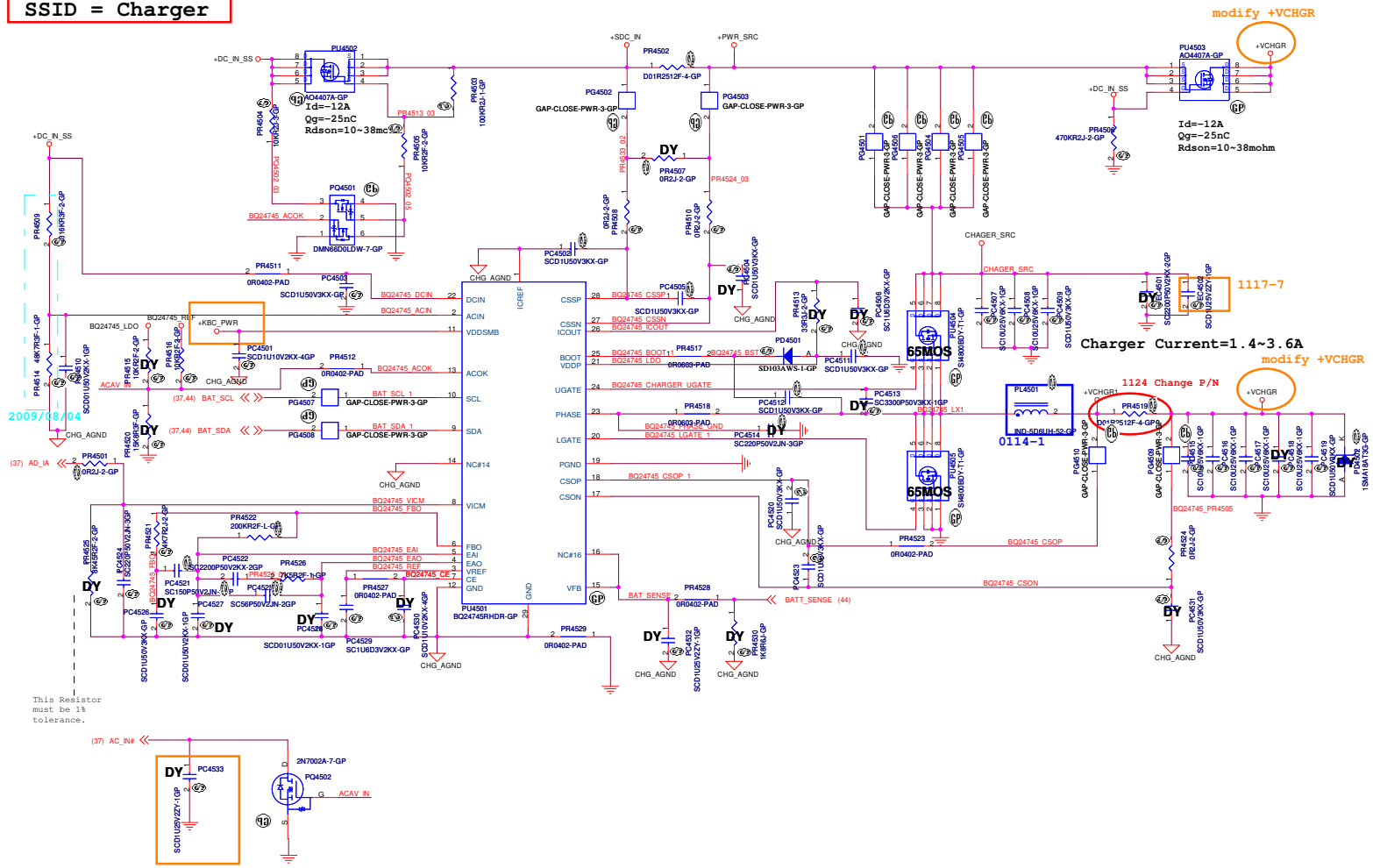


<Core Design>



Title		
BATT CONN		
Size A4	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 44 of 95	

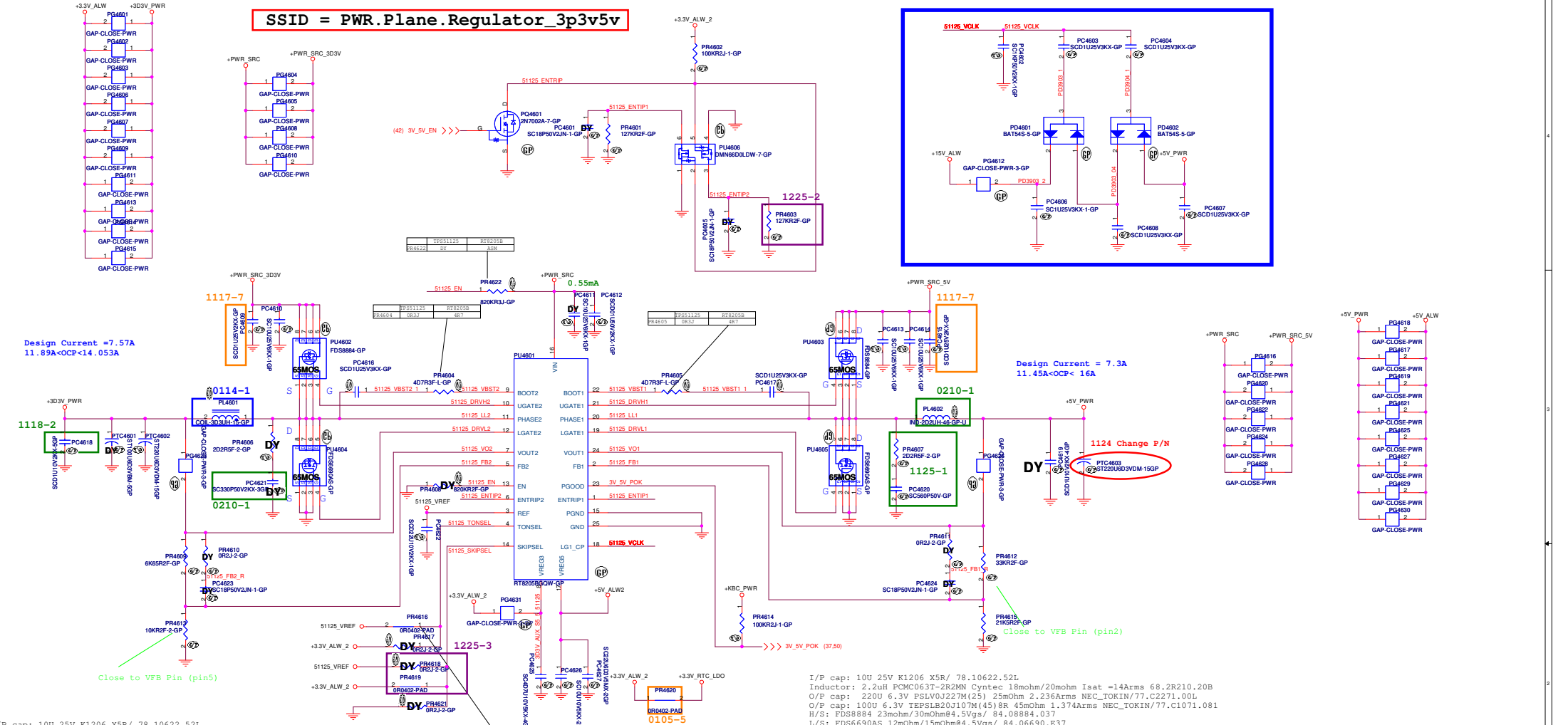
SSID = Charger



20097/08/04

This Resistor must be 1% tolerance.

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
 Inductor: 3.3uH PCMC063T-3R3MN Cynotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
 O/P cap: 220u 6.3V FSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
 O/P cap: 100u 6.3V TEPSLB20J107M(45)8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
 H/S: FDS8884 23mohm/30mohm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS 12mohm/15mohm@4.5Vgs/ 84.06690.E37

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
 Inductor: 2.2uH PCMC063T-2R2MN Cynotec 18mohm/20mohm Isat =14Arms 68.2R210.20B
 O/P cap: 220u 6.3V FSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
 O/P cap: 100u 6.3V TEPSLB20J107M(45)8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
 H/S: FDS8884 23mohm/30mohm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS 12mohm/15mohm@4.5Vgs/ 84.06690.E37

TPS51125		
TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B (4.08298.A73)		
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

TPS51125	74.51125.073
RT8205BQGW	74.08208.A73

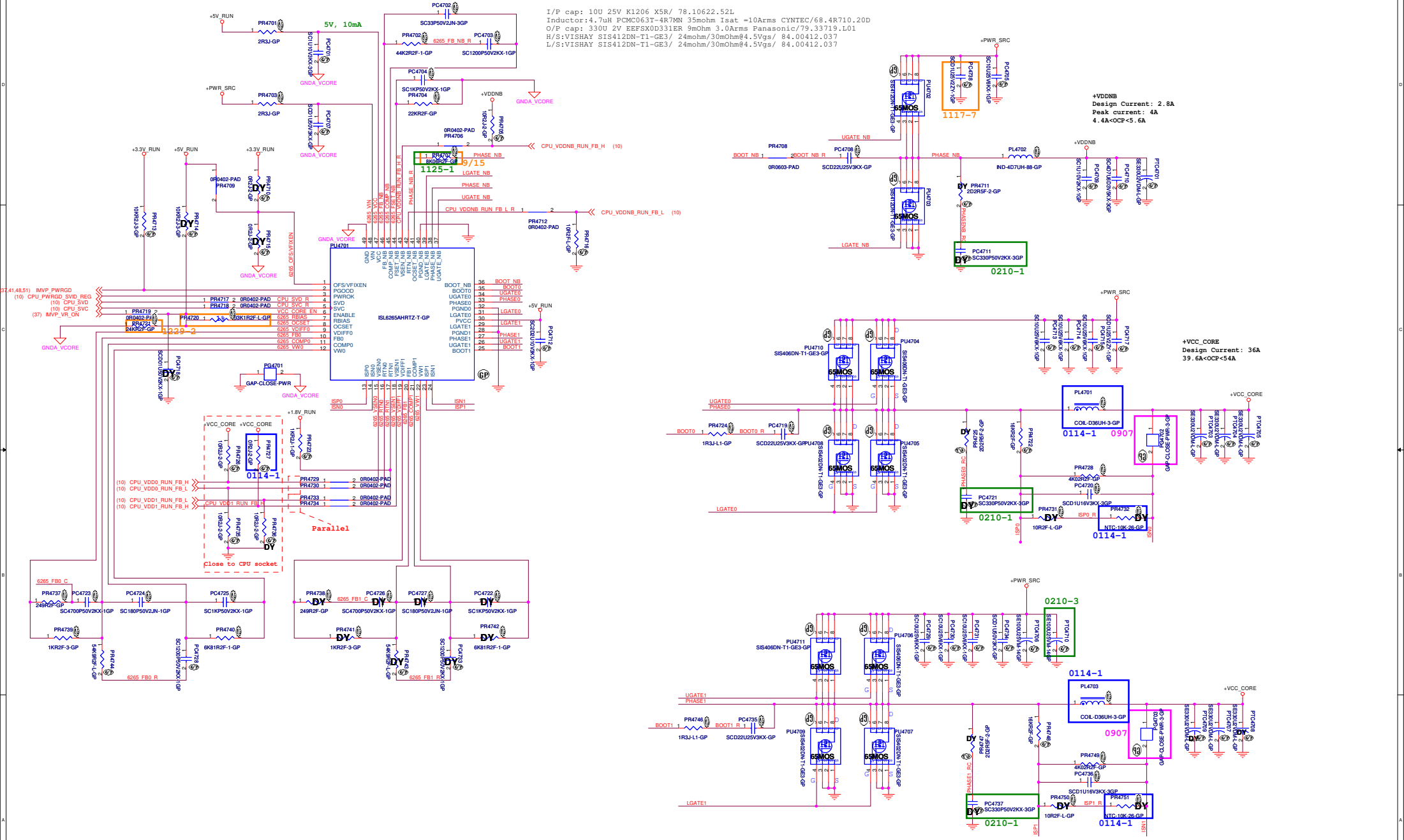
TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only

ENO	Operating Mode	820kΩ to GND	GND
Open	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

SSID = CPU.Regulator

ISL6265HRTZ-T for +VCC_CORE&+VDDNB

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 4.7uH PCMC063T-4R7MN 35mohm Isat =10Arms CYNTEC/68.4R710.20D
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
 L/S:VISHAY SIS412DN-T1-GE3/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36uH PCMC104T-R36MN1R05J CYNTEC DCR 1.05(+5%~-5%)mohm
 Isat =60Arms 68.R3610.20C
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S:VISHAY SIR462DP/ POWERPAK-8.2/810mOhm/ 4.5Vgs/ 84.00462.037
 L/S:VISHAY SI7658AD/ POWERPAK-2.3/ 2.8mOhm/ 4.5Vgs/ 84.07658.037

-Core Design-

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File: **VREG : +VCC_CORE&+VDDNB**
 Size: Document Number
 AZ: **Berry AMD Discrete/UMA** Rev: **A00**
 Date: Thursday, March 04, 2010 Sheet: 47 of 95

SSID = PWR.Plane.Regulator_+1.1V_RUN

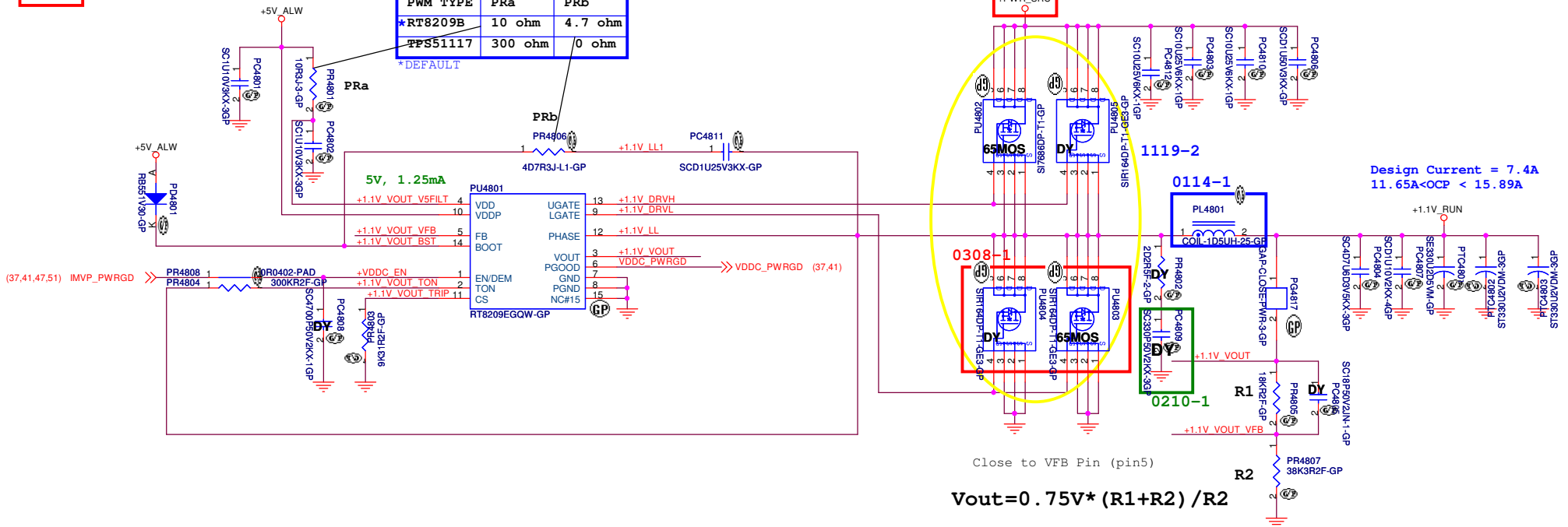
1117-2

RT8209EGQW for +1.1V_RUN

0222-3
Remove

PWM TYPE	PRa	PRb
*RT8209B	10 ohm	4.7 ohm
PPS51117	300 ohm	0 ohm

*DEFAULT

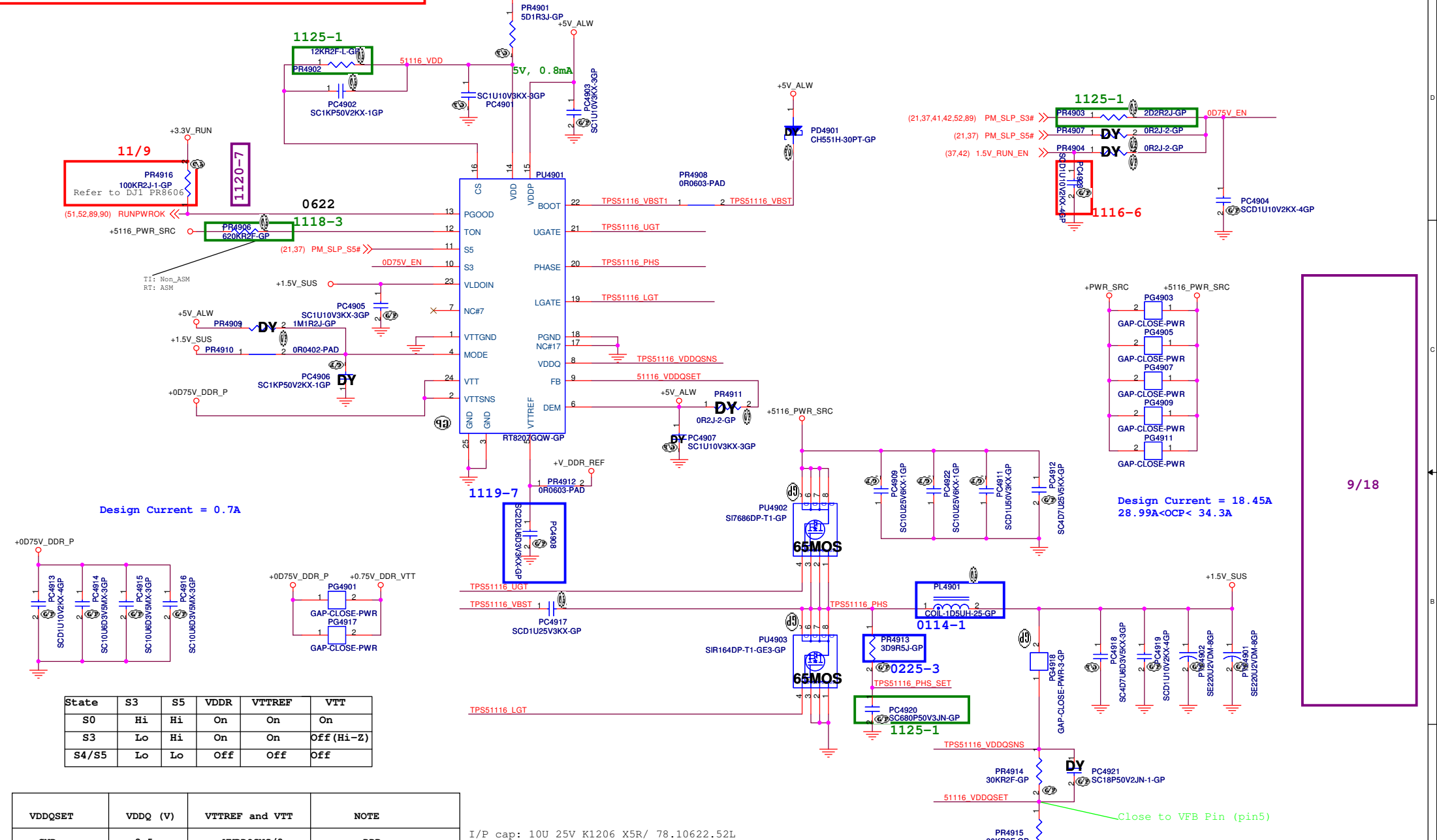


I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH PCMC104T-1R5MN 33Arms CYNTEC/ 68.1R510.10J
 O/P cap: 330U 2.5V EEFC0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title RT8209E_+1.1V_RUN	
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00	
Date: Monday, March 08, 2010		Sheet 48 of 95	

SSID = PWR.Plane.Regulator_1p5v0p75v



Design Current = 0.7A

Design Current = 18.45A
28.99A < OCP < 34.3A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UHPMC104T-1R5MN DCR:3.8/4.2mohm Isat =33Arms Cyntec/ 68.1R510.10U
 O/P cap: 220U 2V EEFX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
 H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: SiR164DP/ POWERPAK-8/ 2.6mOhm/3.2mohm@4.5Vgs/ 84.00164.037

<Core Design>

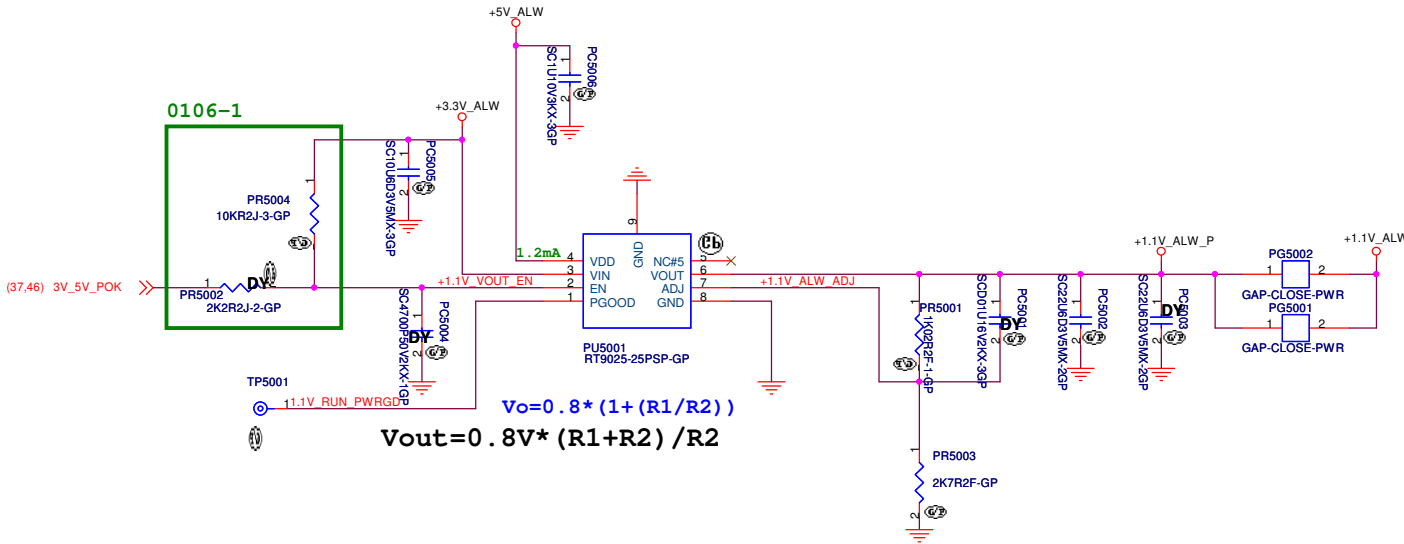
Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8207 +1.5V SUS**

Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 49 of 95	

SSID = PWR.Plane.Regulator_+1.1V_ALW

1117-2
RT9025 for +1.1V_ALW



$$V_o = 0.8 * (1 + (R_1/R_2))$$
$$V_{out} = 0.8V * (R_1 + R_2) / R_2$$

<Core Design>

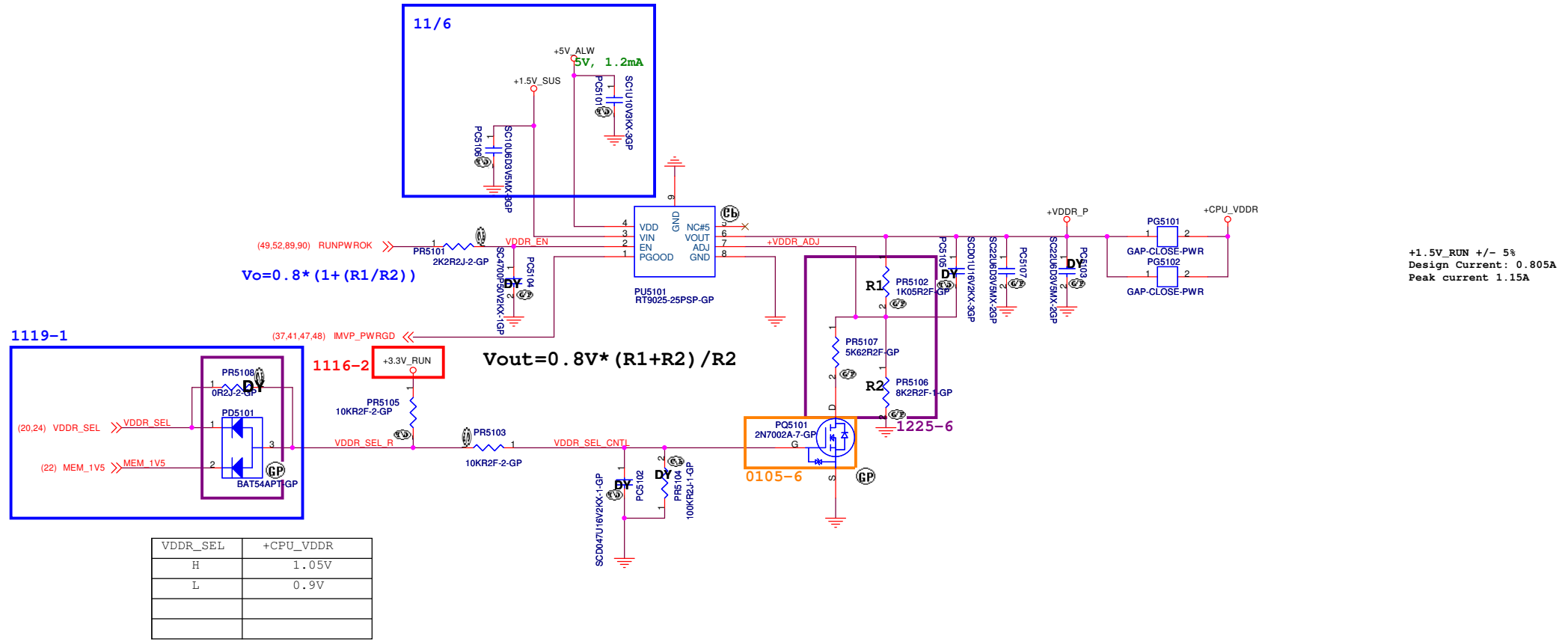
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT9025_+1.1V_ALW**

Size: A3	Document Number:	Rev: A00
Date: 11/03/2010	March 04, 2010	Sheet 50 of 95

SSID = PWR.Plane.Regulator_VDDR

RT9025 for +VDDR



VDDR_SEL	+CPU_VDDR
H	1.05V
L	0.9V

<Core Design>

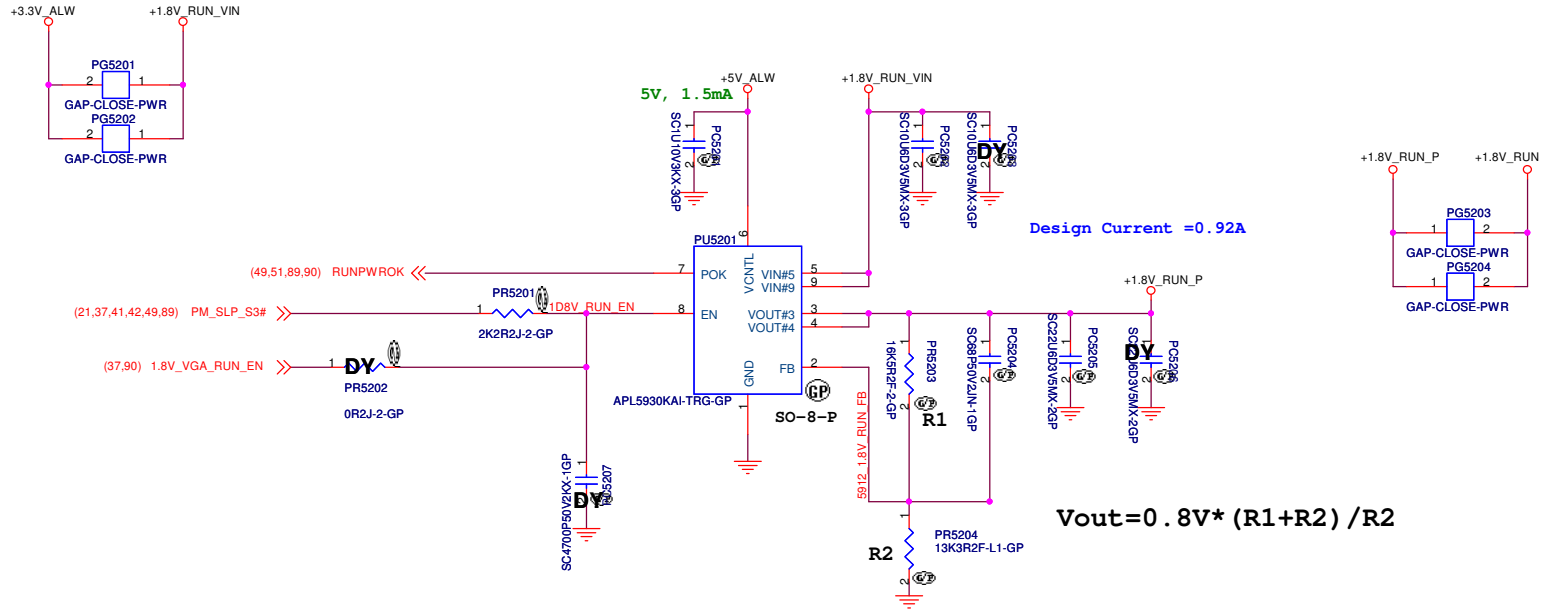
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT9025 +VDDR**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 51	of 95

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



SSID = PWR.Plane.Regulator_1p8v

<Core Design>

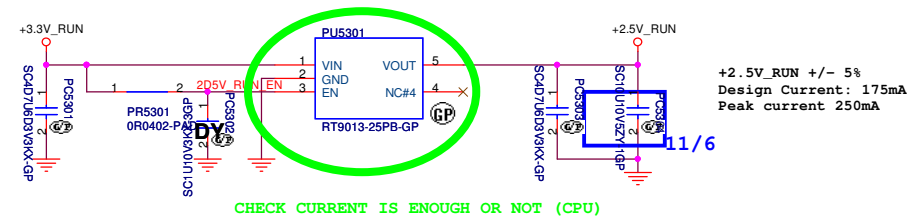


Title APL5930 +1.8V RUN		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 52	of 95


SSID = PWR.Plane.Regulator_0P9v

SSID = PWR.Plane.Regulator_2p5v

RT9013-25PB for +2.5V_RUN

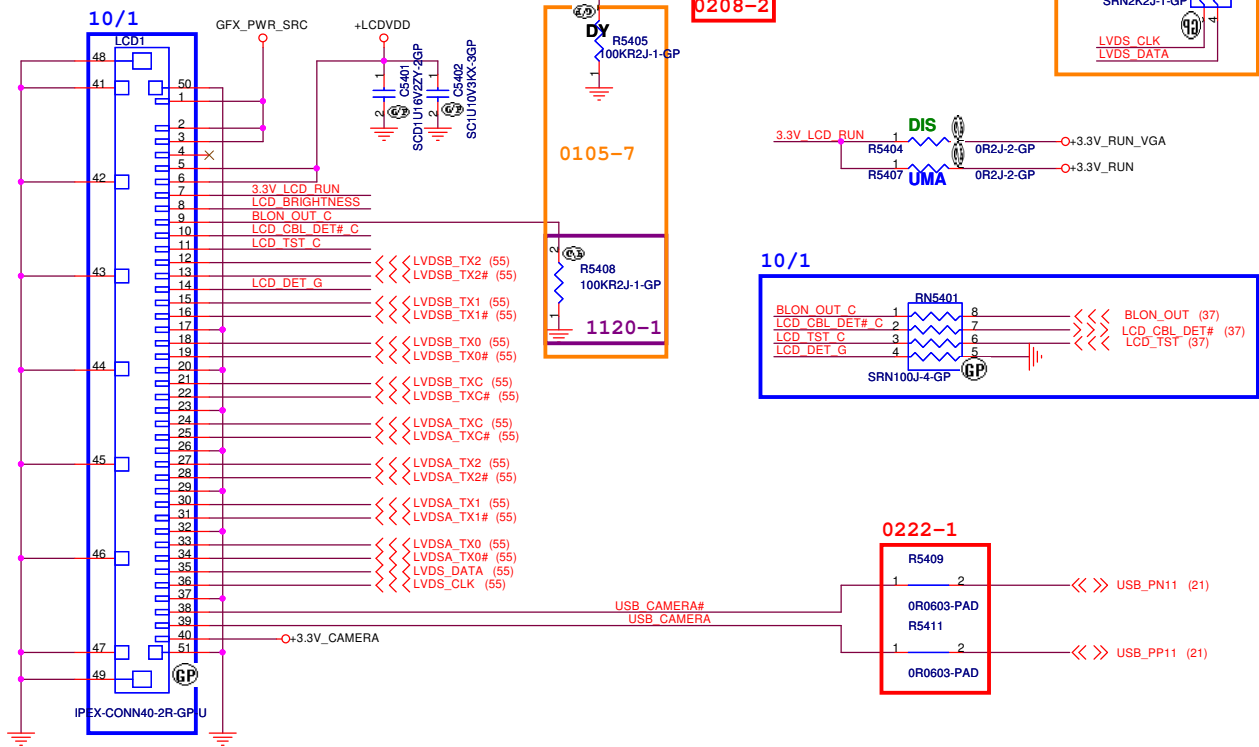


<Core Design>

			Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title VREG : +CPU_VDDR&+2.5V_RUN					
Size A3	Document Number Berry AMD Discrete/UMA				Rev A00
Date: Thursday, March 04, 2010		Sheet 53		of 95	

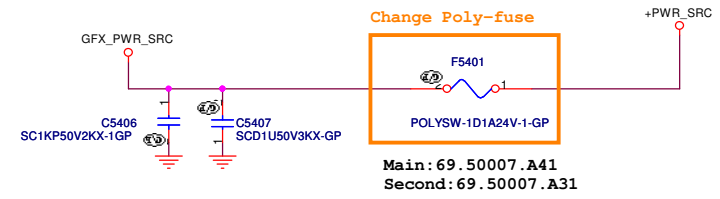
SSID = VIDEO

LVDS CONNECTOR



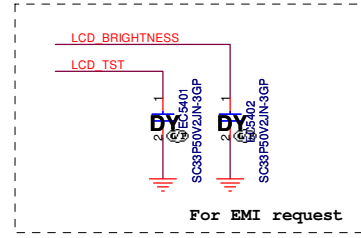
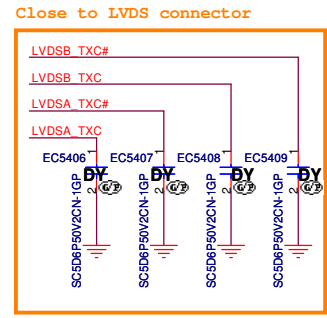
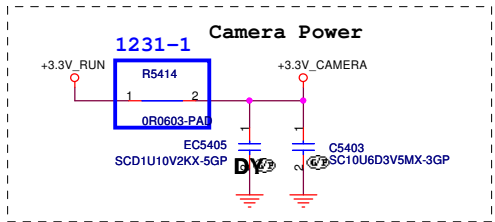
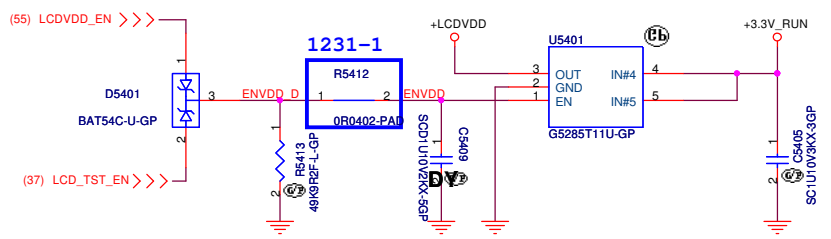
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



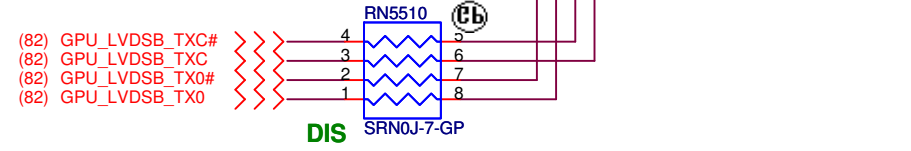
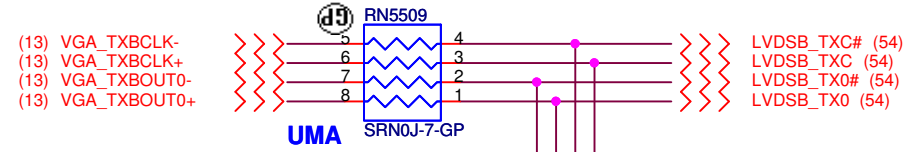
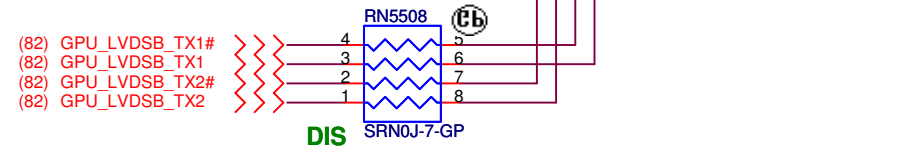
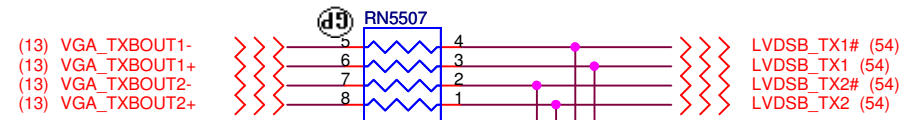
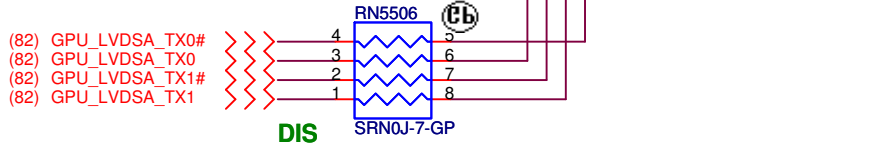
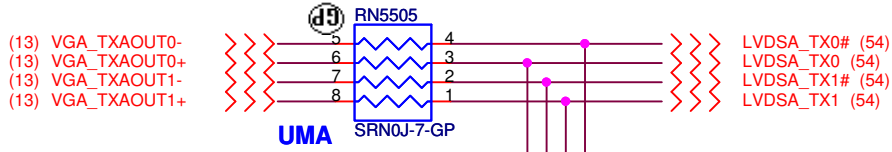
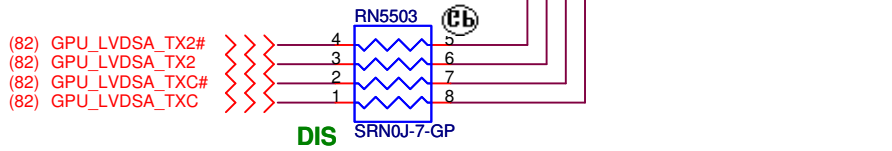
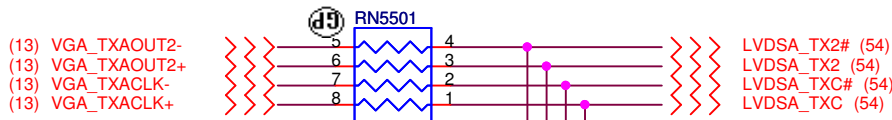
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

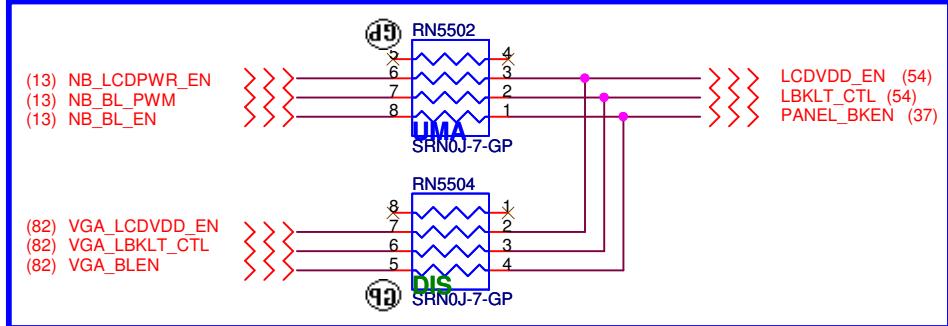
File: **LCD/Inverter Connector**

Size A3	Document Number	Rev
	Berry AMD Discrete/UMA	A00
Date: Thursday, March 04, 2010	Sheet 54 of	95

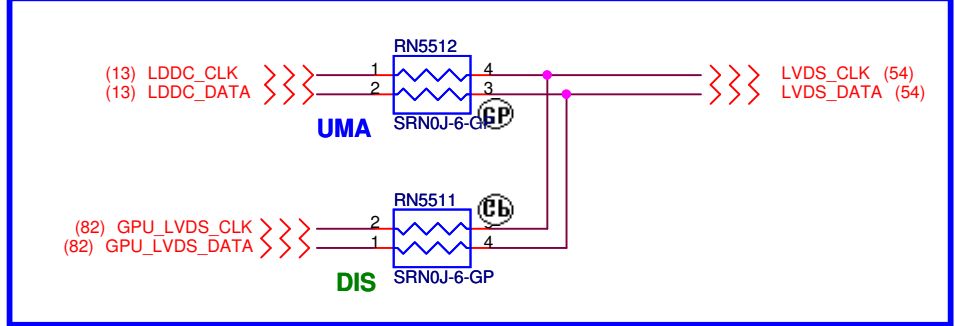
SSID = VIDEO




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10/1




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h3 style="text-align: center;">LVDS Switch</h3>	
Size	Document Number	Rev	
Berry AMD Discrete/UMA		A00	
Date: Thursday, March 04, 2010	Sheet 55	of	95

(Blanking)

<Core Design>

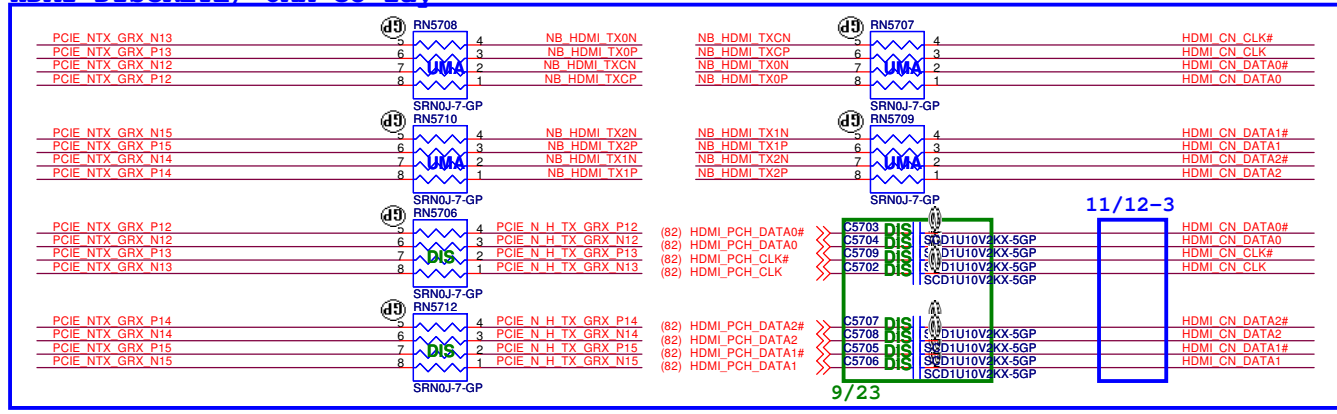
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 56 of 95

SSID = VIDEO

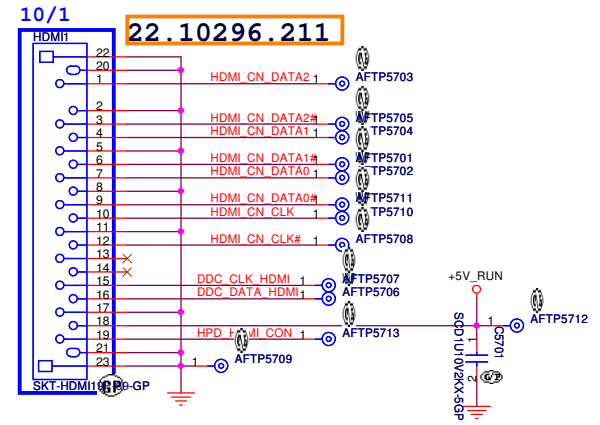
HDMI CONNECTOR



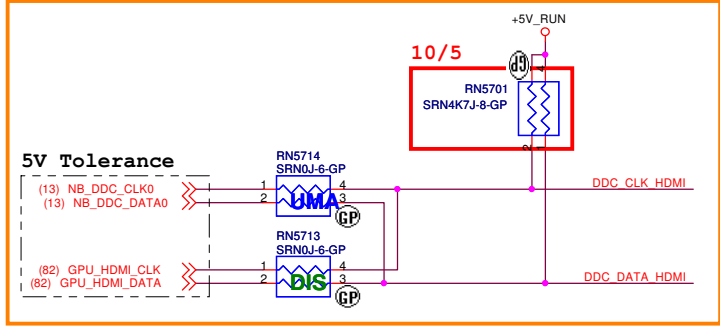
HDMI DISCRETE/ UMA Co-lay



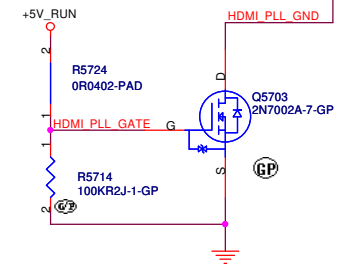
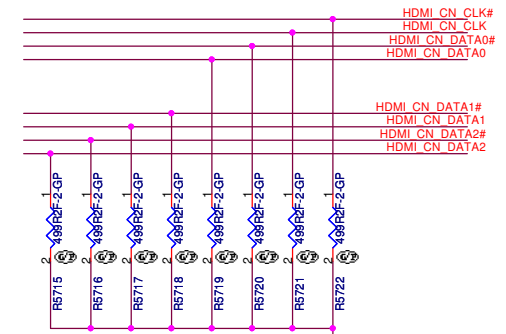
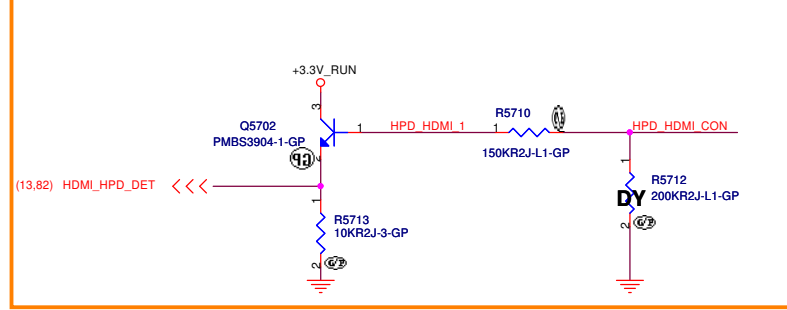
HDMI CONN



9/15



9/22



<Core Design>

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

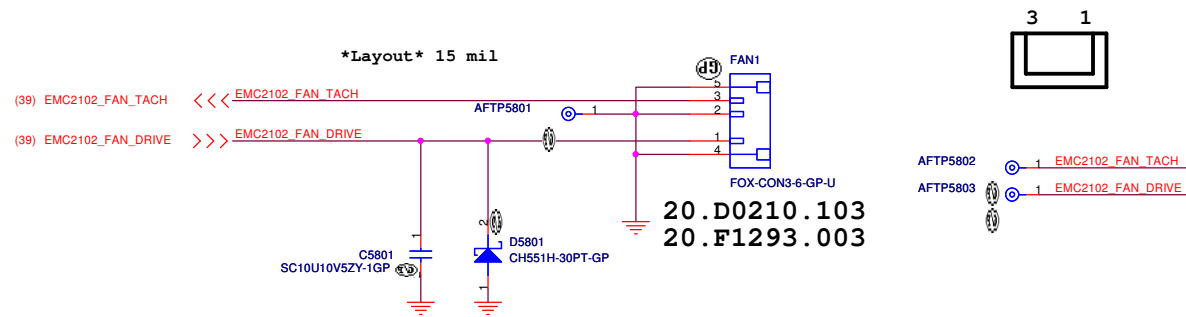
Title: **HDMI Level Shifter/Connector**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 57	of: 95

SSID = User.Interface

SSID = Thermal

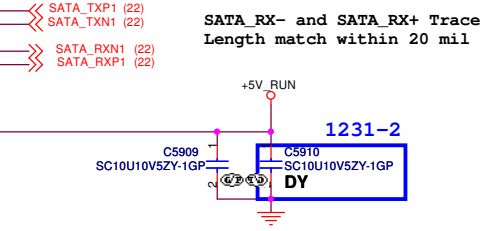
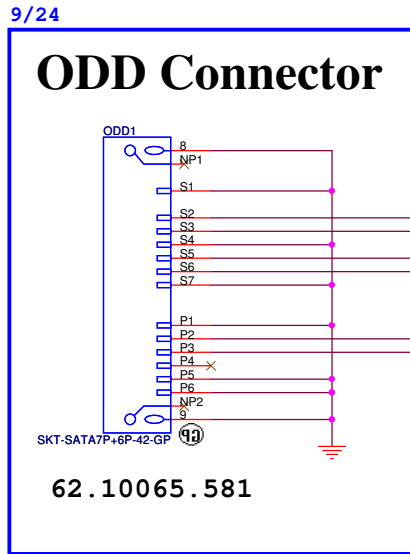
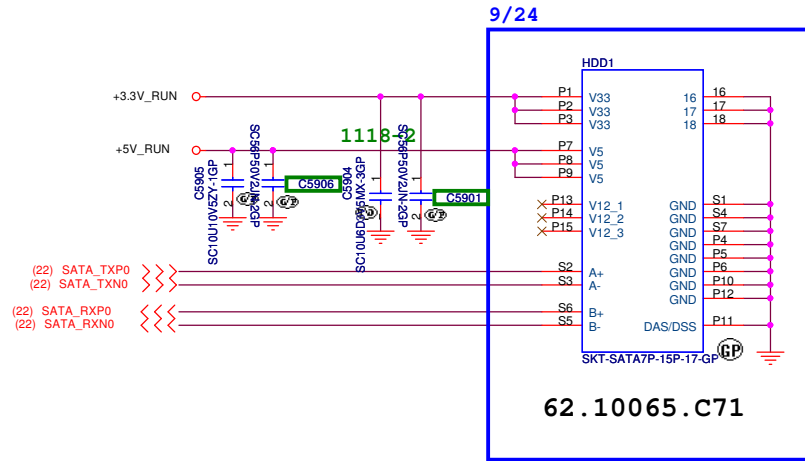
Fan Connector



<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title ITP/Fan Connector		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010 Sheet 58 of 95		

SATA HDD Connector

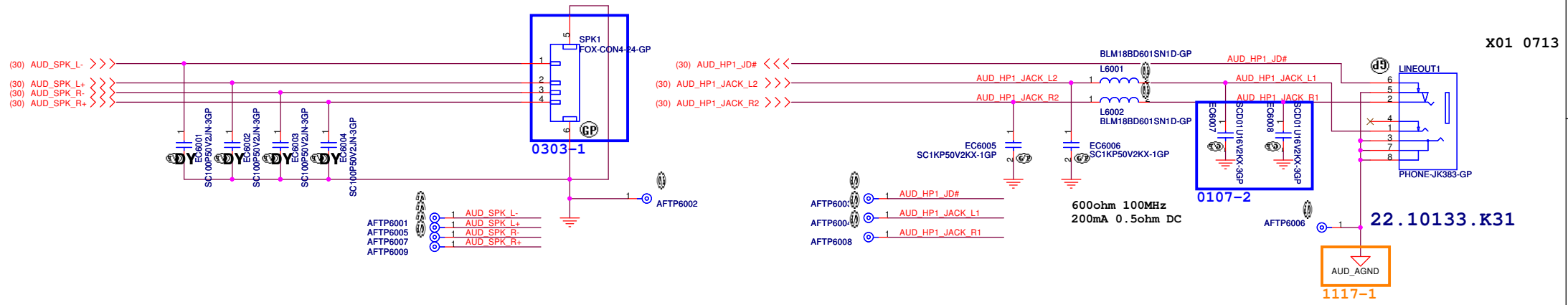


SSID = AUDIO

Speaker Connector

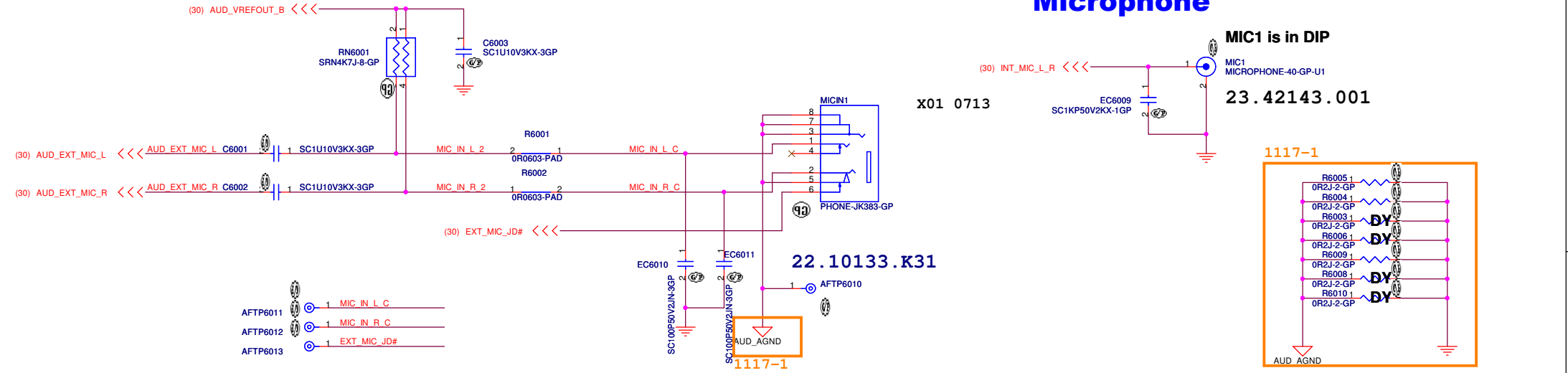
Main 20.F0693.004
SEC. 20.F0693.004

LINE1 OUT



MIC IN

Internal Microphone



<Core Design>


DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

Size: A3	Document Number: Berry	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 60	of: 95

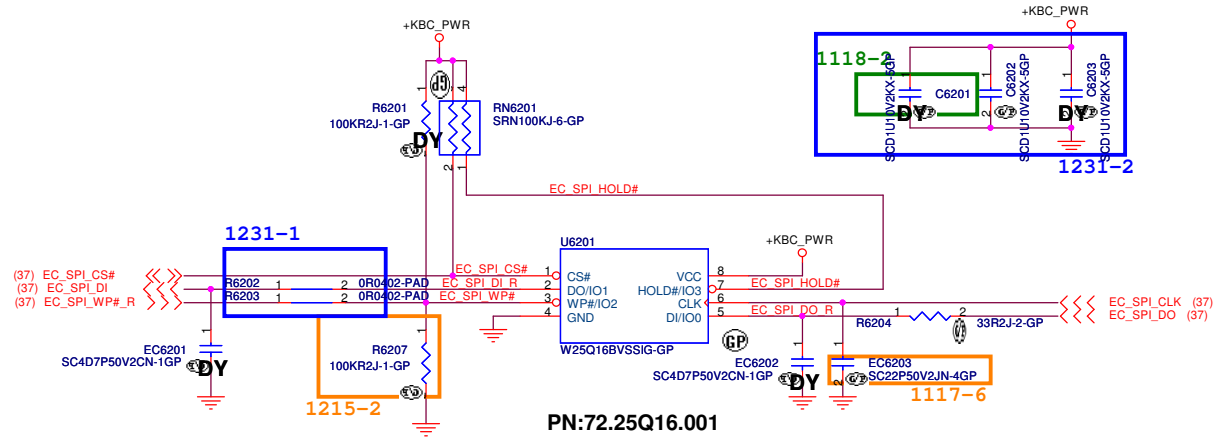
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 61 of 95

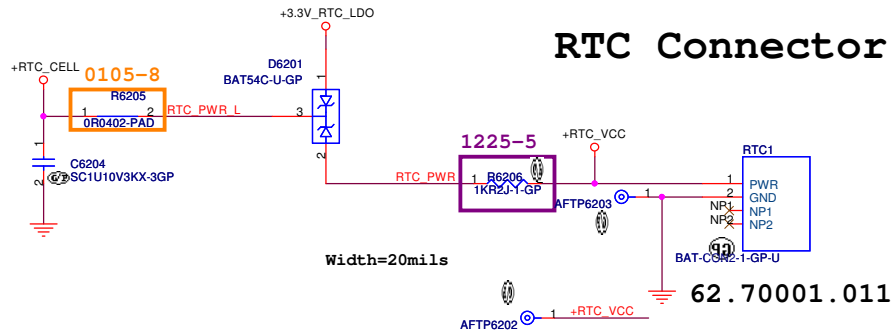
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



<Core Design>

DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

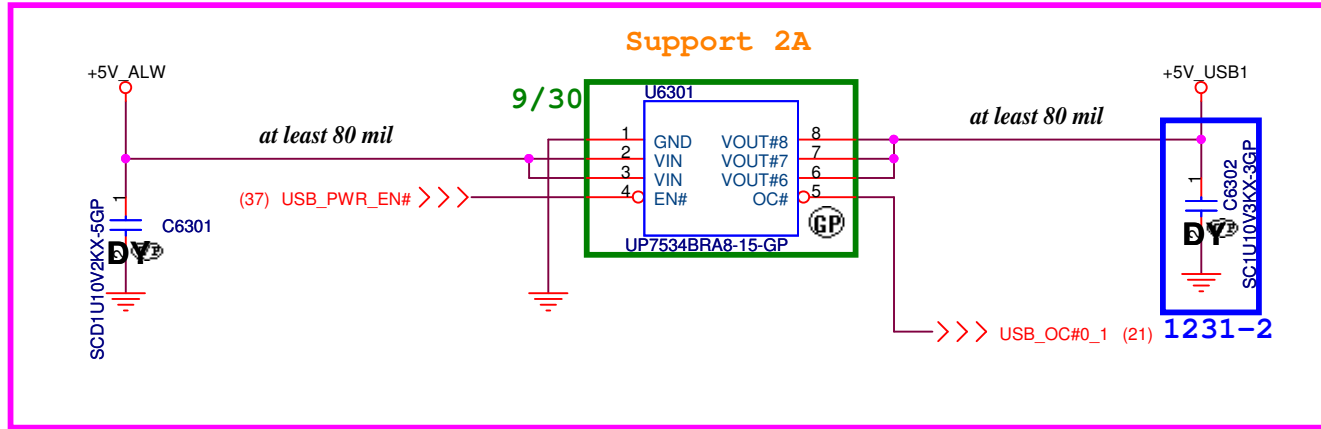
Title: **Flash/RTC**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 62	of: 95

SSID = USB

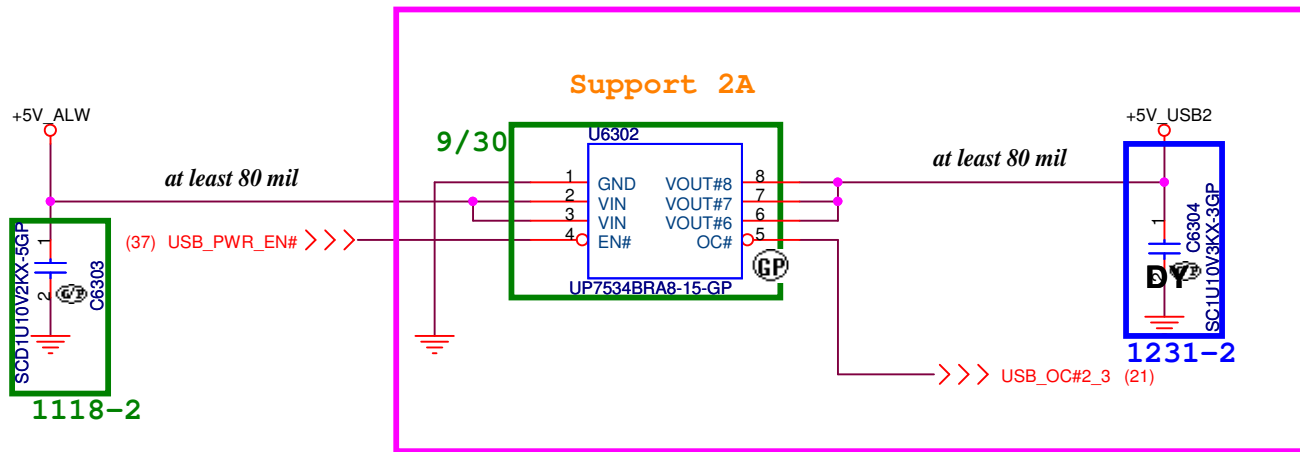
IO Board USB Power

Close to I/O connector



CRT Board USB Power

Close to CRT Board connector



<Core Design>



Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB Power SW		
Size	Document Number	Rev
Berry AMD Discrete/UMA		A00
Date	Thursday, March 04, 2010	Sheet 63 of 95

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Berry AMD Discrete/UMA


Rev
A00

Date: Thursday, March 04, 2010

Sheet 64 of 95

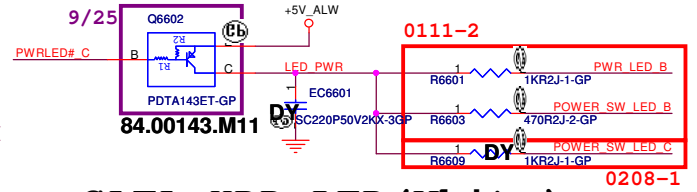
(Blanking)

<Core Design>

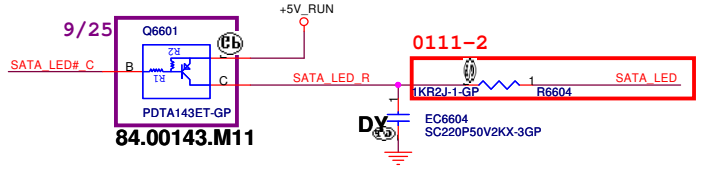
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 65 of 95

SSID = User.Interface

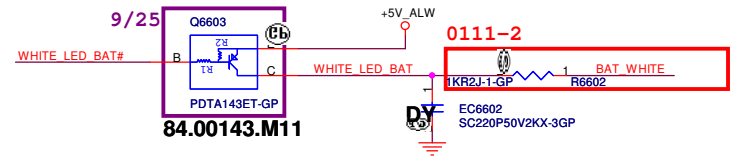
Power LED (White)



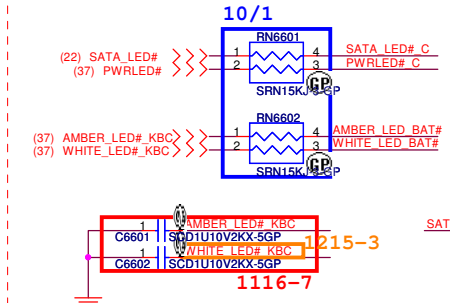
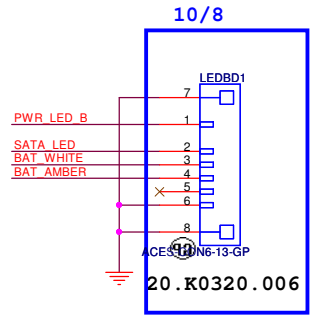
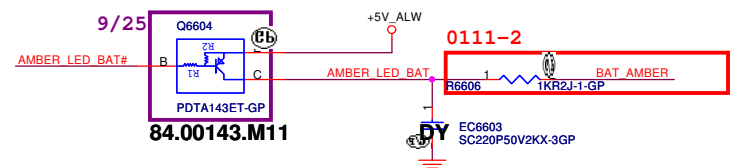
SATA HDD LED (White)



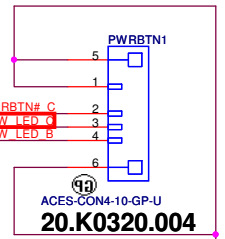
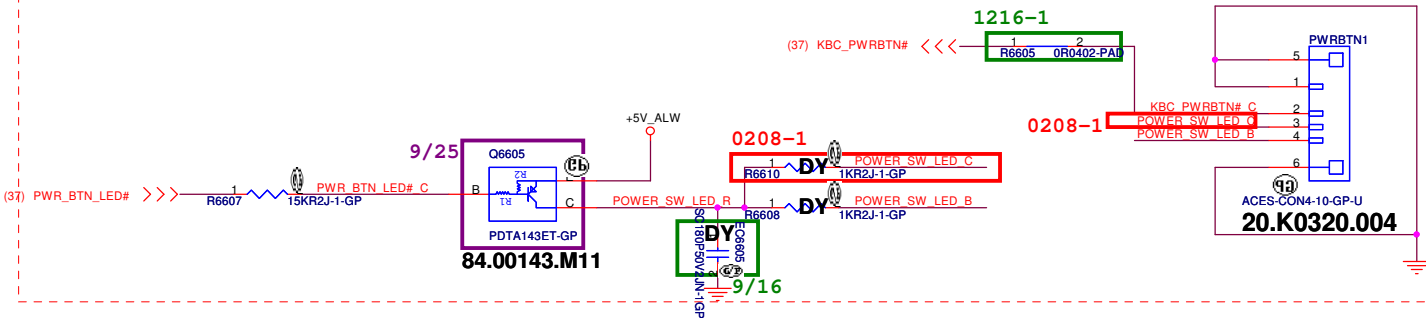
Battery LED1 (White)



Battery LED2 (Amber)




Power button LED (White)



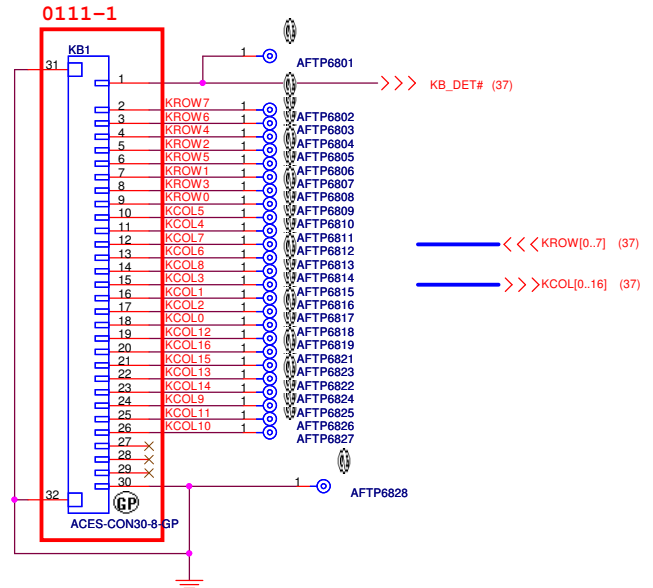
(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010	Sheet 67	of 95

SSID = KBC

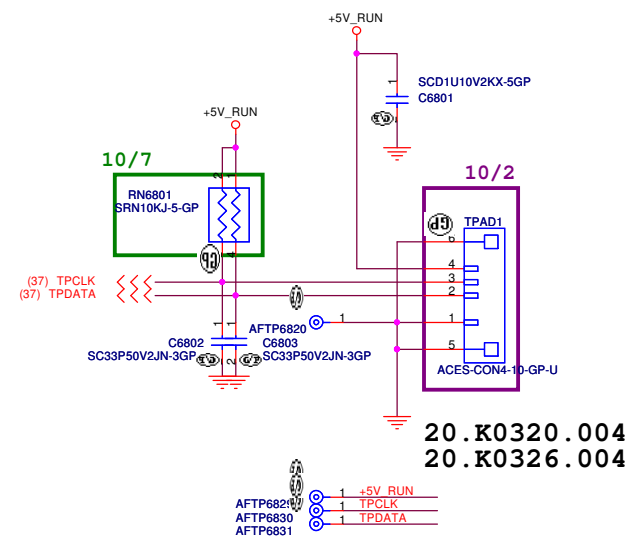
Internal Keyboard Connector



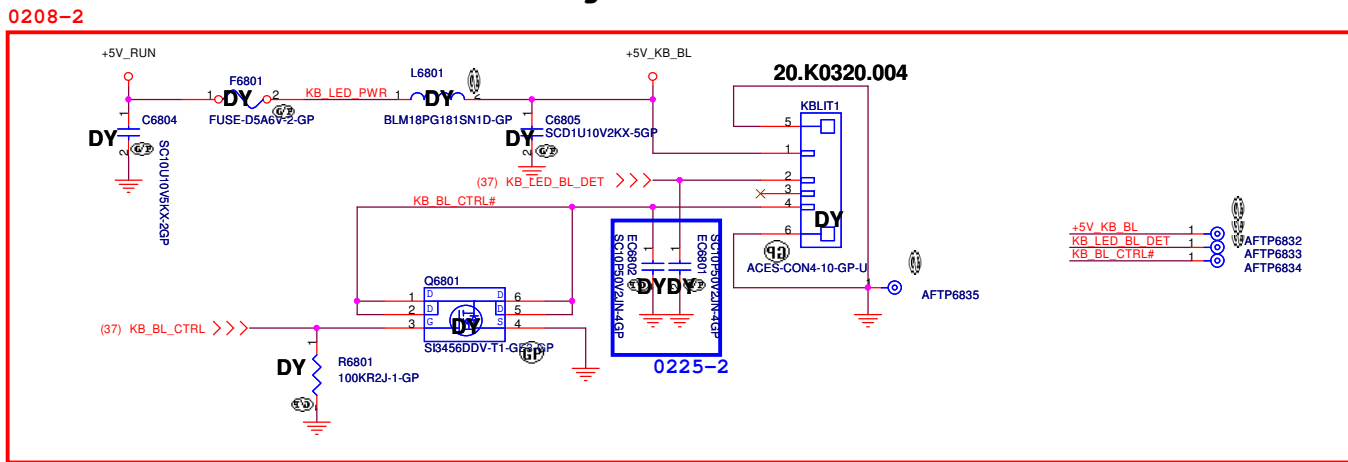
20.K0524.030
20.K0461.030

SSID = Touch.Pad

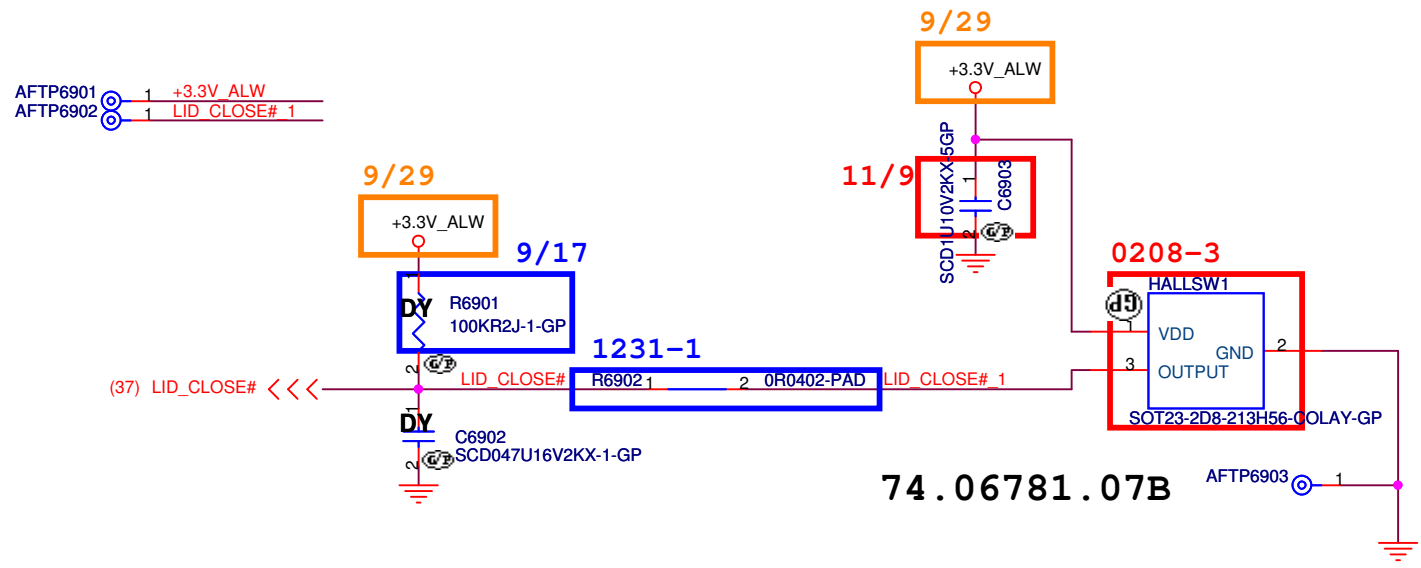
TouchPad Connector



KB Backlight Connector




SSID = Hall.Sensor

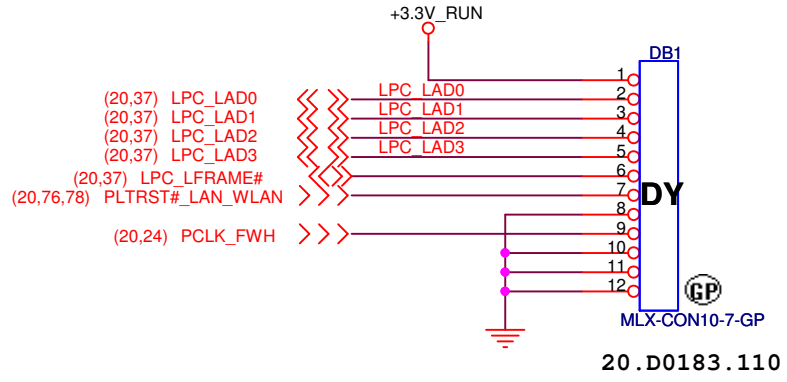


74.06781.07B


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <p style="text-align: center;">Hall Effect Sensor</p>	
Size A4	Document Number <p style="text-align: center;">Berry AMD Discrete/UMA</p>	Rev <p style="text-align: right;">A00</p>	
Date: Thursday, March 04, 2010		Sheet 69 of 95	

SSID = Debug




<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <p style="text-align: center;"><i>Dubug connector</i></p>	
Size A4	Document Number <p style="text-align: center;"><i>Berry AMD Discrete/UMA</i></p>	Rev A00	
Date: Thursday, March 04, 2010		Sheet 70 of 95	


(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title RESERVED		
Size A4	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 71 of 95

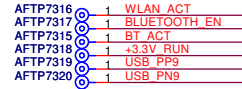
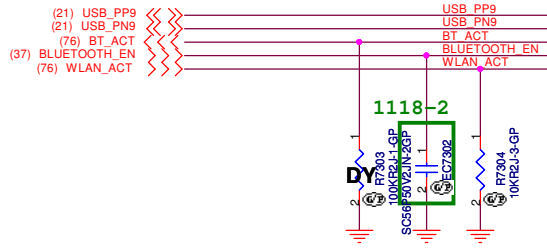
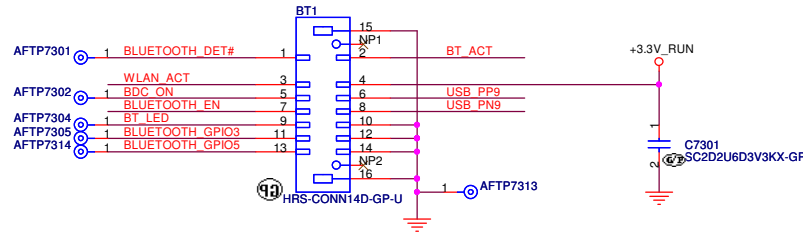
(Blanking)

<Core Design>


		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
RESERVED		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 72 of 95

SSID = User.Interface

Bluetooth Module conn.




<Core Design>

 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Rev
		A00
Title		
Bluetooth		
Size	Document Number	Rev
A3	Berry	A00
Date:	Thursday, March 04, 2010	Sheet 73 of 95

(Blanking)

<Core Design>

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Berry AMD Discrete/UMA	Rev A00
Date: Thursday, March 04, 2010		Sheet 74 of 95

(Blanking)

<Core Design>



Title		
<i>Reserved</i>		
Size A4	Document Number <i>Berry AMD Discrete/UMA</i>	Rev <i>A00</i>
Date: Thursday, March 04, 2010	Sheet 75 of	95

SSID = Int.Conn

10/9

ESATA USB

(21) USB_PP0 <<<>>
(21) USB_PN0 <<<>>

WWAN USB

(21) USB_PP5 <<<>>
(21) USB_PN5 <<<>>

USB PORT

(21) USB_PN1 <<<>>
(21) USB_PP1 <<<>>

WLAN USB

(21) USB_PP4 <<<>>
(21) USB_PN4 <<<>>

WWAN PCIE

(37) E51_RXD <<<>>
(37) E51_TXD <<<>>

WWAN PCIE

(12) PCIE_RXP2 <<<>>
(12) PCIE_RXN2 <<<>>

SMBUS

(18,19) SB_SMBDATA <<<>>
(18,19) SB_SMBCLK <<<>>

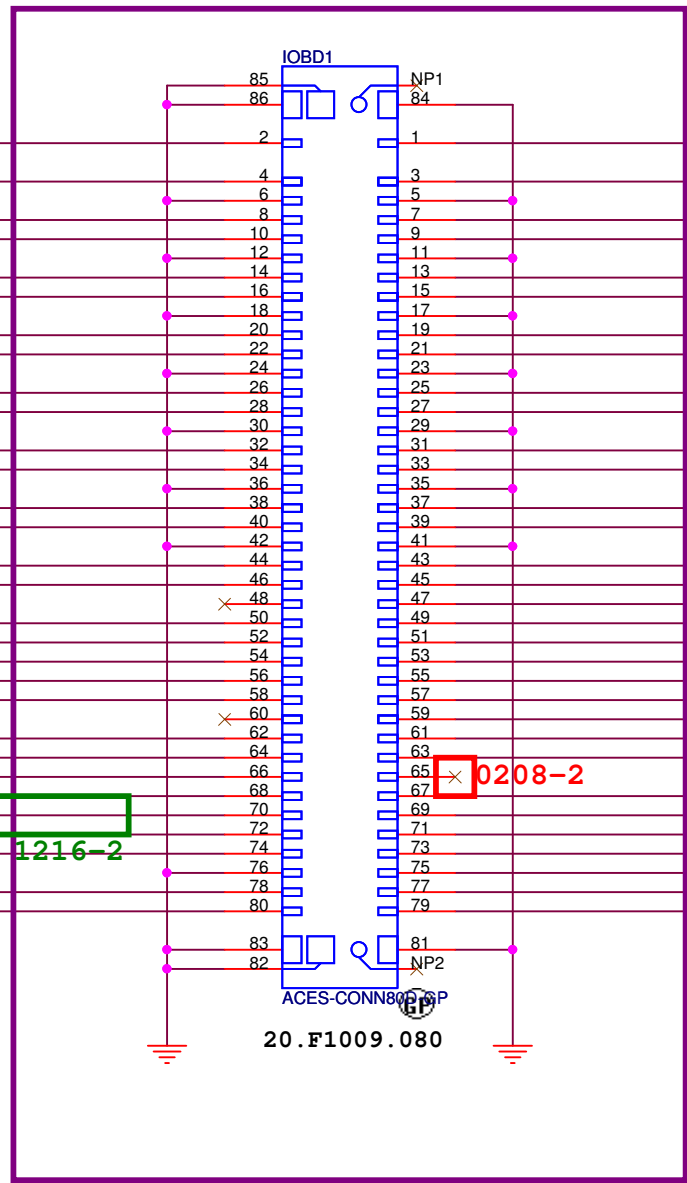
+DC_IN_SS

LAN PCIE

(37) WIFI_RF_EN <<<>>
(7) WWAN_CLK_REQ# <<<>>
(37) WWAN_RADIO_DIS# <<<>>
(37) PSID_DISABLE# <<<>>
(37) 8103_GPO <<<>>

LAN PCIE

(12) PCIE_RXP1 <<<>>
(12) PCIE_RXN1 <<<>>



SATA_TXN2 (22) <<<>>

SATA(ESATA)

SATA_TXP2 (22) <<<>>

SATA(ESATA)

SATA_RXN2 (22) <<<>>
SATA_RXP2 (22) <<<>>

WLAN PCIE

PCIE_TXP0 (12) <<<>>
PCIE_TXN0 (12) <<<>>

WLAN PCIE

PCIE_RXP0 (12) <<<>>
PCIE_RXN0 (12) <<<>>

WLAN CLK

CLK_PCIE_WLAN (7) <<<>>
CLK_PCIE_WLAN# (7) <<<>>

LAN CLK

CLK_PCIE_LAN (7) <<<>>
CLK_PCIE_LAN# (7) <<<>>

WWAN CLK

CLK_PCIE_WWAN (7) <<<>>
CLK_PCIE_WWAN# (7) <<<>>

at least 80 mil

+5V_USB1
+5V_ALW

+3.3V_RUN

+3.3V_ALW
+1.5V_RUN

0208-2

1216-2

PM_LAN_ENABLE (37) <<<>>
PLTRST#_LAN_WLAN (20,70,78) <<<>>
WLAN_CLK_REQ# (7) <<<>>
PCIE_WAKE# (21) <<<>>
BT_ACT (73) <<<>>
WLAN_ACT (73) <<<>>
PSID_EC (37) <<<>>

20.F1009.080

0107-6



<Core Design>

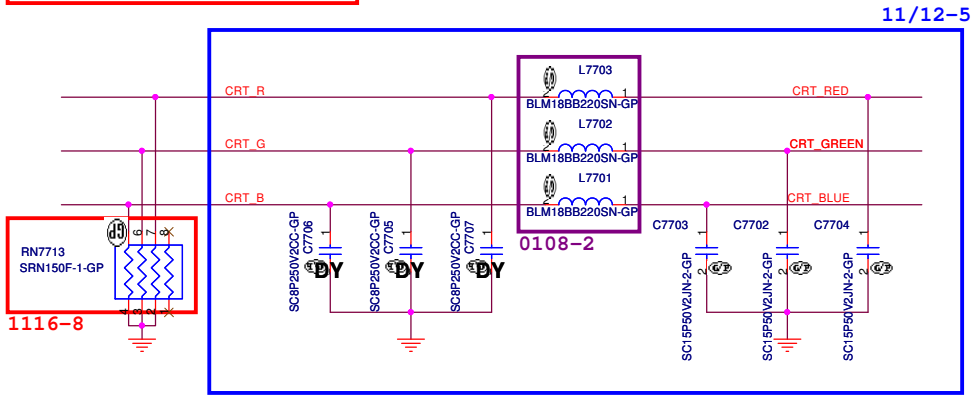
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **IO Board Connector**

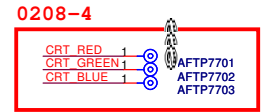
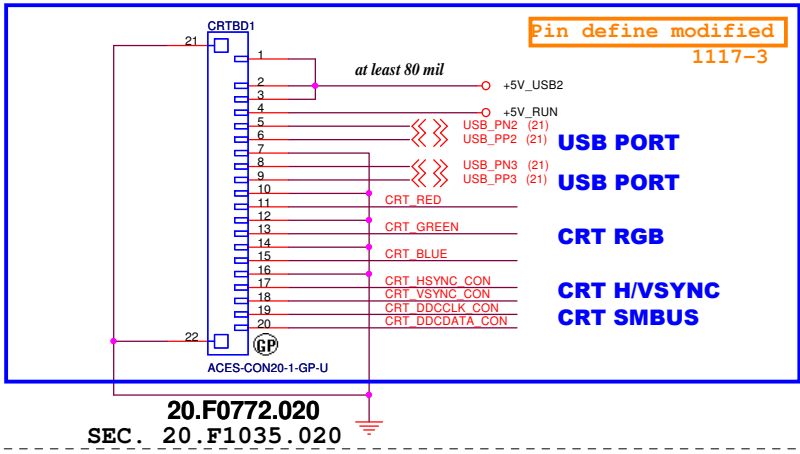
Size A4 Document Number **Berry AMD Discrete/UMA** Rev **A00**

Date: Thursday, March 04, 2010 Sheet 76 of 95

SSID = Int.Conn

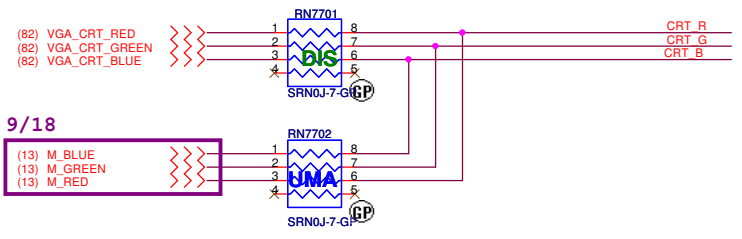


10/1 CRT Board Connector



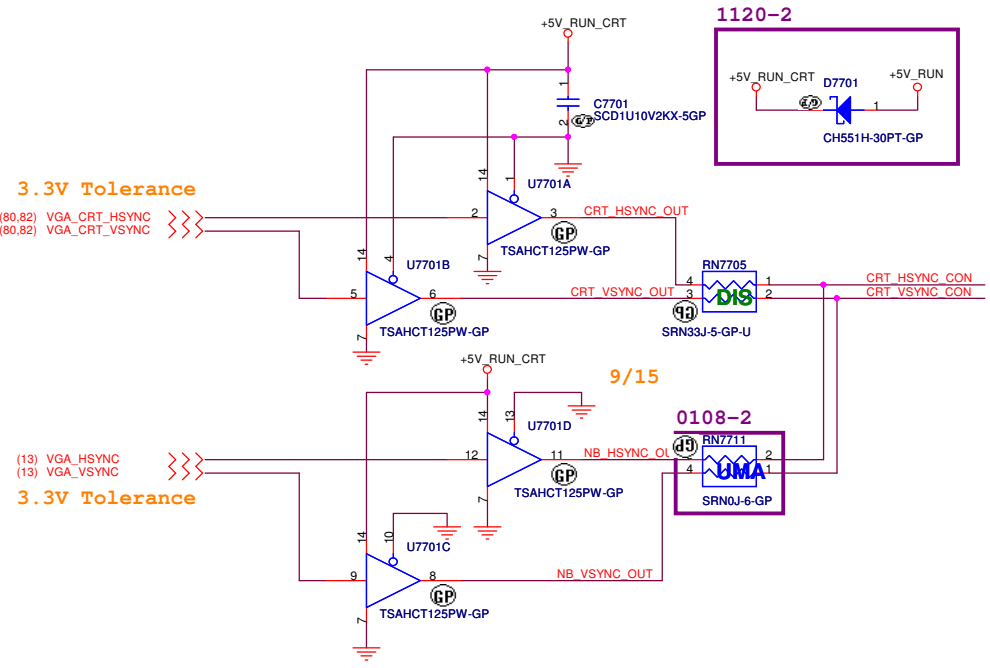
CRT RGB

Close to CRT Board CONN Filter design on CRT Board

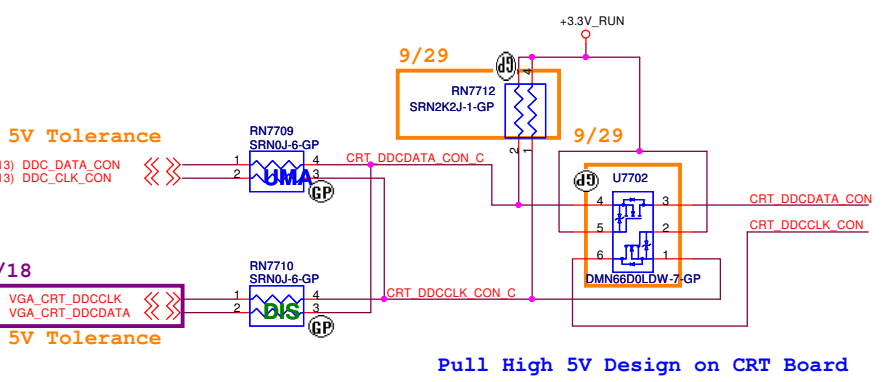


CRT Hsync & Vsync level shift

Close to CRT Board CONN



CRT DDCDATA & DDCCLK



<Core Design>

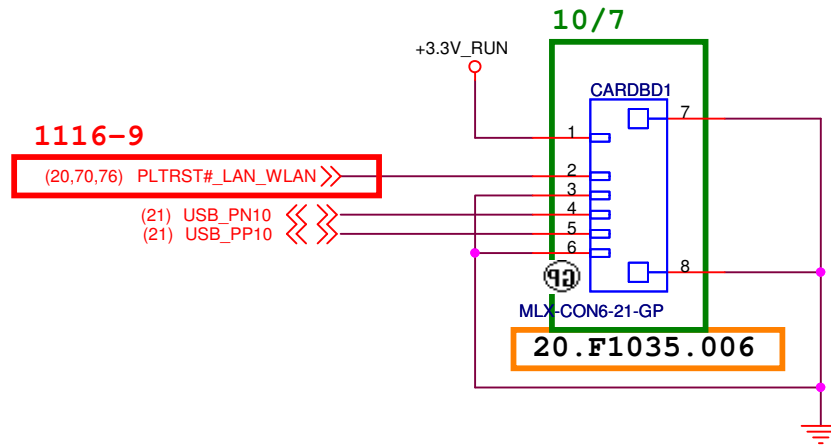
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Title: **CRT Board Connector**

Size: A3	Document Number: Berry AMD Discrete/UMA	Rev: A00
Date: Thursday, March 04, 2010 Sheet 77 of 95		

SSID = SDIO

Card Reader connector



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size
A4

Document Number

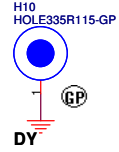
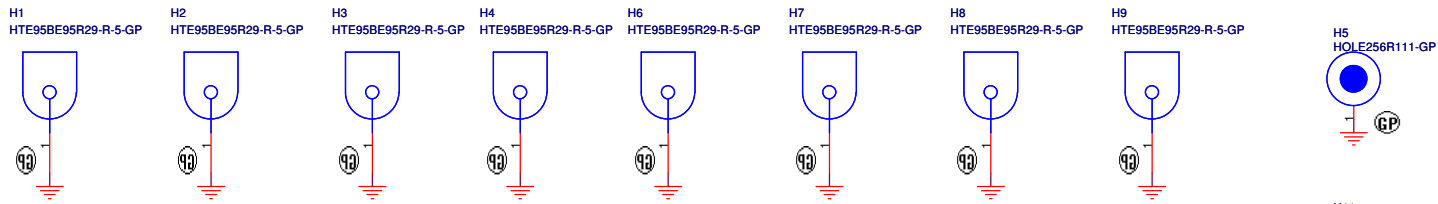
Berry AMD Discrete/UMA

Rev

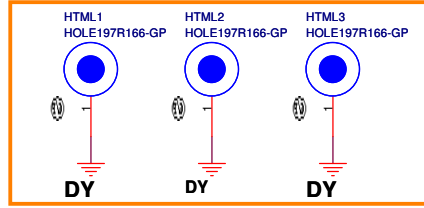
A00

Date: Thursday, March 04, 2010

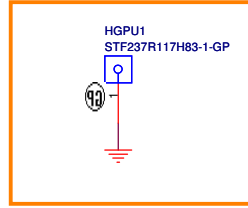
Sheet 78 of 95



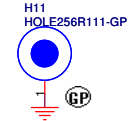
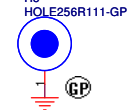
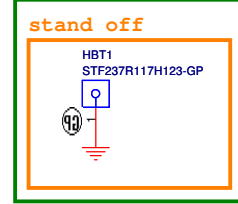
CPU Thermal module hole



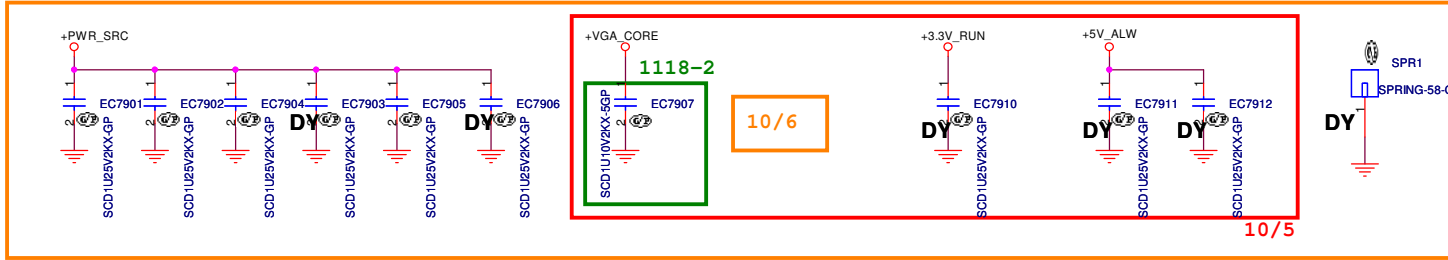
GPU Thermal module hole



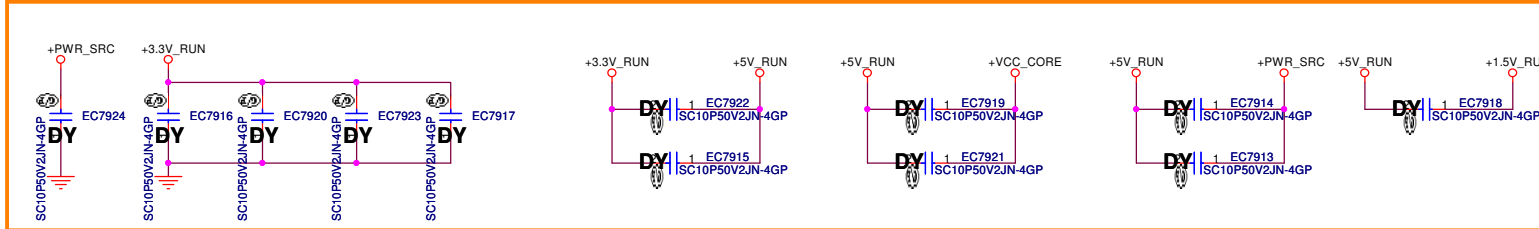
0210-2



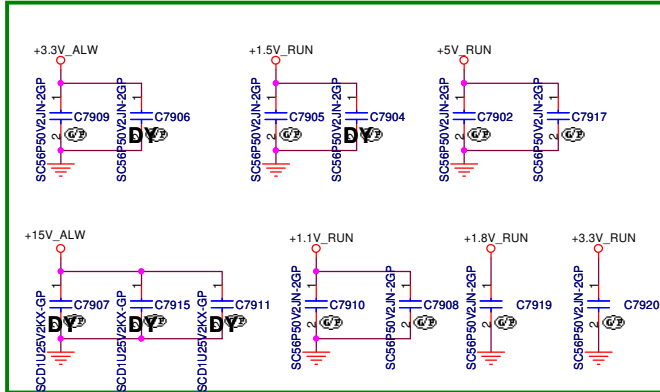
EMI Reserve



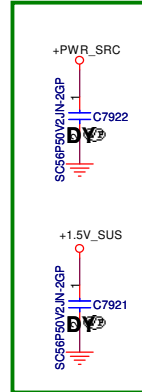
EMI Reserve 1117-4



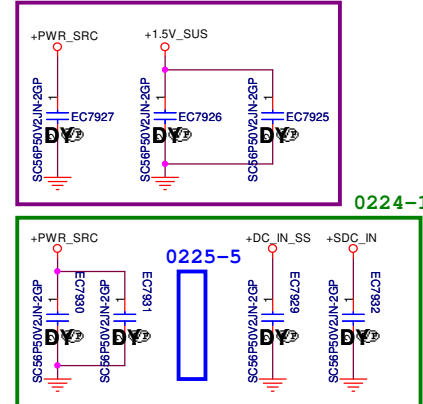
1118-2 RF Team Solution

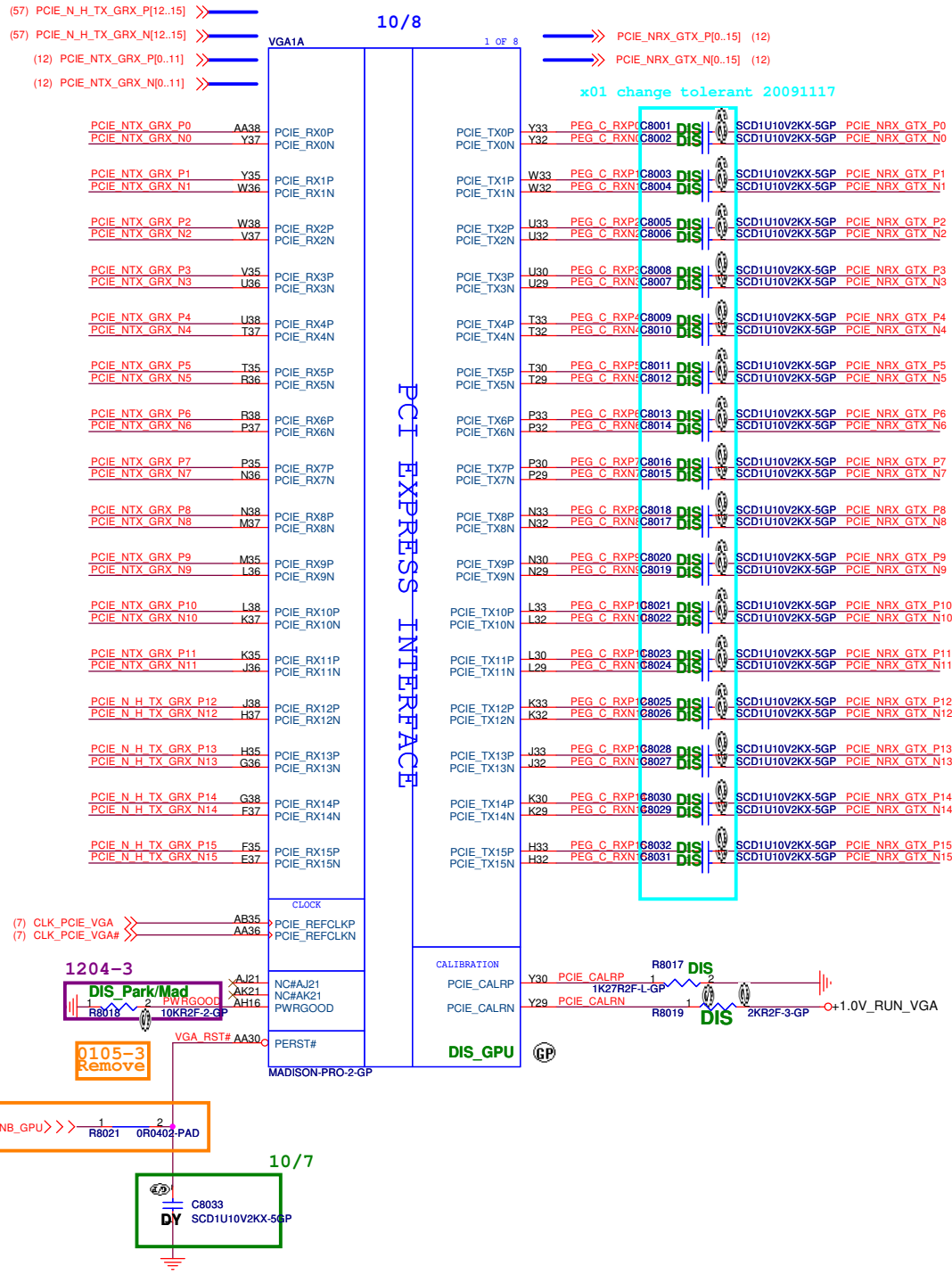


0106-3 RF Team Solution



0108-1 EMC reserved

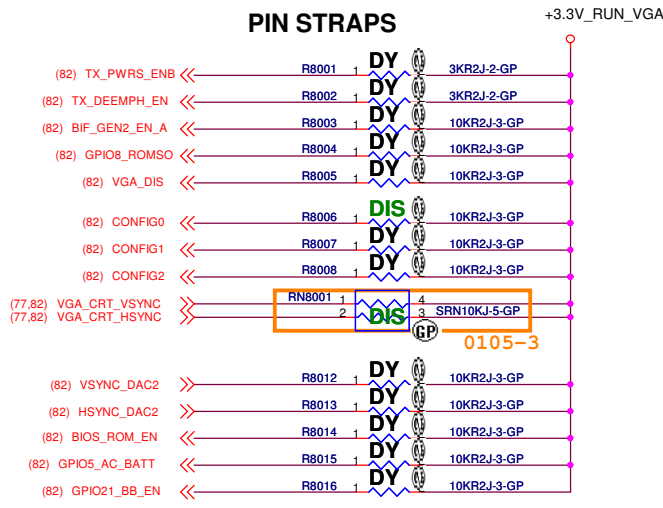




CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]: 11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

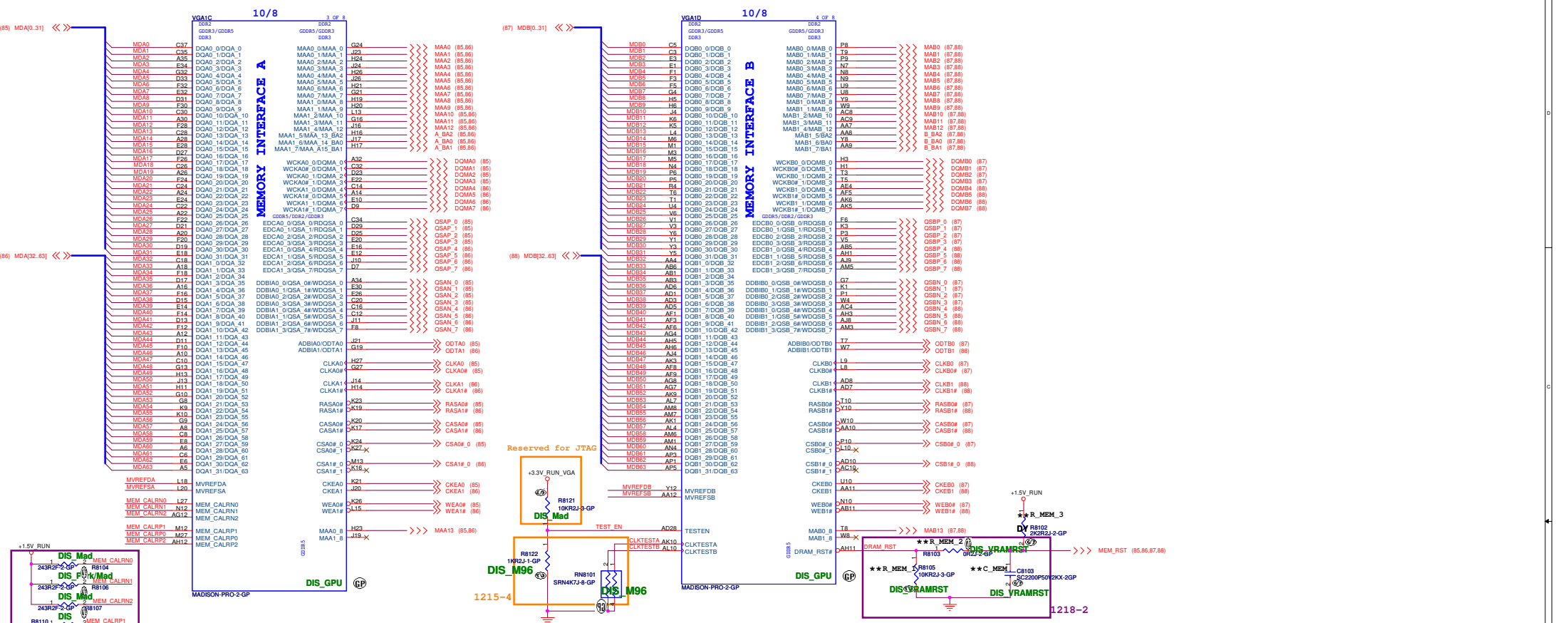


<Core Design>

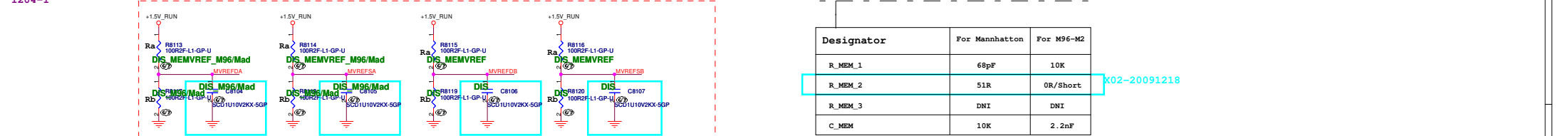
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Title: **GPU PCIe/STRAPPING(1/5)**

Size: A3	Document Number: Berry	Rev: A00
Date: Thursday, March 04, 2010	Sheet: 80	of: 95



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC



DDR3/GDDR3 Memory Stuff Option(Mad/Park) DDR3/GDDR3 Memory Stuff Option(M96/M92)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

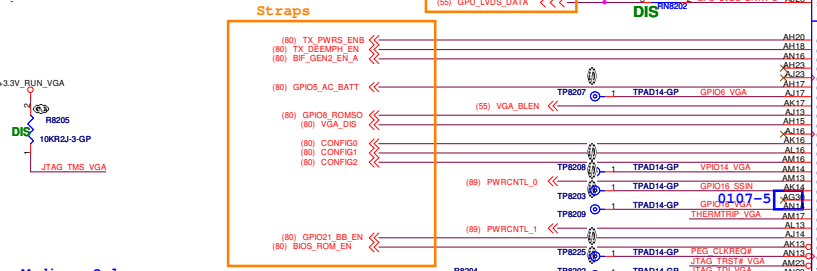
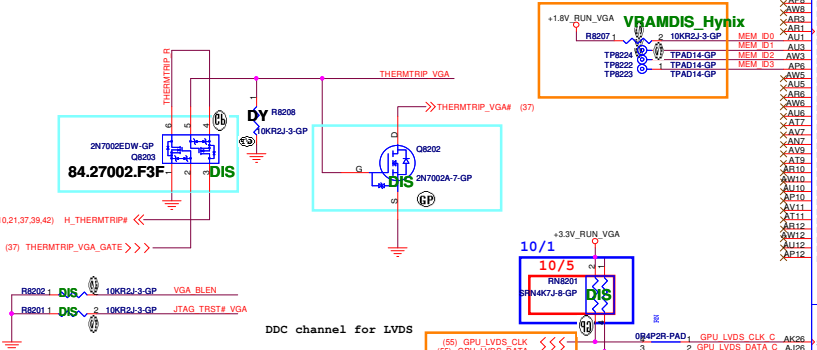
	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

*** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

Designator	For Mannheim	For M96-M2
R_MEM_1	68pF	10K
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	10K	2.2nF

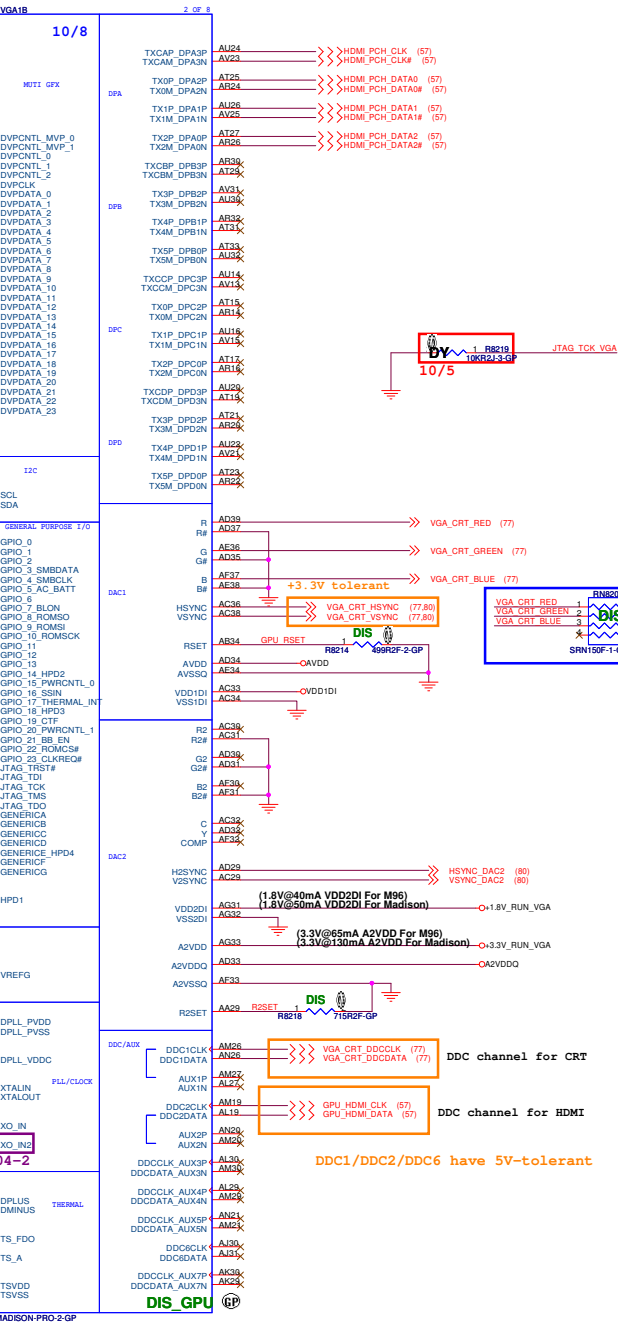
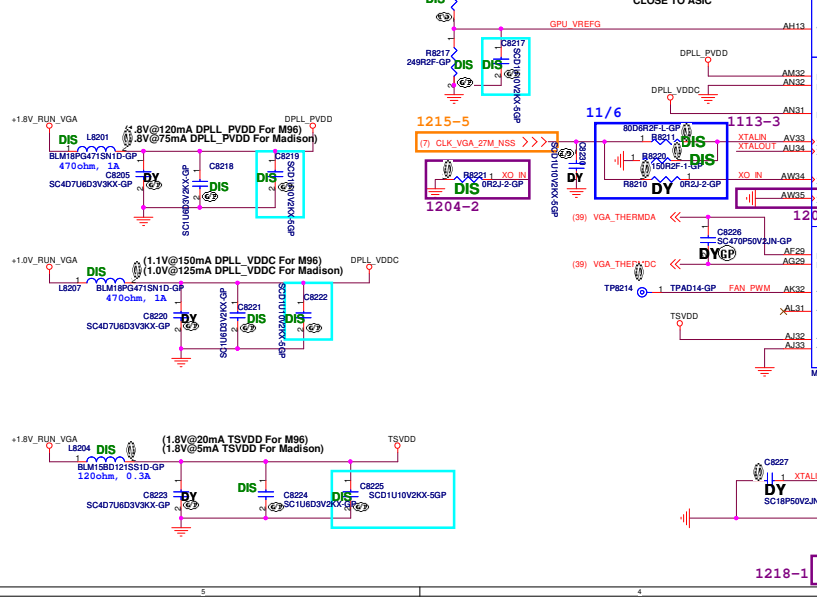
MEMORY ID Table	
DVPPDATA[0:3]	Description
1000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)
0000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)

DVPPDATA[0:3] Default: Pull down

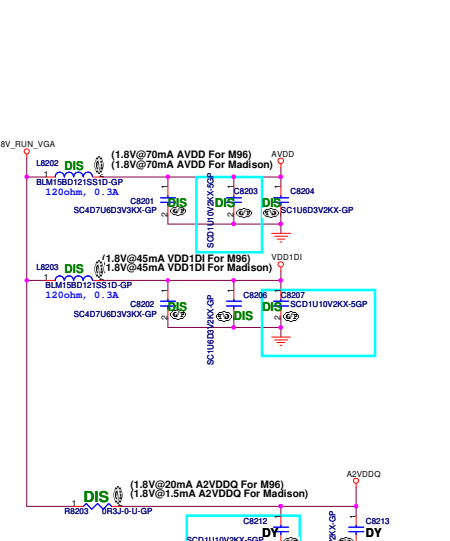
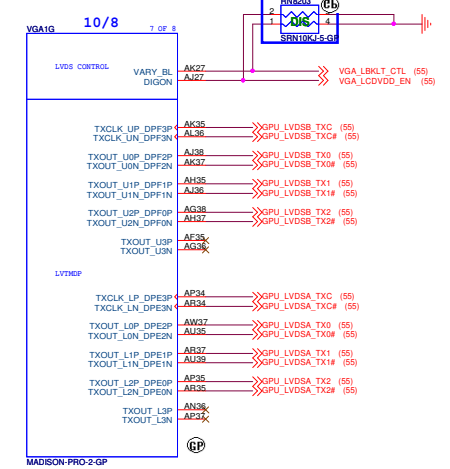


Madison Only JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode
TESTEN#	"1" (FU)	"1" (PU)
JTAG_TRST#	"0" (PD)	"1" (PU)
JTAG_TCK	CLK	"1" (PU)
JTAG_TMS	"1" (FU)	"1" (PU)



LVDS Interface



Clock Input Configuration - GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

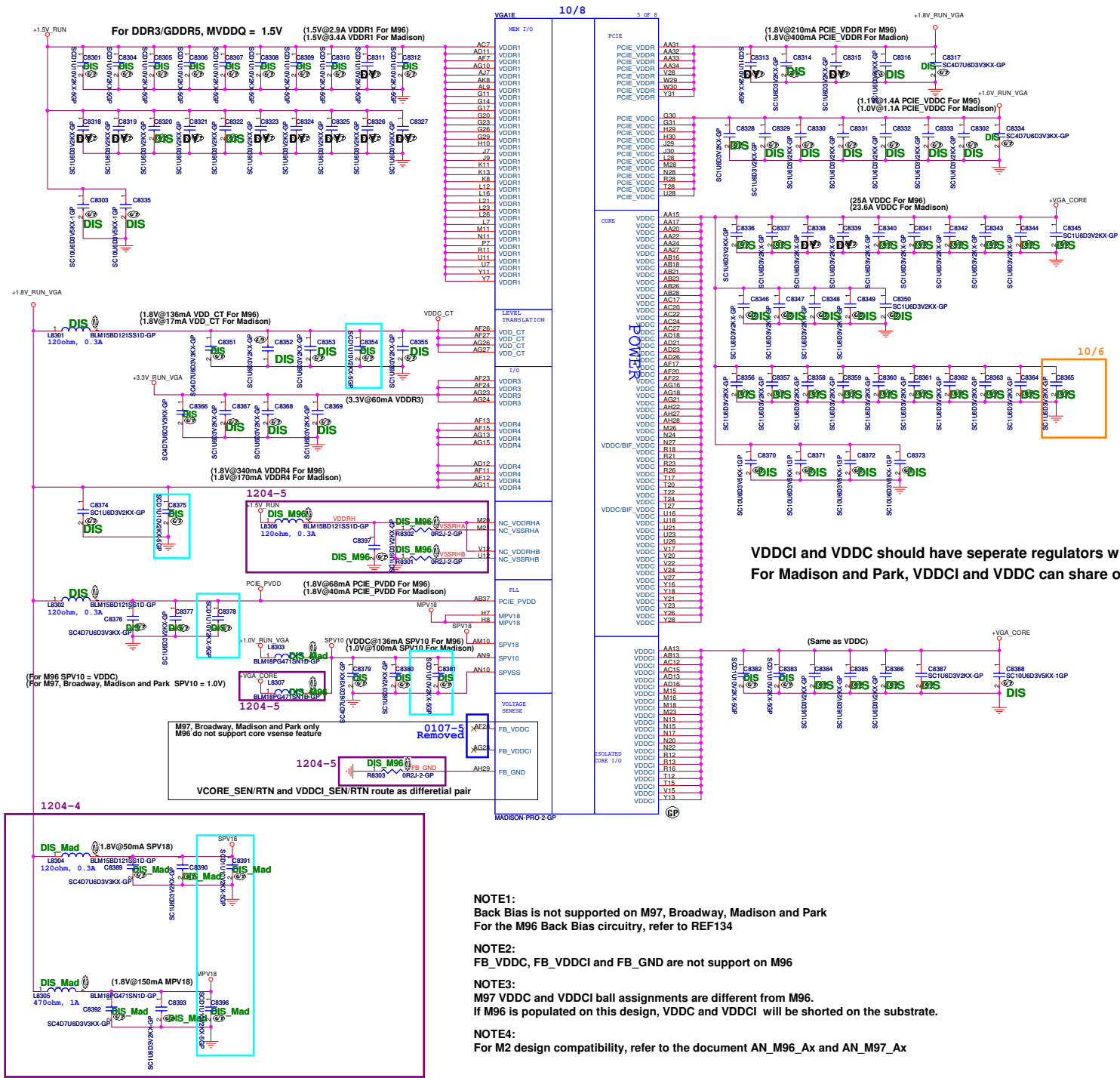
•Core Design•

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Taichung, Taiwan, R.O.C.

File: **GPU_DP/LVDS/CRT/GPIO(3/5)**

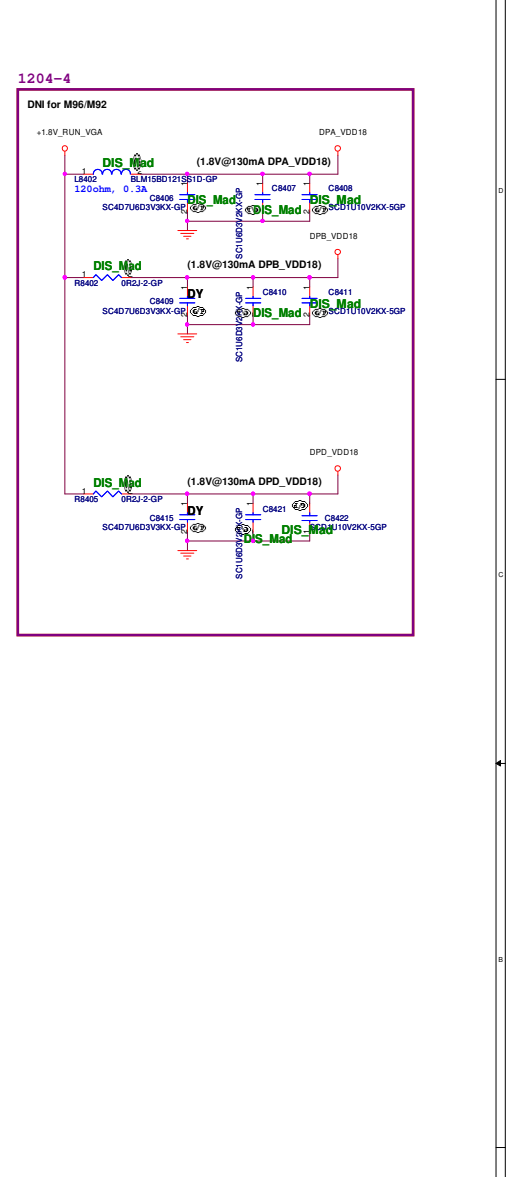
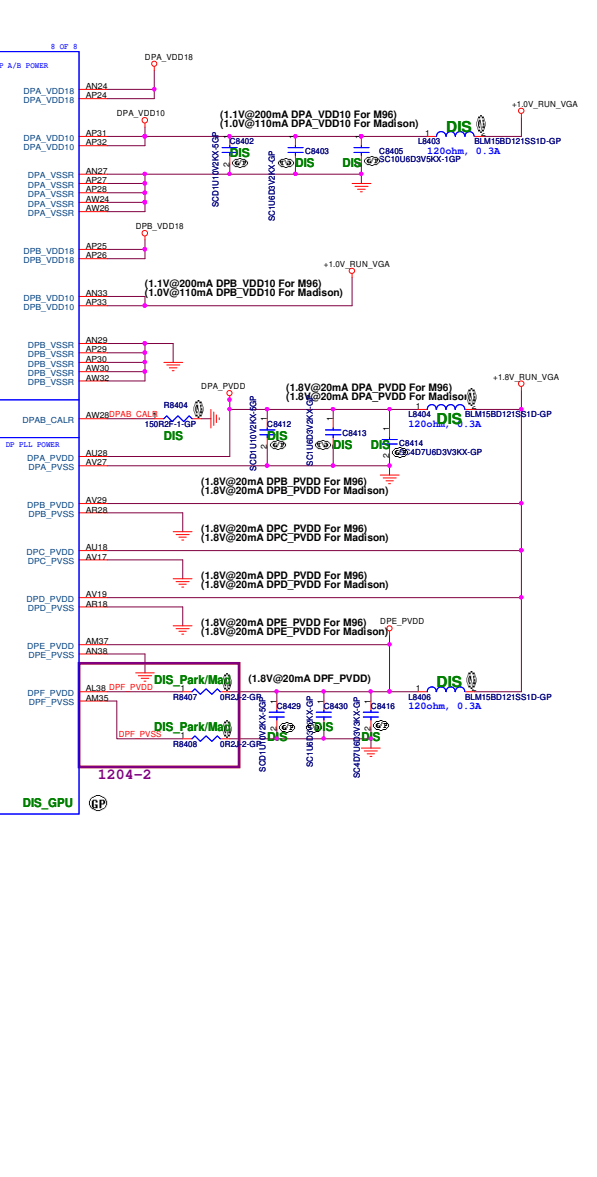
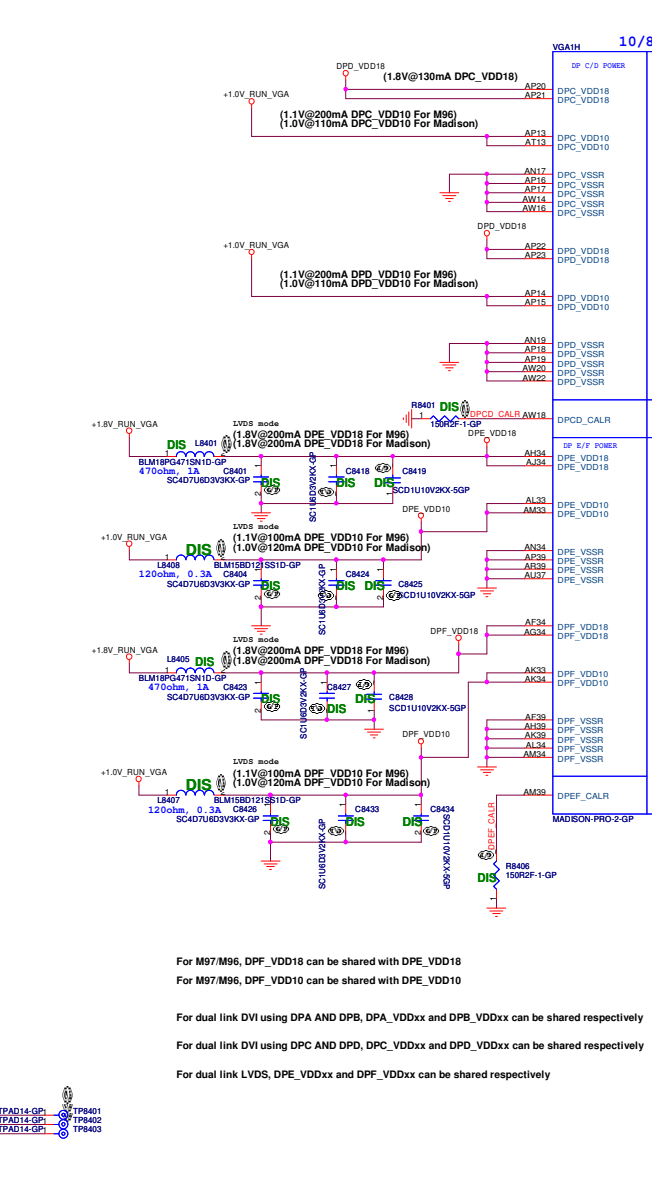
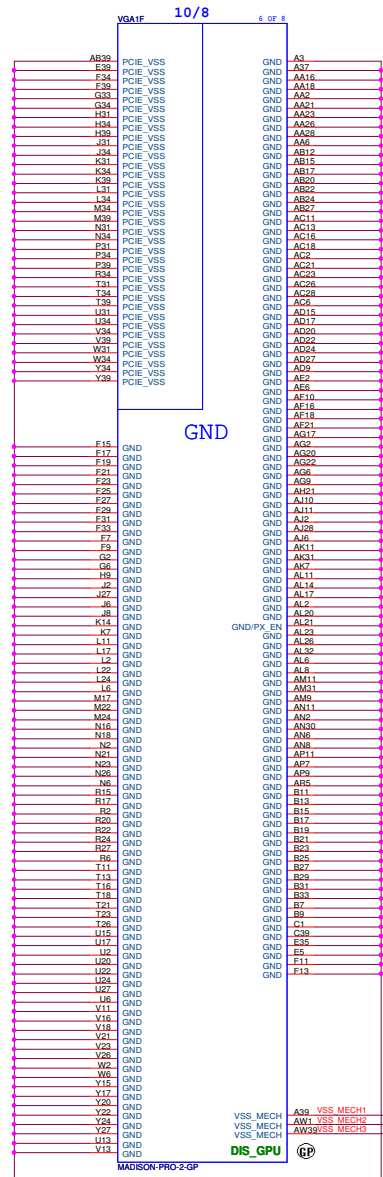
Size: A2 Document Number: **Berry** Rev: **A00**

Date: Thursday, March 04, 2010 Sheet: **R2** of **95**



VDDCI and VDDC should have separate regulators with a merge option for M97, Broadway, Madison and Park, VDDC and VDDCI can share one common regulator

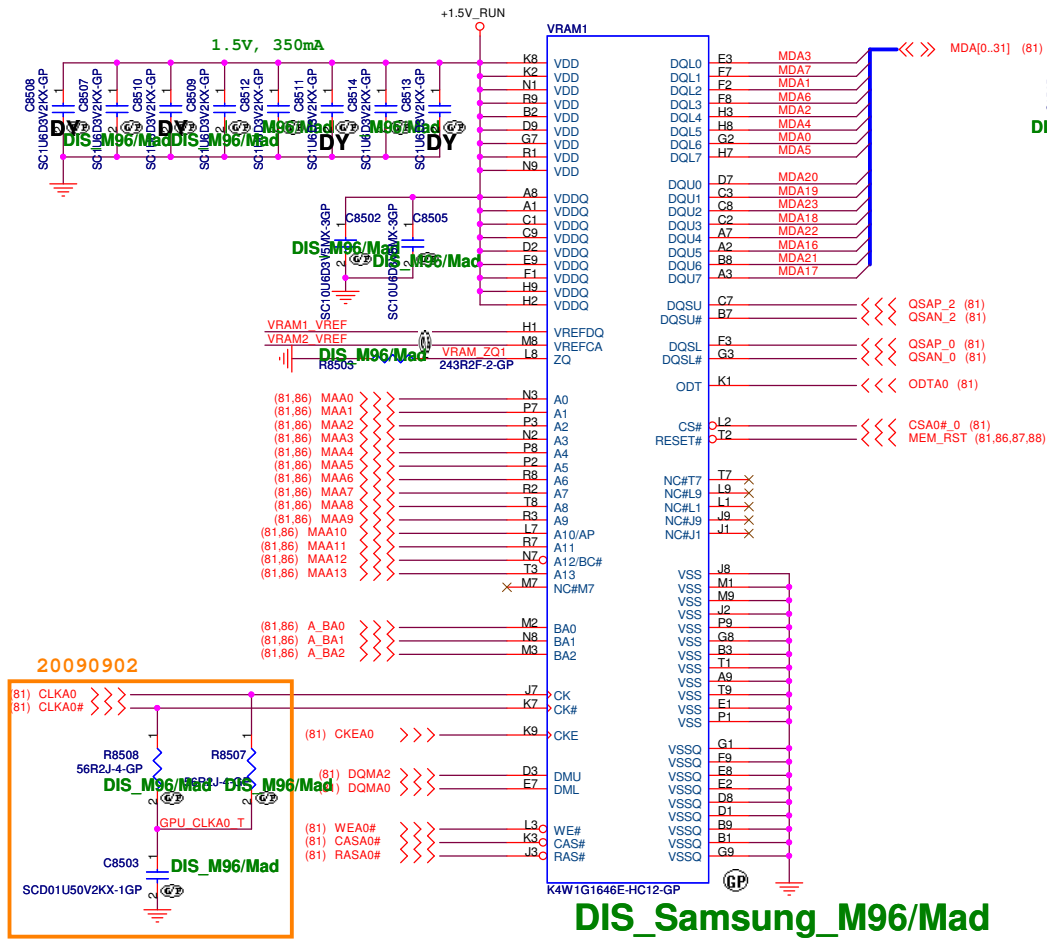
- NOTE1:**
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
- NOTE2:**
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
- NOTE3:**
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
- NOTE4:**
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax



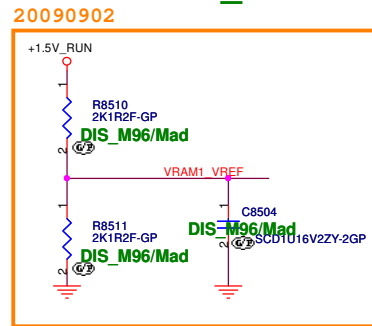
For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
 For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
 For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

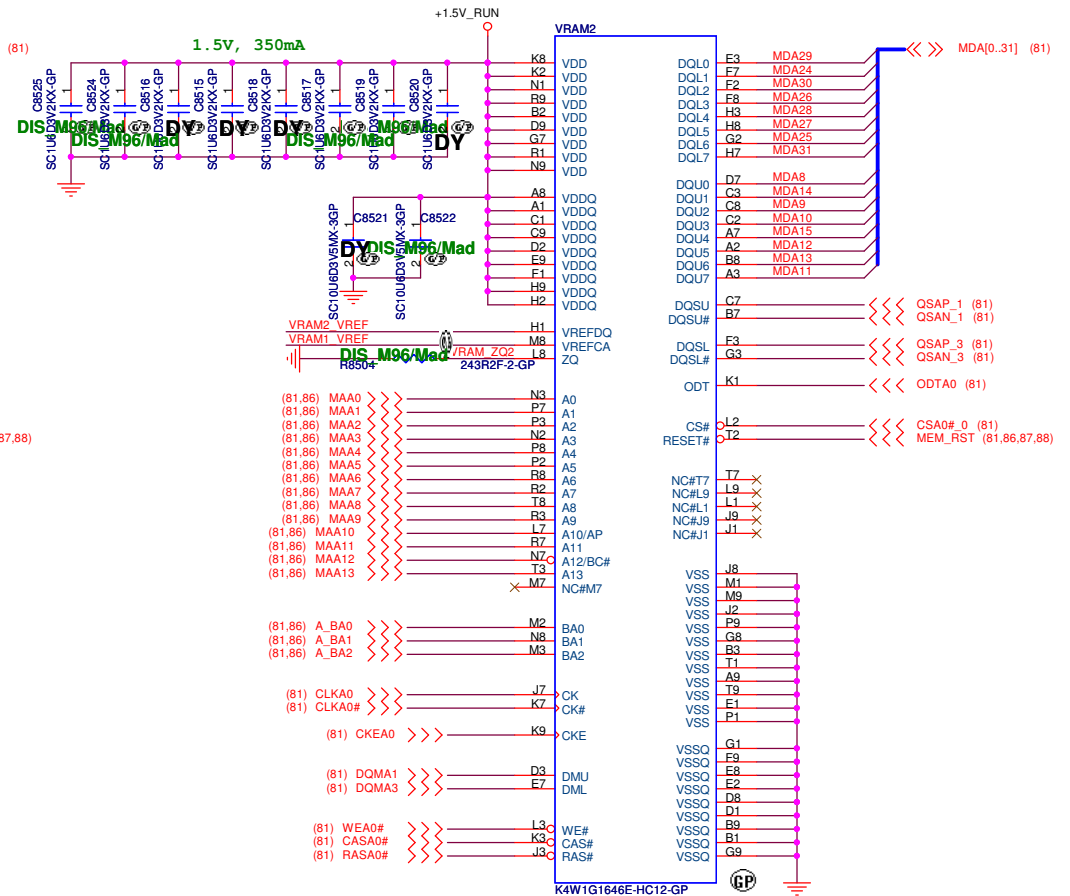
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively



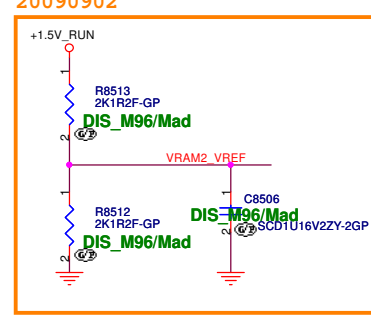
DIS_Samsung_M96/Mad



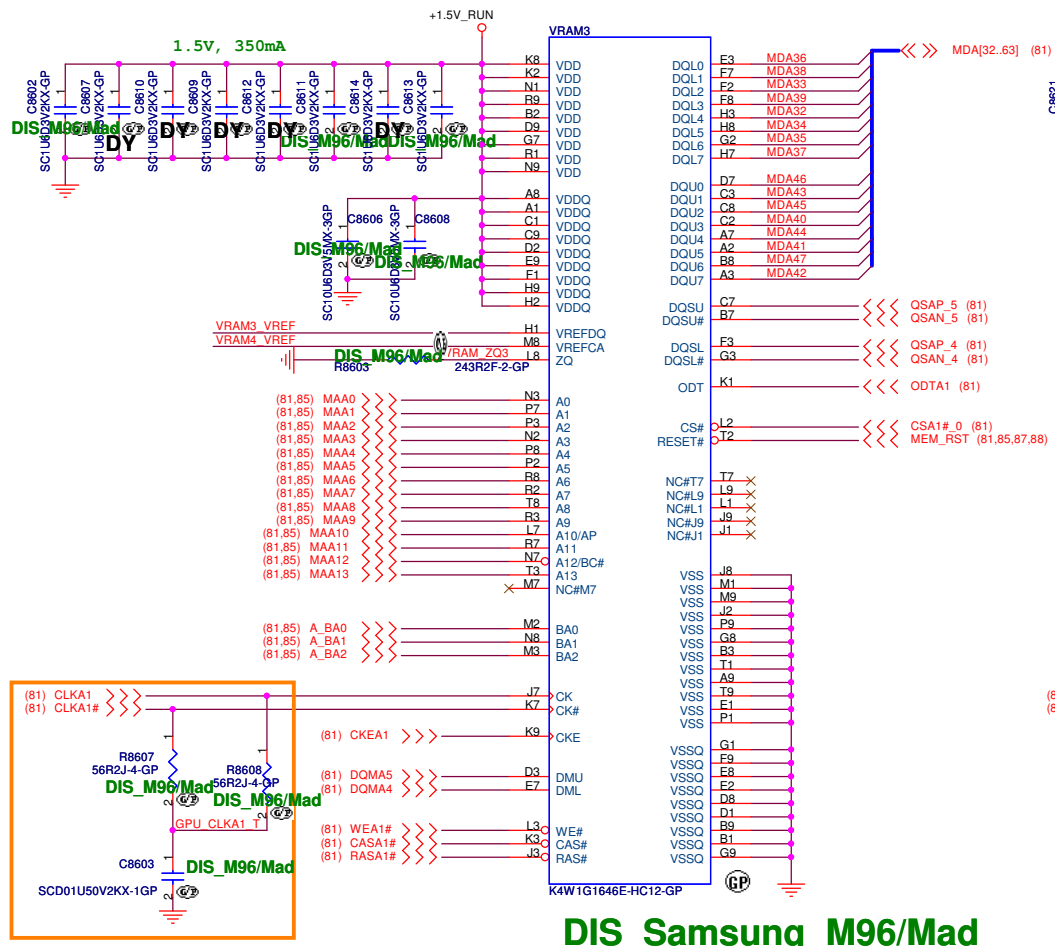
20090902



DIS_Samsung_M96/Mad

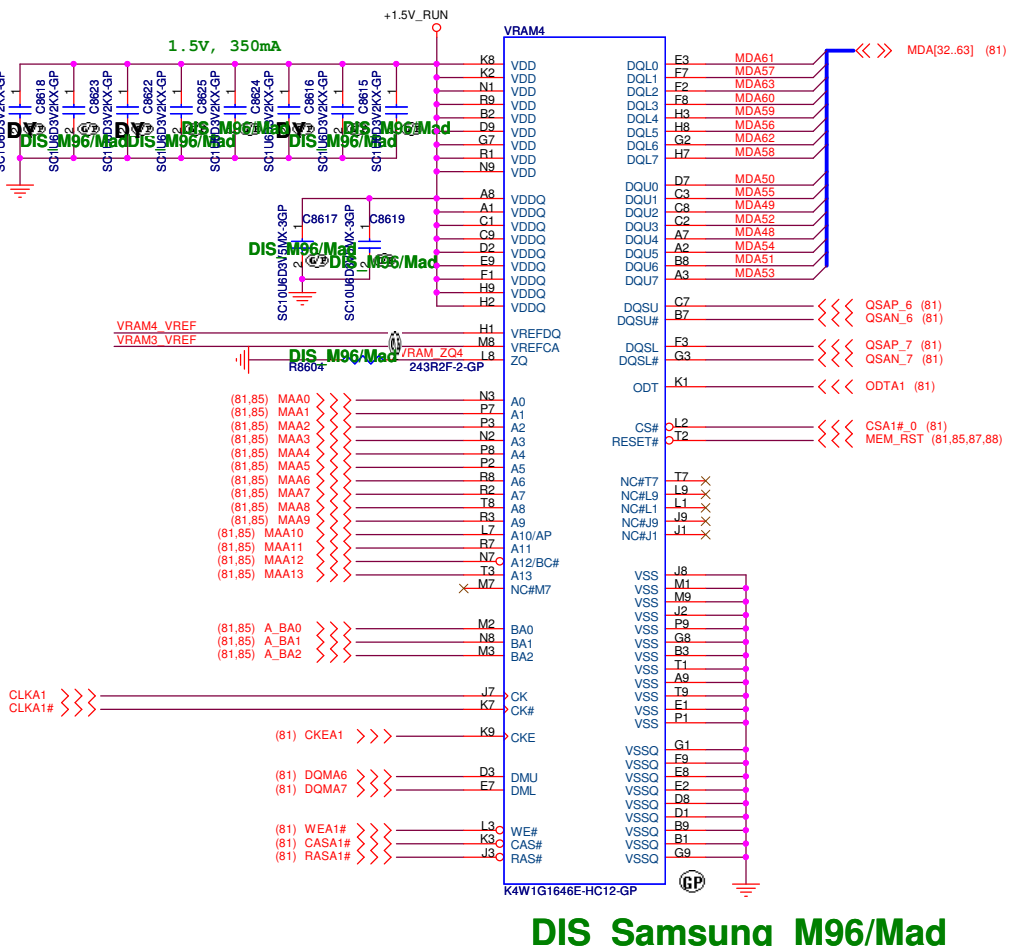
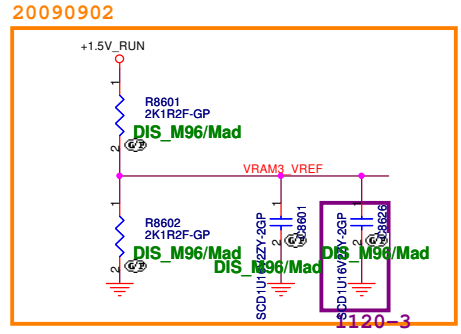


20090902



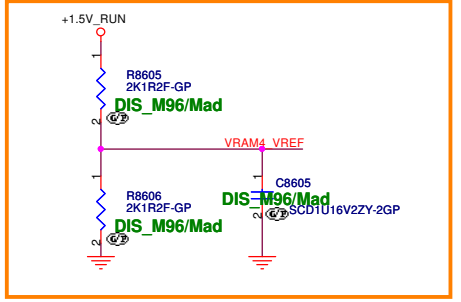
DIS_Samsung_M96/Mad

20090902



DIS_Samsung_M96/Mad

20090902

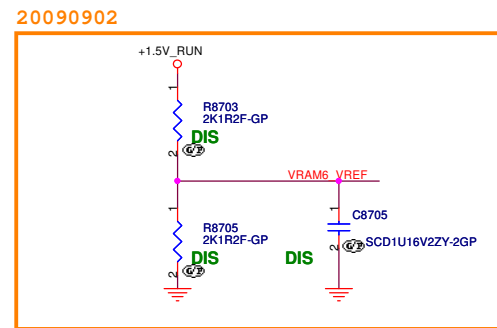
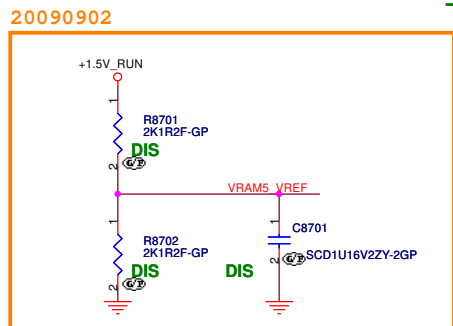
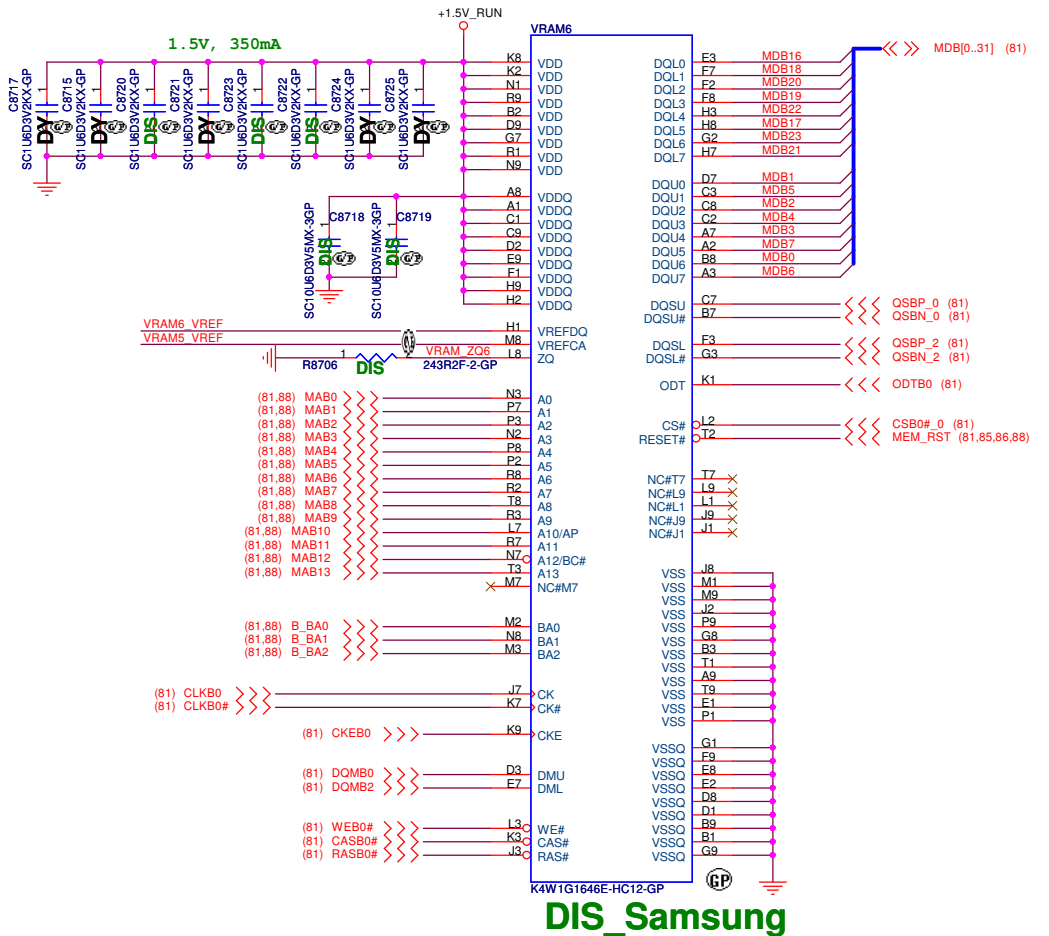
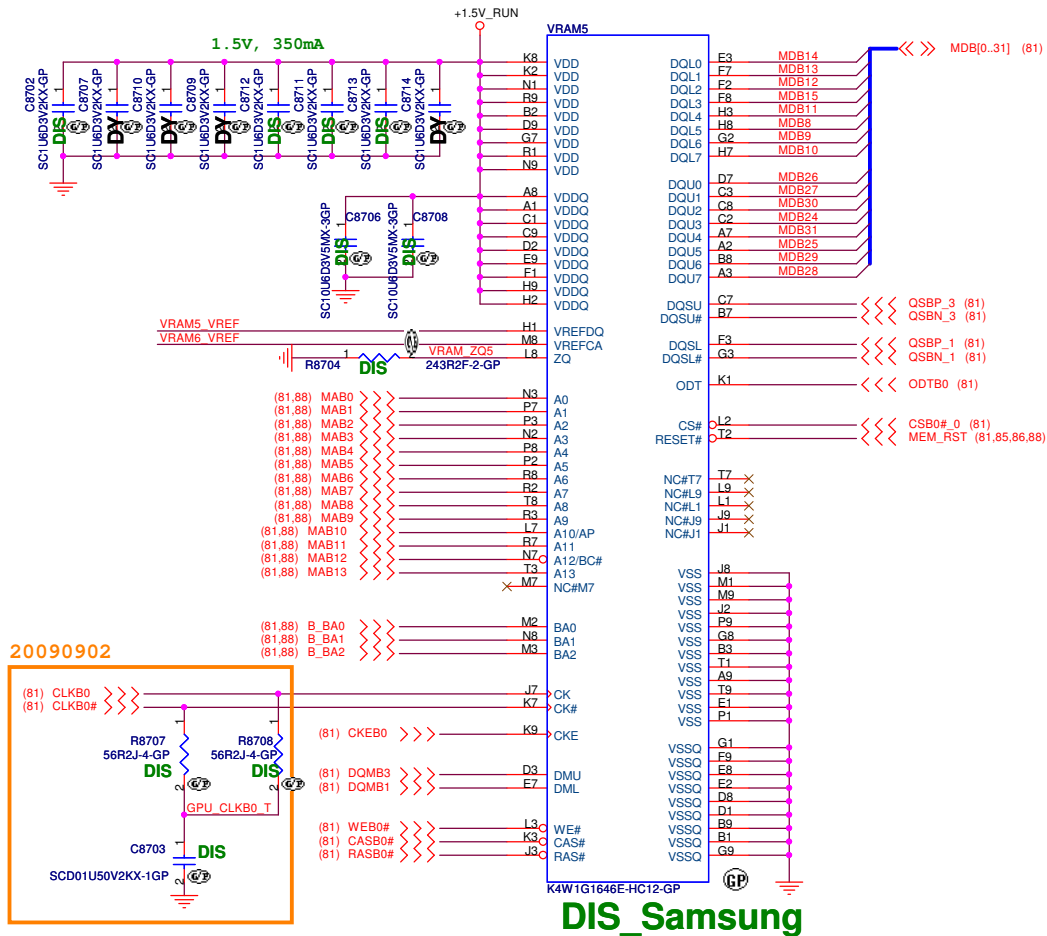


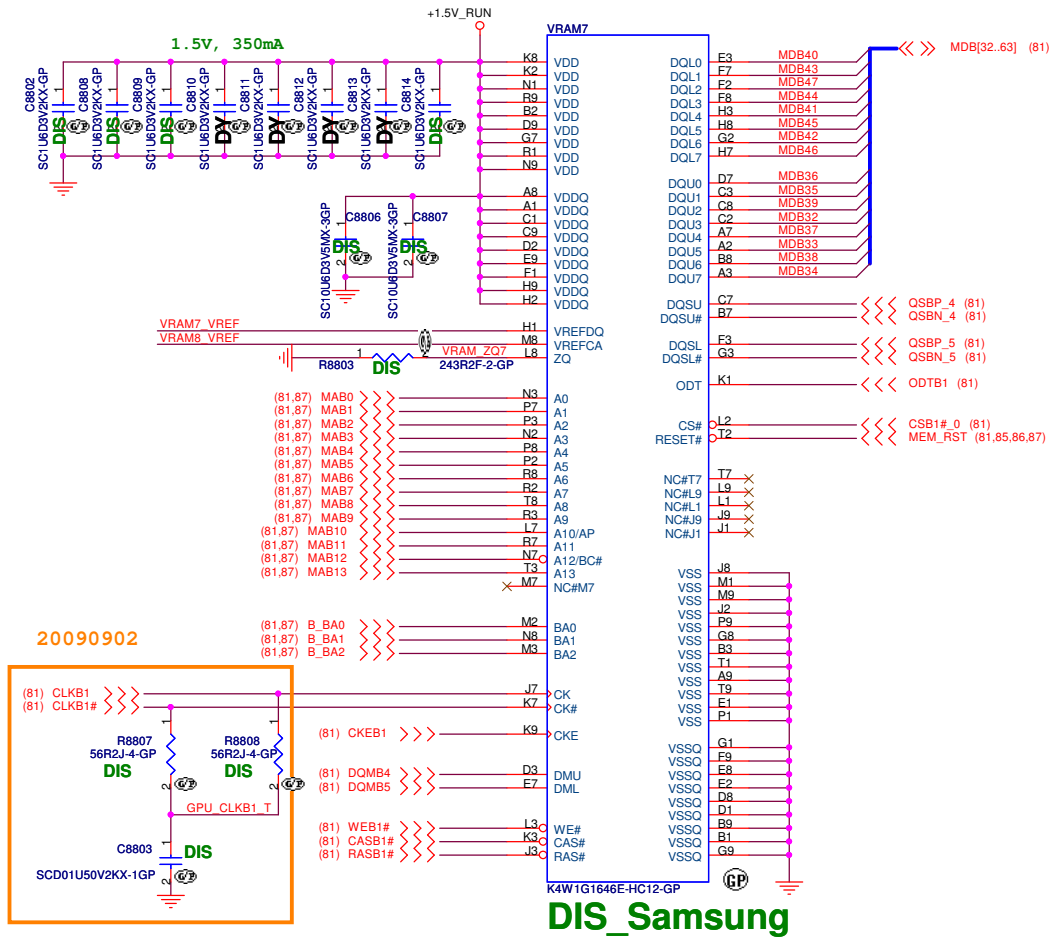
<Core Design>

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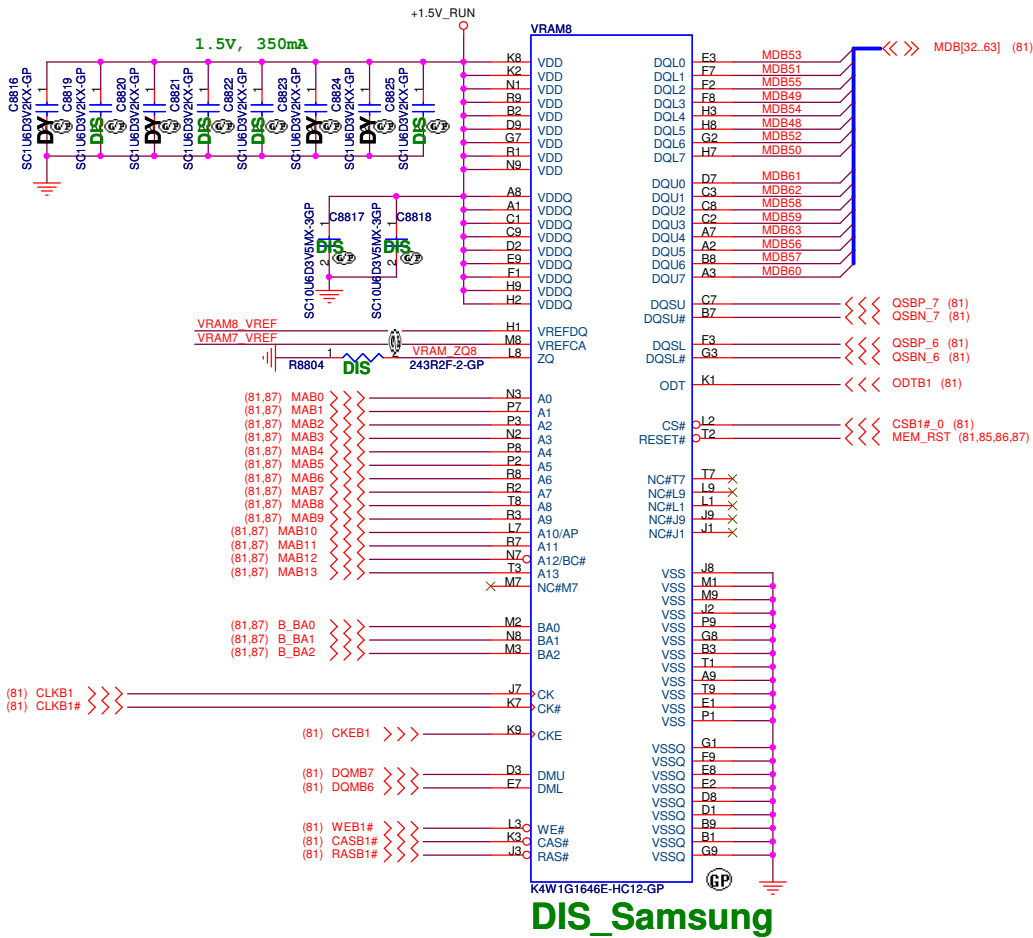
Title: **GPU-VRAM3,4 (2/4)**

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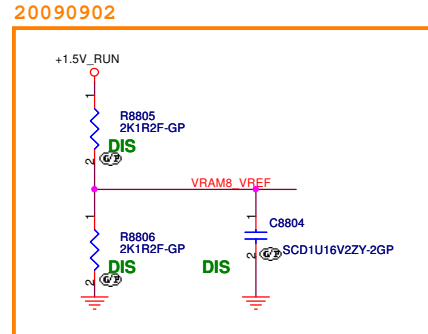
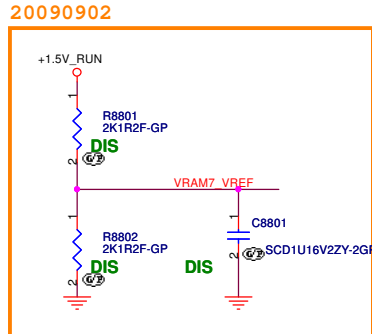




DIS_Samsung

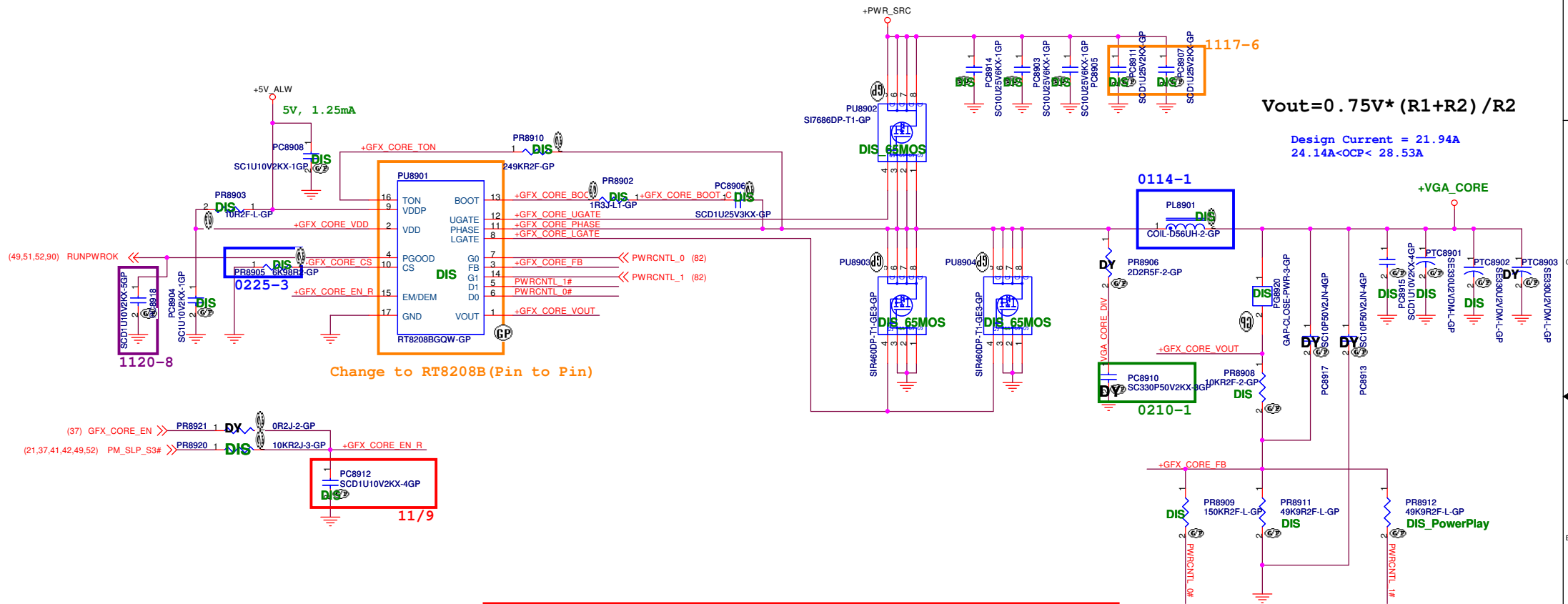


DIS_Samsung



SSID = Video.PWR.Regulator

RT8208AGQW for +VCC_GFX_CORE



$$V_{out} = 0.75V * (R1 + R2) / R2$$

Design Current = 21.94A
24.14A < OCP < 28.53A

Change to RT8208B (Pin to Pin)

M96 Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

PR8912=49.9K
64.49925.6DL

Park Power Table

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

PR8912=49.9K
64.44225.6DL

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEF5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

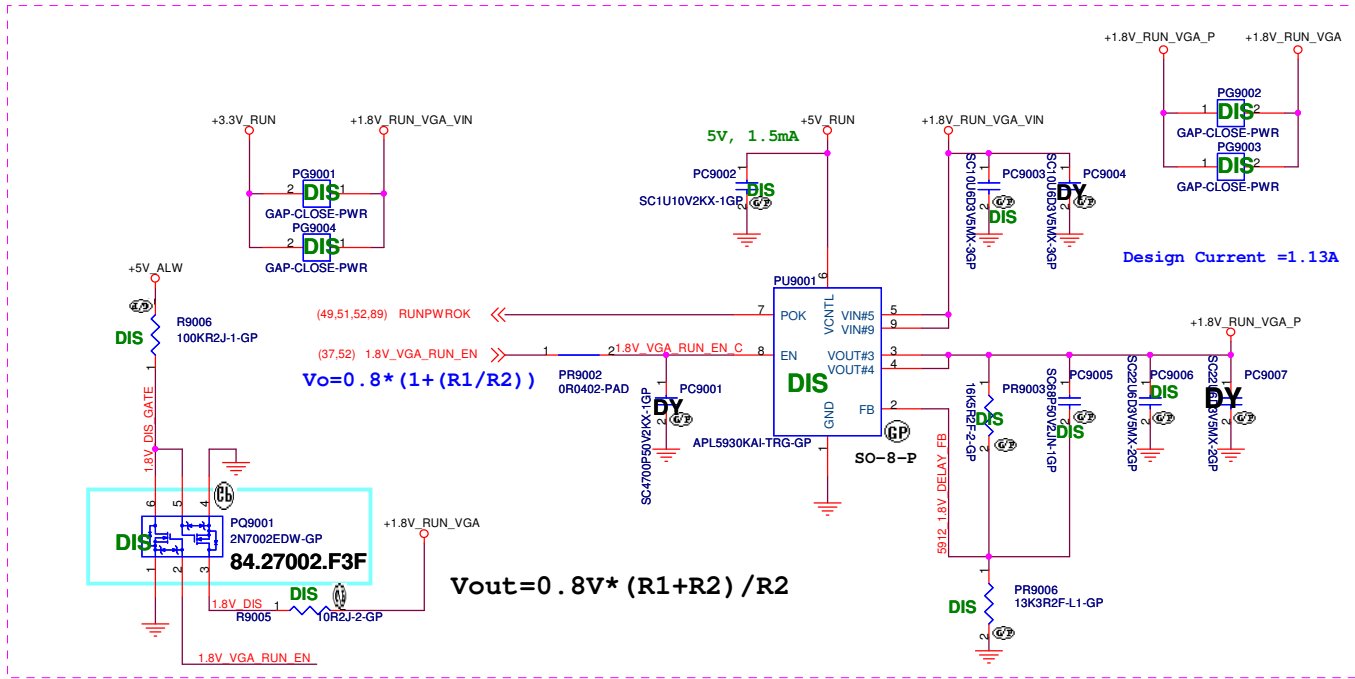
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Title: **RT8208B +VCC GFXCORE**

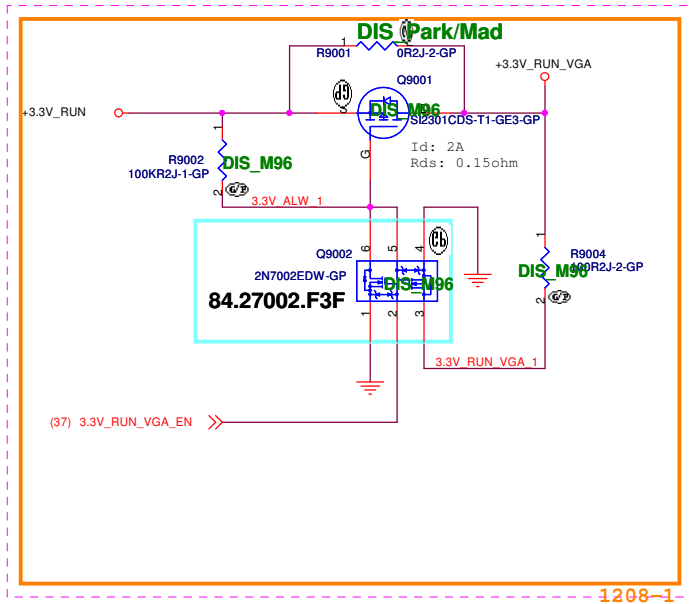
Size A3	Document Number	Rev
	Berry AMD Discrete/UMA	A00

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APL5930 for +1.8V_RUN_VGA

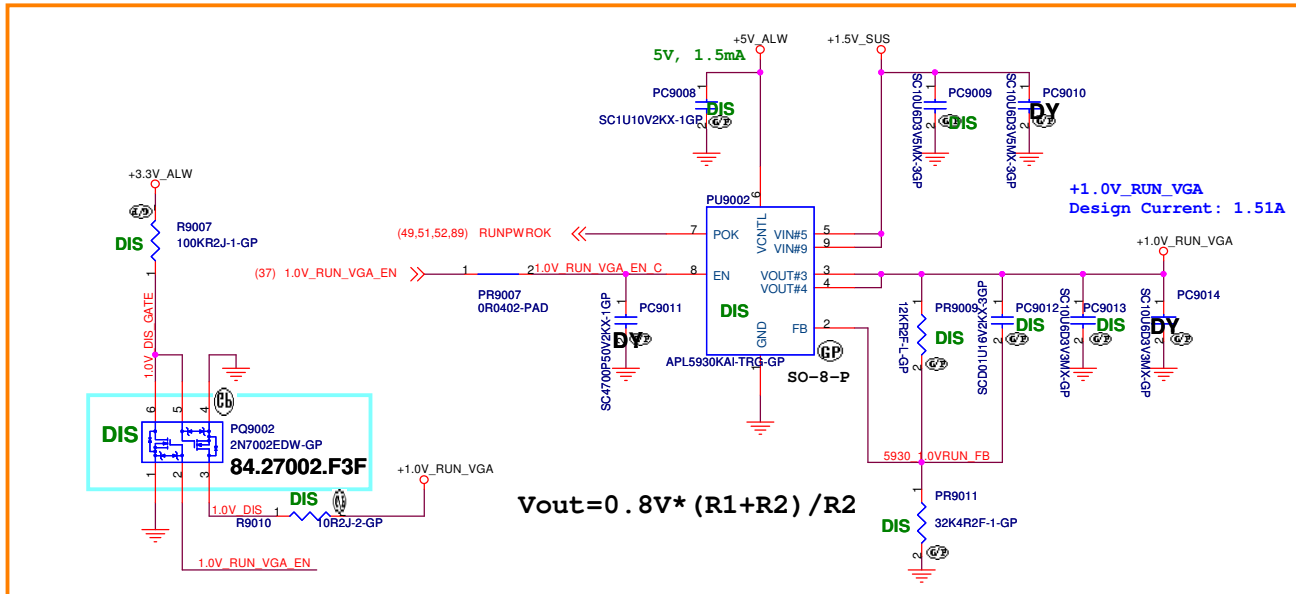


+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA

Will be Change to +1.0V_RUN_VGA

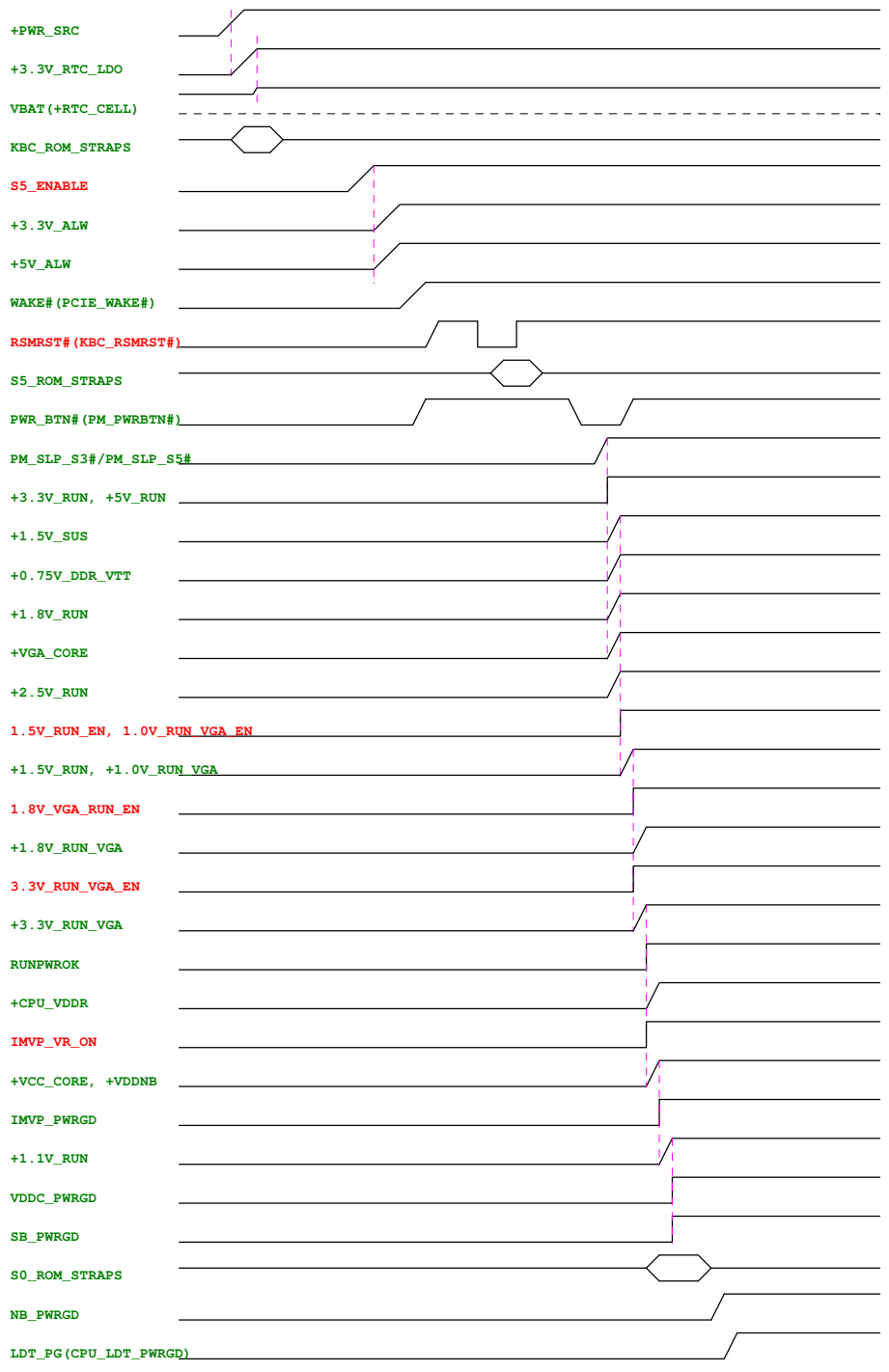


<Core Design>



Title DISCRETE VGA POWER		
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POWER SEQUENCE



<Core Design>




Title POWER SEQUENCE		
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Change notes - Page 1


VERSION	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X01	11/6	1	10	Add C1002 10uF, C1007, EC1001 0.1uF, C1008 10pF.	Insure signal quality.	EE
		2	13	Change R1314 to 4.7K.	Meet CRB.	EE
		3	51	Swap PU5101 pin3, pin4.	Correct input voltage level.	EE
		4	82	Add R8210 0R.	Reserve GPU clock input source.	EE
	11/9	1	30	Change C3014 to 2.2uF.	Reduce package size.	EE
		2	69	Change C6903 to 0.1uF.	Reduce package size.	EE
		3	49	Add PR4916 100KR.	To prevent leakage in S3 status.	EE
	11/10	1	18,19	Change DIMM socket Part Number.	Request by ME.	ME
		2	37	Add R3754 100KR.	To detect leakage current.	EE
	11/11	1	10	Modify R1028 pull-up to +1.5V_RUN.	Solve leakage in S3 status.	EE
	11/12	1	20	Change C2011 to 18pF, C2012 to 15pF.	Set accurate clock frequency.	EE
		2	37	Add C3717 10pF.	Stable singal level.	EE
		3	57	Delete RN5711, RN5705.	Redundant parts.	EE
		4	13	Delete R1331, R1332, R1308.	Redundant parts.	EE
		5	77	Add Pi-filter.	Cure EMI.	EMC
	11/13	1	20	Change X2001 P/N.	Request by Sourcer.	Sourcer
		2	7	Change R713 to 47R.	Fine tune damping.	EE
		3	82	Add R8211 80.6R, R8220 150R.	Set a voltage divider to 1.8V level swing.	EE
		4	21	Add R2133 1KR.	For UMA VRAM vendor selection.	EE
	11/16	1	22	Delete RN2203 pin 4, pin 5 connection.	Solve S5 leakage.	EE
		2	51	Change PR5105 pull-up to +3.3V_RUN.	Prevent leakage.	EE
		3	21	Add C2103, C2104 0.1uF.	For signal stability.	EE
		4	37	Add C3718 0.1uF.	For signal stability.	EE
		5	41	Add C4101, C4102 0.1uF.	For signal stability.	EE
		6	49	Add PC4923 0.1uF.	For signal stability.	EE
		7	66	Add C6601, C6602 0.1uF.	For signal stability.	EE
		8	77	Add RN7713 150R.	Move impedance matching resistor from CRT/B to M/B.	EMC
		9	78	Change CARDBD1 pin 2 link to PLTRST#_LAN_WAN.	Change card reader chip to RTS5159 to solve EMI.	EMC
11/17	1	30	Add R3014, R3017, R3020 0R to link AGND and GND.	Issue for pop noise when system boot.	EE	
	2	42,48,50	Merge 1.1V power solution on main board.	Save components.	EE, Power	
	3	77	Modify CRTBD1 pin define.	Relief EMI.	EMC	
	4	79	Add some decoupled capacitors.	Request by EMC.	EMC	
	5	37	Change R3737 to 33R, stuff C3715 10pF.	Request by EMC.	EMC	
	6	62,89	Sutff EC6203 22pF, PC8911, PC8907 0.1uF.	Request by EMC.	EMC	
	7	45,46,47	Stuff EC4502 0.1uF, PC4605, PC4609, PC4738 0.1uF.	Request by EMC.	EMC	

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X01	11/17	8	9	Delete R904.	Remove redundant layout trace.	EE
	11/18	1	81	Swap R8105, C8103 location.	Meet CRB.	EE
		2	79	Add some decoupled capacitor.	By RF team request.	RF
		3	49	Change PR4903 to 620KR.	Change to common part.	Power
	11/19	1	All	Synchronize with DJ schematic.	Schematic standardlize.	EE
		2	48	Change P/N for PU4802, PU4803, PU4804, PU4805.	Rquest by Power team	Power
		3	All	Review all capacitors tolerance.	Total review for deratig.	EE
		4	21	Add RN2105 OR.	Reserve to fine tune signal quality.	EE
		5	21	Change RN2101 to 4.7KR.	Fine tuned value for signal.	EA
		6	37	Add RN3705, R3755 OR.	To isolate layout trace to DB1 connector.	EA
		7	49	Change PC4908 to 2.2uF.	Changed by EA report.	EA
		11/20	1	54	Modify R5408 connection.	To synchronize with DJ.
	2		57	Add D7701.	To prevent leakage from RGB monitor.	EE
	3		86	Add C8626 0.1uF.	By EA report.	EA
	4		37	Add R3756 10KR, C3720 0.1uF.	Synchronize with DJ.	EE
	5		37	Delete RN3705, R3755.	For more layout space.	EE
	6		13	Delete TP1303, TP1304.	For more layout space.	EE
	7		49	Delete PR4905.	For more layout space.	EE
	8		89	Add PC8918 0.1uF.	Stable signal quality.	EE
	11/24	1	46, 49	Change PU4601, PU4901 Power components.	Request by Power team.	Power
	11/25	1	46, 47, 49, 8	Change power components.	Request by Power team.	Power
	11/29	1	10	Change C1008 to 10pF.	Fine tuned signal slew rate to meet specification.	EE
		2	30	Change R3007 to 2.2KR.	By FAE suggestion.	EE
X02	12/04	1	81	Set BOM mark R8104, R8106, R8107, R8110, R8111, R8112.	Implement co-layout Madison and M96.	EE
		2	82, 84	Add R8407, R8408 OR.	Implement co-layout Madison and M96.	EE
		3	80	Add R8016 10KR.	Implement co-layout Madison and M96.	EE
		4	83, 84	Set BOM mark.	Implement co-layout Madison and M96.	EE
		5	83	Add L8306, L8307, C8397, R8301, R8302, R8303.	Implement co-layout Madison and M96.	EE
	12/05	1	37	Change R3756, C3720 connection.	Correct soft-start for EC power.	EE
	12/08	1	90	Set BOM mark.	Implement co-layout Madison and M96.	EE
	12/15	1	15	Delete RN1501, Add G1501~G1504.	Synchronize with DJ and supply sufficient power rail.	EE
		2	62	Add R6207 100KR.	Insure SPI Write-Protect pin signal level.	EE
		3	66	Change C6602 net name.	Correct signal name.	EE
		4	81	Add R8122 1KR, RN8101 4.7KR.	Meet M96 schematic check list.	EE
		5	82	Swap CLK_VGA_27M_NSS and CLK_VGA_27M_SS connection.	Solve external RGB display tremble issue.	EE

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X02	12/16	1	66	Change R6605 to 0R.	Assure power button level set to low.	EE
		2	37,76	Add net "8103_GPO".	Implement LAN DSM hardware function.	EE
	12/17	1	37	Add U3703.	To solve SPI WP signal malfunction on EC.	EE
12/18		1	82	Add R8222 1MR.	Assure crystal resonant clock stable.	EE
		2	81	Set VRAM reset circuit.	Follow M96 reset circuit and reseve BOM option.	EE
12/25		1	18	Change TC1801 to 330uF, 2V tolerance.	Implement common part for 1.5V power rail.	EE
		2	46	Change PR4603 to 127KR.	Set 5V current limitation.	Power
		3	46	Empty PR4618 and stuff PR4619.	Set Ultra-sonic mode to keep +15V_ALW voltage level.	Power
		4	10	Set RN1006 PU to +1.5V_SUS.	Follow AMD check list and cure +1.5V_RUN leakage.	EE
		5	62	Change R6206 to 1KR.	According to Safety request, verified OK.	Safety
		6	51	Change PR5102 1KR, PR5106 8.2KR, PR5107 5.62KR.	Set VDDR low voltage level to 0.9V.	EE
12/29		1	10,37	Add Q1005, R1039, R1040.	Request by AMD to set CPU into HTC mode in DOS.	EE
		2	47	Change PR4720 93.1KR, PR4721 24KR.	Set power OCP value.	Power
12/31		1	ALL	Change some resistors as short-pad or resistor array.	Save component counts.	EE
		2	ALL	Change some capacitors with smaller value or empty.	Save component counts.	EE
01/04		1	15	Change R1507,R1508,R1509,R1510,R1511 to bead.	Filter power noise.	EMC
01/05		1	7	Combine R707,R721 as RN711.	For more layout space.	EE
		2	81	Delete TP8101,TP8102.	Remove useless test point for more layout space.	EE
		3	7,80	Delete R716,R8020, combine R8009,R8010 as RN8001.	Redundant part.	EE
		4	37,39,41	R3747,R4104 short pad, delete R3722,R3904.	Redundant part.	EE
		5	46	Change PR4620 as short pad.	Redundant part.	EE
		6	51	Change PQ5101 with ESD protector.	Change to common part.	Power
		7	54	Empty R5405 and Stuff R5408.	Avoid LCD white panel.	EE
		8	62	Change R6205 to 0R.	Already have one 1KR ahead.	EE
01/06		1	50	Add PR5004 10KR and empty PR5002.	Avoid +1.1V_ALW leakage in South Bridge.	EE
		2	13	Change R1342 to size 0603.	Synchronous schematic w/DJ.	EE
		3	79	Add R7921 and R7922.	Reserved RF team solution.	RF
01/07		1	7	Add RN712,C722,C723	Reserve for SMBus signal quality tuning.	EE
		2	60	Change EC6007,EC6008 to 0.01uF.	According FAE Request.	IDT FAE
		3	39	Add Q3904.	According thermal team request.	Thermal
		4	21,18	Change location RN2105 to RN1801, add C1823,C1824.	For SMBus signal quality fine tune.	EE
		5	39,82,83	Remove C3912,TP8301,TP8302,TP8213.	Remove dummy part for more layout space.	EE
		6	76	Reserve C7601, C7602.	Fine tune USB signal quality.	EE
01/08		1	79	Reserve EC7925,EC7926,EC7927.	Reserve by EMC team.	EMC
		2	77	Change RN7711 to 0R, L7701,L7702,L7703 to bead 22R.	According EMC measurement result.	EMC

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X02	01/08	3	18, 19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	Accordinging ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory request.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory request to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE
	03/08	1	48	Stuff PU4803 and empty PU4804.	Place the H/S and L/S MOS at the same surface.	Power

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