DJ1 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-02-10

REV : A00

DY : Nopop Component

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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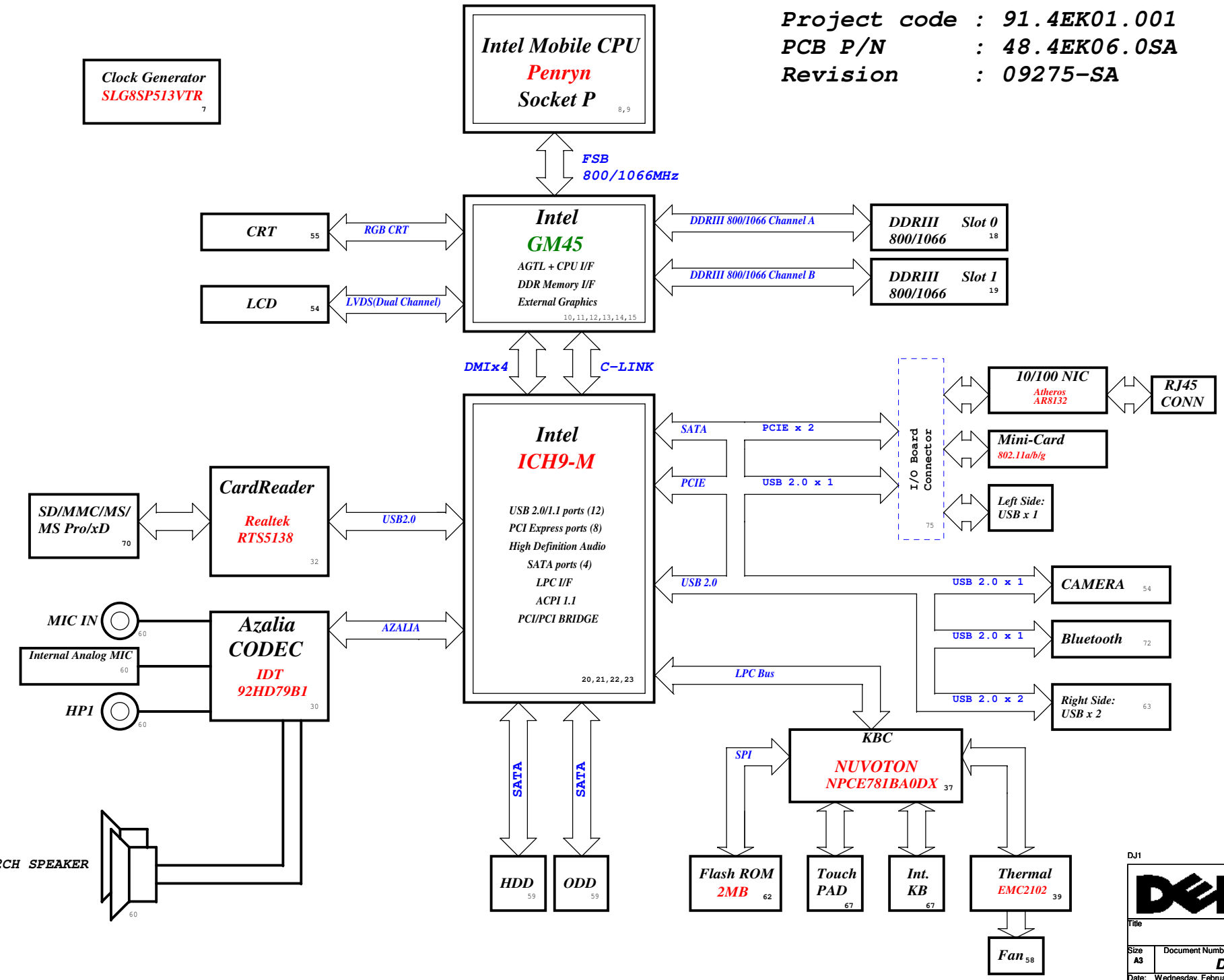
Title: *Cover Page*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 1 of 88

DJ1 Montevina UMA Block Diagram

Project code : 91.4EK01.001
PCB P/N : 48.4EK06.0SA
Revision : 09275-SA



CPU DC/DC TPS51620 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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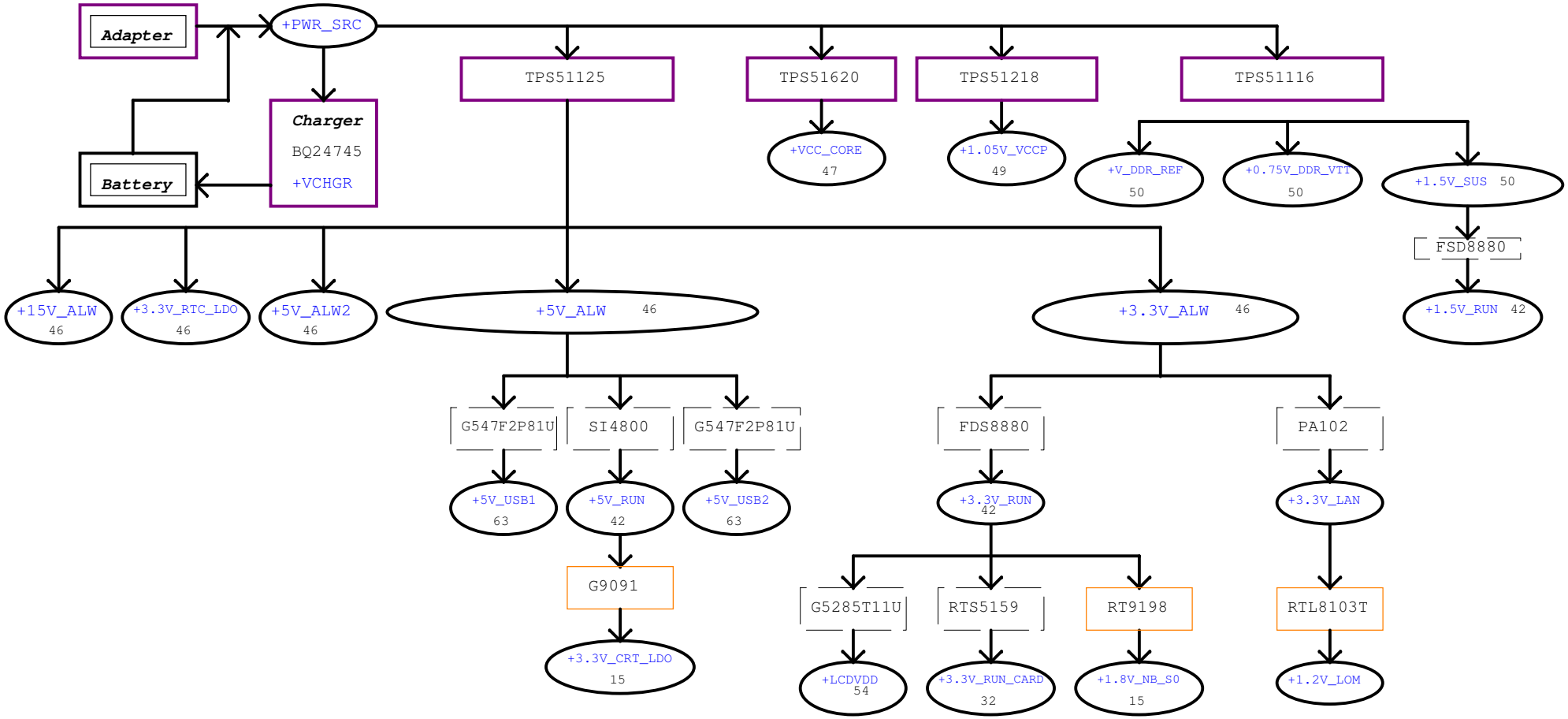
Title: Block Diagram

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 2 of 88

DJ1 Montevina UMA Power Block Diagram



Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

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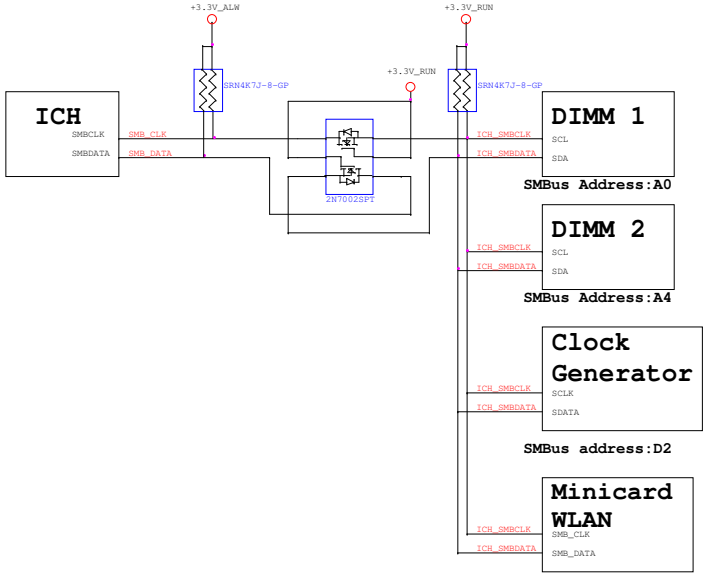
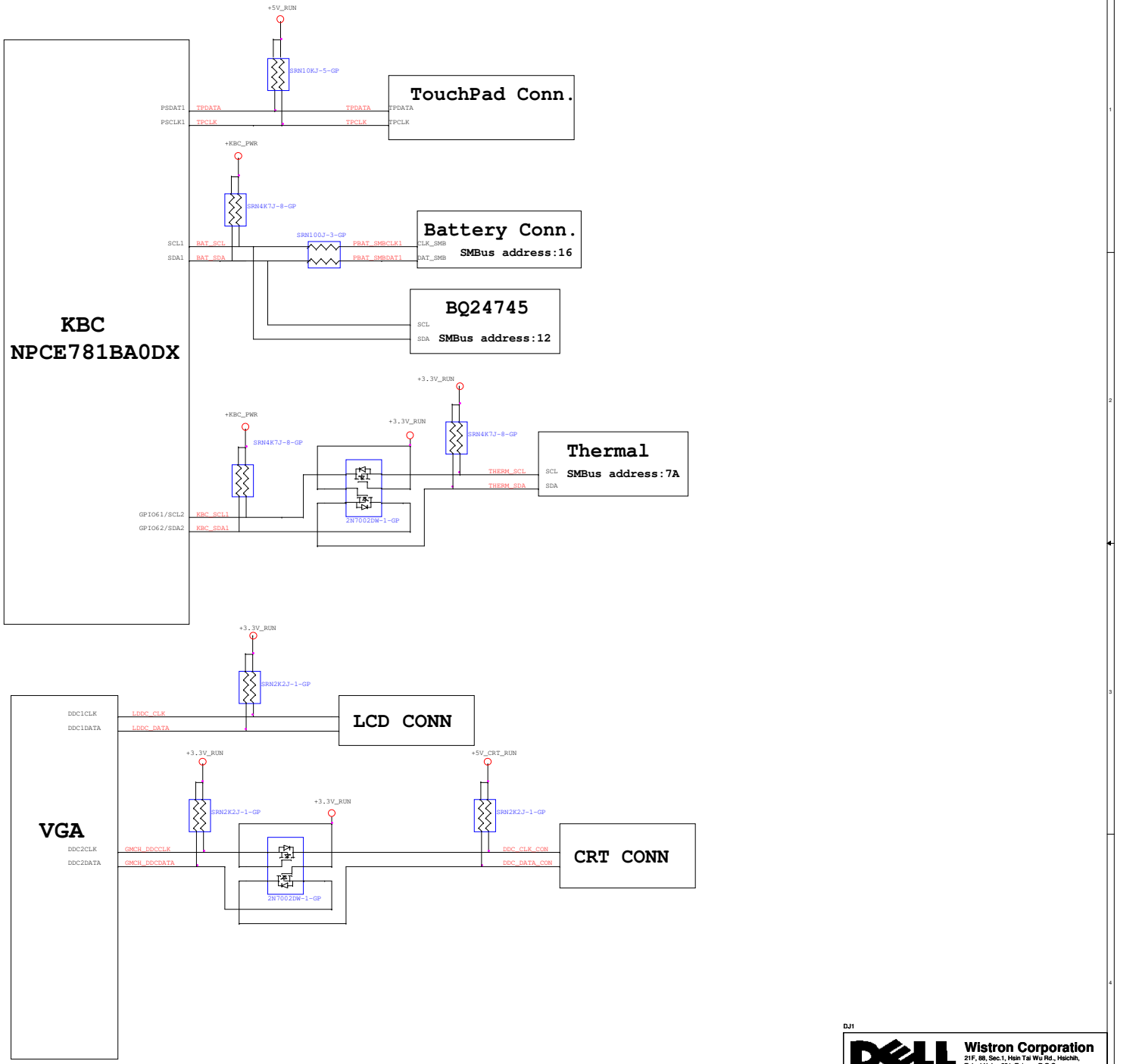
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 3 of 88

ICH SMBus Block Diagram



KBC SMBus Block Diagram



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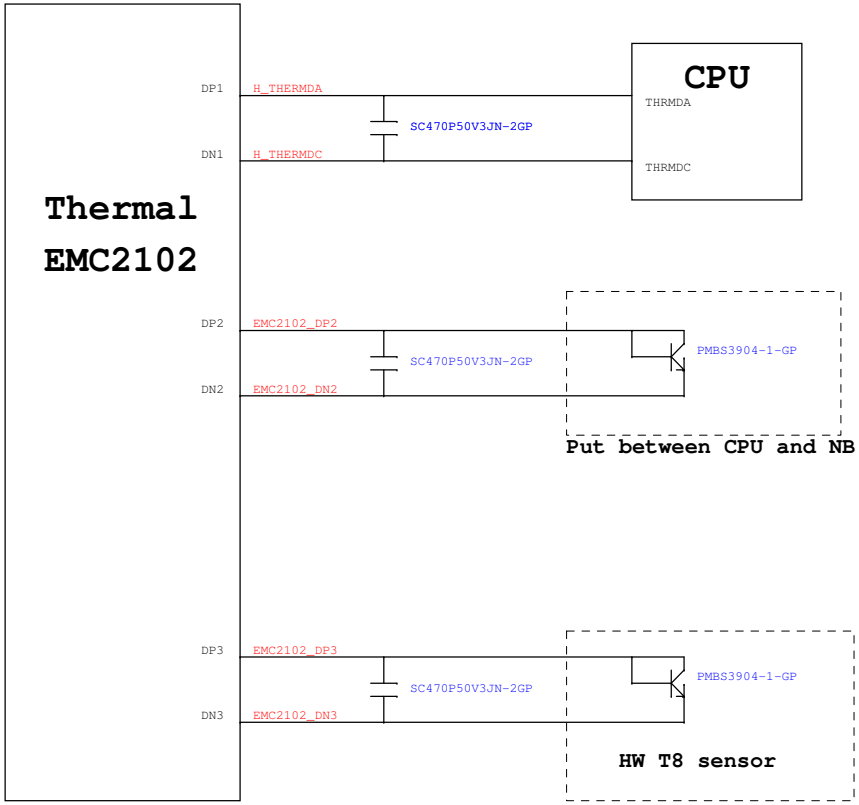
Title: SMBUS Block Diagram

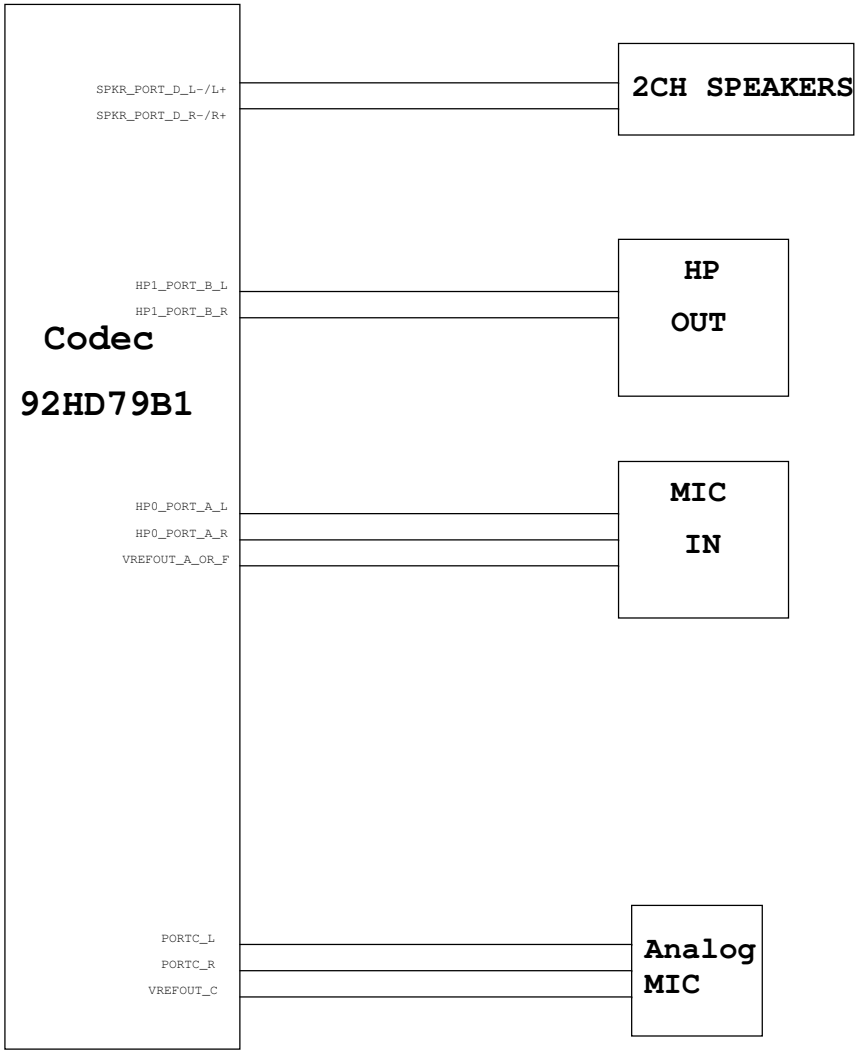
Size	Document Number	Rev
A2	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 4 of 88

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Date: Wednesday, February 24, 2010 | Sheet 5 of 88

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.2.3

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h).This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h)
GNT2#/ GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers:Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1#/ GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIcompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/ GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 (GNT0#) / Bit 10 (SPI_CS1#) / Boot BIOS Destination 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / LPC 0 / 0 / Reserved
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers:Offset 3410h:bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN# (Mobile Only)	Flash Descriptor Security Override Strap. Rising Edge of PWROK.	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Moble Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.2.3

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]#/ GPIO[55,53,51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0 (I/O Board)
1	USB1 (I/O Board 17")
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 355648 Rev.2.3

Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4 (Default)**
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) **1 = The iTPM Host Interface is disabled (default)**
CFG7	Intel Management engine crypto strap	**0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality** **1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	**0 = Reverse Lanes, 15->0, 14->1 etc.** **1 = Normal operation (default): Lane Numbered in Order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1 = Disable (Default)**
CFG12	ALLZ	0 =ALLZ mode enabled (Note 3) **1 = Disable (Default)**
CFG13	XOR	0 = XOR mode enabled (Note 3) **1 = Disable (Default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation (Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe	**0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIe is operational (default)** **1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIe are operating simultaneously via the PEG port**
SDVO _CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1 = LFP Card Present; PCIE disabled
DDPC _CTRLDATA (Note4)	Digital Display Present	**0 = Digital display (HDMI/DP) device absent (default)** **1 = Digital display (HDMI/DP) Device Present**
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

NOTE:

1. All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
4. DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

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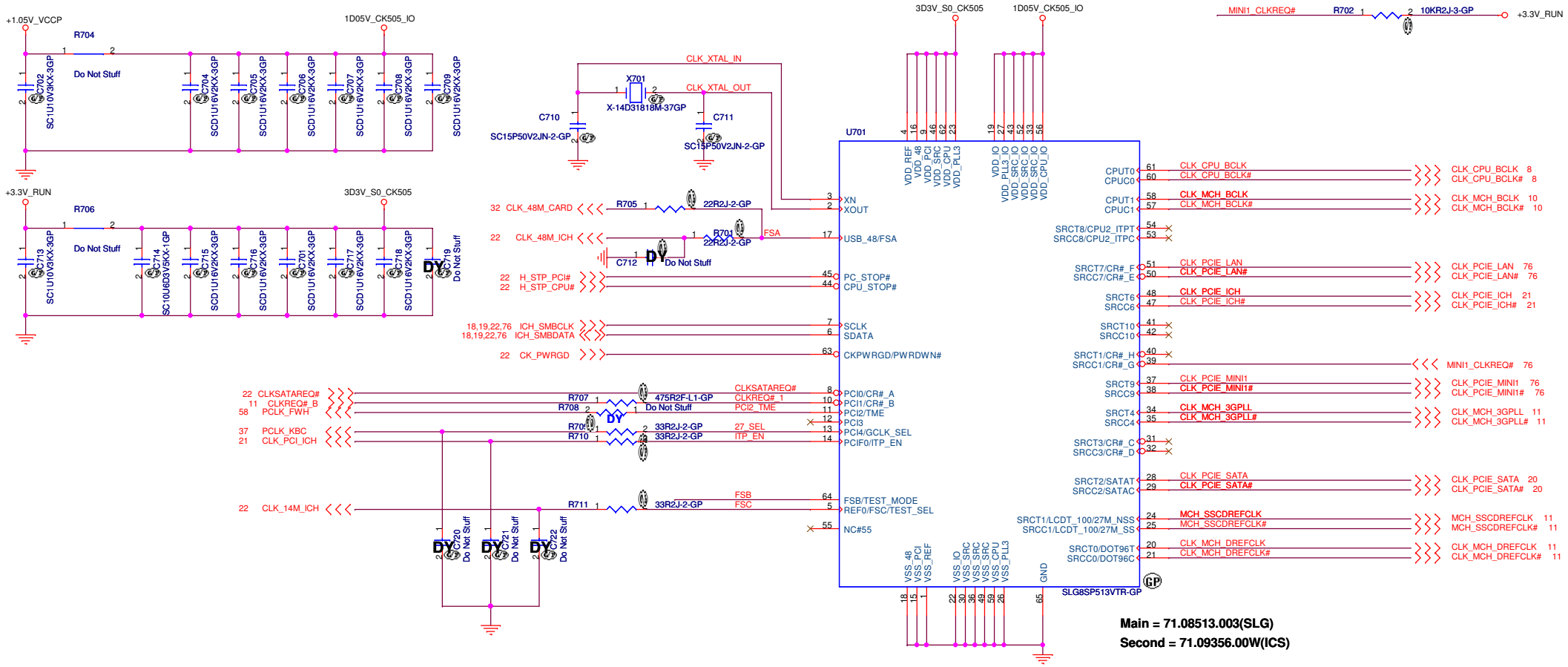
Title: Table of Content

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

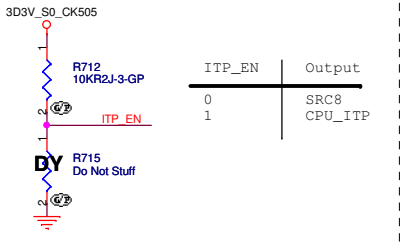
Date: Wednesday, February 24, 2010 | Sheet 6 of 88

SSID = CLOCK

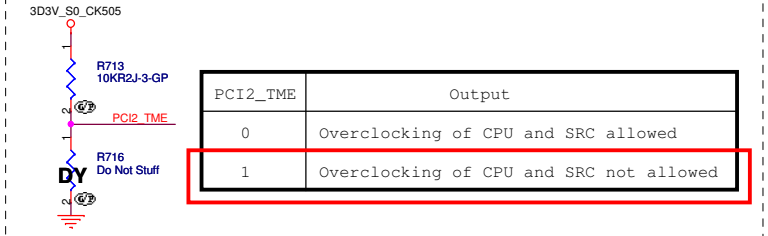


Main = 71.08513.003(SLG)

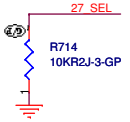
Second = 71.09356.00W(ICS)



ITP_EN	Output
0	SRC8
1	CPU_ITP

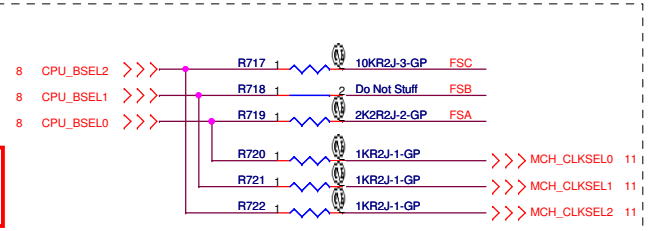


PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed



27_SEL	PIN20/21	PIN24/25
0	96M	100M
1	100M	27M

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M



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Title: **Clock Generator SLG8SP513VTR**

Size: Custom | Document Number: **DJ1 Montevina UMA** | Rev: **A00**

Date: Friday, February 26, 2010 | Sheet 7 of 88

SSID = CPU

CPU1A 1 OF 4

BGA479-SKT6-GPU7
62.10079.001

CPU1B 2 OF 4

BGA479-SKT6-GPU7
62.10079.001

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

H_THRMTRIP# should connect to ICH9 and MCH without T-ing.

Layout notes
Z= 55 Ohm 0.5" MAX for CPU_GTLREF0

All place within 2" to CPU

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

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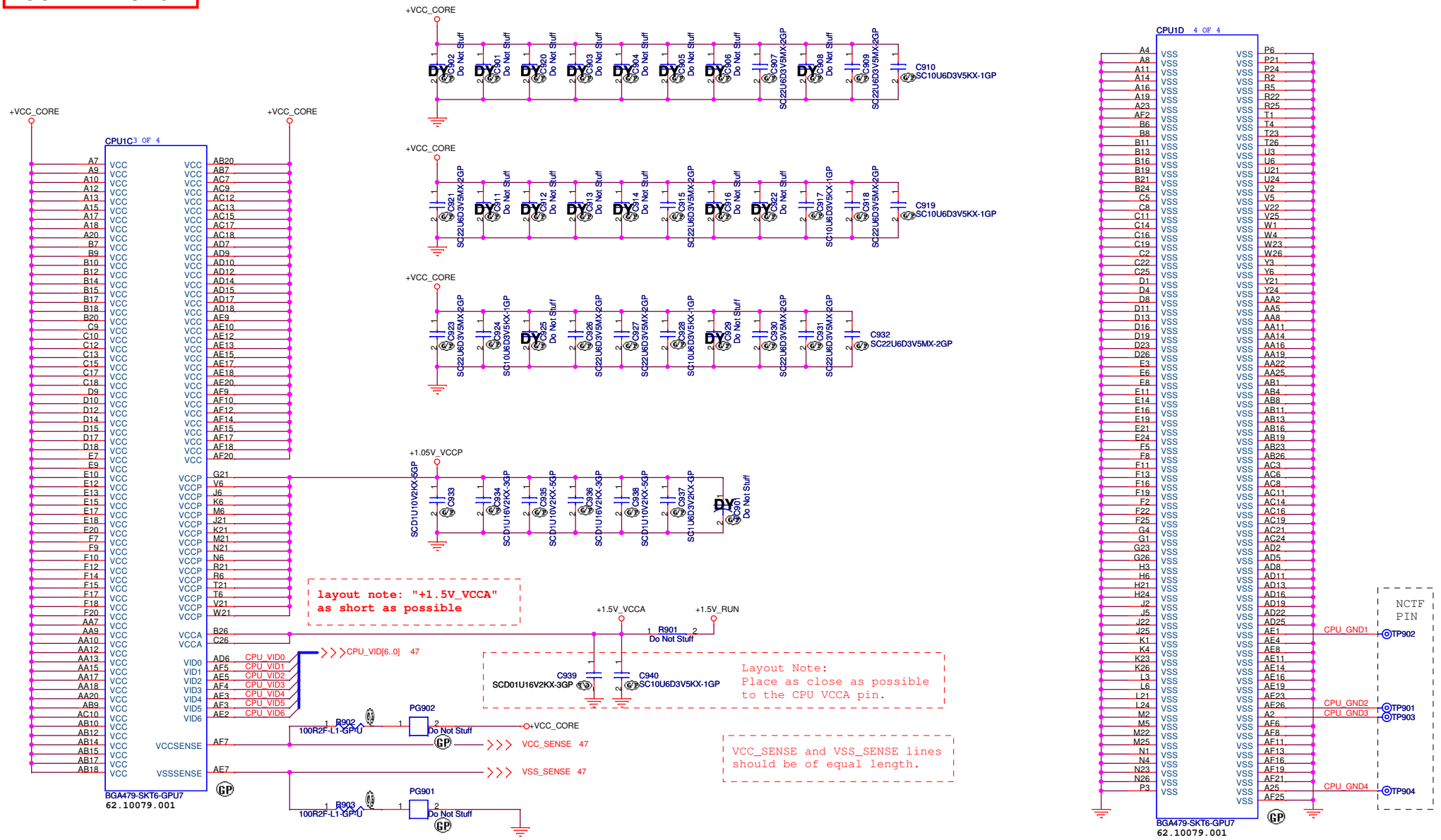
Title: CPU-FSB(1/2)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 8 of 88

SSID = CPU



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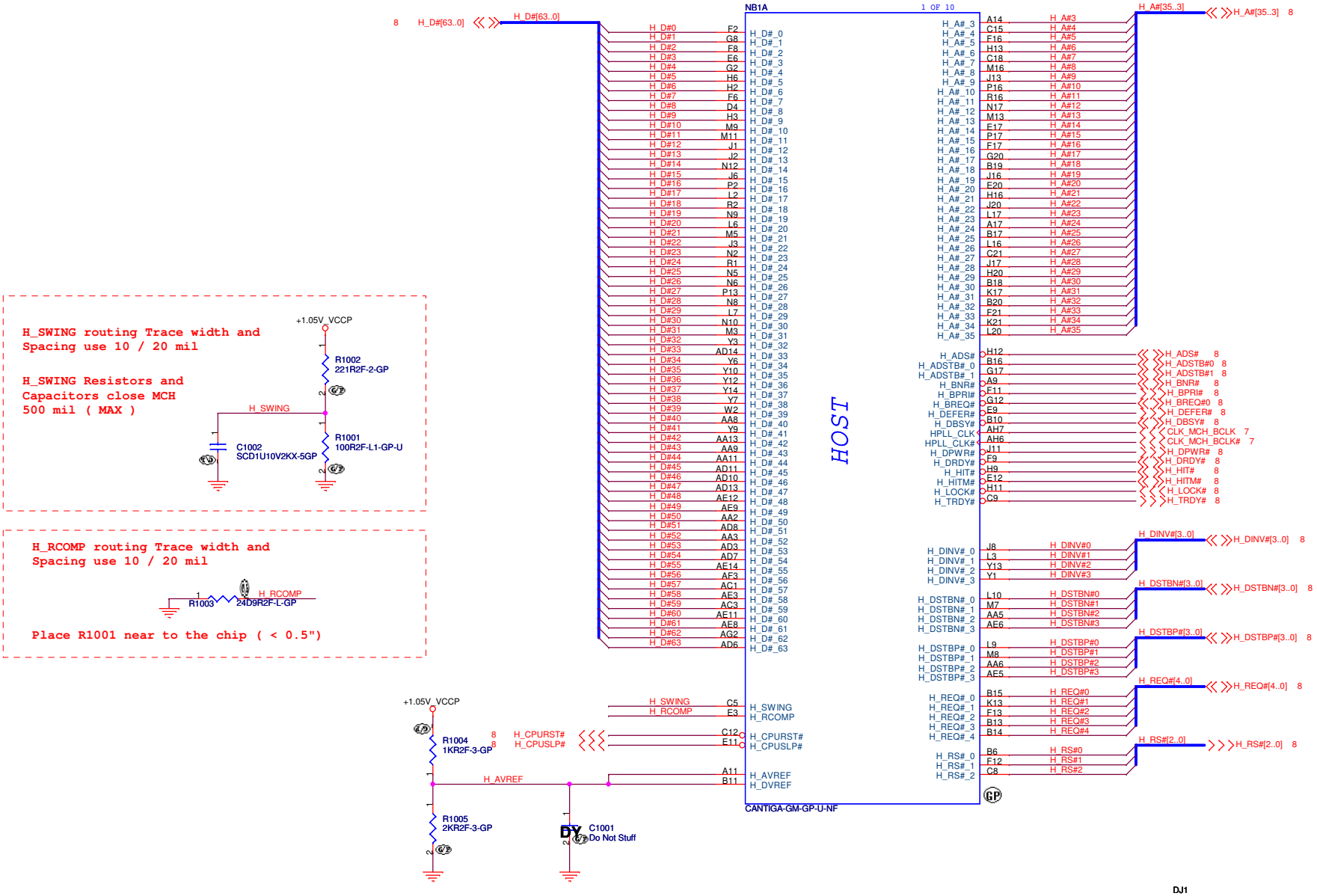
Title: ***CPU-Power(2/2)***

Size	Document Number	Rev
Custom	***DJ1 Montevina UMA***	***A00***

Date: Friday, February 26, 2010 Sheet 9 of 88

SSID = MCH



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Title: *Cantiga-Host(1/6)*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Friday, February 26, 2010 | Sheet 10 of 88

SSID = MCH

* is current setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	ITPM enable	ITPM disable *
CFG 7	TLS cipher suite with no confidentiality	TLS cipher suite with confidentiality *
CFG 9	PCIE GFX lane reversed	PCIE GFX lane numbered in oder *
CFG 10	PCIE loopback enable	PCIE loopback disable *
CFG 12	ALLZ mode enable	ALLZ mode disable *
CFG 13	XOR mode enable	XOR mode disable *
CFG 16	FSB dynamic ODT disable	FSB Dynamic ODT enable *
CFG 19 DMI Lane Reserved	Normal operation *	Reverse DMI lanes
CFG 20 SDVO concurrent with PCIE	Only PCIE or SDVO is operational *	PCIE and SDVO are operatiing simultaneously via the PEG port
SDVO_CTRLDATA	SDVO interface disable *	SDVO interface enable
L_DDC_DATA	LFP disable *	LFP card present
DDPC_CTRLDATA	SDVO/iHDMI/DP interface disabled *	SDVO/iHDMI/DP interface enabled

NB1B — 2 OF 10

CANTIGA-GM-GP-U-NF

RSVD: RESERVED#M36, RESERVED#N36, RESERVED#R33, RESERVED#T33, RESERVED#AH9, RESERVED#AH10, RESERVED#AH12, RESERVED#AH13, RESERVED#K12, RESERVED#AL34, RESERVED#AK34, RESERVED#AN35, RESERVED#AM35, RESERVED#T24, RESERVED#B31, RESERVED#B2, RESERVED#M1, RESERVED#AY21, RESERVED#BG23, RESERVED#BF23, RESERVED#BH18, RESERVED#BF18

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 AP24 → M_CLK_DDR0 18; SA_CK_1 AT21 → M_CLK_DDR1 18; SB_CK_0 AV24 → M_CLK_DDR2 19; SB_CK_1 AU20 → M_CLK_DDR3 19; SA_CK#_0 AR24 → M_CLK_DDR#0 18; SA_CK#_1 AR21 → M_CLK_DDR#1 18; SB_CK#_0 AU24 → M_CLK_DDR#2 19; SB_CK#_1 AV20 → M_CLK_DDR#3 19; SA_CKE_0 BC28 → M_CKE0 18; SA_CKE_1 AY28 → M_CKE1 18; SB_CKE_0 AY36 → M_CKE2 19; SB_CKE_1 BB36 → M_CKE3 19; SA_CS#_0 BA17 → M_CS#0 18; SA_CS#_1 AY16 → M_CS#1 18; SB_CS#_0 AV16 → M_CS#2 19; SB_CS#_1 AR13 → M_CS#3 19; SA_ODT_0 BD17 → M_ODT0 18; SA_ODT_1 AY17 → M_ODT1 18; SB_ODT_0 BF15 → M_ODT2 19; SB_ODT_1 AY13 → M_ODT3 19; SM_RCOMP BG22 → M_RCOMPP; SM_RCOMP# BH21 → M_RCOMPN; SM_RCOMP_VOH BF28 → SM_RCOMP_VOH; SM_RCOMP_VOL BH28 → SM_RCOMP_VOL; SM_VREF AV42 → CANTIGA_SM_VREF; SM_PWROK AR36 → SM_PWROK; SM_REXT BF17 → SM_REXT; SM_DRAMRST# BC36 → DDR3_DRAMRST#

CLK: DPLL_REF_CLK AB38 → CLK_MCH_DREFCLK 7; DPLL_REF_CLK# A38 → CLK_MCH_DREFCLK# 7; DPLL_REF_SSCLK E41 → MCH_SSCDREFCLK 7; DPLL_REF_SSCLK# F41 → MCH_SSCDREFCLK# 7; PEG_CLK F43 → CLK_MCH_3GPLL 7; PEG_CLK# E43 → CLK_MCH_3GPLL# 7

DMI: DMI_RXN_0 AE41 → DMI_ITXN0_MRXN0 21; DMI_RXN_1 AE37 → DMI_ITXN1_MRXN1 21; DMI_RXN_2 AE47 → DMI_ITXN2_MRXN2 21; DMI_RXN_3 AH39 → DMI_ITXN3_MRXN3 21; DMI_RXP_0 AE40 → DMI_ITXP0_MRXP0 21; DMI_RXP_1 AE38 → DMI_ITXP1_MRXP1 21; DMI_RXP_2 AE48 → DMI_ITXP2_MRXP2 21; DMI_RXP_3 AH40 → DMI_ITXP3_MRXP3 21; DMI_TXN_0 AE35 → DMI_IRXN0_MTXN0 21; DMI_TXN_1 AE43 → DMI_IRXN1_MTXN1 21; DMI_TXN_2 AE46 → DMI_IRXN2_MTXN2 21; DMI_TXN_3 AH42 → DMI_IRXN3_MTXN3 21; DMI_TXP_0 AD35 → DMI_IRXP0_MTXP0 21; DMI_TXP_1 AE44 → DMI_IRXP1_MTXP1 21; DMI_TXP_2 AF46 → DMI_IRXP2_MTXP2 21; DMI_TXP_3 AH43 → DMI_IRXP3_MTXP3 21

CFG: CFG_0 T25, CFG_1 R25, CFG_2 P25, CFG_3 P20, CFG_4 P24, CFG_5 C25, CFG_6 N24, CFG_7 M24, CFG_8 E21, CFG_9 C23, CFG_10 C24, CFG_11 N21, CFG_12 P21, CFG_13 T21, CFG_14 R20, CFG_15 M20, CFG_16 L21, CFG_17 H21, CFG_18 P29, CFG_19 R28, CFG_20 T28

PM: PM_SYNC# R29, PM_DPRSTP# B7, PM_EXT_TS#_0 N33, PM_EXT_TS#_1 P32, PWROK AT40, RSTIN# AT11, THERMTRIP# T20, DPRSLPVR R32

GRAPHICS VID: GFX_VID_0 B33, GFX_VID_1 B32, GFX_VID_2 G33, GFX_VID_3 F33, GFX_VID_4 E33, GFX_VR_EN C34

ME: CL_CLK AH37 → CL_CLK0 22; CL_DATA AH36 → CL_DATA0 22; CL_PWROK AN36 → M_PWROK 22; CL_RST# AJ35 → CL_RST#0 22; CL_VREF AH34 → MCH_CLVREF

MISC: DDPC_CTRLCLK N28, DDPC_CTRLDATA M28, SDVO_CTRLCLK G36, SDVO_CTRLDATA E36 → GMCH_HDMI_DATA → TP1106, CLKREQ# K36 → CLKREQ#_B 7, ICH_SYNC# H36 → MCH_ICH_SYNC# 22; TSATN# B12 → TSATN#

HDA: HDA_BCLK B28, HDA_RST# B30, HDA_SDI B29, HDA_SDO C29, HDA_SYNC A28

NC: NC#BG48, NC#BF48, NC#BD48, NC#BC48, NC#BH47, NC#BG47, NC#BE47, NC#BH46, NC#BF46, NC#BG45, NC#BH44, NC#BH43, NC#BH6, NC#BH5, NC#BG4, NC#BH3, NC#BF3, NC#BH2, NC#BG2, NC#BE2, NC#BG1, NC#BF1, NC#BD1, NC#BC1, NC#F1, NC#A47

FSB setting: 7 MCH_CLKSEL0, 7 MCH_CLKSEL1, 7 MCH_CLKSEL2

+1.5V_SUS: R1103 80D6R2F-L-GP; R1105 80D6R2F-L-GP; R1102 1KR2F-3-GP; R1104 3K01R2F-3-GP; R1106 1KR2F-3-GP; SM_RCOMP_VOH; SM_RCOMP_VOL; C1102 SC2D2U6D3V3KX-GP; C1103 SCD01U16V2KX-3GP; C1104 SC2D2U6D3V3KX-GP; C1101 SCD01U16V2KX-3GP

+V_DDR_REF: R1108 Do Not Stuff; R1109 499R2F-2-GP; C1105 Do Not Stuff; C1106 Do Not Stuff

+3.3V_RUN: R1112 DY Do Not Stuff CFG19; R1113 DY Do Not Stuff CFG20; RN1102 PM_EXTTS#0 PM_EXTTS#1 SRN10KJ-5-GP

R1118 DY Do Not Stuff CFG9; R1119 DY Do Not Stuff CFG10; R1124 DY Do Not Stuff CFG16

TP1102 TP1103 CFG3 CFG4; TP1104 TP1105 CFG14 CFG15 CFG16; TP1101 CFG17; CFG9 CFG10 CFG19 CFG20

22 PM_SYNC# 8,20,47 H_DPRSTP# 18 PM_EXTTS#0 19 PM_EXTTS#1; 22,37 PM_PWROK 21,37,58,76 PLT_RST#; R1125 Do Not Stuff 100R2J-2-GP; R1127 Do Not Stuff; C1107 DY; PWROK_R; RSTIN#

8,20,37,42 H_THRMTRIP#; 22,47 DPRSLPVR

+1.05V_VCCP: R1126 1KR2F-3-GP; R1128 499R2F-2-GP; C1108 SCD1U10V2KX-5GP; MCH_CLVREF ~= 0.35V

+3.3V_RUN: R1122 56R2J-4-GP; R1123 DY Do Not Stuff; TSATN# KBC → TSATN# KBC 37; TSATN# B; Q1101 DY Do Not Stuff; R1129 10KR2J-3-GP; CLKREQ# B

DJ1

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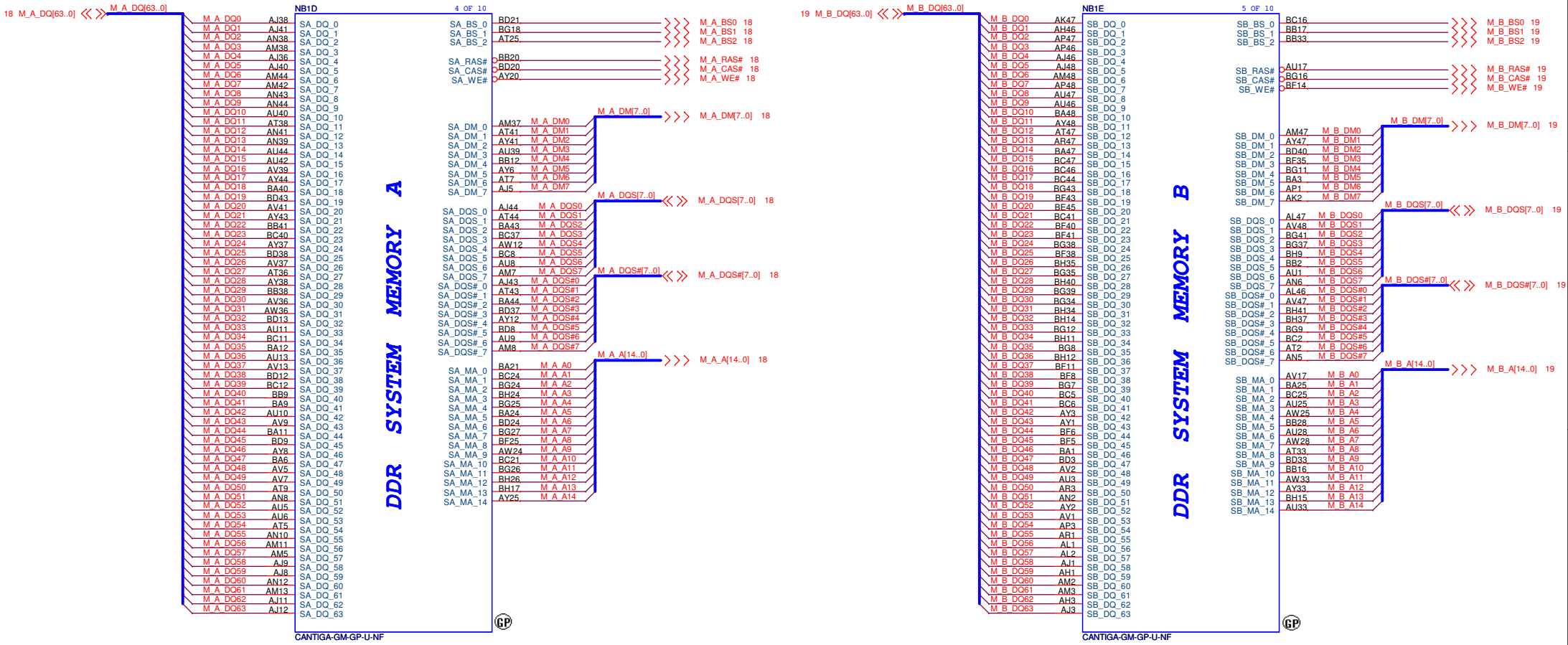
Title: Cantiga-DMI/CFG(2/6)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 11 of 88

SSID = MCH



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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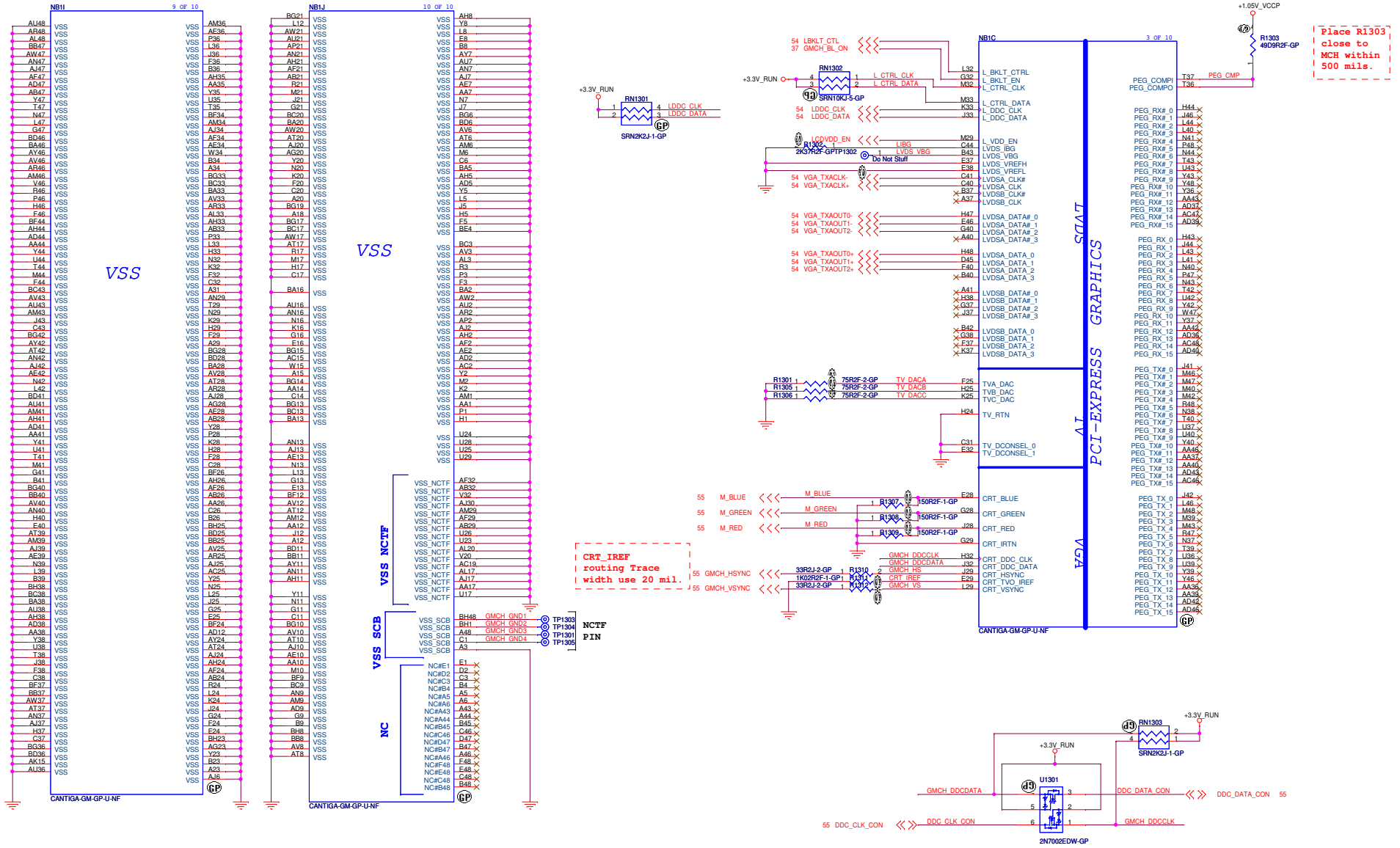
Title: Cantiga-DDR(3/6)

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 12 of 88

SSID = MCH



DJ1

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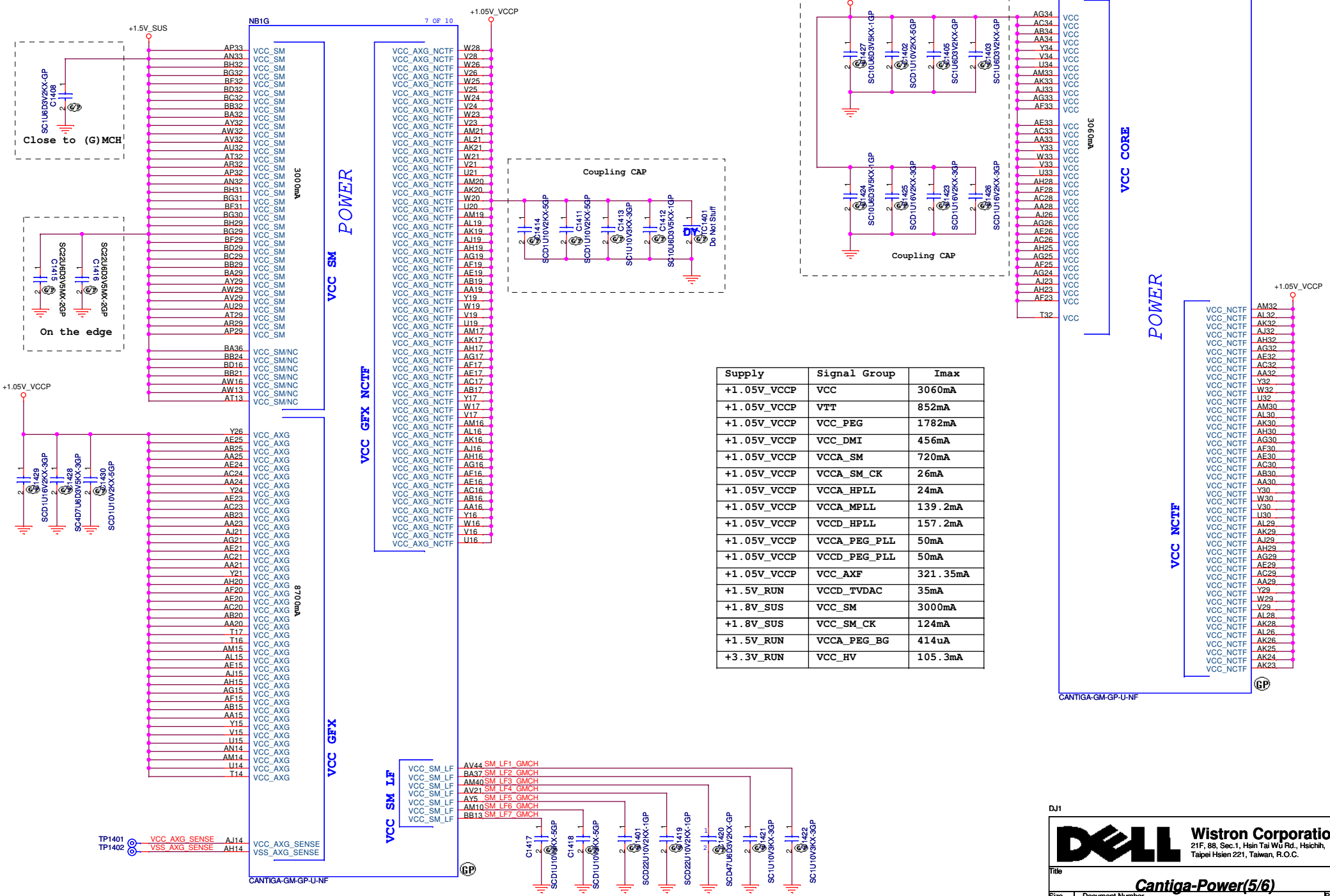
Title: Cantiga-GND/LVDS/VGA(4/6)

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 13 of 88

SSID = MCH



Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCCD_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

DJ1

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Title: ***Cantiga-Power(5/6)***

Size	Document Number	Rev
Custom	***DJ1 Montevina UMA***	***A00***

Date: Wednesday, February 24, 2010 Sheet 14 of 88

SSID = MCH

POWER

NB1H — 8 OF 10 — CANTIGA-GM-GP-U-NF

CRT
- B27 VCCA_CRT_DAC
- A26 VCCA_CRT_DAC
- A25 VCCA_DAC_BG
- B25 VSSA_DAC_BG

PLL
- F47 VCCA_DPLLA 64.8mA
- L48 VCCA_DPLLB
- AD1 VCCA_HPLL 24mA
- AE1 VCCA_MPLL 139.2mA

LVDS
- J48 VCCA_LVDS 13.2mA
- J47 VSSA_LVDS

PEG
- AD48 VCCA_PEG_BG 414uA
- AA48 VCCA_PEG_PLL 50mA

SM
- AR20, AP20, AN20, AB17, AP17, AN17, AT16, AR16, AP16 VCCA_SM 720mA

CK
- AP28, AN28, AP25, AN25, AN24, AM28, AM26, AM25, AL25, AM24, AL24, AM23, AL23 VCCA_SM_CK 37.5mA
- VCCA_SM_CK_NCTF

TV
- B24 VCCA_TV_DAC
- A24 VCCA_TV_DAC 79mA

HDA
- A32 VCC_HDA 50mA

DAC/CRT
- M25 VCCD_TVDAC 35mA
- L28 VCCD_QDAC 2mA
- AF1 VCCD_HPLL 157.2mA
- AA47 VCCD_PEG_PLL 50mA

LVDS
- M38, L37 VCCD_LVDS 60.31mA

VTT
- U13, T13, U12, T12, U11, T11, U10, T10, U9, T9, U8, T8, U7, T7, U6, T6, U5, T5, V3, U3, V2, U2, T2, V1, U1 VTT 852mA

AXF
- B22 VCC_AXF
- B21 VCC_AXF
- A21 VCC_AXF 321.35mA

SM_CK
- BF21 VCC_SM_CK
- BH20 VCC_SM_CK
- BG20 VCC_SM_CK
- BF20 VCC_SM_CK 124mA

VCC_TX_LVDS
- K47 VCC_TX_LVDS 118.8mA

HV
- C35 VCC_HV
- B35 VCC_HV
- A35 VCC_HV 195.3mA

PEG
- V48 VCC_PEG
- U48 VCC_PEG
- V47 VCC_PEG
- U47 VCC_PEG
- U46 VCC_PEG 1792mA

DMI
- AH48 VCC_DMI
- AF48 VCC_DMI
- AH47 VCC_DMI
- AG47 VCC_DMI 456mA

VTTLF
- A8 VTTLF
- L1 VTTLF
- AB2 VTTLF

+1.05V_VCCP
- R1502 Do Not Stuff — M_VCCA_DPLLA — C1502 SCD1U16V2KX-3GP, C1503 SCD1U16V2KX-3GP, DY C1504 Do Not Stuff
- R1504 Do Not Stuff — M_VCCA_DPLLB — C1511 SCD1U16V2KX-3GP, C1512 SCD1U16V2KX-3GP, DY C1513 Do Not Stuff

+3.3V_CRT_LDO
- R1503 Do Not Stuff — 3D3V_CRTDAC_S0 — C1505 SCD01U16V2KX-3GP, C1506 SCD1U10V2KX-5GP
- R1505 Do Not Stuff — M_VCCA_DAC_BG — C1514 SCD01U16V2KX-3GP, C1515 SCD1U10V2KX-5GP

1D8V_TXLVDS_S3
- C1518 SC1KP50V2KX-1GP

+1.5V_RUN
- R1508 Do Not Stuff — VCCA_PEG_BG — C1519 SCD1U10V2KX-5GP

+1.05V_VCCP
- L1502 BLM18PG121SN1D-GP 120ohm 100MHz — M_VCCA_HPLL — C1516 SC4D7U6D3V3KX-GP, C1517 SCD1U10V2KX-5GP
- L1501 BLM18PG121SN1D-GP 120ohm 100MHz — M_VCCA_MPLL — DY C1520 Do Not Stuff, C1521 SCD1U10V2KX-5GP

+1.05V_VCCP
- R1510 Do Not Stuff — 1D05V_SM — DY C1502 Do Not Stuff, DY C1501 Do Not Stuff, C1524 SC22U6D3V5MX-2GP, C1525 SC4D7U6D3V3KX-GP, C1526 SC1U10V3KX-3GP

+1.05V_VCCP
- L1503 BLM18BB221SN1D-GP 220ohm 100MHz — 1D05V_RUN_PEGPLL — C1533 SC10U6D3V5KX-1GP, C1529 SCD1U10V2KX-5GP

+1.05V_VCCP
- R1513 Do Not Stuff — 1D05V_SM_CK — C1530 SC22U6D3V5MX-2GP, DY C1534 Do Not Stuff, C1531 SCD1U10V2KX-5GP

+1.5V_RUN
- L1504 PBY160808T-181Y-GP — 1D5VRUN_QDAC — C1540 SCD01U16V2KX-3GP, C1541 SCD1U10V2KX-5GP

+3.3V_CRT_LDO
- R1515 Do Not Stuff — +3.3V_TV_DAC — Do Not Stuff C1537, DY C1538 Do Not Stuff

+1.5V_RUN
- R1516 Do Not Stuff — VCCD_TVDAC — C1559 SCD1U10V2KX-5GP, C1560 SCD01U16V2KX-3GP

+1.05V_VCCP
- R1520 Do Not Stuff — 1D5VRUN_QDAC, 1D05V_RUN_HPLL, 1D05V_RUN_PEGPLL — C1547 SCD1U10V2KX-5GP, C1548 SCD1U10V2KX-5GP

+1.8V_NB_S0
- R1521 Do Not Stuff — 1D8V_SUS_DLVDS — C1555 SCD1U10V2KX-5GP

R1522 Do Not Stuff — VCC_HDA

+1.05V_VCCP
- C1507 SCD1U16V2KX-3GP
- C1508 SC1U10V3KX-3GP
- C1509 SC1U10V3KX-3GP
- C1510 SC1U10V3KX-3GP
- EC1501 SC1U10V3KX-3GP
- DY C1501 Do Not Stuff

+3.3V_RUN — I=300mA — +1.8V_NB_S0 — NB:180mA
- SC1U6D3V2KX-GP C1557
- U1501 VIN, GND, EN, NC#4, VOUT — G9091-180T11U-GP 74.09091.G3F
- SC1U6D3V2KX-GP C1558

+1.05V_VCCP
- R1509 Do Not Stuff — 1D05V_VCC_AXF — C1522 SC1U10V3KX-3GP, DY C1523 Do Not Stuff

+1.5V_SUS
- R1511 Do Not Stuff — 1D8V_VCC_SM_CK — C1532 SCD1U10V2KX-5GP, R1512 1R3F-GP, C1535 SC10U6D3V3MX-GP

+1.8V_NB_S0
- R1514 Do Not Stuff — 1D8V_TXLVDS_S3 — C1536 SC1KP50V2KX-1GP, C1539 SC22U6D3V5MX-2GP

+3.3V_RUN, +3.3V_VCC_HV
- R1523 Do Not Stuff

+3.3V_VCC_HV
- C1542 SCD1U10V2KX-5GP

+1.05V_VCCP
- C1543 SC4D7U6D3V3KX-GP
- C1544 SC10U6D3V5KX-1GP
- C1545 SC10U6D3V5KX-1GP
- C1546 SC10U6D3V5KX-1GP

+1.05V_VCCP
- R1501 Do Not Stuff — 1D05V_VCC_DMI — C1550 SCD1U10V2KX-5GP

DJ1

- C1551 SCD47U6D3V2KX-GP
- C1552 SCD47U6D3V2KX-GP
- C1553 SCD47U6D3V2KX-GP

VTTLF1, VTTLF2, VTTLF3

+5V_RUN
- C1549 SC1U10V3KX-3GP
- U1502 EN, GND, VIN, VOUT, NC#5 — G9091-330T12U-GP
- +3.3V_CRT_LDO
- C1554 SC10U6D3V5KX-1GP

74.09091.H3F

Second = 74.09198.07F

Reserved for CRT ripple

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Title: Cantiga-Power/Filter(6/6)

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Wednesday, February 24, 2010 | Sheet 15 of 88

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DJ1

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Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 16 of 88

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DJ1

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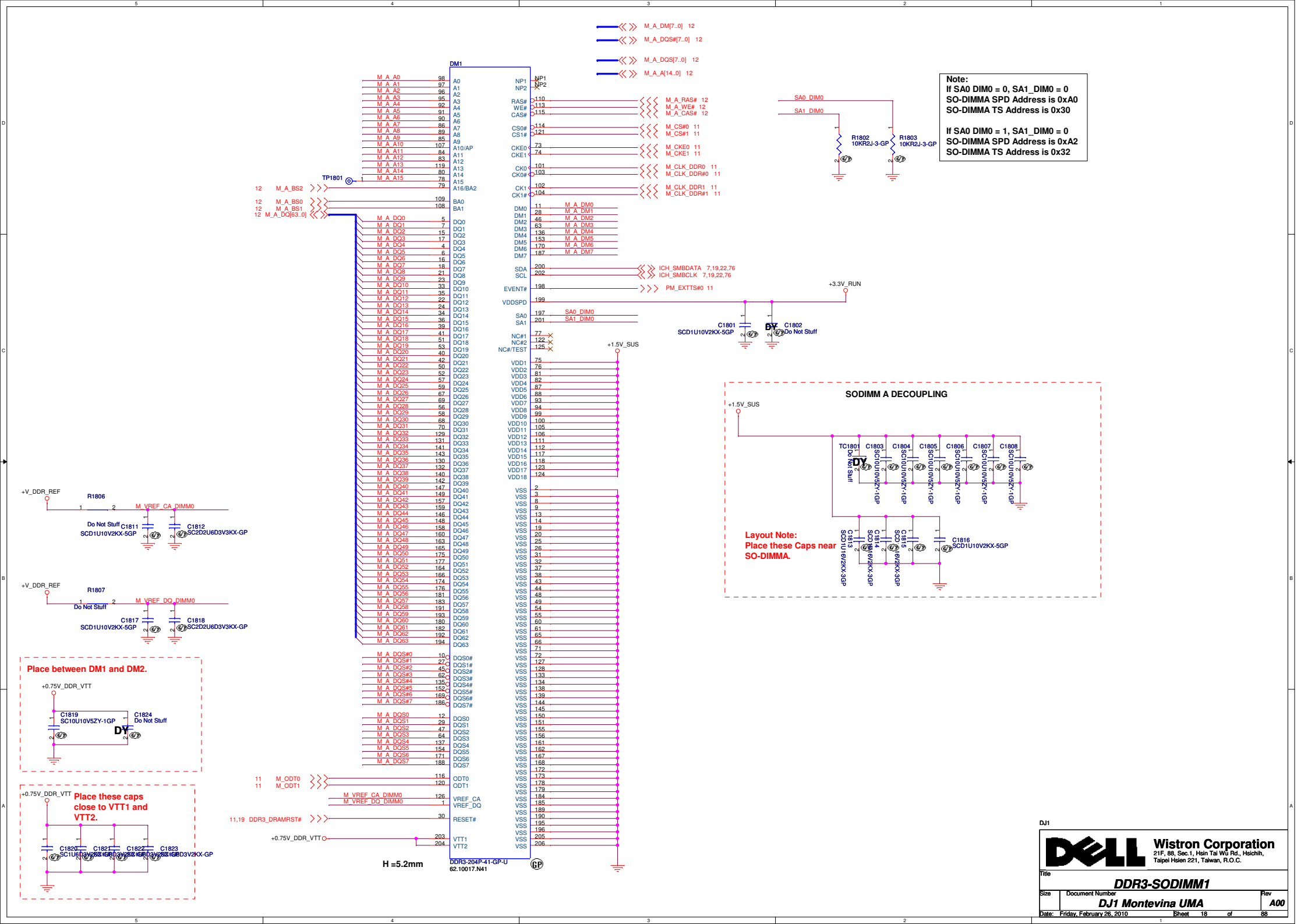
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 17 of 88


M_A_DM[7..0] 12
M_A_DQS#[7..0] 12
M_A_DQS[7..0] 12
M_A_A[14..0] 12
DM1
DDR3-204P-41-GP-U
62.10017.N41
H =5.2mm
TP1801
M_A_BS2 12
M_A_BS0 12
M_A_BS1 12
M_A_DQ[63..0] 12
M_A_RAS# 12
M_A_WE# 12
M_A_CAS# 12
M_CS#0 11
M_CS#1 11
M_CKE0 11
M_CKE1 11
M_CLK_DDR0 11
M_CLK_DDR#0 11
M_CLK_DDR1 11
M_CLK_DDR#1 11
ICH_SMBDATA 7,19,22,76
ICH_SMBCLK 7,19,22,76
PM_EXTTS#0 11
M_ODT0 11
M_ODT1 11
11,19 DDR3_DRAMRST#
+0.75V_DDR_VTT
+1.5V_SUS
+3.3V_RUN
SA0_DIM0
SA1_DIM0
R1802 10KR2J-3-GP
R1803 10KR2J-3-GP
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
C1801 SCD1U10V2KX-5GP
C1802 DY Do Not Stuff
SODIMM A DECOUPLING
TC1801 Do Not Stuff DY
C1803 SC10U10V5ZY-1GP
C1804 SC10U10V5ZY-1GP
C1805 SC10U10V5ZY-1GP
C1806 SC10U10V5ZY-1GP
C1807 SC10U10V5ZY-1GP
C1808 SC10U10V5ZY-1GP
C1813 SCD1U16V2KX-3GP
C1814 SCD1U16V2KX-3GP
C1815 SCD1U16V2KX-3GP
C1816 SCD1U10V2KX-5GP
Layout Note:
Place these Caps near SO-DIMMA.
+V_DDR_REF
R1806
M_VREF_CA_DIMM0
Do Not Stuff
C1811 SCD1U10V2KX-5GP
C1812 SC2D2U6D3V3KX-GP
R1807
M_VREF_DQ_DIMM0
Do Not Stuff
C1817 SCD1U10V2KX-5GP
C1818 SC2D2U6D3V3KX-GP
Place between DM1 and DM2.
+0.75V_DDR_VTT
C1819 SC10U10V5ZY-1GP
C1824 DY Do Not Stuff
Place these caps close to VTT1 and VTT2.
C1820
C1821
C1822
C1823
SC10U6D3V5MX-GP
DJ1
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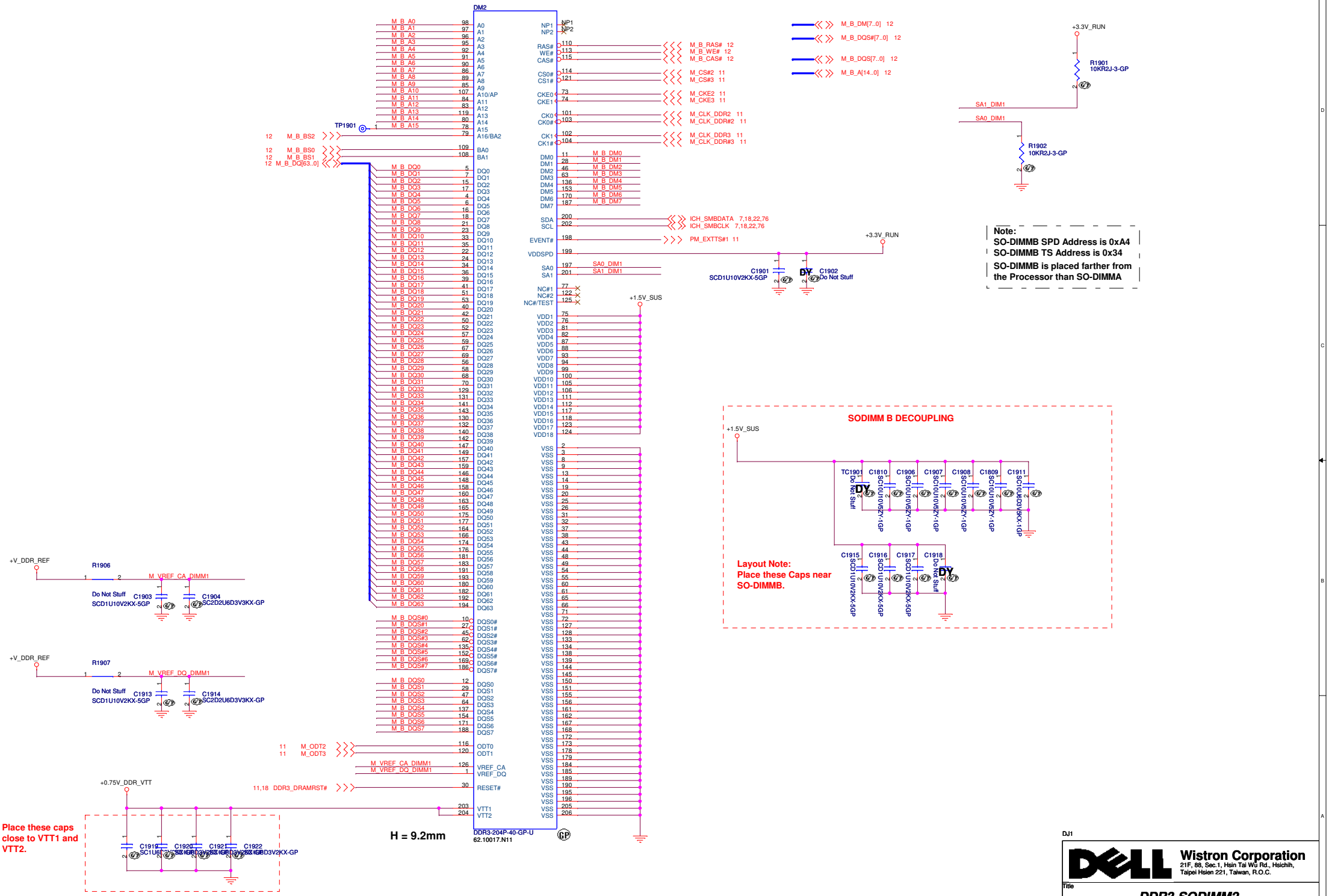
Title
DDR3-SODIMM1
Size
Document Number
DJ1 Montevina UMA
Rev
A00
Date: Friday, February 26, 2010
Sheet 18 of 88



DJ1

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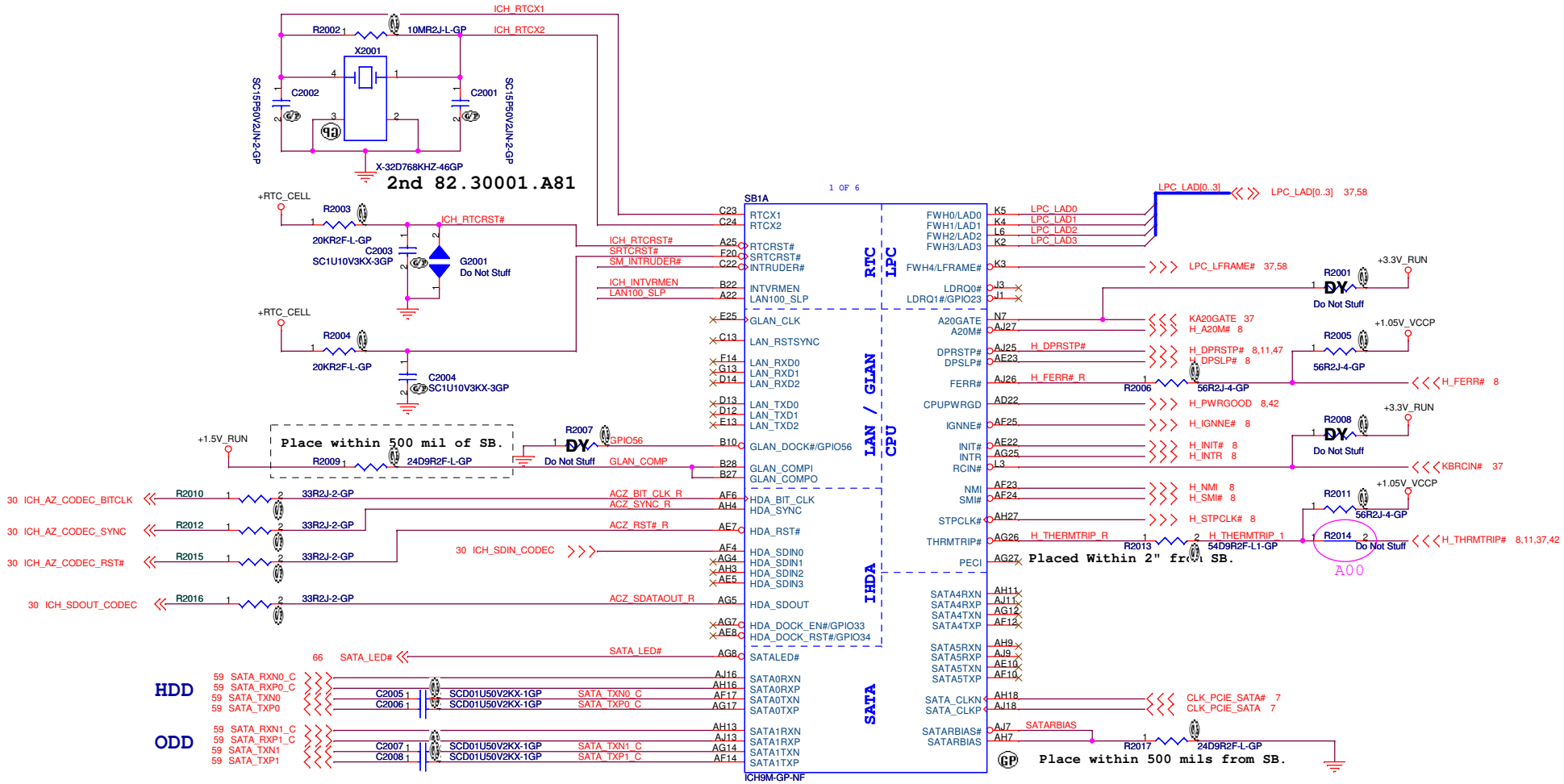
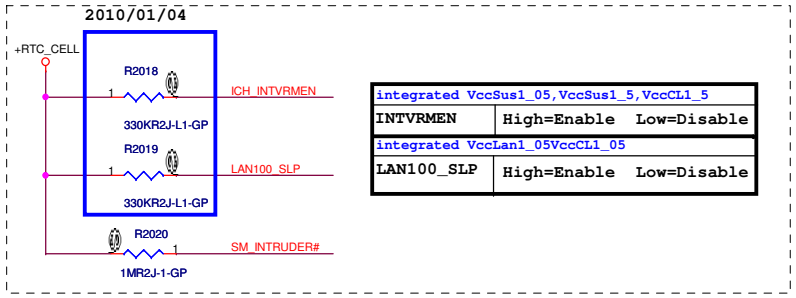
Title: DDR3-SODIMM2

Size | Document Number: DJ1 Montevina UMA | Rev: A00

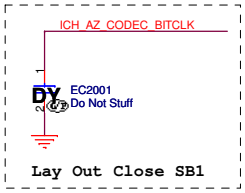
Date: Friday, February 26, 2010 | Sheet 19 of 88

SSID = ICH





integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



DJ1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-LAN/HDA/SATA/LPC(1/4)

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Date: Friday, February 26, 2010 | Sheet 20 of 88

SSID = ICH

SB1E — 5 OF 6

SB1B — 2 OF 6 — PCI

SB1D — 4 OF 6

RP2101 — SRN10KJ-L3-GP

RN2106 — SRN8K2J-4-GP

RN2102 — SRN8K2J-4-GP

RN2101 — SRN8K2J-4-GP

RN2103 — SRN8K2J-4-GP

RN2104 — SRN8K2J-4-GP

RN2105 — SRN8K2J-4-GP

ICH9M-GP-NF

Layout Note:
Place as close as possible
to the ICH Pin

NCTF PIN

WLAN

LAN

USB0

USB2

USB3

WLAN

Card Reader

CAMERA

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

USB Pair	Device
0	USB0 (I/O Board)
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

DJ1

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Title: ICH9-PCI/PCIE/DMI/USB/GND(2/4)

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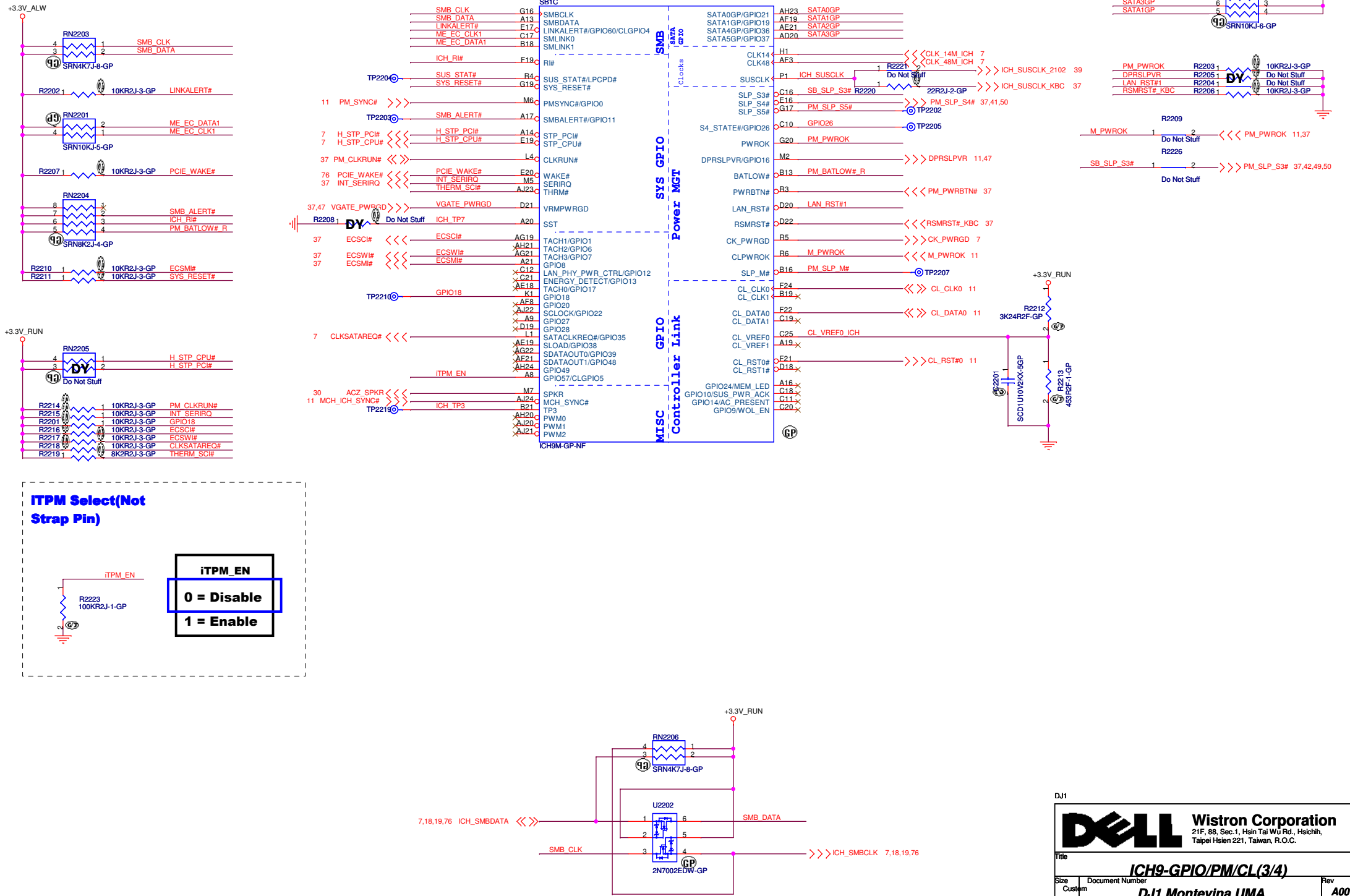
Date: Friday, February 26, 2010 | Sheet 21 of 88

SSID = ICH



DJ1

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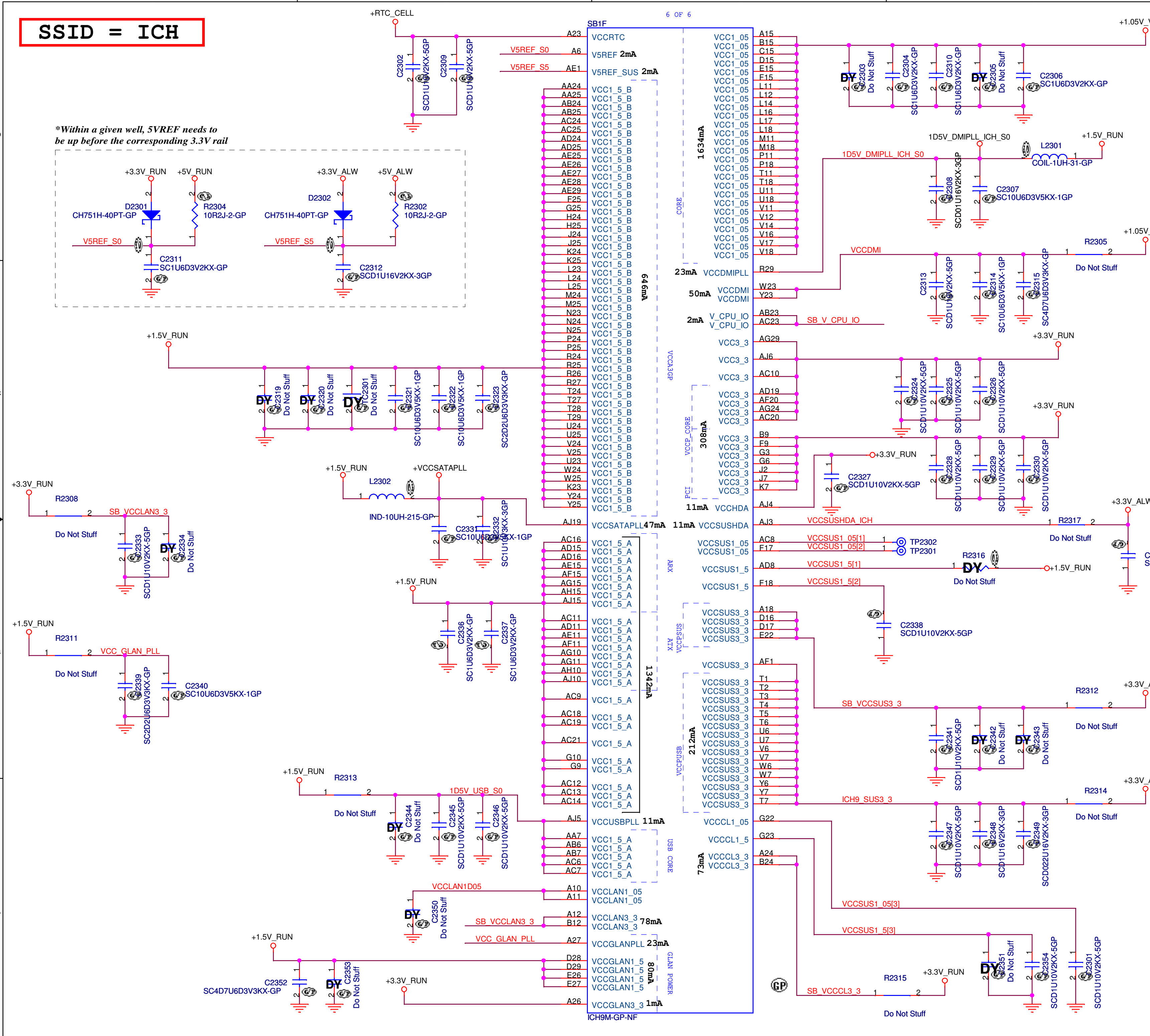
Title: ICH9-GPIO/PM/CL(3/4)

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 22 of 88



DJ1

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Title: ICH9-Power(4/4)

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 — Sheet 23 of 88

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Title: *Reserved*

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Date: Wednesday, February 24, 2010 | Sheet 24 of 88

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DJ1

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Size	Document Number	Rev
Custom	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 25 of 88

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DJ1

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Title: *Reserved*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Wednesday, February 24, 2010 | Sheet 26 of 88

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Wednesday, February 24, 2010 | Sheet 27 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: Custom | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Wednesday, February 24, 2010 | Sheet 28 of 88

(Blanking)

DJ1

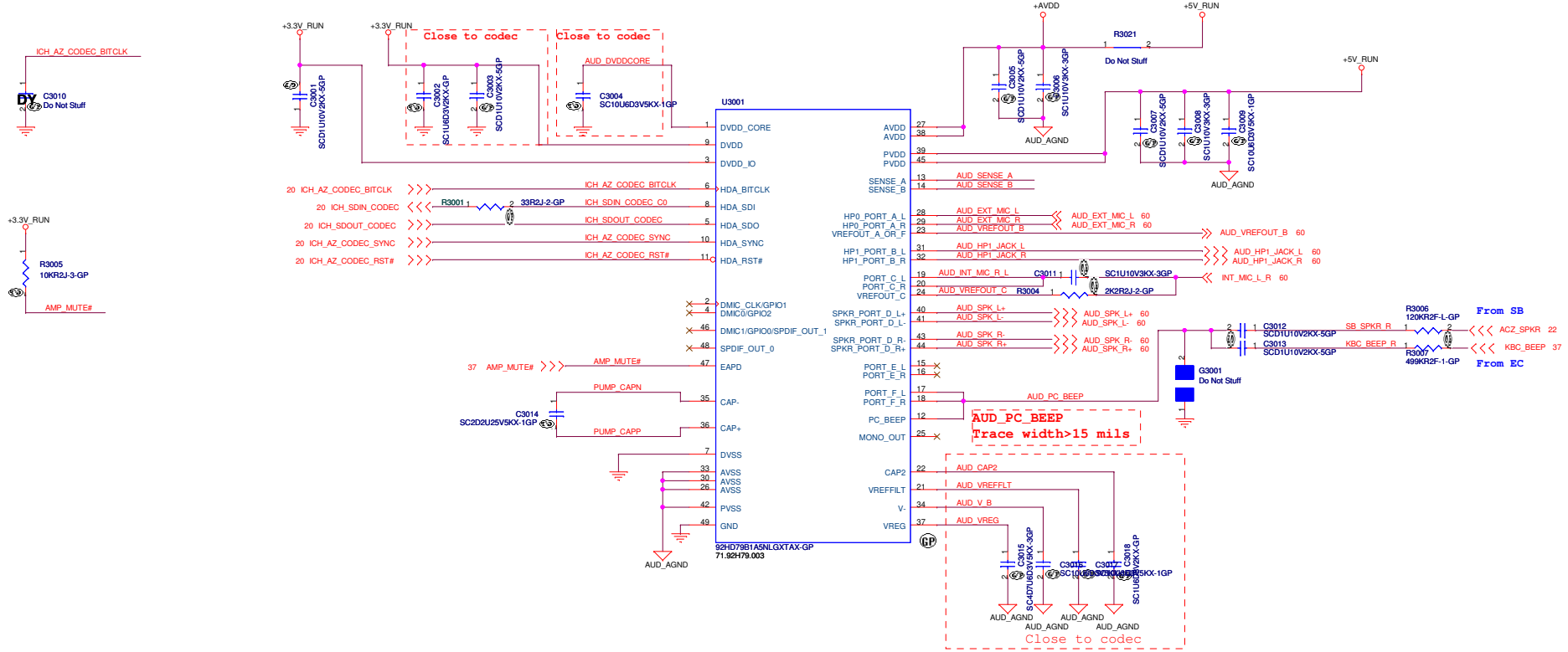
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

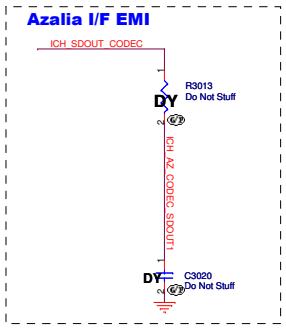
Title: *Reserved*

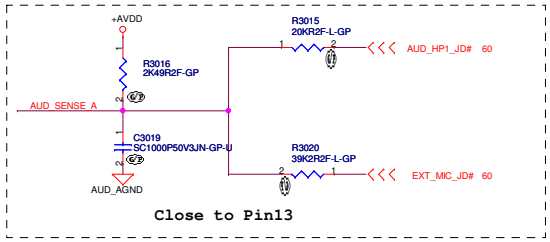
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

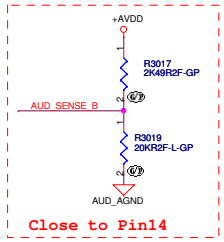
Date: Wednesday, February 24, 2010 Sheet 29 of 88

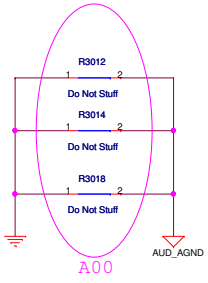
SSID = AUDIO











DJ1

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Audio Codec 92HD79B1
Size: Custom	Document Number: DJ1 Montevina UMA
Rev: A00	
Date: Friday, February 26, 2010	Sheet 30 of 88

(Blanking)

DJ1

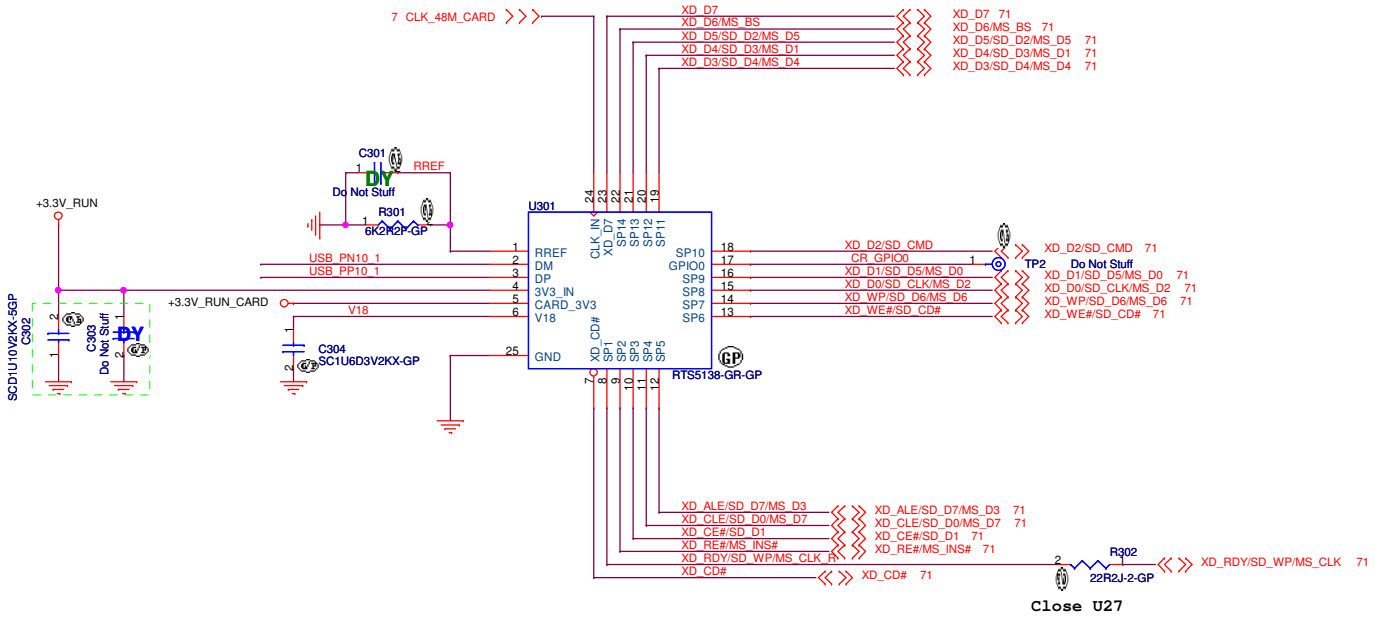
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

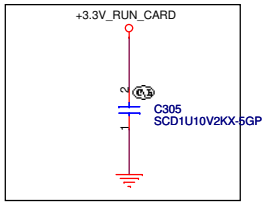
Date: Wednesday, February 24, 2010 Sheet 31 of 88

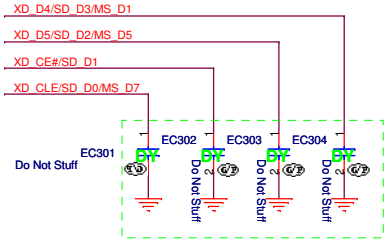
SSID = SDIO

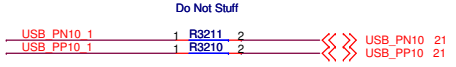


Close U27

Close to U301







2010/01/05

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 32 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 33 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 34 of 88

(Blanking)

DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
	DJ1 Montevina UMA	*A00*

Date: Wednesday, February 24, 2010 Sheet 35 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 36 of 88

SSID = KBC

CAP close to VCC-GND pin pair

U3701A — NPCE781BA0DX-GP (1 OF 2)

A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR

PH for DJ1
PL for DJ2/DJ3

A00
For RCID Function

Layout note:
1. Connect KBC_AGND and GND at one point
2. R3725 close to Pin 103 (AGND)

MB VERSION ID

	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
A00	0	1	0
A01	0	1	1

KBC CLK
EMI

U3701B — NPCE781BA0DX-GP (2 OF 2)

KBC
PS/2
FIU

U3702 — 2N7002EDW-GP

Q3702 — 2N7002EDW-GP

Q3703 — PMBS3904-1-GP

Q3704 — SI2301CDS-T1-GE3-GP

Q3705 — 2N7002E-1-GP

Q3706

Q3701 — PMBS3906-GP

D3702 — BAS16-6-GP

D3703 — BAS16-6-GP

D3704 — BAT54C-U-GP

D3705 — BAT54C-U-GP

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX
Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Friday, February 26, 2010 | Sheet 37 of 88

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DJ1

Wistron Corporation
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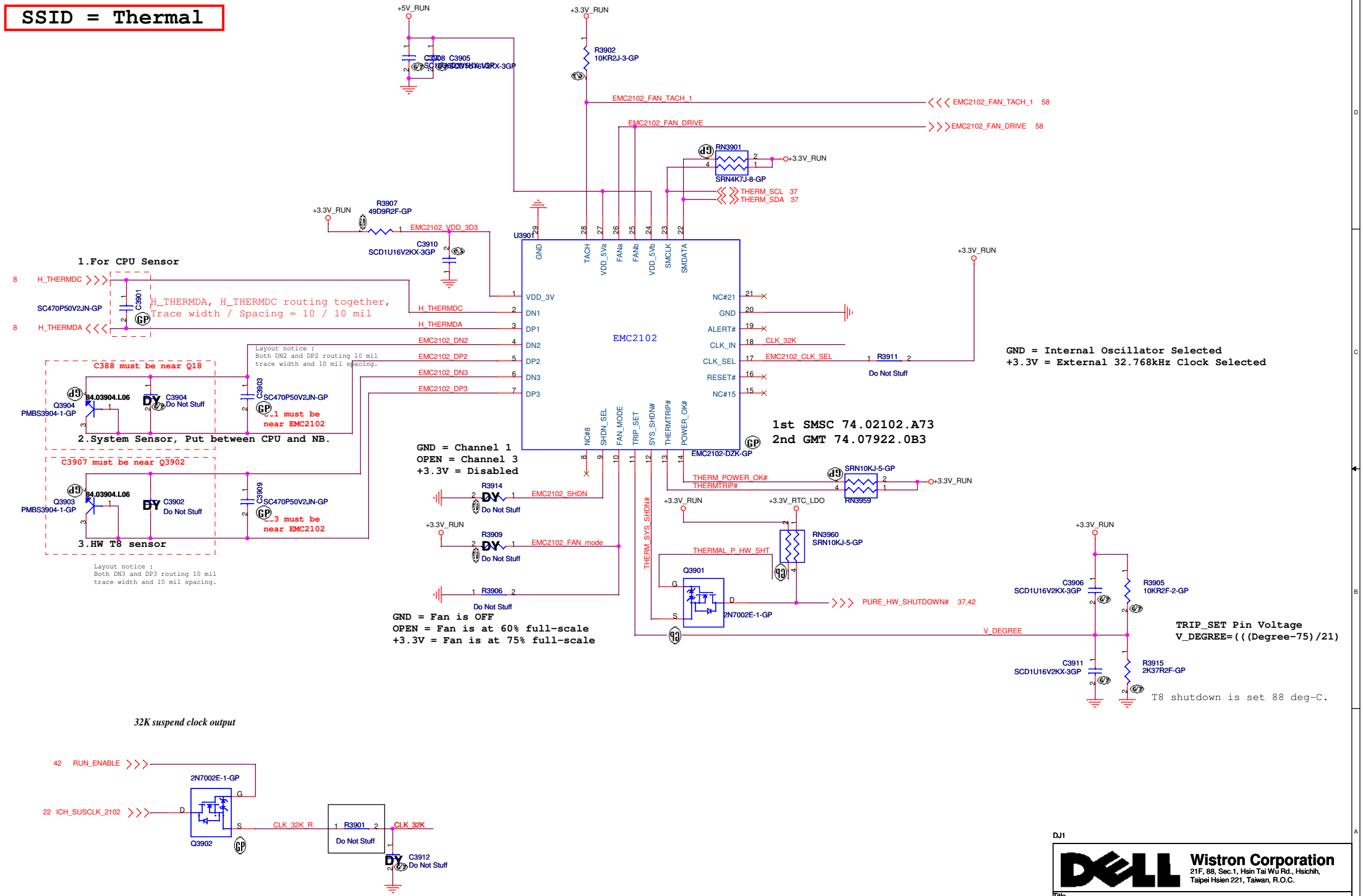
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 38 of 88

SSID = Thermal



32K suspend clock output

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 39 of 88

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DJ1

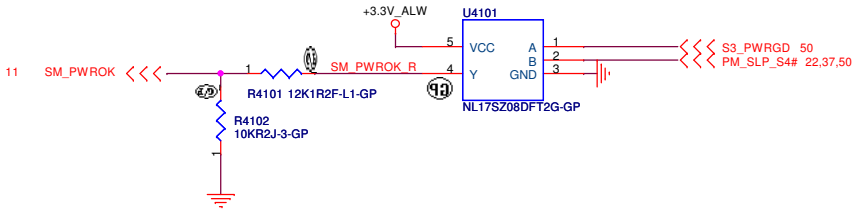
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 40 of 88

SSID = Reset.Suspend



DJ1

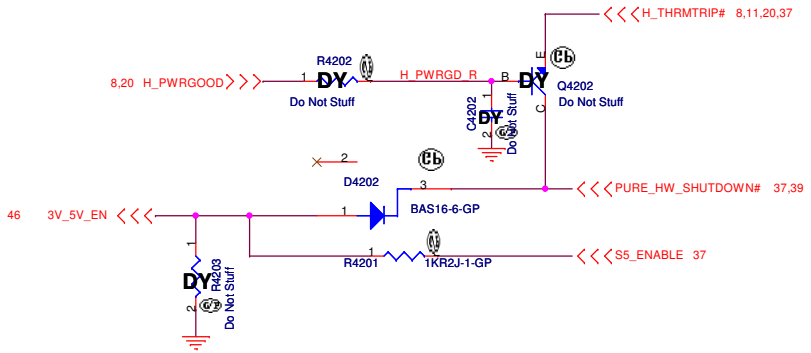
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power On Logic*

Size: A3 | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

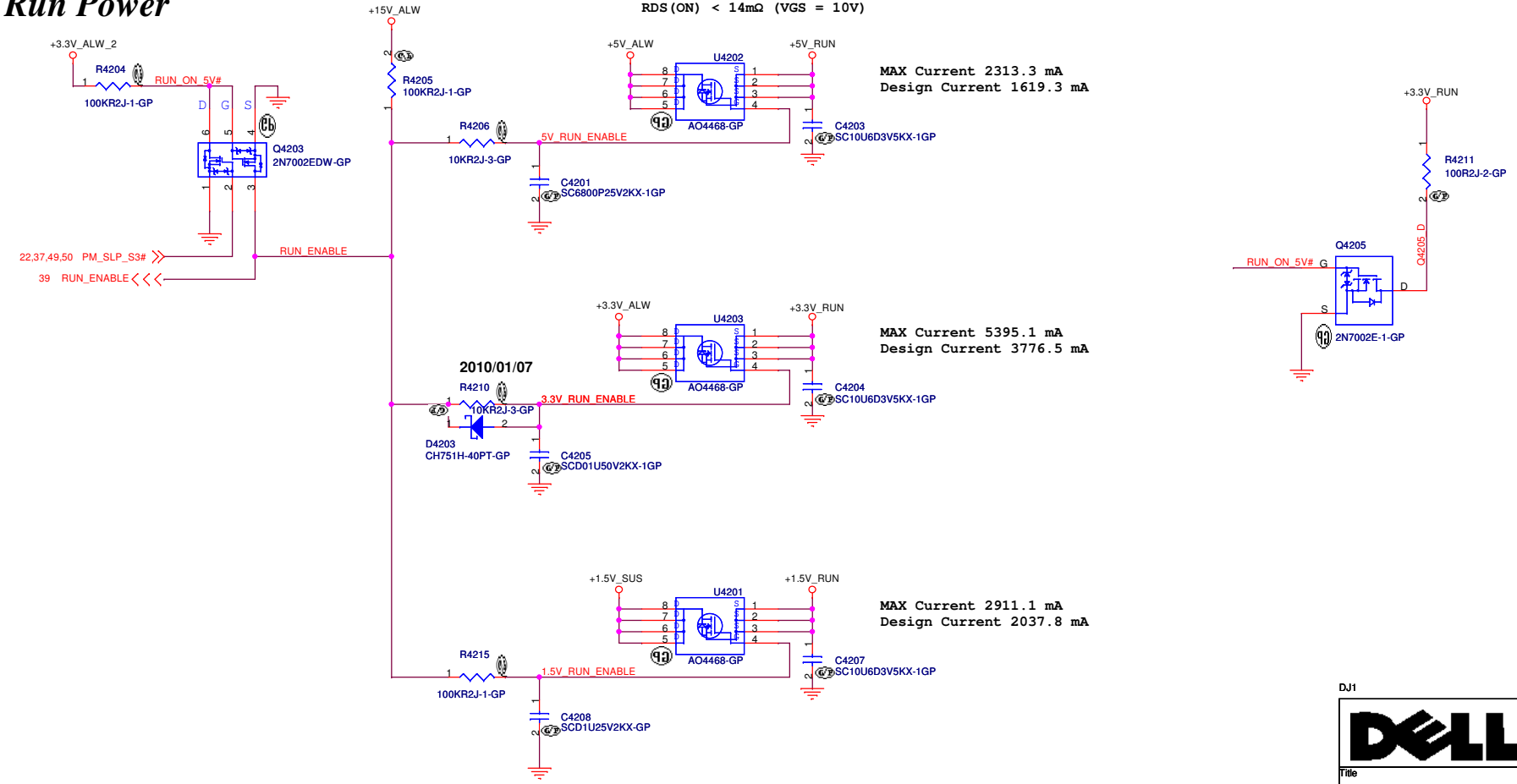
Date: Friday, February 26, 2010 | Sheet 41 of 88

SSID = Reset.Suspend



Run Power

AO4468 MAX 11.6A
RDS(ON) < 14mΩ (VGS = 10V)



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 42 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 43 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 44 of 88

(Blanking)

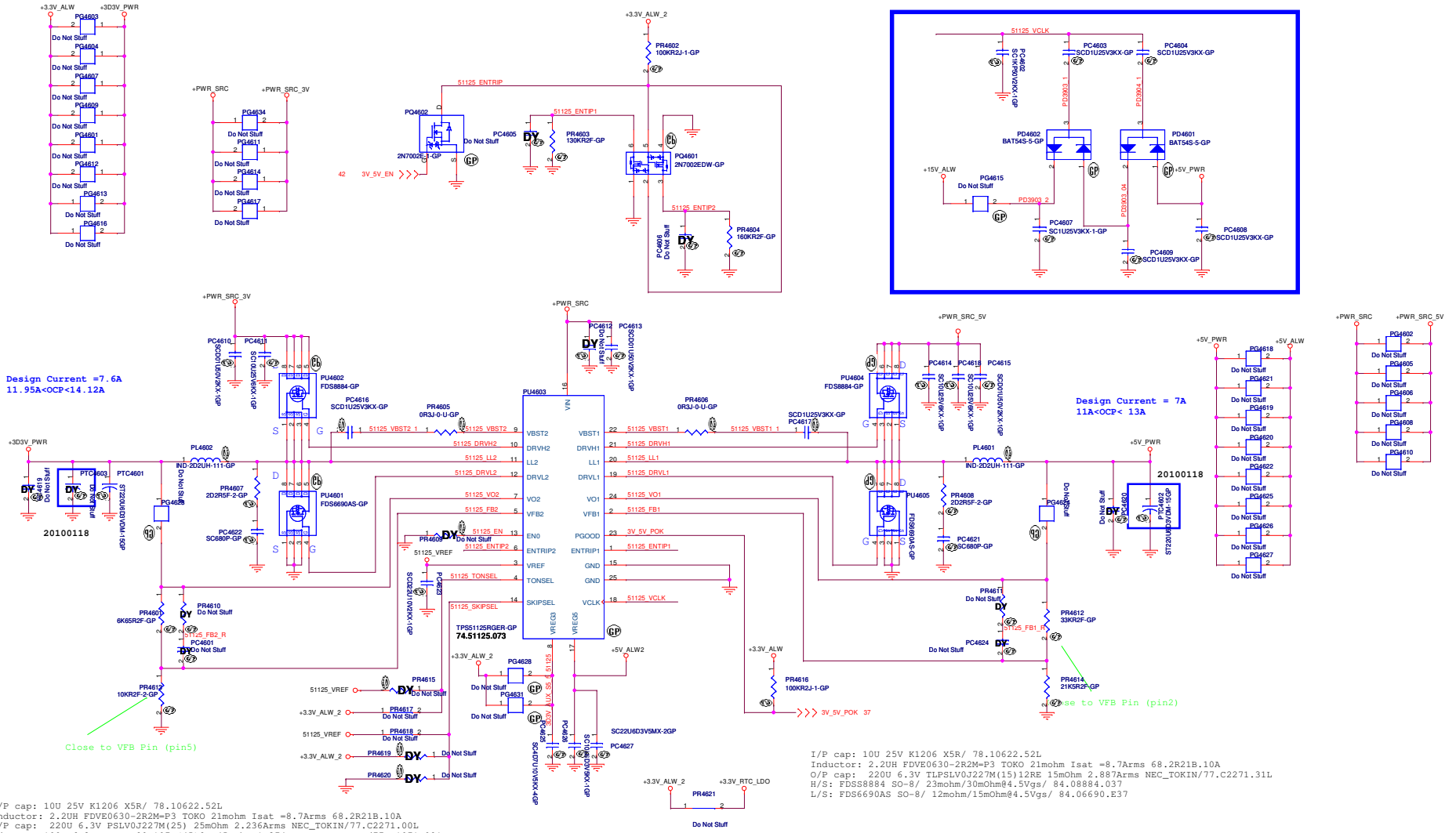
DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 45 of 88



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

DJ1

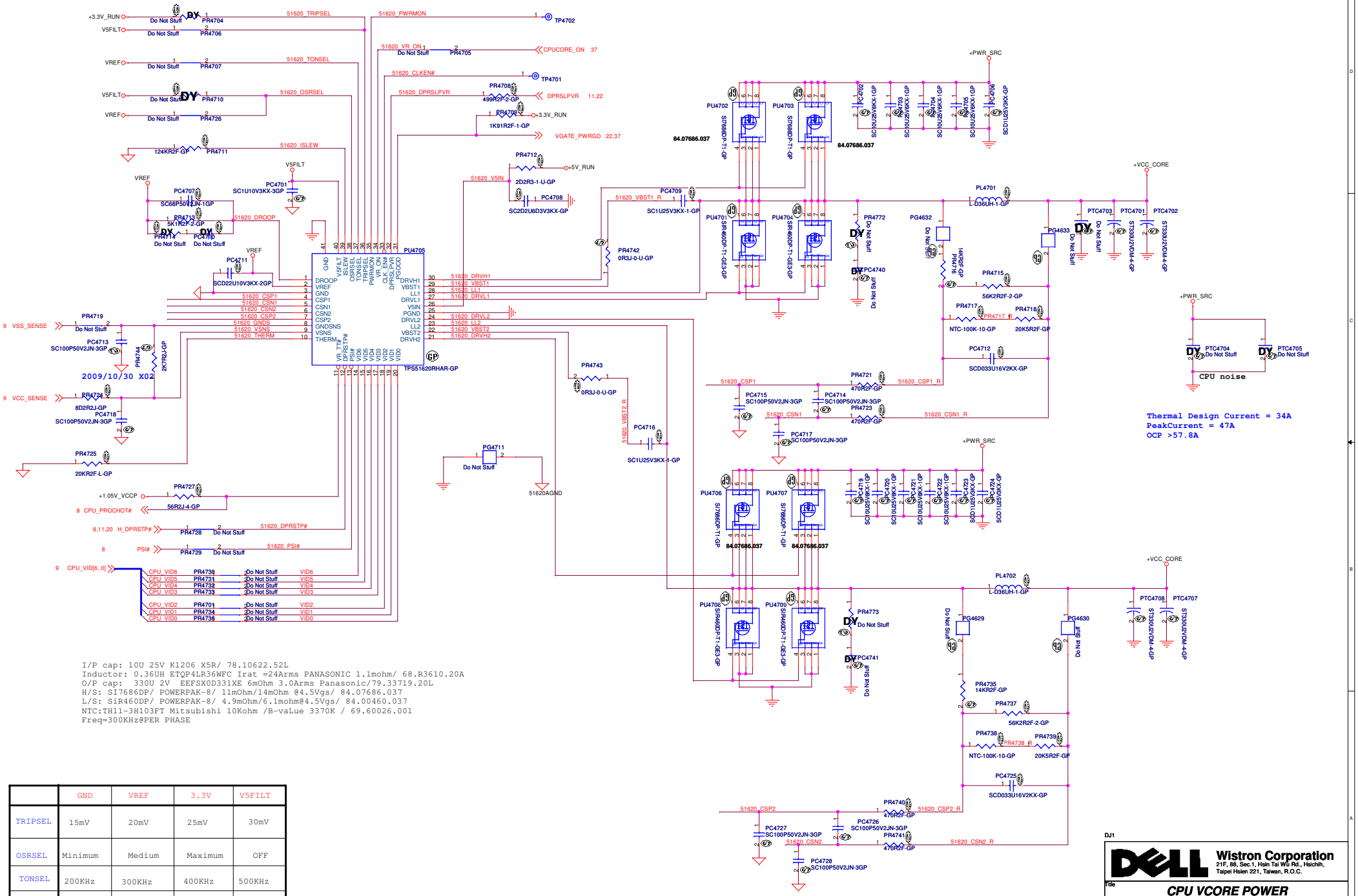
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size	Document Number	Rev
A2	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 46 of 88

SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC Irat =24Arms PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.0Arms Panasonic/79.33719.20L
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm @4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
NTC:TH11-3H103FT Mitsubishi 10Kohm /B-vaLue 3370K / 69.60026.001
Freq=300KHz@PER PHASE

	GND	VREF	3.3V	V5FILT
TRIPSEL	15mV	20mV	25mV	30mV
OSRSEL	Minimum	Medium	Maximum	OFF
TONSEL	200KHz	300KHz	400KHz	500KHz
OVPSEL	ENABLE	DISABLE	N/A	N/A

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU VCORE POWER

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 47 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

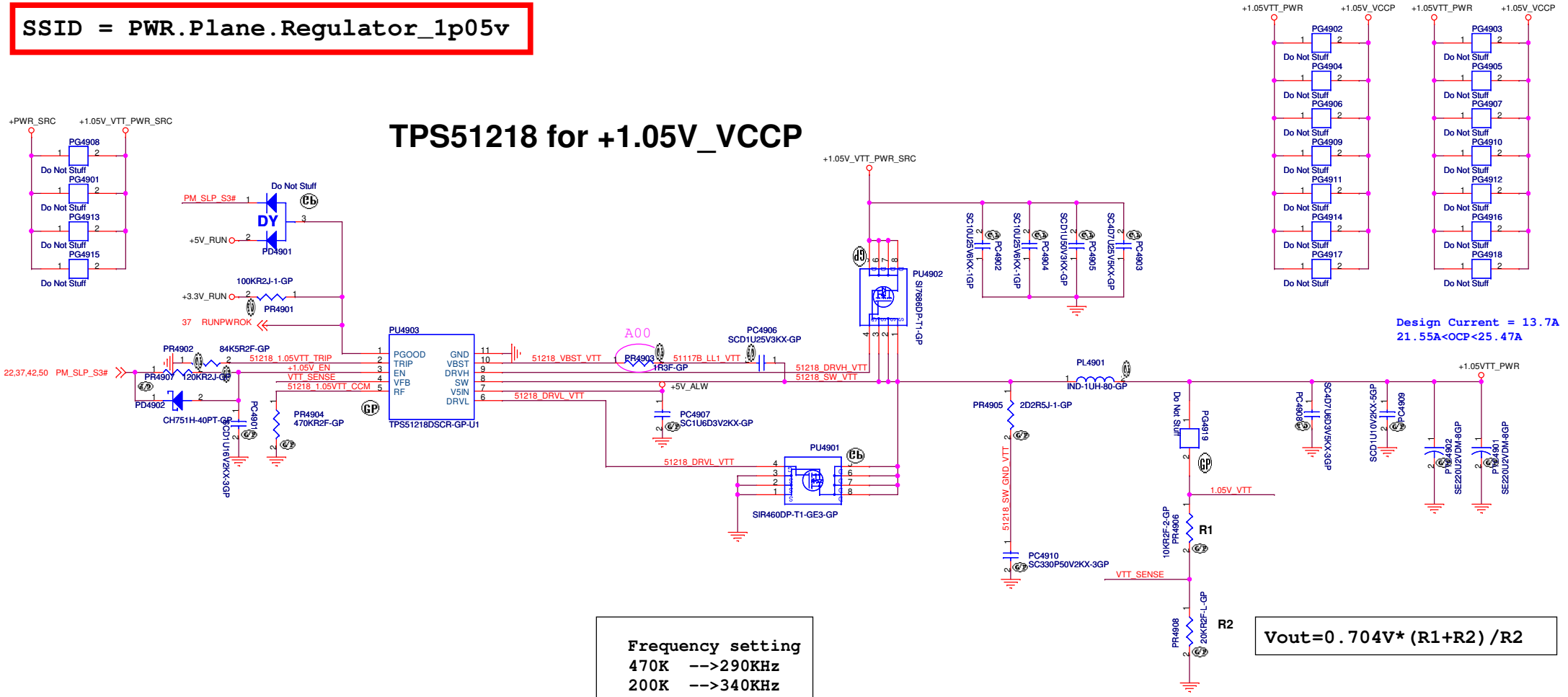
Title: CPU VCORE POWER(2/2)

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 48 of 88

SSID = PWR.Plane.Regulator_1p05v

TPS51218 for +1.05V_VCCP



Design Current = 13.7A
21.55A<OCP<25.47A

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1uH FDUE1040D-1R0M=P3 TOKO DCR:2.35mohm Isat =17.9Arms 68.1R01B.10A
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP-T1-E3/11mohm/ 14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP-T1-GE3-GP/4.5mOhm/6.1mohm@4.5Vgs/ 84.00460.037

DJ1

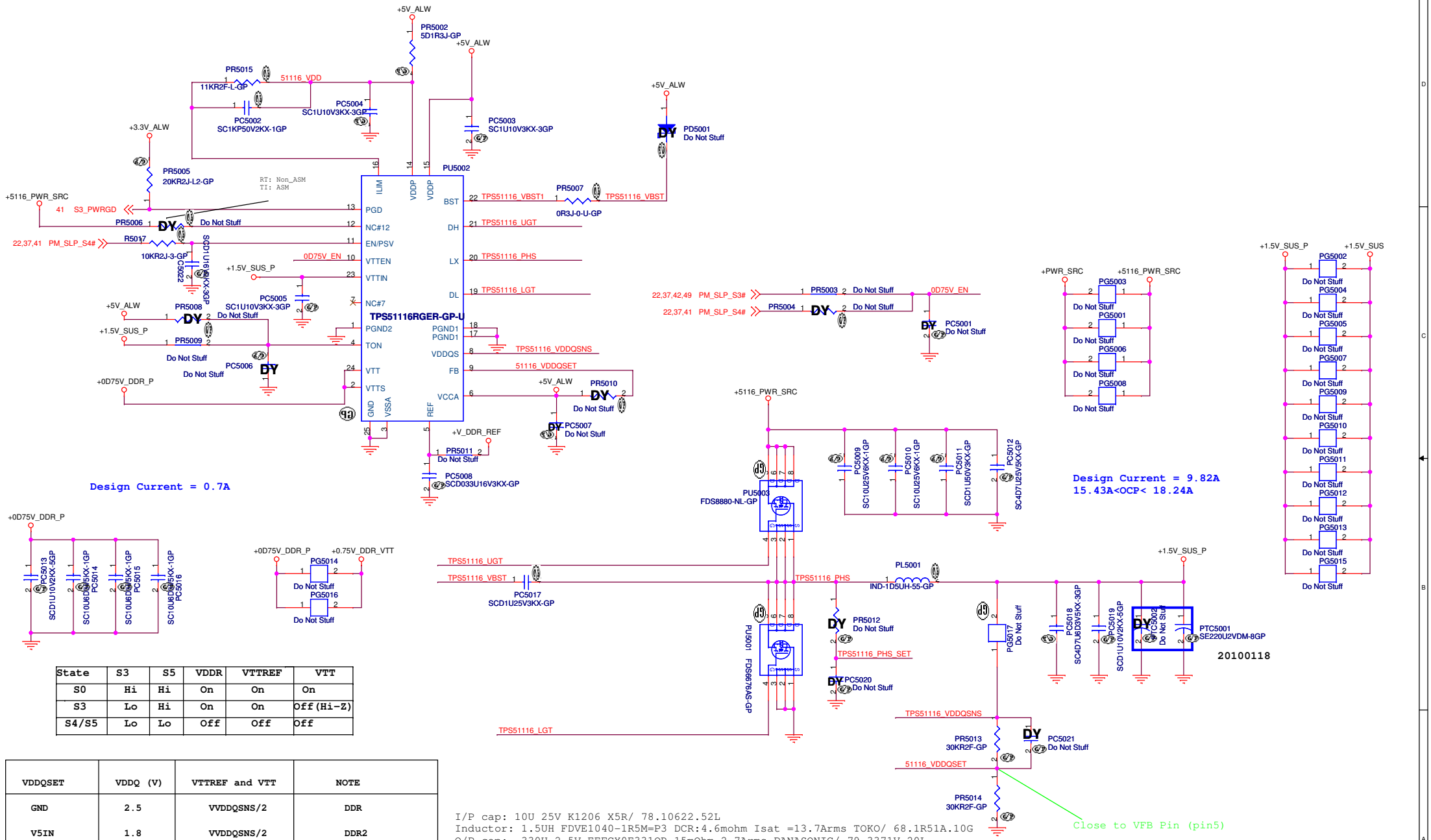
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VCCP

Size	Document Number	Rev
Custom	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 49 of 88

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH FDVE1040-1R5M=P3 DCR:4.6mohm Isat =13.7Arms TOKO/ 68.1R51A.10G
O/P cap: 330U 2.5V EEFCX0E331QR 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS/ 5.9mOhm/7.25mohm@4.5Vgs/ 84.06676.A37
Switching freq-->400KHz

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116 +1.5V SUS

Size: Custom | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 50 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 51 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 52 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

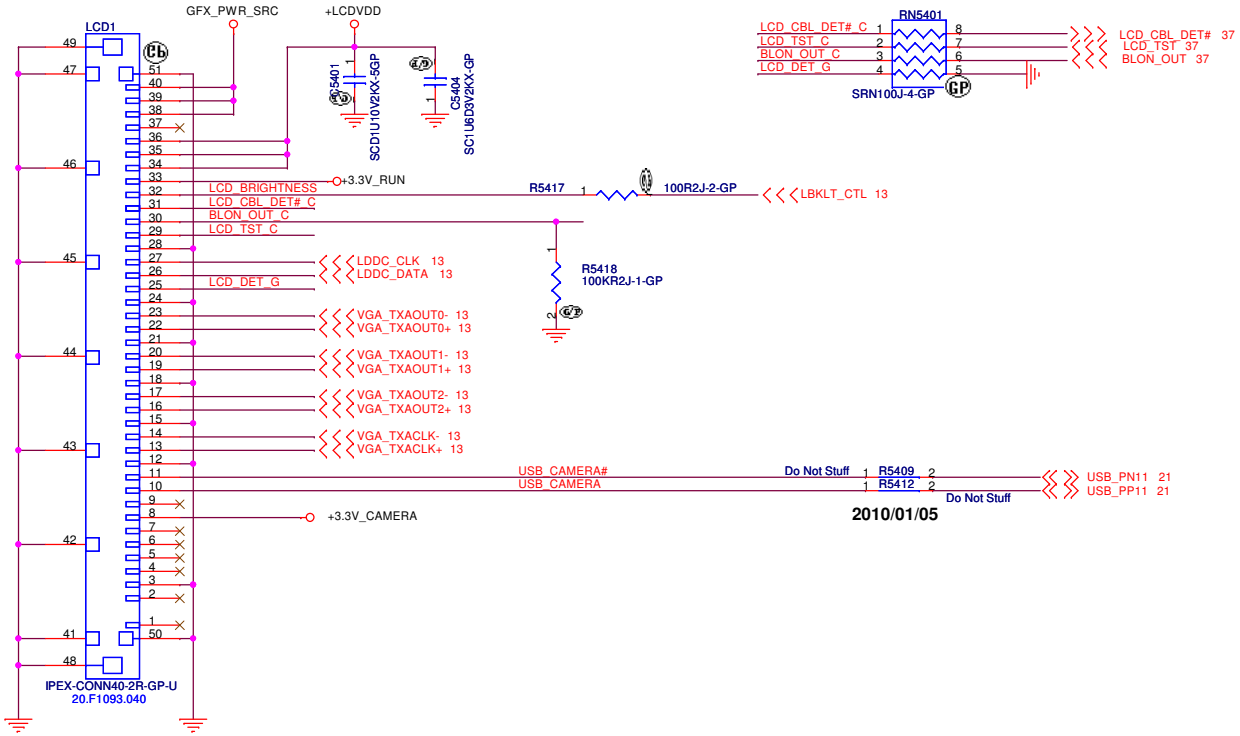
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 53 of 88

SSID = VIDEO

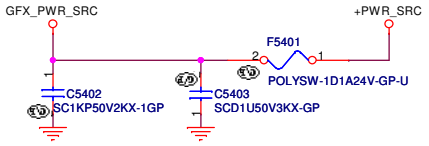
LVDS CONNECTOR



2010/01/05

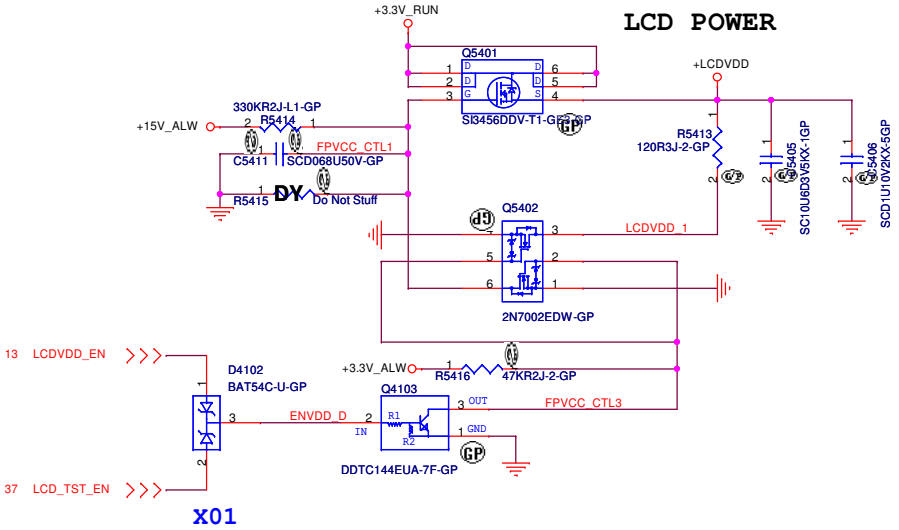
SSID = Inverter

INVERTER POWER



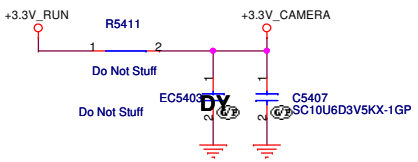
SSID = VIDEO

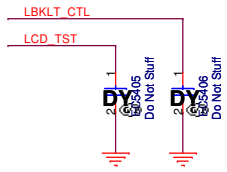
LCD POWER



X01

Camera Power





DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD/Inverter Connector*

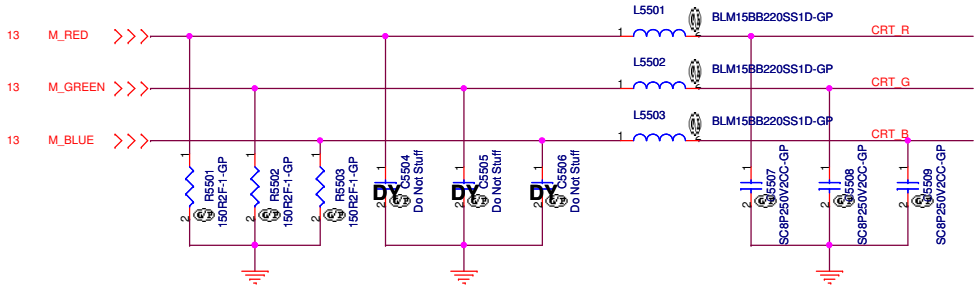
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

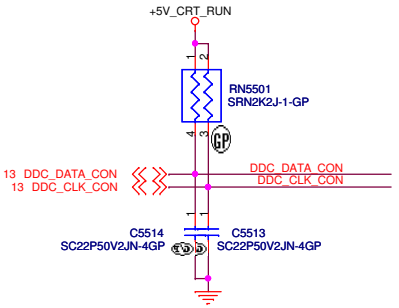
Date: Friday, February 26, 2010 Sheet 54 of 88

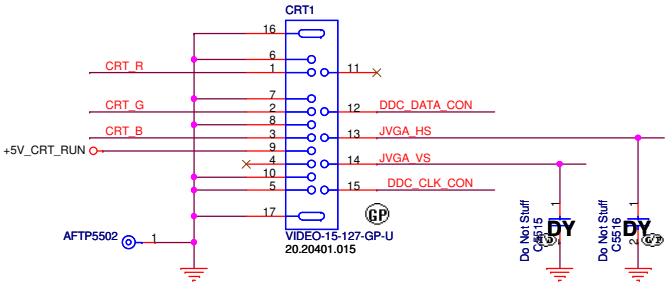
SSID = VIDEO

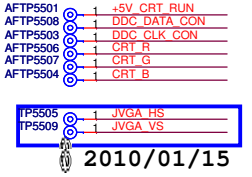
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

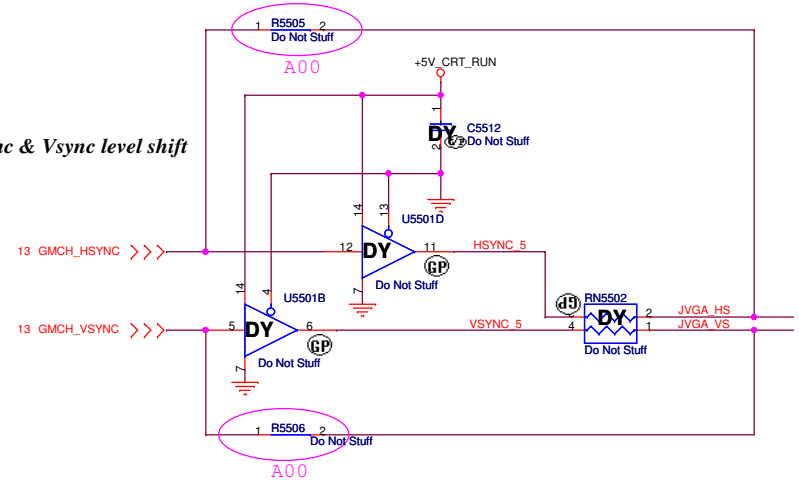


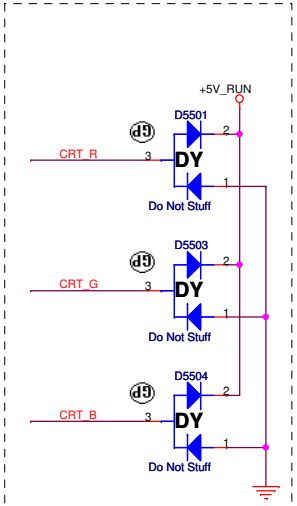


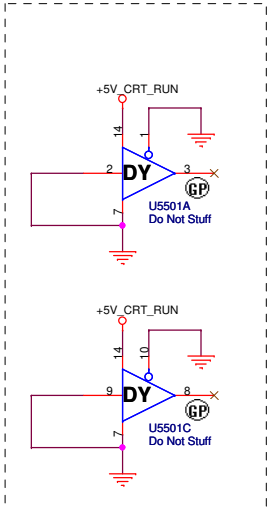


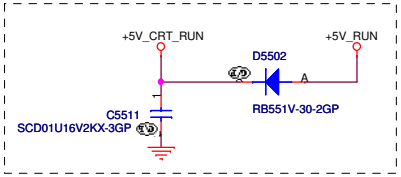


Hsync & Vsync level shift









DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: **DJ1 Montevina UMA** | Rev: **A00**

Date: Friday, February 26, 2010 | Sheet 55 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 10, 2010 Sheet 56 of 88

(Blanking)

DJ1

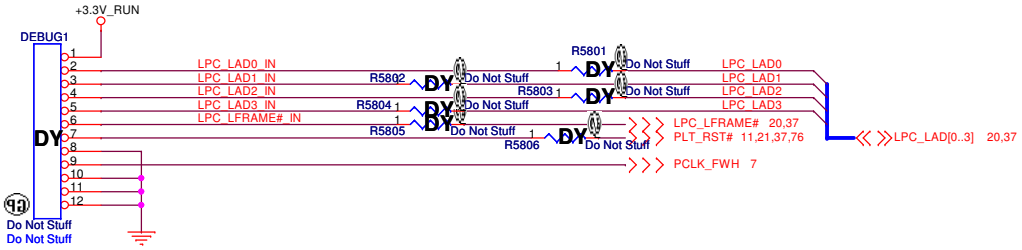
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

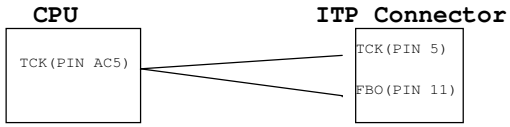
Date: Wednesday, February 24, 2010 Sheet 57 of 88

SSID = User.Interface



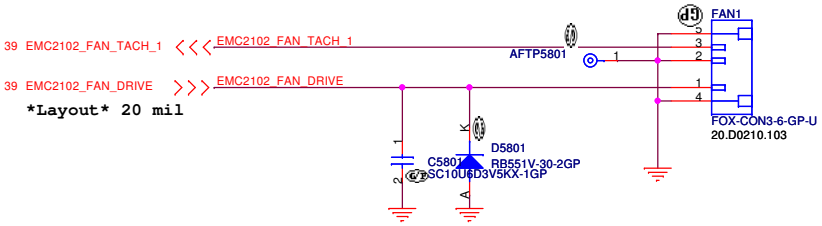
ITP Connector

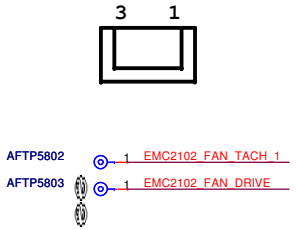
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





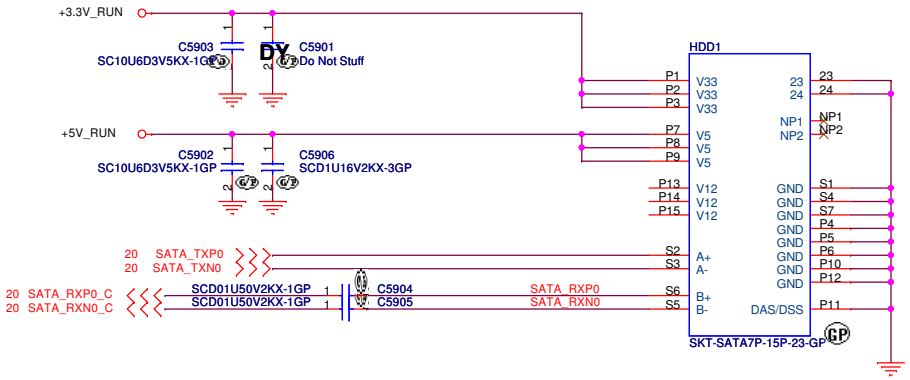
DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

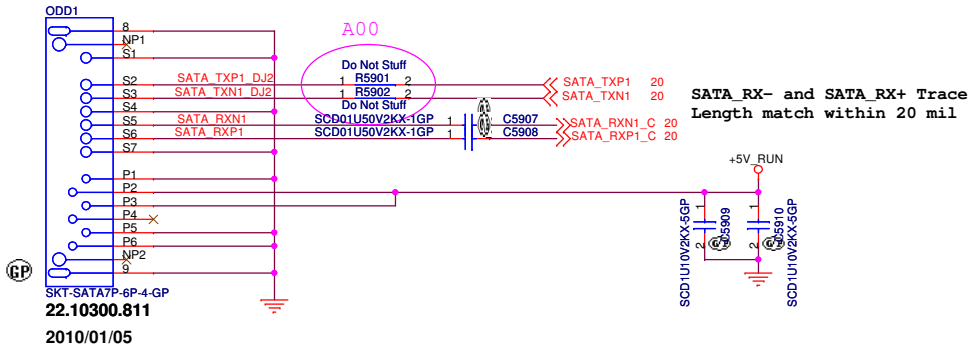
Title		
ITP/Fan Connector		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 58 of 88	

SSID = SATA

SATA HDD Connector



ODD Connector



DJ1

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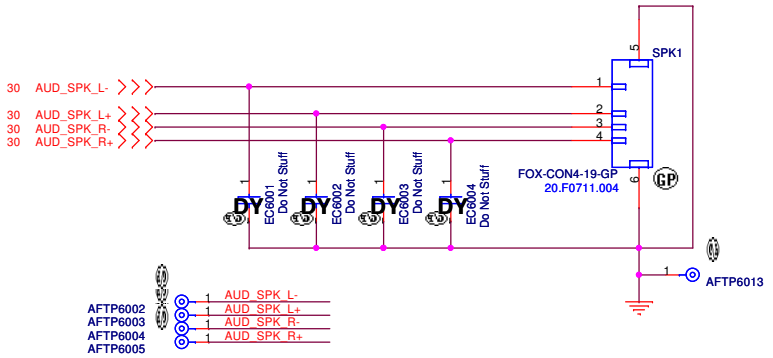
Taipei Hsien 221, Taiwan, R.O.C.

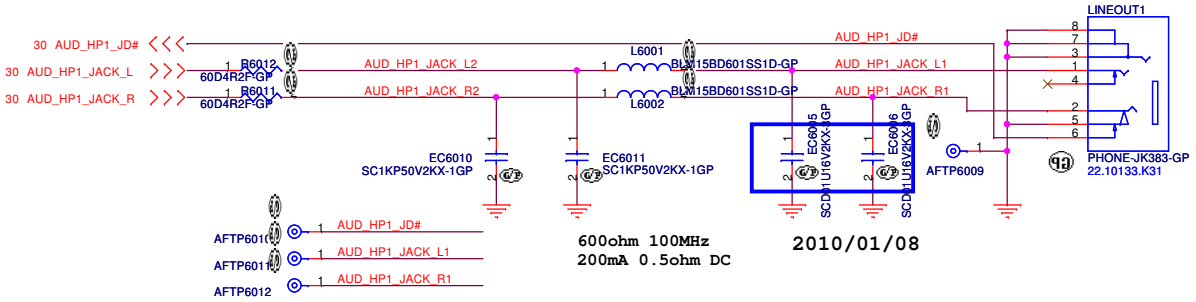
Title		
HDD/ODD		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 59 of 88	

SSID = AUDIO

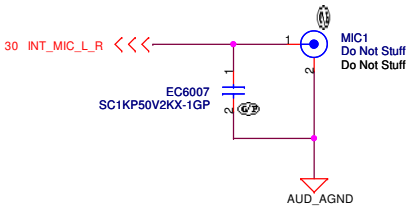
Speaker Connector

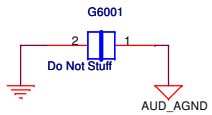


LINE1 OUT

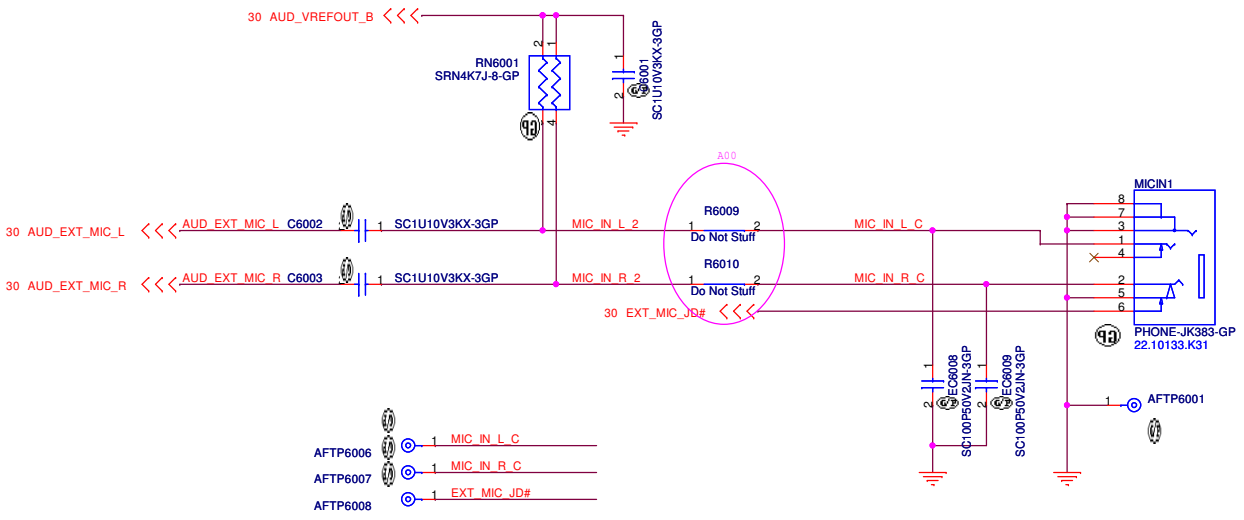


Internal Microphone





MIC IN



DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio Jack/Mic/Speaker	
Size A3	Document Number DJ1 Montevina UMA	Rev A00
Date: Friday, February 26, 2010	Sheet 60 of 88	

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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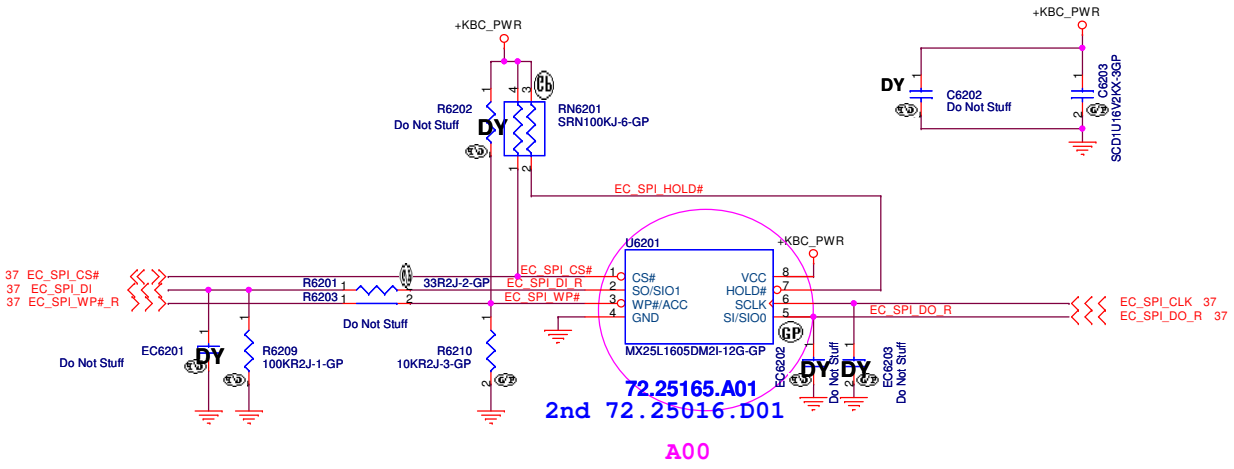
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 61 of 88

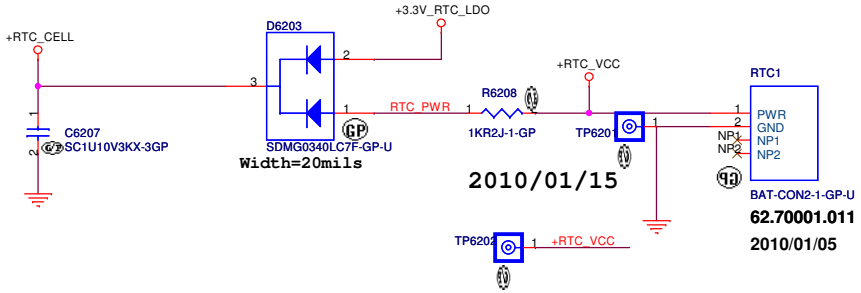
SSID = Flash.ROM

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



DJ1

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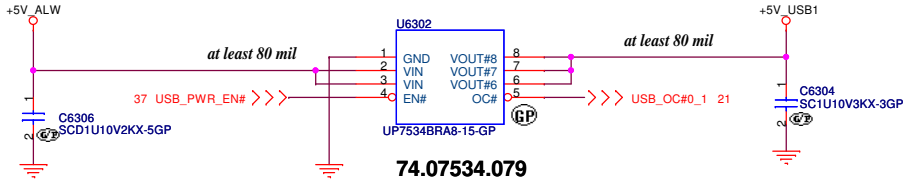
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Flash/RTC		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 62 of 88	

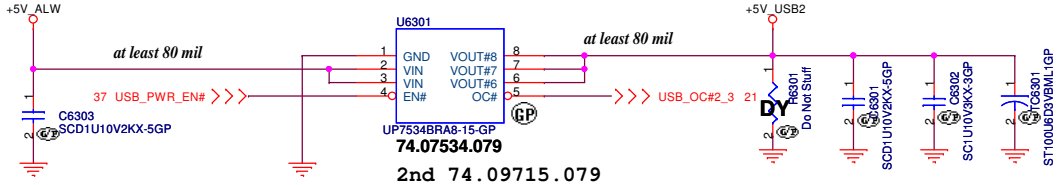
SSID = USB

IO Board USB Power

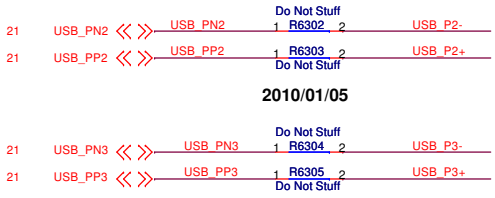


74.07534.079
2nd 74.09715.079
20100111

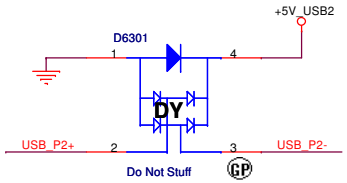
Right USB Power

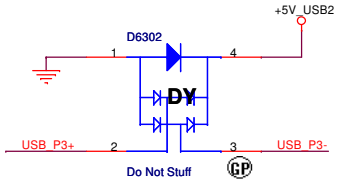


74.07534.079
2nd 74.09715.079
20100111

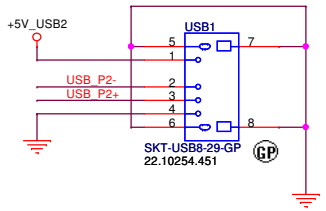


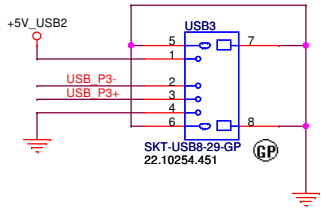
2010/01/05





USB Socket





DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB		
Size	Document Number	Rev
	DJ1 Montevina UMA	A00
Date: Friday, February 26, 2010	Sheet 63 of 88	

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DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 64 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

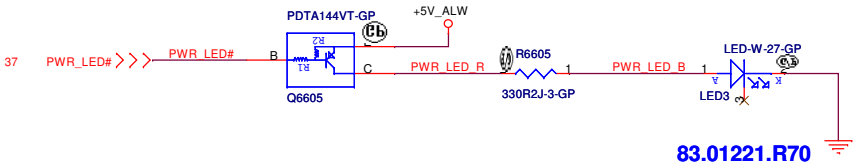
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 65 of 88

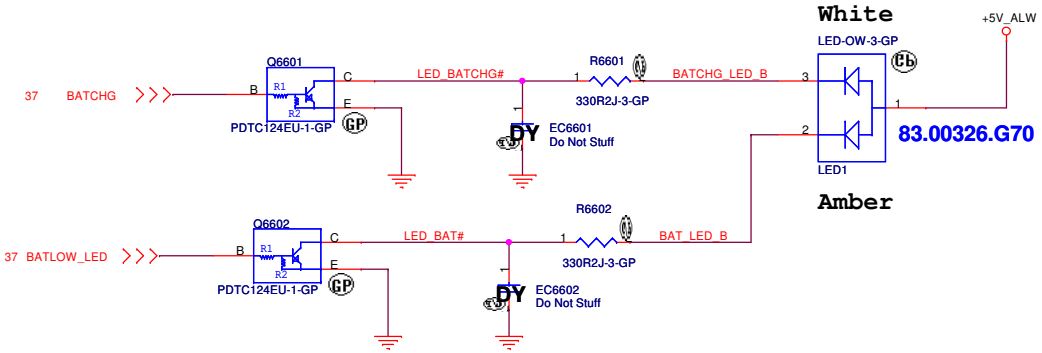
SSID = LED

Power button LED

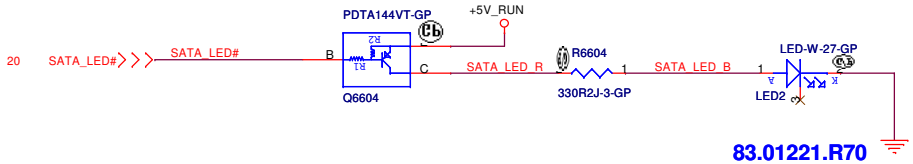
Power LED



Battery LED



HDD LED



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LED		
Size: A3	Document Number: DJ1 Montevina UMA	Rev: A00
Date: Friday, February 26, 2010	Sheet 66 of 88	

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DJ1

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Taipei Hsien 221, Taiwan, R.O.C.

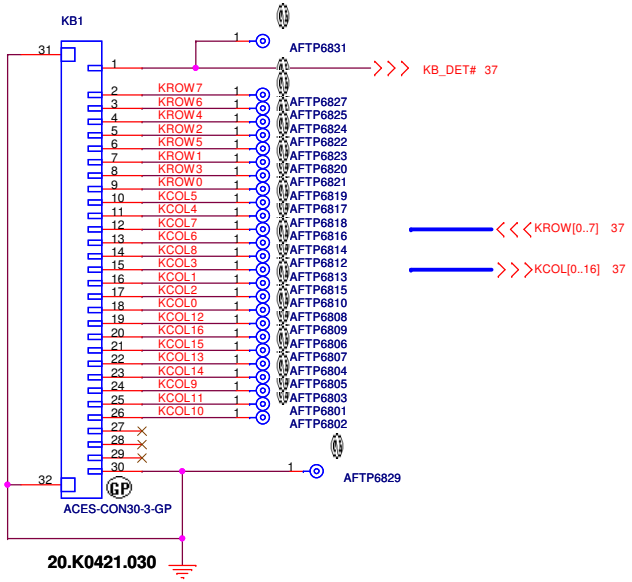
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 67 of 88

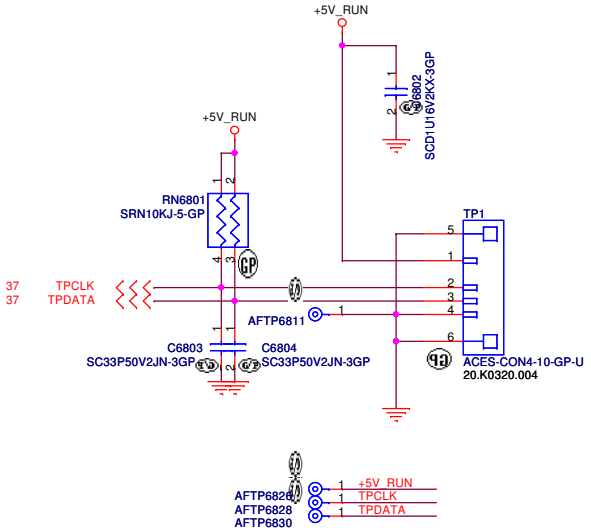
SSID = KBC

Internal KeyBoard Connector



SSID = Touch.Pad

TouchPad Connector



DJ1

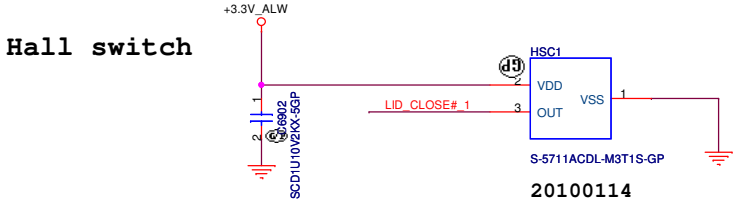
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

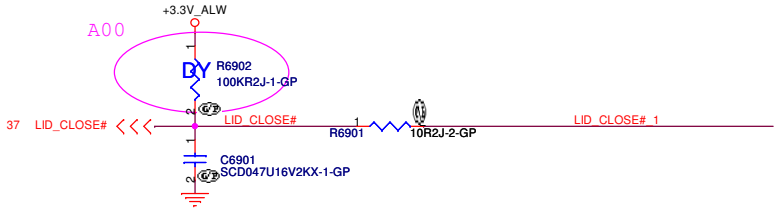
Title: Key Board/Touch Pad

Size: A3 | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 68 of 88

Hall switch





DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall Sensor*		
Size: A3	Document Number: *DJ1 Montevina UMA*	Rev: *A00*
Date: Friday, February 26, 2010	Sheet 69 of 88	

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

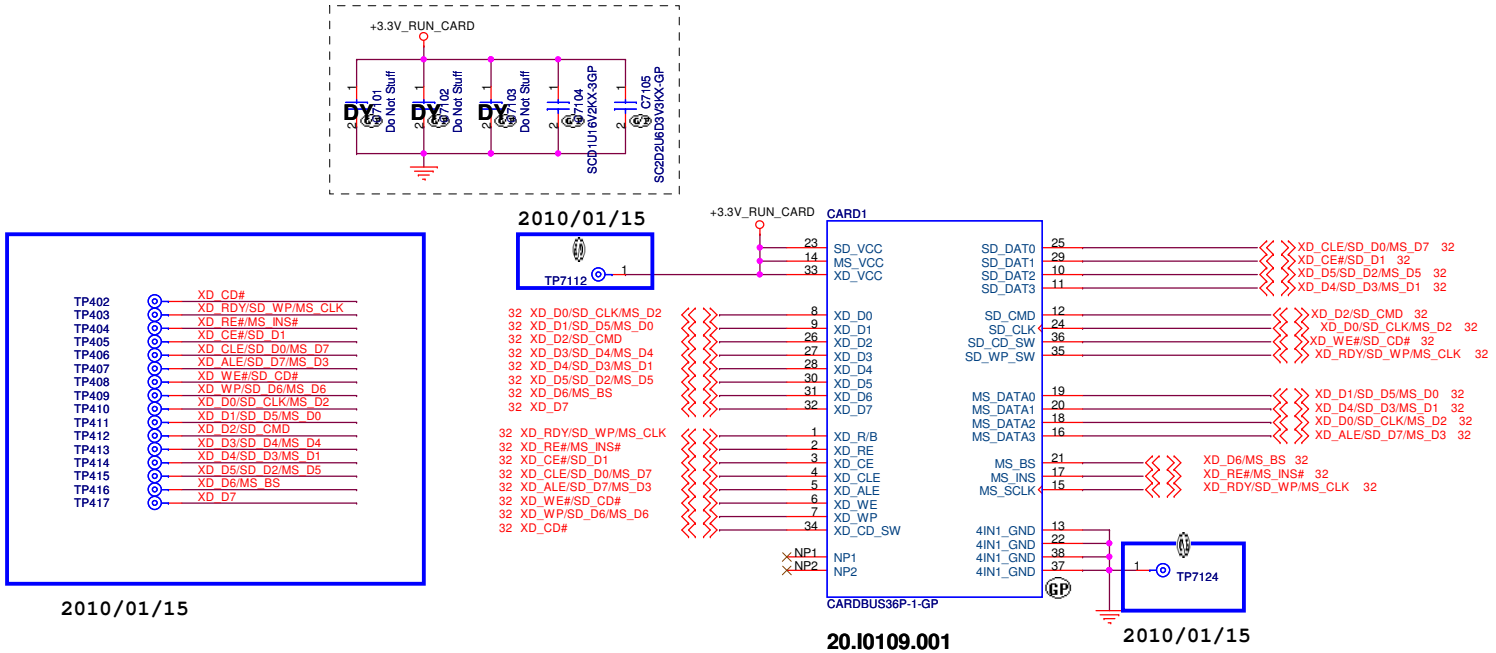
Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 70 of 88

SSID = SDIO

SD/XD/MS Card Reader



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader Connector**

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Friday, February 26, 2010 Sheet 71 of 88

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DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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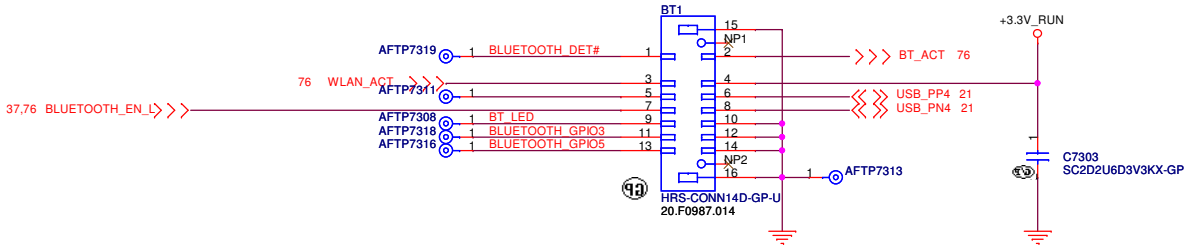
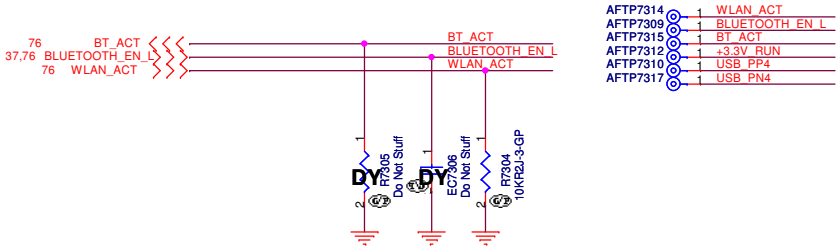
Title: *RESERVED*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 72 of 88

SSID = User.Interface





DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A3	***DJ1 Montevina UMA***	***A00***

Date: Friday, February 26, 2010 Sheet 73 of 88

(Blanking)

DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 74 of 88

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DJ1

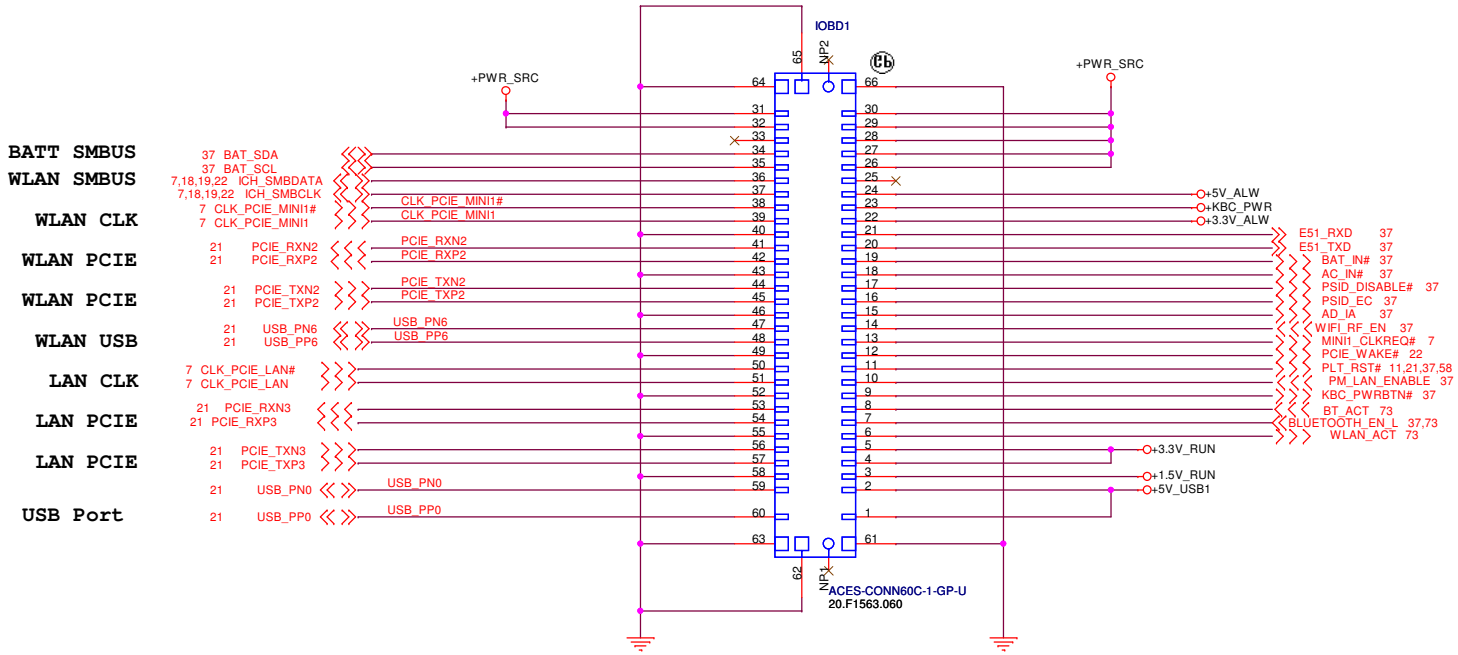
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

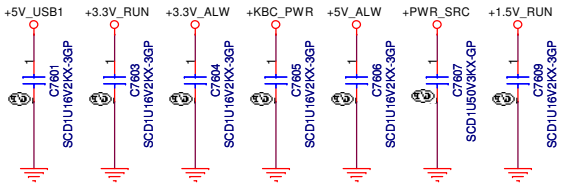
Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 75 of 88

SSID = PWR.Support



Close to IOBD Conn



DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: DJ1 Montevina UMA | Rev: A00

Date: Friday, February 26, 2010 | Sheet 76 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 77 of 88

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DJ1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 78 of 88

SSID = Mechanical

H21 Do Not Stuff
H22 Do Not Stuff
H23 Do Not Stuff
SPR1 SPRING-51-GP 34.4F822.002
HBT1 STF237R115H123-GP 34.4A902.001
HMI2 STF217R128H83-GP 34.4Y702.001
2nd 34.4H103.201

H3 Do Not Stuff
H2 Do Not Stuff
H6 Do Not Stuff
H1 Do Not Stuff
H7 Do Not Stuff
H4 Do Not Stuff
H13 Do Not Stuff
H18 Do Not Stuff
H8 Do Not Stuff
H20 Do Not Stuff

G6002 Do Not Stuff
G6003 Do Not Stuff
G6004 Do Not Stuff

EMI Request

+PWR_SRC SCD1U50V3KX-GP EC7901
+PWR_SRC SCD1U50V3KX-GP EC7902
+PWR_SRC SCD1U50V3KX-GP EC7903
+PWR_SRC SCD1U50V3KX-GP EC7904
+PWR_SRC SCD1U50V3KX-GP EC7905
+PWR_SRC SCD1U50V3KX-GP EC7906

+PWR_SRC SCD1U50V3KX-GP EC7907
+PWR_SRC SCD1U50V3KX-GP EC7908
+PWR_SRC SCD1U50V3KX-GP EC7909
+PWR_SRC SCD1U50V3KX-GP EC7910
+PWR_SRC SCD1U50V3KX-GP EC7911
+PWR_SRC SCD1U50V3KX-GP EC7925
+PWR_SRC SCD1U50V3KX-GP EC7926
+PWR_SRC SCD1U50V3KX-GP EC7922
+PWR_SRC Do Not Stuff DY EC7923
+PWR_SRC Do Not Stuff DY EC7924

+PWR_SRC SCD1U50V3KX-GP EC7912
+PWR_SRC SCD1U50V3KX-GP EC7913
+1.5V_SUS_P Do Not Stuff DY EC7914

+1.05V_VCCP Do Not Stuff DY EC7921
+1.05V_VCCP Do Not Stuff DY EC7915
+1.05V_VCCP Do Not Stuff DY EC7916
+1.05V_VCCP Do Not Stuff DY EC7917

+5V_RUN SCD1U50V3KX-GP EC7927
+5V_RUN SCD1U50V3KX-GP EC7928
+5V_RUN SCD1U50V3KX-GP EC7929

+3.3V_RUN SCD1U50V3KX-GP EC7918
+3.3V_RUN SCD1U50V3KX-GP EC7919
+3.3V_RUN SCD1U50V3KX-GP EC7920

+3.3V_RUN SCD1U50V3KX-GP EC7936
+3.3V_RUN SCD1U50V3KX-GP EC7937
+3.3V_RUN SCD1U50V3KX-GP EC7938

+5V_ALW SCD1U50V3KX-GP EC7930
+5V_ALW SCD1U50V3KX-GP EC7931
+5V_ALW SCD1U50V3KX-GP EC7932
+5V_ALW SCD1U50V3KX-GP EC7933
+5V_ALW Do Not Stuff DY EC7934

2010/01/07

DJ1

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Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: DJ1 Montevina UMA | Rev: A00
Date: Wednesday, February 24, 2010 | Sheet 79 of 88

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Title: *(Reserved)*

Size	Document Number	Rev
A3	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 80 of 88

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
C	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 81 of 88

(Blanking)

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Title: (Reserved)

Size	Document Number	Rev
A2	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 82 of 88

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Size	Document Number	Rev
C	DJ1 Montevina UMA	A00

Date: Wednesday, February 24, 2010 Sheet 83 of 88

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Size	Document Number	Rev
Custom	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 84 of 88

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Size	Document Number	Rev
Custom	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 85 of 88

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Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 86 of 88

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*DJ1 Montevina UMA*	*A00*

Date: Wednesday, February 24, 2010 Sheet 87 of 88

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	20	2010/01/04	Wistron	R2018.R2019 to J accurity	Change R2018 R2019 to 63.33434.1DL	X01
2	54	2010/01/04	Wistron	D4102 Change	D4102 change to 83.00054.Q81	X01
3	37	2010/01/04	Wistron	MB version chang to X01	Change R3722 pop,R3727 dummy.	X01
4	59	2009/01/06	Wistron	ME change ODD&RTC Conn	Change ODD Conn to 22.10300.811 Change RTC Conn to 62.70001.011	X01
5	79	2009/01/07	Wistron	EMI Request	Add EC7927 EC7928 EC7929 EC7936 EC7937 EC7938 EC7930 EC7931 EC7932 EC7933 EC7934 POP EC7913 EC7912 EC7925 EC7922 EC7926 PC4610 PC4615	X01
6	54 32 63	2010/01/07	Wistron	USB layout change	Del TR5401 TR3201 TR6301 TR6302 Change R5409 R5412 R3211 R3210 R6302 R6303 R6304 R6305 to 0ohm	X01
7	42	2010/01/07	Wistron	Change R4210 for POP noise	Change R4210 to 10K 63.10334.1DL	X01
8	60	2010/01/08	IDT	IDT Request change EMI CAP to 0.01u	EC6005 EC6006 change to 0.01u 78.10321.2FL	X01
9	63	2010/01/11	Wistron	USB power switch change	Change U6301 U6302 to 74.07534.079	X01
10	37	2010/01/12	Wistron	Prevent BIOS damage	POP U3702 74.00690.I7B	X01
11	37	2010/01/12	DELL	Add one capacitor for IPCC function	Add C3721 close KBC Pin AD_IA	X01
12	69	2010/01/14	Wistron	SMT issue	Change HSC1 layout symbol to Seiko 74.05711.07B	X01
13	47 49 50	2010/01/16	Wistron	Power team request	change PC4740 PC4741 PC4910 PC5020to 78.33124.2FL	X01
14	46	2010/01/18	Wistron	Power team request	DY PTC4603.change PTC5001 PTC4602	X01
15	37	2010/02/10	Wistron	U3702 reset timing is too long	DY U3702	A00
16	37	2010/02/10	Wistron	Change PCB version from X01 to A00	DY R3722 and R3728, stuff R3727 and R3723	A00
17	20 37 55	2010/02/24	Wistron	Change 0ohm to short pad.	Change R2014 R3725 R3748 R5505 R5506 R3012 R3014 R3018 RN5901 R6009 R6010	A00
18	37	2010/02/24	DELL	Add one FET for RCID function	Reserve Q3706	A00
19	69	2010/02/25	Wistron	Do not stuff R6902	Reserve R6902	A00

DJ1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Change History*

Size: A3 | Document Number: *DJ1 Montevina UMA* | Rev: *A00*

Date: Thursday, February 25, 2010 | Sheet 88 of 88