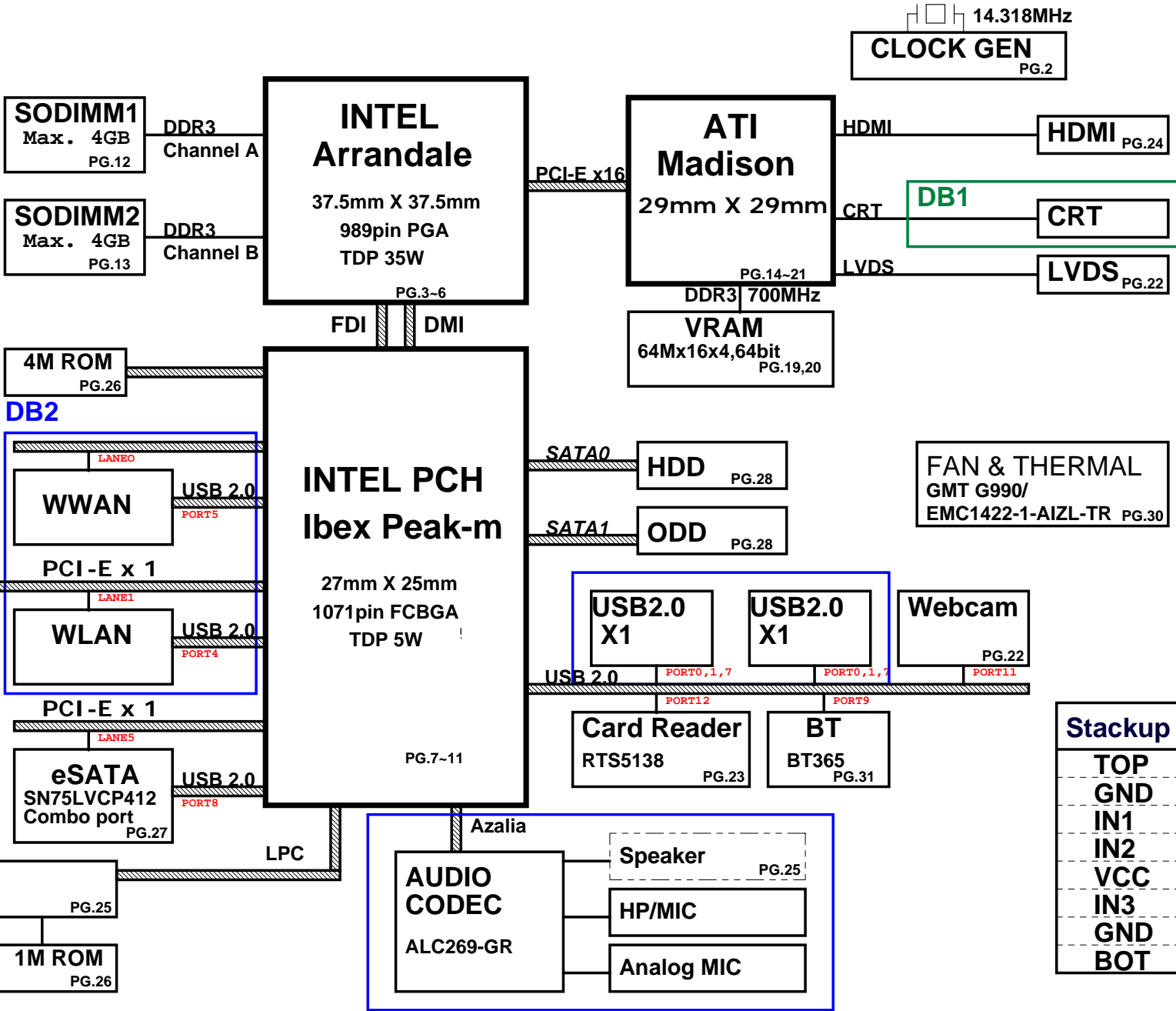


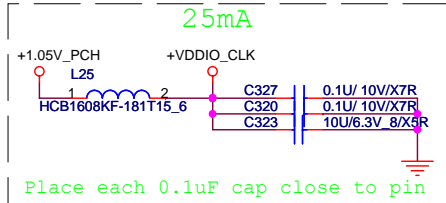
UM8B DIS SYSTEM DIAGRAM

+3V/+5V	PG.34
+1.05V/+1.8V	PG.36
CPU Core	PG.39
VGA Core/+1.1V	PG.38
+1.5V/+0.75V	PG.35
+1.05VTT	PG.37
UMA VGACORE	
Charger	PG.33



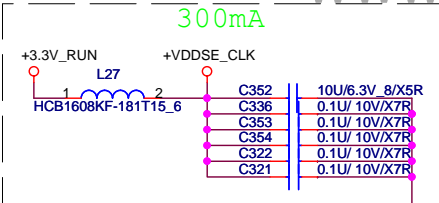
Stackup
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT

PDC (Power Cap quantities follow UM3)



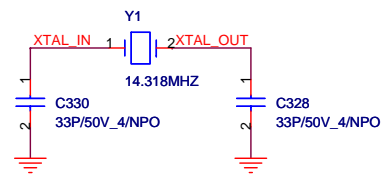
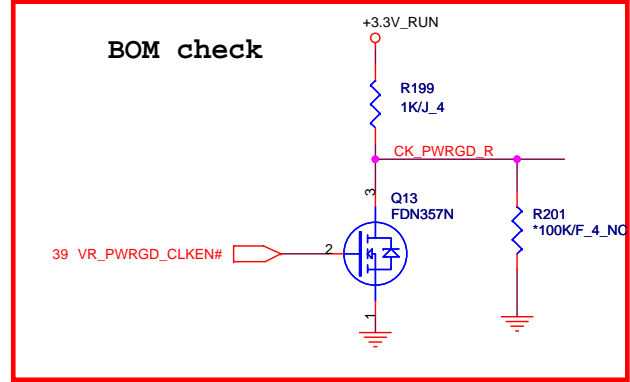
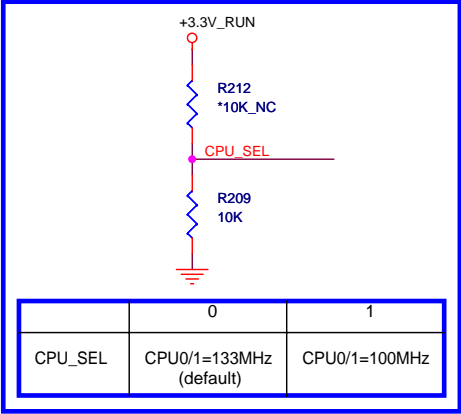
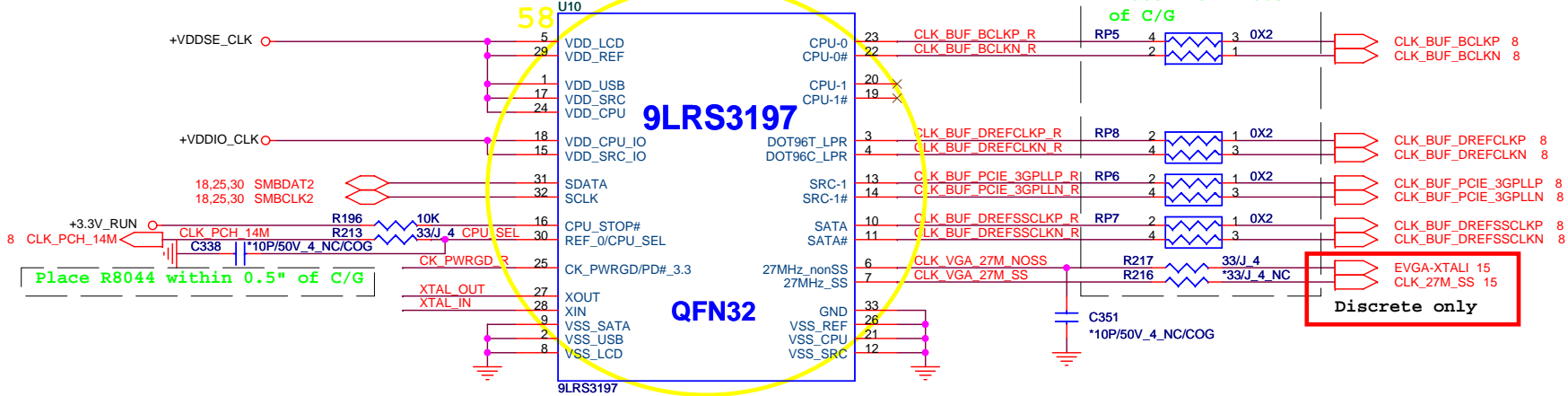
Place each 0.1uF cap close to pin

8/20 Wait Victor check




Place each 0.1uF cap close to pin

Check CLK P/N and footprint



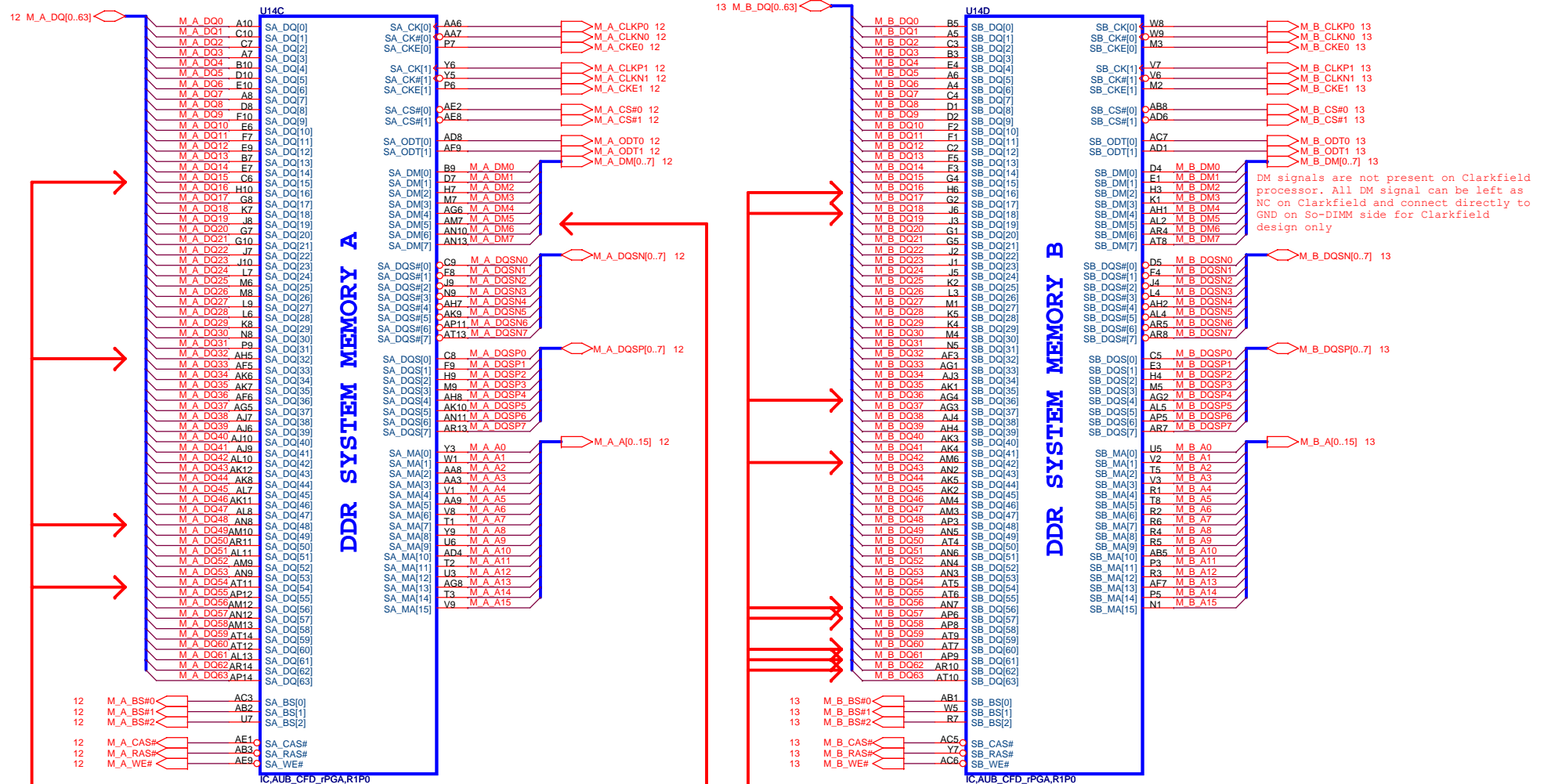
SLG: SLG8SP590VTR Seligo QPN: AL8SP590000
 SLG: SLG8SP585VTR Seligo QPN: AL8SP585000
 RSC: RTM875N-632-VB-GRT Realtek QPN: AL000875002



Quanta Computer Inc.
 PROJECT : UM8B DIS

Size	Document Number	Rev 1A
Clock Gen(9LRS3197)/HOLES		
Date:	Friday, February 05, 2010	Sheet 2 of 46

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
 Requires minimum 12mils spacing
 with all other signals, including data signals.

Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	PROCESSOR 2/4(DDR)	1A
Date:	Friday, February 05, 2010	Sheet 4 of 46

Name different with power

+VCC_CORE

C491	*22U6.3V 8/X5R	AG35	VCC1
C490	*22U6.3V 8/X5R	NG334	VCC2
C92	*22U6.3V 8/X5R	NG33	VCC3
C70	*22U6.3V 8/X5R	NG31	VCC4
C521	*22U6.3V 8/X5R	NG30	VCC6
C125	22U6.3V 8/X5R	AG29	VCC7
C103	22U6.3V 8/X5R	AG29	VCC8
C121	22U6.3V 8/X5R	AG29	VCC9
C126	22U6.3V 8/X5R	AG26	VCC10
C77	22U6.3V 8/X5R	AF35	VCC11
C124	22U6.3V 8/X5R	AF34	VCC12
C129	22U6.3V 8/X5R	AF33	VCC13
C78	10U6.3V 8/X5R	AF32	VCC14
C488	10U6.3V 8/X5R	AF31	VCC15
C505	10U6.3V 8/X5R	AF30	VCC16
C445	10U6.3V 8/X5R	AF29	VCC17
C520	10U6.3V 8/X5R	AF28	VCC18
C80	10U6.3V 8/X5R	AF27	VCC19
C516	10U6.3V 8/X5R	AF27	VCC21
C122	10U6.3V 8/X5R	AD35	VCC20
C515	*10U6.3V 8/X5R	ND34	VCC22
C489	*10U6.3V 8/X5R	ND33	VCC23
C120	10U6.3V 8/X5R	AD32	VCC24
C117	10U6.3V 8/X5R	AD31	VCC25
C522	*10U6.3V 8/X5R	ND30	VCC26
C518	*10U6.3V 8/X5R	ND29	VCC27
C108	*10U6.3V 8/X5R	ND28	VCC28
C123	*10U6.3V 8/X5R	ND27	VCC29
C446	*470U NC/	AD26	VCC30
C18	*470U NC	AC34	VCC31
		AC33	VCC32
		AC32	VCC33
		AC31	VCC34
		AC30	VCC35
		AC29	VCC36
		AC28	VCC37
		AC27	VCC38
		AC26	VCC40
		AA35	VCC41
		AA34	VCC42
		AA33	VCC43
		AA32	VCC44
		AA31	VCC45
		AA30	VCC46
		AA29	VCC47
		AA28	VCC48
		AA27	VCC49
		AA26	VCC50
		Y35	VCC51
		Y34	VCC52
		Y33	VCC53
		Y32	VCC54
		Y31	VCC55
		Y30	VCC56
		Y29	VCC57
		Y28	VCC58
		Y27	VCC59
		Y26	VCC60
		Y35	VCC61
		Y34	VCC62
		Y33	VCC63
		Y32	VCC64
		Y31	VCC65
		Y30	VCC66
		Y29	VCC67
		Y28	VCC68
		Y27	VCC69
		Y26	VCC70
		U34	VCC71
		U33	VCC72
		U32	VCC73
		U31	VCC74
		U30	VCC75
		U29	VCC76
		U28	VCC77
		U27	VCC78
		U26	VCC79
		U25	VCC80
		R35	VCC81
		R34	VCC82
		R33	VCC83
		R32	VCC84
		R31	VCC85
		R30	VCC86
		R29	VCC87
		R28	VCC88
		R27	VCC89
		R26	VCC90
		P35	VCC91
		P34	VCC92
		P33	VCC93
		P32	VCC94
		P31	VCC95
		P30	VCC96
		P29	VCC97
		P27	VCC98
		P26	VCC99
		P25	VCC100

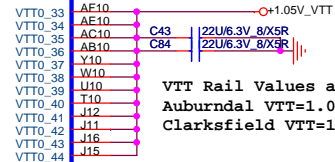
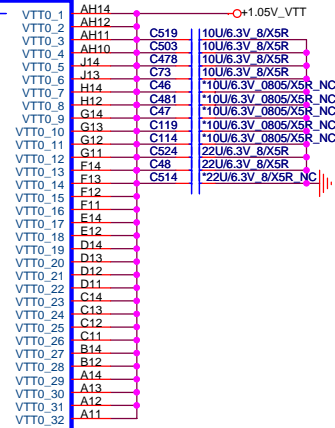
IC_AUB_CFD_PGA_R1P0

1.1V RAIL POWER

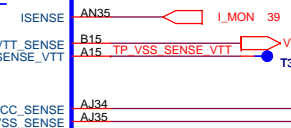
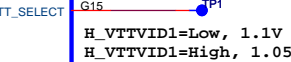
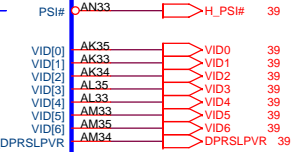
CPU CORE SUPPLY

POWER

SENSE LINES



VTT Rail Values are
 Auburndal VTT=1.05V
 Clarksville VTT=1.1V



VSS_SENSE_VTT:
 SC(V1.0)P20
 Connect VSS_SENSE_VTT to GND
 or can be left floating.
 Note: CRB has the VSS_SENSE_VTT floating.

PROC_DPRSPLVR:
 SC(V1.0)P19
 It is important to have the resistor stuffing options
 in the design for the Turbo functionality.
 The stuffing and no-stuffing of the resistors
 will depend on the POC configuration of AUB
 and CFB

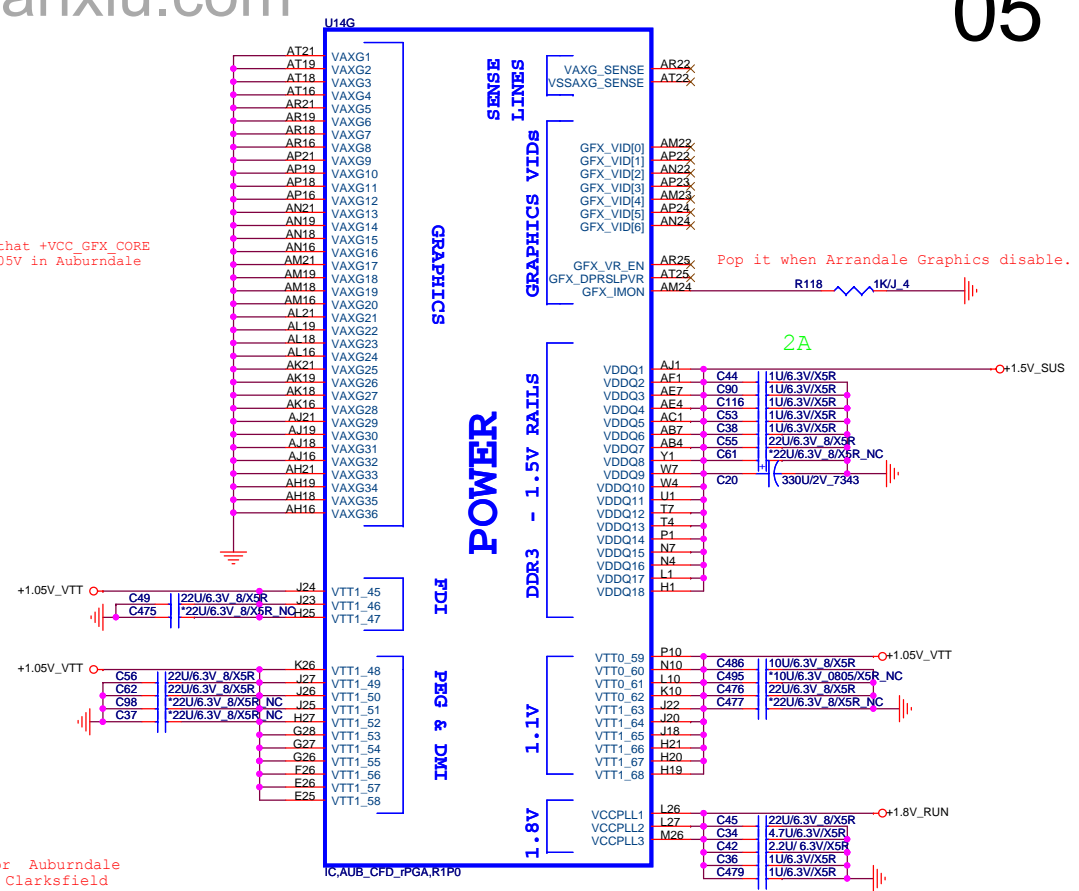
CRB(V1.0)P67:
 uses 1K pull-up and pull-down resistors
 CRB default setting is "1"

Please note that +VCC_GFX_CORE
 should be 1.05V in Auburndale

VTT_SELECT:
 High level 1.05V for Auburndale
 Low level 1.1V for Clarksville

VCC_SENSE & VSS_SENSE:
 SC(V1.0)P19
 100- ohm pull-down to GND near processor

0525 Steg : As an option, VTT_SENSE pin on the
 processor can be left floating. But the platform
 needs to have the FB (feedback) pin of the VR tied
 to the VTT plane regulation.



GRAPHICS

POWER

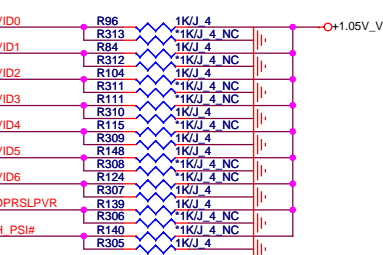
FDI

PEG & DMI

DDR3 - 1.5V RAILS

1.1V

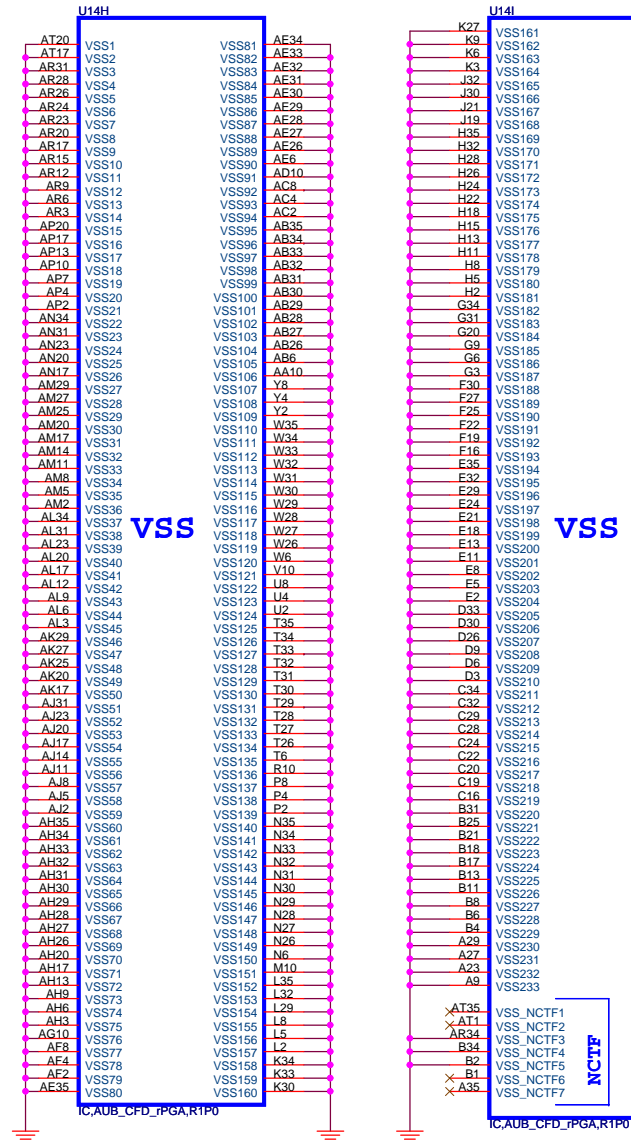
1.8V



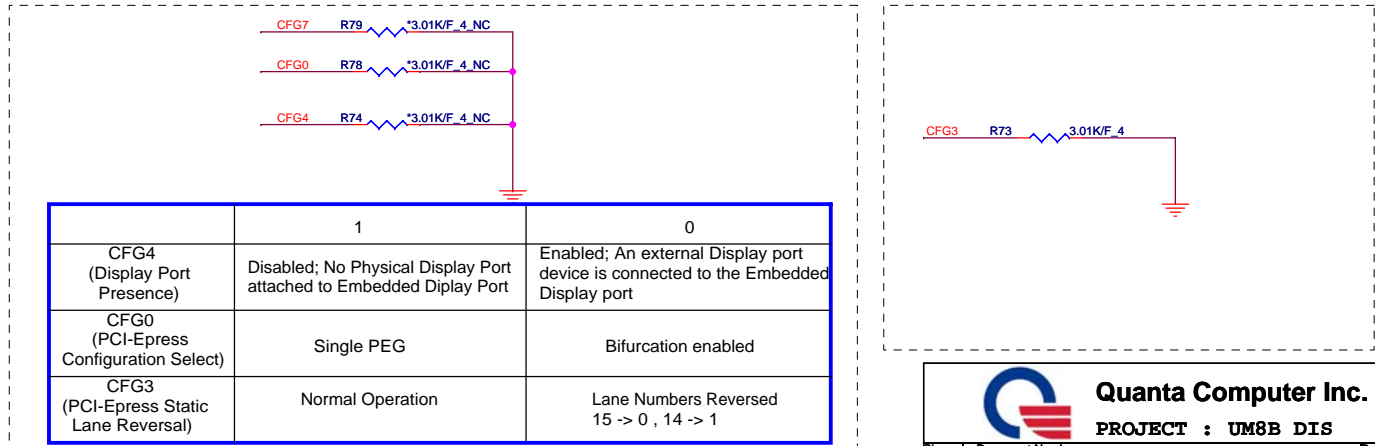
HFM_VID : Max 1.4V
 LFM_VID : Min 0.65V

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

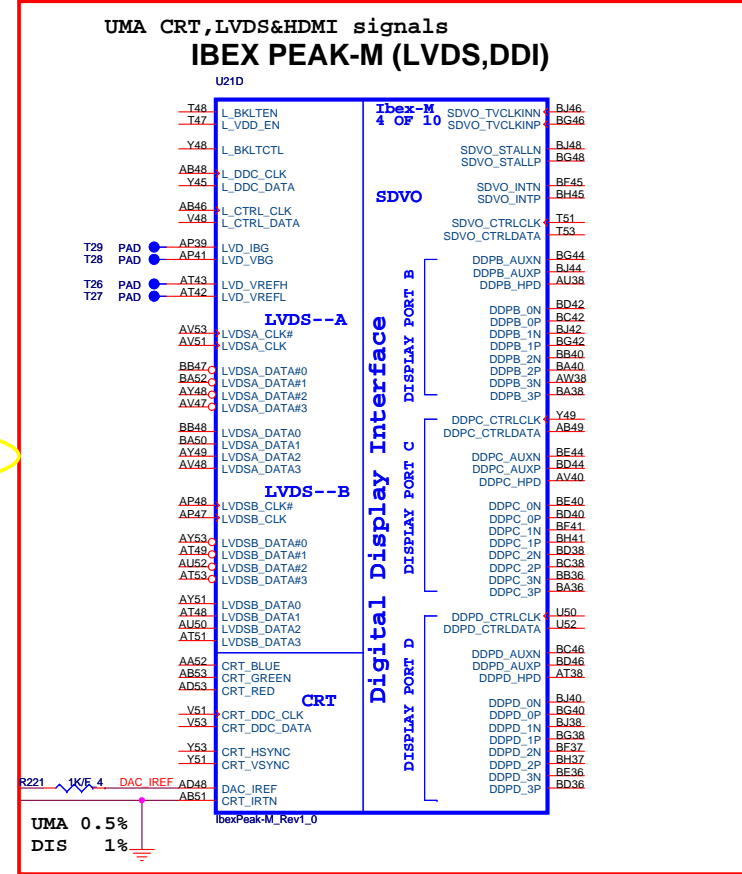
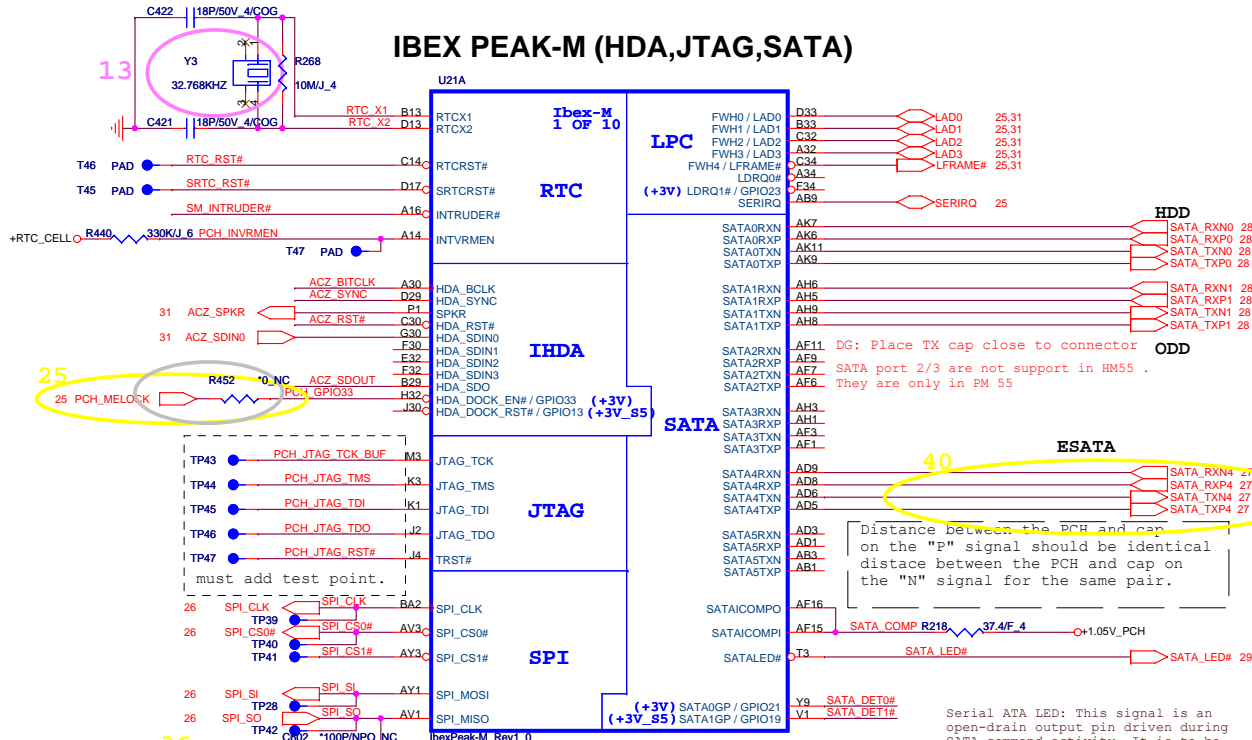


Quanta Computer Inc.
PROJECT : UM8B DIS

PROCESSOR 4/4 (GND)

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IBEX PEAK-M (HDA,JTAG,SATA)



Flash Descriptor Security Override

GPIO33	Low = Enabled High = Disabled
--------	----------------------------------

R245 1 2 *1K_NC PCH_GPIO33

(Internal 20K/F pull high to +3.3V_RUN)

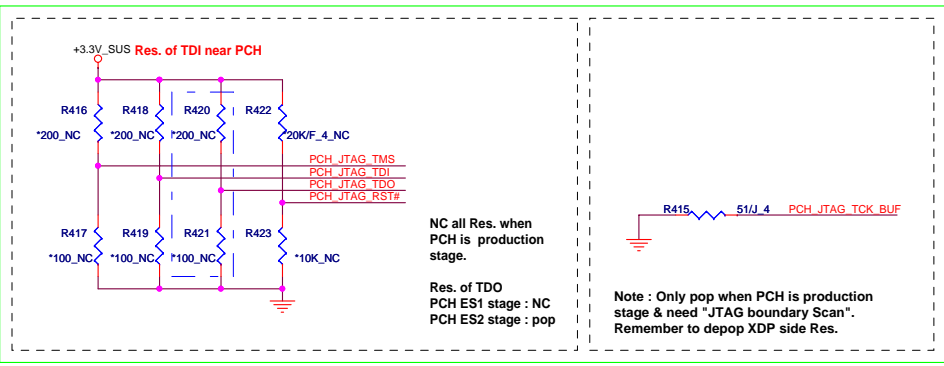
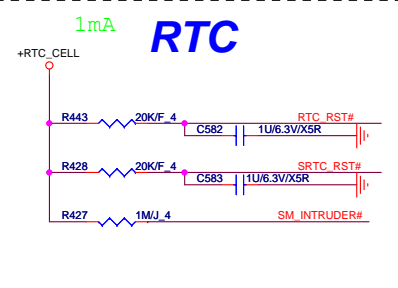
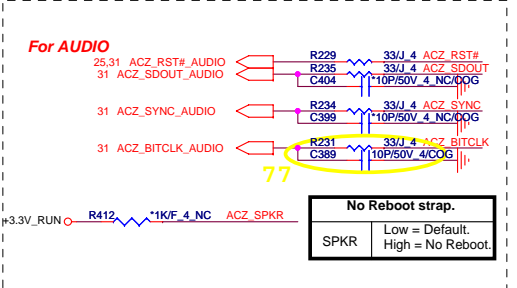
Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode. This signal should be only asserted low through an external pull-down in manufacturing or debug environments ONLY.

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

Serial ATA LED: This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc_3 is required.

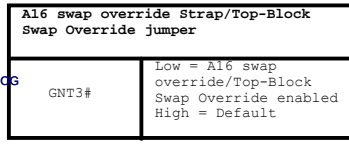
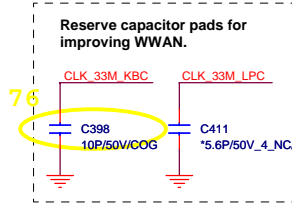
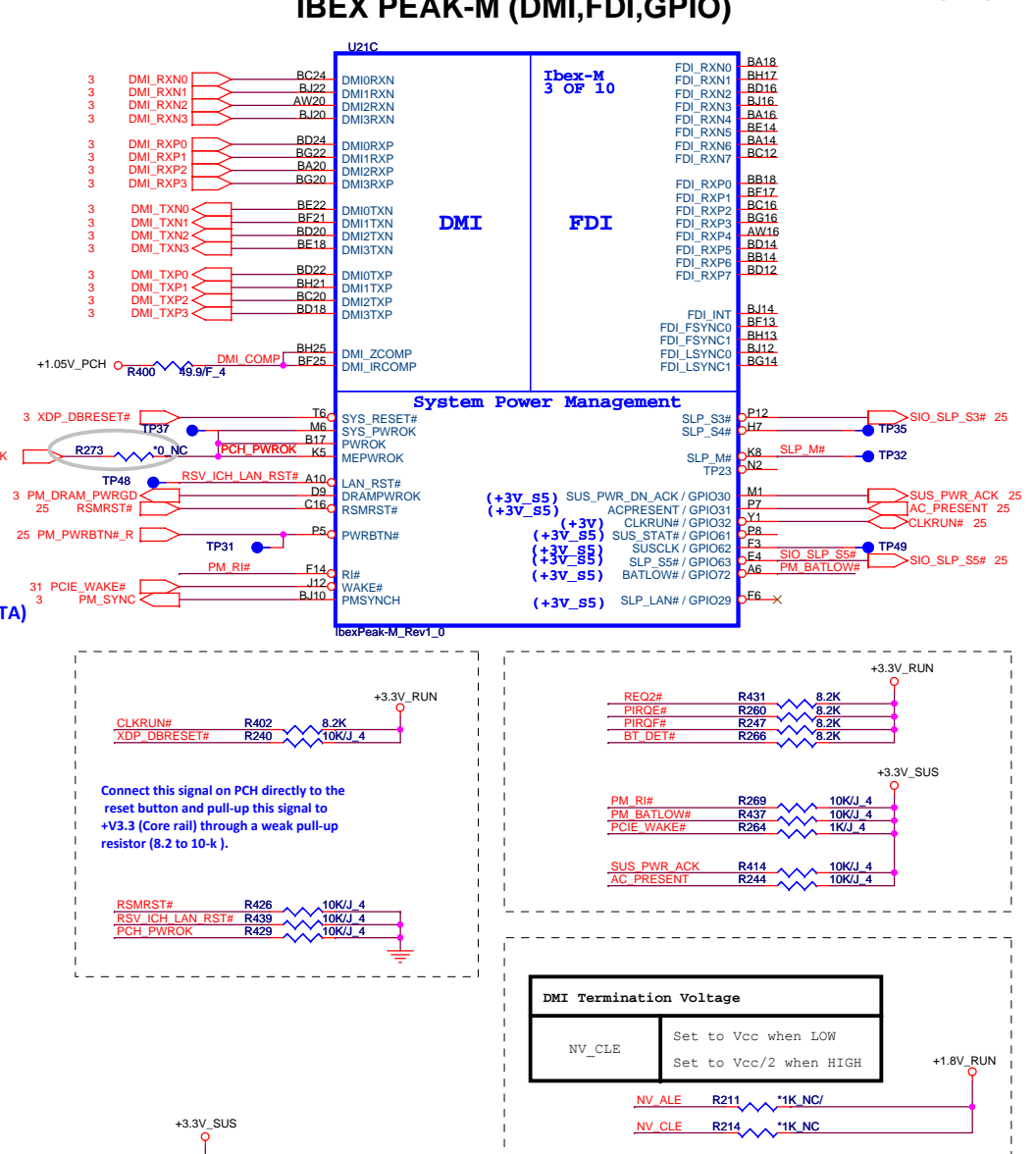
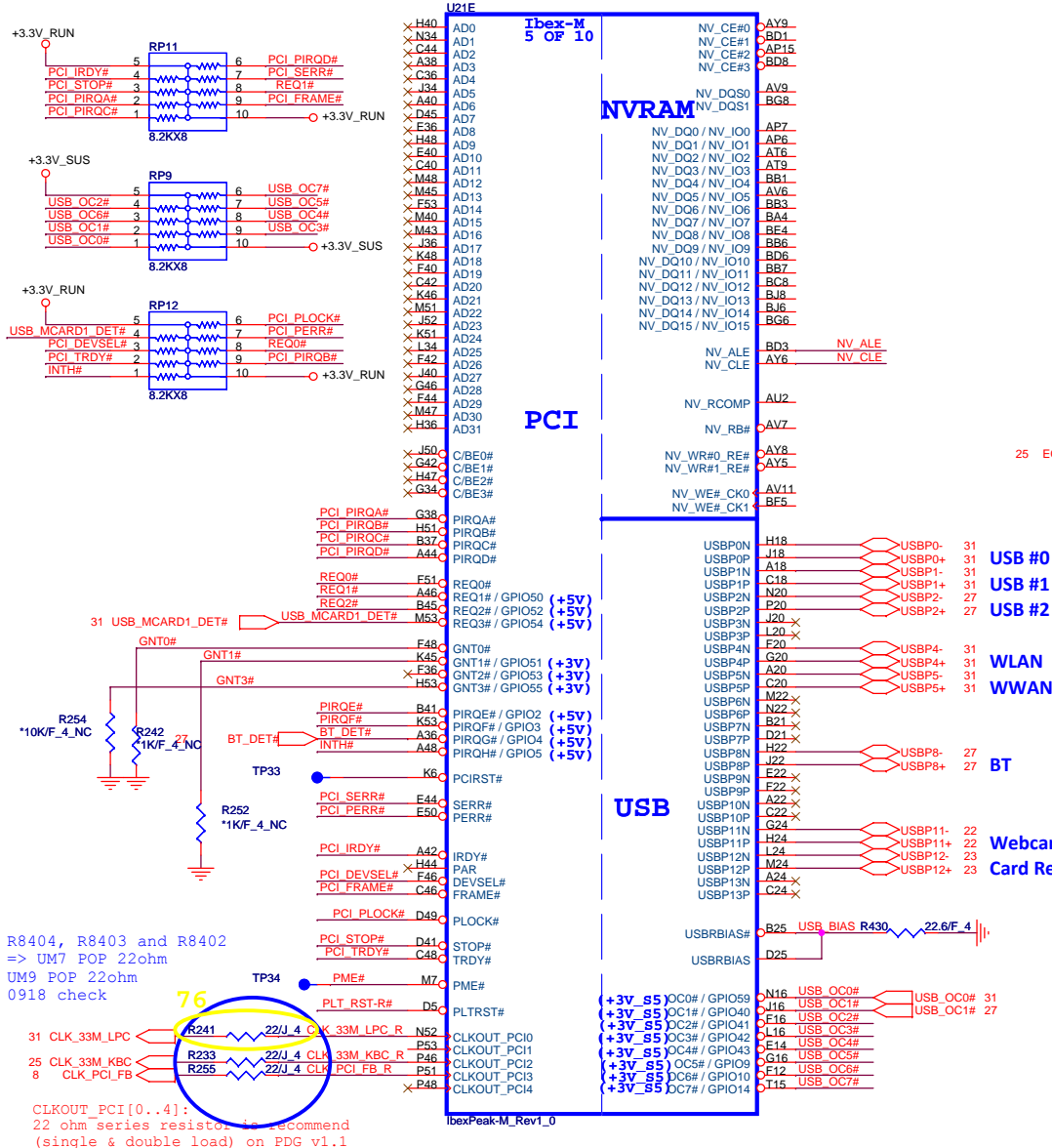
iTPM ENABLE/DISABLE

TPM Function	Mount
Enable	Mount
Disable	NC (Default)



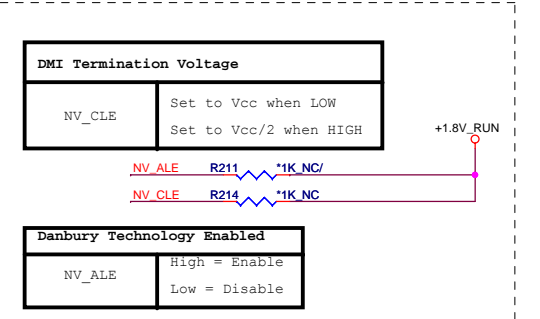
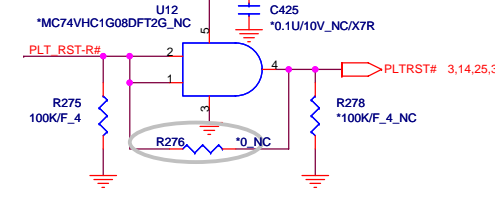
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (DMI,FDI,GPIO)



Boot BIOS Strap

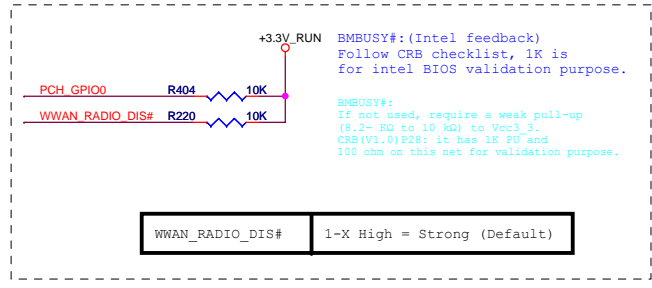
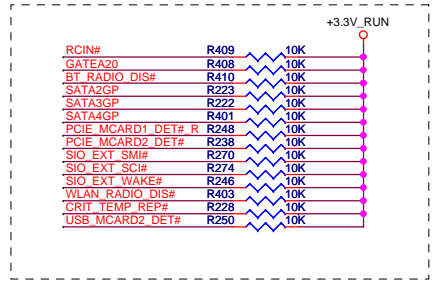
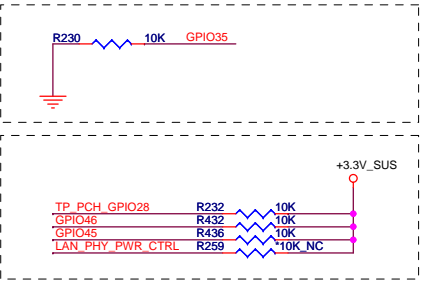
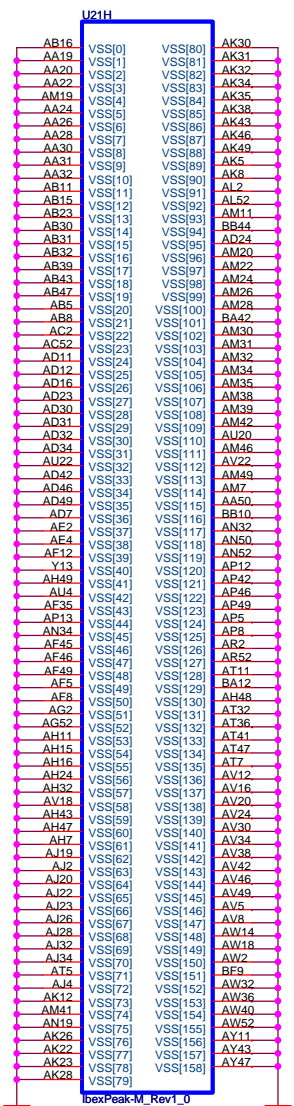
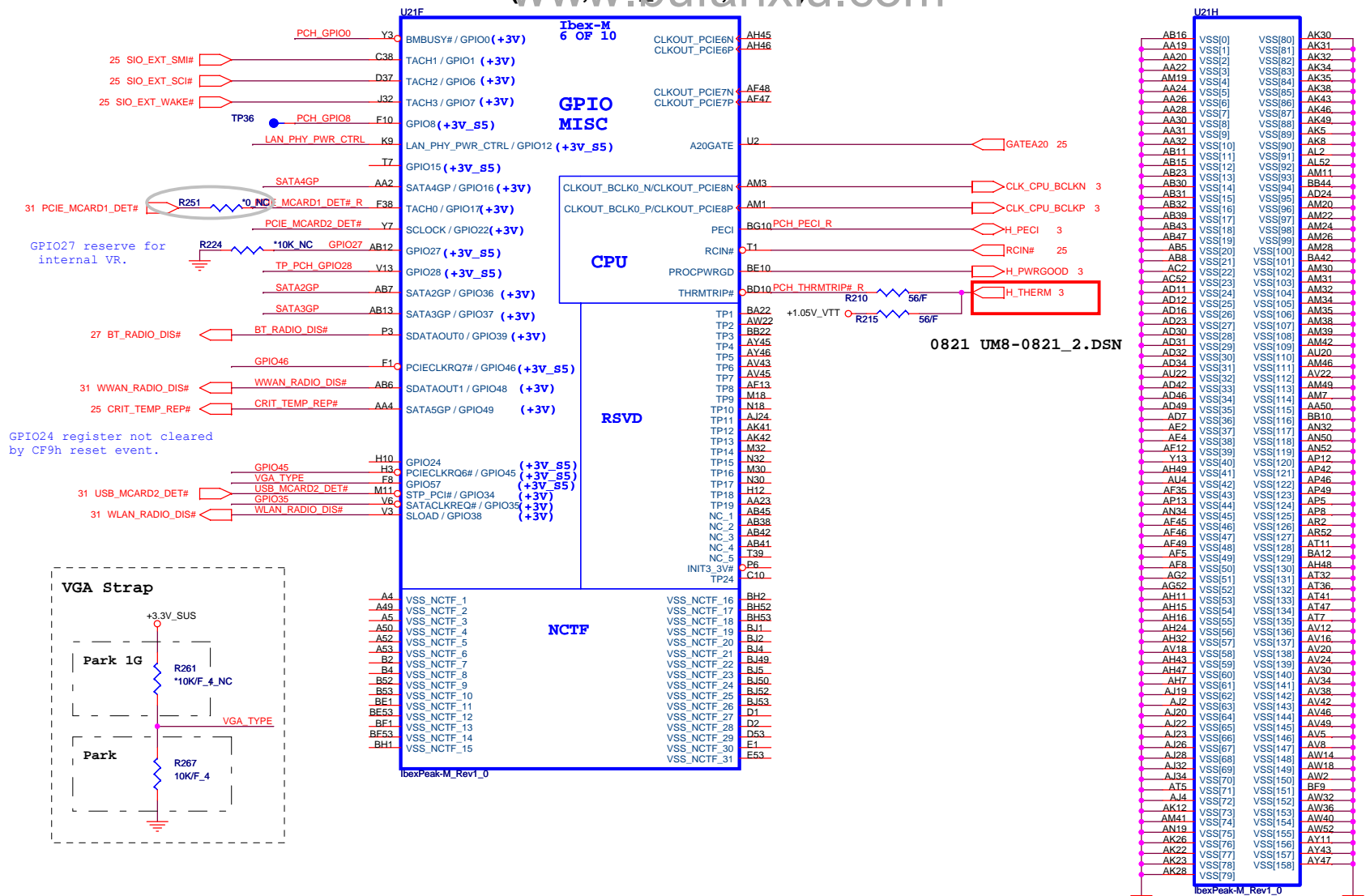
GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



Quanta Computer Inc. PROJECT : UM8B DIS

Size Document Number PCH 3/5 (PCI,ONFI,USB,DMI) Rev 1A

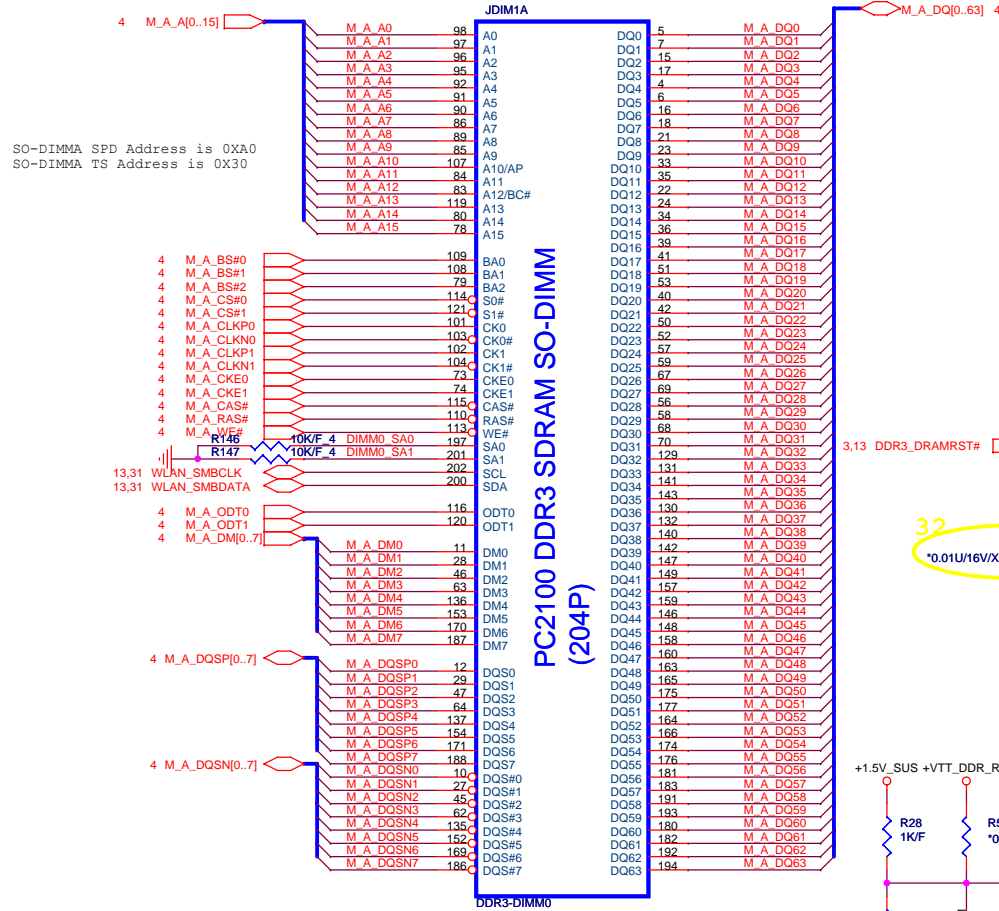
Date: Friday, February 05, 2010 Sheet 9 of 46



Quanta Computer Inc.
PROJECT : UM8B DIS
PCH 4/5 (GPIO & Strap)

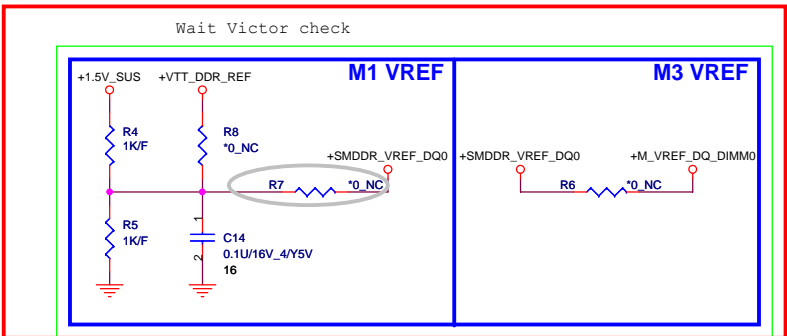
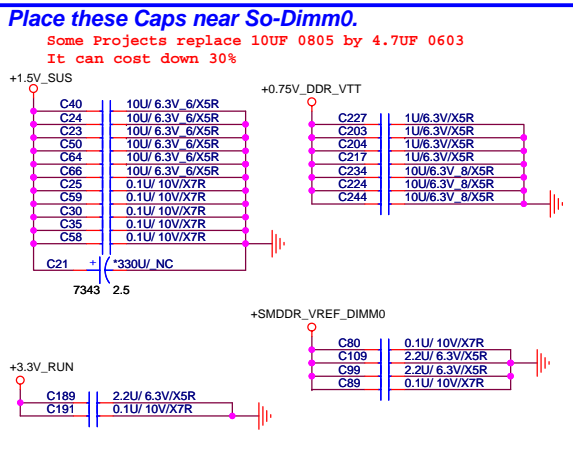
Size	Document Number	Rev
		1A

Date: Friday, February 05, 2010 Sheet 10 of 46



The EVENT# pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT# bus line to Vdspd on the system planer to act as a pullup. (DDR3 DS REV0.5)

for S3 power reduction



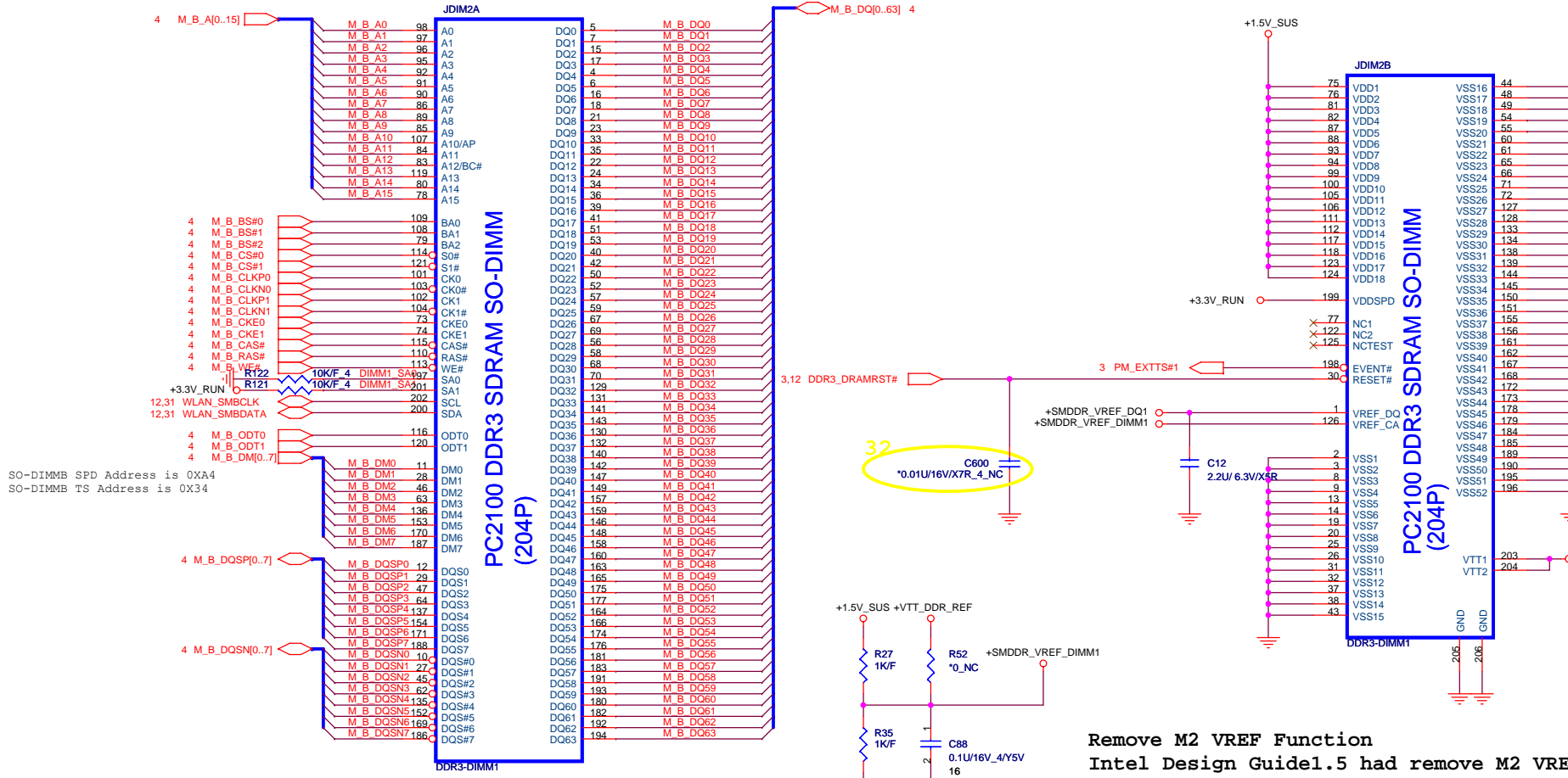
M2 VREF

Remove M2 VREF Function
Intel Design Guidel.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarkfield processor

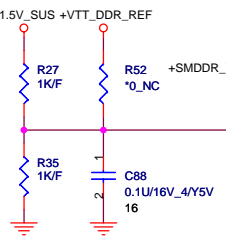
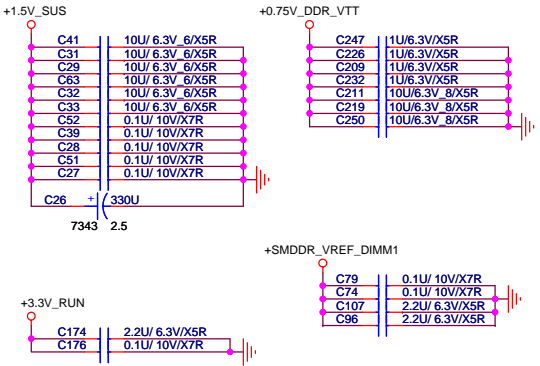
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	DDR3 DIMM-0	1A
Date:	Friday, February 05, 2010	Sheet 12 of 46



SO-DIMMB SPD Address is 0XA4
 SO-DIMMB TS Address is 0X34

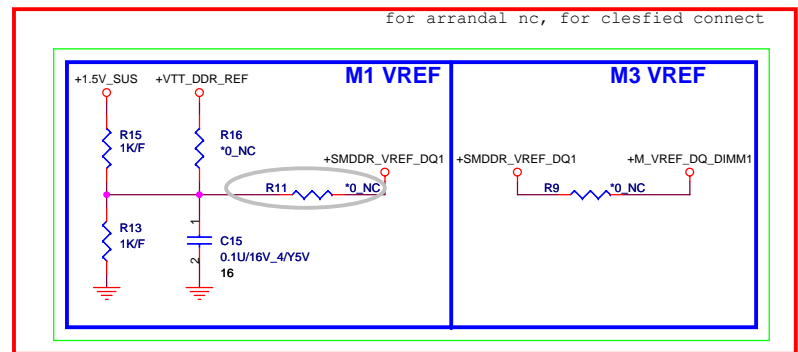
Place these Caps near So-Dimm1.
 Some Projects replace 10UF 0805 by 4.7UF 0603
 It can cost down 30%

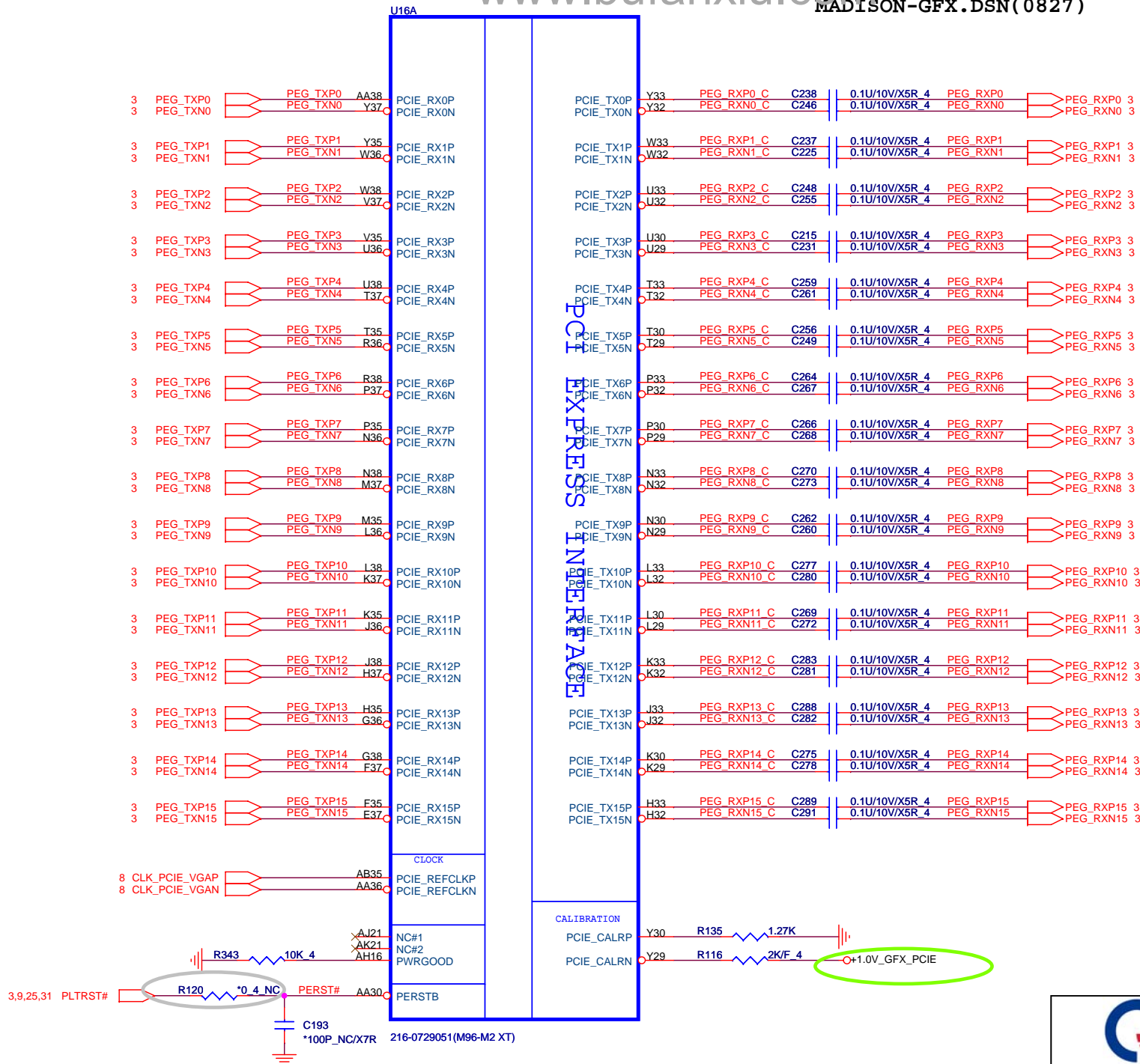


Remove M2 VREF Function
 Intel Design Guidel.5 had remove M2 VREF (I2C programble VREF)

M3 => support for Clarkfield processor

Wait Victor check

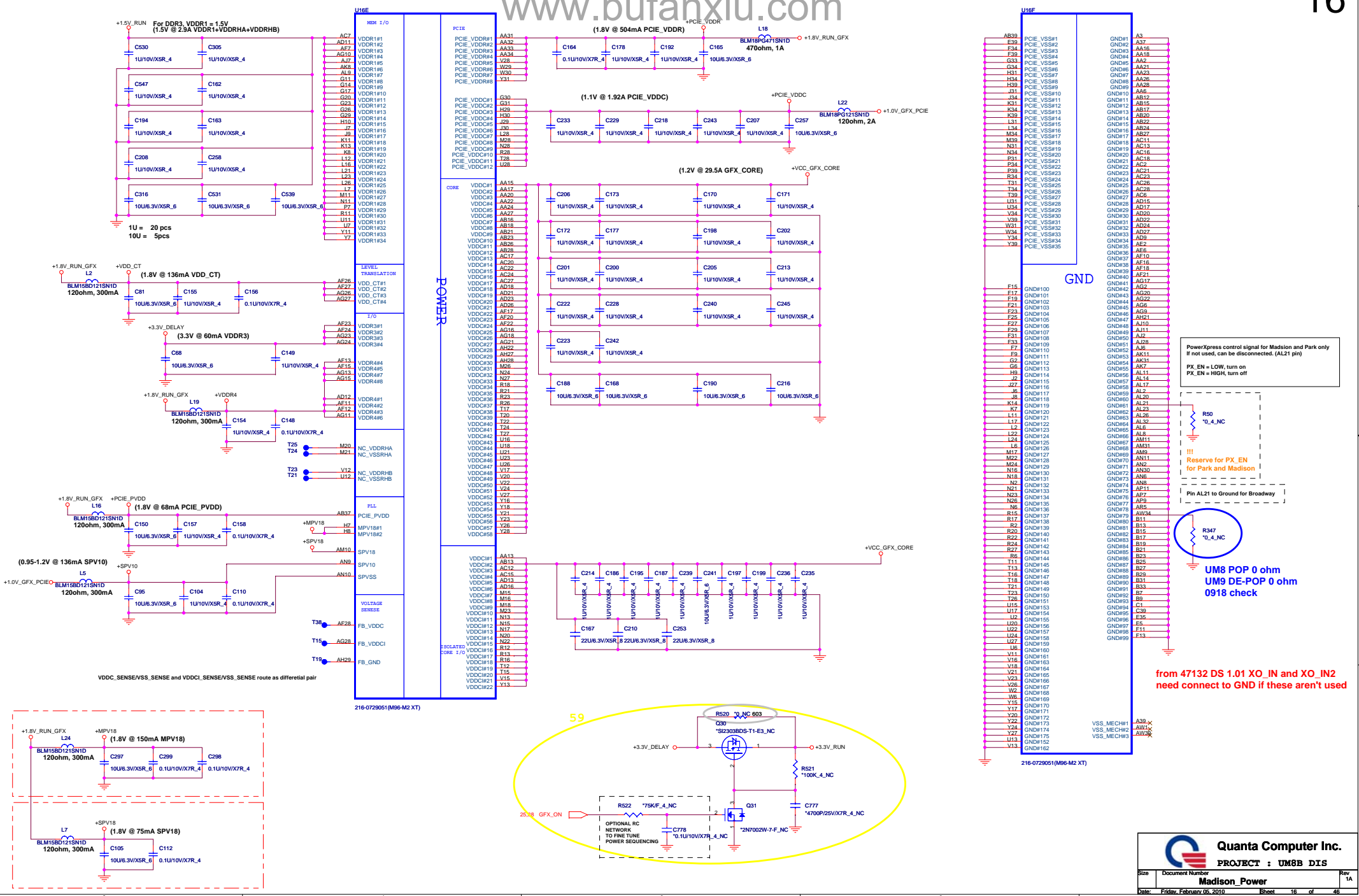




Quanta Computer Inc.
PROJECT : UM8B DIS

Size Document Number Rev #
Madison PCIE I/F 1A

Date: Friday, February 05, 2010 Sheet 14 of 46



PowerXpress control signal for Madison and Park only
 If not used, can be disconnected. (AL21 pin)
 PX_EN = LOW, turn on
 PX_EN = HIGH, turn off

Reserve for PX_EN
 for Park and Madison

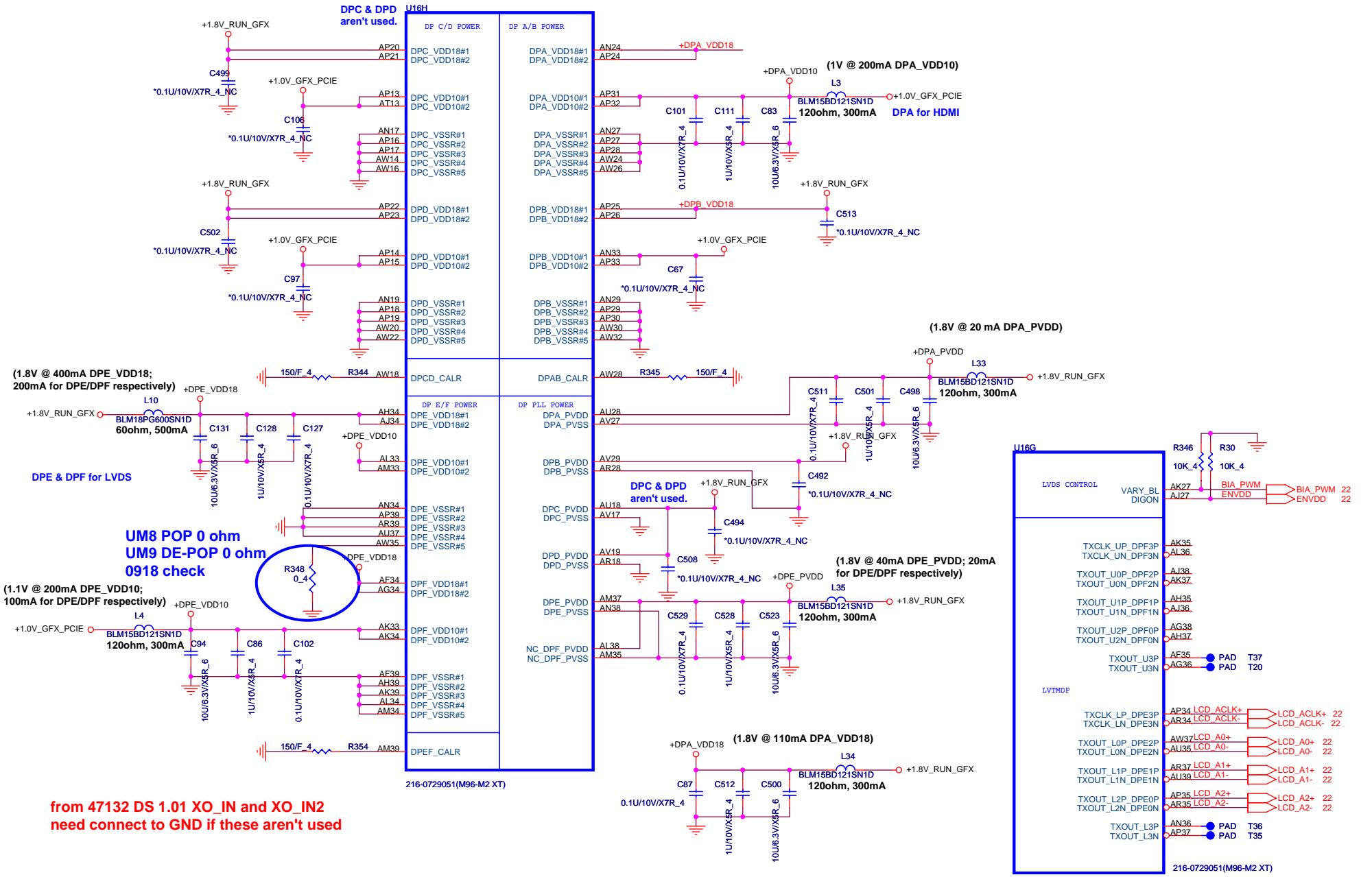
UM8B POP 0 ohm
 UM9 DE-POP 0 ohm
 0918 check

from 47132 DS 1.01 XO_IN and XO_IN2
 need connect to GND if these aren't used

Quanta Computer Inc.
PROJECT : UM8B DIS

Size: Document Number: **Madison Power** Rev: A
 Date: Friday, February 05, 2010 Sheet: 16 of 48

!!!
For M96/92, DPx_VDD10 = 1.1
For M97 DPx_VDD10 = 1.0V

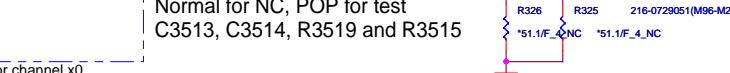
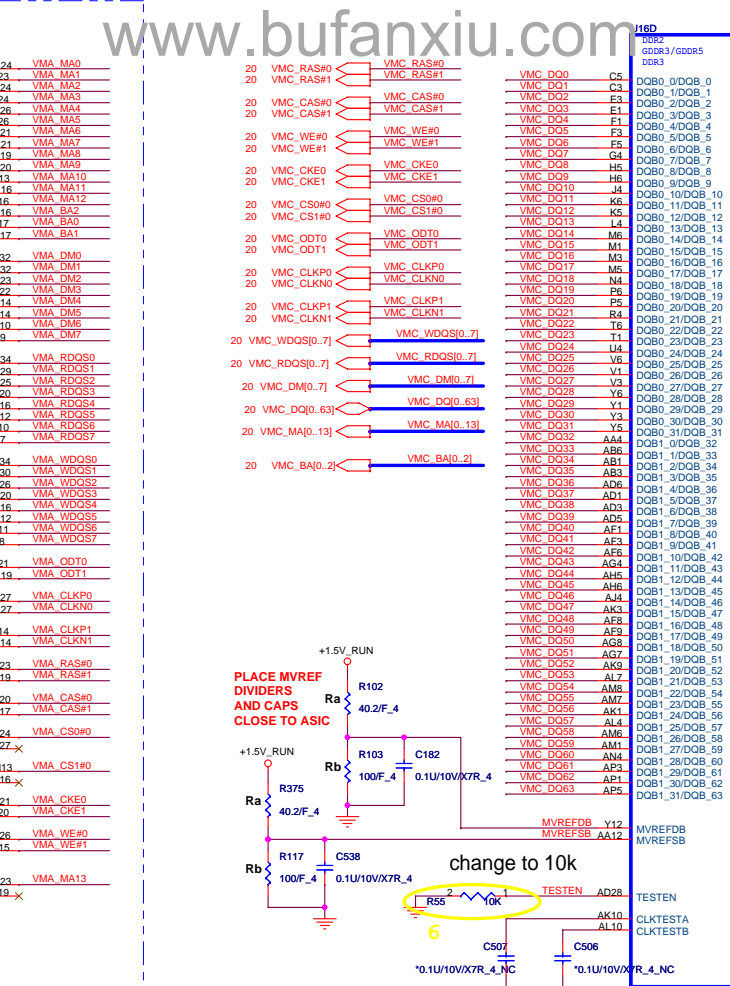
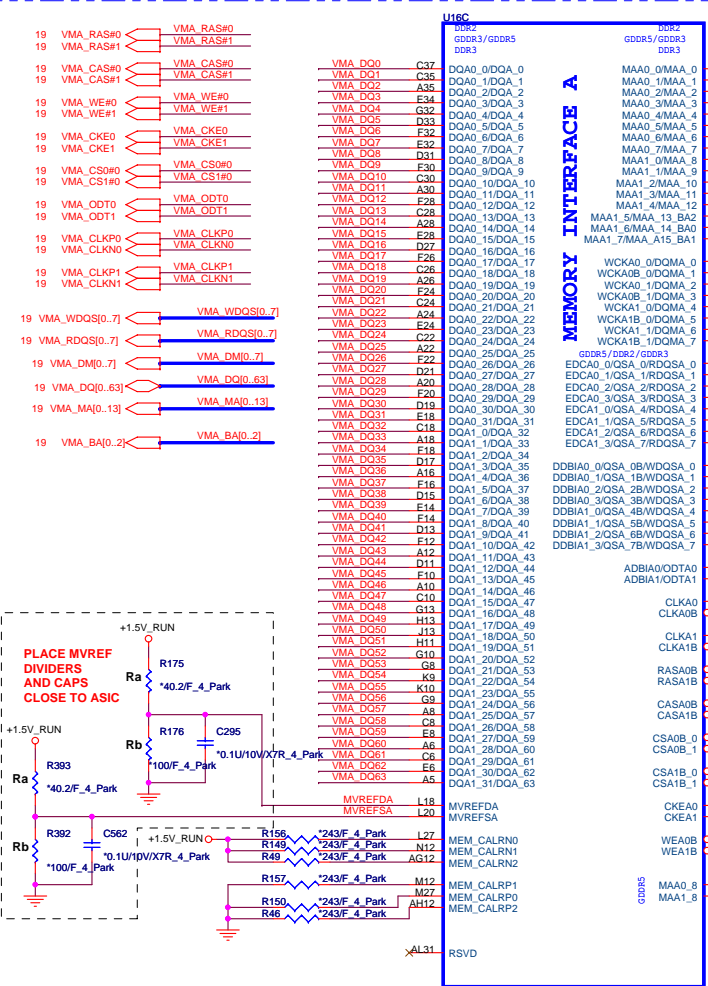


216-0729051(M96-M2 XT)

216-0729051(M96-M2 XT)

Quanta Computer Inc.
PROJECT : UM8B DIS
Madison_DP_POWER

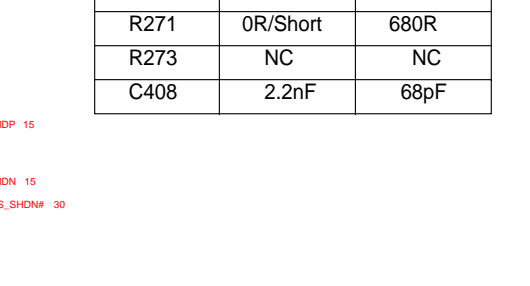
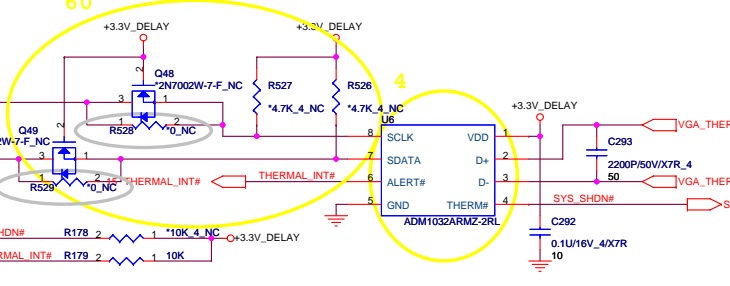
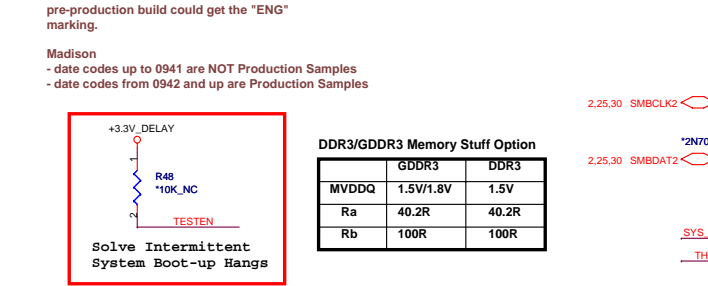
Size: Document Number: Rev 1A
Date: Friday, February 05, 2010 Sheet 17 of 46

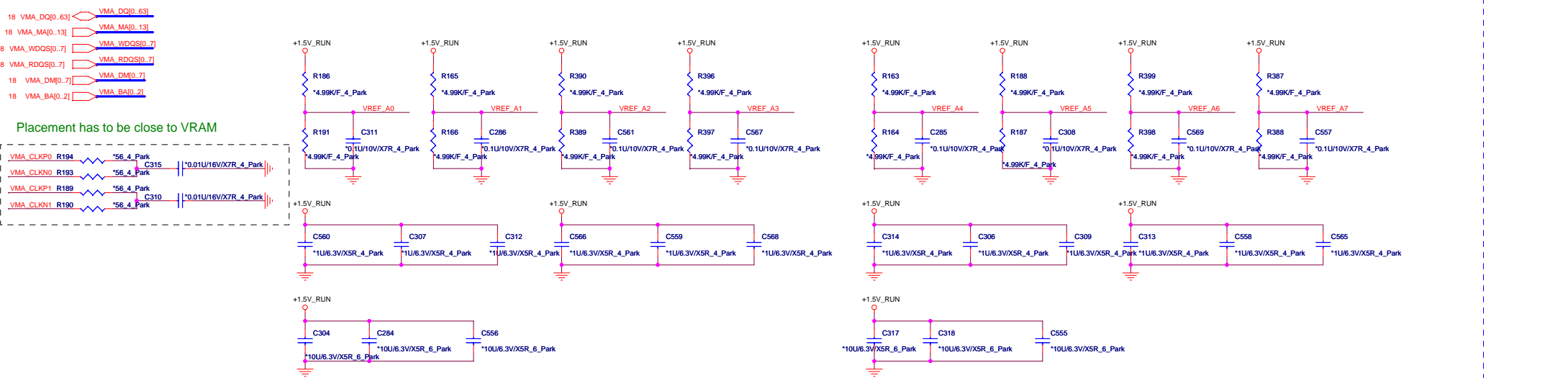
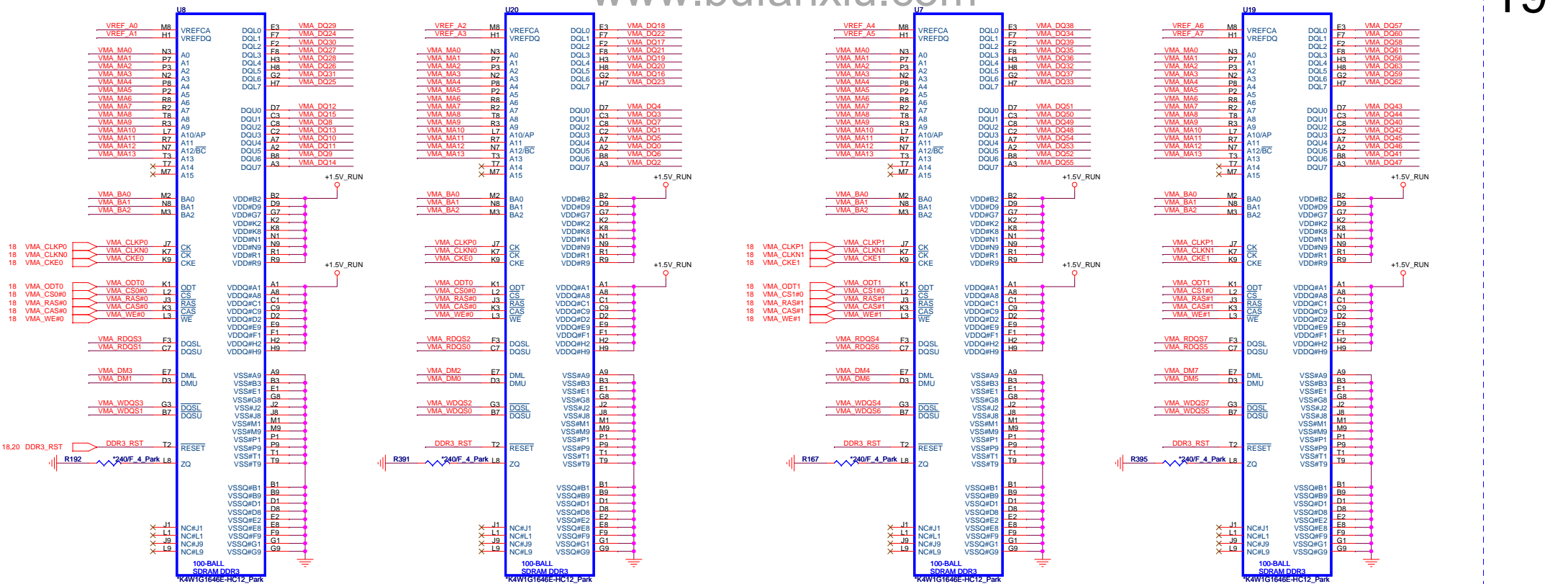


NC for GFX Park portion
 For Park, Madison production version ASIC is need removed workaround.
 Park pre-production build could get the "ENG" marking.
 Madison
 - date codes up to 0941 are NOT Production Samples
 - date codes from 0942 and up are Production Samples

Normal for NC, POP for test
 C3513, C3514, R3519 and R3515
 ADM1032-1 => Hex 4C (1001 100) AL001032001
 ADM1032-2 => Hex 4D (1001 101) AL001032002

Designator	For M97-M2	For Madison
R272	10K	10K
R271	0R/Short	680R
R273	NC	NC
C408	2.2nF	68pF

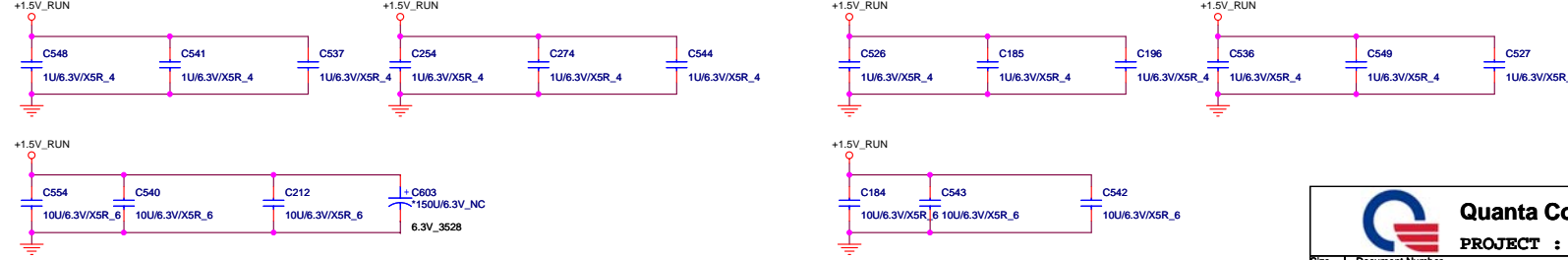
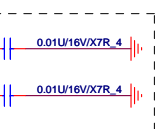
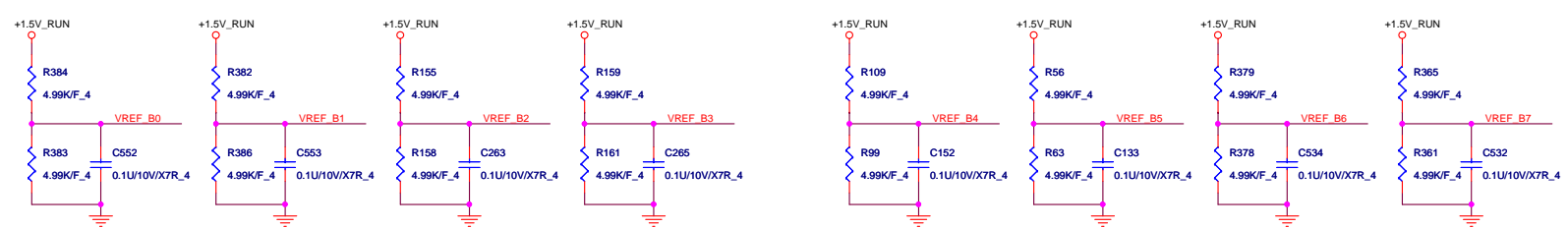
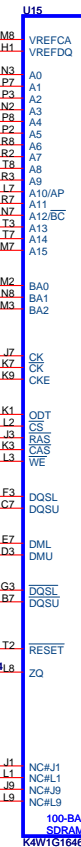
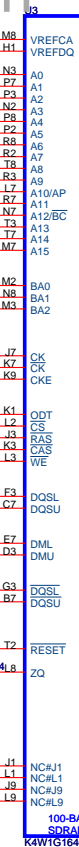
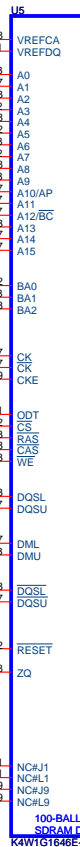
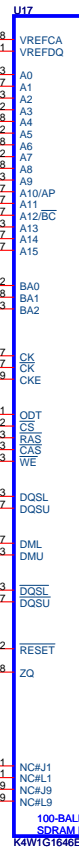




NC for GFX Park portion

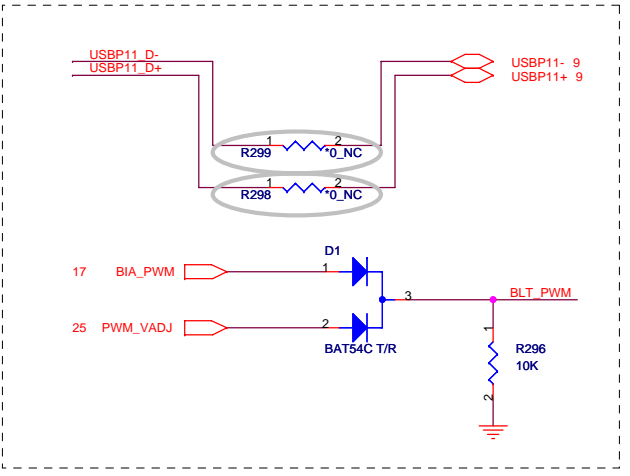
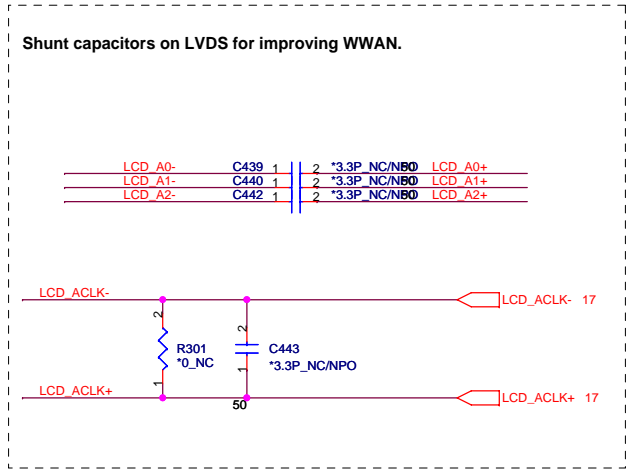
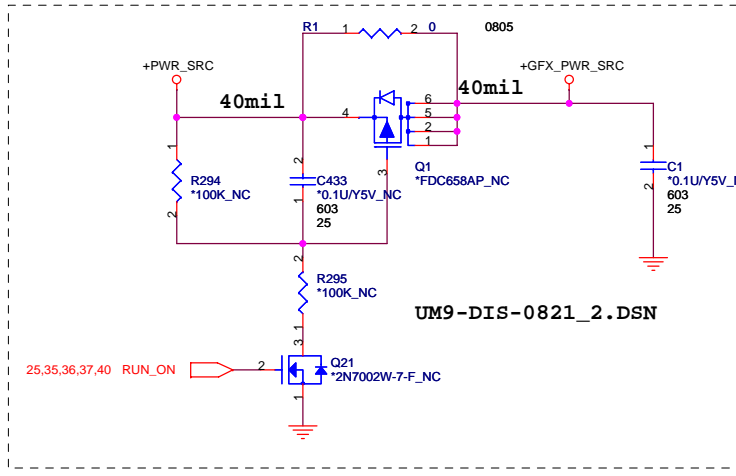
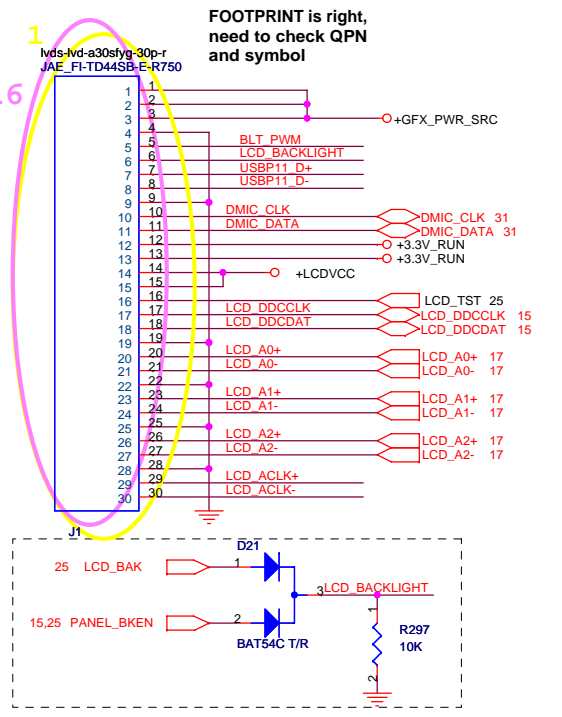
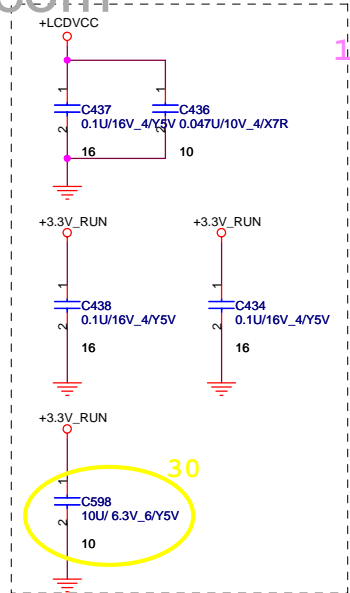
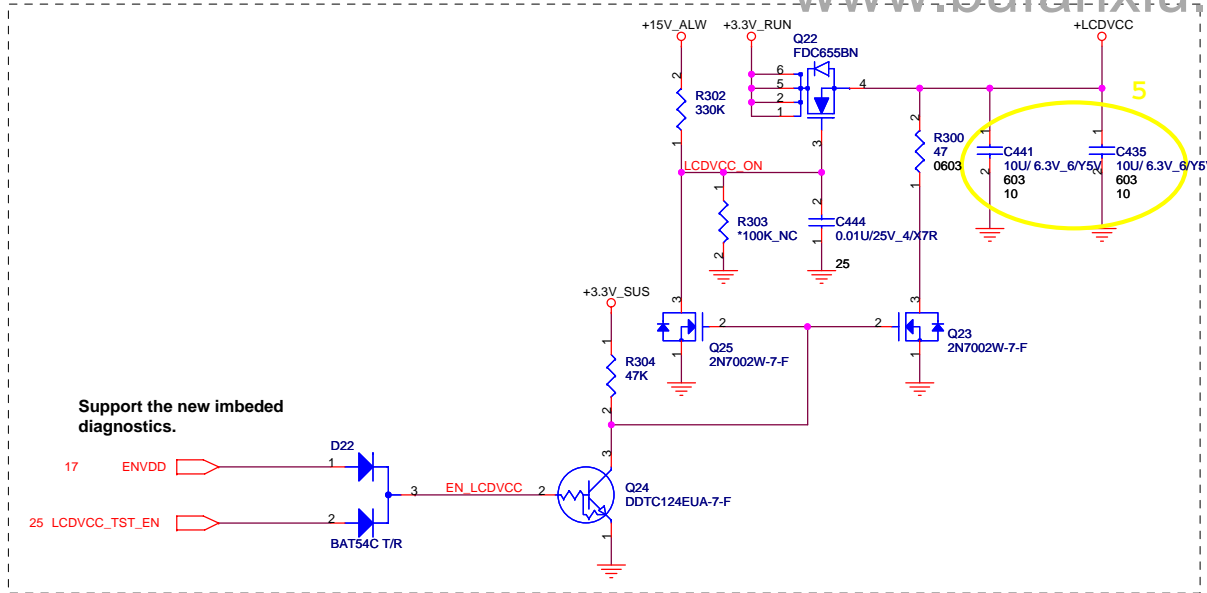
Samsung: AKD5LGGT505
Hynix: AKD5LZGTW03

Quanta Computer Inc.
PROJECT : UM8B DIS
Madison_DDR3_A_512M
Date: Friday, February 05, 2010 Sheet 19 of 46



Placement has to be close to VRAM

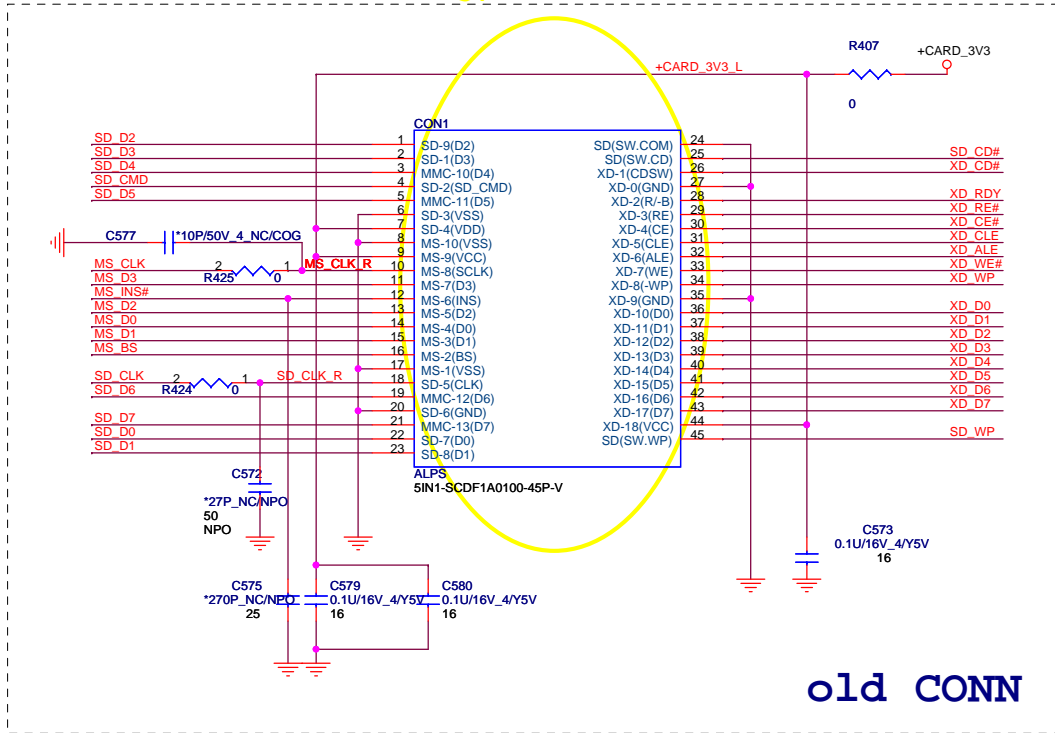
Quanta Computer Inc.
PROJECT : UM8B DIS
Madison_DDR3_B_512M
 Date: Friday, February 05, 2010 Sheet 20 of 46



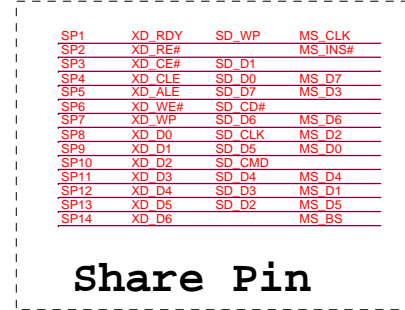
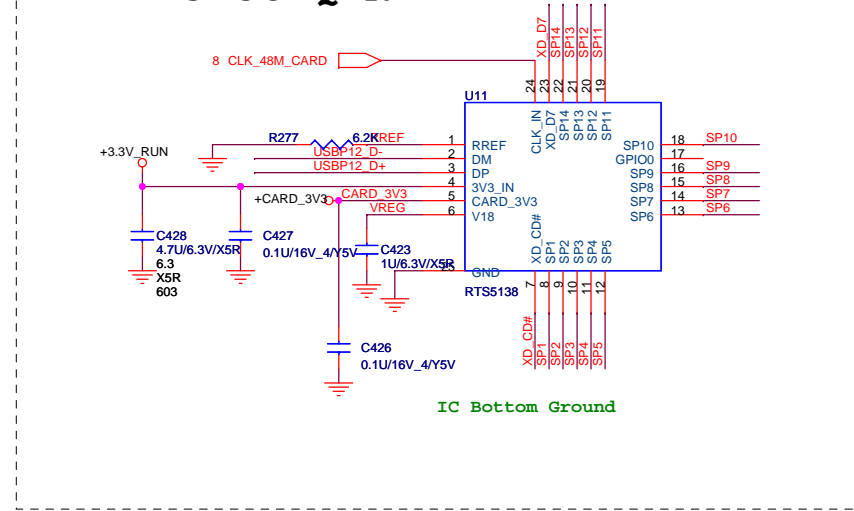
Quanta Computer Inc.
PROJECT : UM8B DIS

Size	Document Number	Rev
	LCD CONN	1A
Date:	Friday, February 05, 2010	Sheet 22 of 46

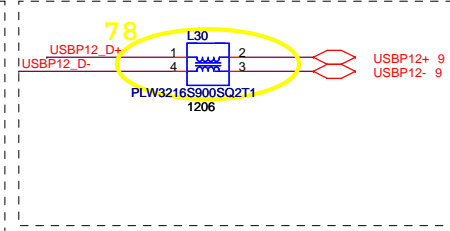
37

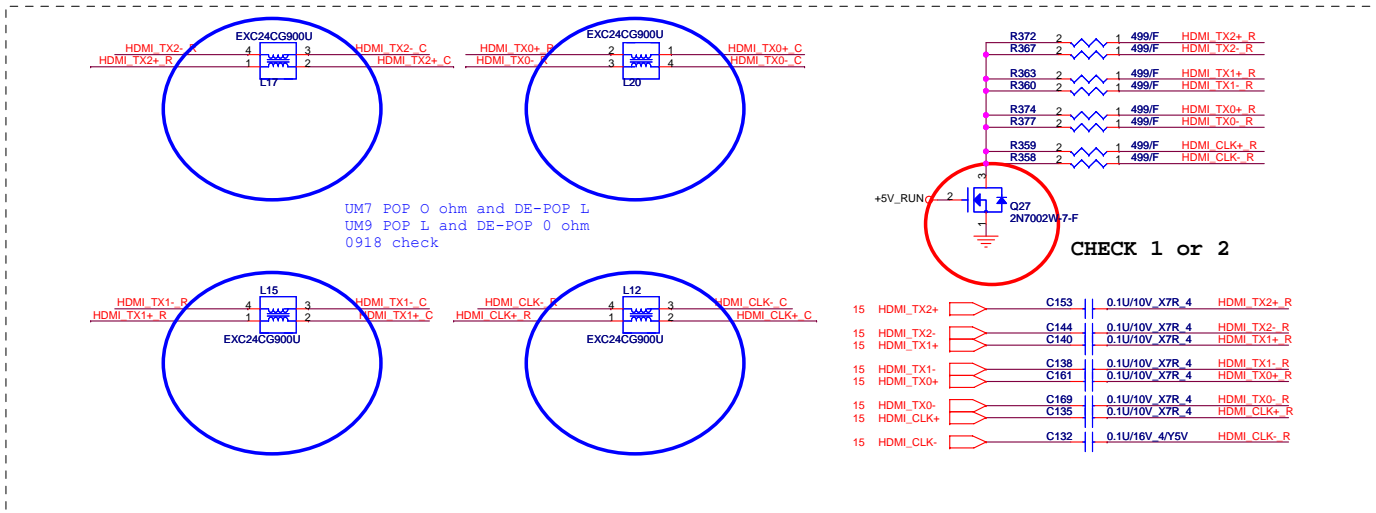
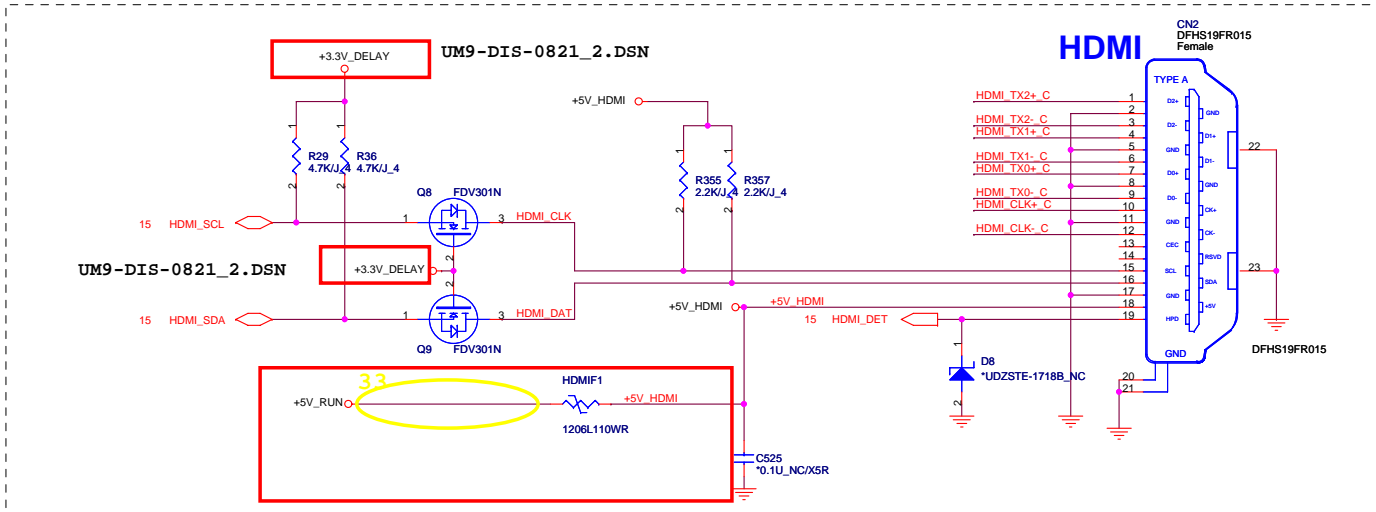


RTS5138-QFN24

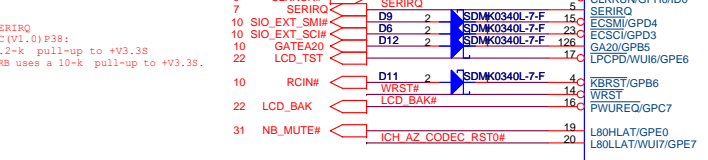
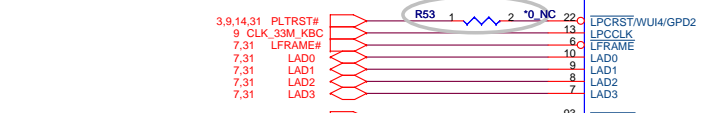
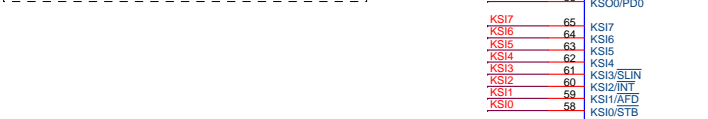
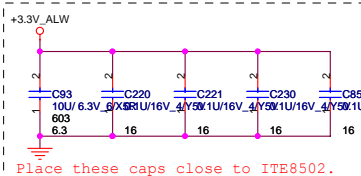


Share Pin





ITE8502 LQFP-128L

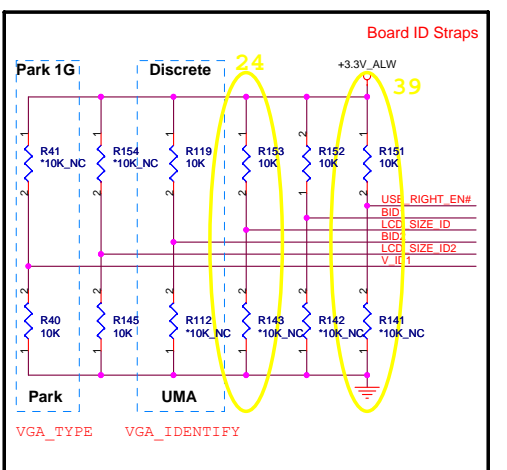
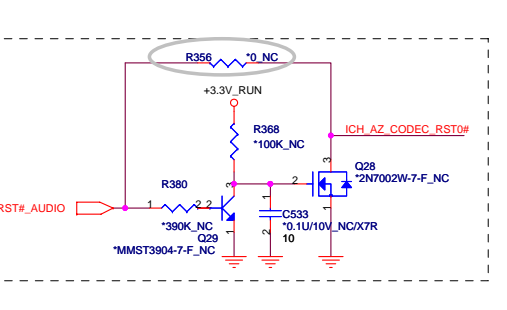
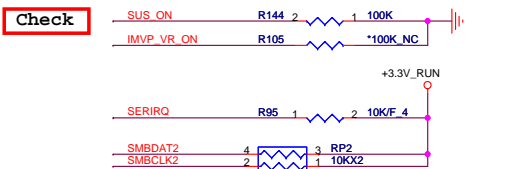
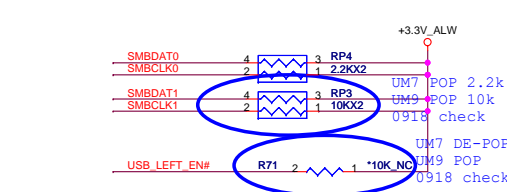
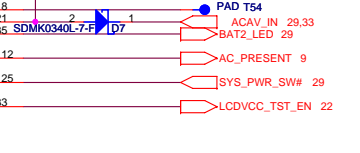
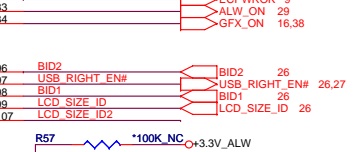
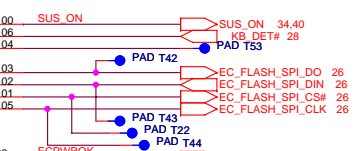
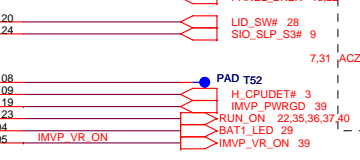
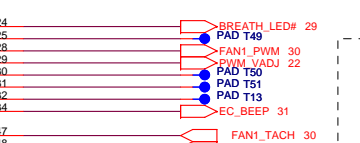
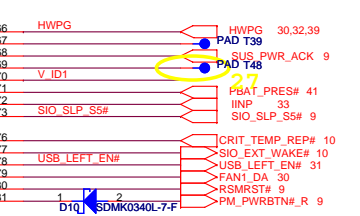
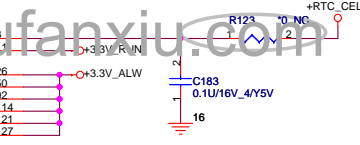
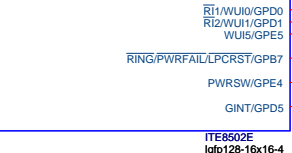
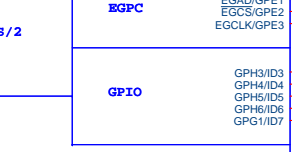
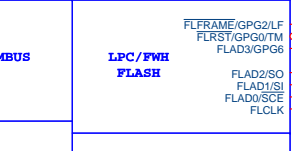
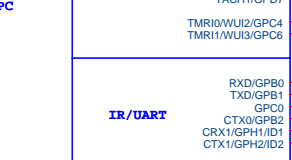
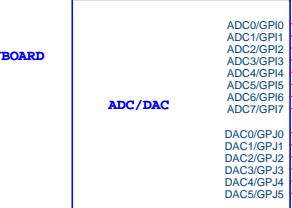
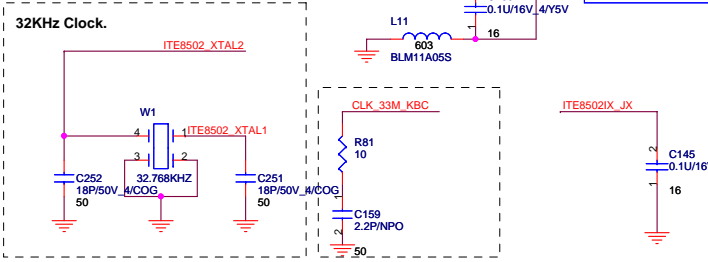
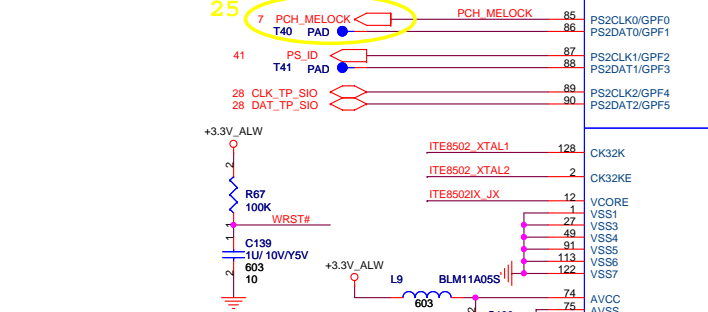


Charge and BAT

PCH

LAN, Clock

Thermal IC

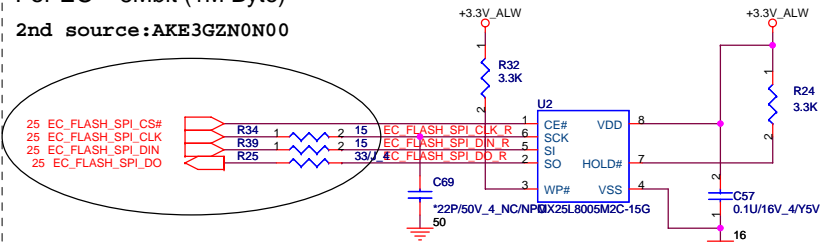


BID1	USB_RIGHT_EN#	UM8(UMA)	UM8C(Dis)
0	0	SSI (X00)	SSI (X00)
0	0	PT (X01)	PT (X01)
0	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

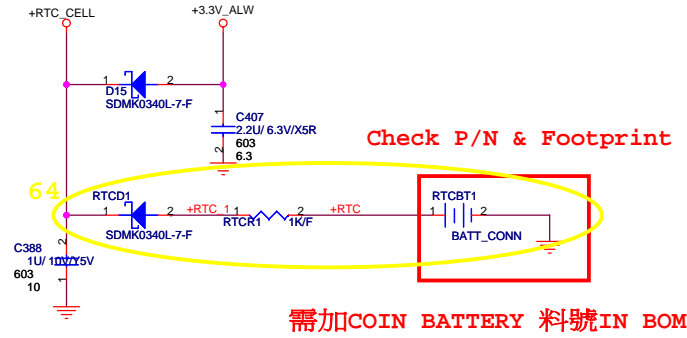
LCD SIZE_ID (99)	LCD SIZE_ID2 (107)
13"	0
14"	0
15"	1
17"	0

For EC 8Mbit (1M Byte)

2nd source:AKE3GZN0N00



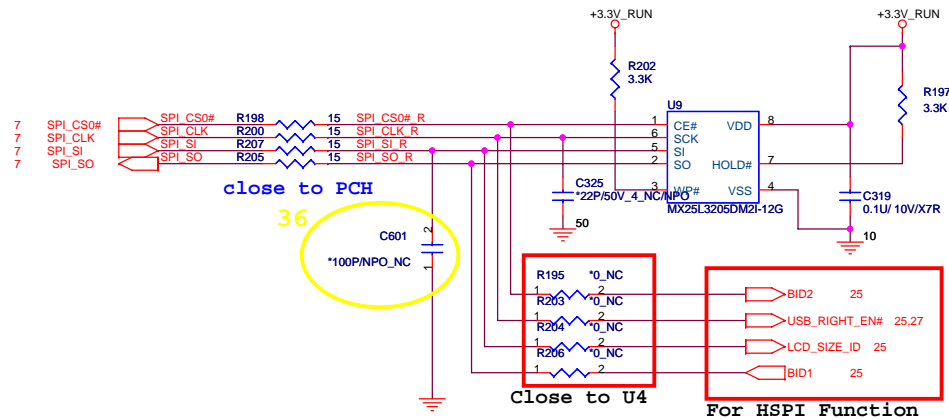
RTC BATTERY



For PCH

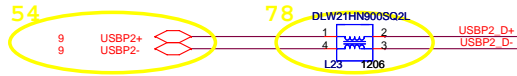
32Mbit (4M Byte)

2nd source:AKE39ZP0N00

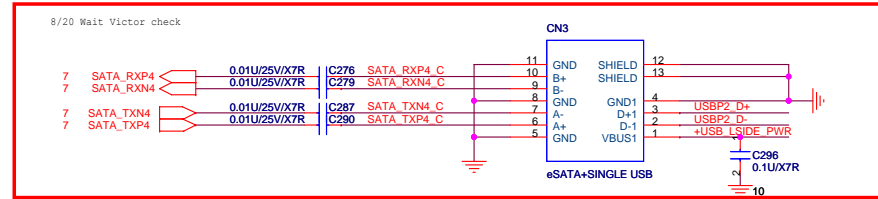


eSATA and USB To DB

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

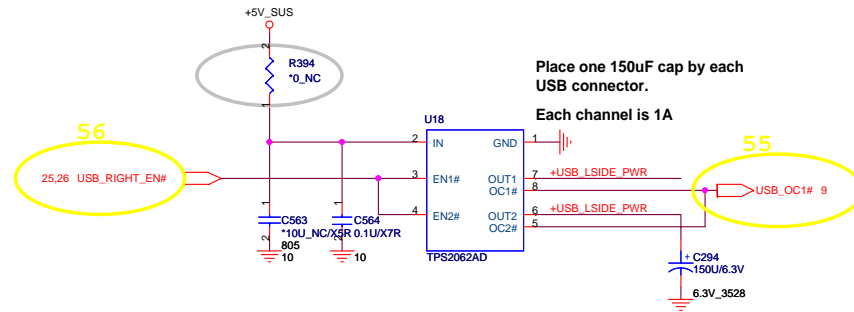
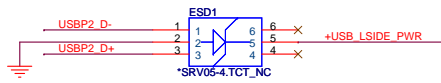


USB and eSATA Conn.



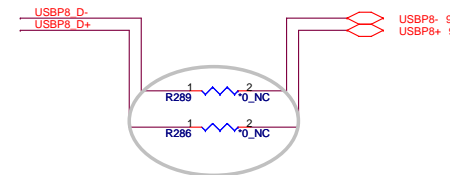
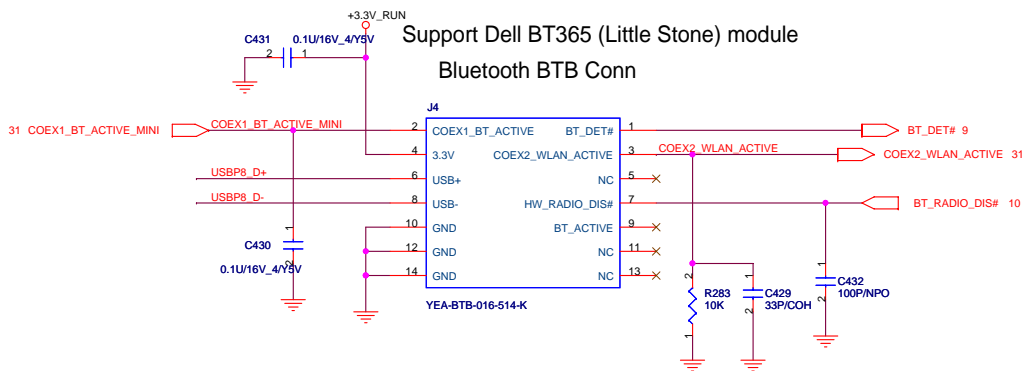
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

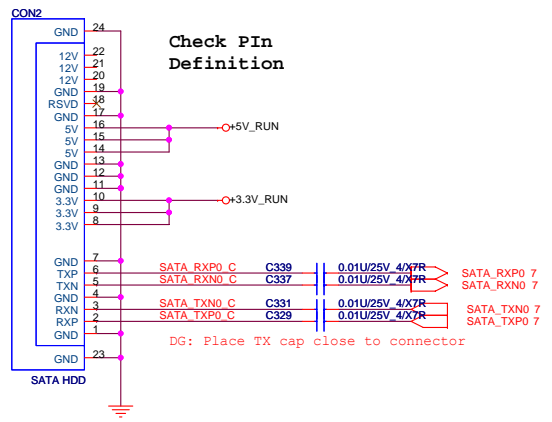


Support Dell BT365 (Little Stone) module

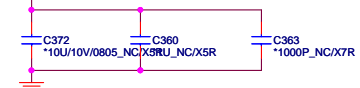
Bluetooth BTB Conn



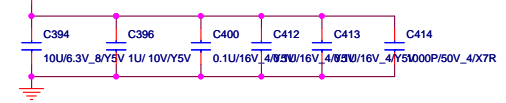
SATA Connector.



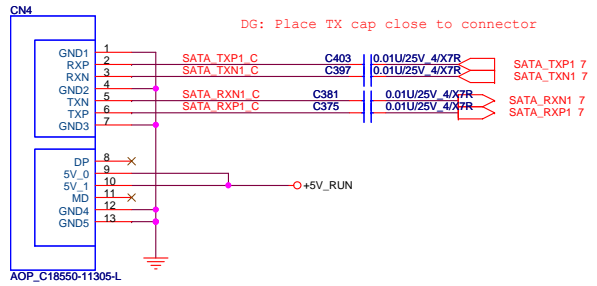
+3.3V_RUN Place caps close to connector.



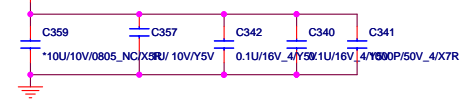
+5V_RUN Place caps close to connector.



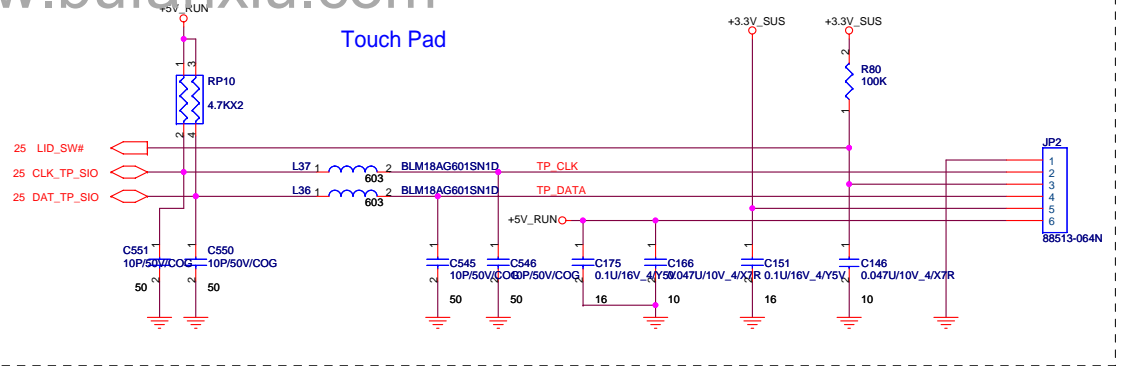
ODD Connector



+5V_RUN Place caps close to connector.

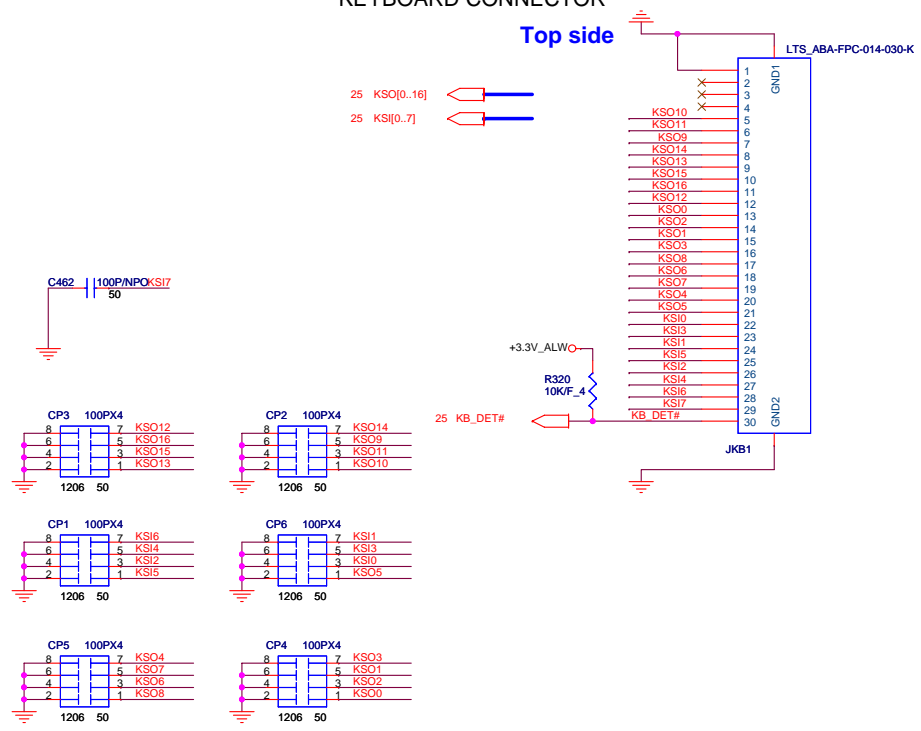


Touch Pad

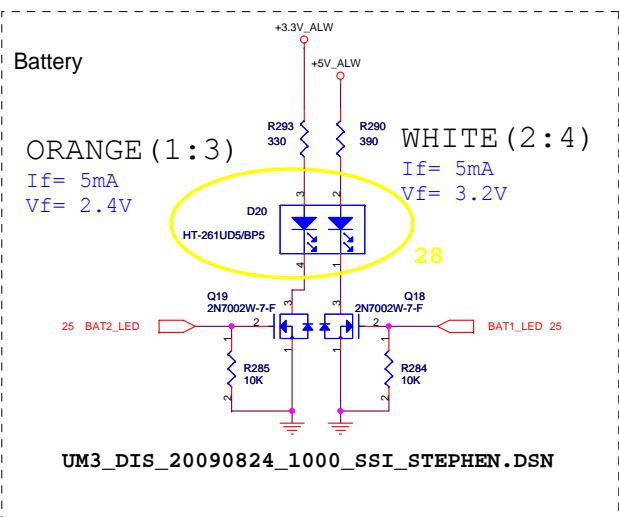
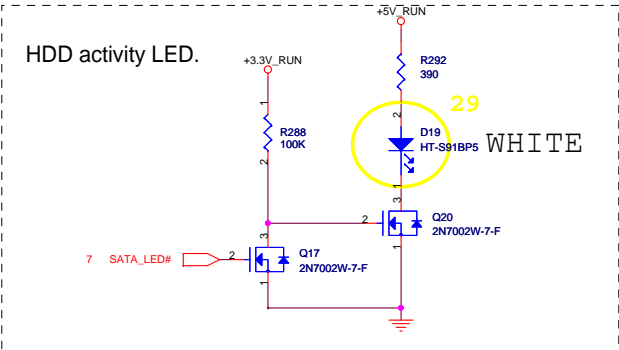
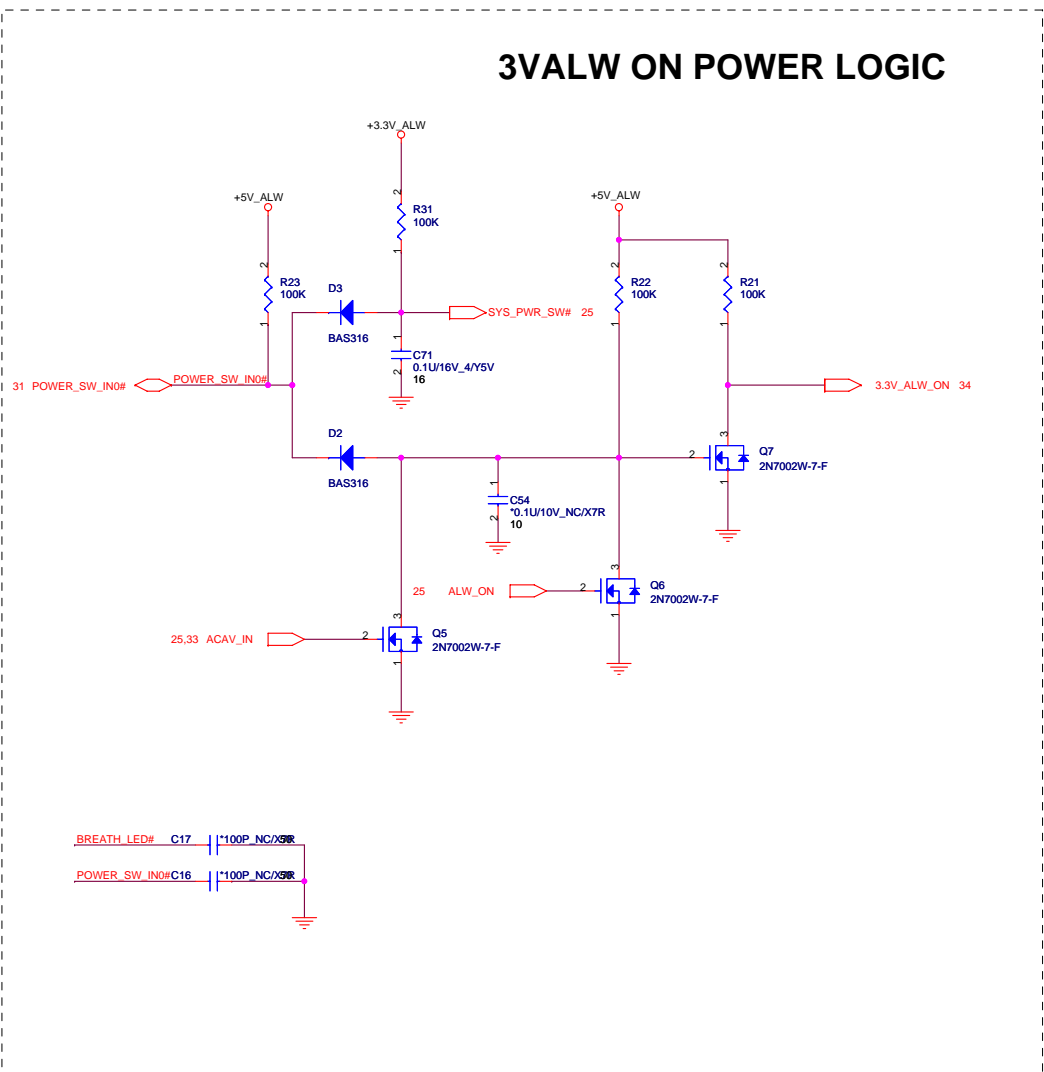
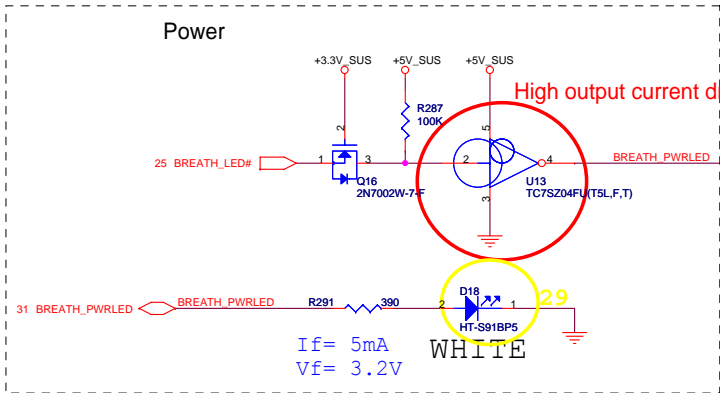


KEYBOARD CONNECTOR

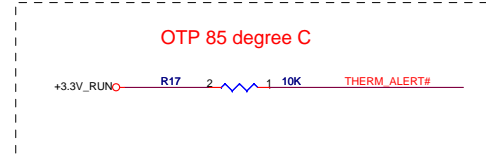
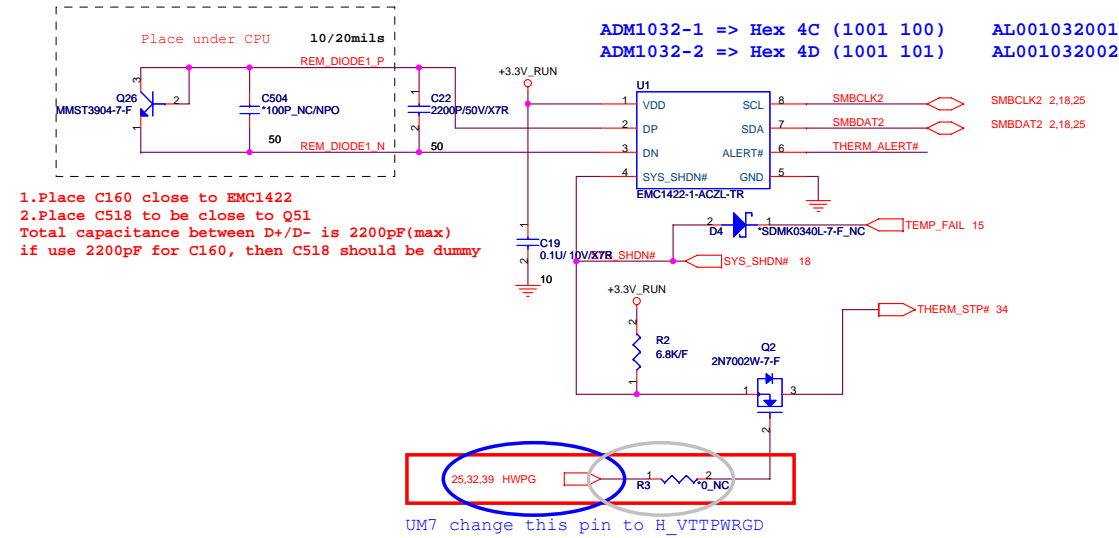
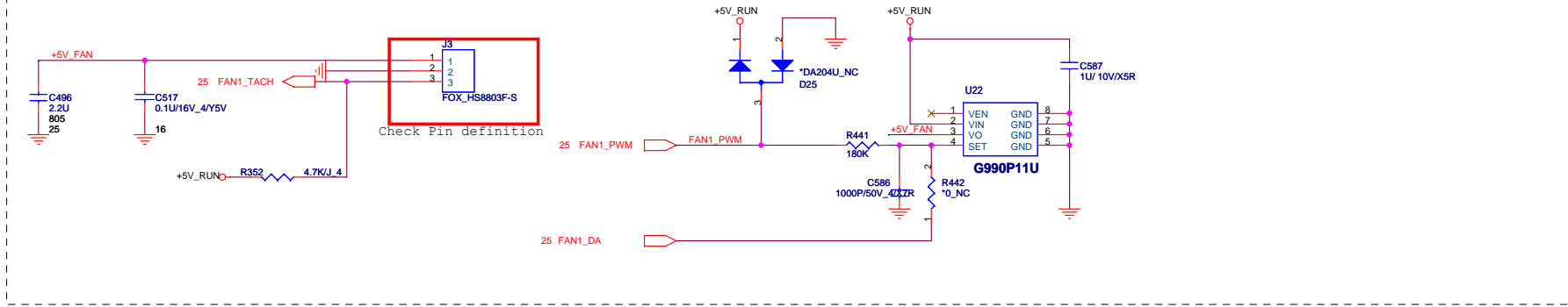
Top side



100P CAPS CLOSE TO JKB1

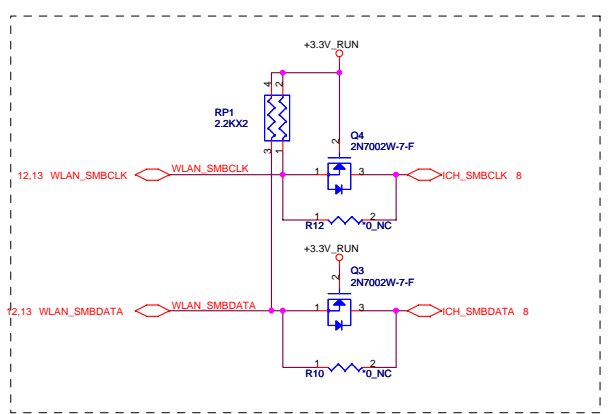
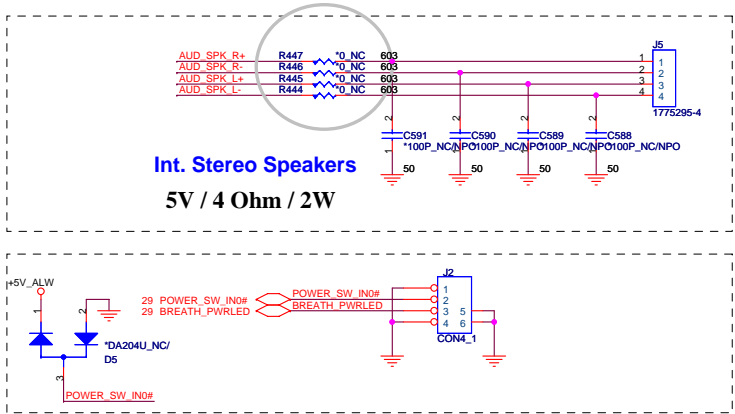
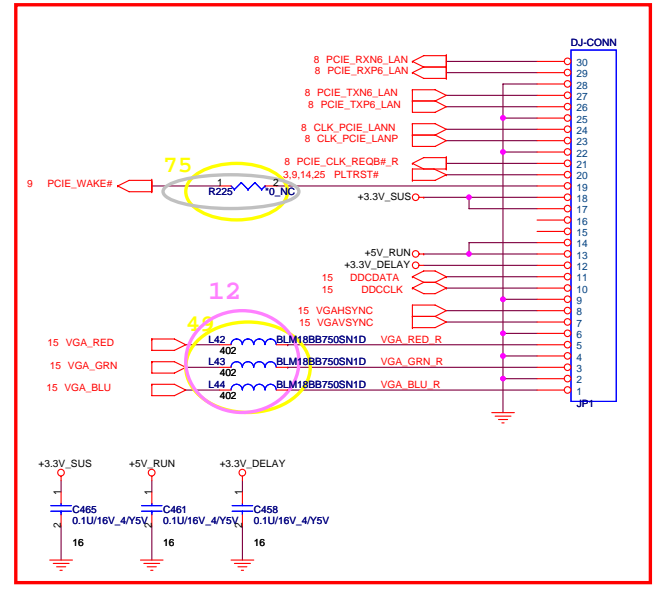
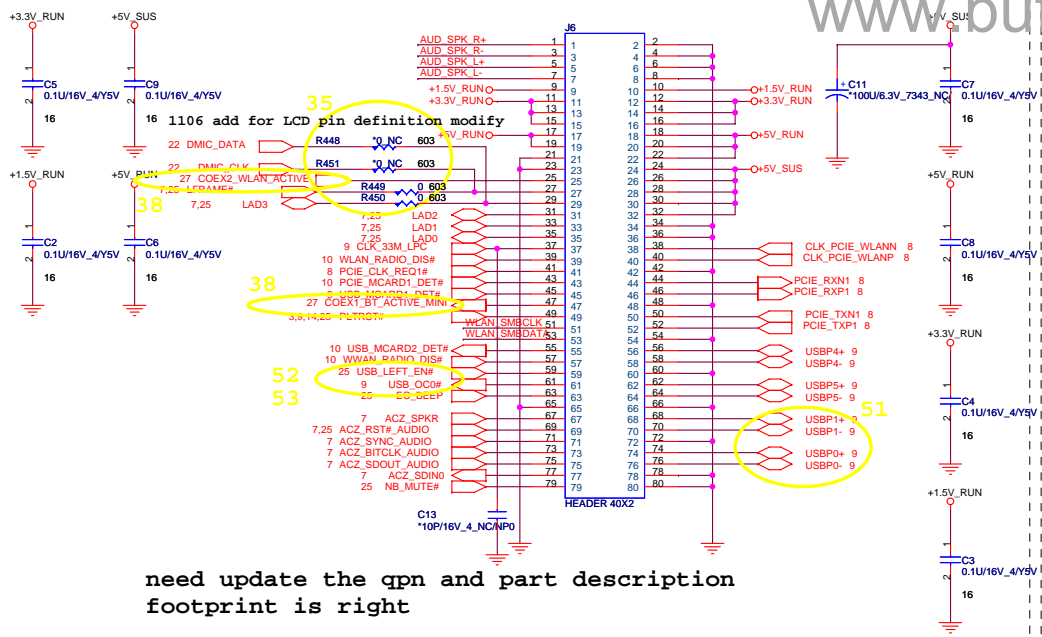


FAN CONTROL

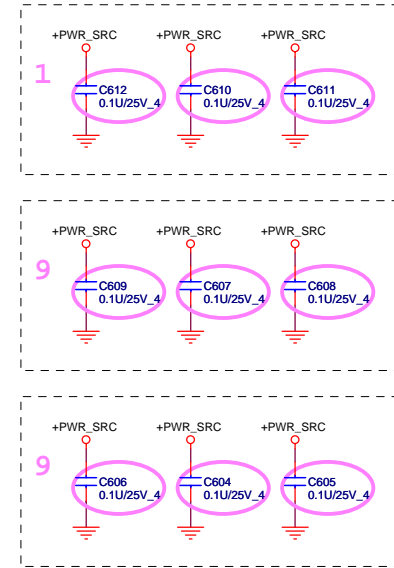
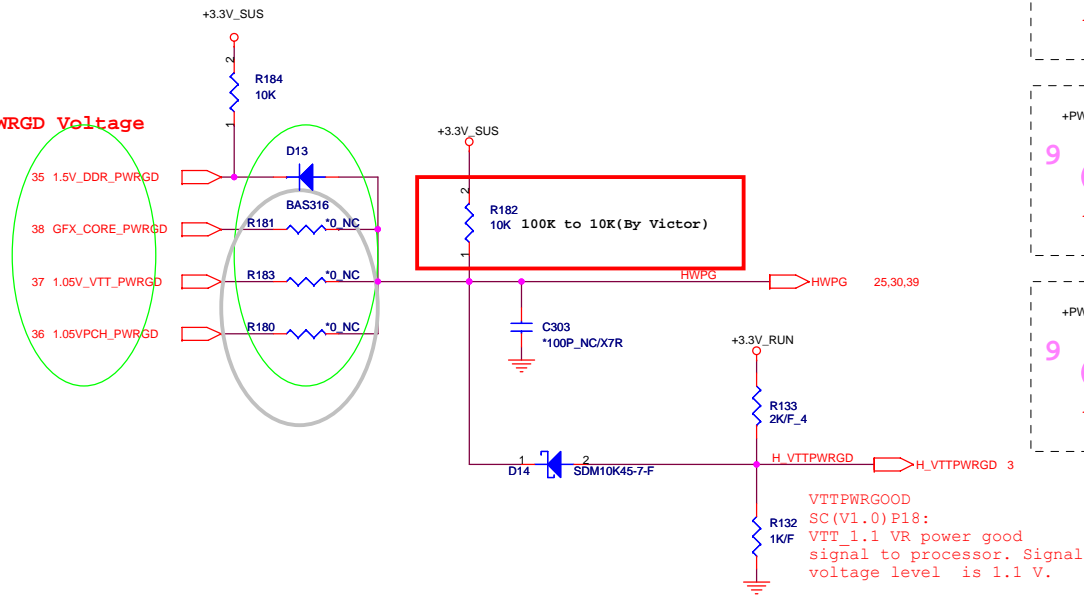


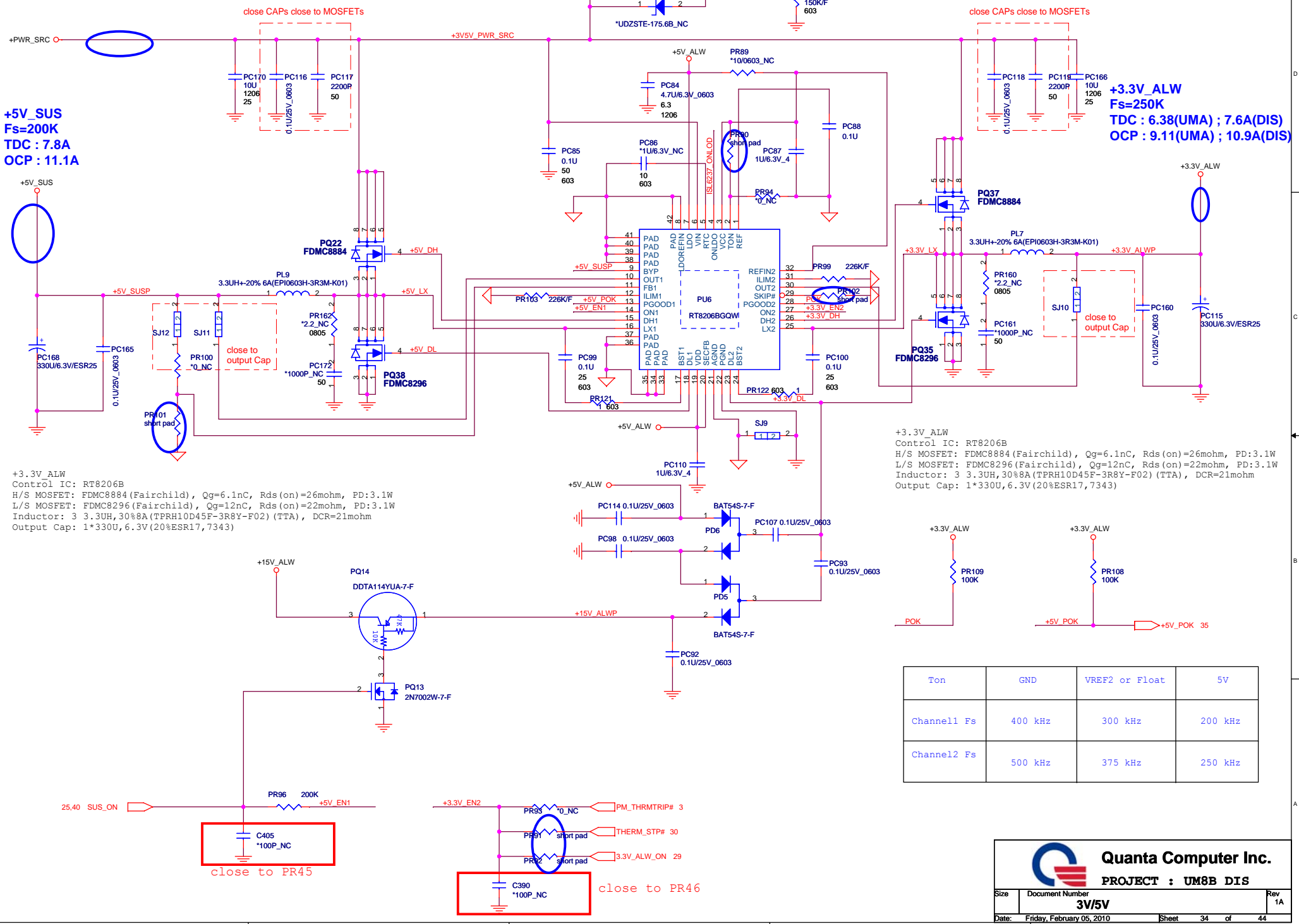
SYS_SHD# \ ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77°C	83°C	89°C	95°C	101°C	107°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C

Check I/N and footprint



Check PWRGD Voltage





+5V_SUS
Fs=200K
TDC : 7.8A
OCP : 11.1A

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17, 7343)

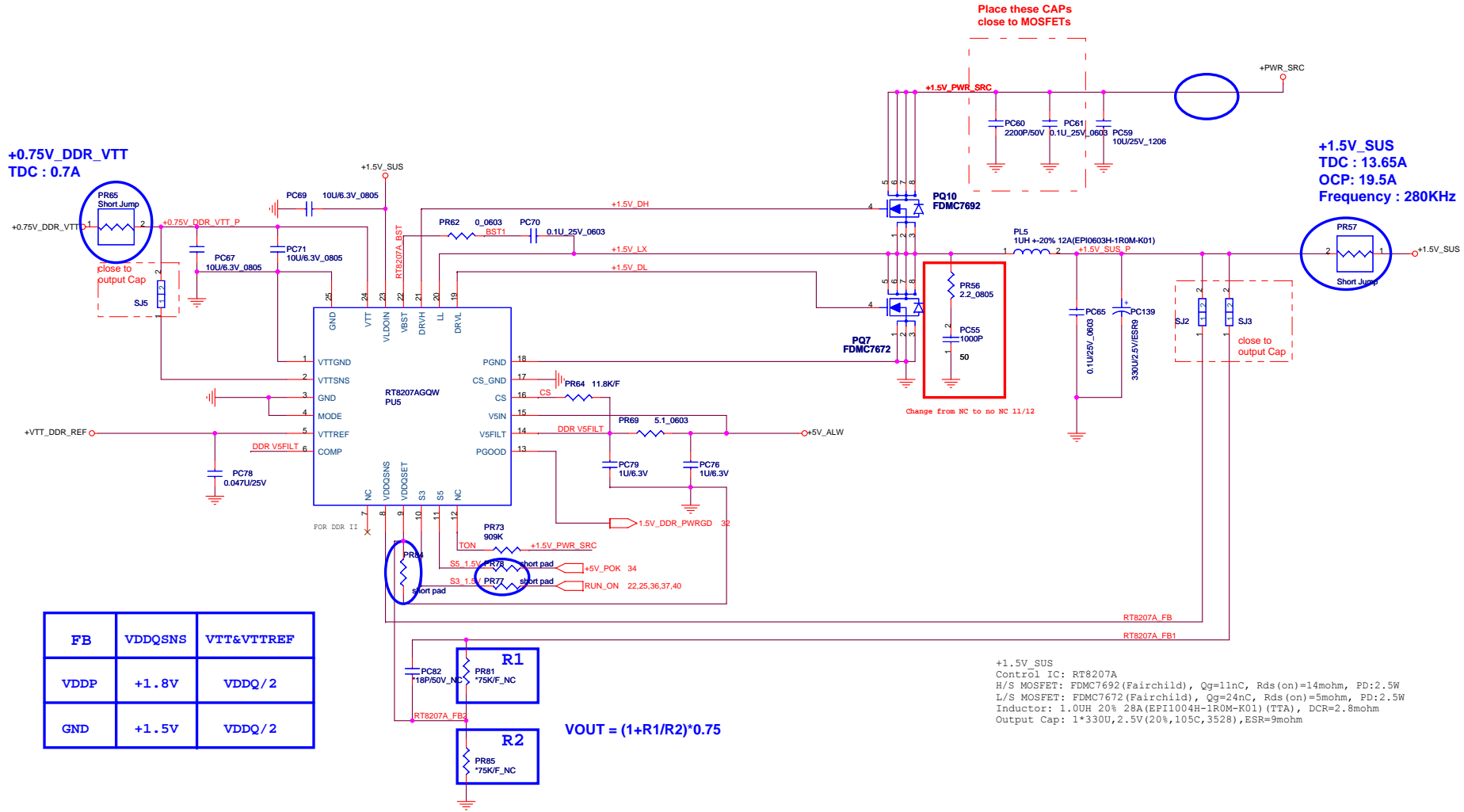
+3.3V_ALW
Fs=250K
TDC : 6.38(UMA) ; 7.6A(DIS)
OCP : 9.11(UMA) ; 10.9A(DIS)

+3.3V_ALW
Control IC: RT8206B
H/S MOSFET: FDMC8884 (Fairchild), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
L/S MOSFET: FDMC8296 (Fairchild), Qg=12nC, Rds(on)=22mohm, PD:3.1W
Inductor: 3 3.3UH, 30%8A (TPRH10D45F-3R8Y-F02) (TTA), DCR=21mohm
Output Cap: 1*330U, 6.3V (20%ESR17, 7343)

Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	300 kHz	200 kHz
Channel2 Fs	500 kHz	375 kHz	250 kHz

Quanta Computer Inc.
PROJECT : UM8B DIS

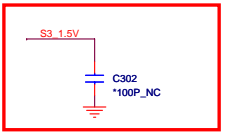
Size	Document Number	Rev
	3V/5V	1A
Date:	Friday, February 05, 2010	Sheet 34 of 44



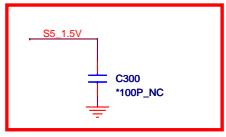
FB	VDDQNS	VTT&VTTREF
VDDP	+1.8V	VDDQ/2
GND	+1.5V	VDDQ/2

$V_{OUT} = (1+R1/R2) \cdot 0.75$

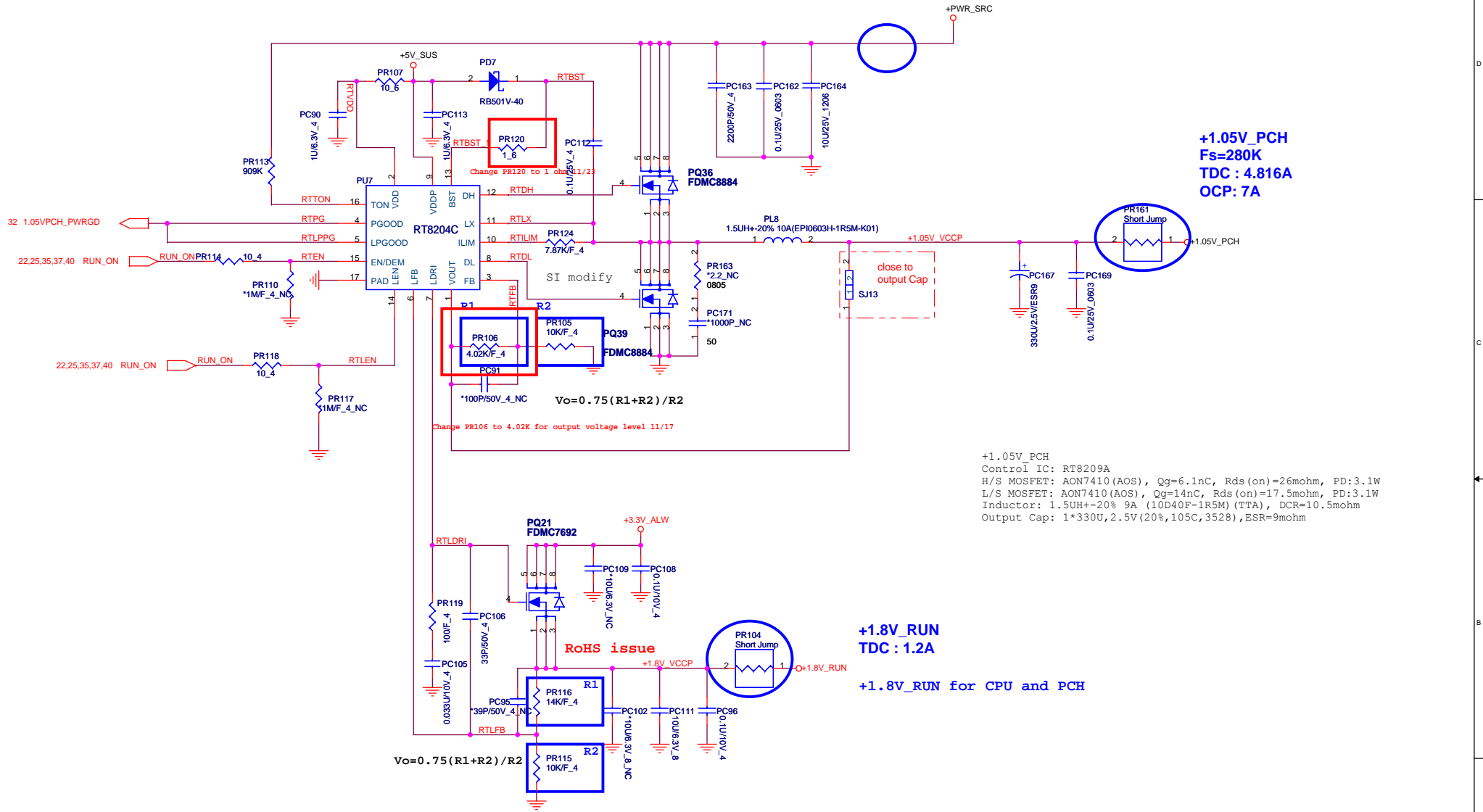
+1.5V_SUS
 Control IC: RT8207A
 H/S MOSFET: FDMC7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDMC7672 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
 Inductor: 1.0UH 20% 28A (EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
 Output Cap: 1*330U, 2.5V (20%, 105C, 3528), ESR=9mohm

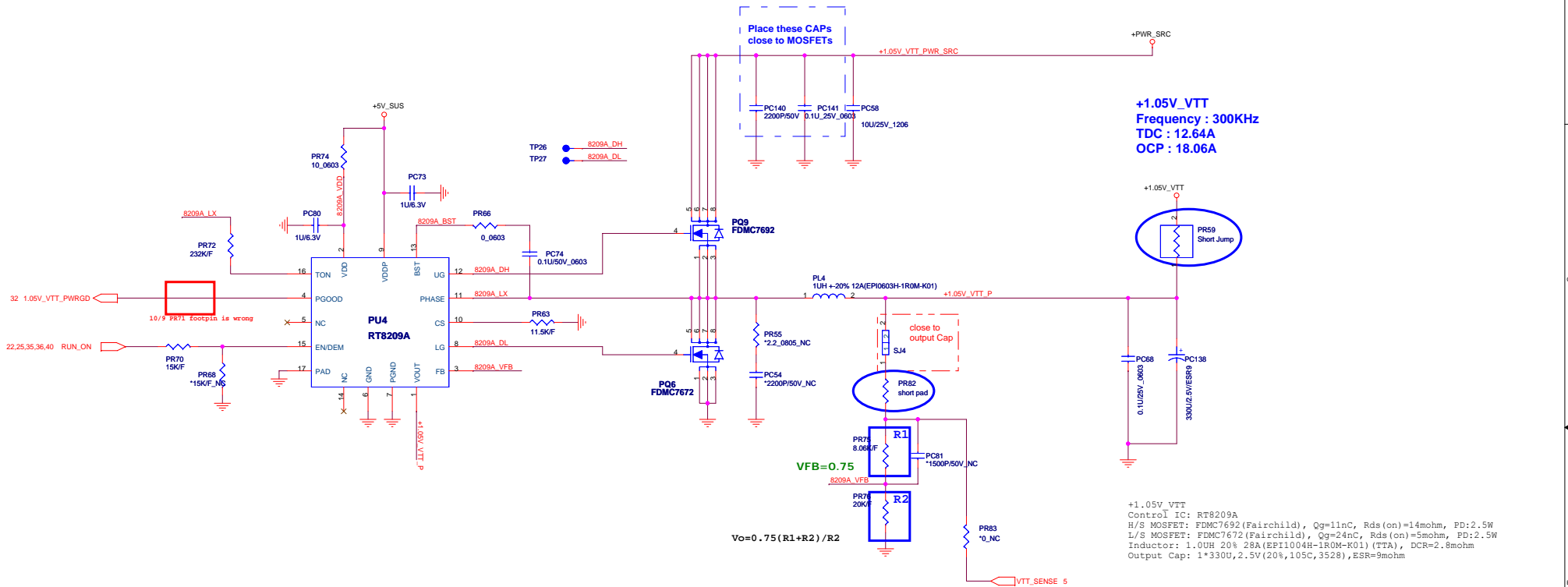


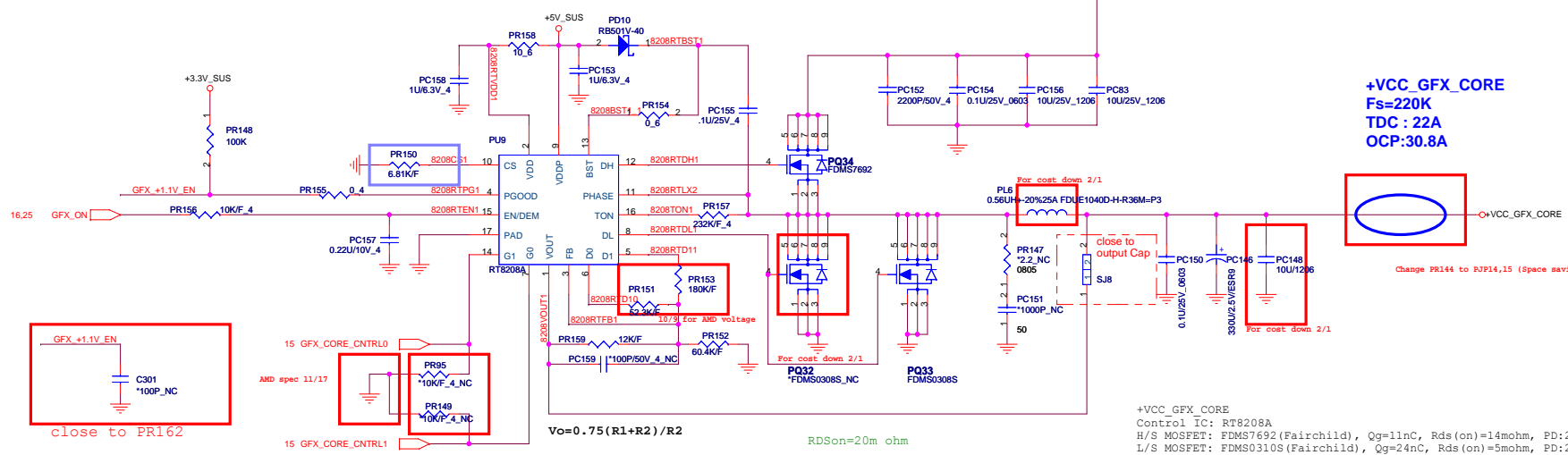
close to PR56



close to PR55







+VCC_GFX_CORE
 Fs=220K
 TDC : 22A
 OCP:30.8A

$V_o = 0.75 (R1+R2) / R2$

RDSon=20m ohm

+VCC_GFX_CORE
 Control IC: RT8208A
 H/S MOSFET: FDMC7692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDMC308S (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
 Inductor: 0.36UH 20% 28A (EPI1004H-1R0M-K01) (TTA), DCR=2.8mohm
 Output Cap: 2*330U, 2.5V (20%, 105C, 3528), ESR=9mohm

+VCC_GFX_CORE_M92

For M96-LP:

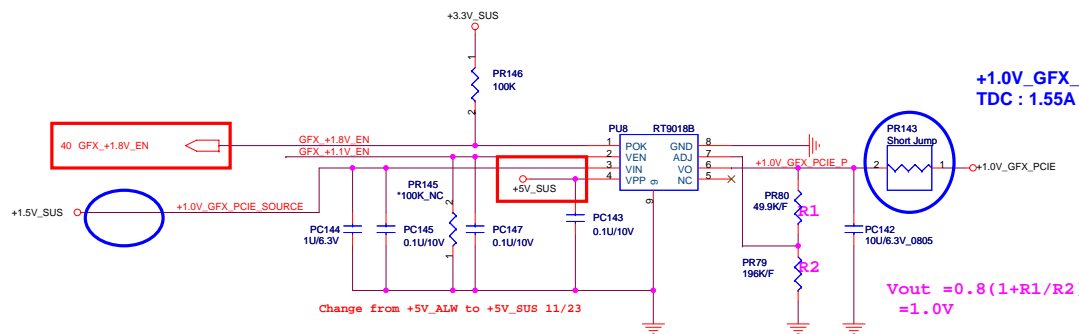
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.0V
HIGH	HIGH	1.05V(N/A)

For Park-XT:

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
LOW	HIGH	1.07V(N/A)
HIGH	HIGH	1.12V

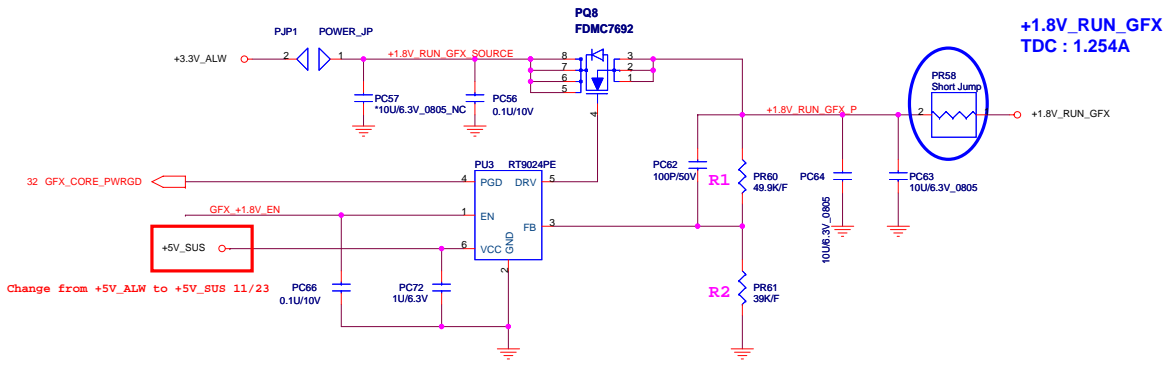
Change List:

For Park-XT:	For M96-LP:
PR151:52.3K	PR151:90.9K
PN:CS35232FB10	PN:CS39092FB11
PR79:196K	PR79:133K
PN:CS41962FB01	PN:CS41332FB06

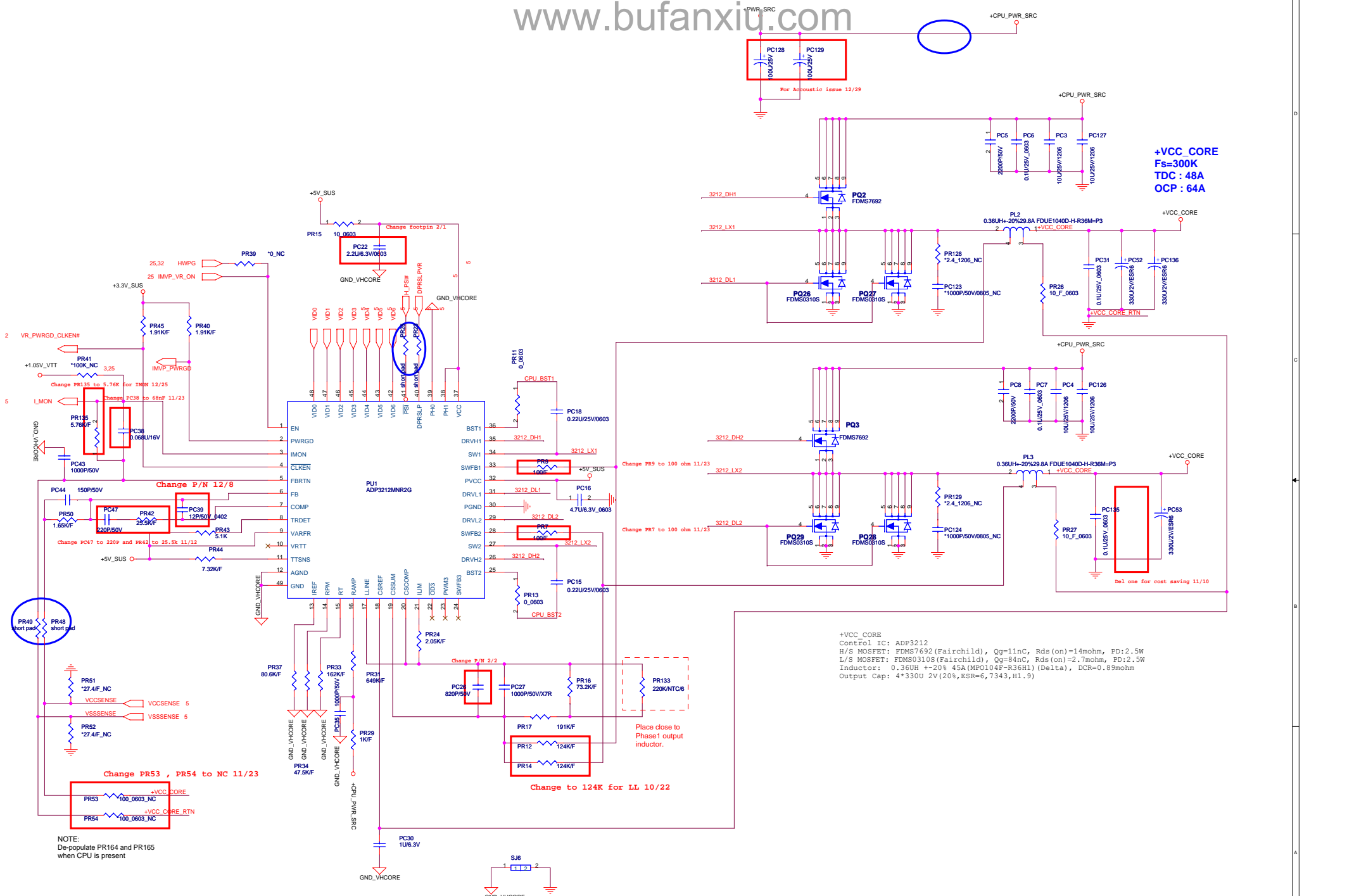


+1.0V_GFX_PCIE
 TDC : 1.55A

$V_{out} = 0.8(1+R1/R2) = 1.0V$

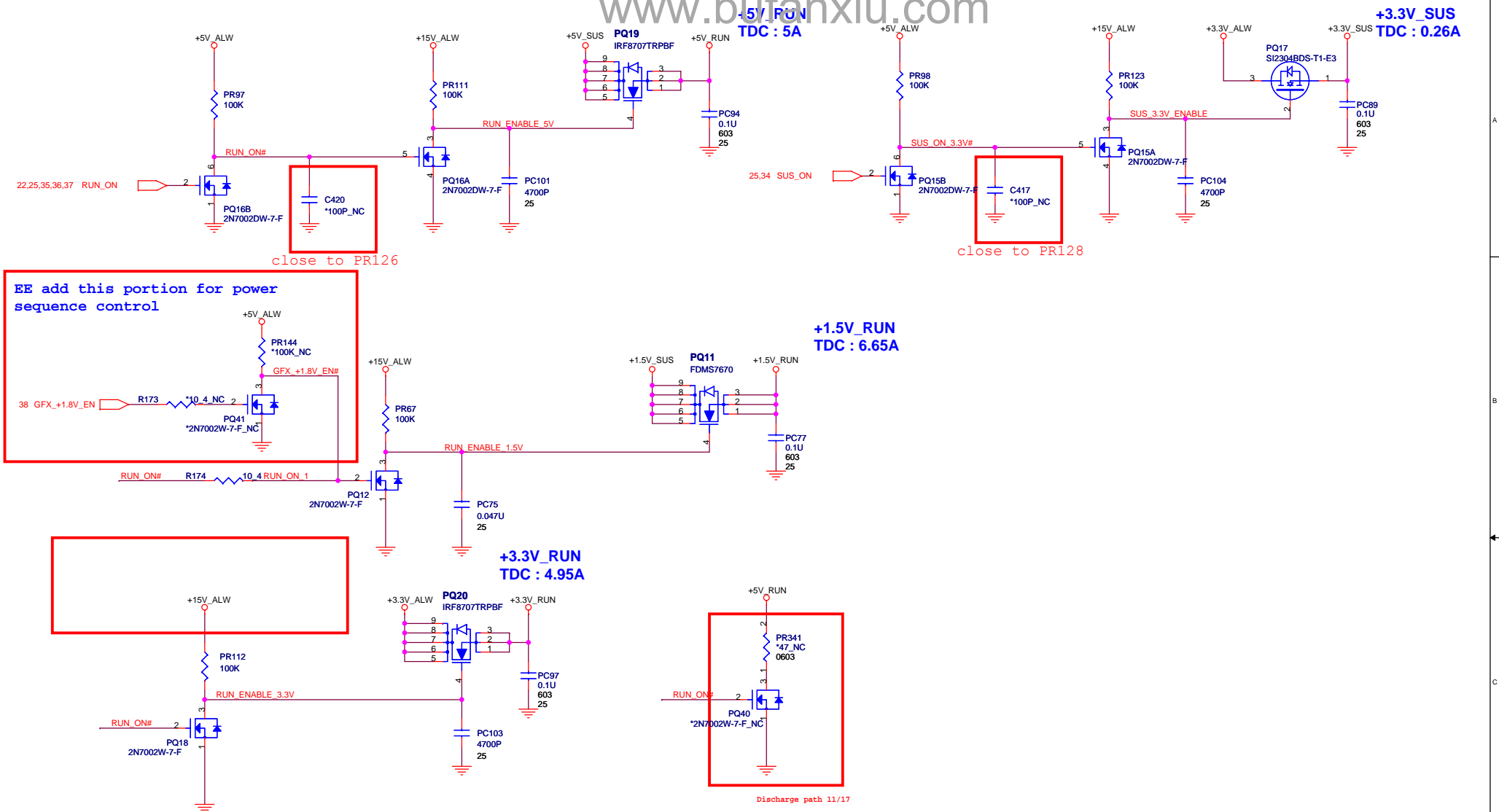


+1.8V_RUN_GFX
 TDC : 1.254A



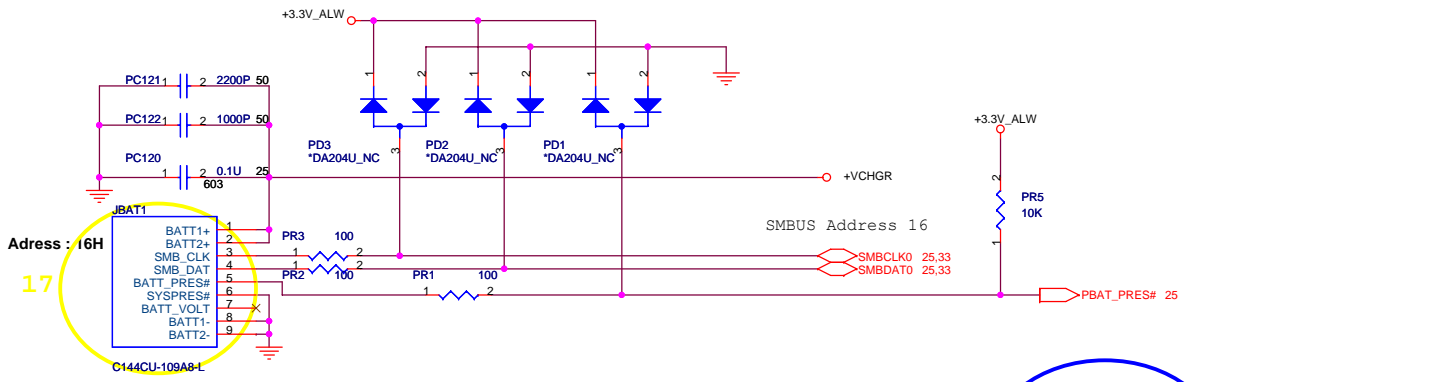
+VCC_CORE
Fs=300K
TDC : 48A
OCp : 64A

+VCC_CORE
 Control IC: ADP3212
 H/S MOSFET: FDM57692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDM50310S (Fairchild), Qg=84nC, Rds(on)=2.7mohm, PD:2.5W
 Inductor: 0.36uH +/-20% 45A (MPO104F-R36H1) (Delta), DCR=0.89mohm
 Output Cap: 4*330u 2V (20%, ESR=6,7343,H1.9)

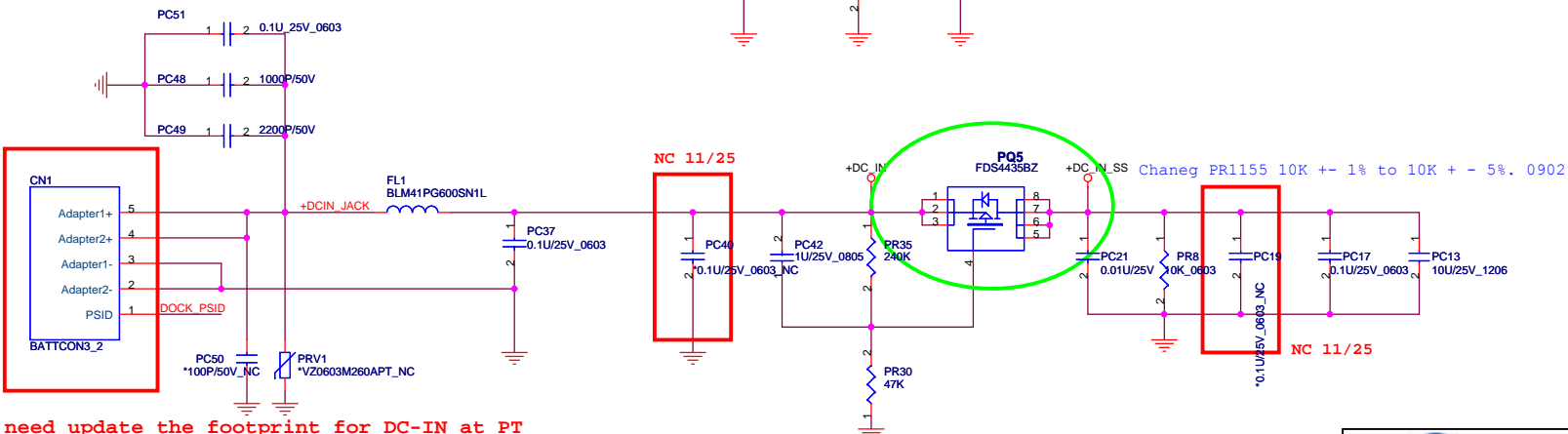
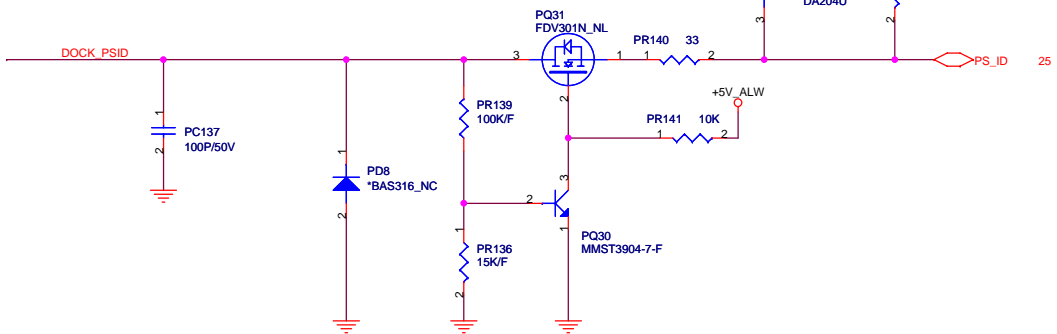
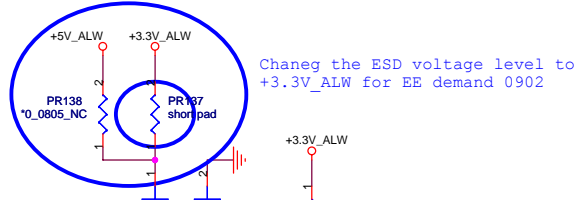


EE add this portion for power sequence control

[Redacted area]



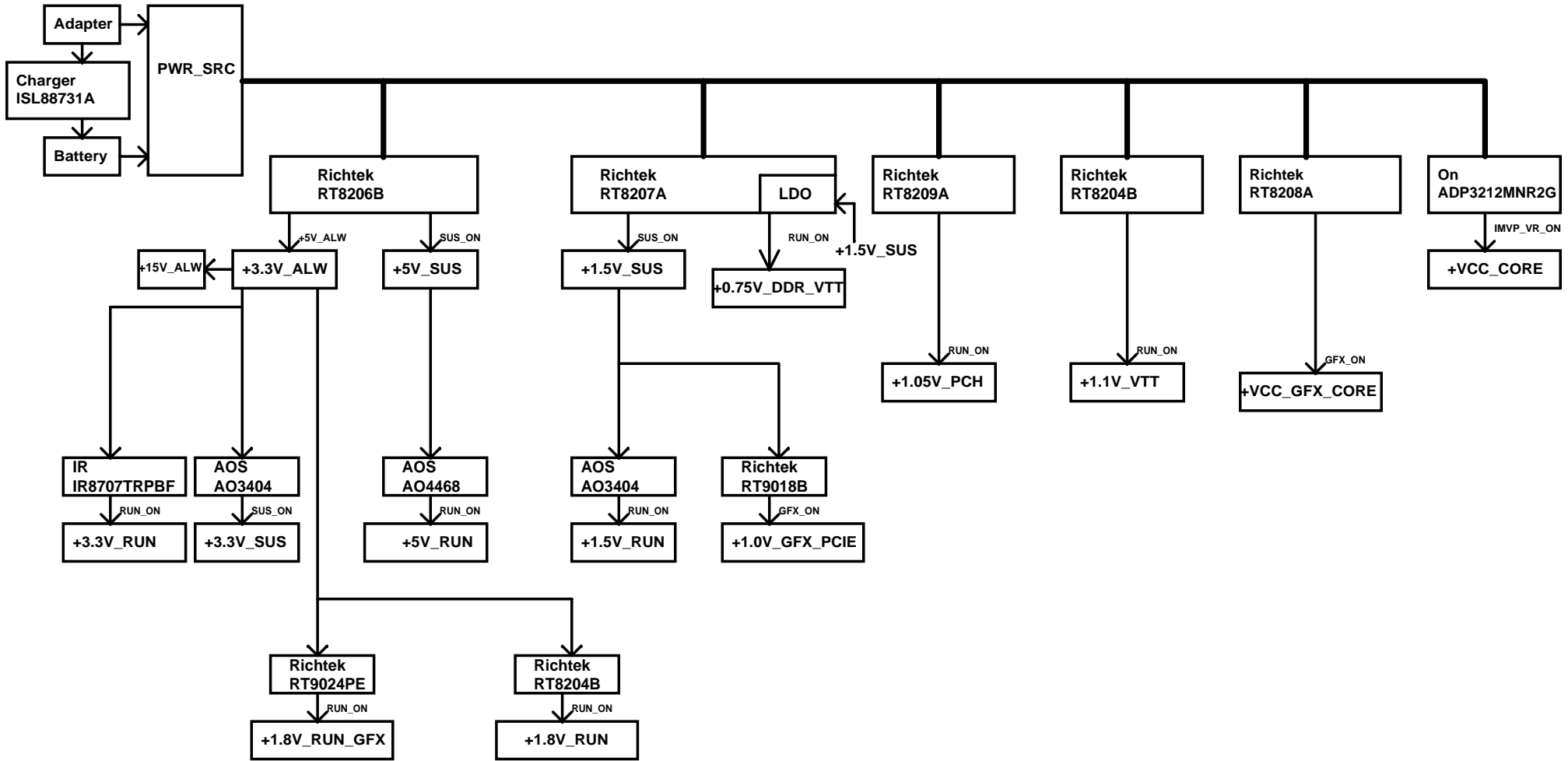
Adress : 16H
17

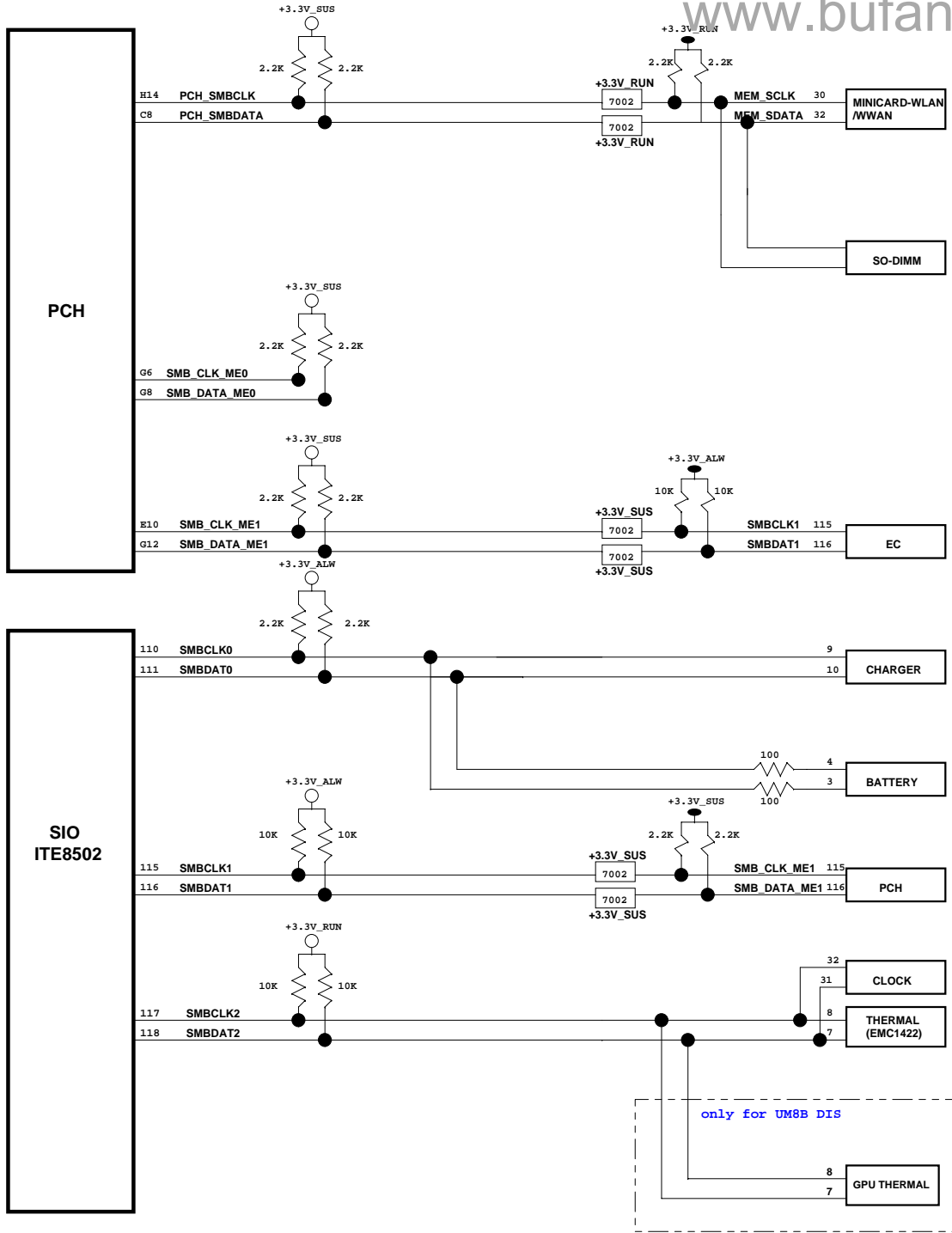


need update the footprint for DC-IN at PT

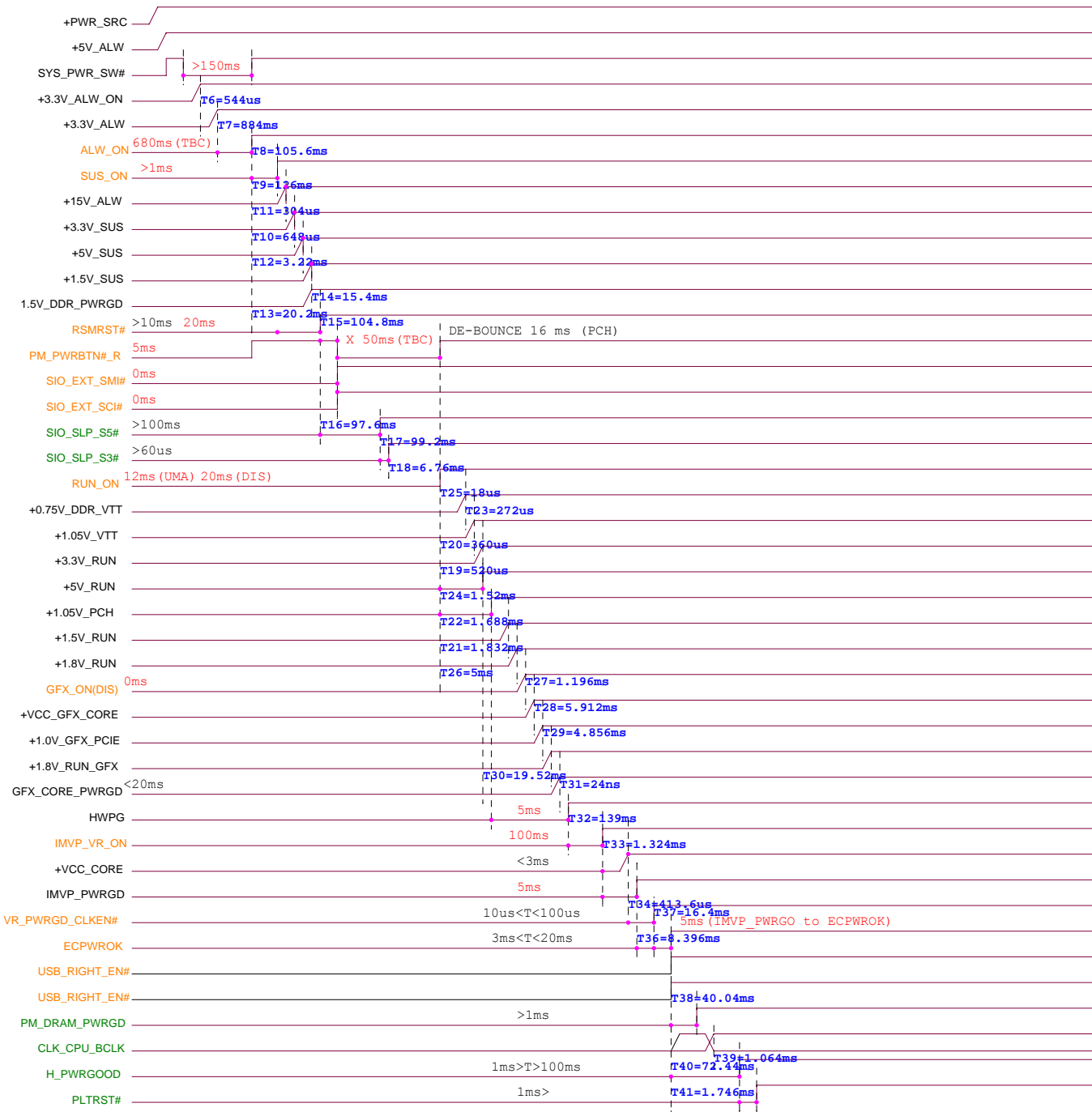
Quanta Computer Inc.
PROJECT : UM8B DIS

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	Batt & DC-IN	1A
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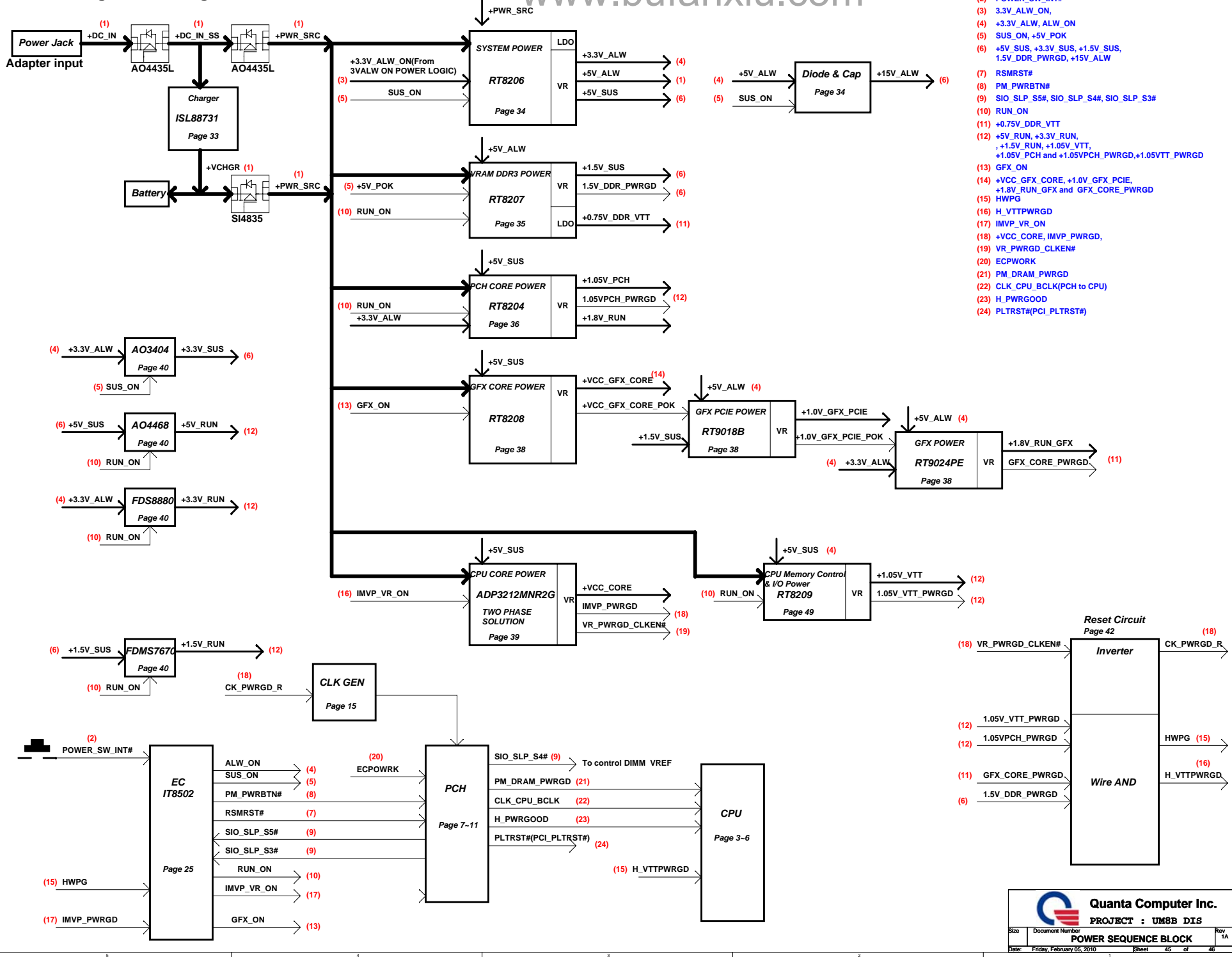




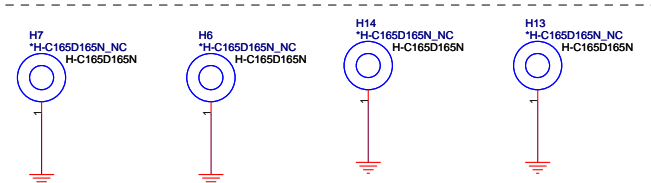
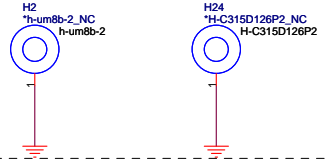
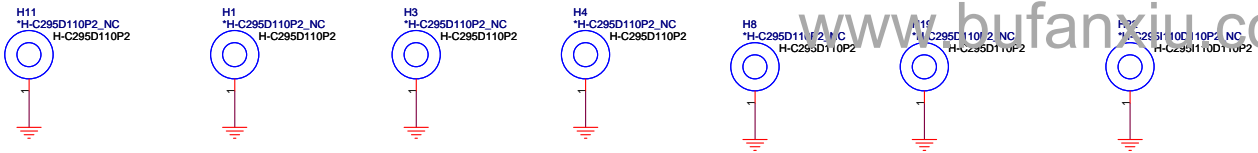
UM8B_X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)



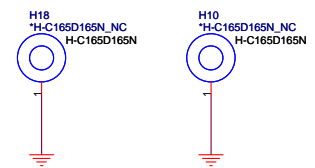
Power Design Block Diagram



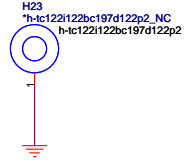
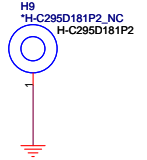
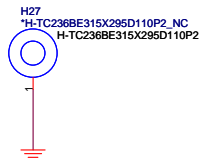
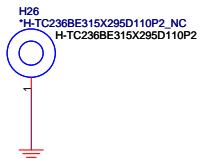
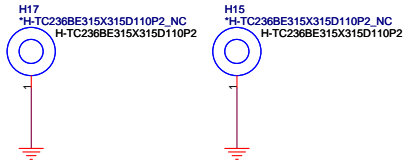
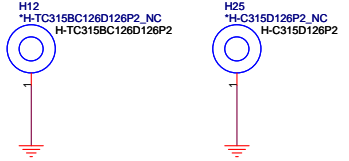
- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- Bat : +VCHGR -> +PWR_SRC, +5V_ALW
- (2) POWER_SW_INT#
- (3) 3.3V_ALW_ON,
- (4) +3.3V_ALW, ALW_ON
- (5) SUS_ON, +5V_POK
- (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD, +15V_ALW
- (7) RSMRST#
- (8) PM_PWRBTN#
- (9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (10) RUN_ON
- (11) +0.75V_DDR_VTT
- (12) +5V_RUN, +3.3V_RUN, +1.5V_RUN, +1.05V_VTT, +1.05V_PCH and +1.05VPCH_PWRGD, +1.05VTT_PWRGD
- (13) GFX_ON
- (14) +VCC_GFX_CORE, +1.0V_GFX_PCIE, +1.8V_RUN_GFX and GFX_CORE_PWRGD
- (15) HWPG
- (16) H_VTTPWRGD
- (17) IMVP_VR_ON
- (18) +VCC_CORE, IMVP_PWRGD,
- (19) VR_PWRGD_CLKEN#
- (20) ECPWORK
- (21) PM_DRAM_PWRGD
- (22) CLK_CPU_BCLK(PCH to CPU)
- (23) H_PWRGOOD
- (24) PLTRST#(PCI_PLTRST#)



CPU

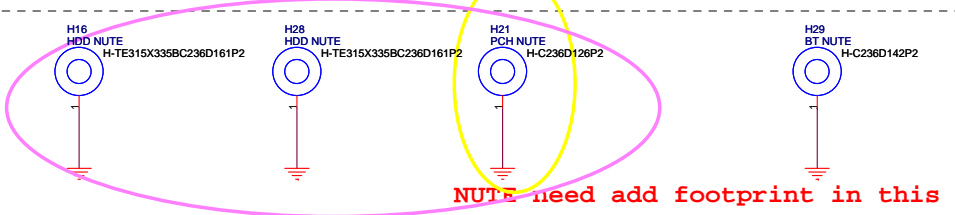


VGA



6, 7

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NUTE need add footprint in this

UM8B_ X00 Power On Timing(BATTERY MODE BY SOFTWARE SETUP, W/O ADAPTOR)

