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Schematic Document

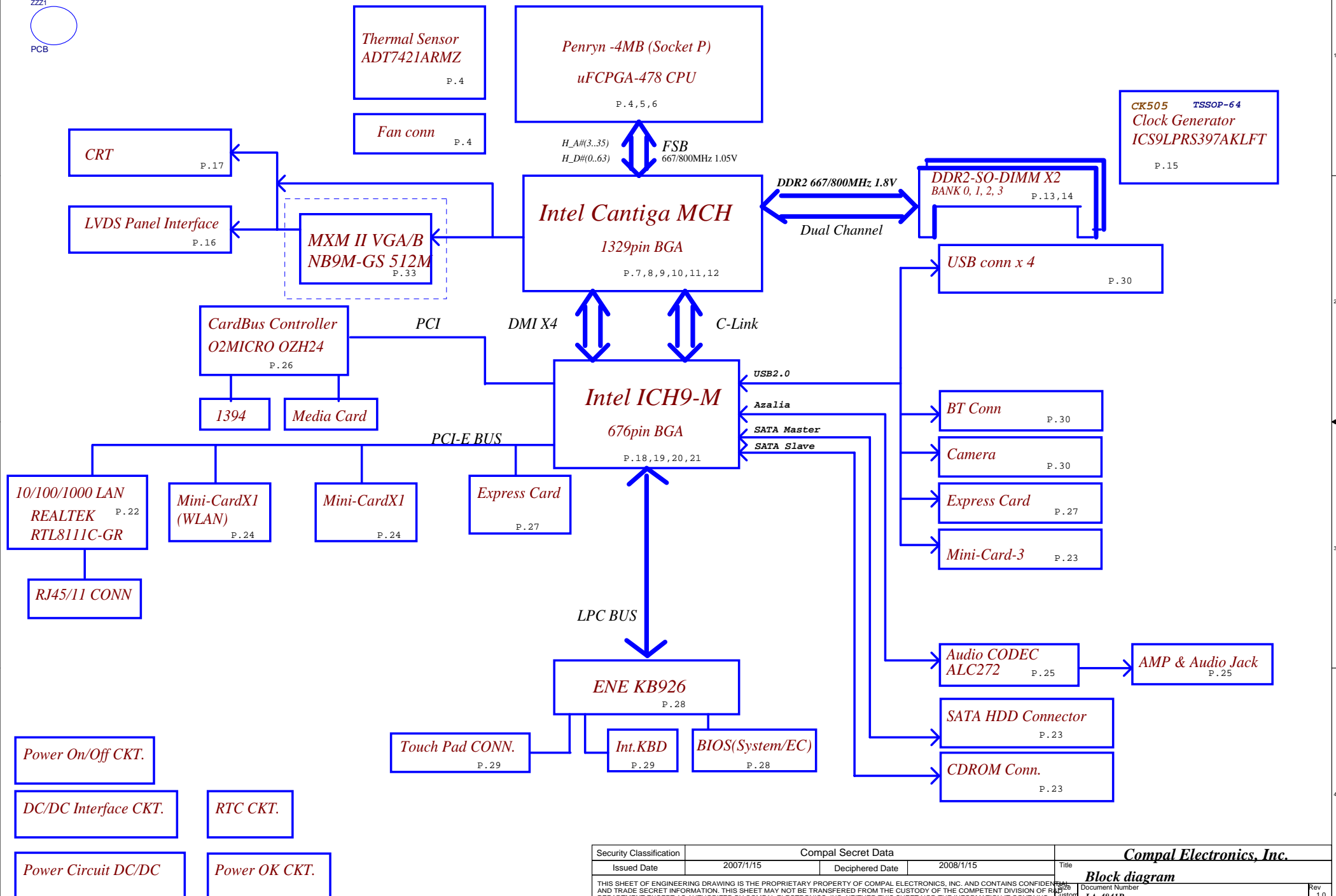
Cantiga + ICH9

2008 / 12 / 10 Rev:1.0

Security Classification	Compal Secret Data		Title		<i>Compal Electronics, Inc.</i>	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Part		Rev
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				Document Number	LA-4841P	

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PCB



Security Classification	Compal Secret Data		Title	
Issued Date	2007/1/15	Deciphered Date	2008/1/15	Block diagram
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power plane State	+B	+5VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE
		+3VALW		+VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

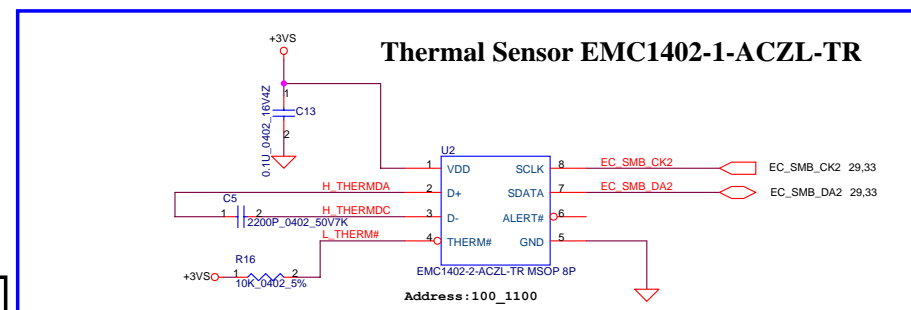
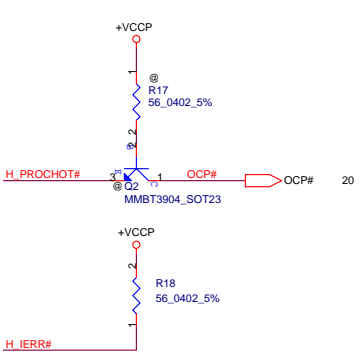
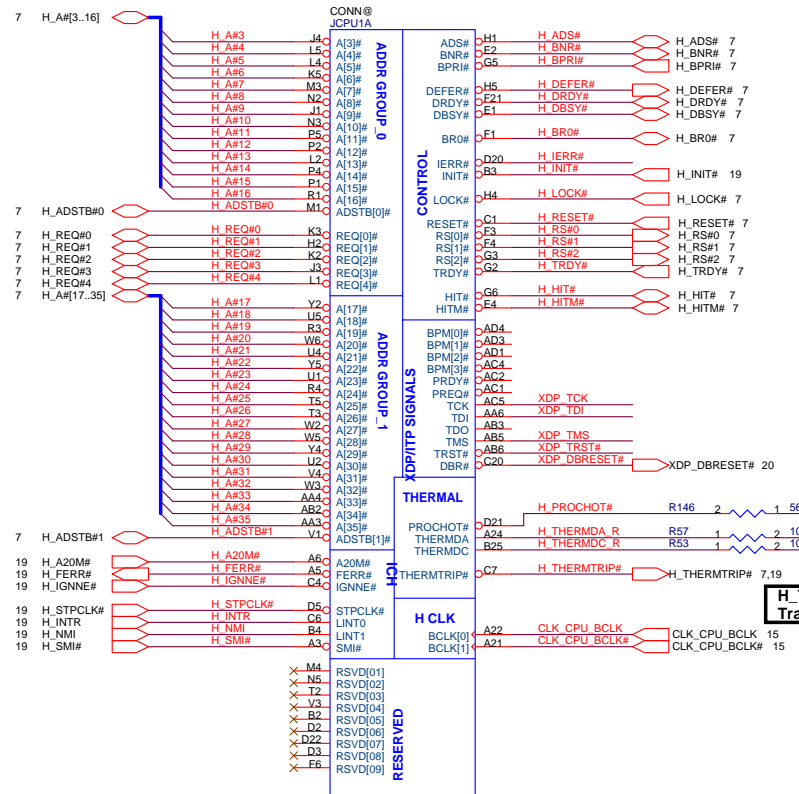
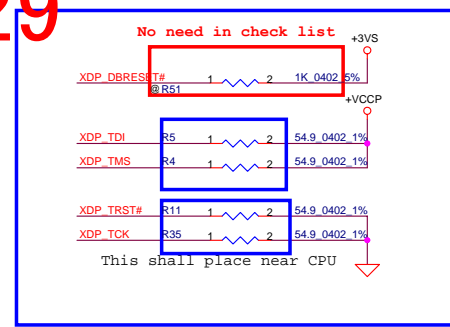
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

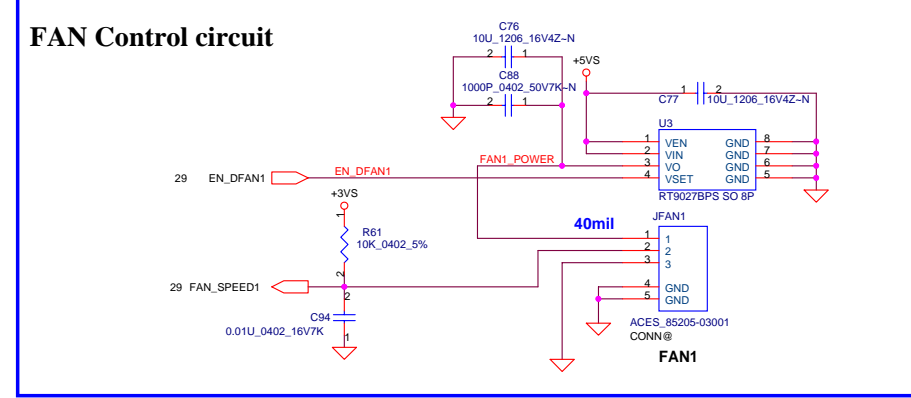
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

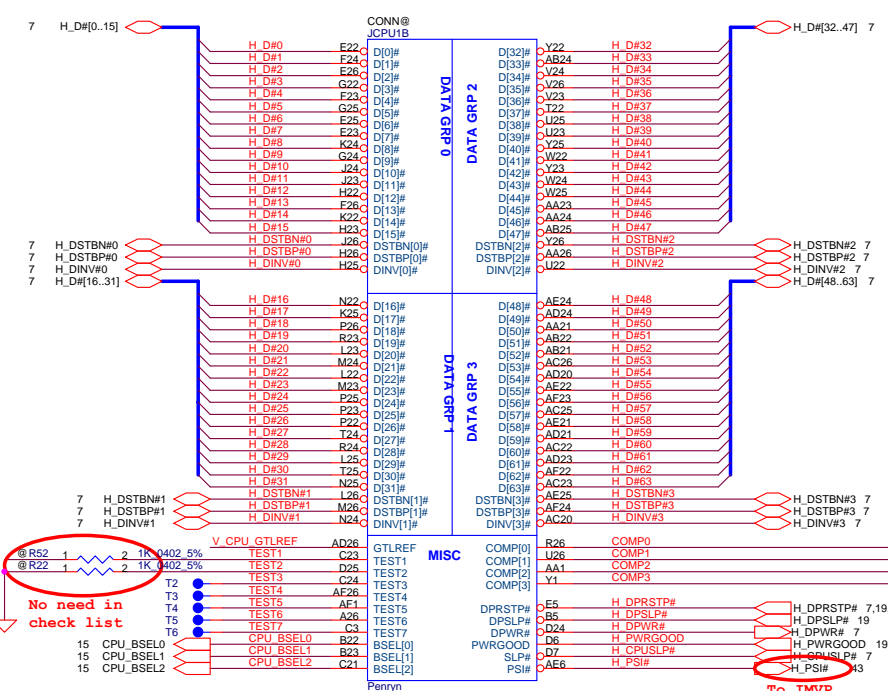
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Notes List		
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H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



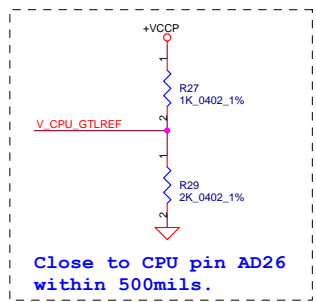
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No need in check list

layout note: Rout H DPRSTP# from ICH9 to IMPV6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

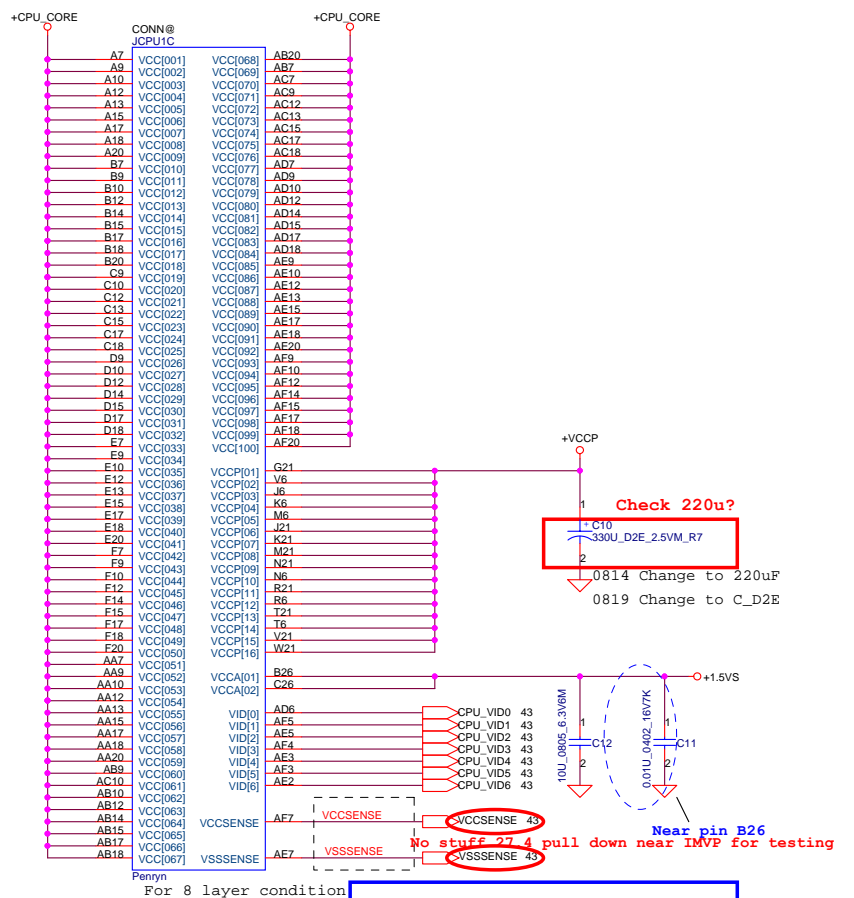
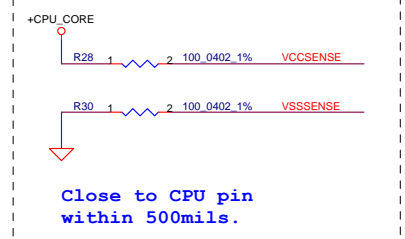
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4

For 6 layer
 $Z=27.4 \text{ ohm}$
 VCCSENSE, VSSSENSE/ 14mils (MS), 16mils (SL) width, 7mils space, 25mils space to other signals Mismatch =25mils.

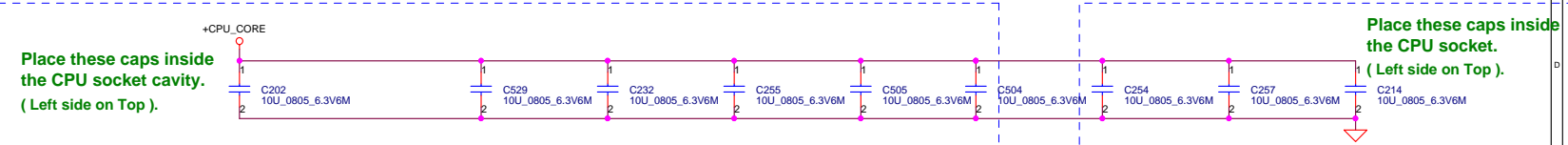
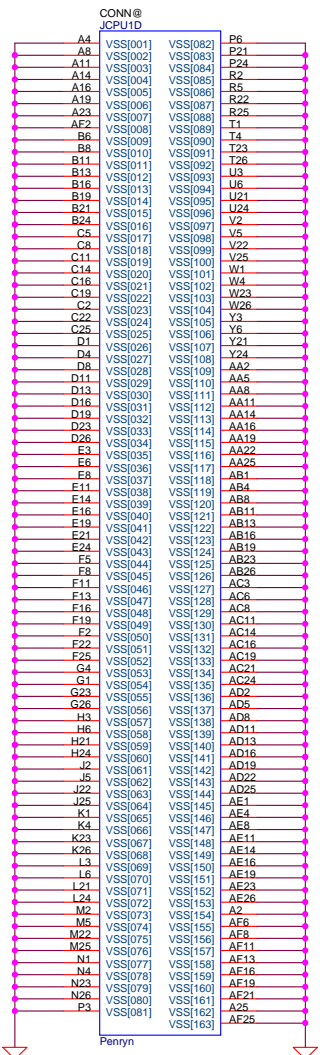
Length match within 25 mils. The trace width/space/other is 20/7/25.



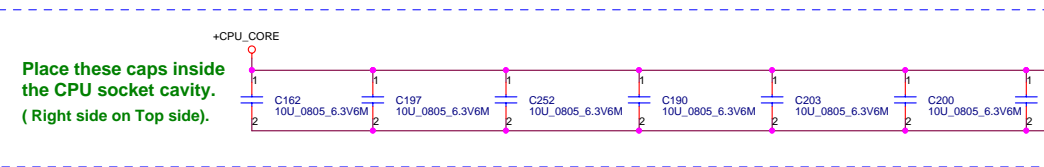
Check 220u?
 330u D2E_2.5VM_R7
 0814 Change to 220uF
 0819 Change to C_D2E

No stuff 27.4 pull down near IMVP for testing

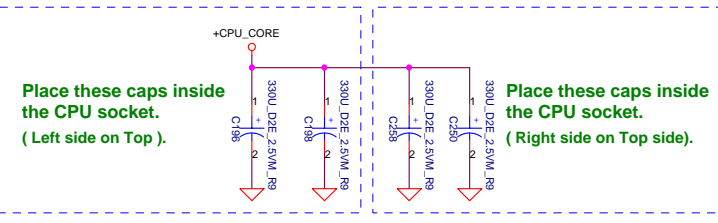
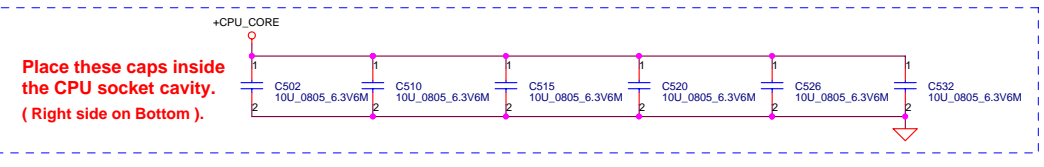
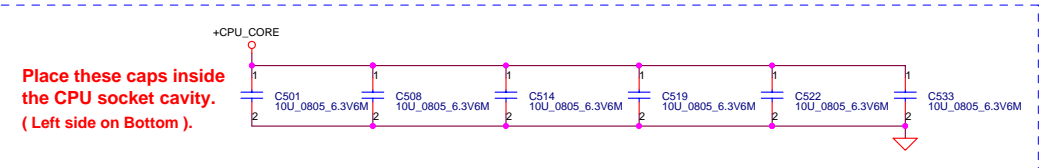
High Frequency Decoupling
10uF 0805 X5R -> 85 degree.



Place these caps inside the CPU socket. (Left side on Top).

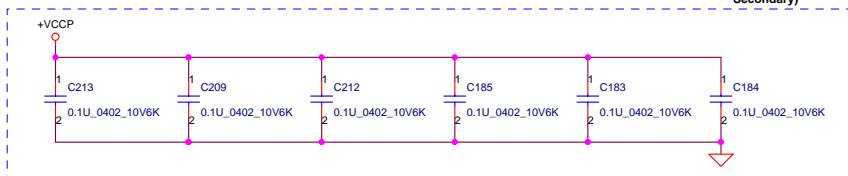


Place these caps inside the CPU socket. (Right side on Top).

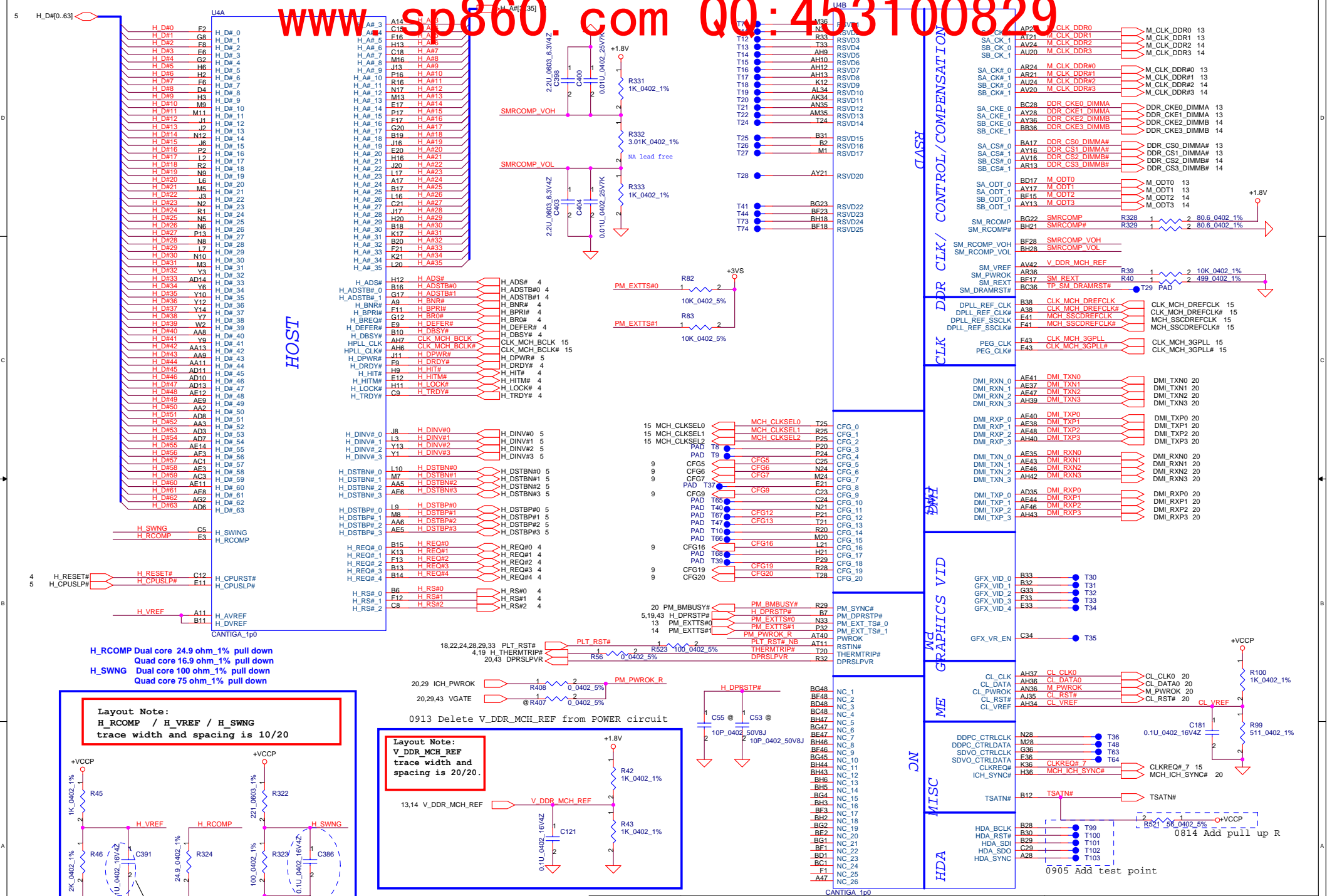


ESR <= 1.5m ohm
Capacitor > 880 uF

Place these inside socket cavity on L8 (North side Secondary)

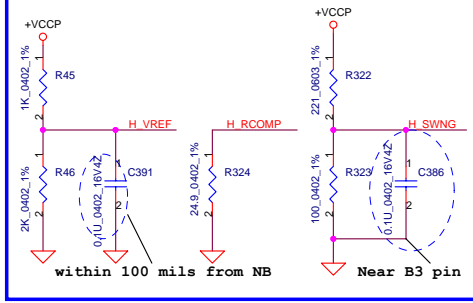


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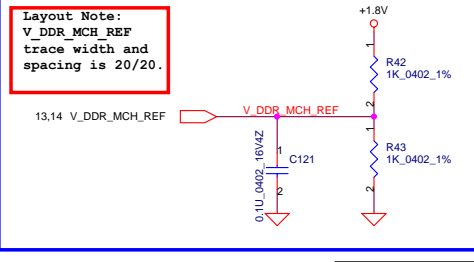


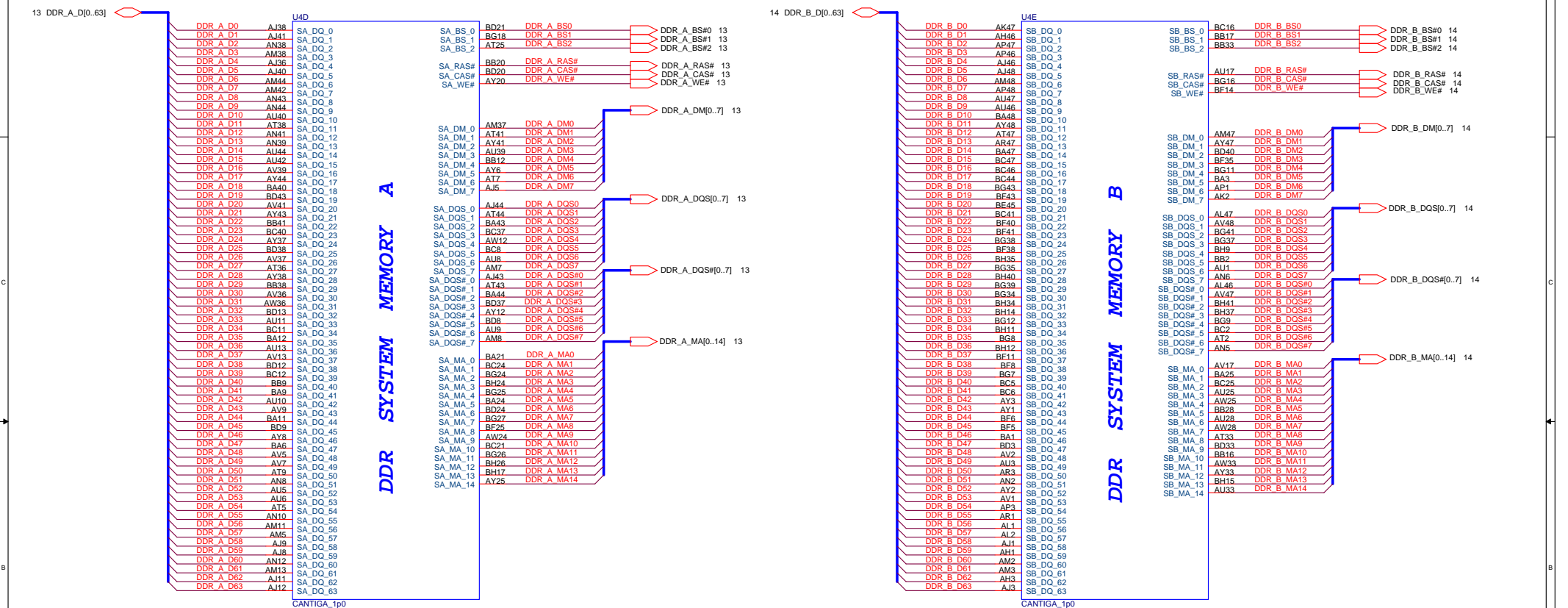
H_RCOMP Dual core 24.9 ohm_1% pull down
 Quad core 16.9 ohm_1% pull down
 H_SWNG Dual core 100 ohm_1% pull down
 Quad core 75 ohm_1% pull down

Layout Note:
 H_RCOMP / H_VREF / H_SWNG
 trace width and spacing is 10/20



Layout Note:
 V_DDR_MCH_REF
 trace width and spacing is 20/20.





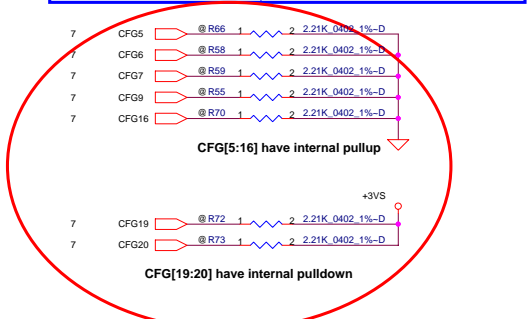
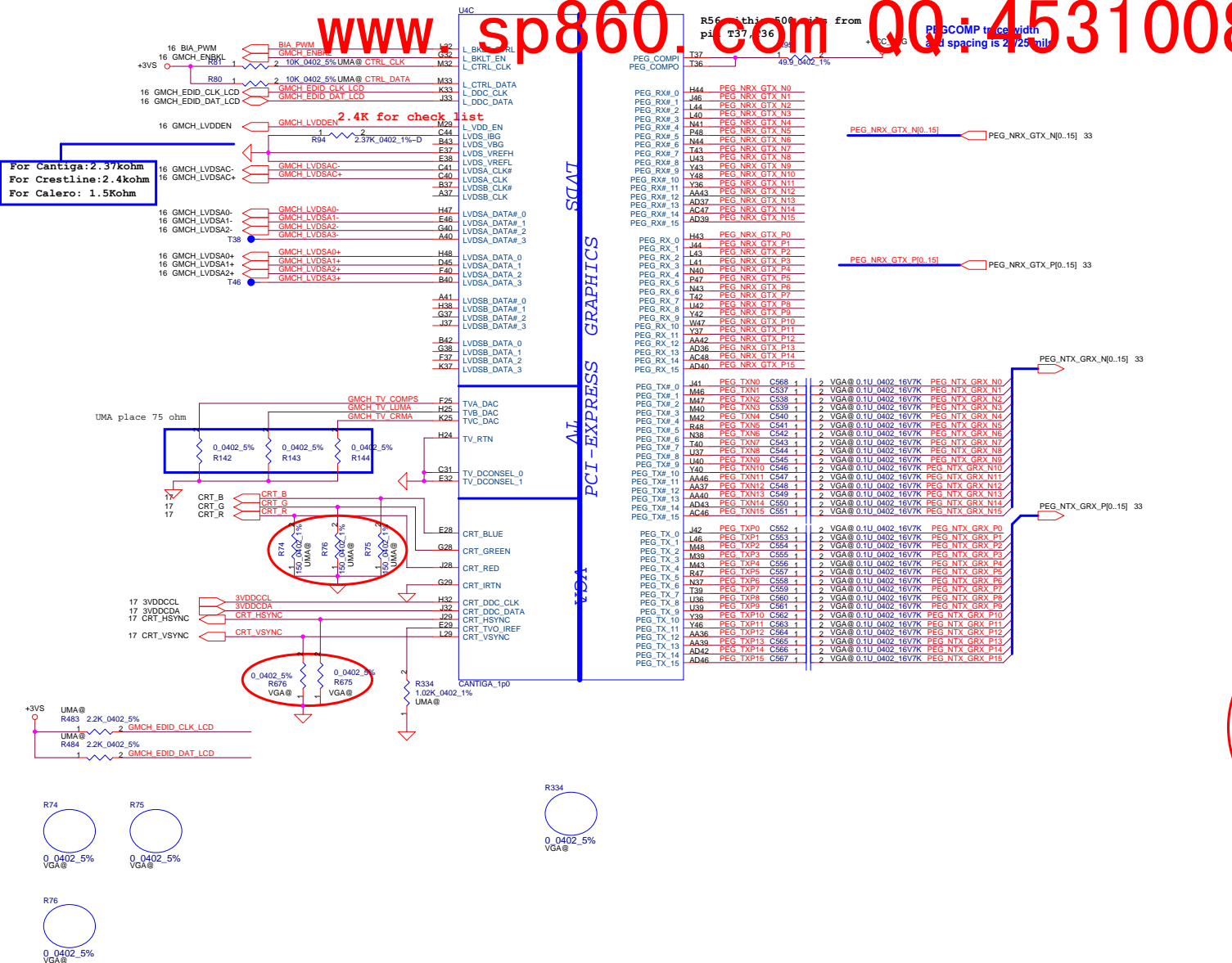
CANTIGA_1p0

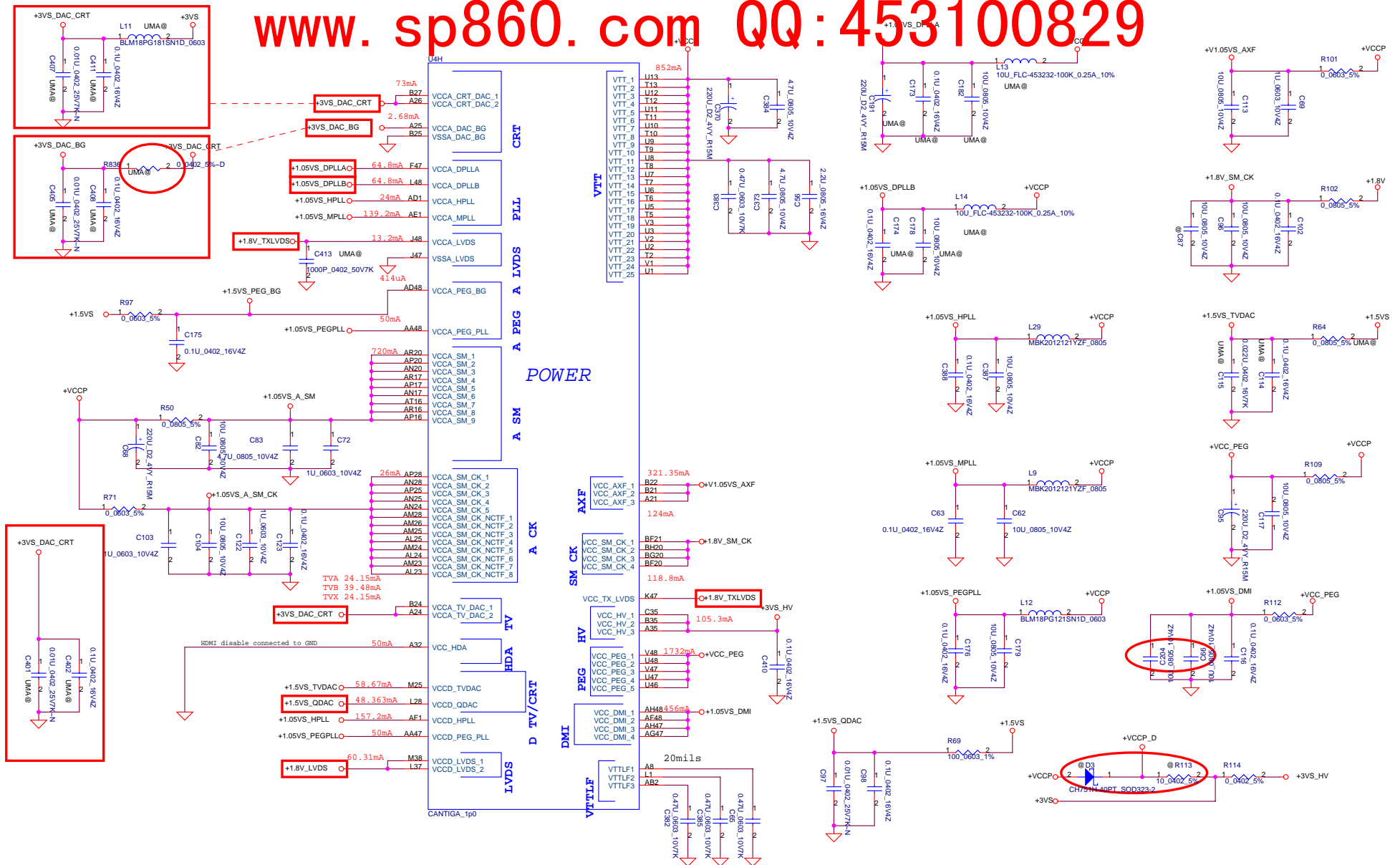
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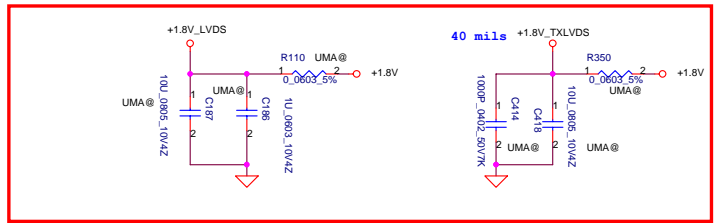
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 = (T)LSchiper suite with no confidentiality 1 = (T)LSchiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

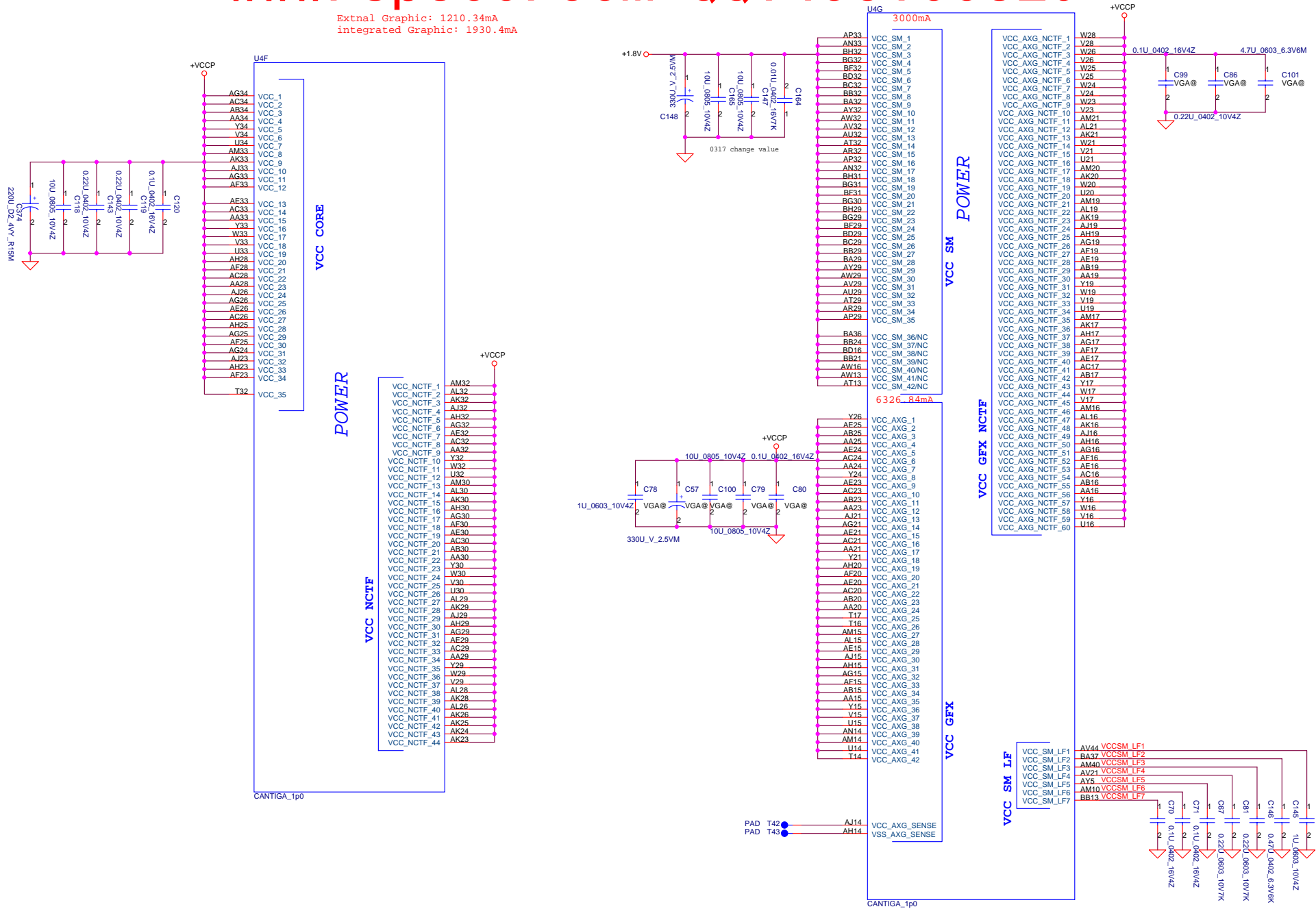




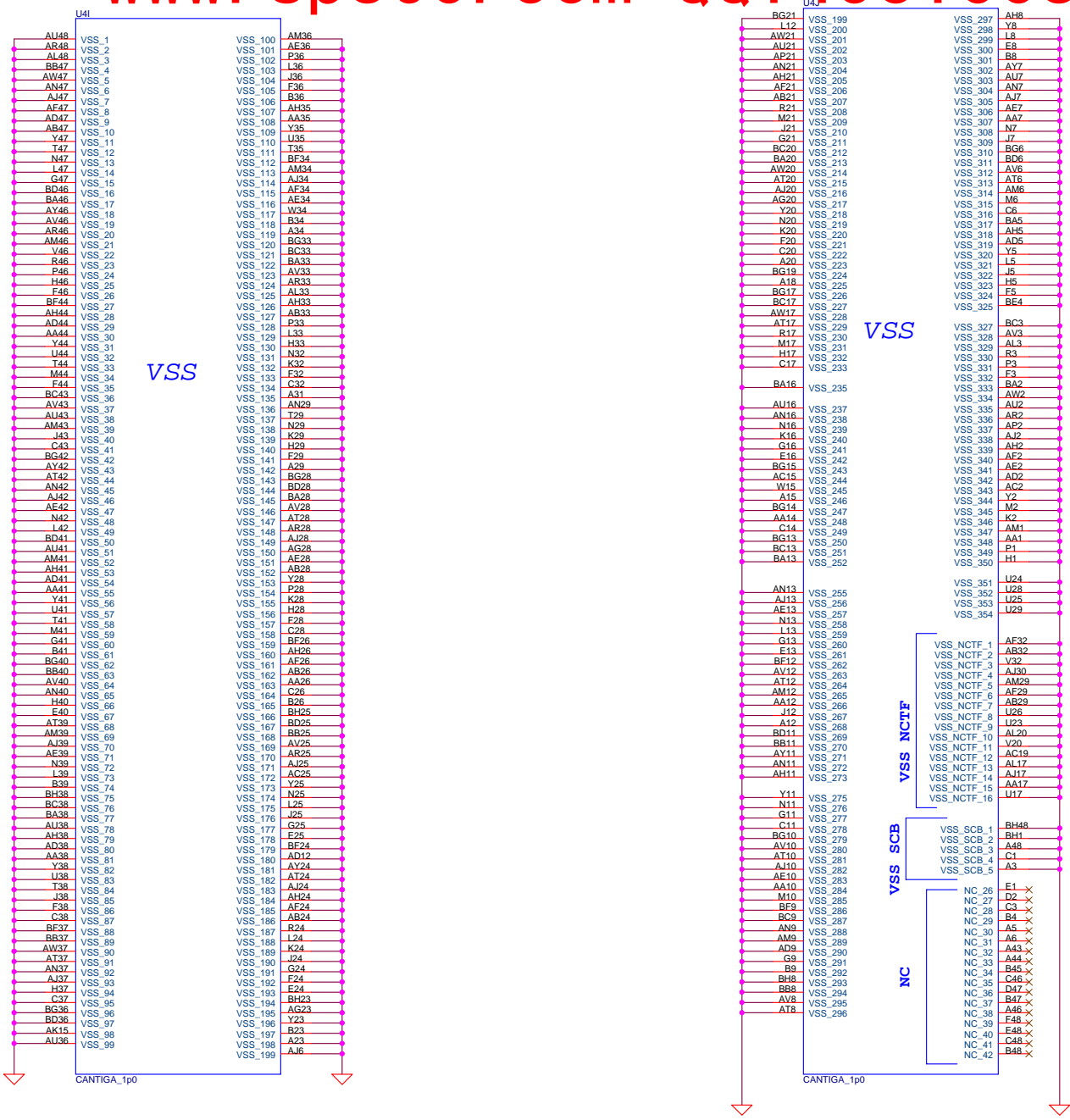
- C401: 0.0402_5% VGA@
- C405: 0.0402_5% VGA@
- C413: 0.0402_5% VGA@
- C174: 0.0402_5% VGA@
- U4: CRESTLINE_1p0 VGA@
- C407: 0.0402_5% VGA@
- C173: 0.0402_5% VGA@
- C115: 0.0402_5% VGA@
- C186: 0.0603_5% VGA@



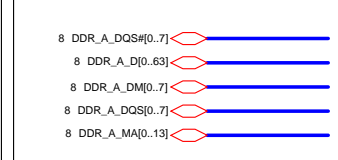
Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



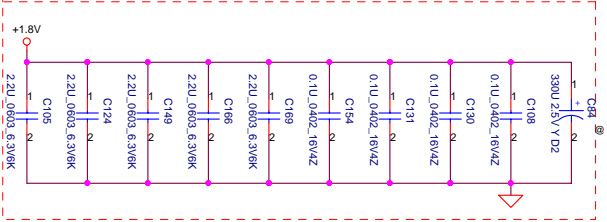
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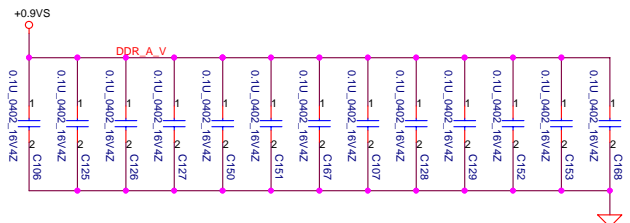
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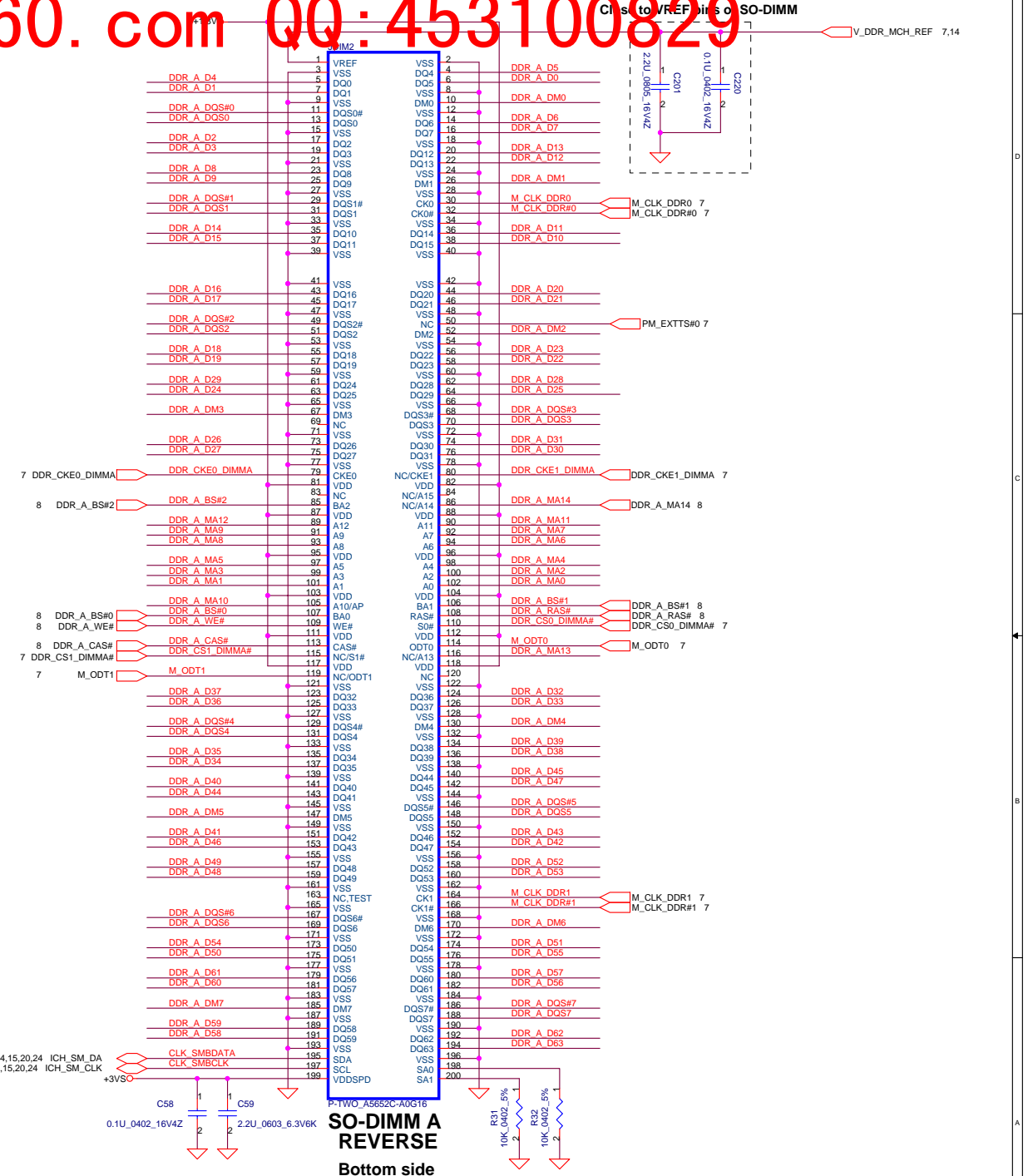
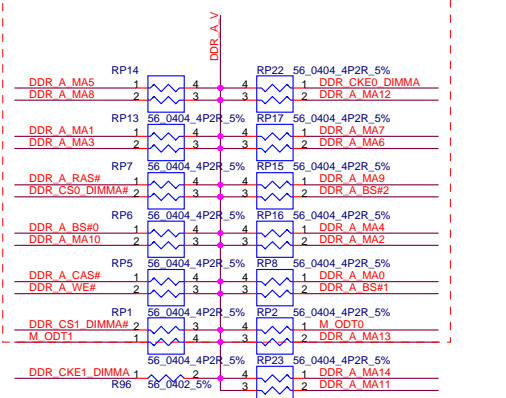
Layout Note:
Place near JDIM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

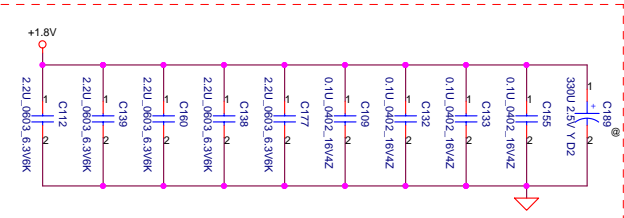


Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"

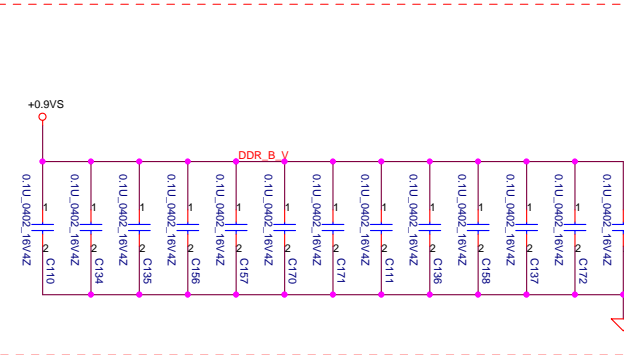


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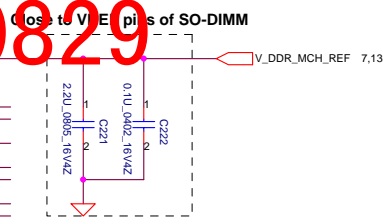
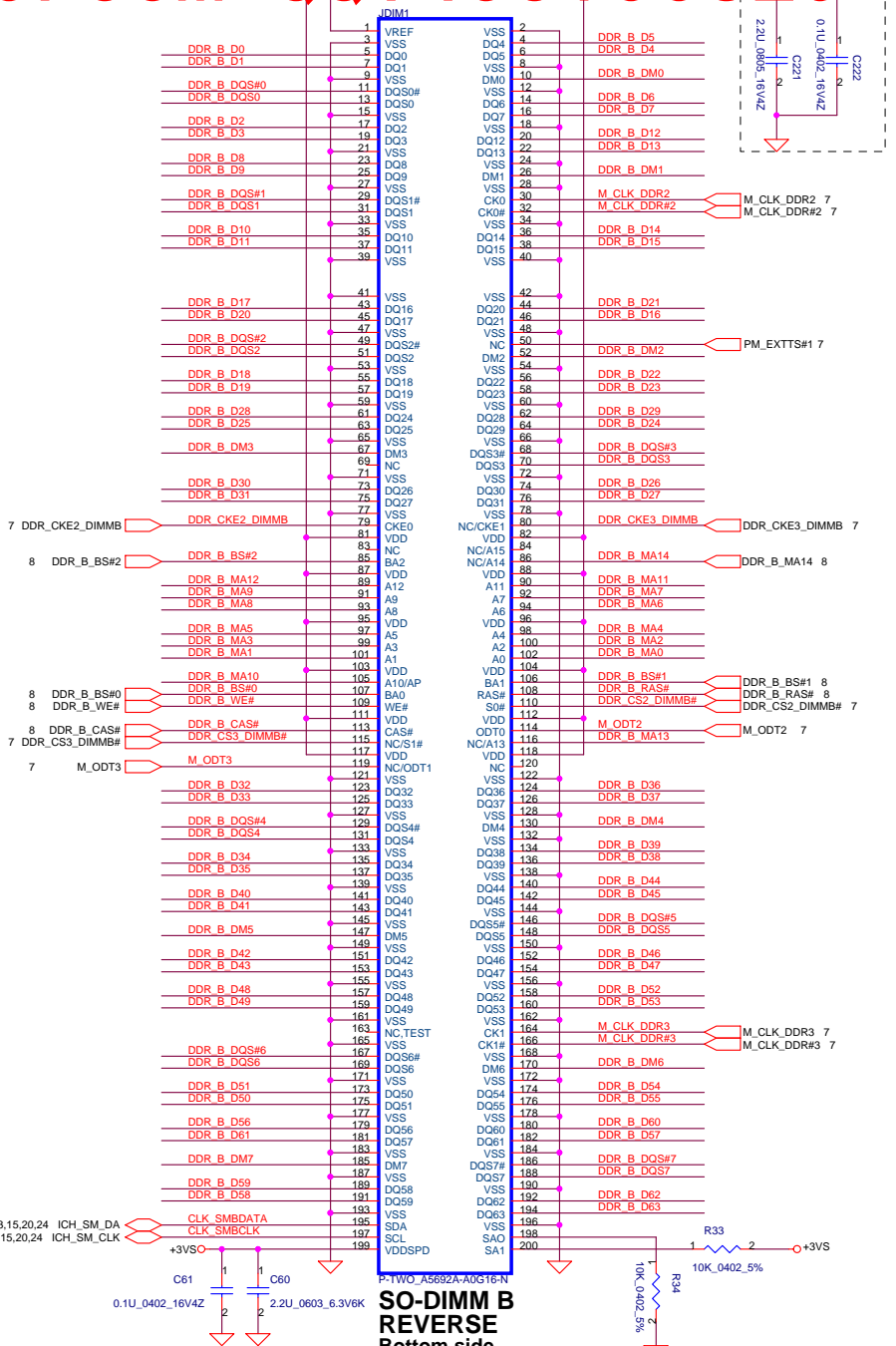
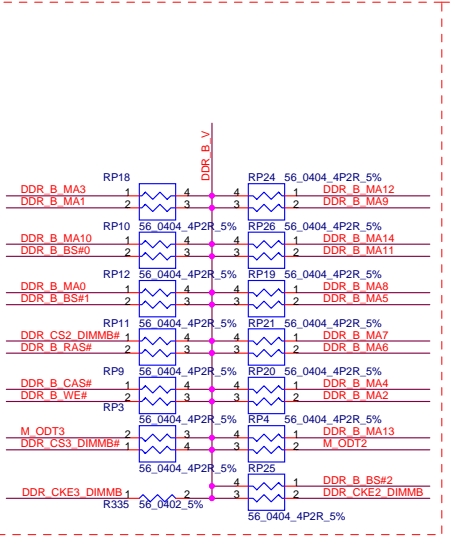
Layout Note:
Place near JDM12



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



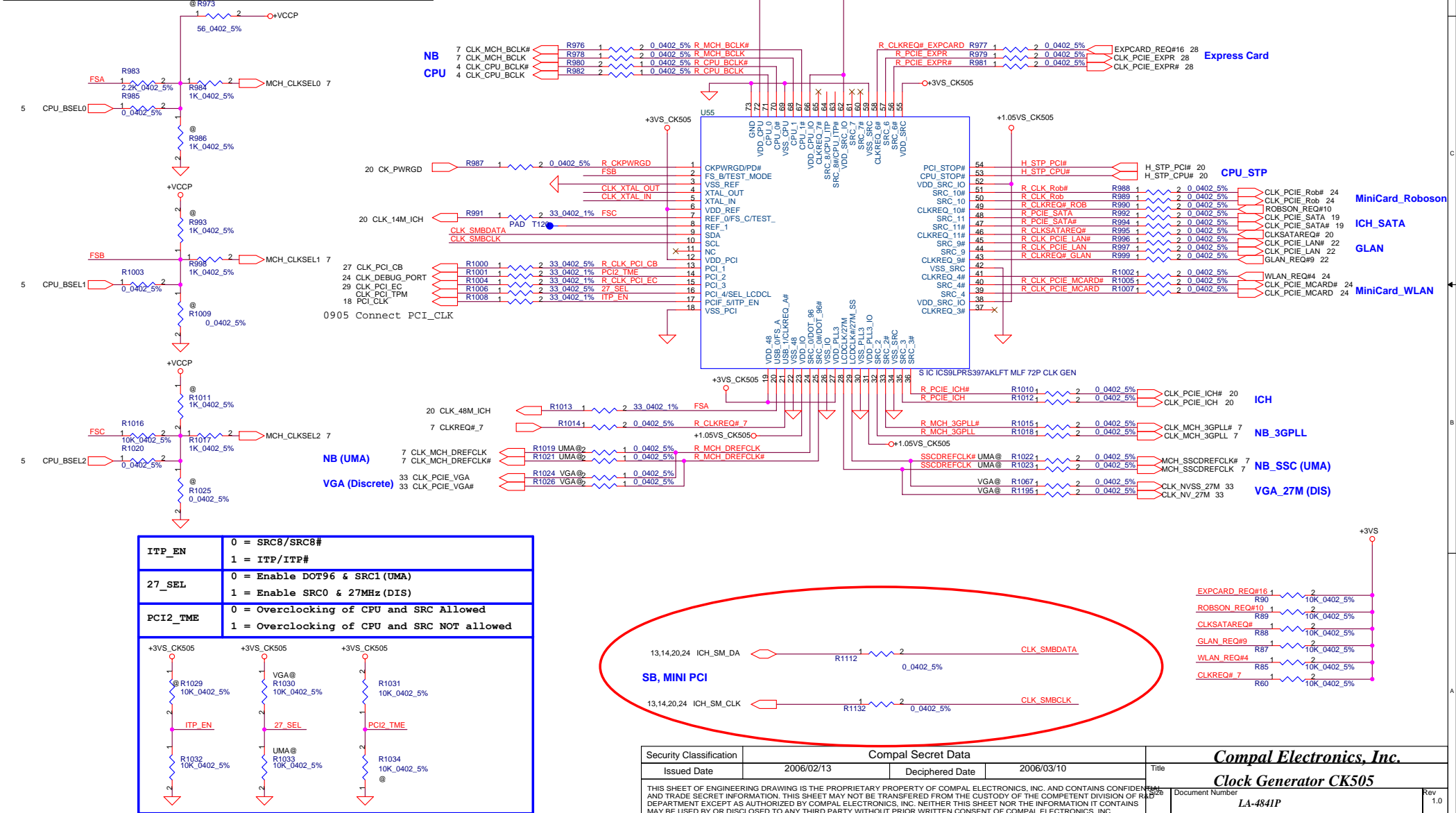
Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"



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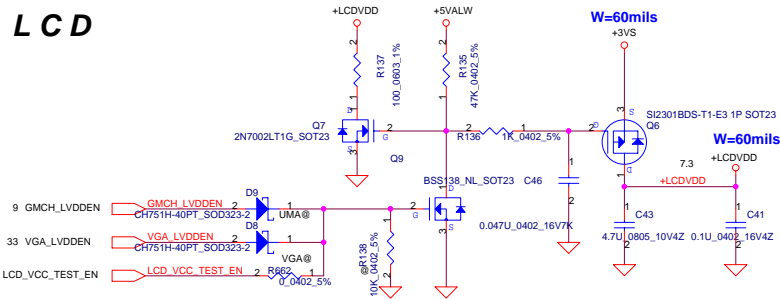
FSC	FSB	FSA	CPU	SRC	PCI	Rob	GLAN	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

www.sp860.com QQ:453100829

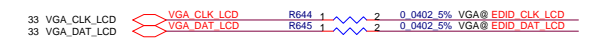
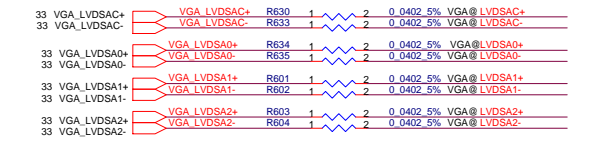
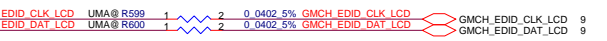
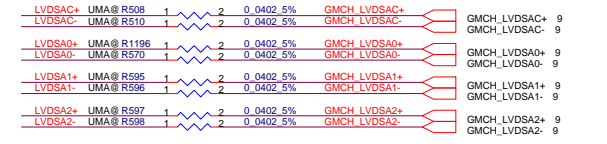
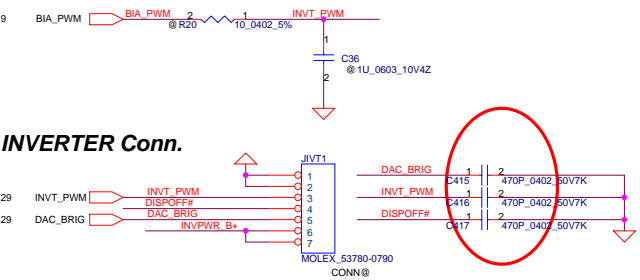
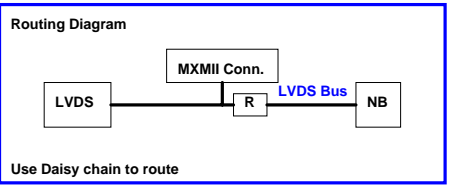
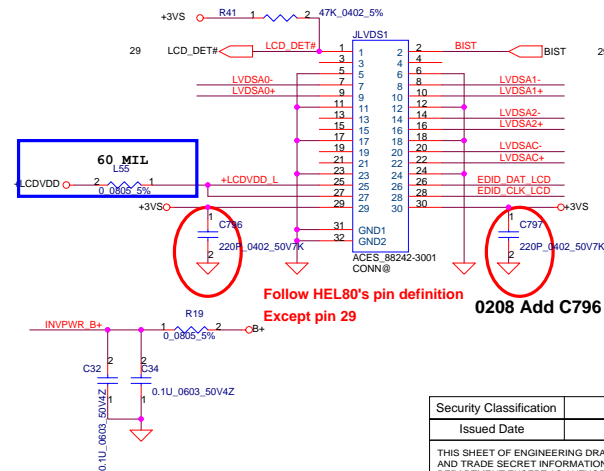


JEPICO Conn.

LCD



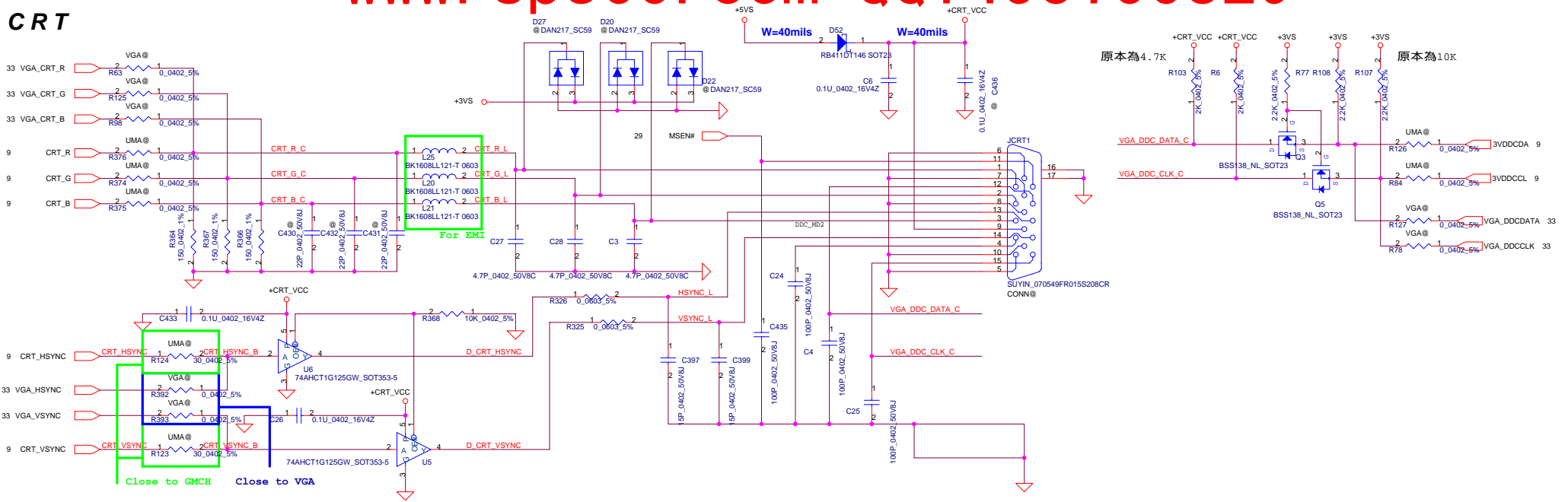
LCD/PANEL BD. Conn.



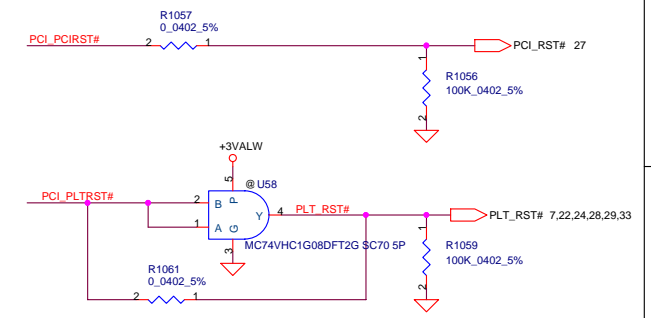
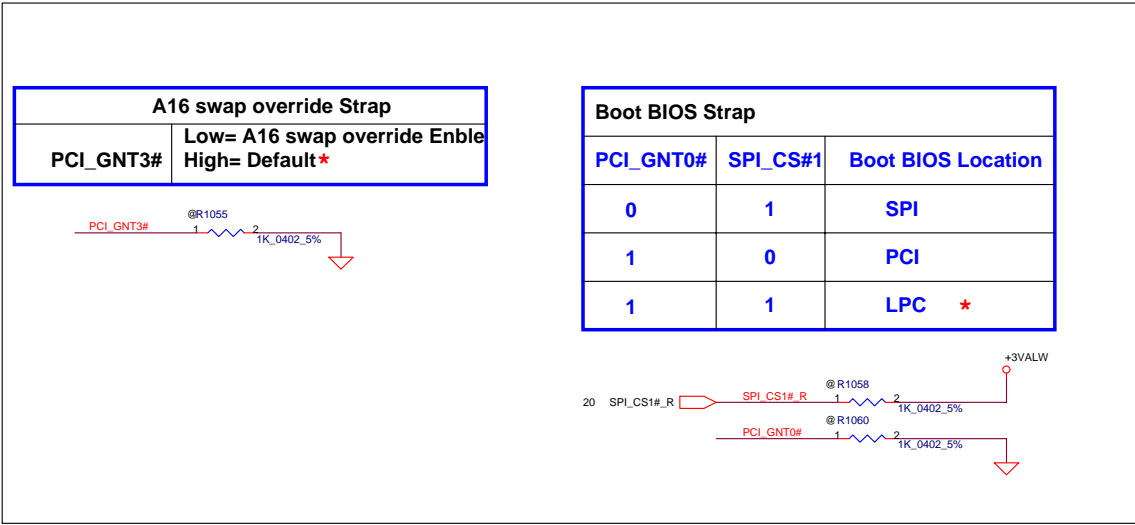
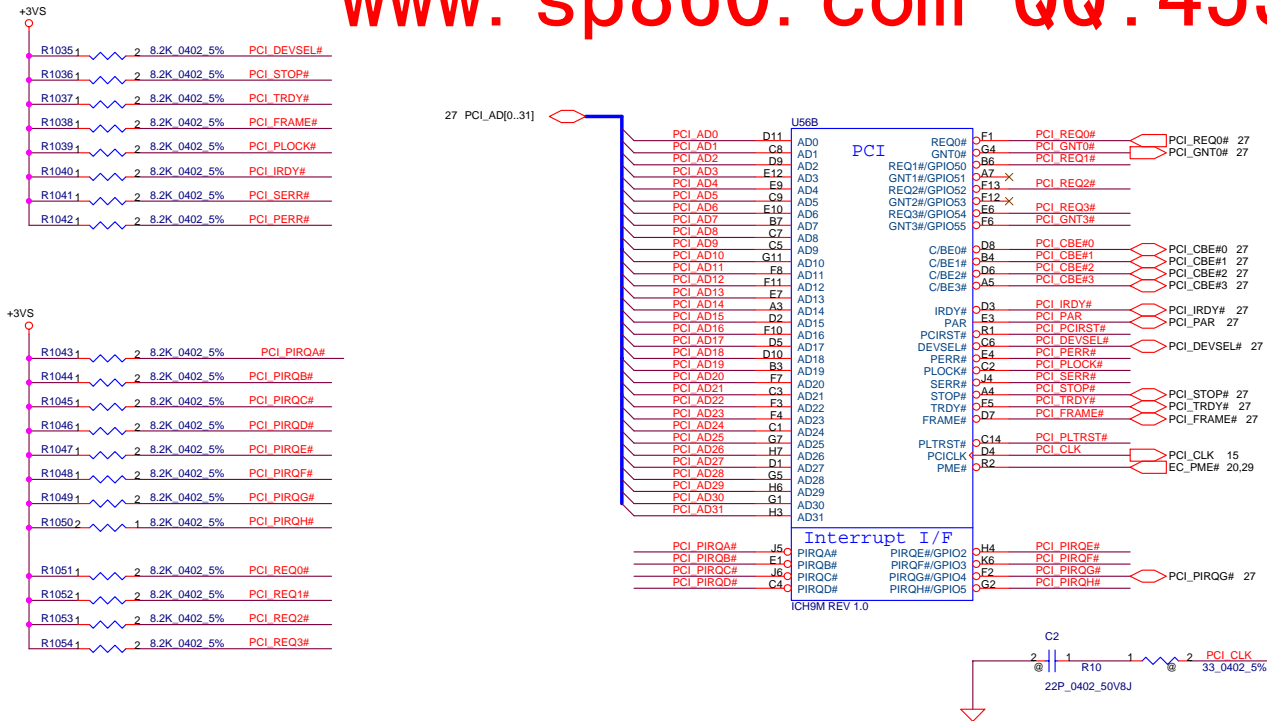
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Issued Date	2007/1/15	Deciphered Date	2008/1/15
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		Customer	LA-48A1P
Date:	Monday, December 15, 2008	Sheet	16 of 45
		Rev	1.0

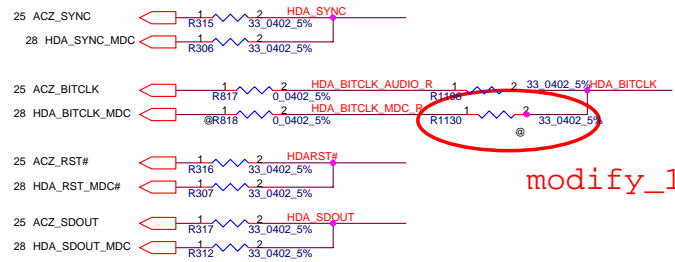
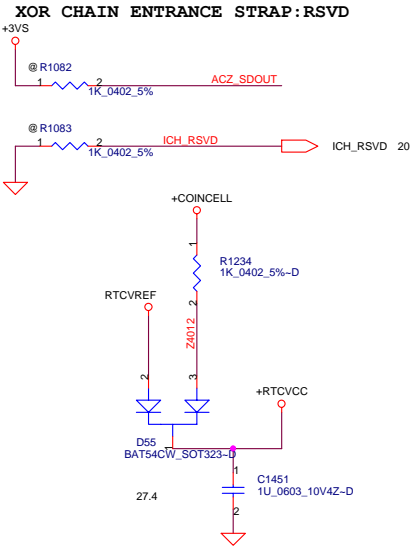
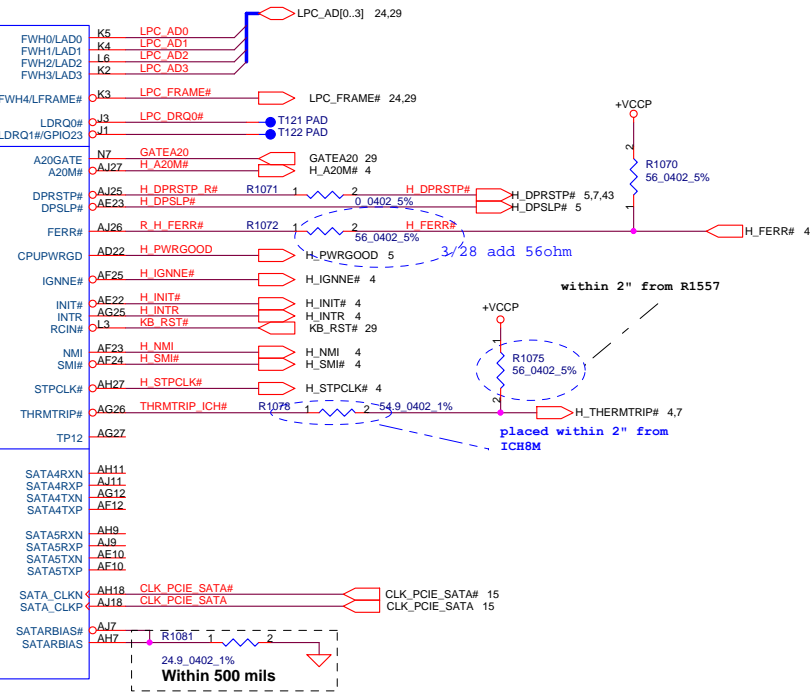
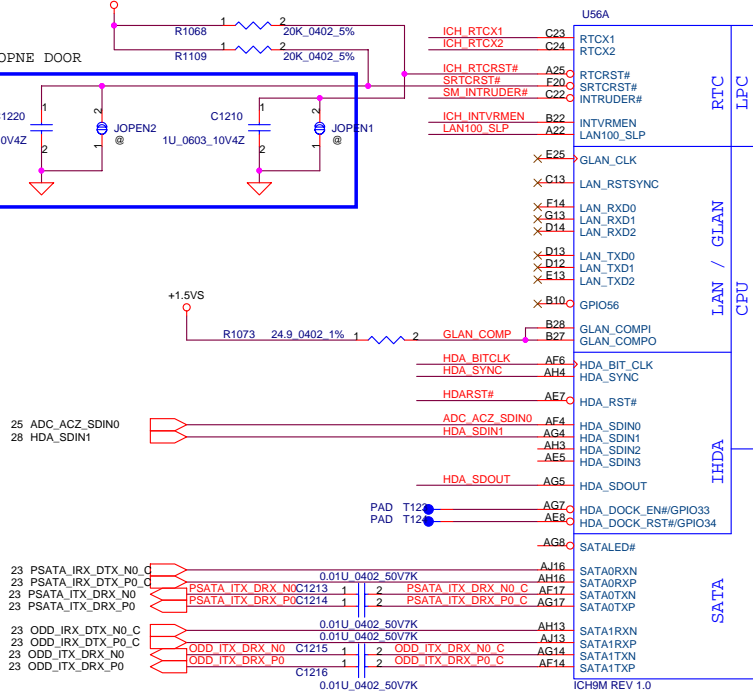
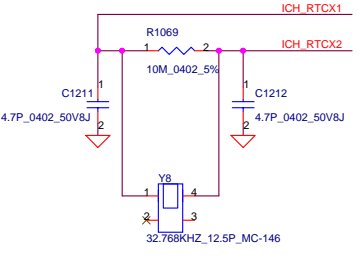
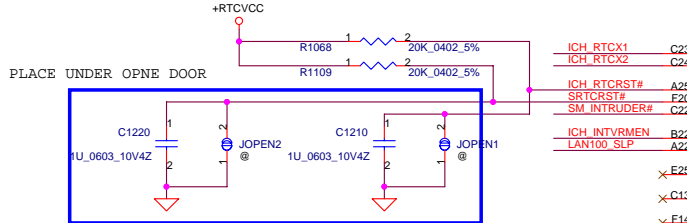
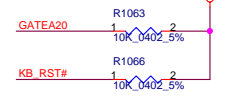
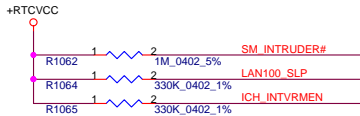
Compal Electronics, Inc.
CRT CONN/LCD CONN

CRT



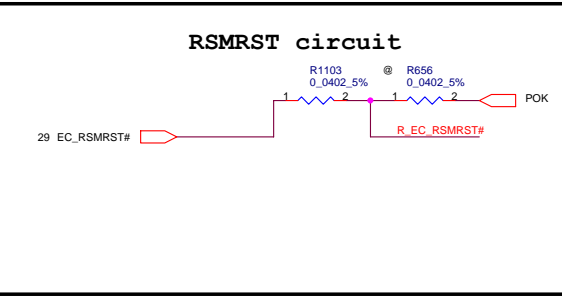
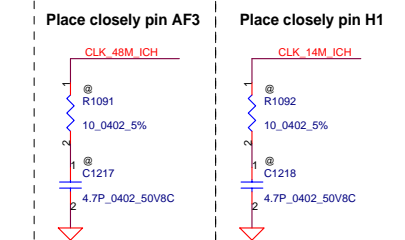
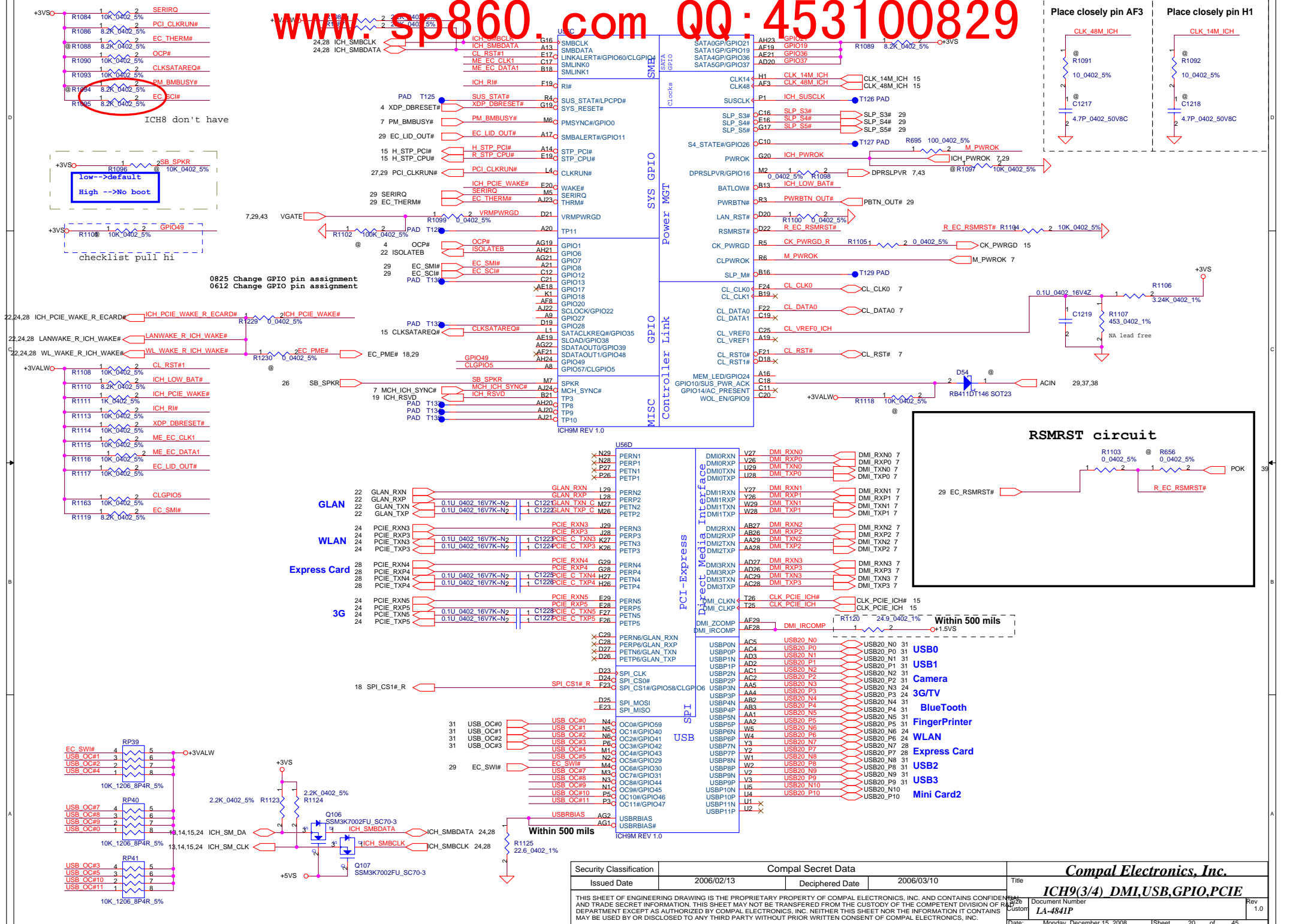
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Size	Document Number	Rev	
Custom	LA-4841P	1.0	
Date:	Monday, December 15, 2008	Sheet	17 of 45



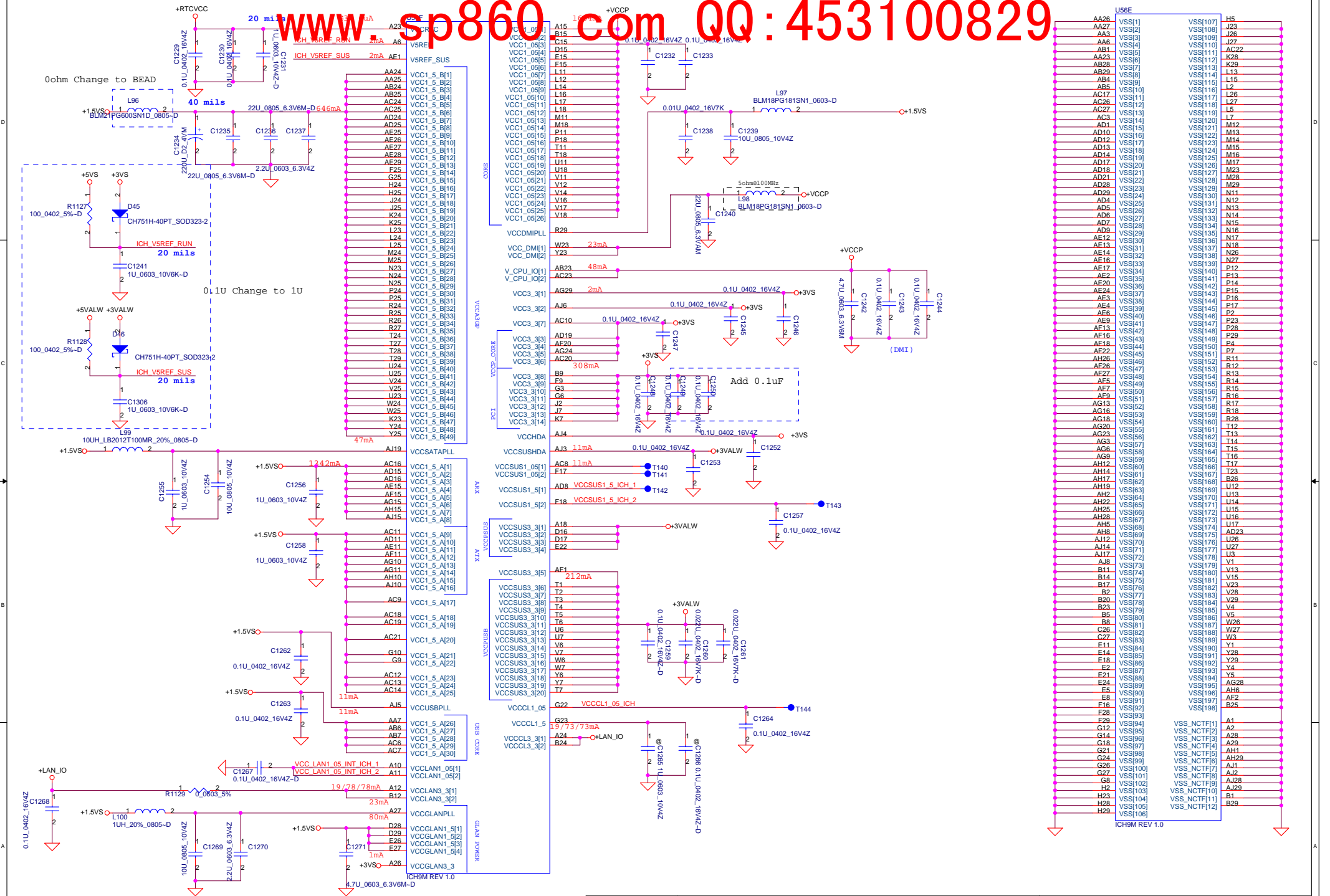


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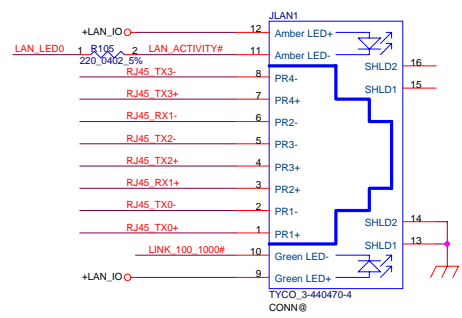
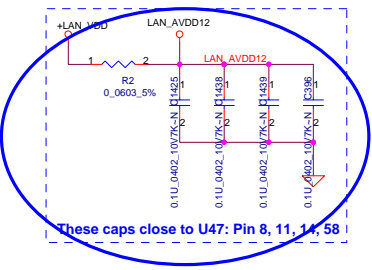
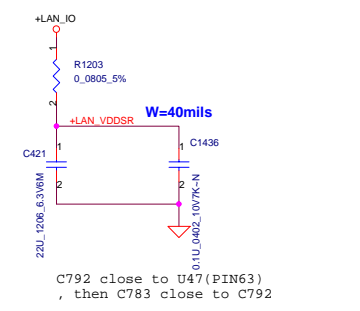
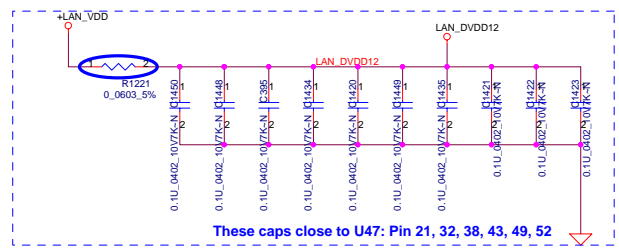
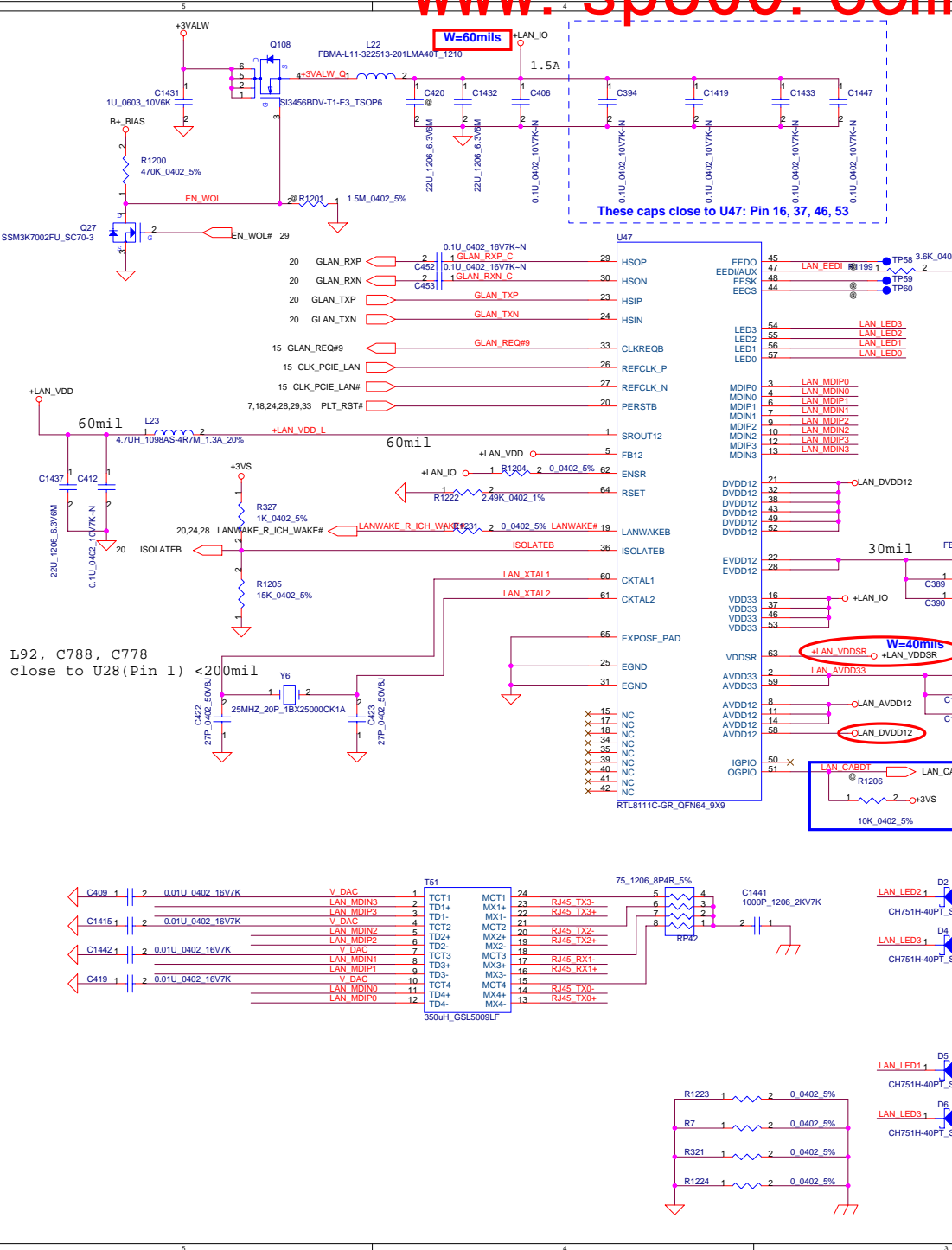
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	ICH9(2/4) LAN,HD,IDE,LPC	
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				LA-481P	1.0
Date:	Monday, December 15, 2008	Sheet	20	of 45	

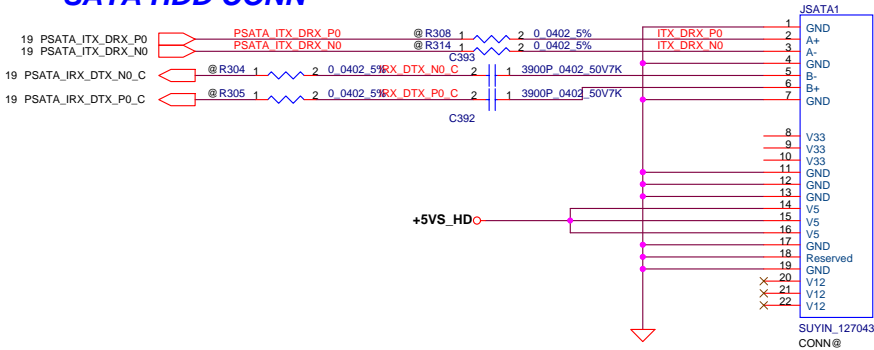


Security Classification		Compal Secret Data		Title	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Compal Electronics, Inc.	
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				LA-481P	1.0
Date:	Monday, December 15, 2008	Sheet	21	of	45



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		Sheet Number LA-4841P	Rev 1.0
		Date Monday, December 15, 2008	Sheet 22 of 45

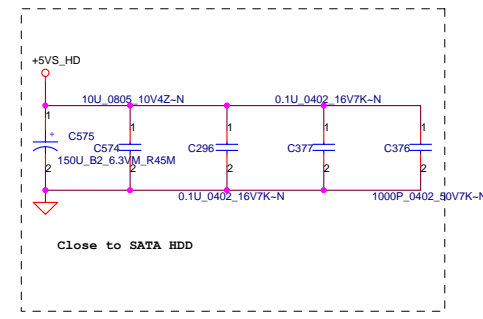
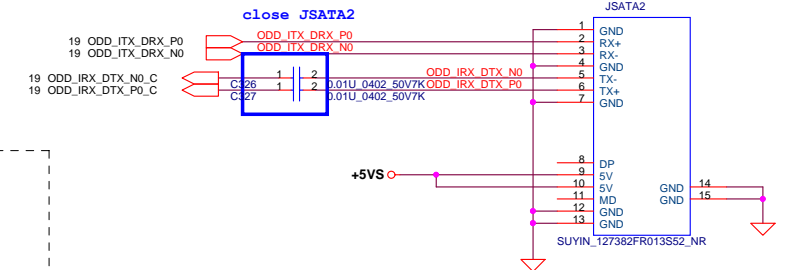
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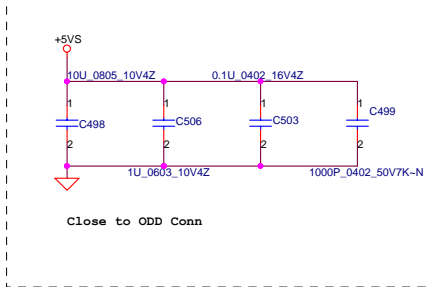
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FBMA-L11-160808-301LMA20T_1206-D

SATA ODD CONN



Close to SATA HDD



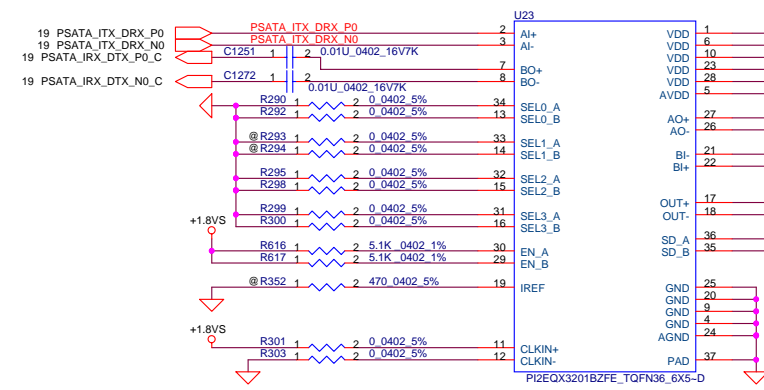
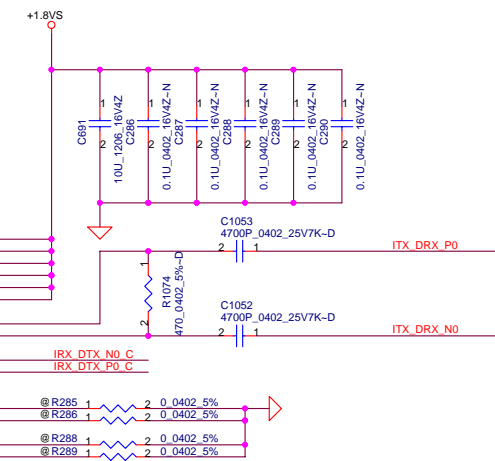
Close to ODD Conn

Output Swing Control

SEL2_ [A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

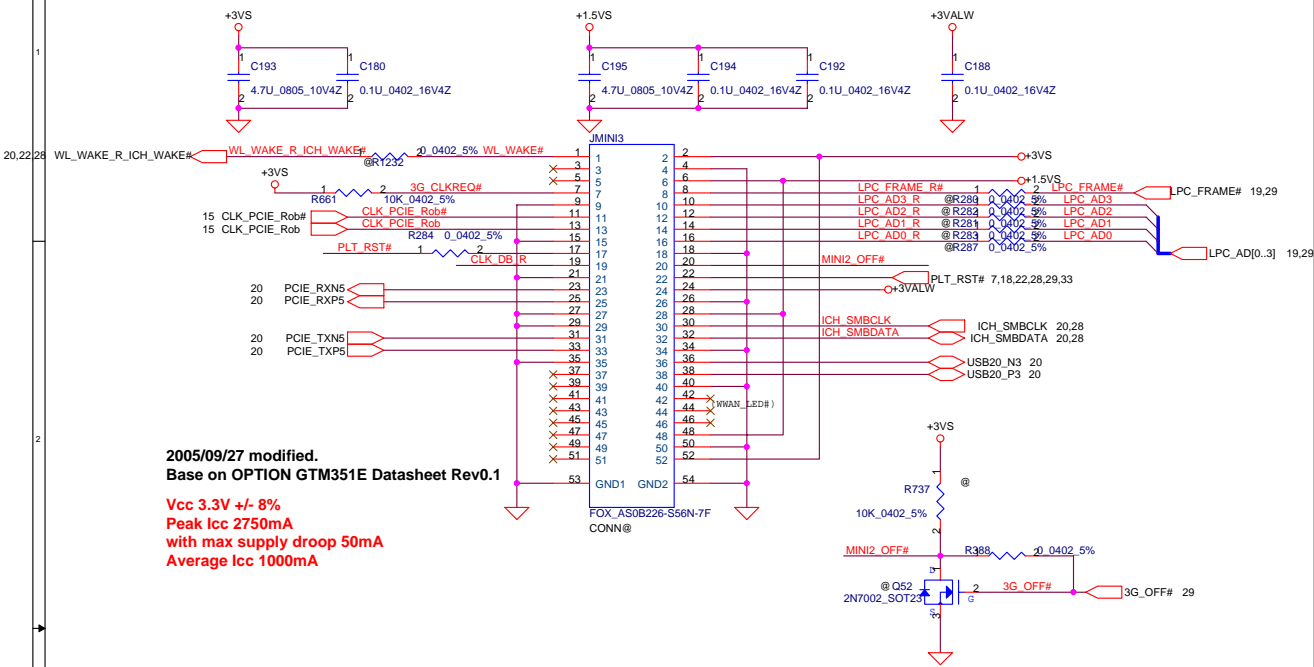
SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



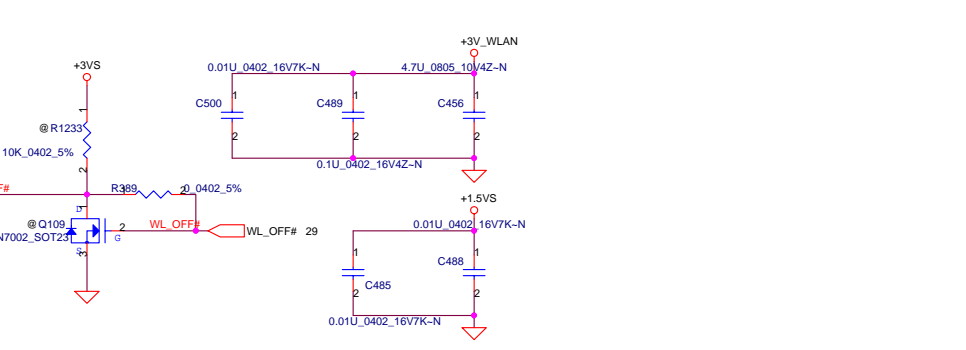
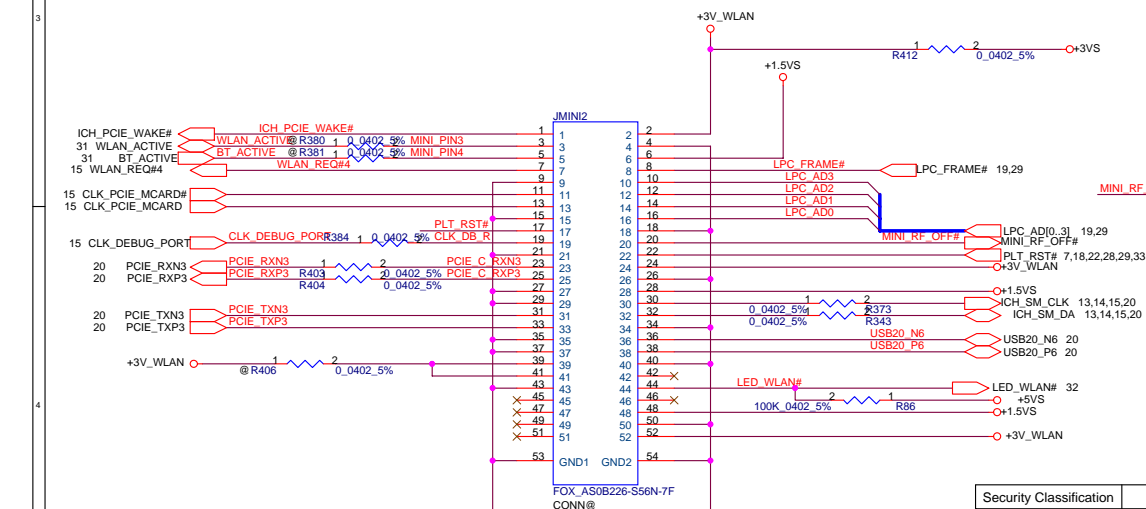
Equalizer Selection

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

Mini-Express Card for 3G Or TV Tuner



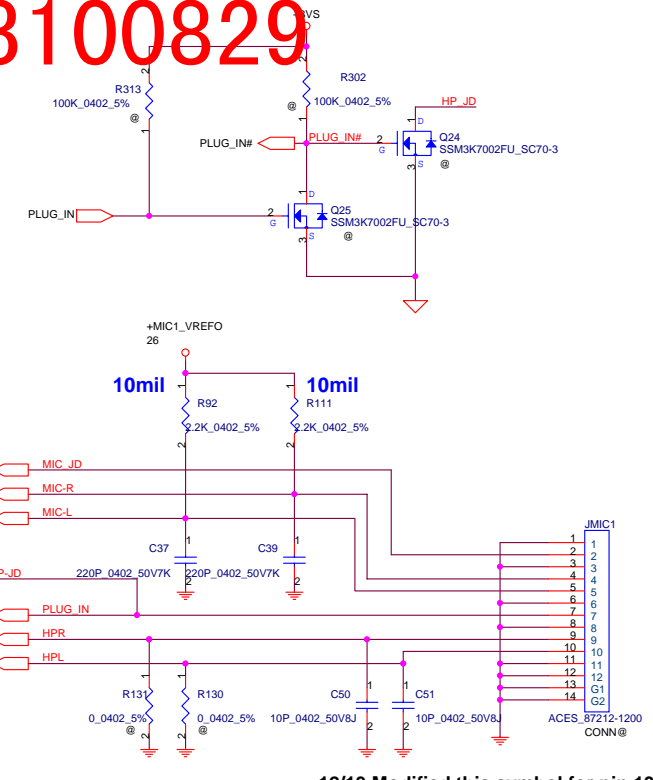
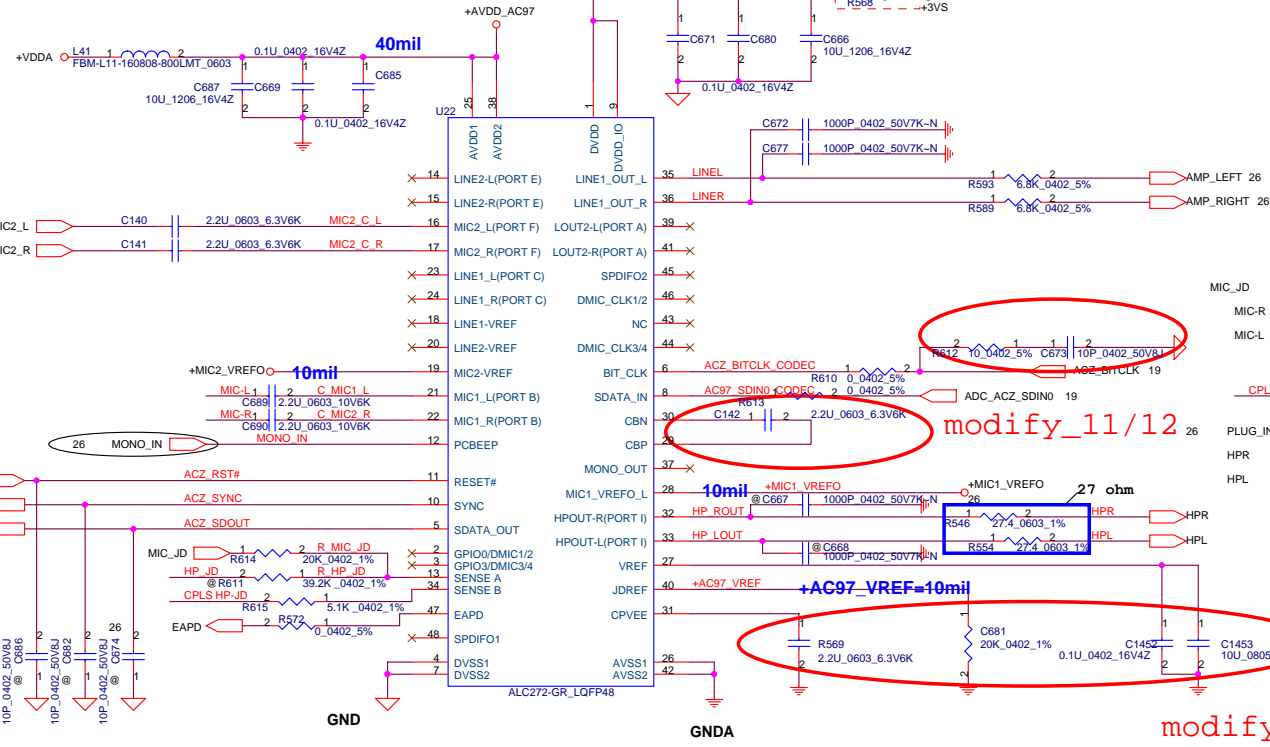
Mini-Express Card---WLAN



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Date:	Monday, December 15, 2008	Sheet	24	of 45

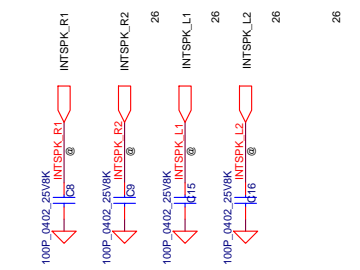
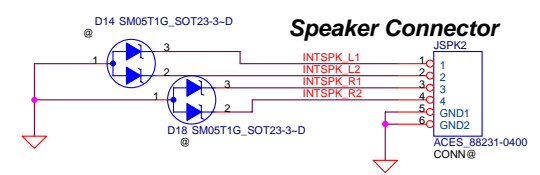
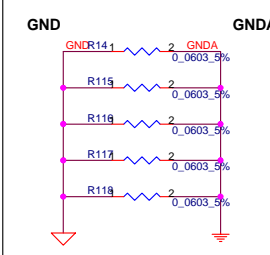
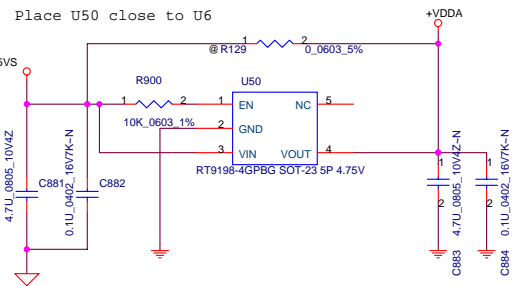
Compal Electronics, Inc.
Mini-Card/LED
 LA-481P

HD Audio Codec

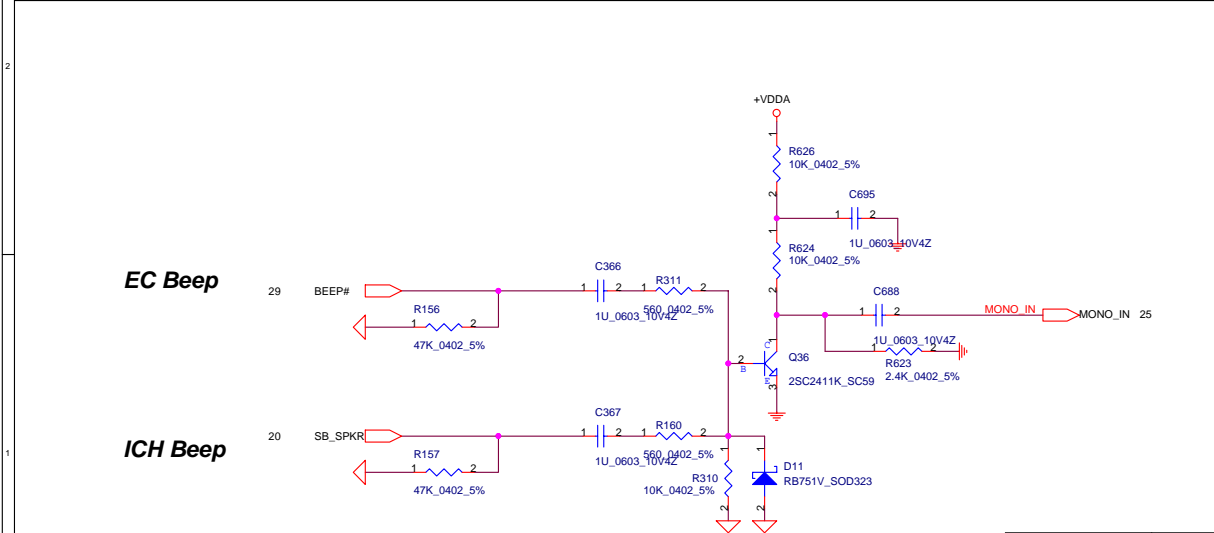
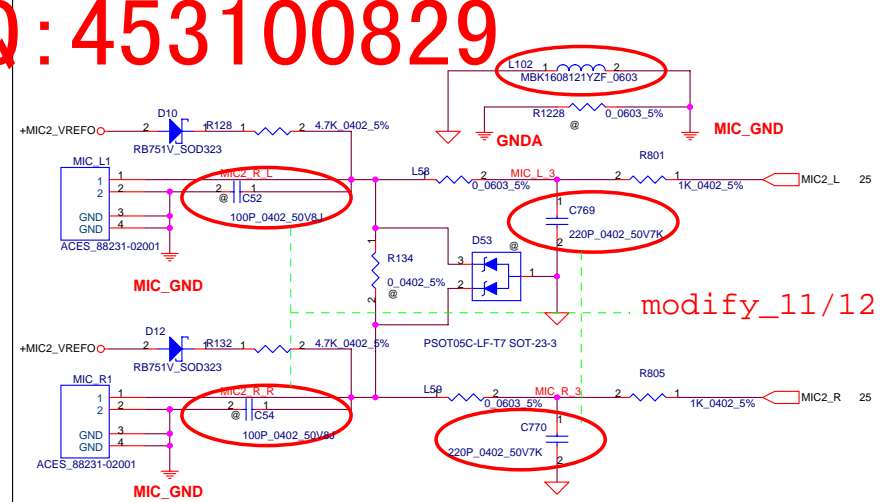
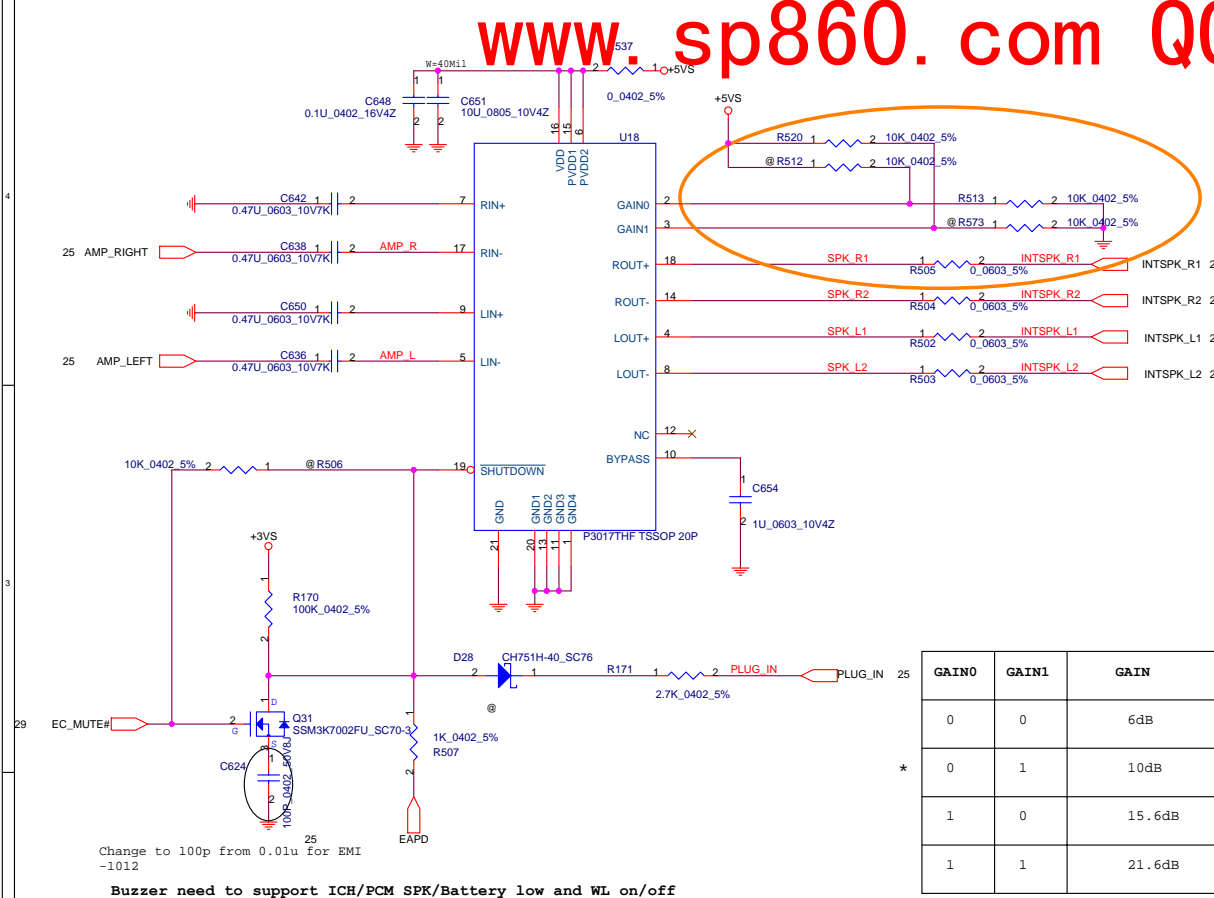


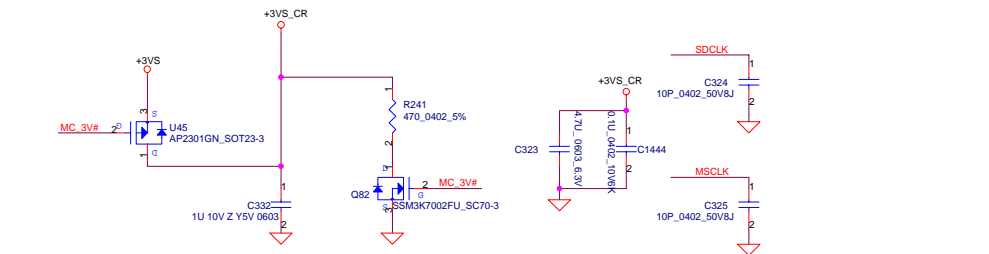
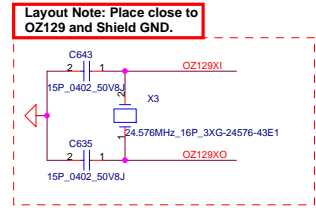
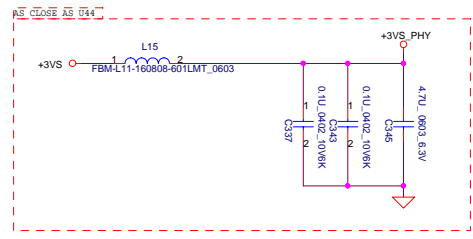
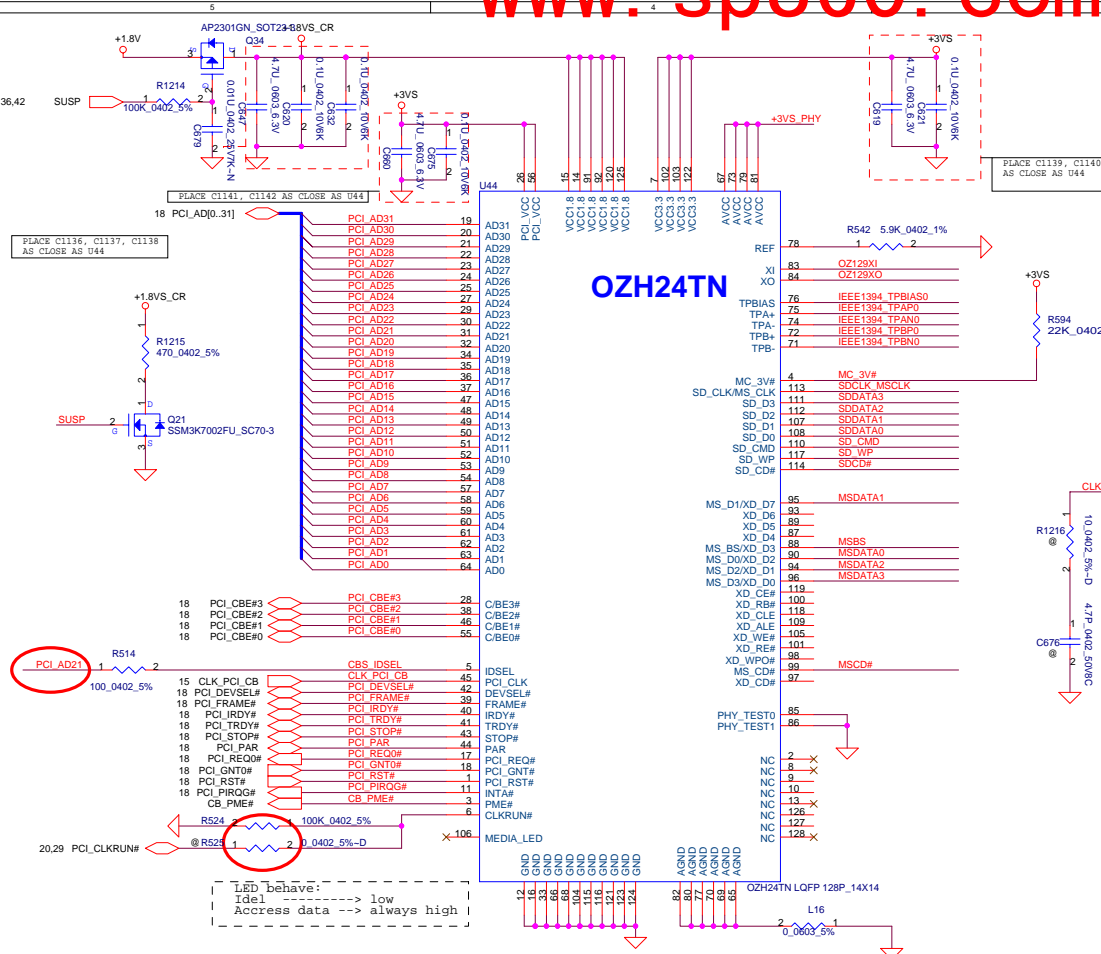
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modify_11/12

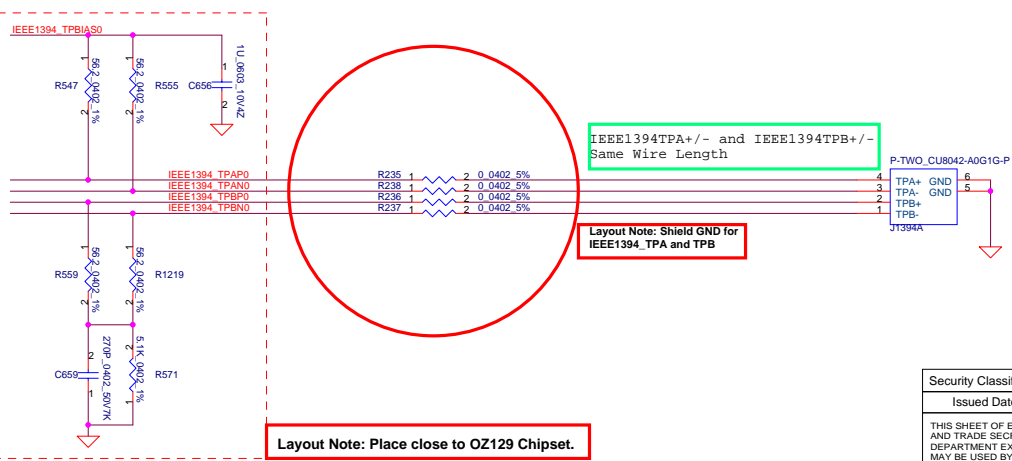
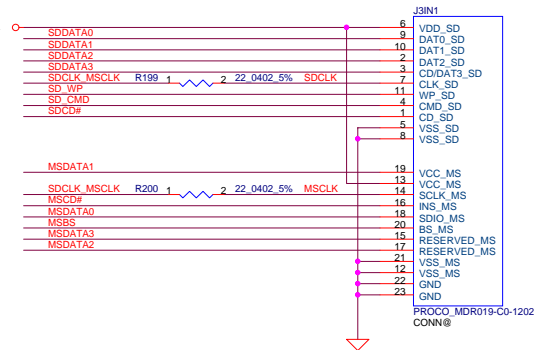


Security Classification	Compal Secret Data		Title	
Issued Date	2008/05/07	Deciphered Date	2009/05/07	HD CODEC 92HD81
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Date:	Monday, December 15, 2008	Sheet	25	of 45



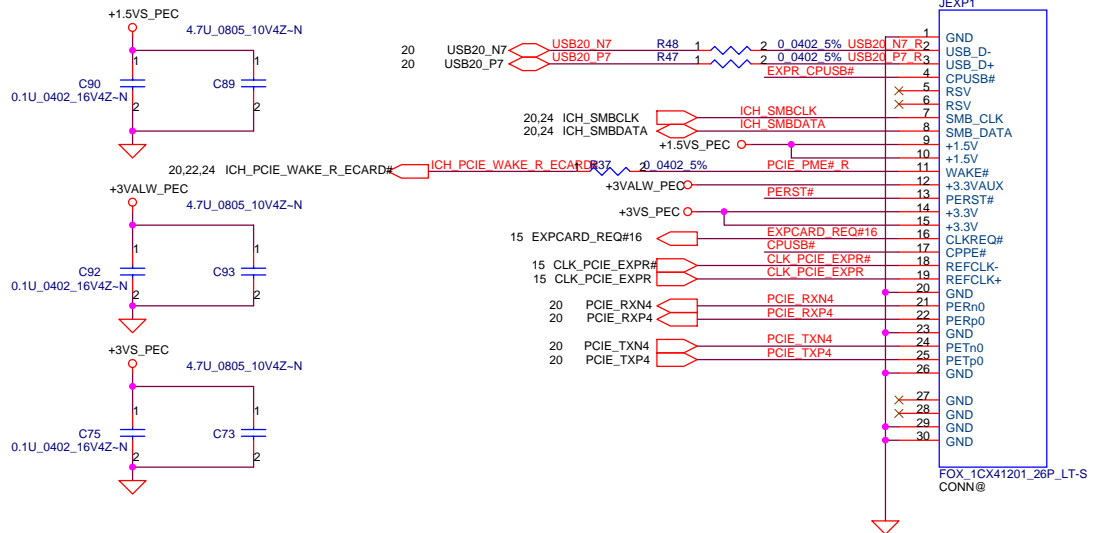
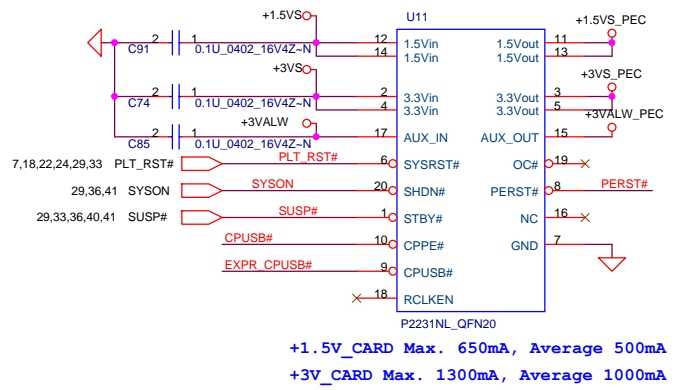


3 in 1 Card Reader

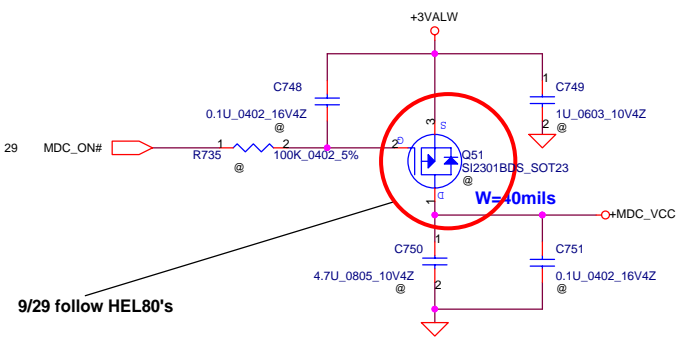
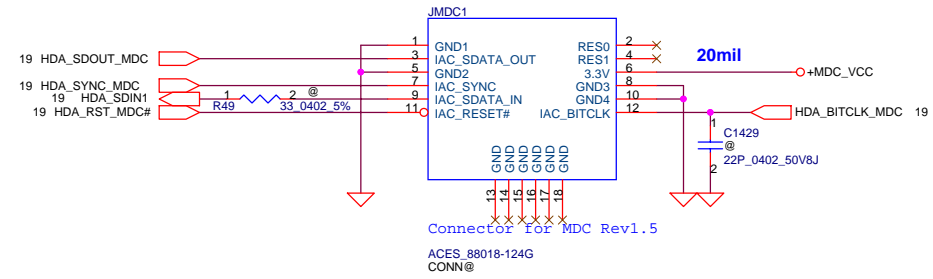


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Customer	LA-4841P	Document Number	Rev		1.0
Date	Monday, December 15, 2008	Sheet	27	of	45

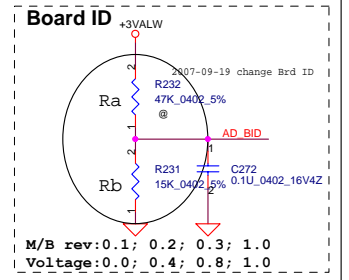
Express Card Power Switch



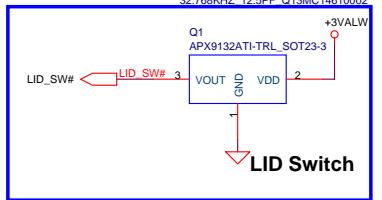
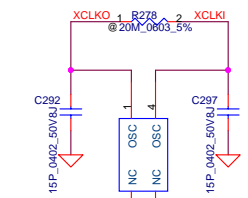
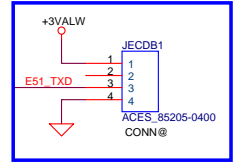
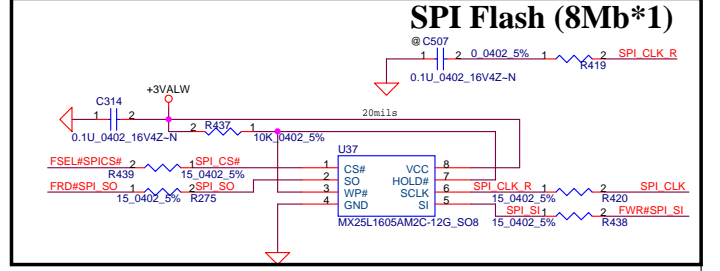
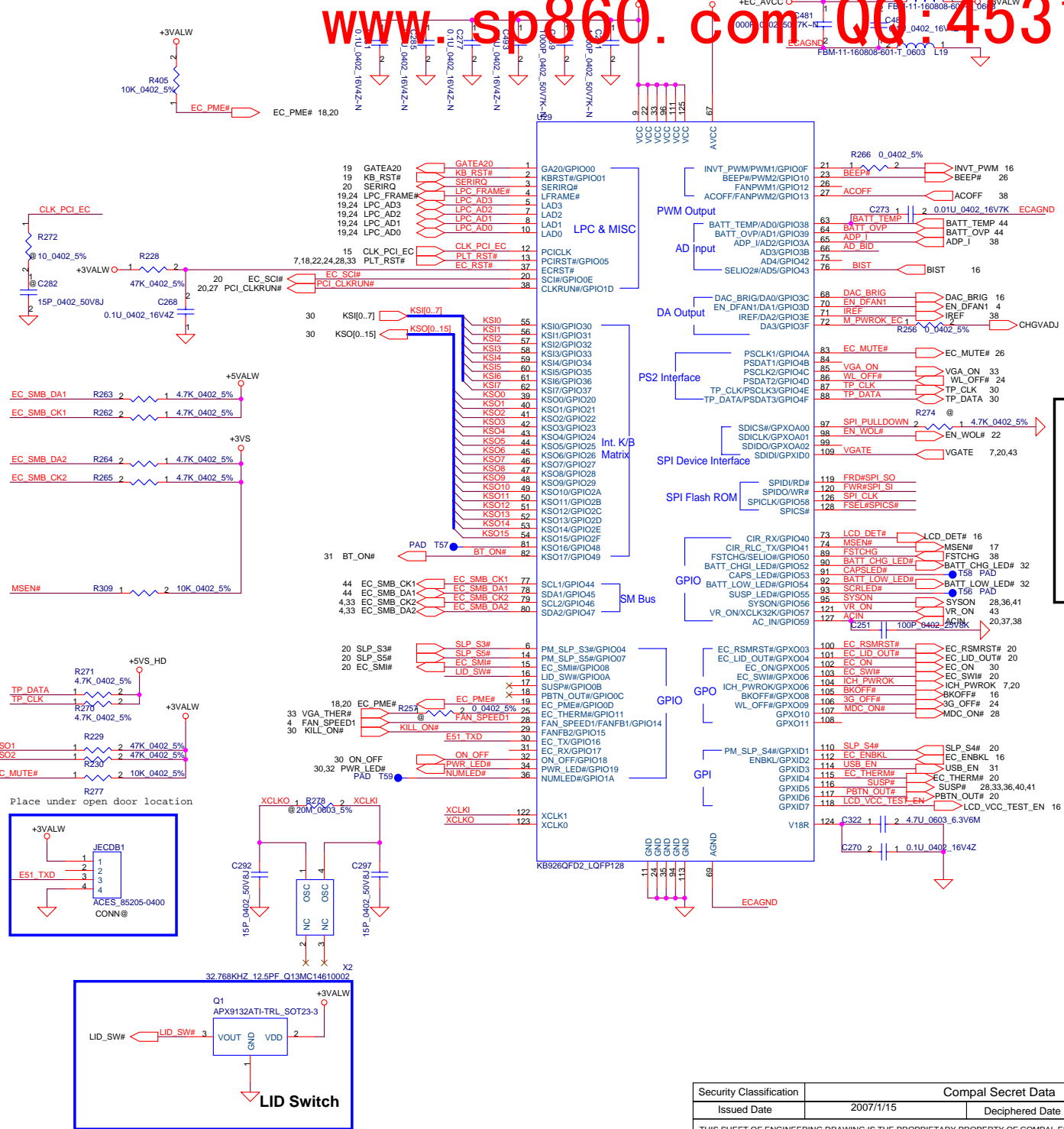
MDC Conn.



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Date:	Monday, December 15, 2008	Sheet	28 of 45	Document Number LA-4841P

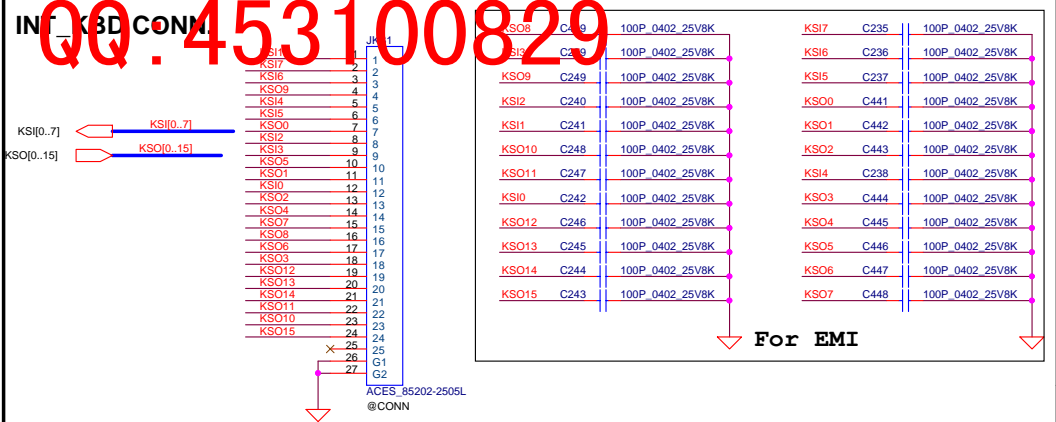
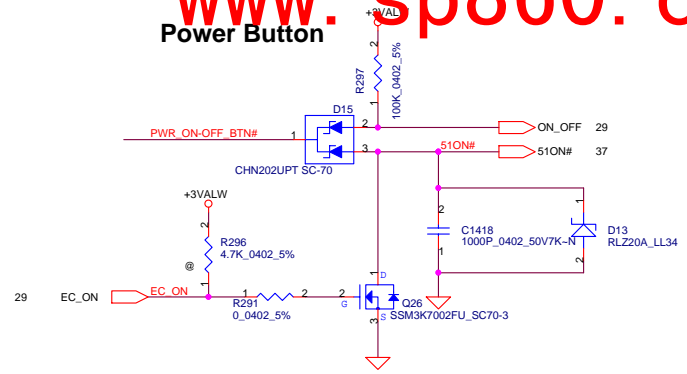


M/B rev:0.1; 0.2; 0.3; 1.0
Voltage:0.0; 0.4; 0.8; 1.0

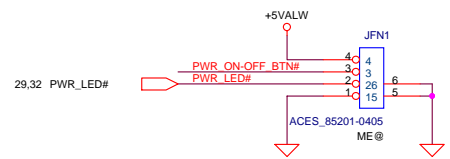


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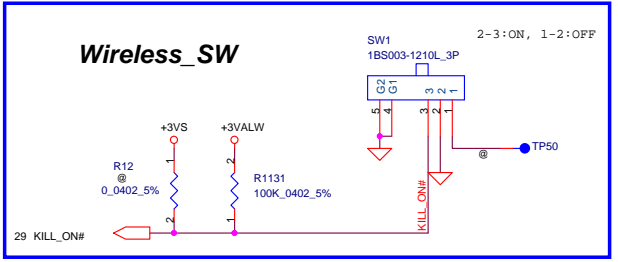
Power Button



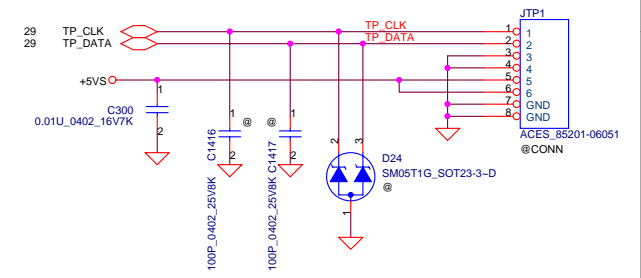
SW/B CONN.

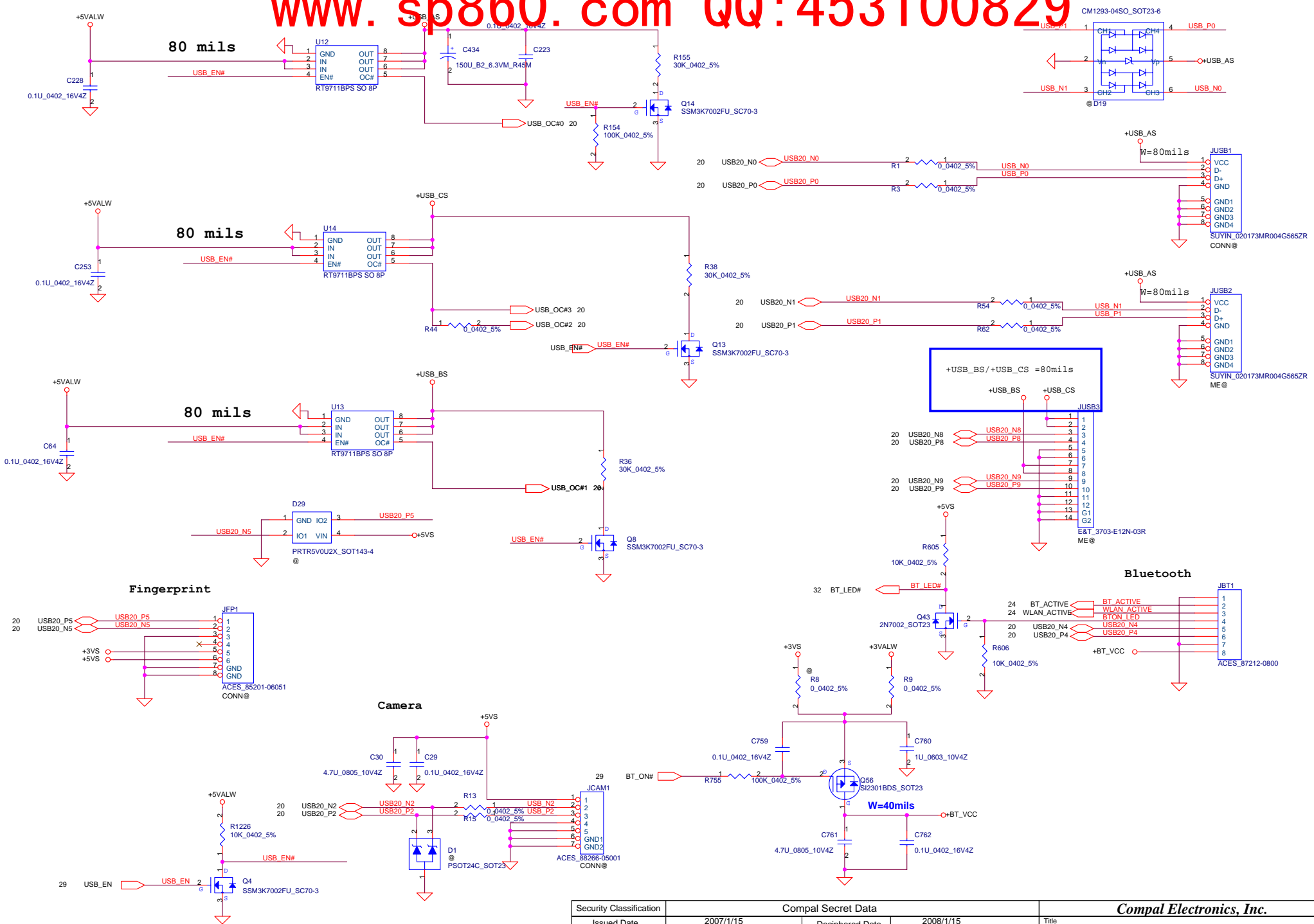


Wireless_SW

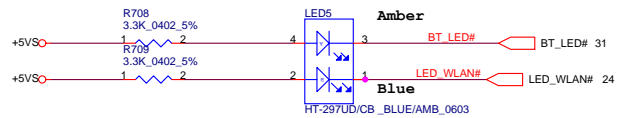
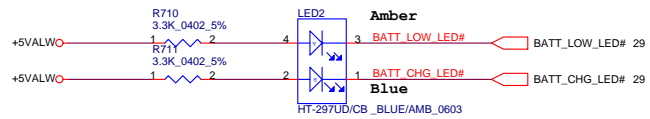
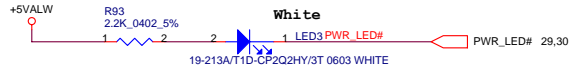


Touch PAD/B CONN.

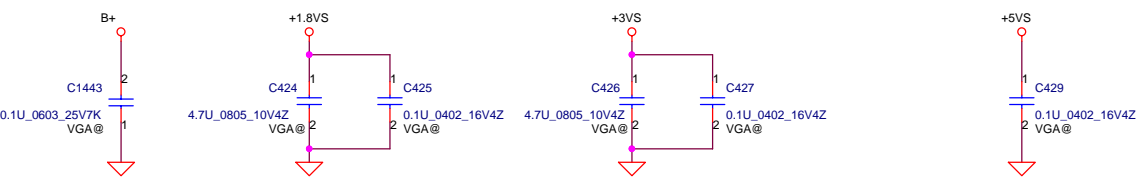
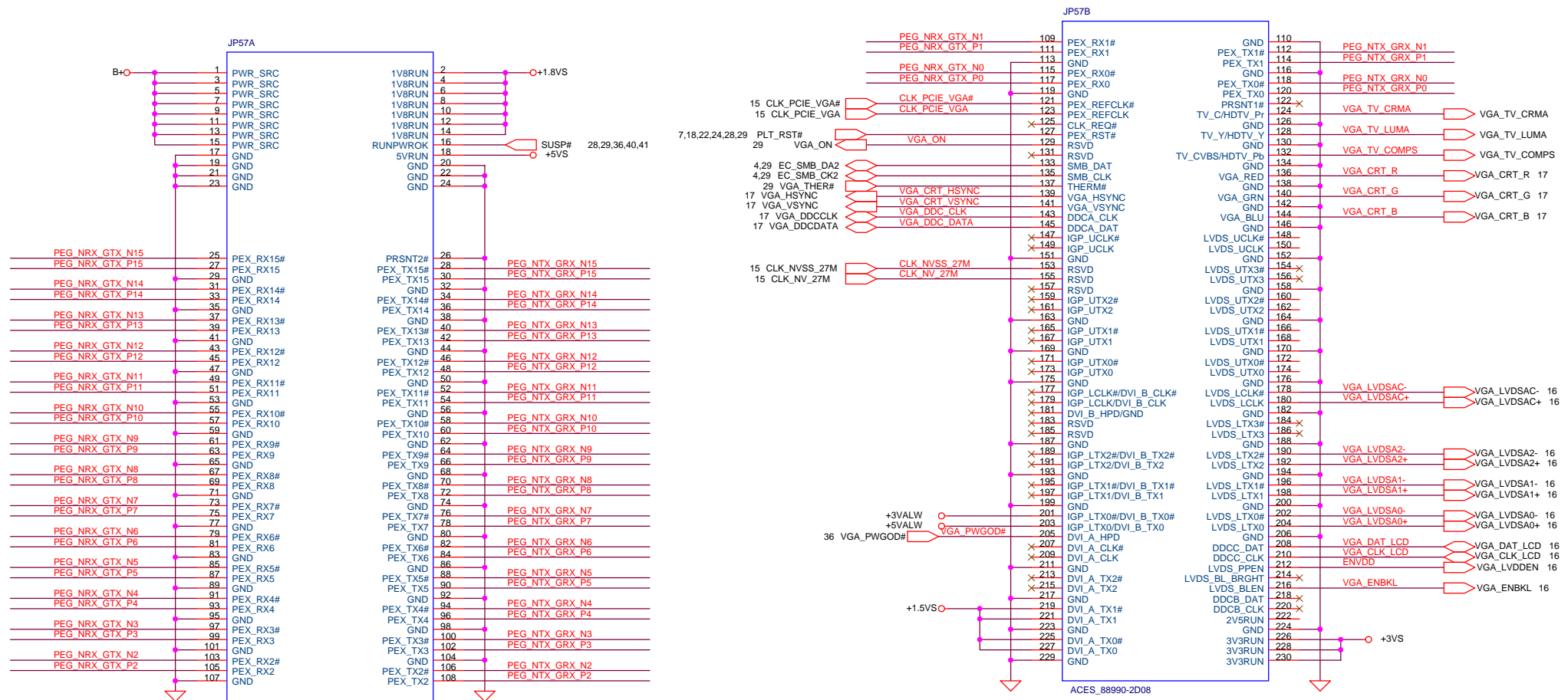




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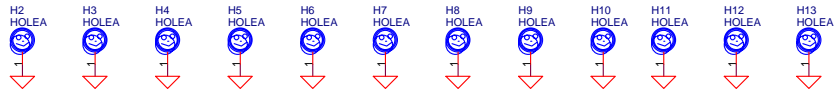


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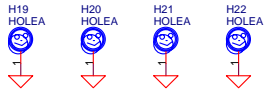
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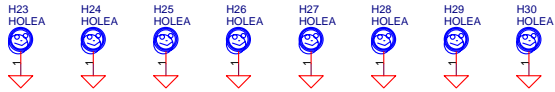
H_3P7



H_4P2



H_3P2

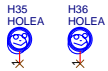
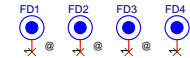


H_5P6

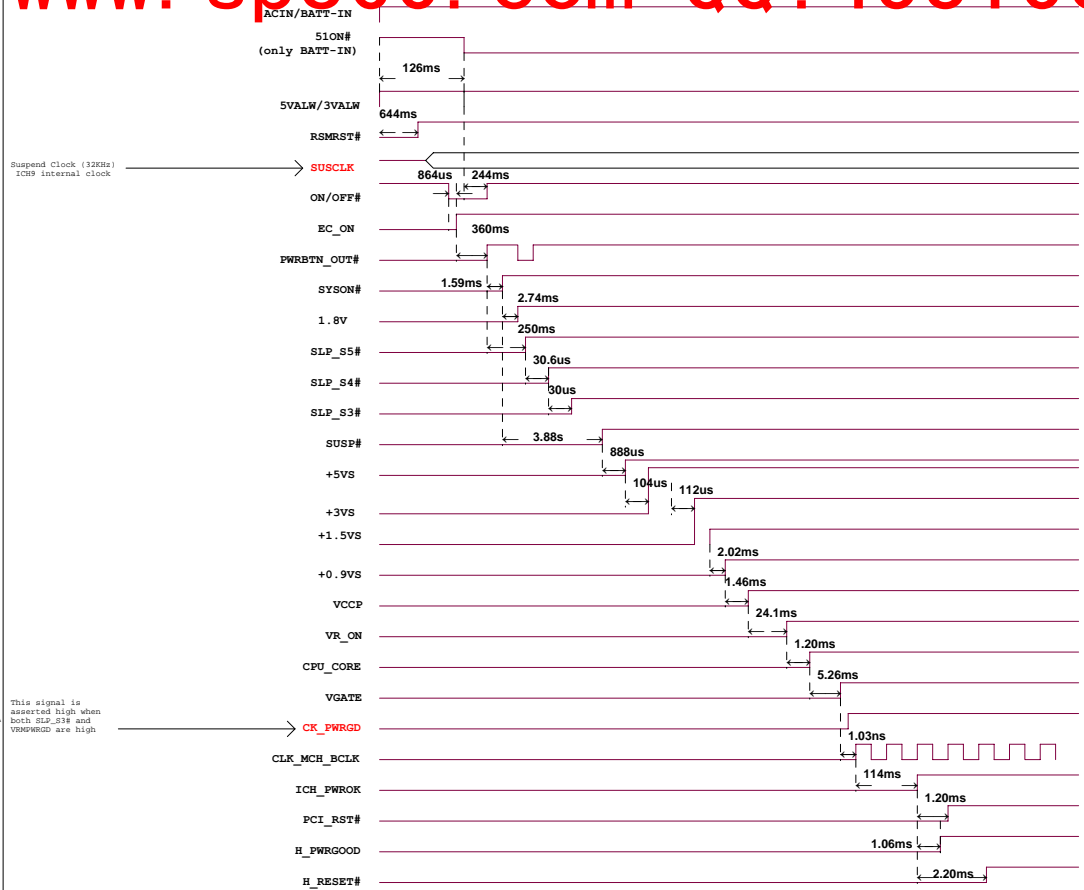


H_4P4

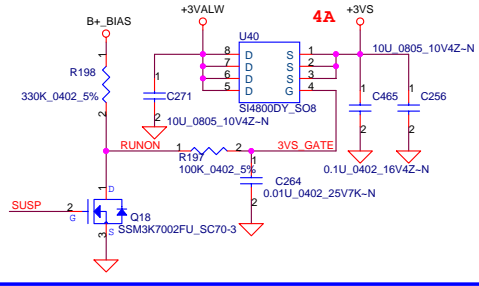
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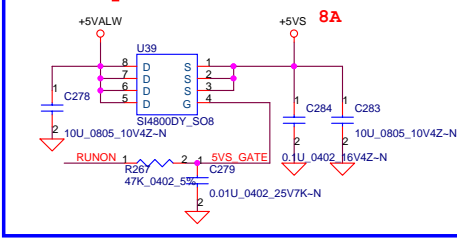


+3VALW to +3VS Transfer

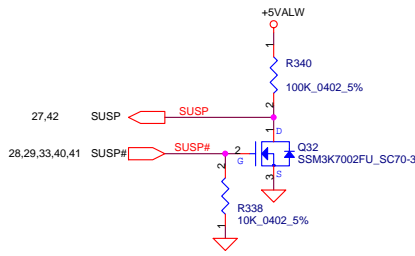
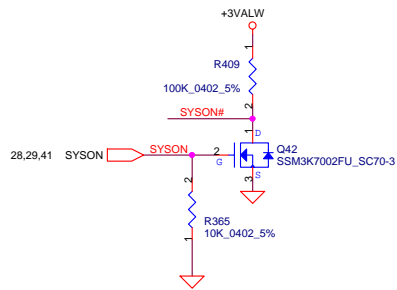
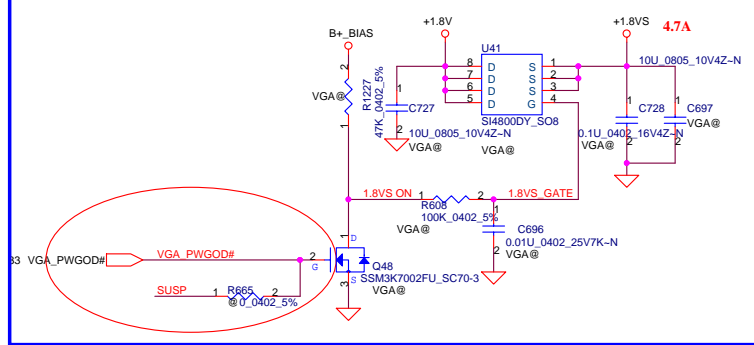


www.sp860.com QQ:453100829

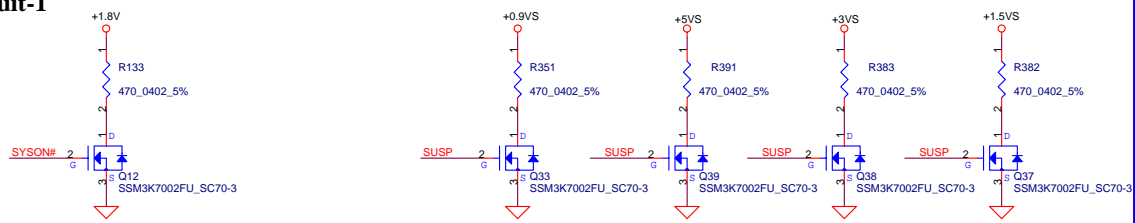
+5VALW to +5VS Transfer



+1.8VALW to +1.8VS Transfer

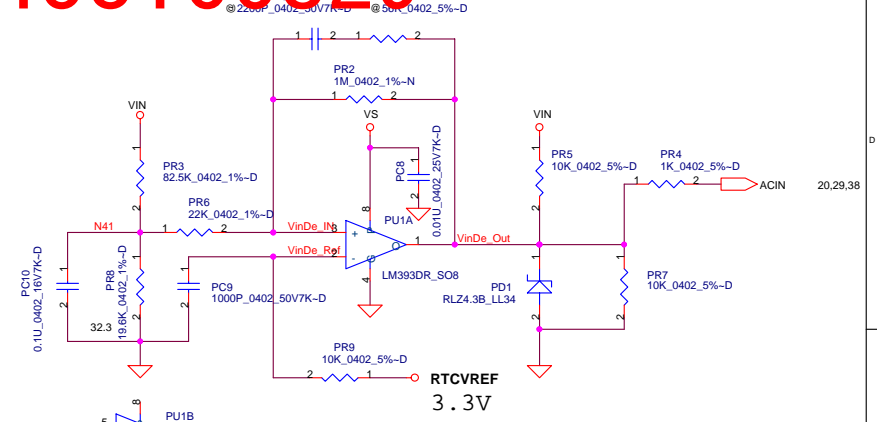
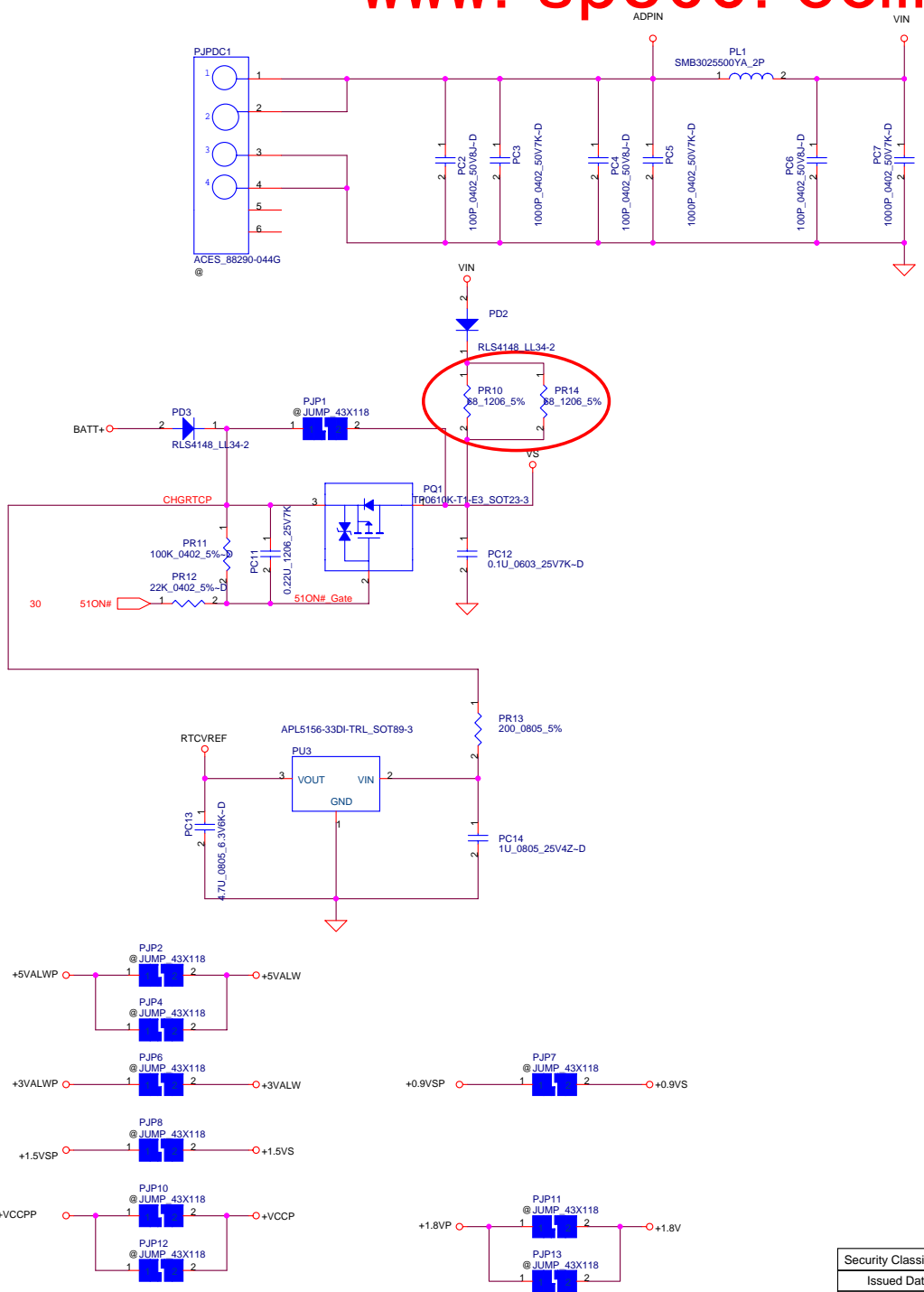


Discharge circuit-1

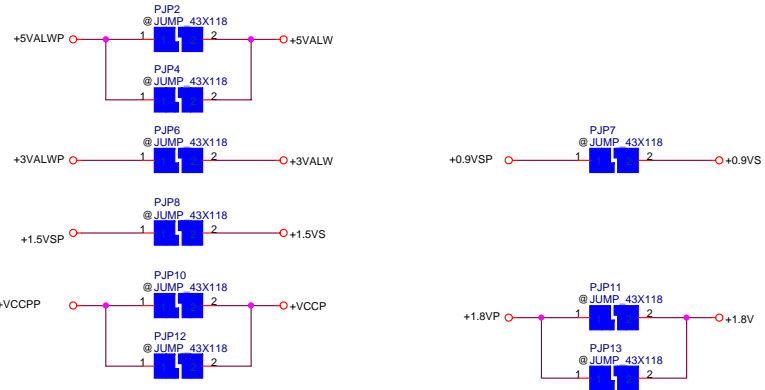


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

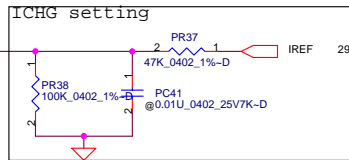
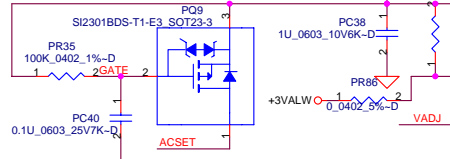
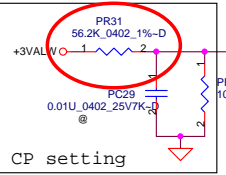
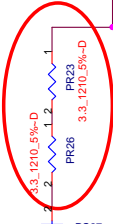
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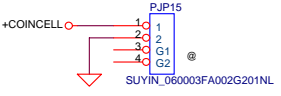
Vin Detector				
	Max.	typ.	Min.	
L-->H	18.234	17.841	17.449	
H-->L	17.597	17.210	16.813	



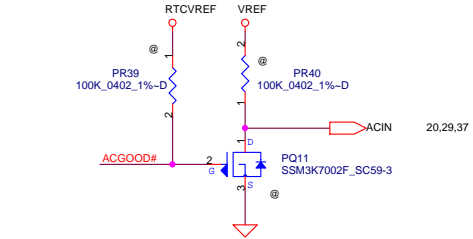
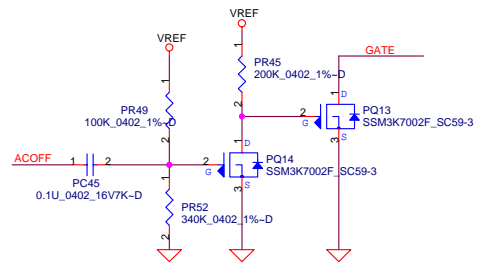
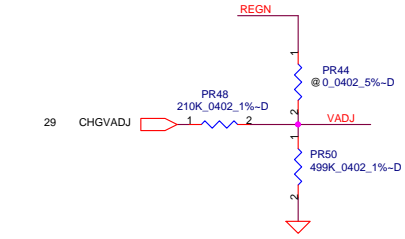
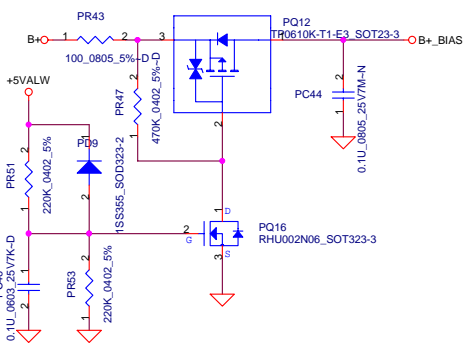
90W adapter
 $I_{charge} = (V_{rset}/V_{vdac}) * (0.1/PR222) = 3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR217) = 4.27A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



COIN RTC Battery

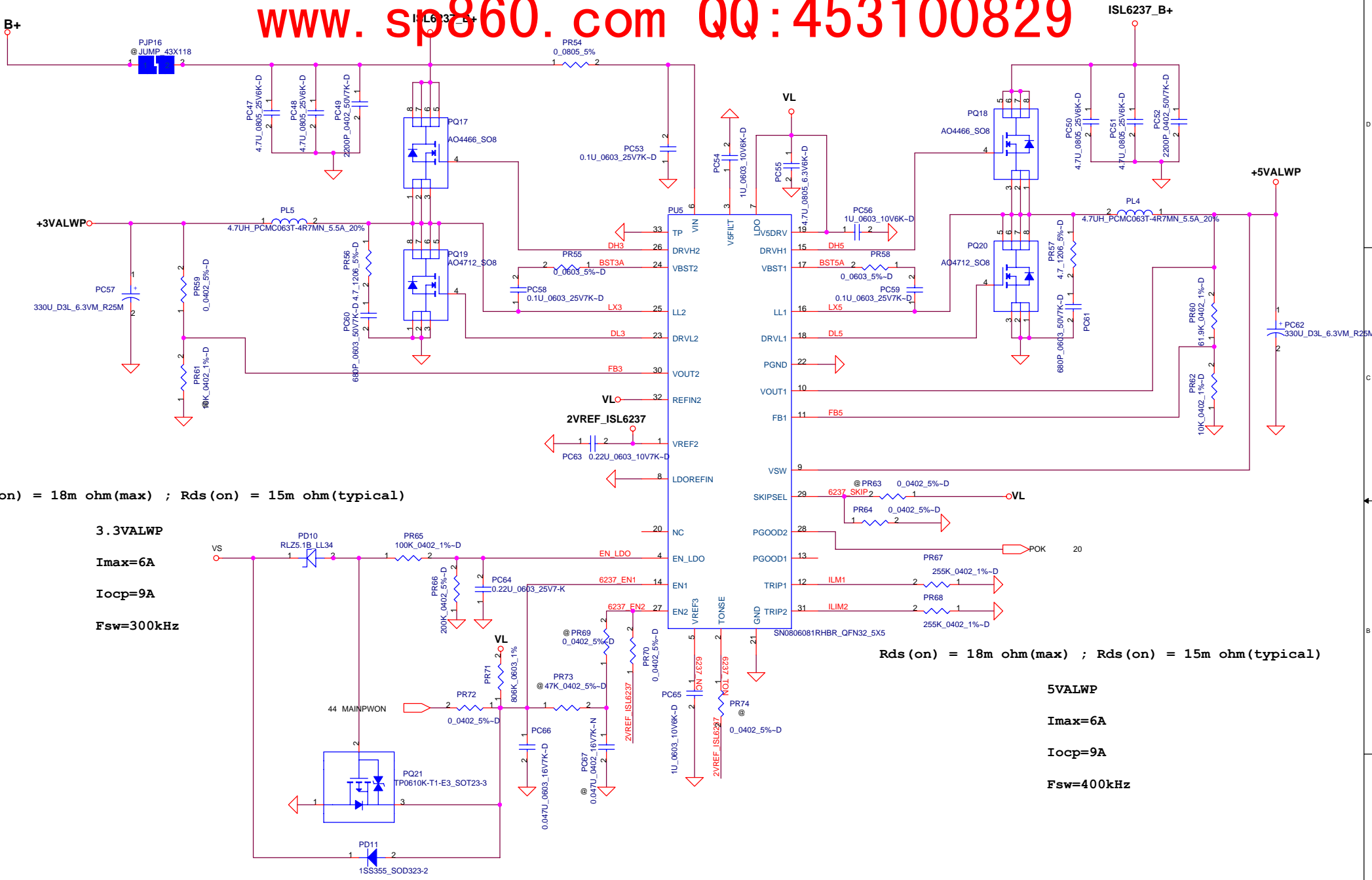


IREF	Current
0.486V	0.5A
2.916V	3A



CHGVADJ	Battery Voltage/per cell
0V	3V
3.3V	4.2V

Security Classification: Compal Secret Data
 Issued Date: 2006/10/1
 Deciphered Date: 2007/5/01
 Title: Charger
 Document Number: KFW11
 Date: Monday, December 15, 2008



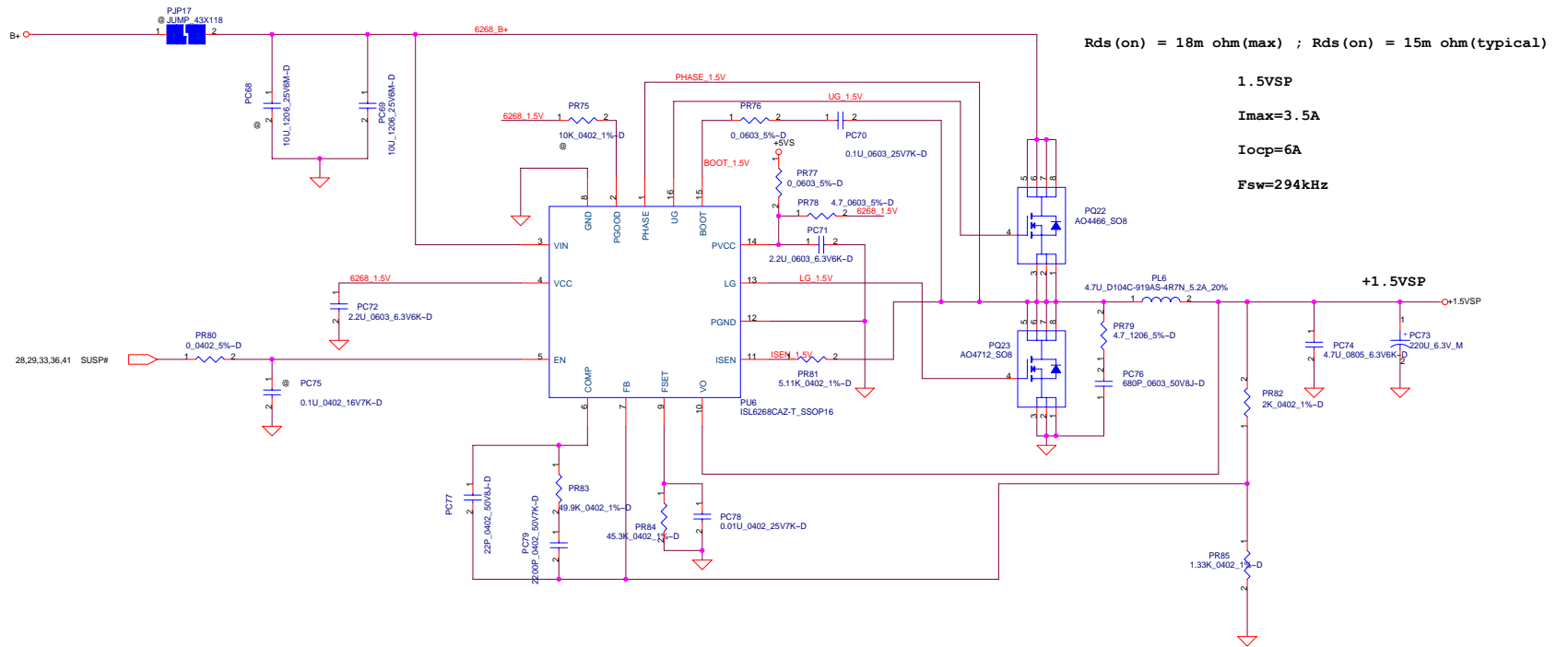
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

3. 3VALWP
 I_{max}=6A
 I_{ocp}=9A
 F_{sw}=300kHz

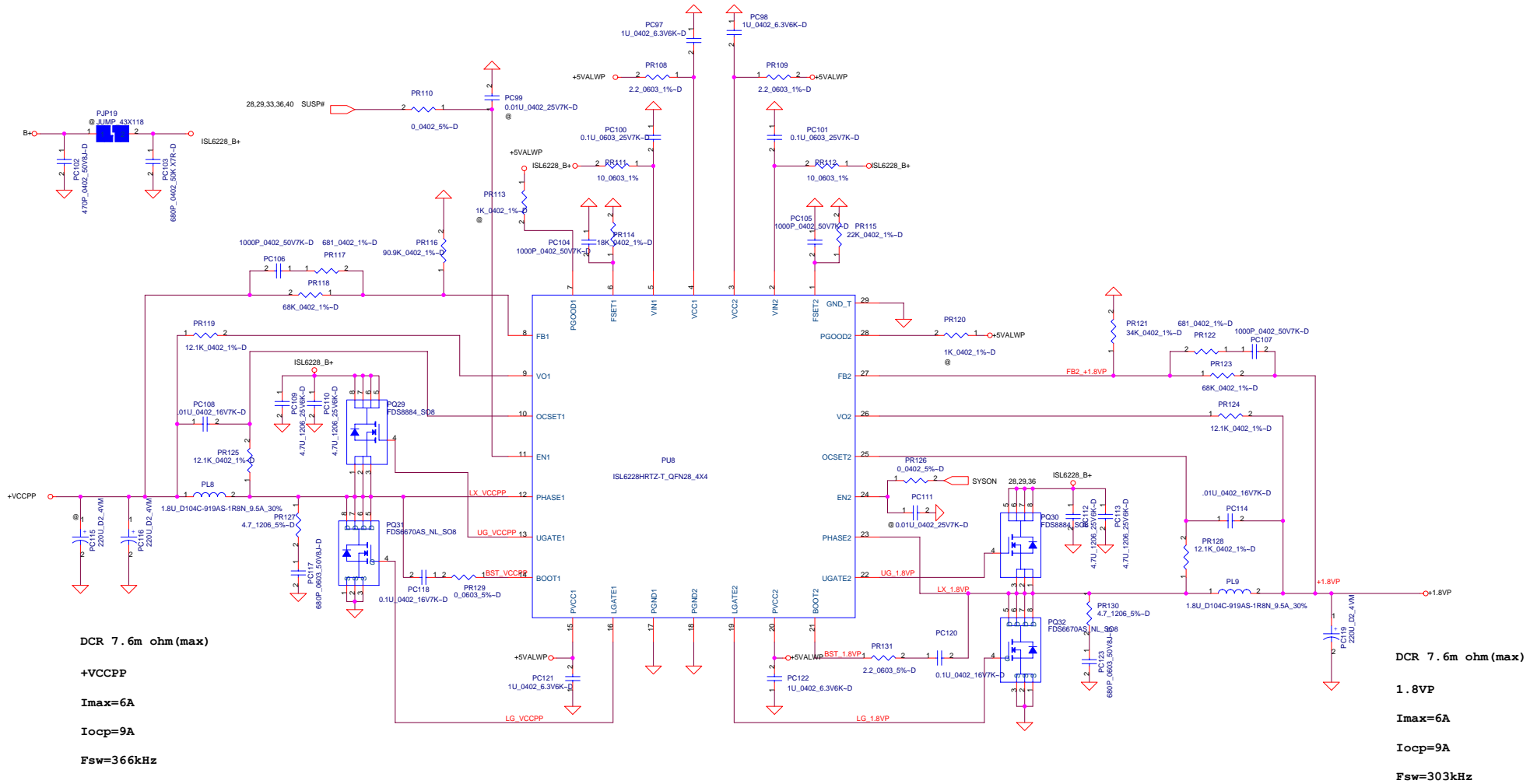
Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

5VALWP
 I_{max}=6A
 I_{ocp}=9A
 F_{sw}=400kHz

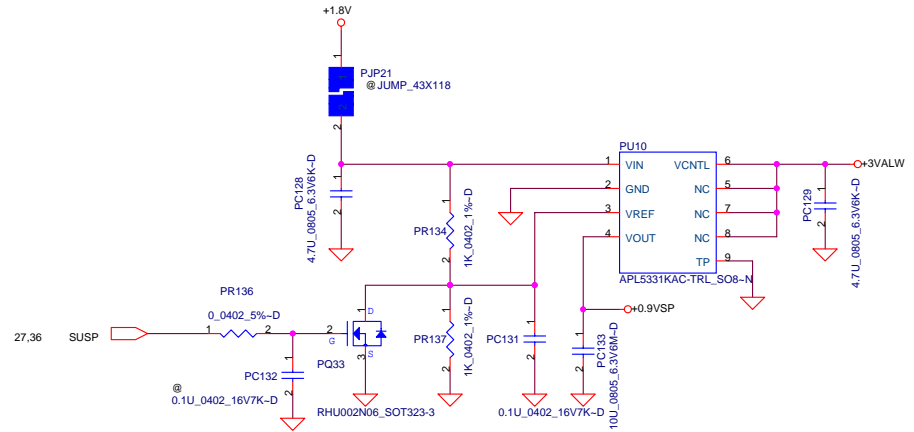
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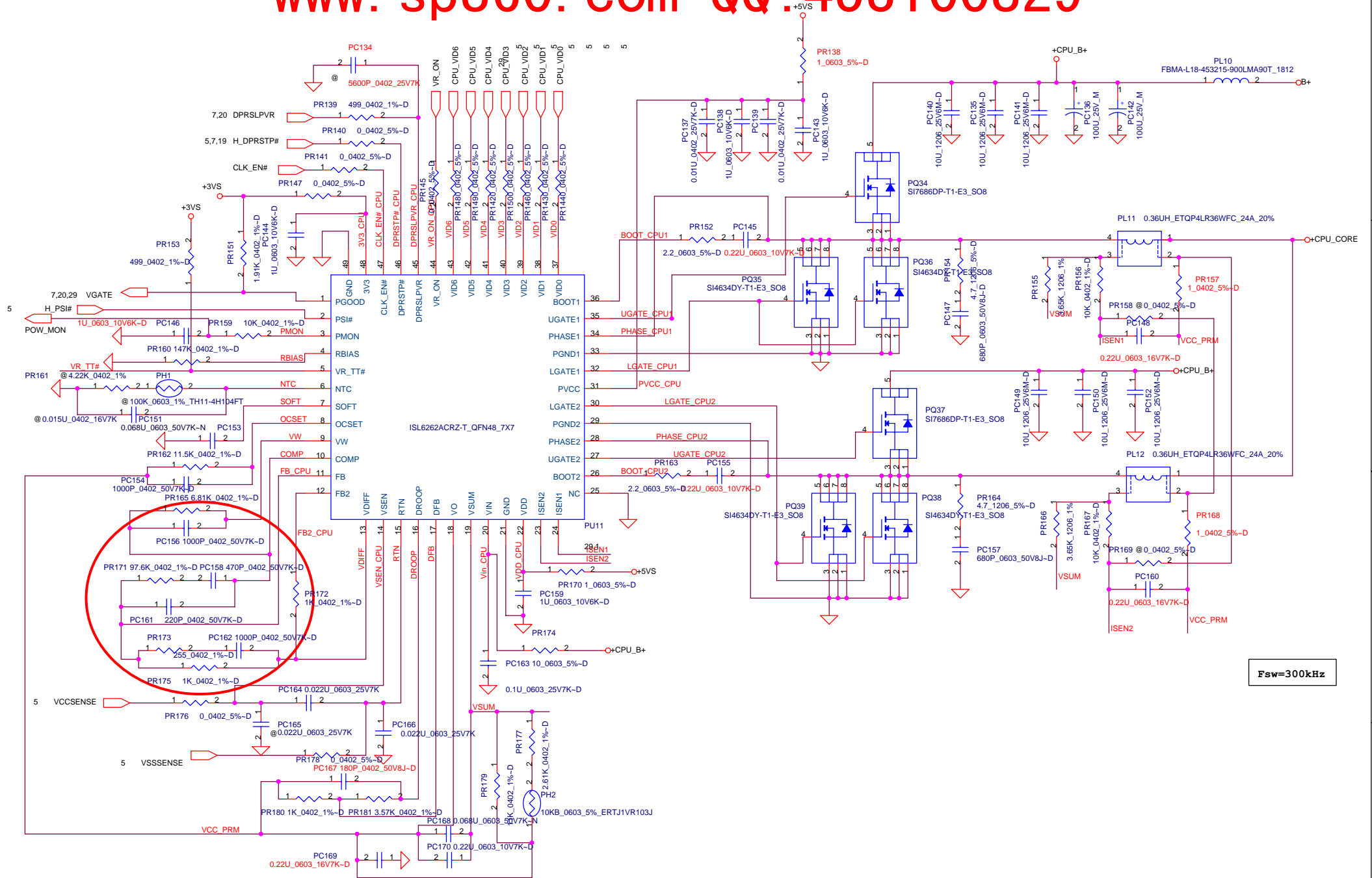
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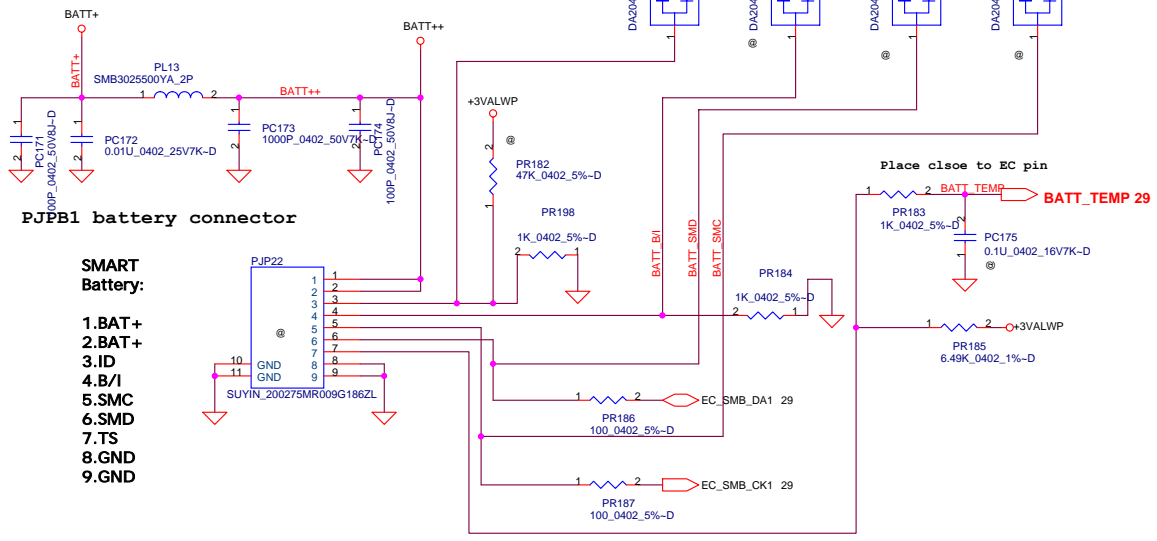


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Fsw=300kHz

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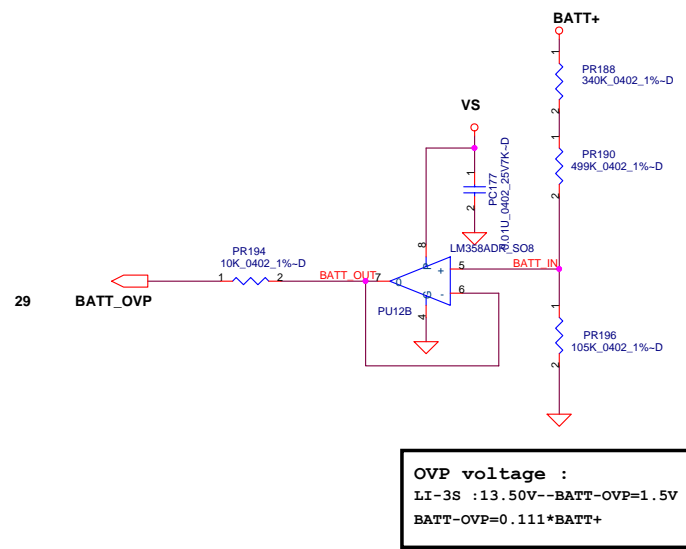


Battery Connect/OTP

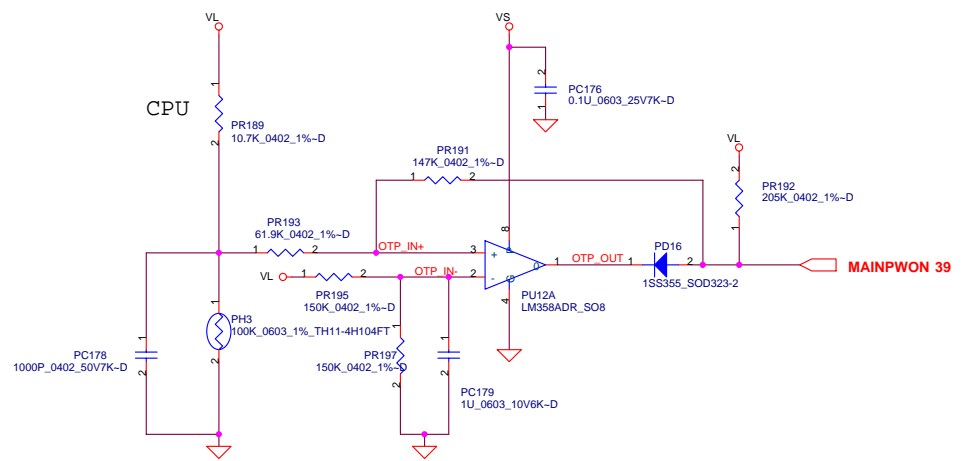
PJPB1 battery connector

- SMART Battery:
- 1.BAT +
 - 2.BAT +
 - 3.ID
 - 4.B/I
 - 5.SMC
 - 6.SMD
 - 7.TS
 - 8.GND
 - 9.GND

CPU
 PH1 under CPU botten side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C



OVP voltage :
 LI-3S :13.50V--BATT-OVP=1.5V
 BATT-OVP=0.111*BATT+



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				BATTERY CONN
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