

Compal confidential

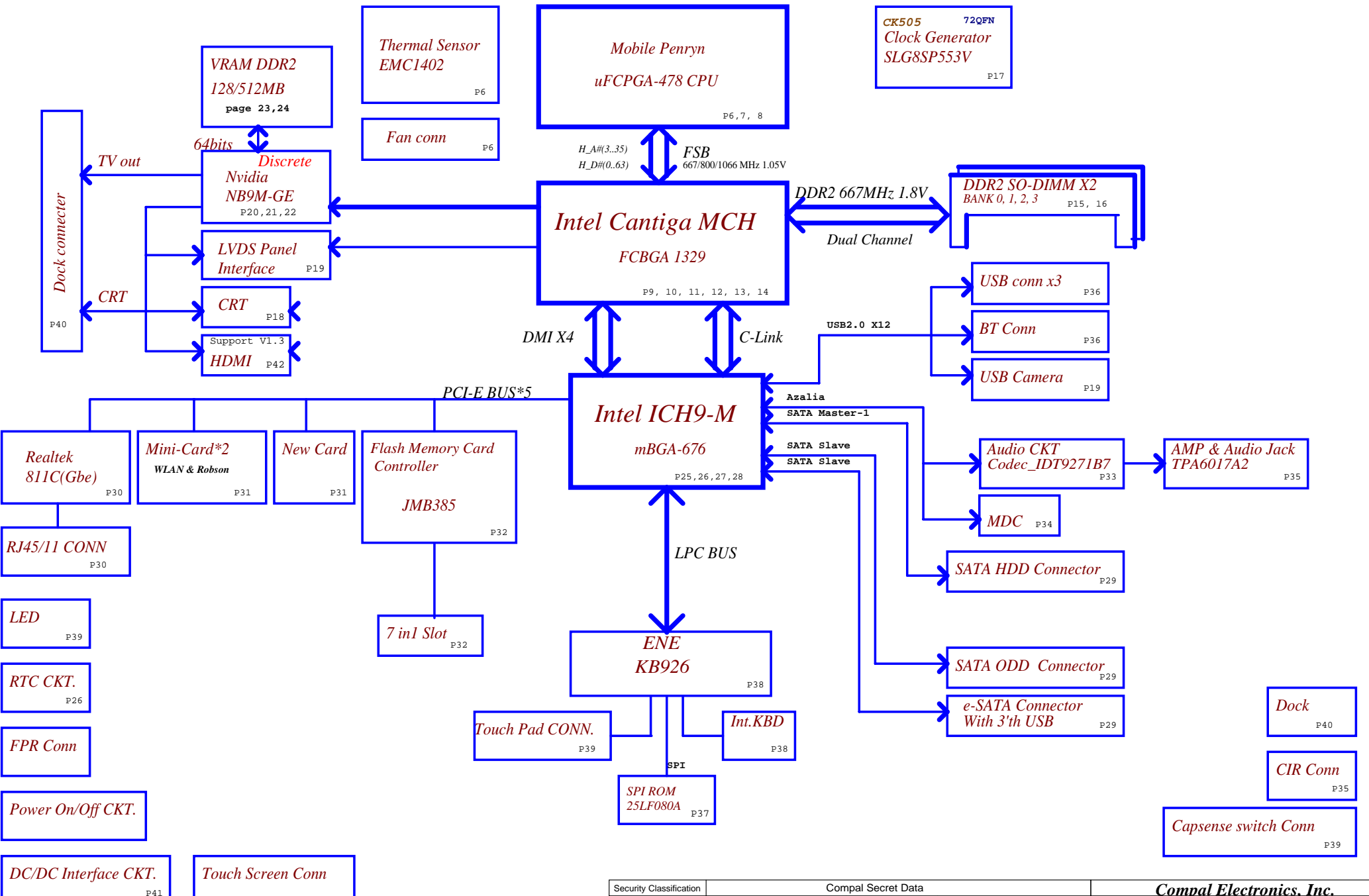
Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

2008-04-29



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Issued Date	2008/02/25	Deciphered Date	2008/04/29	Cover Sheet		
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				LA-4102P Blade discrete	1.0	
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Issued Date	2008/02/25	Deciphered Date	2008/04/29	Block Diagram	
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Voltage Rails

O MEANS ON

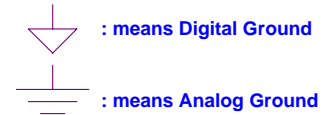
X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS +NVVDD +PCIE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM

NB	SA00002JJ80	R1	FRU
NB	SA00002JJE0	R3	
SB	SA00002JH50	R1	FRU
SB	SA00002JHB0	R3	

Symbol Note :



@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

USB assignment:

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express card
- USB-10 X
- USB-11 X

PCIe assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 GLAN (Marvell)
- PCIe-5 Card reader
- PCIe-6 New Card

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	Sensor board	NB9M Thermal Sensor	NB9M	G-sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	V	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V	V	V	X	X	X	V

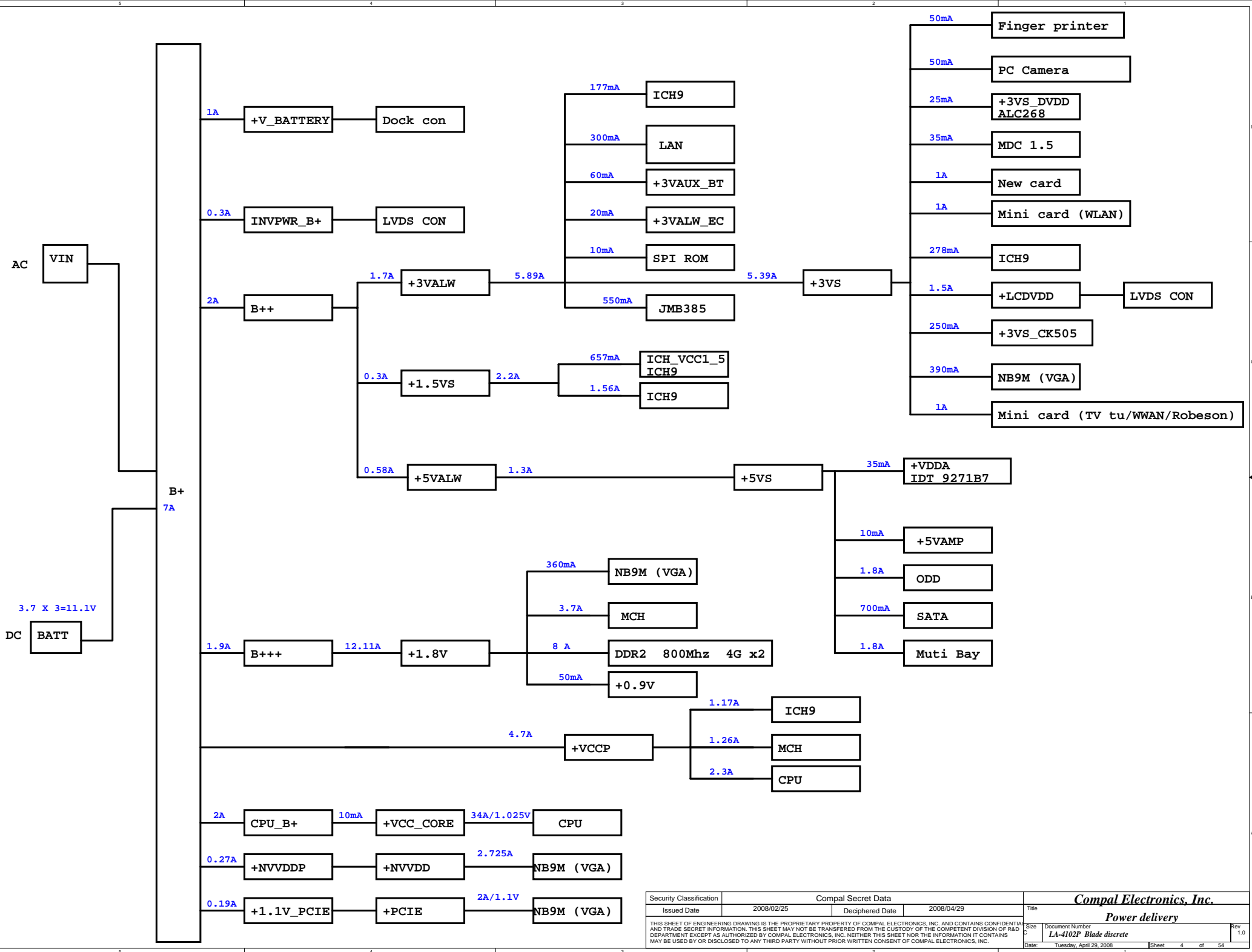
NB9M SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
DDC2_DATA DDC2_CLK	NB9M	V	X	X
3VDDCDA 3VDDCCL	NB9M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB9M	X	X	V

I2C / SMBUS ADDRESSING

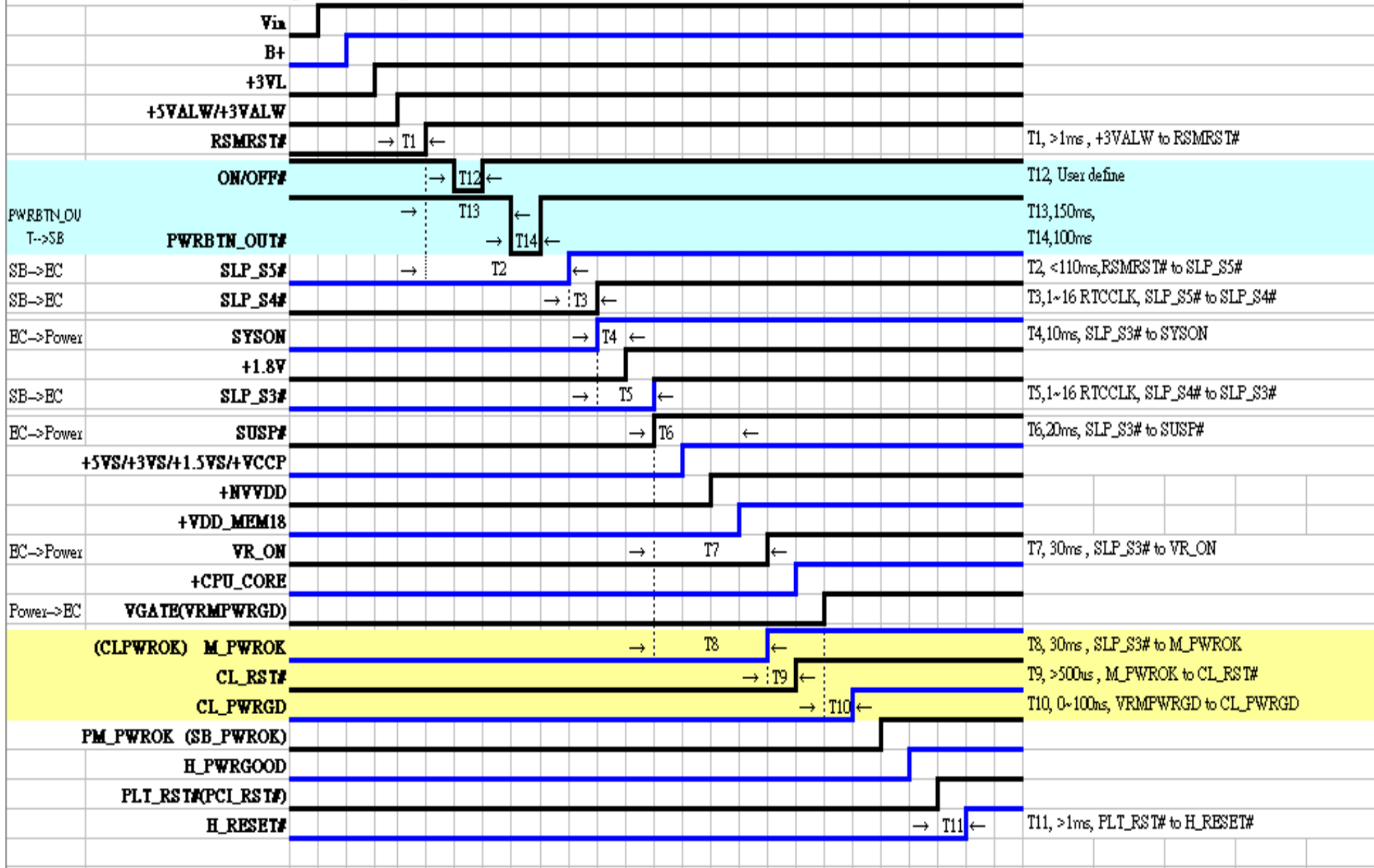
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

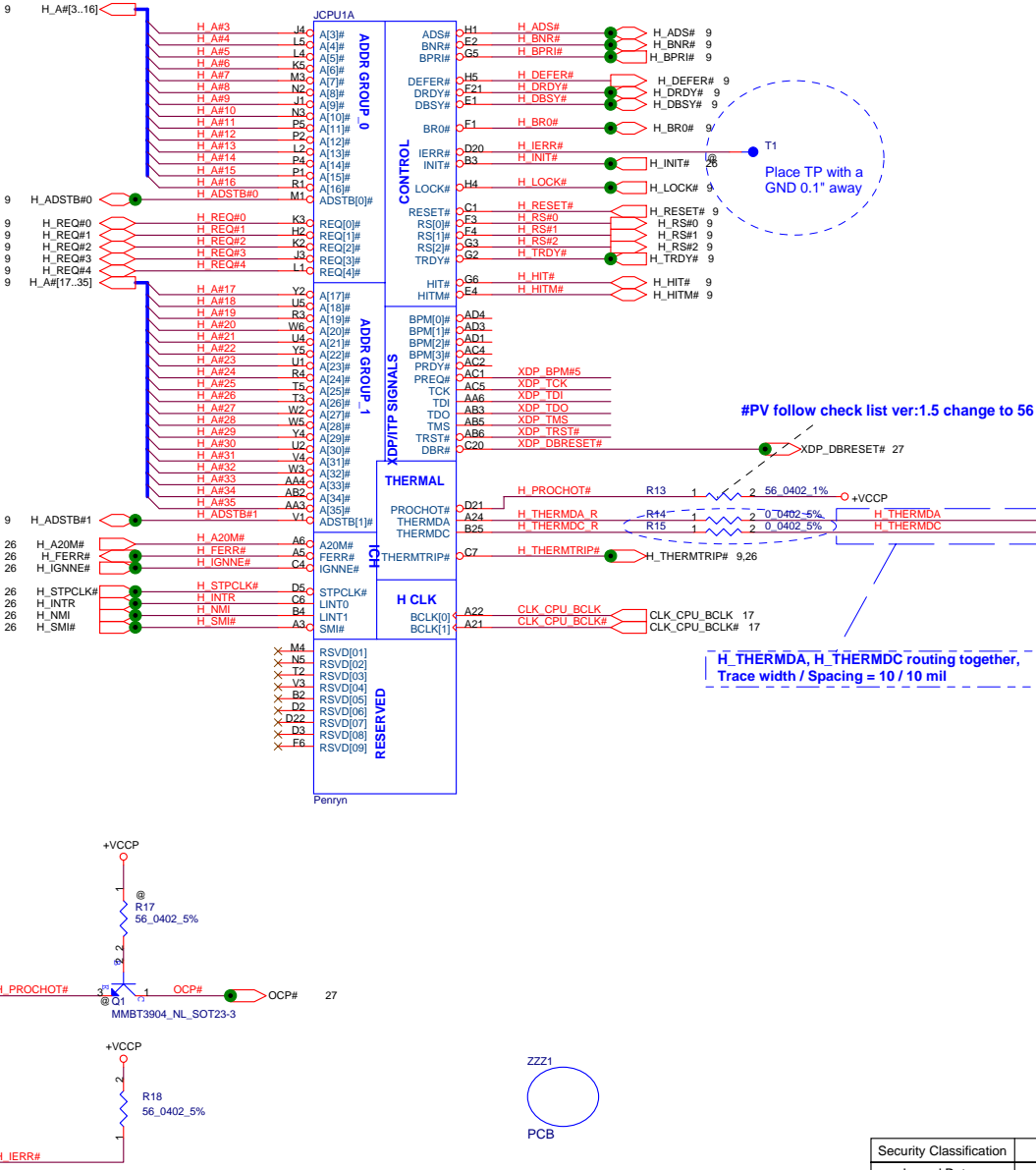
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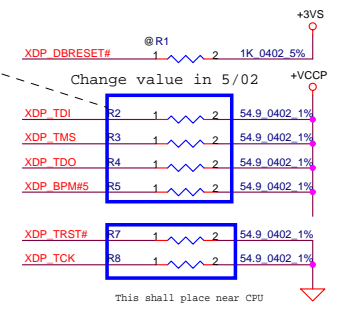
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JAL50 Discrete power sequence AC mode

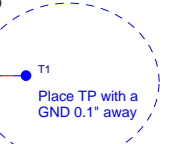




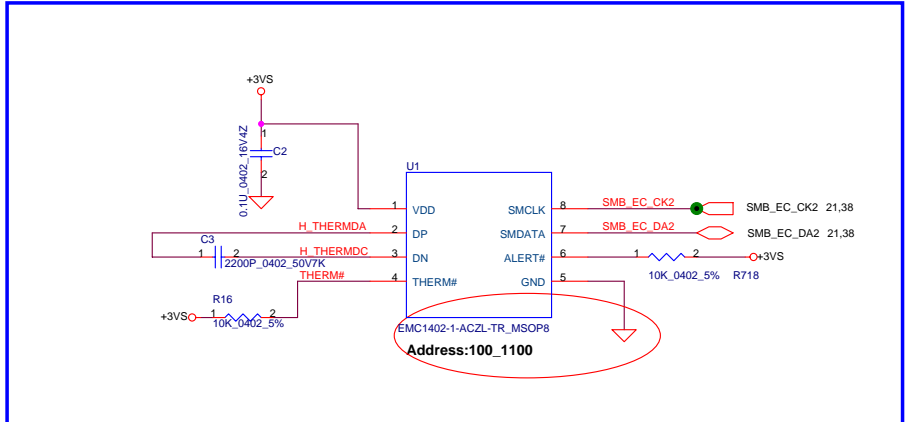
#PV follow check list ver:1.5 change to 51 ohm
 #MVfollow check list ver:2.0 change to 55 ohm



#PV2 remove XDP connector

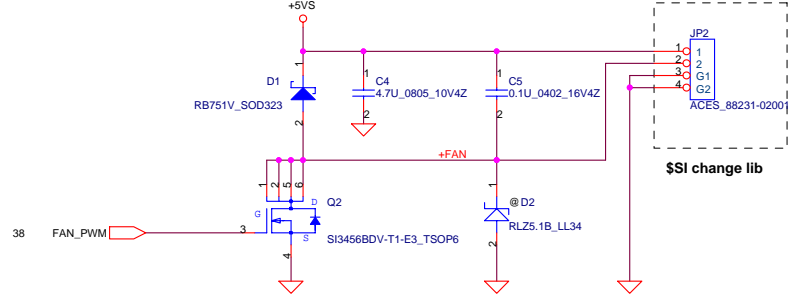


#PV follow check list ver:1.5 change to 56 ohm

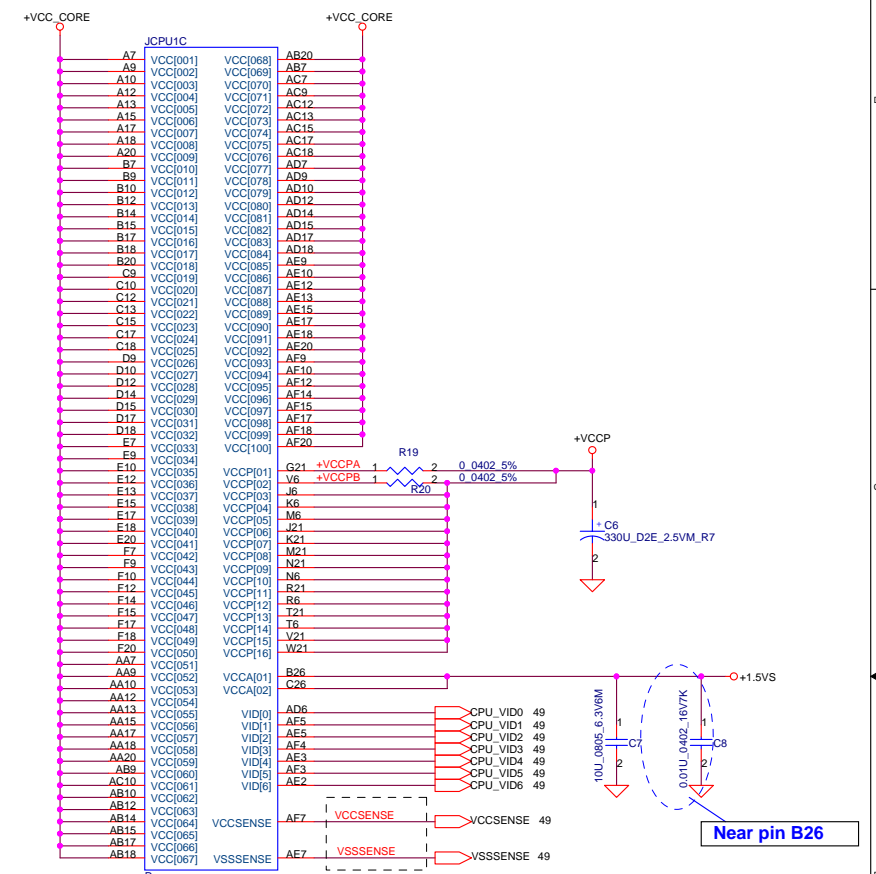
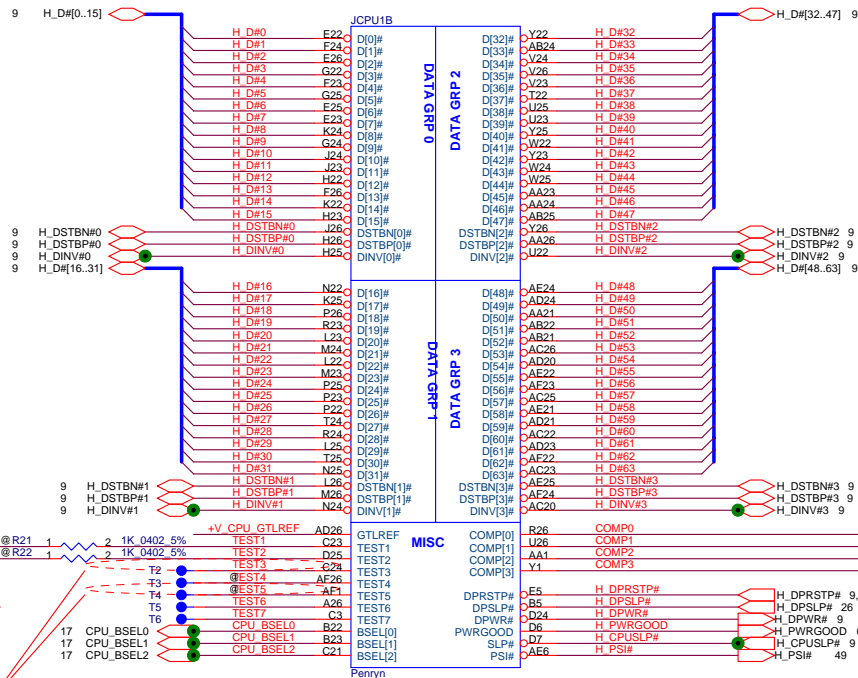


H_THERMDA, H_THERMDC routing together,
 Trace width / Spacing = 10 / 10 mil

PWM Fan Control circuit



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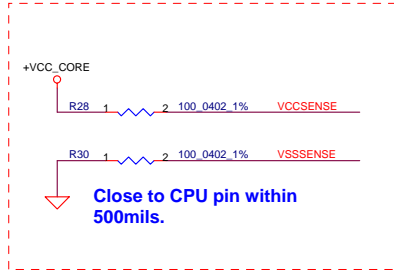
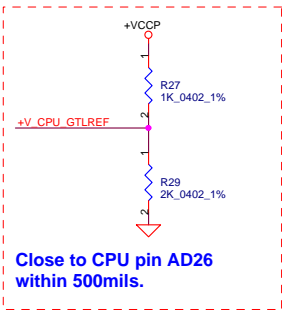


* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

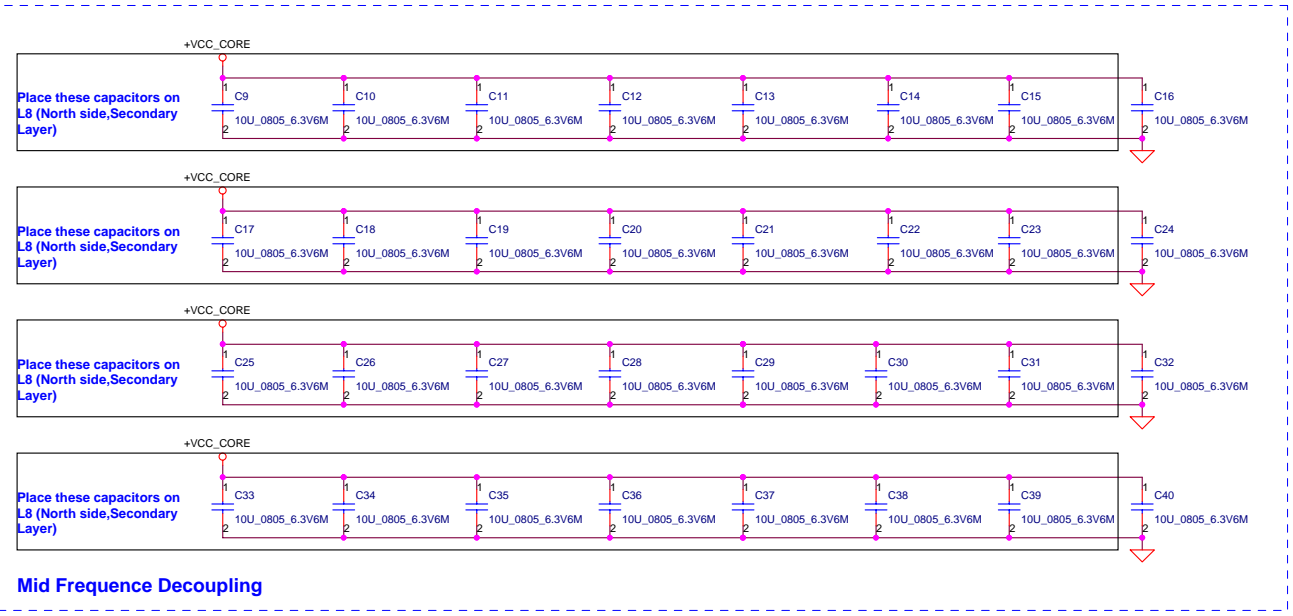
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

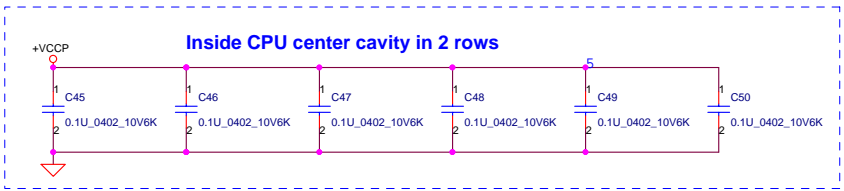
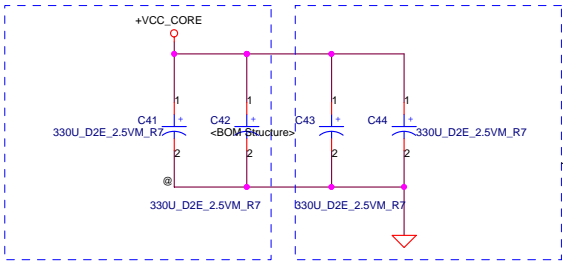
Length match within 25 mils. The trace width/space/other is 20/7/25.



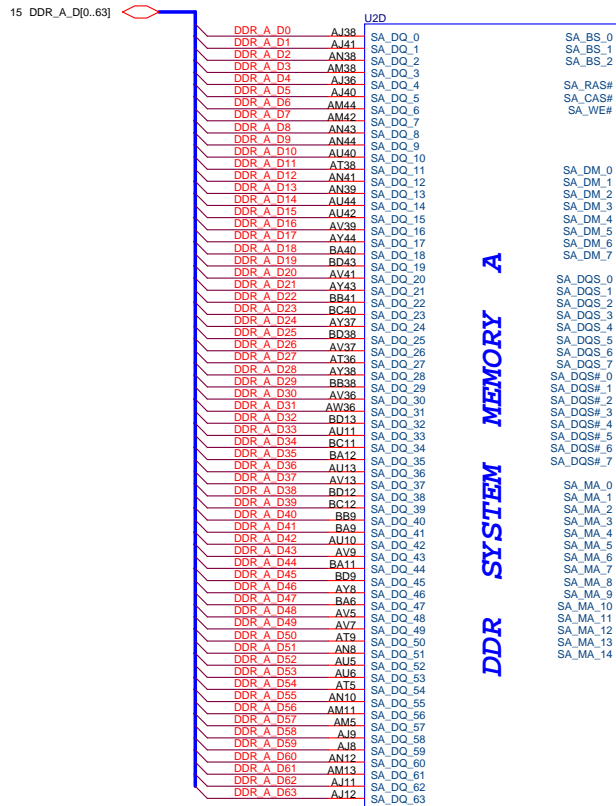
JCPU1D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R5
A16	VSS[005]	R22
A19	VSS[006]	R25
A23	VSS[007]	T1
AE2	VSS[008]	T4
B6	VSS[009]	T23
B8	VSS[010]	T26
B11	VSS[011]	U3
B13	VSS[012]	U6
B16	VSS[013]	U21
B19	VSS[014]	U24
B21	VSS[015]	V5
B24	VSS[016]	V22
C5	VSS[017]	V25
C8	VSS[018]	V26
C11	VSS[019]	V1
C14	VSS[020]	V4
C16	VSS[021]	V23
C19	VSS[022]	V26
C2	VSS[023]	V3
C22	VSS[024]	V6
C25	VSS[025]	V21
D1	VSS[026]	V24
D4	VSS[027]	V8
D8	VSS[028]	V9
D11	VSS[029]	V10
D13	VSS[030]	V11
D16	VSS[031]	V12
D19	VSS[032]	V13
D23	VSS[033]	V14
D26	VSS[034]	V15
E3	VSS[035]	V16
E6	VSS[036]	V17
ER	VSS[037]	V18
E11	VSS[038]	V19
E14	VSS[039]	V20
E16	VSS[040]	V21
E19	VSS[041]	V22
E21	VSS[042]	V23
E24	VSS[043]	V24
F5	VSS[044]	V25
F8	VSS[045]	V26
F11	VSS[046]	V27
F13	VSS[047]	V28
F16	VSS[048]	V29
F19	VSS[049]	V30
F2	VSS[050]	V31
F25	VSS[051]	V32
F22	VSS[052]	V33
G4	VSS[053]	V34
G1	VSS[054]	V35
G23	VSS[055]	V36
G26	VSS[056]	V37
H3	VSS[057]	V38
H6	VSS[058]	V39
H21	VSS[059]	V40
H24	VSS[060]	V41
J2	VSS[061]	V42
J5	VSS[062]	V43
J22	VSS[063]	V44
J25	VSS[064]	V45
K1	VSS[065]	V46
K4	VSS[066]	V47
K23	VSS[067]	V48
K26	VSS[068]	V49
L3	VSS[069]	V50
L6	VSS[070]	V51
L21	VSS[071]	V52
L24	VSS[072]	V53
M2	VSS[073]	V54
M5	VSS[074]	V55
M22	VSS[075]	V56
M25	VSS[076]	V57
N1	VSS[077]	V58
N4	VSS[078]	V59
N23	VSS[079]	V60
N26	VSS[080]	V61
P3	VSS[081]	V62
	VSS[081]	V62
	VSS[163]	



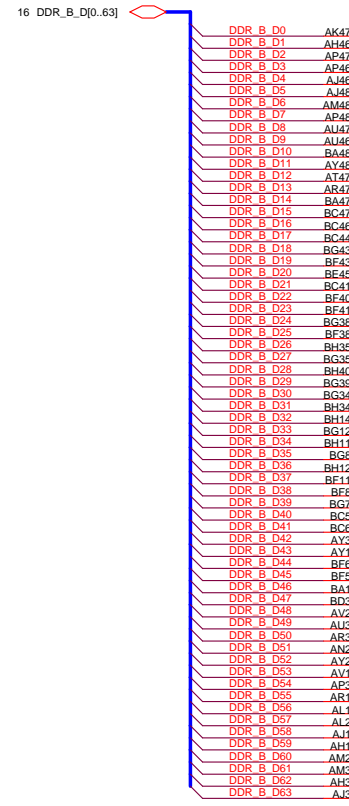
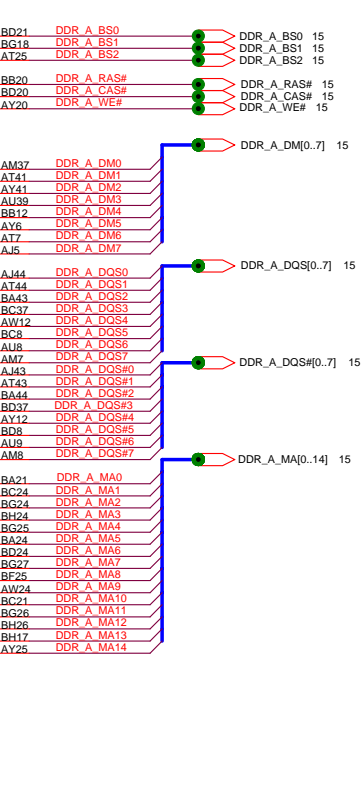
Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



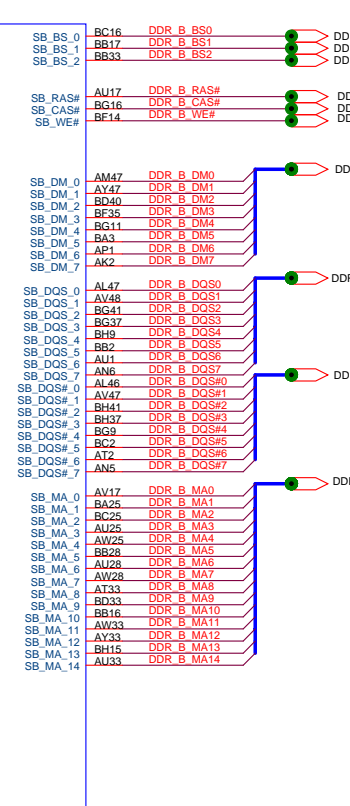
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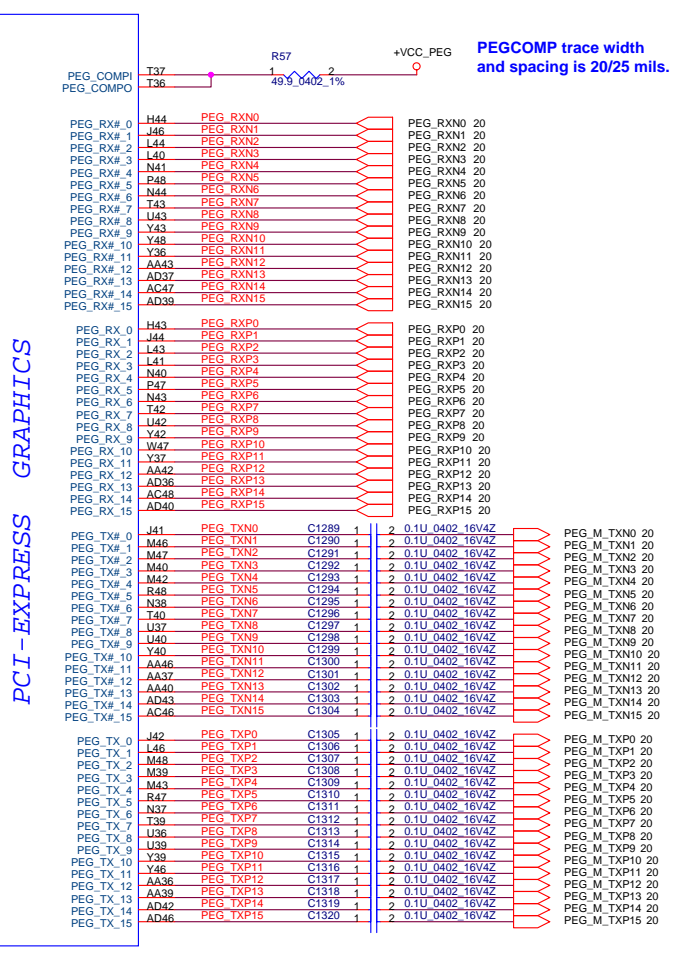
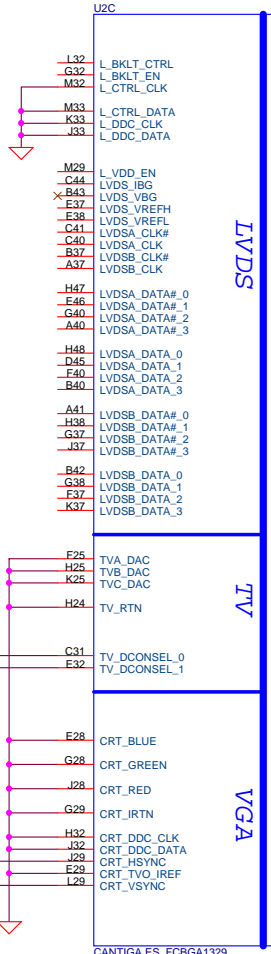
CANTIGA ES_FCBGA1329



CANTIGA ES_FCBGA1329

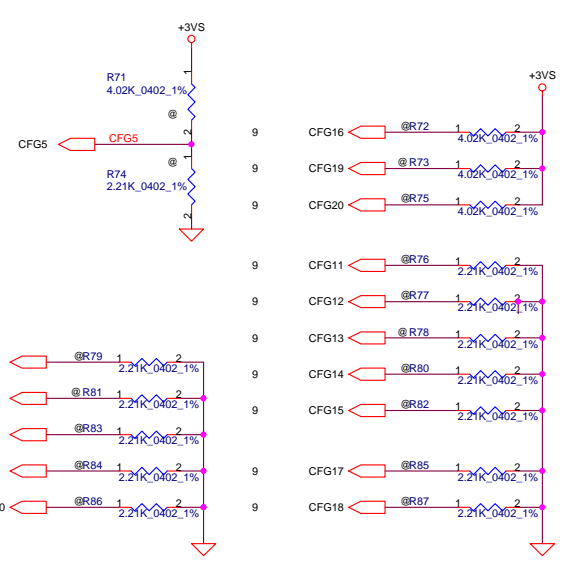


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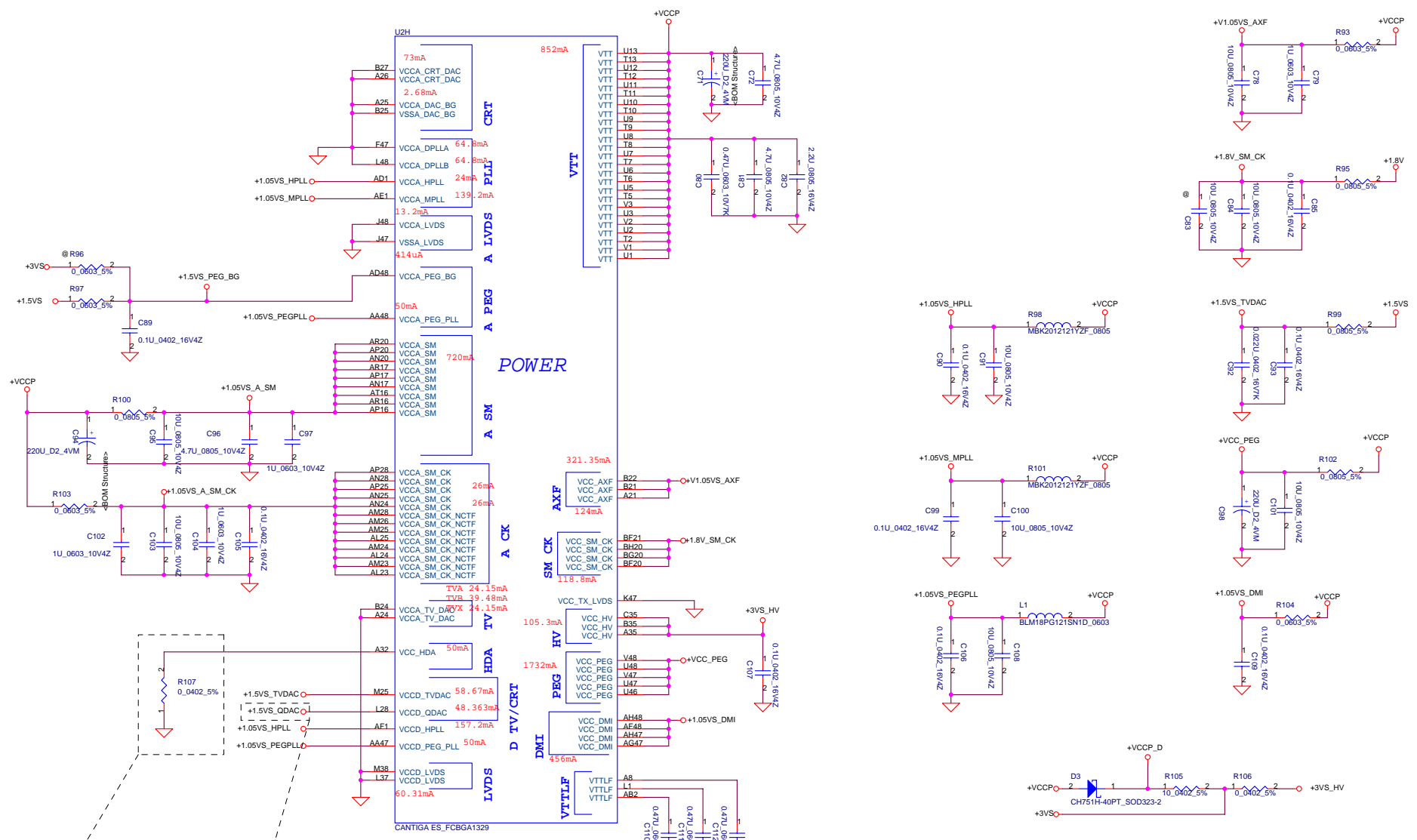


Strap Pin Table

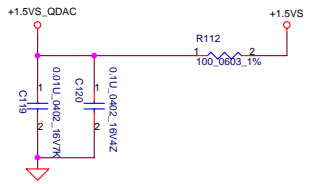
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable 1 = The ITPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



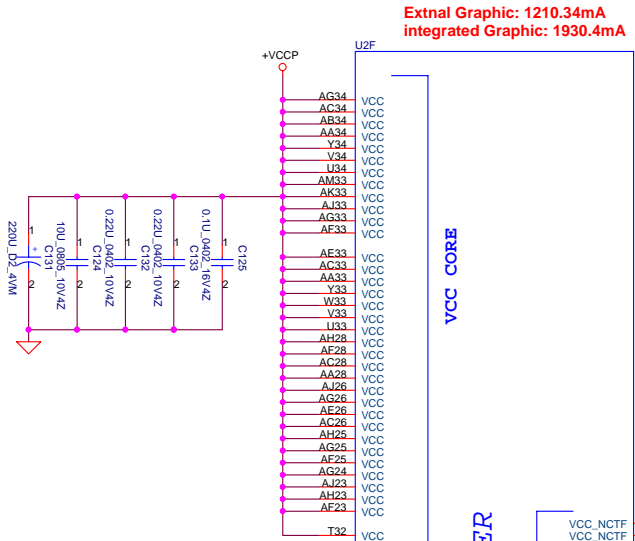
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#SI discrete don't use HDA #SI VCCD_QDAC connect to 1.5VS

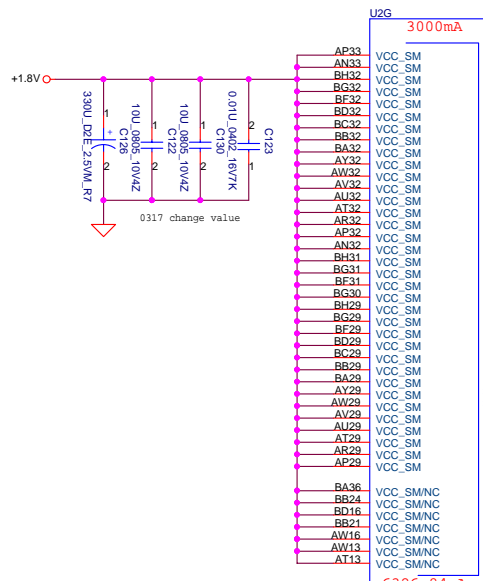


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Extral Graphic: 1210.34mA
Integrated Graphic: 1930.4mA

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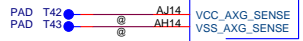


U2G
3000mA

CANTIGA ES_FCBGA1329

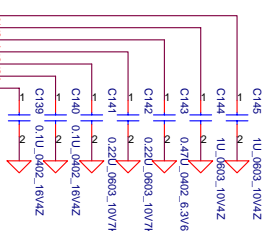
- VCC_NCTF AM32
- VCC_NCTF AK32
- VCC_NCTF AJ32
- VCC_NCTF AH32
- VCC_NCTF AG32
- VCC_NCTF AA32
- VCC_NCTF W32
- VCC_NCTF U32
- VCC_NCTF AM30
- VCC_NCTF AL30
- VCC_NCTF AH30
- VCC_NCTF AG30
- VCC_NCTF AF30
- VCC_NCTF AE30
- VCC_NCTF AC30
- VCC_NCTF AB30
- VCC_NCTF AA30
- VCC_NCTF Y30
- VCC_NCTF W30
- VCC_NCTF V30
- VCC_NCTF U30
- VCC_NCTF AL29
- VCC_NCTF AK29
- VCC_NCTF AJ29
- VCC_NCTF AH29
- VCC_NCTF AG29
- VCC_NCTF AE29
- VCC_NCTF AC29
- VCC_NCTF AA29
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- VCC_NCTF AK25
- VCC_NCTF AK24
- VCC_NCTF AK23

- V26 VCC_AXG
- AE25 VCC_AXG
- AB25 VCC_AXG
- AA25 VCC_AXG
- AE24 VCC_AXG
- AC24 VCC_AXG
- AA24 VCC_AXG
- Y24 VCC_AXG
- AE23 VCC_AXG
- AC23 VCC_AXG
- AB23 VCC_AXG
- AA23 VCC_AXG
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- AA21 VCC_AXG
- Y21 VCC_AXG
- AF20 VCC_AXG
- AE20 VCC_AXG
- AC20 VCC_AXG
- AB20 VCC_AXG
- AA20 VCC_AXG
- T17 VCC_AXG
- T16 VCC_AXG
- AM15 VCC_AXG
- AL15 VCC_AXG
- AE15 VCC_AXG
- AJ15 VCC_AXG
- AH15 VCC_AXG
- AG15 VCC_AXG
- AF15 VCC_AXG
- AB15 VCC_AXG
- AA15 VCC_AXG
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- AM14 VCC_AXG
- U14 VCC_AXG
- T14 VCC_AXG

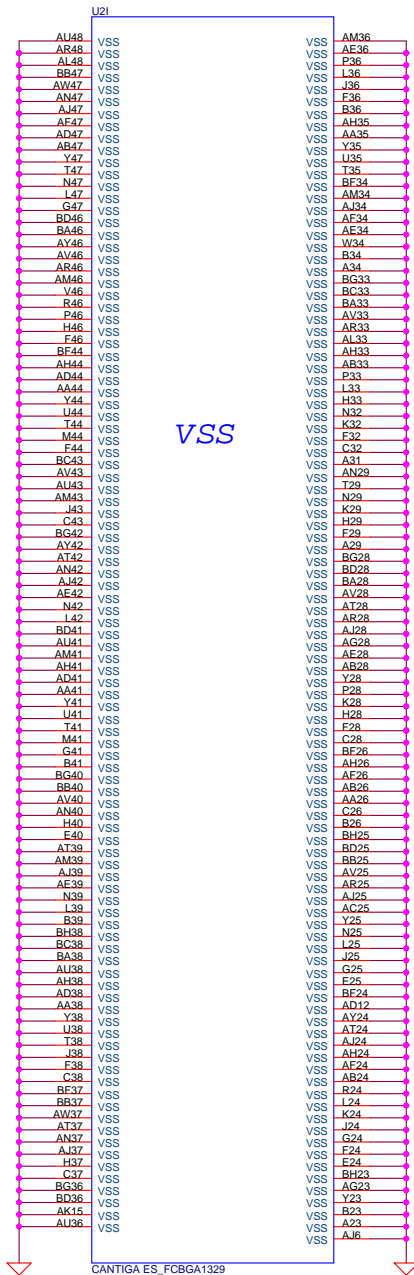


- VCC_AXG_NCTF W28
- VCC_AXG_NCTF W28
- VCC_AXG_NCTF W26
- VCC_AXG_NCTF W26
- VCC_AXG_NCTF W25
- VCC_AXG_NCTF W25
- VCC_AXG_NCTF W24
- VCC_AXG_NCTF W24
- VCC_AXG_NCTF W23
- VCC_AXG_NCTF W23
- VCC_AXG_NCTF AM21
- VCC_AXG_NCTF AL21
- VCC_AXG_NCTF AK21
- VCC_AXG_NCTF W21
- VCC_AXG_NCTF U21
- VCC_AXG_NCTF AM20
- VCC_AXG_NCTF W20
- VCC_AXG_NCTF U20
- VCC_AXG_NCTF AM19
- VCC_AXG_NCTF AL19
- VCC_AXG_NCTF Y19
- VCC_AXG_NCTF AJ19
- VCC_AXG_NCTF AH19
- VCC_AXG_NCTF AG19
- VCC_AXG_NCTF AE19
- VCC_AXG_NCTF AB19
- VCC_AXG_NCTF AA19
- VCC_AXG_NCTF Y19
- VCC_AXG_NCTF W19
- VCC_AXG_NCTF V19
- VCC_AXG_NCTF U19
- VCC_AXG_NCTF AM17
- VCC_AXG_NCTF AK17
- VCC_AXG_NCTF AH17
- VCC_AXG_NCTF AG17
- VCC_AXG_NCTF AE17
- VCC_AXG_NCTF AE17
- VCC_AXG_NCTF AC17
- VCC_AXG_NCTF AB17
- VCC_AXG_NCTF Y17
- VCC_AXG_NCTF W17
- VCC_AXG_NCTF V17
- VCC_AXG_NCTF AM16
- VCC_AXG_NCTF AL16
- VCC_AXG_NCTF AK16
- VCC_AXG_NCTF AJ16
- VCC_AXG_NCTF AH16
- VCC_AXG_NCTF AG16
- VCC_AXG_NCTF AE16
- VCC_AXG_NCTF AC16
- VCC_AXG_NCTF AB16
- VCC_AXG_NCTF AA16
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- VCC_AXG_NCTF W16
- VCC_AXG_NCTF V16
- VCC_AXG_NCTF U16

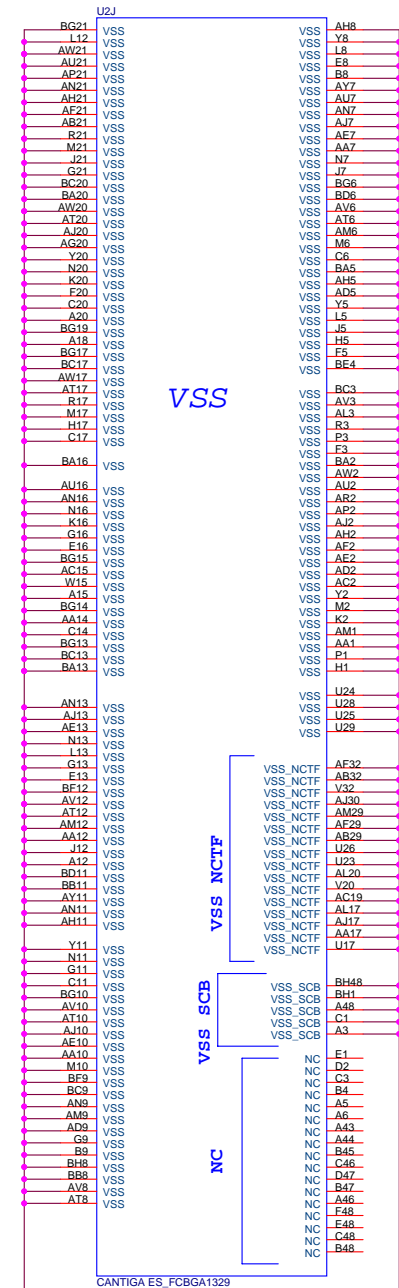
- VCC_SM_LF AV44 VCCSM_LF1
- VCC_SM_LF BA37 VCCSM_LF2
- VCC_SM_LF AM40 VCCSM_LF3
- VCC_SM_LF AV21 VCCSM_LF4
- VCC_SM_LF AY5 VCCSM_LF5
- VCC_SM_LF AM10 VCCSM_LF6
- VCC_SM_LF BB13 VCCSM_LF7



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Date:	Monday, May 12, 2008	Sheet	13	of	54	



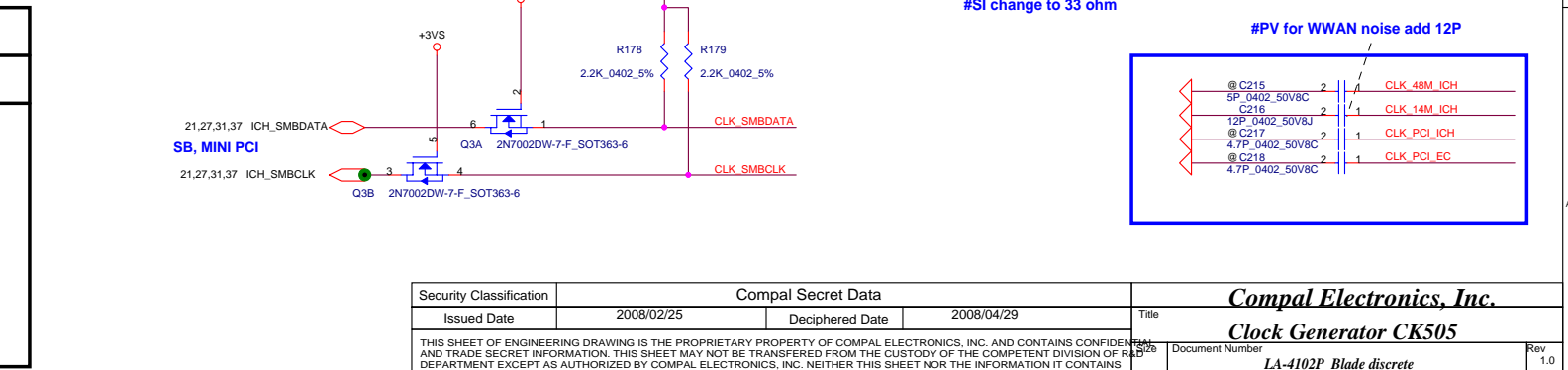
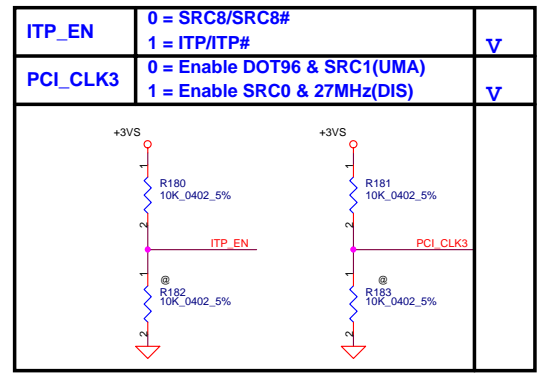
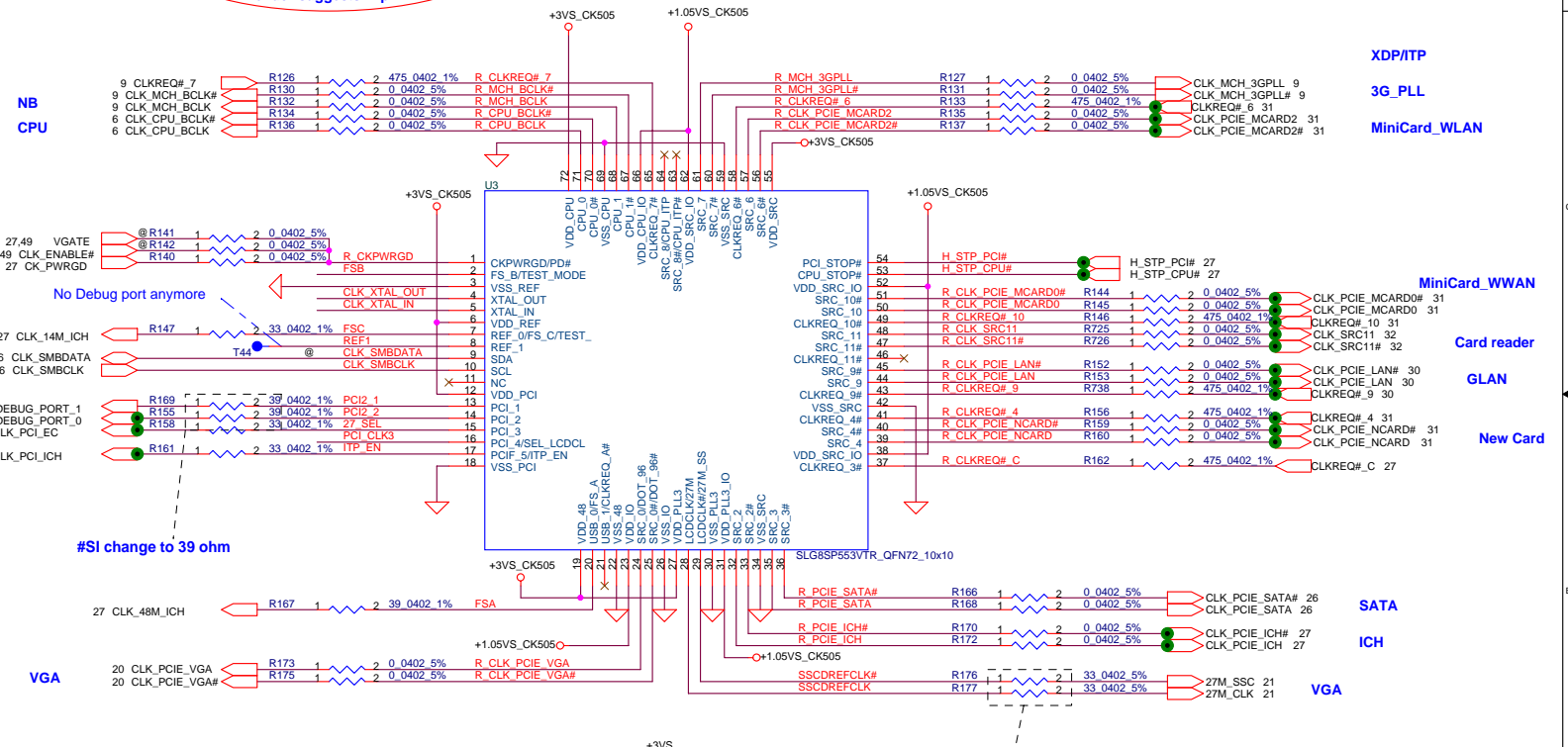
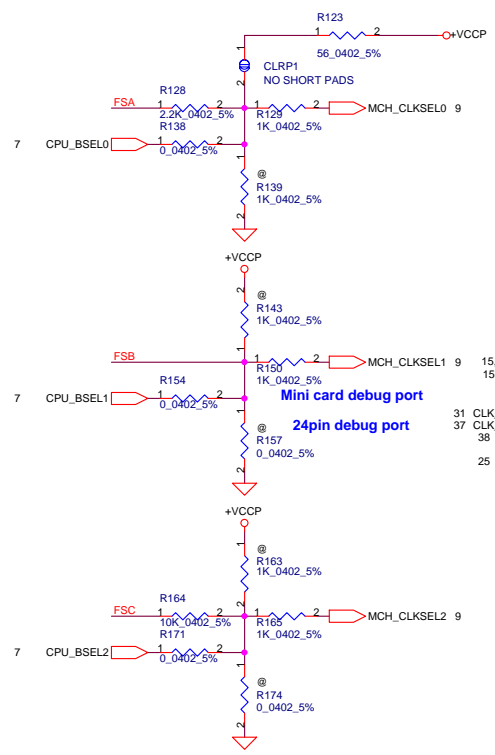
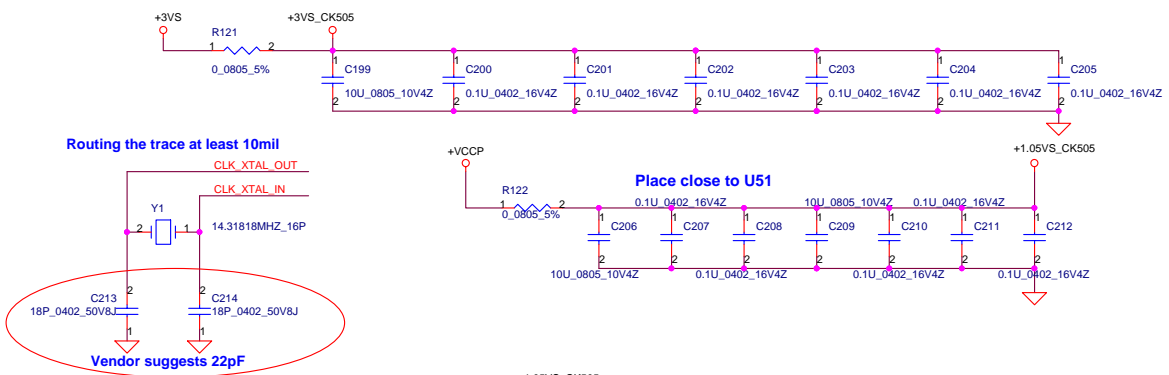
CANTIGA ES_FCBGA1329



CANTIGA ES_FCBGA1329

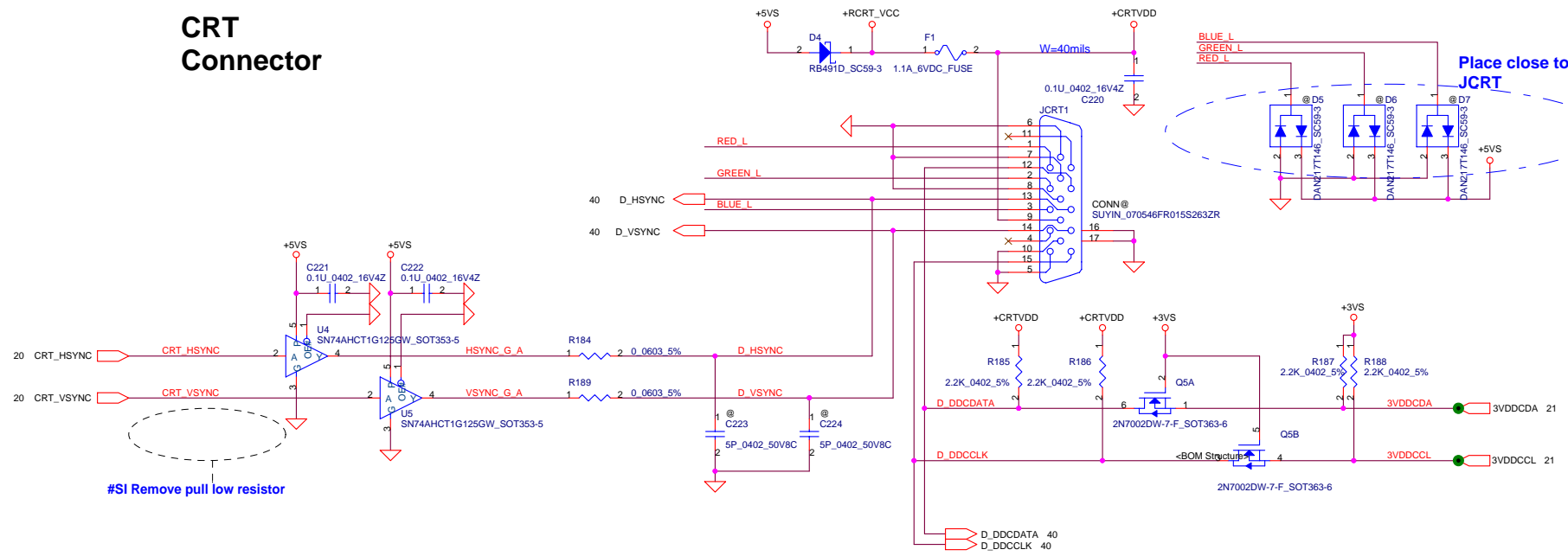
Security Classification		Compal Secret Data		Title	
Issued Date	2008/02/25	Deciphered Date	2008/04/29	Compal Electronics, Inc.	
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				LA-4102P Blade discrete	1.0
Date: Monday, May 12, 2008				Sheet	14 of 54

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

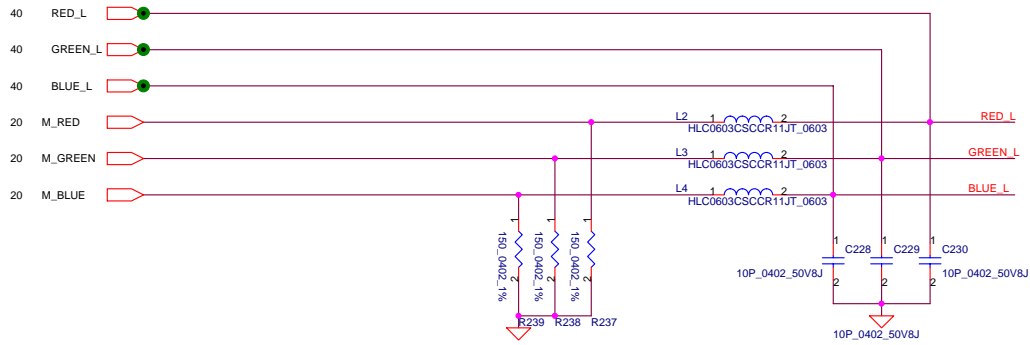


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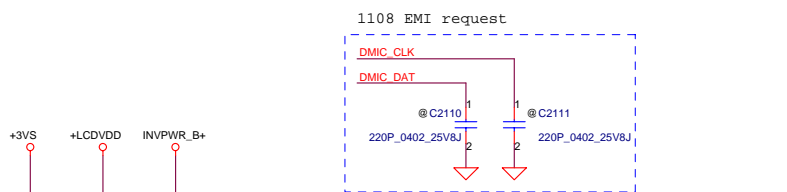
CRT Connector



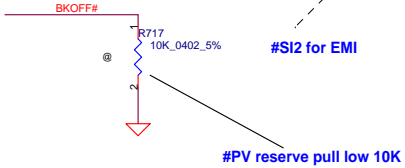
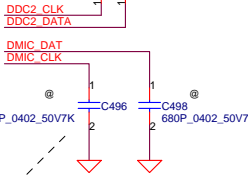
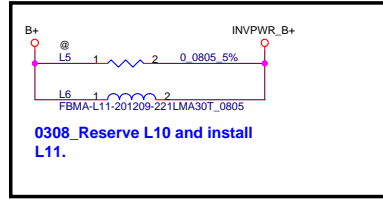
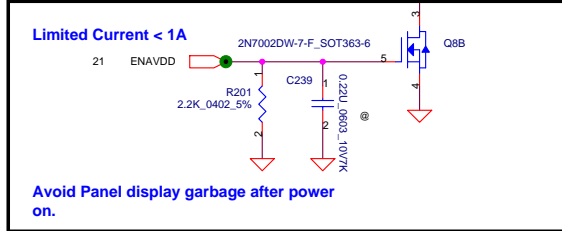
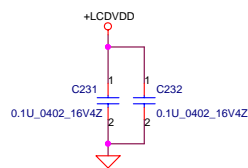
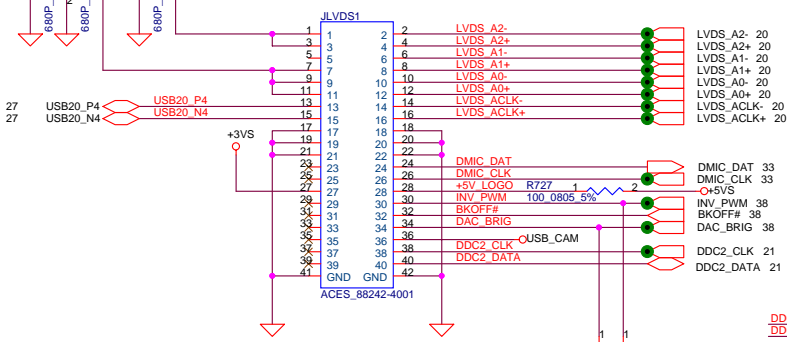
#SI Remove pull low resistor



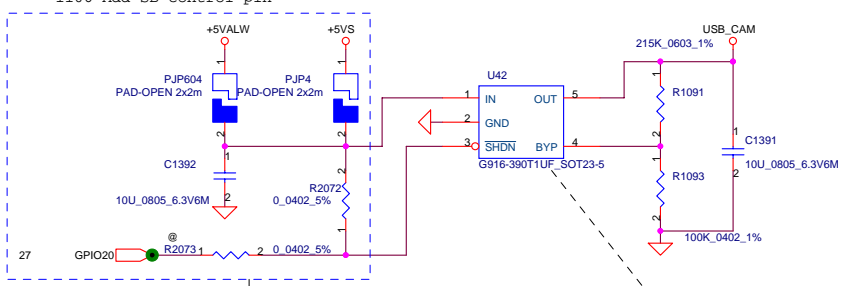
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LVDS CONN WITH Camera and Digi MIC



USB Camera Power



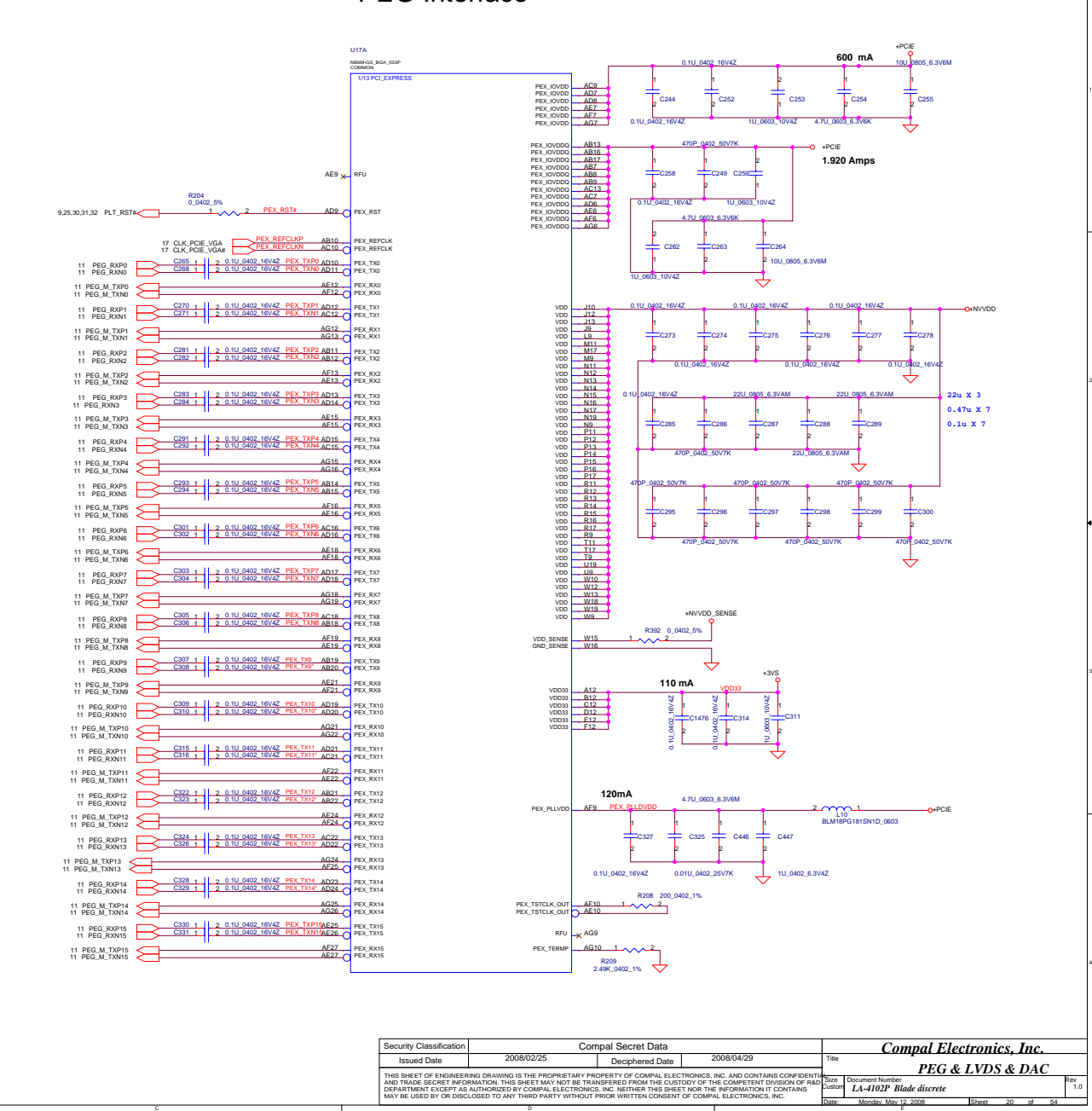
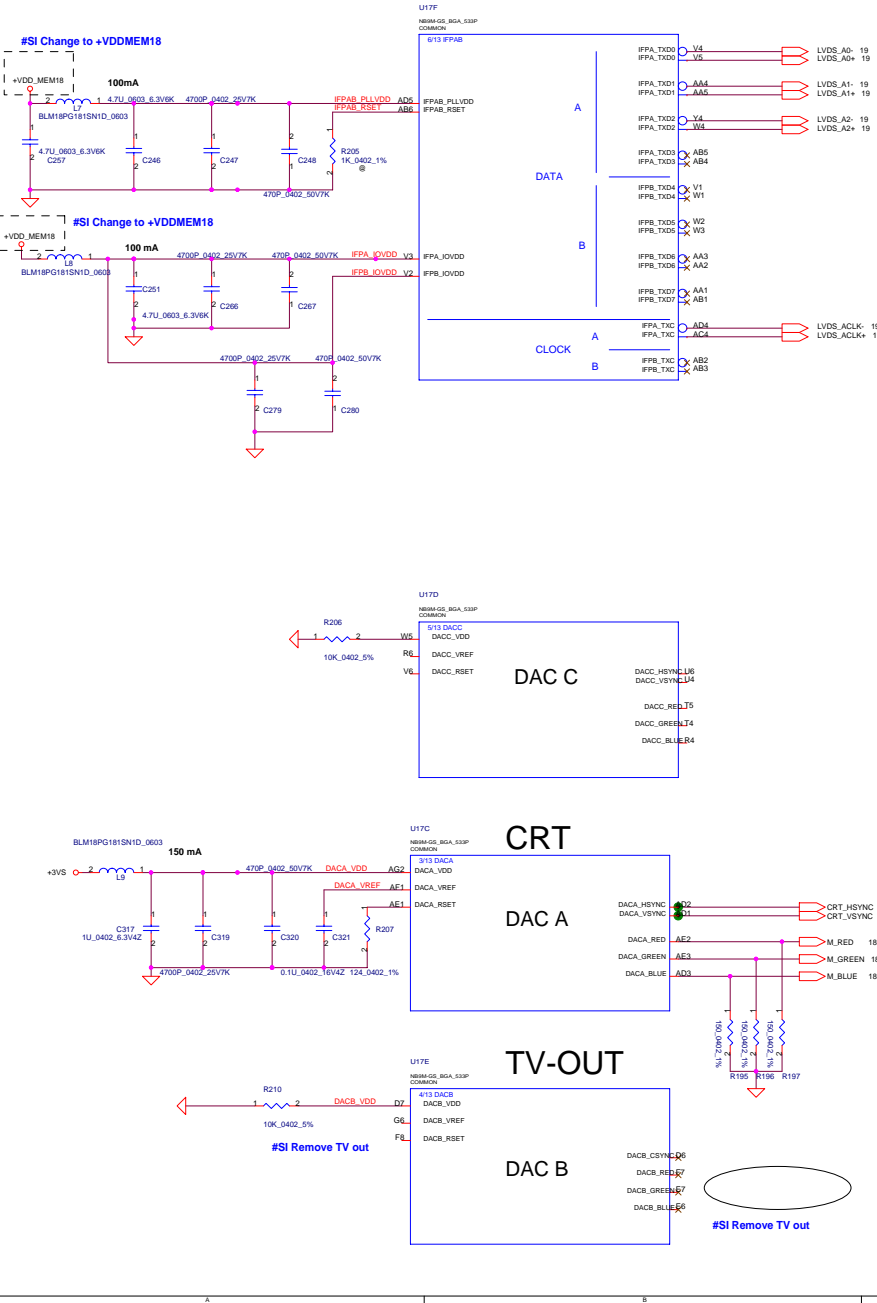
USB_VCCA is +3.9V
 USB_VCCA = 1.25X(1+R1091/R1093)

#SI Add GPIO20 control and reserve +5VS

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				LA-4102P Blade discrete	1.0
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LVDS & DAC Interface

PEG Interface

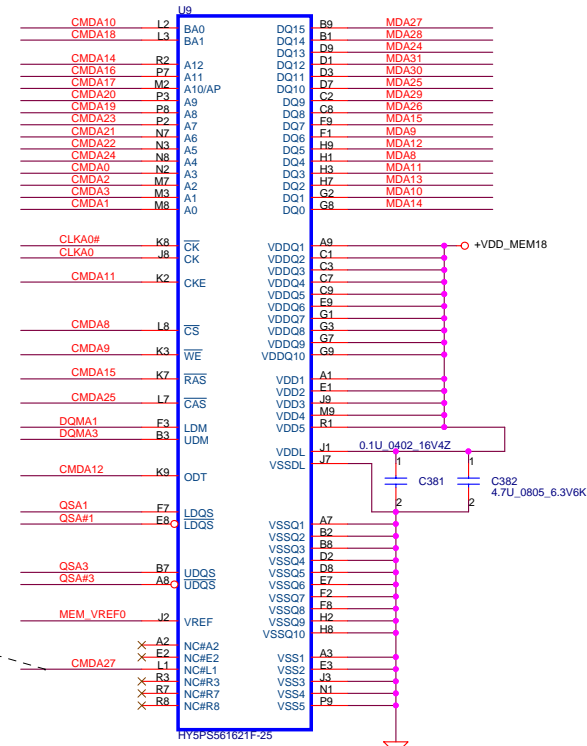
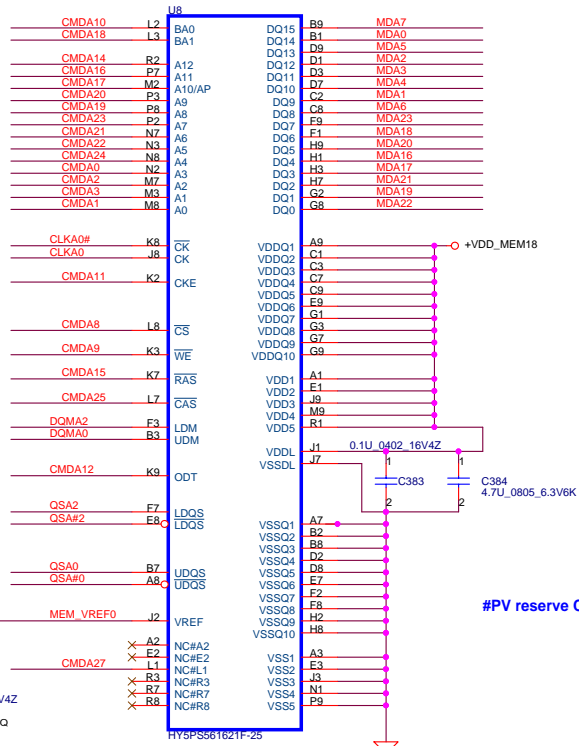
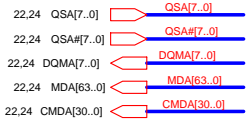


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Issued Date	2008/02/25	Deciphered Date	2008/04/29	PEG & LVDS & DAC	
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Size	L30	Document Number	LA-1102P	Rev	1.0
Custom			Blade discrete	Date	Monday, May 12, 2008
				Sheet	20 of 24

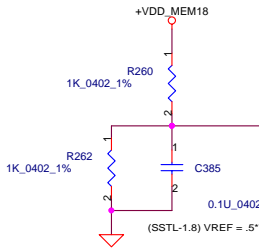
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

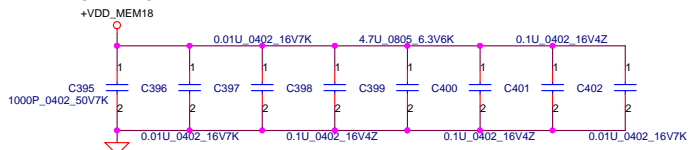
64Mx16 DDR2 400MHz*4==>512MB



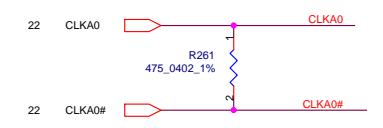
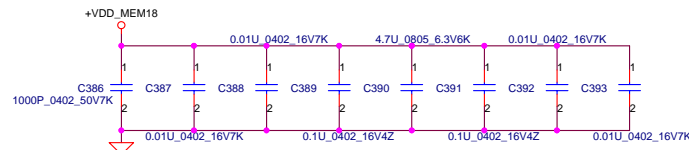
Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



DDR2 BGA MEMORY



DDR BGA MEMORY

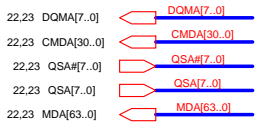


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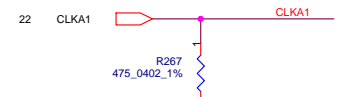
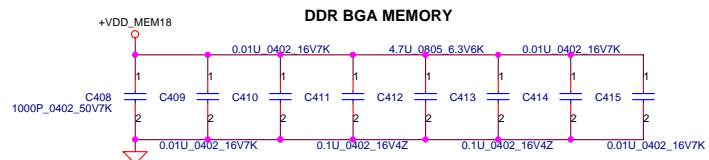
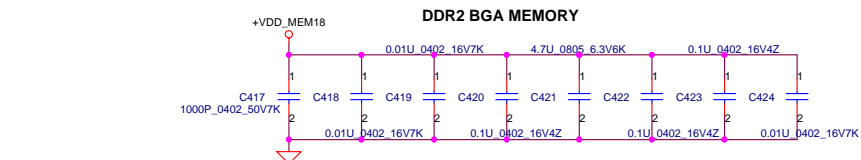
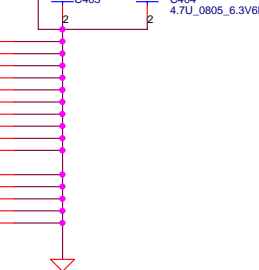
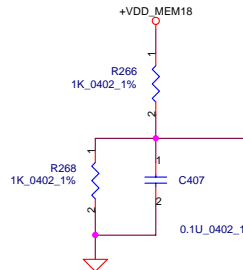
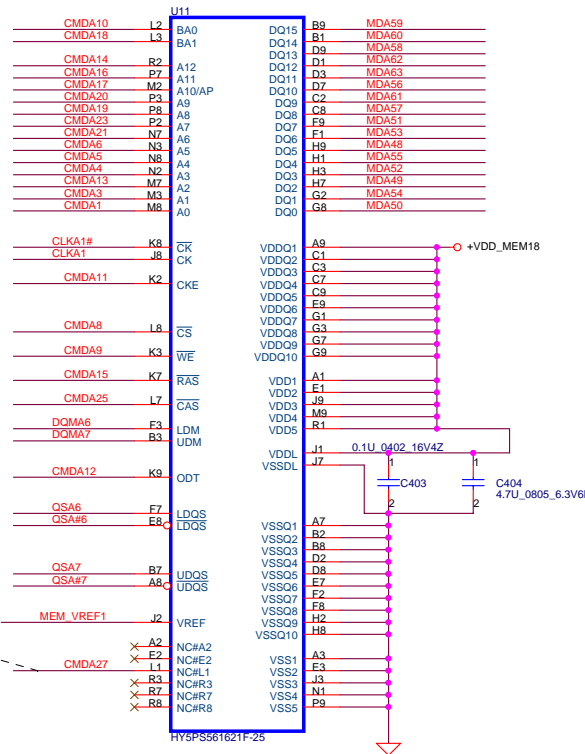
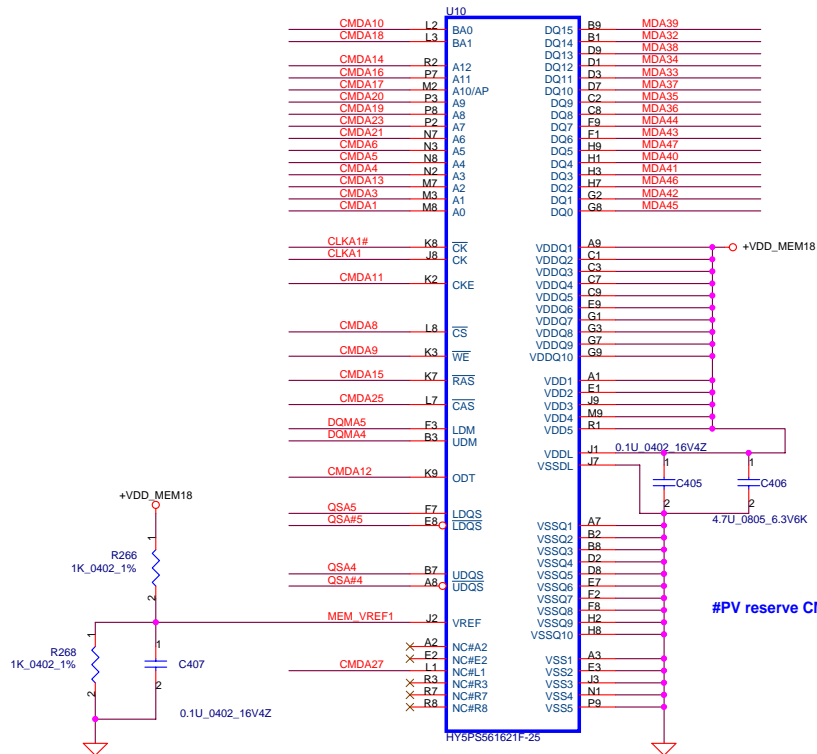
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *4==>256MB

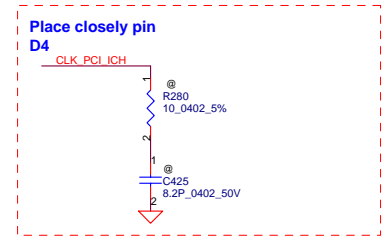
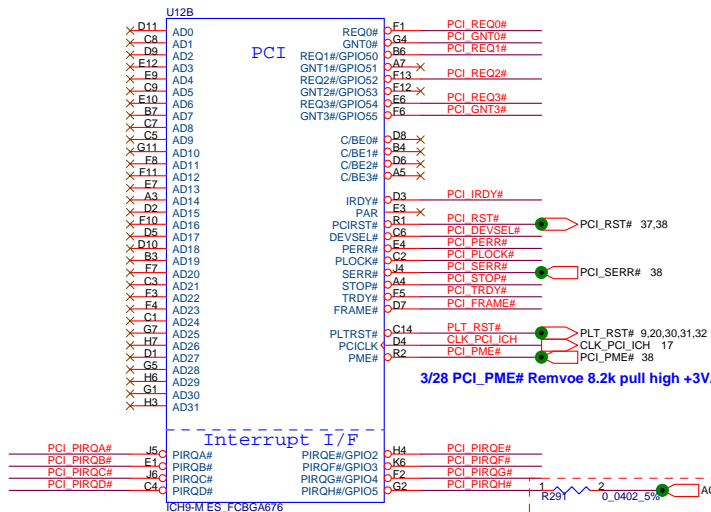
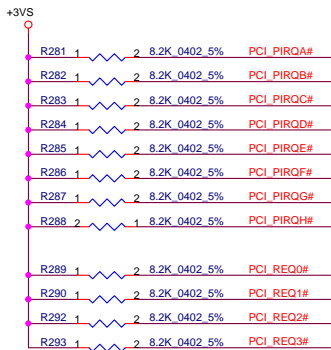
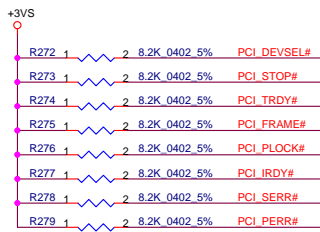
64Mx16 DDR2 400MHz*4==>512MB



DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



Security Classification	Compal Secret Data		Title	
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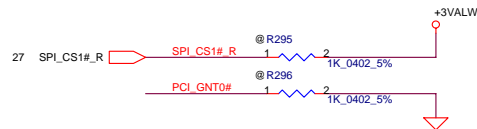
A16 swap override Strap

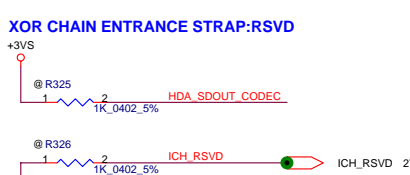
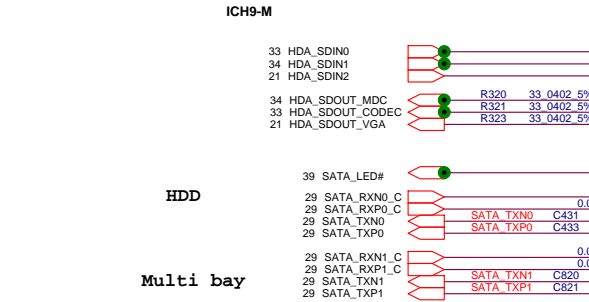
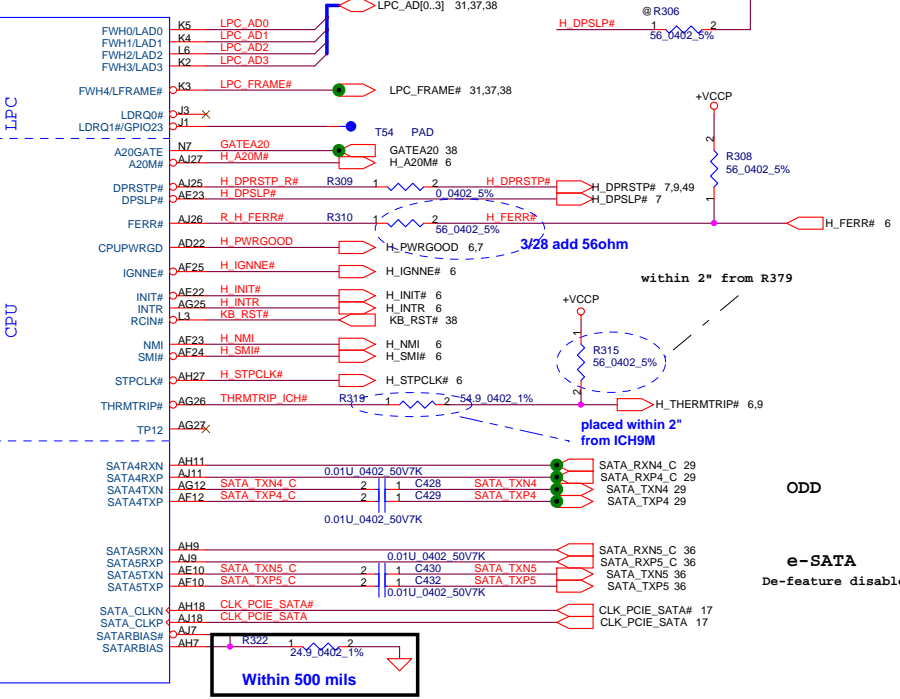
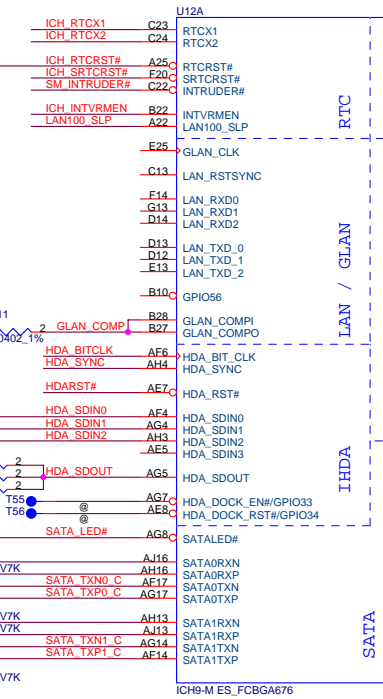
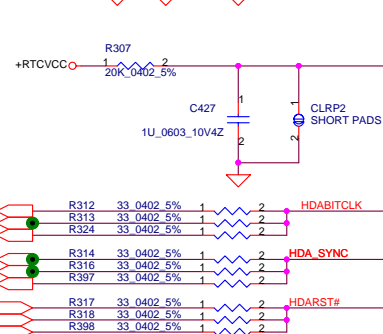
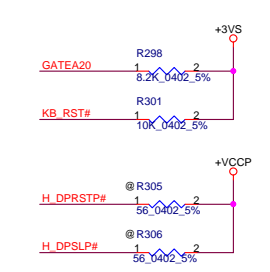
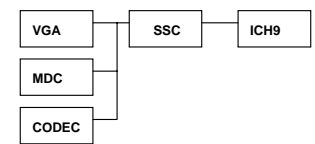
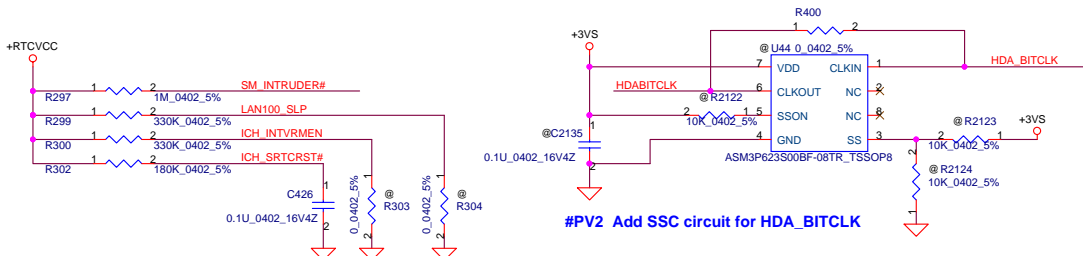
PCI_GNT3# Low= A16 swap override Enable
High= Default *



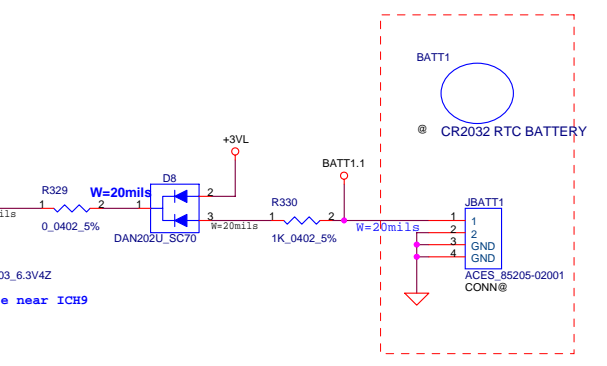
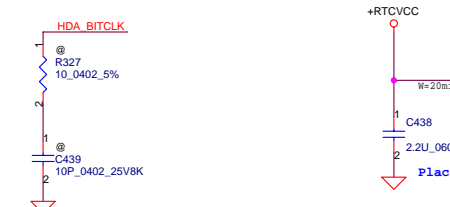
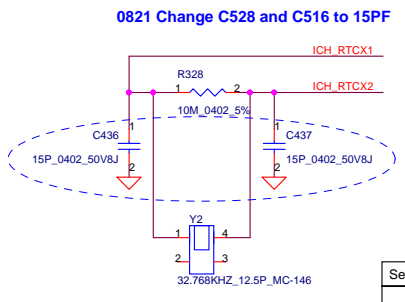
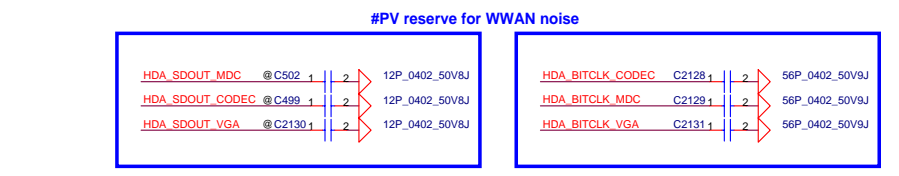
Boot BIOS Strap

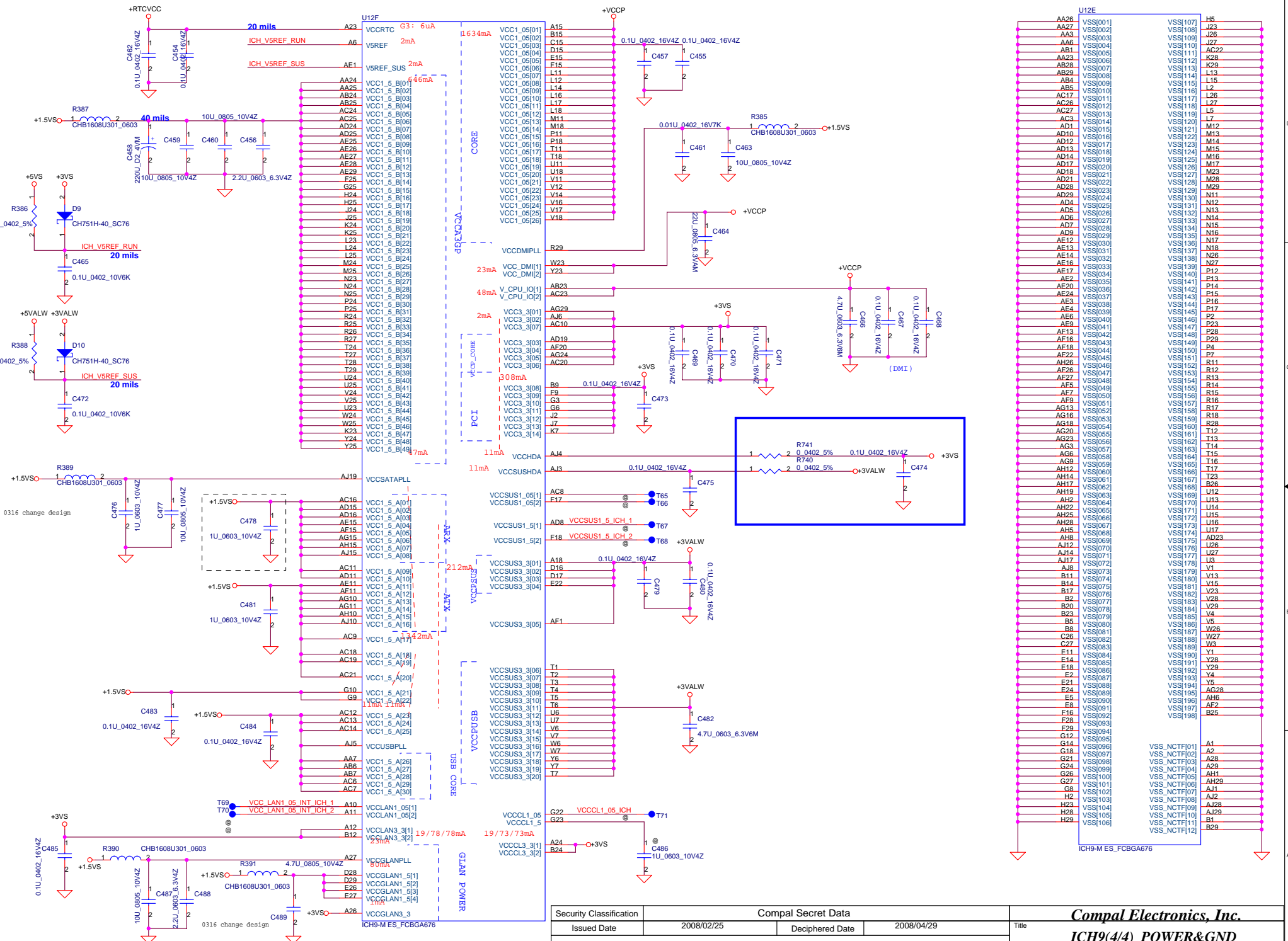
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





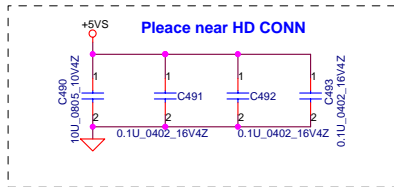
ICH_RSVD	HDA_SDOOUT_CODEDC
0	0
0	1
1	0
1	1



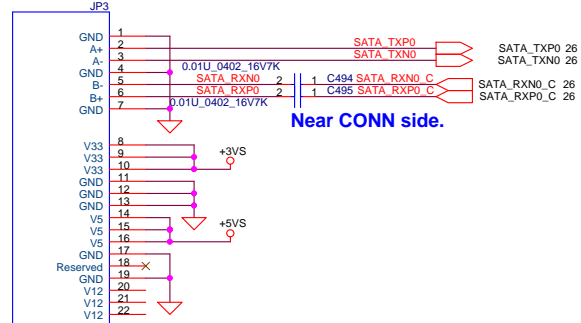


U12E	Pin	Signal	Pin	Signal
AA26	VSS[001]	VSS[107]	H5	
AA27	VSS[002]	VSS[108]	J23	
AA3	VSS[003]	VSS[109]	J26	
AA6	VSS[004]	VSS[110]	J27	
AA7	VSS[005]	VSS[111]	AC22	
AA8	VSS[006]	VSS[112]	K28	
AA23	VSS[007]	VSS[113]	K29	
AB28	VSS[008]	VSS[114]	L13	
AB29	VSS[009]	VSS[115]	L15	
AB4	VSS[010]	VSS[116]	L2	
AC17	VSS[011]	VSS[117]	L26	
AC26	VSS[012]	VSS[118]	L27	
AC27	VSS[013]	VSS[119]	L7	
AC3	VSS[014]	VSS[120]	M12	
AD1	VSS[015]	VSS[121]	M17	
AD10	VSS[016]	VSS[122]	M13	
AD12	VSS[017]	VSS[123]	M14	
AD13	VSS[018]	VSS[124]	M15	
AD14	VSS[019]	VSS[125]	M16	
AD17	VSS[020]	VSS[126]	M17	
AD18	VSS[021]	VSS[127]	M23	
AD21	VSS[022]	VSS[128]	M28	
AD28	VSS[023]	VSS[129]	M29	
AD29	VSS[024]	VSS[130]	N11	
AD4	VSS[025]	VSS[131]	N12	
AD5	VSS[026]	VSS[132]	N13	
AD6	VSS[027]	VSS[133]	N14	
AD7	VSS[028]	VSS[134]	N15	
AD9	VSS[029]	VSS[135]	N16	
AE12	VSS[030]	VSS[136]	N17	
AE13	VSS[031]	VSS[137]	N18	
AE14	VSS[032]	VSS[138]	N26	
AE16	VSS[033]	VSS[139]	N27	
AE17	VSS[034]	VSS[140]	P12	
AE2	VSS[035]	VSS[141]	P13	
AE24	VSS[036]	VSS[142]	P14	
AE3	VSS[037]	VSS[143]	P15	
AE4	VSS[038]	VSS[144]	P16	
AE6	VSS[039]	VSS[145]	P17	
AE9	VSS[040]	VSS[146]	P2	
AE11	VSS[041]	VSS[147]	P23	
AE16	VSS[042]	VSS[148]	P28	
AE18	VSS[043]	VSS[149]	P29	
AE20	VSS[044]	VSS[150]	P49	
AE22	VSS[045]	VSS[151]	P7	
AH26	VSS[046]	VSS[152]	R11	
AH27	VSS[047]	VSS[153]	R12	
AF27	VSS[048]	VSS[154]	R13	
AF5	VSS[049]	VSS[155]	R14	
AF7	VSS[050]	VSS[156]	R15	
AF9	VSS[051]	VSS[157]	R16	
AG13	VSS[052]	VSS[158]	R17	
AG16	VSS[053]	VSS[159]	R18	
AG18	VSS[054]	VSS[160]	R28	
AG20	VSS[055]	VSS[161]	T12	
AG23	VSS[056]	VSS[162]	T13	
AG3	VSS[057]	VSS[163]	T14	
AG6	VSS[058]	VSS[164]	T15	
AH12	VSS[059]	VSS[165]	T16	
AH14	VSS[060]	VSS[166]	T23	
AH17	VSS[061]	VSS[167]	T26	
AH19	VSS[062]	VSS[168]	T27	
AH22	VSS[063]	VSS[169]	T31	
AH25	VSS[064]	VSS[170]	U13	
AH28	VSS[065]	VSS[171]	U14	
AH5	VSS[066]	VSS[172]	U15	
AH8	VSS[067]	VSS[173]	U16	
AH9	VSS[068]	VSS[174]	U17	
AJ12	VSS[069]	VSS[175]	AD23	
AJ14	VSS[070]	VSS[176]	AD26	
AJ17	VSS[071]	VSS[177]	AD27	
AJ18	VSS[072]	VSS[178]	AD28	
AJ19	VSS[073]	VSS[179]	AD29	
B11	VSS[074]	VSS[180]	AD30	
B14	VSS[075]	VSS[181]	V1	
B17	VSS[076]	VSS[182]	V13	
B2	VSS[077]	VSS[183]	V15	
B20	VSS[078]	VSS[184]	V23	
B23	VSS[079]	VSS[185]	V28	
B5	VSS[080]	VSS[186]	V29	
B8	VSS[081]	VSS[187]	V4	
C26	VSS[082]	VSS[188]	V5	
C27	VSS[083]	VSS[189]	W26	
E11	VSS[084]	VSS[190]	W27	
E18	VSS[085]	VSS[191]	W3	
E2	VSS[086]	VSS[192]	Y1	
E21	VSS[087]	VSS[193]	Y2	
E24	VSS[088]	VSS[194]	Y4	
E5	VSS[089]	VSS[195]	Y5	
F28	VSS[090]	VSS[196]	AG28	
F29	VSS[091]	VSS[197]	AH6	
G12	VSS[092]	VSS[198]	AF2	
G14	VSS[093]	VSS[199]	B25	
G17	VSS[094]	VSS_NCTF[01]	A1	
G21	VSS[097]	VSS_NCTF[02]	A2	
G24	VSS[098]	VSS_NCTF[03]	A28	
G26	VSS[099]	VSS_NCTF[04]	A29	
G27	VSS[100]	VSS_NCTF[05]	AH1	
G8	VSS[101]	VSS_NCTF[06]	AH29	
H2	VSS[102]	VSS_NCTF[07]	AJ1	
H23	VSS[103]	VSS_NCTF[08]	AJ2	
H28	VSS[104]	VSS_NCTF[09]	AJ28	
H29	VSS[105]	VSS_NCTF[10]	AJ29	
	VSS[106]	VSS_NCTF[11]	B1	
		VSS_NCTF[12]	B29	

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		LA-4102P Blade discrete	Sheet	28	of 54

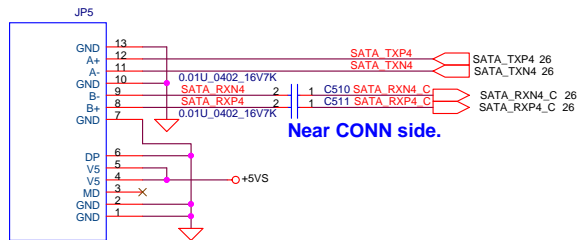


HDD Connector



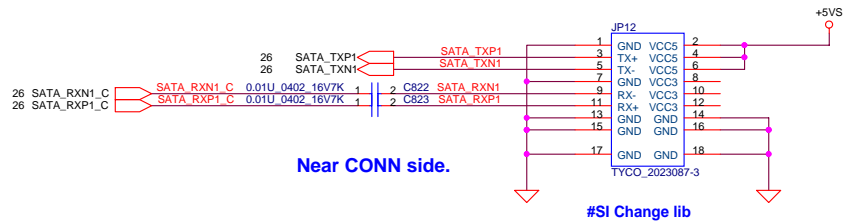
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CONN@

CD-ROM Connector



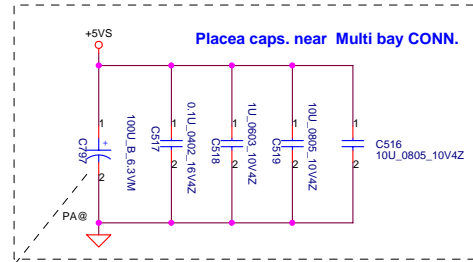
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CONN@

Multi Bay Connector



Near CONN side.

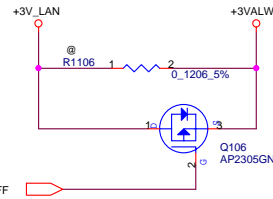
#SI Change lib



#MV Add cap

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1025 add to meet HP request

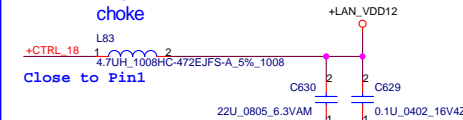


#MV clock REQ pull high



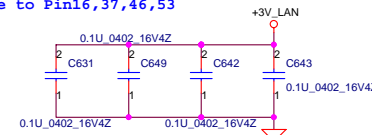
Close to Pin2 & pin59

4.7uH choke

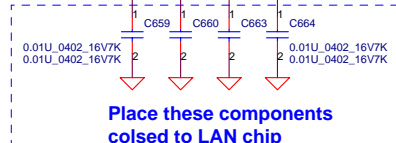
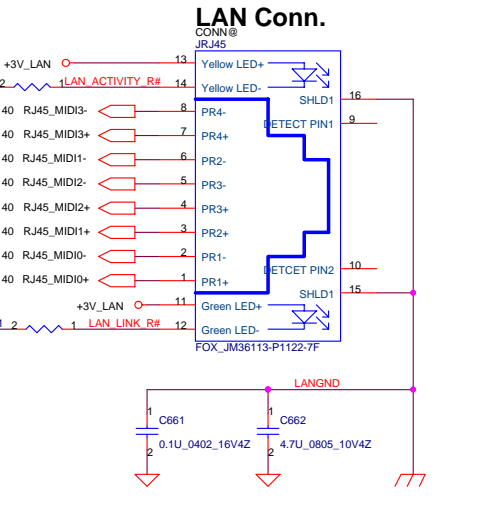
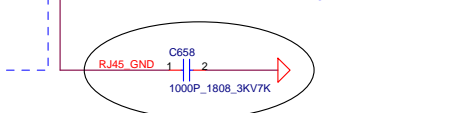
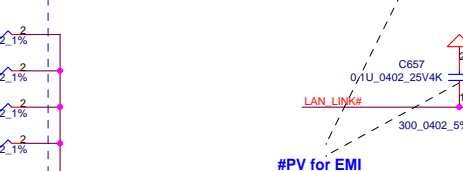
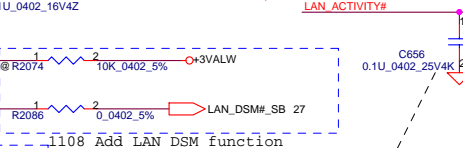
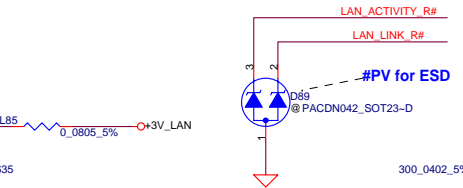
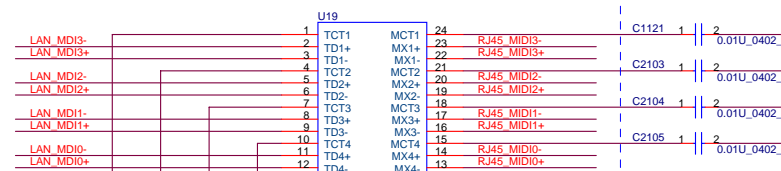
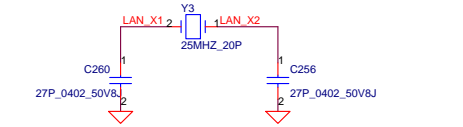
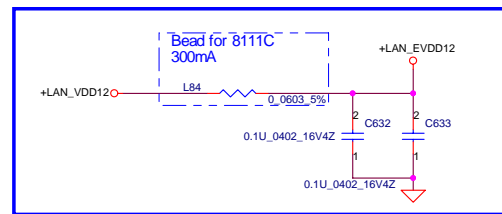
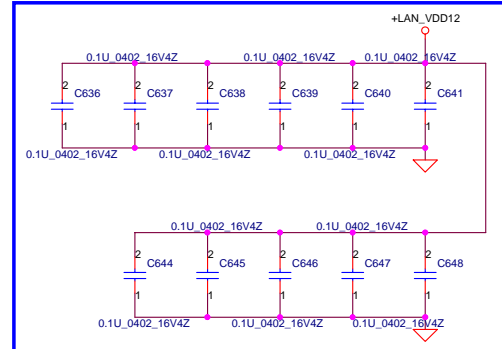
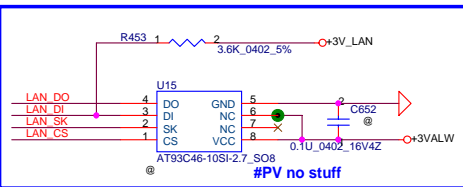
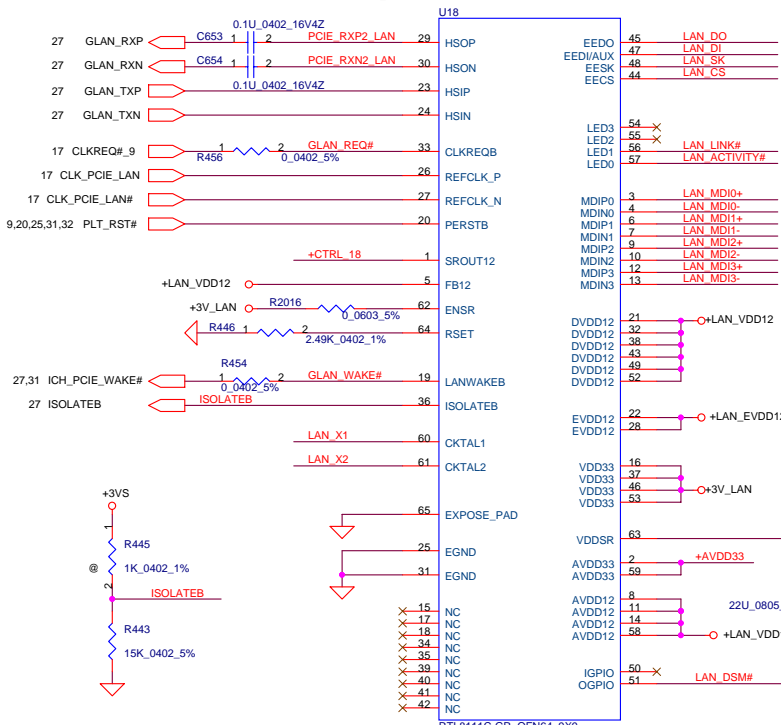


Close to Pin1

Close to Pin16,37,46,53



Place Close to Chip

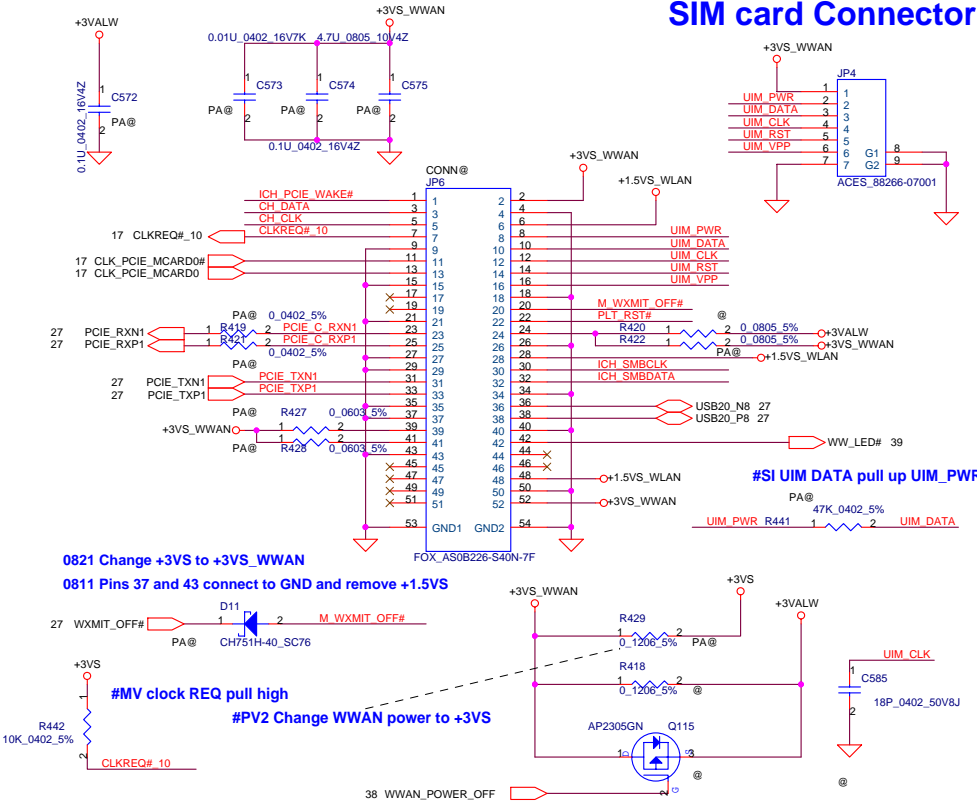


Place these components close to LAN chip

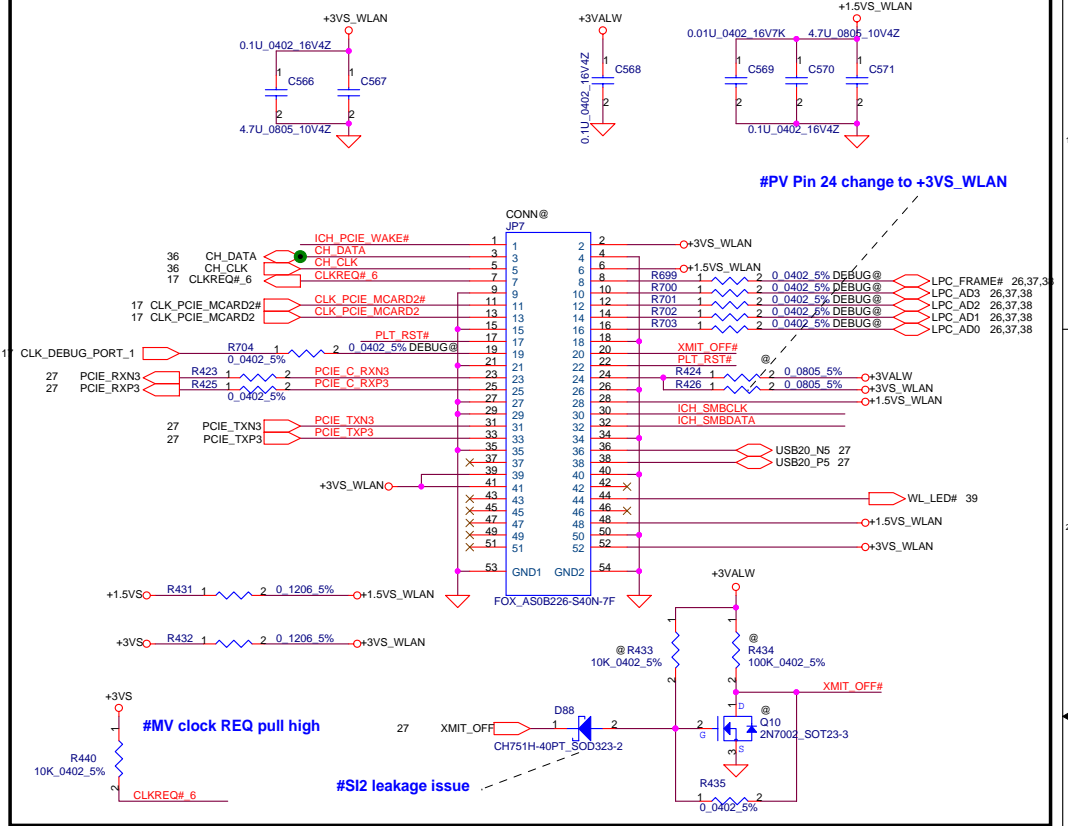
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Date:	Tuesday, April 29, 2008	Sheet	30	of	54

Mini Card 0--TV tuner/WWAN/Robson

SIM card Connector

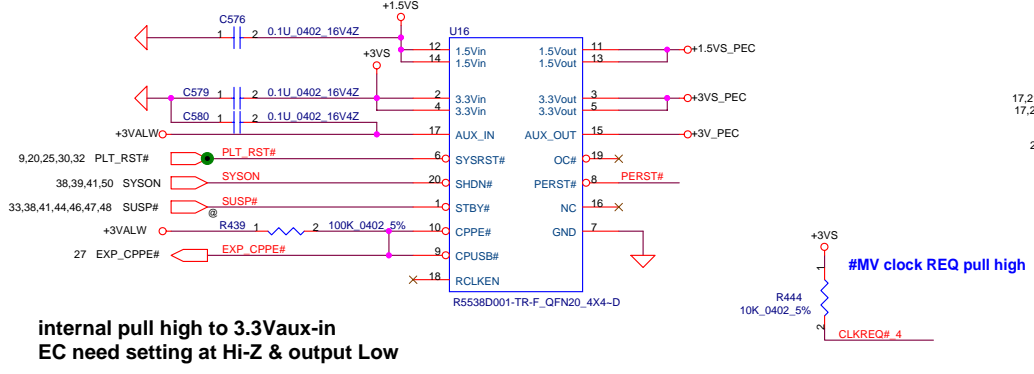


Mini Card 2---WLAN

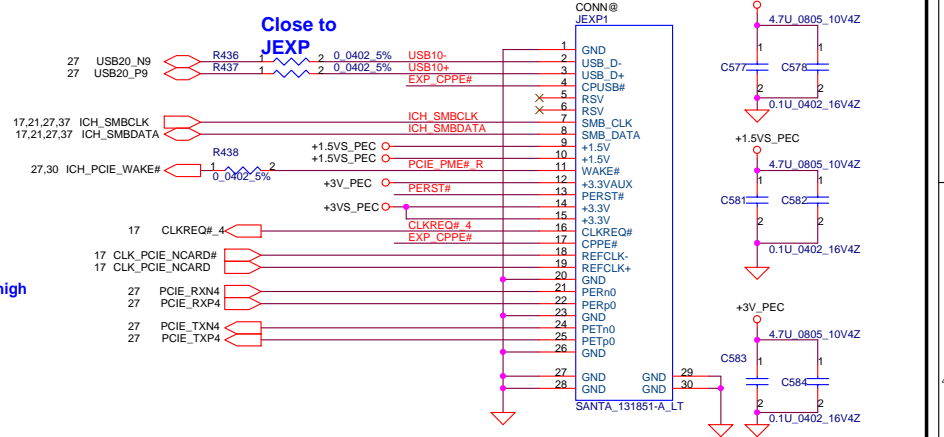


New Card

Express Card Power Switch



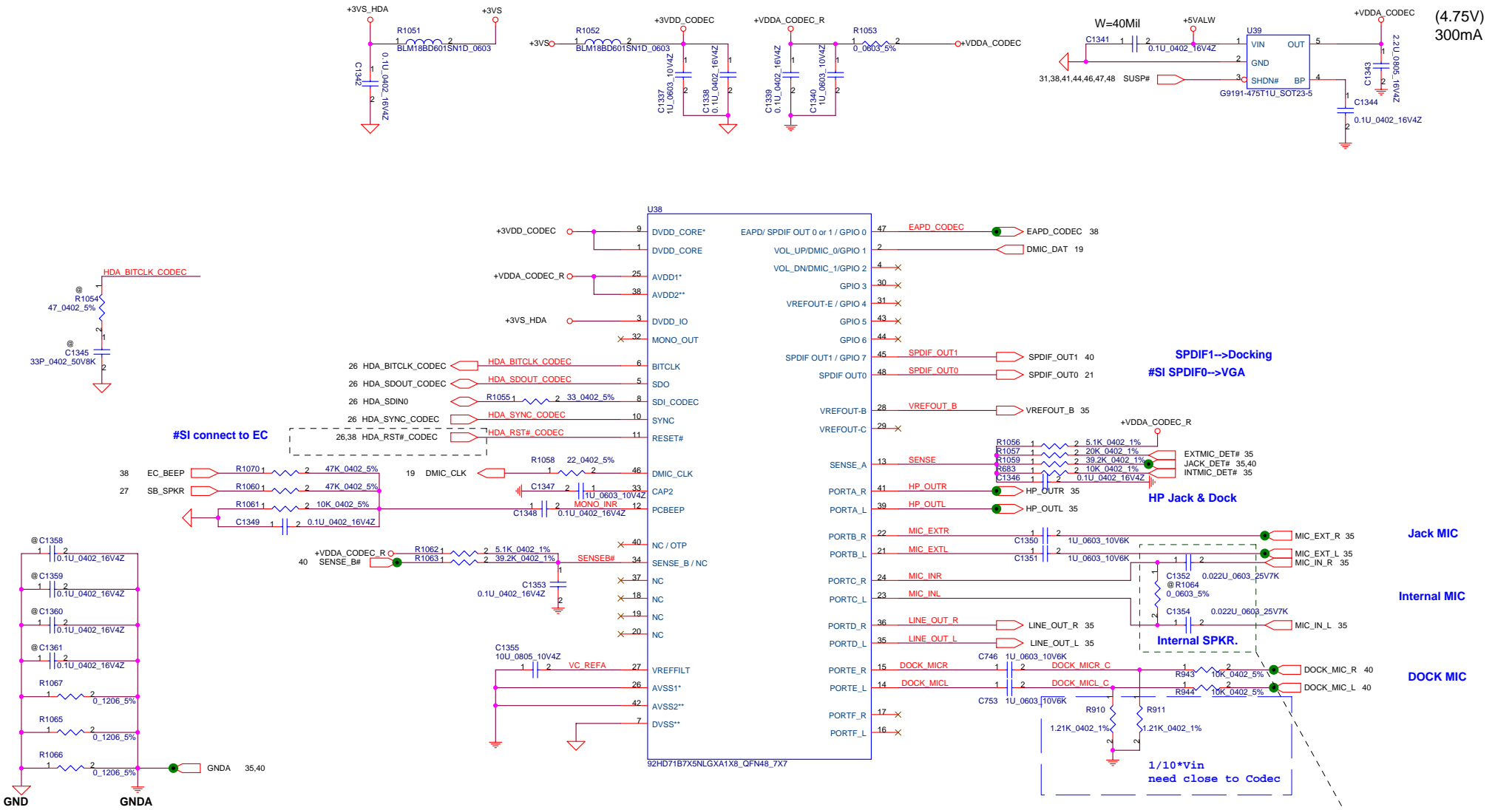
Near to Express Card slot.



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Rev	1.0	Document Number	LA-4102P Blade discrete		
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CODEC POWER

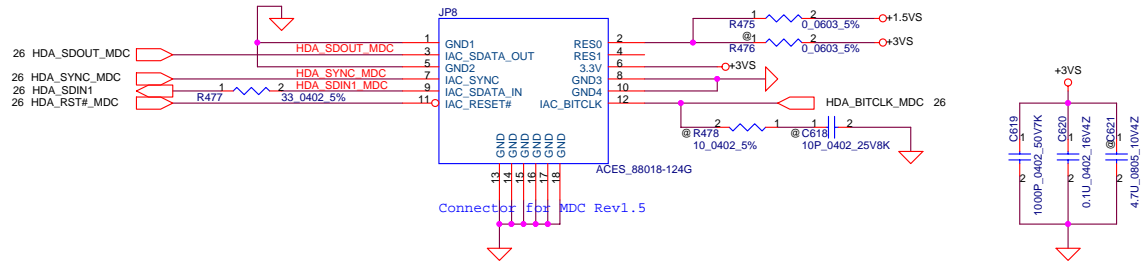
(4.75V)
300mA



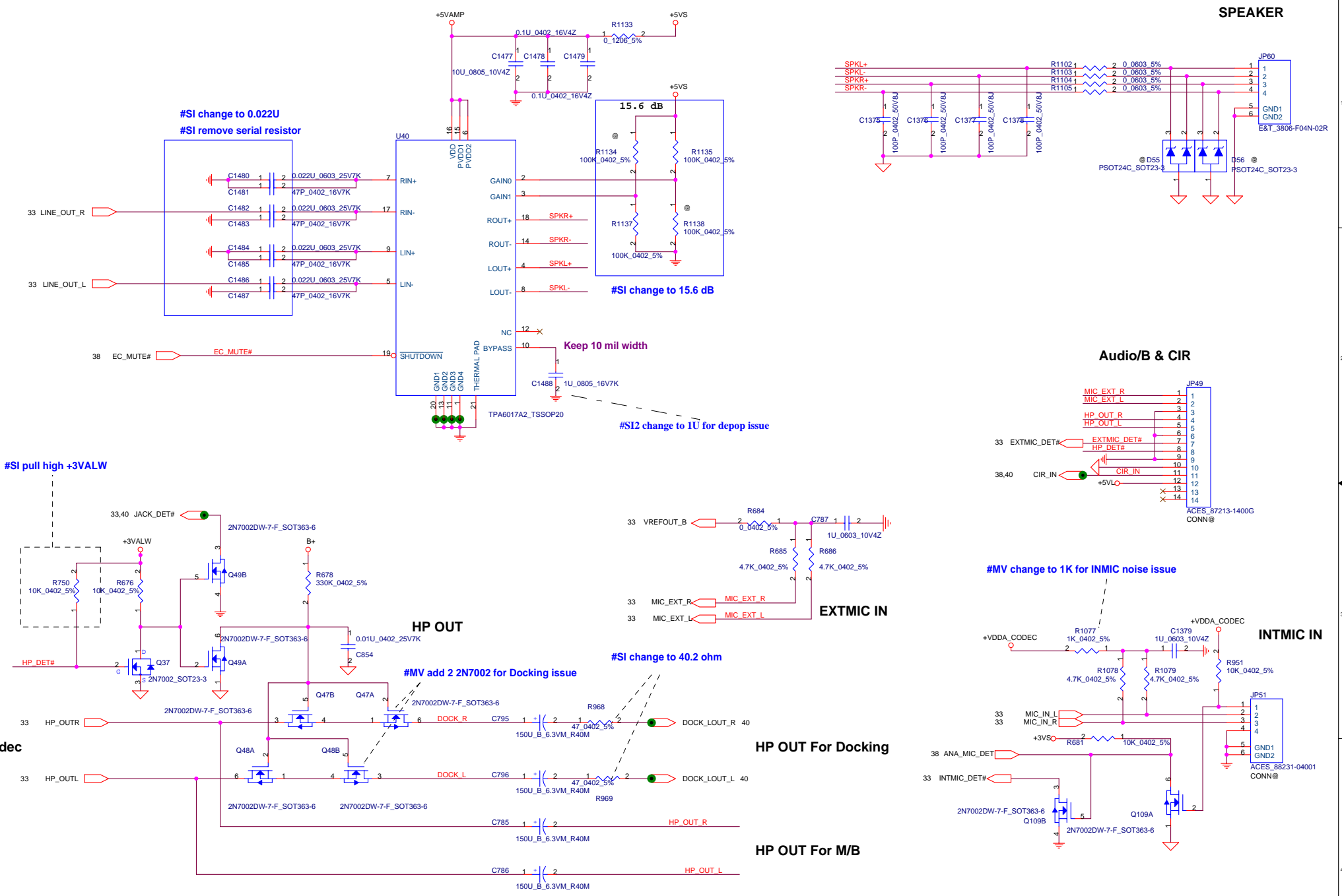
SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

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Date:	Tuesday, April 29, 2008	Sheet	33 of 54

MDC 1.5 Conn.

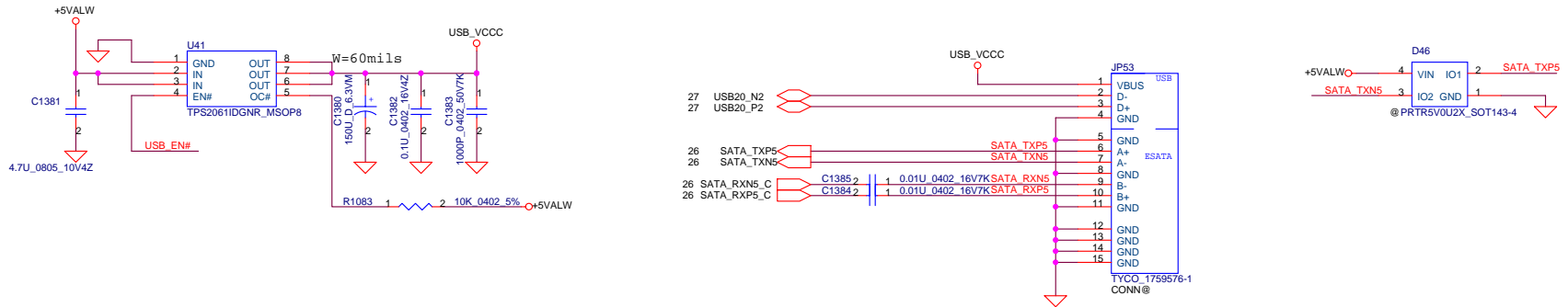


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Date:	Tuesday, April 29, 2008	Sheet	34	of	54

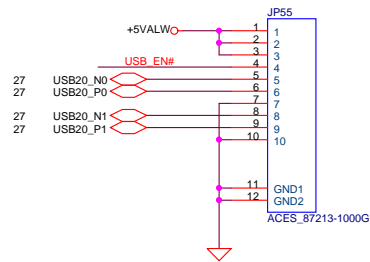


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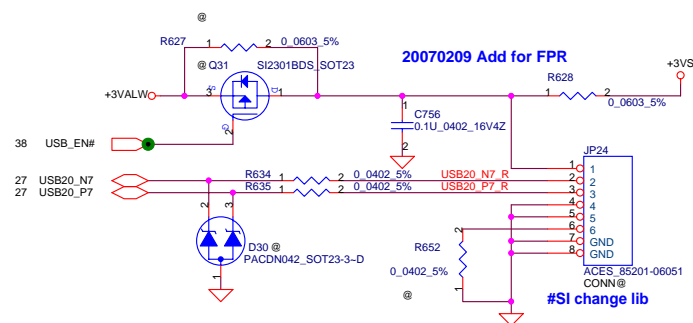
Left side ESATA/USB combination Connector



USB cable connector for Right side

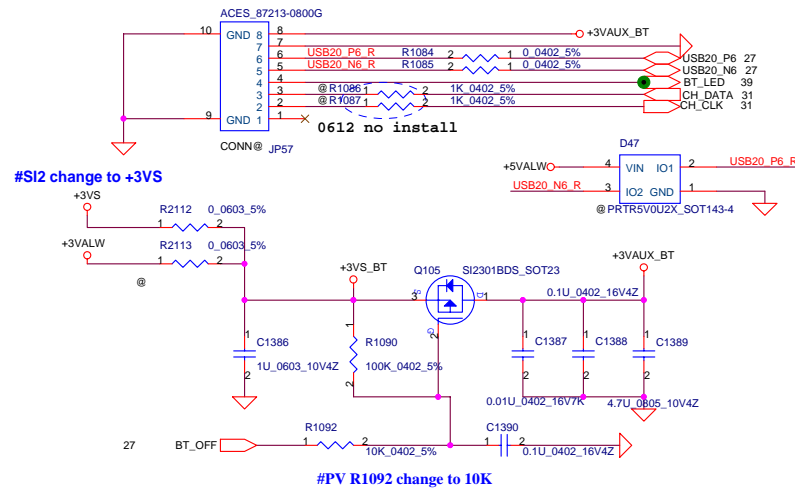


Finger printer

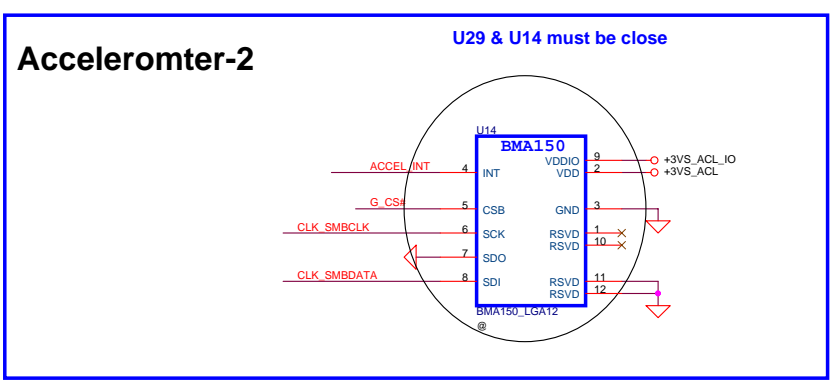
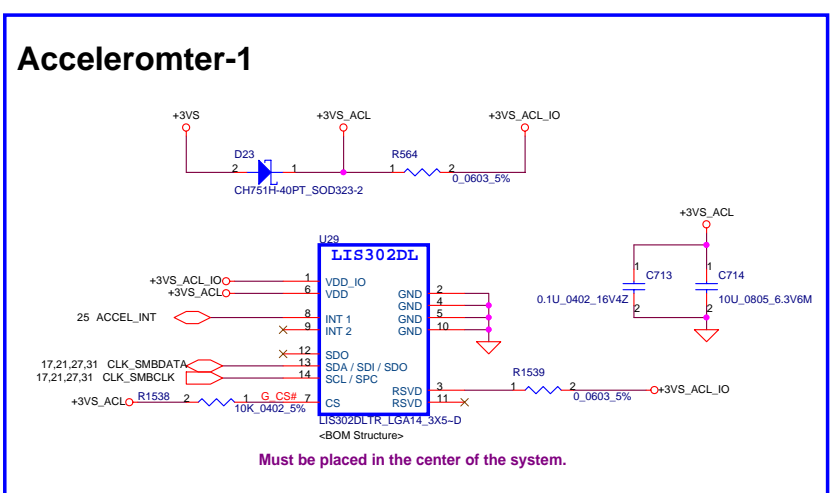
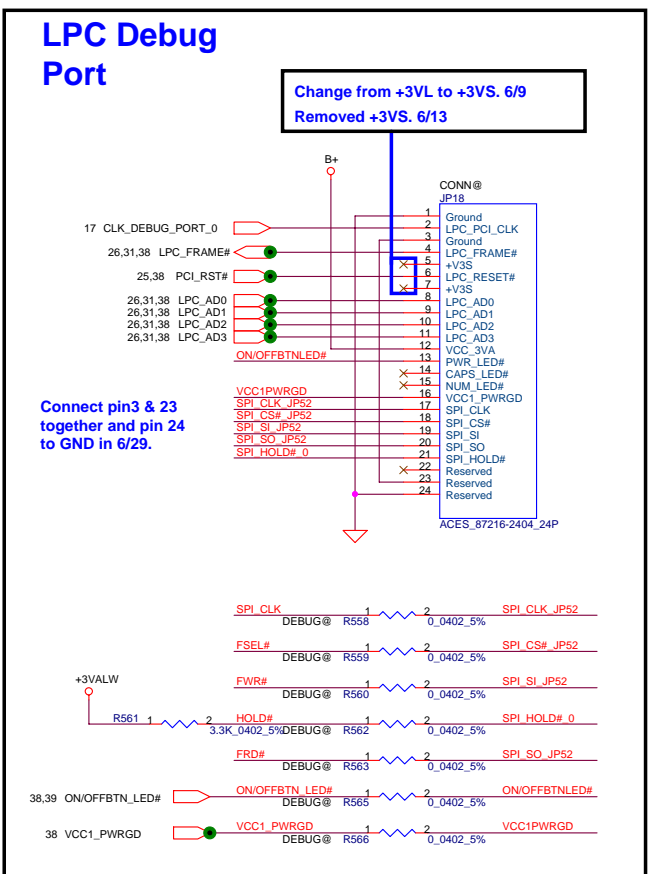
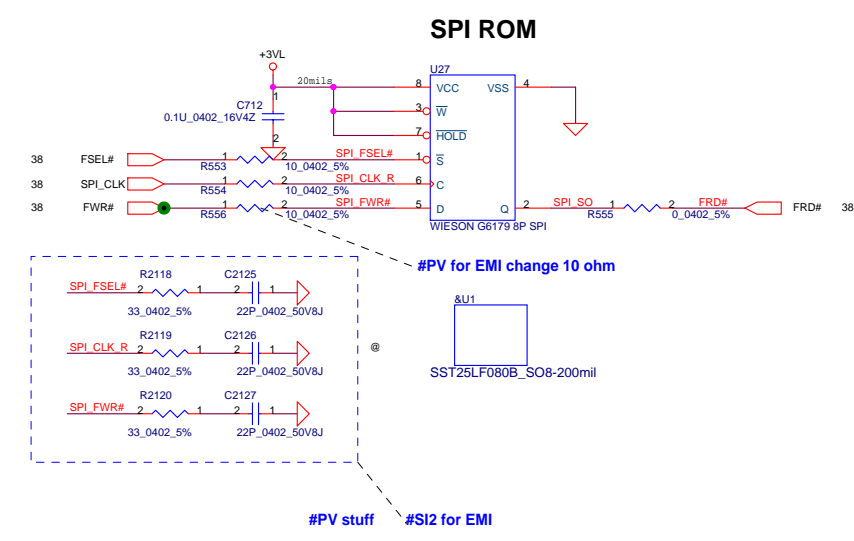
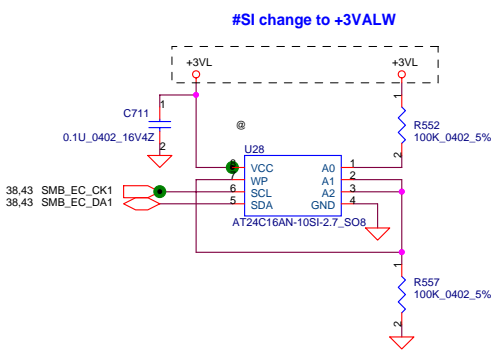


BT Connector

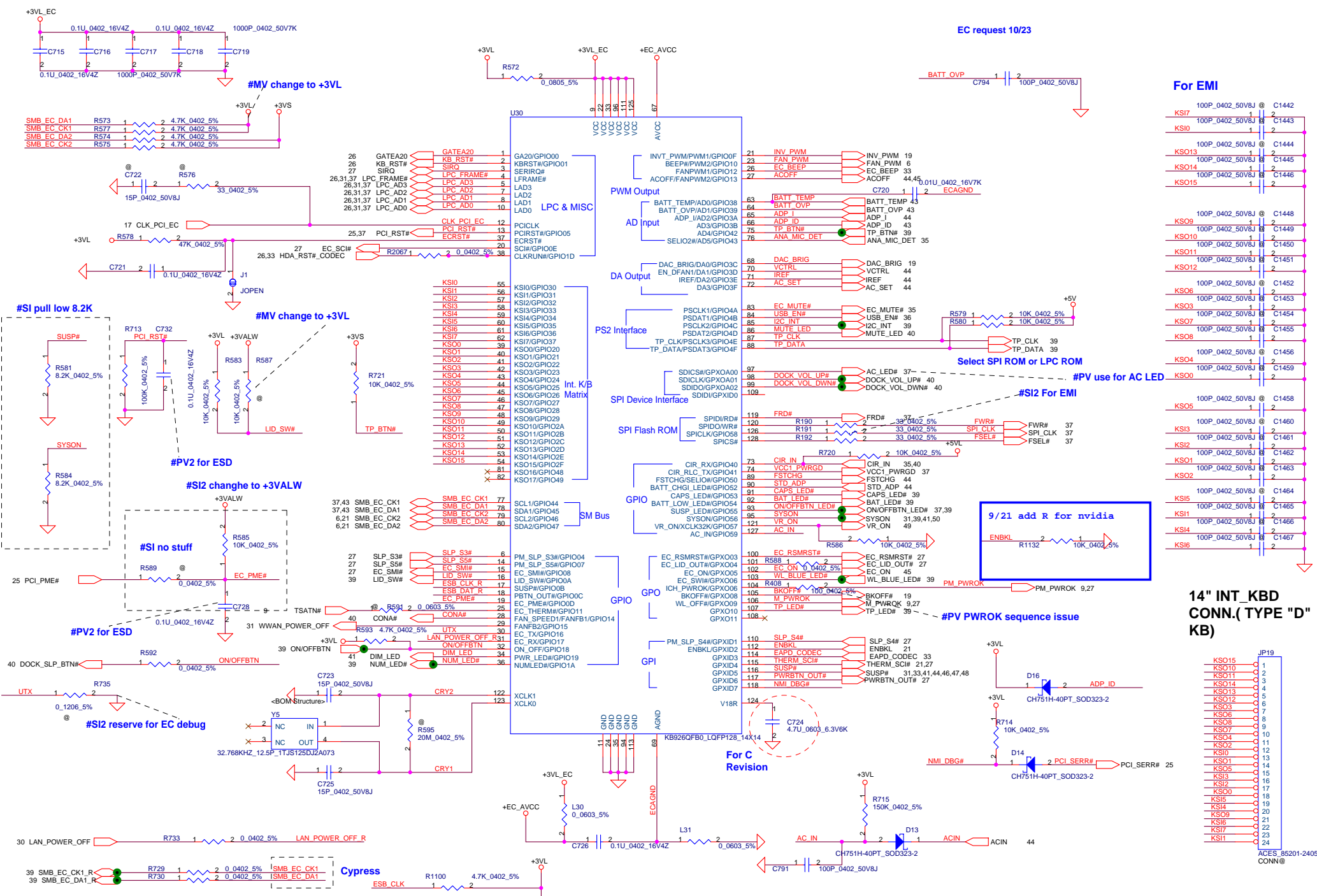
Need change to New version



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				Date:	Tuesday, April 29, 2008	
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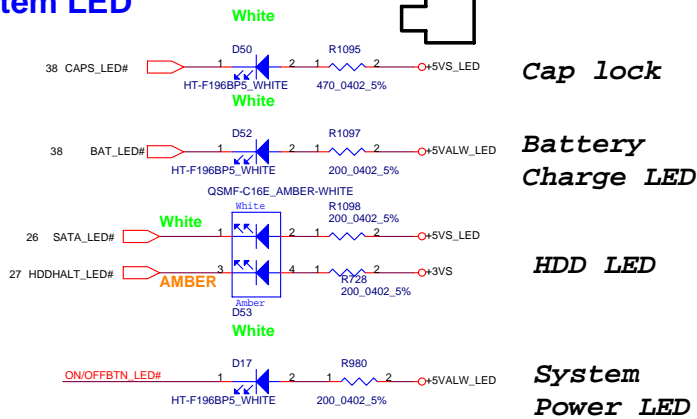


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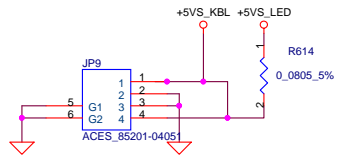


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Document Number	LA-4102P Blade discrete		Rev 1.0
Date	Tuesday, May 06, 2008	Sheet	38 of 54

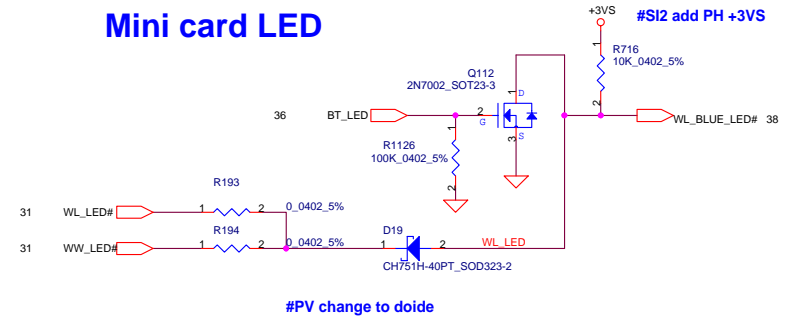
System LED



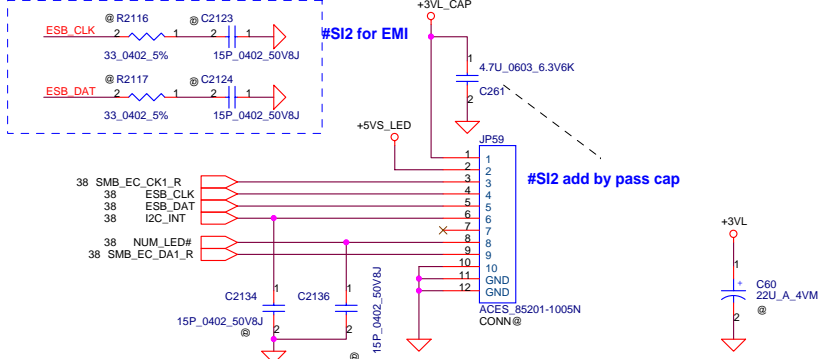
Keyboard backlight Conn



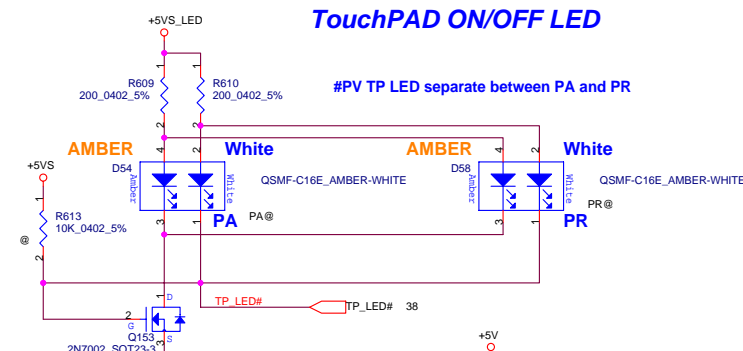
Mini card LED



Capacitor Sensor Conn



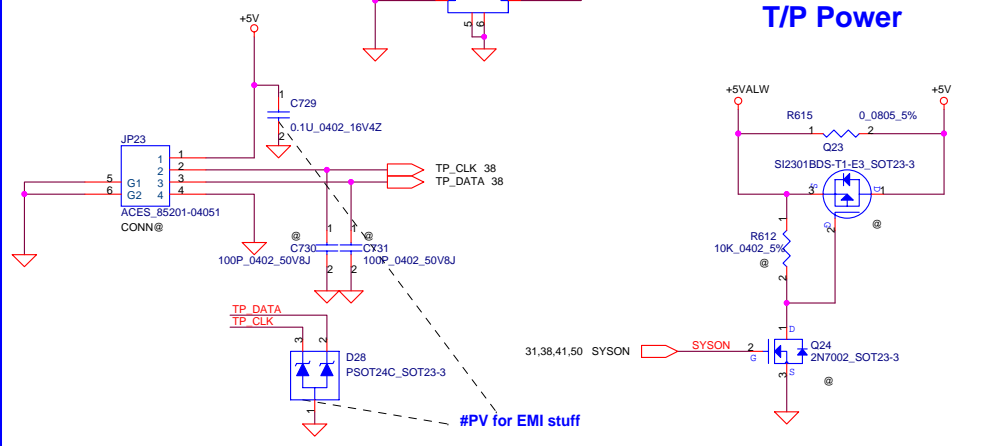
TouchPAD ON/OFF LED



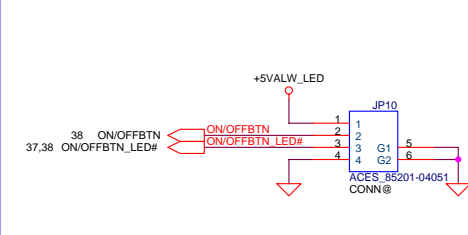
TP ON/OFF

TP Board

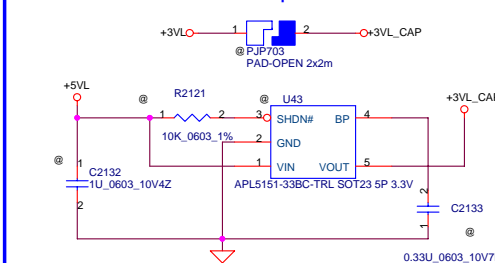
T/P Power



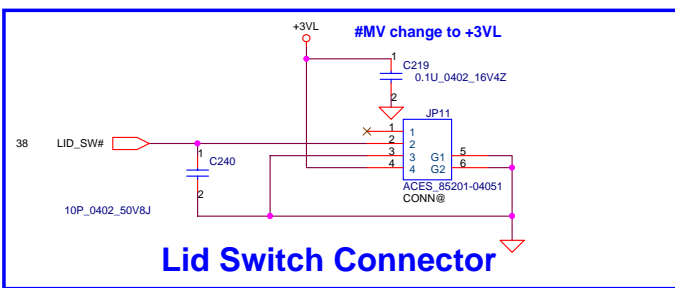
ON/OFF Button Connector



#PV reserve LDO for capacitor sensor board



Lid Switch Connector

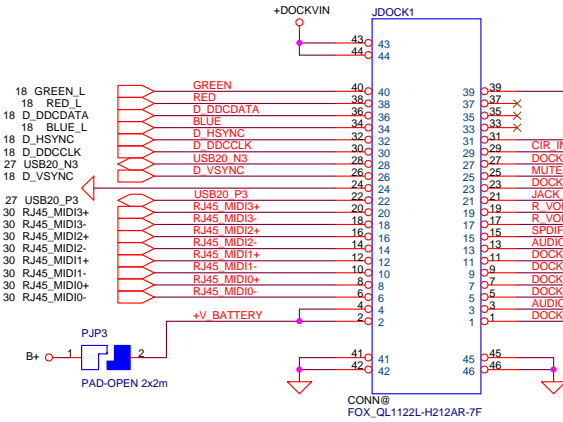
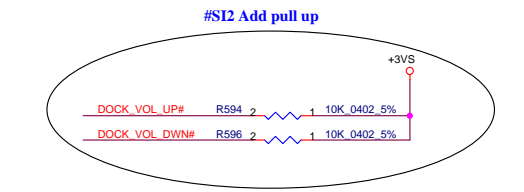
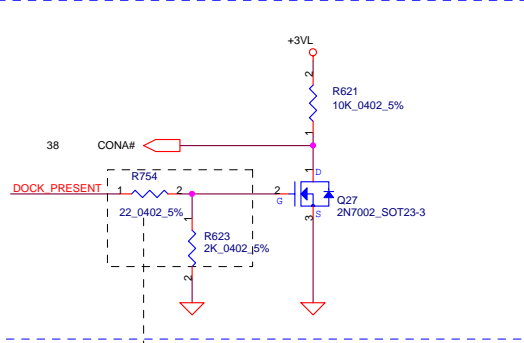
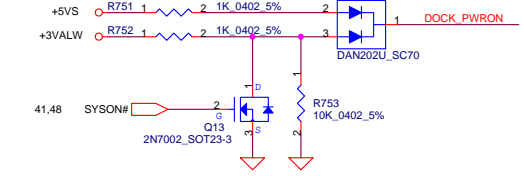


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				LA-4102P Blade discrete	1.0
Date: Monday, May 12, 2008				Sheet	39 of 54

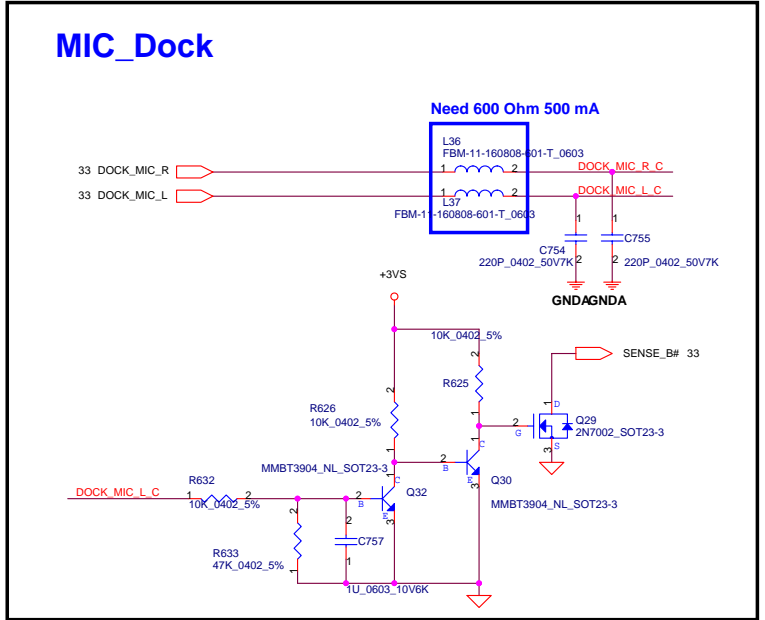
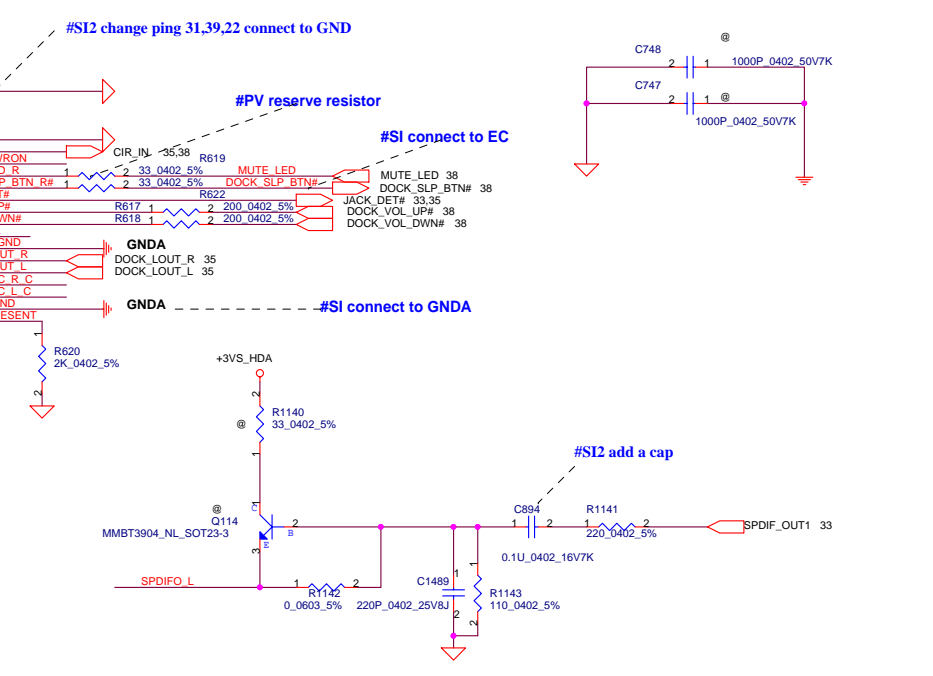
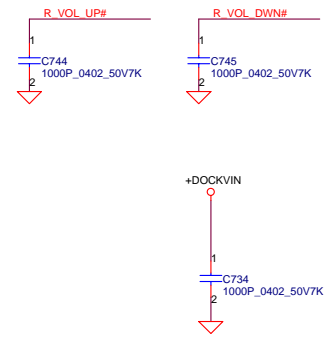
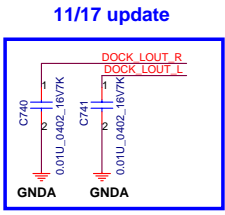
Atlas/ Saturn Dock

DOCK_PWR_ON Spec

- 0V = Notebook S4/S5, Dock off
- 2.5V = Notebook S3, Dock on
- 4V = Notebook S0, Dock on

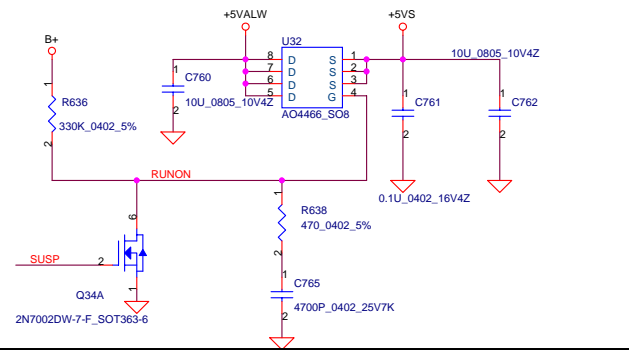


need change to reverse type connector

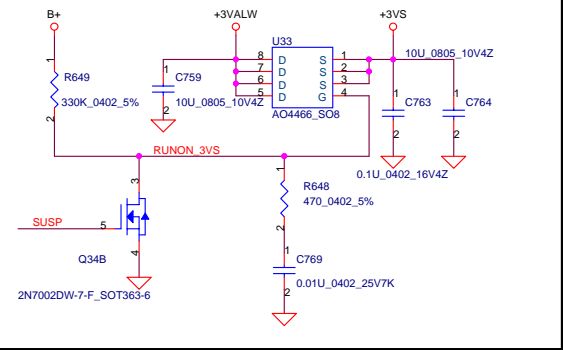


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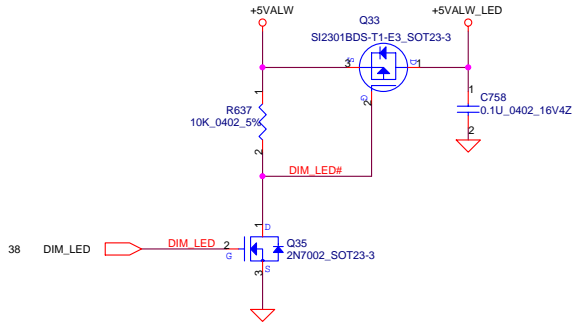
+5VALW to +5VS Transfer



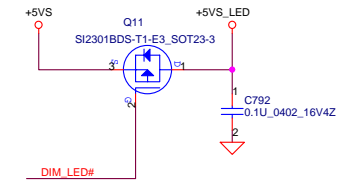
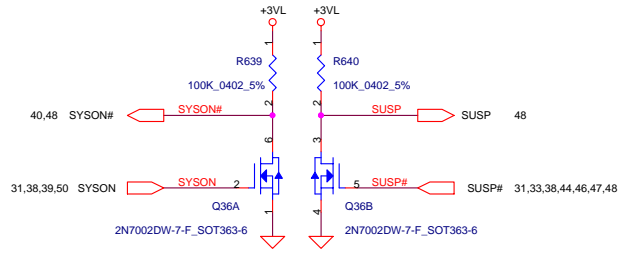
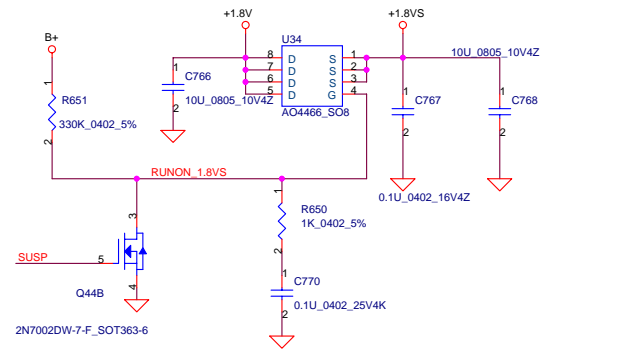
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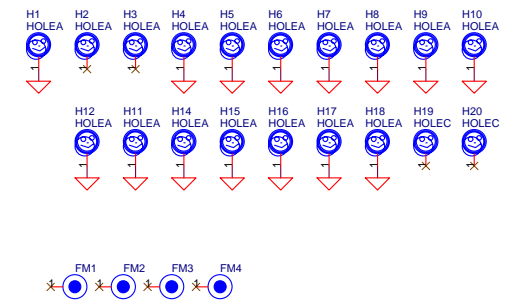
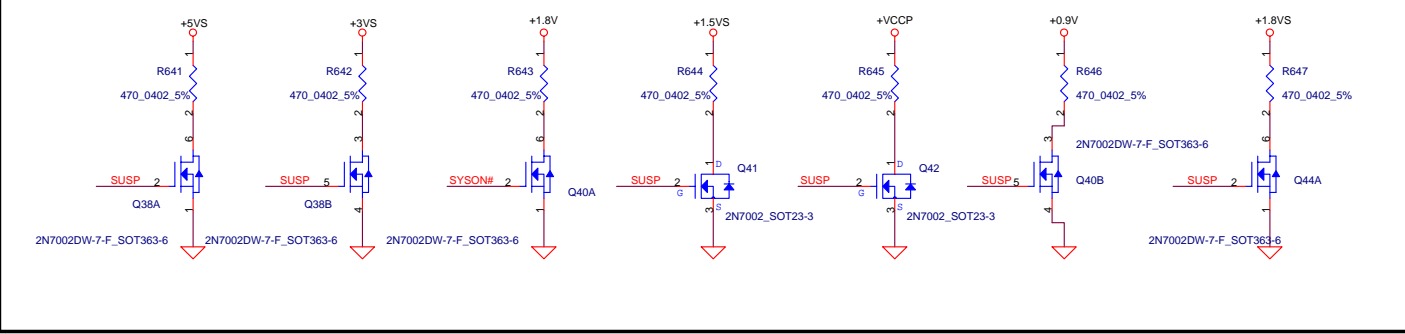
DIM LED



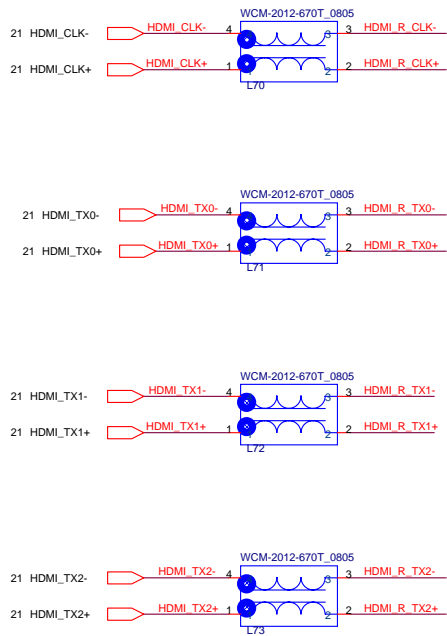
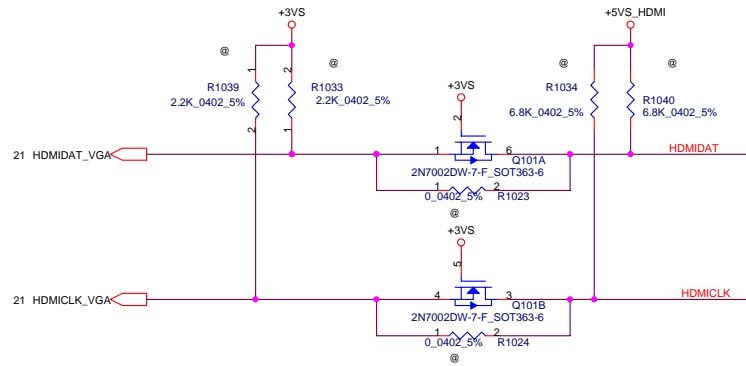
+1.8V to +1.8VS Transfer



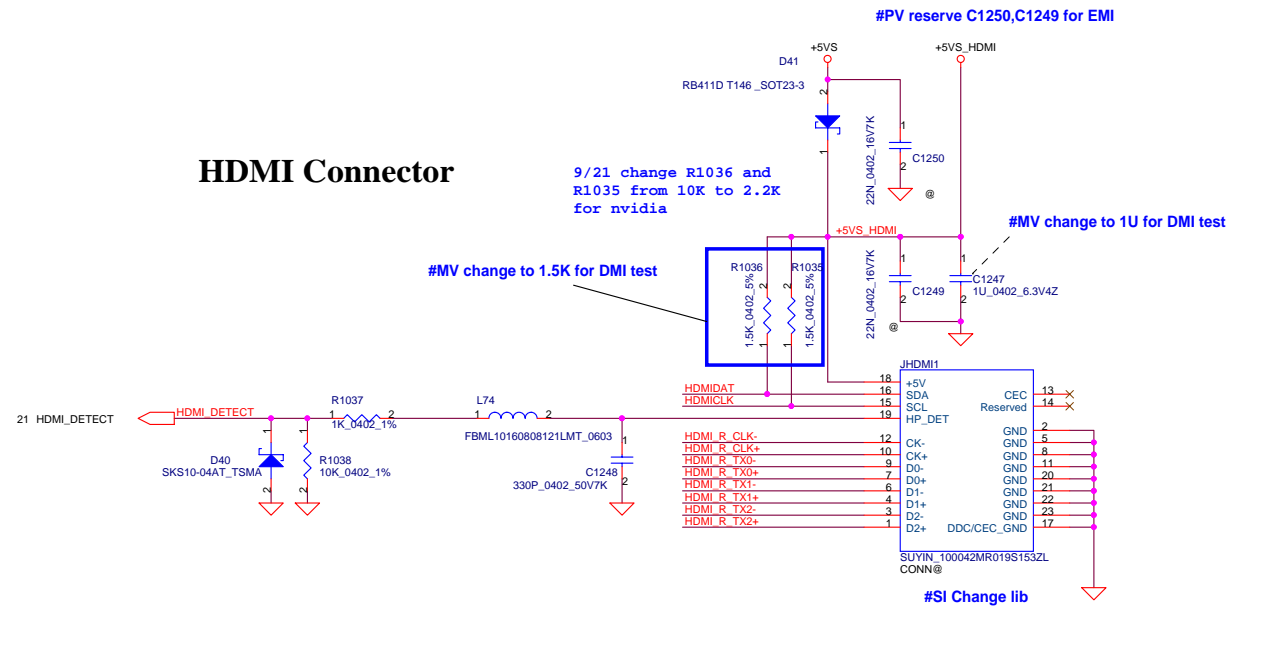
Discharge circuit



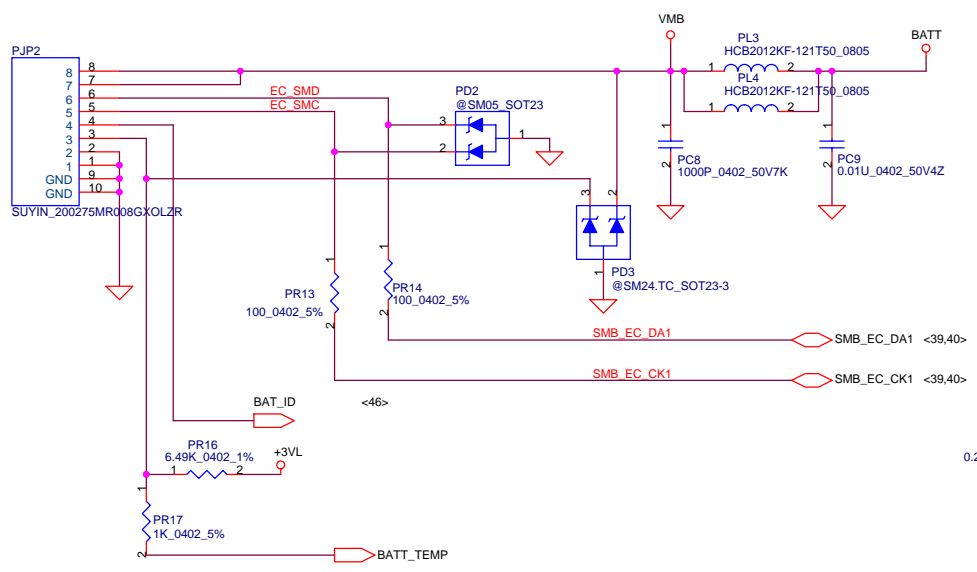
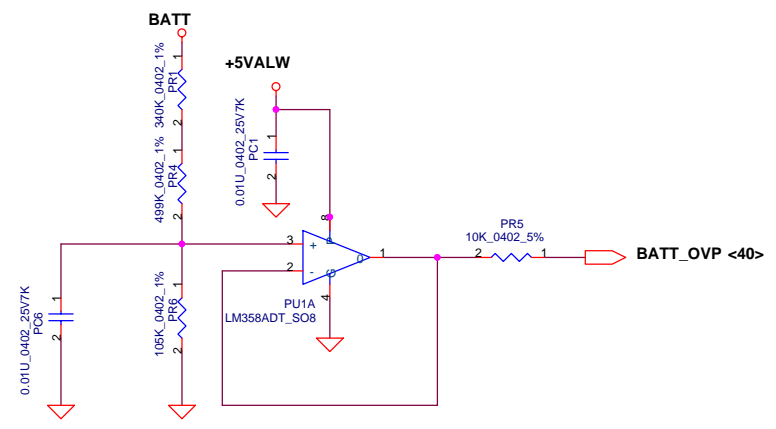
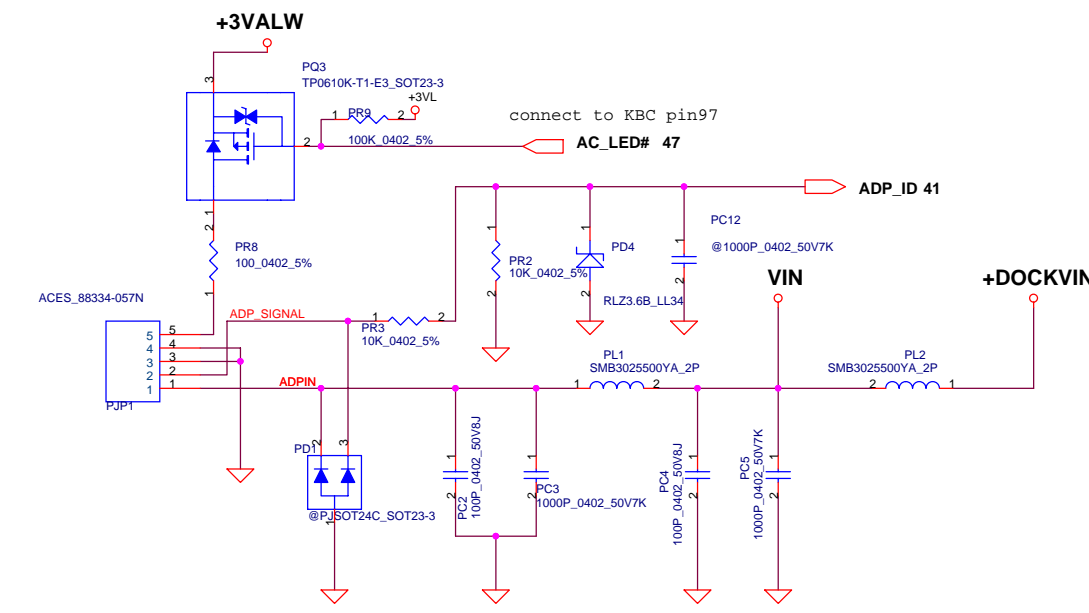
Security Classification	Compal Secret Data			Title	Compal Electronics, Inc.		
Issued Date	2008/02/25	Deciphered Date	2008/04/29	DC/DC Interface			
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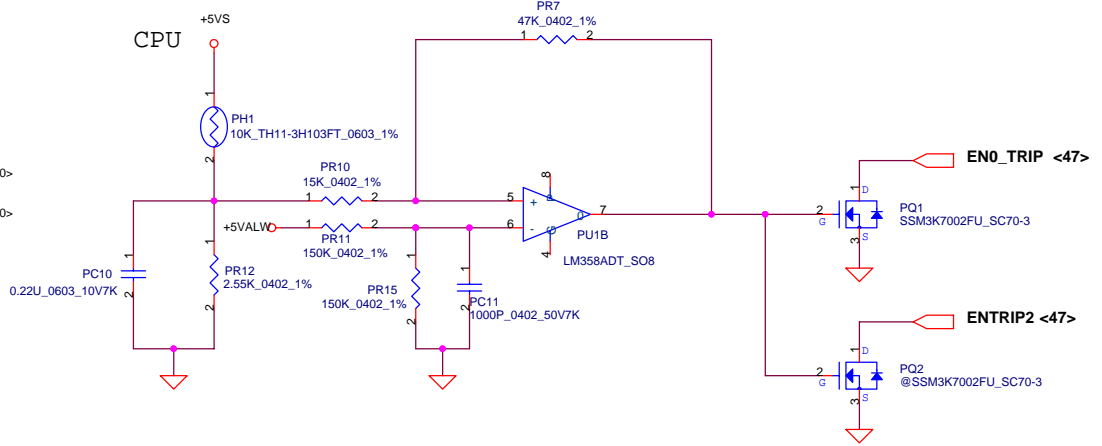
HDMI Connector



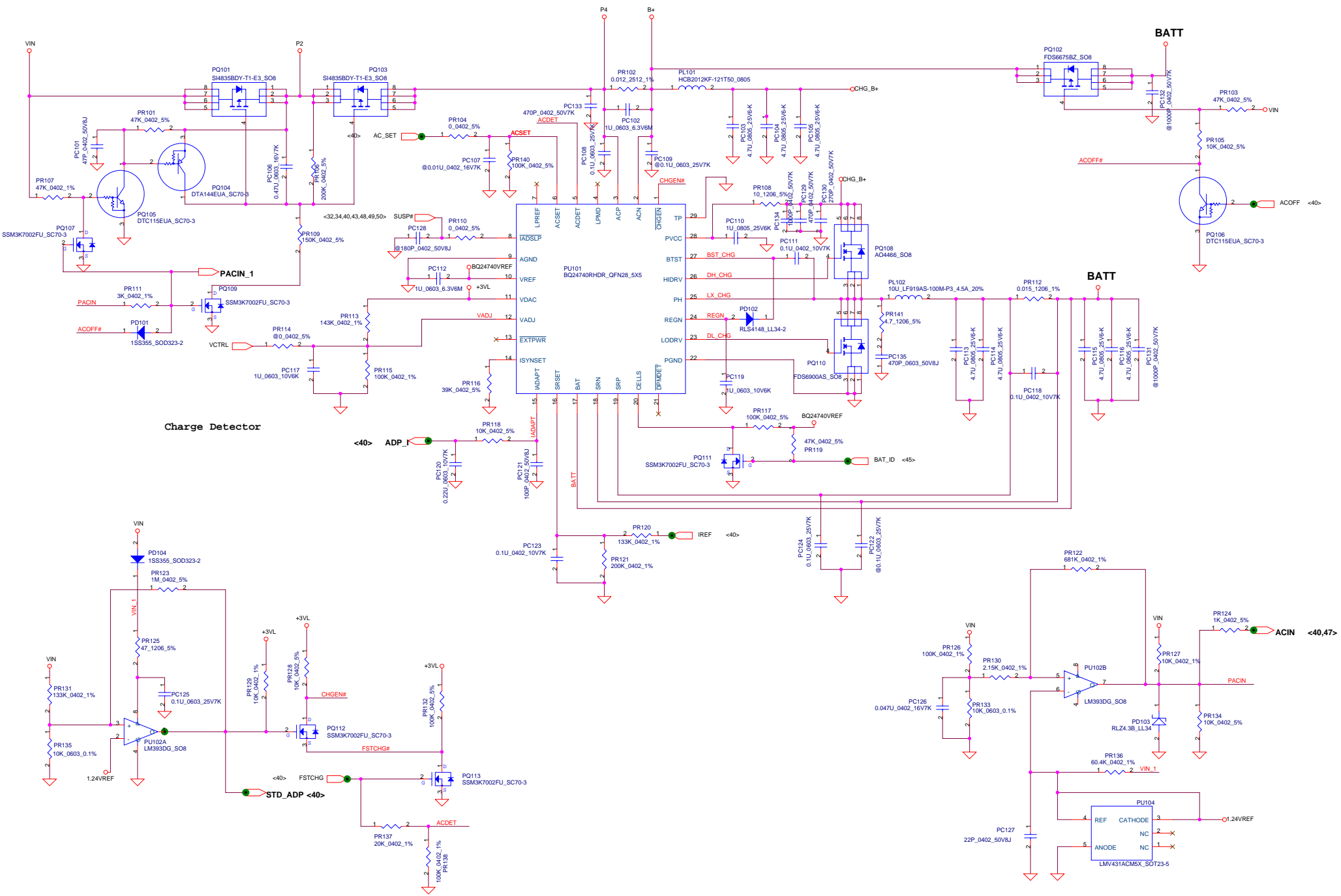
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Issued Date	2008/02/25	Deciphered Date	2008/04/29	Compal Electronics, Inc.	
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PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C



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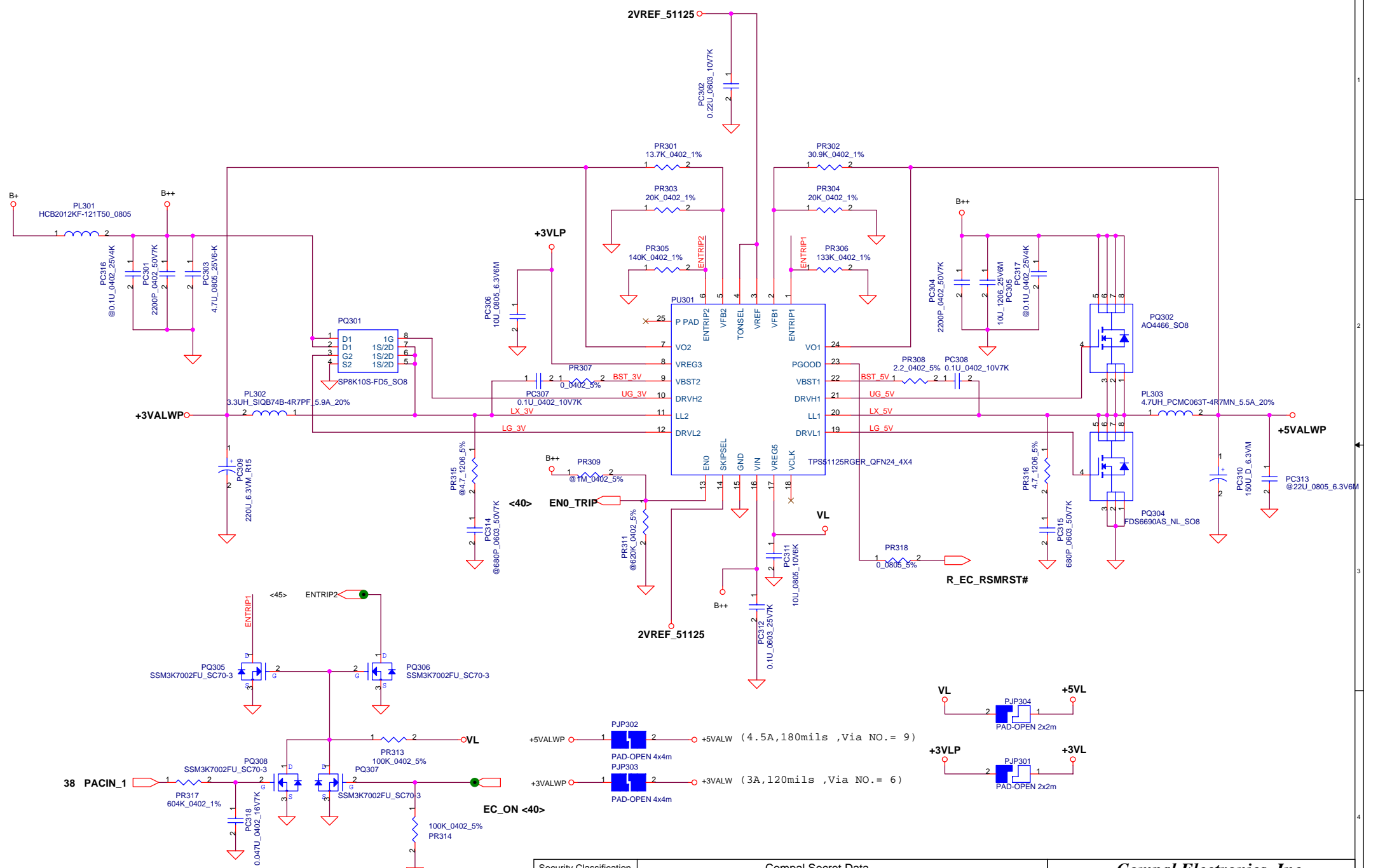


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Compal Electronics, Inc.

Charger

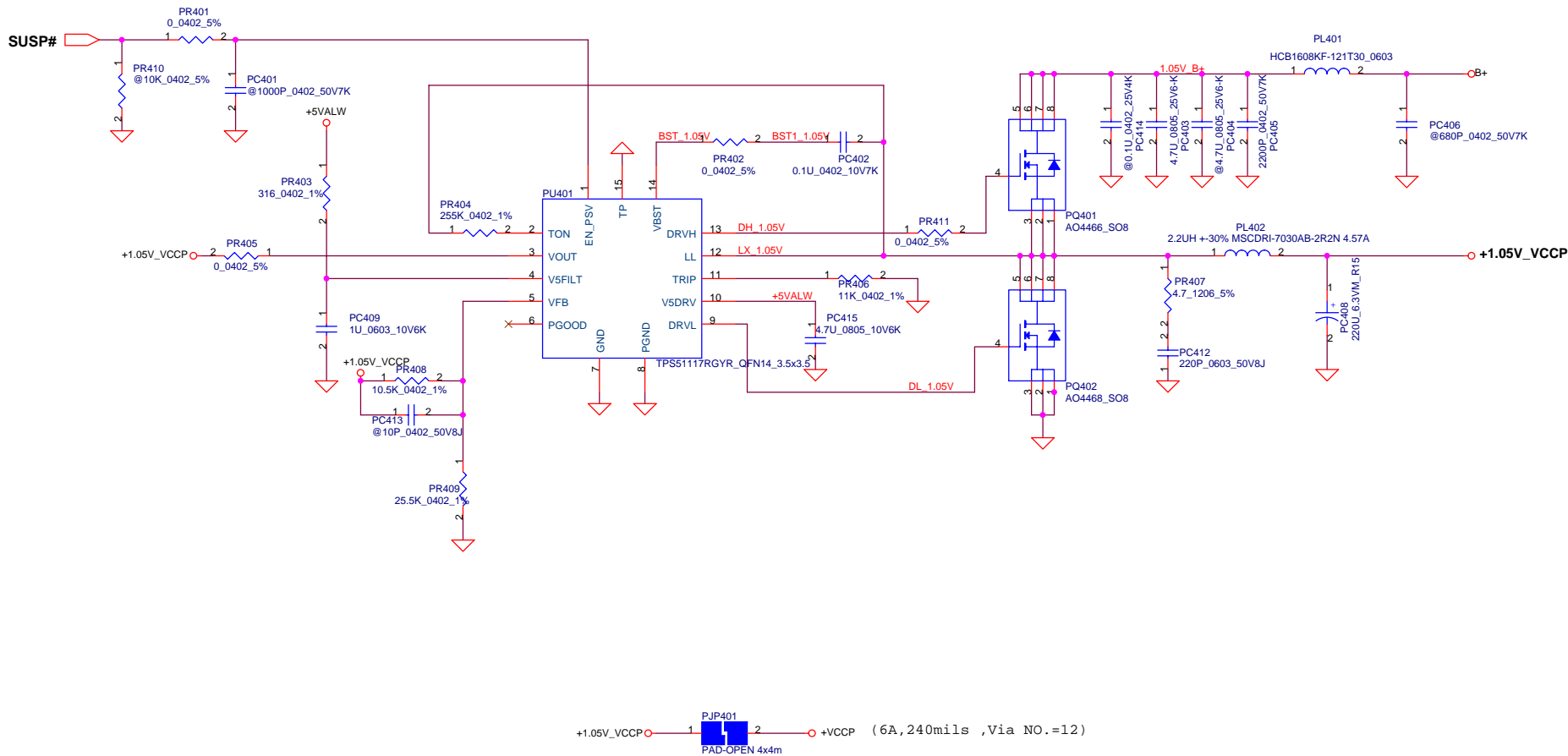
LA-4102P Blade discrete



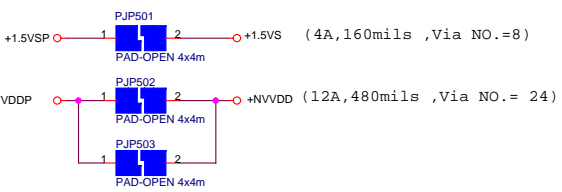
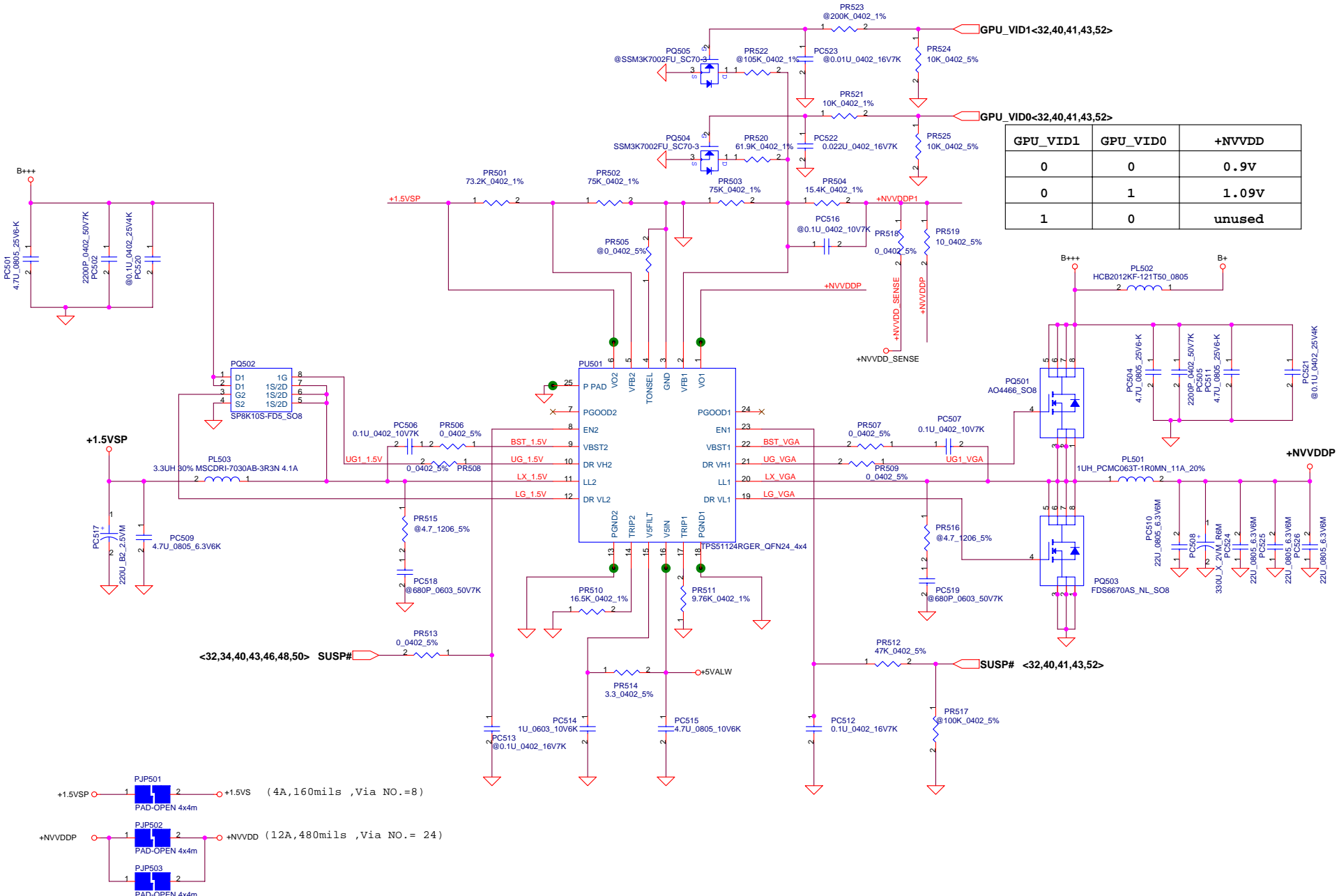
38 PACIN_1

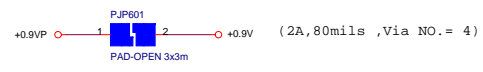
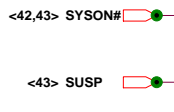
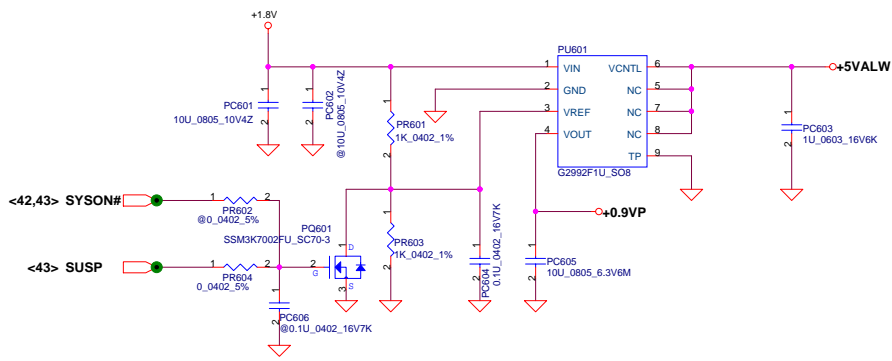
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Title		Compal Electronics, Inc.	
Document Number		3.3VALWP/5VALWP	
Date		Tuesday, April 29, 2008	
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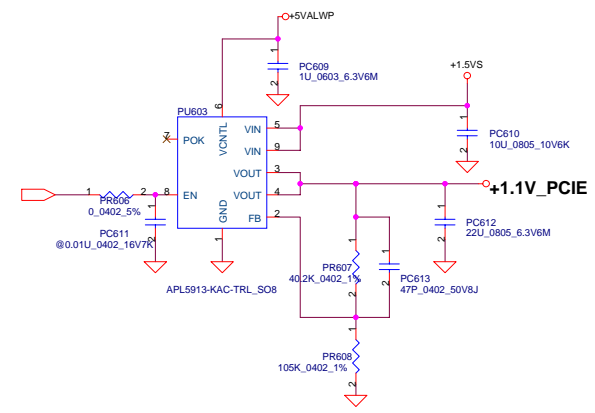


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<32,34,40,43,46,48,49> SUSP#



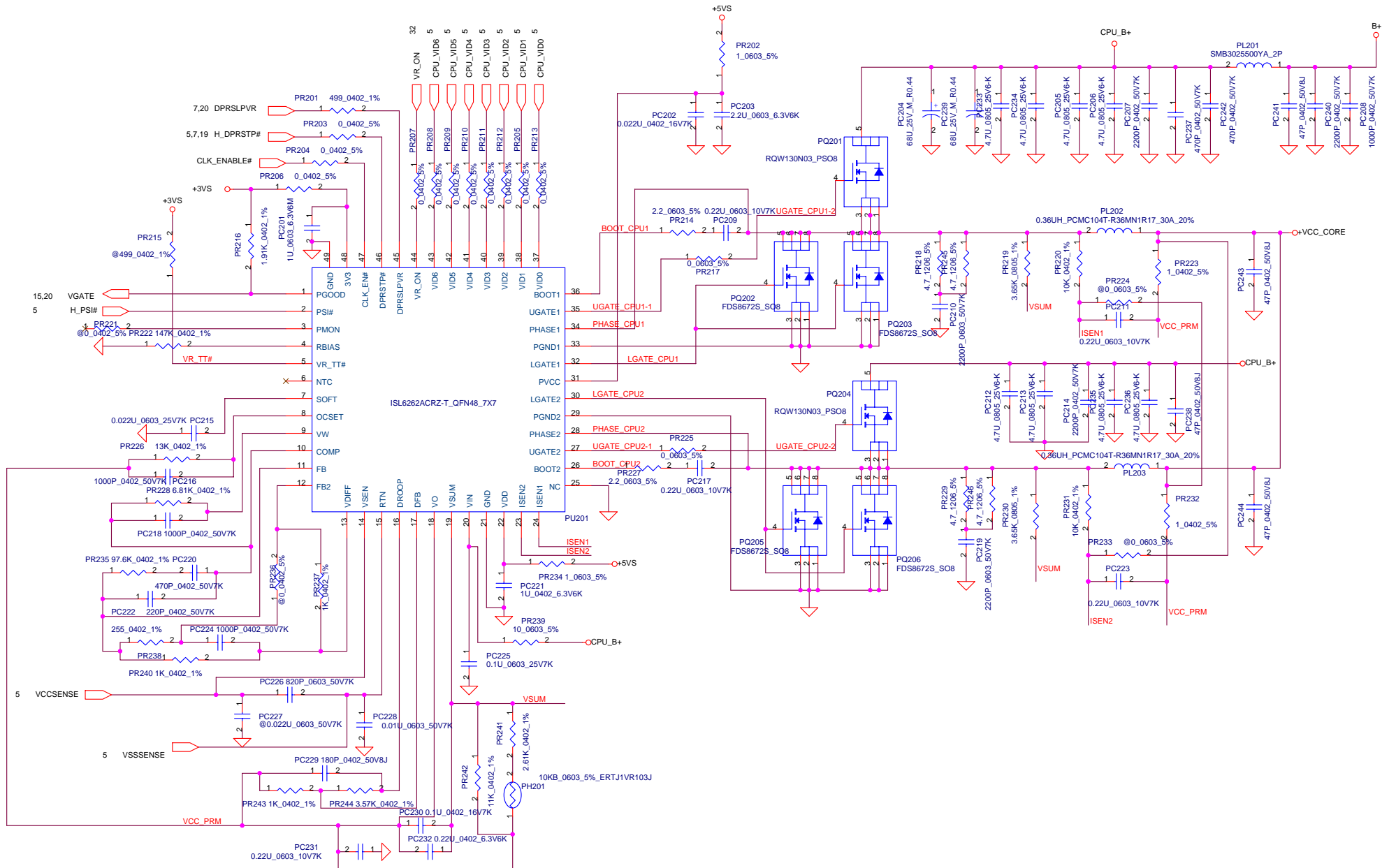
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Compal Electronics, Inc.

0.9VP/1.1V PCIE

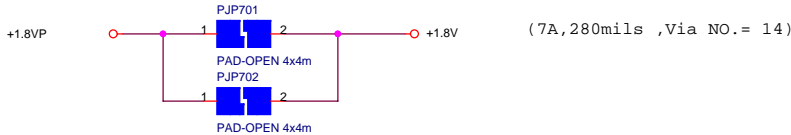
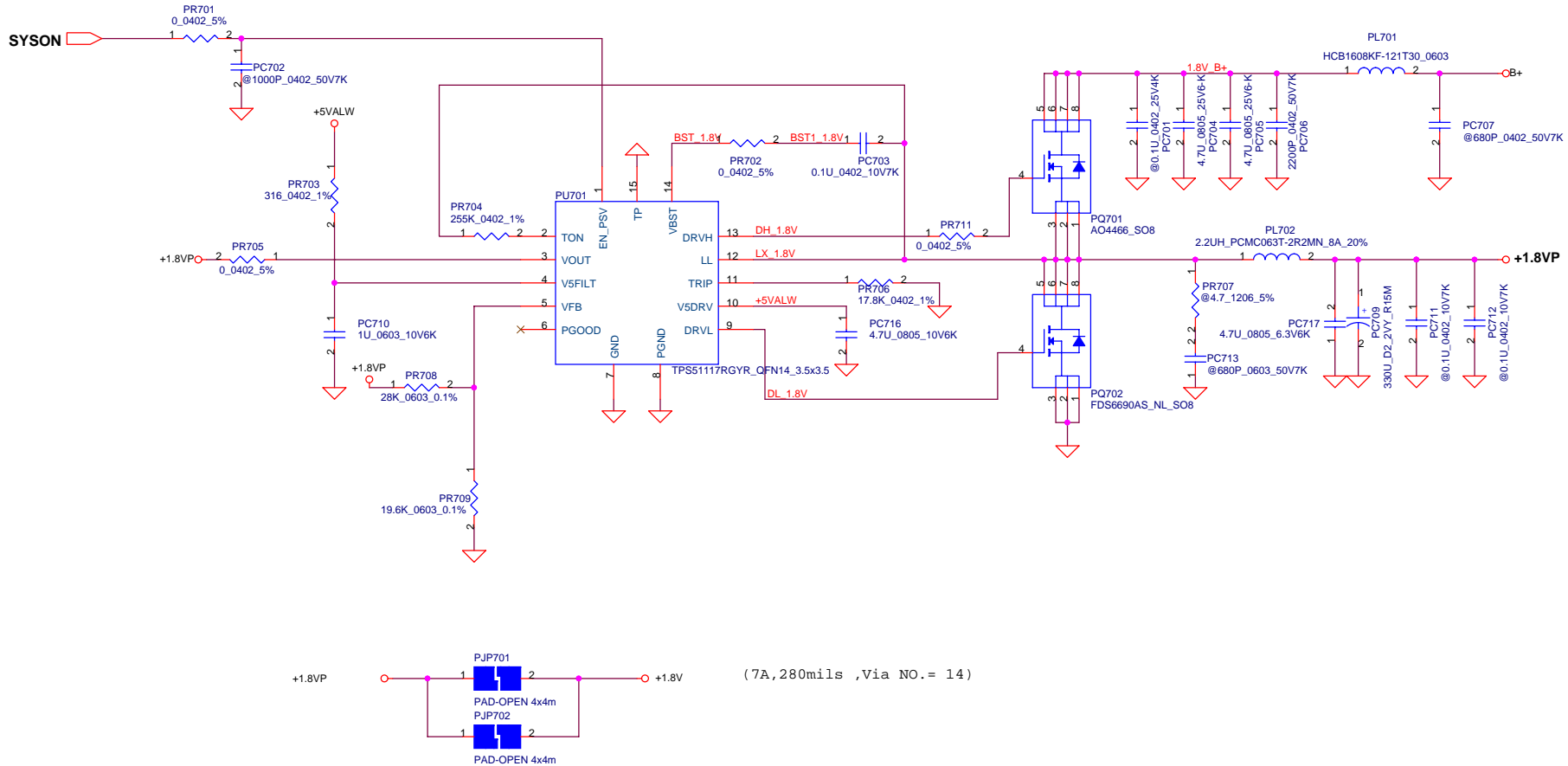
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Compal Electronics, Inc.	
Title	+CPU_CORE
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Size	Document Number	Date			Rev
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	43	DC Connector /CPU_OTP	11/06	Compal	Add PD4 & PC12	Add PD4 & PC12	
2	45	3.3VALWP/5VALWP	11/06	Compal	for Layout	Change PQ301, cancel PQ303.	
3	44	Charger	11/06	Compal	EMI solution	Add PC128	
4	49	CPU_CORE	11/06	Compal	EMI solution	Add PC240	
5	47	1.5VSP/VGA_CORE	11/06	Compal	for VGA voltage steps	Add PQ505, PR523, PR524, PR525	
6	45	3.3VALWP/5VALWP	12/31	Compal	PWR request	Add PU302, control signal changed to ACOFF	
7	44	Charger	12/31	Compal	EMI solution	Add PC129, PC130, PC131, PC132, PC133	
8	49	+CPU_CORE	12/31	Compal	EMI solution	Add PC242	
9	47	+1.5VSP/VGA COREP	01/02	Compal	HW request	Change PR513 to 0_ohm	
10	44	Charger	01/02	Compal	EMI solution	Add PC135 and PR141	
11	49	+CPU_CORE	02/15	Compal	Change high-side MOS for WWAN	Change PQ201 and PQ204 to powerpak	
12	43	DC Connector /CPU_OTP	02/15	Compal	AC LED change to KBC control	ACLEd# connect to EC pin 97	
13	43	DC Connector /CPU_OTP	02/19	Compal	WWAM issue	add PC241 47pF	
14	49	+CPU_CORE	02/19	Compal	WWAM issue	add PC243 PC244 47pF	
15	43	DC Connector /CPU_OTP	04/02	Compal	AC LED issue	Change AC_LED# pull-high to +3VL	

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Transation Fail	08	C41、 C42、 C43、 C44 Change ESR=7m ohm	11/21	DB
2	Disable TV out function from Docking	20	TV signal unconnected,DACB_VDD pull low 10K (R948).	11/07	DB
3	Update Connetor Library		CRT(JCRT1)、 HDMI(JHDMI1)、 ESATA(JP53)、 Finger print(JJP24)、 FAN(JP2)、 Speaker(JP60)、 Multi bay(JP12)、 Dual LED(D53、 D54	11/17	DB
4	Delete LVDS B channel	19,20	Schematic Delete	11/17	DB
5	USB camera Footprint error	19	Change U42 to G916-390T1UF SOT23, it adjustable mode, R1091=215K , R1093=100K,Add GPIO 20 to turn off power	11/07	DB
6	Reserve Card reader D3E function	27,32	GPIO6= CR_CPPE# , GPIO22=CR_WAKE#	11/17	DB
7	Swap PCIE LAN and New card	27	Swap PCIE4 and PICE6	11/17	DB
8	Change GPU 1.8VS power	20、 21	Change 1.8VS to +VDD_MEM18	11/17	DB
9	Change G sensor control from SB、 LED drive by +5VS	27、 39	Change G sensor control from SB	11/17	DB
10	Avoid Battery mode can't boot issue	38、 45	Add +3VALW GD to EC_RSMRST# to fix Battery mode can't boot issue	11/17	DB
11	Add G sensor ST and Bosch	37	Add G sensor ST and Bosch	11/17	DB
12	Change LAN solution (Marvell to Realtek)	30	Change LAN solution (Marvell to Realtek)	11/17	DB
13	LAN transformer interfere	30	U19 Change to correct transformer type	11/17	DB
14	Cardreader schematic review,add D3E function	32	R709-->10K、 R1047-->8.2K、 R1128-->Stuff、 R705-->@、 U37-->@、 Cardreader LED-->+5VS、 add D3E function	11/17	DB
15	Jack can't detect normal	33	R1059 change from 39.2 to 39.2K	11/17	DB
16	Docking can not power on	40	Add power on circuit D57,Q13R751,R752,R753	11/17	DB
17	HP audio team recommend	33、 35	C1480-C1487、 C1352、 C1354 change to 0.022U、 Amp output setup to 15.6 dB、 Reserve C747、 C748 for GNDA and GND	11/17	DB
18	Audio jack can't detect normal	35	Add Pull up resistor R750 to +3VALW	11/17	DB
19	Docking HP audio test fail	35	Add C795、 C796 to avoid DC level, and add R968、 R969 to reduce HP out level	11/17	DB
20	Leakage problem	38	Correct direction prectek leakage	11/07	DB
21	EC pin define update	38	Delete EC_PME#、 SYSON PU、 SUSP# PU、 LID_SW# change to +3VALW、 Delete CLKRUN#、 R582->@ for C0 chip、 CIR PU+5VL、 add 100P to BATT_OVP(EC recommend)	11/07	DB
22	Can't Hibernation(SLP_S4#)	38	Connect SLP_S4# to SB	11/17	DB
23	EC can't receive docking present	40	CONA# change +3VL	11/12	DB
24	Reserve capacitor on digital MIC for EMI request	19	Add C496,C498	11/07	DB
25	Add 2N7002 to GND on HDMI to avoid leakage.	21	Add Q74	01/04	SI
26	+VDD_MEM18 to +1.8VS, change to jumpper	22	Delete R1124,R1125 add PJP605	01/04	SI
27	HDCP ROM fail. HDCP_SCL need pull high.	22	R224 no stuff. R213 stuff.	01/04	SI
28	Reserve capacitor on digital MIC for SED. WWAN noise	26	Add C499,C502	01/04	SI

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	Change transformer vendor	30	change U19 library	01/04	SI
2	XMIT_OFF add a diode to avoid leakage.	31	Add D88	01/04	SI
3	Card reader recommend	32	XD_ALE need pull +3VS not pull low.	01/04	SI
4	change Q54 from transistor to MOS for cardreader LED.	32	Change Q54	01/04	SI
5	speaker pop issue	35	Change C1488 to 1U	01/04	SI
6	Reserve capacitor on SPI_FSEL#,CLK#,FER for EMI request	36	Add C2125,C2126,C2127	01/04	SI
7	Change EC_PME pull high from +3VL to +3VALW	38	R585 stuff	01/04	SI
8	Reserve damping resistor on SPI_CLK for EMI request	38	Add R191	01/04	SI
9	WLAN LED issue,WL_BLUE_LED# pull +3VS	39	Add R716	01/04	SI
10	Add bypass capacitance on sensor bottom	39	Add C261(4.7U)	01/04	SI
11	EC can't detect DOCK_PRESENT.	40	change R754 to 22 Ohm,R623 to 2K	01/04	SI
12	Add DOCK_VOL_UP#,DOCK_VOL_Down# pull +3VS	40	Add R594,R596	01/04	SI
13	SPDIF issue	40	follow Vader	01/04	SI
14	Docking CRT blurred	40	Change ping 31,39,22 connect to GND	01/04	SI
15	Change R650 and C770 to modify the power sequence	41	change R650 to 1K, C770 to 0.1u	01/04	SI
16	Add 12P on CLK_14M_ICH for WWAN noise	17	Add 12P on CLK_14M_ICH	02/15	PV
17	BKOFF# reserve pull low 10K	19	reserve R717	02/15	PV
18	Reserve CMD27 to support 64M X16	7,8	Reserve CMD27 to support 64M X16	02/15	PV
19	Reserve cap on HDA_BITCLK for WWAN noise issue	26	Reserve cap on HDA_BITCLK	02/15	PV
20	Reserve to prevent ESD issue	30	Reserve ESD diode on LAN LED pin	02/15	PV
21	Change WLAN and WWAN 0402 resistor to 0805	31	Change WLAN and WWAN 0402 resistor to 0805, and WLAN change to +3VS power plane	02/15	PV
22	Direct drive LED, and add D3E function diode	32	Direct drive LED and XD_ALE Pull L, and add D86 for D3E function	02/15	PV
23	Change R1092 value on BT power switch Gate	36	Change R1092 to 10K	02/15	PV
24	Correct AC_LED control by EC	38	AC_LED Change controll by EC	02/15	PV
25	Change all LED limit current resistor to 200 ohm	39	Change all LED limit current resistor to 200 ohm and add Touch pad LED for PR	02/15	PV
26	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	40	Add 33 ohm for MUTE_LED and DOCK_SLP_BTN#	02/15	PV
27	follow check list ver:1.5	6	change R13 to 56 ohm;change R2-R8 to 51 ohm;change R11 to 0ohm	02/20	PV
28	Reserve Cap for EMI	42	add C1250,C1249	02/20	PV

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Item	Fixed Issue (Reason for change)	PAGE	Modify List	Date	Phase
1	follow check list Ver:1.5	17	reserve R148	02/15	PV
2	follow check list Ver:1.5	9	change R45,R48 to 10K	02/15	PV
3	boot code "88" power sequence fail	27	add Diode from PWROK to RSMRST	02/15	PV
4	Change BT,LAN,DOCK,Multibay connect for DFX			02/15	PV
5	Change WWAN and WLAN LED	39		02/15	PV
6	For EMI	37	SPI_CLK add R2118 , R2119 , R2120 => 33ohm add C2125 , C2126 , C2127 => 22pF;R553, 554, 556 =>10ohm	02/15	PV
7	For EMI	30	LAN add C656 and C657 => 0.1uF	02/15	PV
8	For EMI	39	T/P add D28 and C729	02/15	PV
9	remove LAN EEPROM	30		02/15	PV
10	For EMI	26	Add SSC circuit for HDA_BITCLK	03/11	PV2
11	For ESD	38	add 0.1U for EC_PME# and PCI_RST#	03/11	PV2
12	Change WWAN power to +3VS	31	Change WWAN power to +3VS	03/11	PV2
13	For ESD	06	Delete XDP connector	03/11	PV2
14	Delete LID switch pin1(+3VALW)	39	Delete LID switch pin1(+3VALW)	03/11	PV2
15	AT24C16B rising/falling time issue	21	change R213,R215 form 10K to 2.2K.	03/11	PV2
16	the Smbus pull wrong power rail	38	change R573,R577 pull +3VL	04/29	MV
17	change Lid pull high power	38,39	change R583 pull +3VL;JP11 pin4 connect to +3VL	04/29	MV
18	Clock REQ need external pull high	31,30	add R442,R440,R444,R455	04/29	MV
19	For HDMI certification	42	C1247 change to 1U;R1036,R1035 change to 1.5K	04/29	MV
20	For 2nd source thermal sensor	6	U1 pin 6 pull high 10K ohm	04/29	MV
21	Docking headphone issue	11	Add Q48	04/29	MV
22	Multibay shout down issue	35	Add C797	04/29	MV
23	wrong strap pin setting	11	no stuff R71,R81,R72,R77,R78	05/08	MV
24	reduce internal MIC noise	35	changw R1077 to 1K	05/08	MV
25					
26					
27					
28					

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