DELL Vostro 1320
COMPAL LA-4232P - KAL80

Half Penny Bridge 13.3
Compal Confidential

Schematic Document

Cantiga + ICH9

2009 / 06 / 01 Rev:1.0(A00)

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DELL Vostro 1320
COMPAL LA-4232P

Half Penny Bridge 13.3

ZZZ1
PCB

CRT
+CRT_VCC P.16

LVDS Panel Interface
+LCDVDD
+3VS
B+ P.16

Thermal Sensor
ADT7421ARMZ
+3VS P.4

Fan conn
+5VS P.4

Penryn -4MB (Socket P)
uFCPGA-478 CPU
+CPU_CORE
+VCCP
+1.5VS P.4,5,6

H_A#(3..35)
H_D#(0..63)
FSB
800/1066 MHz 1.05V

CK505 SM IC -72
Clock Generator
CS9LPRS387BKLFT
+1.05VS_CK505
+3VS_CK505 P.15

nVidia
NB9M-GS
+1.8VS
+VGA_CORE
+1.1V_GFX_PCIE
+3VS P.31,32,33,34

VRAM x 2
+1.8VS P.35

Intel Cantiga MCH
1329pin BGA
+3VS_DAC_CRT
+3VS_DAC_BG
+1.05VS_DPLLA
+1.05VS_DPLLB
+VCCP
+1.8V_TXLVDS P.7,8,9,10,11,12

DDR2 667/800MHz 1.8V
Dual Channel

DDR2-SO-DIMM X2
BANK 0, 1, 2, 3
+1.8V +0.9VS P.13,14

DMI X4
C-Link

Intel ICH9-M
676pin BGA
+RTCVCC
+1.5VS
+VCCP
+3VALW P.17,18,19,20

USB2.0
Azalia
SATA 0
SATA 1
PCI-E BUS

USB conn x 4
+5VALW P.29

FingerPrinter
+3VS P.29

Felica Conn
+5VS P.29

BT Conn
+3VS P.29

Camera
+5VS +3VS P.29

Express Card
+3VS +1.5VS P.26

Mini-Card-1
+1.5VS +3VS P.23

10/100/1000 LAN
REALTEK
RTL8111DL
+LAN_IO P.21

RJ45/11 CONN

Mini-Card-1
(WLAN)
+1.5VS
+3VS P.23

CardBus Controller
O2MICRO OZ888
+1.8VS_CB
+3VS_PHY P.30

1394

Media Card
+3VS_CR

Express Card
+1.5VS
+3VS P.26

LPC
LPC BUS

TPM
SLB 9635
+3VS P.28

Mini-Card-2
(WLAN)
+1.5VS
+3VS P.23

ENE KB926
+3VALW
+EC_AVCC P.27

Touch Pad CONN.
+5VS P.28

Int.KBD
P.28

BIOS(System/EC)
+3VALW P.27

Audio CODEC
92HD81
+3VS
+5VS P.24

Digital Mic
P.24

Audio Jack
P.24

SATA HDD Connector
+5VS P.22

CDROM Conn.
+5VS P.22

Power On/Off CKT.
P.28

DC/DC Interface CKT.
+5VS P.36

Power Circuit DC/DC
P.36~P.45

RTC CKT.
+RTCVCC P.39

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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
CONN@: connect
VGA@: discrete component
UMA@: uma component
TPM@: TPM compoent

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

	USB PORT#	DESTINATION
ICH9-M	0	JUSBP1
	1	CAMERA
	2	JUSBP3(SINGLE)
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3(DUEL TOP)
	9	JUSBP3(DUEL BOTTOM)
	10	NA
	11	NA

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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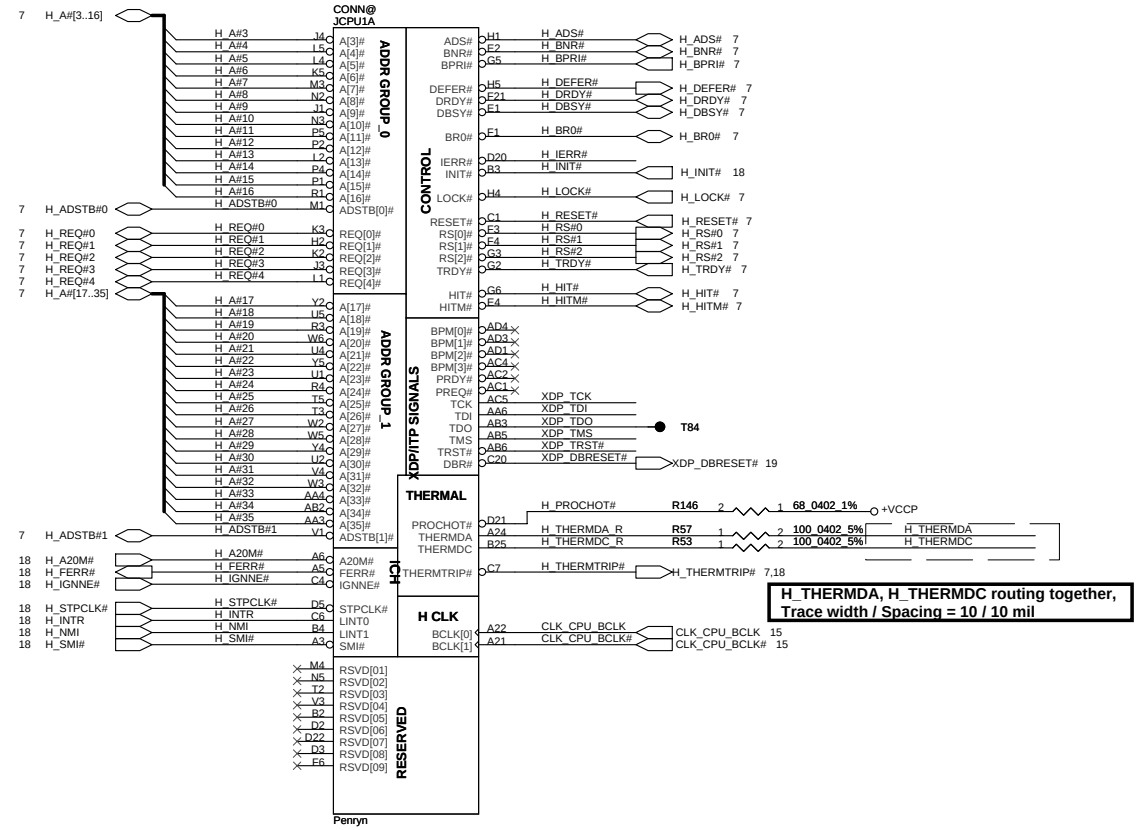

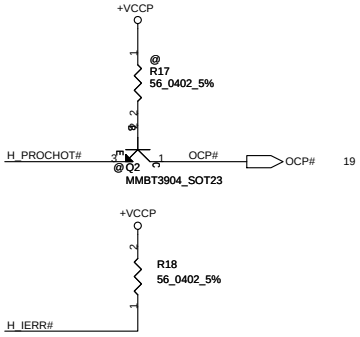

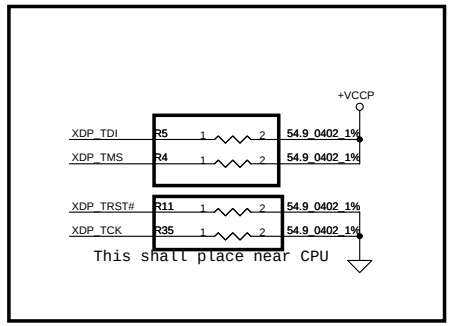

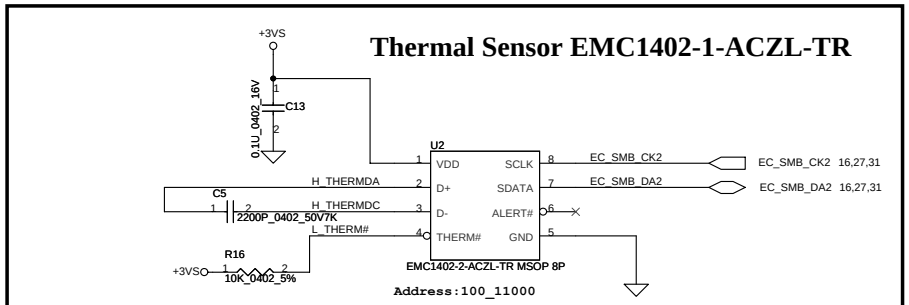

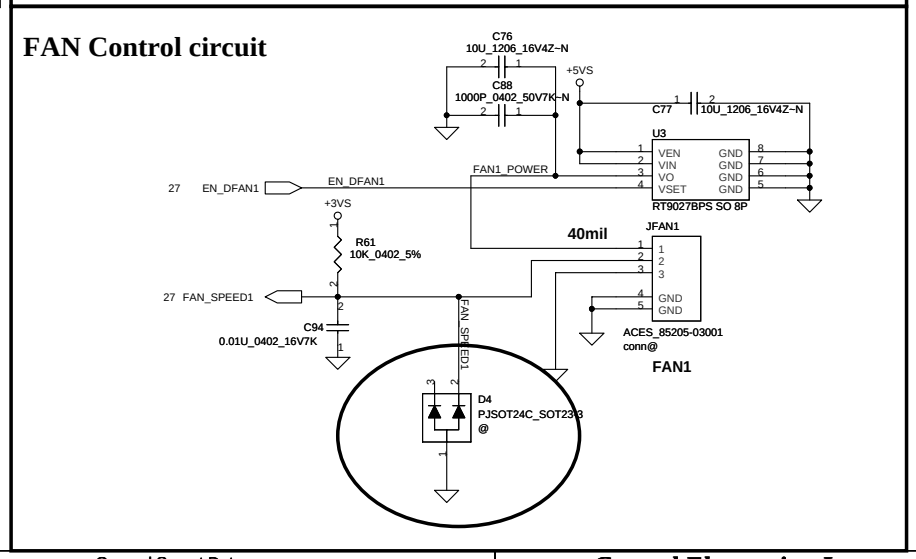

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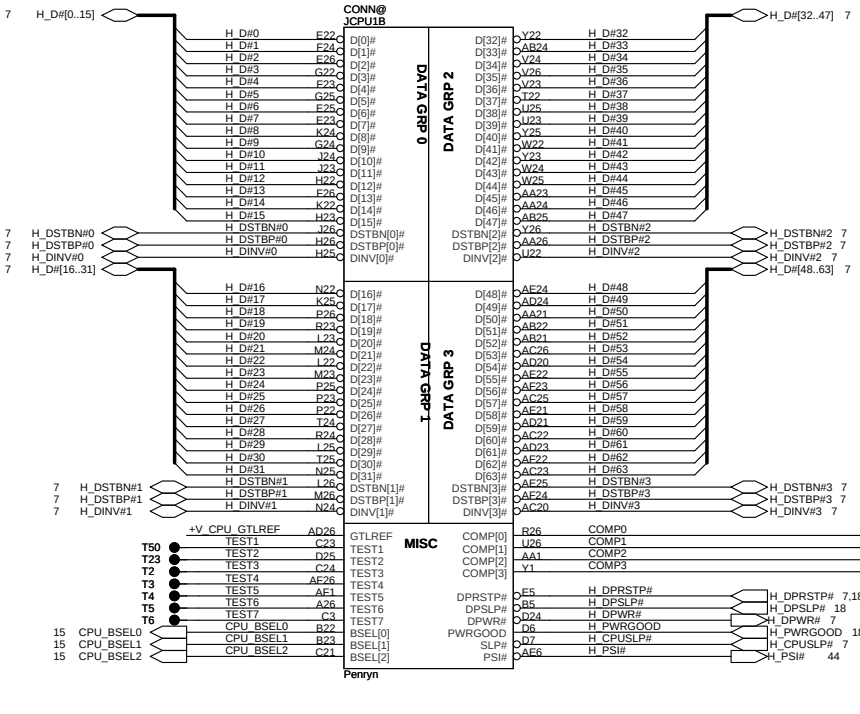
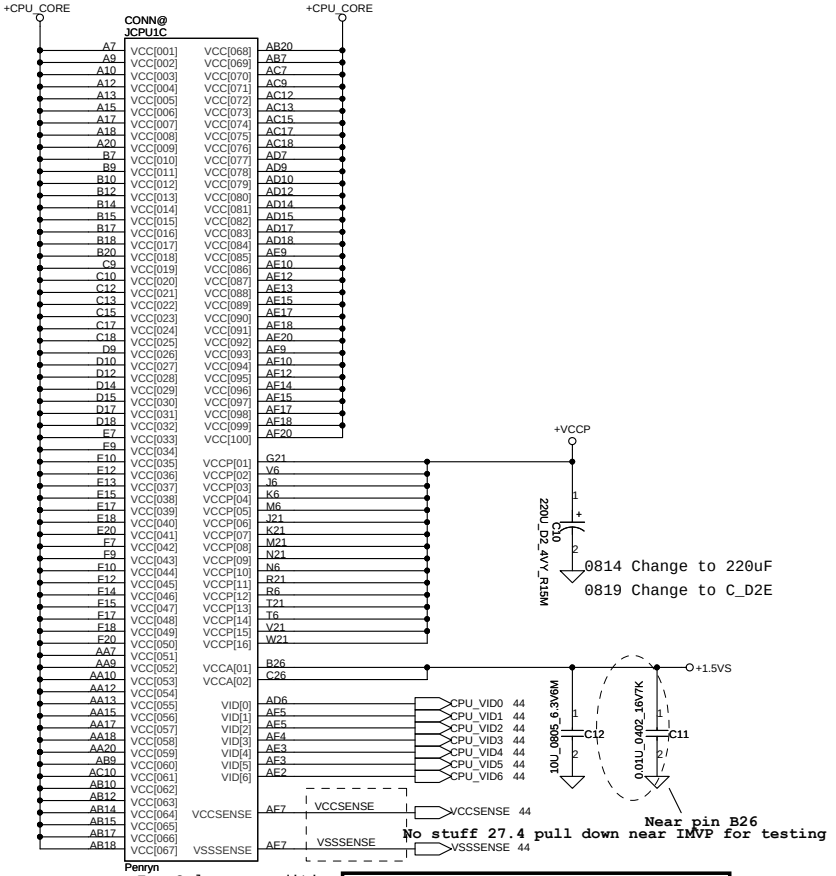




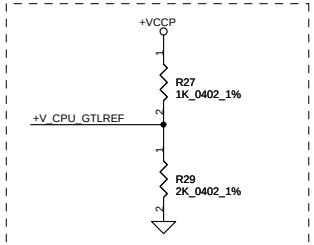
layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU

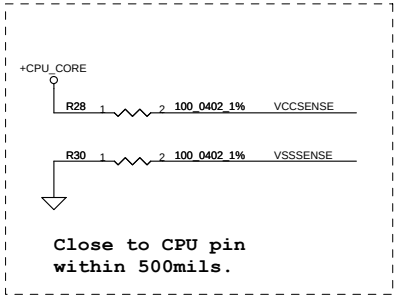
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 21 mils. COMP[1,3] trace width is 5

Length match within 25 mils. The trace width/space/other is 20/7/25.





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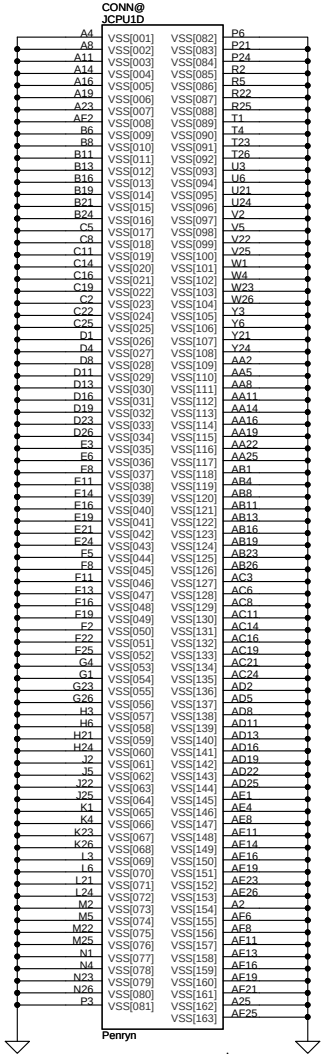
High Frequence Decoupling

10uF 0805 X5R -> 85 degree.



Place these caps inside the CPU socket cavity.
(Left side on Top).

+CPU_CORE

C216 10U_0805_6.3V6M — C205 10U_0805_6.3V6M — C529 10U_0805_6.3V6M — C232 10U_0805_6.3V6M — C258 10U_0805_6.3V6M — C505 10U_0805_6.3V6M — C504 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Left side on Top).

C257 10U_0805_6.3V6M — C261 10U_0805_6.3V6M — C214 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Top side).

+CPU_CORE

C190 10U_0805_6.3V6M — C210 10U_0805_6.3V6M — C254 10U_0805_6.3V6M — C208 10U_0805_6.3V6M — C203 10U_0805_6.3V6M — C200 10U_0805_6.3V6M — C206 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Right side on Top).

C204 10U_0805_6.3V6M — C215 10U_0805_6.3V6M — C226 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Left side on Bottom).

+CPU_CORE

C501 10U_0805_6.3V6M — C508 10U_0805_6.3V6M — C514 10U_0805_6.3V6M — C519 10U_0805_6.3V6M — C522 10U_0805_6.3V6M — C533 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Bottom).

+CPU_CORE

C502 10U_0805_6.3V6M — C510 10U_0805_6.3V6M — C515 10U_0805_6.3V6M — C520 10U_0805_6.3V6M — C526 10U_0805_6.3V6M — C532 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Left side on Top).

+CPU_CORE

C202 330U_D2E_2.5VM_R9 — C207 330U_D2E_2.5VM_R9

C259 330U_D2E_2.5VM_R9 — C255 330U_D2E_2.5VM_R9

Place these caps inside the CPU socket.
(Right side on Top side).

ESR <= 1.5m ohm

Capacitor > 880 uF

+VCCP

C213 0.1U_0402_16V — C209 0.1U_0402_16V — C212 0.1U_0402_16V — C185 0.1U_0402_16V — C183 0.1U_0402_16V — C184 0.1U_0402_16V

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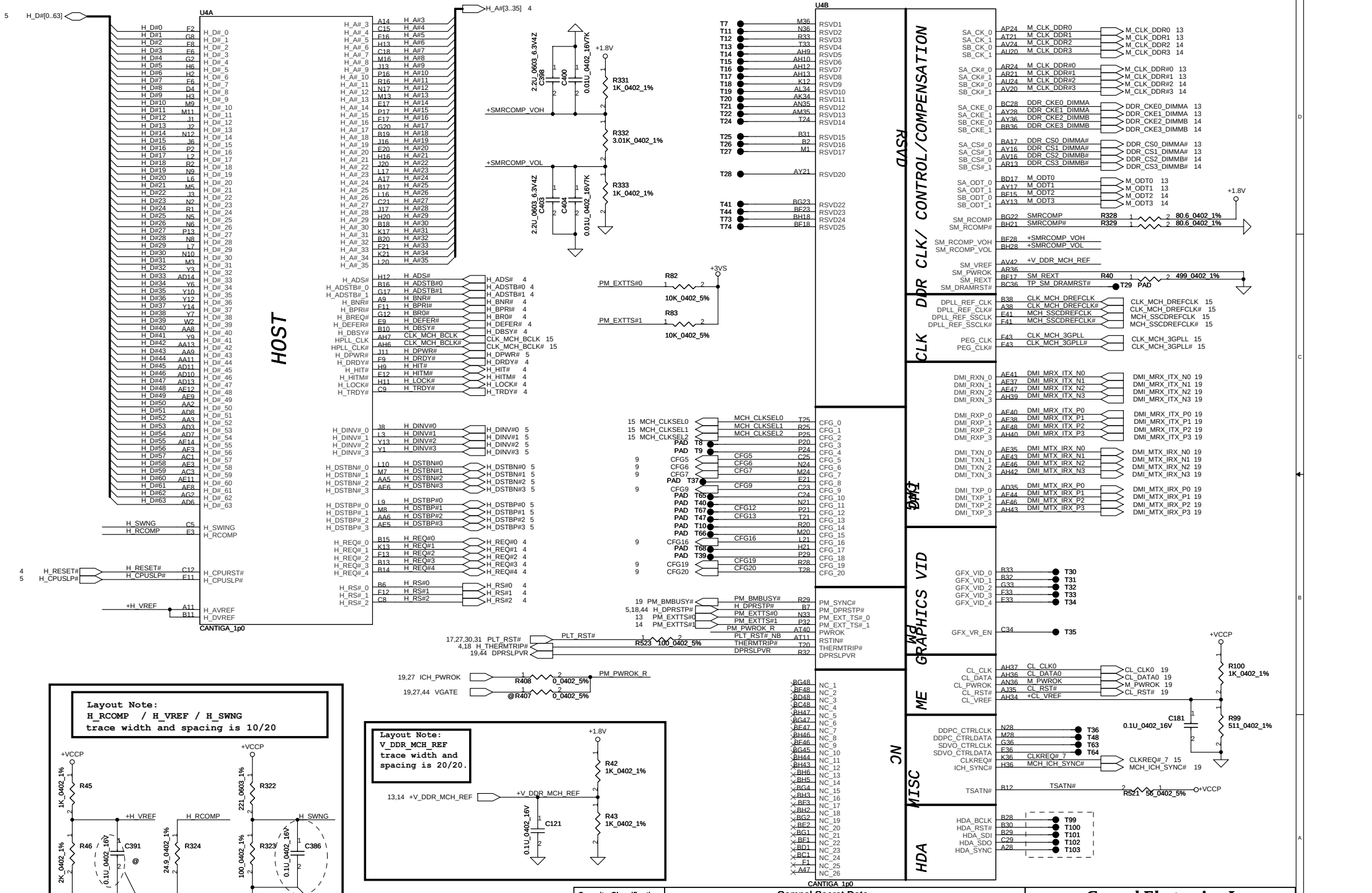

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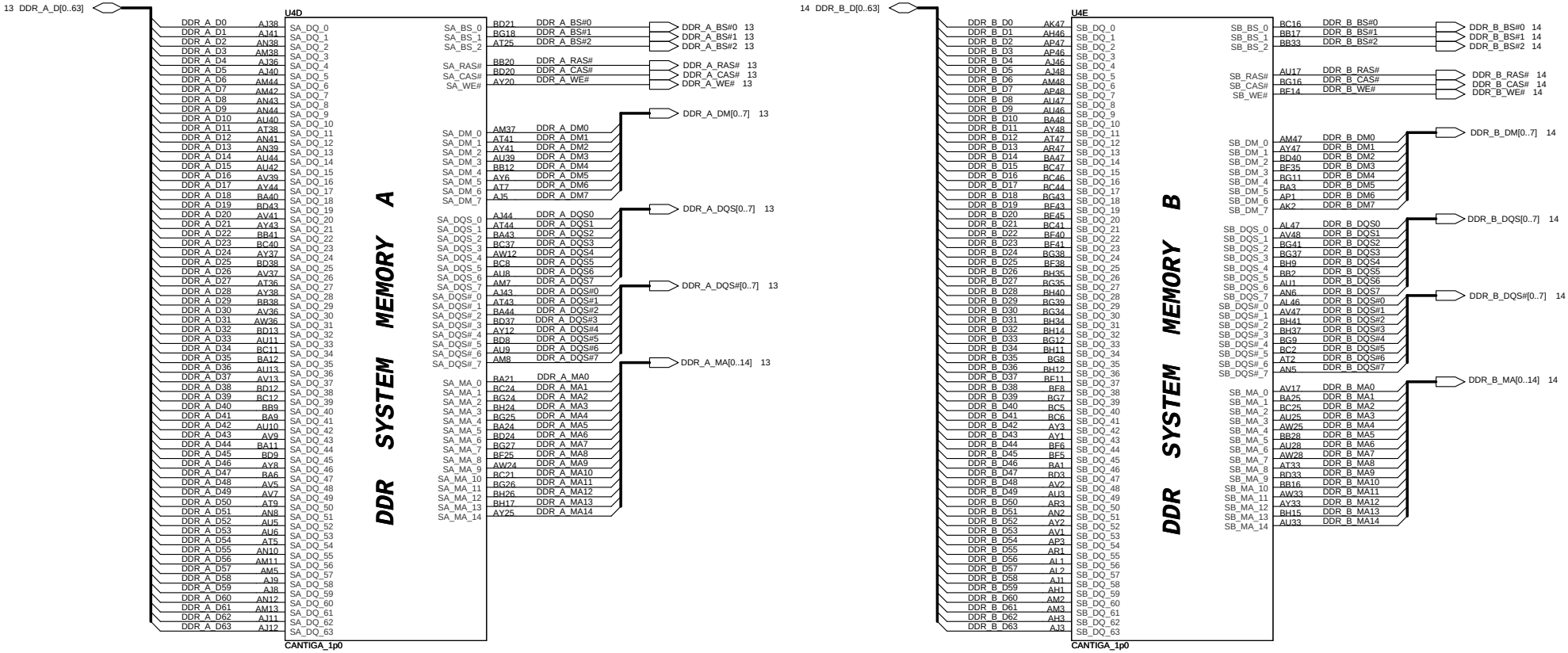

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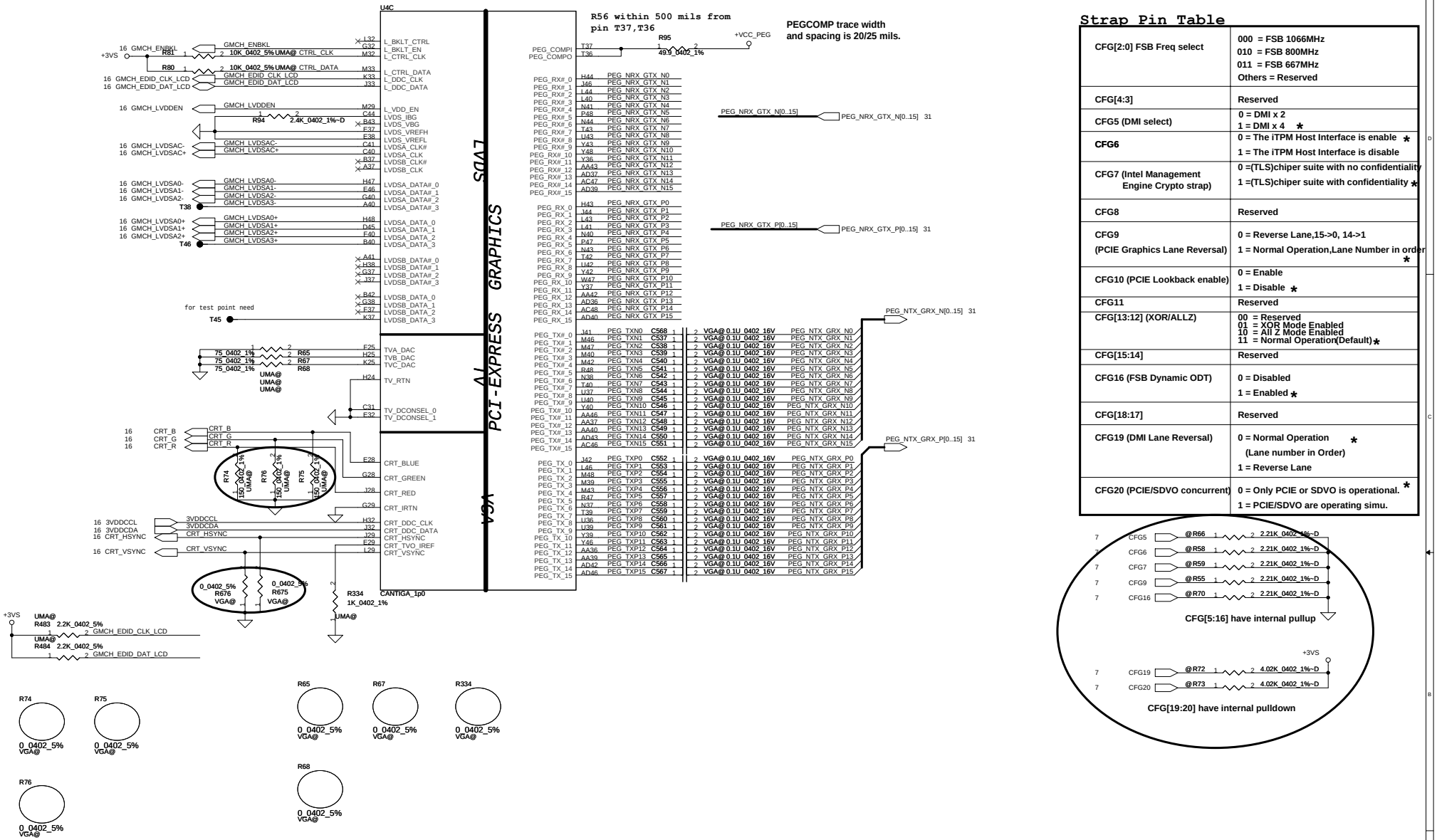

Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable * 1 = The iTPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIE Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

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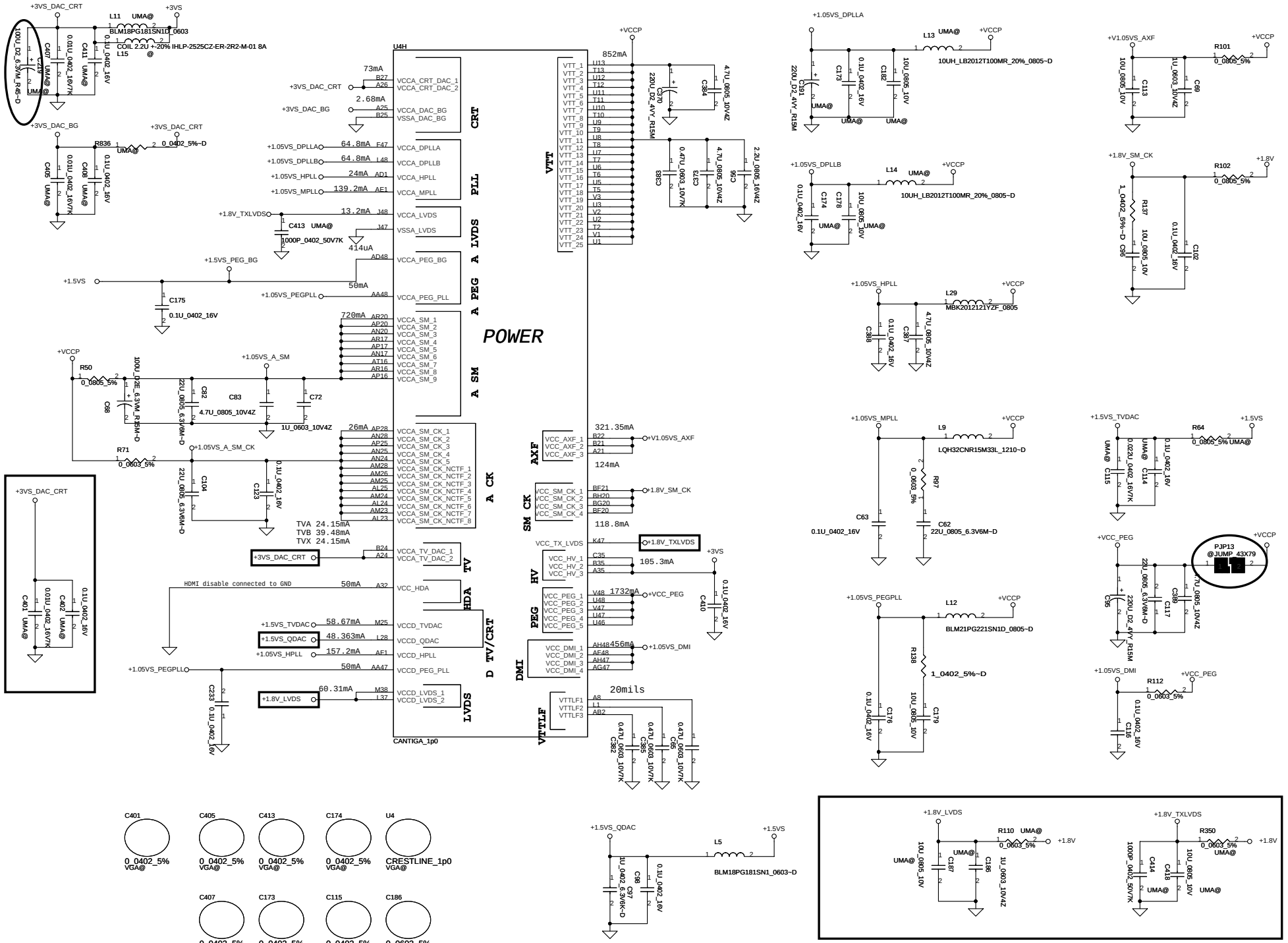

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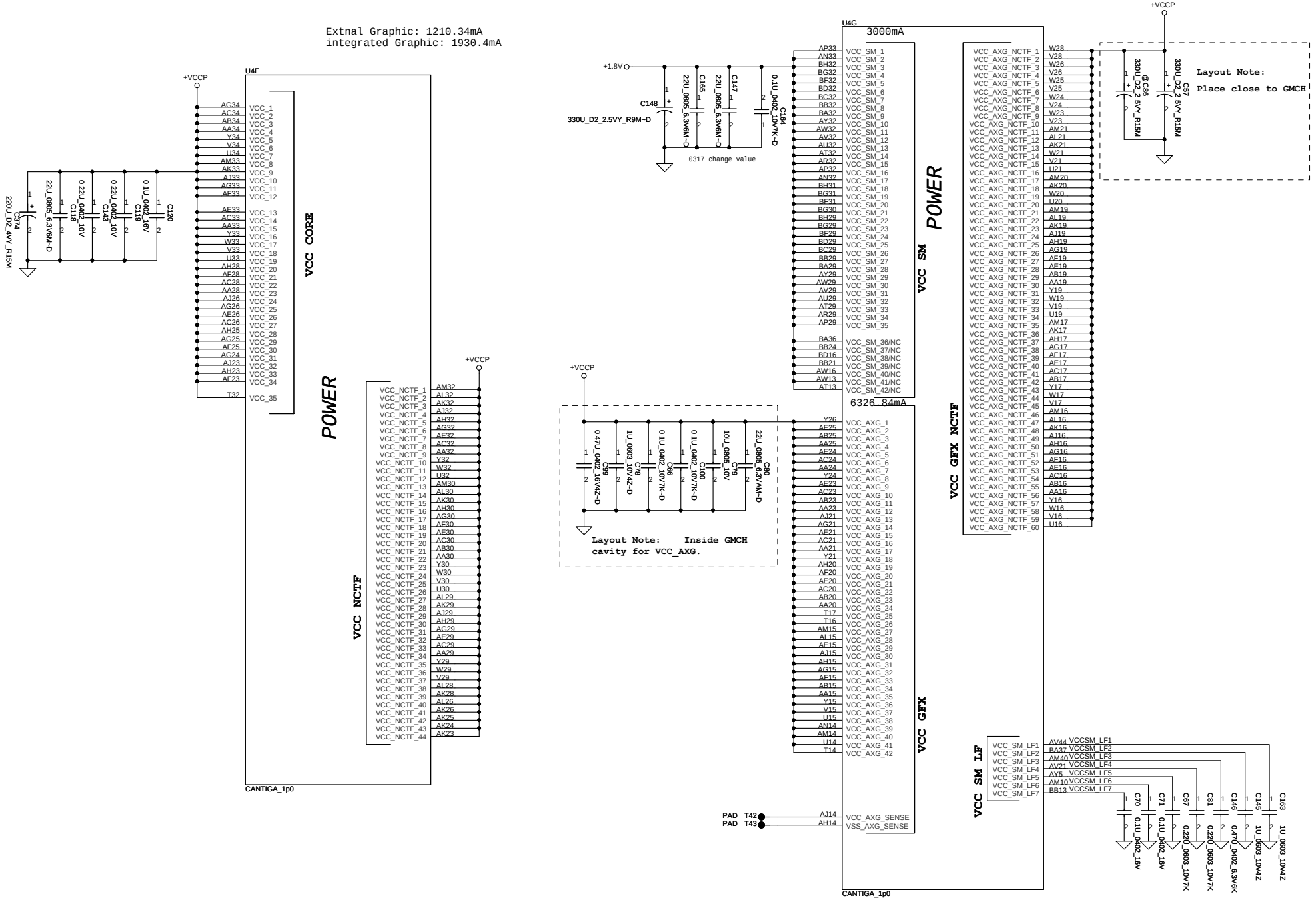
Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



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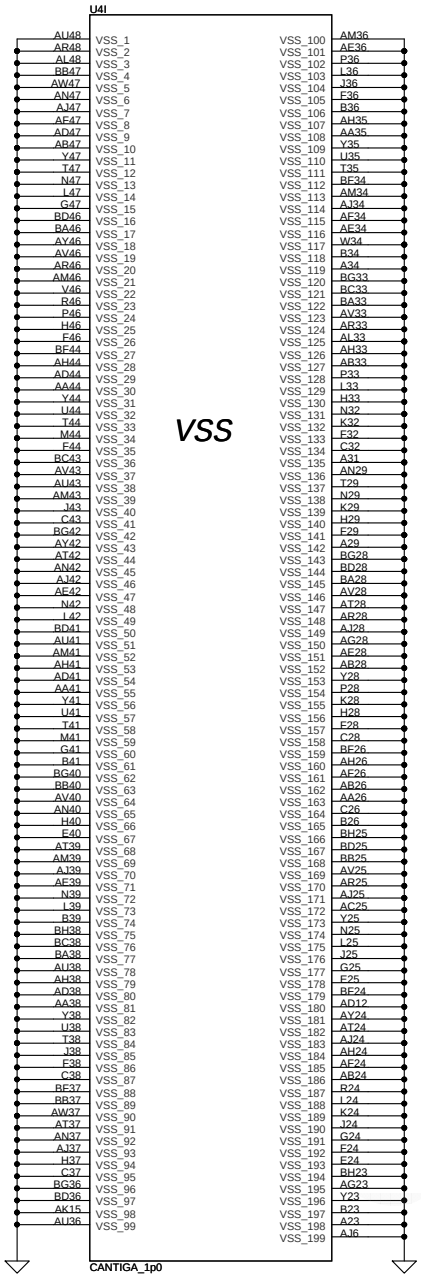

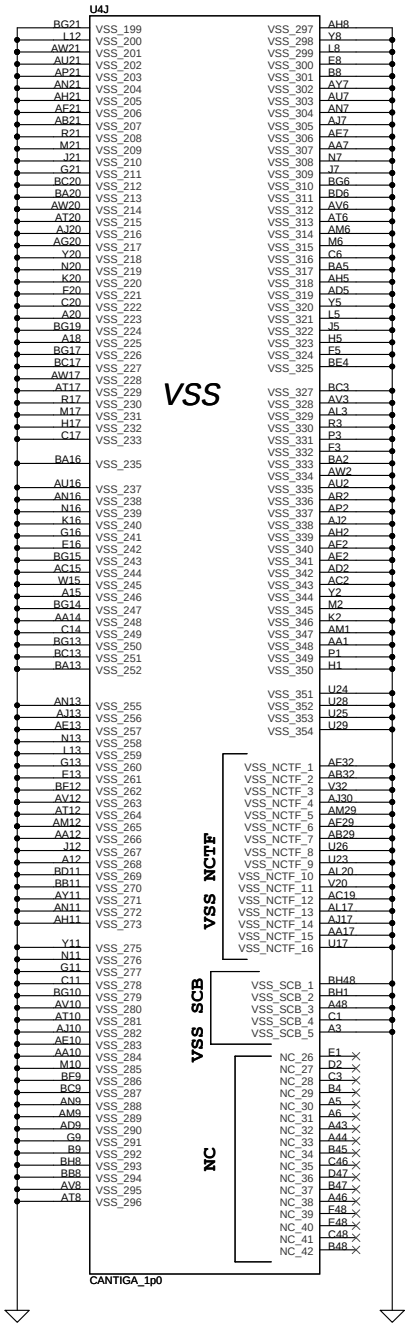

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8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

Layout Note:
Place near JDIM1

+1.8V

C105 2.2U_0603_6.3V6K
C124 2.2U_0603_6.3V6K
C149 2.2U_0603_6.3V6K
C166 2.2U_0603_6.3V6K
C169 2.2U_0603_6.3V6K
C154 0.1U_0402_16V
C131 0.1U_0402_16V
C130 0.1U_0402_16V
C108 0.1U_0402_16V
C84 330U 2.5V Y D2 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9VS

C106 0.1U_0402_16V
C125 0.1U_0402_16V
C126 0.1U_0402_16V
C127 0.1U_0402_16V
C150 0.1U_0402_16V
C151 0.1U_0402_16V
C167 0.1U_0402_16V
C107 0.1U_0402_16V
C128 0.1U_0402_16V
C129 0.1U_0402_16V
C152 0.1U_0402_16V
C153 0.1U_0402_16V
C168 0.1U_0402_16V

Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"

+0.9VS

RP14 56_0404_4P2R_5%: DDR_A_MA5, DDR_A_MA8
RP22 56_0404_4P2R_5%: DDR_A_MA12, DDR_CKE0_DIMMA
RP13 56_0404_4P2R_5%: DDR_A_MA1, DDR_A_MA3
RP17 56_0404_4P2R_5%: DDR_A_MA7, DDR_A_MA6
RP7 56_0404_4P2R_5%: DDR_A_RAS#, DDR_CS0_DIMMA#
RP15 56_0404_4P2R_5%: DDR_A_MA9, DDR_A_BS#2
RP6 56_0404_4P2R_5%: DDR_A_BS#0, DDR_A_MA10
RP16 56_0404_4P2R_5%: DDR_A_MA4, DDR_A_MA2
RP5 56_0404_4P2R_5%: DDR_A_CAS#, DDR_A_WE#
RP8 56_0404_4P2R_5%: DDR_A_MA0, DDR_A_BS#1
RP1 56_0404_4P2R_5%: DDR_CS1_DIMMA#, M_ODT1
RP2 56_0404_4P2R_5%: M_ODT0, DDR_A_MA13
RP23 56_0404_4P2R_5%: DDR_CKE1_DIMMA, DDR_A_MA14, DDR_A_MA11
R96 56_0402_5%

Close to VREF pins of SO-DIMM

+V_DDR_MCH_REF 7,14
C201 2.2U_0805_16V4Z
C220 0.1U_0402_16V

+1.8VO

JDIM2

	1	VREF	VSS	2	
	3	VSS	DQ4	4	DDR_A_D5
DDR_A_D4	5	DQ0	DQ5	6	DDR_A_D0
DDR_A_D1	7	DQ1	VSS	8	
	9	VSS	DM0	10	DDR_A_DM0
DDR_A_DQS#0	11	DQS0#	VSS	12	
DDR_A_DQS0	13	DQS0	DQ6	14	DDR_A_D6
	15	VSS	DQ7	16	DDR_A_D7
DDR_A_D2	17	DQ2	VSS	18	
DDR_A_D3	19	DQ3	DQ12	20	DDR_A_D13
	21	VSS	DQ13	22	DDR_A_D12
DDR_A_D8	23	DQ8	VSS	24	
DDR_A_D9	25	DQ9	DM1	26	DDR_A_DM1
	27	VSS	VSS	28	
DDR_A_DQS#1	29	DQS1#	CK0	30	M_CLK_DDR0 7
DDR_A_DQS1	31	DQS1	CK0#	32	M_CLK_DDR#0 7
	33	VSS	VSS	34	
DDR_A_D14	35	DQ10	DQ14	36	DDR_A_D11
DDR_A_D15	37	DQ11	DQ15	38	DDR_A_D10
	39	VSS	VSS	40	
	41	VSS	VSS	42	
DDR_A_D16	43	DQ16	DQ20	44	DDR_A_D20
DDR_A_D17	45	DQ17	DQ21	46	DDR_A_D21
	47	VSS	VSS	48	
DDR_A_DQS#2	49	DQS2#	NC	50	PM_EXTTS#0 7
DDR_A_DQS2	51	DQS2	DM2	52	DDR_A_DM2
	53	VSS	VSS	54	
DDR_A_D18	55	DQ18	DQ22	56	DDR_A_D23
DDR_A_D19	57	DQ19	DQ23	58	DDR_A_D22
	59	VSS	VSS	60	
DDR_A_D29	61	DQ24	DQ28	62	DDR_A_D28
DDR_A_D24	63	DQ25	DQ29	64	DDR_A_D25
DDR_A_DM3	65	VSS	VSS	66	
	67	DM3	DQS3#	68	DDR_A_DQS#3
	69	NC	DQS3	70	DDR_A_DQS3
	71	VSS	VSS	72	
DDR_A_D26	73	DQ26	DQ30	74	DDR_A_D31
DDR_A_D27	75	DQ27	DQ31	76	DDR_A_D30
	77	VSS	VSS	78	
7 DDR_CKE0_DIMMA	79	CKE0	NC/CKE1	80	DDR_CKE1_DIMMA DDR_CKE1_DIMMA 7
	81	VDD	VDD	82	
	83	NC	NC/A15	84	
8 DDR_A_BS#2	85	BA2	NC/A14	86	DDR_A_MA14 DDR_A_MA14 8
	87	VDD	VDD	88	
DDR_A_MA12	89	A12	A11	90	DDR_A_MA11
DDR_A_MA9	91	A9	A7	92	DDR_A_MA7
DDR_A_MA8	93	A8	A6	94	DDR_A_MA6
	95	VDD	VDD	96	
DDR_A_MA5	97	A5	A4	98	DDR_A_MA4
DDR_A_MA3	99	A3	A2	100	DDR_A_MA2
DDR_A_MA1	101	A1	A0	102	DDR_A_MA0
	103	VDD	VDD	104	
DDR_A_MA10	105	A10/AP	BA1	106	DDR_A_BS#1 DDR_A_BS#1 8
8 DDR_A_BS#0	107	BA0	RAS#	108	DDR_A_RAS# DDR_A_RAS# 8
8 DDR_A_WE#	109	WE#	S0#	110	DDR_CS0_DIMMA# DDR_CS0_DIMMA# 7
	111	VDD	VDD	112	
8 DDR_A_CAS#	113	CAS#	ODT0	114	M_ODT0 M_ODT0 7
7 DDR_CS1_DIMMA#	115	NC/S1#	NC/A13	116	DDR_A_MA13
	117	VDD	VDD	118	
7 M_ODT1	119	NC/ODT1	NC	120	
	121	VSS	VSS	122	
DDR_A_D37	123	DQ32	DQ36	124	DDR_A_D32
DDR_A_D36	125	DQ33	DQ37	126	DDR_A_D33
	127	VSS	VSS	128	
DDR_A_DQS#4	129	DQS4#	DM4	130	DDR_A_DM4
DDR_A_DQS4	131	DQS4	VSS	132	
	133	VSS	DQ38	134	DDR_A_D39
DDR_A_D35	135	DQ34	DQ39	136	DDR_A_D38
DDR_A_D34	137	DQ35	VSS	138	
	139	VSS	DQ44	140	DDR_A_D45
DDR_A_D40	141	DQ40	DQ45	142	DDR_A_D47
DDR_A_D44	143	DQ41	VSS	144	
	145	VSS	DQS5#	146	DDR_A_DQS#5
DDR_A_DM5	147	DM5	DQS5	148	DDR_A_DQS5
	149	VSS	VSS	150	
DDR_A_D41	151	DQ42	DQ46	152	DDR_A_D43
DDR_A_D46	153	DQ43	DQ47	154	DDR_A_D42
	155	VSS	VSS	156	
DDR_A_D49	157	DQ48	DQ52	158	DDR_A_D52
DDR_A_D48	159	DQ49	DQ53	160	DDR_A_D53
	161	VSS	VSS	162	
	163	NC,TEST	CK1	164	M_CLK_DDR1 M_CLK_DDR1 7
DDR_A_DQS#6	165	VSS	CK1#	166	M_CLK_DDR#1 M_CLK_DDR#1 7
DDR_A_DQS6	167	DQS6#	VSS	168	
	169	DQS6	DM6	170	DDR_A_DM6
DDR_A_D54	171	VSS	VSS	172	
DDR_A_D50	173	DQ50	DQ54	174	DDR_A_D51
	175	DQ51	DQ55	176	DDR_A_D55
DDR_A_D61	177	VSS	VSS	178	
DDR_A_D60	179	DQ56	DQ60	180	DDR_A_D57
	181	DQ57	DQ61	182	DDR_A_D56
DDR_A_DM7	183	VSS	VSS	184	
	185	DM7	DQS7#	186	DDR_A_DQS#7
DDR_A_D59	187	VSS	DQS7	188	DDR_A_DQS7
DDR_A_D58	189	DQ58	VSS	190	
	191	DQ59	DQ62	192	DDR_A_D62
	193	VSS	DQ63	194	DDR_A_D63
14,15,19 ICH_SM_DA	195	SDA	VSS	196	
14,15,19 ICH_SM_CLK	197	SCL	SA0	198	
+3VSO	199	VDDSPD	SA1	200	

FOX_ASOA426-M2RN-7F

C58 0.1U_0402_16V
C59 2.2U_0603_6.3V6K

SO-DIMM A REVERSE

Bottom side

R31 10K_0402_5%
R32 10K_0402_5%

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Issued Date	2007/1/15	Deciphered Date	2008/1/15

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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V

C112 2.2U_0603_6.3V6K
C139 2.2U_0603_6.3V6K
C160 2.2U_0603_6.3V6K
C138 2.2U_0603_6.3V6K
C177 2.2U_0603_6.3V6K
C109 0.1U_0402_16V
C132 0.1U_0402_16V
C133 0.1U_0402_16V
C155 0.1U_0402_16V
C189 330U 2.5V Y D2

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS

C110 0.1U_0402_16V
C134 0.1U_0402_16V
C135 0.1U_0402_16V
C156 0.1U_0402_16V
C157 0.1U_0402_16V
C170 0.1U_0402_16V
C171 0.1U_0402_16V
C111 0.1U_0402_16V
C136 0.1U_0402_16V
C158 0.1U_0402_16V
C137 0.1U_0402_16V
C172 0.1U_0402_16V
C159 0.1U_0402_16V
C199 0.1U_0402_16V

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

+0.9VS

RP18 56_0404_4P2R_5%: DDR_B_MA3, DDR_B_MA1 — DDR_B_MA12, DDR_B_MA9
RP10 56_0404_4P2R_5%: DDR_B_BS#0, DDR_B_MA10 — DDR_B_MA14, DDR_B_MA11
RP12 56_0404_4P2R_5%: DDR_B_MA0, DDR_B_BS#1 — DDR_B_MA5, DDR_B_MA8
RP11 56_0404_4P2R_5%: DDR_B_RAS#, DDR_CS2_DIMMB# — DDR_B_MA7, DDR_B_MA6
RP9 56_0404_4P2R_5%: DDR_B_CAS#, DDR_B_WE# — DDR_B_MA4, DDR_B_MA2
RP3 56_0404_4P2R_5%: DDR_CS3_DIMMB#, M_ODT3 — DDR_B_MA13, M_ODT2
RP25 56_0404_4P2R_5%: DDR_CKE3_DIMMB — DDR_B_BS#2, DDR_CKE2_DIMMB
R335 56_0402_5%: DDR_CKE3_DIMMB

RP24 56_0404_4P2R_5%: DDR_B_MA12, DDR_B_MA9
RP26 56_0404_4P2R_5%: DDR_B_MA14, DDR_B_MA11
RP19 56_0404_4P2R_5%: DDR_B_MA5, DDR_B_MA8
RP21 56_0404_4P2R_5%: DDR_B_MA7, DDR_B_MA6
RP20 56_0404_4P2R_5%: DDR_B_MA4, DDR_B_MA2
RP4 56_0404_4P2R_5%: DDR_B_MA13, M_ODT2

Close to VREF pins of SO-DIMM

+V_DDR_MCH_REF 7,13
C221 2.2U_0805_16V4Z
C222 0.1U_0402_16V

+1.8V
+3VSO
13,15,19 ICH_SM_DA
13,15,19 ICH_SM_CLK
C61 0.1U_0402_16V
C60 2.2U_0603_6.3V6K
R33 10K_0402_5%
R34 10K_0402_5%
+3VS

JDIM1 — FOX_AS0A426-NARN-7F-N

	VREF	1	2	VSS	
	VSS	3	4	DQ4	DDR_B_D5
DDR_B_D0	DQ0	5	6	DQ5	DDR_B_D4
DDR_B_D1	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_B_DM0
DDR_B_DQS#0	DQS0#	11	12	VSS	
DDR_B_DQS0	DQS0	13	14	DQ6	DDR_B_D6
	VSS	15	16	DQ7	DDR_B_D7
DDR_B_D2	DQ2	17	18	VSS	
DDR_B_D3	DQ3	19	20	DQ12	DDR_B_D12
	VSS	21	22	DQ13	DDR_B_D13
DDR_B_D8	DQ8	23	24	VSS	
DDR_B_D9	DQ9	25	26	DM1	DDR_B_DM1
	VSS	27	28	VSS	
DDR_B_DQS#1	DQS1#	29	30	CK0	M_CLK_DDR2 — M_CLK_DDR2 7
DDR_B_DQS1	DQS1	31	32	CK0#	M_CLK_DDR#2 — M_CLK_DDR#2 7
	VSS	33	34	VSS	
DDR_B_D10	DQ10	35	36	DQ14	DDR_B_D14
DDR_B_D11	DQ11	37	38	DQ15	DDR_B_D15
	VSS	39	40	VSS	
		41	42	VSS	
DDR_B_D17	DQ16	43	44	DQ20	DDR_B_D21
DDR_B_D20	DQ17	45	46	DQ21	DDR_B_D16
	VSS	47	48	VSS	
DDR_B_DQS#2	DQS2#	49	50	NC	PM_EXTTS#1 7
DDR_B_DQS2	DQS2	51	52	DM2	DDR_B_DM2
	VSS	53	54	VSS	
DDR_B_D18	DQ18	55	56	DQ22	DDR_B_D22
DDR_B_D19	DQ19	57	58	DQ23	DDR_B_D23
	VSS	59	60	VSS	
DDR_B_D28	DQ24	61	62	DQ28	DDR_B_D29
DDR_B_D25	DQ25	63	64	DQ29	DDR_B_D24
	VSS	65	66	VSS	
DDR_B_DM3	DM3	67	68	DQS3#	DDR_B_DQS#3
	NC	69	70	DQS3	DDR_B_DQS3
	VSS	71	72	VSS	
DDR_B_D30	DQ26	73	74	DQ30	DDR_B_D26
DDR_B_D31	DQ27	75	76	DQ31	DDR_B_D27
	VSS	77	78	VSS	
7 DDR_CKE2_DIMMB — DDR_CKE2_DIMMB	CKE0	79	80	NC/CKE1	DDR_CKE3_DIMMB — DDR_CKE3_DIMMB 7
	VDD	81	82	VDD	
	NC	83	84	NC/A15	
8 DDR_B_BS#2 — DDR_B_BS#2	BA2	85	86	NC/A14	DDR_B_MA14 — DDR_B_MA14 8
	VDD	87	88	VDD	
DDR_B_MA12	A12	89	90	A11	DDR_B_MA11
DDR_B_MA9	A9	91	92	A7	DDR_B_MA7
DDR_B_MA8	A8	93	94	A6	DDR_B_MA6
	VDD	95	96	VDD	
DDR_B_MA5	A5	97	98	A4	DDR_B_MA4
DDR_B_MA3	A3	99	100	A2	DDR_B_MA2
DDR_B_MA1	A1	101	102	A0	DDR_B_MA0
	VDD	103	104	VDD	
DDR_B_MA10	A10/AP	105	106	BA1	DDR_B_BS#1 — DDR_B_BS#1 8
8 DDR_B_BS#0 — DDR_B_BS#0	BA0	107	108	RAS#	DDR_B_RAS# — DDR_B_RAS# 8
8 DDR_B_WE# — DDR_B_WE#	WE#	109	110	S0#	DDR_CS2_DIMMB# — DDR_CS2_DIMMB# 7
	VDD	111	112	VDD	
8 DDR_B_CAS# — DDR_B_CAS#	CAS#	113	114	ODT0	M_ODT2 — M_ODT2 7
7 DDR_CS3_DIMMB# — DDR_CS3_DIMMB#	NC/S1#	115	116	NC/A13	DDR_B_MA13
	VDD	117	118	VDD	
7 M_ODT3 — M_ODT3	NC/ODT1	119	120	NC	
	VSS	121	122	VSS	
DDR_B_D32	DQ32	123	124	DQ36	DDR_B_D36
DDR_B_D33	DQ33	125	126	DQ37	DDR_B_D37
	VSS	127	128	VSS	
DDR_B_DQS#4	DQS4#	129	130	DM4	DDR_B_DM4
DDR_B_DQS4	DQS4	131	132	VSS	
	VSS	133	134	DQ38	DDR_B_D39
DDR_B_D34	DQ34	135	136	DQ39	DDR_B_D38
DDR_B_D35	DQ35	137	138	VSS	
	VSS	139	140	DQ44	DDR_B_D44
DDR_B_D40	DQ40	141	142	DQ45	DDR_B_D45
DDR_B_D41	DQ41	143	144	VSS	
	VSS	145	146	DQS5#	DDR_B_DQS#5
DDR_B_DM5	DM5	147	148	DQS5	DDR_B_DQS5
	VSS	149	150	VSS	
DDR_B_D42	DQ42	151	152	DQ46	DDR_B_D46
DDR_B_D43	DQ43	153	154	DQ47	DDR_B_D47
	VSS	155	156	VSS	
DDR_B_D48	DQ48	157	158	DQ52	DDR_B_D52
DDR_B_D49	DQ49	159	160	DQ53	DDR_B_D53
	VSS	161	162	VSS	
	NC,TEST	163	164	CK1	M_CLK_DDR3 — M_CLK_DDR3 7
	VSS	165	166	CK1#	M_CLK_DDR#3 — M_CLK_DDR#3 7
DDR_B_DQS#6	DQS6#	167	168	VSS	
DDR_B_DQS6	DQS6	169	170	DM6	DDR_B_DM6
	VSS	171	172	VSS	
DDR_B_D51	DQ50	173	174	DQ54	DDR_B_D54
DDR_B_D50	DQ51	175	176	DQ55	DDR_B_D55
	VSS	177	178	VSS	
DDR_B_D56	DQ56	179	180	DQ60	DDR_B_D60
DDR_B_D61	DQ57	181	182	DQ61	DDR_B_D57
	VSS	183	184	VSS	
DDR_B_DM7	DM7	185	186	DQS7#	DDR_B_DQS#7
	VSS	187	188	DQS7	DDR_B_DQS7
DDR_B_D59	DQ58	189	190	VSS	
DDR_B_D58	DQ59	191	192	DQ62	DDR_B_D62
	VSS	193	194	DQ63	DDR_B_D63
13,15,19 ICH_SM_DA — ICH_SM_DA	SDA	195	196	VSS	
13,15,19 ICH_SM_CLK — ICH_SM_CLK	SCL	197	198	SAO	
	VDDSPD	199	200	SA1	

SO-DIMM B
REVERSE
Bottom side

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	*
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

Routing the trace at least 10mil

0905 Connect to +VCCP

Place close to U55

ITP_EN	* 0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed

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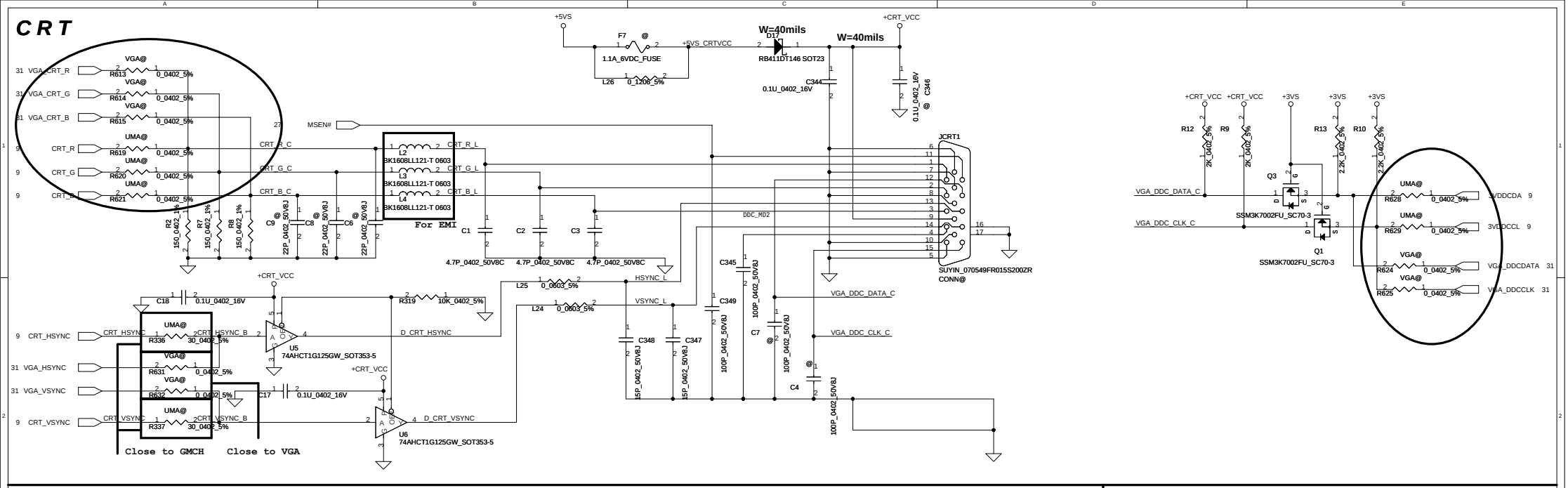
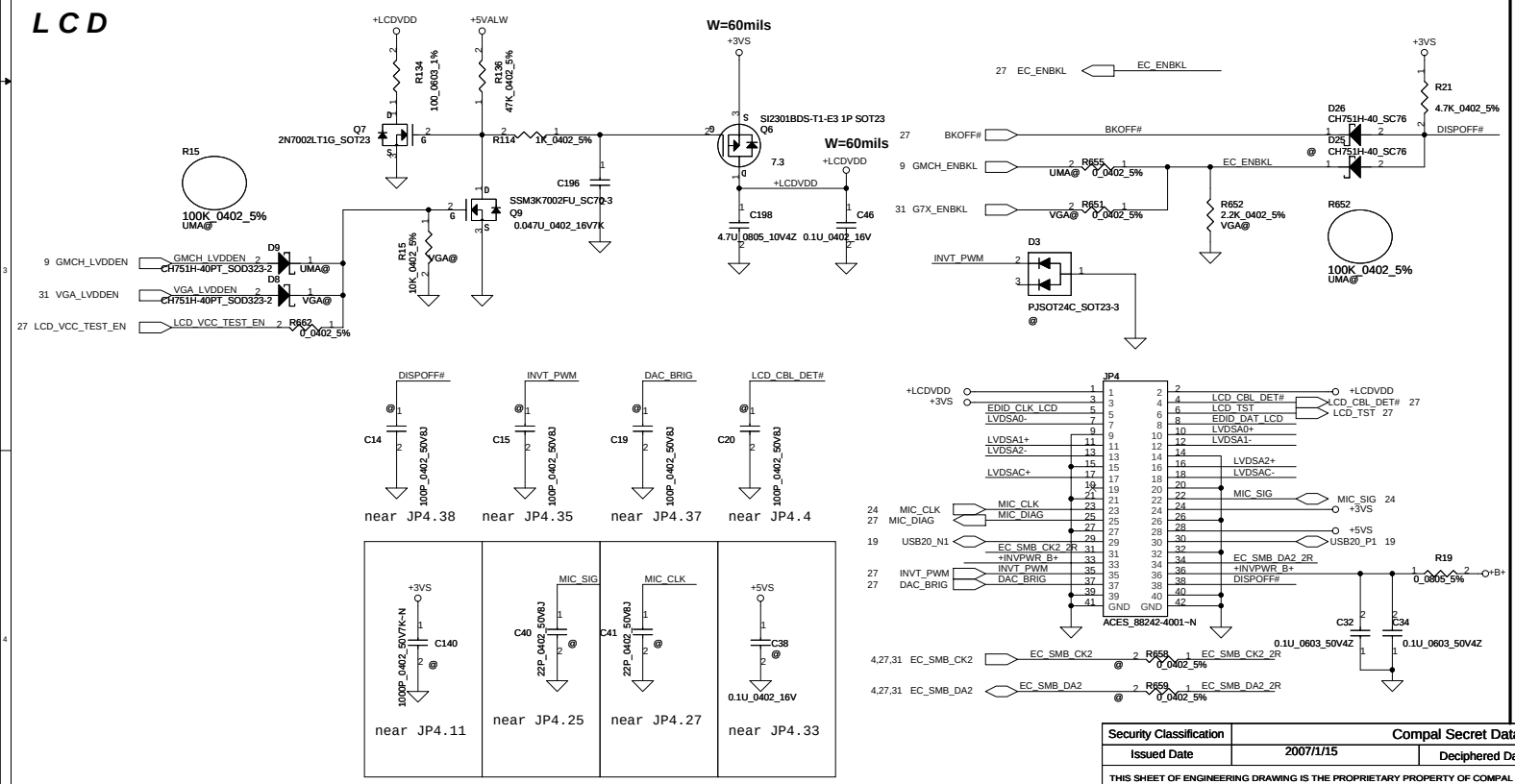
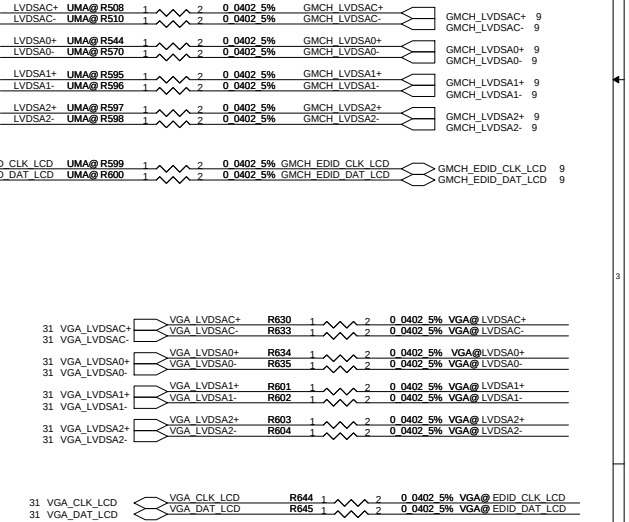
CRT



LCD





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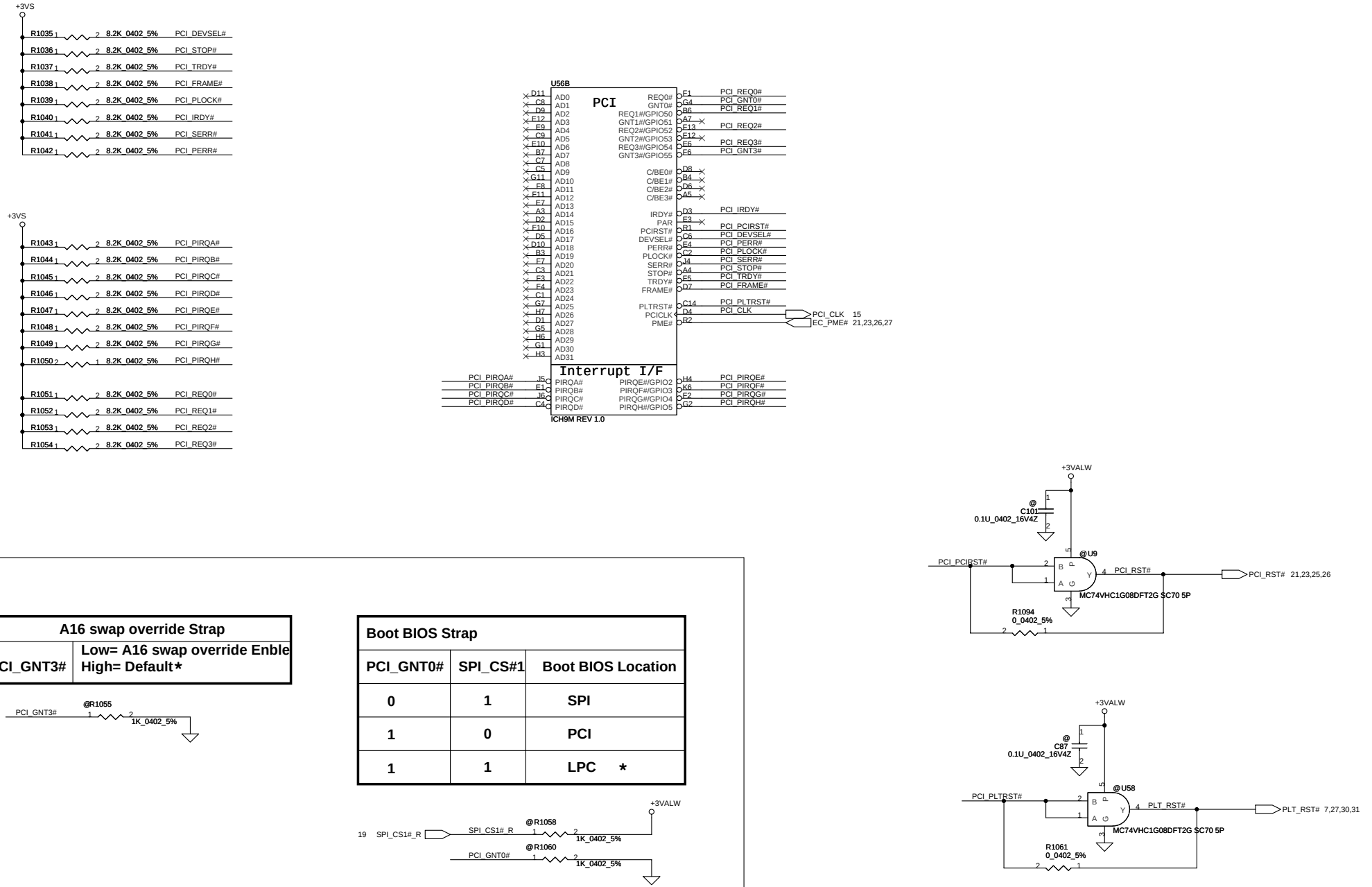

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

PCI_GNT3# @R1055 1K_0402_5%

Boot BIOS Strap		
PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

19 SPI_CS1#_R @R1058 1K_0402_5%
PCI_GNT0# @R1060 1K_0402_5%
+3VALW

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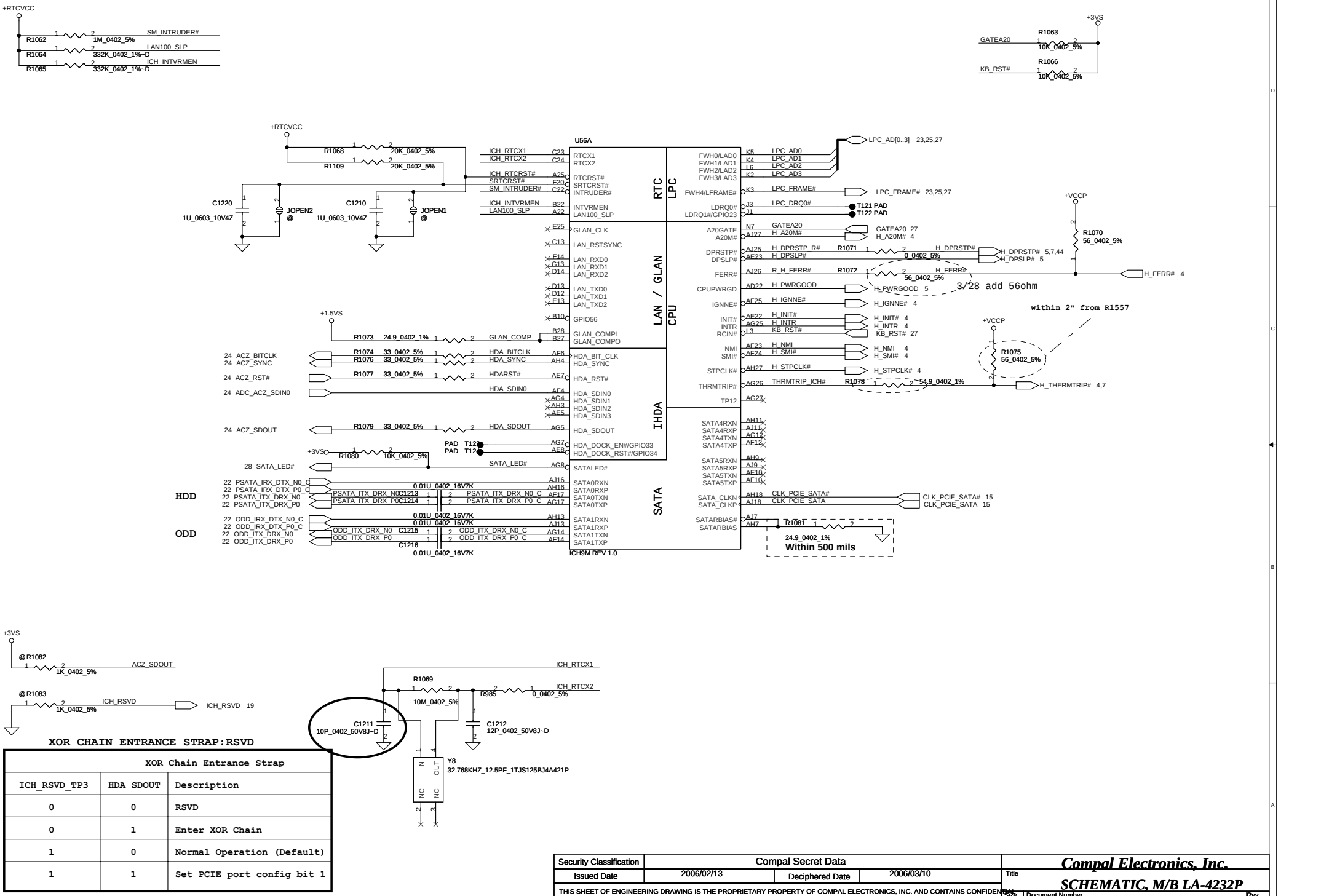

XOR CHAIN ENTRANCE STRAP:RSVD

XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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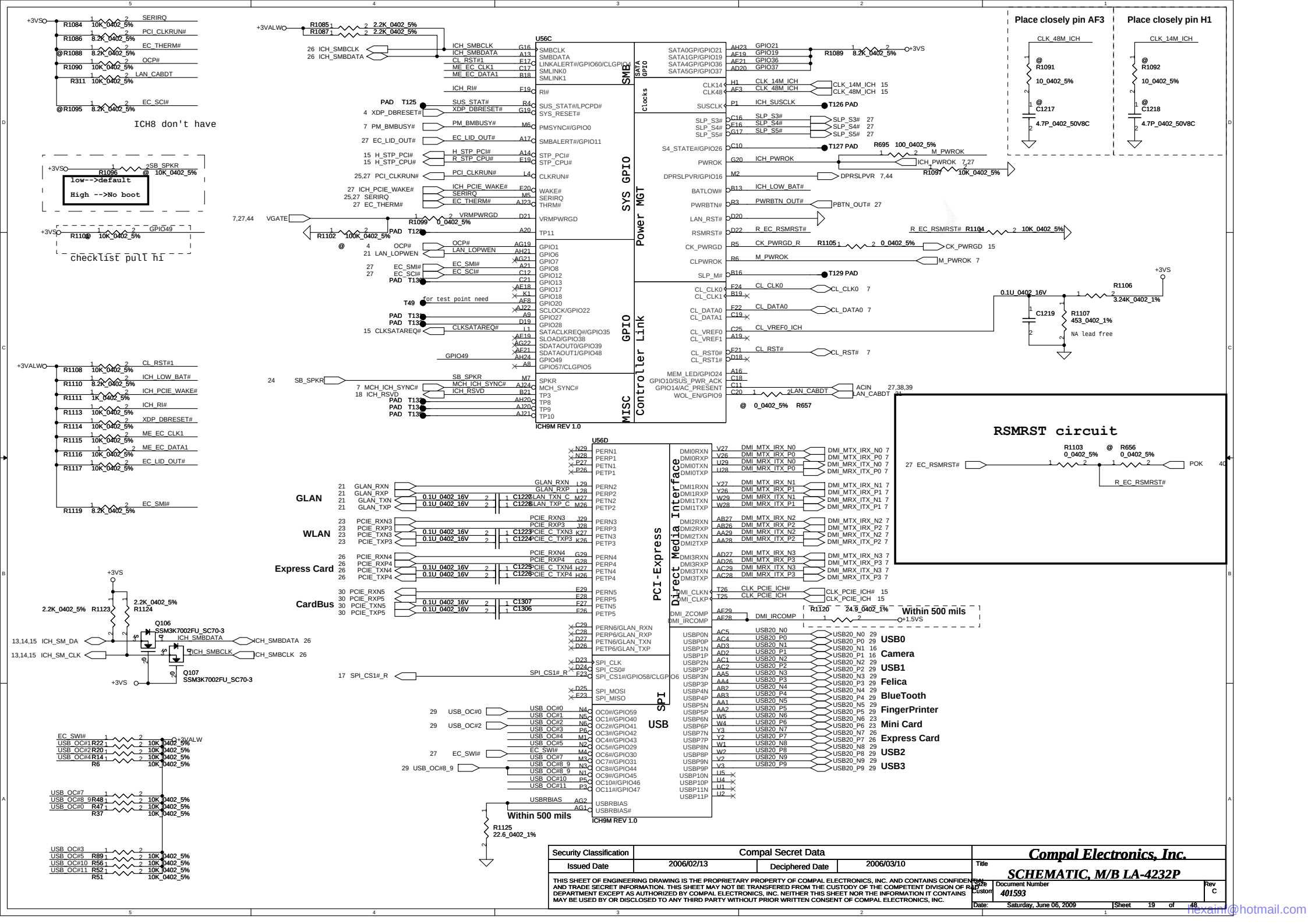

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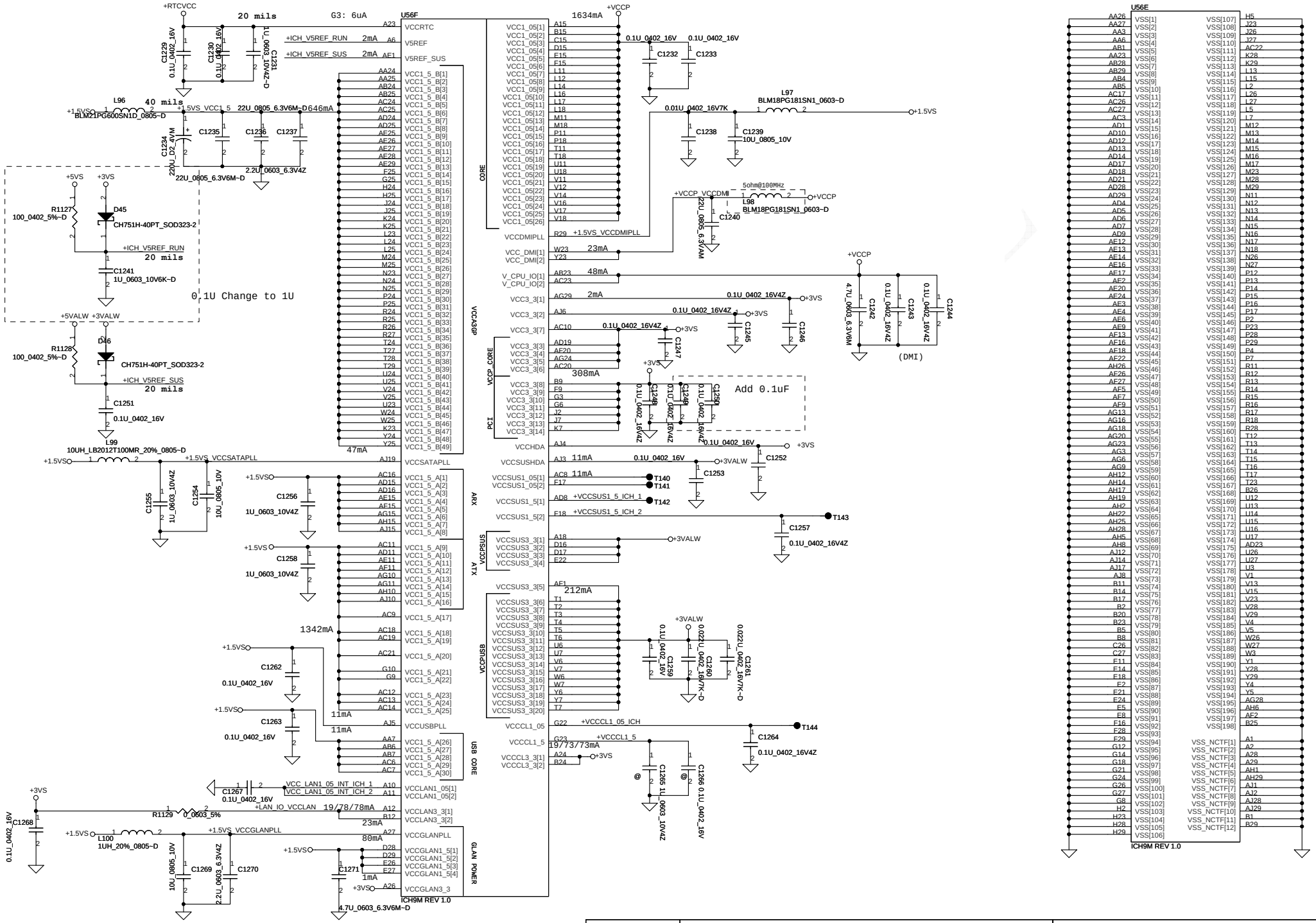

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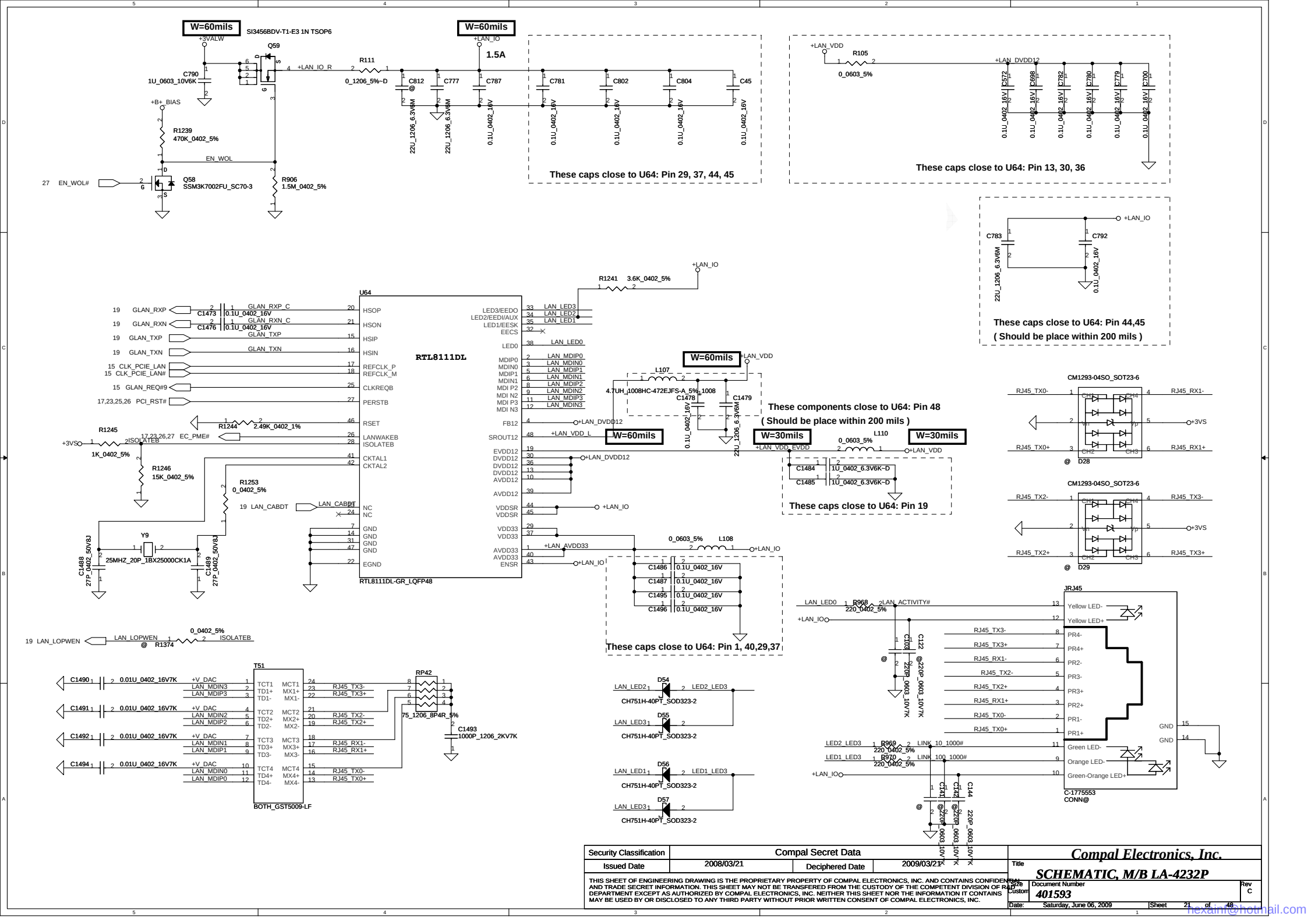

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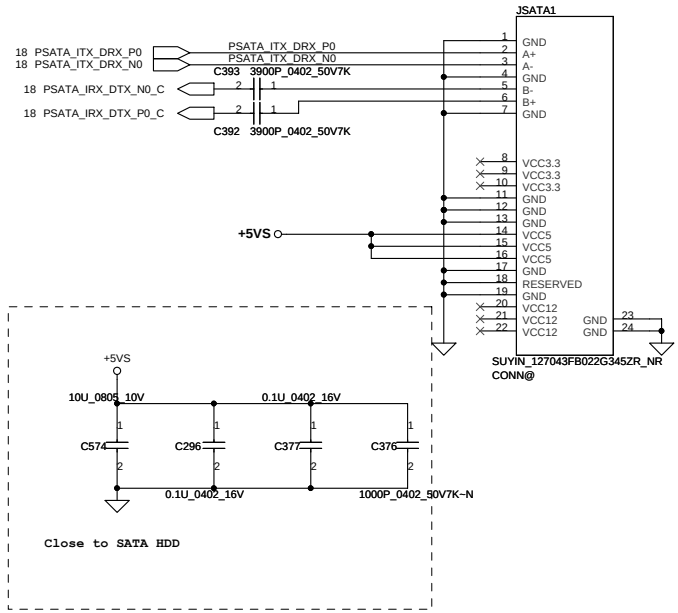
SATA HDD CONN



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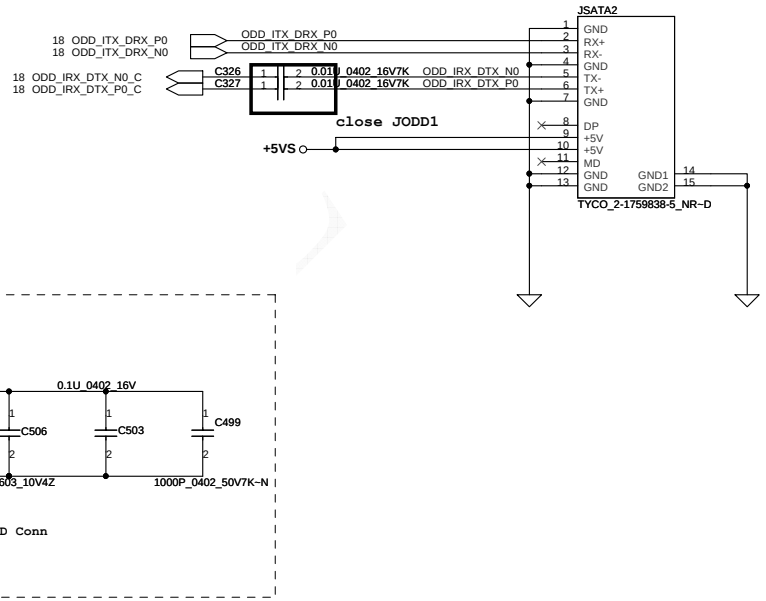

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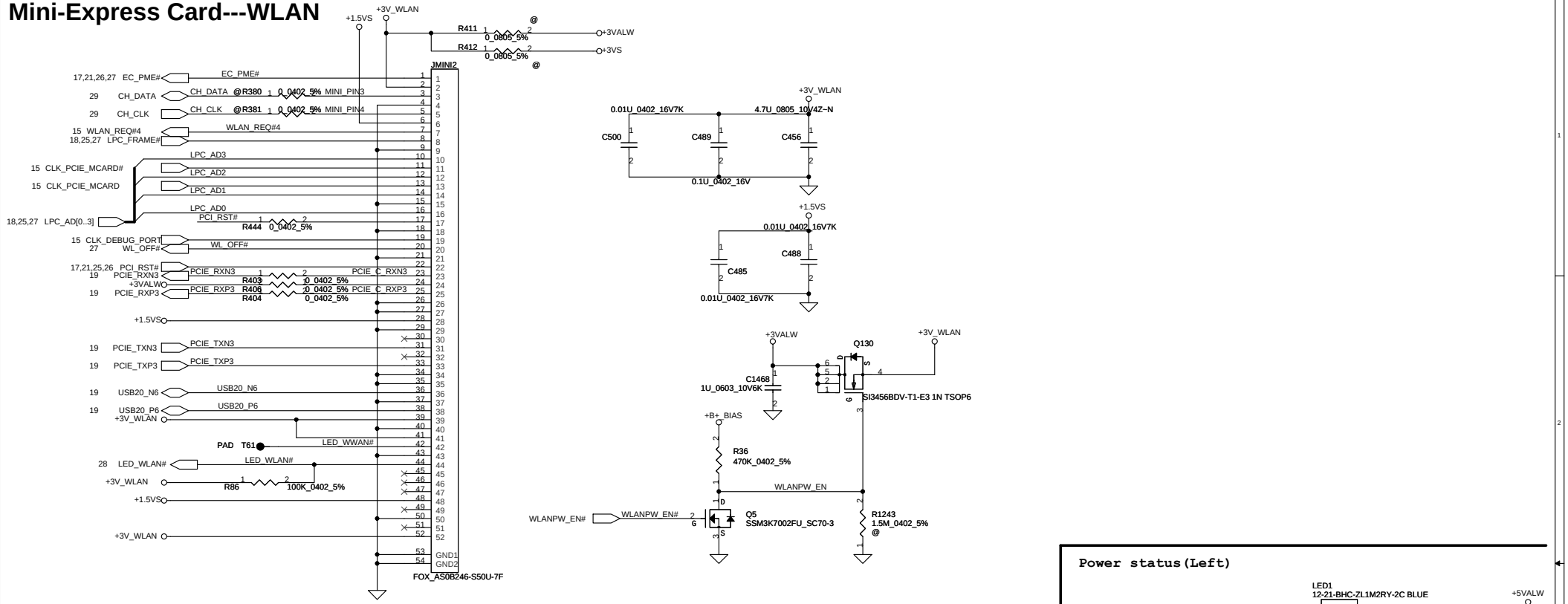
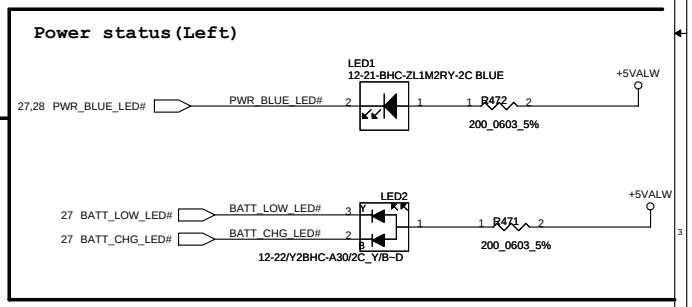
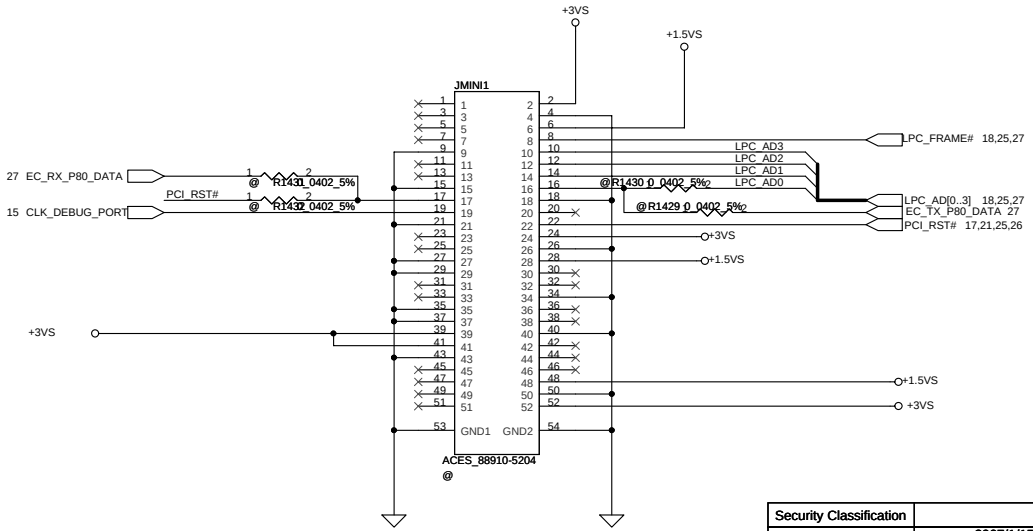
Mini-Express Card---WLAN







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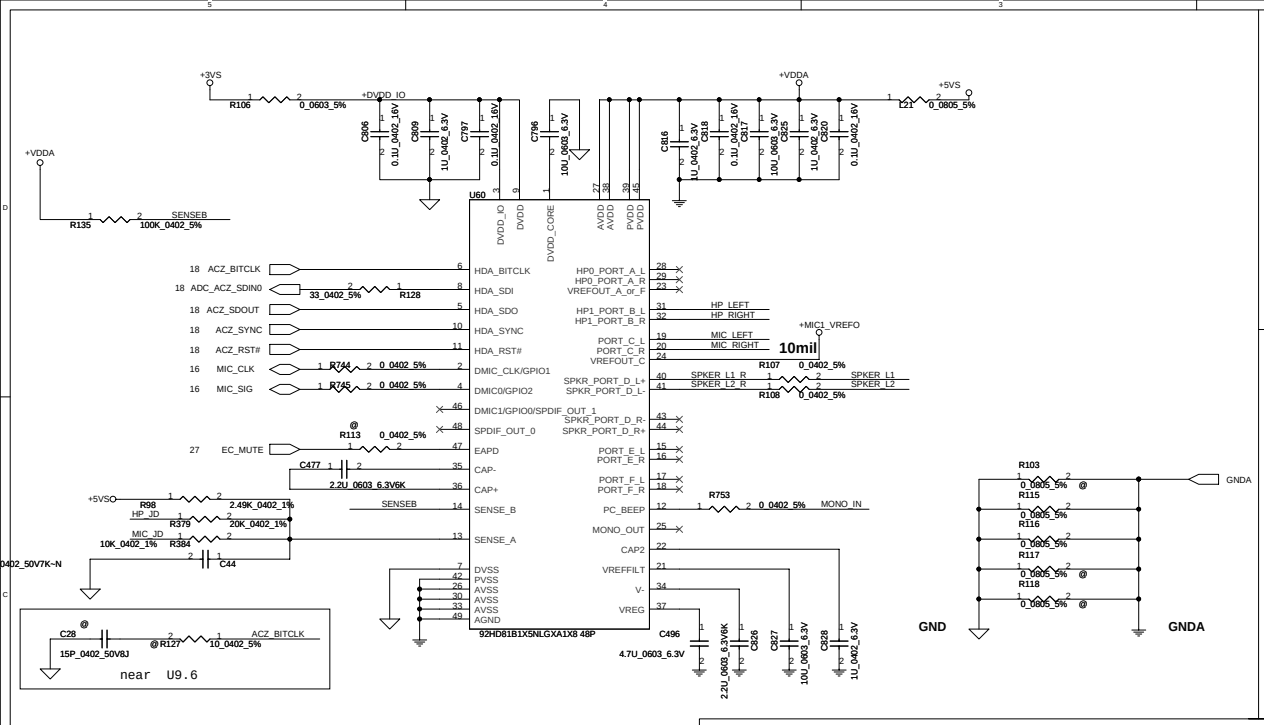

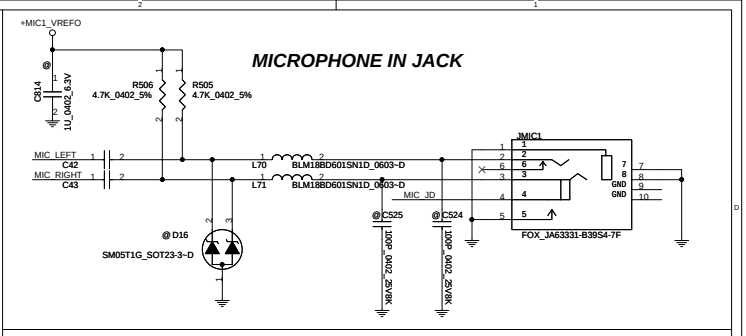

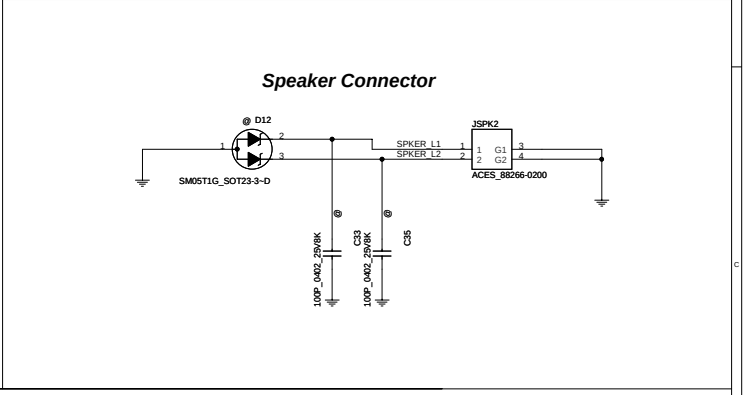

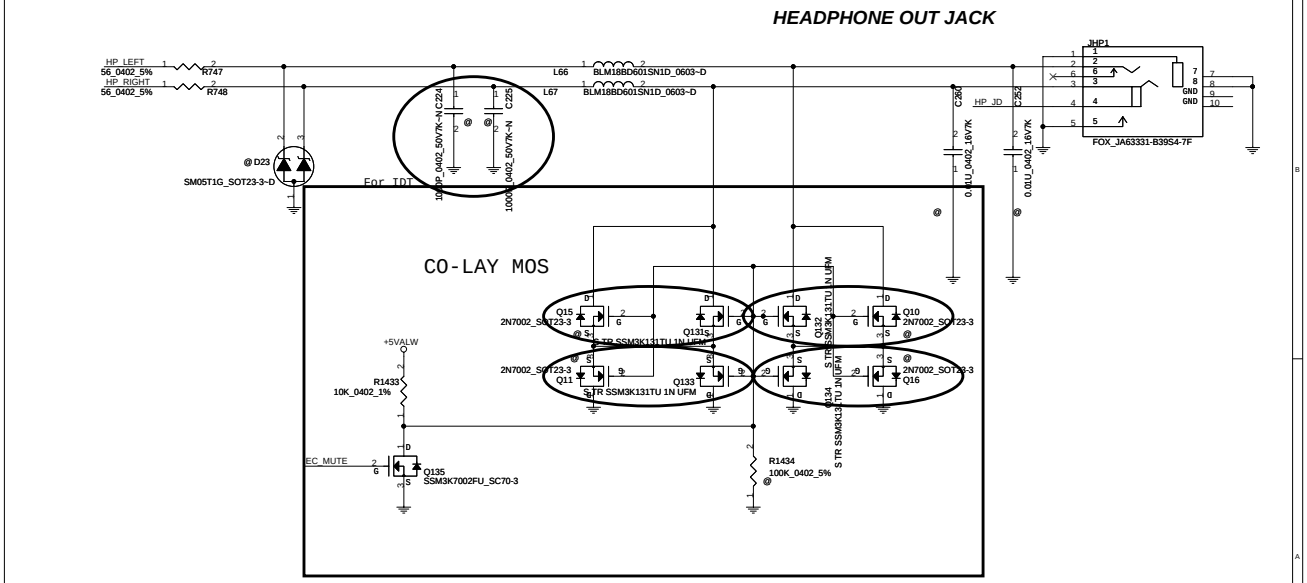

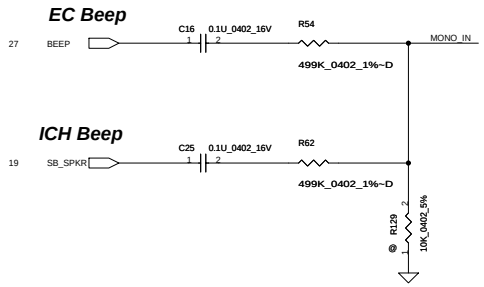

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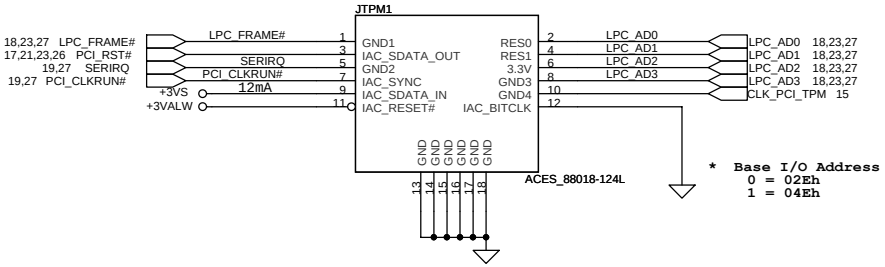
TPM 1.2



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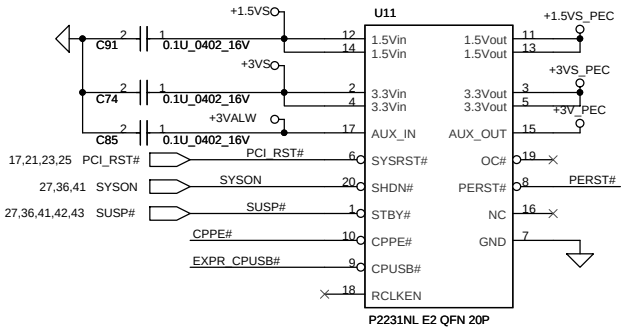
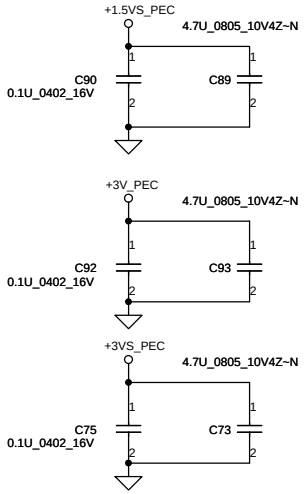
Express card

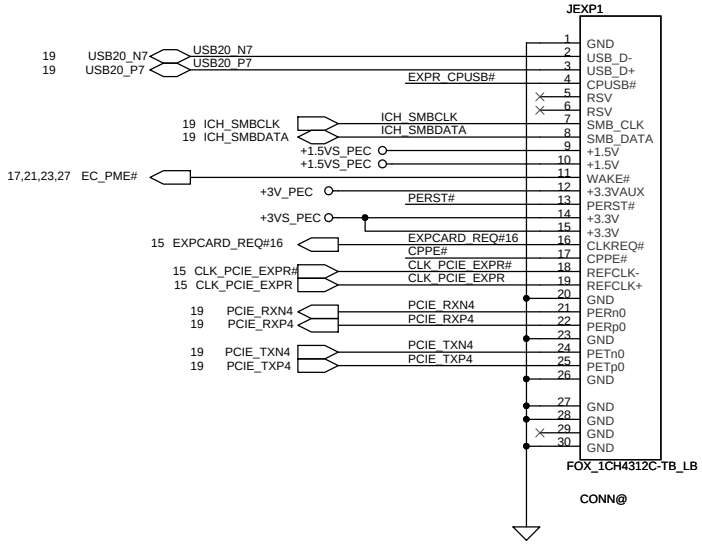
Express Card Power Switch



+1.5V_CARD Max. 650mA, Average 500mA

+3V_CARD Max. 1300mA, Average 1000mA





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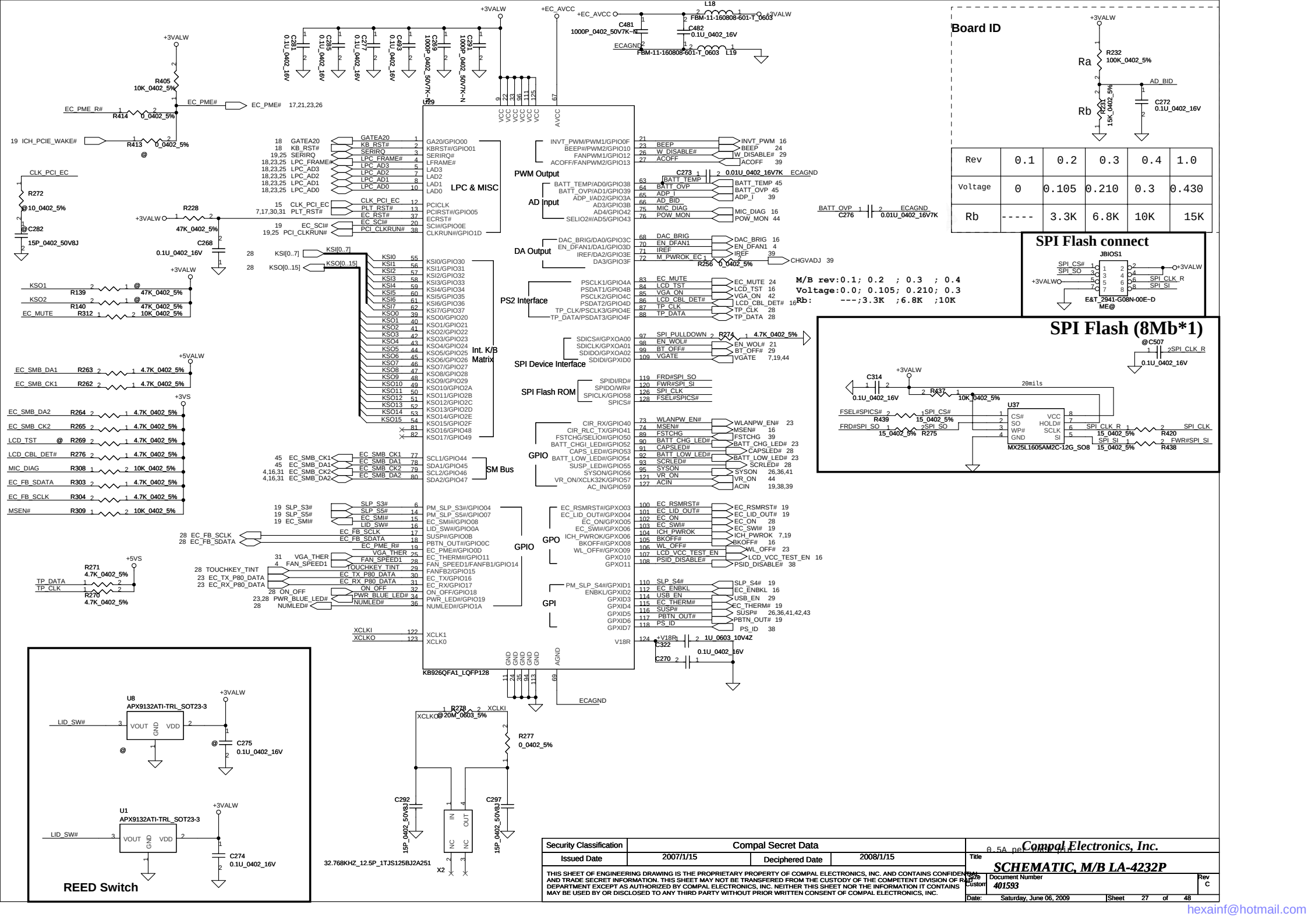
Board ID
Ra
R232 100K_0402_5%
AD_BID
Rb
R231 15K_0402_5%
C272 0.1U_0402_16V
Rev | 0.1 | 0.2 | 0.3 | 0.4 | 1.0
Voltage | 0 | 0.105 | 0.210 | 0.3 | 0.430
Rb | ----- | 3.3K | 6.8K | 10K | 15K
SPI Flash connect
JBIOS1
SPI_CS#
SPI_SO
SPI_CLK_R
SPI_SI
+3VALW
E&T_2941-G08N-00E-D
ME@
SPI Flash (8Mb*1)
U37
MX25L1605AM2C-12G_SO8
M/B rev:0.1; 0.2 ; 0.3 ; 0.4
Voltage:0.0; 0.105; 0.210; 0.3
Rb: ---;3.3K ;6.8K ;10K
KB926QFA1_LQFP128
REED Switch
U8
U1
APX9132ATI-TRL_SOT23-3
32.768KHZ_12.5P_1TJS125BJ2A251
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Compal Secret Data
Issued Date
2007/1/15
Deciphered Date
2008/1/15
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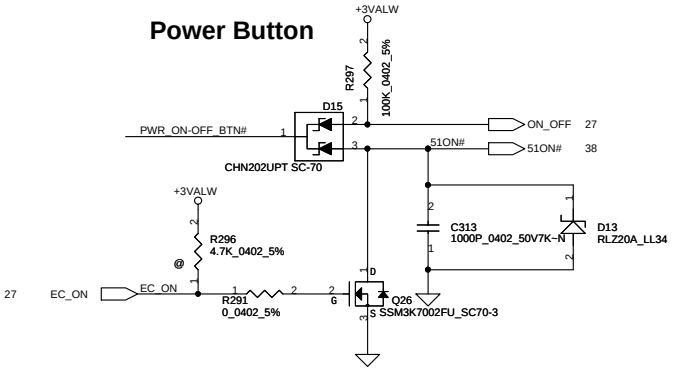
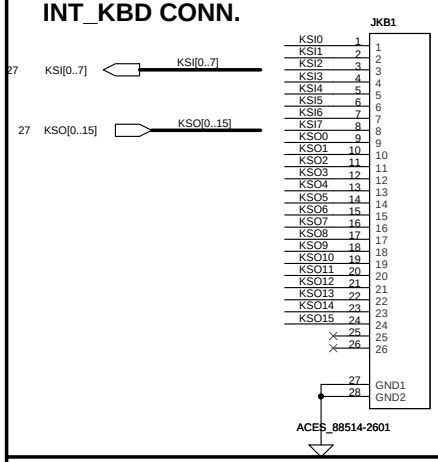
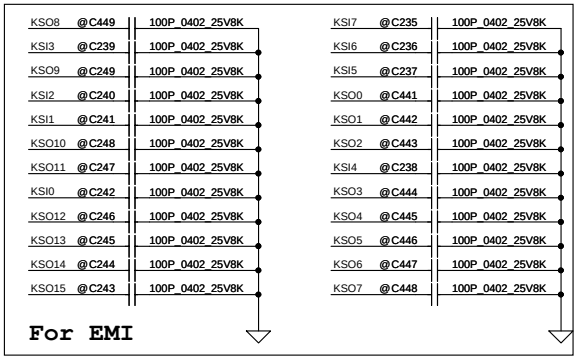
hexainf@hotmail.com

Power Button

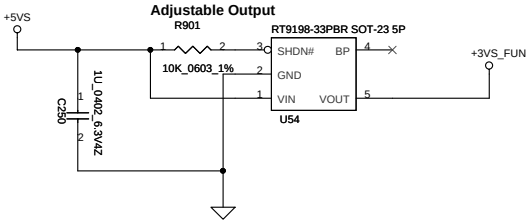


INT_KBD CONN.

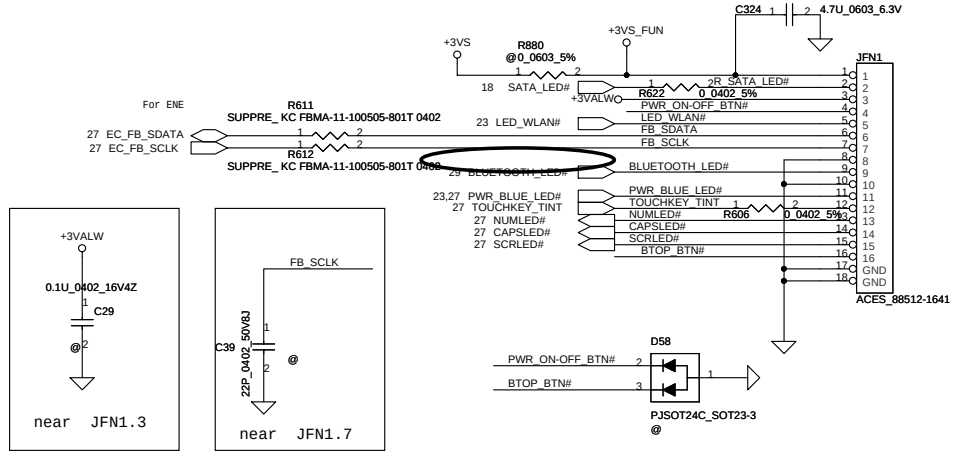




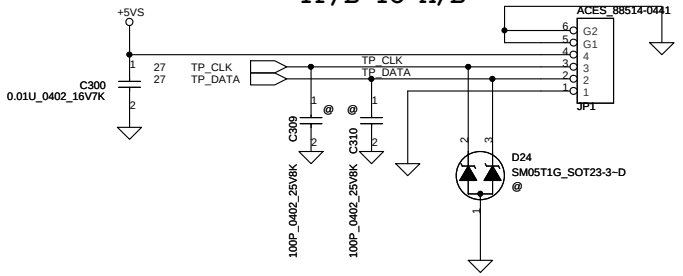
Regulator for ENE sensor



Function/B CONN.



Touch PAD/B CONN.



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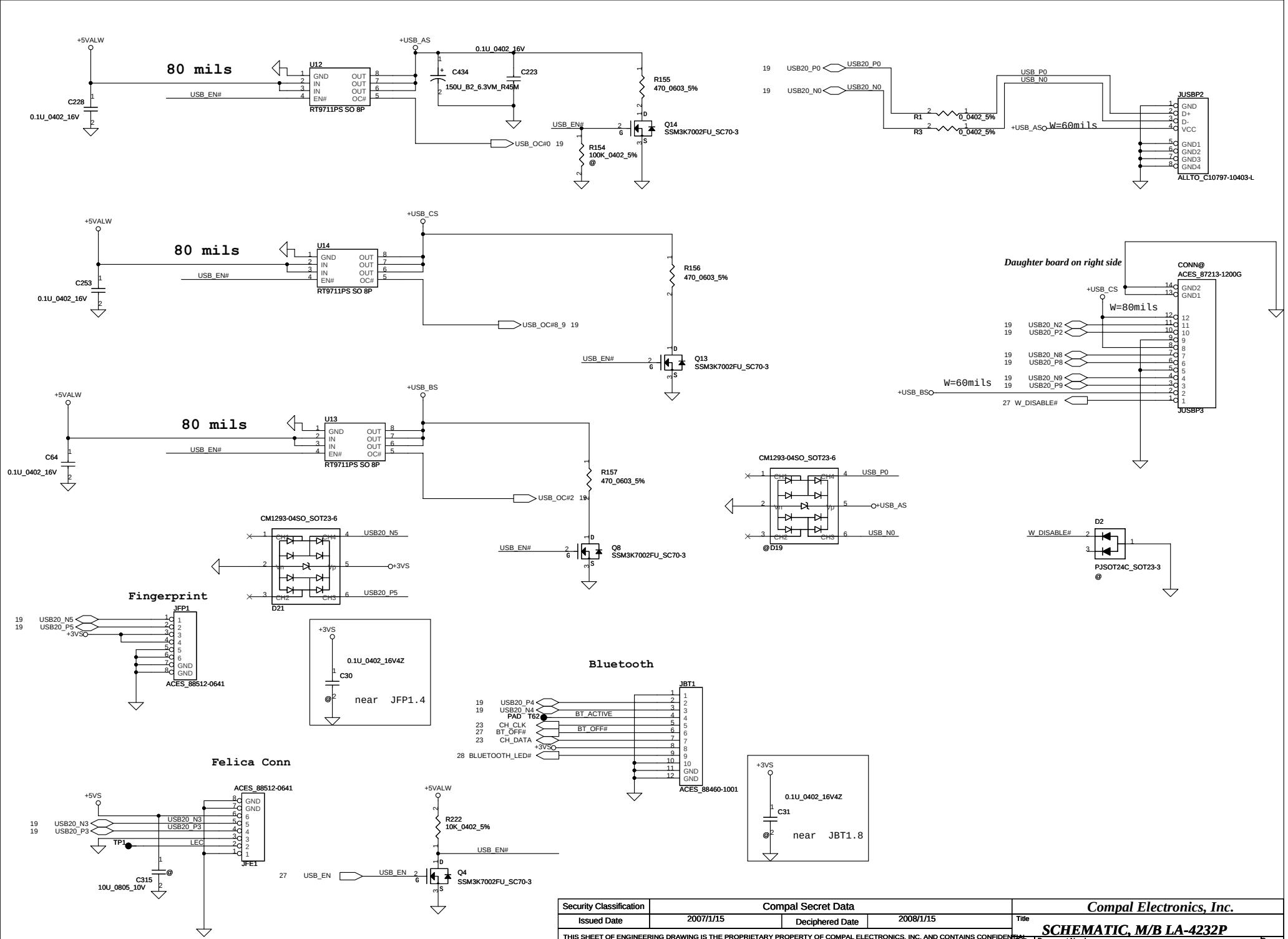

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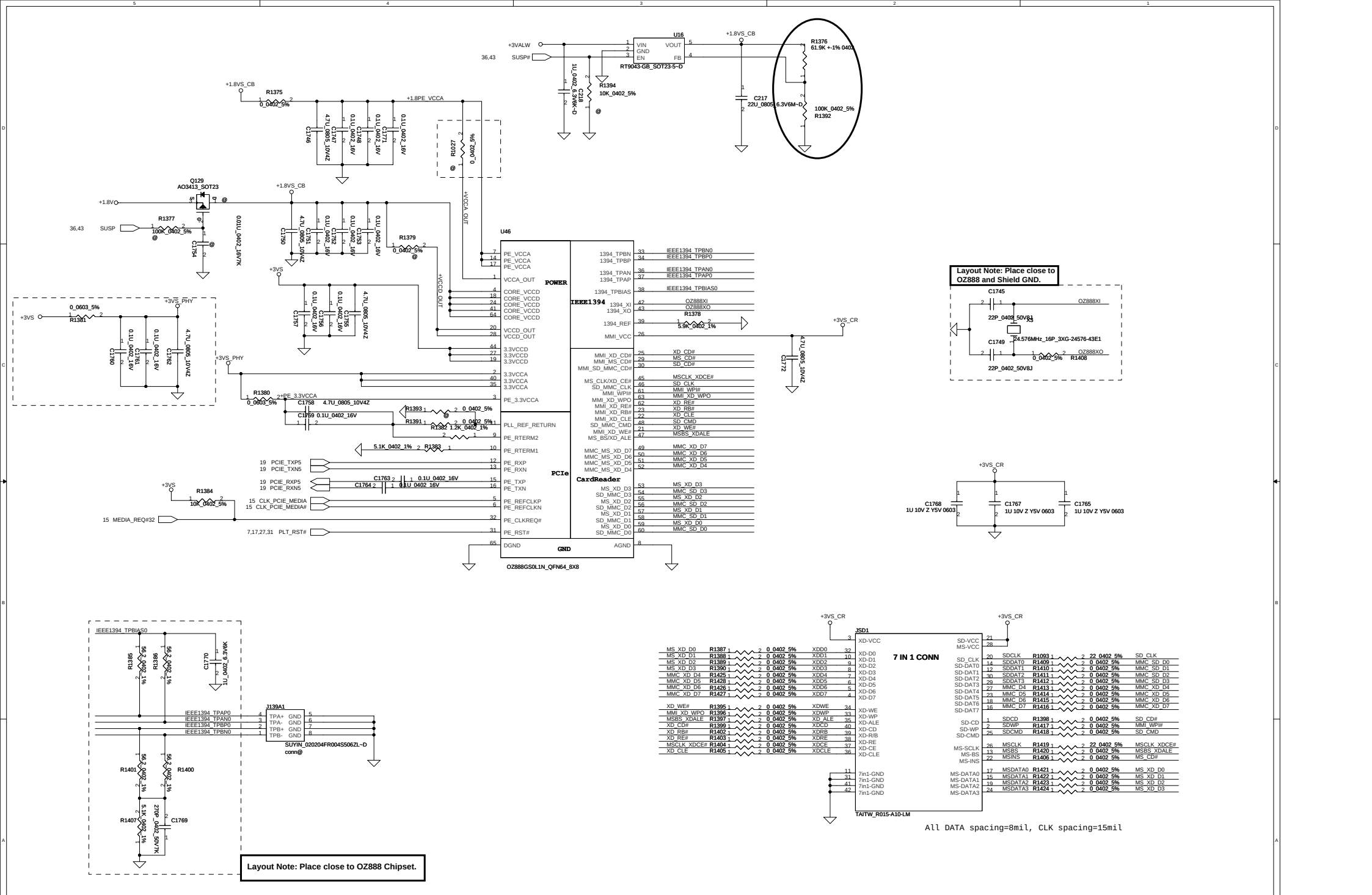

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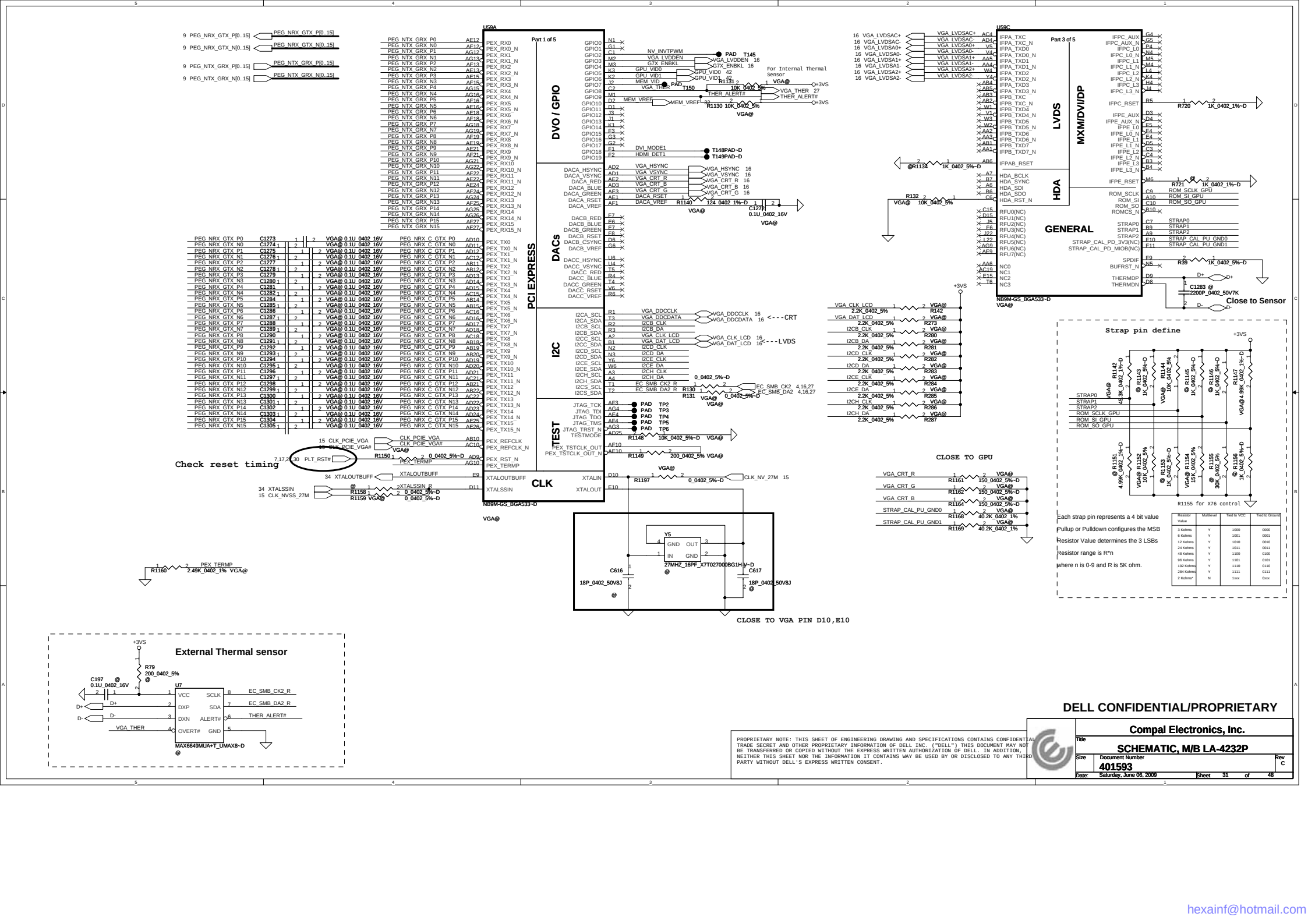

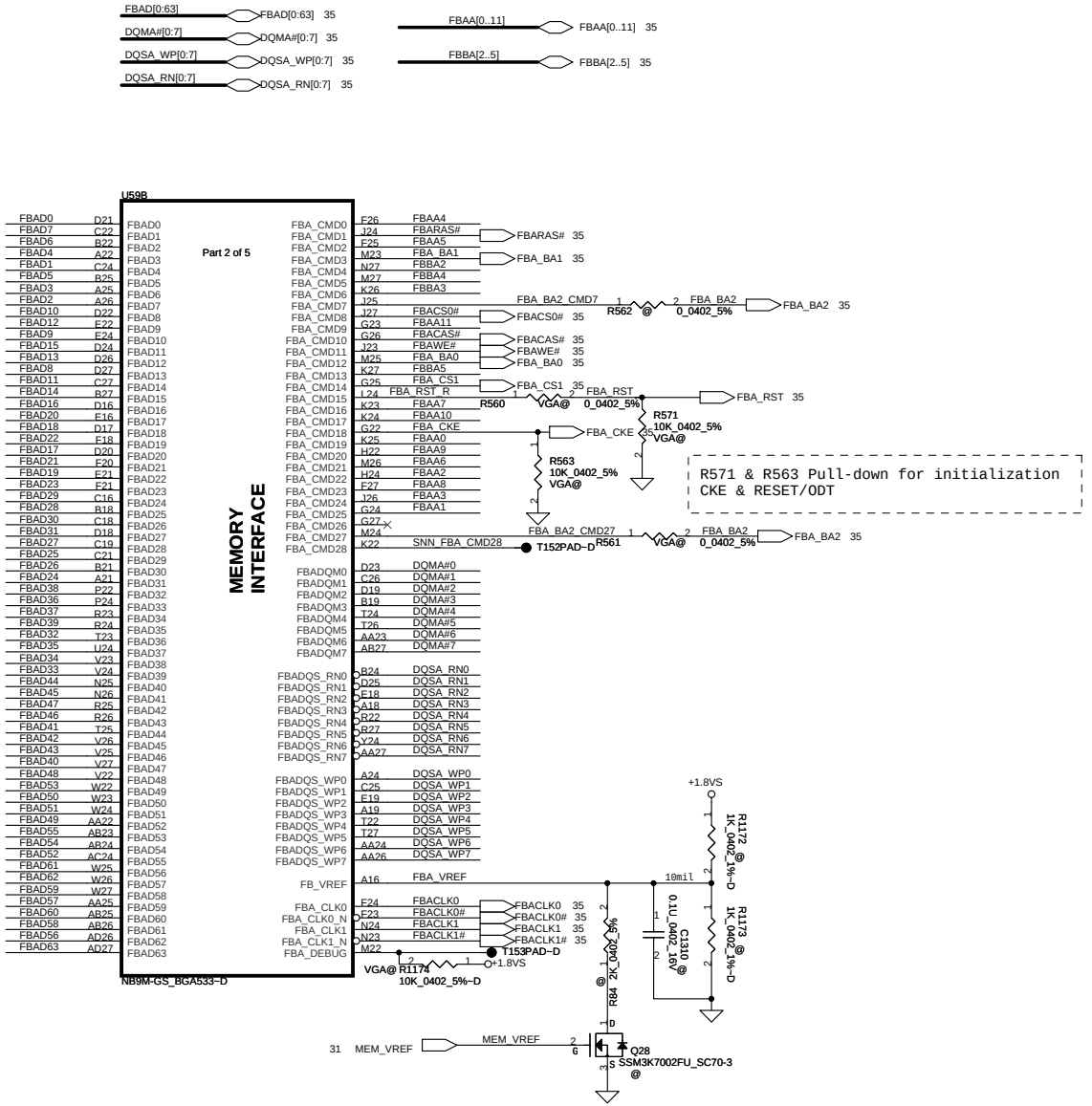

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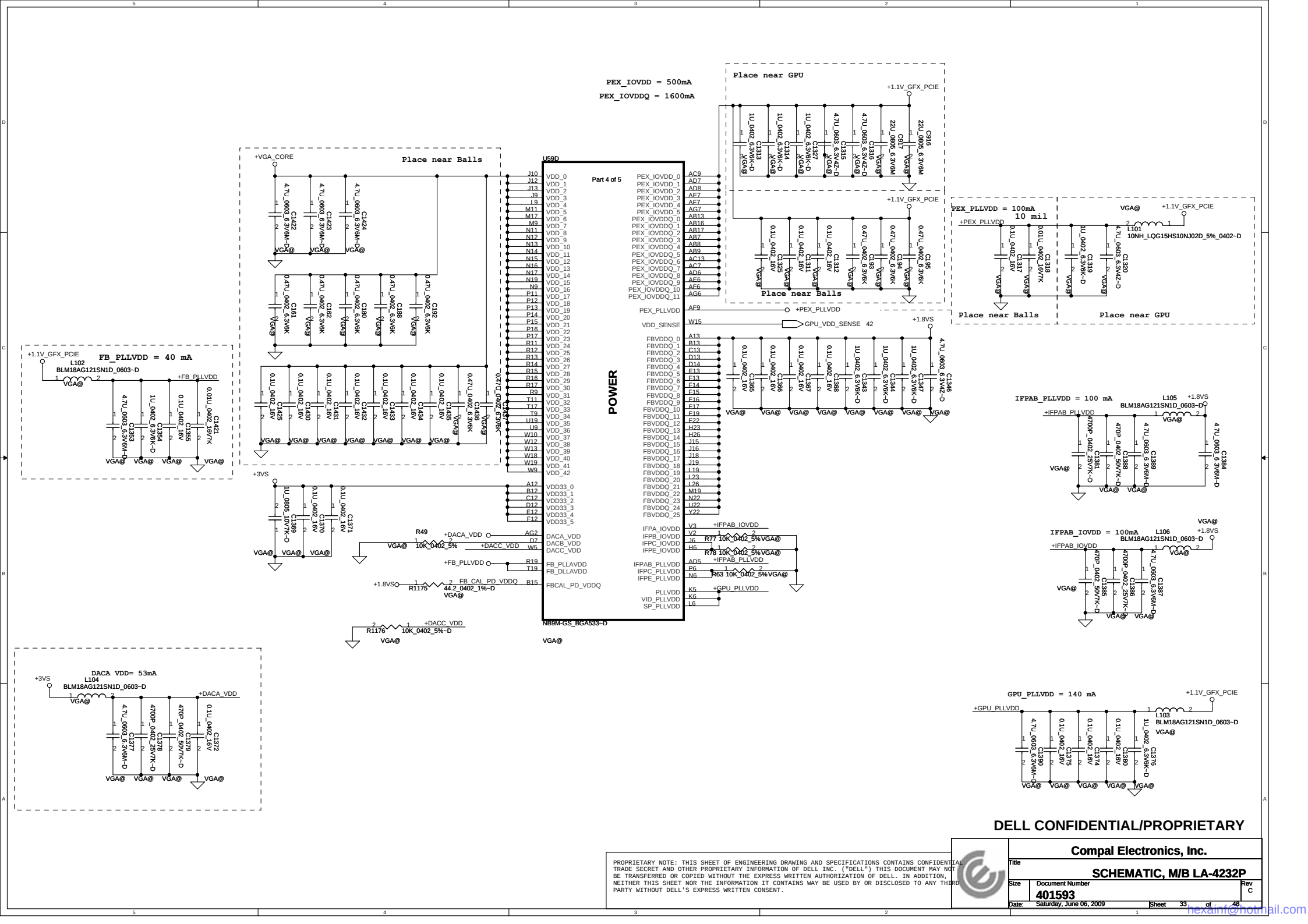

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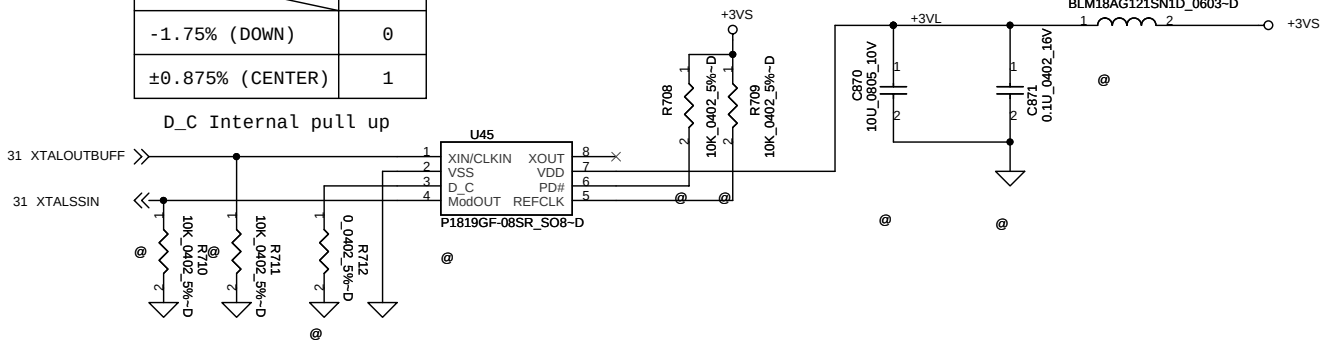
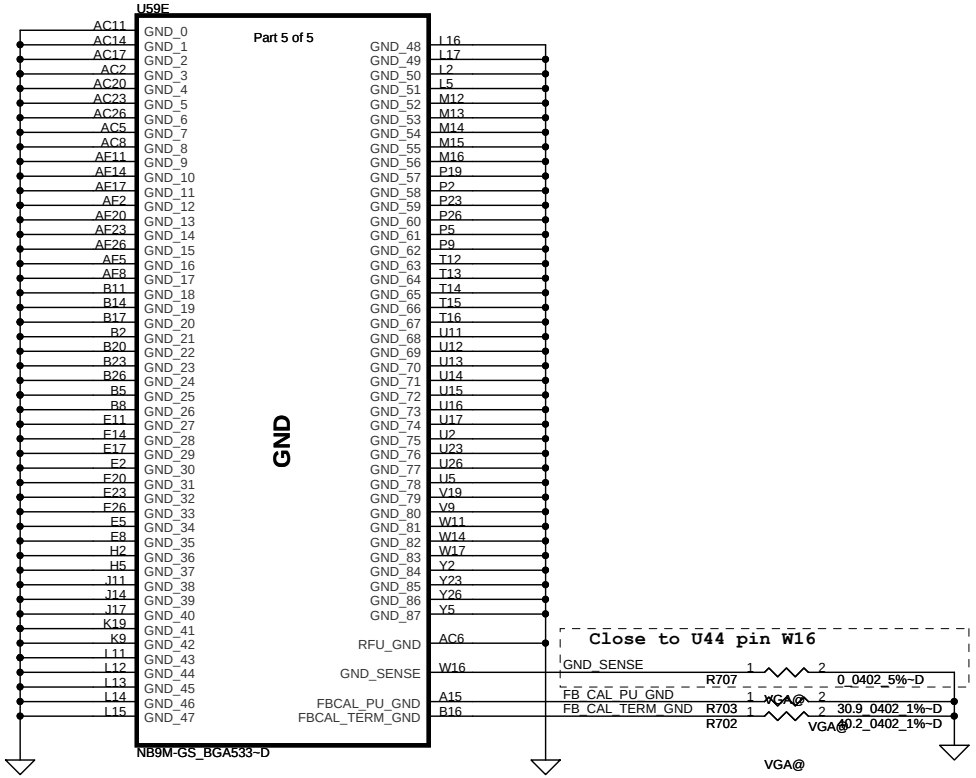
	D_C
-1.75% (DOWN)	0
±0.875% (CENTER)	1

D_C Internal pull up





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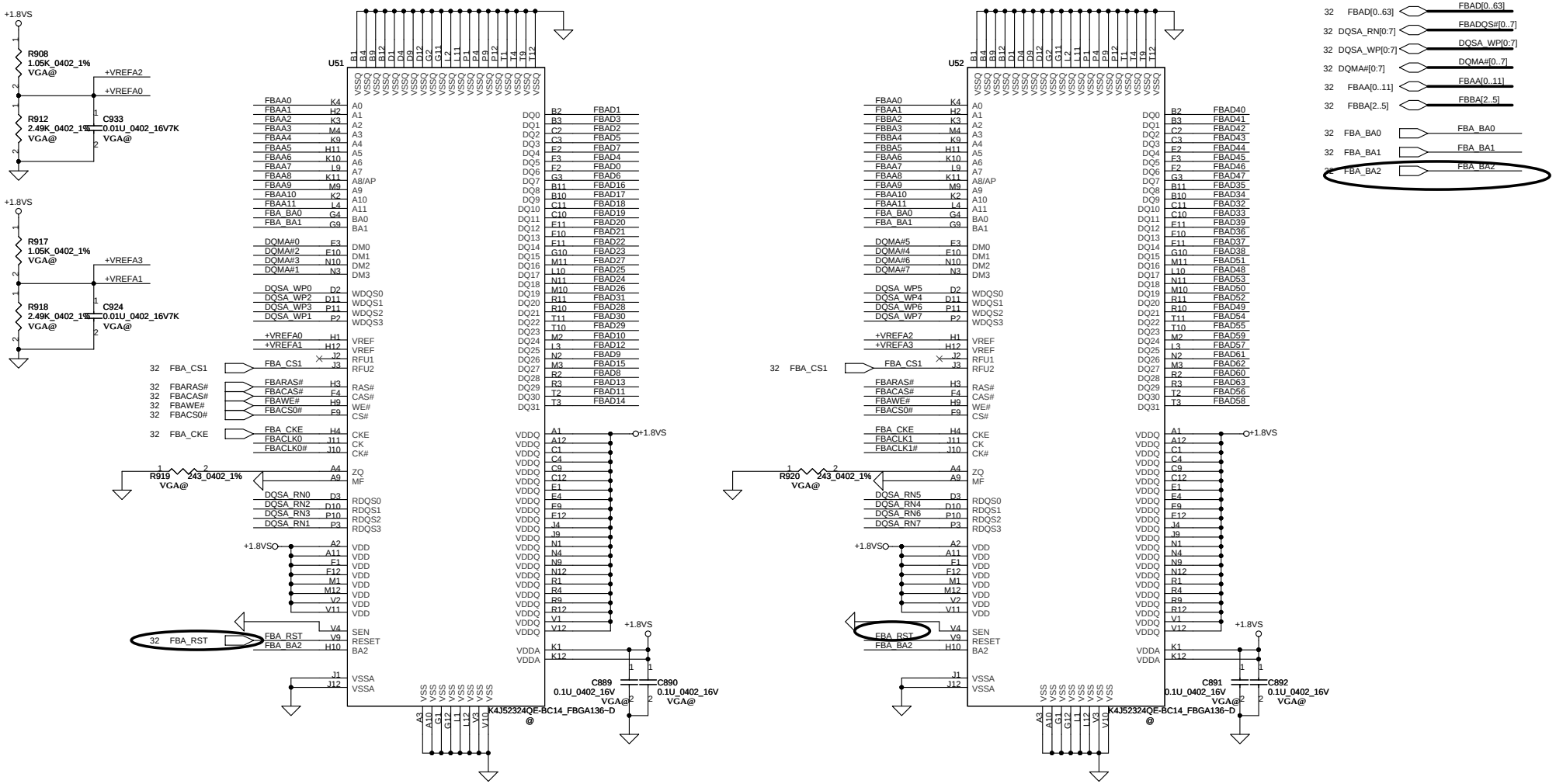

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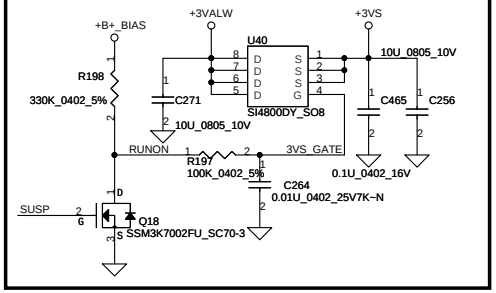
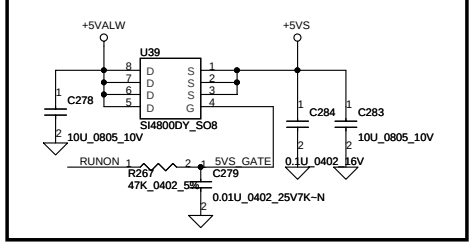
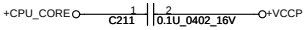
+3VALW to +3VS Transfer

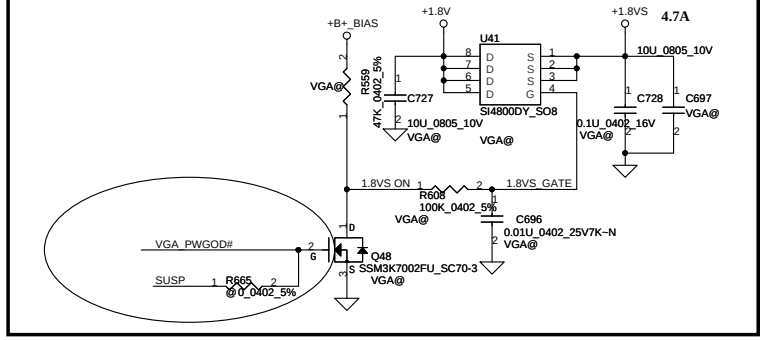


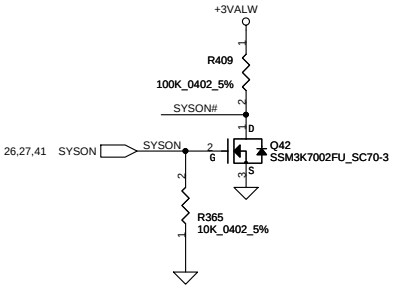
+5VALW to +5VS Transfer

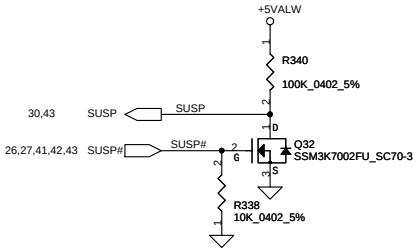


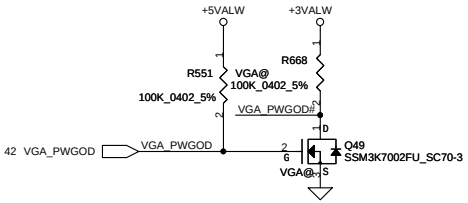


+1.8V to +1.8VS Transfer



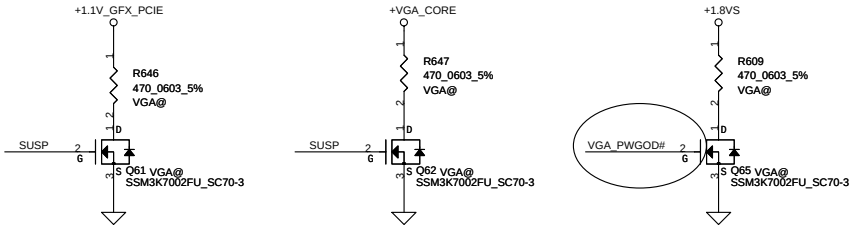




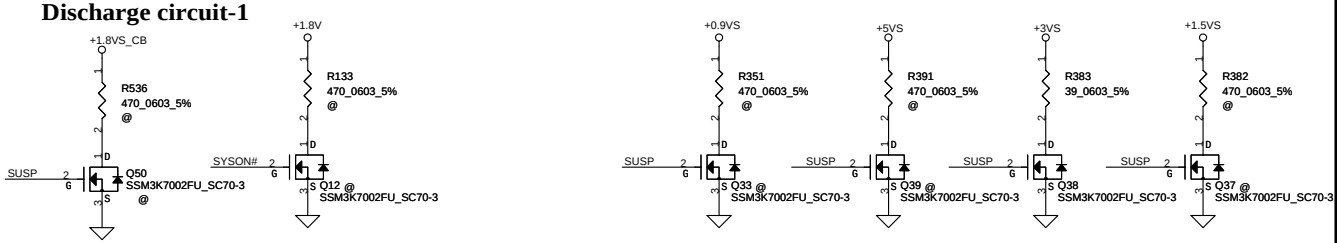


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



Discharge circuit-1



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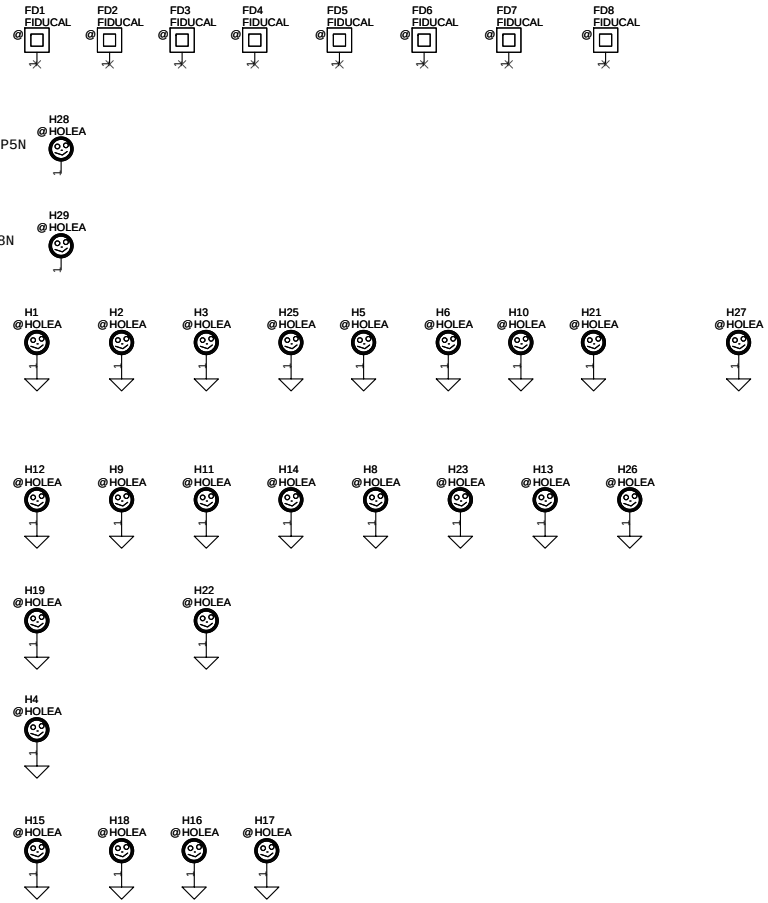

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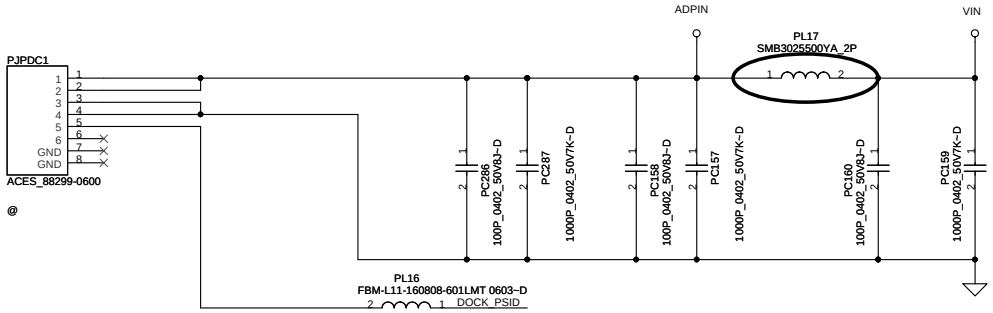
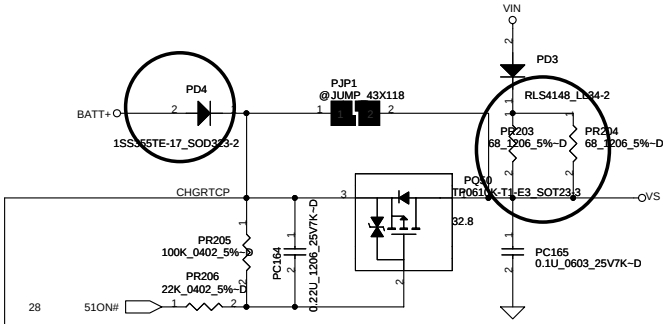
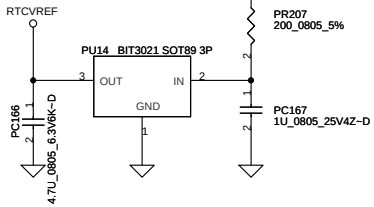
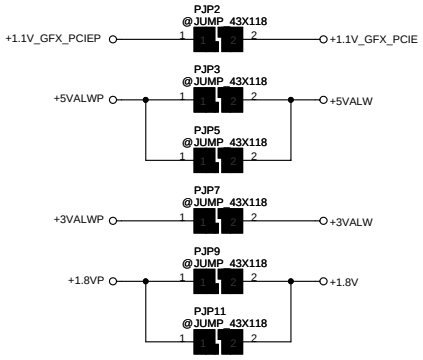
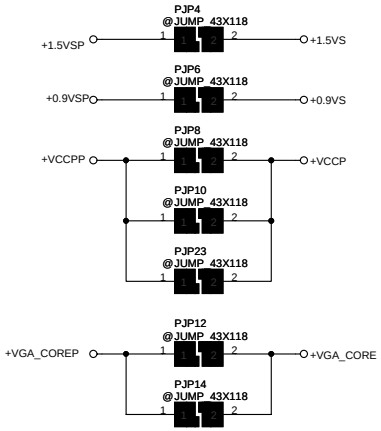
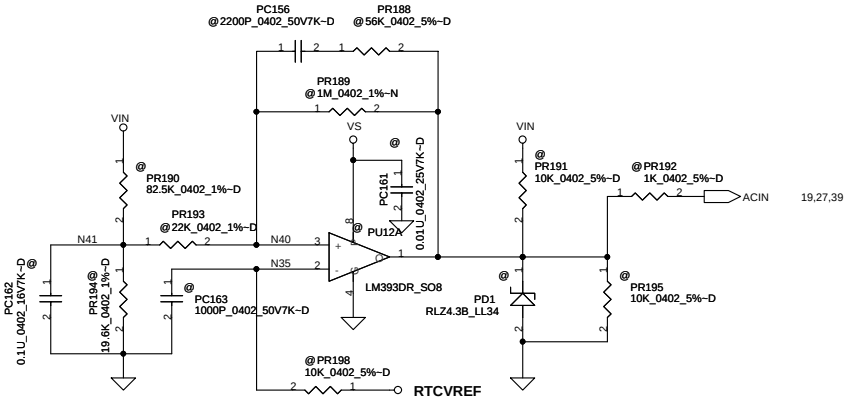






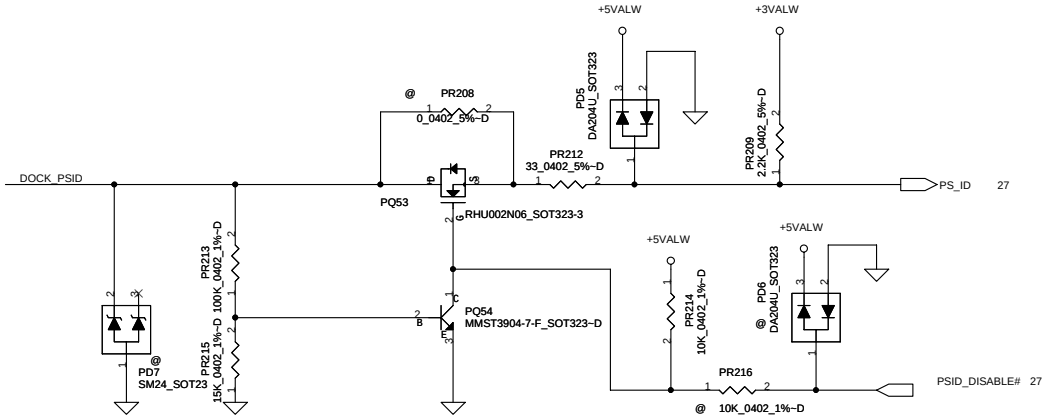






Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813



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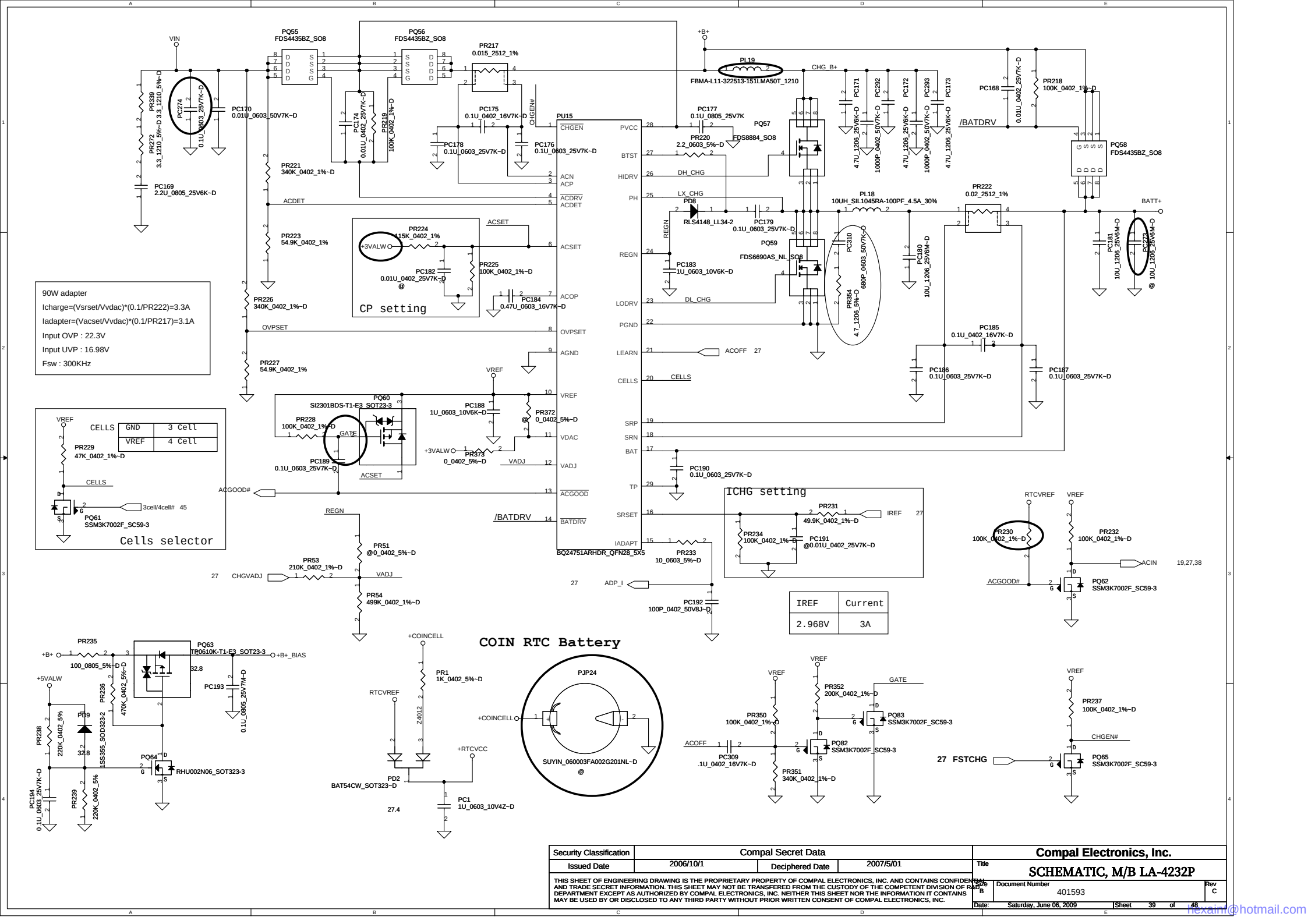

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Issued Date	2006/10/1	Deciphered Date	2007/5/01

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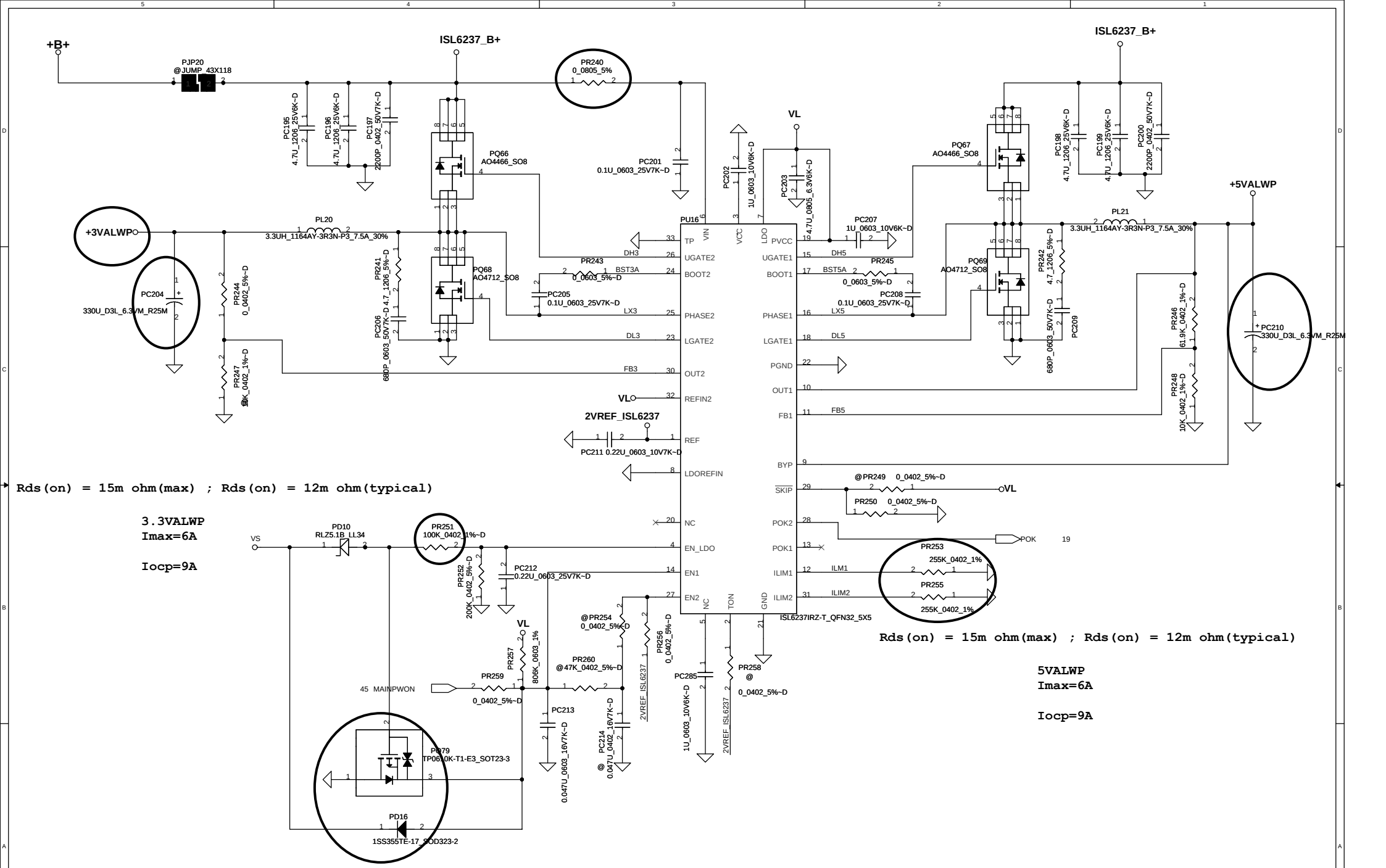

Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

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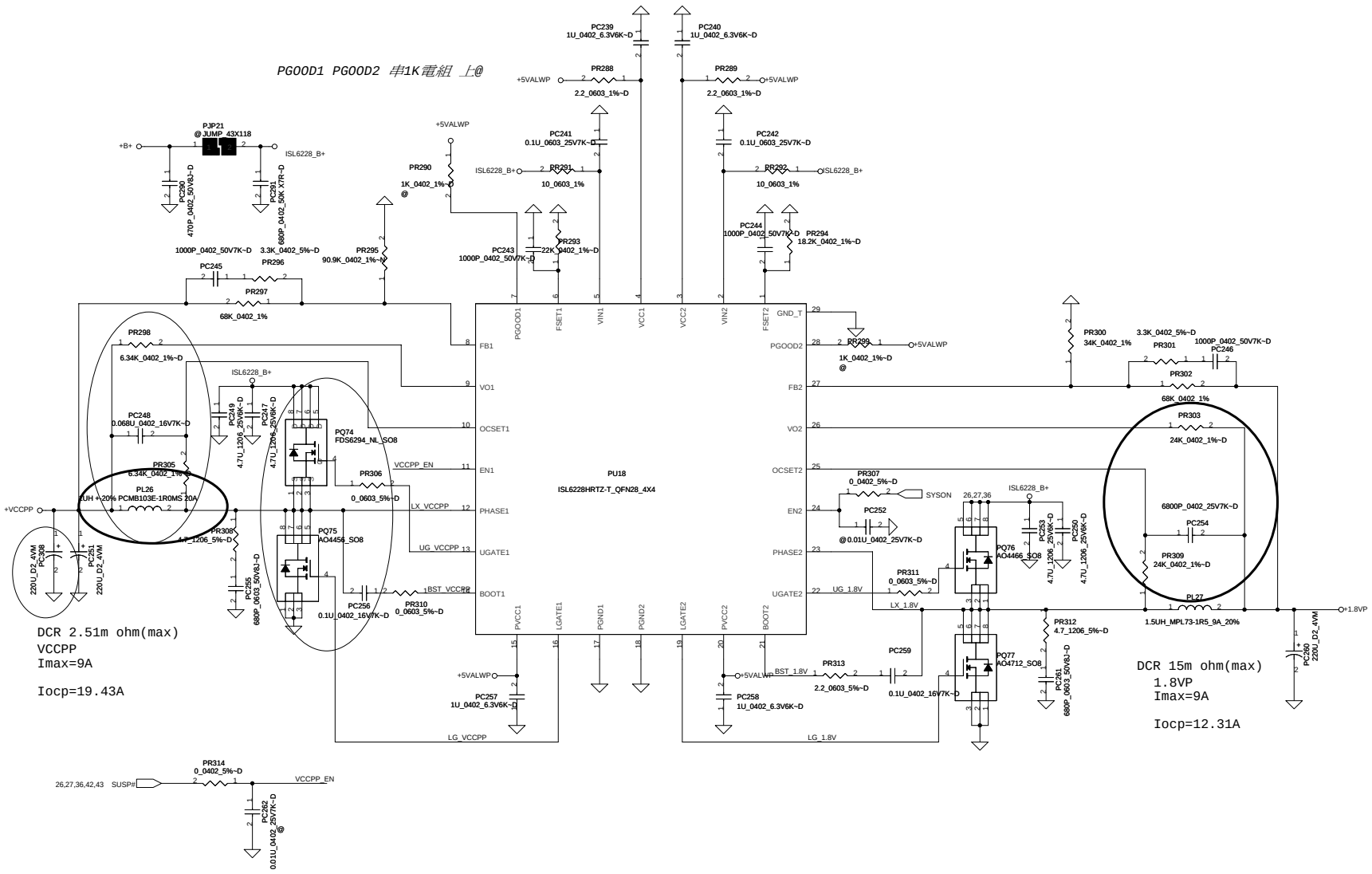

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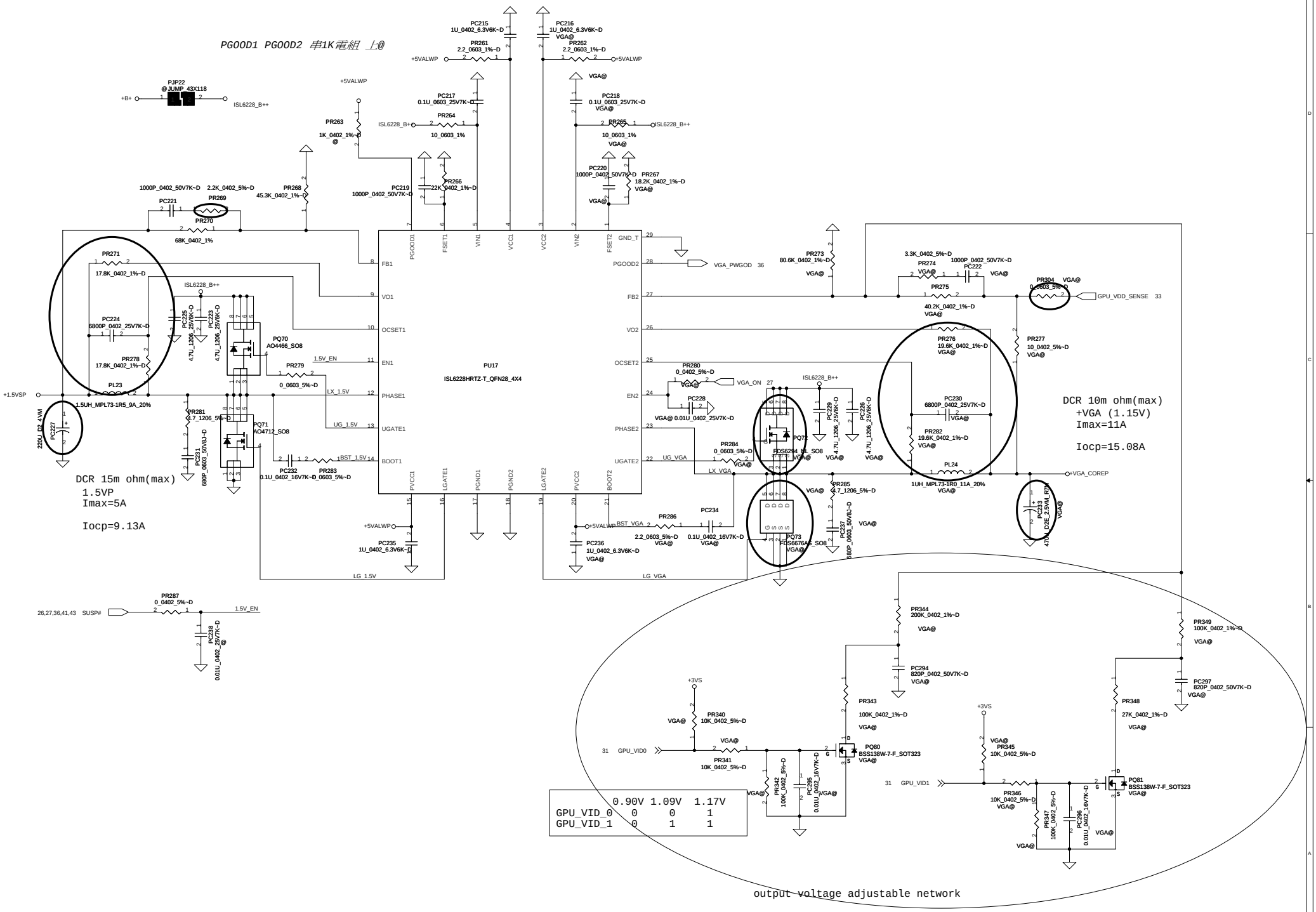

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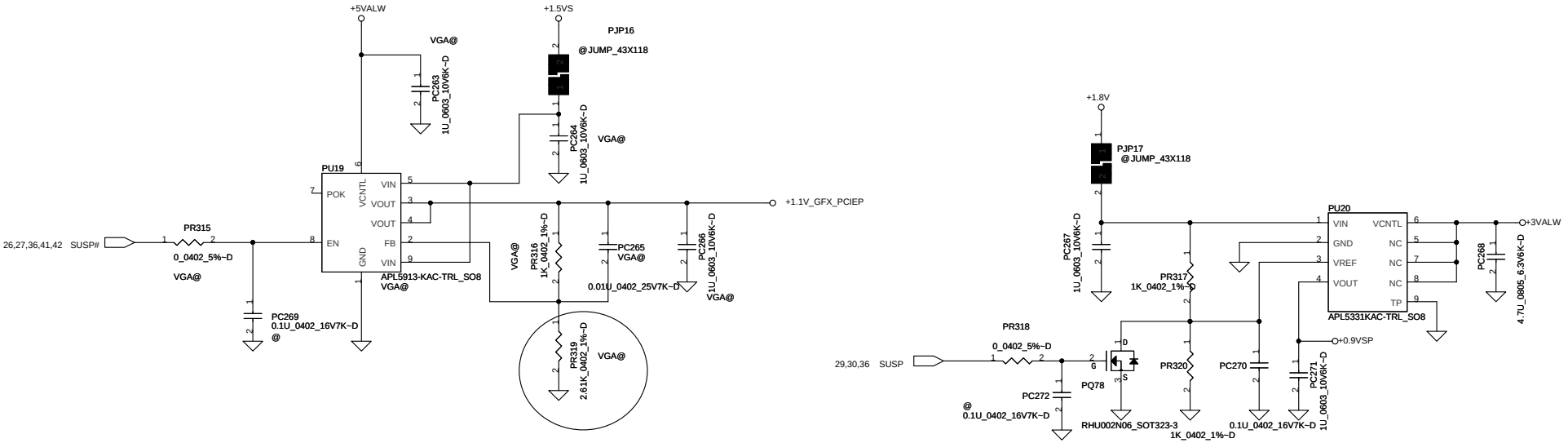

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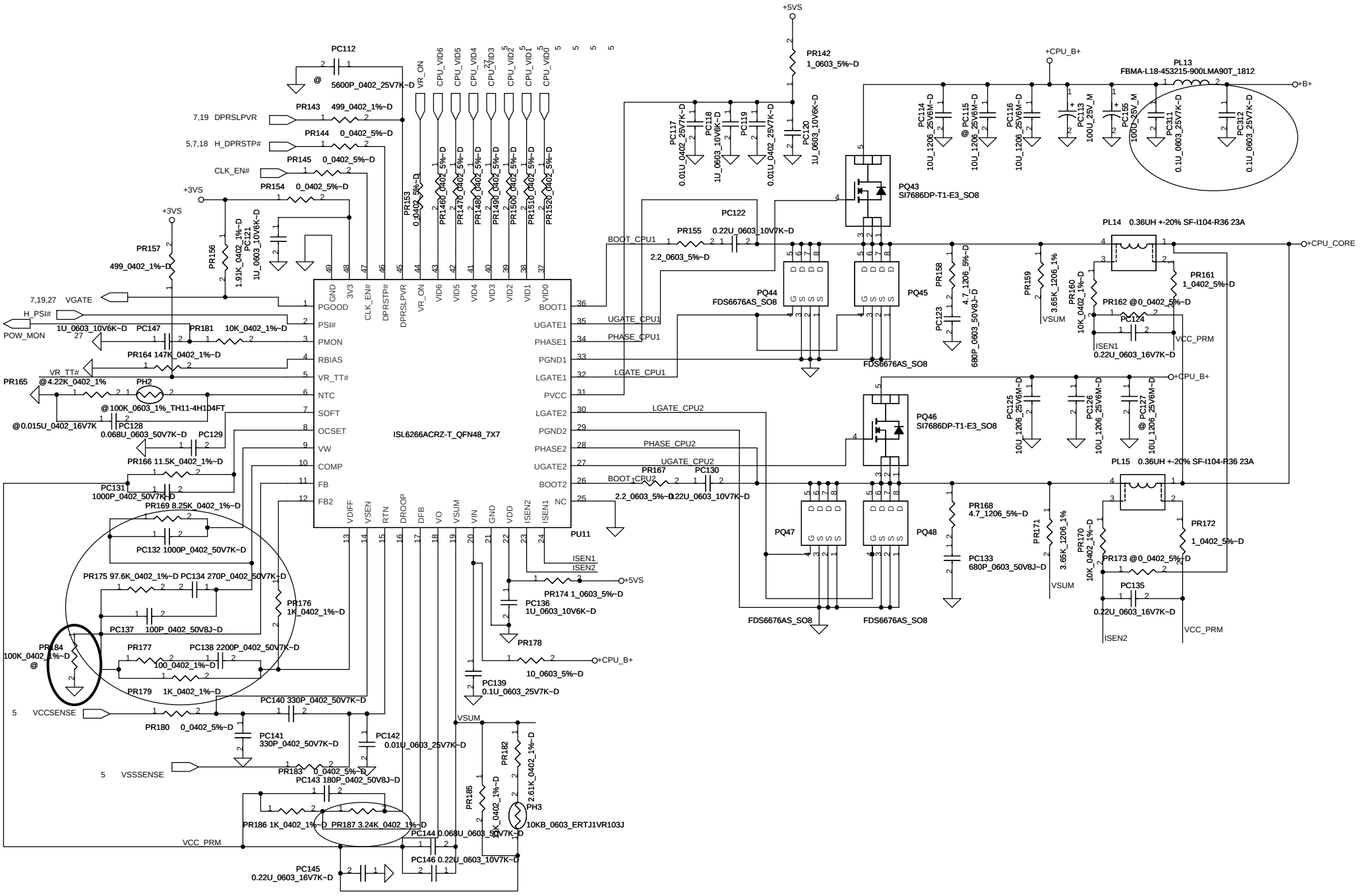

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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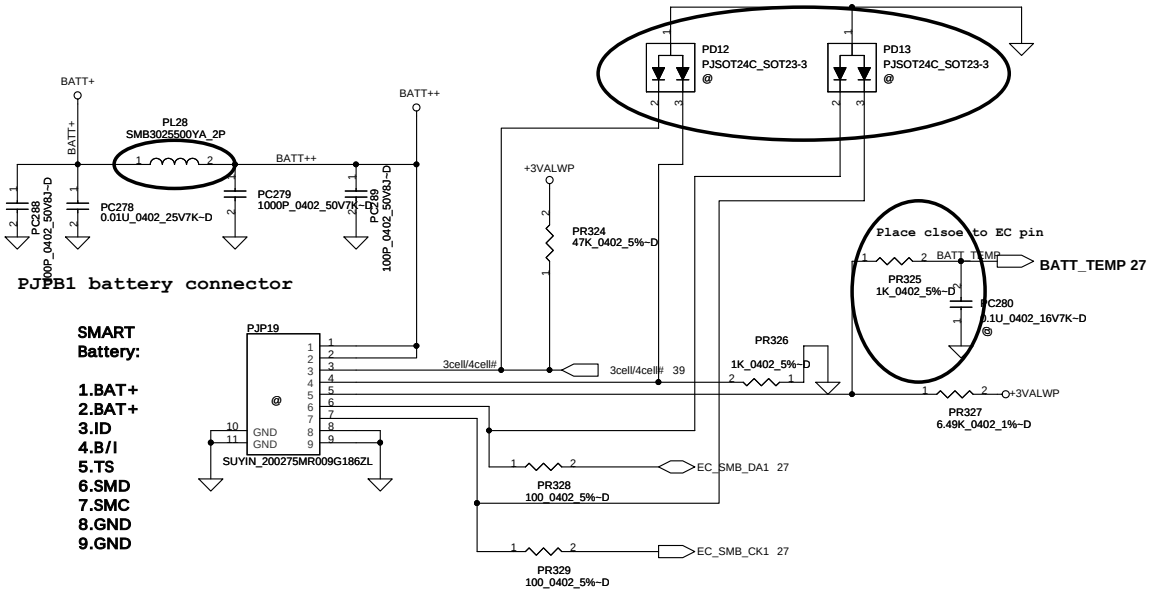
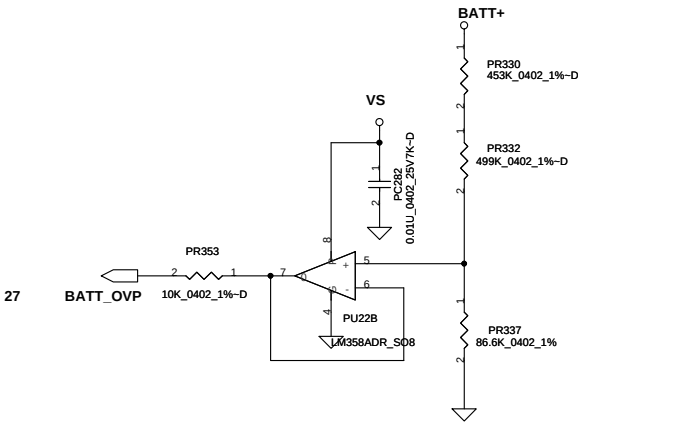
Battery Connect/OTP

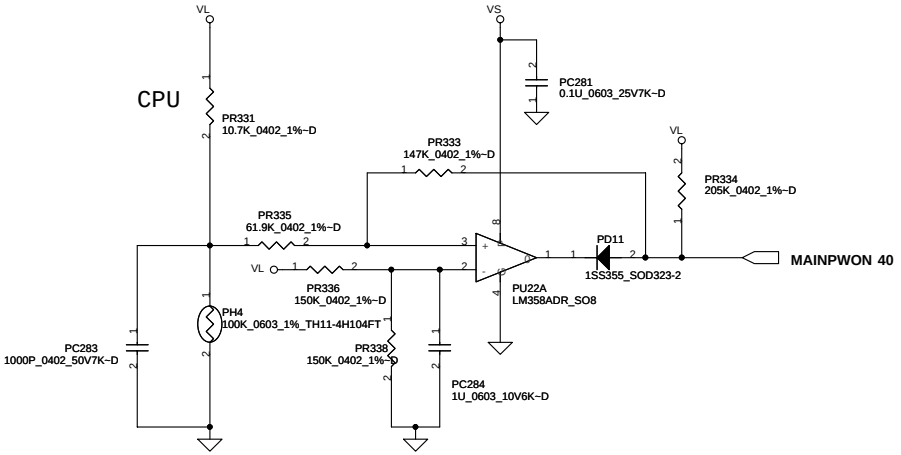


CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-OZ129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to OZ129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Frequence Decoupling Capacitance	C195 change to C1150~C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
18	20	P20-ICH9(4/4)_POWER&GND	08/04/22	compal	+5VS & +3VS have leakage	Change VCCCL3[1] [2] & VCCLAN3_3[1] [2] power source to +LAN_IO	
19	20	P09-Cantiga(3/6)-VGA/LVDS/TV	08/04/22	compal	Can't boot to OS	Add BOM Structure @	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	1.8VP/+VCCPP	08/10/22	COMPAL	adjust +VCCP OCP set	Change PC248 from 0.033u to 0.068u	0.2
2	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	ripple voltage fail	Change PC227 from SF22001M300 to SGA20221150	0.2
3	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	convenient test	Add PR304	0.2
4	44	CPU_CORE	08/10/22	COMPAL	load line fail	Change PR187 from 2.21K to 3.24K	0.2
5	38	DCIN / Precharge	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
6	39	Charger	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
7	40	+3VALWP/+5VALWP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
8	41	1.8VP/+VCCPP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
9	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
10	43	+0.9VSP/+1.1V_GFX_PCIEP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
11	44	CPU_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
12	45	BATTERY CONN	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
13	40	+3VALWP/+5VALWP	08/10/24	COMPAL	boost choke current rating	change PL20 PL21 from SH000006380 to SH00000AY00	0.2
14	45	BATTERY CONN	08/10/30	COMPAL	delete diode for EMD request	del PD14 PD15	0.2
15	45	BATTERY CONN	08/10/30	COMPAL	change diode for EMD request	change PD12 PD13 from SC1A204U00L to SCA00000E00	0.2
16	39	Charger	08/10/31	COMPAL	design modify	add PR372 PR373	0.2
17	41	1.8VP/+VCCPP	08/11/03	COMPAL	dynamic fail	change PC233 from SGA20221150 to SGA00001U80	0.2
18	44	CPU_CORE	08/12/08	COMPAL	cost down	change PU11 from SA00001HU80 to SA000031W00 and interrelated components	0.3
19	38	DCIN / Precharge	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
20	39	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
21	38	DCIN / Precharge	08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
22	45	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
23	39	Charger	08/12/15	COMPAL	change component for EMD request	change PJP15 to PL19 SM010016410	0.3
24	39	Charger	08/12/15	COMPAL	add capacitor for EMD request	add PC274 0.1u	0.3
25	42	1.5VSP/+VGA_CORE	09/01/19	COMPAL	adjust VGA_CORE OCP set	change PQ72 from SB00000CG00 to SB562940080	0.4
26						change PQ73 from SB00000AJ00 to SB000003W00	0.4
27						change PL24 from SH000008700 to SH000005400	0.4
28						change PR276 PR282 from 24K to 19.6K	0.4
29						change PC230 from 0.022u to 6800p	0.4
30					consumption adjust	change PR269 from 3.3K to 2.2K	0.4
31	44	CPU_CORE	09/01/19	COMPAL	vendor FAE suggest	add PC141 330p	0.4
32	45	BATTERY CONN	09/02/18	COMPAL	delete diode for ESD request	del PD12 PD13	0.4

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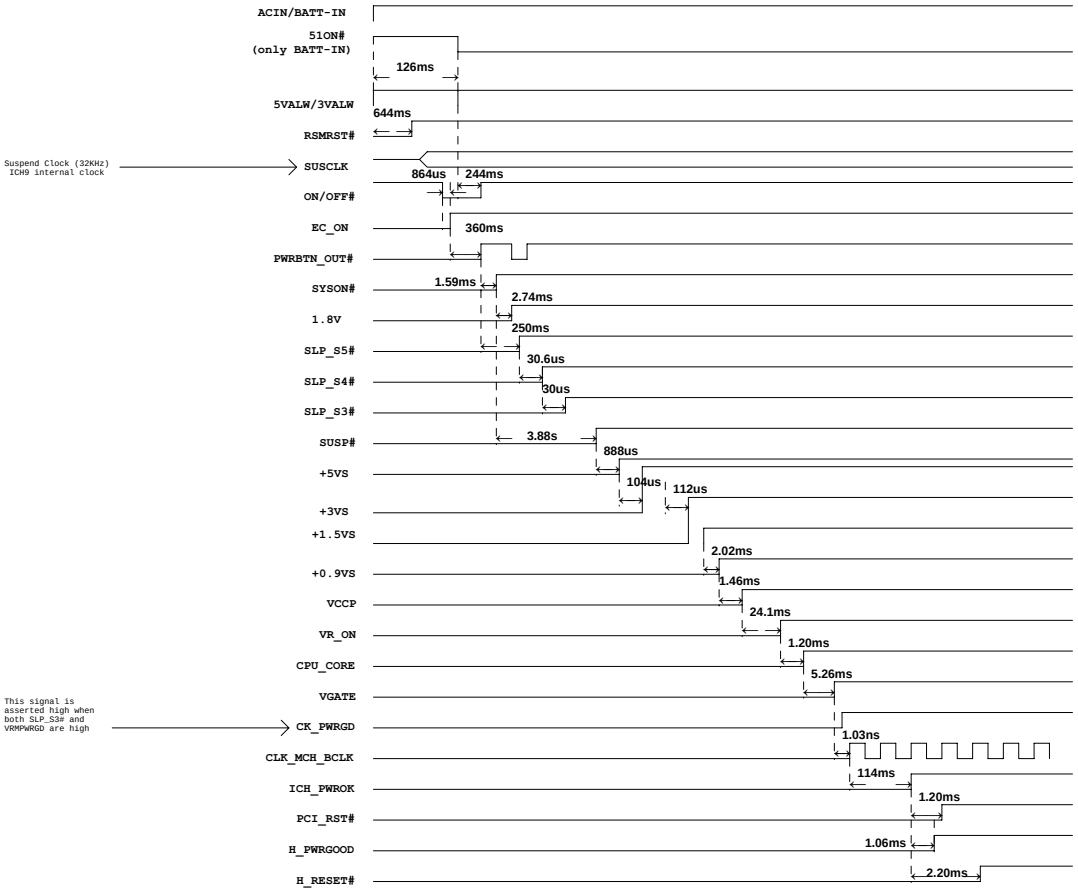
KAL80 POWER UP SEQUENCE



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