DELL Vostro 1310
COMPAL LA-4231P - JAL80

Compal Confidential

Schematic Document

Crestline + ICH8

2007 / 11 / 14 Rev:0.2

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

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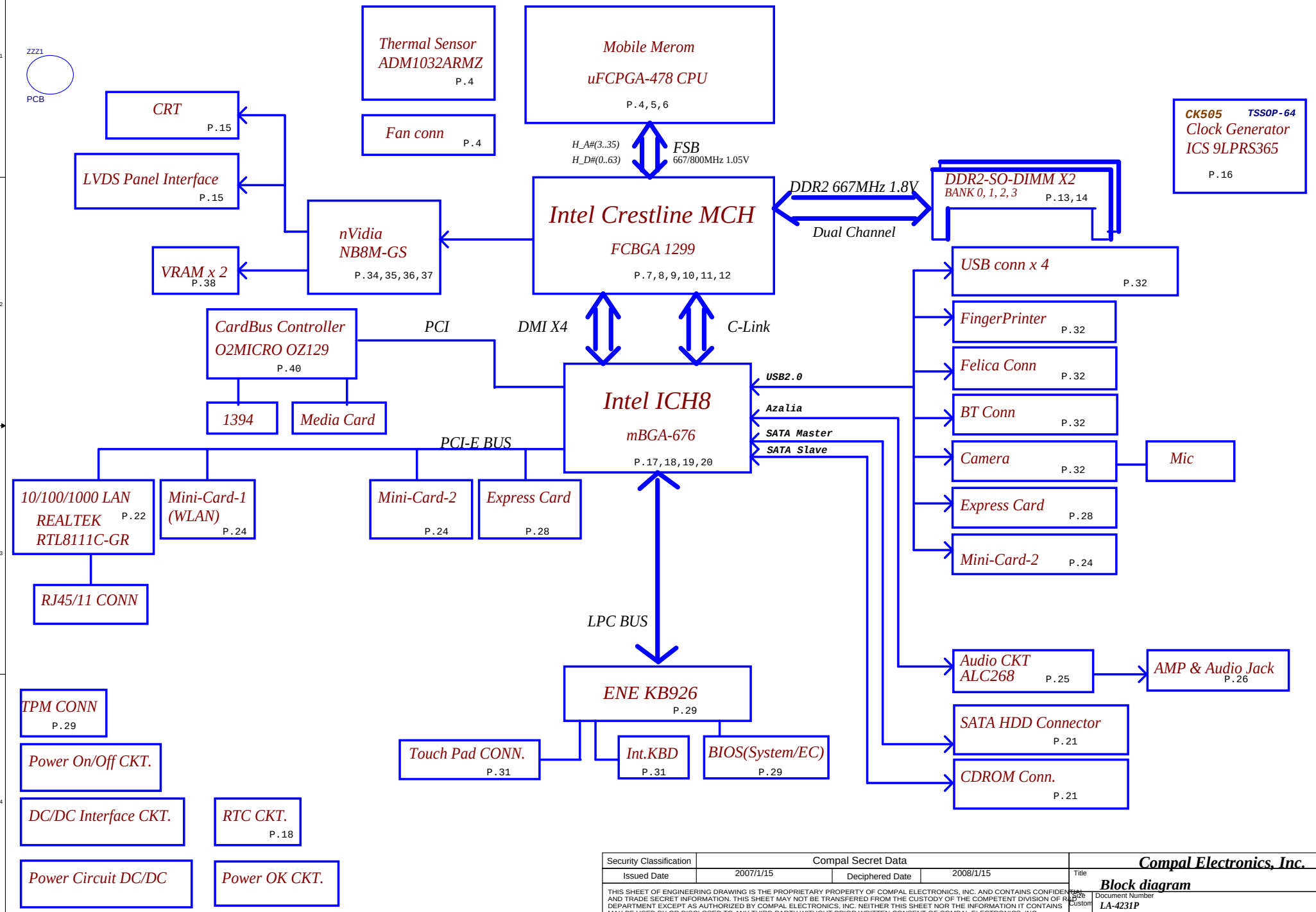
Title: *Cover Sheet*

Size	Document Number	Rev
Custom	*LA-4231P*	0.1

Date: Thursday, January 10, 2008 Sheet 1 of 49

DELL Vostro 1310
COMPAL LA-4231P

SMB 13.3



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Title: **Block diagram**

Size: Custom	Document Number: LA-4231P	Rev: 0.1
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Voltage Rails

O MEANS ON X MEANS OFF

State \ power plane	+B	+5VALW +3VALW	+3V +1.8V	+5VS +3VS +1.8VS +1.5VS +1.25VS +CPU_CORE +VCCP	CLOCK
S0	O	O	O	O	O
S3	O	O	O	X	O
S5 S4/AC	O	O	X	X	O
S5 S4/ Battery only	O	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

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Title: Notes

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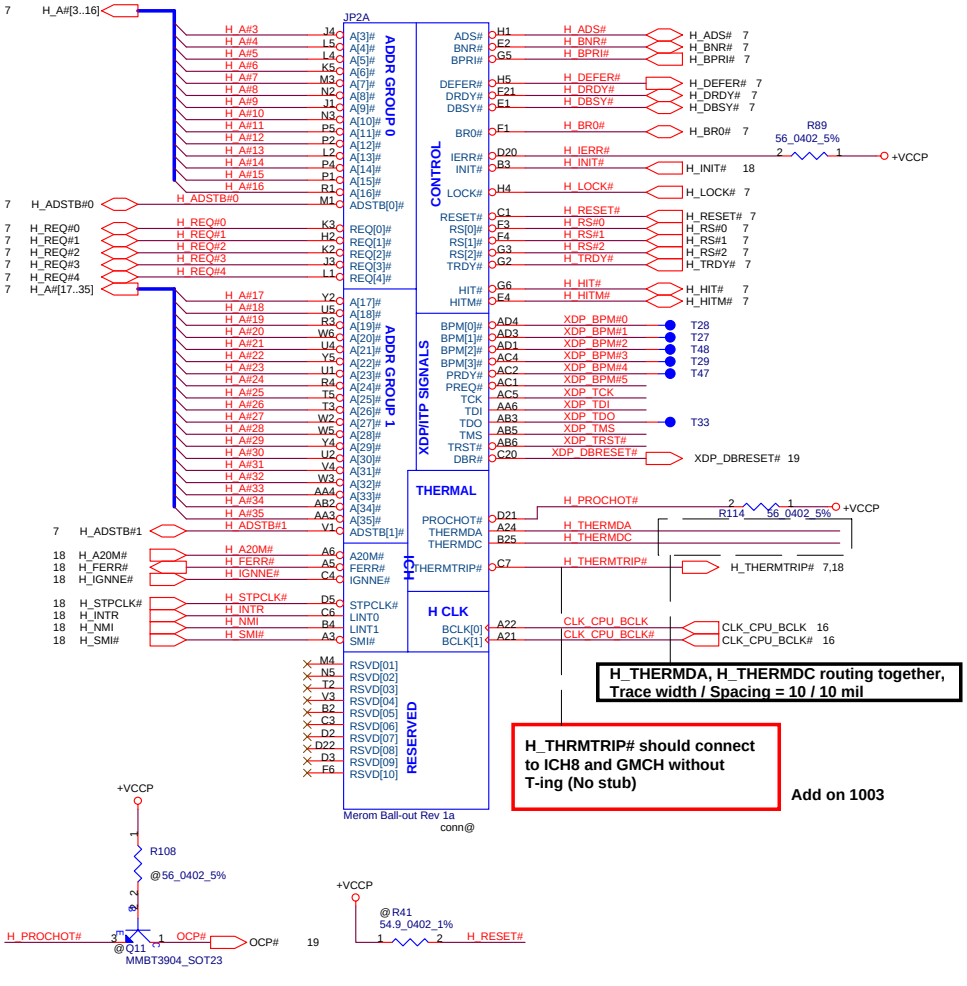
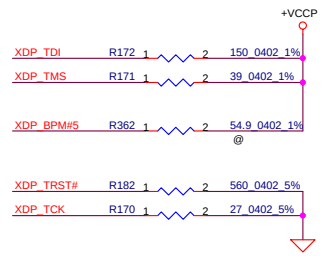


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

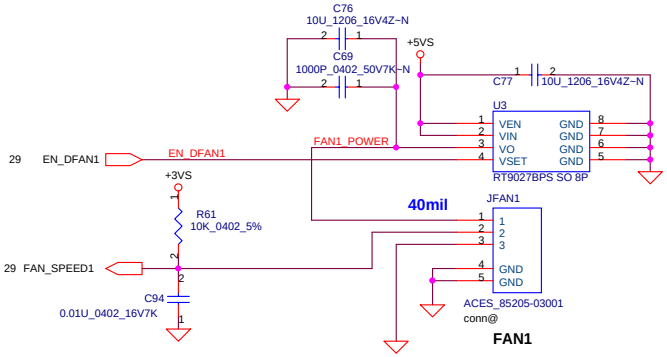
H_THRMTRIP# should connect to ICH8 and GMCH without T-ing (No stub)

Add on 1003

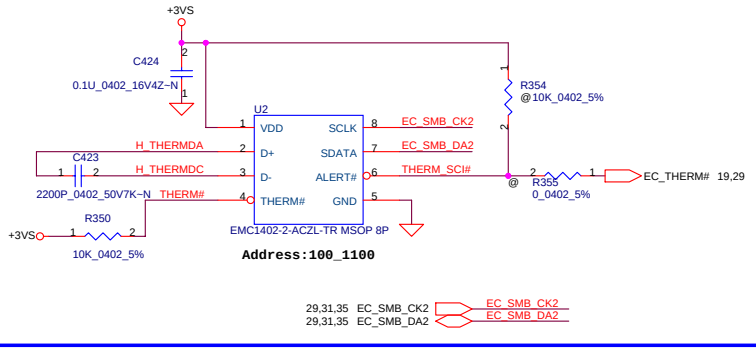
XDP Reserve



FAN1 Control and Tachometer



Thermal Sensor EMC1402-1-ACZL-TR



29,31,35 EC_SMB_CK2 — EC_SMB_CK2
29,31,35 EC_SMB_DA2 — EC_SMB_DA2

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Compal Electronics, Inc.

Title: **Merom(1/3)-AGTL+/XDP**

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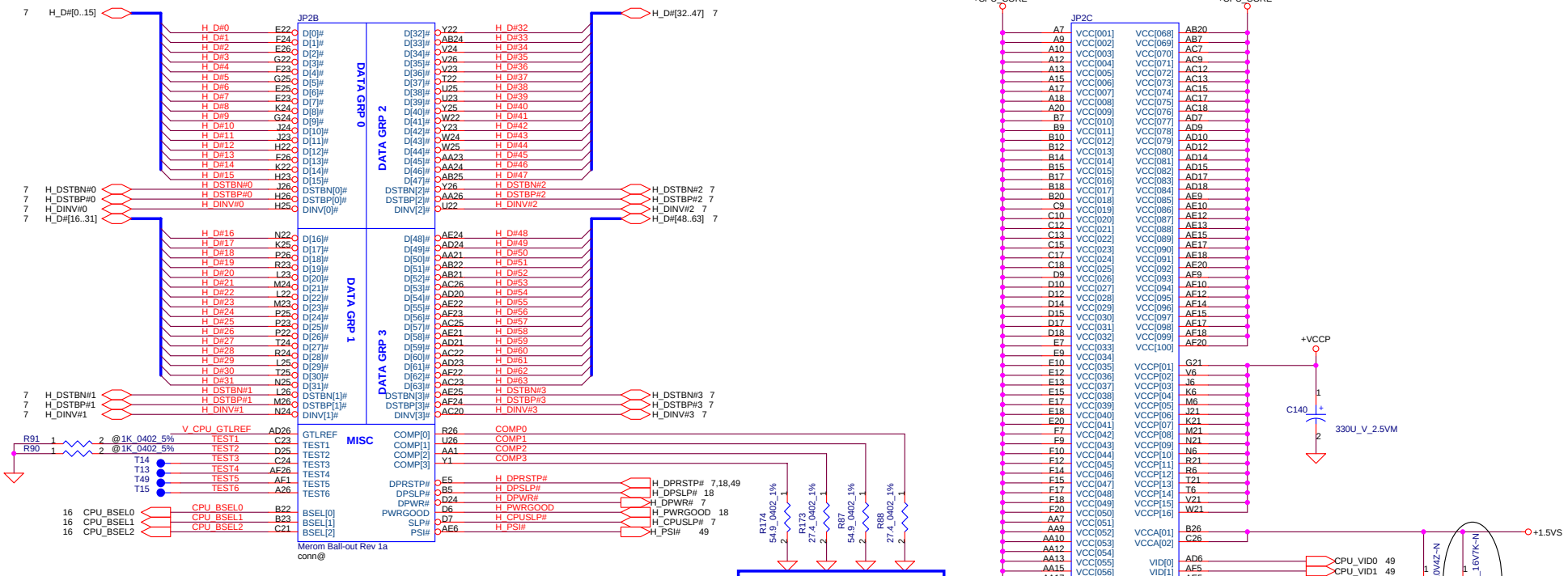
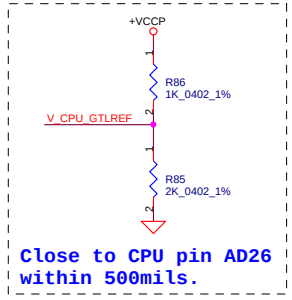


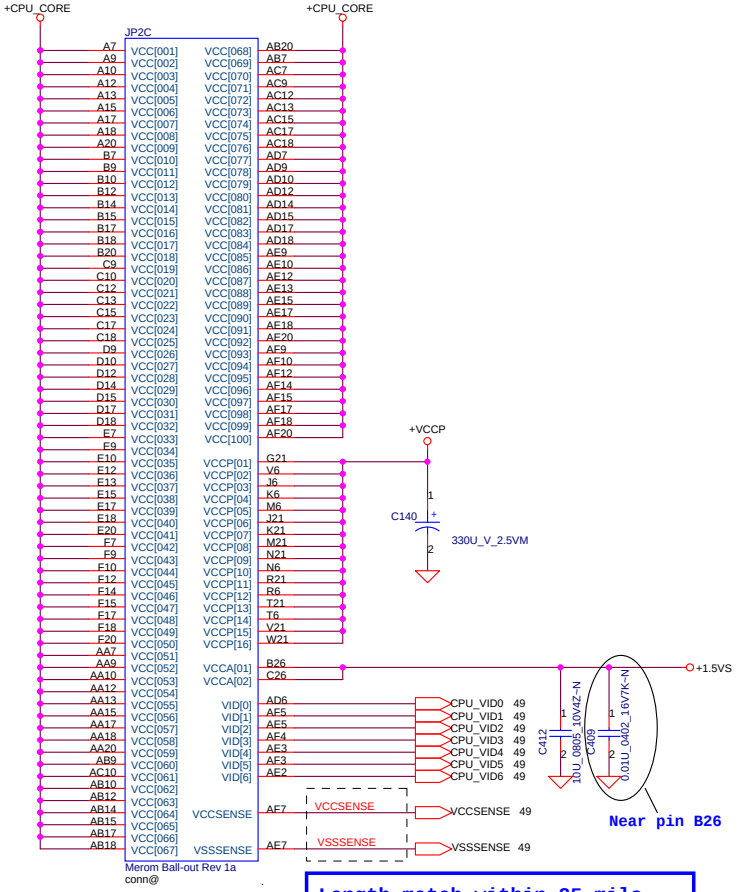
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

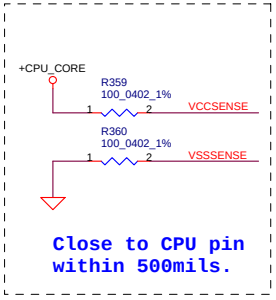
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal.
COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Close to CPU pin AD26 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Merom(2/3)-AGTL+/PWR

Size	Document Number	Rev
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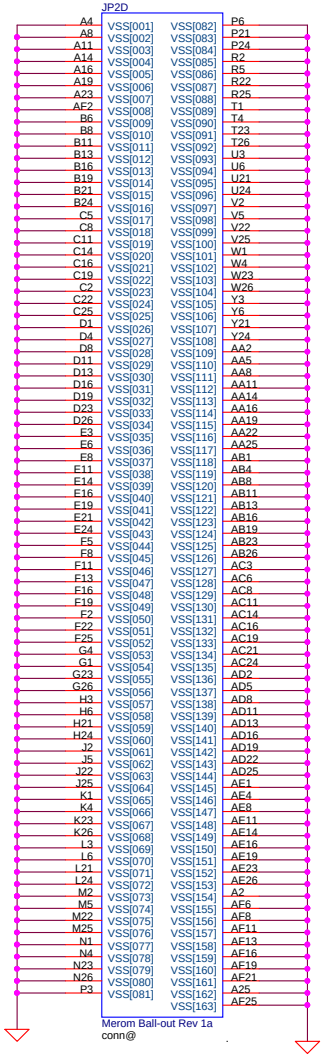
High Frequence Decoupling

10uF 0805 X5R -> 85 degree.



Place these caps inside the CPU socket cavity.
(Left side on Top).

+CPU_CORE

C1150 10U_0805_6.3V6M
C1151 10U_0805_6.3V6M
C1152 10U_0805_6.3V6M
C1153 10U_0805_6.3V6M
C1154 10U_0805_6.3V6M
C1155 10U_0805_6.3V6M
C1156 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Left side on Top).

C1157 10U_0805_6.3V6M
C1158 10U_0805_6.3V6M
C1159 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Top side).

+CPU_CORE

C1160 10U_0805_6.3V6M
C1161 10U_0805_6.3V6M
C1162 10U_0805_6.3V6M
C1163 10U_0805_6.3V6M
C1164 10U_0805_6.3V6M
C1165 10U_0805_6.3V6M
C1166 10U_0805_6.3V6M

Place these caps inside the CPU socket.
(Right side on Top).

C1167 10U_0805_6.3V6M
C1168 10U_0805_6.3V6M
C1169 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Left side on Bottom).

+CPU_CORE

C1170 10U_0805_6.3V6M
C1171 10U_0805_6.3V6M
C1172 10U_0805_6.3V6M
C1173 10U_0805_6.3V6M
C1174 10U_0805_6.3V6M
C1175 10U_0805_6.3V6M

Place these caps inside the CPU socket cavity.
(Right side on Bottom).

+CPU_CORE

C1176 10U_0805_6.3V6M
C1177 10U_0805_6.3V6M
C1178 10U_0805_6.3V6M
C1179 10U_0805_6.3V6M
C1180 10U_0805_6.3V6M
C1181 10U_0805_6.3V6M

Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

+CPU_CORE

C190 330U_V_2.5VM
C429 330U_V_2.5VM @
C207 330U_V_2.5VM
C426 330U_V_2.5VM

Place these inside socket cavity on L8 (North side Secondary)

+VCCP

C212 220U_D2_4VY_R15M
C210 0.1U_0402_10V6K
C209 0.1U_0402_10V6K
C208 0.1U_0402_10V6K
C185 0.1U_0402_10V6K
C183 0.1U_0402_10V6K
C184 0.1U_0402_10V6K

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Title: **Merom(3/3)-GND&Bypass**

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For Crestline: 20ohm
For Calero: 80.6ohm

layout note:

Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20

within 100 mils from NB

Near B3 pin

Layout Note:
+DDR_MCH_REF
trace width and
spacing is 20/20.

close to NB

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size: Custom | Document Number: LA-4231P | Rev: 0.1

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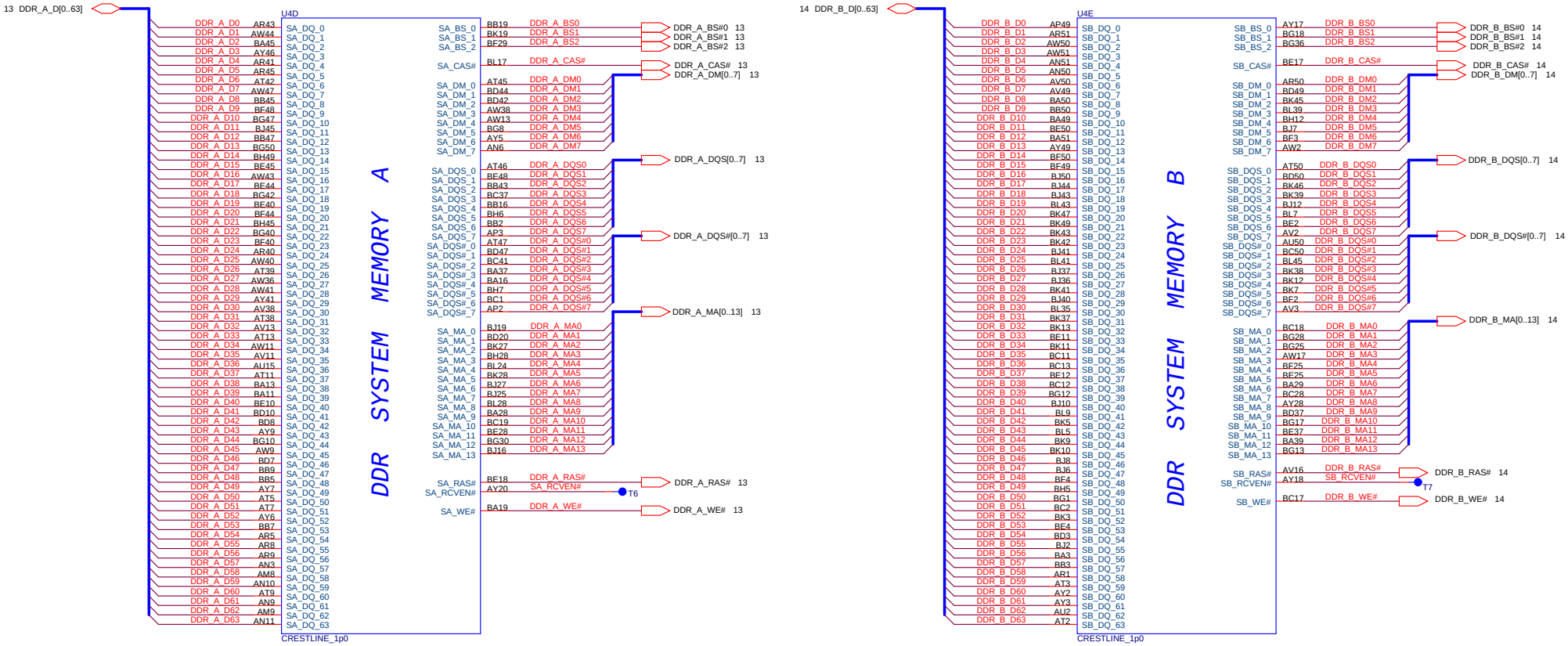

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **CRESTLINE((2/6)-DDR2 A/B CH**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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For Crestline:2.4kohm
For Calero: 1.5Kohm

PEGCOMP trace width
and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline:1.3kohm
For Calero: 255ohm

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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Title: CRESTLINE((3/6)-VGA/LVDS/TV

Size	Document Number	Rev
Custom	LA-4231P	0.1

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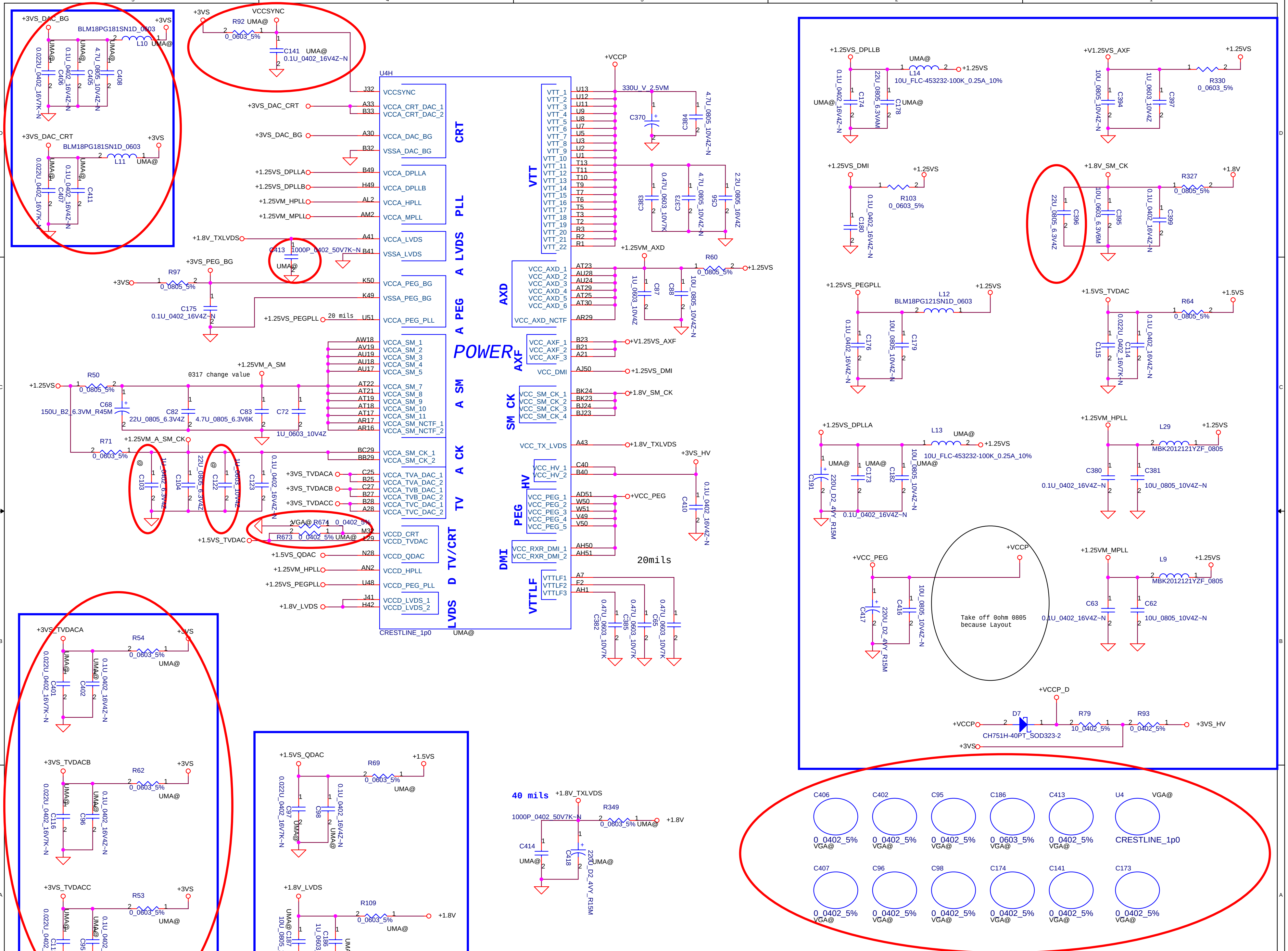
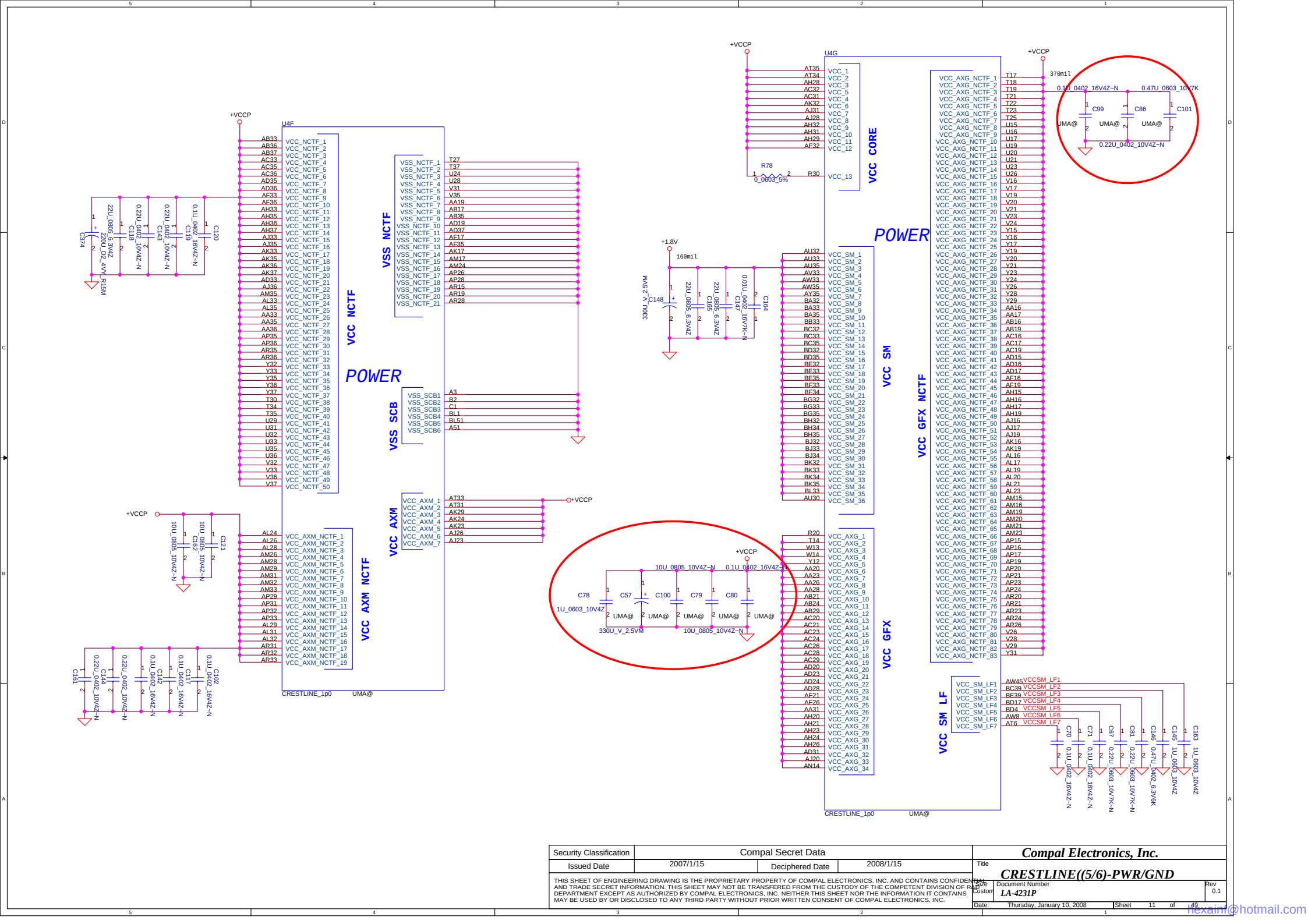


Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **CRESTLINE(4/6)-PWR**

Size	Document Number	Rev
Custom	LA-4231P	0.1



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Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: **CRESTLINE((5/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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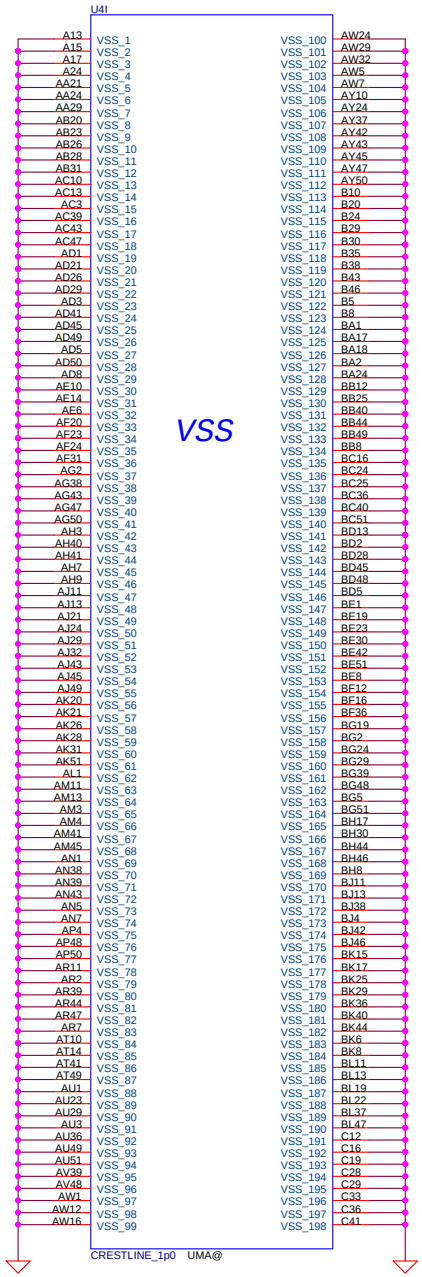

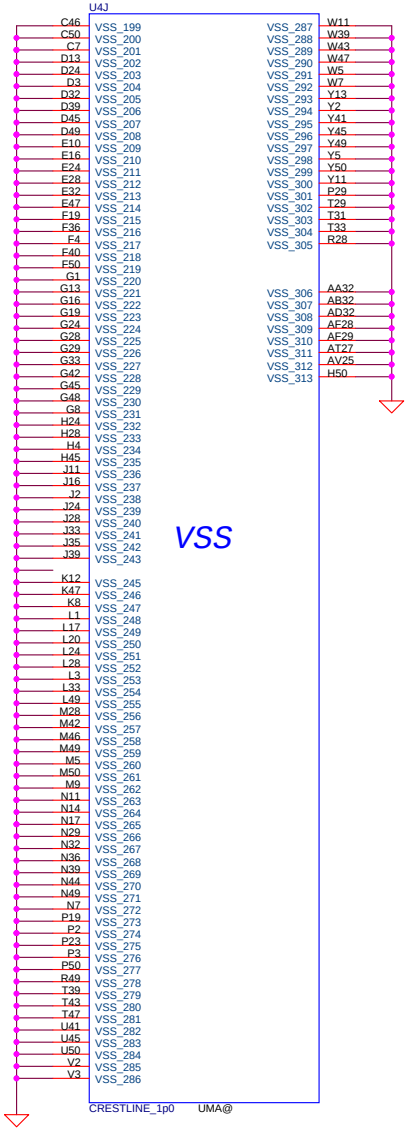

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **CRESTLINE((6/6)-PWR/GND**

Size	Document Number	Rev
Custom	LA-4231P	0.1

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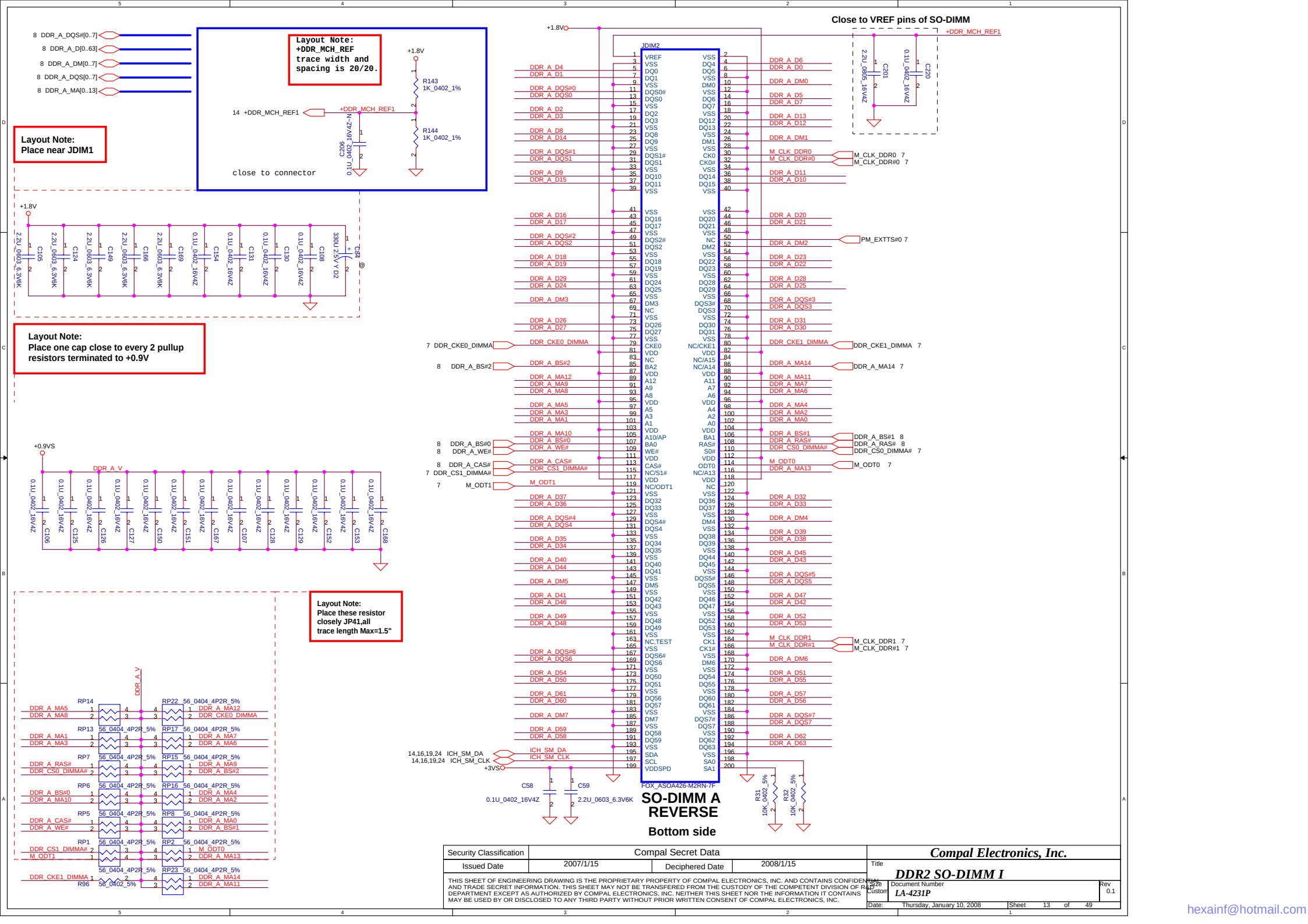

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Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: DDR2 SO-DIMM I			
Size: Custom	Document Number: LA-4231P		Rev: 0.1
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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V
C112 2.2U_0603_6.3V6K
C139 2.2U_0603_6.3V6K
C160 2.2U_0603_6.3V6K
C138 2.2U_0603_6.3V6K
C177 2.2U_0603_6.3V6K
C109 0.1U_0402_16V4Z
C132 0.1U_0402_16V4Z
C133 0.1U_0402_16V4Z
C155 0.1U_0402_16V4Z
C189 330U 2.5V Y D2 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
DDR_B_V
C110 0.1U_0402_16V4Z
C134 0.1U_0402_16V4Z
C135 0.1U_0402_16V4Z
C156 0.1U_0402_16V4Z
C157 0.1U_0402_16V4Z
C170 0.1U_0402_16V4Z
C171 0.1U_0402_16V4Z
C111 0.1U_0402_16V4Z
C136 0.1U_0402_16V4Z
C158 0.1U_0402_16V4Z
C137 0.1U_0402_16V4Z
C172 0.1U_0402_16V4Z
C159 0.1U_0402_16V4Z

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

DDR_B_V
RP18 56_0404_4P2R_5%: DDR_B_MA3, DDR_B_MA1 / DDR_B_MA12, DDR_B_MA9
RP24 56_0404_4P2R_5%
RP10 56_0404_4P2R_5%: DDR_B_BS#0, DDR_B_MA10 / DDR_B_MA14, DDR_B_MA11
RP26 56_0404_4P2R_5%
RP12 56_0404_4P2R_5%: DDR_B_MA0, DDR_B_BS#1 / DDR_B_MA5, DDR_B_MA8
RP19 56_0404_4P2R_5%
RP11 56_0404_4P2R_5%: DDR_B_RAS#, DDR_CS2_DIMMB# / DDR_B_MA7, DDR_B_MA6
RP21 56_0404_4P2R_5%
RP9 56_0404_4P2R_5%: DDR_B_CAS#, DDR_B_WE# / DDR_B_MA4, DDR_B_MA2
RP20 56_0404_4P2R_5%
RP3 56_0404_4P2R_5%: DDR_CS3_DIMMB#, M_ODT3 / DDR_B_MA13, M_ODT2
RP4 56_0404_4P2R_5%
RP25 56_0404_4P2R_5%: DDR_CKE3_DIMMB, R335 56_0402_5% / DDR_B_BS#2, DDR_CKE2_DIMMB

Close to VREF pins of SO-DIMM

+1.8V
+DDR_MCH_REF1 → +DDR_MCH_REF1 13
C221 2.2U_0805_16V4Z
C222 0.1U_0402_16V4Z

JDIM1 — FOX_AS0A426-NARN-7F-N

	VREF	1	2	VSS	
	VSS	3	4	DQ4	DDR_B_D5
DDR_B_D0	DQ0	5	6	DQ5	DDR_B_D4
DDR_B_D1	DQ1	7	8	VSS	
	VSS	9	10	DM0	DDR_B_DM0
DDR_B_DQS#0	DQS0#	11	12	VSS	
DDR_B_DQS0	DQS0	13	14	DQ6	DDR_B_D6
	VSS	15	16	DQ7	DDR_B_D7
DDR_B_D2	DQ2	17	18	VSS	
DDR_B_D3	DQ3	19	20	DQ12	DDR_B_D12
	VSS	21	22	DQ13	DDR_B_D13
DDR_B_D8	DQ8	23	24	VSS	
DDR_B_D9	DQ9	25	26	DM1	DDR_B_DM1
	VSS	27	28	VSS	
DDR_B_DQS#1	DQS1#	29	30	CK0	M_CLK_DDR2 → M_CLK_DDR2 7
DDR_B_DQS1	DQS1	31	32	CK0#	M_CLK_DDR#2 → M_CLK_DDR#2 7
	VSS	33	34	VSS	
DDR_B_D10	DQ10	35	36	DQ14	DDR_B_D14
DDR_B_D11	DQ11	37	38	DQ15	DDR_B_D15
	VSS	39	40	VSS	
		41	42	VSS	
DDR_B_D17	DQ16	43	44	DQ20	DDR_B_D21
DDR_B_D20	DQ17	45	46	DQ21	DDR_B_D16
	VSS	47	48	VSS	
DDR_B_DQS#2	DQS2#	49	50	NC	
DDR_B_DQS2	DQS2	51	52	DM2	DDR_B_DM2 → PM_EXTTS#1 7
	VSS	53	54	VSS	
DDR_B_D18	DQ18	55	56	DQ22	DDR_B_D22
DDR_B_D19	DQ19	57	58	DQ23	DDR_B_D23
	VSS	59	60	VSS	
DDR_B_D28	DQ24	61	62	DQ28	DDR_B_D26
DDR_B_D25	DQ25	63	64	DQ29	DDR_B_D24
	VSS	65	66	VSS	
DDR_B_DM3	DM3	67	68	DQS3#	DDR_B_DQS#3
	NC	69	70	DQS3	DDR_B_DQS3
	VSS	71	72	VSS	
DDR_B_D30	DQ26	73	74	DQ30	DDR_B_D29
DDR_B_D31	DQ27	75	76	DQ31	DDR_B_D27
	VSS	77	78	VSS	
7 DDR_CKE2_DIMMB → DDR_CKE2_DIMMB	CKE0	79	80	NC/CKE1	DDR_CKE3_DIMMB → DDR_CKE3_DIMMB 7
	VDD	81	82	VDD	
	NC	83	84	NC/A15	
8 DDR_B_BS#2 → DDR_B_BS#2	BA2	85	86	NC/A14	DDR_B_MA14 → DDR_B_MA14 7
	VDD	87	88	VDD	
DDR_B_MA12	A12	89	90	A11	DDR_B_MA11
DDR_B_MA9	A9	91	92	A7	DDR_B_MA7
DDR_B_MA8	A8	93	94	A6	DDR_B_MA6
	VDD	95	96	VDD	
DDR_B_MA5	A5	97	98	A4	DDR_B_MA4
DDR_B_MA3	A3	99	100	A2	DDR_B_MA2
DDR_B_MA1	A1	101	102	A0	DDR_B_MA0
	VDD	103	104	VDD	
DDR_B_MA10	A10/AP	105	106	BA1	DDR_B_BS#1 → DDR_B_BS#1 8
8 DDR_B_BS#0 → DDR_B_BS#0	BA0	107	108	RAS#	DDR_B_RAS# → DDR_B_RAS# 8
8 DDR_B_WE# → DDR_B_WE#	WE#	109	110	S0#	DDR_CS2_DIMMB# → DDR_CS2_DIMMB# 7
	VDD	111	112	VDD	
8 DDR_B_CAS# → DDR_B_CAS#	CAS#	113	114	ODT0	M_ODT2 → M_ODT2 7
7 DDR_CS3_DIMMB# → DDR_CS3_DIMMB#	NC/S1#	115	116	NC/A13	DDR_B_MA13
	VDD	117	118	VDD	
7 M_ODT3 → M_ODT3	NC/ODT1	119	120	NC	
	VSS	121	122	VSS	
DDR_B_D32	DQ32	123	124	DQ36	DDR_B_D36
DDR_B_D33	DQ33	125	126	DQ37	DDR_B_D37
	VSS	127	128	VSS	
DDR_B_DQS#4	DQS4#	129	130	DM4	DDR_B_DM4
DDR_B_DQS4	DQS4	131	132	VSS	
	VSS	133	134	DQ38	DDR_B_D39
DDR_B_D34	DQ34	135	136	DQ39	DDR_B_D38
DDR_B_D35	DQ35	137	138	VSS	
	VSS	139	140	DQ44	DDR_B_D44
DDR_B_D40	DQ40	141	142	DQ45	DDR_B_D45
DDR_B_D41	DQ41	143	144	VSS	
	VSS	145	146	DQS5#	DDR_B_DQS#5
DDR_B_DM5	DM5	147	148	DQS5	DDR_B_DQS5
	VSS	149	150	VSS	
DDR_B_D42	DQ42	151	152	DQ46	DDR_B_D46
DDR_B_D43	DQ43	153	154	DQ47	DDR_B_D47
	VSS	155	156	VSS	
DDR_B_D48	DQ48	157	158	DQ52	DDR_B_D52
DDR_B_D49	DQ49	159	160	DQ53	DDR_B_D53
	VSS	161	162	VSS	
	NC,TEST	163	164	CK1	M_CLK_DDR3 → M_CLK_DDR3 7
	VSS	165	166	CK1#	M_CLK_DDR#3 → M_CLK_DDR#3 7
DDR_B_DQS#6	DQS6#	167	168	VSS	
DDR_B_DQS6	DQS6	169	170	DM6	DDR_B_DM6
	VSS	171	172	VSS	
DDR_B_D51	DQ50	173	174	DQ54	DDR_B_D54
DDR_B_D50	DQ51	175	176	DQ55	DDR_B_D55
	VSS	177	178	VSS	
DDR_B_D56	DQ56	179	180	DQ60	DDR_B_D60
DDR_B_D61	DQ57	181	182	DQ61	DDR_B_D57
	VSS	183	184	VSS	
DDR_B_DM7	DM7	185	186	DQS7#	DDR_B_DQS#7
	VSS	187	188	DQS7	DDR_B_DQS7
DDR_B_D59	DQ58	189	190	VSS	
DDR_B_D58	DQ59	191	192	DQ62	DDR_B_D62
	VSS	193	194	DQ63	DDR_B_D63
13,16,19,24 ICH_SM_DA → ICH_SM_DA	SDA	195	196	VSS	
13,16,19,24 ICH_SM_CLK → ICH_SM_CLK	SCL	197	198	SAO	
+3VSO	VDDSPD	199	200	SA1	R33 → +3VS

C61 0.1U_0402_16V4Z
C60 2.2U_0603_6.3V6K
R34 10K_0402_5%
R33 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **DDR2 SO-DIMM II**

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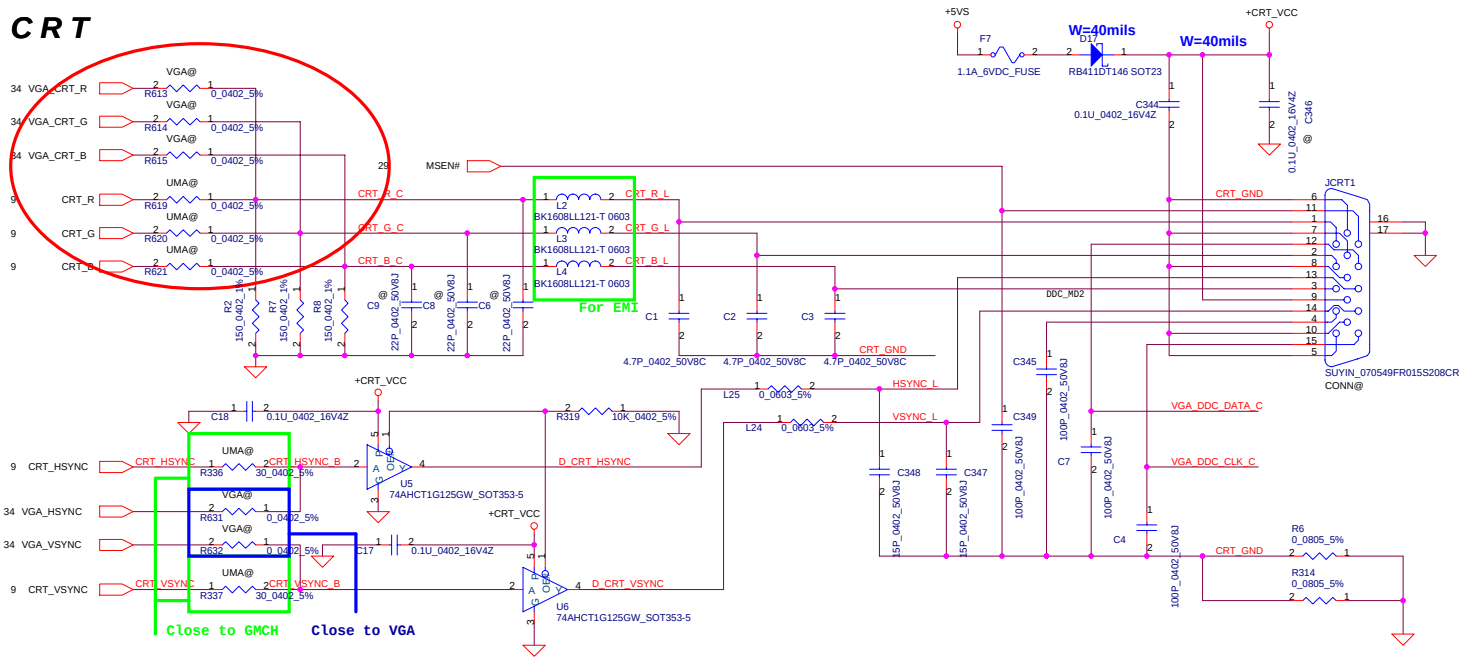
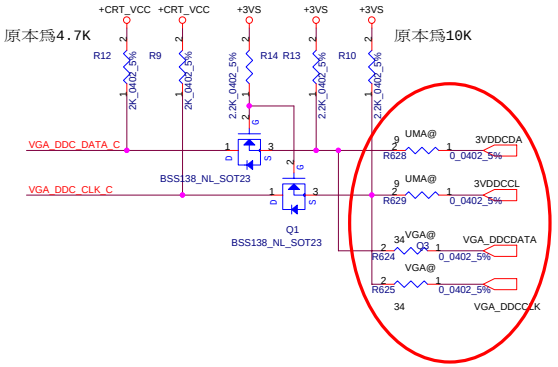
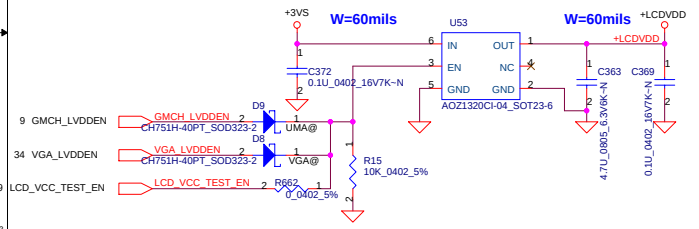
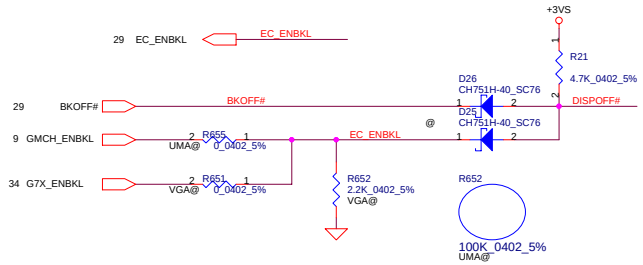
CRT

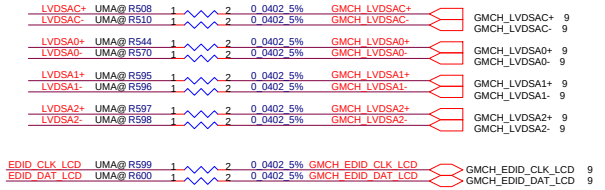


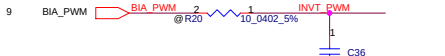


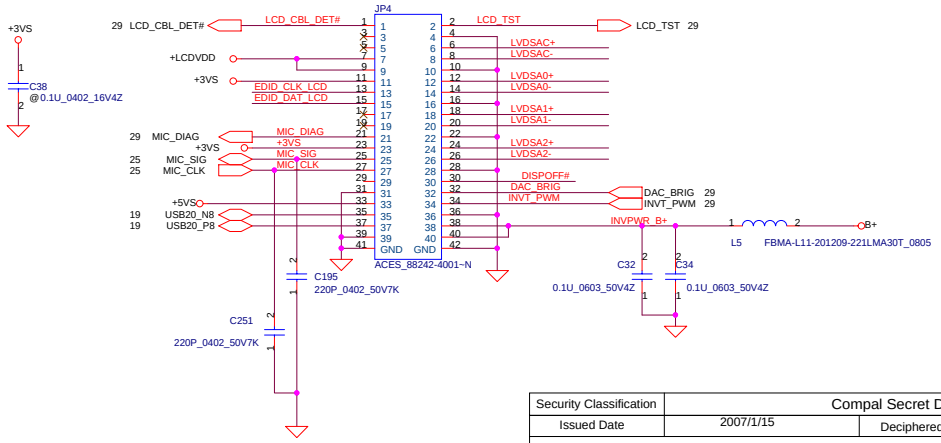
LCD

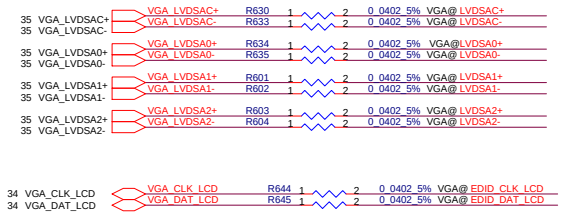












Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: CRT CONN/LCD CONN			
Size: Custom	Document Number: LA-4231P		Rev: 0.1
Date: Thursday, January 10, 2008		Sheet 15 of 49	

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

+3VM_CK505 — R397 0_1206_5% — +3VS

C479 10U_0805_10V4Z~N; C480, C478, C476, C464, C463, C460 0.1U_0402_16V4Z~N

+1.25VS — R261 0_1206_5% — +1.25VM_CK505

Place close to U7

C459 22U_0805_6.3V4Z; C462, C461, C474, C477, C475, C473 0.1U_0402_16V4Z~N; 22U_0805_6.3V4Z

R402 2.2K_0402_5% — FSA — MCH_CLKSEL0 7

5 CPU_BSEL0 — R410 0_0402_5% — R411 1K_0402_5%

+VCCP — R379 1K_0402_5%

FSB — MCH_CLKSEL1 7

5 CPU_BSEL1 — @R378 0_0402_5% — R377 1K_0402_5%

R200 10K_0402_5% — FSC — MCH_CLKSEL2 7

5 CPU_BSEL2 — @R184 0_0402_5% — R185 1K_0402_5%

R199 0_0402_5%

U7

2	VDDPCI	NC	48
9	VDD48		
16	VDDPLL3		
61	VDDREF		
39	VDDSRC	SCLK	64
55	VDDCPU	SDATA	63
		PCI_STOP#	38
		CPU_STOP#	37
12	VDD96_IO		
20	VDDPLL3_IO		
26	VDDSRC_IO		
36	VDDSRC_IO		
49	VDDCPU_IO		
1	PCI0/CR#_A	SATA_REQ	
3	PCI1/CR#_B	MCH_REQ	
4	PCI2/TME	PCI2_TME	
5	PCI3	PCI_CLK3	
6	PCI4/27_Select	27_SEL	
7	PCI_F5/ITP_EN	ITP_EN	
60	X1	CLK_XTAL_IN	
59	X2	CLK_XTAL_OUT	
10	USB_48MHZ/FSLA	FSA	
57	FSLB/TEST_MODE	FSB	
62	REF0/FSLC/TEST_SEL	FSC	
45	VDDSRC_IO		
42	GNDSRC		
8	GNDPCI		
11	GND48		
15	GND		
19	GND		
52	GNDCPU		
23	GNDSRC		
29	GNDSRC		
58	GNDREF		

ICS9LPRS365BGLFT_TSSOP64

ICH_SM_CLK 13,14,19,24 — ICH_SM_DA 13,14,19,24

H_STP_PCI# 19 — H_STP_CPU# 19

R202 — CPU0 R_CPU_BCLK — CLK_CPU_BCLK 4; CPU0# R_CPU_BCLK# — CLK_CPU_BCLK# 4 — R203

R204 — CPU1_F R_MCH_BCLK — CLK_MCH_BCLK 7; CPU1#_F R_MCH_BCLK# — CLK_MCH_BCLK# 7 — R205

R208 — SRC8/CPU2_ITP R_PCIE_LAN — CLK_PCIE_LAN 22; SRC8#/CPU2_ITP# R_PCIE_LAN# — CLK_PCIE_LAN# 22 — R209

R213 — SRC10 R_PCIE_EXPR — CLK_PCIE_EXPR 28; SRC10# R_PCIE_EXPR# — CLK_PCIE_EXPR# 28 — R212

R396 — SRC11/CR#_H R_CLKREQ#_H — EXPR_CARD_REQ# 28; SRC11#/CR#_G R_CLKREQ#_G — MCARD_REQ#G 24 — R375

R374 10K_0402_5% — +3VS; R395 10K_0402_5% — +3VS

R251 — SRC9 R_CLK_PCIE_MCard — CLK_PCIE_MCARD 24; SRC9# R_CLK_PCIE_MCard# — CLK_PCIE_MCARD# 24 — R252

R398 — SRC7/CR#_F R_CLKREQ#_F — MCARD_REQ#F 22; SRC7#/CR#_E R_CLKREQ#_E — MCARD_REQ#E 24 — R386

R385 10K_0402_5% — +3VS; R399 10K_0402_5% — +3VS

R210 — SRC6 R_CLK_Rob — CLK_PCIE_Rob 24; SRC6# R_CLK_Rob# — CLK_PCIE_Rob# 24 — R211

SRC4 R_MCH_3GPLL — CLK_MCH_3GPLL 7; SRC4# R_MCH_3GPLL# — CLK_MCH_3GPLL# 7

R247 — SRC3/CR#_C R_PCIE_ICH — CLK_PCIE_ICH 19; SRC3#/CR#_D R_PCIE_ICH# — CLK_PCIE_ICH# 19 — R248

SRC2/SATA R_PCIE_SATA — CLK_PCIE_SATA 18; SRC2#/SATA# R_PCIE_SATA# — CLK_PCIE_SATA# 18

R243 — SRC1/SE1/27MHz_NonSS SSCDREFCLK — UMA@0_0402_5% — MCH_SSCDREFCLK 7; SRC1#/SE2/27MHz_SS SSCDREFCLK# — UMA@0_0402_5% — MCH_SSCDREFCLK# 7 — R244

R241 — SRC0/DOT96 R_MCH_DREFCLK — UMA@0_0402_5% — CLK_MCH_DREFCLK 7; SRC0#/DOT96# R_MCH_DREFCLK# — UMA@0_0402_5% — CLK_MCH_DREFCLK# 7 — R242

R344 — VGA@0_0402_5% — CLK_PCIE_VGA 34; R493 — VGA@0_0402_5% — CLK_PCIE_VGA# 34

CK_PWRGD/PD# — CK_PWRGD 19

@R376 — 0_0402_5% — CLK_EN# 49

+3VM_CK505 — R235 10K_0402_5% — +3VS; R234 10K_0402_5% — +3VS

19 CLKSATAREQ# — 475_0402_1% — R237 — SATA_REQ

7 CLKMCHREQ# — 475_0402_1% — R233 — MCH_REQ

40 CLK_PCI_CB — 33_0402_5% — R257 — PCI2_TME

29 CLK_PCI_TPM — 12_0402_5% — R239

24 CLK_DEBUG_PORT — 12_0402_5% — R258 — PCI_CLK3

29 CLK_PCI_EC — 33_0402_5% — R259 — 27_SEL

17 CLK_PCI_ICH — 33_0402_5% — R260 — ITP_EN

19 CLK_48M_ICH — 33_0402_5% — R401 — FSA

19 CLK_14M_ICH — 33_0402_1% — R201 — FSC

+1.25VM_CK505

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

CLK_XTAL_OUT — CLK_XTAL_IN — 14.31818MHZ_16P — Y3

C265 18P_0402_50V8J~N; C257 18P_0402_50V8J~N

Placed within 500 mils of CK505M

Routing the trace at least 10mil

+3VM_CK505 — R492 10K_0402_5% VGA@ — 27_SEL — R268 10K_0402_5% UMA@

+3VM_CK505 — R236 10K_0402_5% — PCI2_TME — R238 10K_0402_5% @

ITP_EN — R240 10K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Clock generator

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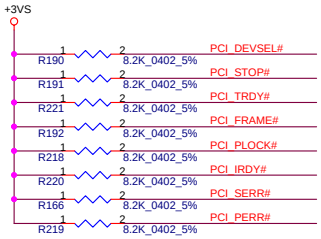
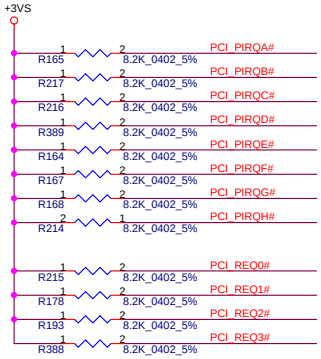
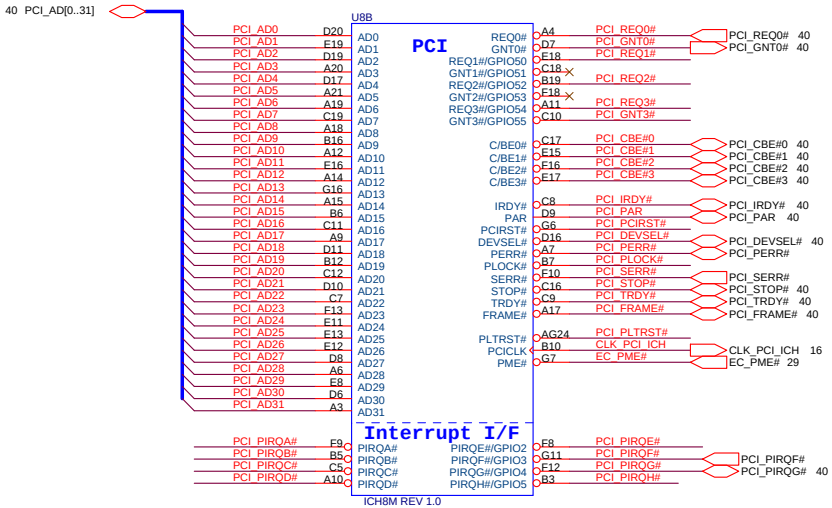
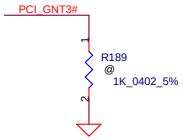




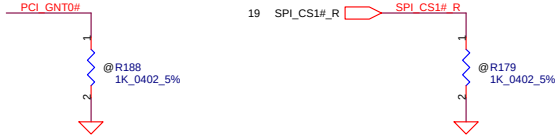


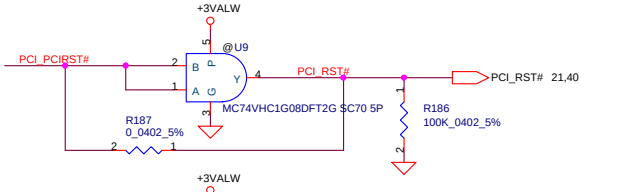


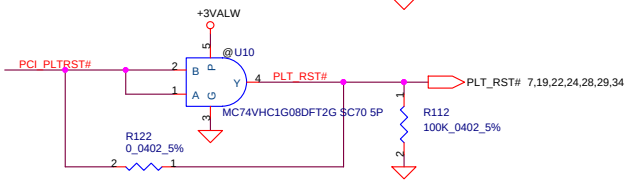
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

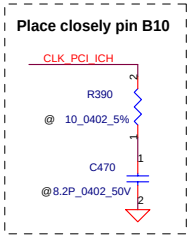
Check if use LPC?

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *









Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

Size	Document Number	Rev
Custom	LA-4231P	0.1

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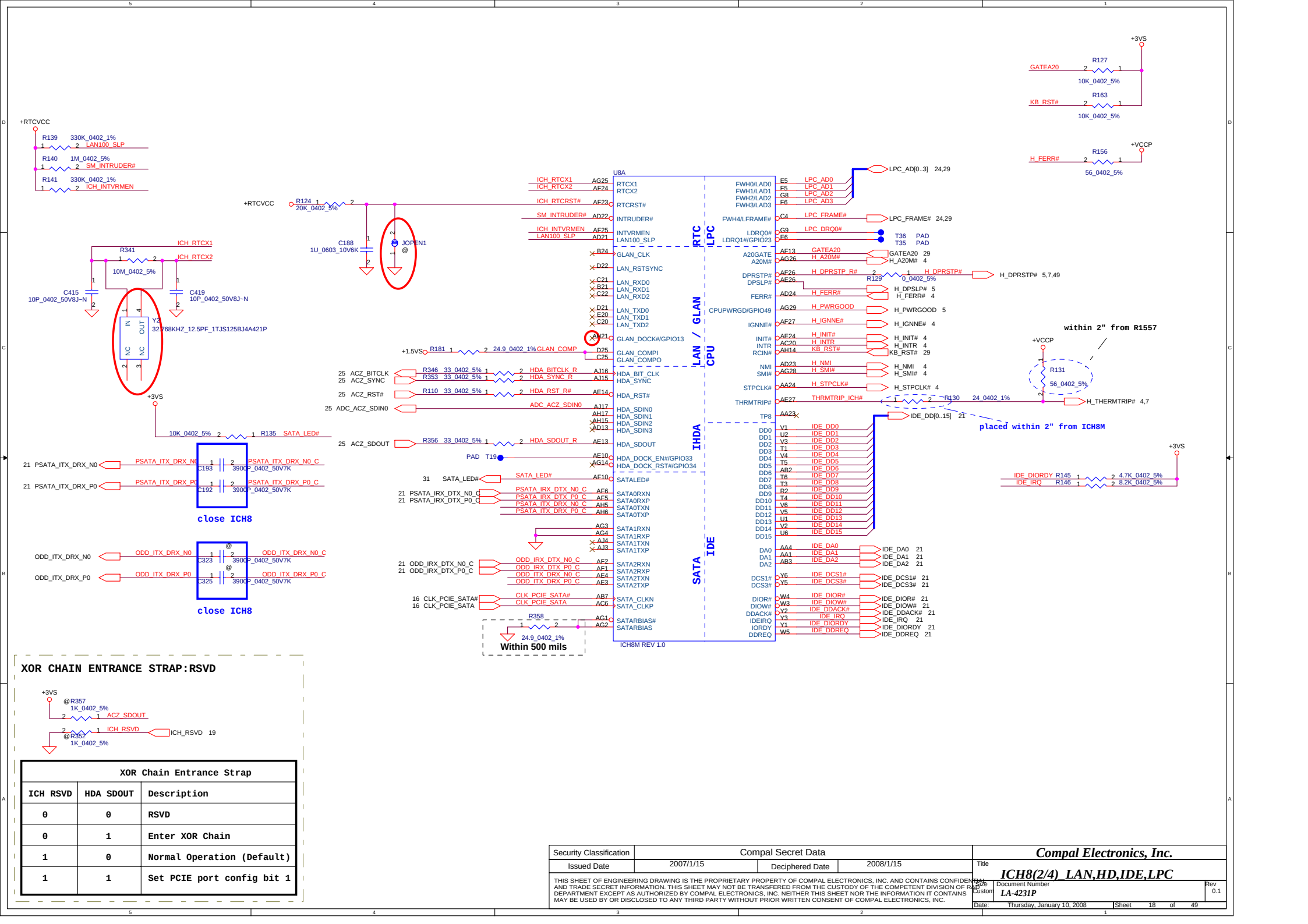

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(2/4)_LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-4231P | Rev: 0.1

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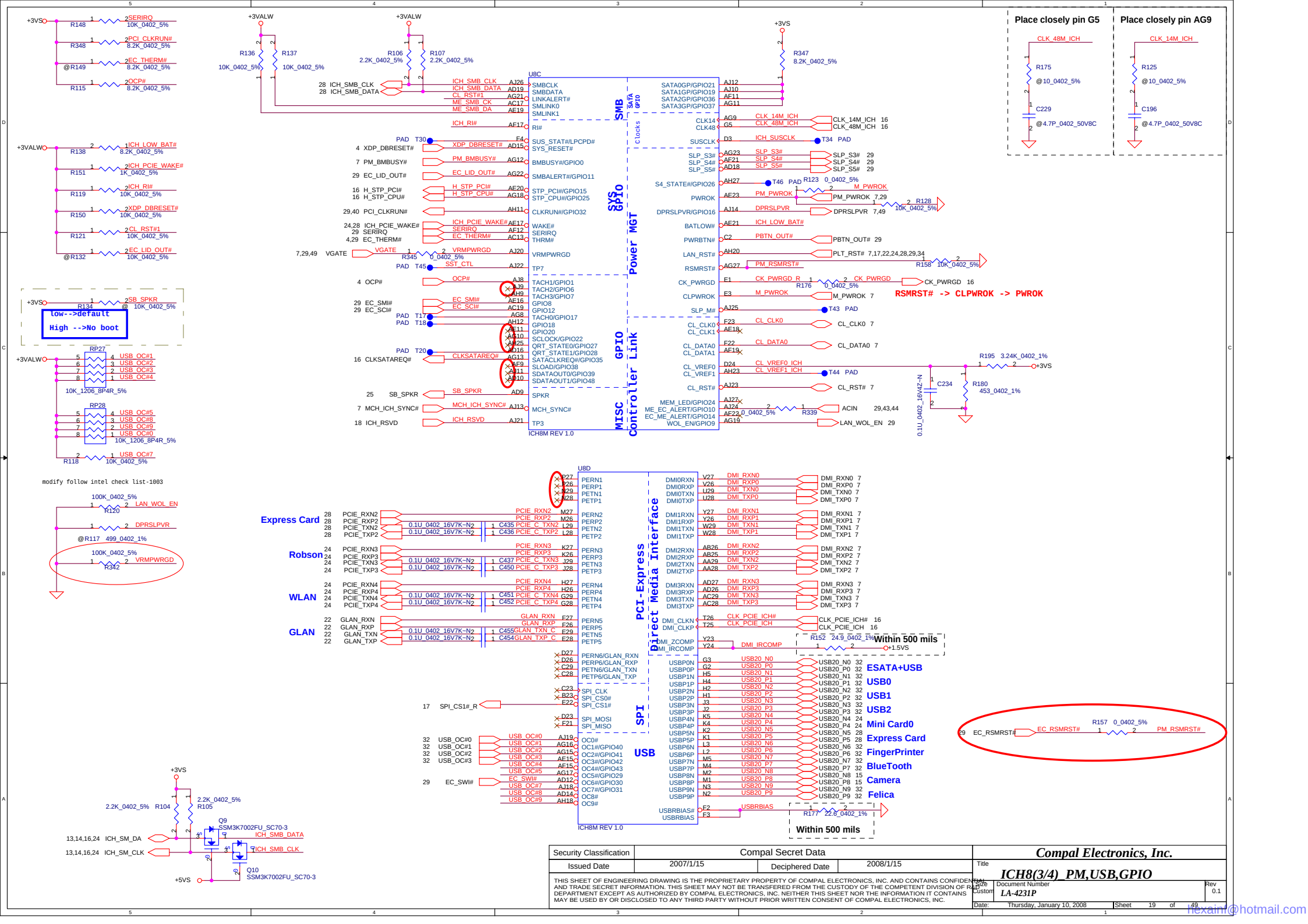

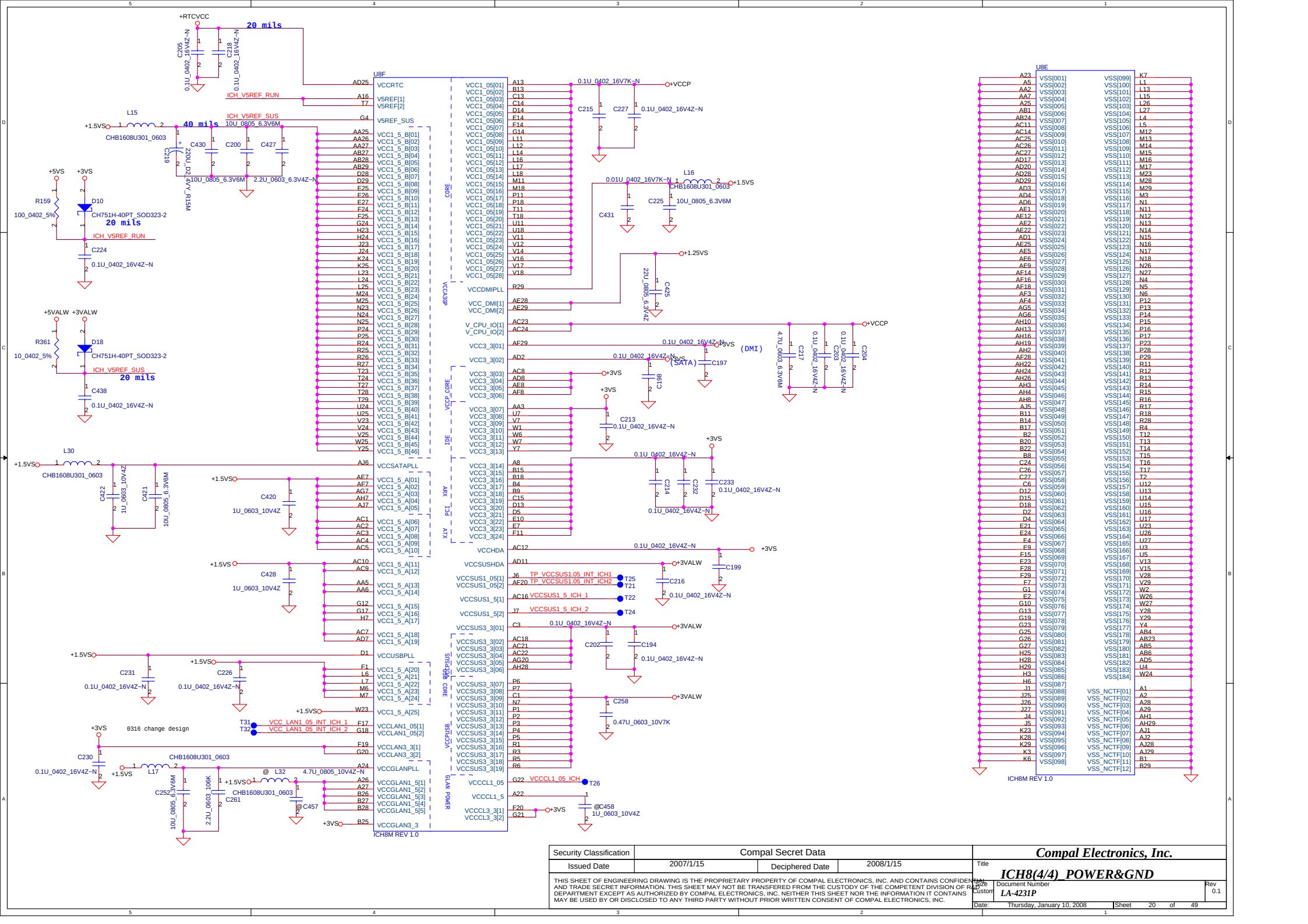

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **ICH8(4/4)_POWER&GND**

Size	Document Number	Rev
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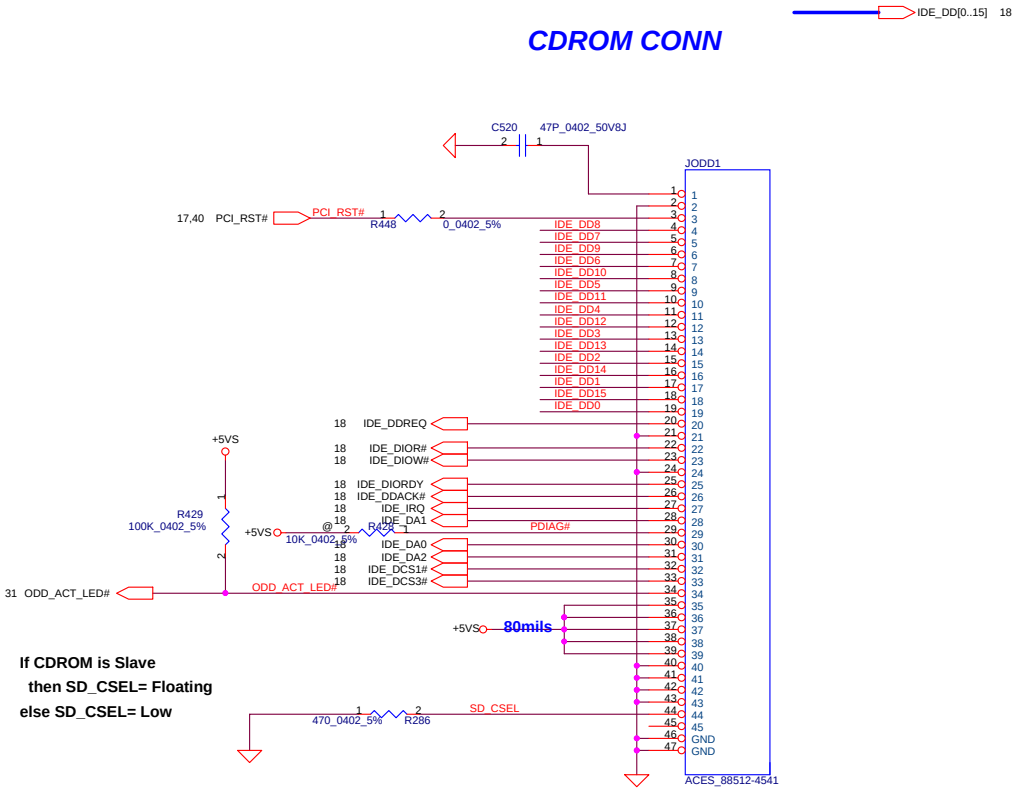
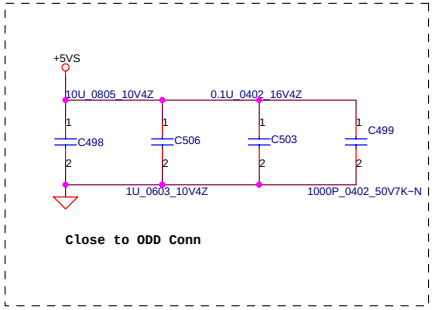
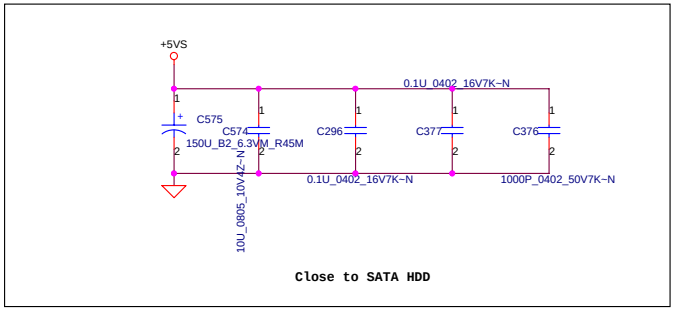
CDROM CONN

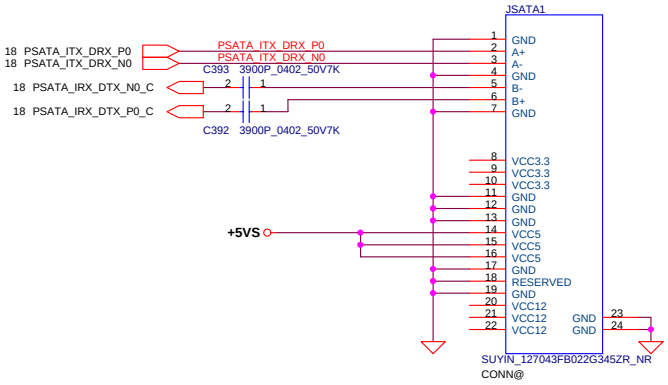


If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low

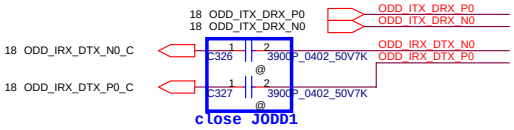




SATA HDD CONN

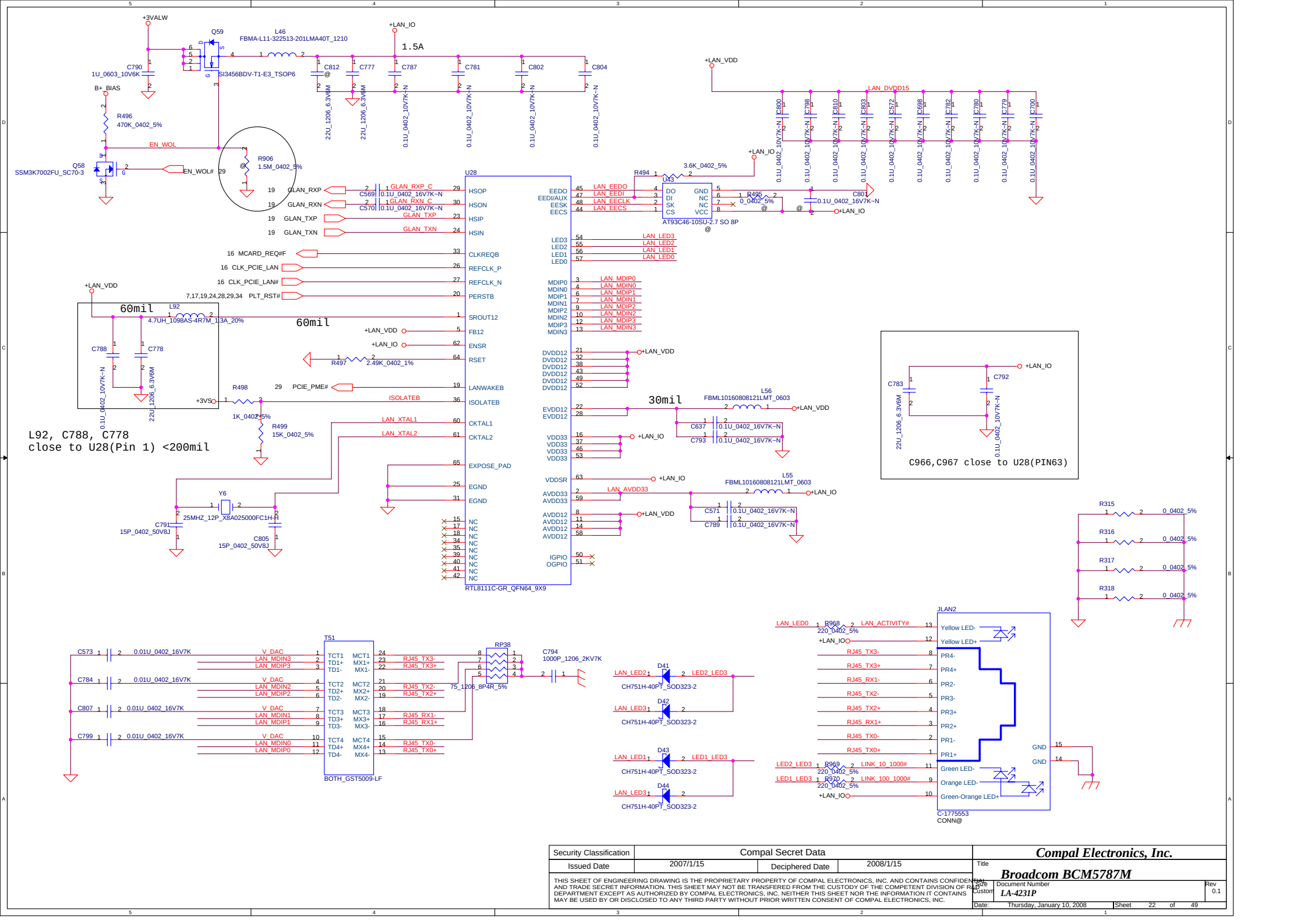


RESERVE(SATA ODD NET)



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title	HDD/CDROM		
Size: Custom	Document Number: LA-4231P		Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 21 of 49		



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Broadcom BCM5787M**

Size	Document Number	Rev
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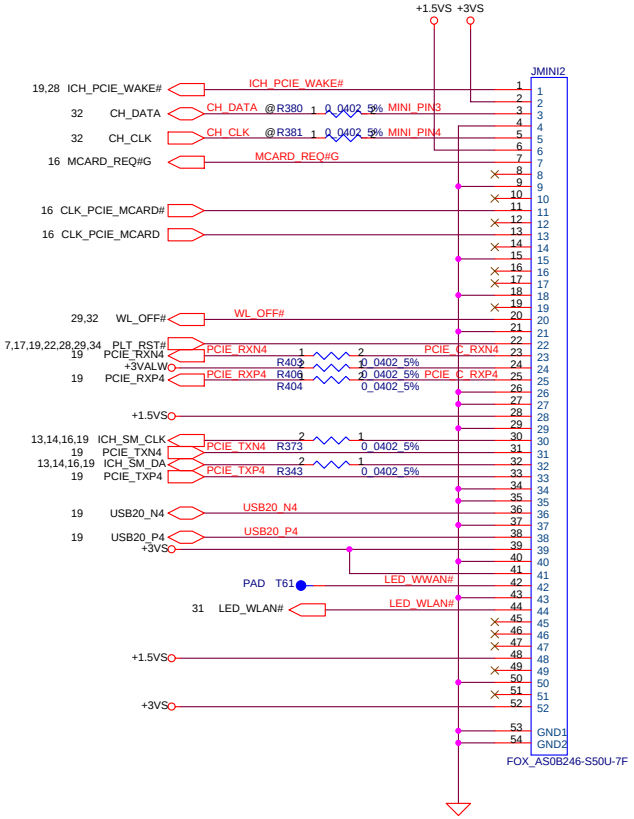
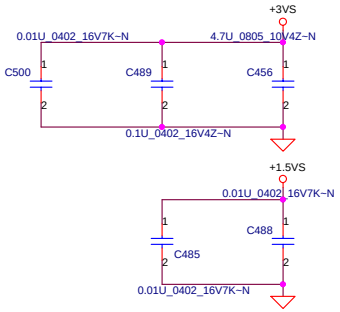
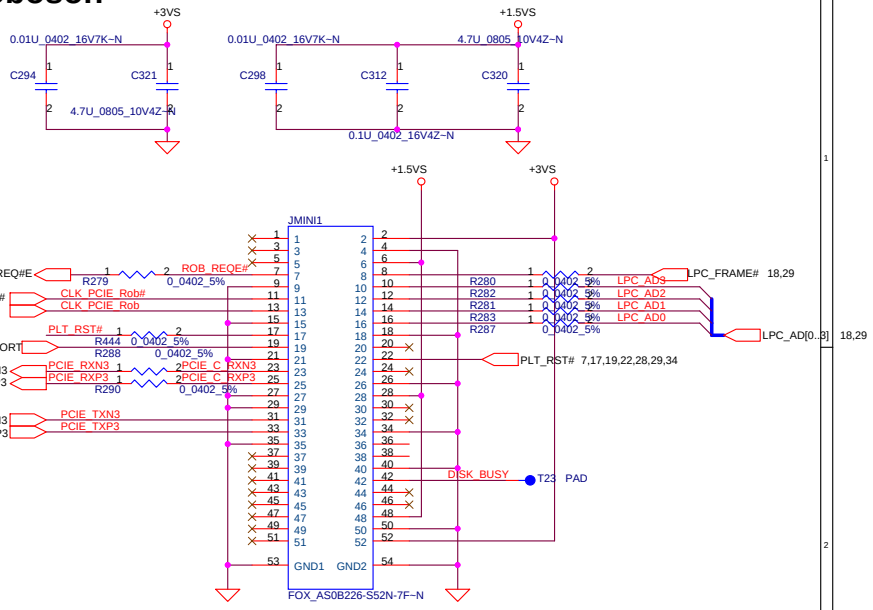
Mini-Express Card---WLAN

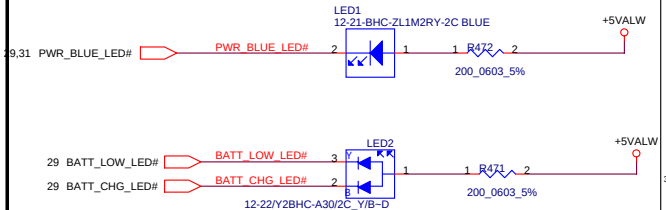




Roboson



Power status(Left)



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

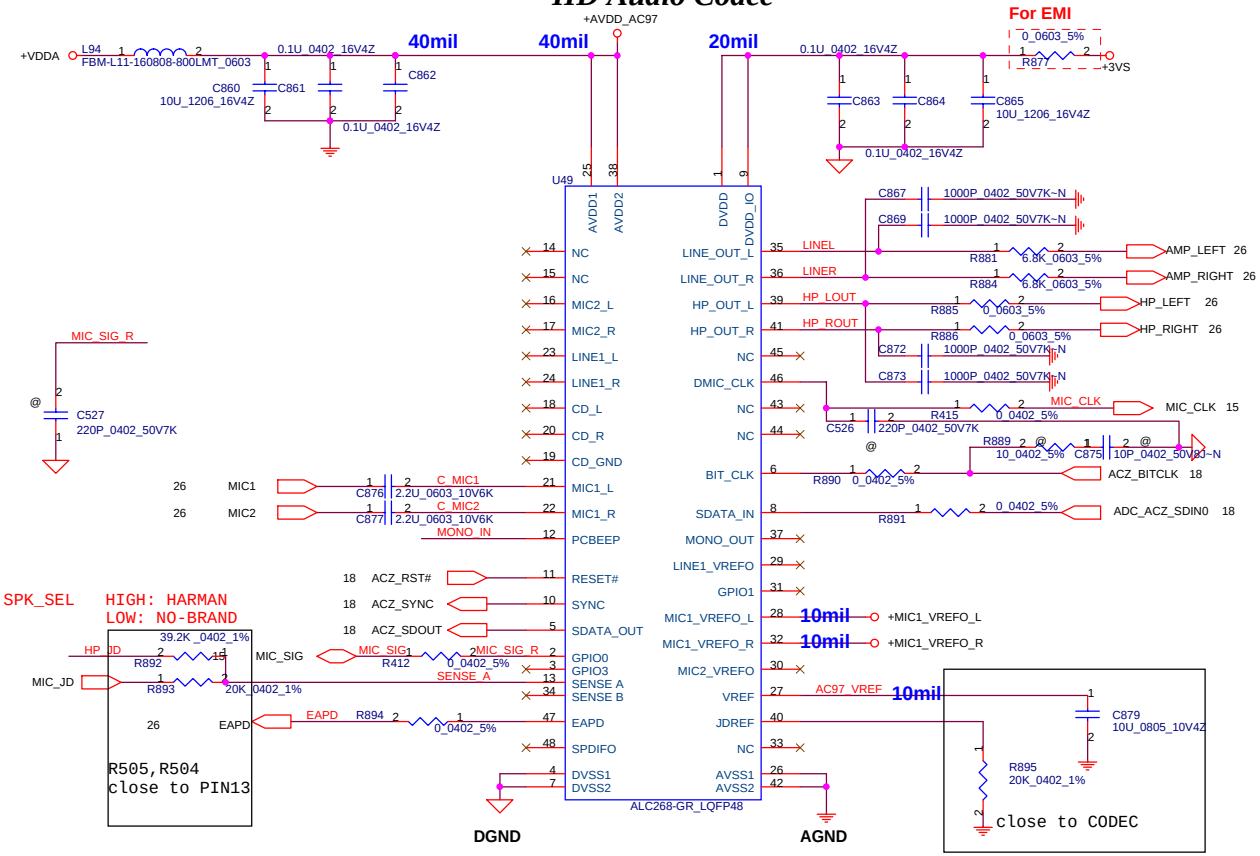
Compal Electronics, Inc.

Title: **Mini-Card/LED**

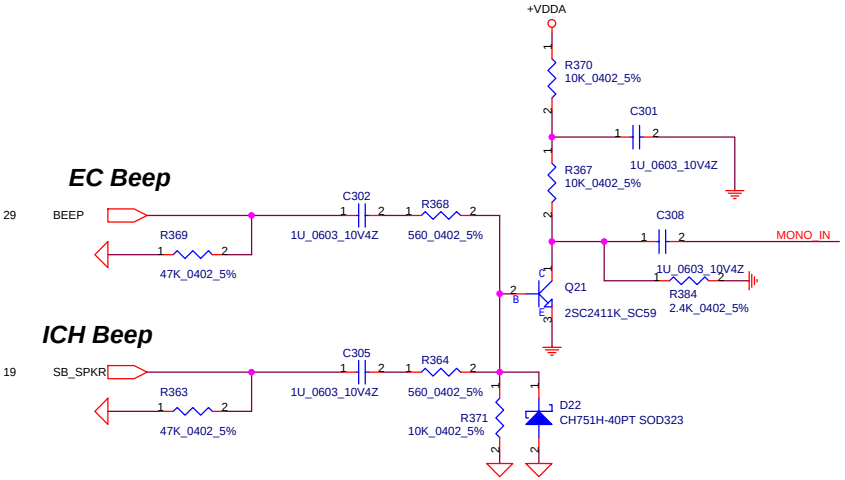
Size	Document Number	Rev
Custom	LA-4231P	0.1

Date: Thursday, January 10, 2008 Sheet 24 of 49

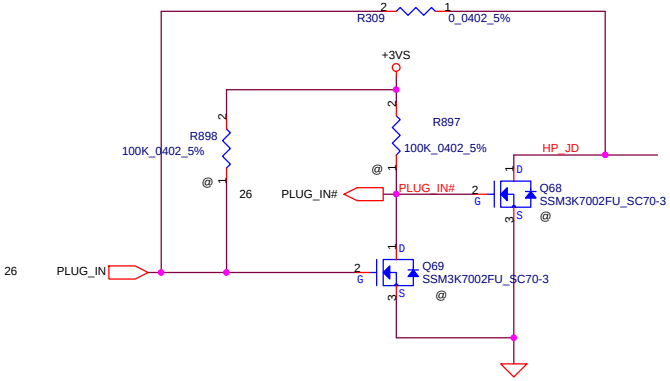
HD Audio Codec



EC Beep

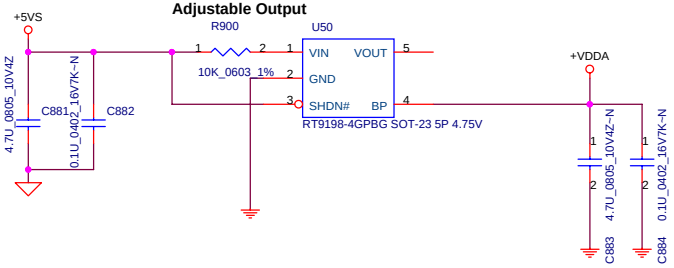


ICH Beep

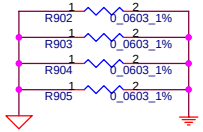


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Regulator for CODEC



Moat Bridge



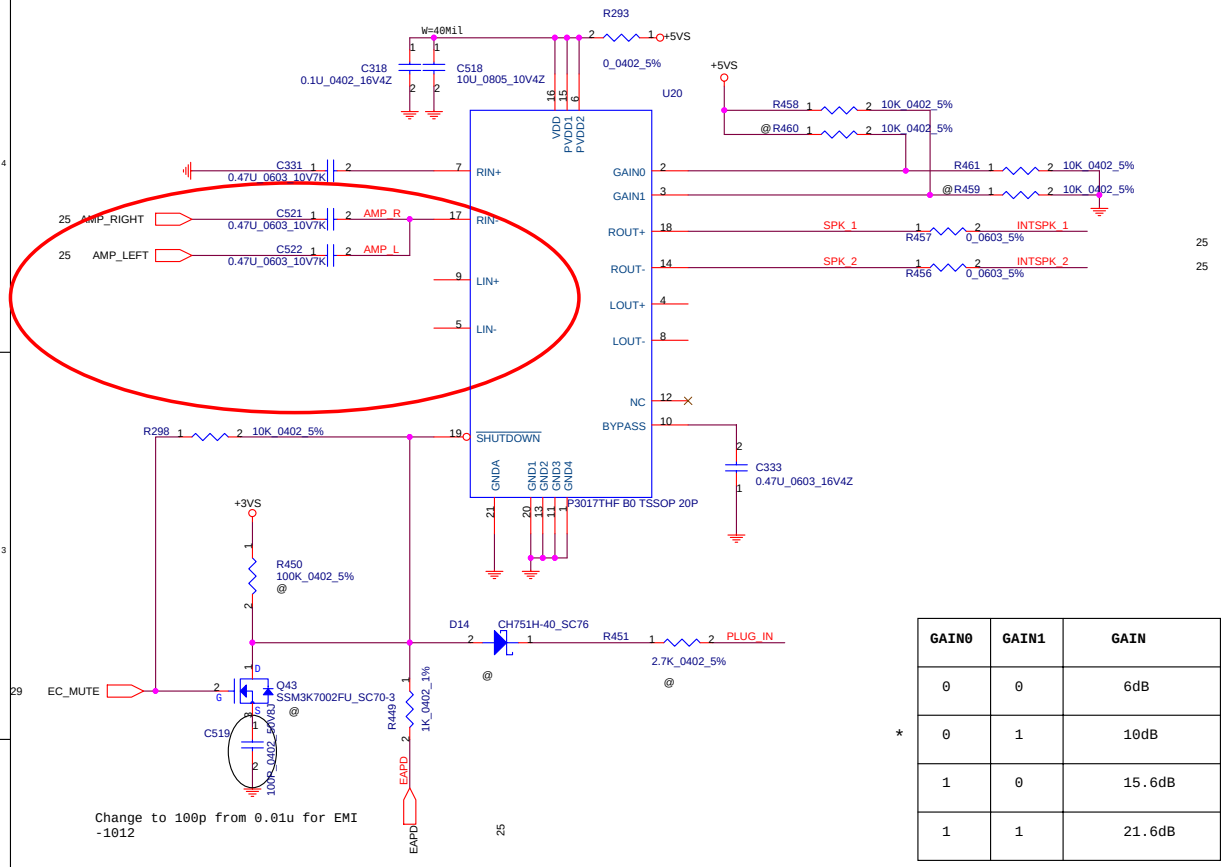
Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

Compal Electronics, Inc.

Title: **HD Audio Codec_ALC268**

Size	Document Number	Rev
	LA-4231P	1.0

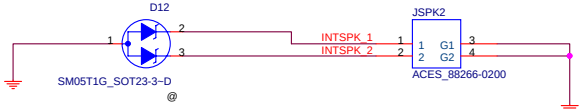
Date: Thursday, January 10, 2008 | Sheet 25 of 49



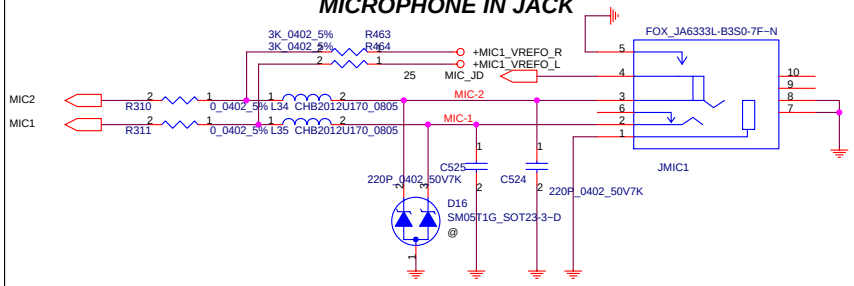
GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

*

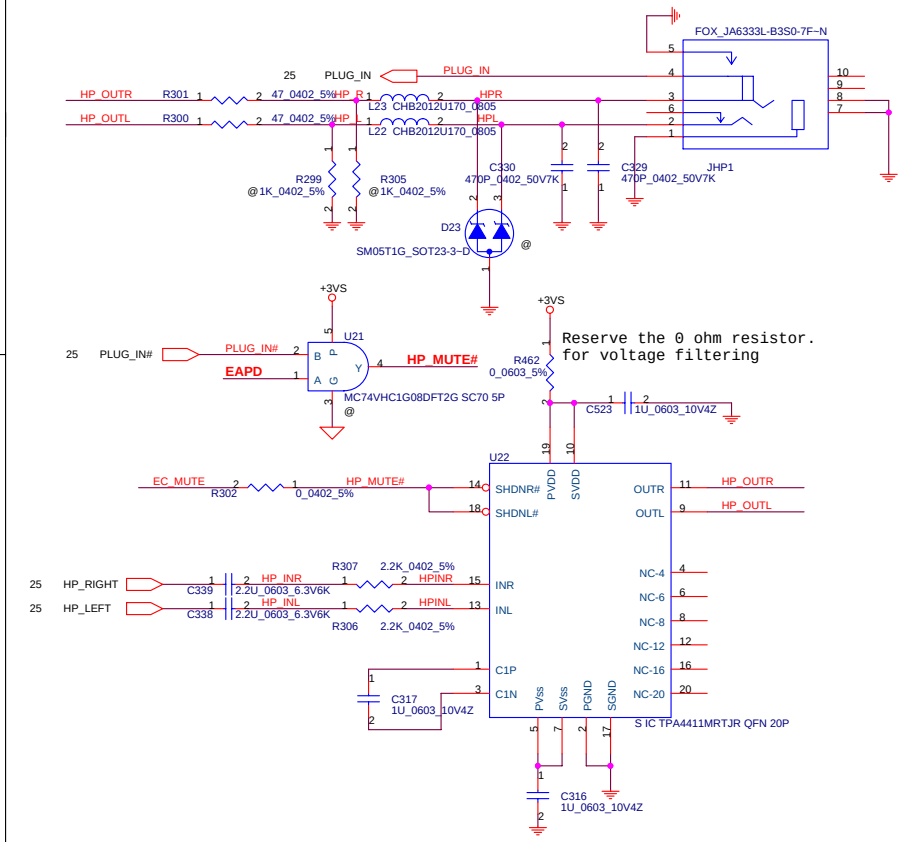
Speaker Connector



MICROPHONE IN JACK



HEADPHONE OUT JACK



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

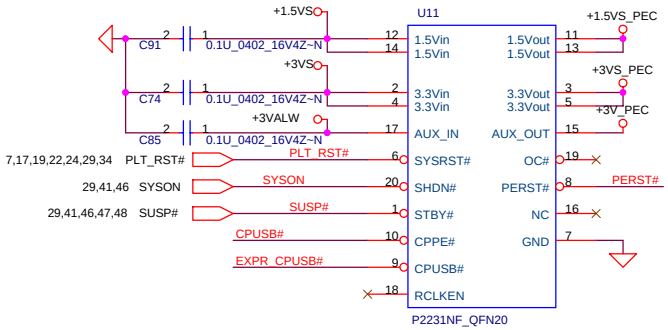
Title: **AMP/Audio Jack**

Size	Document Number	Rev
Custom	LA-4231P	0.1

Date: Thursday, January 10, 2008 Sheet 26 of 49

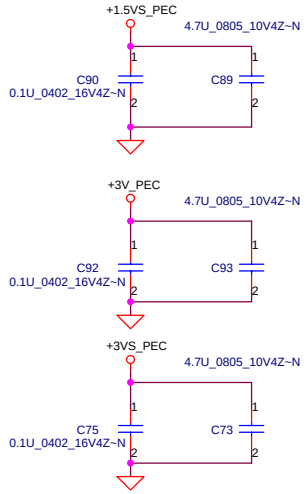
Express card

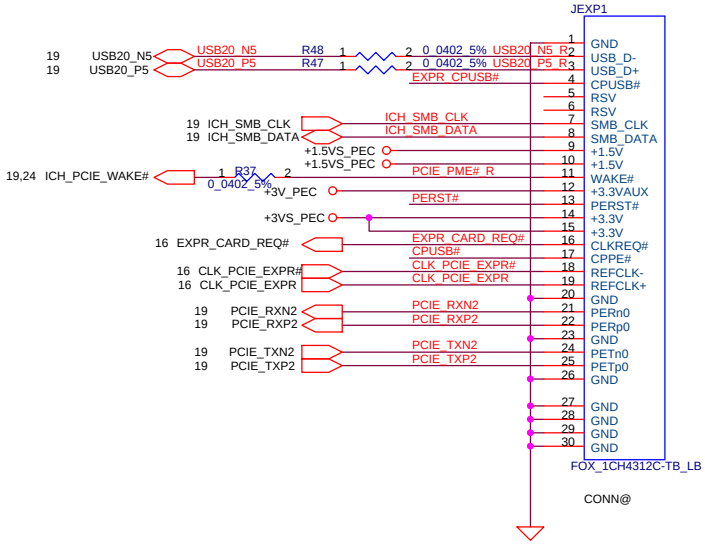
Express Card Power Switch



+1.5V_CARD Max. 650mA, Average 500mA

+3V_CARD Max. 1300mA, Average 1000mA



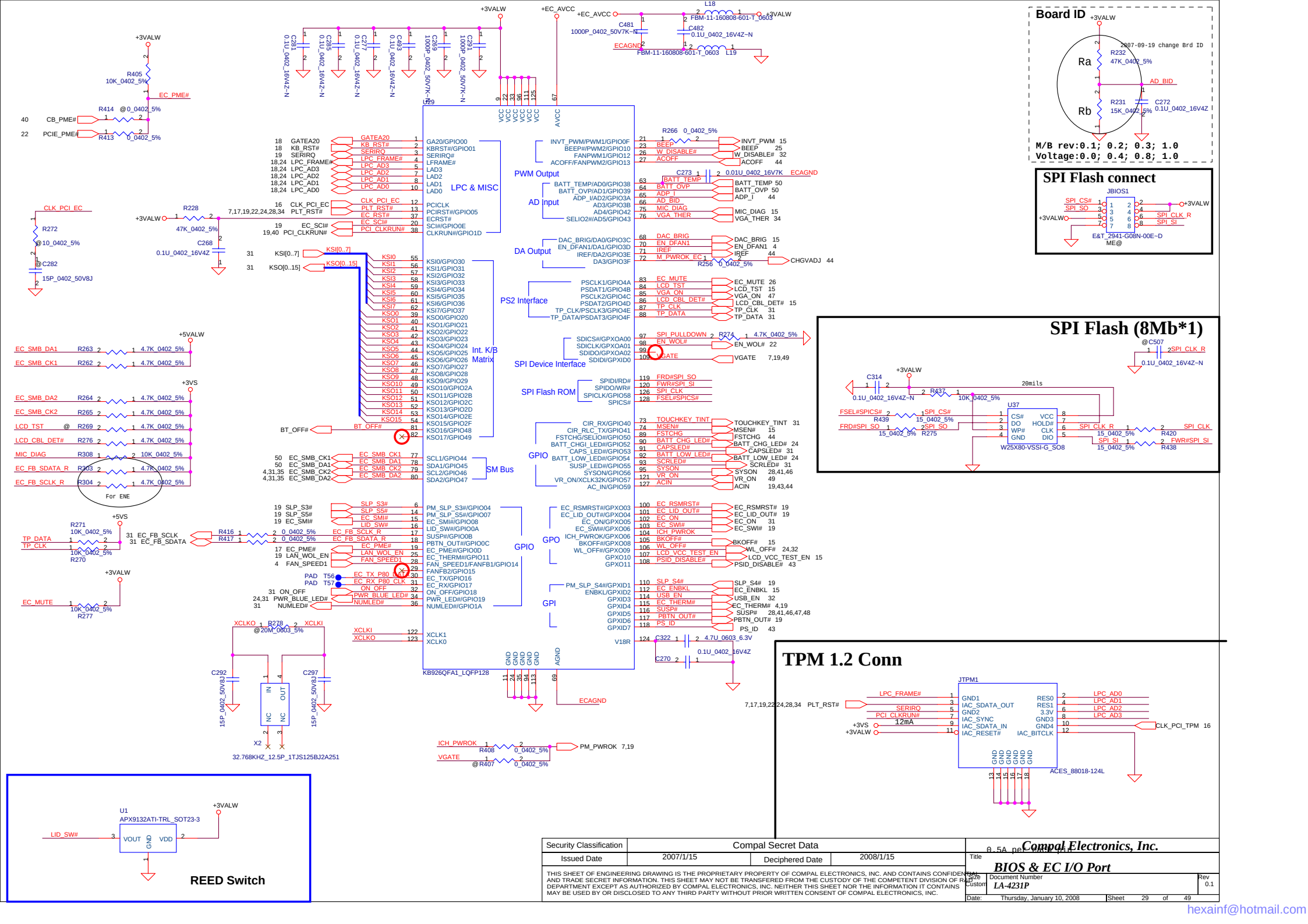


Compal Electronics, Inc.

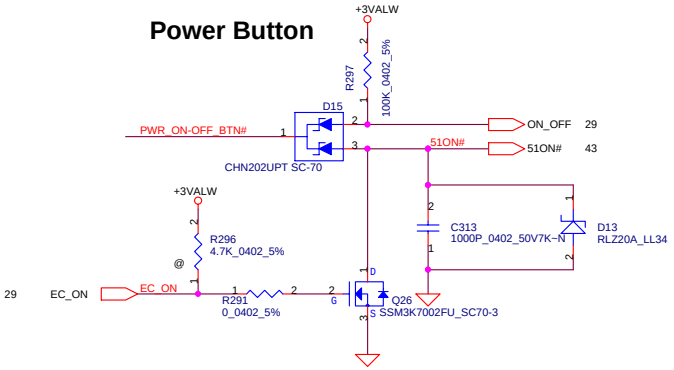
Title: **EXPRESS CARD**

Size	Document Number	Rev
Custom	LA-4231P	0.1

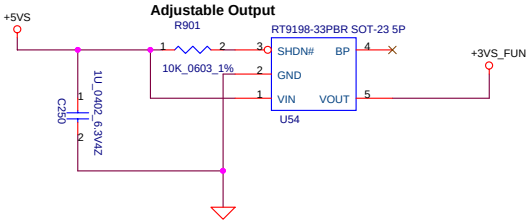
Date: Thursday, January 10, 2008 Sheet 28 of 49



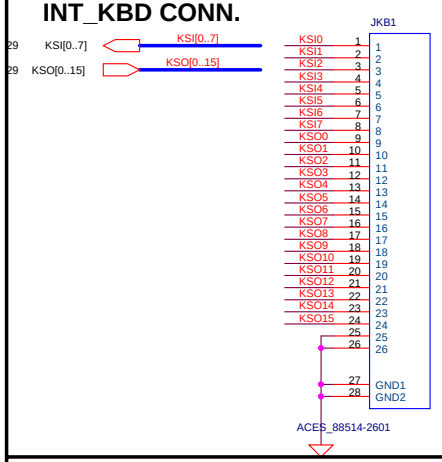
Power Button

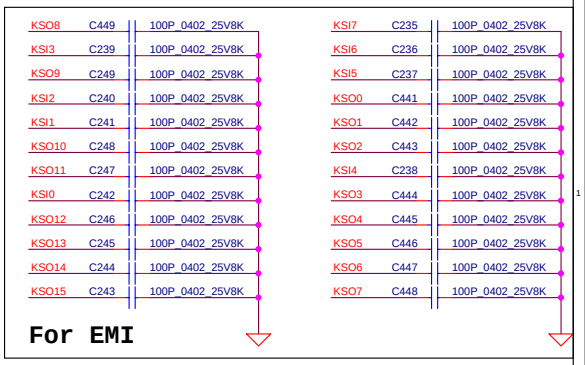


Regulator for ENE sensor

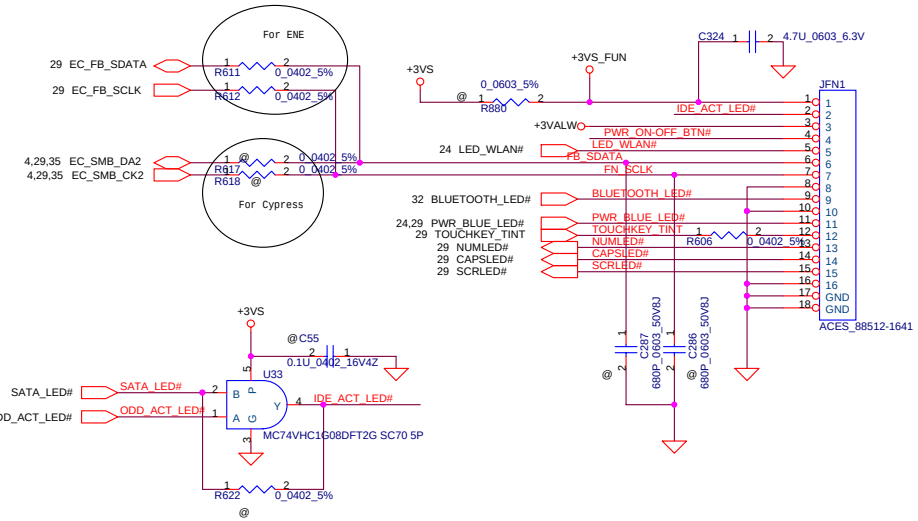


INT_KBD CONN.

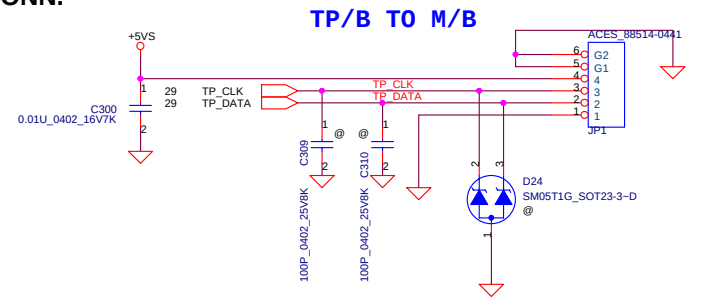




Function/B CONN.



Touch PAD/B CONN.



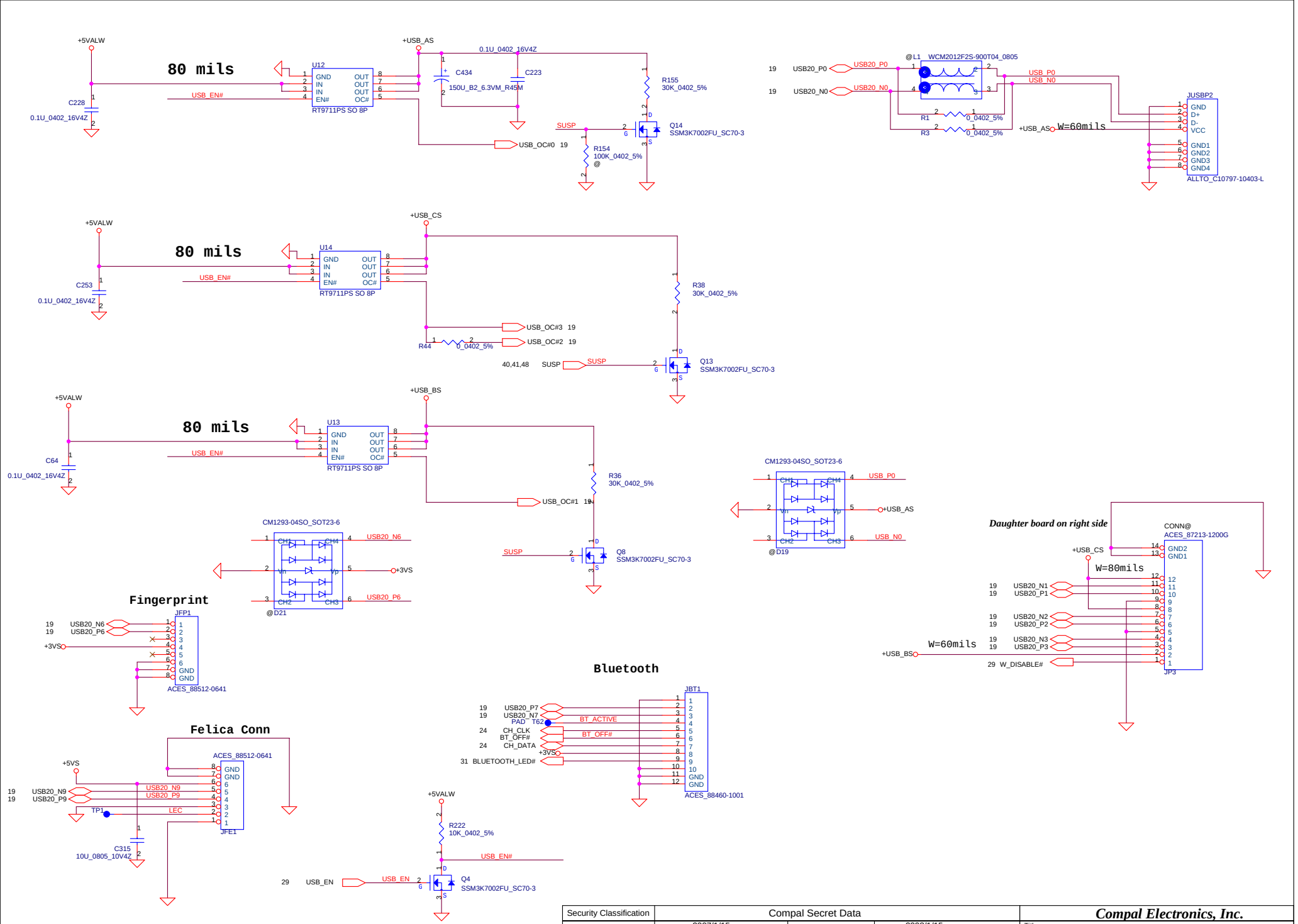
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ***PWR_OK/BTN/TP***

Size	Document Number	Rev
Custom	*LA-4231P*	0.1

Date: Thursday, January 10, 2008 Sheet 31 of 49



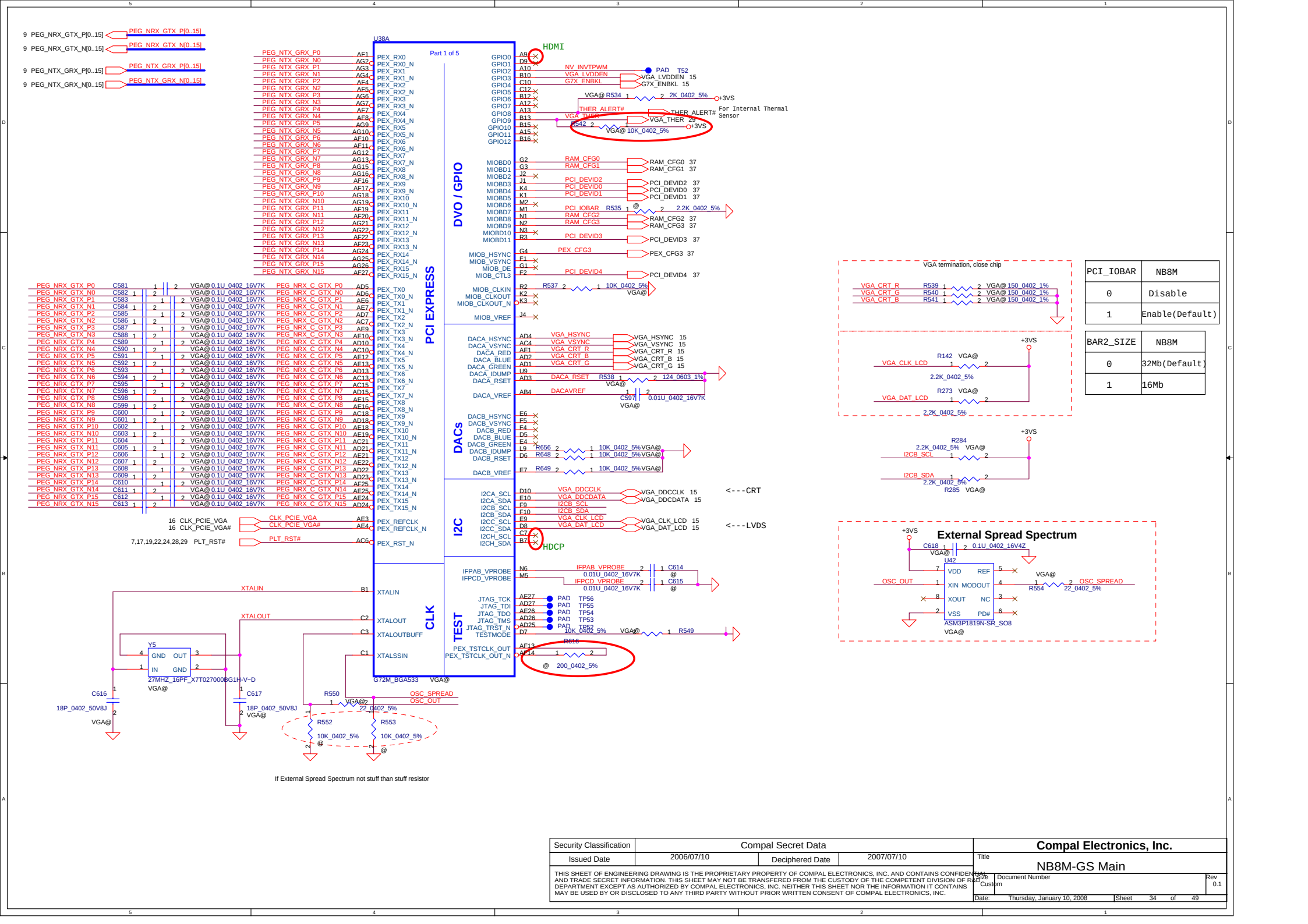
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **USB/BlueTooth/FP/Felcia**

Size	Document Number	Rev
Custom	LA-4231P	0.1

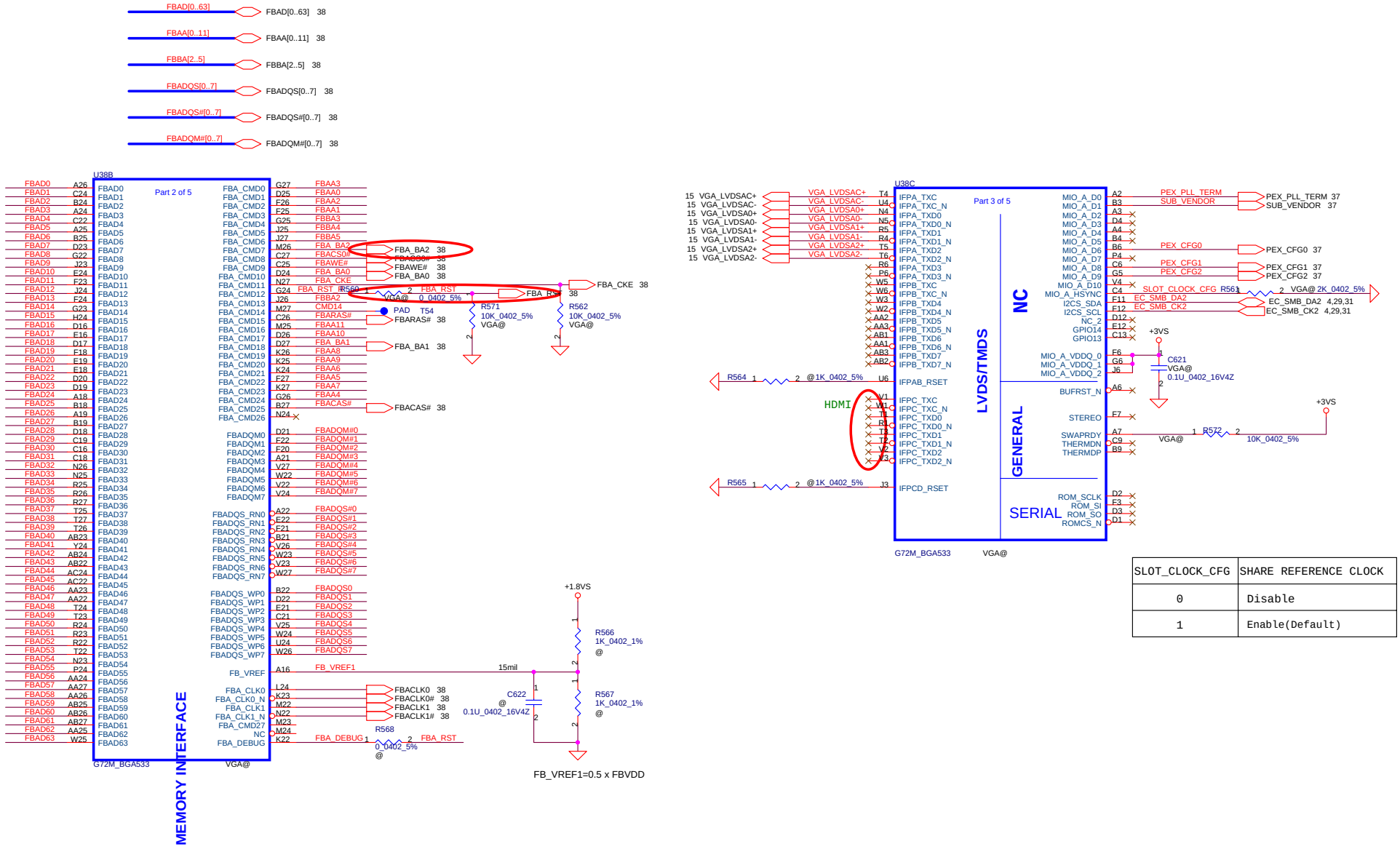
Date: Thursday, January 10, 2008 | Sheet 32 of 49



PCI_IOBAR	NB8M
0	Disable
1	Enable(Default)

BAR2_SIZE	NB8M
0	32Mb(Default)
1	16Mb

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/07/10	Deciphered Date	2007/07/10
Title	NB8M-GS Main		
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 34 of 49		



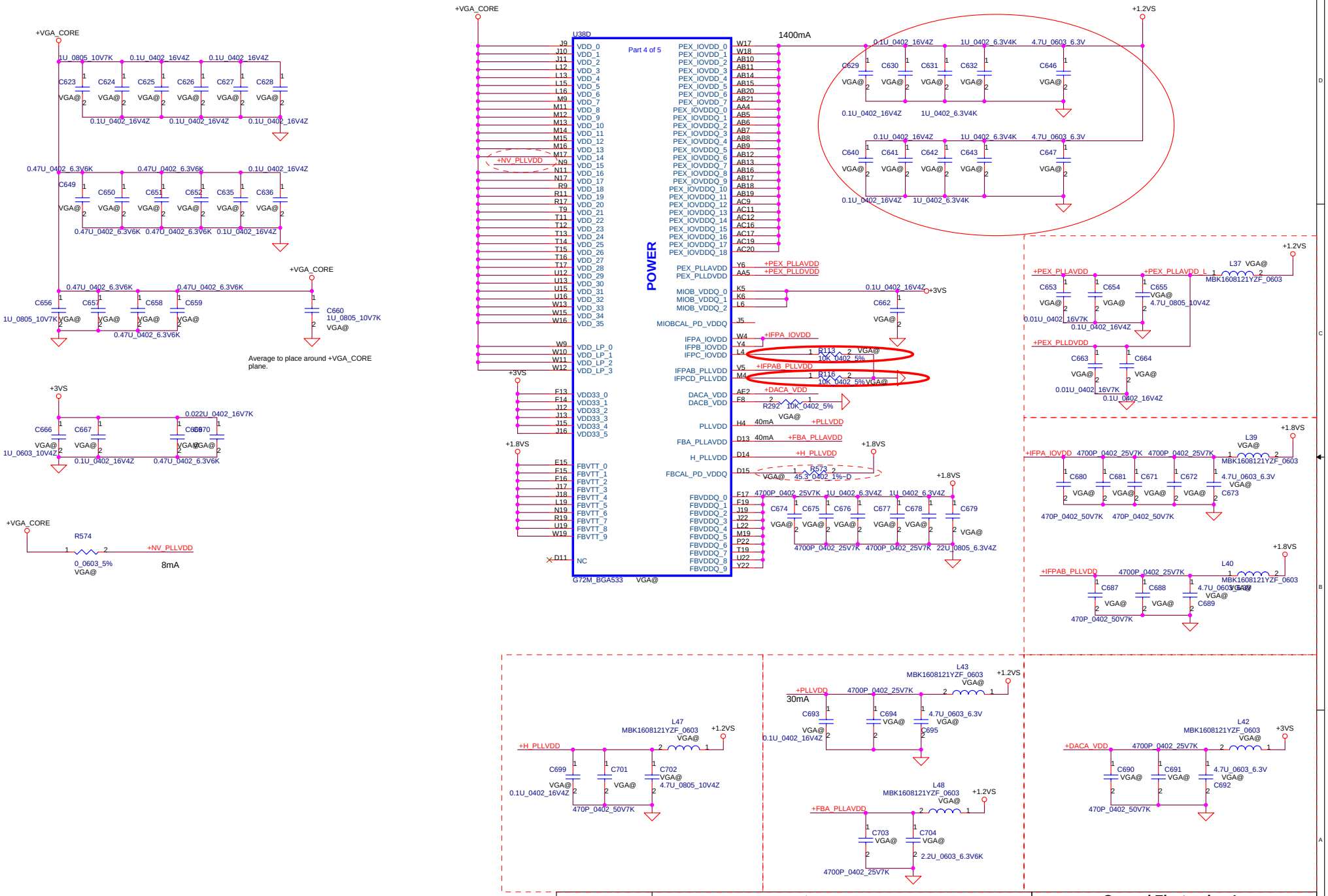
SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)

Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Memory

Size: Custom	Document Number	Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 35 of 49	



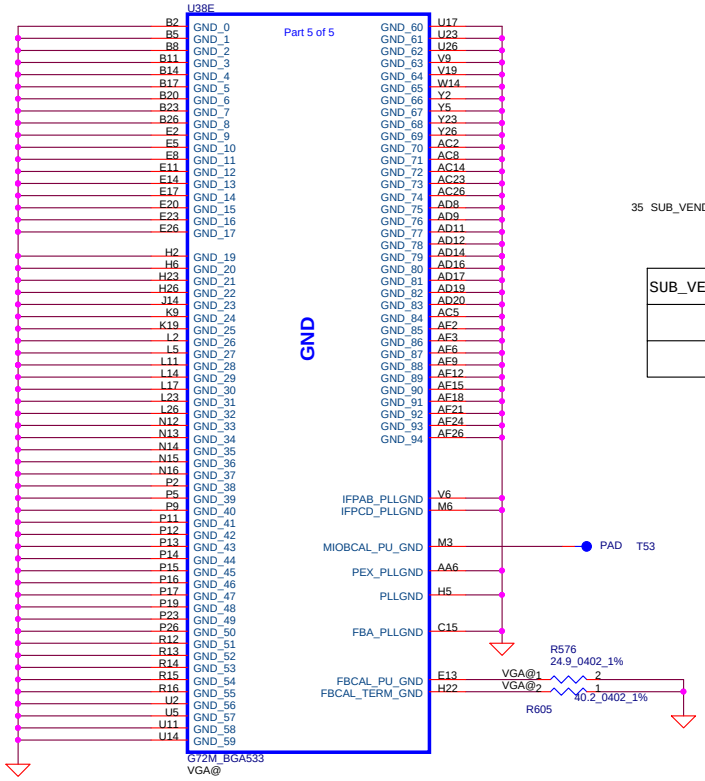
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS Power

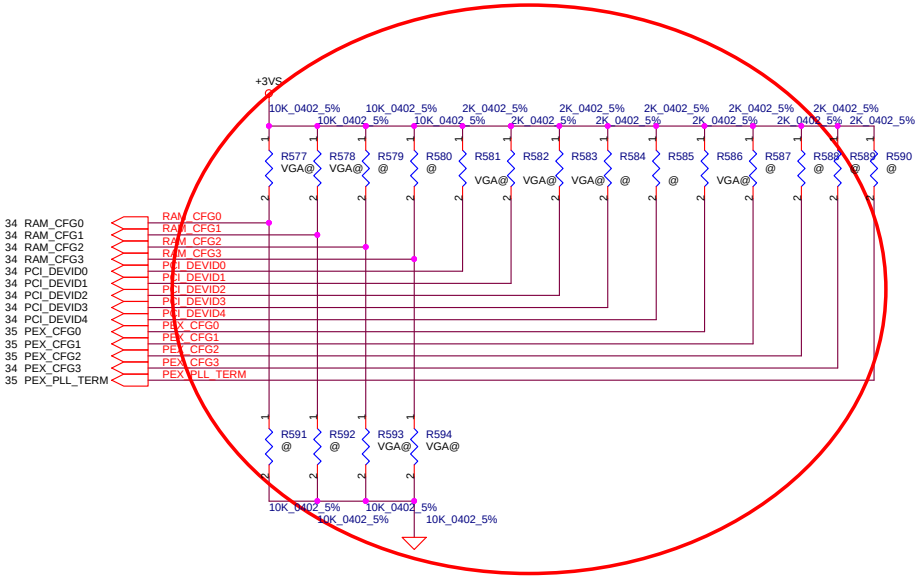
Size	Document Number	Rev
Custom		0.1

Date: Thursday, January 10, 2008 | Sheet 36 of 49



SUB_VENDOR	
0	N0 VIDEO BIOS ROM
1	BIOS ROM is present(Default)

STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIO_A_D1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIO_A_D0	PCI-E PLL termination 0---->Enable (Default) 1---->Disable	0	
PEX_CFG[3:0]	MIOAD [9,8,6] MIOBD_HSYNC	Recommended for G8x	0001	
RAM_CFG[3:0]	MIOAD0 MIOAD1 MIOAD8 MIOAD9	0001 ---> Qimonda 16Mx32 0010 ---> Hynix 16Mx32 0011 ---> Samsung 16Mx32	0011	
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SE : 0X0428	0111 1000	
		G72MV-0x01D7 TBD/TBD	0111	



Bandwidth	RAM Type	Vendor	
FULL R17	32M R11	Samsung	R20, R19
HALF R12	16M R16	Hynix	R18, R19
		Infineon	R18, R21

Package		
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

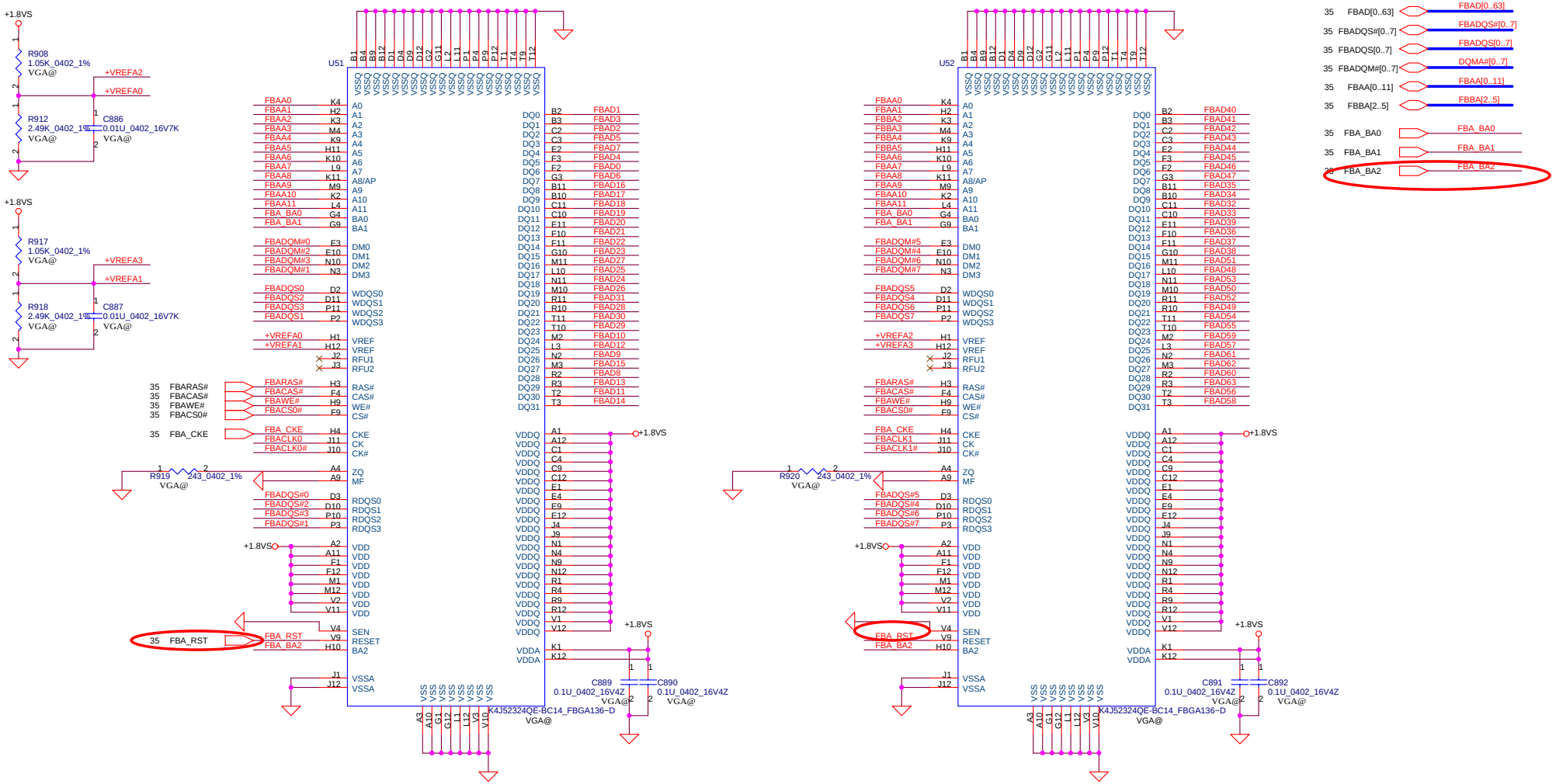
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

Title: NB8M-GS GND & STRAP

Size	Document Number	Rev
Custom		0.1

Date: Thursday, January 10, 2008 Sheet 37 of 49



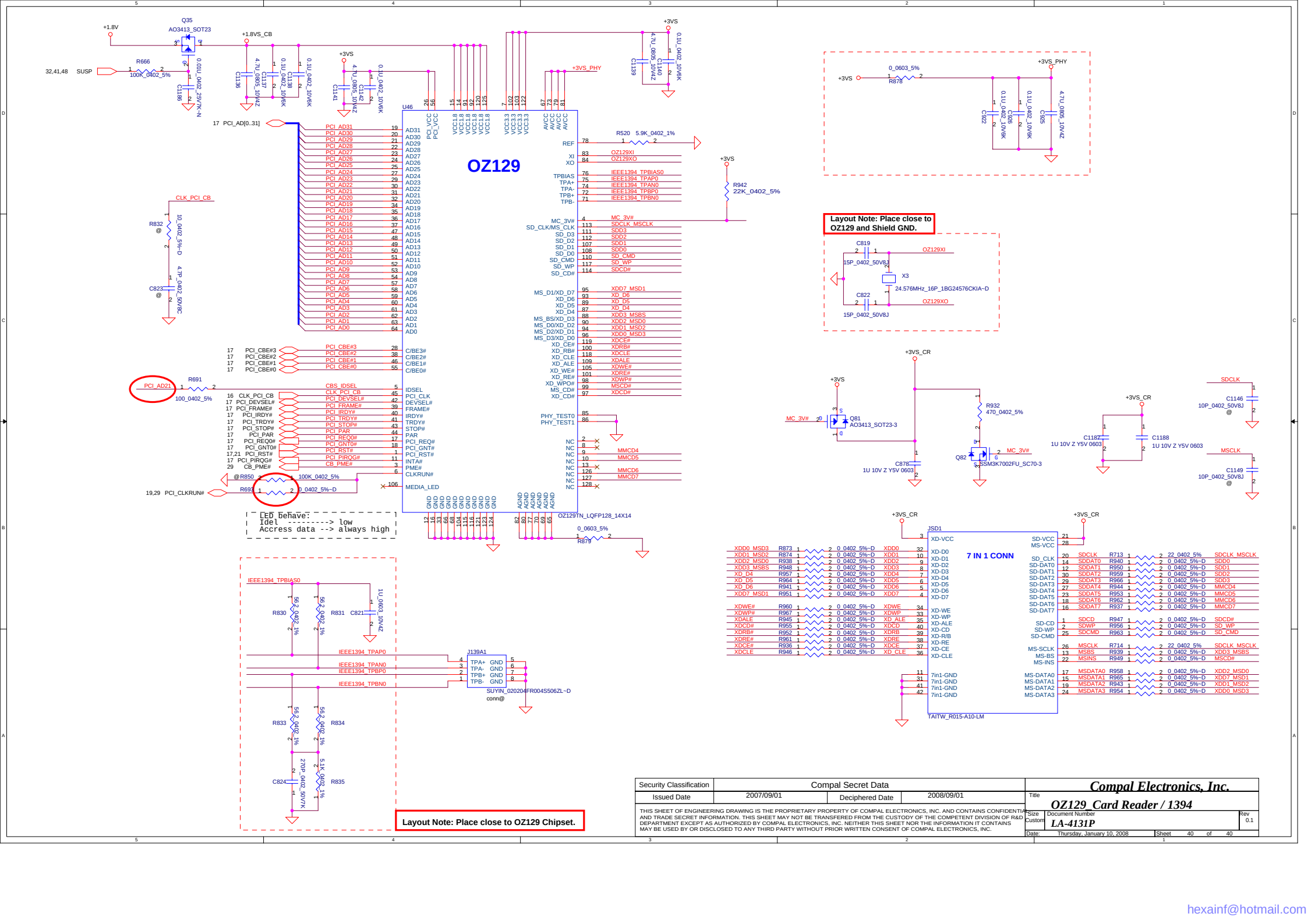
Security Classification	Compal Secret Data		
Issued Date	2007/02/12	Deciphered Date	2008/02/12

Compal Electronics, Inc.

Title: **VRAM GDDR3 A**

Size: | Document Number: *LA-4231P* | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 38 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/09/01	Deciphered Date	2008/09/01

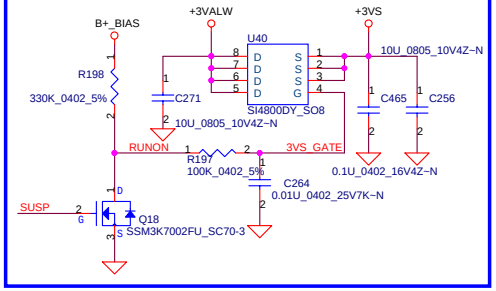
Compal Electronics, Inc.

Title: *OZ129_Card Reader / 1394*

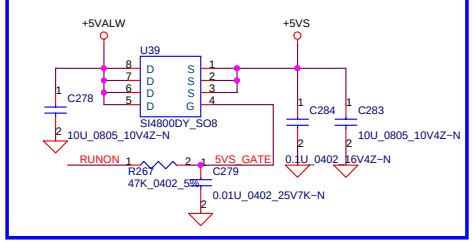
Size	Document Number	Rev
Custom	LA-4131P	0.1

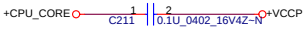
Date: Thursday, January 10, 2008 Sheet 40 of 40

+3VALW to +3VS Transfer

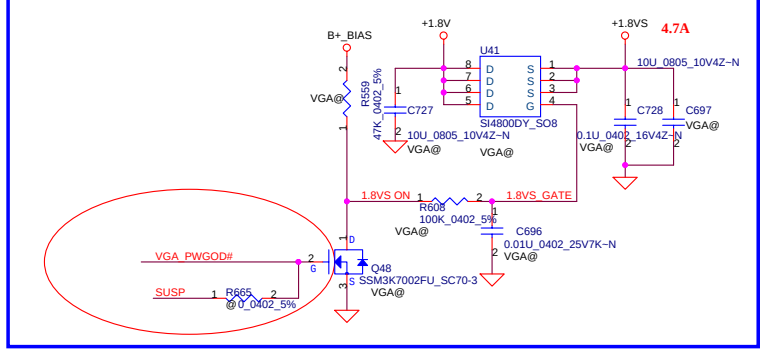


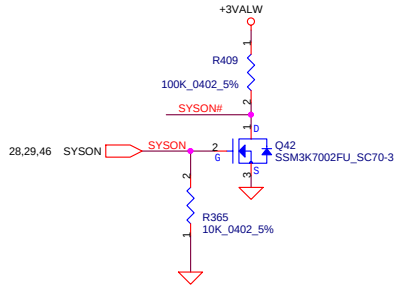
+5VALW to +5VS Transfer

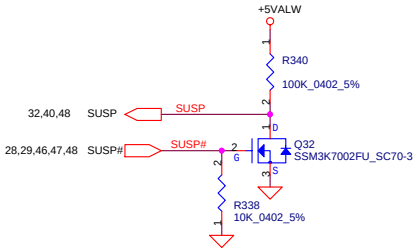


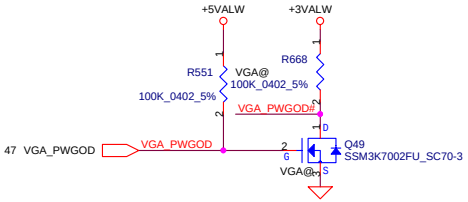


+1.8V to +1.8VS Transfer



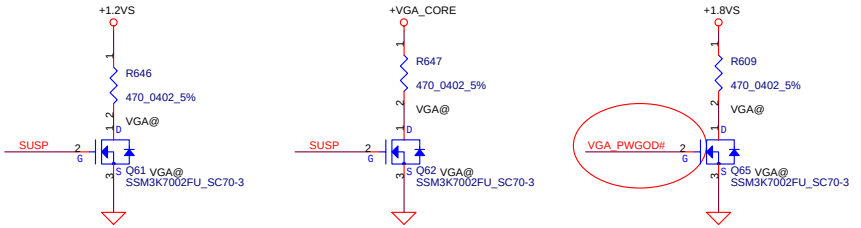




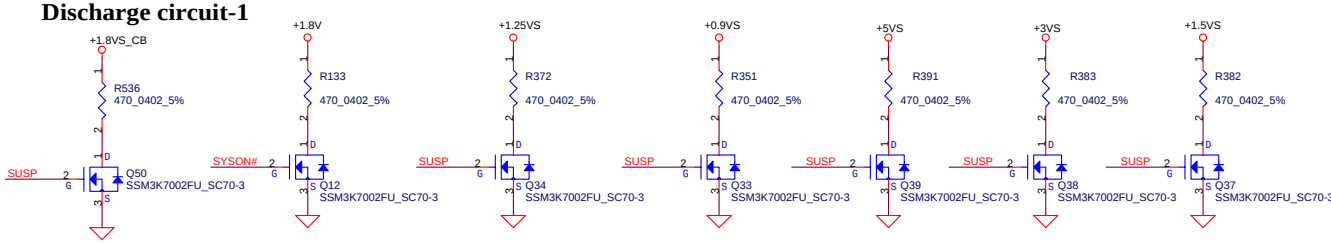


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

VGA Discharge circuit



Discharge circuit-1



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: DC/DC Circuits			
Size: Custom	Document Number: LA-4231P		Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 41 of 49		

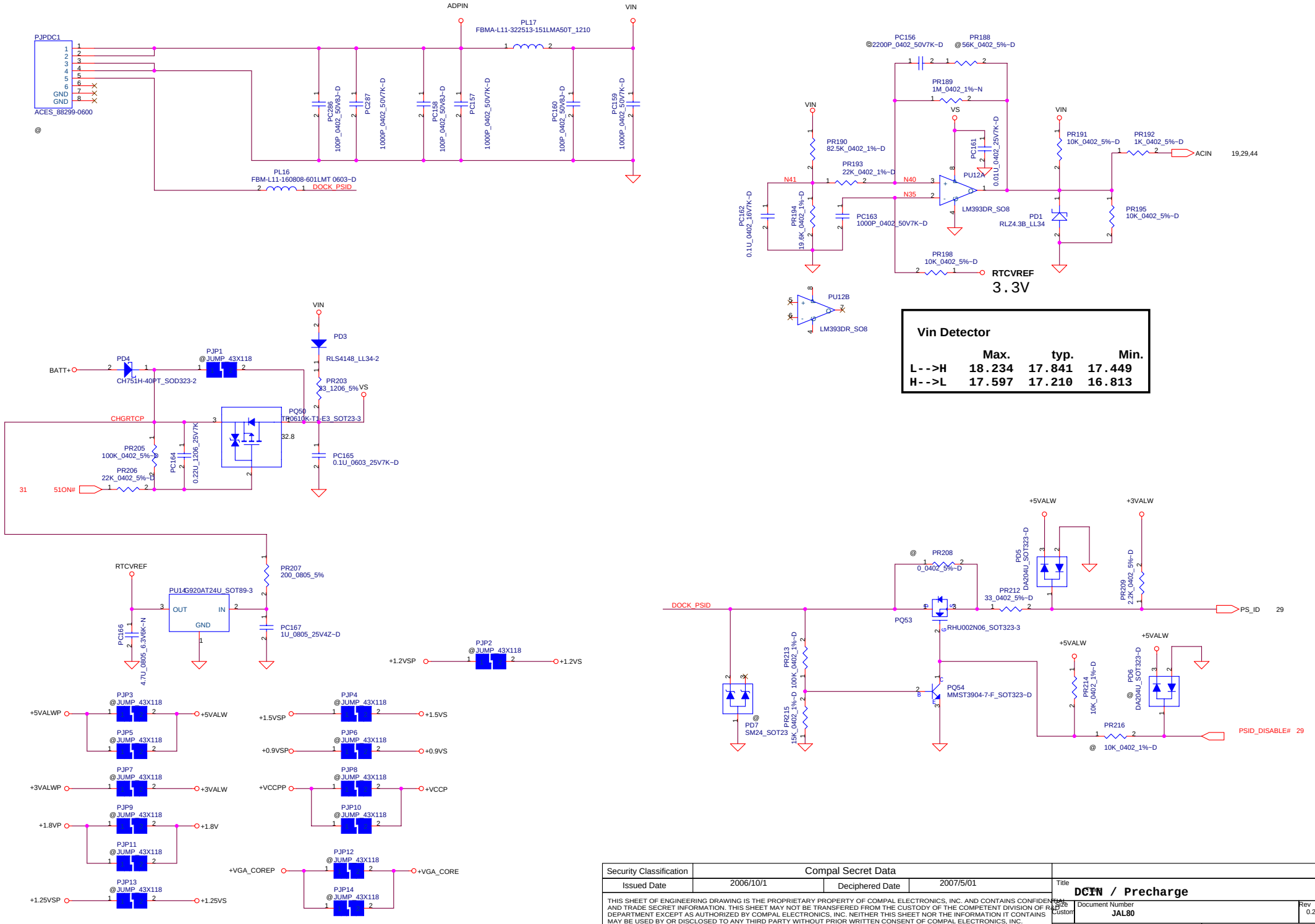
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Screws**

Size	Document Number	Rev
Custom	LA-4231P	0.1

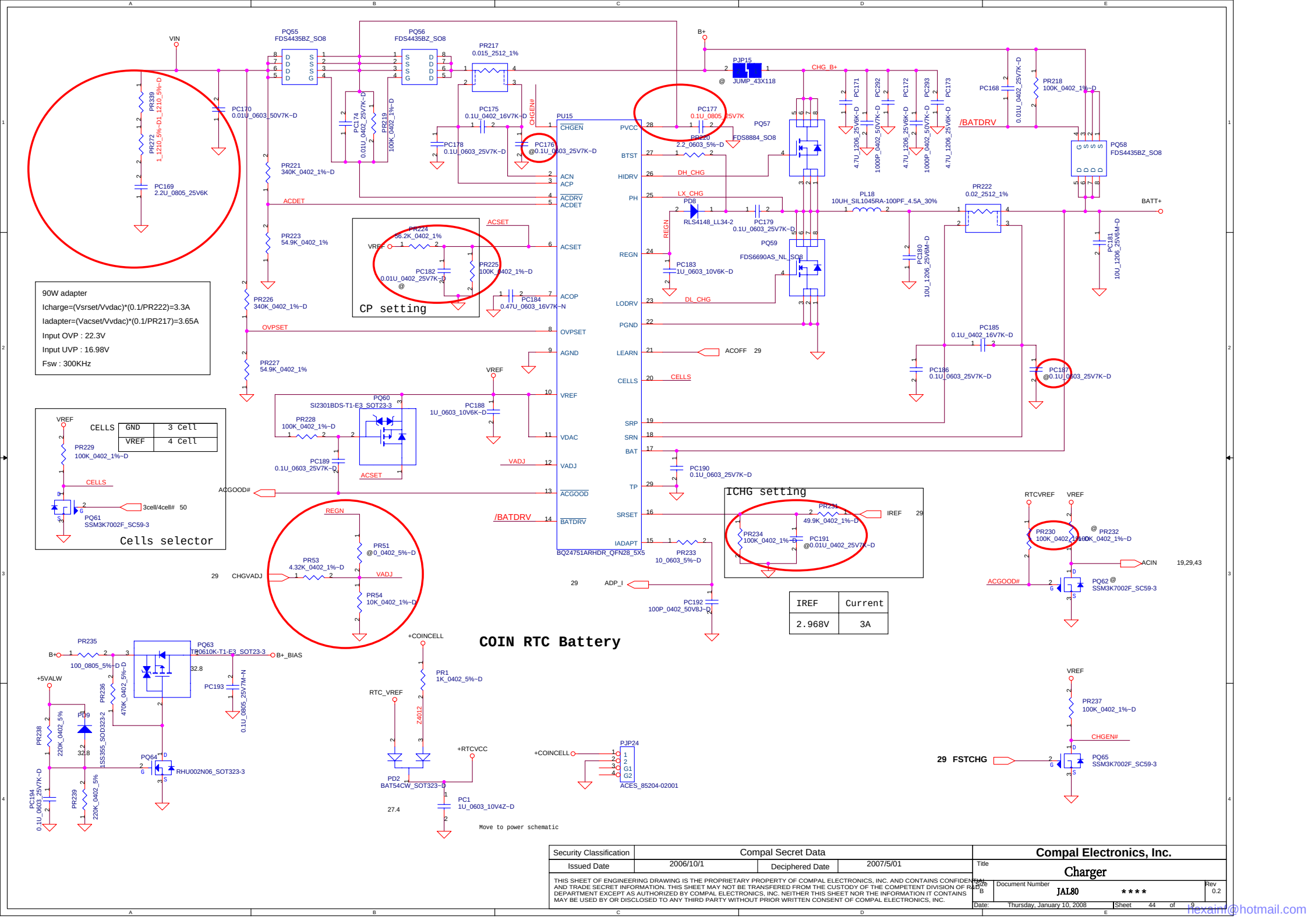
Date: Thursday, January 10, 2008 Sheet 42 of 49

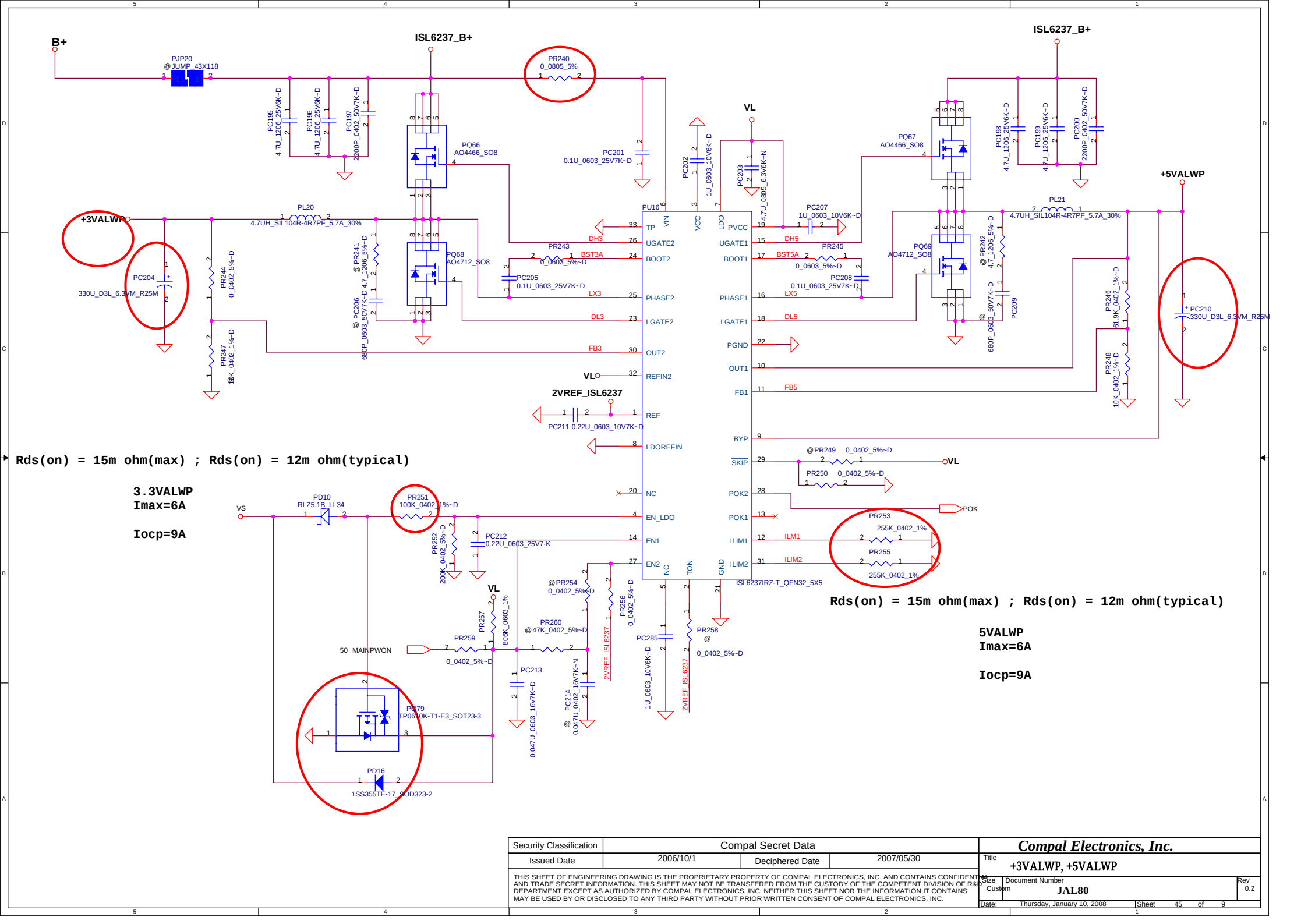


Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title: **DCIN / Precharge**

Size: Custom	Document Number: JAL80	Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 43 of 9	

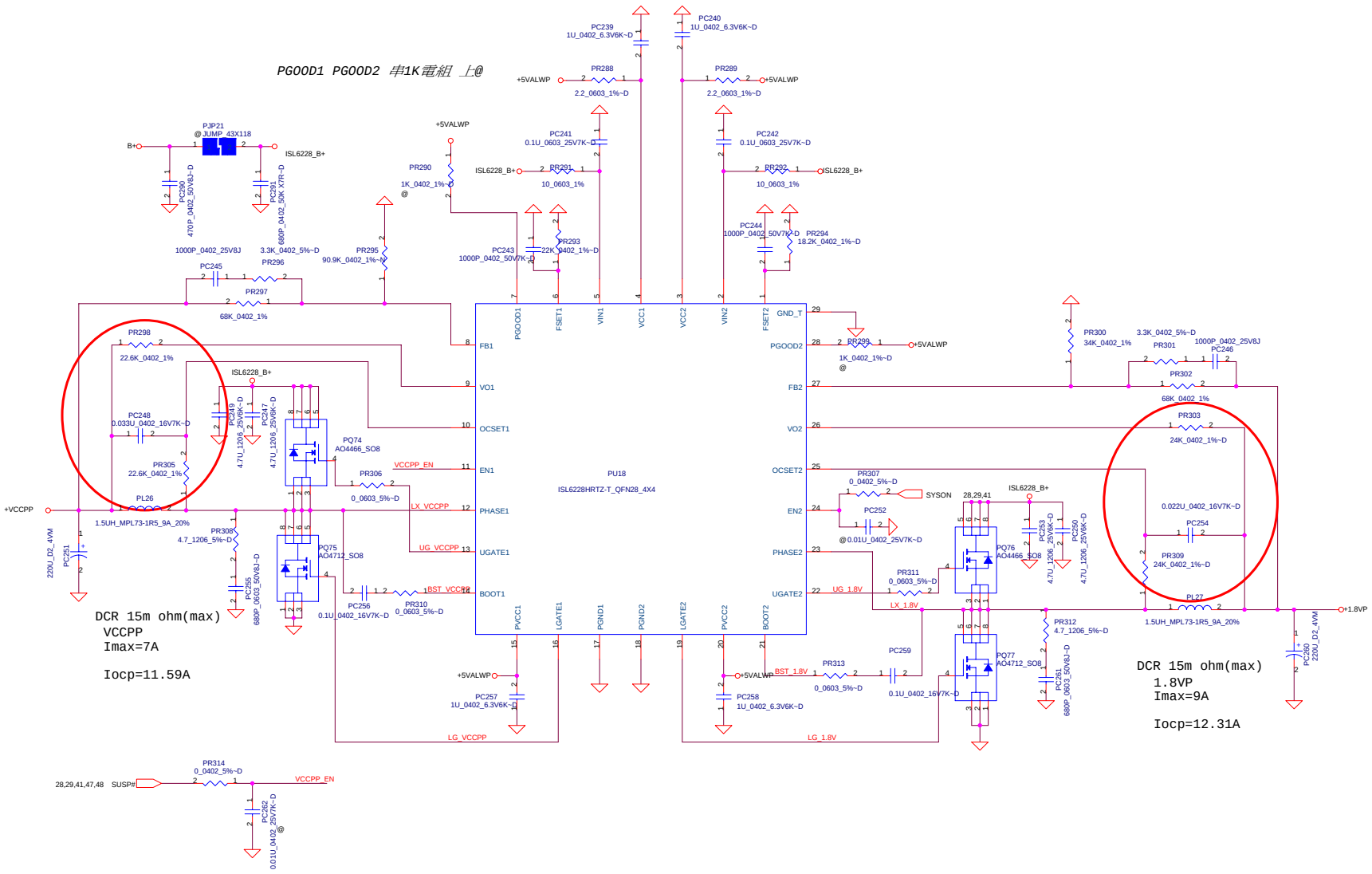




Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

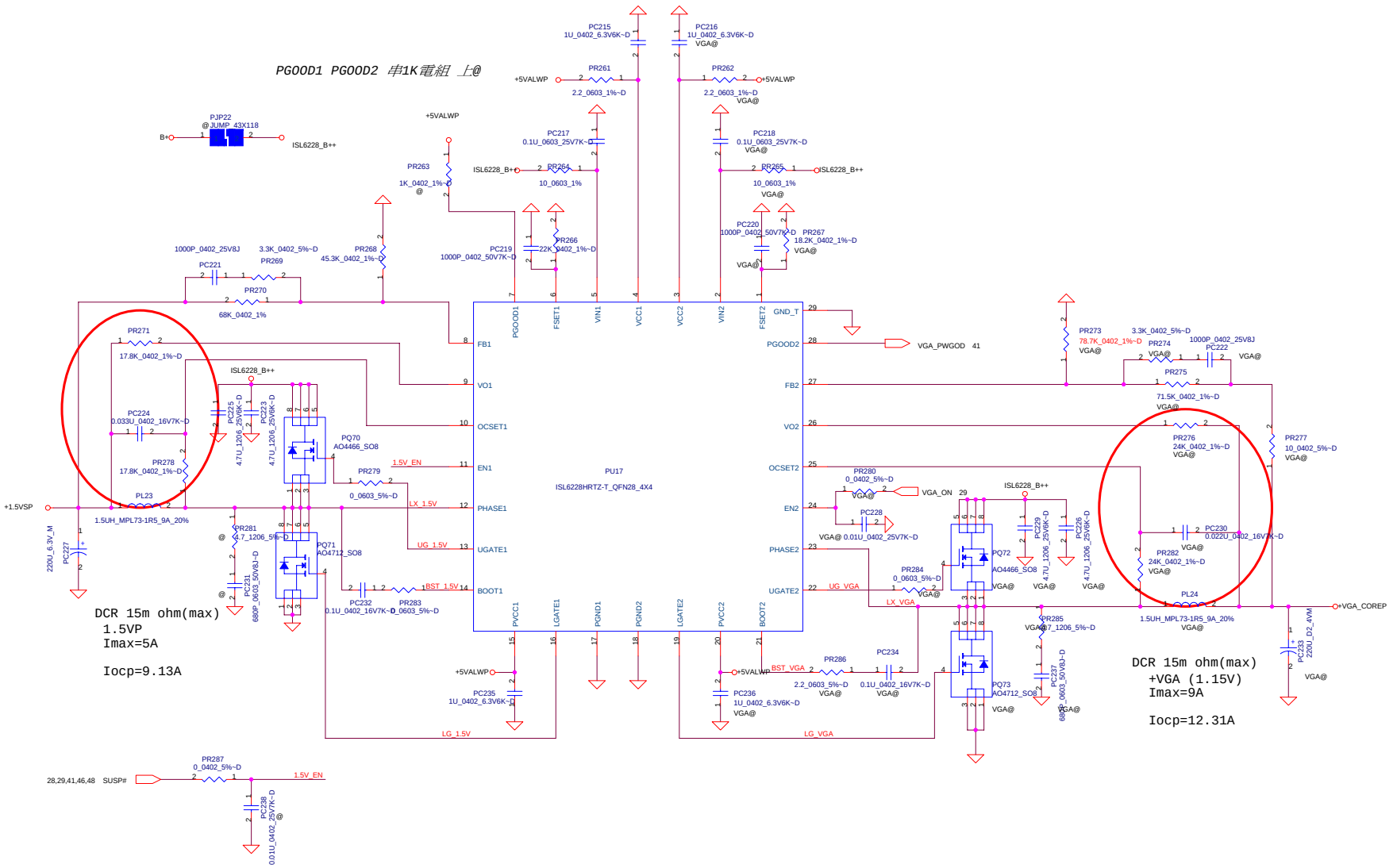
Compal Electronics, Inc.

Title	+3VALWP, +5VALWP		
Size	Custom	Document Number	JAL80
Rev	0.2		
Date:	Thursday, January 10, 2008	Sheet	45 of 9



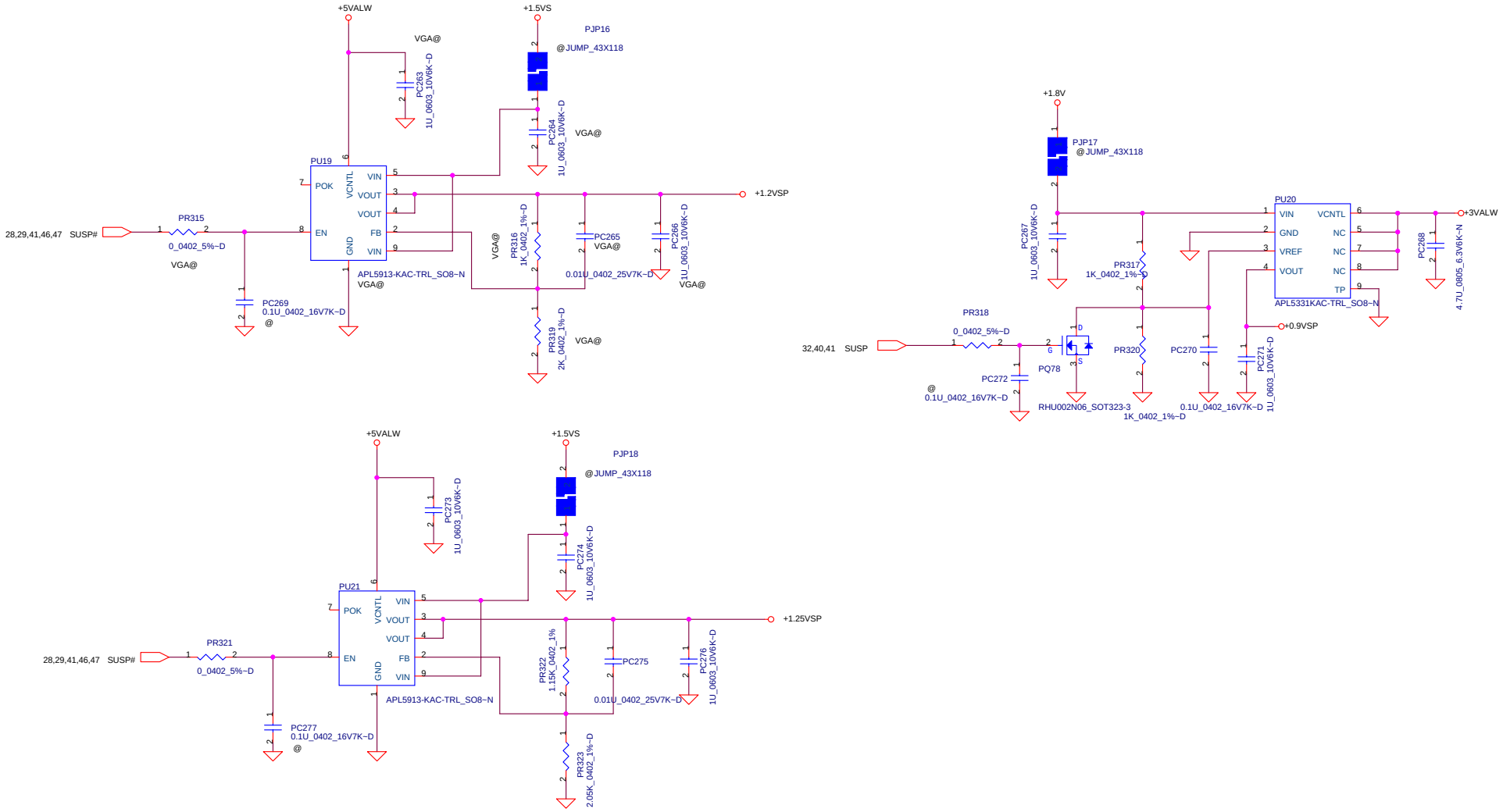
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.8VP/+VCCPP		
Size	Document Number JAL80		Rev 0.2
Date: Thursday, January 10, 2008	Sheet 46 of 9		



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.5VP/+VGA		
Size	Document Number JAL80		Rev 0.2
Date: Thursday, January 10, 2008		Sheet 47 of 9	



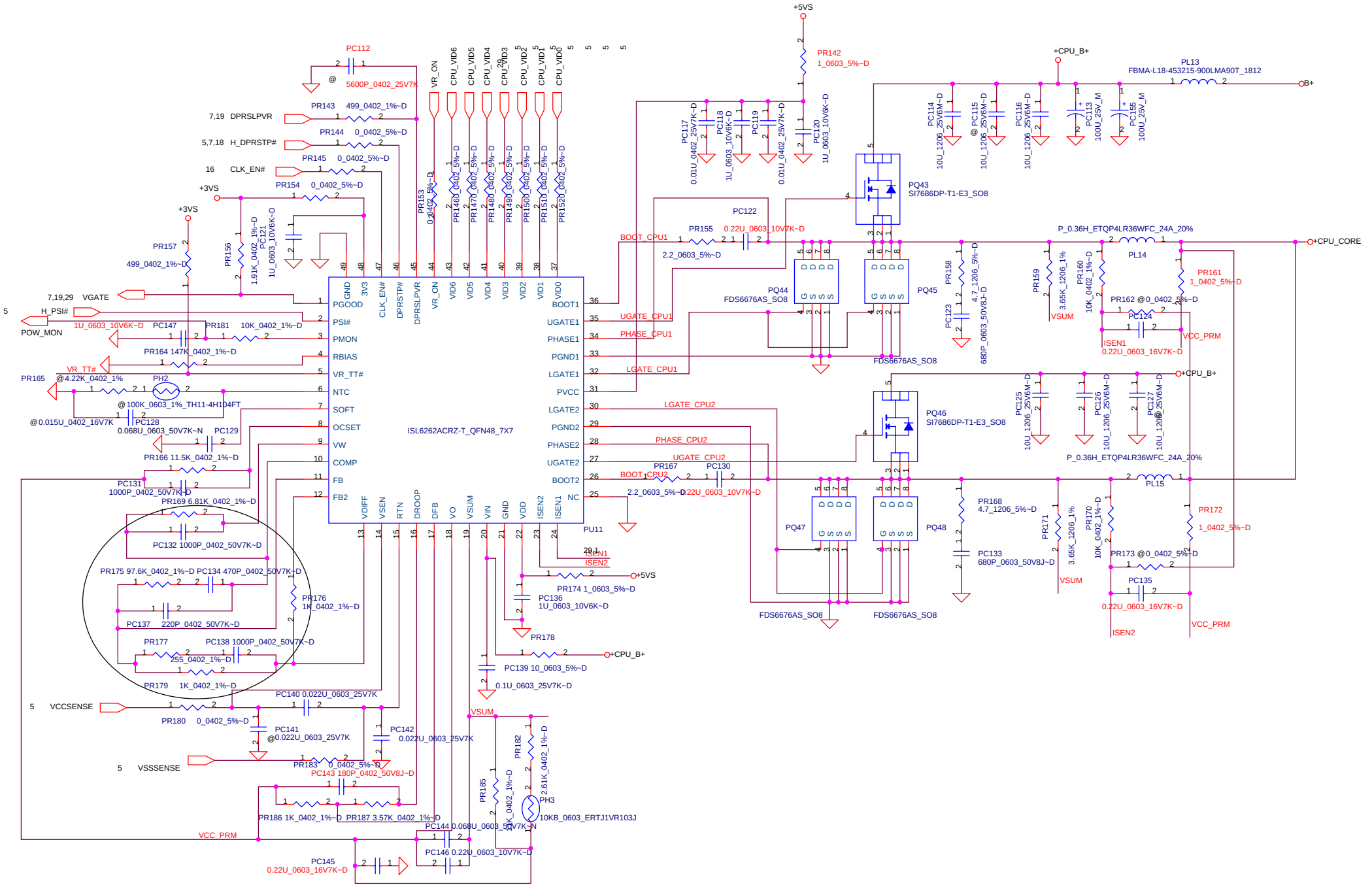
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **+1.25VSP / +0.9VSP/ +1.2VSP**

Size	Document Number	Rev
Custom	JAL80	0.2

Date: Thursday, January 10, 2008 Sheet 48 of 49



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

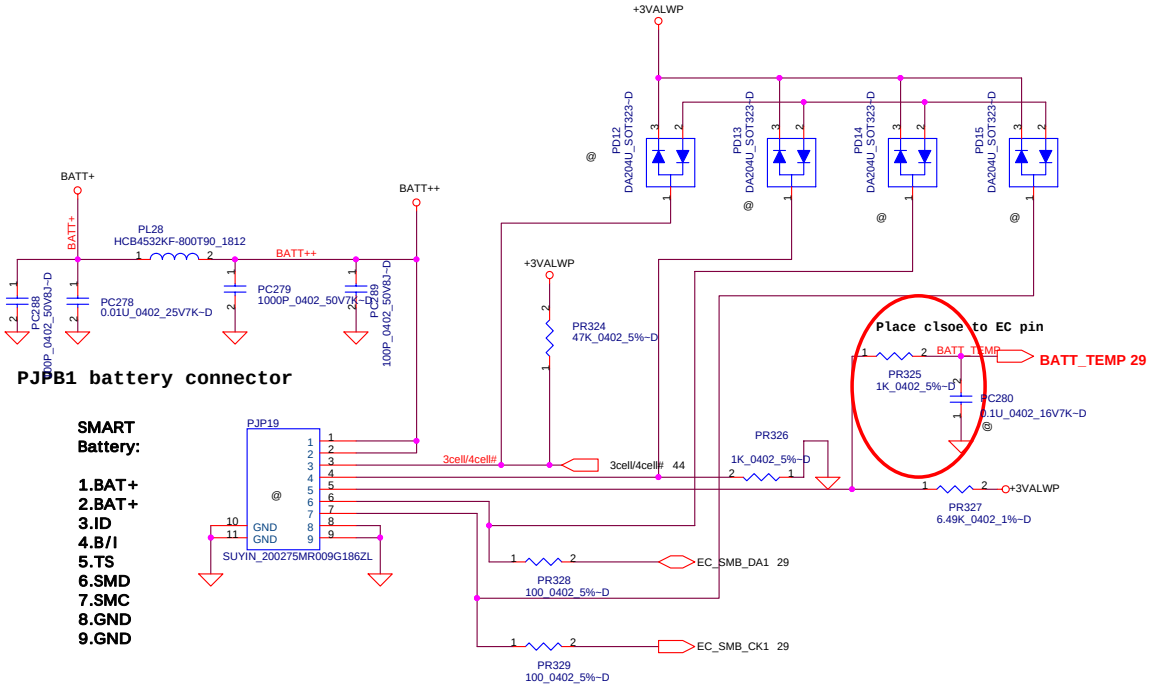
Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	LA-4121P	0.1

Date: Thursday, January 10, 2008 Sheet 49 of 9

Battery Connect/OTP



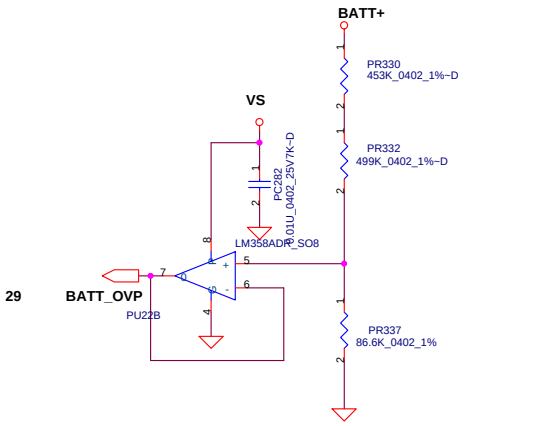
PJPB1 battery connector

SMART Battery:

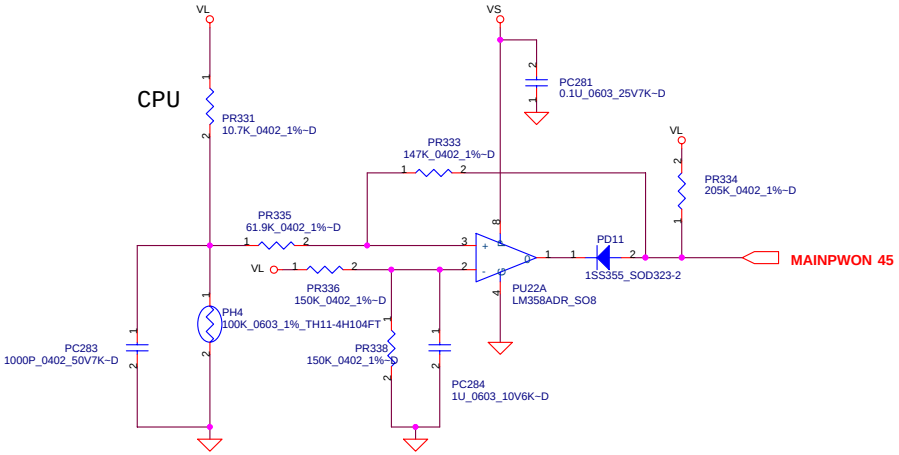
1.BAT+
2.BAT+
3.ID
4.B/I
5.TS
6.SMD
7.SMC
8.GND
9.GND

CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title	BATTERY CONN		
Size	Document Number		Rev
Custom	JAL80		0.2
Date:	Thursday, January 10, 2008	Sheet	50 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-OZ129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to OZ129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ BlueTooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Frequence Decoupling Capacitance	C195 change to C1150~C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
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Compal Electronics, Inc.

Title: EE PIR-1

Size: Custom | Document Number: LA-4231P | Rev: 0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ79 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	44	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
3	49	CPU_CORE	07/12/26	COMPAL	Increase Resistor 0ohm on CPU_CORE high side gate for EMI request	ADD PR163 PR184	
4	45	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location is wrong	DEL PL19	
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Compal Electronics, Inc.

Title: PW PIR-1

Size: Custom | Document Number: LA-3682P | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 52 of 59