

IM3 (Jolie) Discrete 256M & UMA Block Diagram

VER : 3A

POWER

AC/BATT CONNECTOR PG 55

BATT CHARGER PG 48

HybridSLI POWER

VGA Core
+1.1V_GFX PG 53

REGULATOR For GDDR3
+1.8V_RUN PG 50

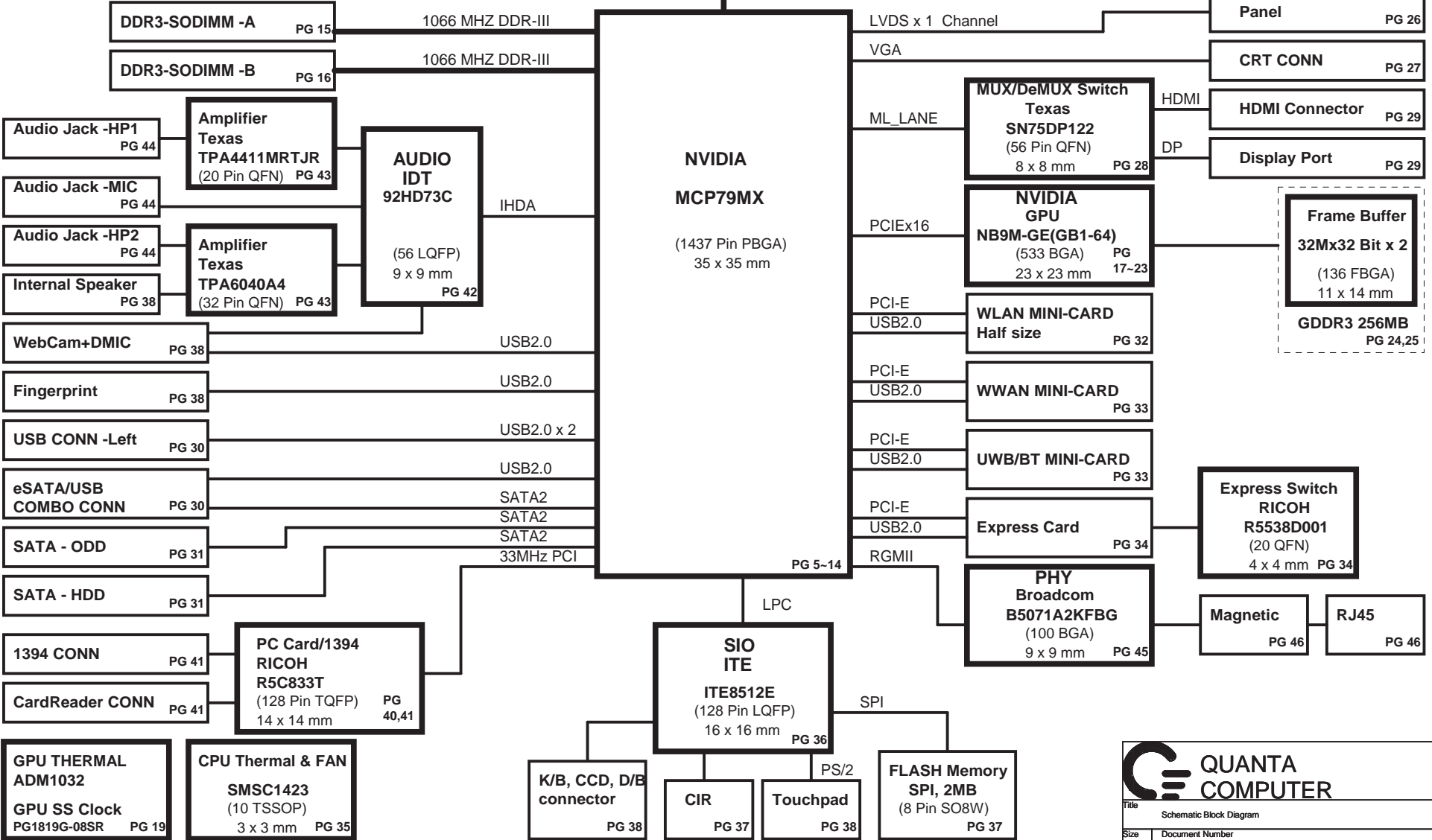
HybridSLI SW
+3.3V_NB9X/+1.8V_FBVDDQ/
+1.1V_GFX_PCIE PG 23

Dual Core CPU Intel Penryn (25W)

(478 Micro-FCPGA)
35 x 35 mm PG 3,4

SYSTEM POWER

MCP VR +MCP_CORE PG 50	CPU VR +VCC_CORE/ +1.05V_VCCP PG 49,54
REGULATOR For DDR3 +1.5V_DDR/ +0.75V_DDR_VTT PG 51	REGULATOR +3.3V_ALW/+5V_SRC/ +15V_ALW PG 52
RUN/SUS POWER SW +5V/+3.3V/+1.5V_RUN +3.3V_SUS PG 56	LDO +1.1V_SUS PG 53
	LDO +1.1V_RUN PG 51



QUANTA COMPUTER

Title: Schematic Block Diagram


Size: Document Number IM3 (XPS-Jolie) Rev 2A

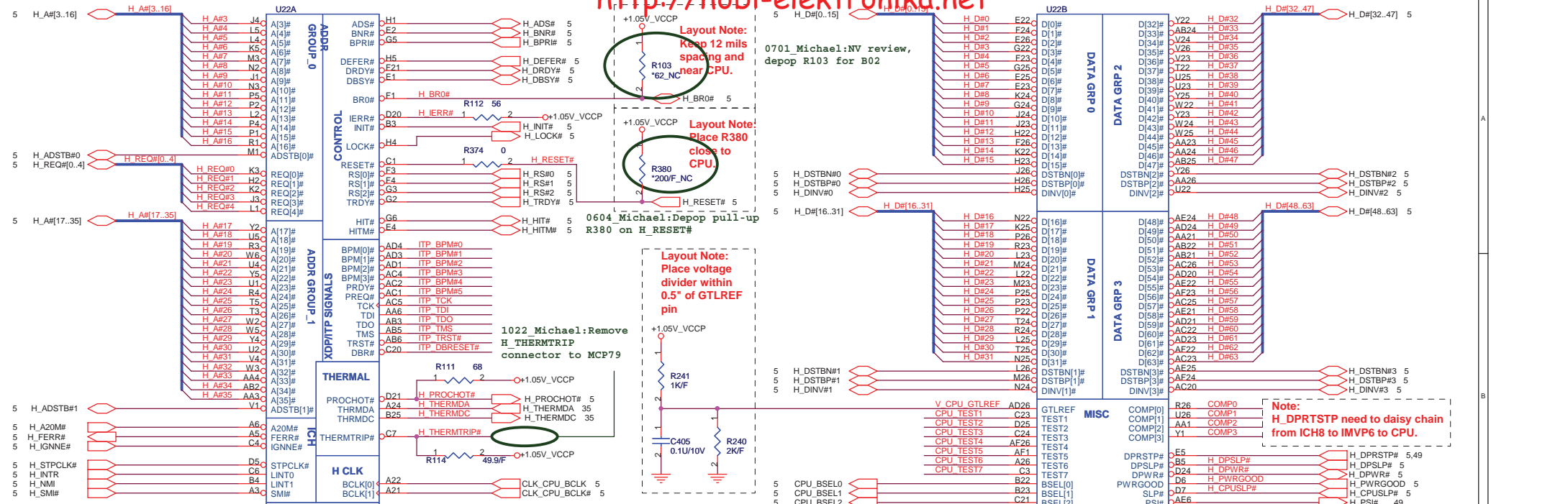
Date: Thursday, October 23, 2008 Sheet 1 of 59

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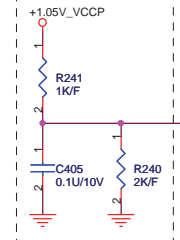
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5-14	MCP79 (NB+SB+CKG)
15-16	DDRIII SO-DIMM(204P)
17-25	VGA (NB9M)
26	LCD CONN
27	CRT CONN
28	DeMux SW (SN75DP122)
29	HDMI & DP CONN
30	USB & eSATA & TV
31	HDD & ODD (SATA)
32	MINI-CARD (WLAN)
33	MINI-CARD (WPAN,WWAN)
34	Express Card
35	FAN & Thermal
36	SIO (ITE8512)
37	Flash ROM/ RTC/ CIR
38	KB/ CCD/ User Interface
39	LED
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52	SYS 5V/ 3V(MAX17020)
53	NB9 Core (MAX8632)
54	GRAM_1.8V (TPS51117)
55	DCIN,Batt
56	RUN POWER SW
57	Debug Port (Mini PCI)
58	PAD & SCREW

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBVDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			

 QUANTA COMPUTER		Title	
		Index & Power Status	
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	2A	
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Layout Note:
Place voltage divider within 0.5" of GTLREF pin

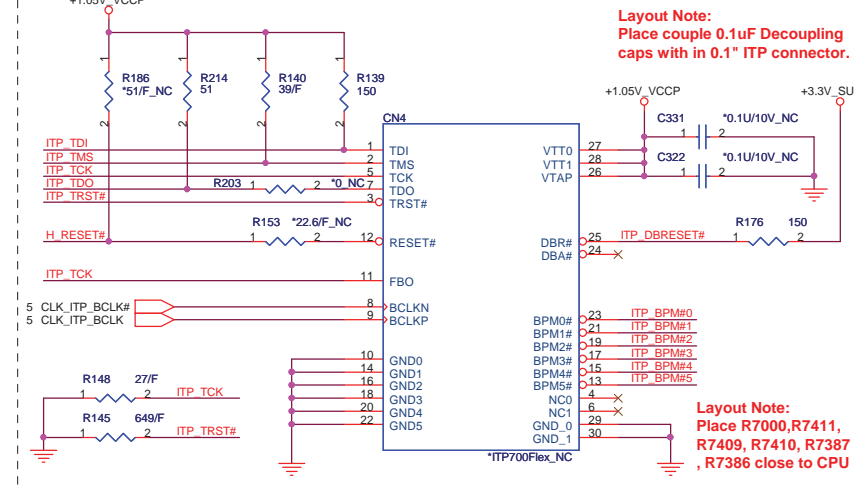


FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

Note:
H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

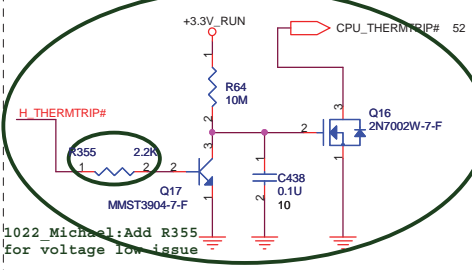
Populate ITP700Flex for bringup



Layout Note:
Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.

Layout Note:
Place R7000, R7411, R7409, R7410, R7387, R7386 close to CPU

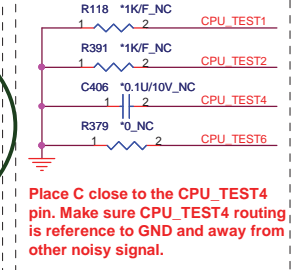
CPU THERMTRIP Circuit



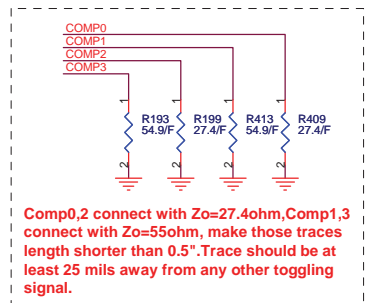
1022 Michael: Add R355 for voltage low issue

0823_Michael: Follow RM2 to change CPU THERMTRIP circuit

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8



Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.



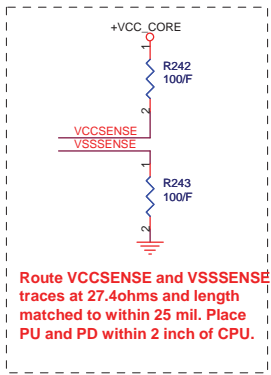
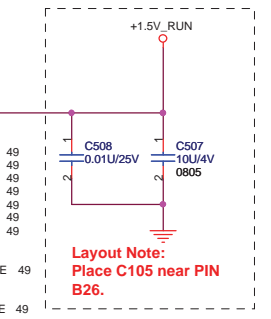
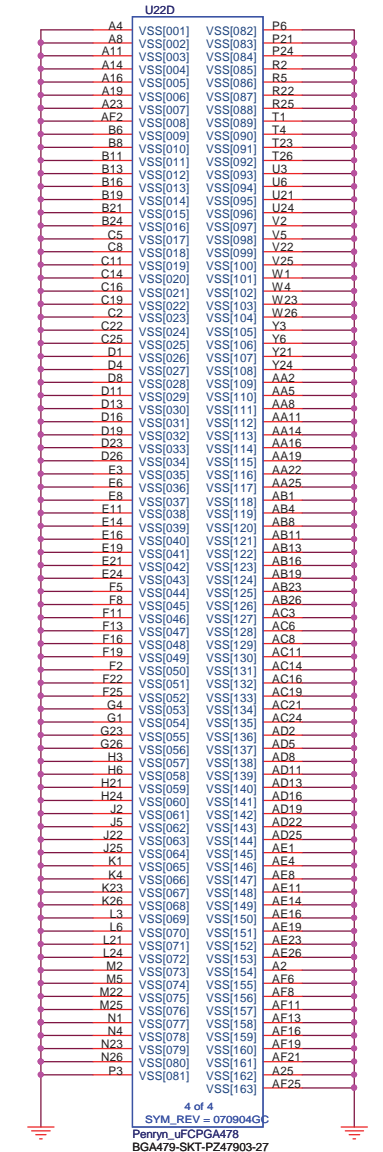
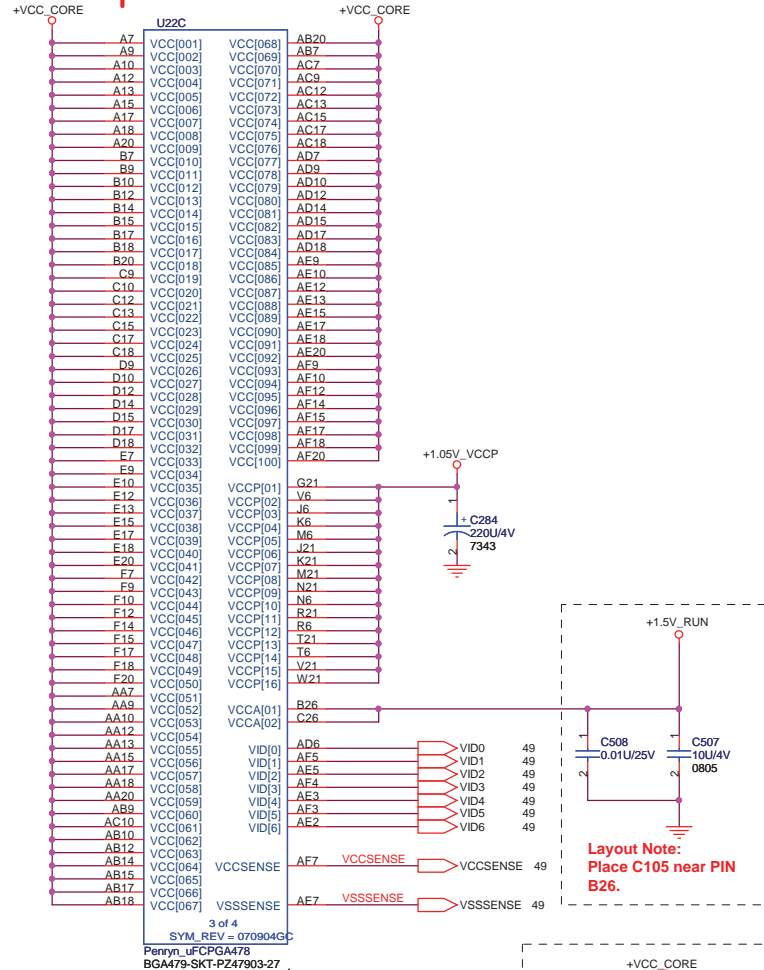
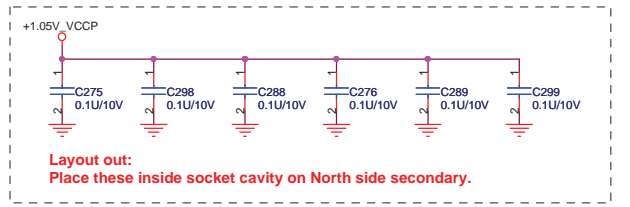
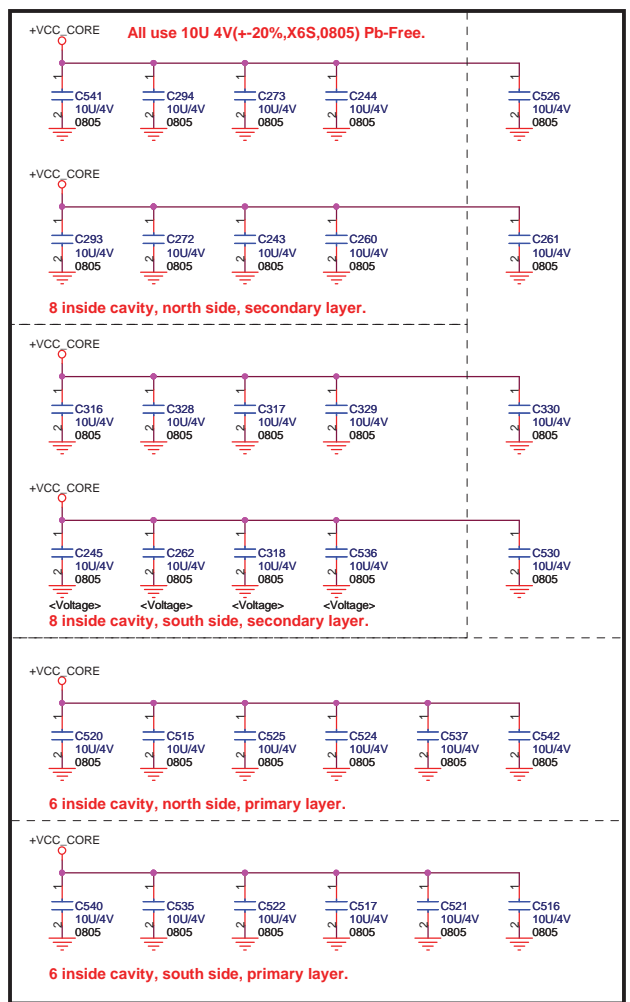
Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

**QUANTA
COMPUTER**

Title: Penryn Processor (HOST BUS)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

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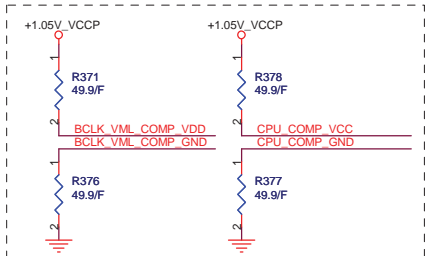
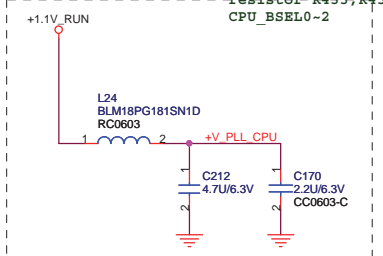
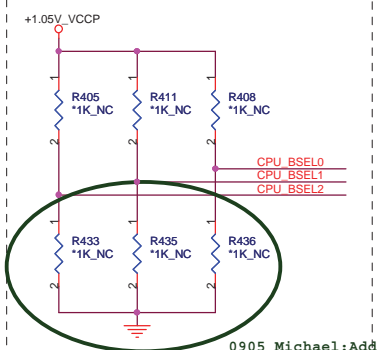
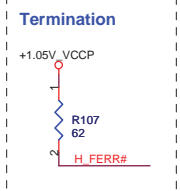
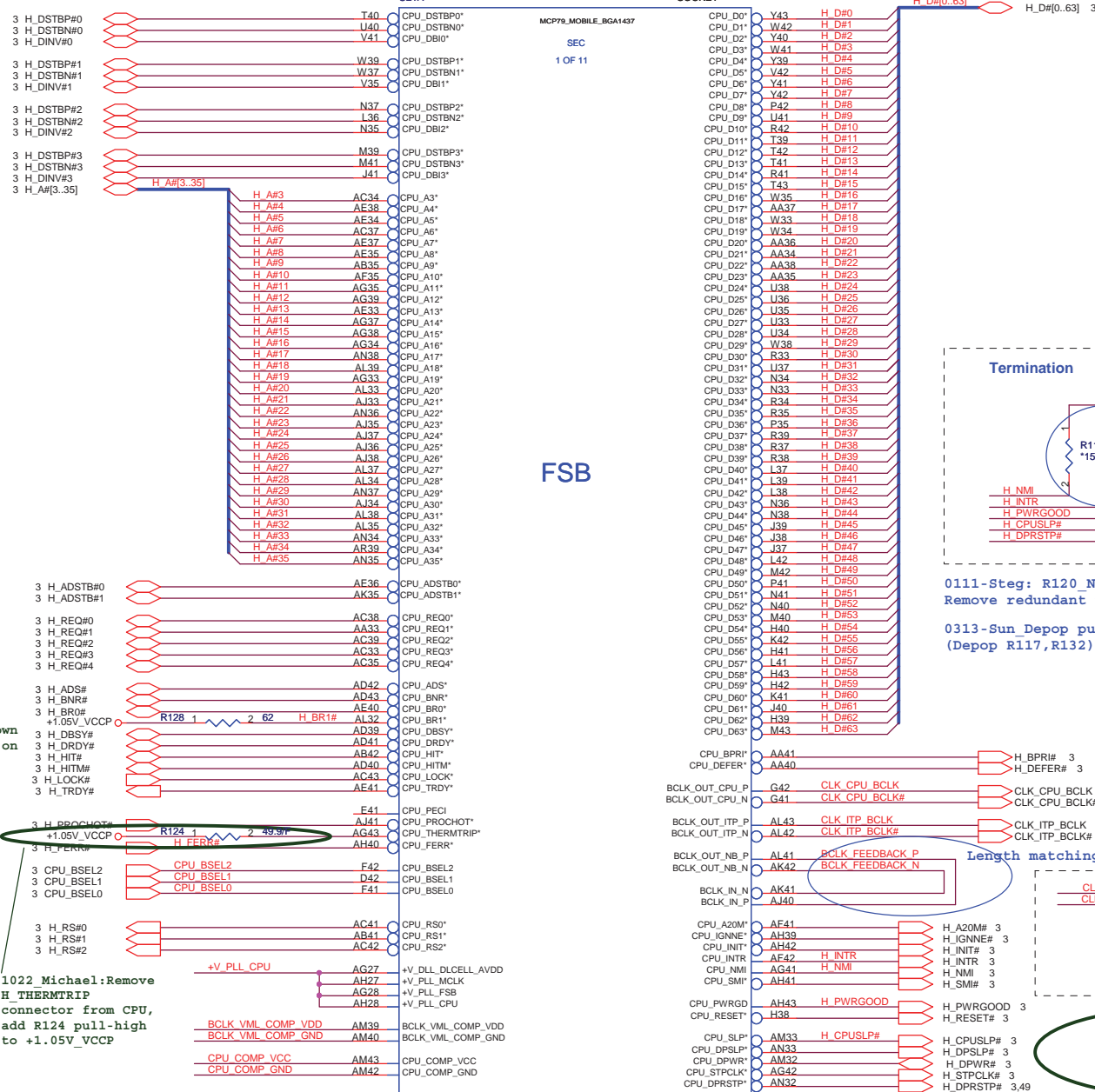
Layout Note:
Place C105 near PIN B26.

Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

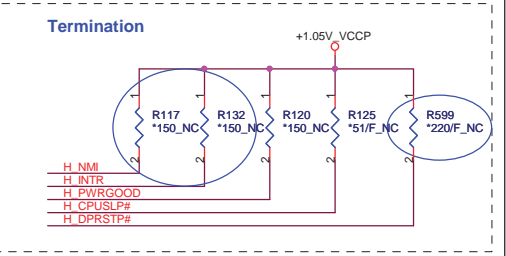
3 of 4
SYM_REV = 070904G
Penryn_uFCPGA478
BGA478-SKT-PZ47903-27

4 of 4
SYM_REV = 070904G
Penryn_uFCPGA478
BGA478-SKT-PZ47903-27



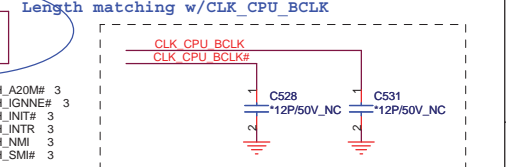


+V_DLL_DLCELL_AVDD 150mA with RUN rail	+V_PLL_MCLK 20mA with RUN rail	+V_PLL_FSB 29mA with RUN rail	+V_PLL_CPU 15mA with RUN rail
1 x ferrite bead	1 x ferrite bead	1 x ferrite bead	1 x ferrite bead
1 x 4.7uF X5R ceramic	1 x 1uF X5R ceramic	1 x 4.7uF X5R ceramic	1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic



0111-Steg: R120_NC. Remove redundant pull-up R120 on H_PWRGOOD

0313-Sun Depop pull-up on H_NMI & H_INTR. (Depop R117, R132)



0605 Michael: NV review, remove pull-down C509 on CLK_ITP_BCLK & C510 on CLK_ITP_BCLK#

QUANTA COMPUTER

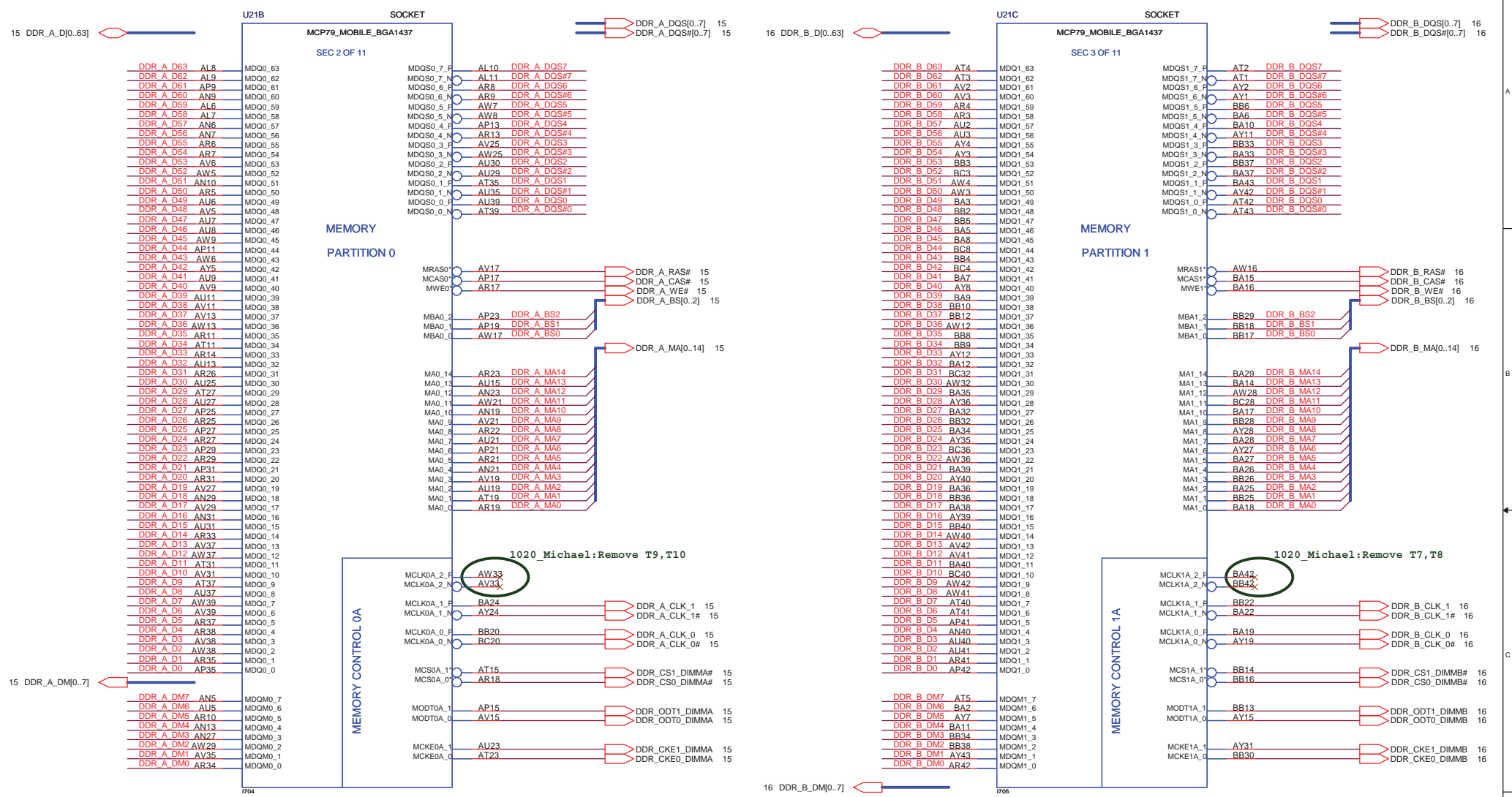
Title: MCP79 (HOST)

Size: Document Number IM3 (XPS-Joie)

Date: Thursday, October 23, 2008

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Rev: 2A



Layout Notice:
Memory Data Signal Group
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

Memory Data Strobes
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

QUANTA COMPUTER

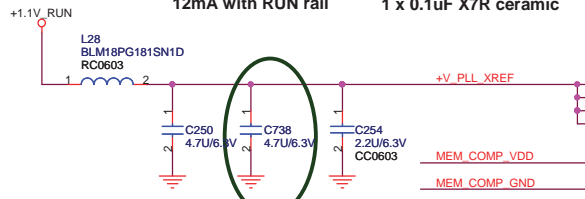
Title: MCP79 (DDR3)

Size	Document Number IM3 (XPS-Joie)	Rev 2A
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Date: Wednesday, October 29, 2008 Sheet 6 of 59

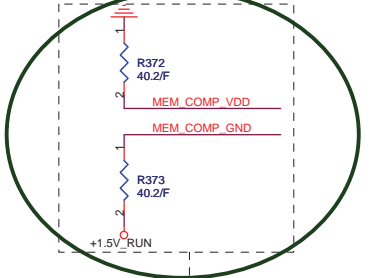
- +V_VPLL**
39mA with RUN rail
- +V_PLL_XREF_XS**
17mA with RUN rail
- +V_PLL_CORE**
19mA with RUN rail
- +V_PLL_DP**
12mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

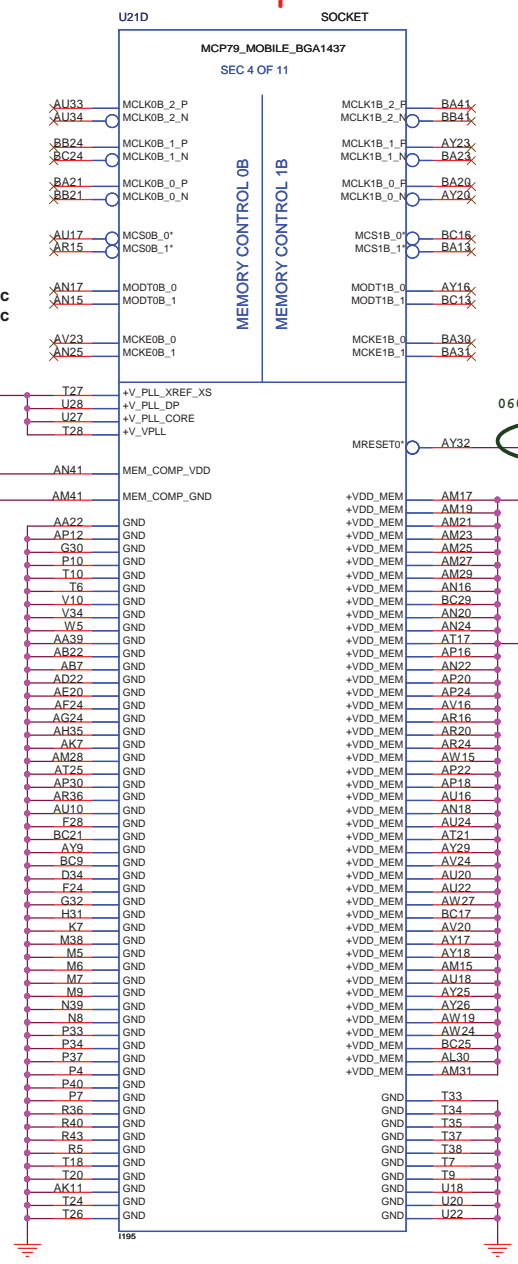


0910 Michael: Follow NV check list
add 4.7U C738

0102-Sun_Change MEM_COMP_VDD & MEM_COMP_GND setting
MEM_COMP_VDD from +1.5V_RUN to GND &
MEM_COMP_GND from GND to +1.5V_RUN

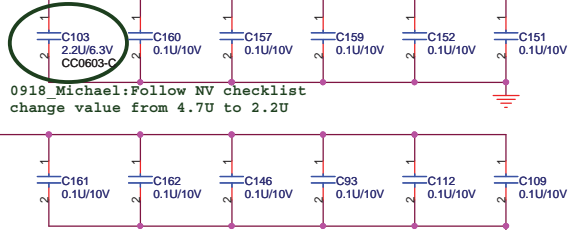


Layout Notice:
1. 40.2 +/-1% ohm to +1.5V_SUS less than 1 inch from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils spacing to termination resistor.

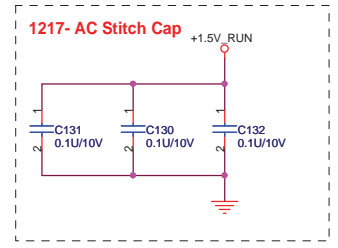


0605_Michael: Remove 0ohm R93

4.3A with ALW rail for S0
318mA for S0 Idle
1 x 2.2uF ceramic
12 x 0.1uF X7R ceramic



0918 Michael: Follow NV checklist
change value from 4.7U to 2.2U



1217- AC Stitch Cap



17 PCIE_MRX_GTX_P[0..15]
17 PCIE_MRX_GTX_N[0..15]

PCIE_MTX_GRX_P[0..15] 17
PCIE_MTX_GRX_N[0..15] 17

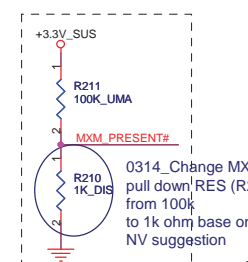
PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

0605 Michael:Remove 0ohm
R185 on MXM_ON#
R433,R435,168 pull-down to GND
R177 on PE_RESET# MXM#
R458 on PCIE_WAKE#

Table of PCIE MRX GTX signals (P0-P15, N0-N15) and their corresponding pins (E7-E15, D7-D15, C7-C15, B7-B15, A7-A15).

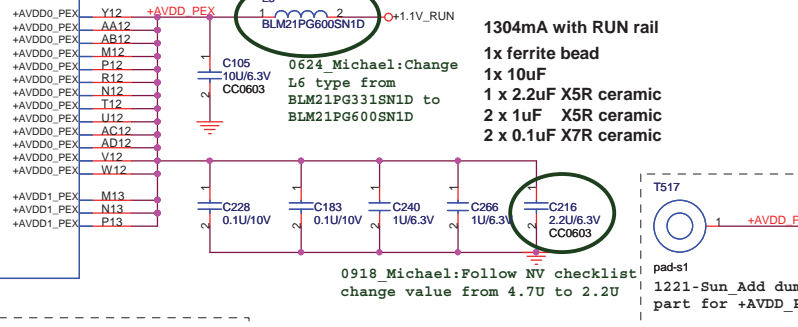
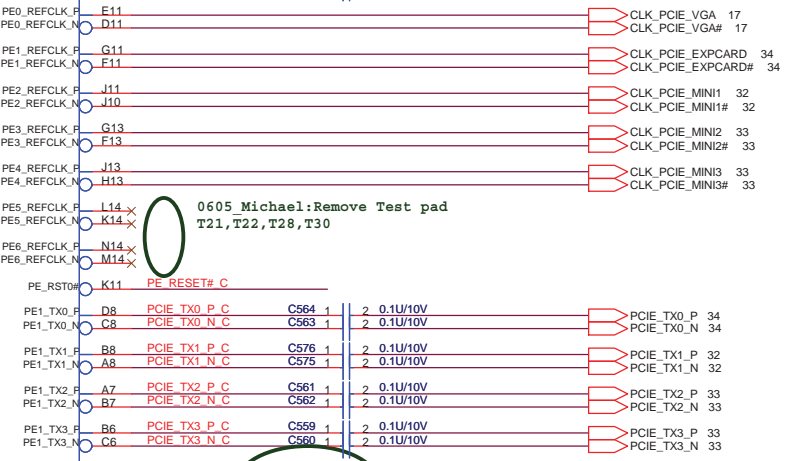
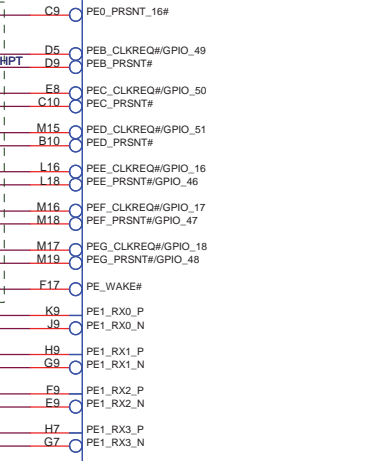
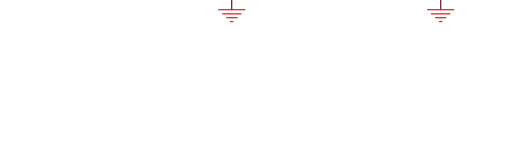
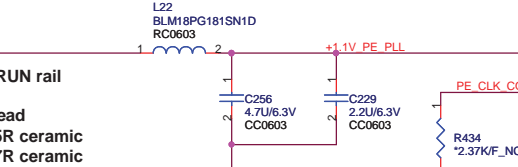
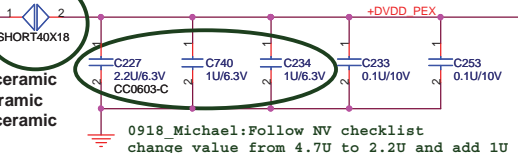
PCIE

Table of PCIE MTX GRX signals (P0-P15, N0-N15) and their corresponding pins (C5-C15, D4-D15, C4-C15, B4-B15, A4-A15, B3-B15, A3-A15, B2-B15, C1-C15, D1-D15, D2-D15, E1-E15, E2-E15, F2-F15, G3-G15, H4-H15, H3-H15, H2-H15, H1-H15, J1-J15, J2-J15, J3-J15, K2-K15, K3-K15, L4-L15, L3-L15, M4-M15, M3-M15, M2-M15, M1-M15).



Express Card
34 CARD_CLK_REQ#
34,36 EXPRCD_PWREN#
WLAN
32 MINI1CLK_REQ#
UWB/BT
33 MINI2CLK_REQ#
WWAN
33 MINI3CLK_REQ#
17 PE_RESET_MXM#

Express Card
34 PCIE_RX0_P
34 PCIE_RX0_N
WLAN
32 PCIE_RX1_P
32 PCIE_RX1_N
UWB/BT
33 PCIE_RX2_P
33 PCIE_RX2_N
WWAN
33 PCIE_RX3_P
33 PCIE_RX3_N



0825 Michael:Add KB detect function
0918 Michael:Remove KB detect function
0920 Michael:Add KB detect function

0918 Michael:Follow NV checklist change value from 4.7U to 2.2U and add 1U

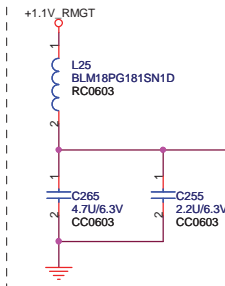
0605 Michael:Remove Test pad
T21,T22,T28,T30

1304mA with RUN rail
1x ferrite bead
1x 10uF
1x 2.2uF X5R ceramic
2 x 1uF X5R ceramic
2 x 0.1uF X7R ceramic

0918 Michael:Follow NV checklist change value from 4.7U to 2.2U

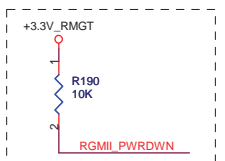
QUANTA COMPUTER logo and title block containing: Title: MCP79 (PCIE), Size: Document Number IM3 (XPS-Joie), Rev: 2A, Date: Saturday, September 20, 2008, Sheet: 8 of 59.

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic



5mA with RUN rail

Layout Notice:
124 ohm +-1% to GND and within 750 mils of MCP79.
0.01uF to GND and within 500 mils of MCP79.



190mA with RUN-rail

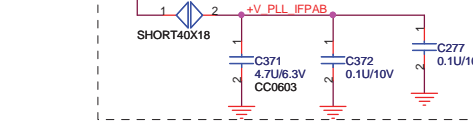
0606 Michael: Add DR_PLUG on HPLUG_DET2 for DP detect

0312-Sun_Change footprint to normal short type "short40x18"

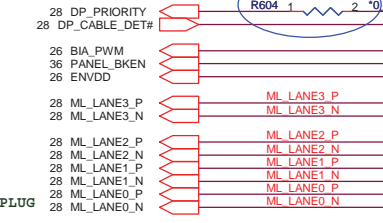
0918 Michael: Follow NV checklist change value from 4.7uF to 2.2uF

0918 Michael: Follow NV checklist change value from 4.7uF to 2.2uF

8mA with RUN rail
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic



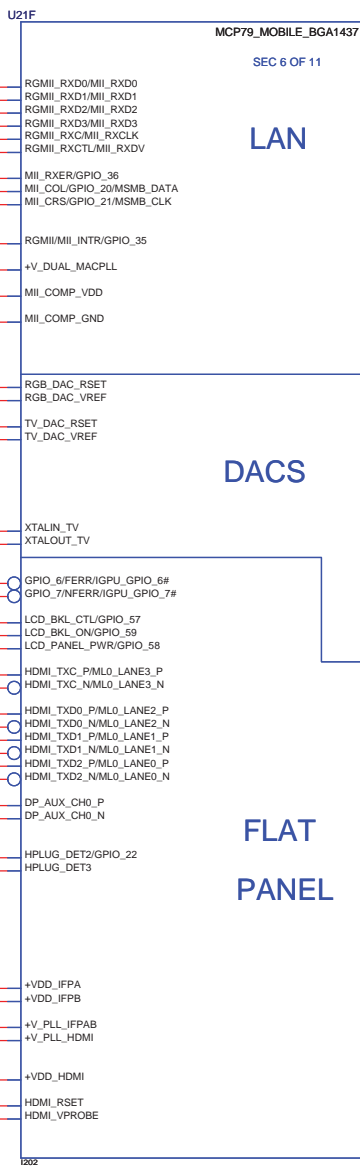
0318-Sun_Connect GPIO6 to DP_PRIORITY, add R604 & del T39



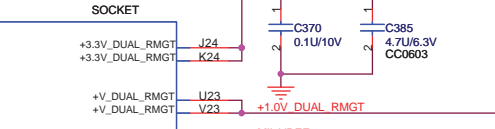
LAN

DACS

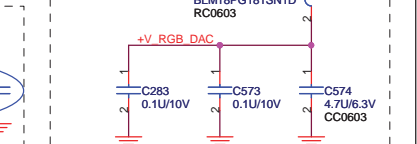
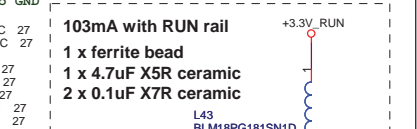
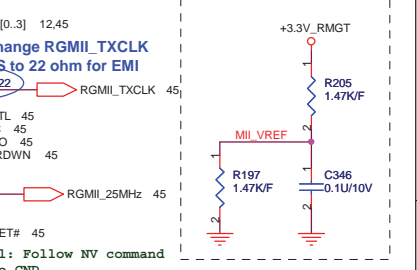
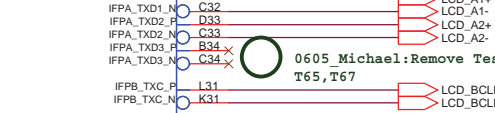
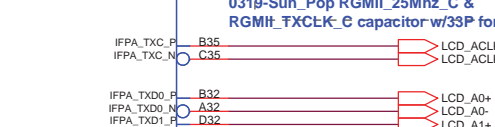
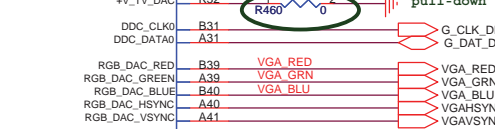
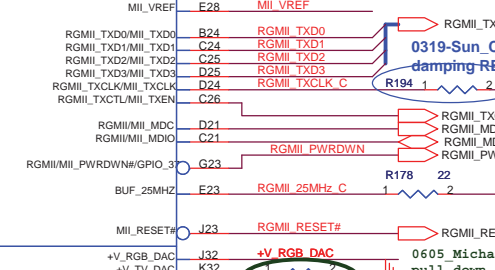
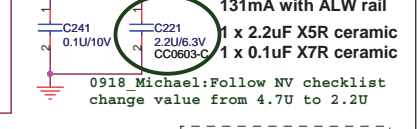
FLAT PANEL



83mA with ALW rail

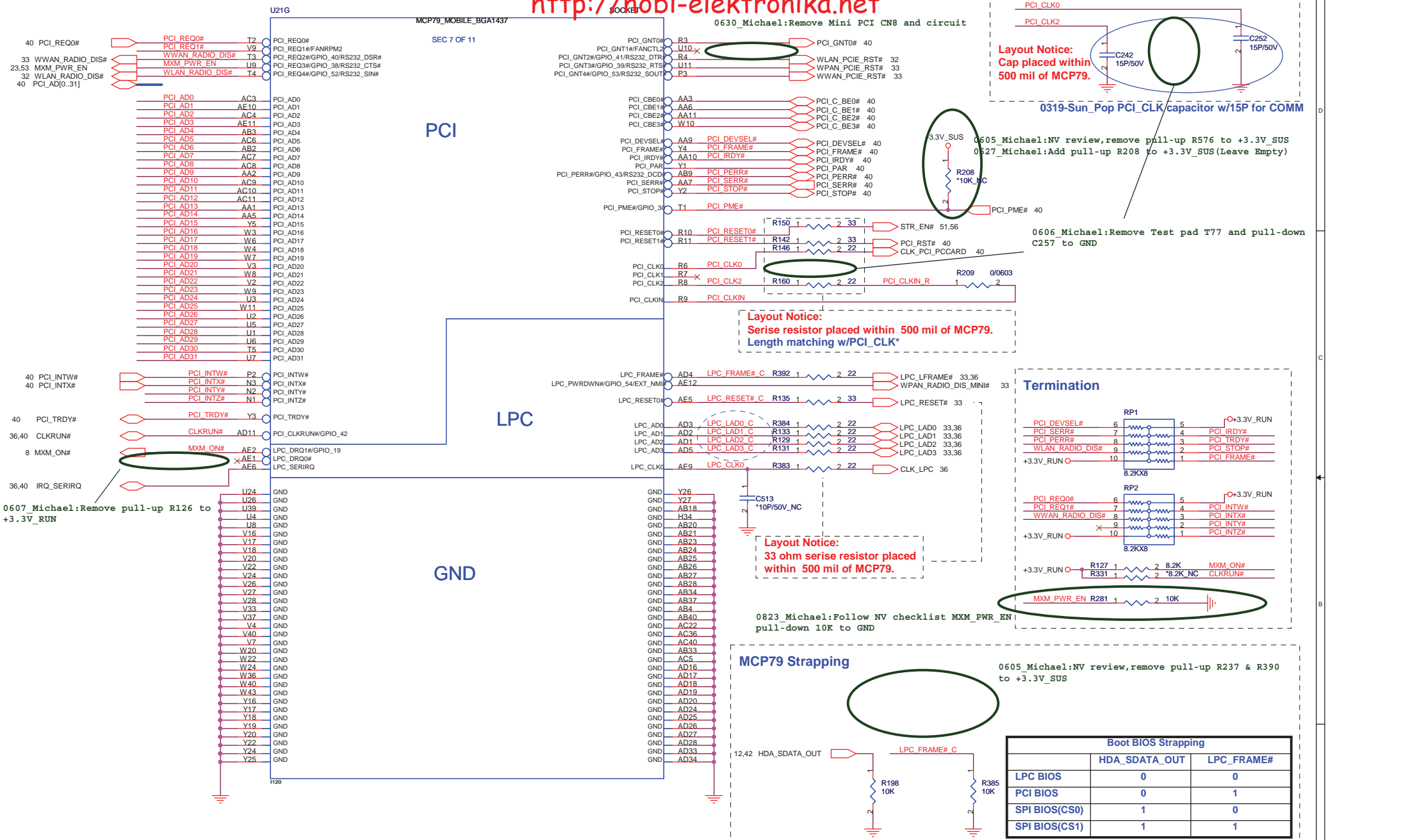


131mA with ALW rail



Layout Note: Place 150 ohm termination resistors close to ATI CHIP.



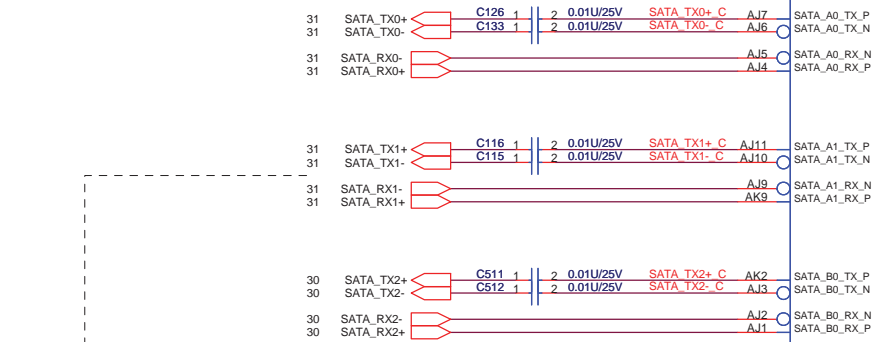


Boot BIOS Strapping

	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS(CS0)	1	0
SPI BIOS(CS1)	1	1



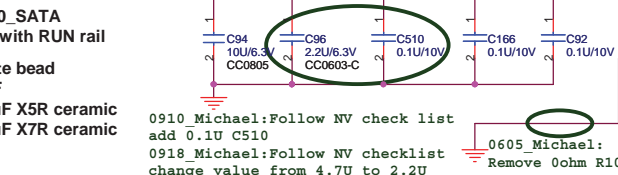
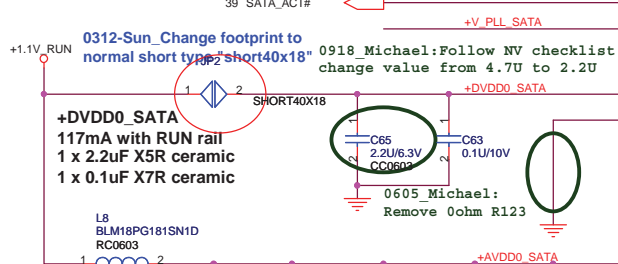
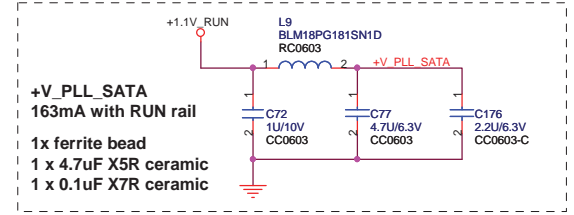
0318-Sun_change left USB port from port1 to port0 for NV remote SW debug.



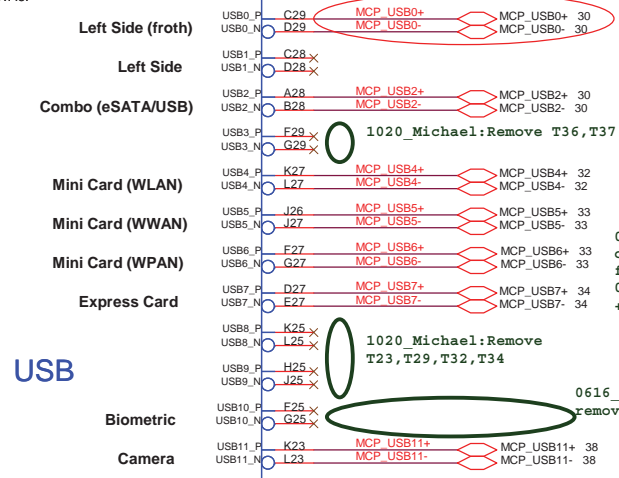
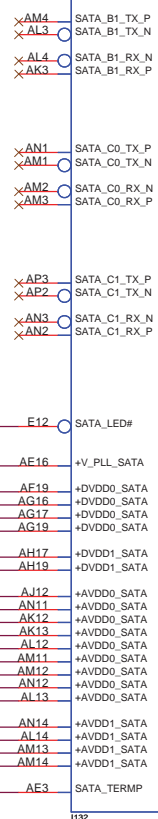
SATA Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 400 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 500 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.

SATA

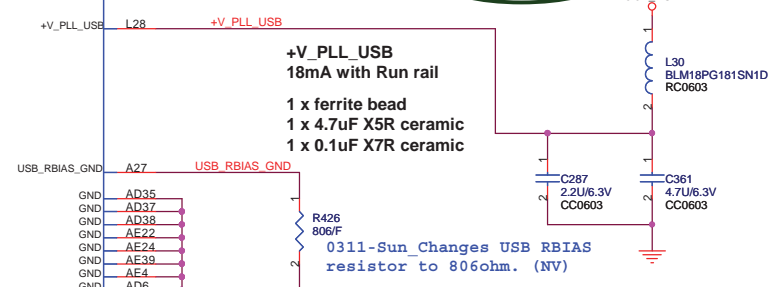
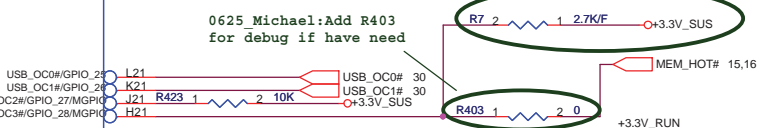
USB



Layout Notice:
 2.49K ohm to GND within 500 mils of MCP79.
 Routing 8 mils spacing to resistor.



- Left Side (froth)
- Left Side
- Combo (eSATA/USB)
- Mini Card (WLAN)
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card
- Biometric
- Camera



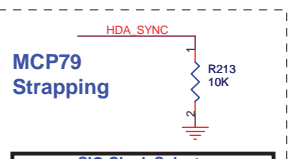
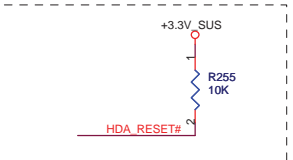
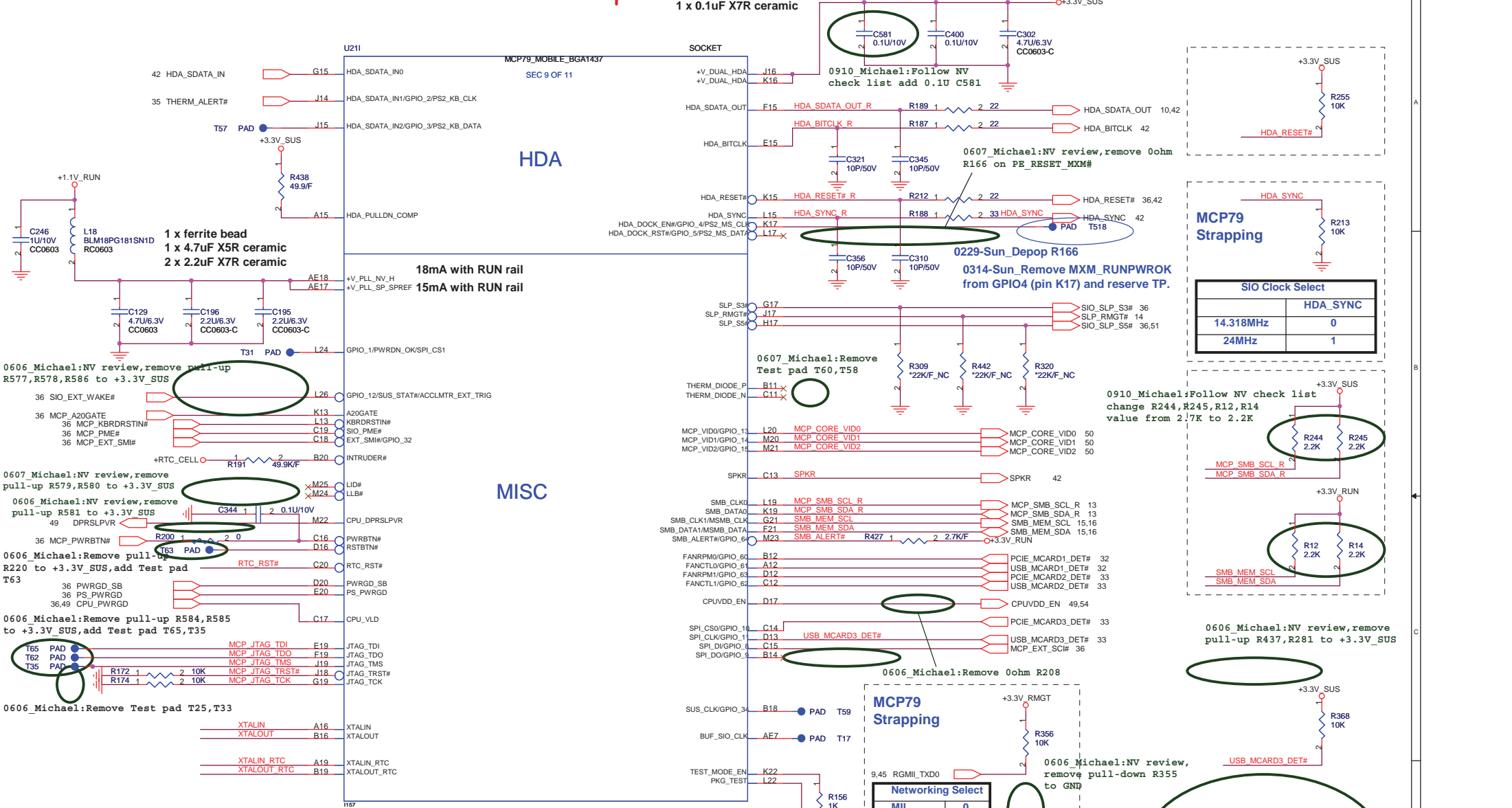
Layout Notice:
 909 ohm +-1% to GND within 1000 mil of MCP79.
 Routing trace at least 8 mil wide to resistor.

USB Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum brackout distance is 300 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA brackout plus Fan-out distance is 400 mils.
After Brackout:
 Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
 Each USB pair must be length matched to within 50 mil.

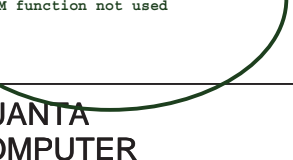
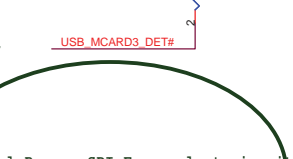
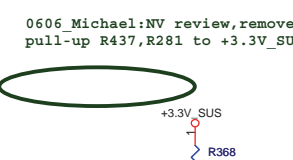
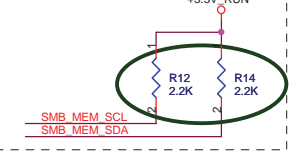
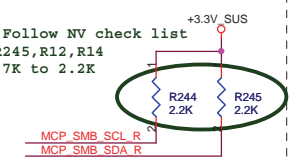


Title MCP79 (SATA,USB)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Monday, October 20, 2008	Sheet 11 of 59

1 x 0.1uF X7R ceramic



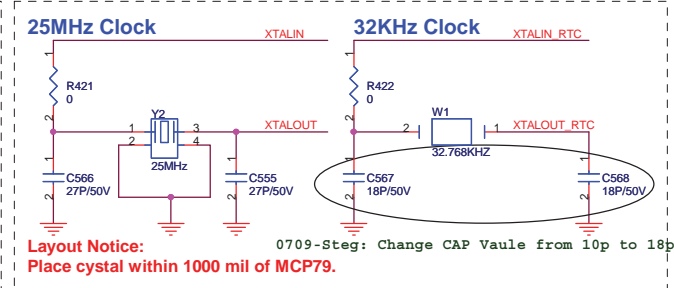
SIO Clock Select	
	HDA_SYNC
14.318MHz	0
24MHz	1



Networking Select	
MII	0
RGMI	1

MCP79 Strapping	
0606 Michael:NV review, remove pull-up R491 to +3.3V_SUS	
Boot Mode Select	
User Mode	0
Safe Mode	1

CLEAR CMOS ONLY	
CLEAR	RTC_RST# 0
NORMAL	RTC_RST# 1



Layout Notice: 0709-Step: Change CAP Vaule from 10p to 18p. Place crystal within 1000 mil of MCP79.

QUANTA COMPUTER

Title: MCP79 (HDA,MISC)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, September 18, 2008 Sheet 12 of 59

1 x 10uF ceramic
 2 x 2.2uF X5R ceramic
 3 x 1uF X5R ceramic
 3 x 0.22uF X5R ceramic
 12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0
 2850mA for S0 Idle

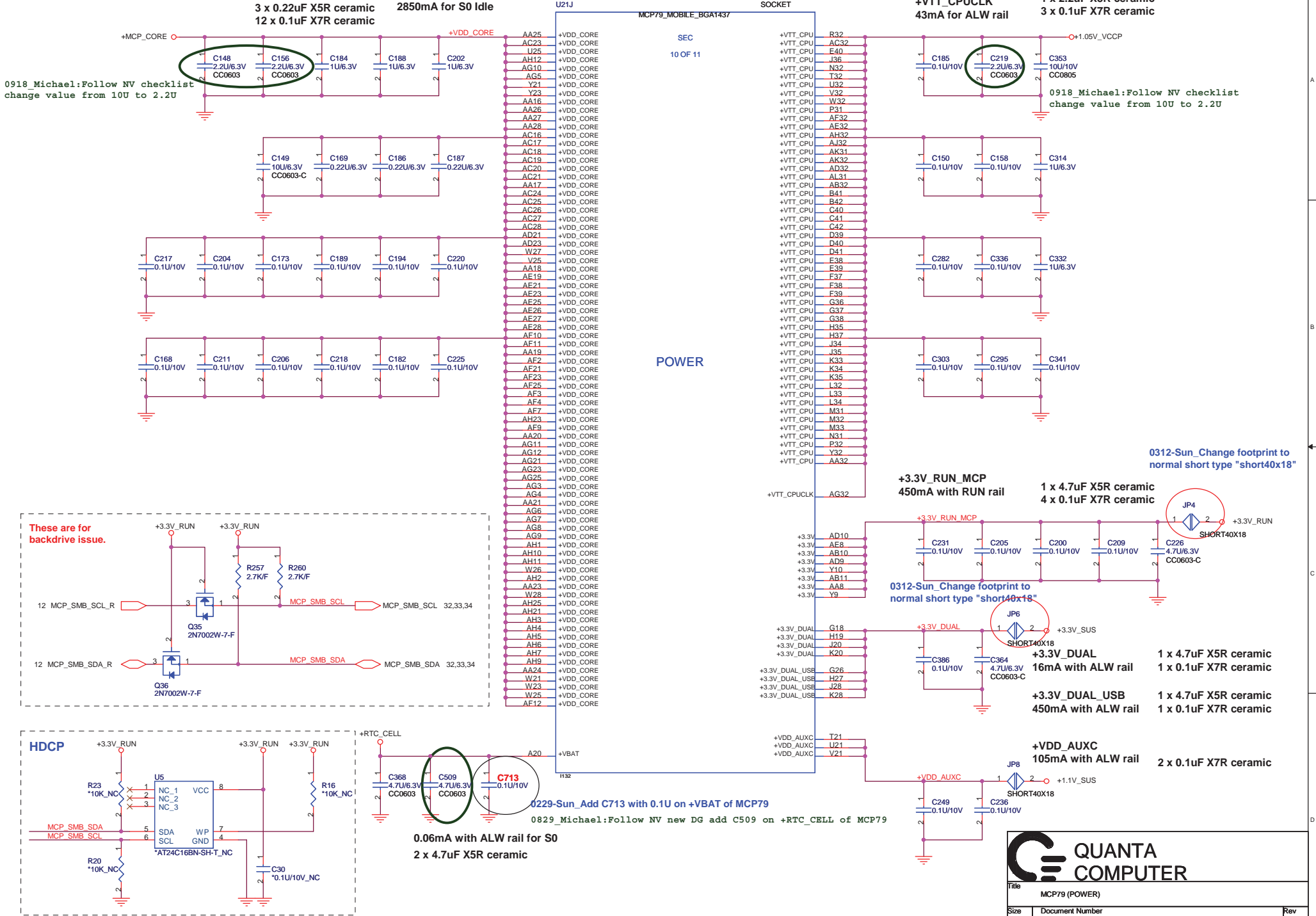
+VTT_CPU
 1139mA for ALW rail

+VTT_CPUCLK
 43mA for ALW rail

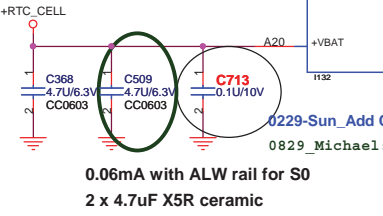
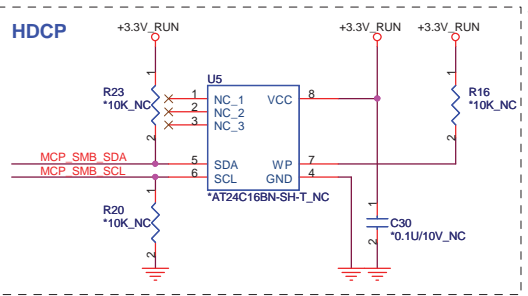
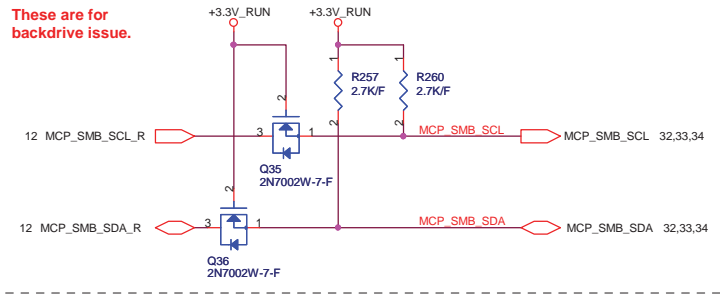
1 x 10uF ceramic
 1 x 2.2uF X5R ceramic
 3 x 0.1uF X7R ceramic

0918 Michael:Follow NV checklist
 change value from 10U to 2.2U

0918 Michael:Follow NV checklist
 change value from 10U to 2.2U



POWER



0229-Sun_Add C713 with 0.1U on +VBAT of MCP79
 0829 Michael:Follow NV new DG add C509 on +RTC_CELL of MCP79

0.06mA with ALW rail for S0
 2 x 4.7uF X5R ceramic

+3.3V_RUN_MCP
 450mA with RUN rail

1 x 4.7uF X5R ceramic
 4 x 0.1uF X7R ceramic

0312-Sun_Change footprint to normal short type "short40x18"

+3.3V_DUAL
 16mA with ALW rail

1 x 4.7uF X5R ceramic
 1 x 0.1uF X7R ceramic

+3.3V_DUAL_USB
 450mA with ALW rail

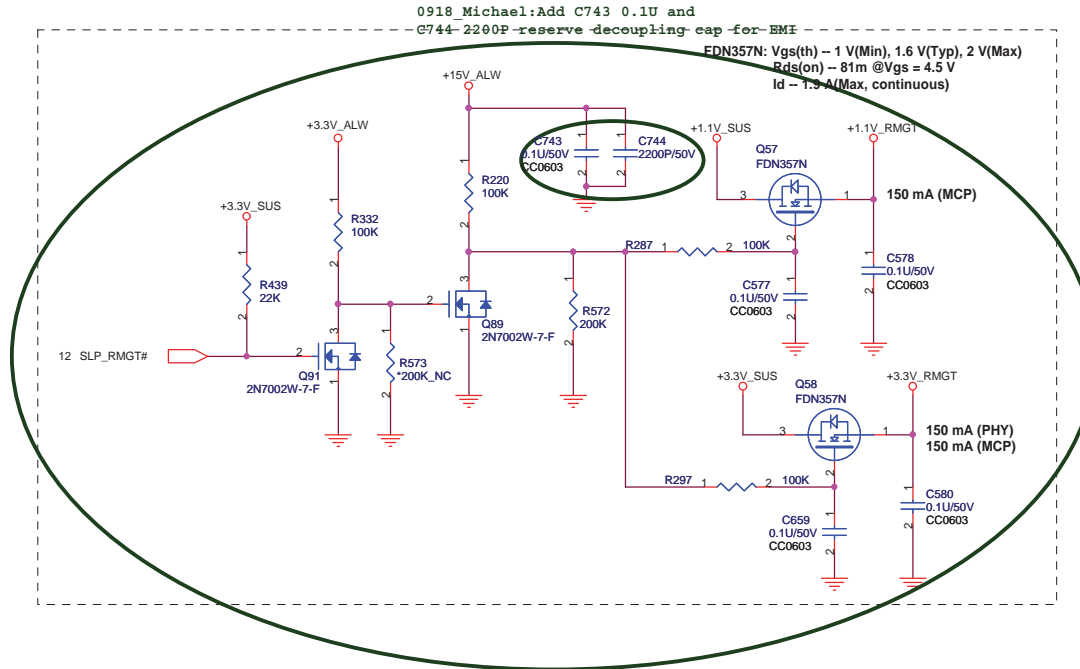
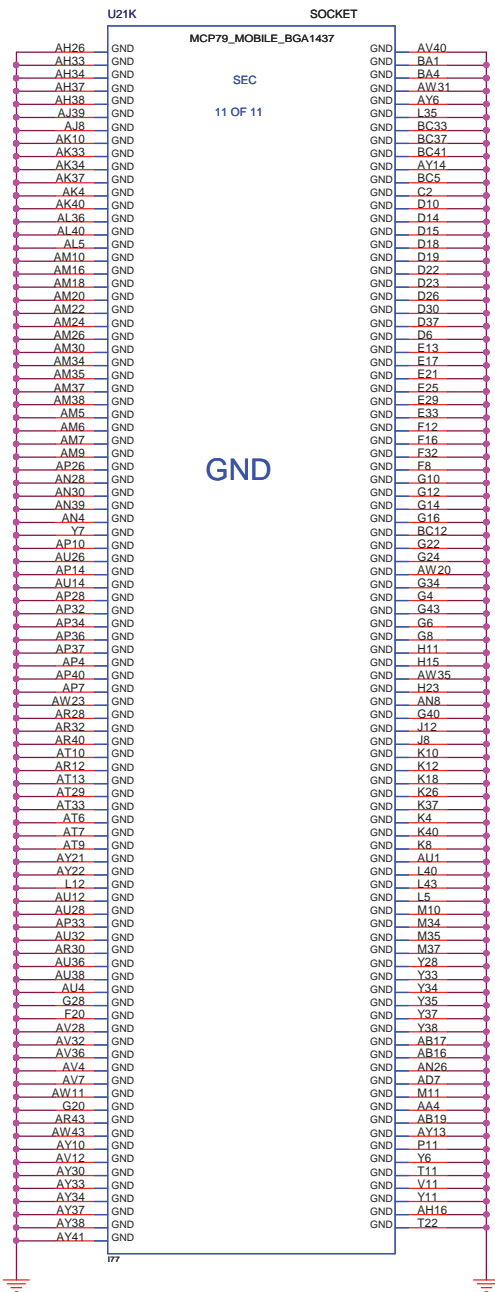
1 x 4.7uF X5R ceramic
 1 x 0.1uF X7R ceramic

+VDD_AUXC
 105mA with ALW rail

2 x 0.1uF X7R ceramic



Title MCP79 (POWER)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Friday, September 19, 2008	Sheet 13 of 59



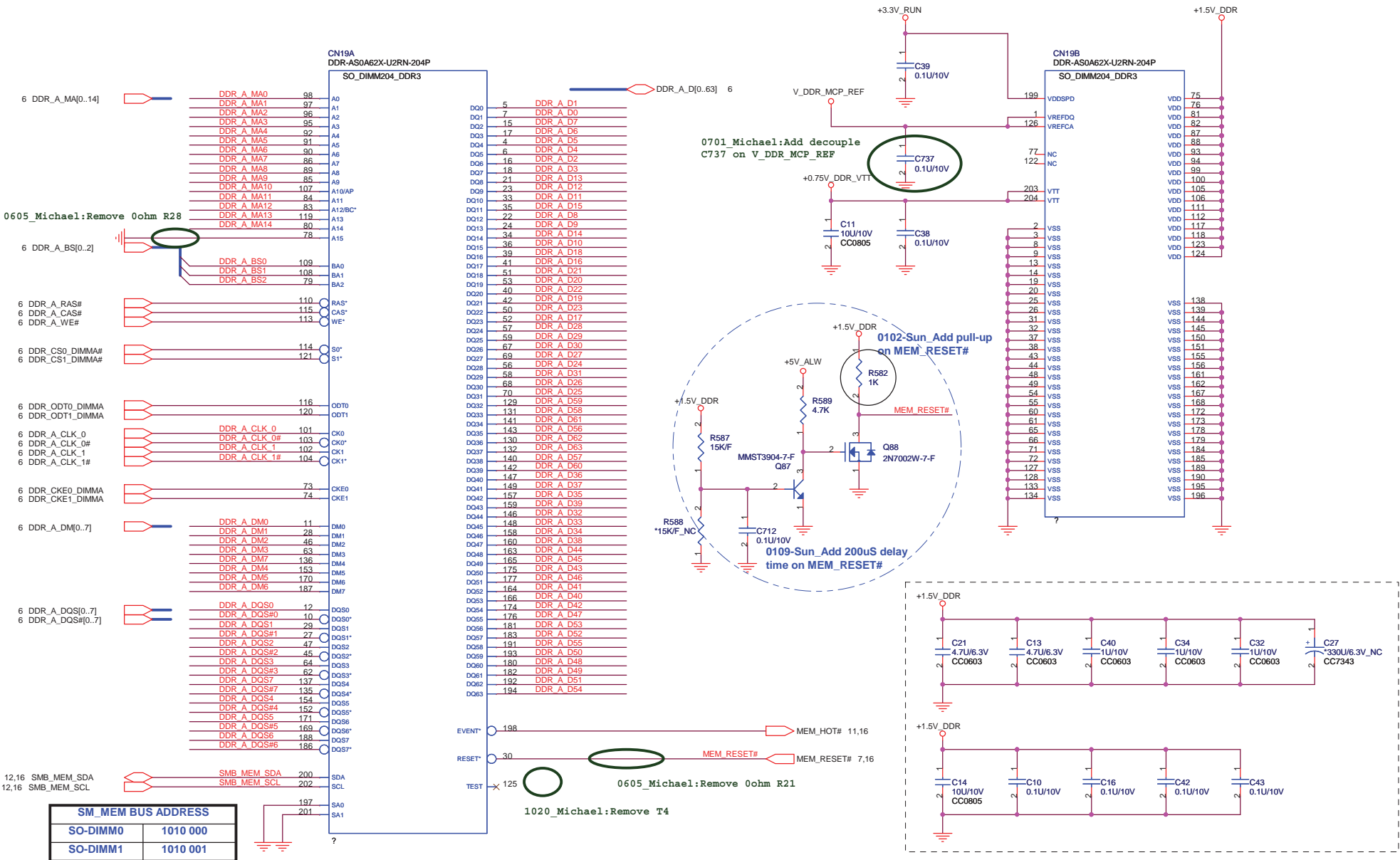
0229-Sun 1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB (Del JP11, JP12)

Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3

Add Q89 with 2N7002, R591 with 10K

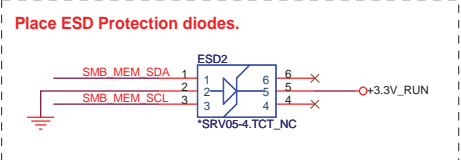
0825 Michael: Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F, R&C for +1.1V_RMGT and +3.3V_RMGT power low issue





For EMI Reserved

DDR_A_CLK_1 R19 1 *200/F_NC DDR_A_CLK_1#
 DDR_A_CLK_0 R30 1 *200/F_NC DDR_A_CLK_0#

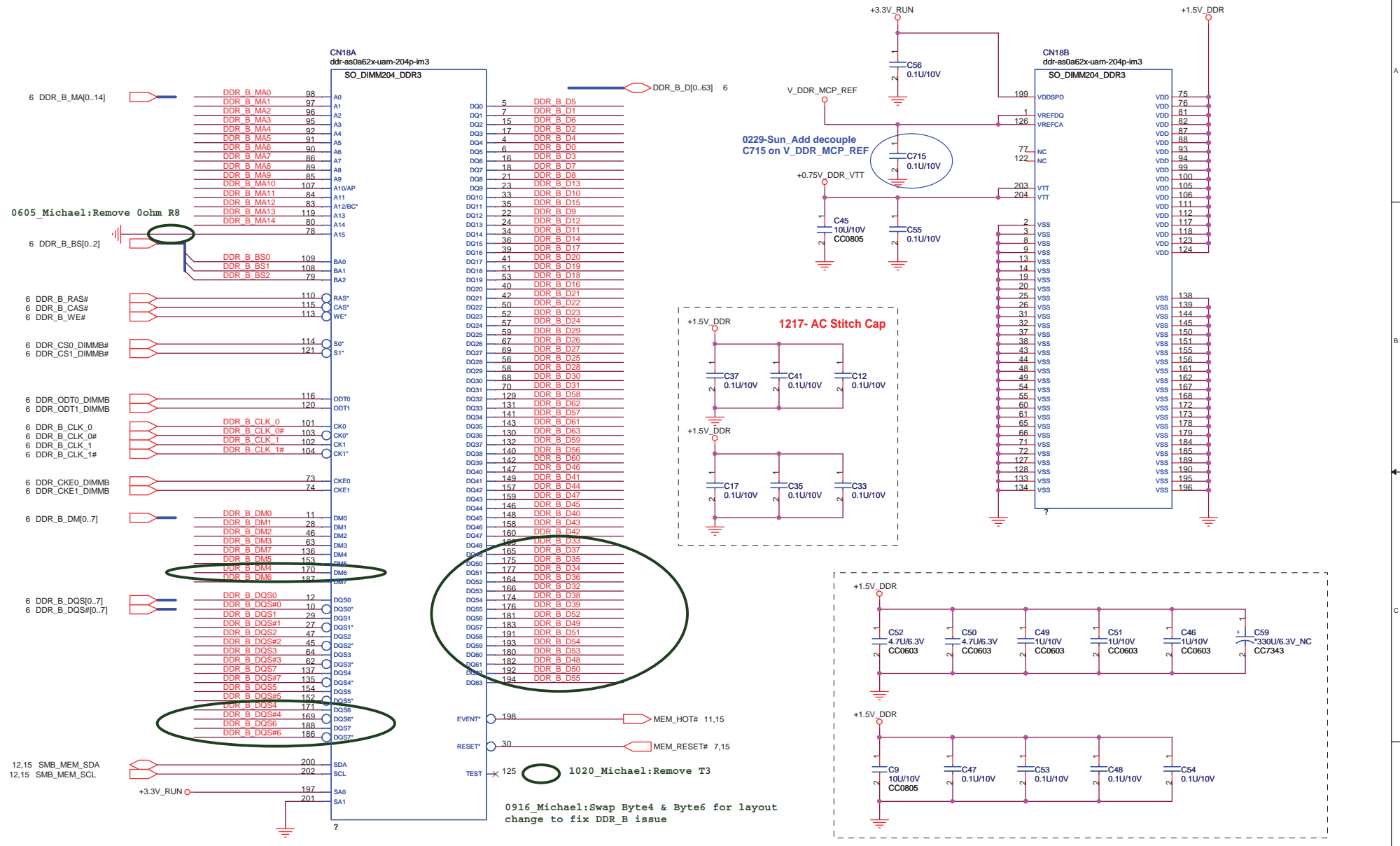


QUANTA COMPUTER

Title: DDR3 SO-DIMM (204P)

Size: Document Number IM3 (XPS-Joie) Rev 2A

Date: Monday, October 20, 2008 Sheet 15 of 59

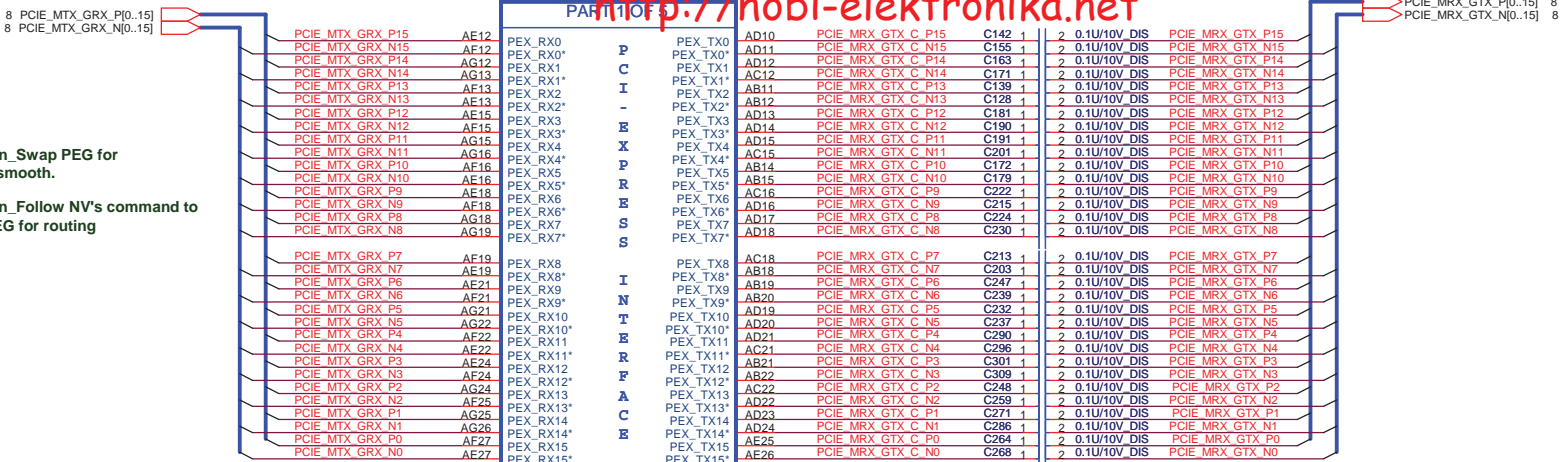


For EMI Reserved
 DDR_B_CLK_1 R9 1 2 *200/F NC DDR_B_CLK_1#
 DDR_B_CLK_0 R11 1 2 *200/F NC DDR_B_CLK_0#

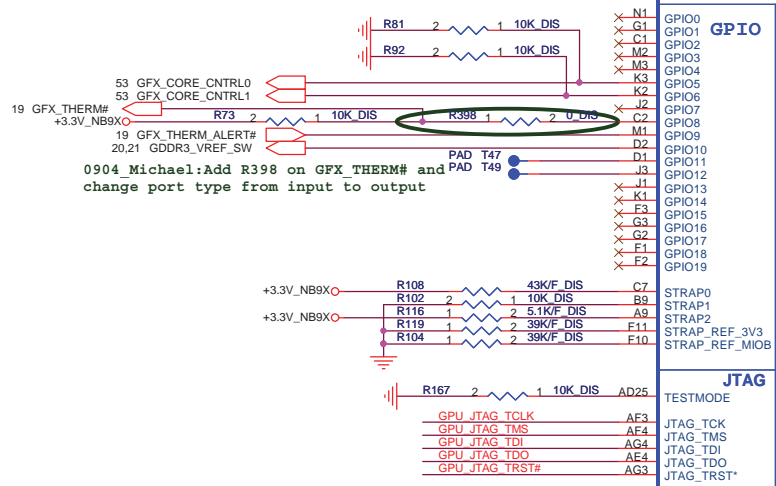


1113-Sun_Swap PEG for routing smooth.
1115-Sun_Follow NV's command to swap PEG for routing

IM3 dedicated.

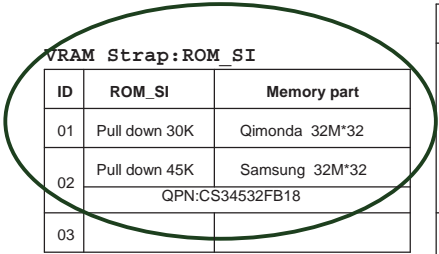


1115-Sun_Follow NV's command to swap PEG for routing smooth

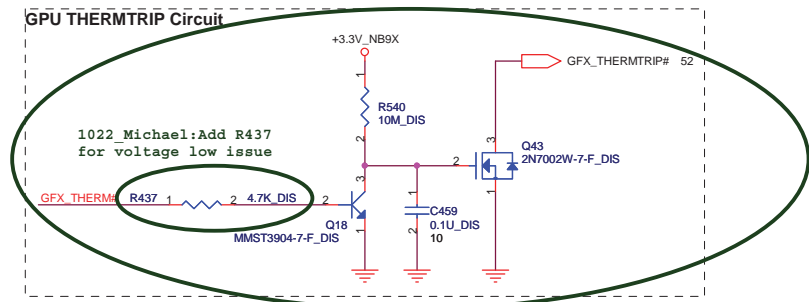
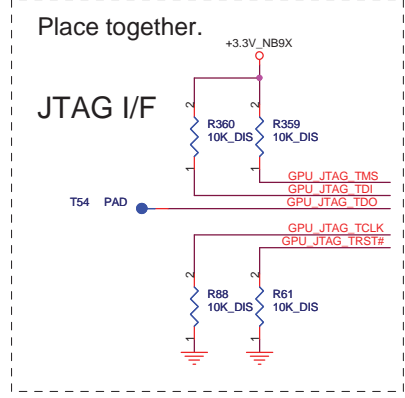


GPIO USAGE

GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVVDD ALTV0	
6	OUT	HIGH	NVVDD ALTV1	
7	OUT	HIGH	FBVDD VIDO	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No

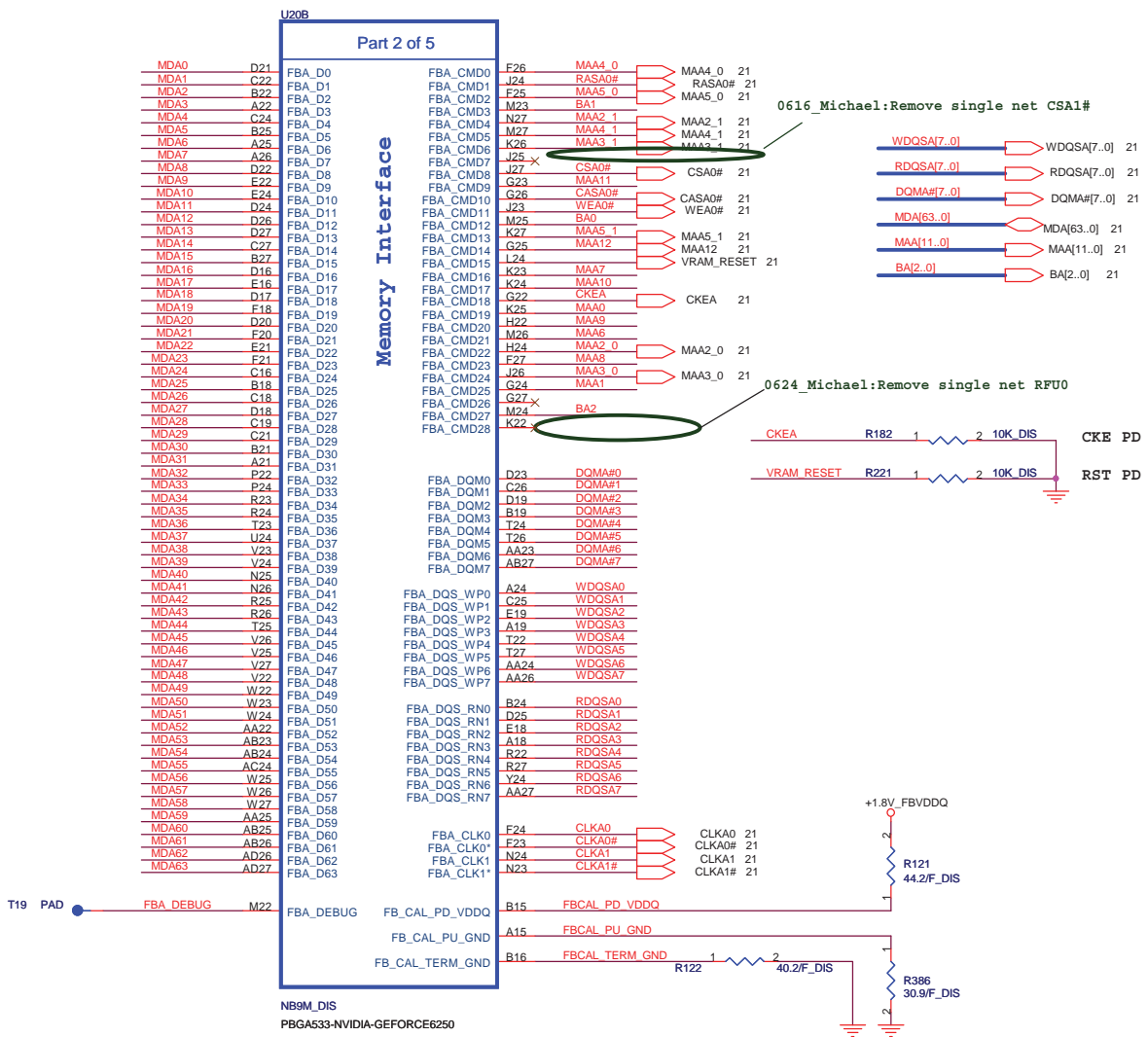


0604_Michael: Follow NV command to modify VRAM Strap resistor vaule



0825 Michael: Modify THERMTRIP circuit, add MOS and CAP





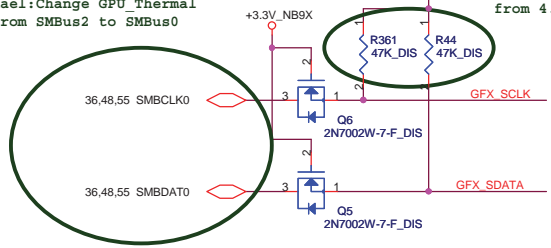
Update as "PUN-03303-001_V01".

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

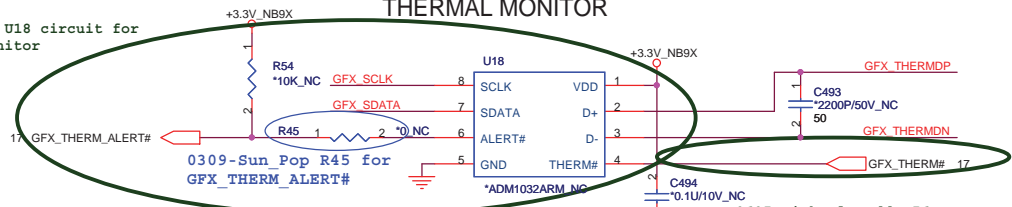
Note: Use only 1% resistors for driver calibration



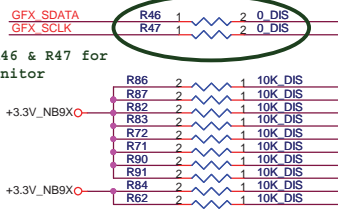
0627 Michael:Change GPU_Thermal control from SMBus2 to SMBus0



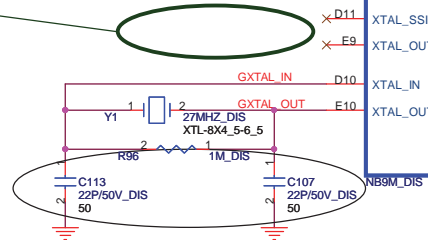
0708 Michael:Depop U18 circuit for internal thermal monitor



0708 Michael:Pop R46 & R47 for internal thermal monitor



0701 Michael:Remove SPREAD SPECTRUM circuit

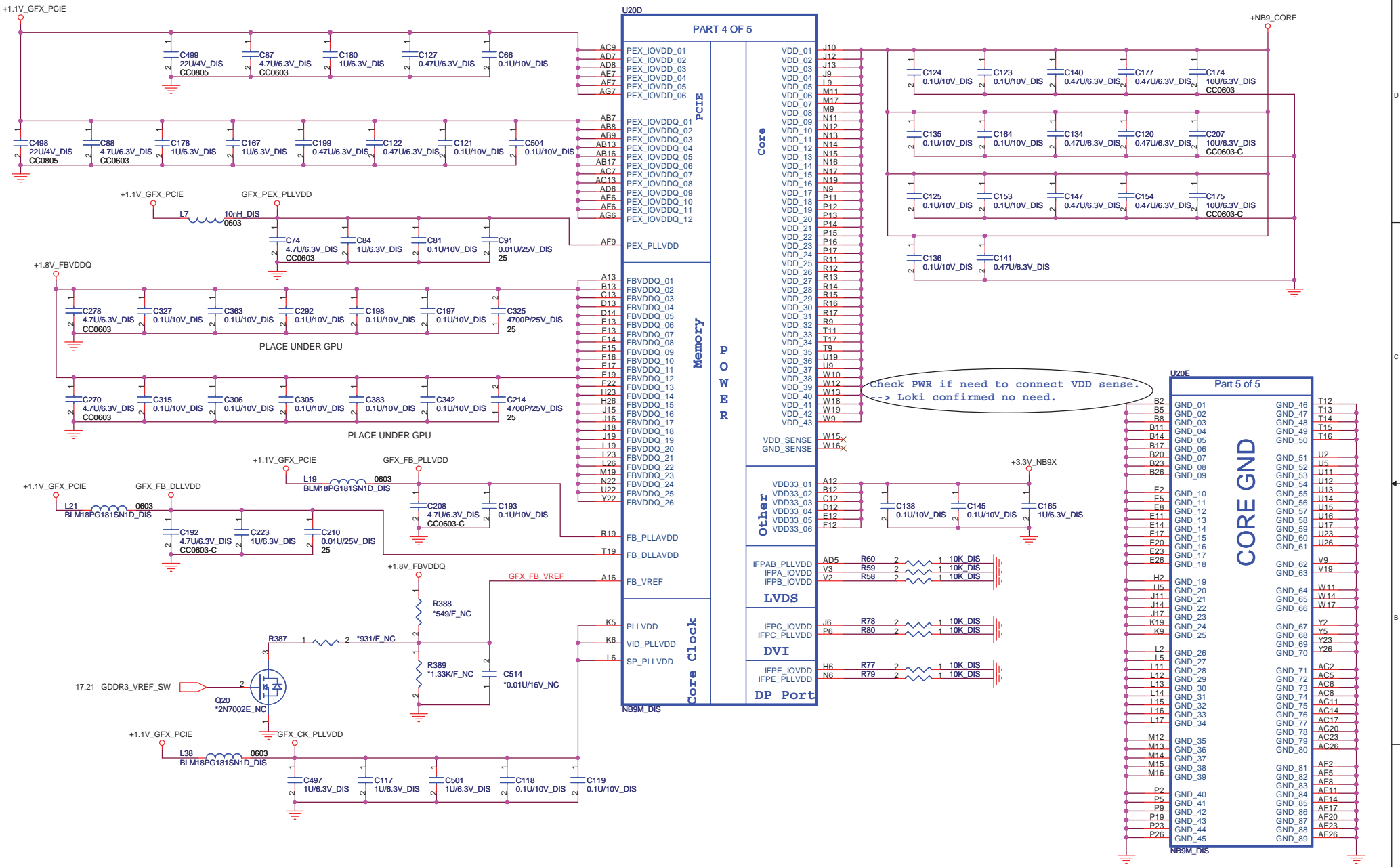


0709-Steg: Change CAP Value from 18p to 22p

PART 3 OF 5					
DVI	G5	IFPC_AUX*	IFPA_TXD0	V5	
	G4	IFPC_AUX	IFPA_TXD0*	V4	
	H4	IFPC_L3*	IFPA_TXD1	AA5	
	K4	IFPC_L2*	IFPA_TXD1*	AA4	
	L4	IFPC_L2	IFPA_TXD2	W4	
LVDS	M4	IFPC_L1*	IFPA_TXD2*	AB4	
	N4	IFPC_L1	IFPA_TXD3	AB5	
	P4	IFPC_L0*	IFPA_TXD3*	AC4	
	R5	IFPC_L0	IFPA_TXC	AD4	
		IFPC_RSET	IFPA_TXC*		
	DP Port	F5	IFPE_L0	IFPB_TXD4	W1
		F4	IFPE_L0*	IFPB_TXD4*	V1
		E4	IFPE_L1	IFPB_TXD5	W3
		D5	IFPE_L1*	IFPB_TXD5*	W2
		C3	IFPE_L2	IFPB_TXD6	AA2
C4		IFPE_L2*	IFPB_TXD6*	AA3	
B3		IFPE_L3	IFPB_TXD7	AB1	
B4		IFPE_L3*	IFPB_TXD7*	AA1	
D3		IFPE_AUX	IFPB_TXC	AB3	
D4		IFPE_AUX*	IFPB_TXC*	AB2	
HDA	M6	IFPE_RSET	IFPAB_RSET	AB6	
	A7	HDA_BCLK	DACA_RED	AE2	
DACA	B7	HDA_SYNC	DACA_GREEN	AE3	
	A6	HDA_SDI	DACA_BLUE	AD3	
	B6	HDA_SDO	DACA_HSYNC	AD2	
	C6	HDA_RST*	DACA_VSYNC	AD1	
THERMAL	F9	SPDIF	DACA_VDD	AG	
	D9	THERMDP	DACA_VREF	AF1	
	D8	THERMDN	DACA_RSET	AE1	
	T2	I2CS_SDA	DACB_RED	F7	
SERIAL BUS	T1	I2CS_SCL	DACB_GREEN	E7	
	W6	I2CE_SDA	DACB_BLUE	E6	
	Y6	I2CE_SCL	DACB_CSYNCS	D6	
	N3	I2CD_SDA	DACB_VDD	D7	
	N2	I2CD_SCL	DACB_VREF	G6	
	A2	I2CC_SDA	DACB_RSET	F8	
	R3	I2CC_SCL	DACC_RED	T5	
	R2	I2CB_SDA	DACC_GREEN	T4	
	T3	I2CB_SCL	DACC_BLUE	R4	
	R1	I2CA_SDA	DACC_HSYNC	U6	
Clock	D11	XTAL_SSIN	DACC_VSYNC	U4	
	E9	XTAL_OUTBUFF	DACC_VDD	W5	
	D10	XTAL_IN	DACC_VREF	R6	
	E10	XTAL_OUT	DACC_RSET	V6	

Reserve CRT for debug on first build.
Remove all of parts except DACA_VDD supply before QT
1020 Michael: Remove T48, T52, T50, T53, T51, R49, C89, R89





**QUANTA
COMPUTER**

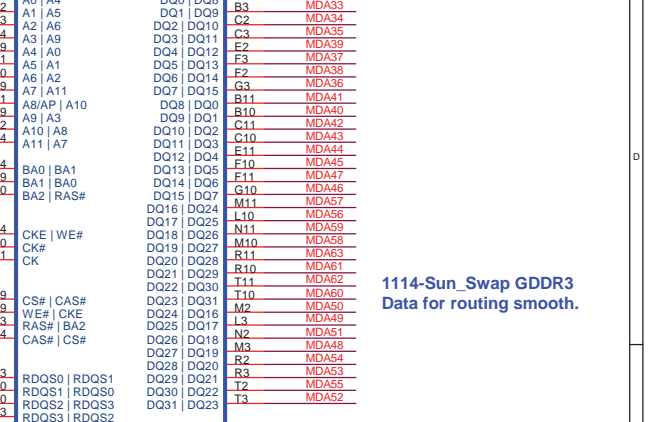
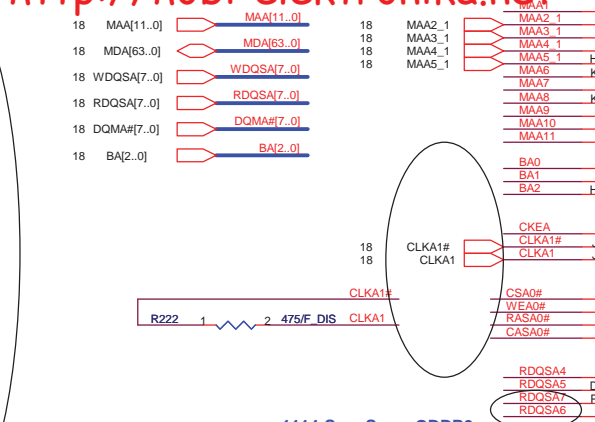
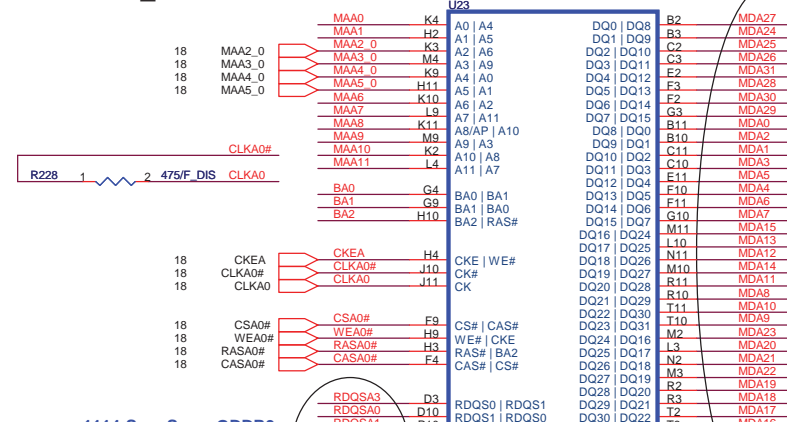
Title: VGA-NB9X GB1-64 (POWER,GND)

Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Friday, September 05, 2008 Sheet 20 of 59

GDDR3_M*32

http://hobi-elektronika.net

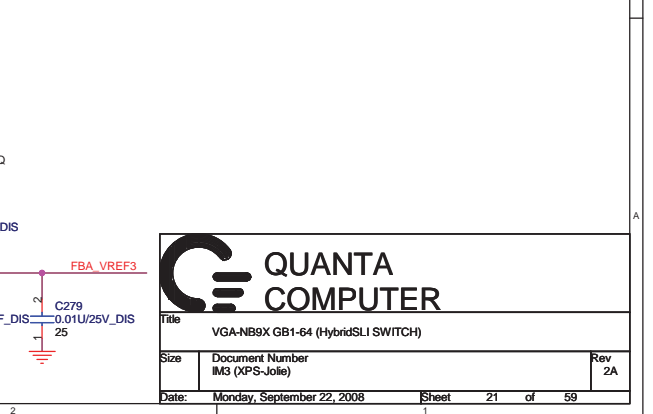
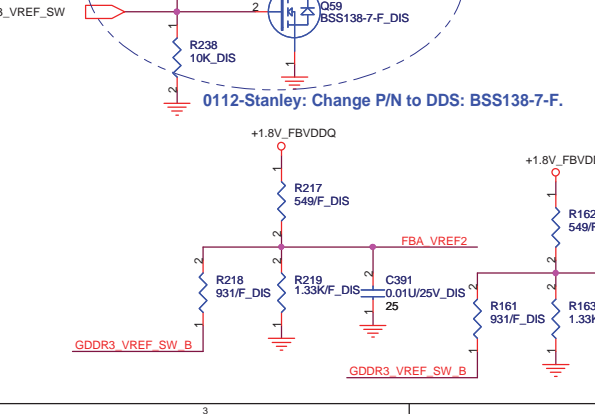
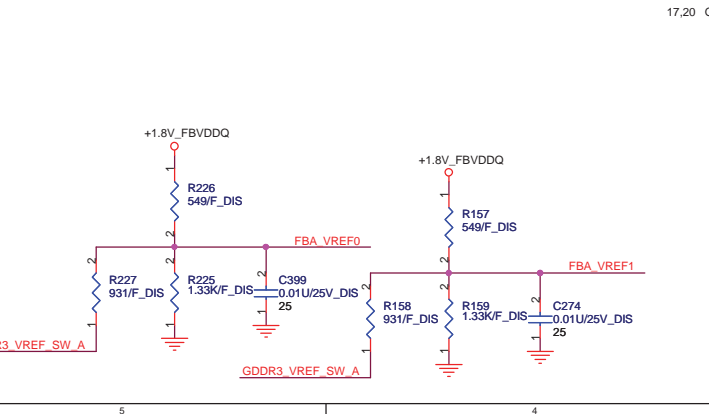
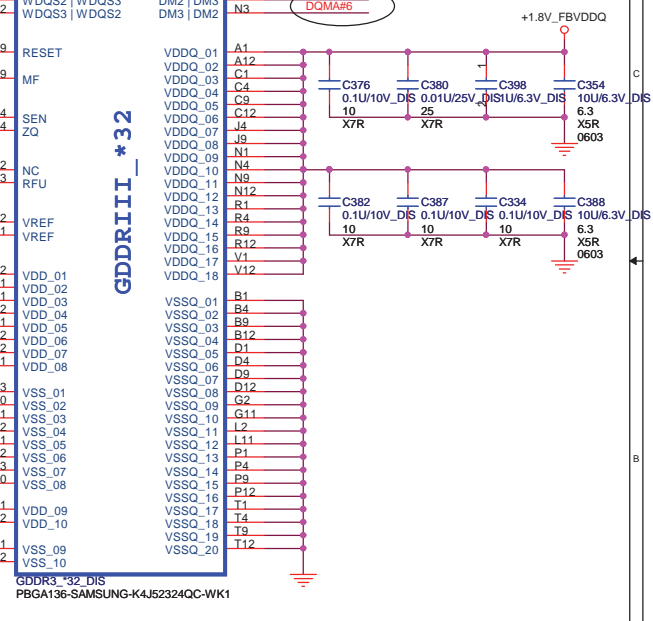
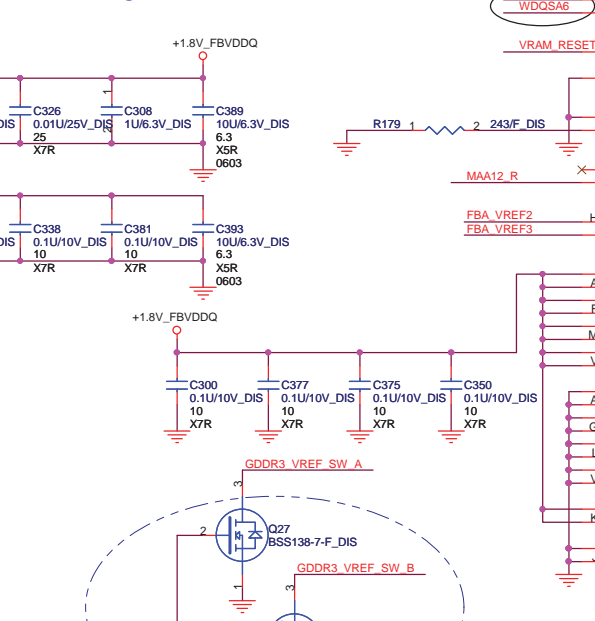
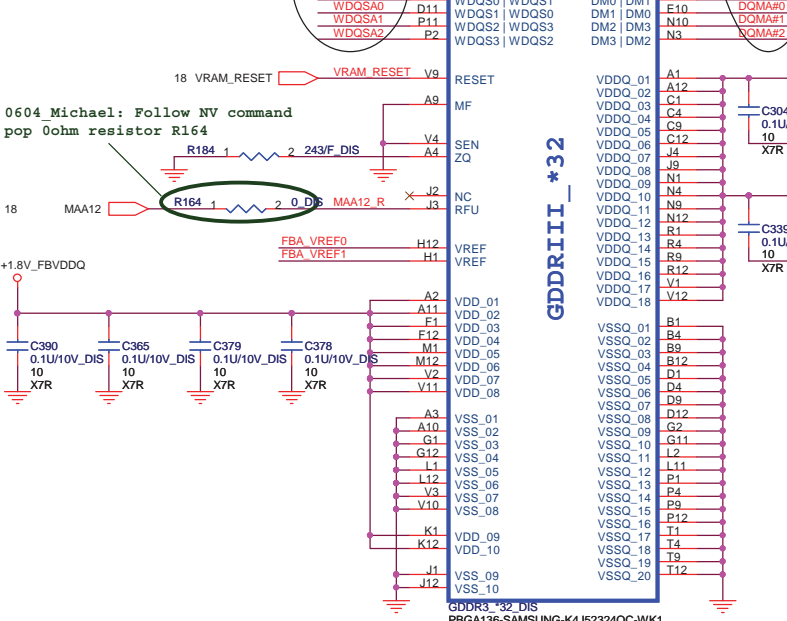


1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.



0112-Stanley: Change P/N to DDS: BSS138-7-F.

QUANTA COMPUTER

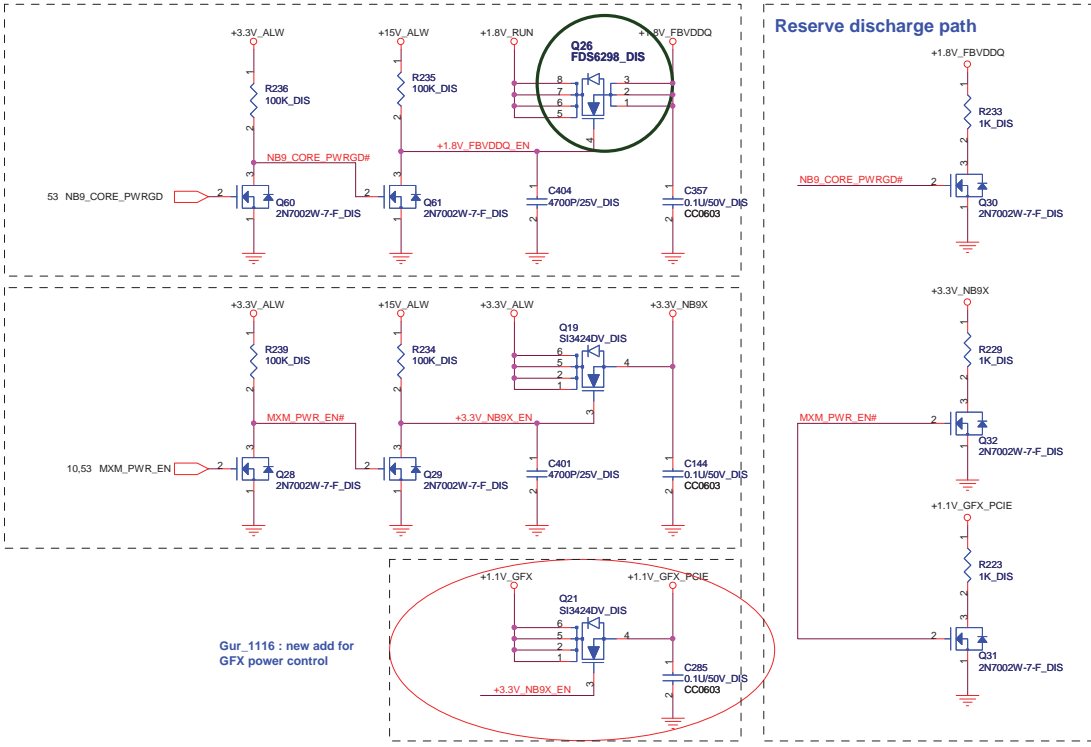
Title: VGA-NB9X GB1-64 (HybridSLI SWITCH)

Size: Document Number IM3 (XP-S-Jolie) Rev 2A

Date: Monday, September 22, 2008 Sheet 21 of 59

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

1225-Sun_Chenge Q26 from SI4812BDY to SI4800BDY-T1-E3
 1022_Michael:Change Q26 from SI4800BDY-T1-E3 to BAM62980005



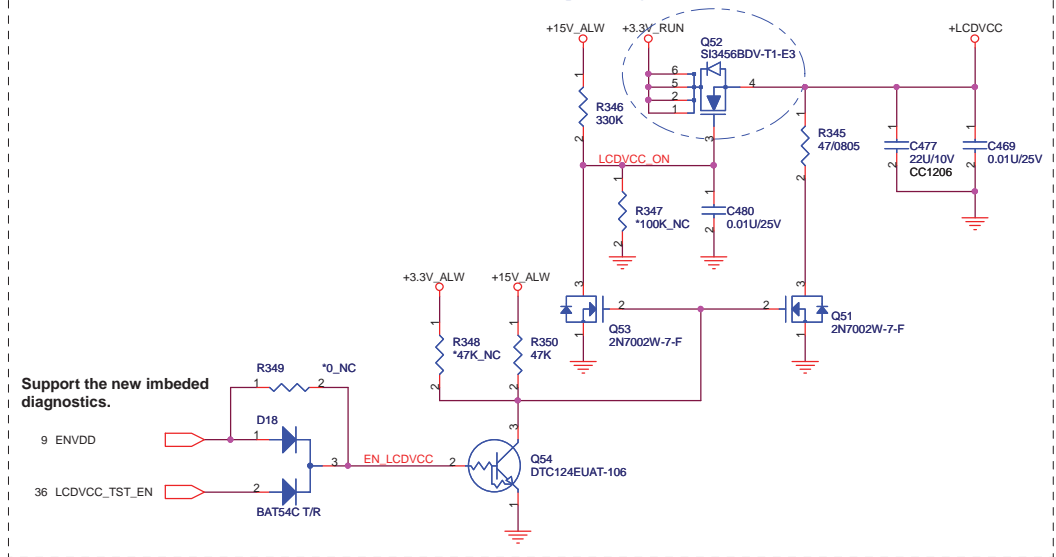
Gur_1116 : new add for GFX power control

**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

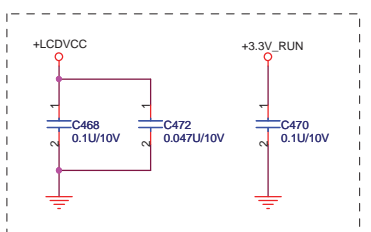
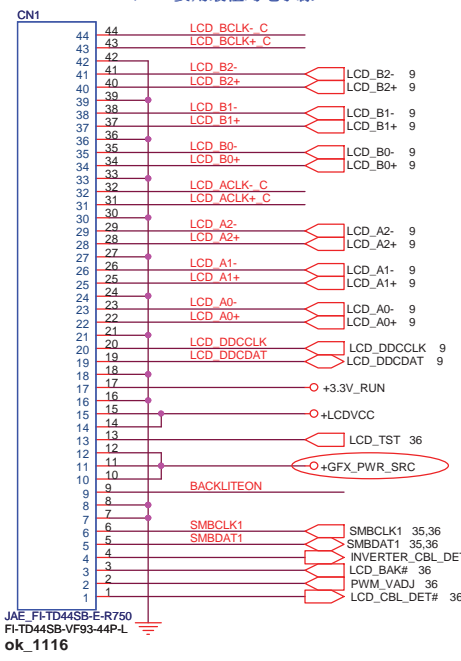
**BLANK PAGE FOR PAGE
NUMBER SAME AS DISCRETE**

0112-Stanley: Change BOM for EOL issue (SI3456BDV).

GND,VCC要用最粗的電子線



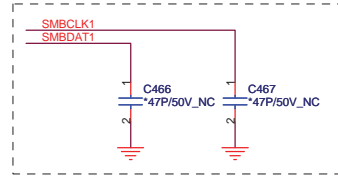
Support the new imbedded diagnostics.



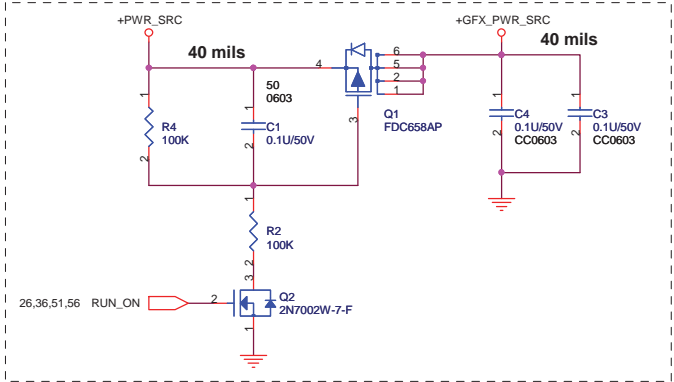
WXGA 1280*800=>70 MHz
 WXGA+ 1440*900=>108 MHz
 WSXGA+ 1680*1050=>120MHz
 WUXGA 1920*1200=>166 MHz

Address : A9H --Contrast
 AAH --Backlight

MBRAI specification of antenna gain is
 10dBi@474MHz, -7dBi@698MHz,
 -5dBi@858MHz.

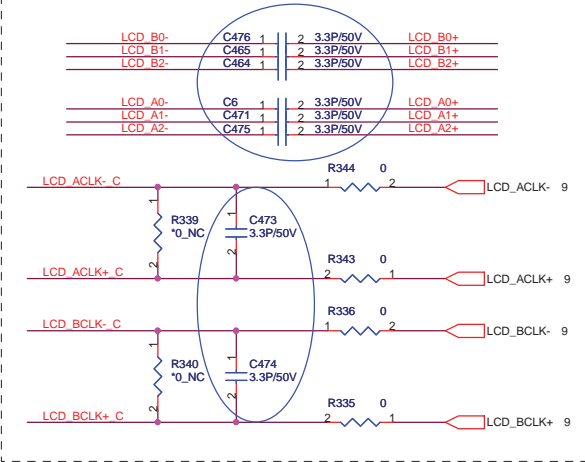


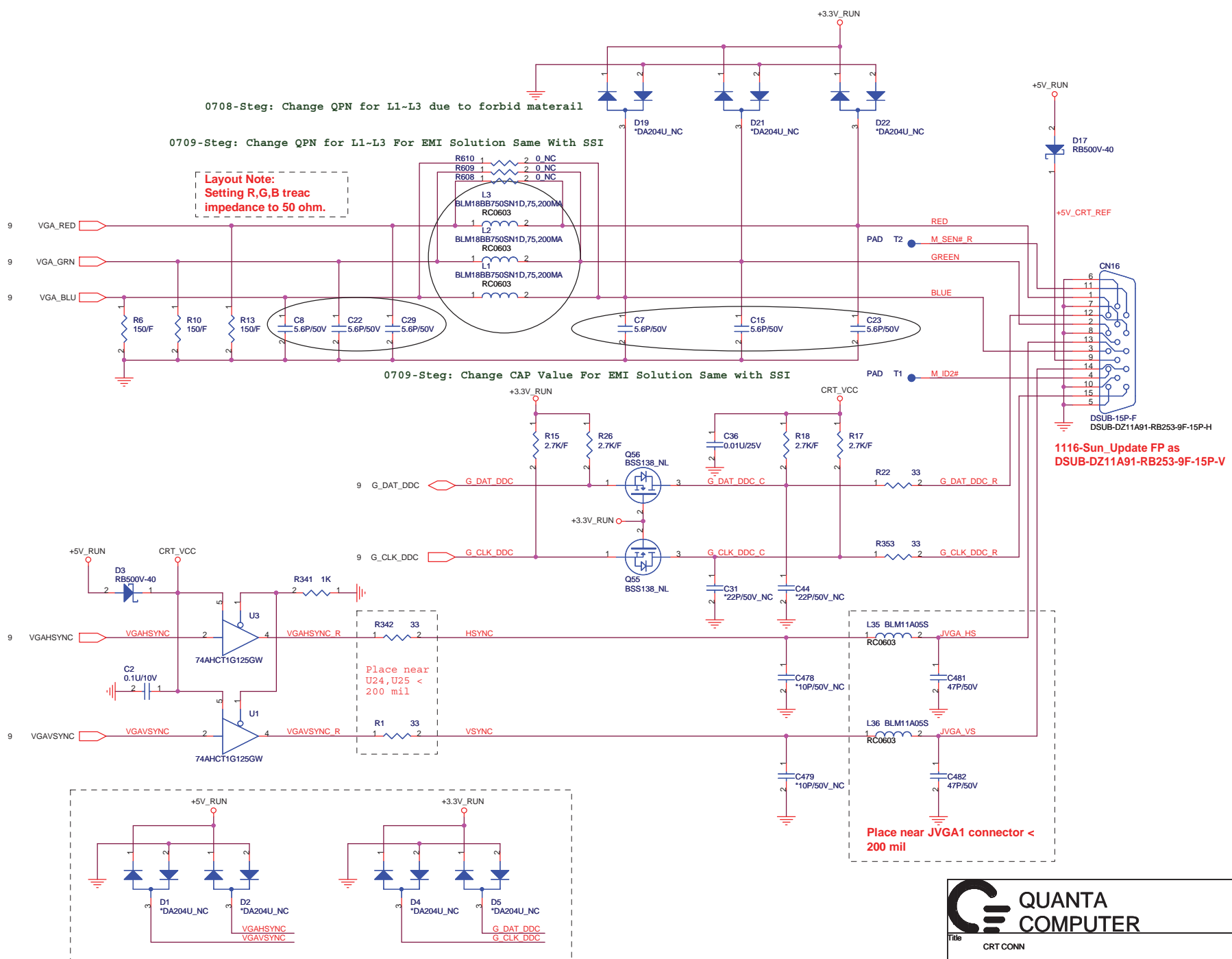
Populate R65 for DPST implementation only.
 Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

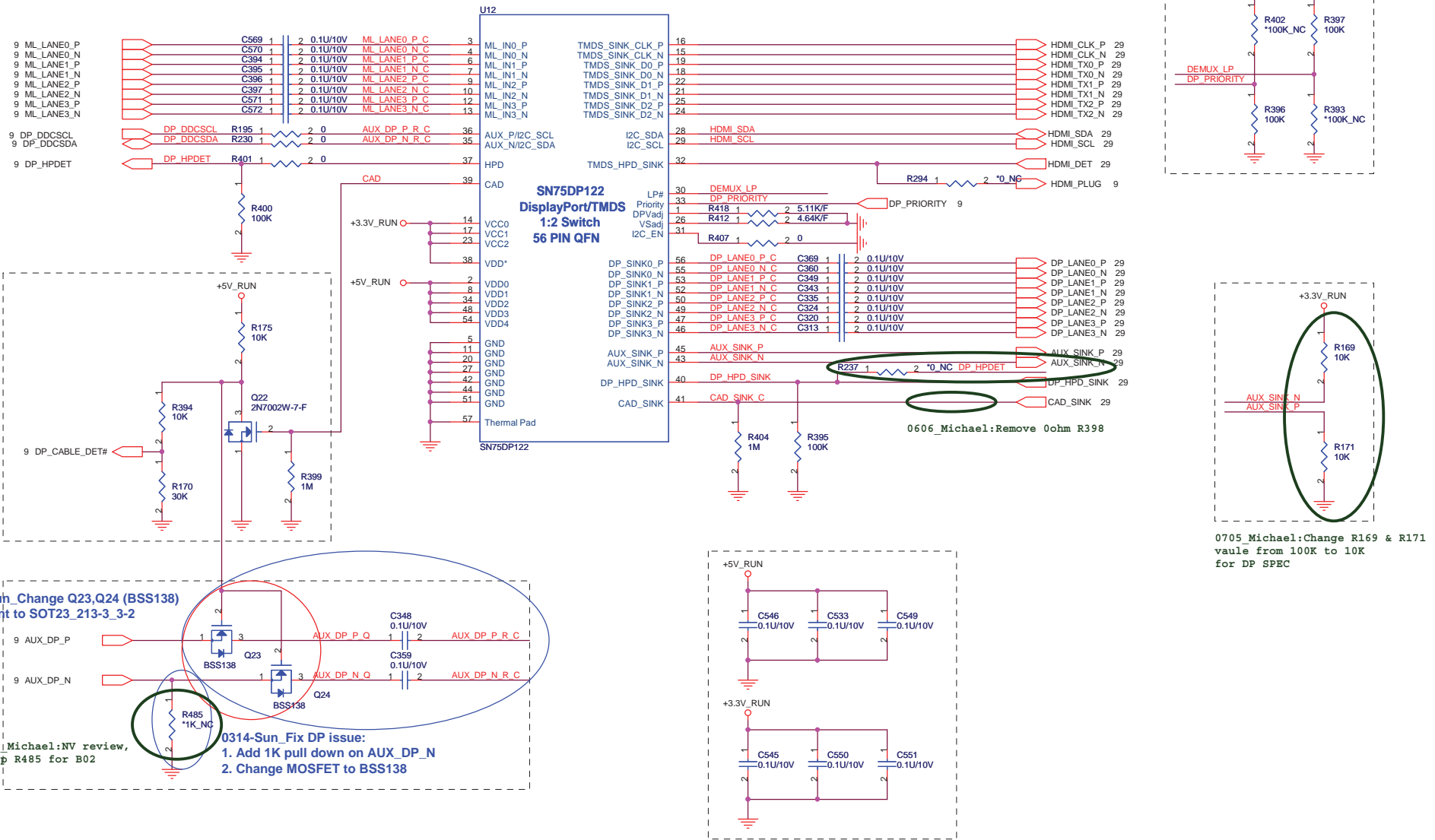


0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

Shunt capacitors on LVDS for improving WWAN.





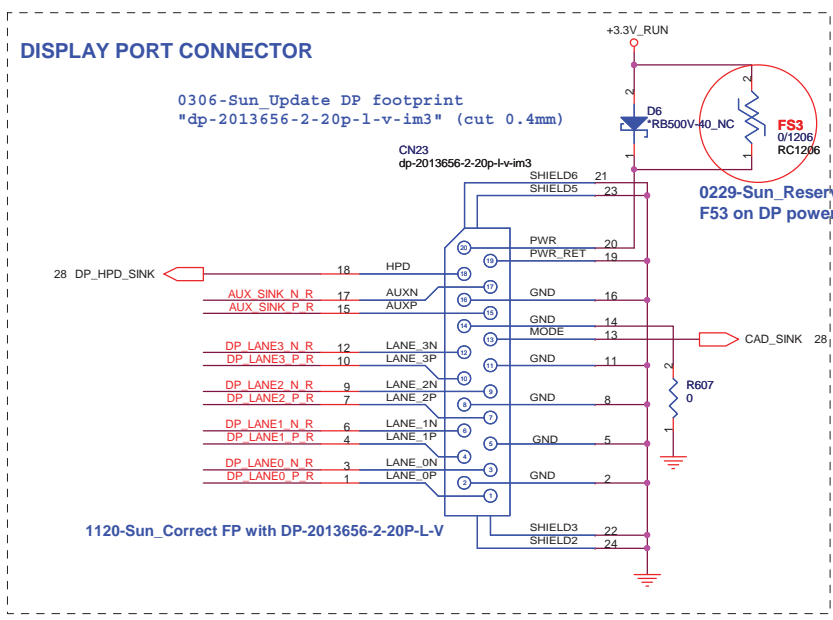
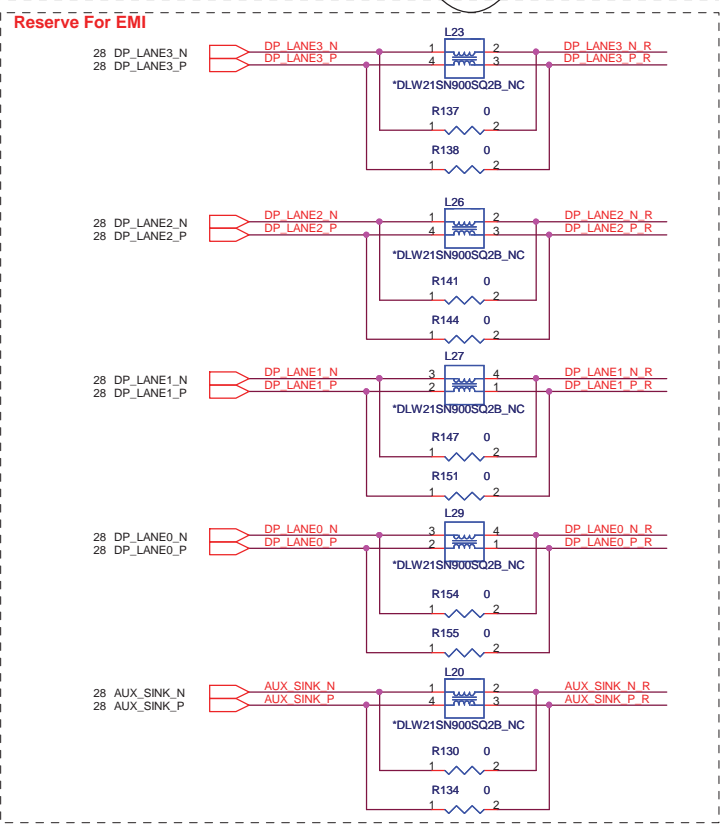
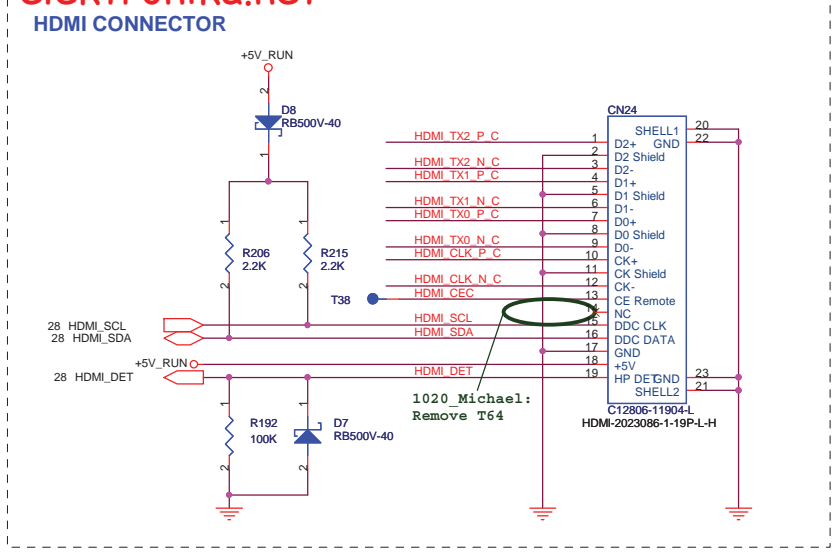
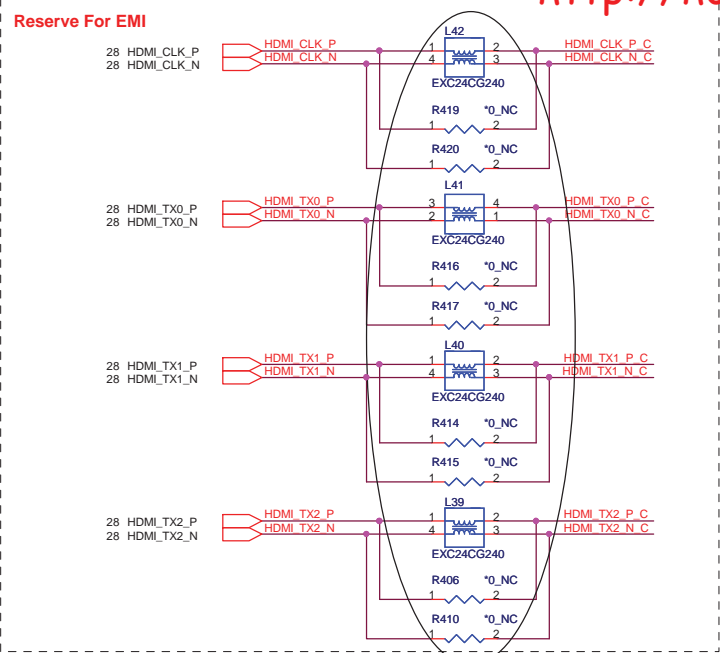


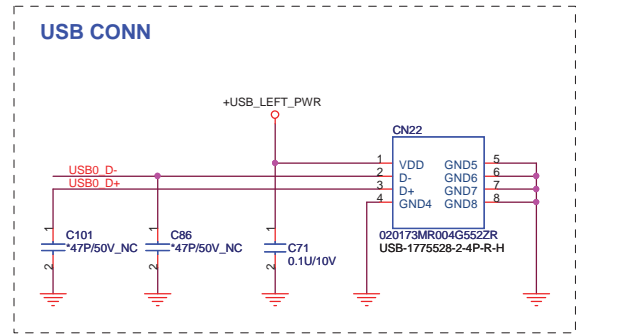
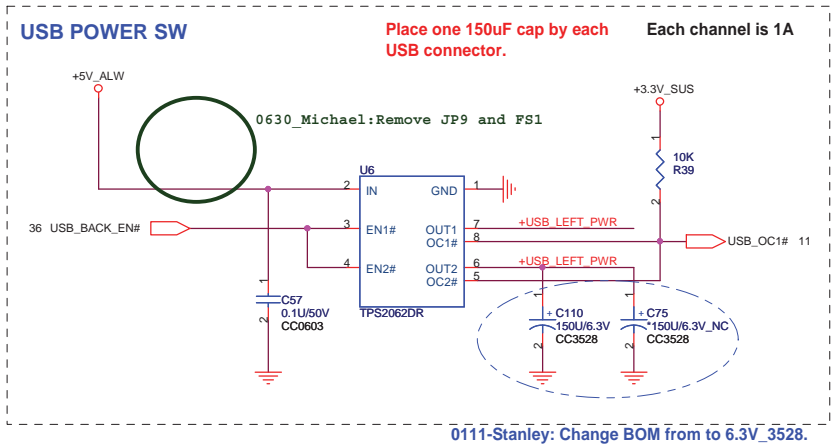
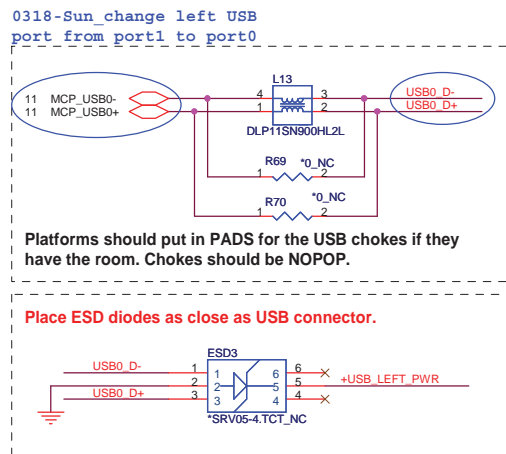
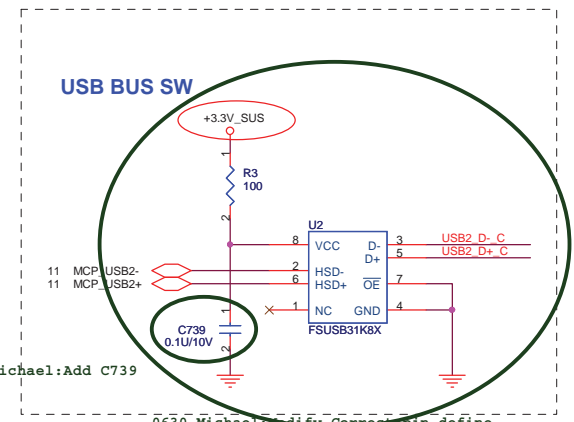
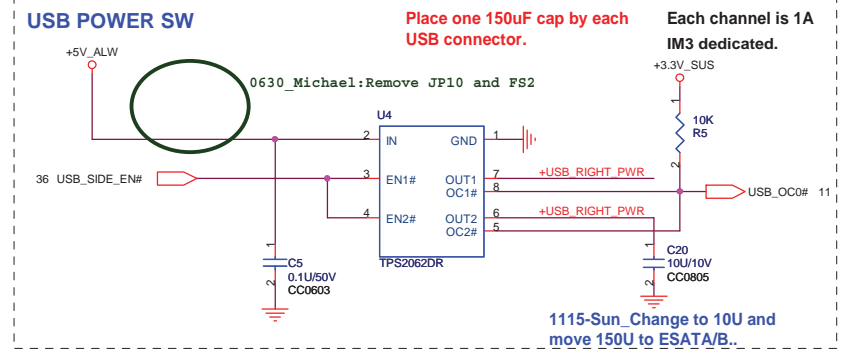
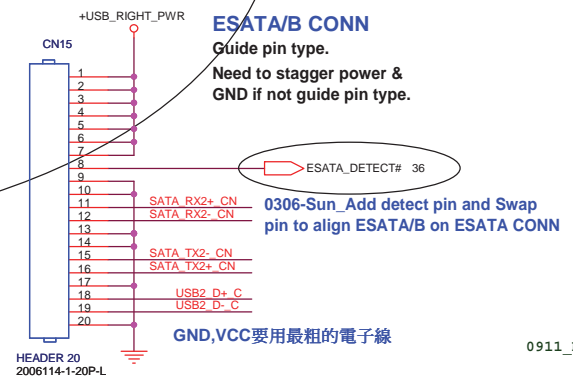
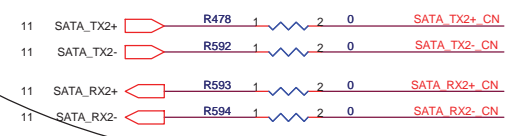
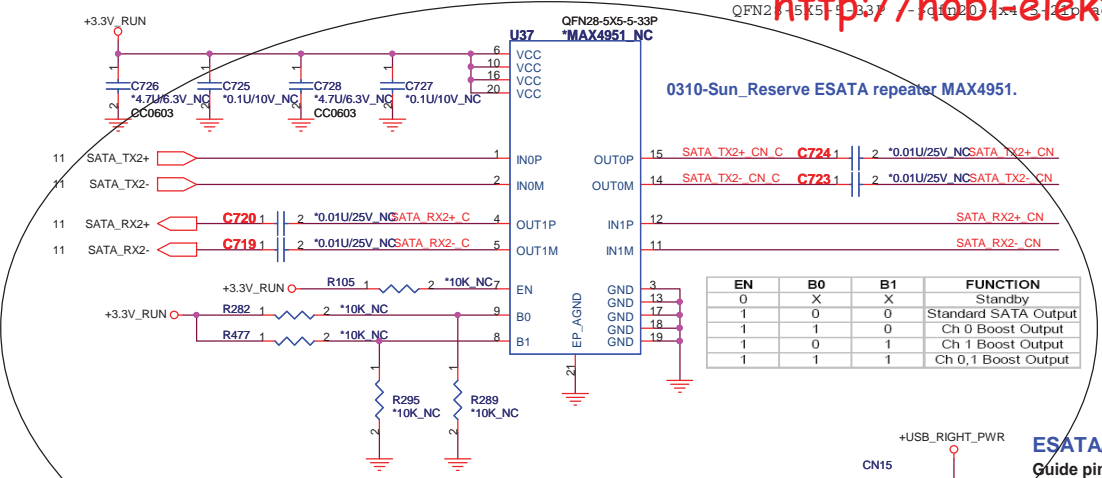
QUANTA COMPUTER

Title: DeMUX Switch (SN75DP122)

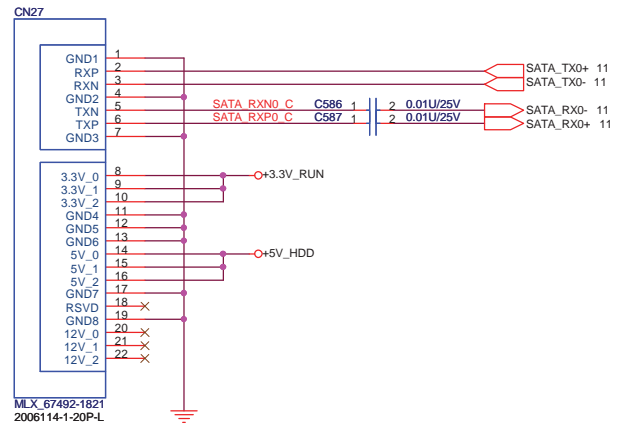
Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Friday, September 05, 2008 Sheet 28 of 59

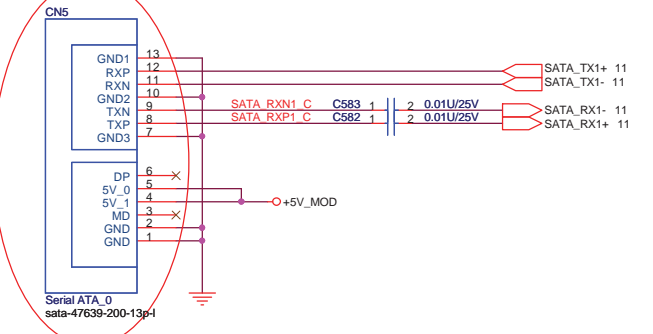




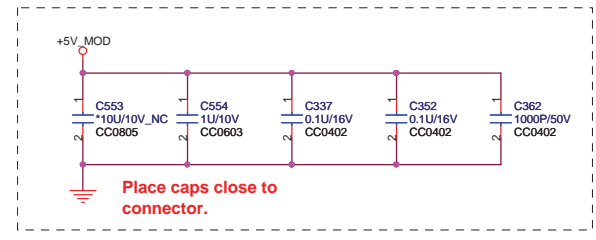
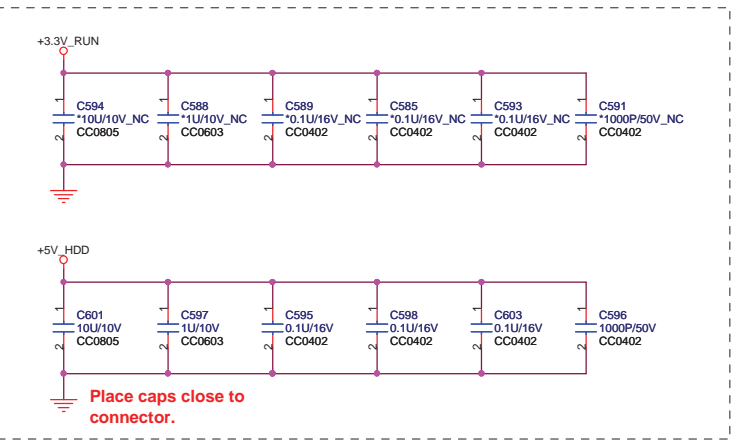
SATA HDD Connector



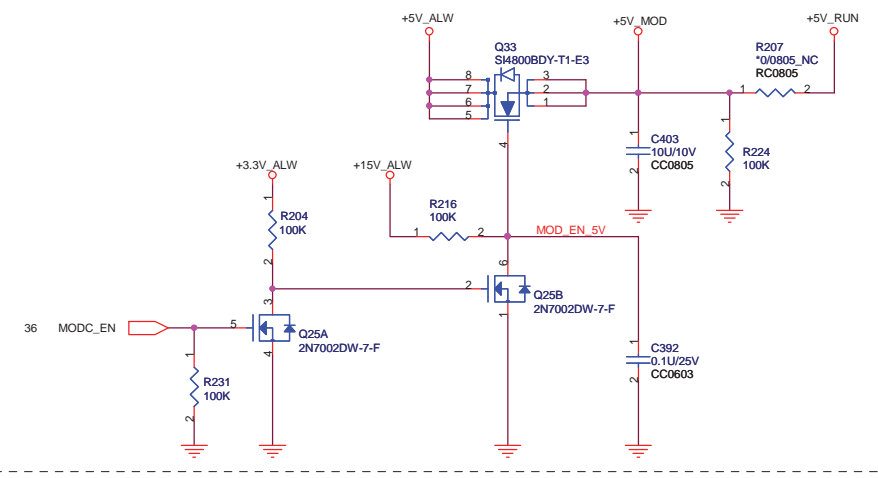
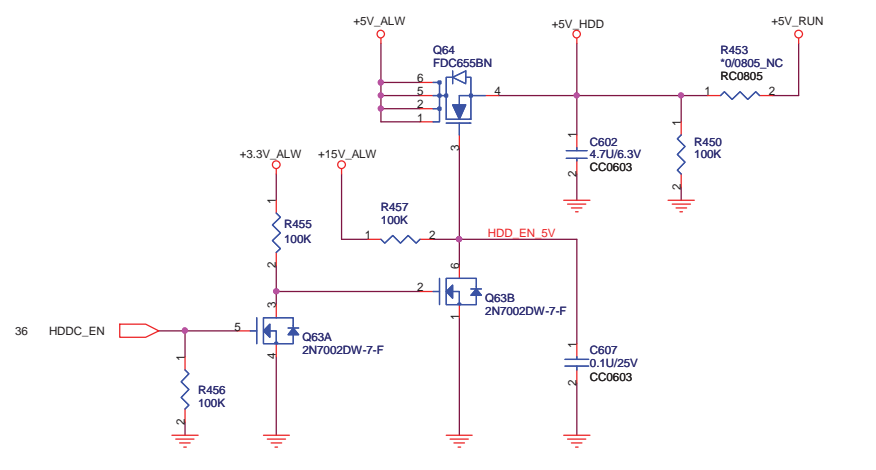
SATA ODD Connector



0306-Sun_Change to new footprint_sata-47639-200-13p-l
 0407-Sun_Swap pin assignment due to pin direction is reversed

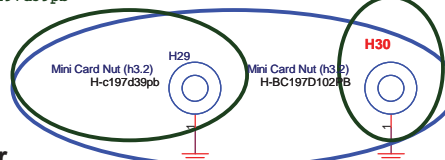


Place caps close to connector.



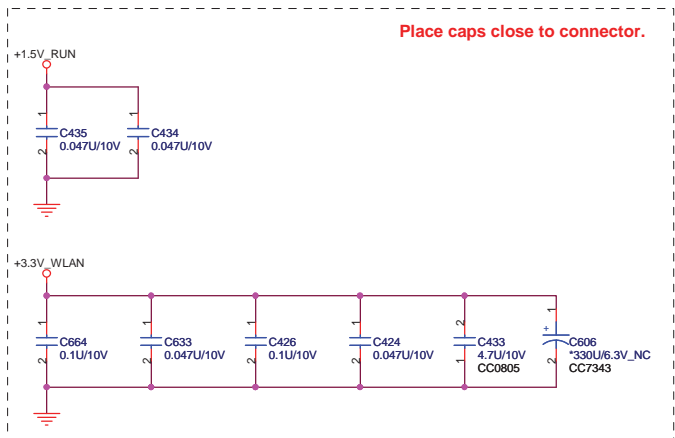
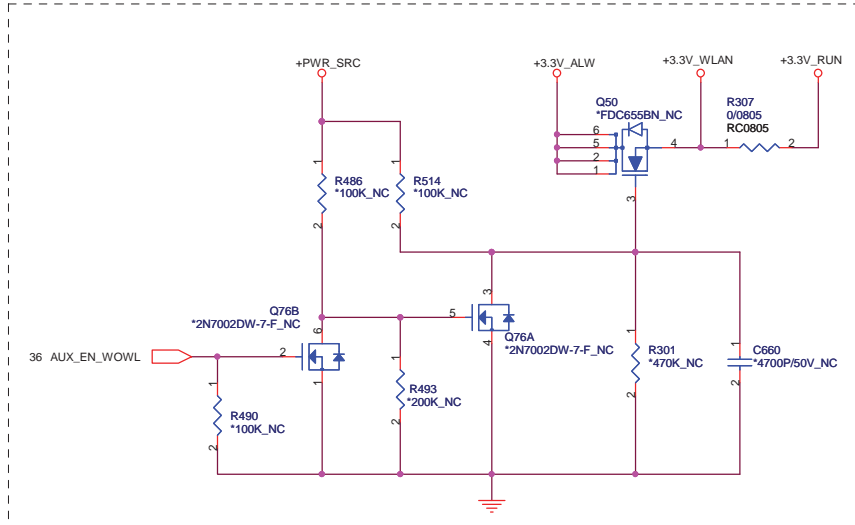
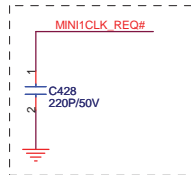
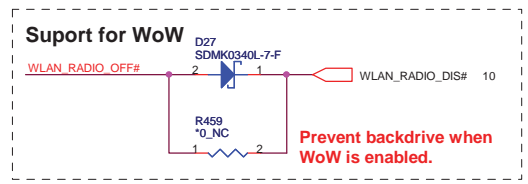
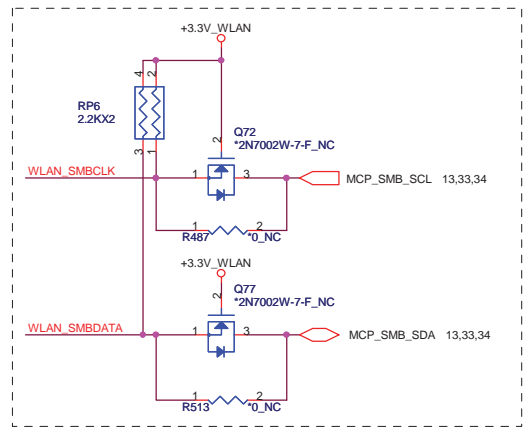
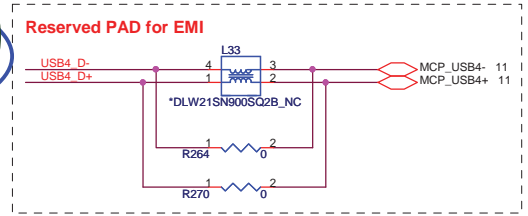
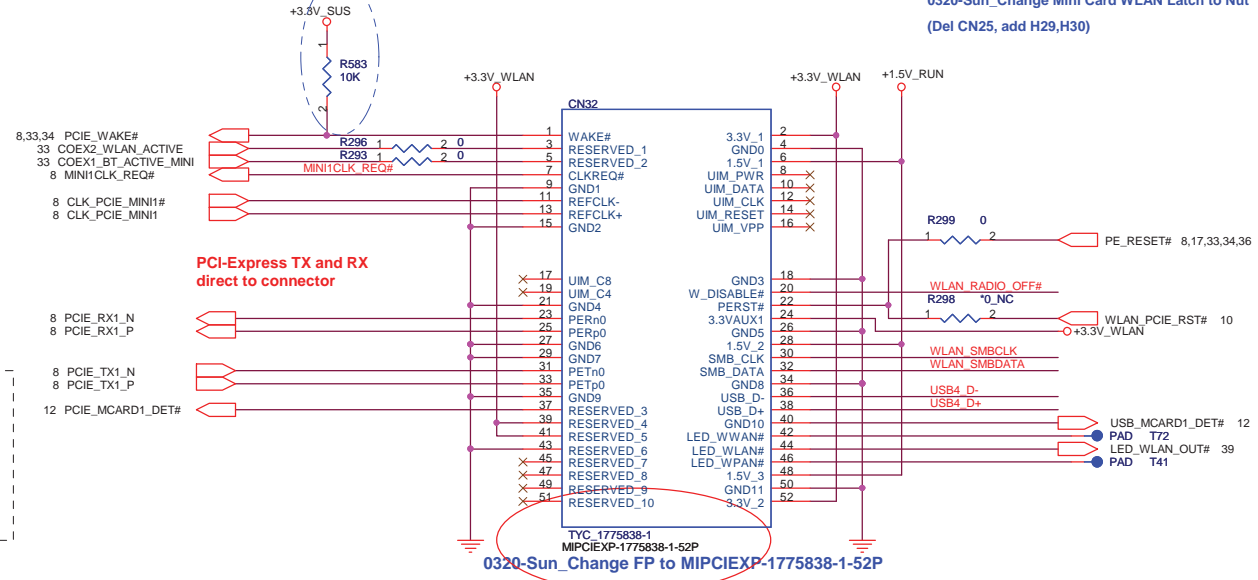
0829_Michael:Change Footprint from H-C197PB to H-c197d39pb

0616_Michael:Change footprint



MiniCard WLAN Connector

0320-Sun_Change Mini Card WLAN Latch to Nut
(Del CN25, add H29,H30)



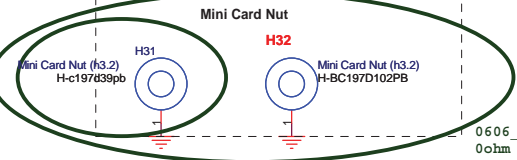
QUANTA COMPUTER

Title: MINI-CARD (WLAN)

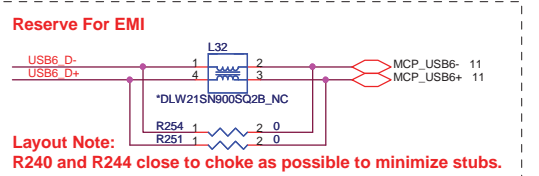
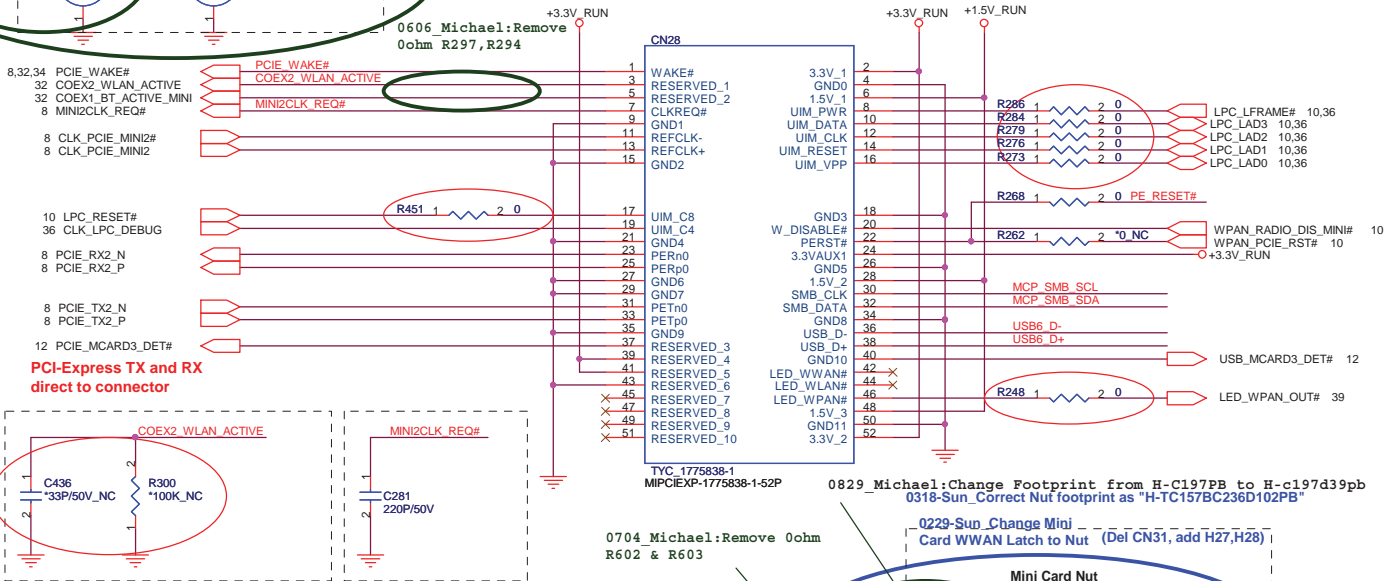
Size: Document Number IM3 (XPS-Jolie) Rev 2A

Date: Thursday, October 23, 2008 Sheet 32 of 59

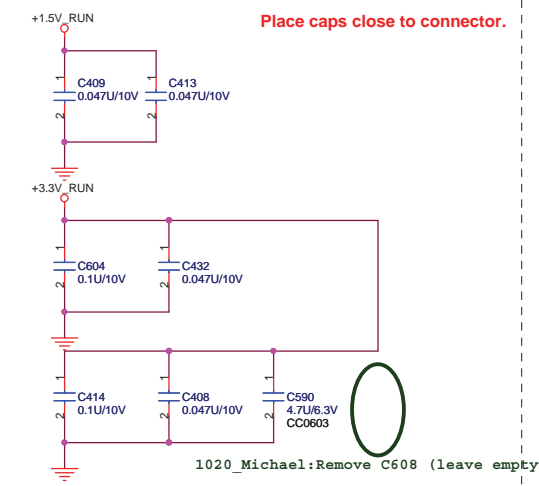
0829_Michael:Change Footprint from H-C197PB to H-c197d39pb
0605_Michael: Del MiniCard WPAN latch add Nut H31,H32



MiniCard Robson, BT. UWB Connector



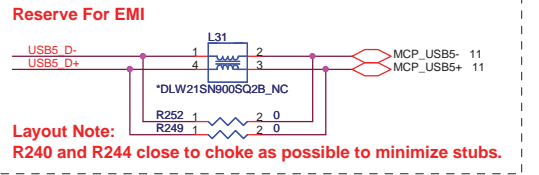
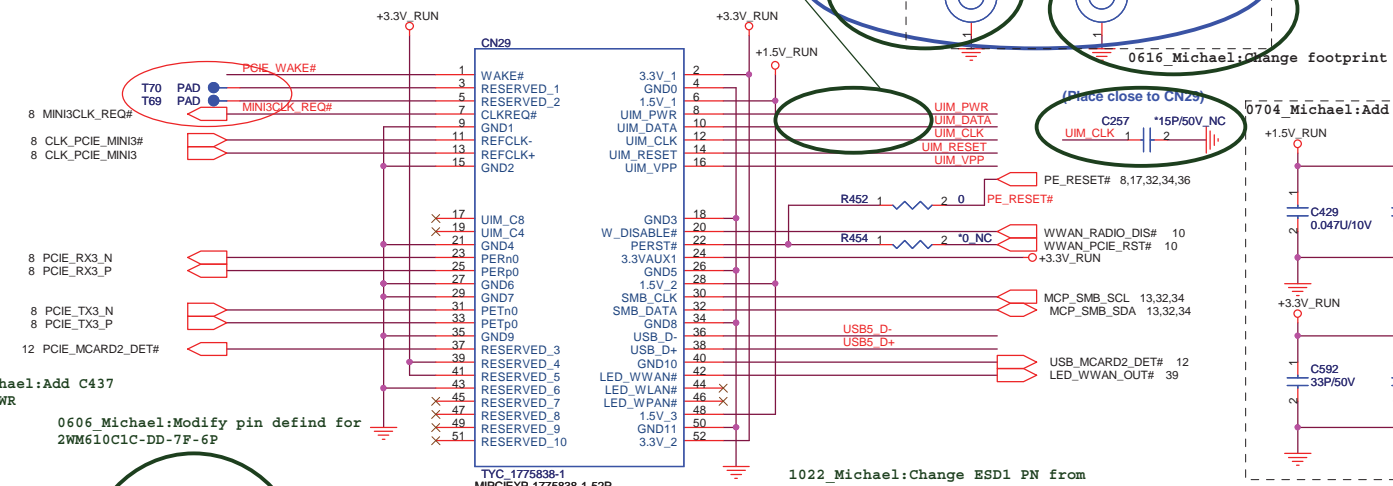
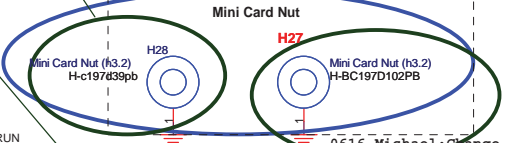
Layout Note: R240 and R244 close to choke as possible to minimize stubs.



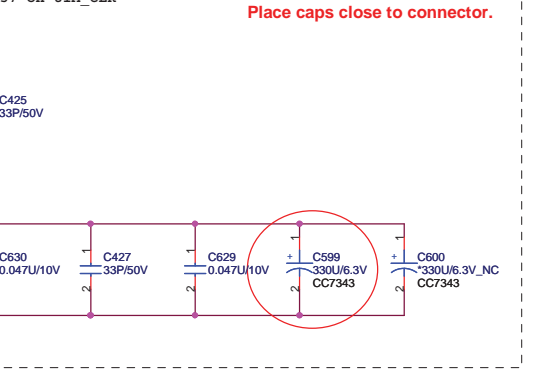
Place caps close to connector.

1020_Michael:Remove C608 (leave empty)

MiniCard WWAN Connector



Layout Note: R240 and R244 close to choke as possible to minimize stubs.

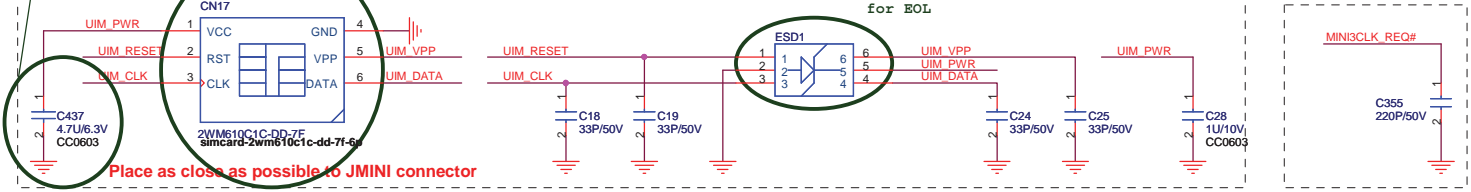


Place caps close to connector.

0704_Michael:Add C437 on UIM_PWR

0606_Michael:Modify pin defind for 2WM610C1C-DD-7F-6P

1022_Michael:Change ESD1 PN from ALSRV054011-to-ALB04220007-for EOL

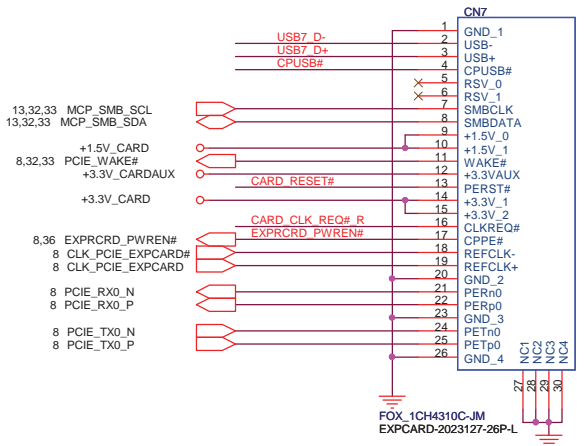


Place as close as possible to JMINI connector

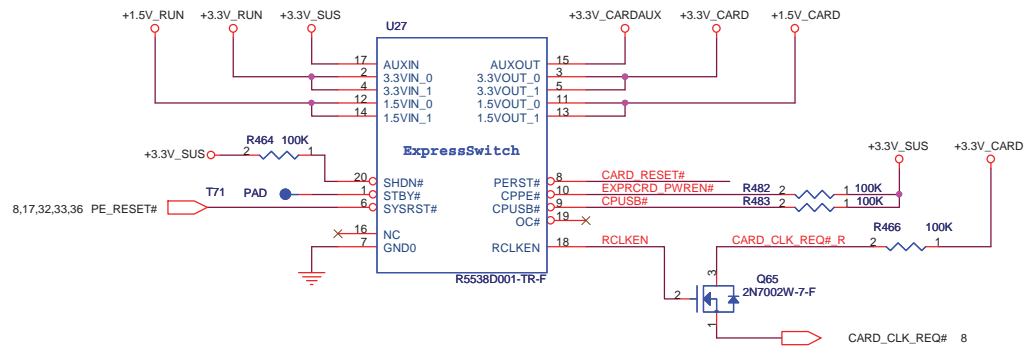


Title MINI-CARD (WWAN,WPAN)		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Thursday, October 23, 2008	Sheet 33 of 59

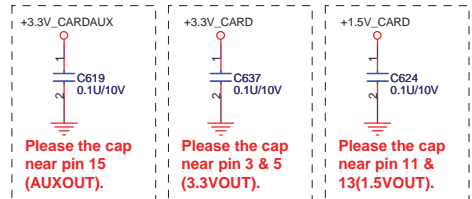
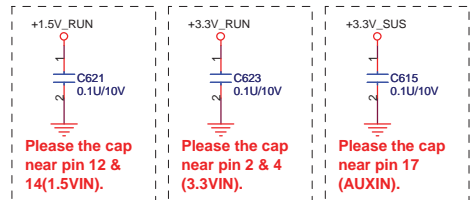
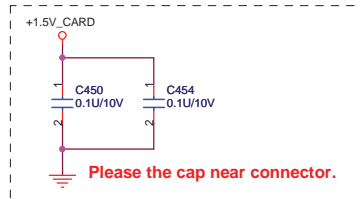
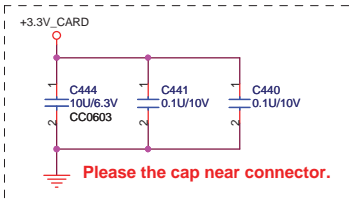
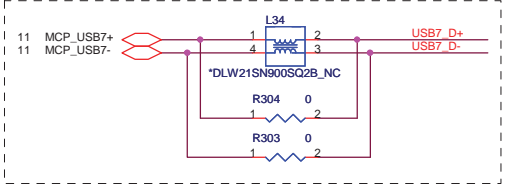
Express Card

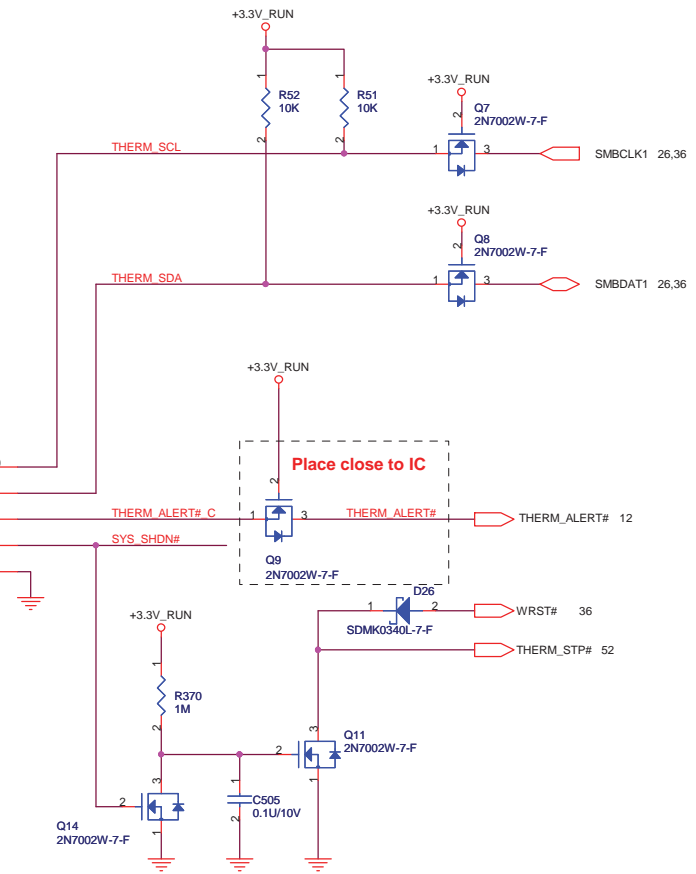
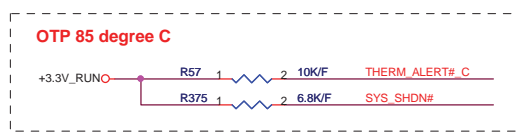
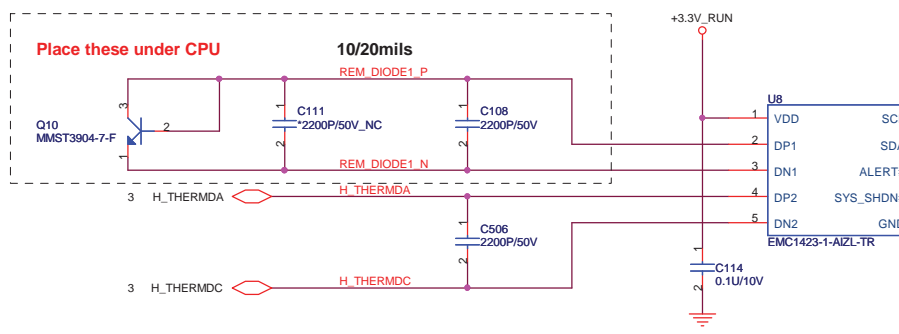
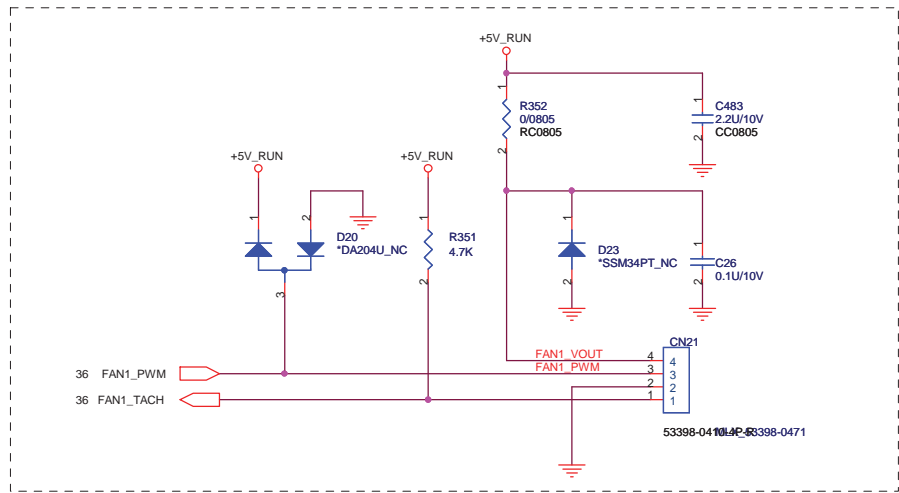


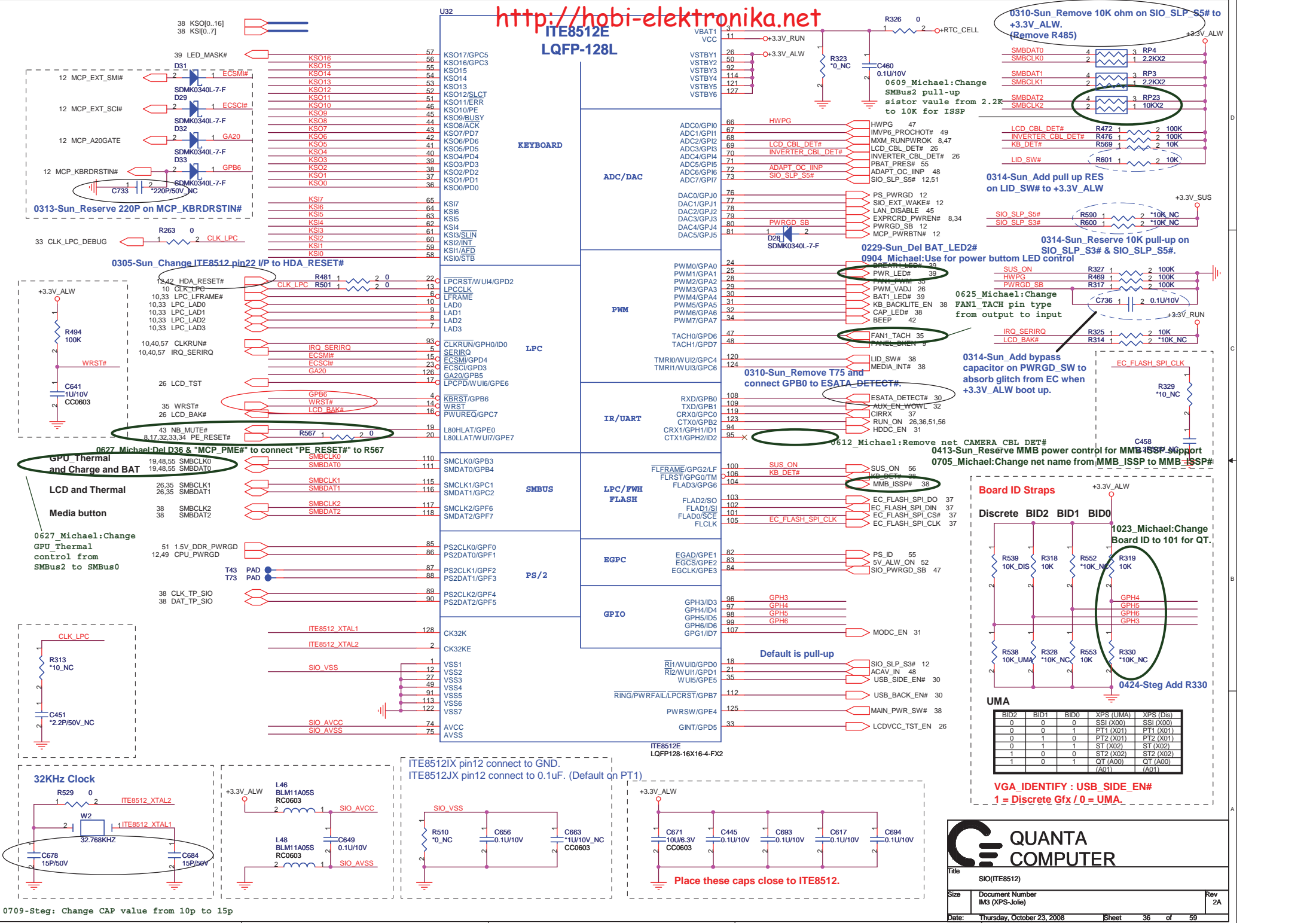
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.







0313-Sun_Reserve 220P on MCP_KBRDRSTIN#

0305-Sun_Change ITE8512 pin22 I/P to HDA_RESET#

0627 Michael:Del D36 & "MCP_PME#" to connect "PE_RESET#" to R567

GPU Thermal and Charge and BAT

LCD and Thermal

Media button

0627 Michael:Change GPU_Thermal control from SMBus2 to SMBus0

32KHz Clock

0709-Steg: Change CAP value from 10p to 15p

ITE8512X pin12 connect to GND.
ITE8512JX pin12 connect to 0.1uF. (Default on PT1)

Place these caps close to ITE8512.

0310-Sun_Remove 10K ohm on SIO_SLP_S5# to +3.3V_ALW. (Remove R485)

0314-Sun_Add pull up RES on LID_SW# to +3.3V_ALW

0314-Sun_Reserve 10K pull-up on SIO_SLP_S3# & SIO_SLP_S5#.

0314-Sun_Add bypass capacitor on PWRGD_SW to absorb glitch from EC when +3.3V_ALW boot up.

Board ID Straps

Discrete BID2 BID1 BID0

UMA

VGA_IDENTIFY : USB_SIDE_EN#
1 = Discrete Gfx / 0 = UMA

QUANTA COMPUTER

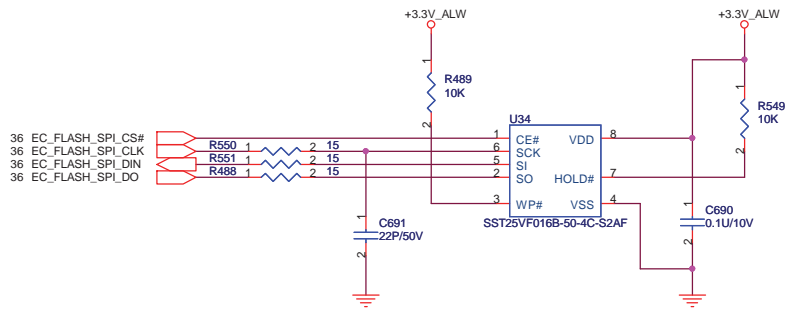
Title: SIO(ITE8512)

Size: Document Number IM3 (XPS-Joie) Rev 2A

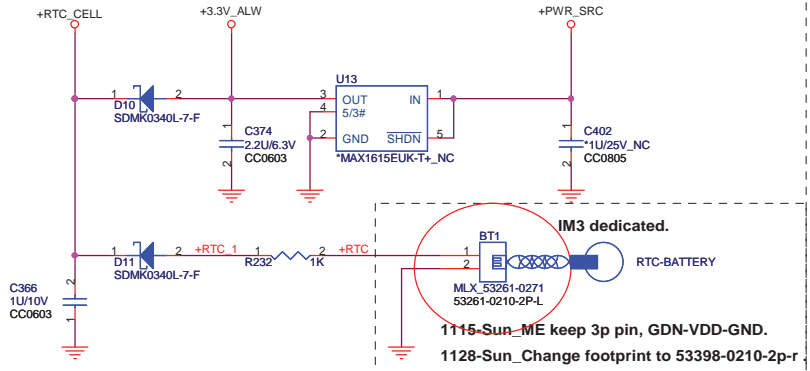
Date: Thursday, October 23, 2008 Sheet 36 of 59

BID2	BID1	BID0	XPS (UMA)	XPS (Dis)
0	0	0	SSI (X01)	SSI (X01)
0	0	1	PT1 (X01)	PT1 (X01)
0	1	0	PT2 (X01)	PT2 (X01)
0	1	1	ST (X02)	ST (X02)
1	0	0	ST2 (X02)	ST2 (X02)
1	0	1	QT (A00)	QT (A00)

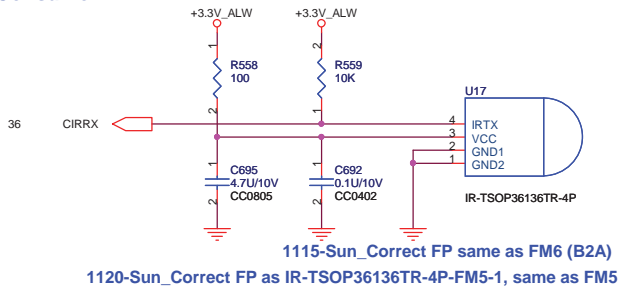
16Mbit (2M Byte), SPI



RTC BATTERY



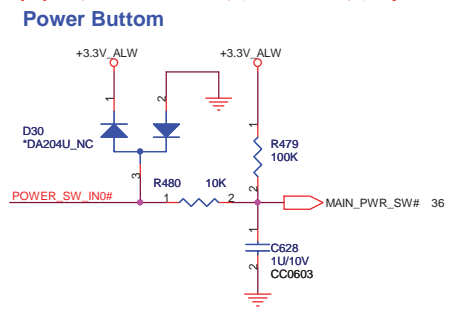
Consumer IR



0605_Michael: Change CN6 from 32pin to 28pin but need to check footprint and PN

BREATH_PWRLED_BOT:
 Solid = System On, Normal Activity, "Breathing" = System in Standby; Off = System Off (or in Hibernation)

0420 Michael: Add KB detect function
 1023 Michael: Disable KB LED function
 depop R722 and change R723 from 200K to 0 ohm



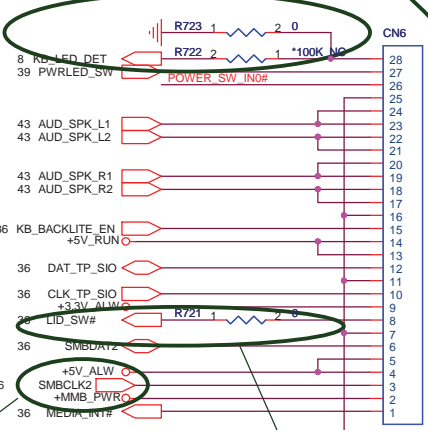
Power Button

Speaker

KB LED

Touch Pad

Media Button

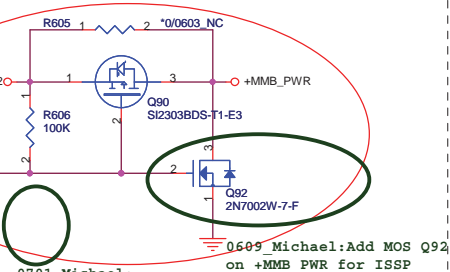


0909 Michael: Remove LID_SW# and connector to GND

0624 Michael: Change net name from +5V_ALW2 to +MMB_PWR
 0704 Michael: Swap SMBCLK2 and +MMB_PWR for Ass'y issue

0825 Michael: Add KB detect function
 0911 Michael: Change pin from 16 to 8
 0918 Michael: Return to LID_SW#

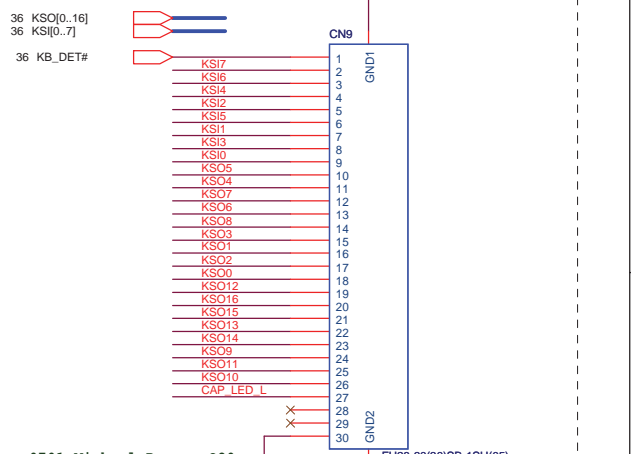
0411-Sun_Reserve circuit for MMB ISSP support
 0414-Sun_Change MOSFET control voltage level



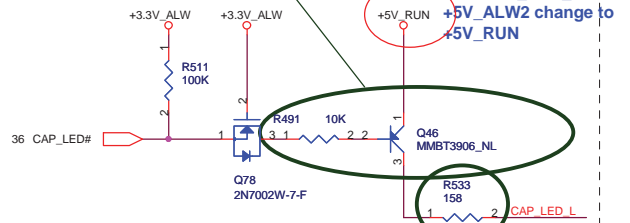
0609 Michael: Add MOS Q92 on +MMB_PWR for ISSP

0701 Michael: Remove Q91 for ISSP

KEYBOARD CONNECTOR

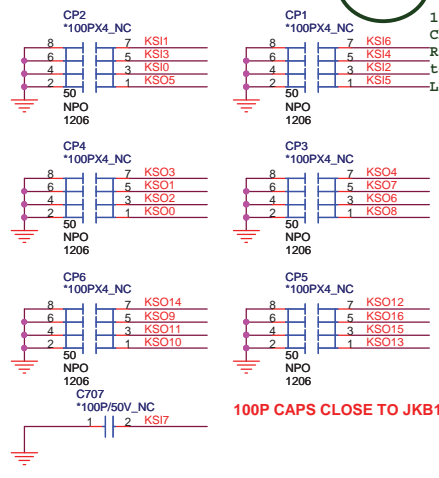


0701 Michael: Remove Q80 and add Q46 & R491 for leakage issue on S3



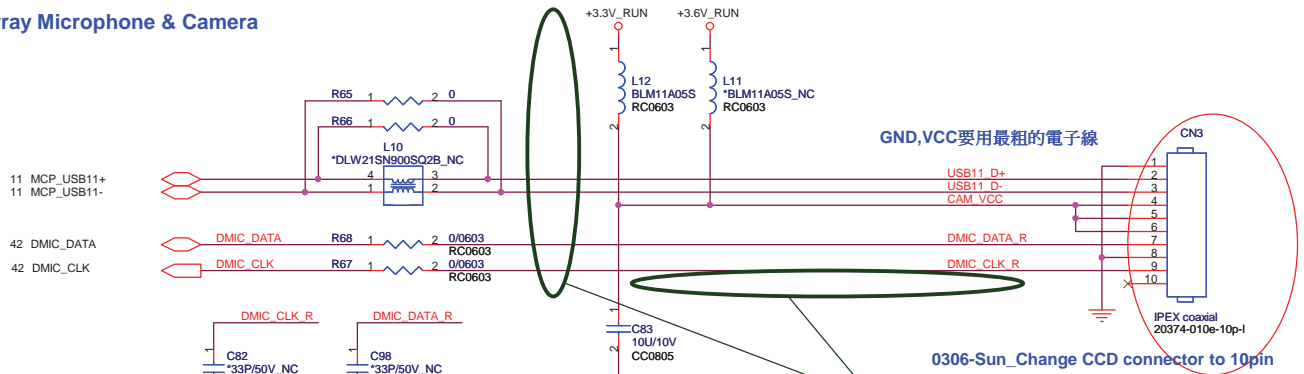
0310-Sun_CAP_LED +5V_ALW2 change to +5V_RUN

1022 Michael: Change R533 from 2.49K to 158ohm for LED brightness



100P CAPS CLOSE TO JKB1

Array Microphone & Camera

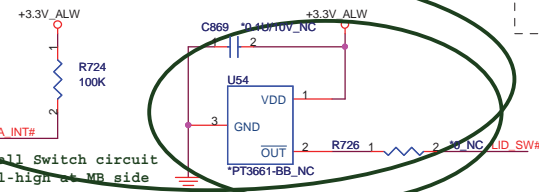


GND,VCC要用最粗的电子线

0306-Sun_Change CCD connector to 10pin

0612 Michael: Remove CAMERA DET circuit, R64 pull-up to +3.3V_RUN and connector to U32 pin95

Hall Switch

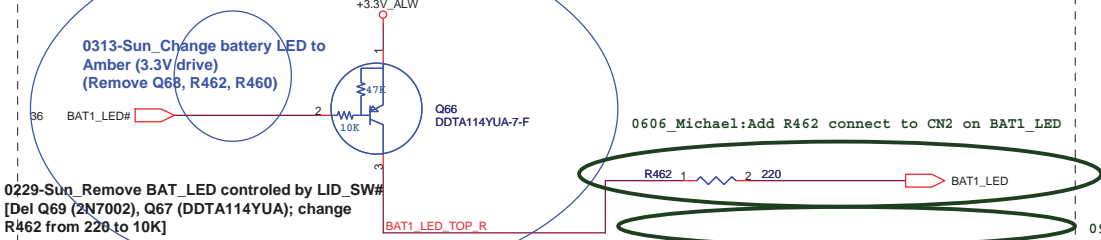


0815 Michael: Add Hall Switch circuit and MEDIA_INT# pull-high at MB side

1023_Michael: Depop LID_Switch function on MB side

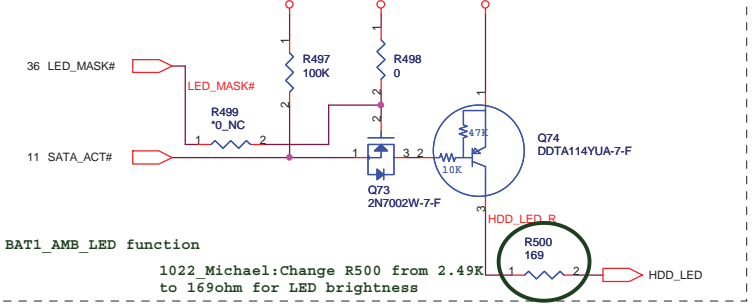


Battery status

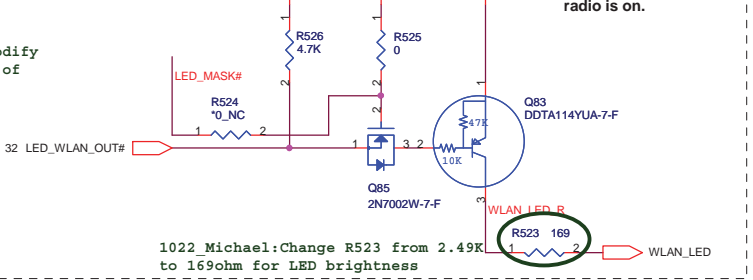


0229-Sun_Del BAT_LED2 [Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

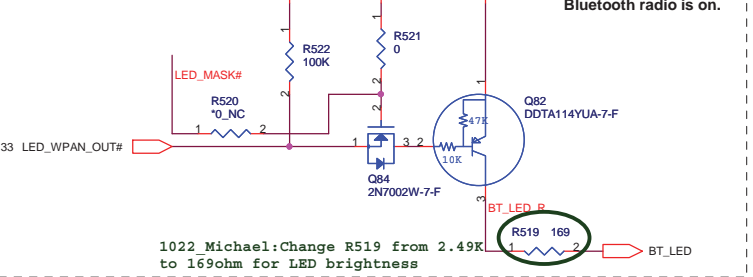
HDD Activity LED



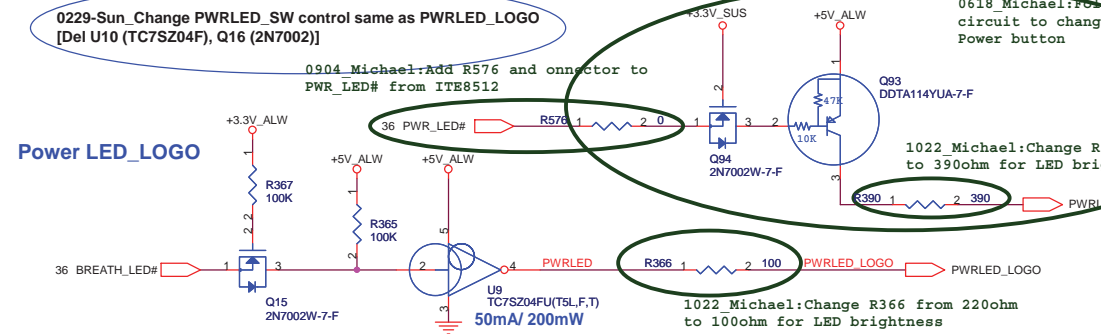
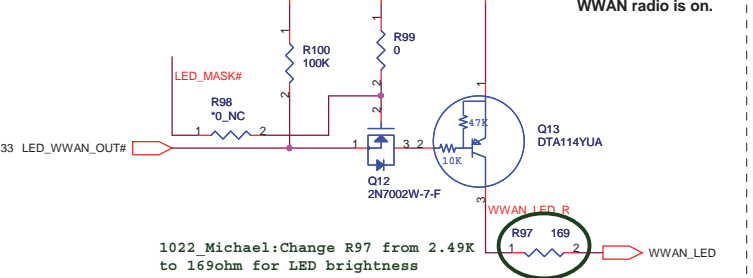
WLAN



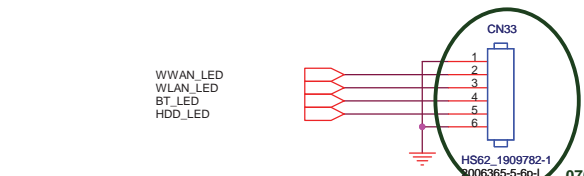
BT / UWB LED



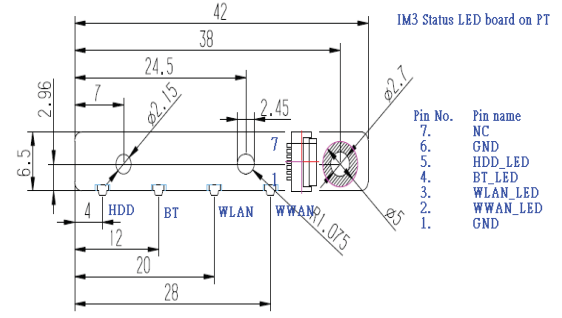
WWAN



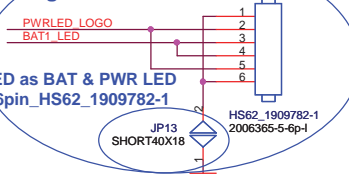
Power LED_LOGO



0229-Sun_Remove LED control by LID_SW# (Del R478,R477,Q75)



Logo LED/B connector

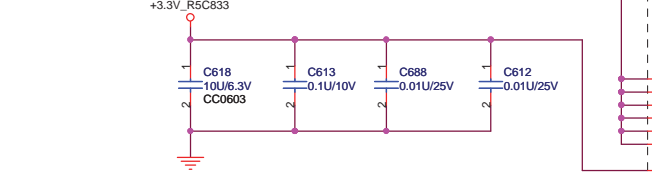
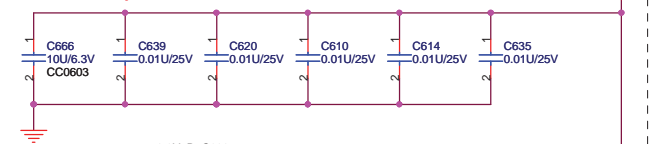


0314-Sun_Add short pad on GND of Logo LED/B connector for EMI request.

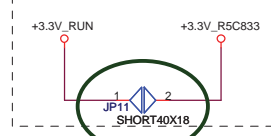
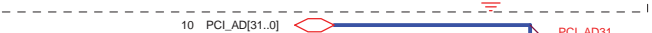


Title LED		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Wednesday, October 22, 2008	Sheet 39 of 59

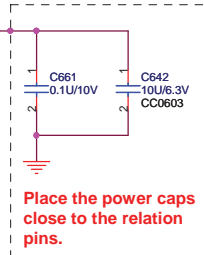
Place the power caps close to the relation pins.



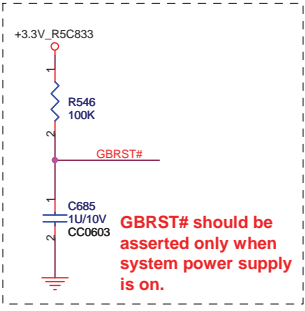
Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



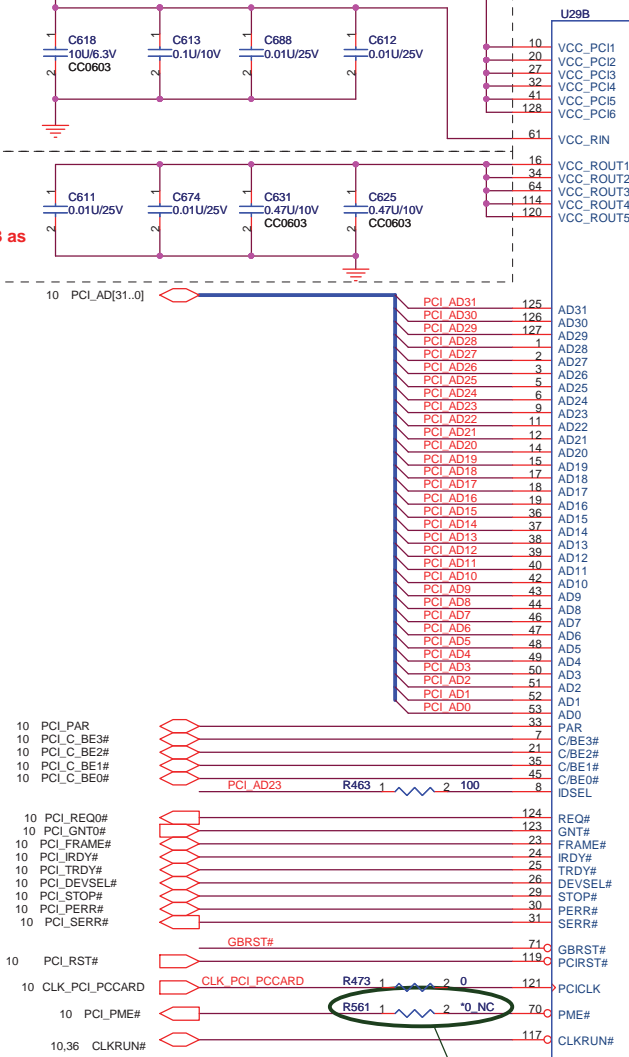
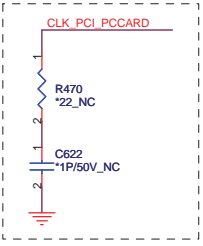
0606_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)



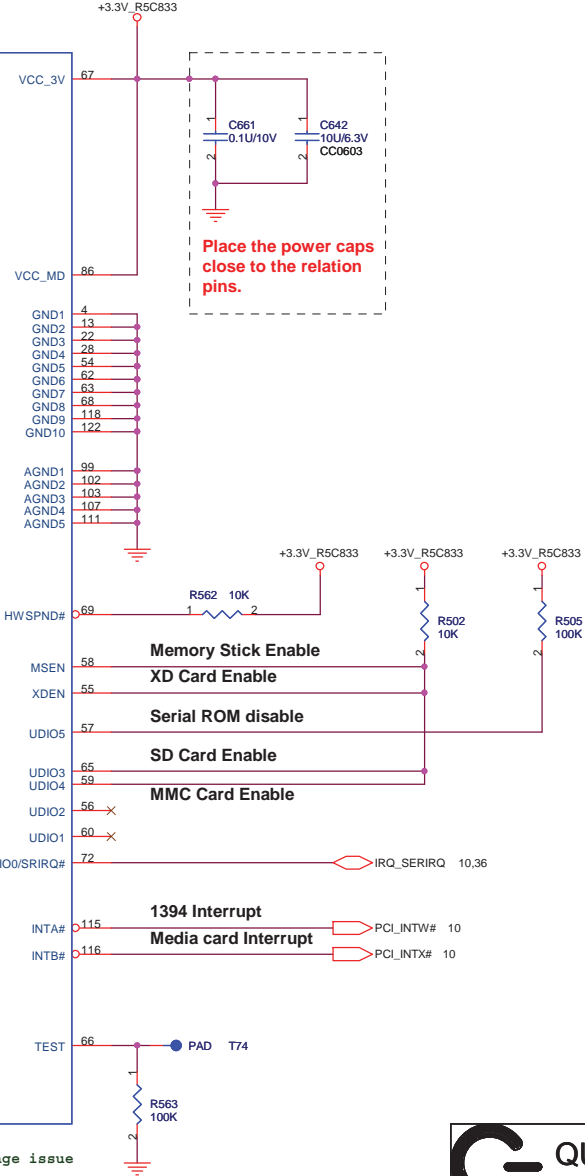
Place the power caps close to the relation pins.



GBRST# should be asserted only when system power supply is on.



PCI / OTHER



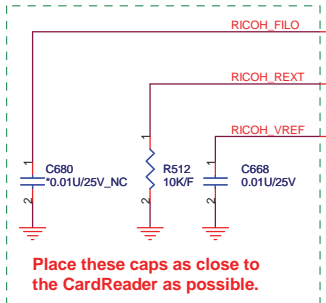
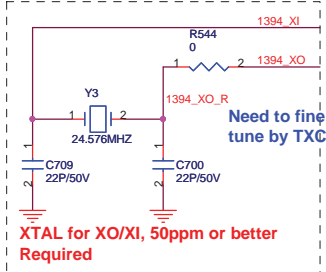
Memory Stick Enable
 XD Card Enable
 Serial ROM disable
 SD Card Enable
 MMC Card Enable

1394 Interrupt
 Media card Interrupt

0630_Michael:Remove Mini PCI CN8 and circuit

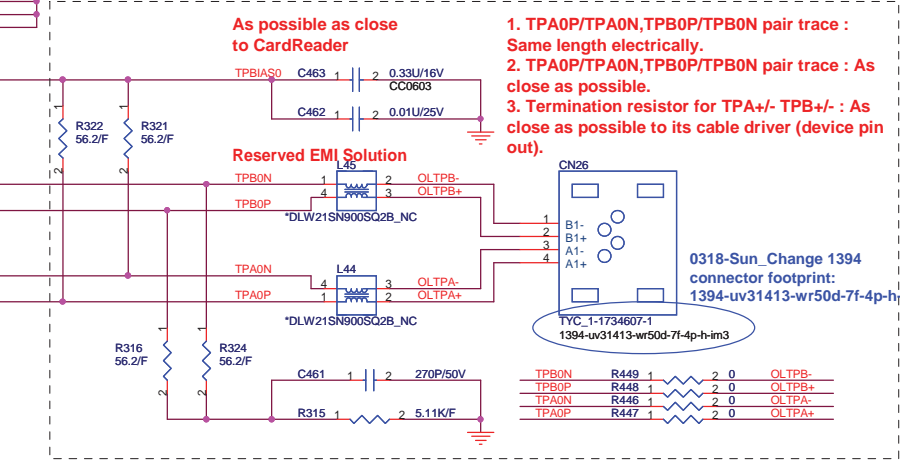
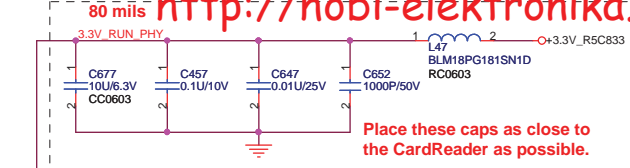
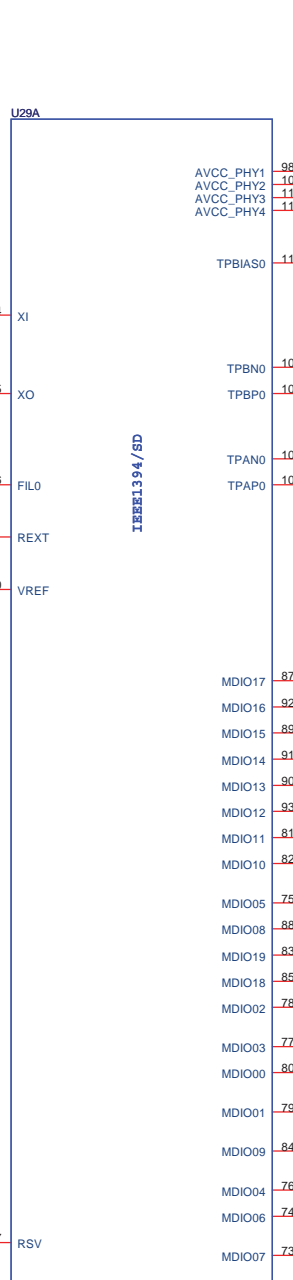
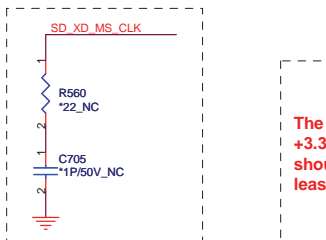
0707_Michael:Depop R561 for leakage issue



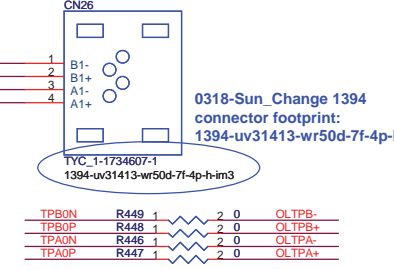


Card Reader interface signal mapping

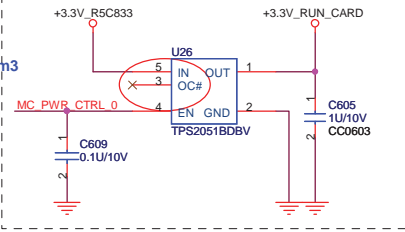
PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#	MS_CD#	XD_CD#
MDIO01	SD_CD#	MMC_CD#	MS_CD#	XD_CD#
MDIO02	SD_WP#	MMC_PWR	MS_PWR	XD_E/B#
MDIO04	SD_PWR0	MMC_PWR	MS_PWR	XD_PWR
MDIO05	SD_PWR1	MMC_PWR	MS_PWR	XD_PWR
MDIO06	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO07	MTEST			
MDIO08	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO09	SD_CLK	MMC_CLK	MS_CLK	XD_BE#
MDIO10	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO11	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO12	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO13	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO14		MMC_D4		XD_D4
MDIO15		MMC_D5		XD_D5
MDIO16		MMC_D6		XD_D6
MDIO17		MMC_D7		XD_D7
MDIO18				XD_CLE
MDIO19				XD_ALE



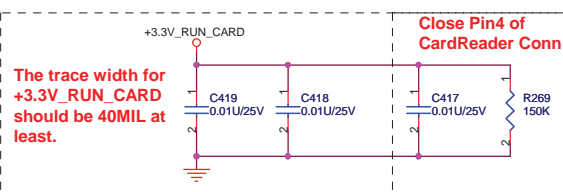
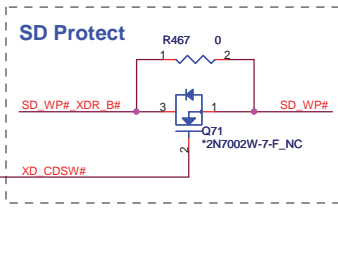
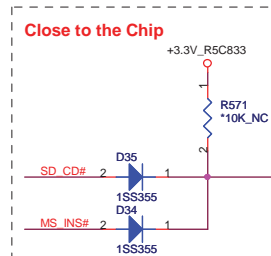
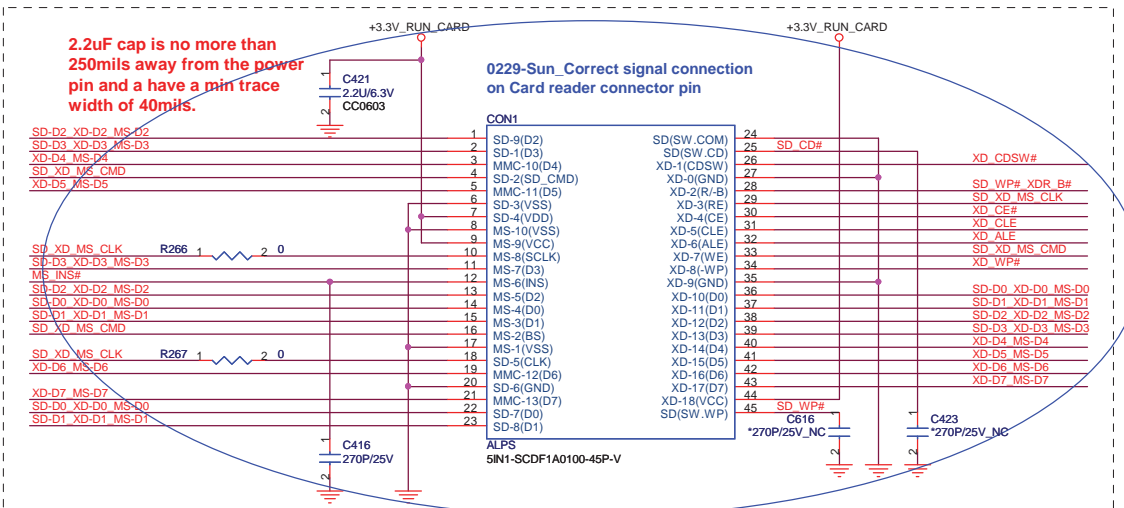
1. TPA0P/TPA0N, TPB0P/TPB0N pair trace : Same length electrically.
2. TPA0P/TPA0N, TPB0P/TPB0N pair trace : As close as possible.
3. Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

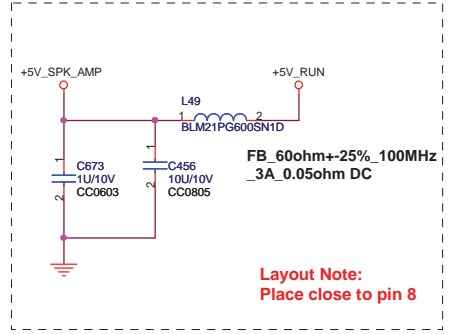
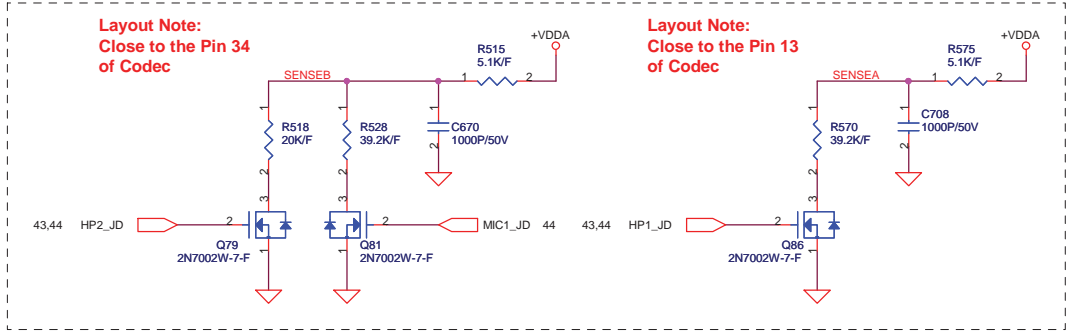


- Layout Note:**
- 1). The distance between Media Card Power Switch and Media Socket should be less than 2-inches.
 - 2). The trace width for +3.3V_RUN_CARD should be 40MIL at least.
 - 3). The GND trace for Media Card Socket should be 40MIL at least.

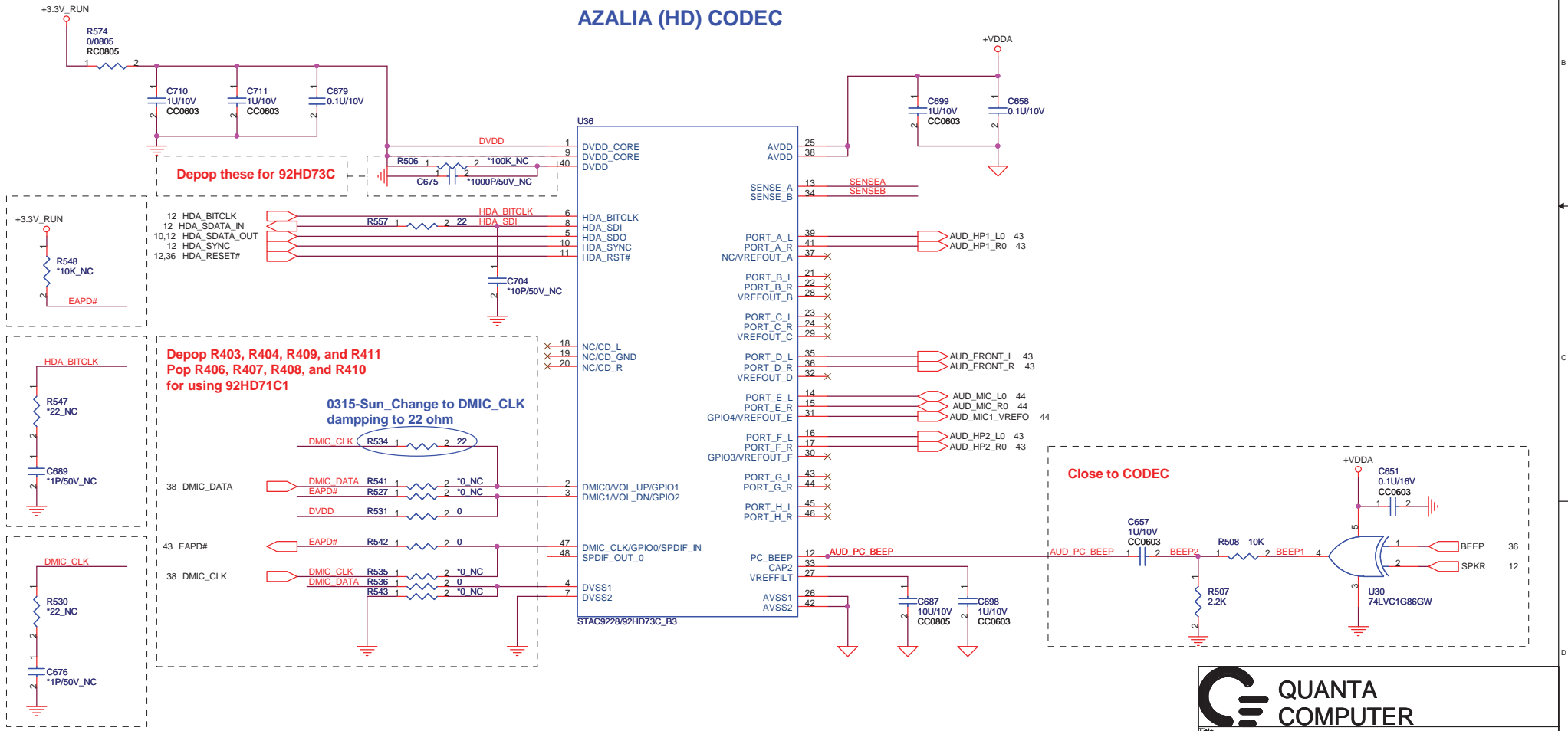


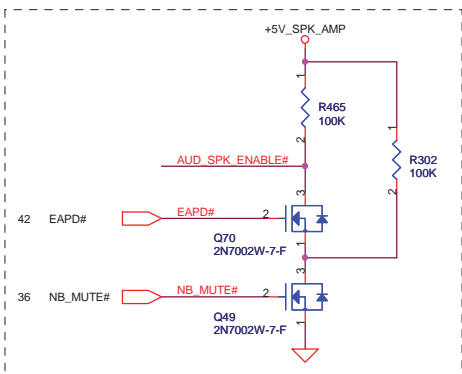
- MDIO17 XD-D7 MS-D7
- MDIO16 XD-D6 MS-D6
- MDIO15 XD-D5 MS-D5
- MDIO14 XD-D4 MS-D4
- MDIO13 SD-D3 XD-D3 MS-D3
- MDIO12 SD-D2 XD-D2 MS-D2
- MDIO11 SD-D1 XD-D1 MS-D1
- MDIO10 SD-D0 XD-D0 MS-D0
- MDIO05 XD_WP#
- MDIO08 SD_XD_MS_CMD
- MDIO19 XD_ALE
- MDIO18 XD_CLE#
- MDIO02 SD_WP# XDR_B#
- MDIO03 SD_CD#
- MDIO00 MS_INS#
- MDIO09 SD_XD_MS_CLK
- MDIO04 MC_PWR_CTRL_0
- MDIO06 T44 PAD
- MDIO07 R5C833T_V00



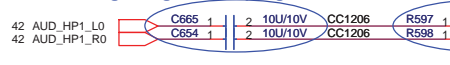


AZALIA (HD) CODEC





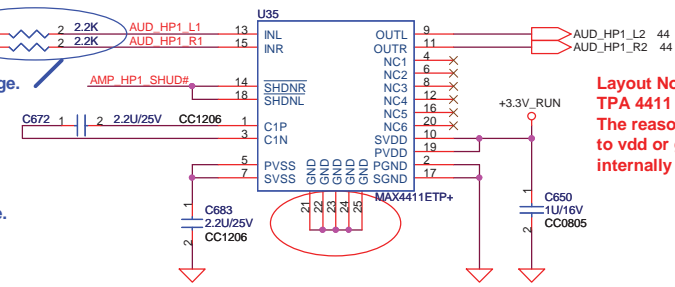
0315-Sun_Improve Dynamic Range.
0320-StegeChange AC coupling to 10U/10V



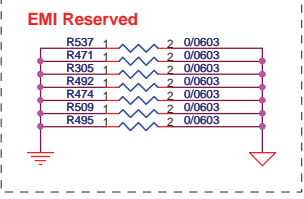
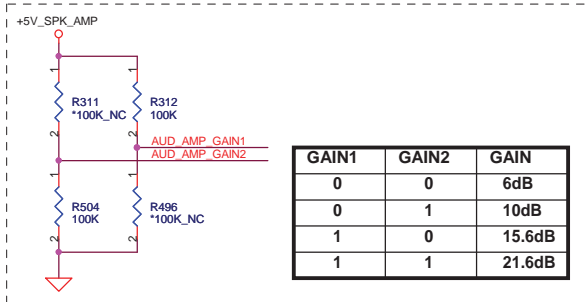
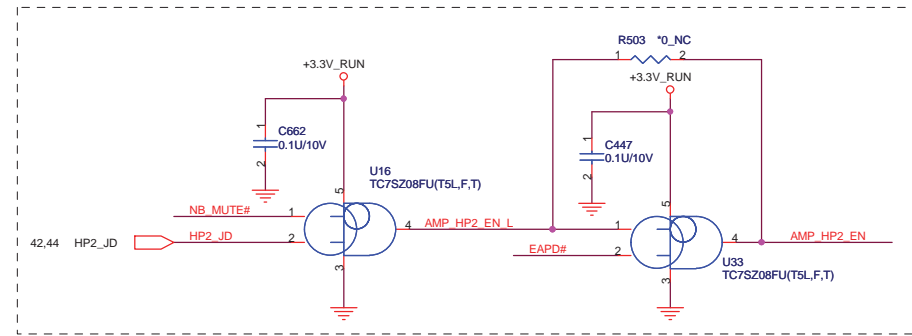
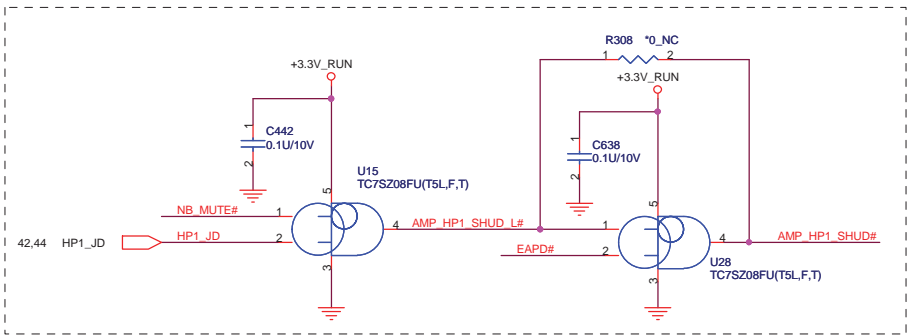
0310-Sun_Improve Dynamic Range.
Add R597,R598 w/2.2K



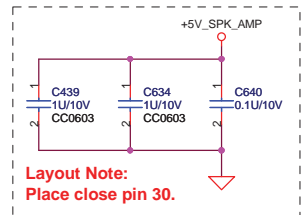
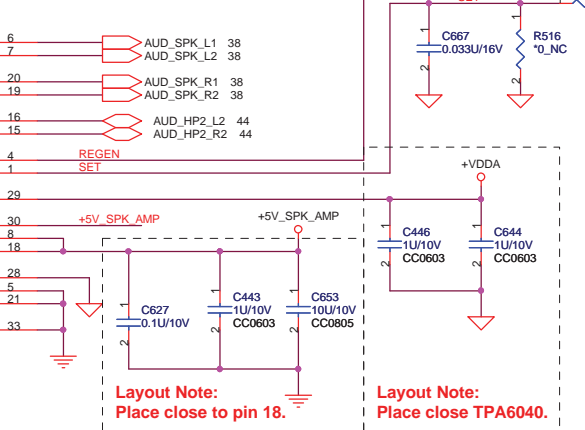
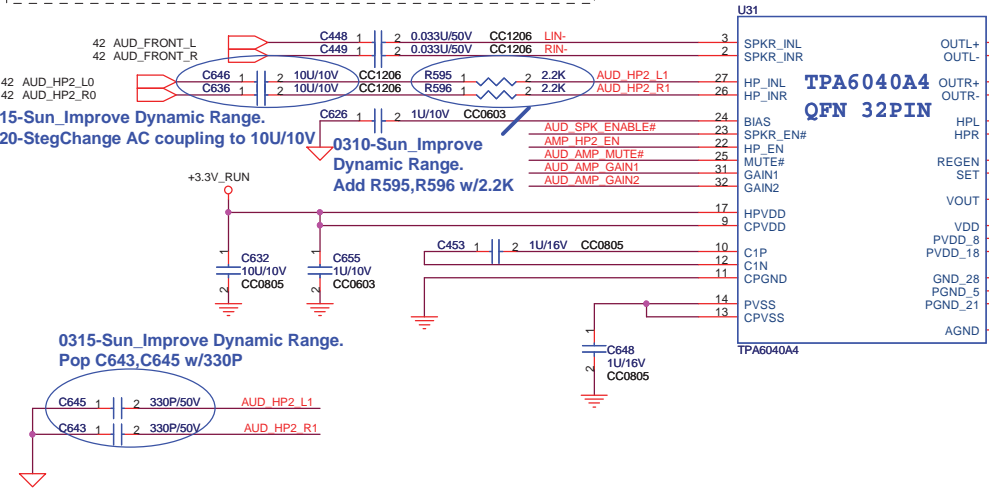
0315-Sun_Improve Dynamic Range.
Pop C452,C455 to 330P



Layout Note:
TPA 4411 : cannot connect EP to GND.
The reason that we can't solder the pad to vdd or ground is because it is internally connected to VSS.



Layout Note:
MAX9789A/TPA6040A : need to connect EP (exposed paddle) to GND.
TPA 4411 : cannot connect EP to GND.
MAX 4411: can connect EP to GND.



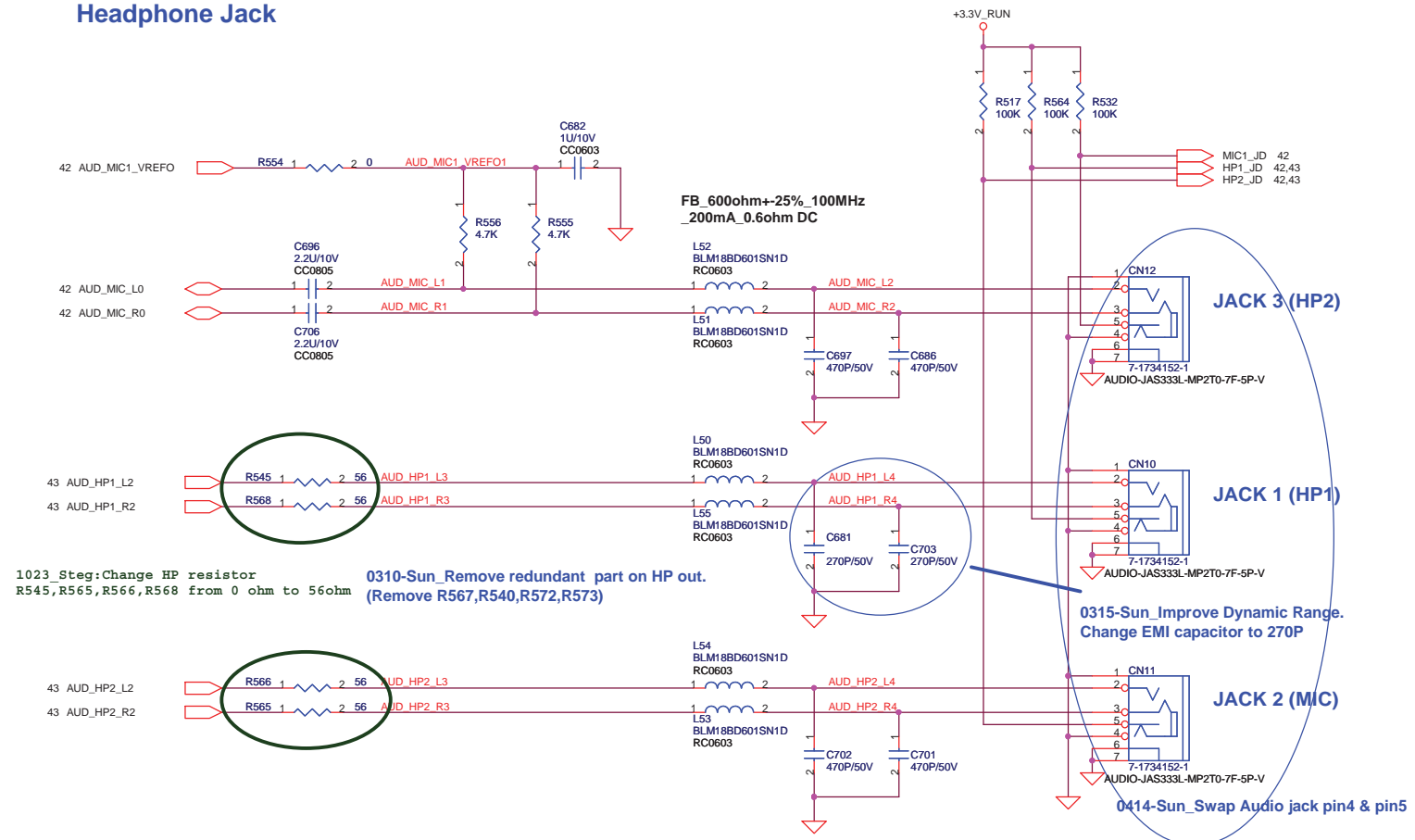
Layout Note:
Place close pin 30.

Layout Note:
Place close to pin 18.

Layout Note:
Place close TPA6040.



Headphone Jack



1023_Step: Change HP resistor
R545, R565, R566, R568 from 0 ohm to 56ohm

0310-Sun_Remove redundant part on HP out.
(Remove R567, R540, R572, R573)

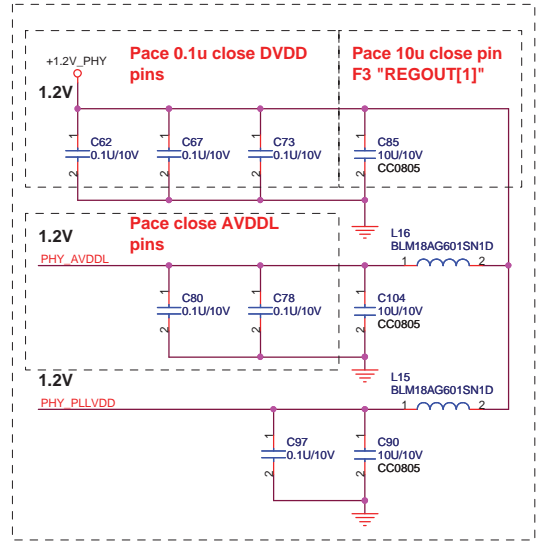
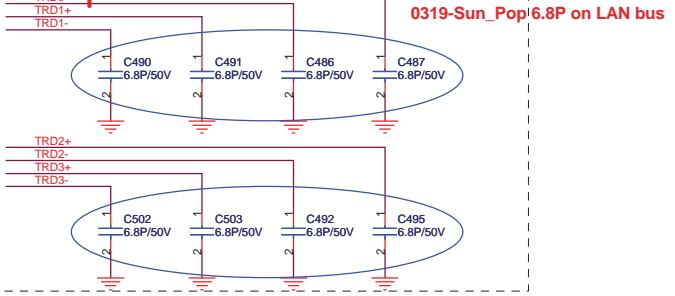
0315-Sun_Improve Dynamic Range.
Change EMI capacitor to 270P

0414-Sun_Swap Audio jack pin4 & pin5

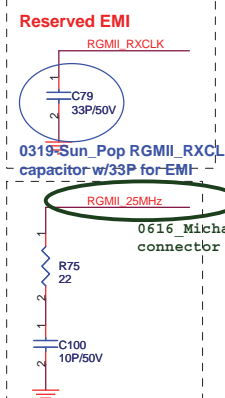
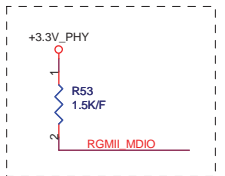


Title			AUDIO CONN
Size	Document Number	Rev	
	IM3 (XPS-Jolie)	2A	
Date:	Thursday, October 30, 2008	Sheet	44 of 59

Layout Note:
 1. Use 50 ohm impedance for all trace.
 2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
 3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.

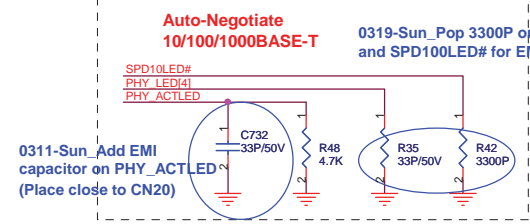
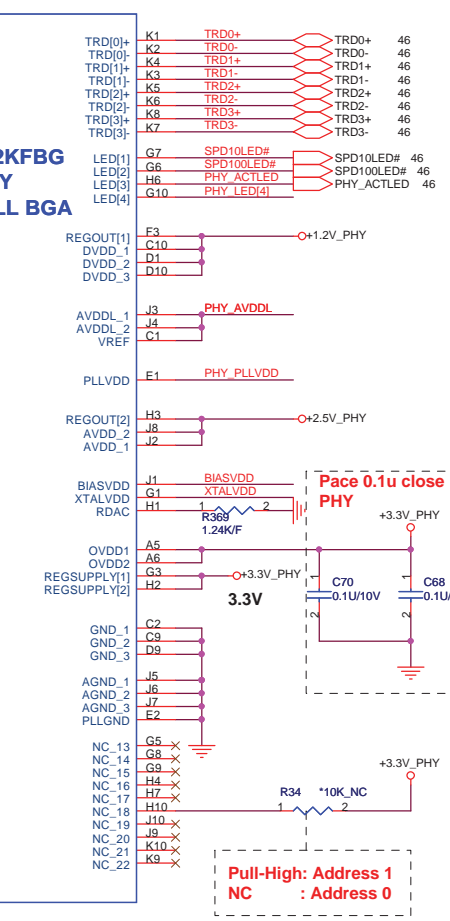
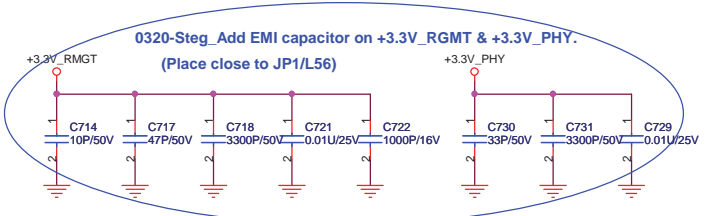
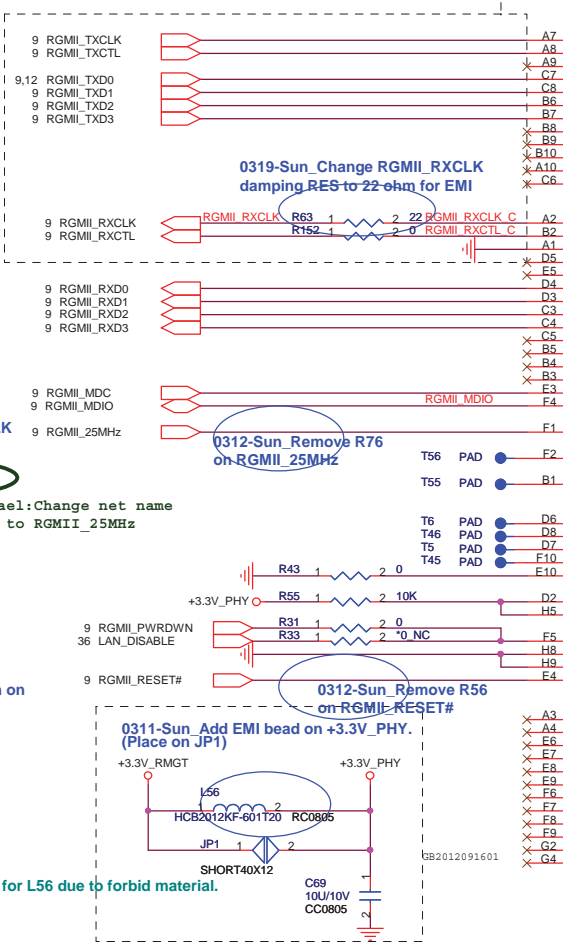
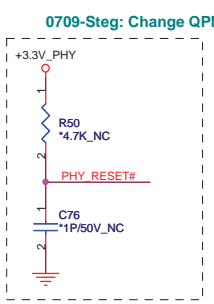


Layout Note:
 Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.



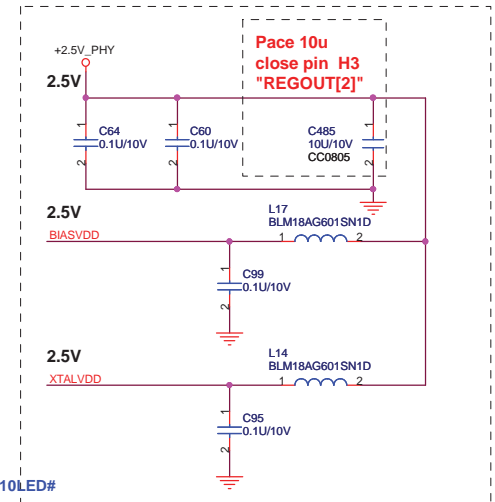
0319-Sun_Pop AC termination on PHY_XTALI for EMI

0312-Sun_Remove R74 on PHY_XTALI.



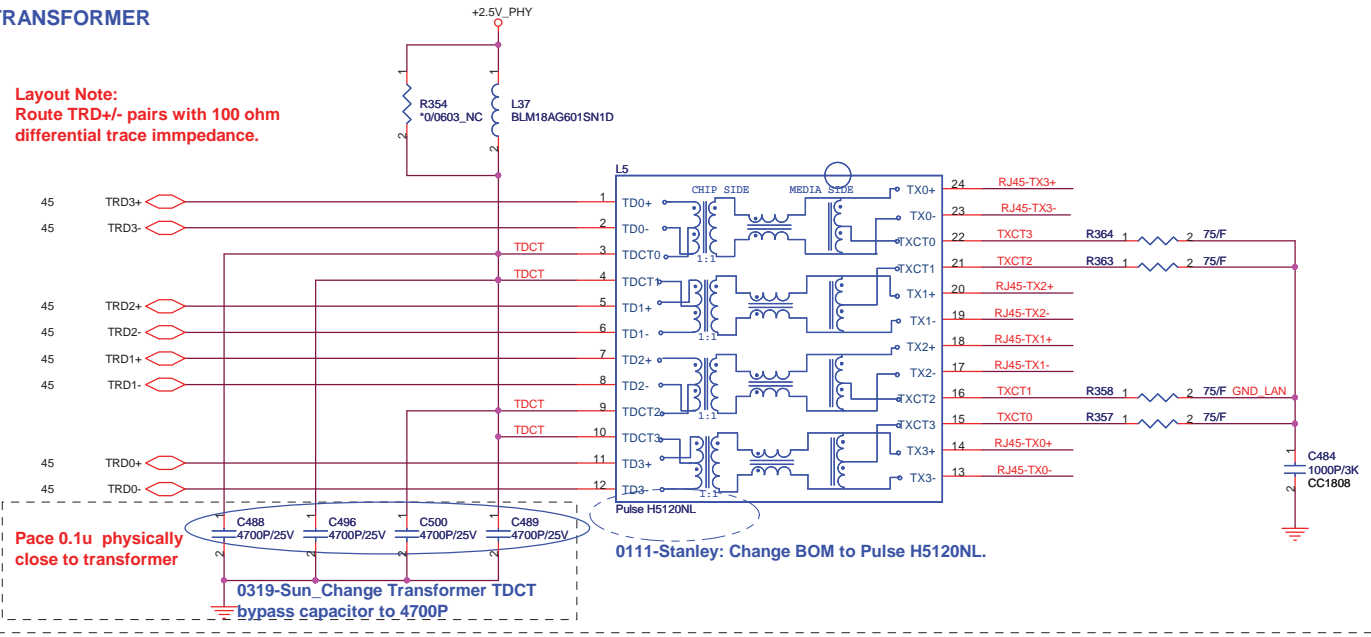
0311-Sun_Add EMI capacitor on PHY_ACTLED (Place close to CN20)

Auto-Negotiate 10/100/1000BASE-T
 0319-Sun_Pop 3300P on SPD10LED# and SPD100LED# for EMI



TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



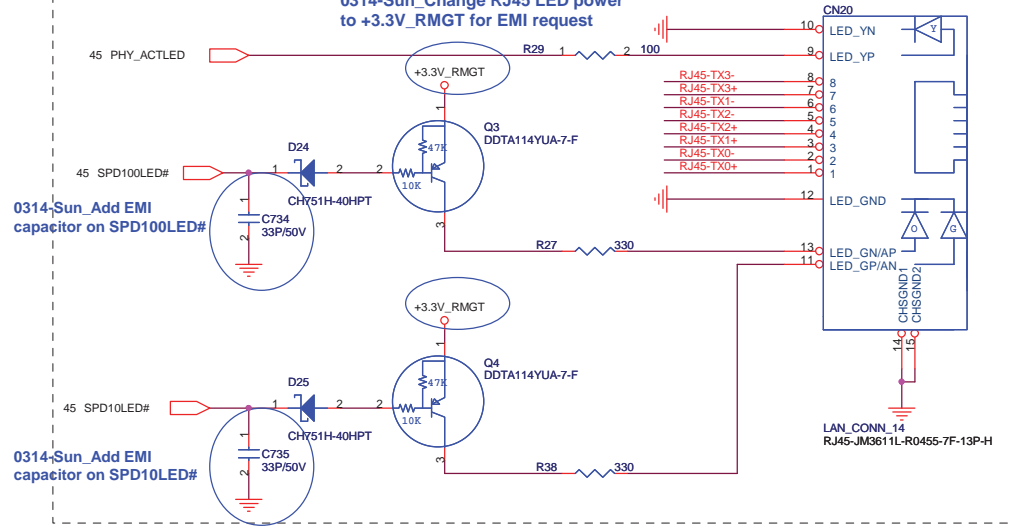
Place 0.1u physically close to transformer

0319-Sun_Change Transformer TDCT bypass capacitor to 4700P

0111-Stanley: Change BOM to Pulse H5120NL.

RJ-45 Connector

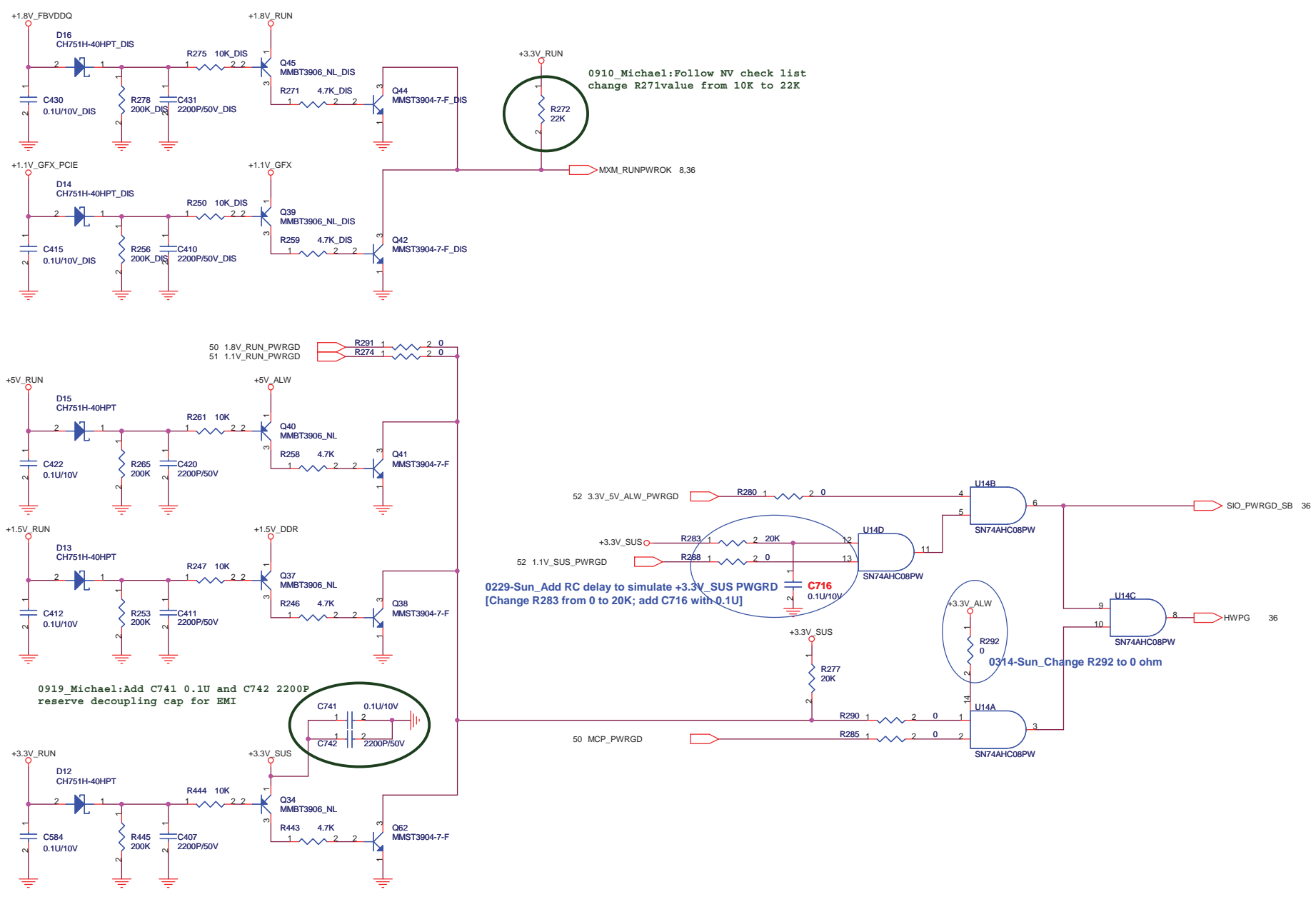
0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request

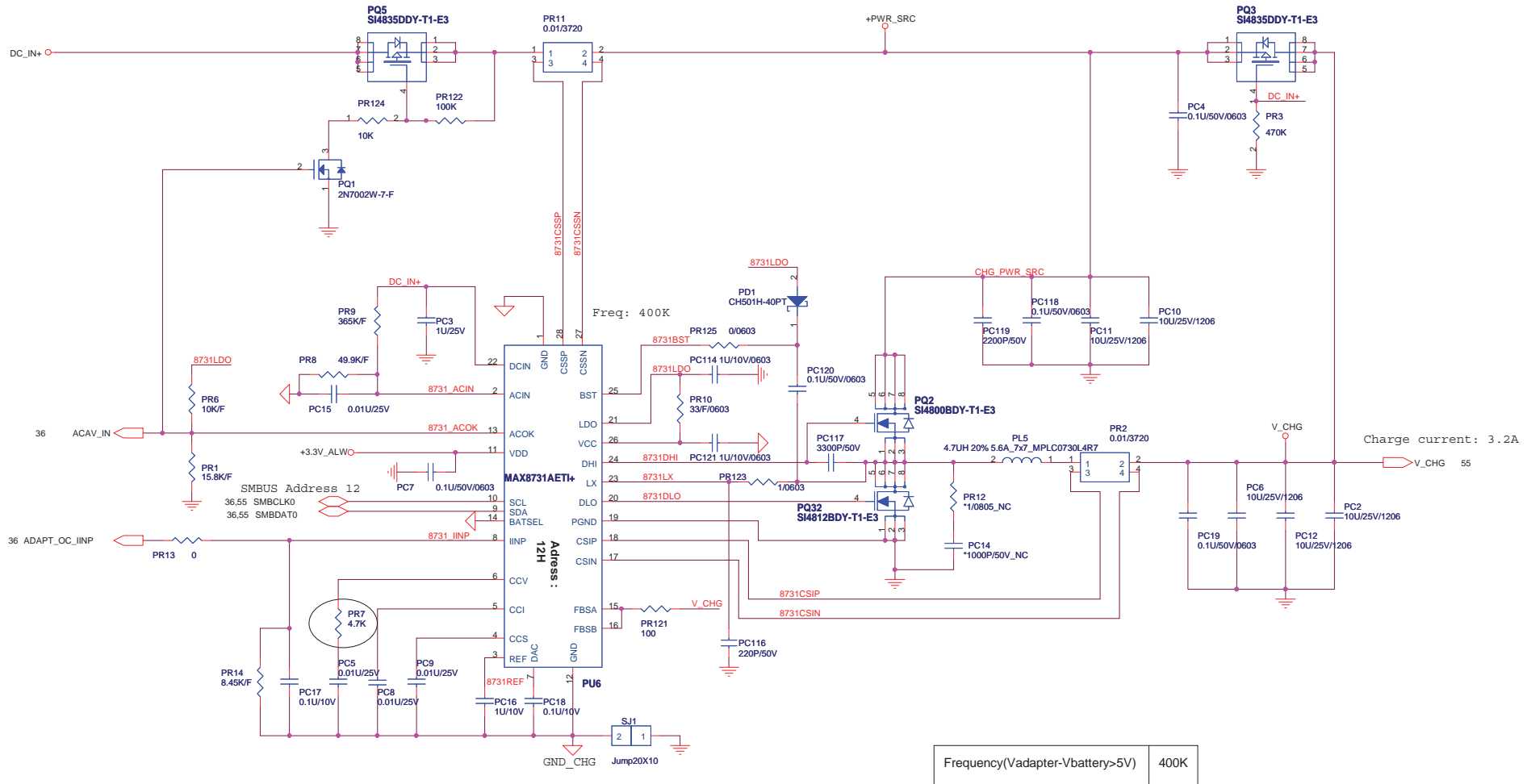


0314-Sun_Add EMI capacitor on SPD100LED#

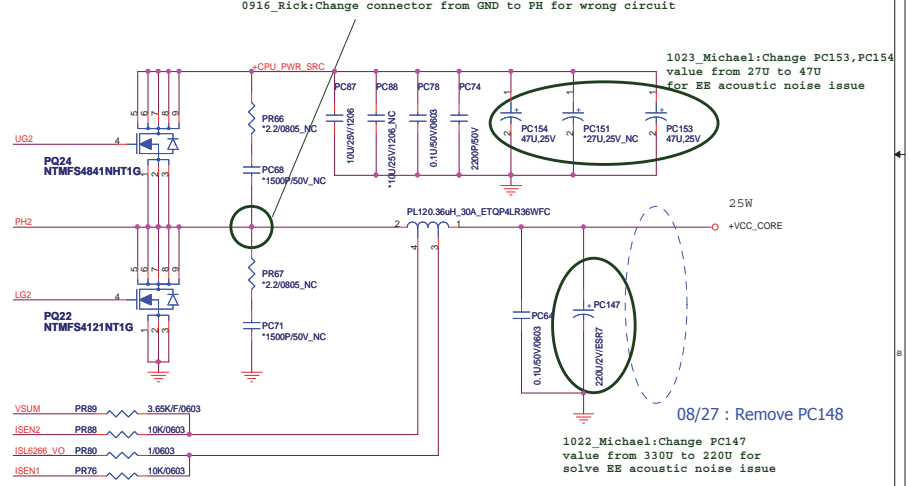
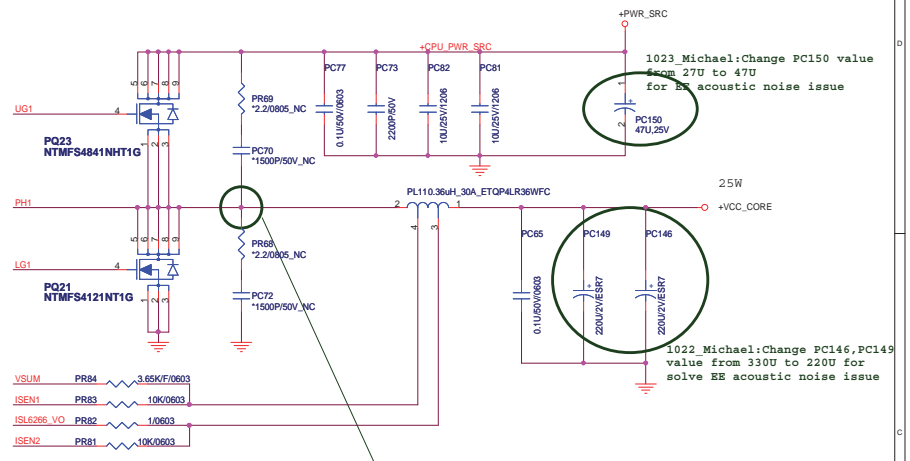
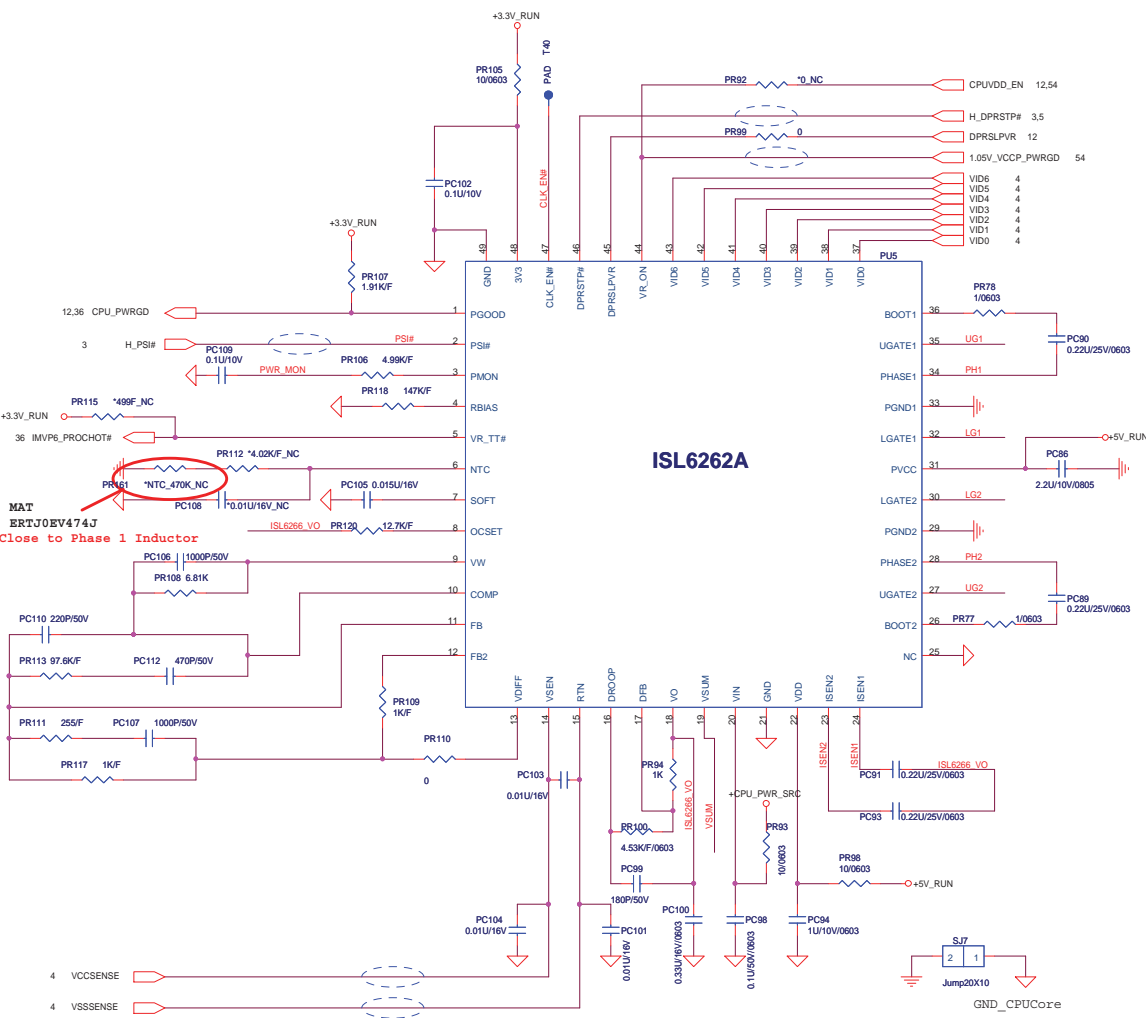
0314-Sun_Add EMI capacitor on SPD10LED#



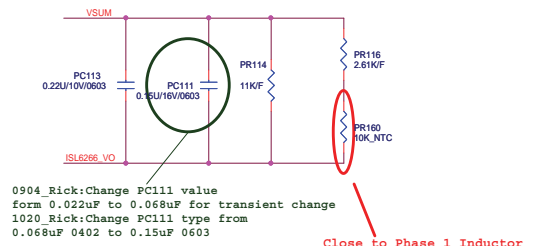




08/27 : Remove 0 ohm (PR102, PR97, PR119, PR104, PR103)

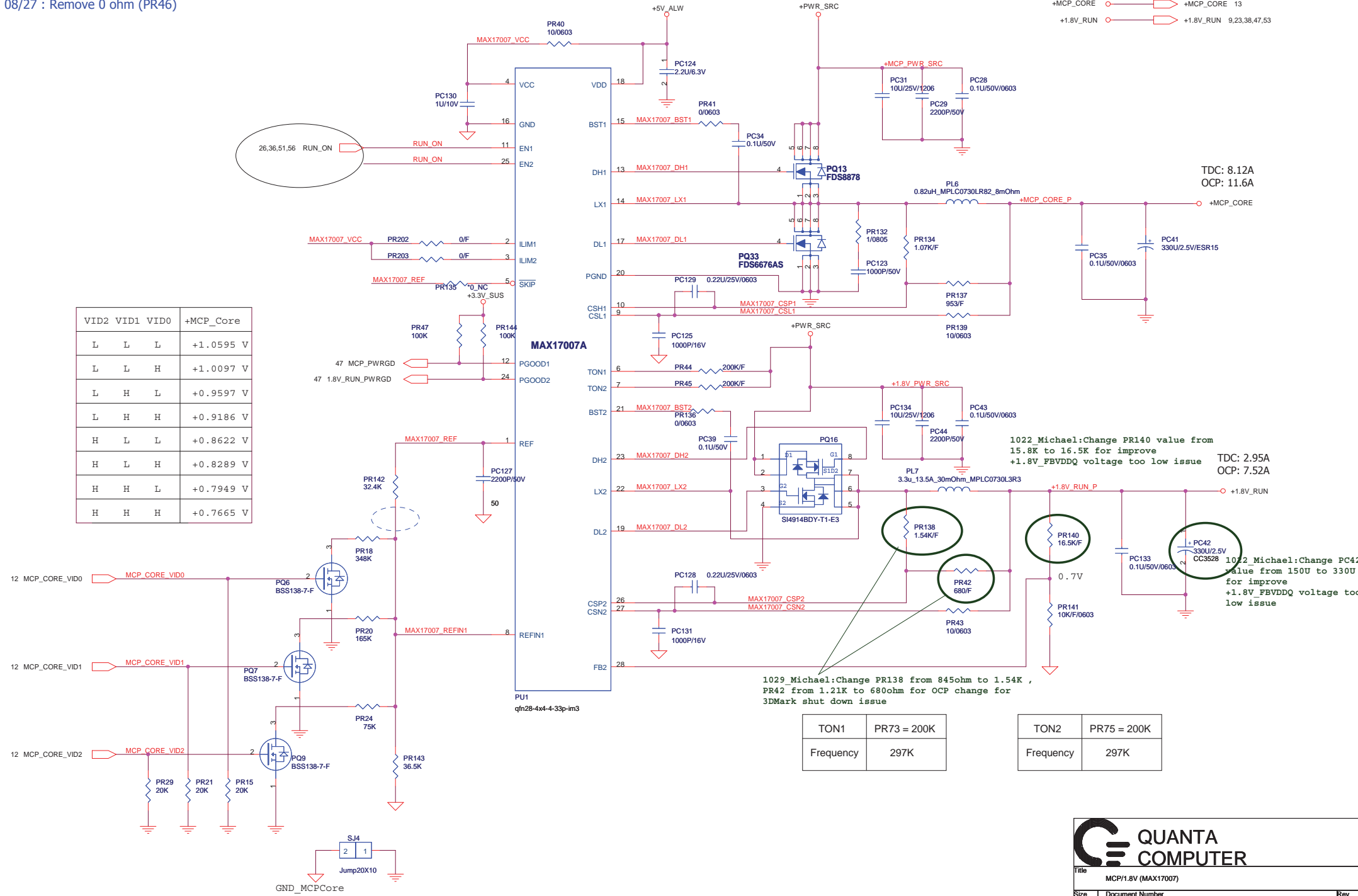


VW	PR37
Frequency	270KHZ@0A / 310KHZ@44A



08/27 : Remove 0 ohm (PR46)

+MCP_CORE ○ → +MCP_CORE 13
 +1.8V_RUN ○ → +1.8V_RUN 9,23,38,47,53



VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V

TON1	PR73 = 200K
Frequency	297K

TON2	PR75 = 200K
Frequency	297K

QUANTA COMPUTER

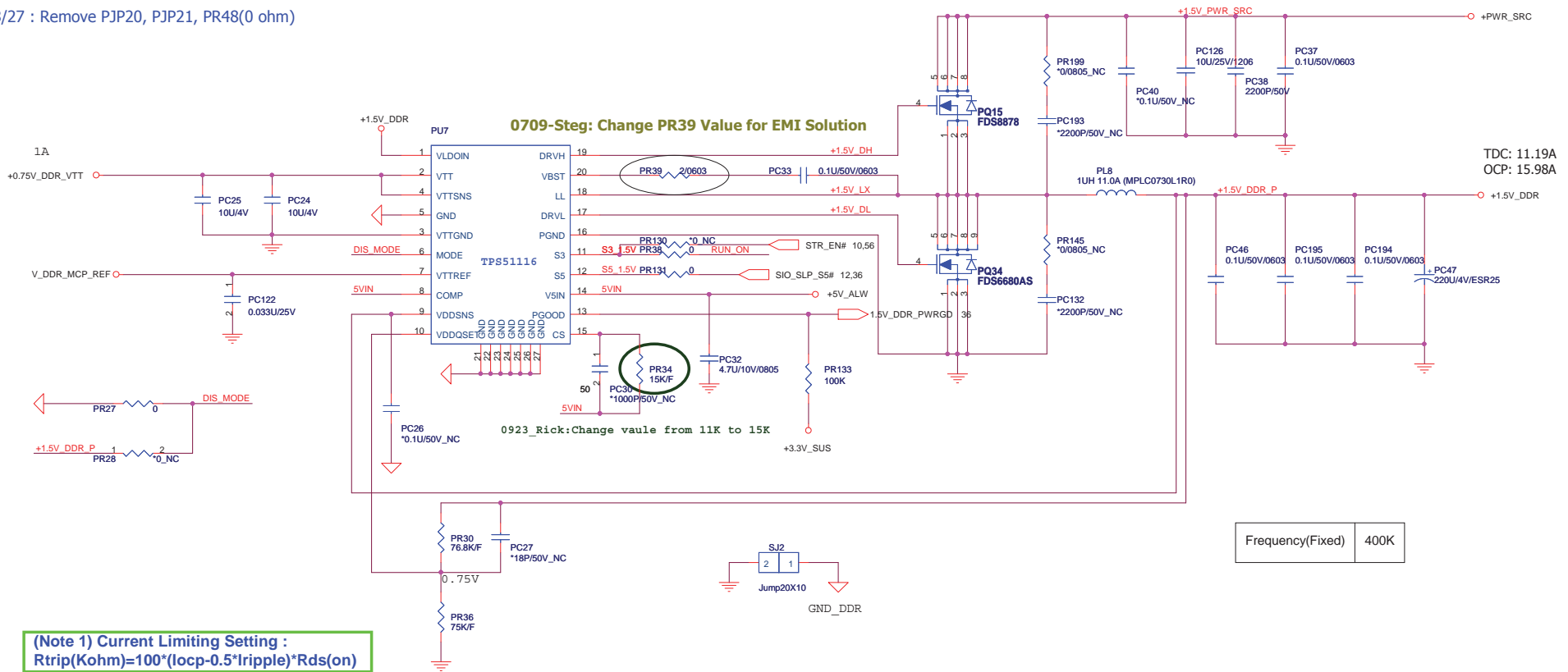
Title: MCP/1.8V (MAX17007)

Size: Document Number IM3 (XPS-Jolie) Rev 1B

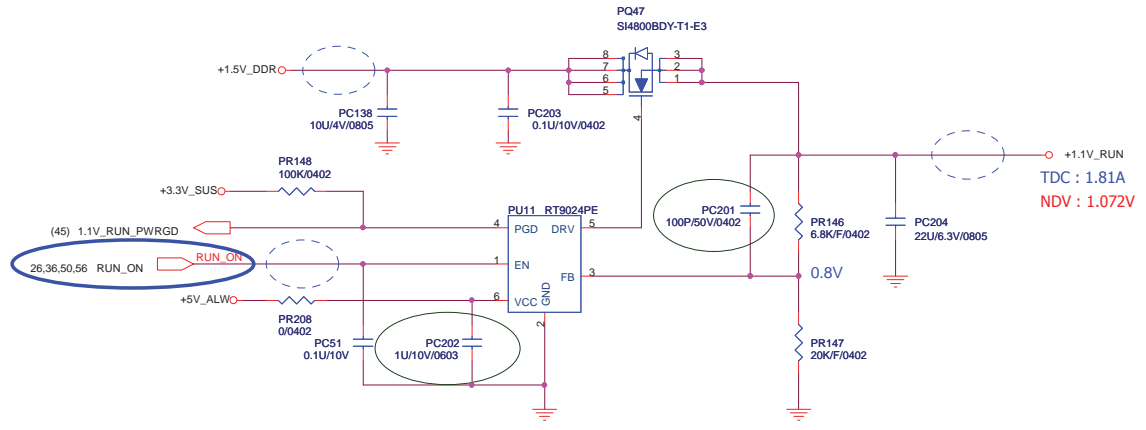
Date: Thursday, October 30, 2008 Sheet 50 of 59

- +1.5V_DDR ○ → +1.5V_DDR 15,16,47,56
- +0.75V_DDR_VTT ○ → +0.75V_DDR_VTT 15,16,56
- +1.1V_RUN ○ → +1.1V_RUN 5,7,8,9,11,12
- V_DDR_MCP_REF ○ → V_DDR_MCP_REF 15,16

08/27 : Remove PJP20, PJP21, PR48(0 ohm)



(Note 1) Current Limiting Setting :
 $R_{trip(Kohm)} = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$



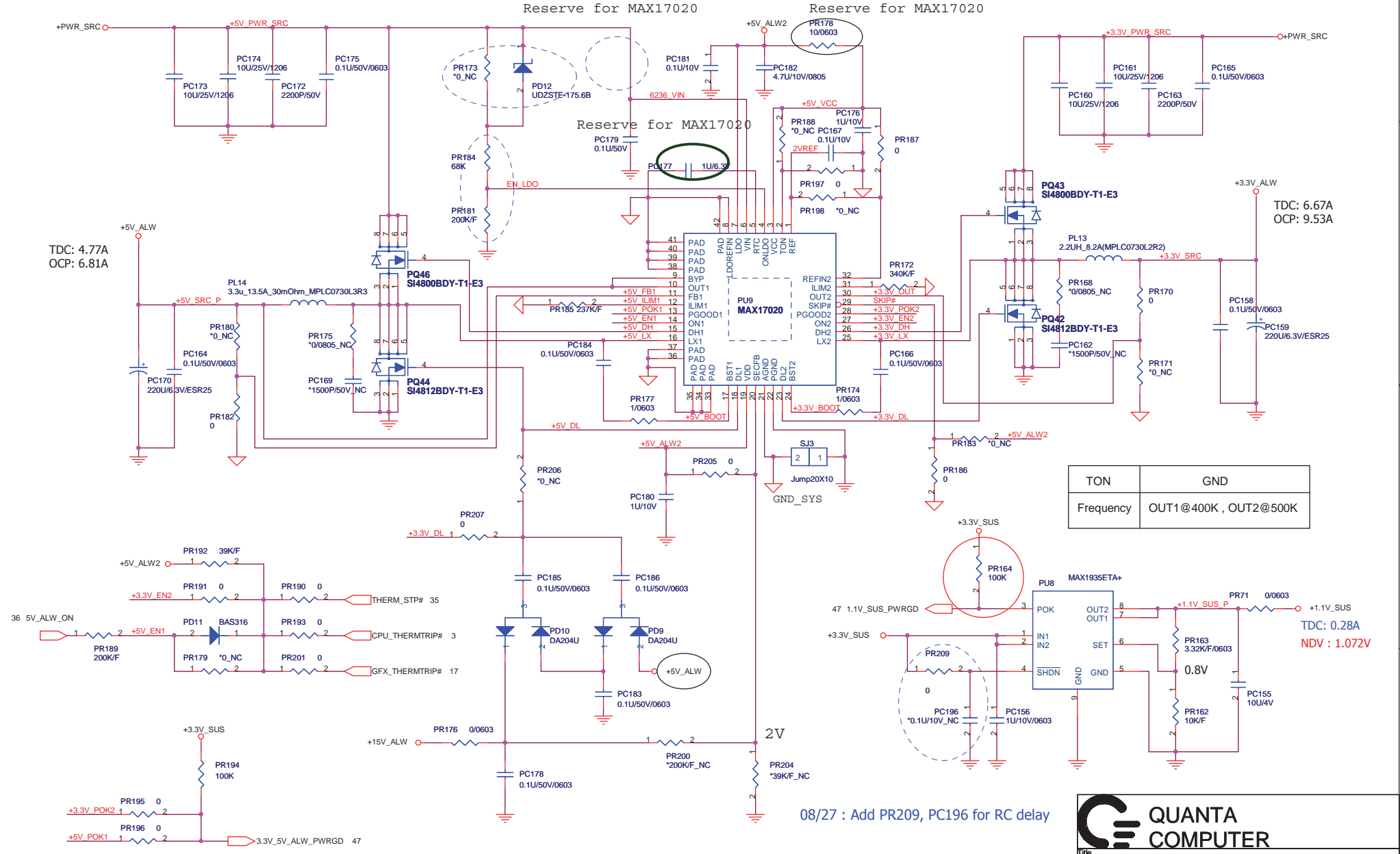
QUANTA COMPUTER

Title		1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number	Rev	
IM3 (XPS-Jolie)		1A	
Date:	Tuesday, October 28, 2008	Sheet	51 of 59

+1.1V_SUS +1.1V_SUS 13,14
 +5V_ALW +5V_ALW 15,30,31,38,39,47,50,51,53,54,56
 +3.3V_ALW +3.3V_ALW 23,26,31,32,36,37,38,39,47,48,55,56

08/27 : Remove PR169, PR173 (0 ohm)
 08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V_ALW glitch issue when adapter unplug

0916_Rick:Change PC177 value from 0.1u to 1u



TDC: 4.77A
 OCP: 6.81A

TDC: 6.67A
 OCP: 9.53A

TDC: 0.28A
 NDV : 1.072V

TON	GND
Frequency	OUT1@400K , OUT2@500K

08/27 : Add PR209, PC196 for RC delay

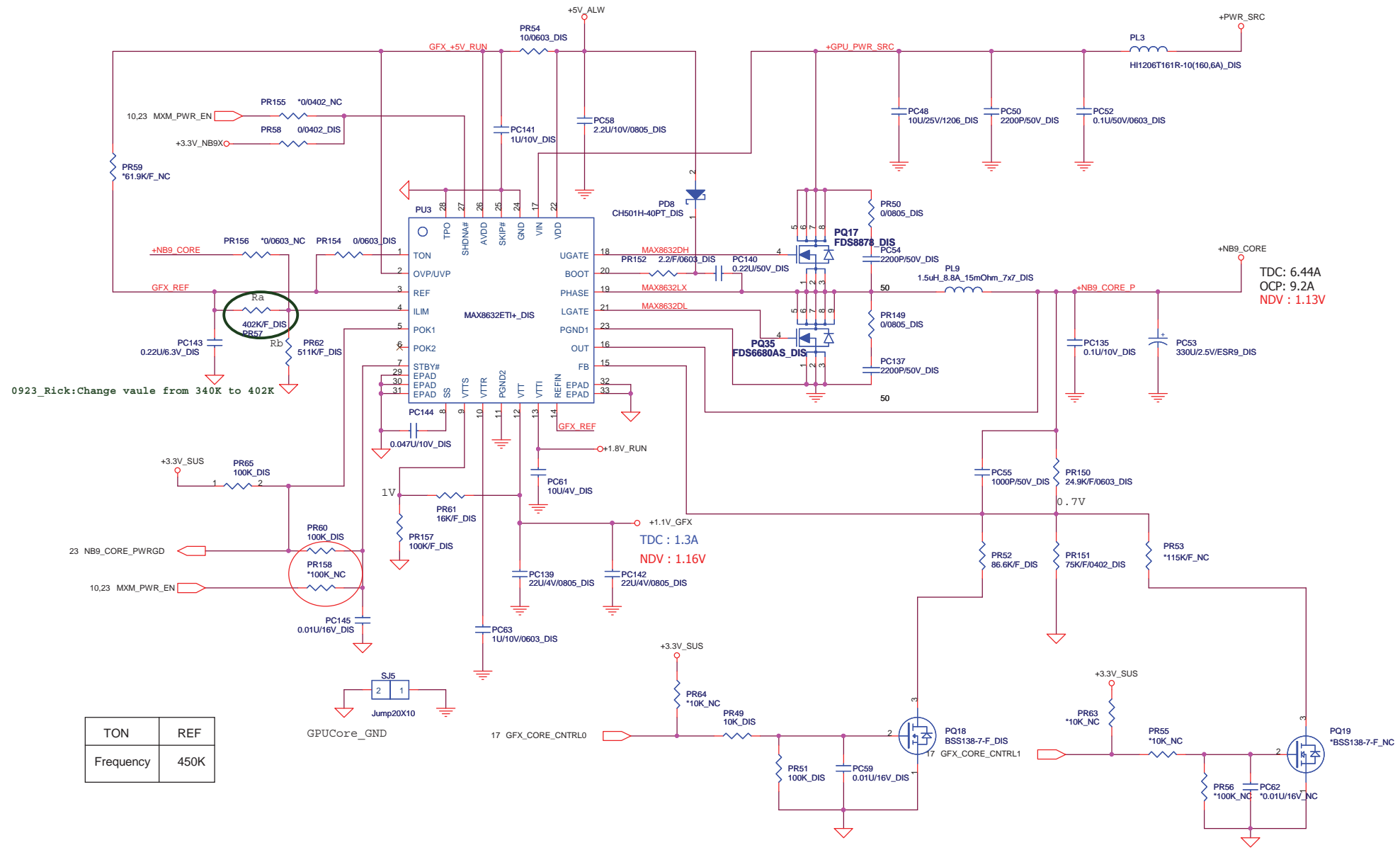
QUANTA COMPUTER

Title: SYS 5V/3V(MAX17020)

Size: Document Number IM3 (XPS-JoSe) Rev 1A

Date: Thursday, October 30, 2008 Sheet 52 of 59

+NB9_CORE 20
+1.1V_GFX 23.47



0923_Rick:Change vaule from 340K to 402K

TDC: 6.44A
OCP: 9.2A
NDV: 1.13V

TDC: 1.3A
NDV: 1.16V

TON	REF
Frequency	450K

ILIM	$I_{ovp} = (2 * (R_b / (R_a + R_b)) * 0.1 * (1 / RDSON) + (I_{DELTA} / 2))$
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVFP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

QUANTA COMPUTER

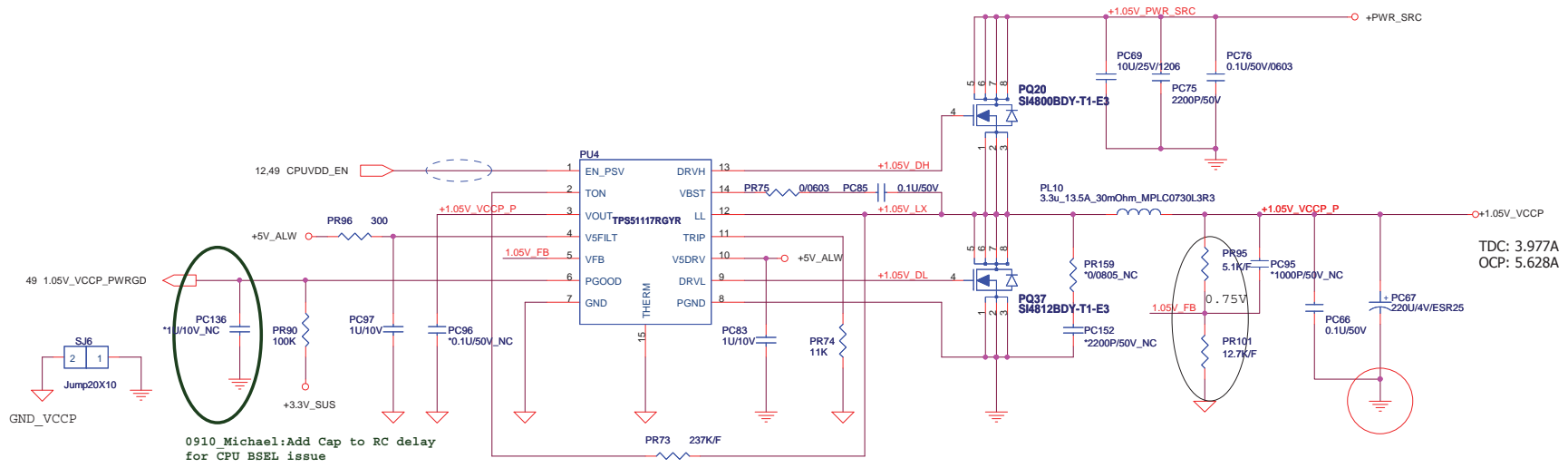
Title: VGA DC/DC

Size: Document Number IM3 (XPS-Jolie) Rev 1A

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+1.05V_VCCP +1.05V_VCCP 3,4,5,13

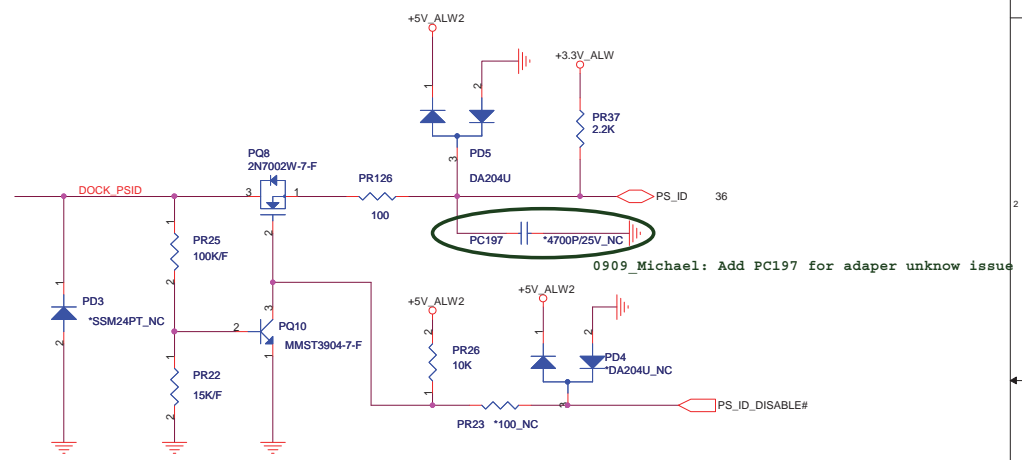
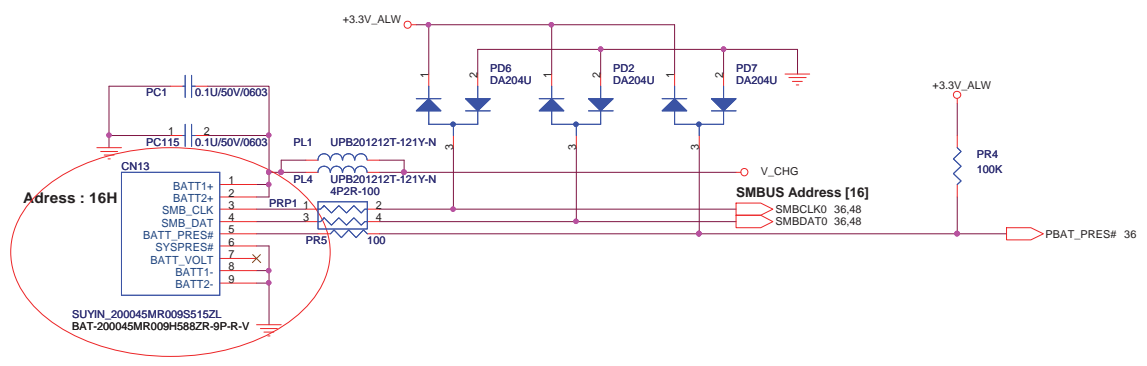
08/27 : Remove 0 ohm (PR79)



0910 Michael: Add Cap to RC delay for CPU BSEL issue

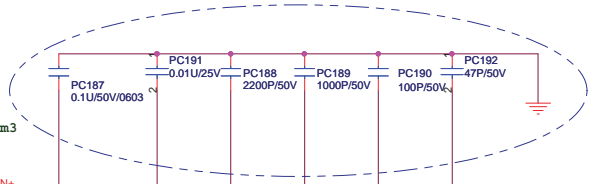
TDC: 3.977A
OCP: 5.628A

TON	PR185=237K
Frequency	300K

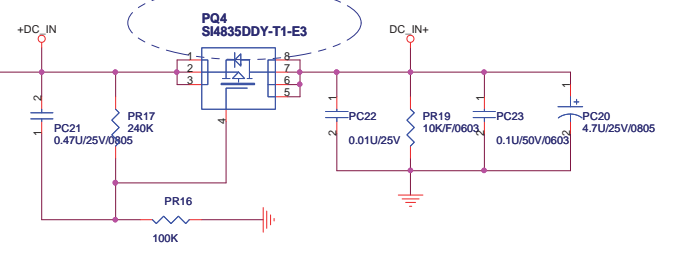


0909 Michael: Add PC197 for adaper unknow issue

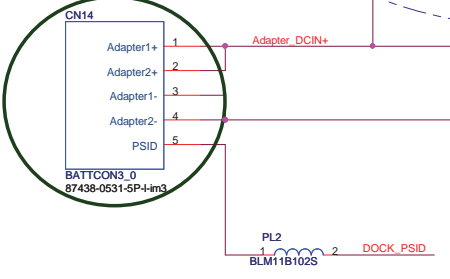
0311-Rick: Add PC187~PC192 for EMC



0709-Rick: Change PQ4 Value



0823 Michael: Change Footprint from 87438-0531-5p-L to 87438-0531-5p-1-im3

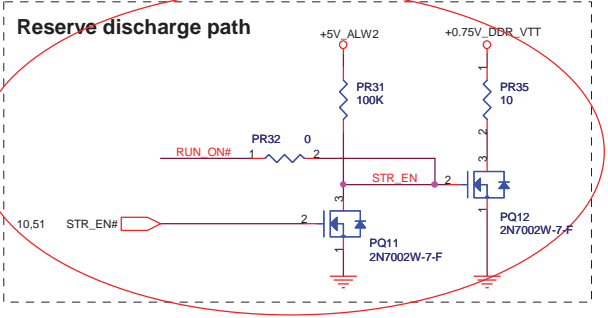
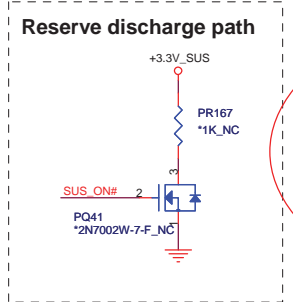
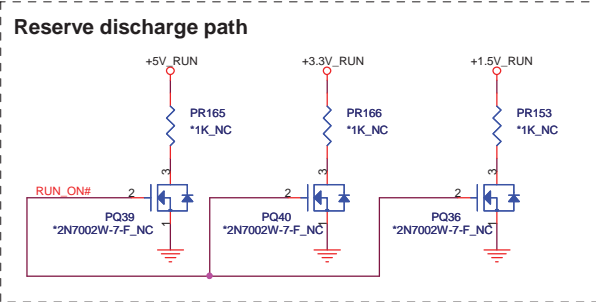
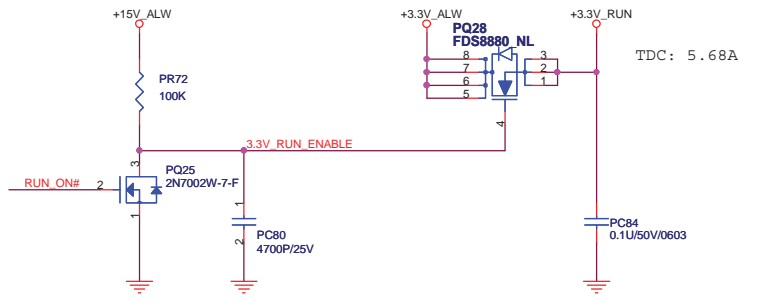
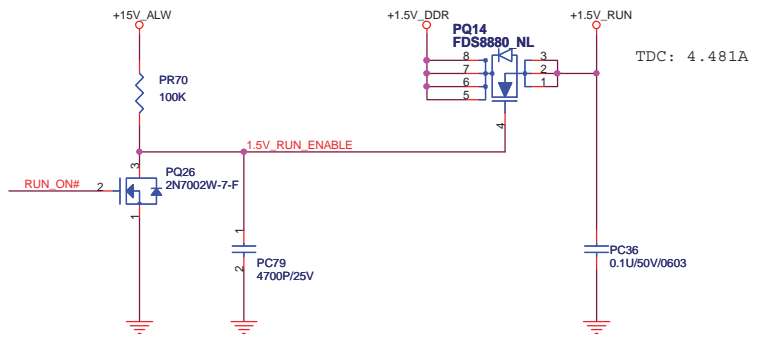
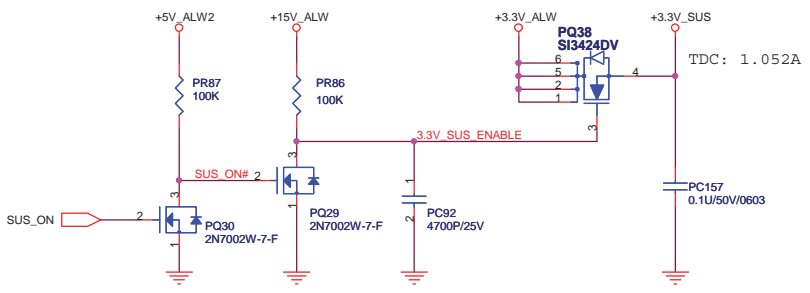
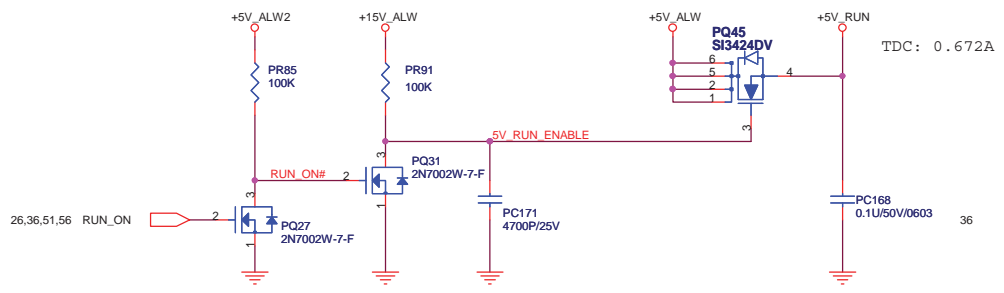


QUANTA COMPUTER

Title: DCIN,Batt

Size	Document Number	Rev
	IM3 (XPS-Jolie)	1A

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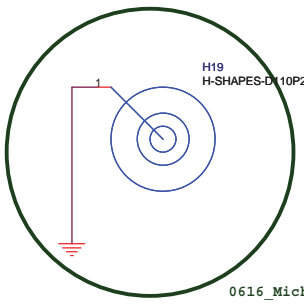


QUANTA COMPUTER

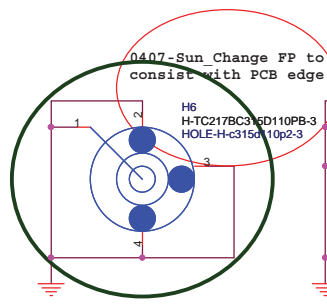
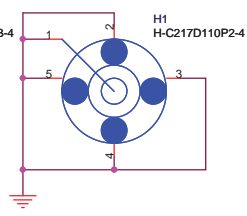
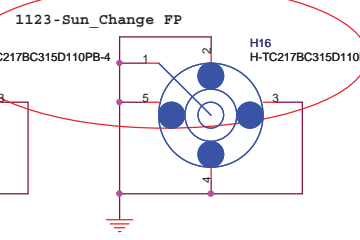
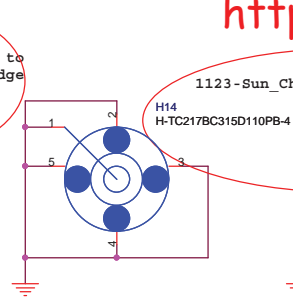
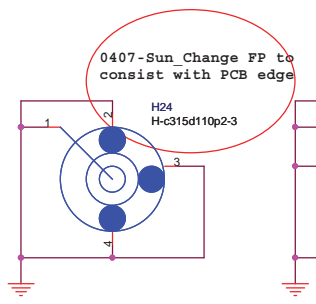
Title: RUN POWER SW

Size: Document Number IM3 (XPS-Jolie) Rev 1A

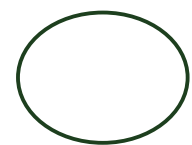
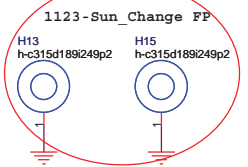
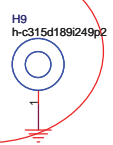
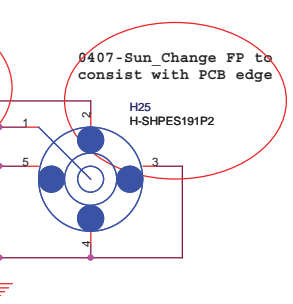
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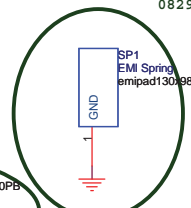
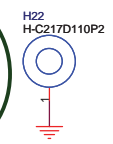
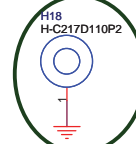
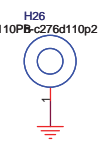
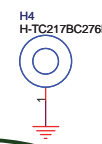
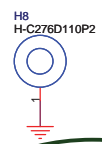
0616_Michael:Change footprint



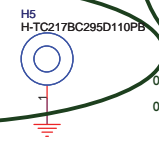
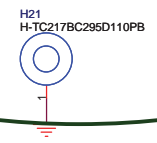
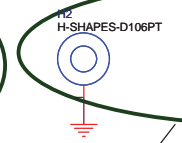
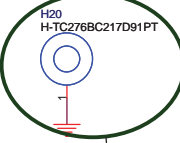
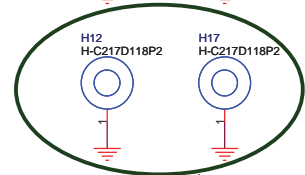
0616_Michael:Change footprint



0829_Michael:Remove H3



0605_Michael: Add connect to GND



0616_Michael:Change footprint

