Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00

```
DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
M96:DIS M96 platform installed
VRAM_1G:VRAM 128M*16 installed
Colay :Manual modify BOM
```

<Core Design>

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Title		
	Cover Page	
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Berry Block Diagram (Discrete/UMA co-lay)

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-1

1.Park-XT;512MB
(64Mx16b*4)
Dell P/N:9TGTN$AA HYNIX
Dell P/N:C995R$AA SAMSUNG
2.Park-XT;1GB (128Mx16b*4)
Dell P/N:PXFYJ$AA HYNIX
Dell P/N:C09DT$AA SAMSUNG
(1 and 2 co-lay)

##OnMainBoard
VRAM 1GB/512MB 85,86,87,88
DDR3 800MHz
Clock Generator SLG8SP585 7
AMD Graphic Park-XT (Discrete only) 80,81,82,83,84
PCIe x 16 (Discrete only)
Intel CPU Arrandale 8,9,10,11,12,13,14
DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B
DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19
FDIx4x2 (UMA only)
DMIx4
Discreet/UMA Co-lay
HDMI 57
LCD 54
HDMI Level shifter 57
LVDS(Dual Channel)
RGB CRT
Intel PCH HM57
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28
PCIE x 3
SATA x 1
USB 2.0 x 4
I/O Board Connector 76
PCIE x 1 USB x 1
PCIE x 1
Mini-Card 802.11a/b/g
10/100 NIC Realtek RTL8103T-VB
RJ45 CONN
SATAx1 / USB2.0x1
ESATA/USB Combo
PCIE x 1,USB x 1
Mini-Card WWAN
SIM
USB 2.0 x 1
Right Side: USB x 1
CRT
Left Side: USB x 2
CRT Board 77
Bluetooth 73
CAMERA 54
USB2.0 x 4
AZALIA
USB 2.0 x 1
CardReader Realtek RTS5159 78
SD/MMC+/MS/ MS Pro/xD
Internal Analog MIC
HP1
MIC IN
2CH SPEAKER
Azalia CODEC IDT 92HD79B1 30
SPI
Flash ROM 4MB 62
LPC Bus
LPC debug port 70
SATA x 2
HDD 59
ODD 59
KBC NUVOTON NPCE781BA0DX 37
SPI
SMBus
Flash ROM 256kB 62
Touch PAD 68
Int. KB 68
Thermal Main:G7922 Sec.EMC2102 39
Fan 58

CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA

SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA

Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: Block Diagram
Size: A3 | Document Number: Berry | Rev: A00
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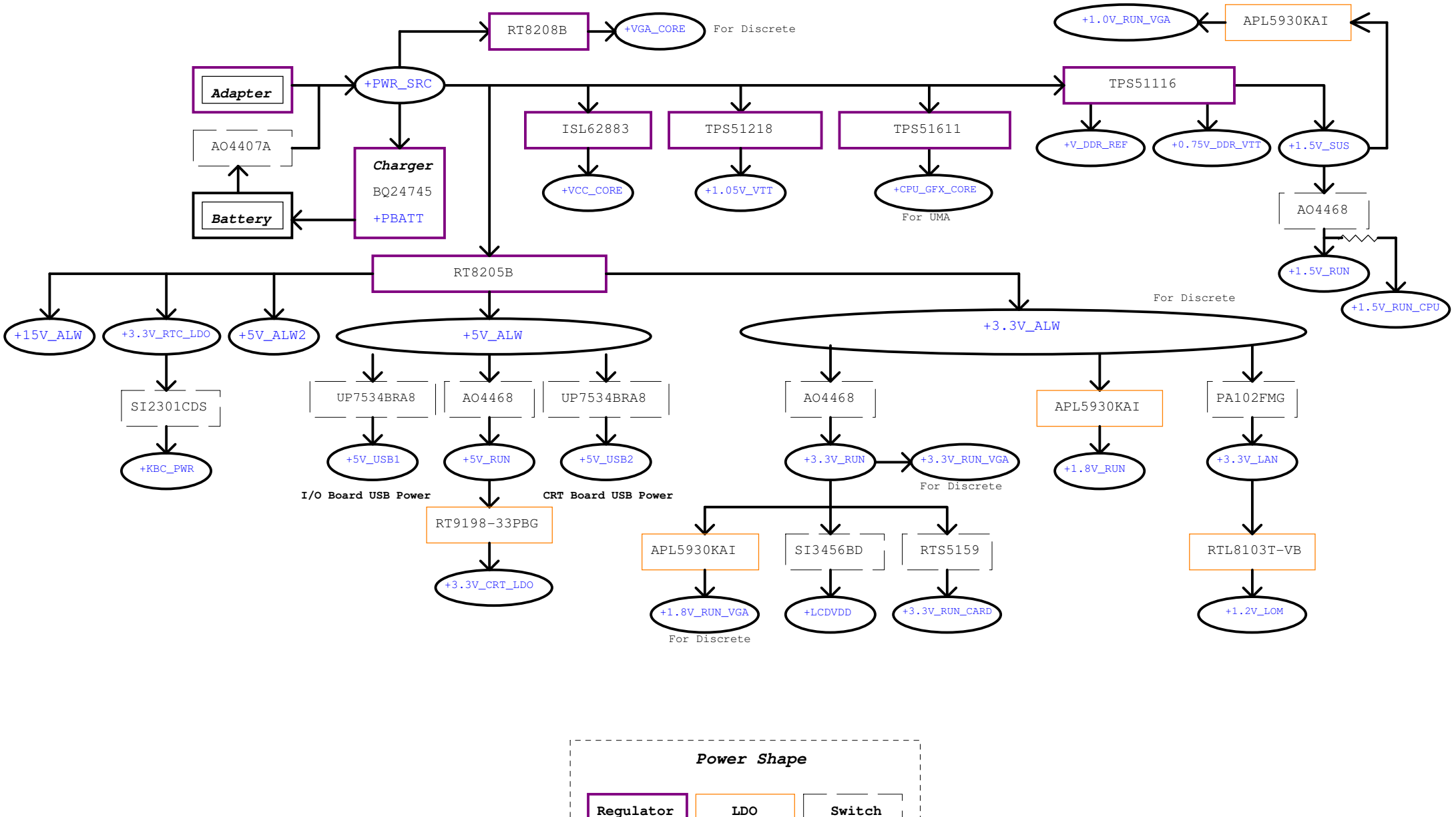

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Title: Power Block Diagram

Size	Document Number	Rev
A3	Berry	A00

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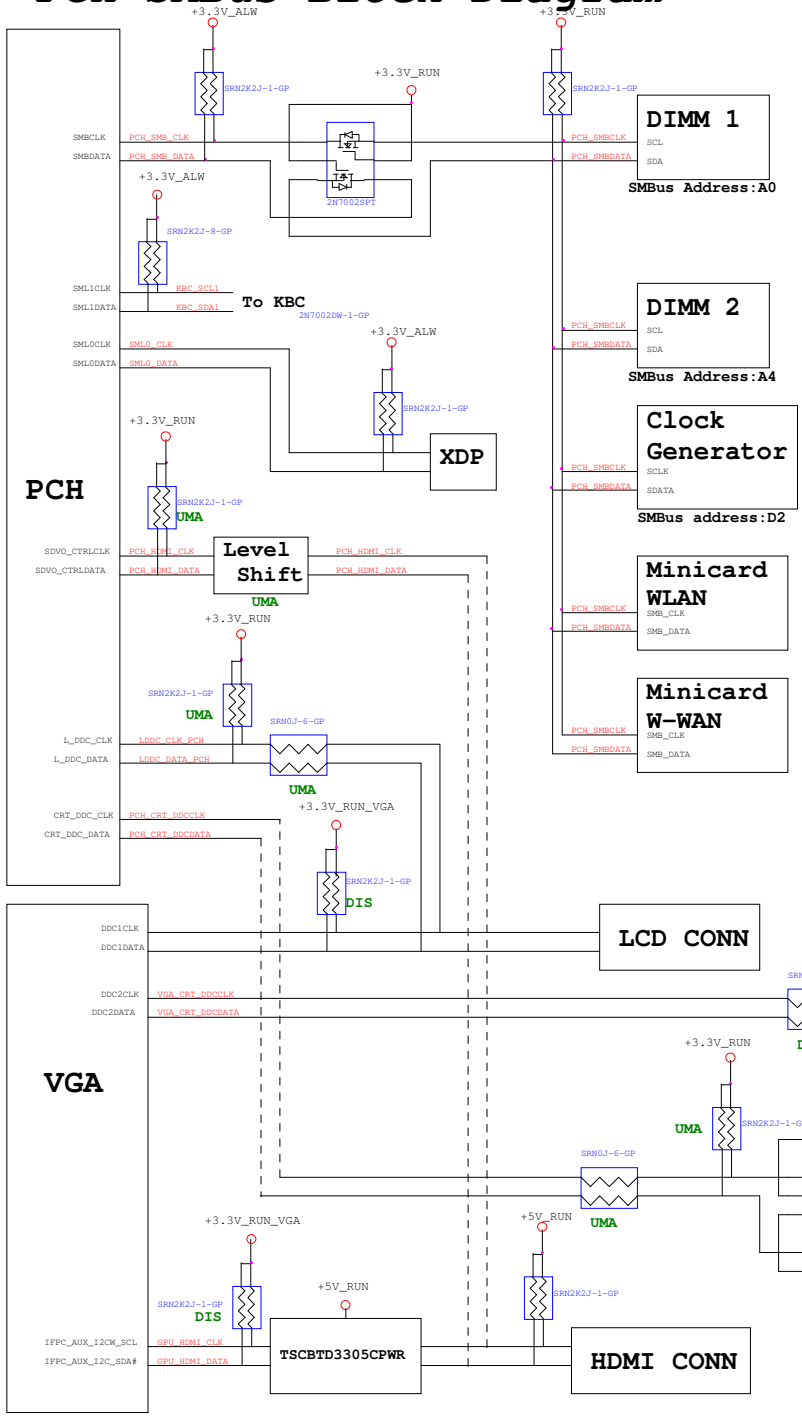
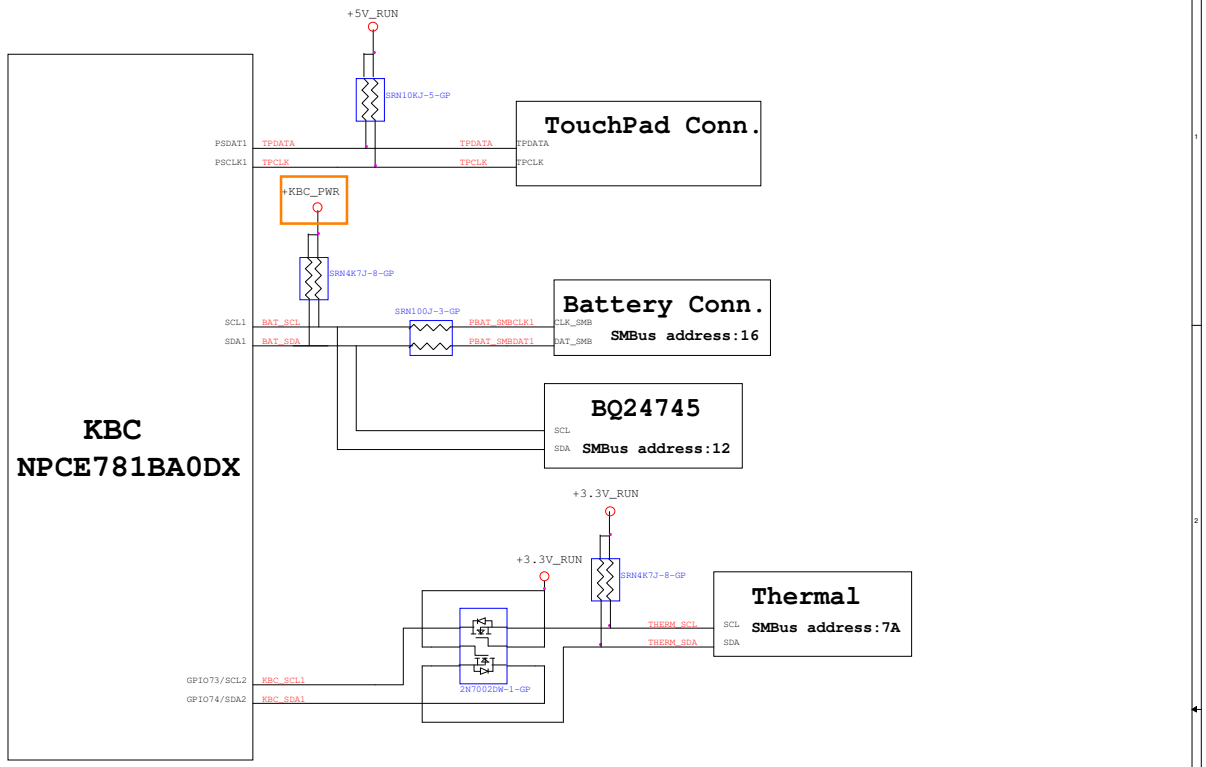
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Berry	A00

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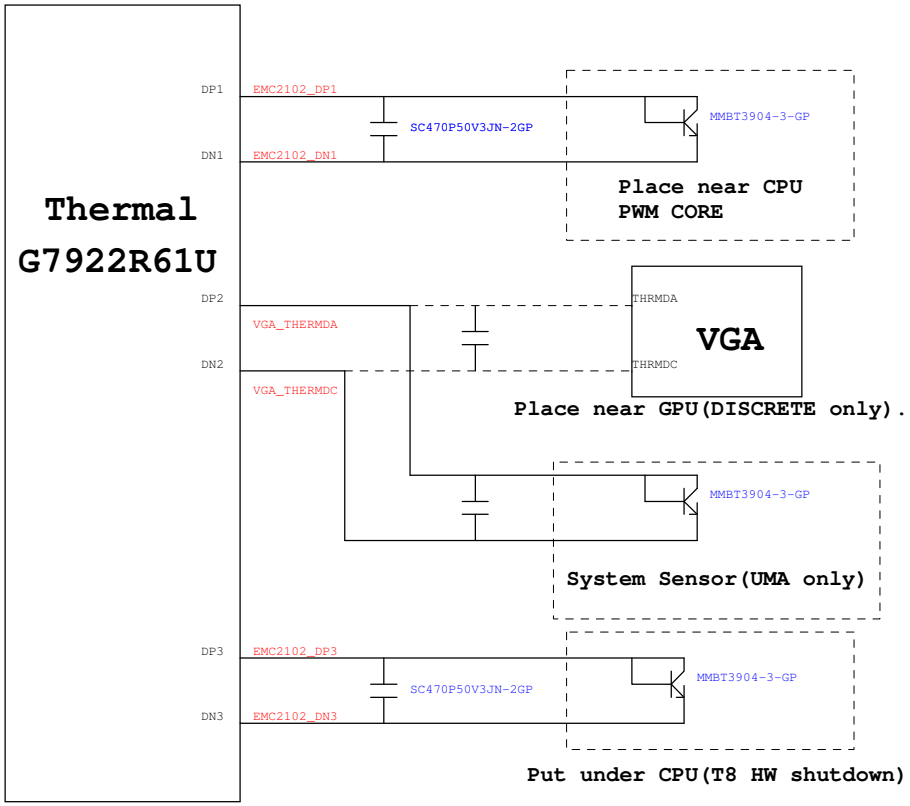
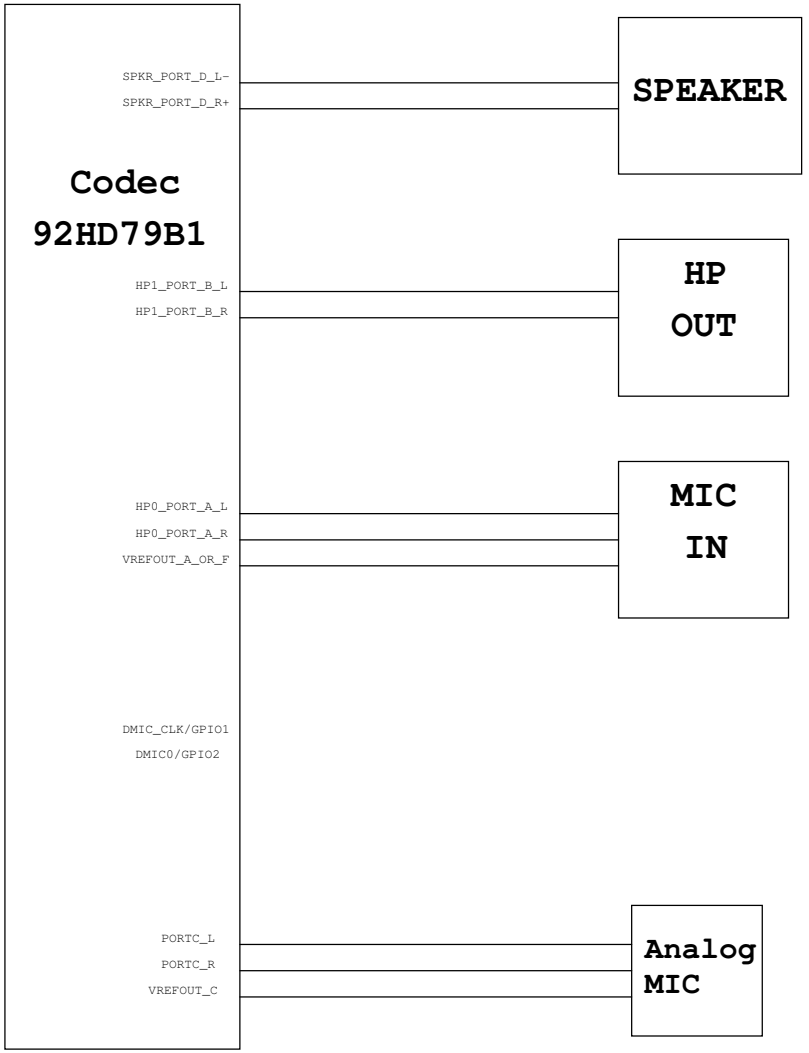
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Berry | Rev: A00

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

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Title: Table of Content

Size	Document Number	Rev
A3	Berry	A00

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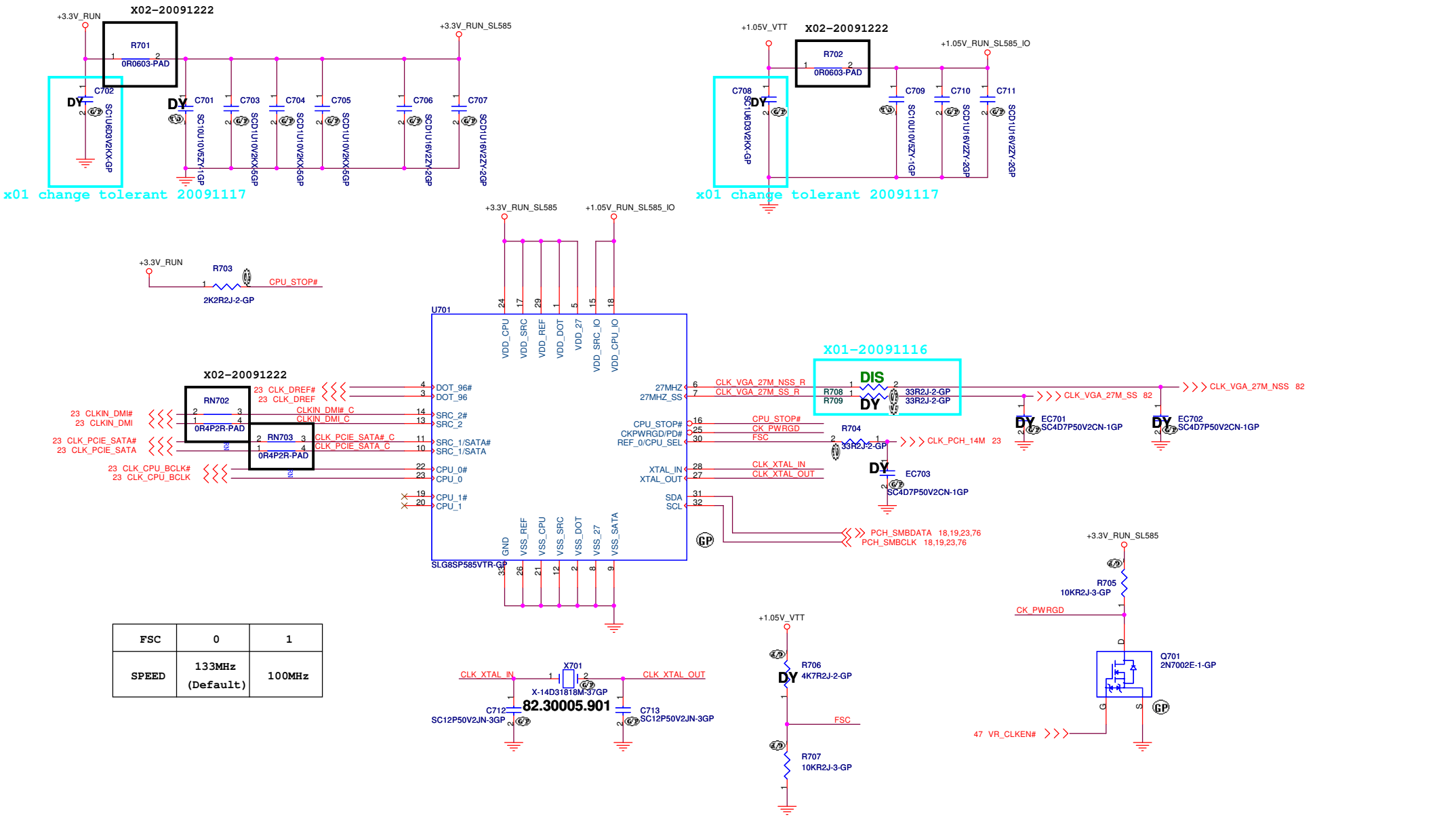
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

Size | Document Number: Berry | Rev: A00

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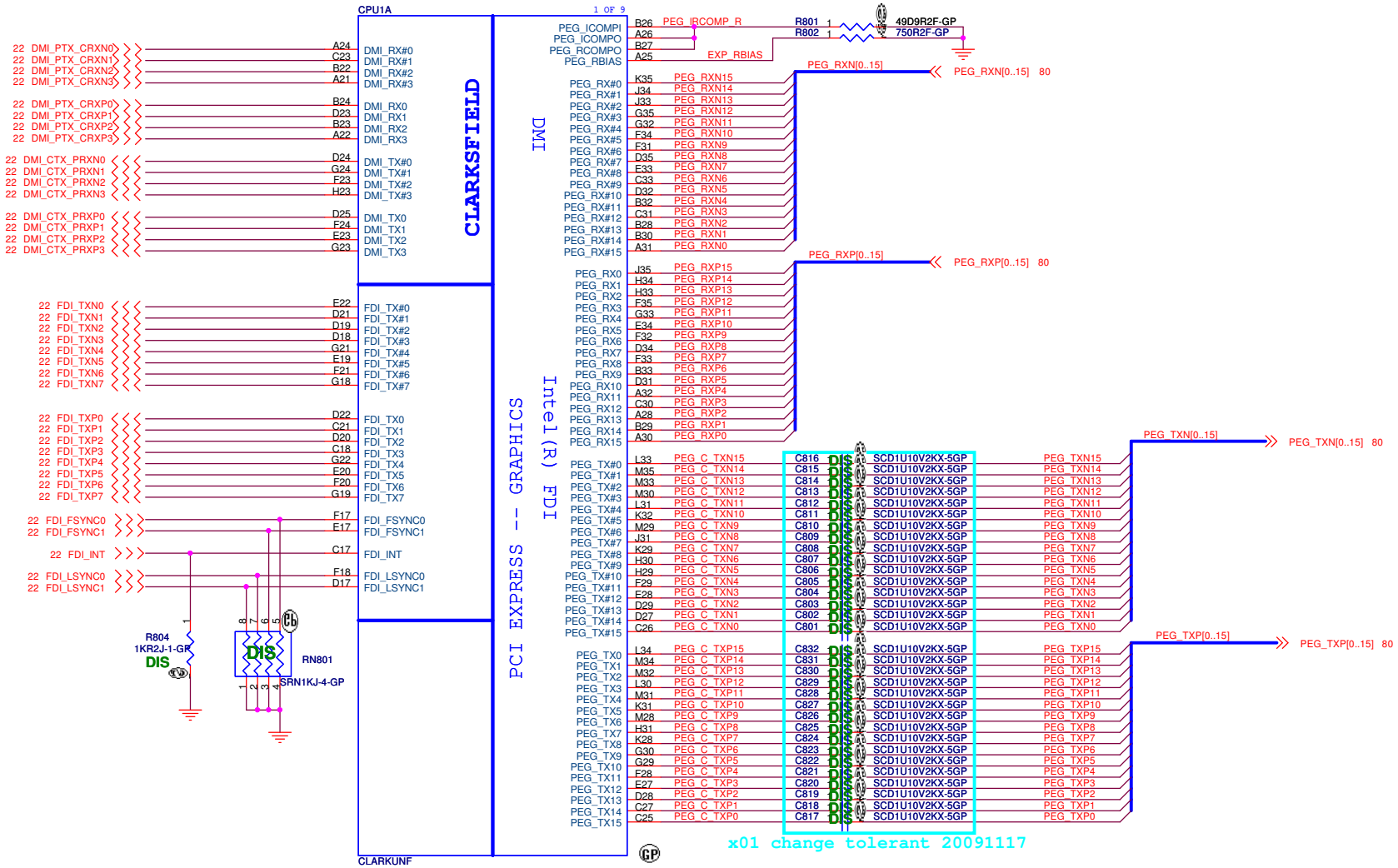
SSID = CPU



62.10055.341

SEC. 62.10053.561

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Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
	Berry	A00

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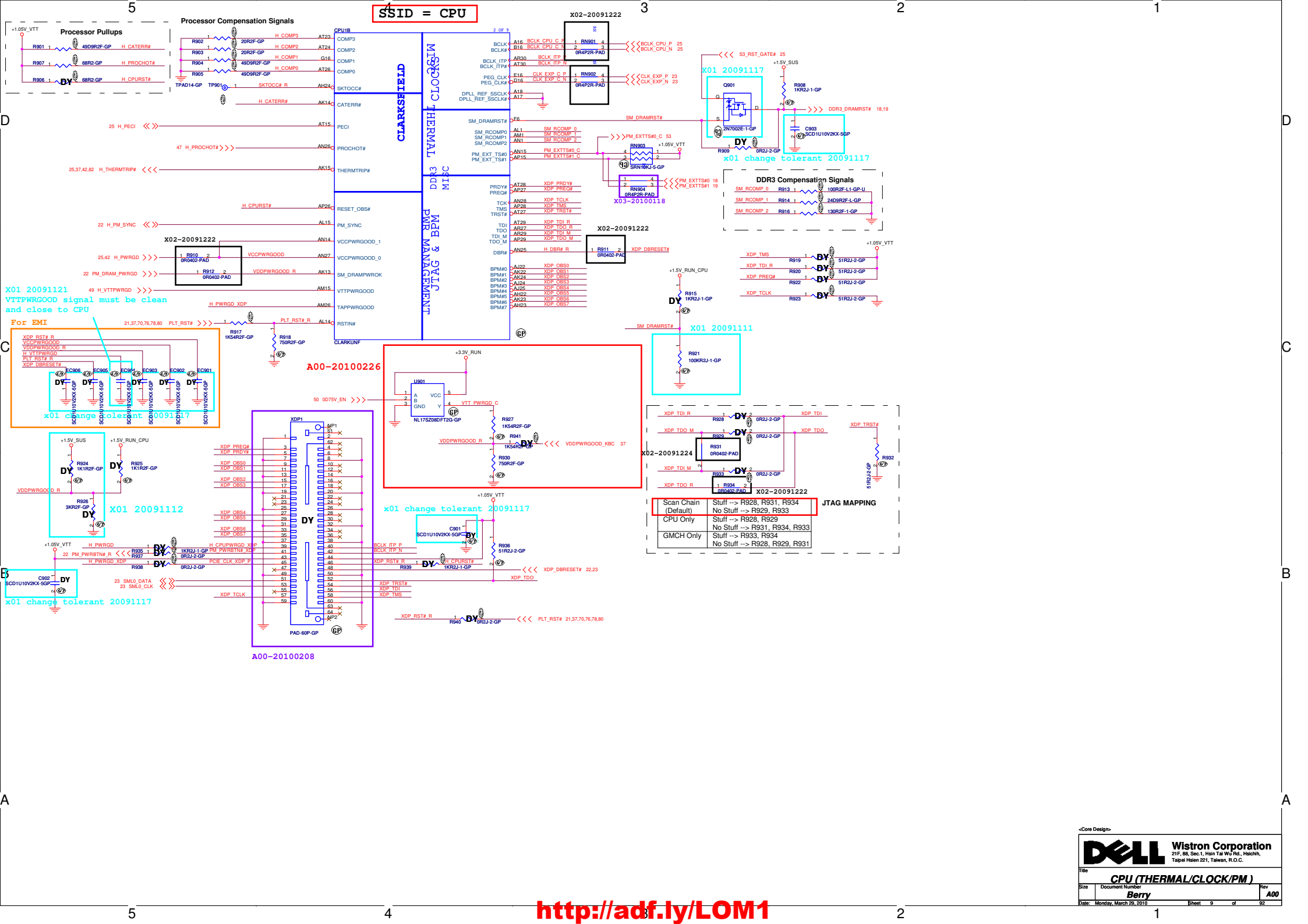
SSID = CPU
Processor Pullups
Processor Compensation Signals
CLARKSFIELD
THERMAL
CLOCKS
MISC
DDR3
MISC
PWR MANAGEMENT
JTAG & BPM
CLARKUNF
DDR3 Compensation Signals
X01 20091121
VTTPWRGOOD signal must be clean
and close to CPU
For EMI
x01 change tolerant 20091117
X01 20091112
A00-20100226
A00-20100208
X01 20091117
X01 20091111
X02-20091222
X03-20100118
X02-20091224
JTAG MAPPING
Scan Chain (Default) Stuff --> R928, R931, R934
No Stuff --> R929, R933
CPU Only Stuff --> R928, R929
No Stuff --> R931, R934, R933
GMCH Only Stuff --> R933, R934
No Stuff --> R928, R929, R931
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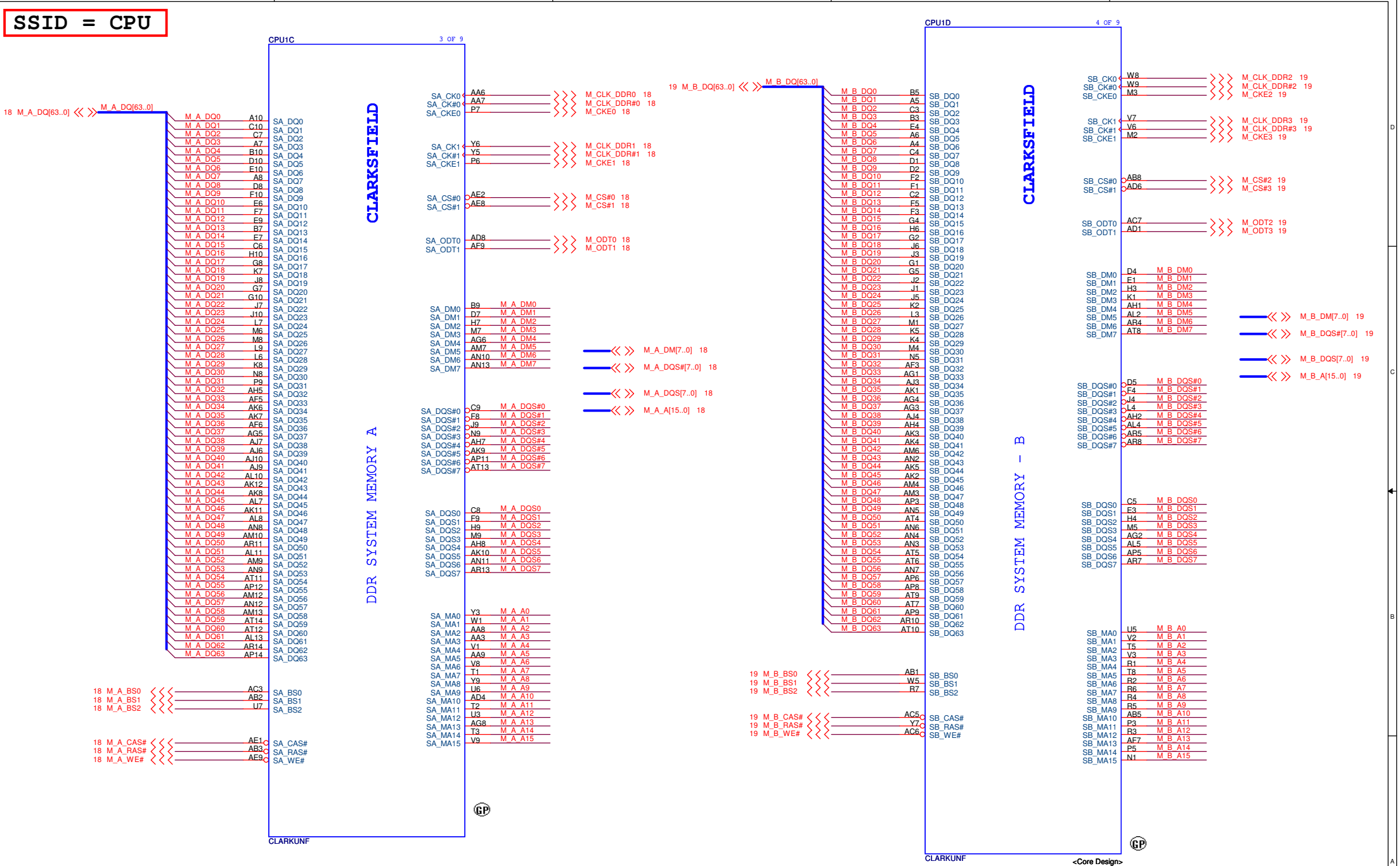
CPU (THERMAL/CLOCK/PM)
Berry
A00
Monday, March 29, 2010
http://adf.ly/LOM1

SSID = CPU



Title	CPU (DDR)	
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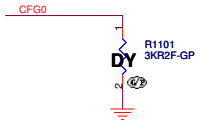
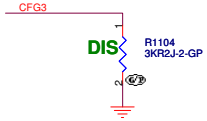
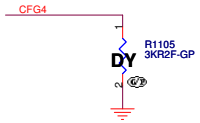
SSID = CPU



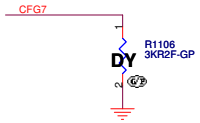
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



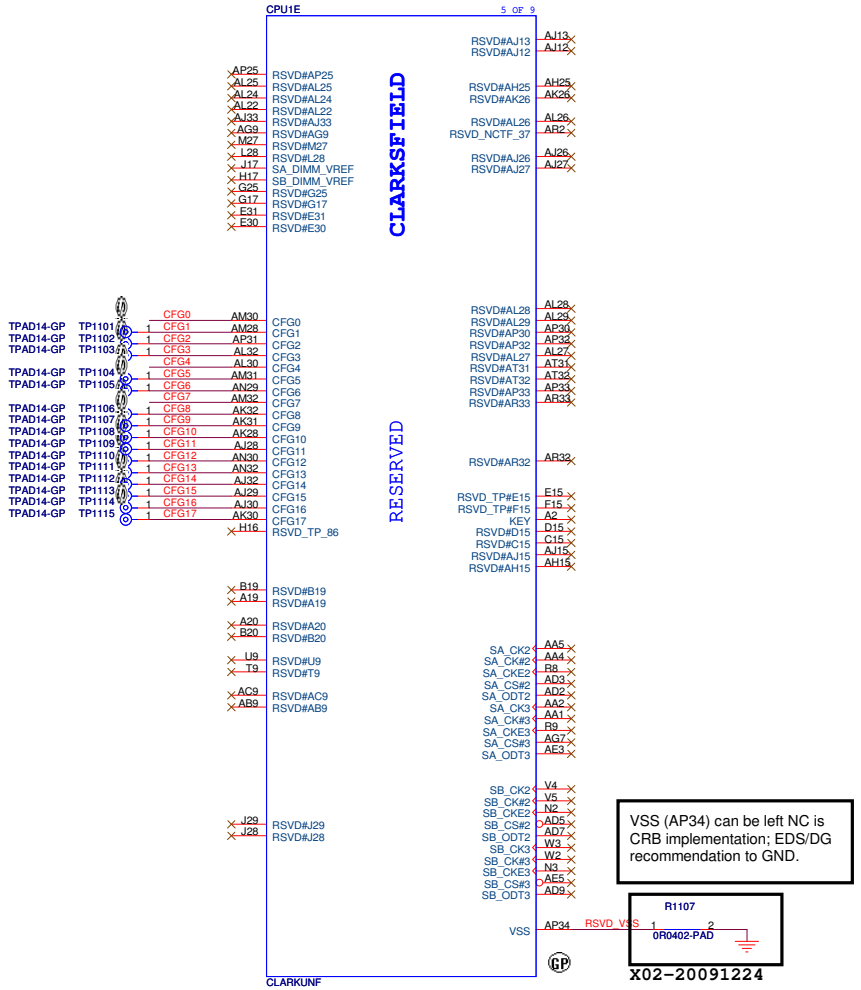
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



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Title: CPU (RESERVED)

Size | Document Number: Berry | Rev: A00

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SSID = CPU

PROCESSOR CORE POWER

48A

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

CPU VIDS

SENSE LINES

POWER

CLARKUNF

+VCC_CORE

+1.05V_VTT

x01 change tolerant 20091117

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

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Title: CPU (VCC_CORE)

Size | Document Number: Berry | Rev: A00

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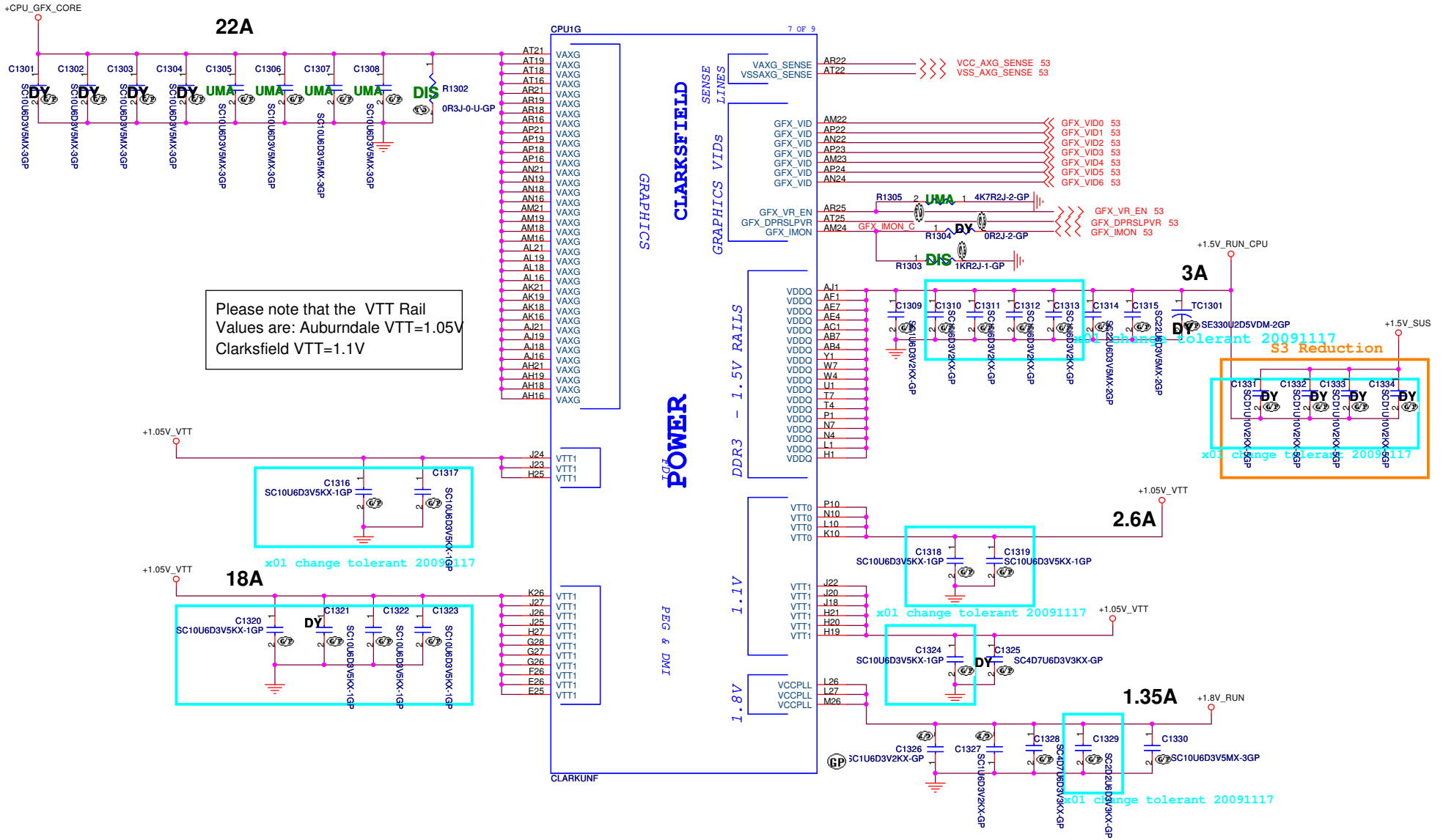
SSID = CPU



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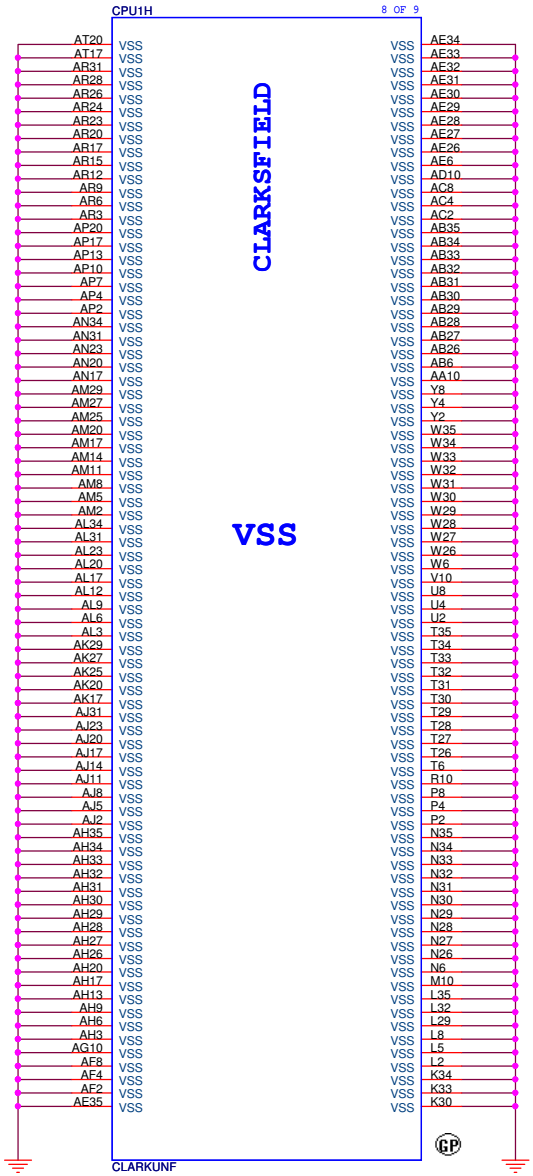

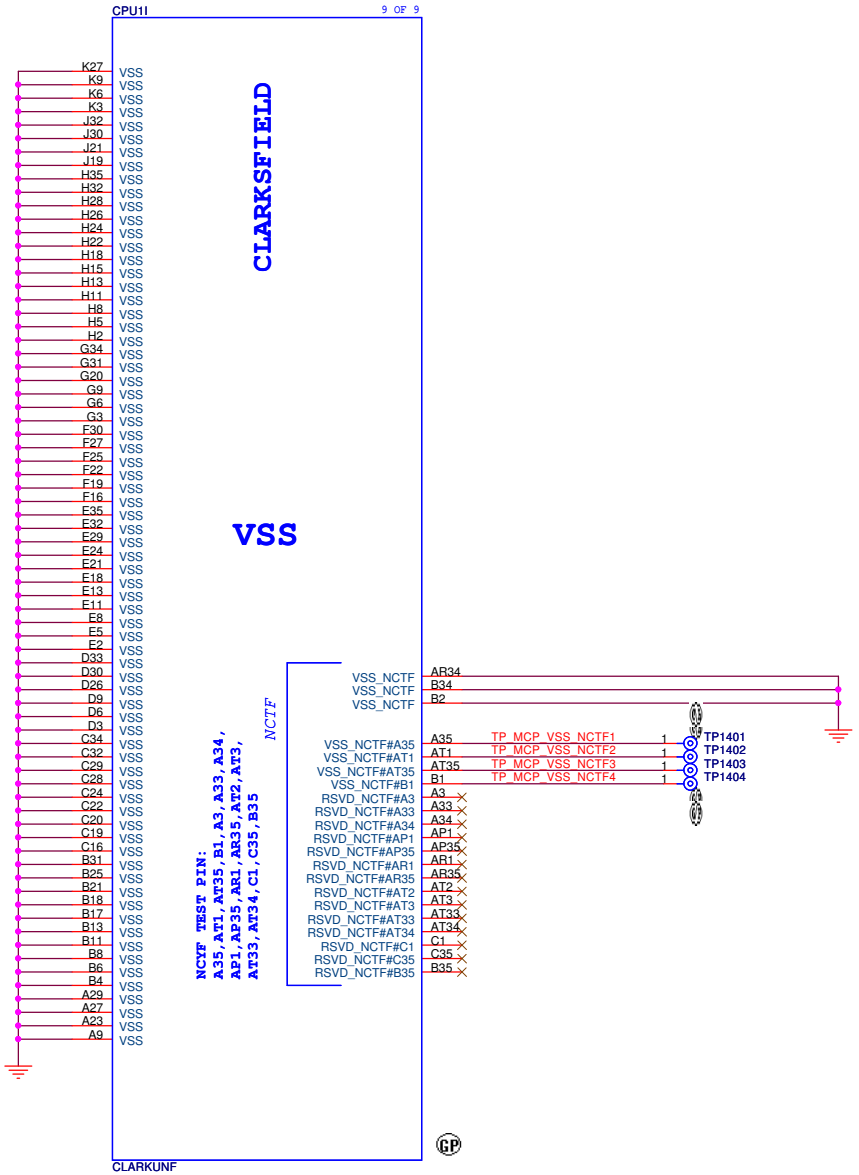

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Title	CPU (VSS)	
Size	Document Number: Berry	Rev: A00
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Title: *Reserved*		
Size: A3	Document Number: *Berry*	Rev: *A00*
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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

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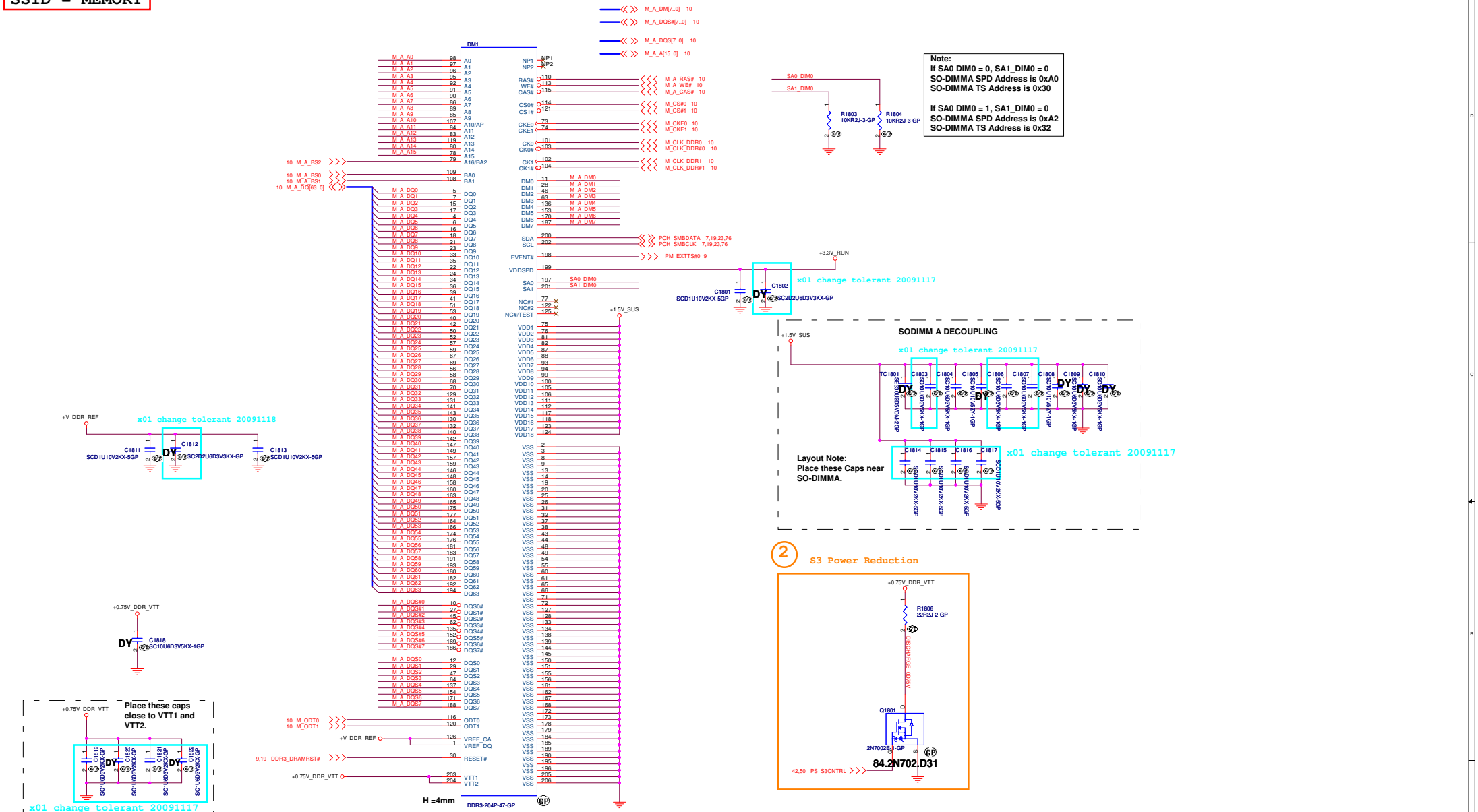
SSID = MEMORY



62.10017.P31

SEC. 62.10017.P11

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Title: DDR3-SODIMM1

Size | Document Number: Berry | Rev: A00

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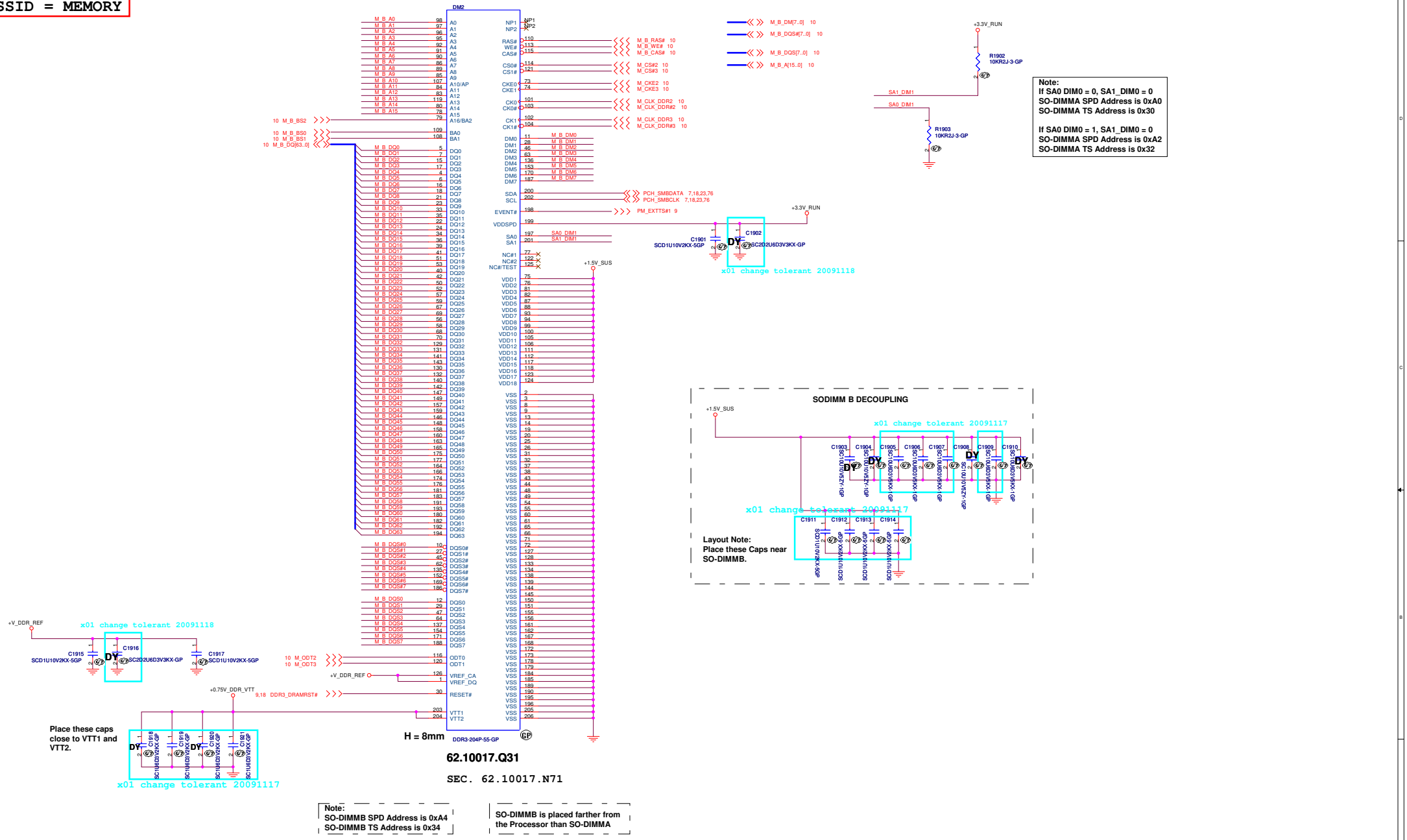

62.10017.Q31

SEC. 62.10017.N71

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Title: DDR3-SODIMM2

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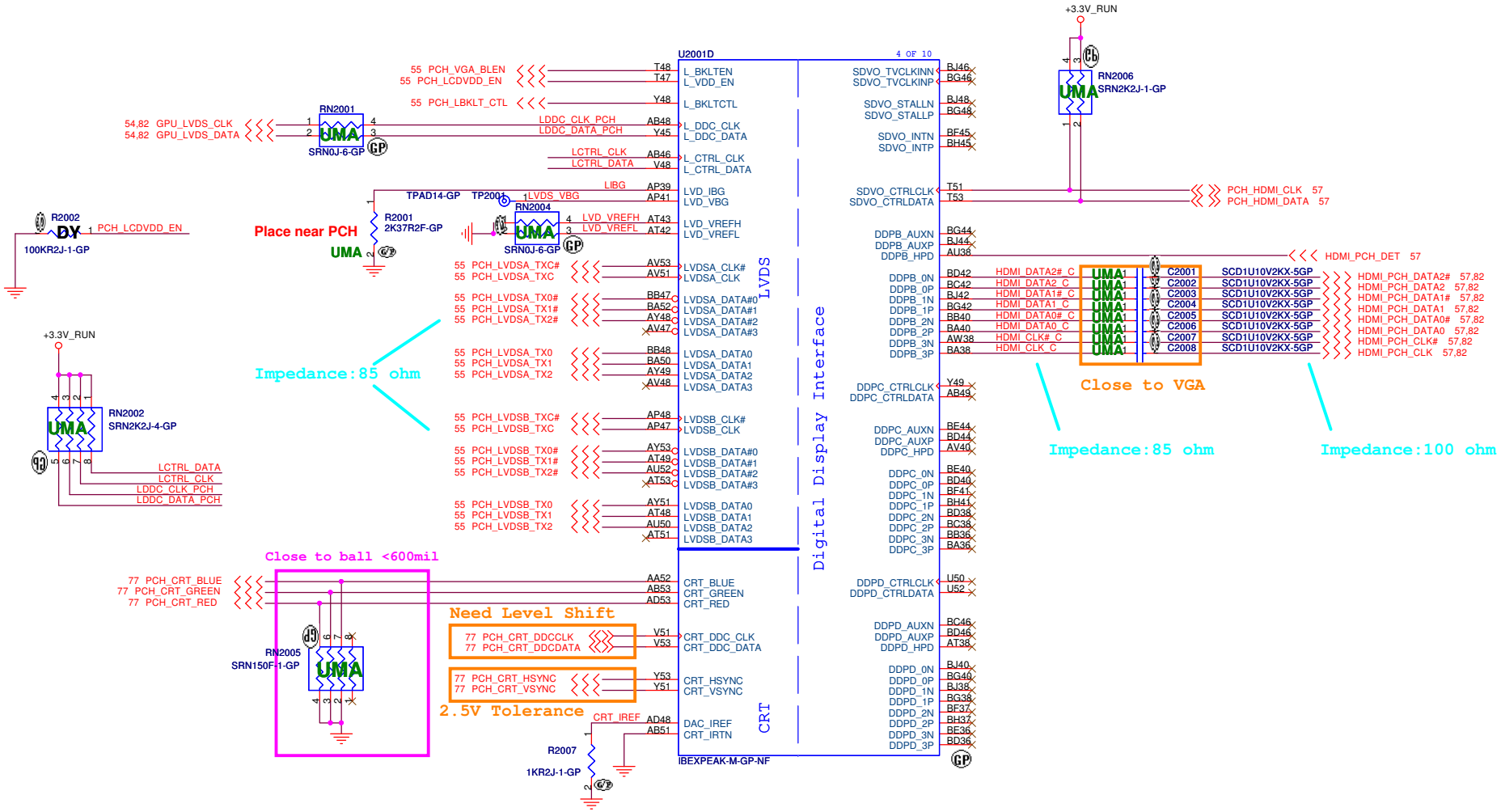

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Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
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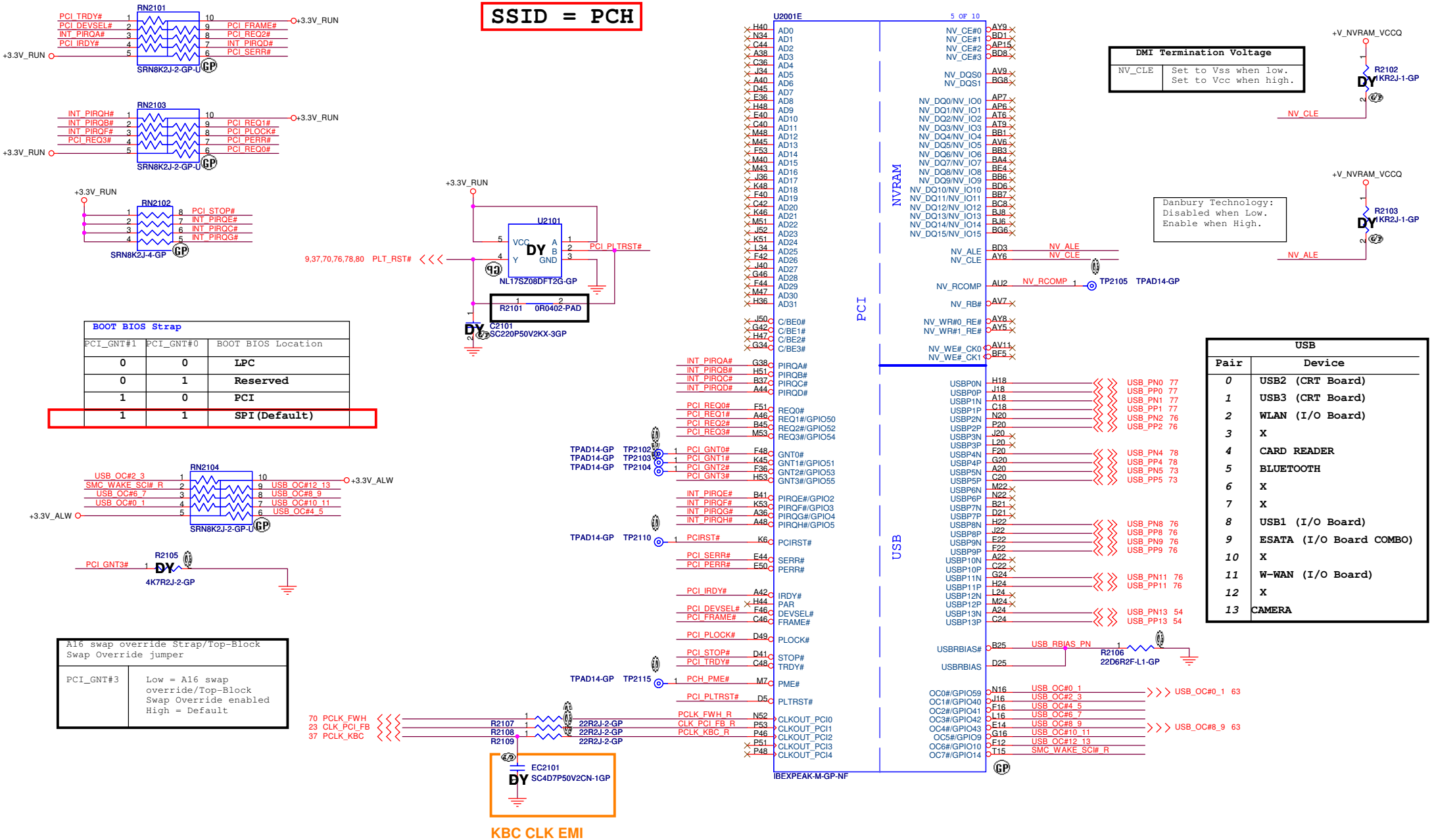
SSID = PCH



<Core Design>

Wistron Corporation
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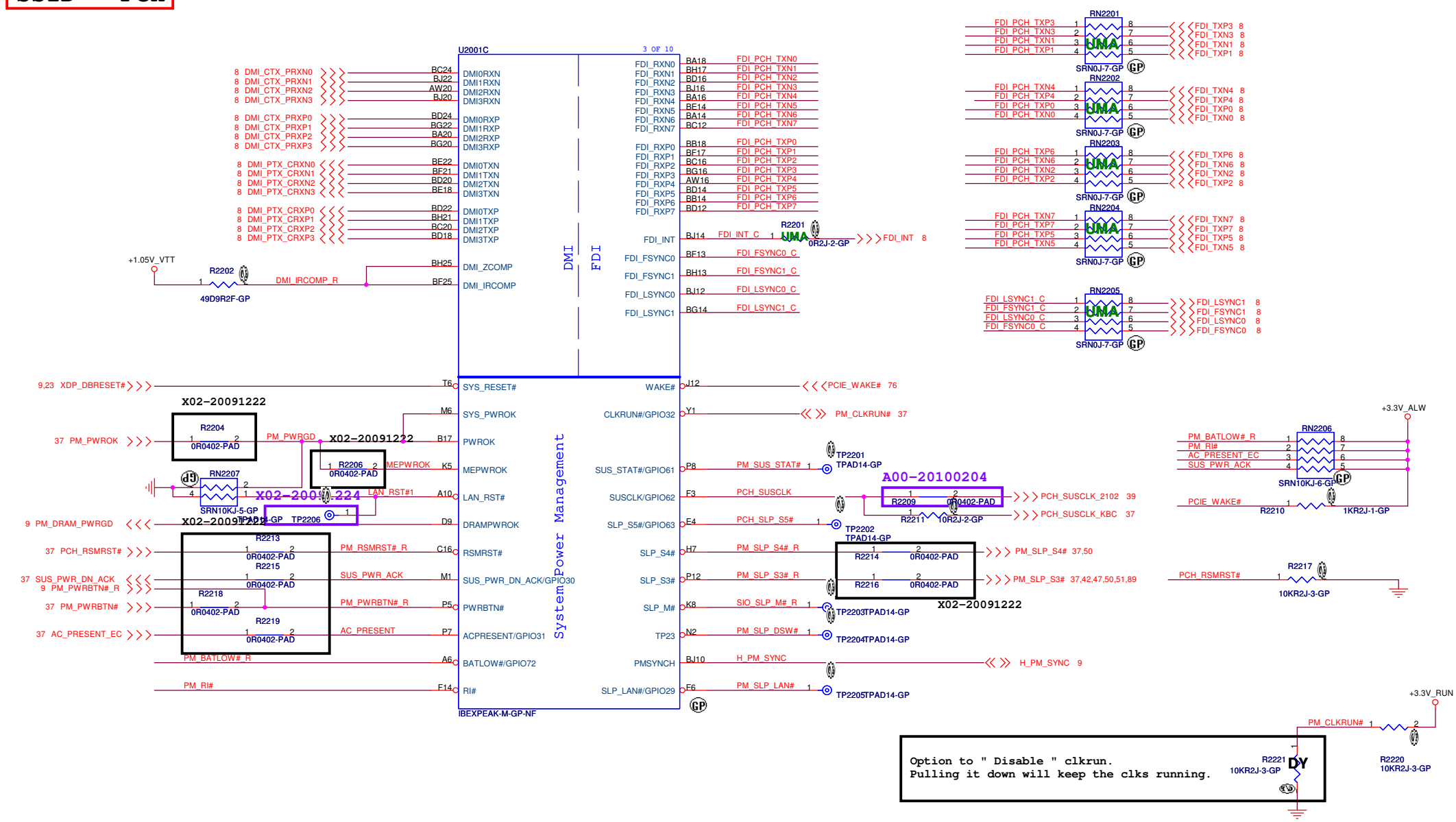
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size: | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 21 of 92

SSID = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 22 of 92

SSID = PCH

U2001B

2 OF 10

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

x01 change tolerant 20091117

x01 20091118

DIS uses 0ohm 63.R0034.1DL
UMA uses 12pF 78.12034.1FL

x01 2009/11/06

x01 2009/11/05

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

U2001A — 1 OF 10 — IBEXPEAK-M-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
HDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

X01 20091118 layout swap

RN2403 SRN33J-5-GP: 30 PCH_AZ_CODEC_SYNC, 30 PCH_SDOUT_CODEC → ACZ_SYNC_R, ACZ_SDATAOUT_R
RN2402 SRN33J-5-GP-U: 30 PCH_AZ_CODEC_RST#, 30 PCH_AZ_CODEC_BITCLK → ACZ_RST#_R, ACZ_BIT_CLK

x01 Change tolerant 20091117

SATA0RXN/RXP → SATA_RXN0_C, SATA_RXP0_C → C2409, C2410 (SCD01U16V2KX-3GP) → SATA_RXN0 59, SATA_RXP0 59 → SATA_TXN0, SATA_TXP0 59 — HDD
SATA1RXN/RXP → SATA_RXN1_C, SATA_RXP1_C → C2405, C2406 (SCD01U16V2KX-3GP) → SATA_RXN1 59, SATA_RXP1 59 → SATA_TXN1, SATA_TXP1 59 — ODD
SATA4RXN/RXP → SATA_RXN4_C, SATA_RXP4_C → C2407, C2408 (SCD01U16V2KX-3GP) → SATA_RXN4 76, SATA_RXP4 76 → SATA_TXN4, SATA_TXP4 76 — ESATA

NO REBOOT STRAP

+3.3V_RUN — R2410 DY 1KR2J-1-GP — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

For EMI

PCH_AZ_CODEC_BITCLK, PCH_AZ_CODEC_RST# → EC2402 SCD1U10V2KX-5GP DY, EC2401 DY SC22P50V2JN-4GP

x01 Change tolerant 20091117

X01

PCH_RTCX1 — R2402 10MR2J-L-GP — PCH_RTCX2
X2401 X-32D768KHZ-65-GP
C2403 SC15P50V2JN-2-GP, C2401 SC15P50V2JN-2-GP
82.30001.A41
X01 X01

+RTC_CELL — R2401 20KR2J-L2-GP — C2402 SC1U6D3V2KX-GP
+RTC_CELL — R2403 20KR2J-L2-GP — C2404 SC1U6D3V2KX-GP — G2401 GAP-OPEN
R2407 1M1R2J-GP, R2404 330KR2F-L-GP

PCH_RTCRST#, SRTCRST#, SM_INTRUDER#, PCH_INTVRMEN
ACZ_BIT_CLK, ACZ_SYNC_R, 30 ACZ_SPKR, ACZ_RST#_R, 30 PCH_SDIN_CODEC, ACZ_SDATAOUT_R, 37 ME_UNLOCK#

TPAD14-GP TP2404 PCH_JTAG_TCK, TP2405 PCH_JTAG_TMS, TP2406 PCH_JTAG_TDI, TP2407 PCH_JTAG_TDO, TP2408 PCH_JTAG_RST#

62 PCH_SPI_CLK → R2413 15R2J-GP → SPI_CLK_R
62 PCH_SPI_CS0# → R2414 15R2J-GP → SPI_CS0#_R
R2415 DY 0R2J-2-GP → SPI_CS1#
62 PCH_SPI_DO → R2416 15R2J-GP → SPI_MOSI_R
62 PCH_SPI_DI

LPC_LAD[0..3] — LPC_LAD[0..3] 37,70
FWH4/LFRAME# → LPC_LFRAME# 37,70
SERIRQ → INT_SERIRQ 23,37

SATAICOMPO, SATAICOMPI → SATAICOMP — R2412 37D4R2F-GP — +1.05V_VTT
SATALED# → SATA_LED# 66
SATA0GP/GPIO21 → SATA_DET#0_R
SATA1GP/GPIO19 → SATA_DET#1_R
+3.3V_RUN — RN2401 SRN10KJ-5-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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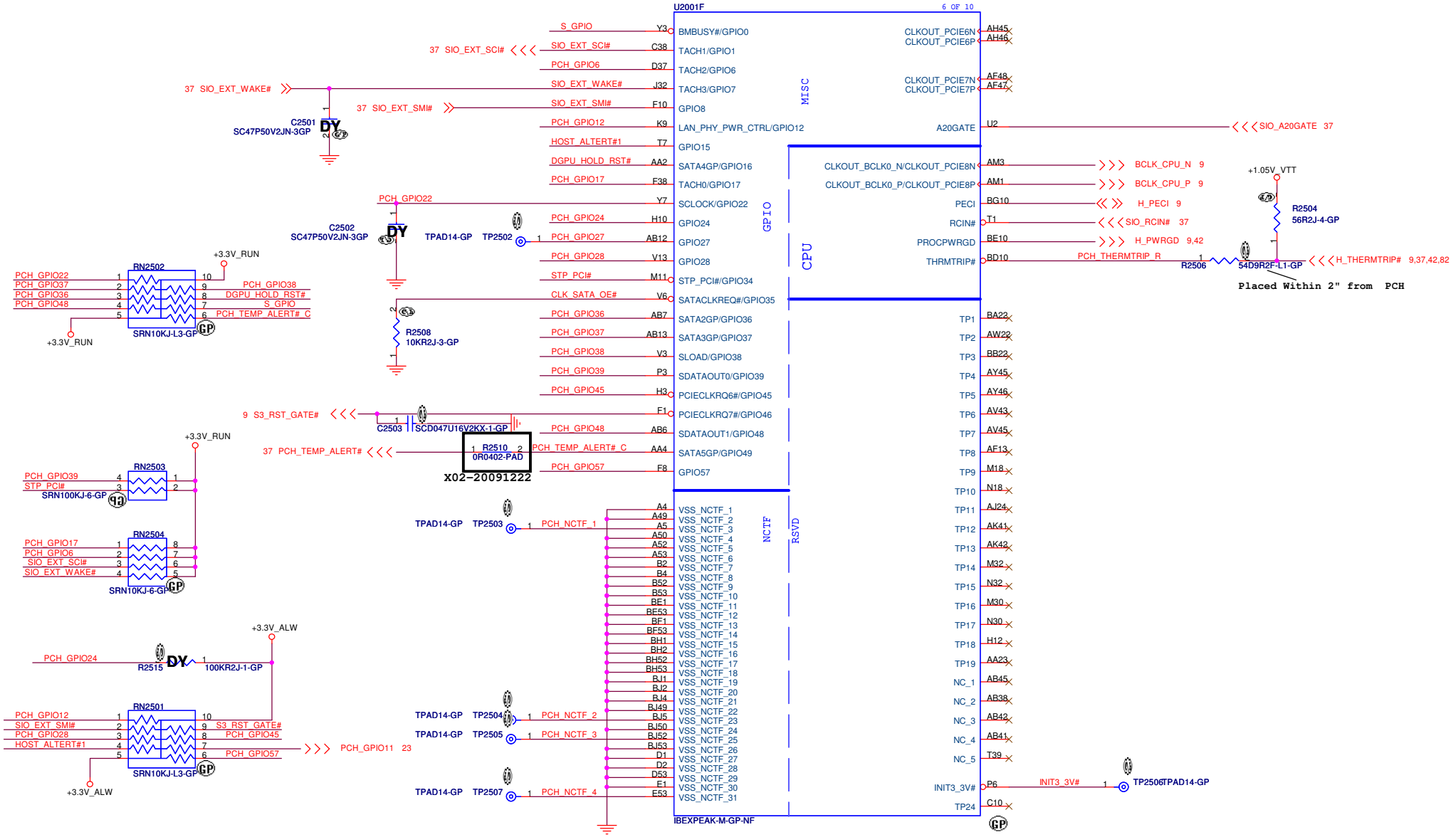
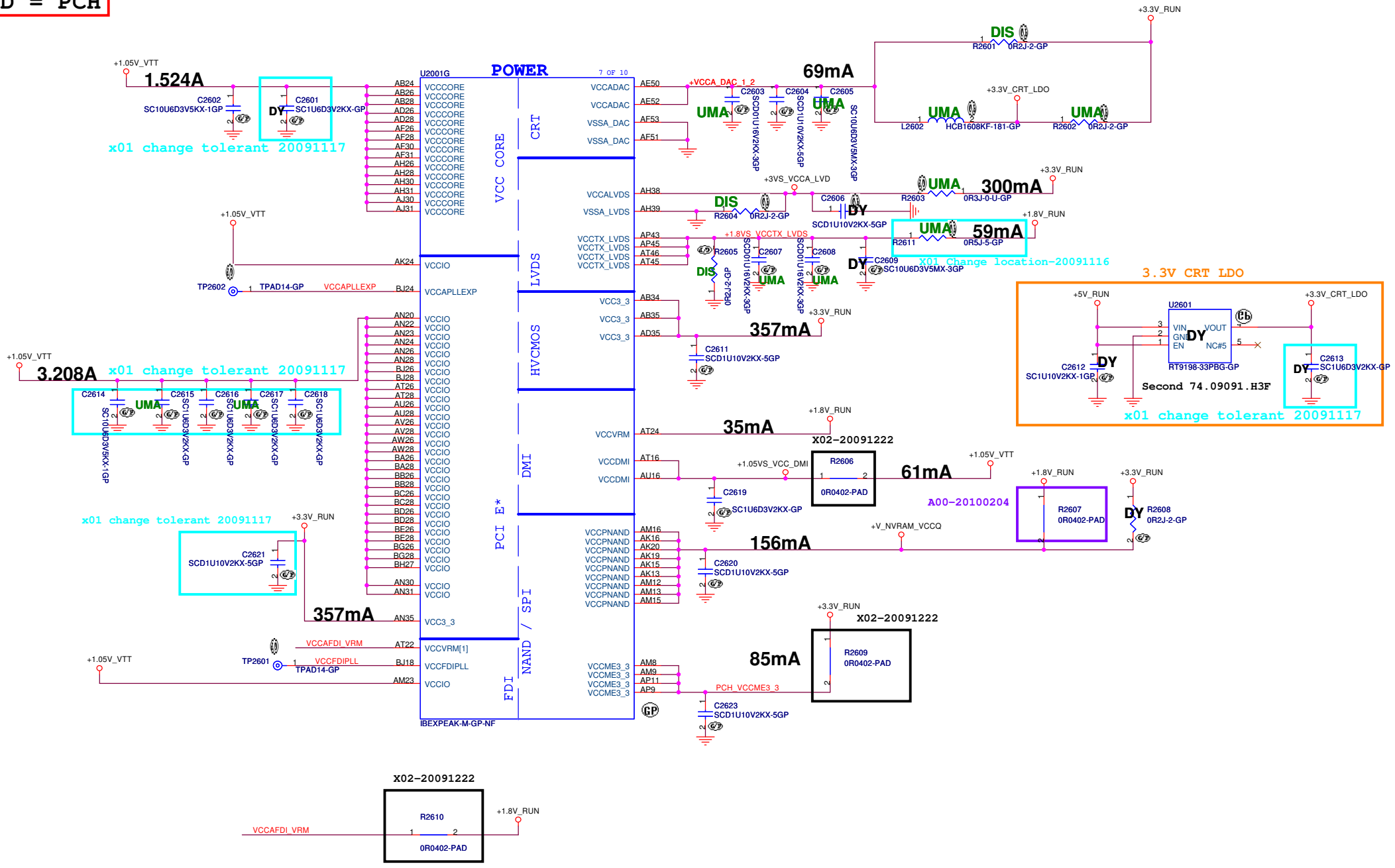
Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size | Document Number: Berry | Rev: A00
Date: Monday, March 29, 2010 | Sheet 24 of 92

SSID = PCH



SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER1)	
Size	Document Number: Berry	Rev: A00
Date: Wednesday, February 10, 2010	Sheet 26 of 92	

SSID = PCH

U2001J POWER 10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
AF23 VCCLAN
AF24 VCCLAN
Y20 DCPSUSBYP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
V9 DCPRTC
AU24 VCCVRM
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
V12 DCPSST
Y22 DCPSUS
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
AT18 V_CPU_IO
AU18 V_CPU_IO
A12 VCCRTC
IBEXPEAK-M-GP-NF

V24 VCCIO
V26 VCCIO
Y24 VCCIO
Y26 VCCIO
V28 VCCSUS3_3
U28 VCCSUS3_3
U26 VCCSUS3_3
U24 VCCSUS3_3
P28 VCCSUS3_3
P26 VCCSUS3_3
N28 VCCSUS3_3
N26 VCCSUS3_3
M28 VCCSUS3_3
M26 VCCSUS3_3
L28 VCCSUS3_3
L26 VCCSUS3_3
J28 VCCSUS3_3
J26 VCCSUS3_3
H28 VCCSUS3_3
H26 VCCSUS3_3
G28 VCCSUS3_3
G26 VCCSUS3_3
F28 VCCSUS3_3
F26 VCCSUS3_3
E28 VCCSUS3_3
E26 VCCSUS3_3
C28 VCCSUS3_3
C26 VCCSUS3_3
B27 VCCSUS3_3
A28 VCCSUS3_3
A26 VCCSUS3_3
U23 VCCSUS3_3
V23 VCCIO
F24 V5REF_SUS
K49 V5REF
J38 VCC3_3
L38 VCC3_3
M36 VCC3_3
N36 VCC3_3
P36 VCC3_3
U35 VCC3_3
AD13 VCC3_3
AK3 VCCSATAPLL
AK1 VCCSATAPLL
AH22 VCCIO
AT20 VCCVRM
AH19 VCCIO
AD20 VCCIO
AF22 VCCIO
AD19 VCCIO
AF20 VCCIO
AE19 VCCIO
AH20 VCCIO
AB19 VCCIO
AB20 VCCIO
AB22 VCCIO
AD22 VCCIO
AA34 VCCME
Y34 VCCME
Y35 VCCME
AA35 VCCME
L30 VCCSUSHDA

C2705 SC1U6D3V2KX-GP DY
C2706 SCD1U10V2KX-5GP
C2709 SCD1U10V2KX-5GP
C2713 SC1U10V2KX-1GP
C2715 SC1U10V2KX-1GP
C2718 SCD1U10V2KX-5GP
C2719 SCD1U10V2KX-5GP
C2727 SC1U6D3V2KX-GP
C2733 SC1U6D3V2KX-GP
R2703 0R0402-PAD
X02-20091222

D2701 CH751H-40PT-GP
D2702 CH751H-40PT-GP
R2702 10R2J-2-GP
R2701 10R2J-2-GP
TP2702 VCCSATAPLL TPAD14-GP

C2703 SCD1U10V2KX-5GP
C2704 SC10U6D3V5MX-GP DY
C2707 SC10U6D3V5KX-1GP
C2708 SC1U6D3V2KX-GP
C2710 SC1U6D3V2KX-GP DY
C2711 SC10U6D3V5MX-3GP DY
C2712 SC1U6D3V2KX-GP
C2714 SCD1U10V2KX-5GP
C2716 SC10U6D3V5MX-3GP DY
C2717 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
C2721 SC1U6D3V2KX-GP
C2722 SC1U6D3V2KX-GP
C2725 SCD1U10V2KX-5GP
C2726 SCD1U10V2KX-5GP
C2728 SCD1U10V2KX-5GP
C2729 SCD1U10V2KX-5GP
C2730 SC10U6D3V5KX-1GP
C2731 SCD1U10V2KX-5GP
C2732 SCD1U10V2KX-5GP
C2734 SCD1U10V2KX-5GP
C2735 SCD1U10V2KX-5GP

L2702 IND-10UH-218-GP
L2703 IND-10UH-218-GP

+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+1.8V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+1.05VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
VCCSATAPLL
+VCCSUSHDA
+RTC_CELL

x01 change tolerant 20091117
x01 20091121
x01 change tolerant 20091118

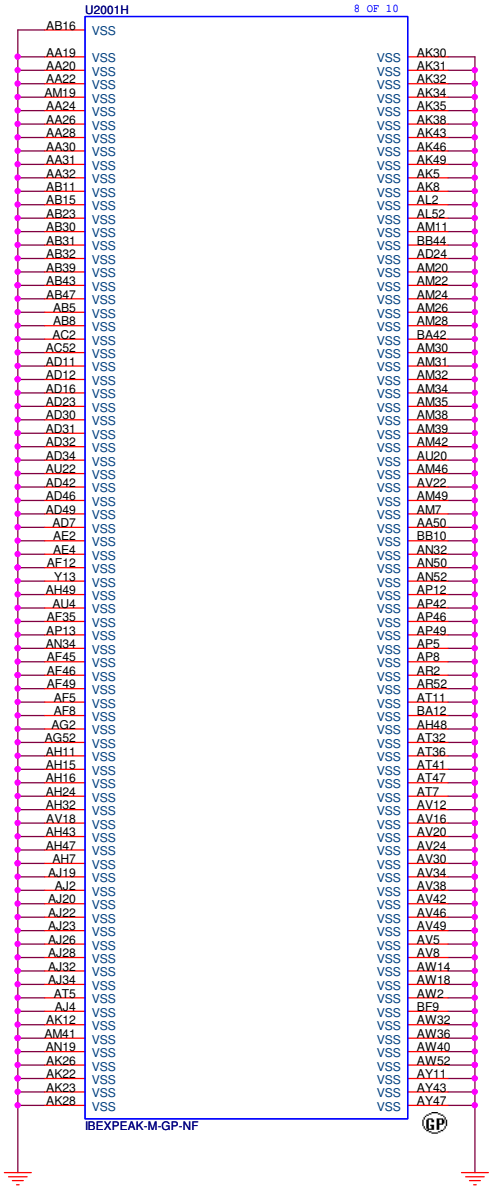
1.998A
72mA
73mA
163mA
1mA
2mA
6mA

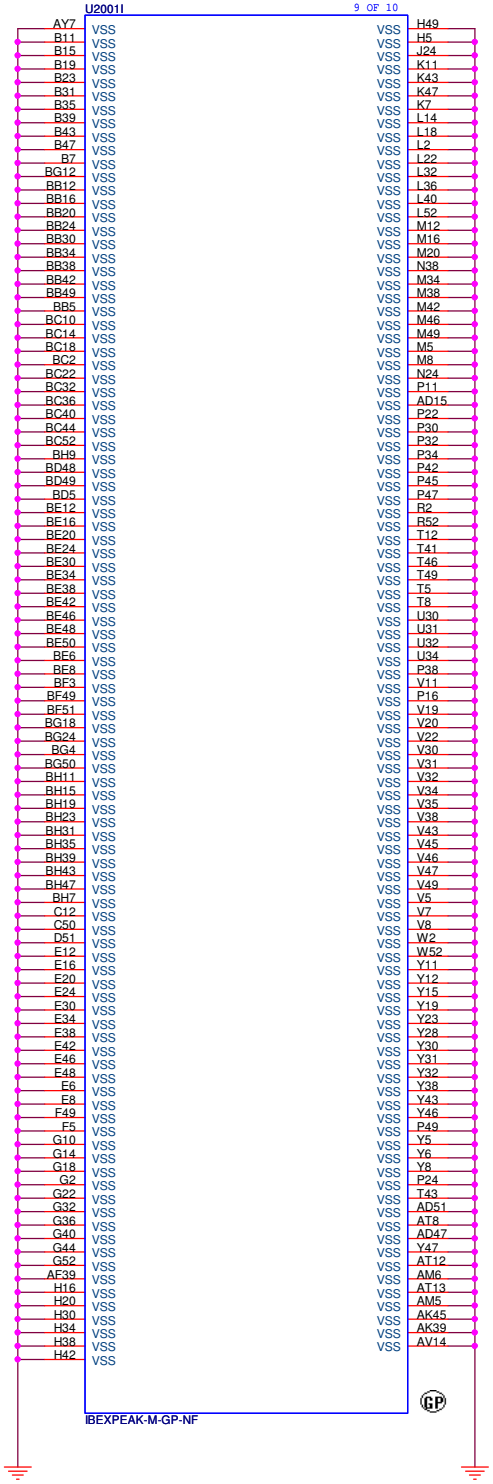
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size:
Document Number: Berry
Rev: A00
Date: Wednesday, February 10, 2010 Sheet 27 of 92

SSID = PCH





<Core Design>

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Title: PCH (VSS)

Size | Document Number: Berry | Rev: A00

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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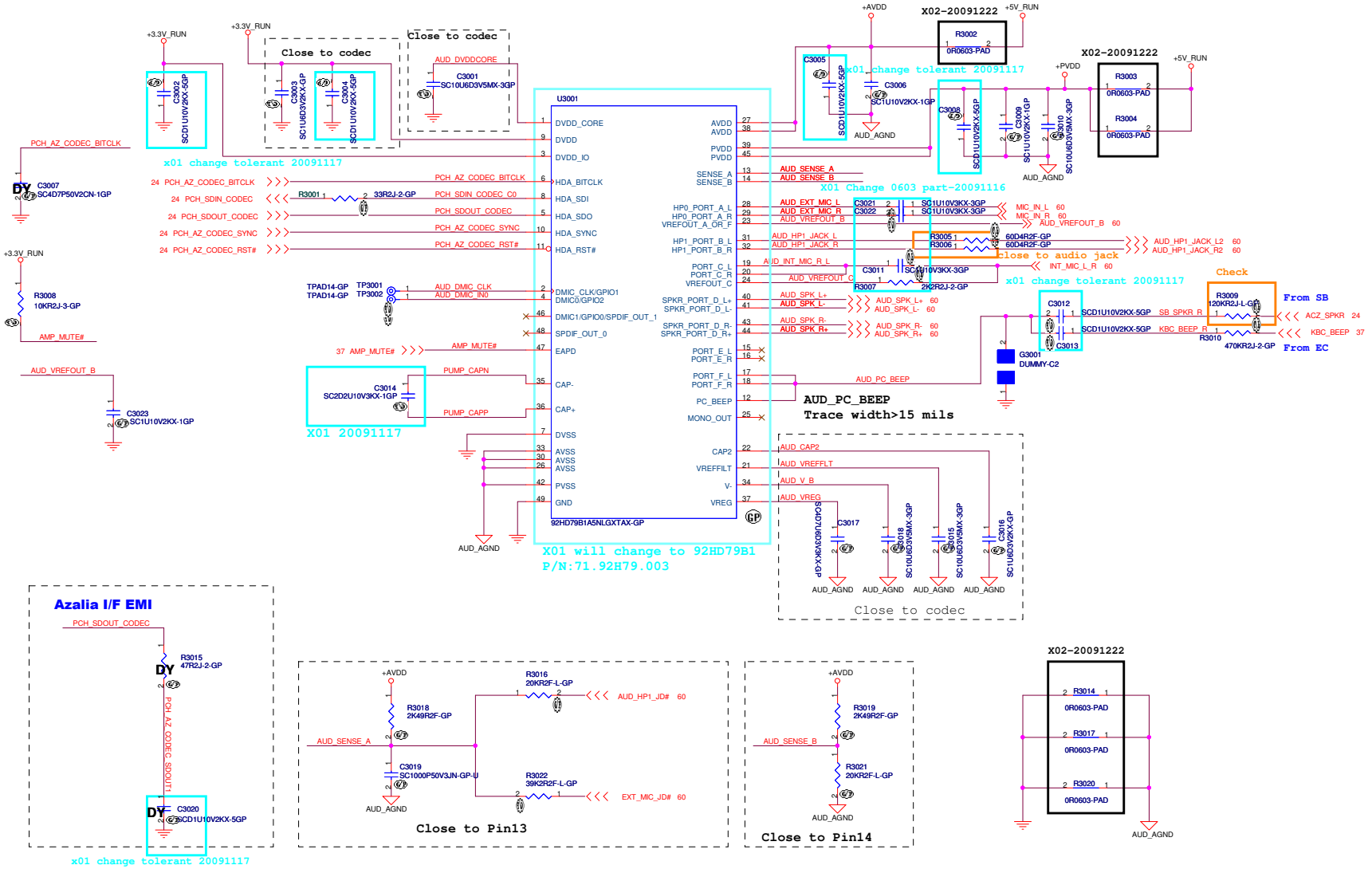
SSID = AUDIO



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD81B1

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 30 of 92

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*		
Size: A3	Document Number: *Berry*	Rev: *A00*
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<Core Design>

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Title: Reserved

Size: Custom | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 32 of 92

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 34 of 92

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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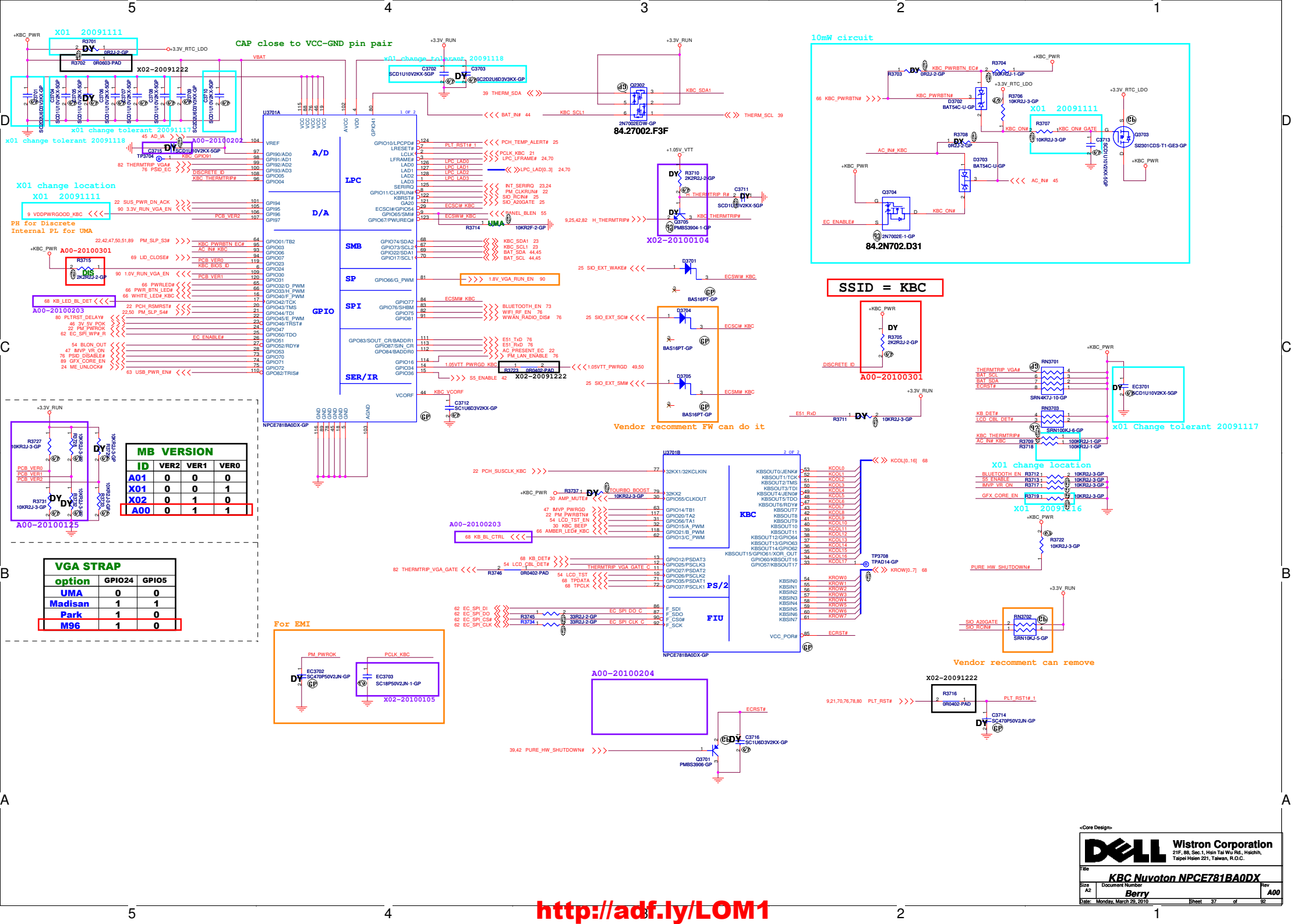
X01 20091111
CAP close to VCC-GND pin pair
X02-20091222
x01 change tolerant 20091118
x01 change tolerant 20091117
A00-20100202
X01 change location
X01 20091111
PH for Discrete
Internal PL for UMA
A00-20100301
A00-20100203
A00-20100125
MB VERSION
ID VER2 VER1 VER0
A01 0 0 0
X01 0 0 1
X02 0 1 0
A00 0 1 1
VGA STRAP
option GPIO24 GPIO5
UMA 0 0
Madisan 1 1
Park 1 0
M96 1 0
U3701A
NPCE781BA0DX-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
X02-20100104
84.27002.F3F
84.2N702.D31
10mW circuit
SSID = KBC
Vendor recommend FW can do it
Vendor recommend can remove
For EMI
A00-20100204
X02-20100105
U3701B
KBC
PS/2
FIU
x01 Change tolerant 20091117
X01 20091116
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
Berry
A00
Monday, March 29, 2010
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http://adf.ly/LOM1

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<Core Design>

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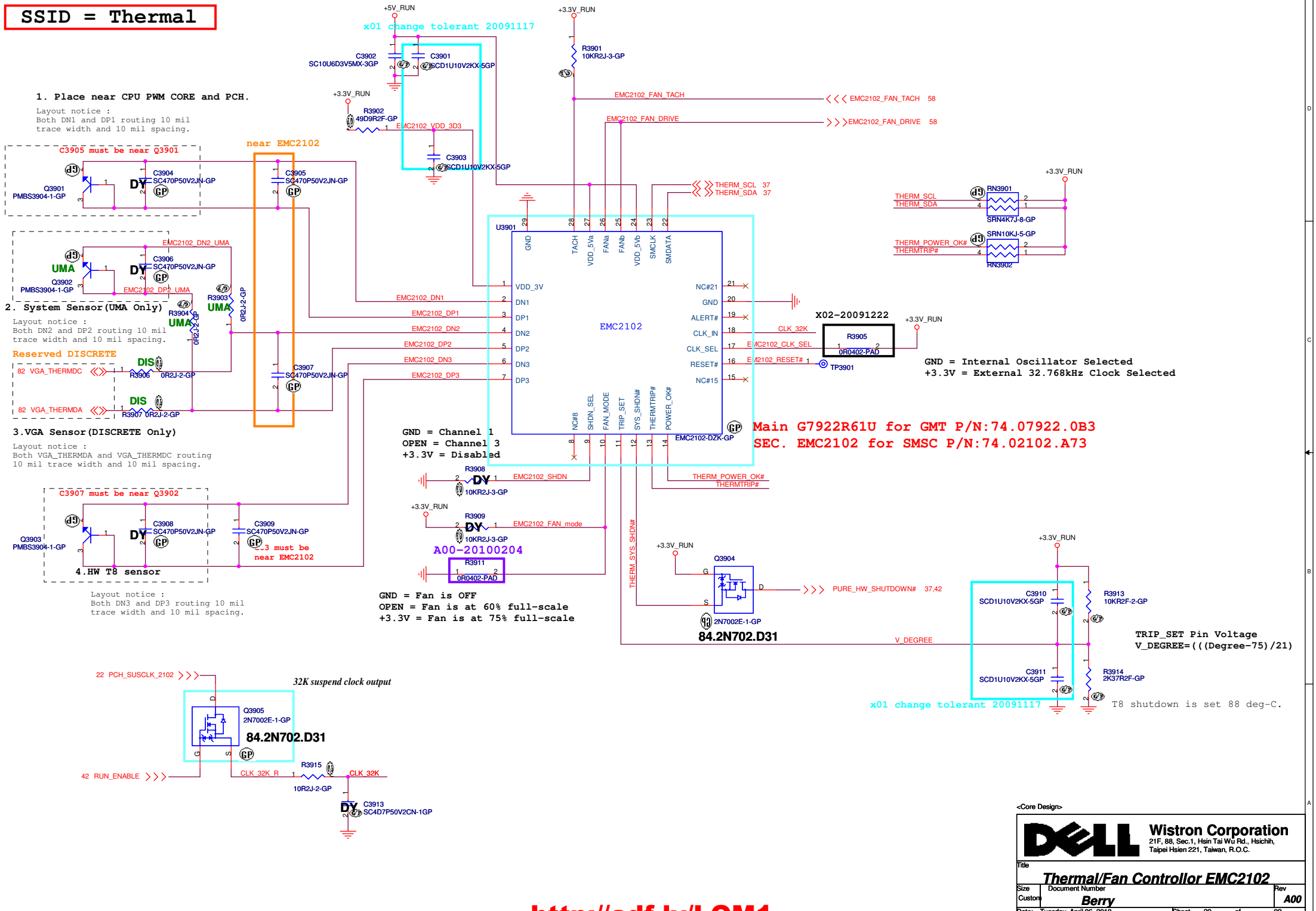
Title

Reserved

Size	Document Number	Rev
A4	***Berry***	***A00***

Date: Wednesday, February 10, 2010 Sheet 38 of 92

SSID = Thermal



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size	Document Number	Rev
Custom	Berry	A00

Date: Tuesday, April 06, 2010 Sheet 39 of 92

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 40 of 92

(Blanking)

<Core Design>

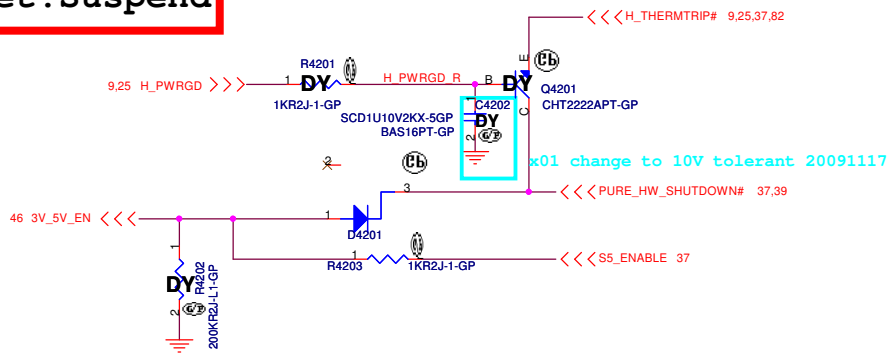
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

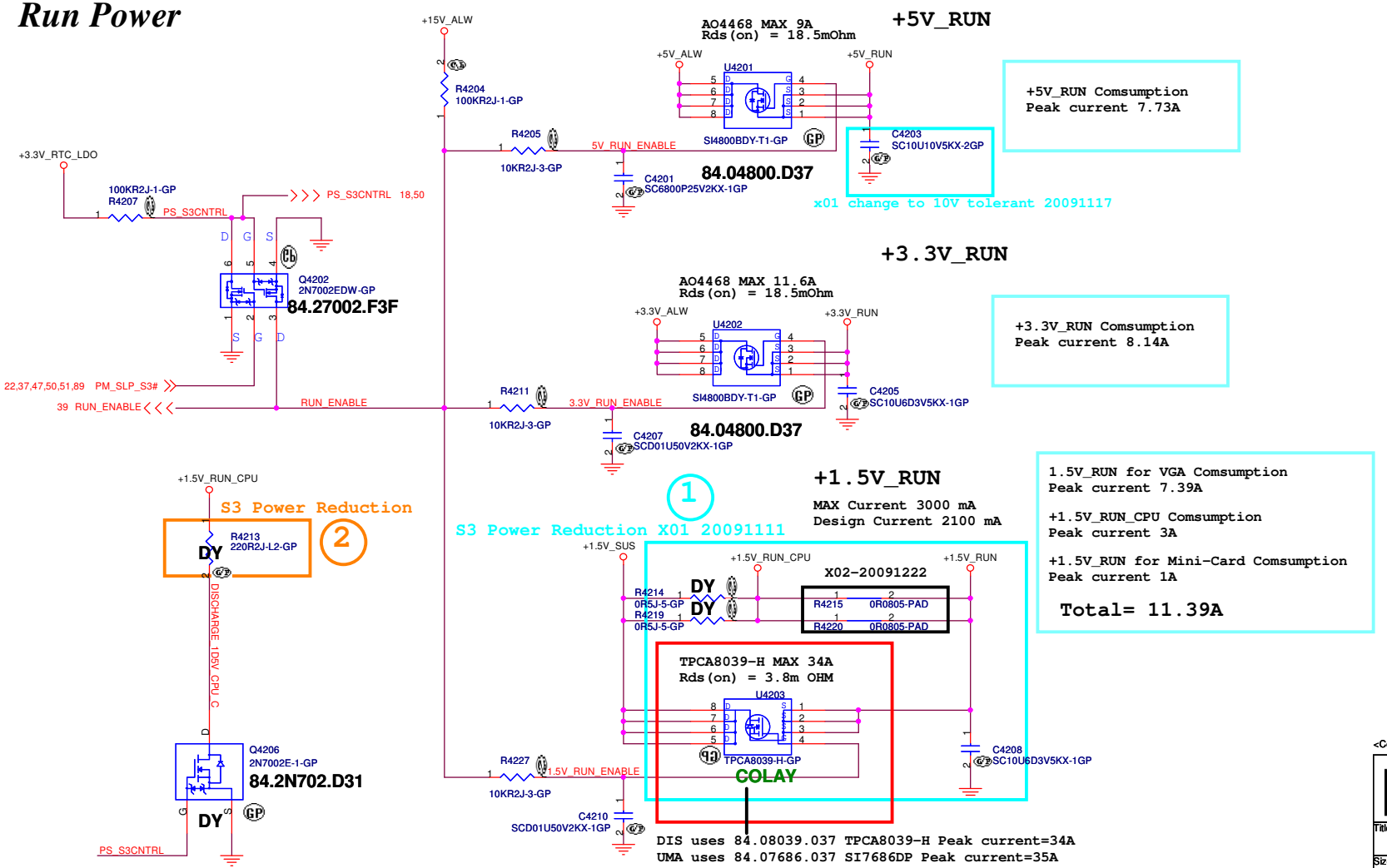
Size: A3 | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 41 of 92

SSID = Reset.Suspend



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

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A3	Berry	A00

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<Core Design>

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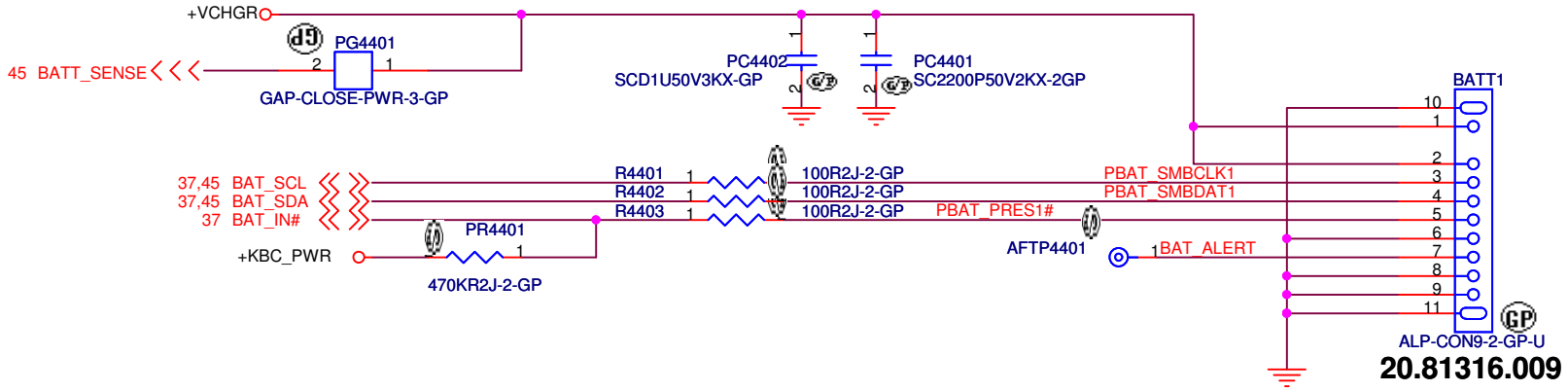
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

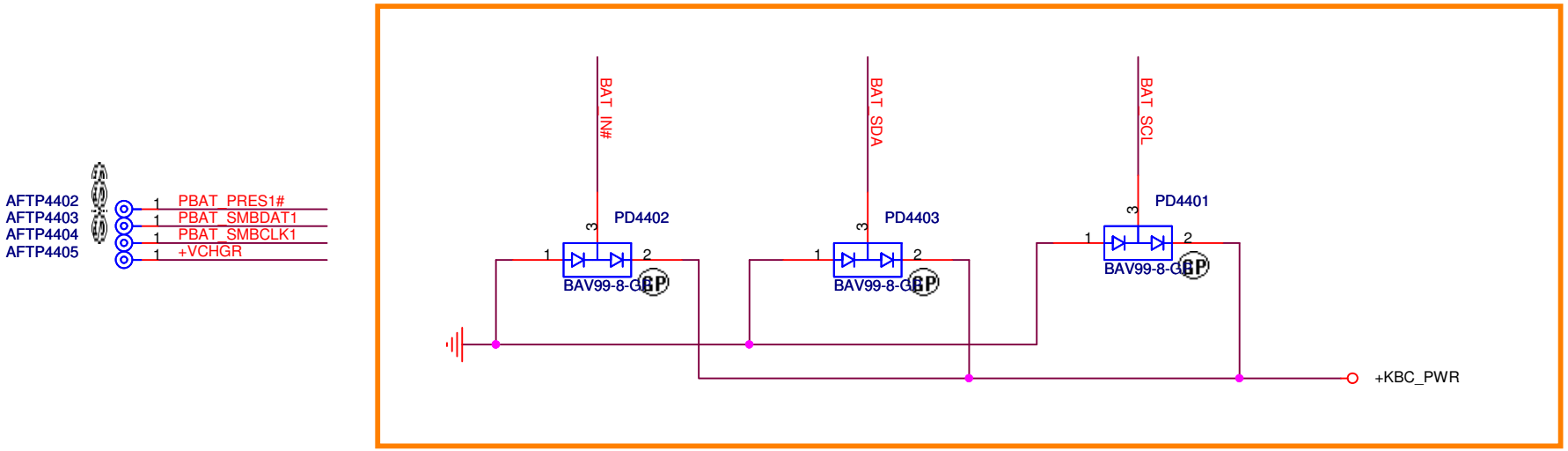
Date: Wednesday, February 10, 2010 | Sheet 43 of 92

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

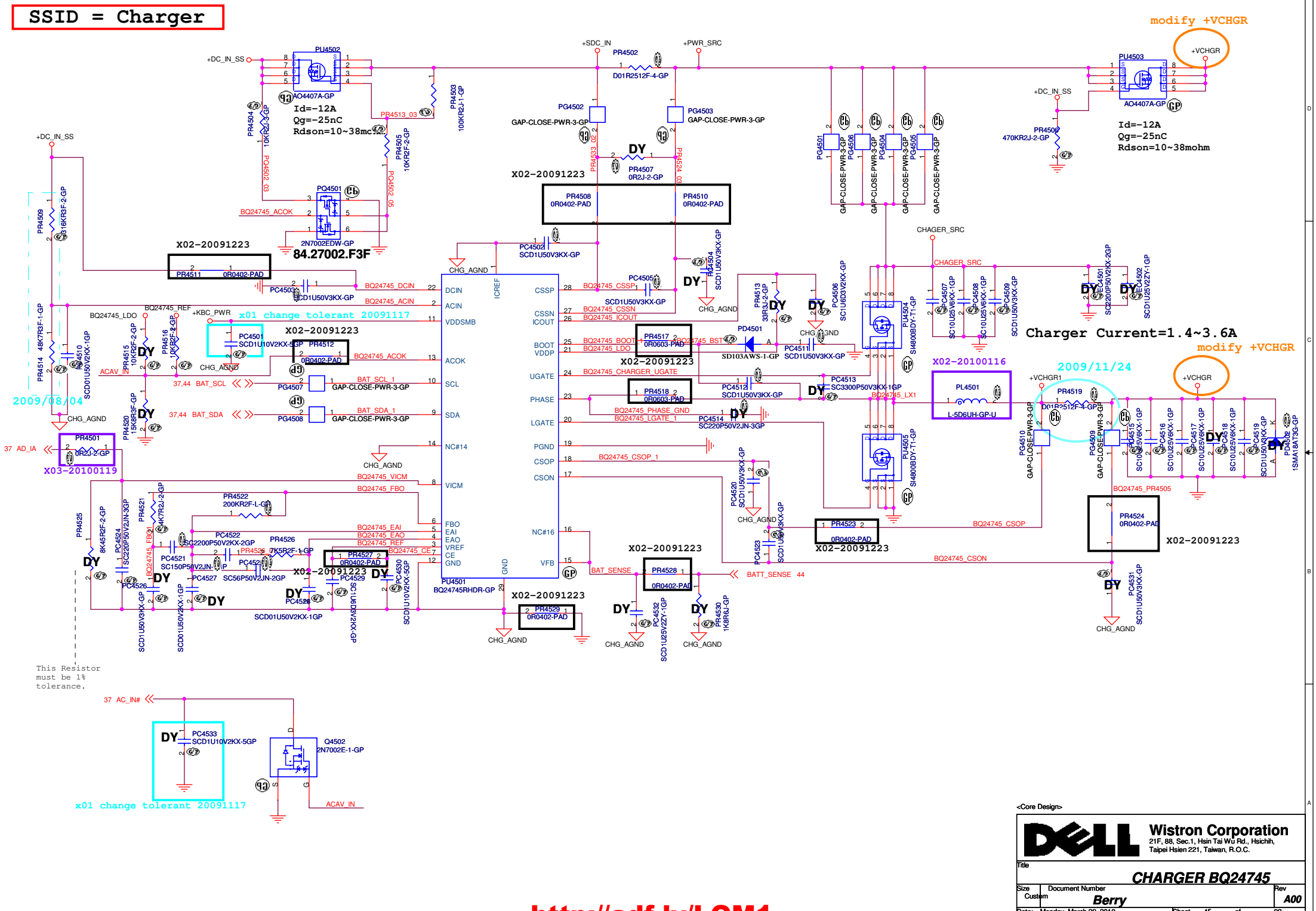
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

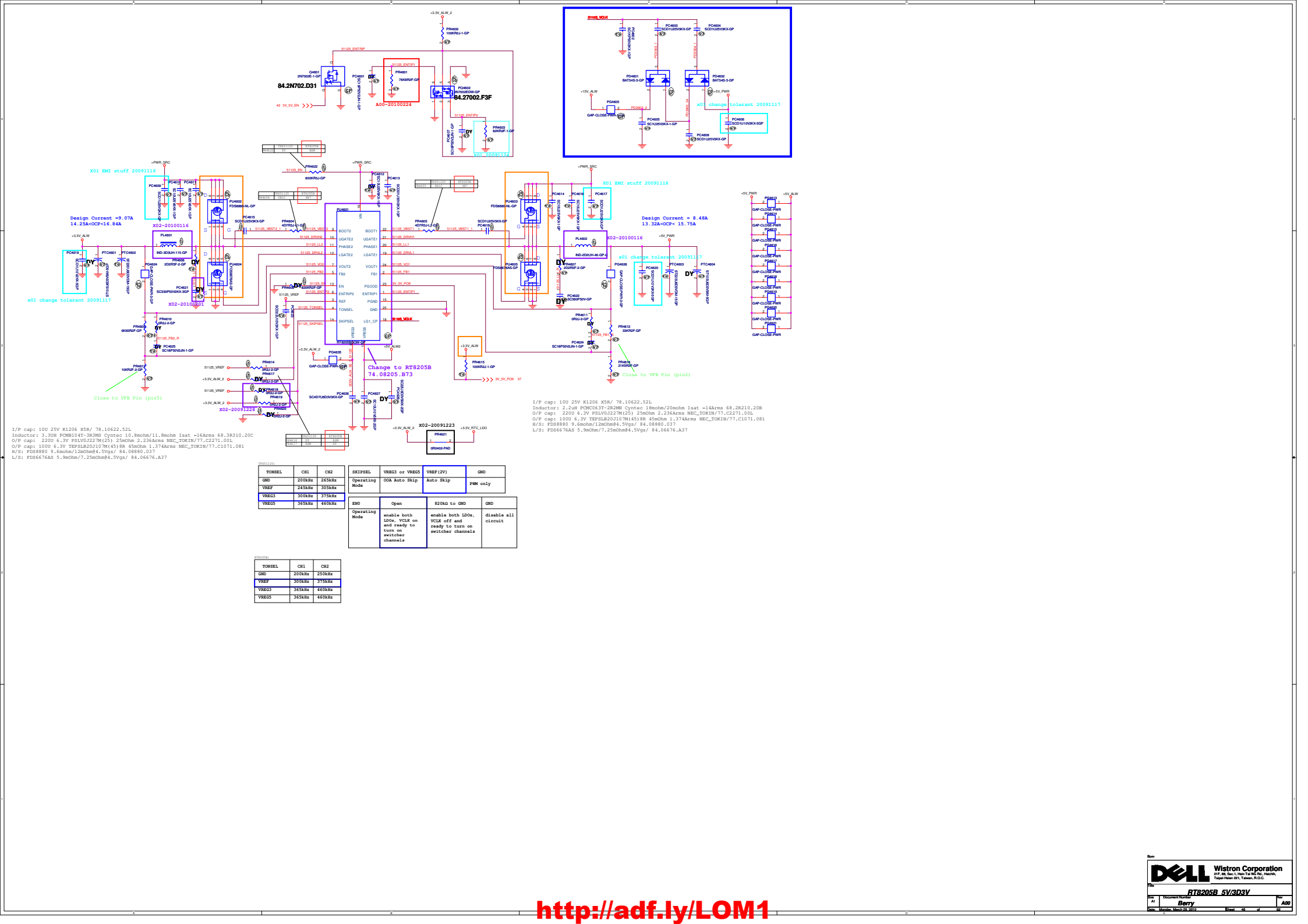
Title: **BATT CONN**

Size	Document Number	Rev
A4	Berry	A00

Date: Monday, March 29, 2010 Sheet 44 of 92

SSID = Charger





TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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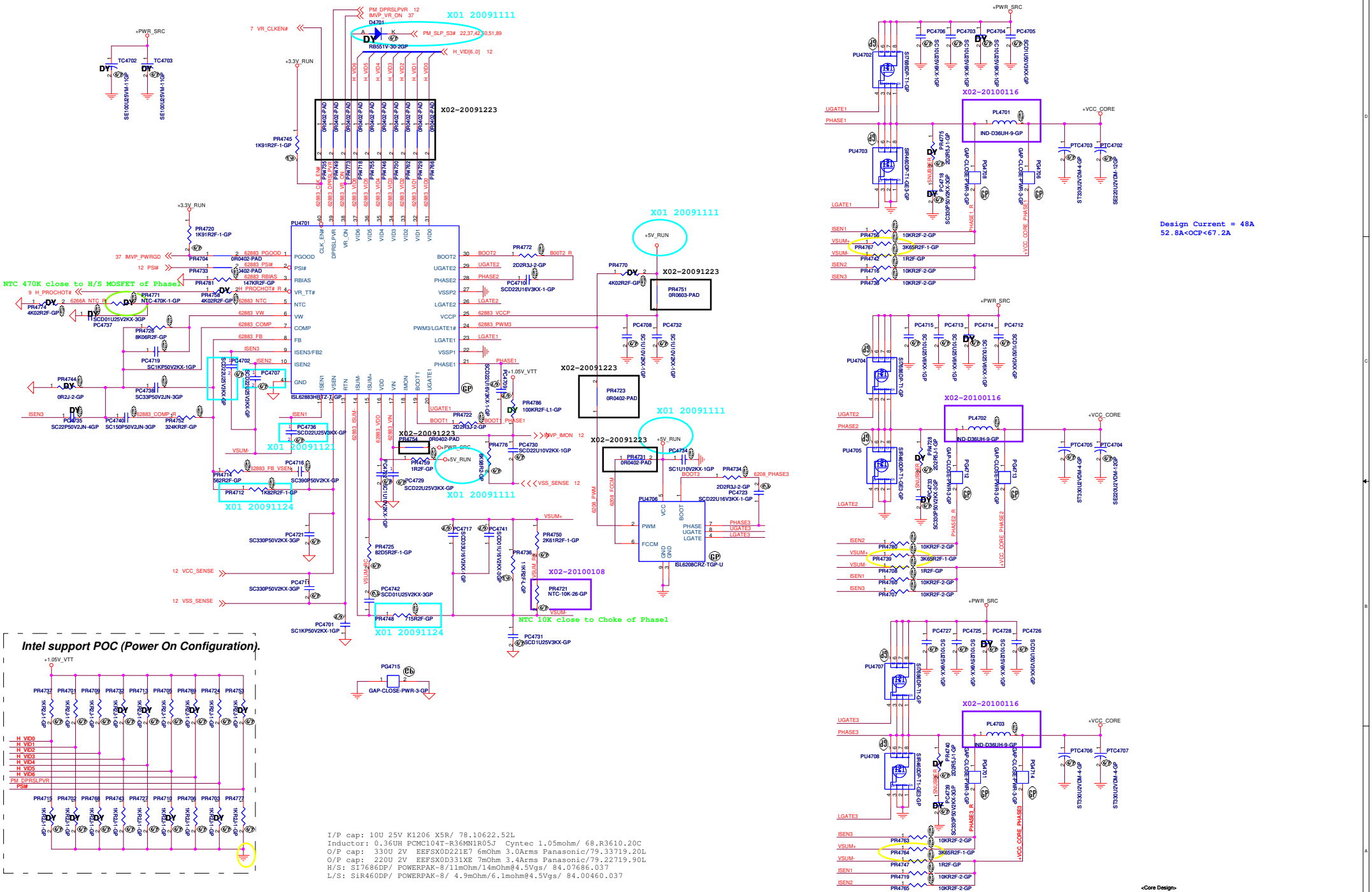
File: RT8205B_5V/3D3V

Size	Document Number	Rev
A1	Berry	A00

Date: Monday, March 29, 2010 Sheet 46 of 50



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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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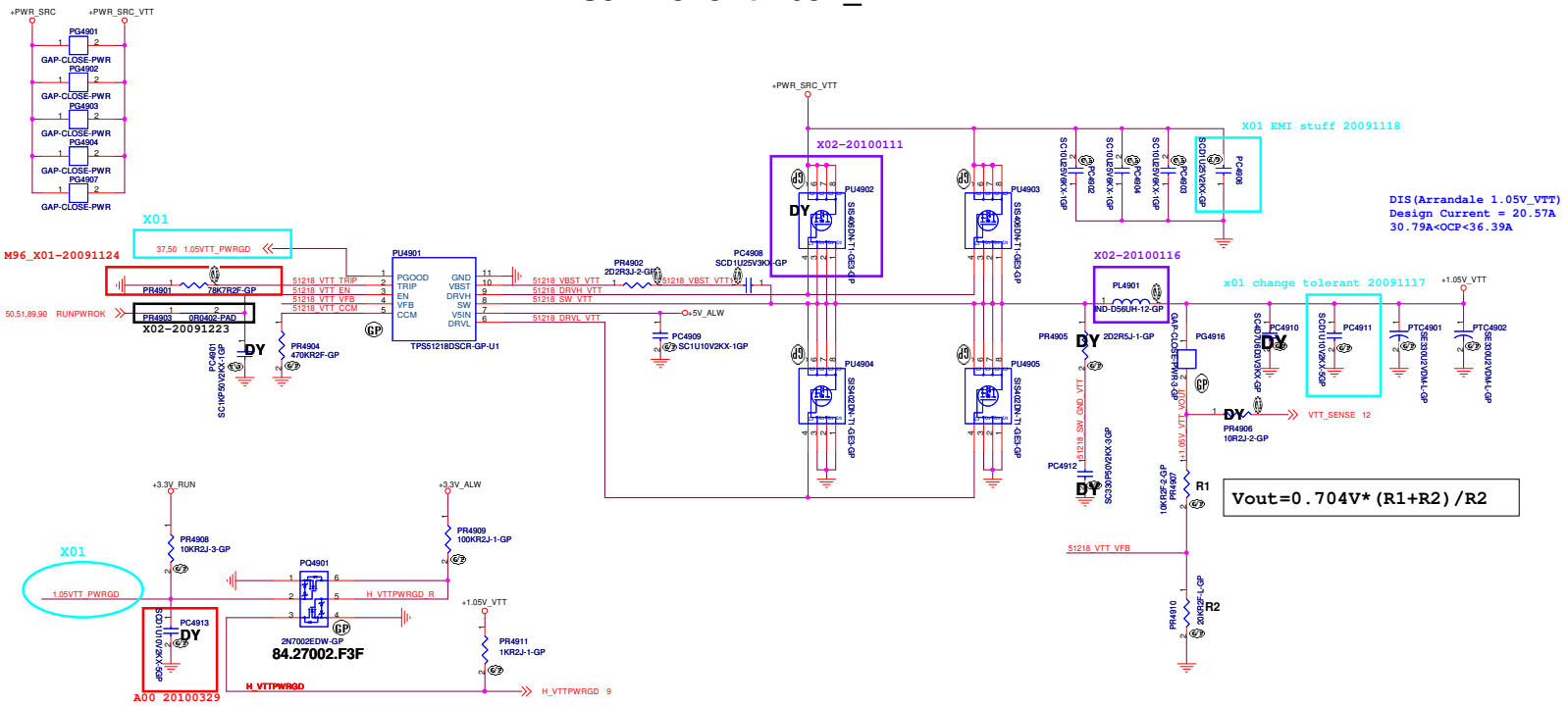
TPS51218 for +1.05V_VTT



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

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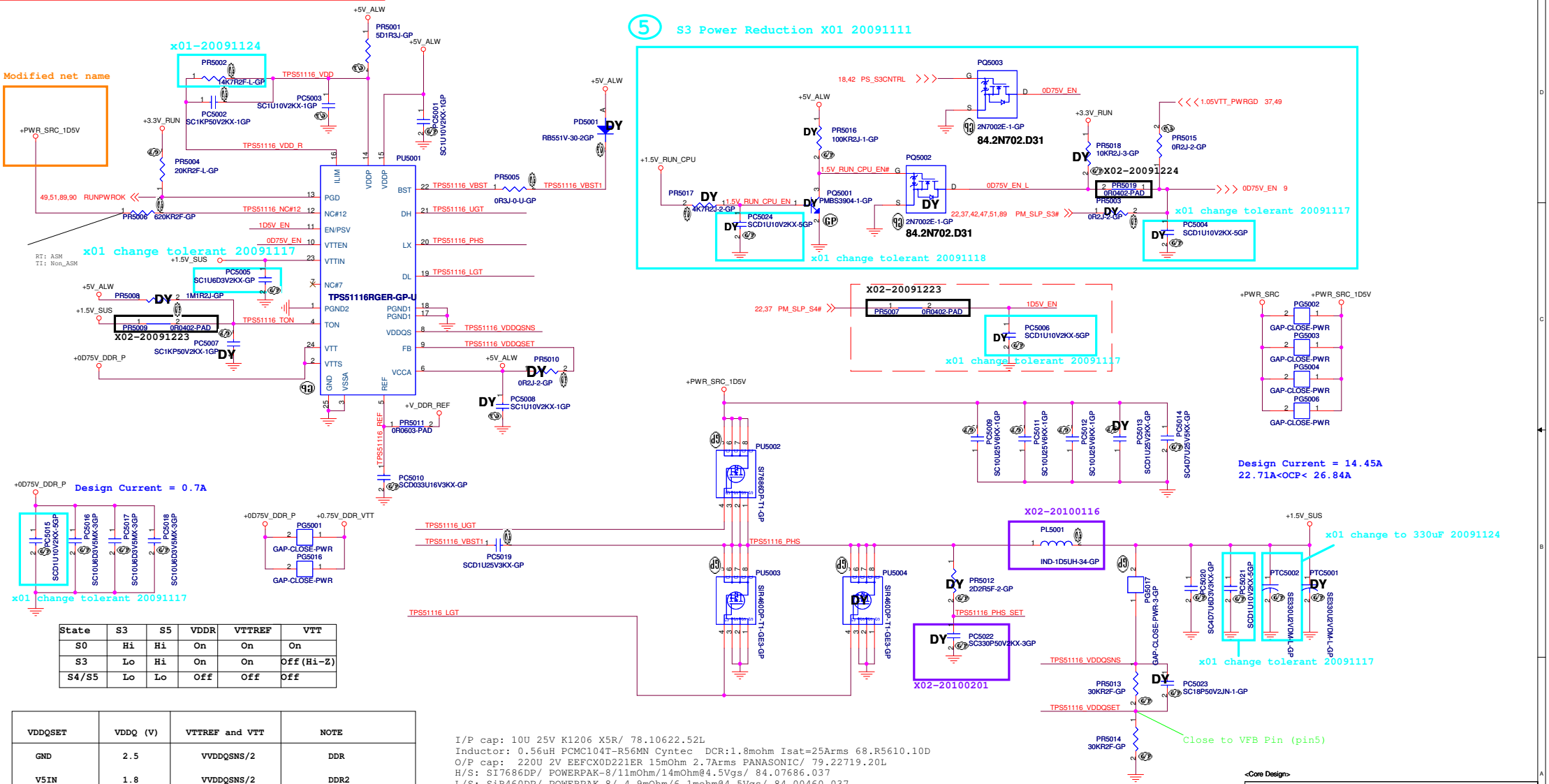
Title: TPS51218 +1.05V VTT

Size	Document Number	Rev
A2	Berry	A00

Date: Tuesday, April 06, 2010 Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

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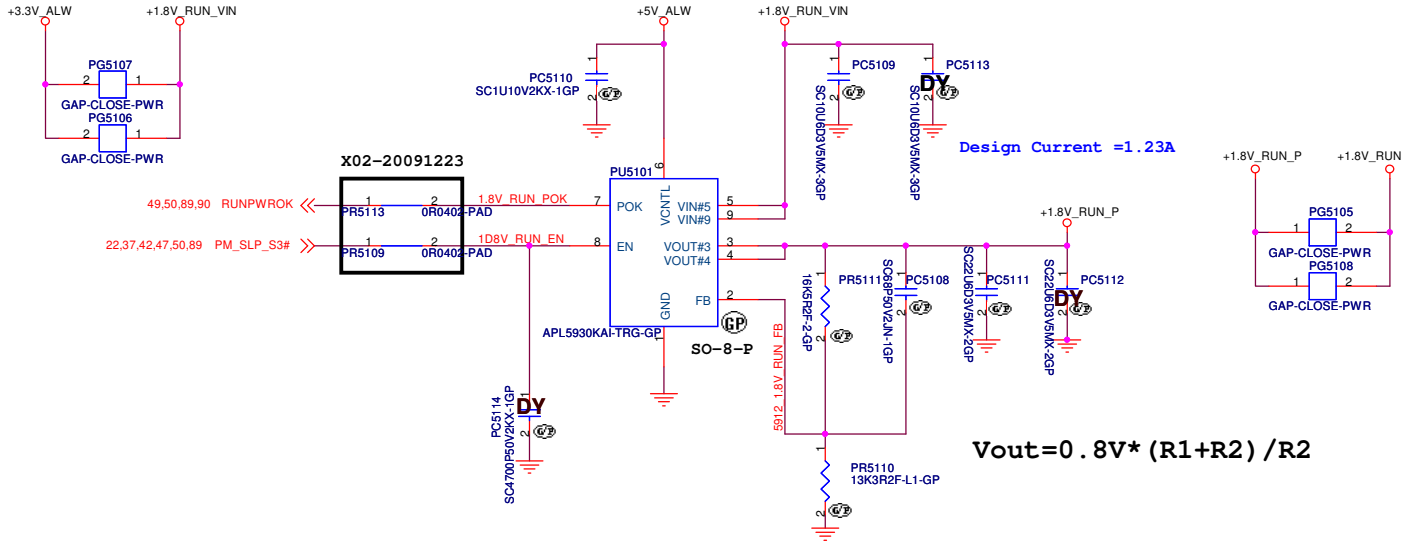
Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	Berry	A00

Date: Monday, March 29, 2010 Sheet 50 of 92

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

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Title: APL5930 +1.8V RUN

Size: A3 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 51 of 92

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

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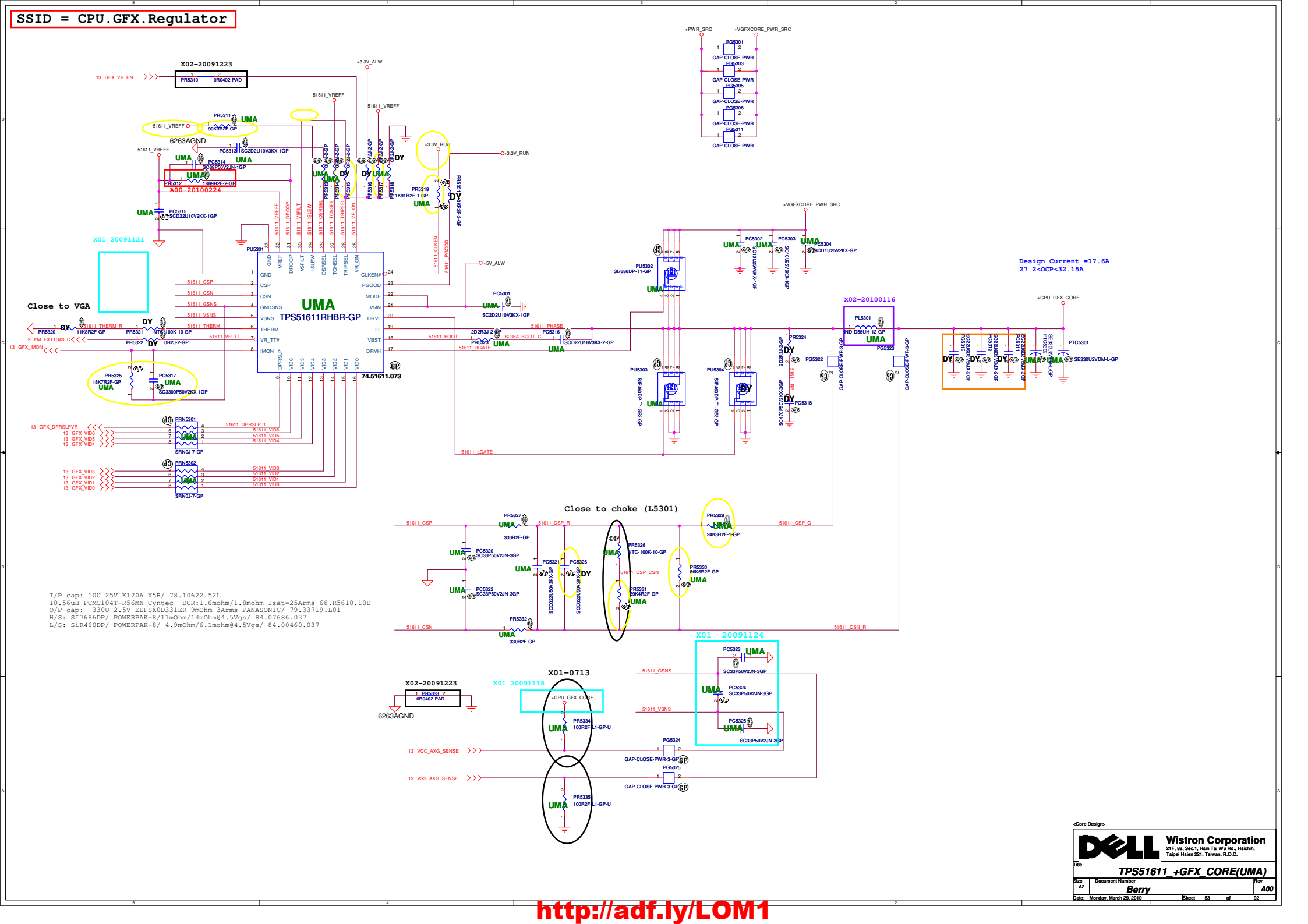
SSID = CPU.GFX.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
I0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

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Title: TPS51611_+GFX_CORE(UMA)

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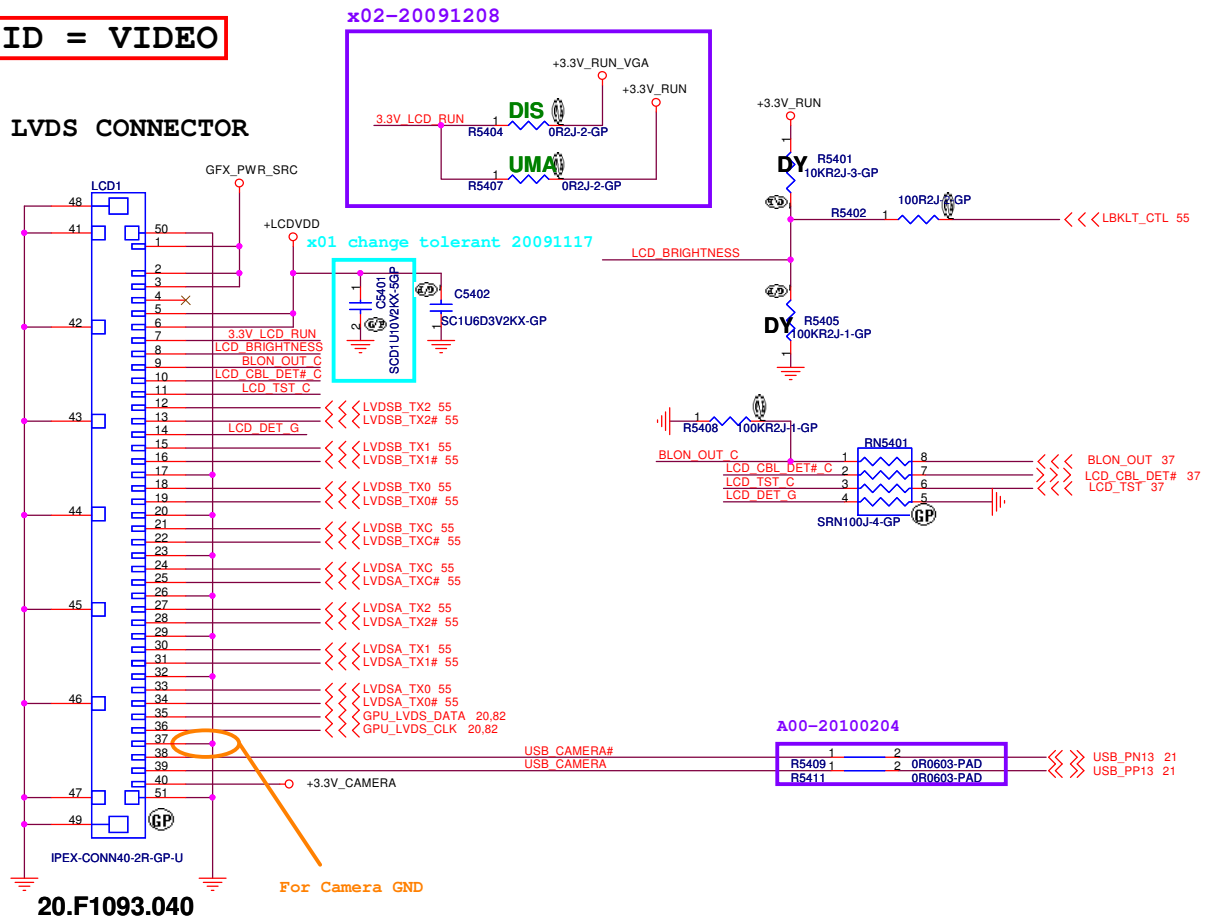
Date: Monday, March 29, 2010 Sheet 53 of 92

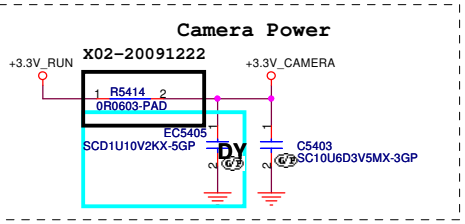
SSID = VIDEO

LVDS CONNECTOR



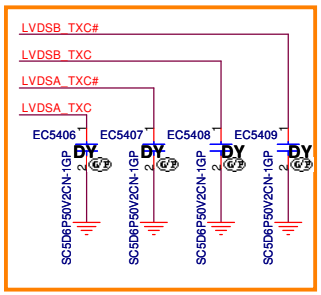
20.F1093.040

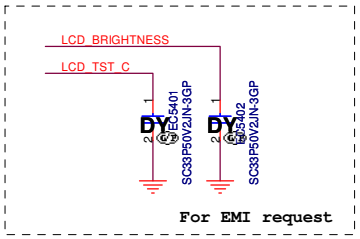
Camera Power



x01 change tolerant 20091117

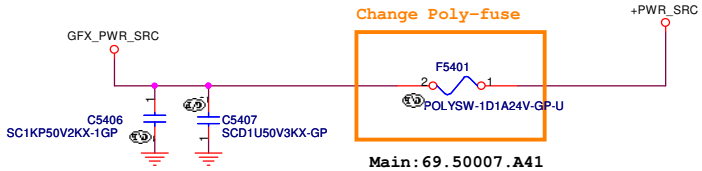
Close to LVDS connector





SSID = Inverter

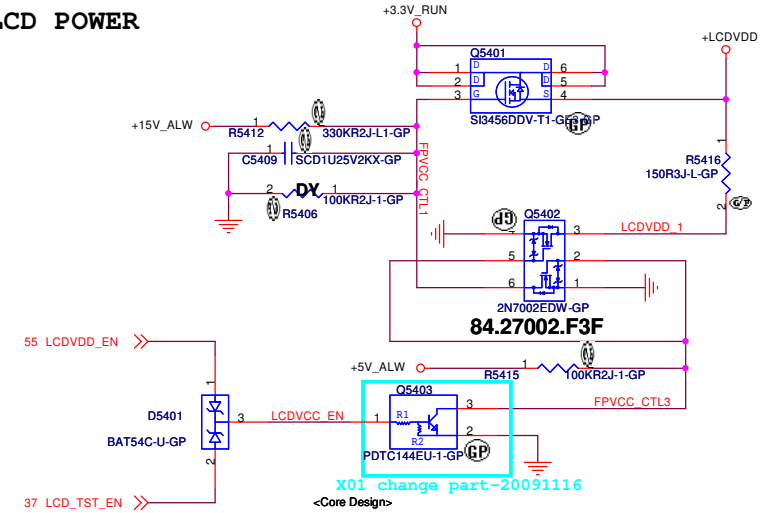
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



<Core Design>

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Title		
LCD/Inverter Connector		
Size: A3	Document Number: Berry	Rev: A00
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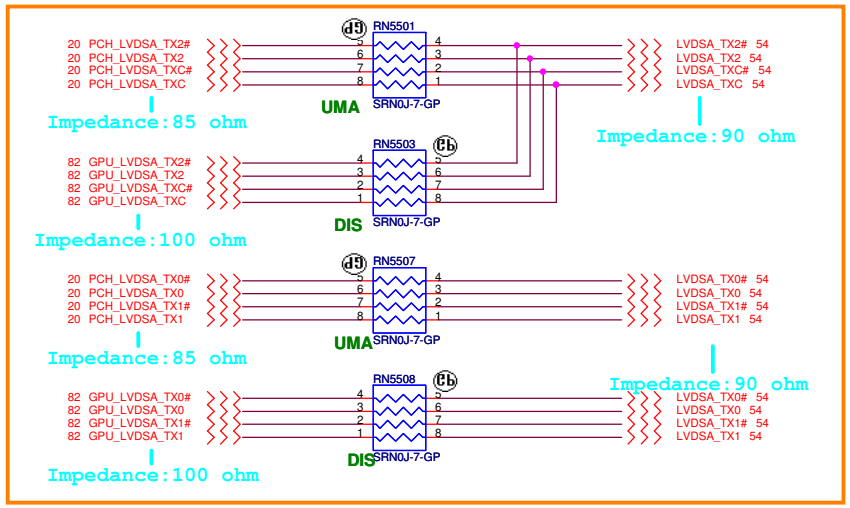
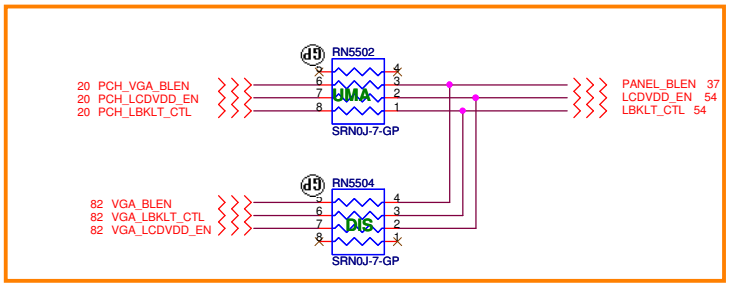
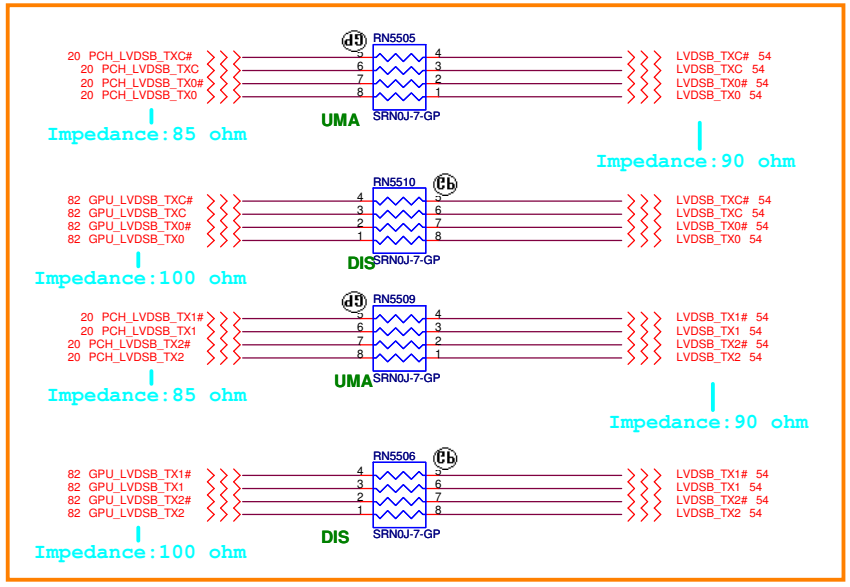
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

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Title: LVDS Switch

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 55 of 92

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<Core Design>

Wistron Corporation
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Title	LVDS_Switch	
Size: A3	Document Number: Berry	Rev: A00
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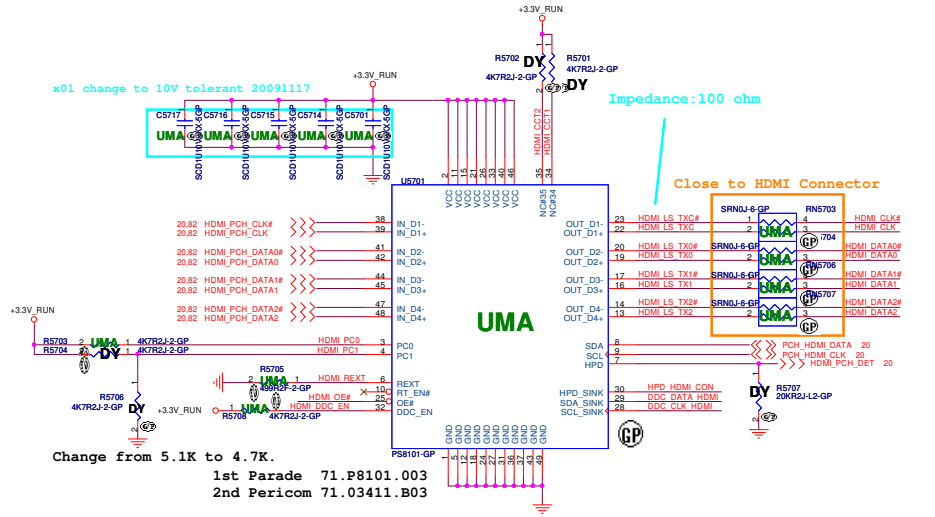
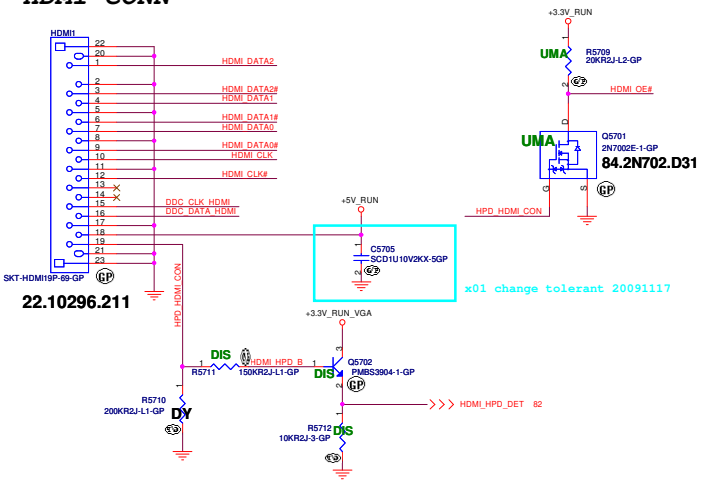
SSID = VIDEO

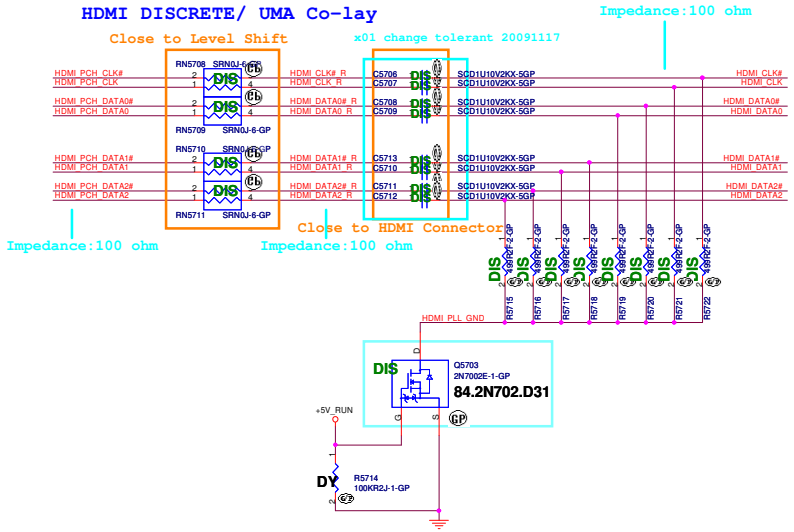
HDMI Level Shifter & CONNECTOR

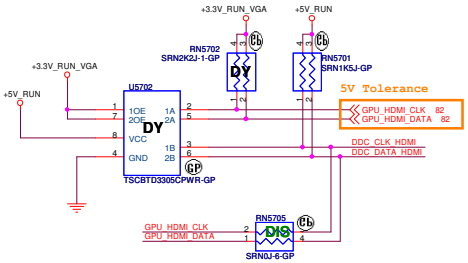


HDMI CONN



HDMI DISCRETE/ UMA Co-lay

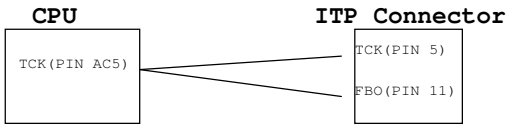




SSID = User.Interface

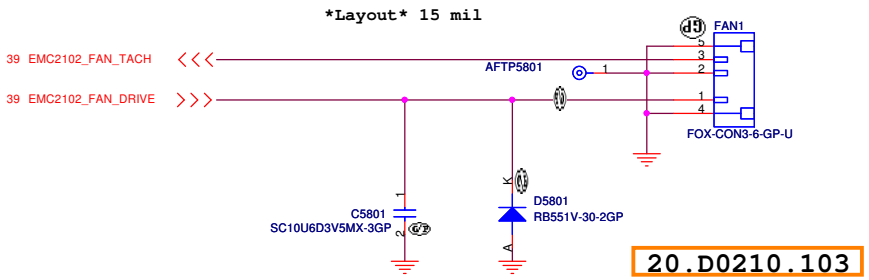
ITP Connector

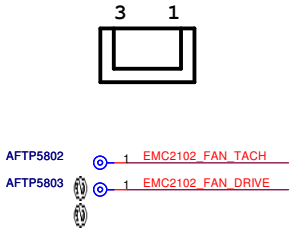
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





<Core Design>

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Title: ITP/Fan Connector

Size: A3 | Document Number: Berry | Rev: A00

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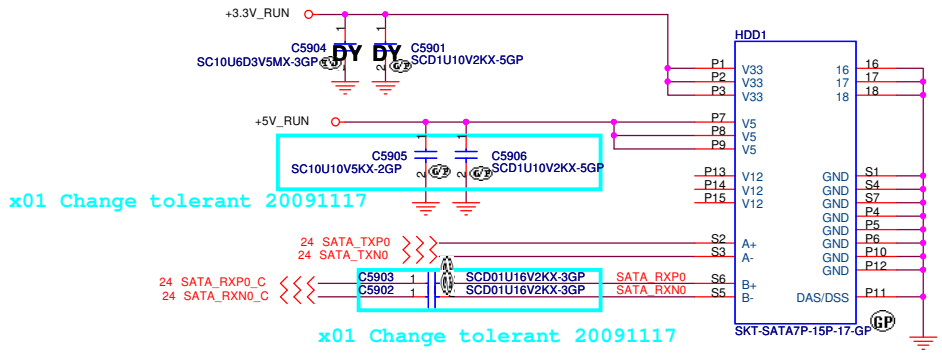
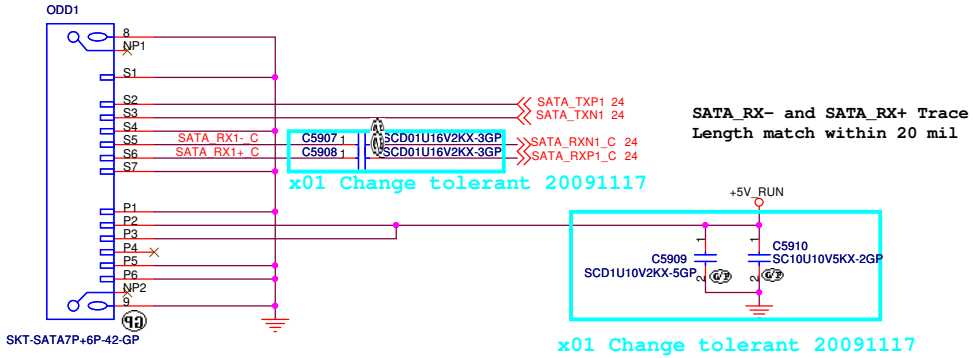
SSID = SATA

SATA HDD Connector



62.10065.C71

ODD Connector



62.10065.581

<Core Design>

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Title: HDD/ODD

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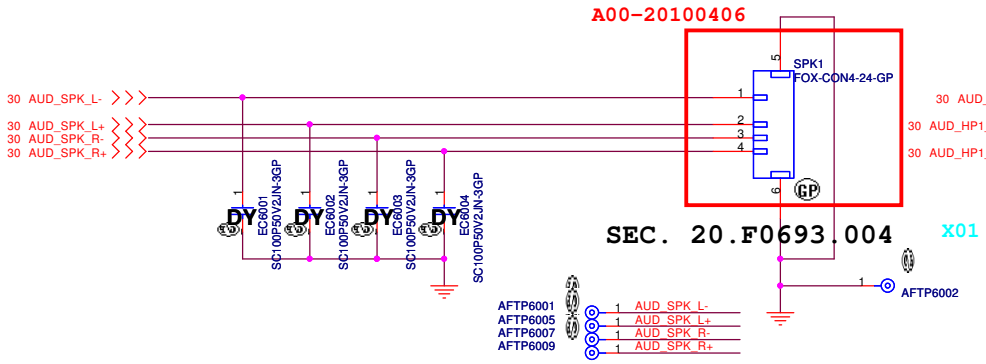
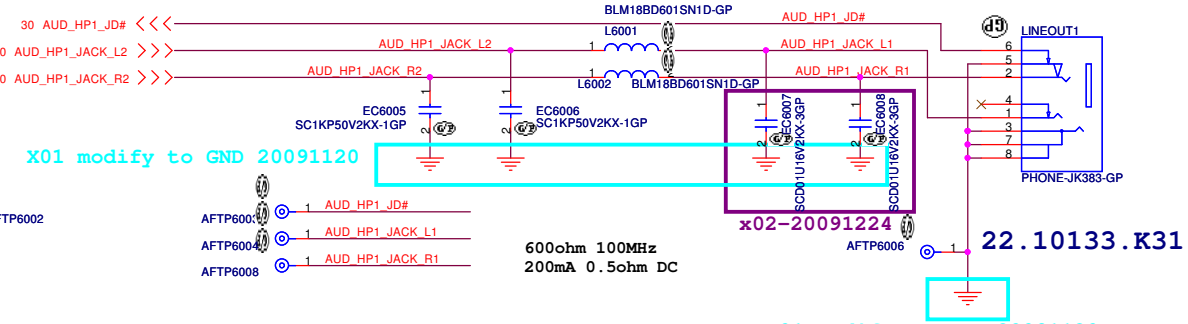
SSID = AUDIO

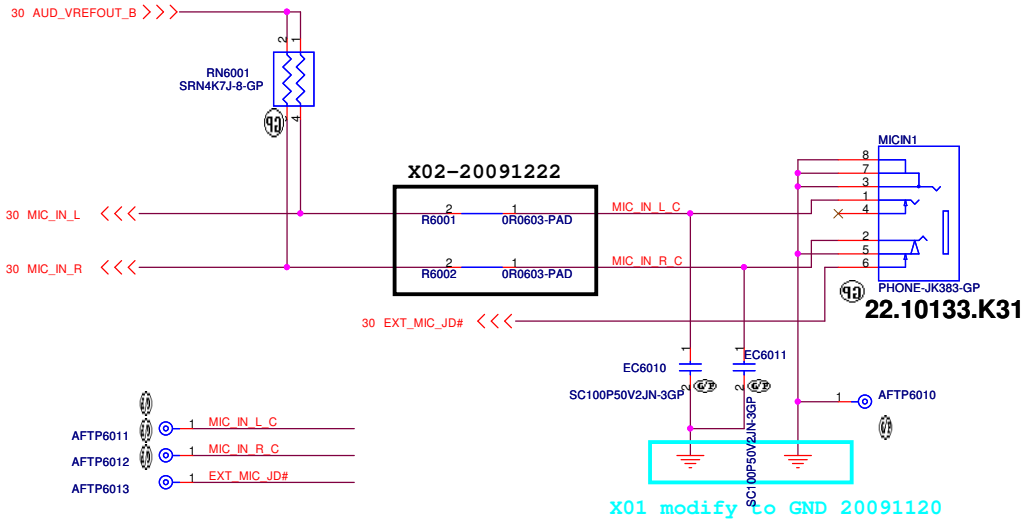
Speaker Connector



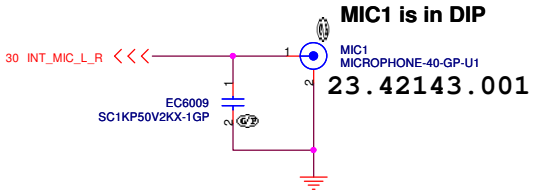
LINE1 OUT

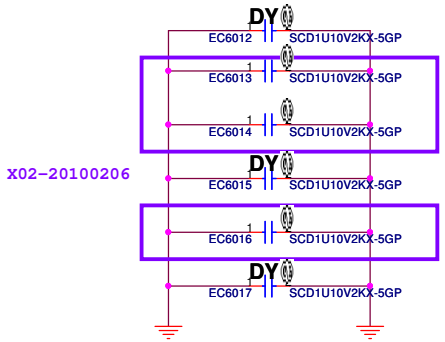


MIC IN



Internal Microphone





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack
Size: A3
Document Number: Berry
Rev: A00
Date: Monday, April 26, 2010
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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: A00

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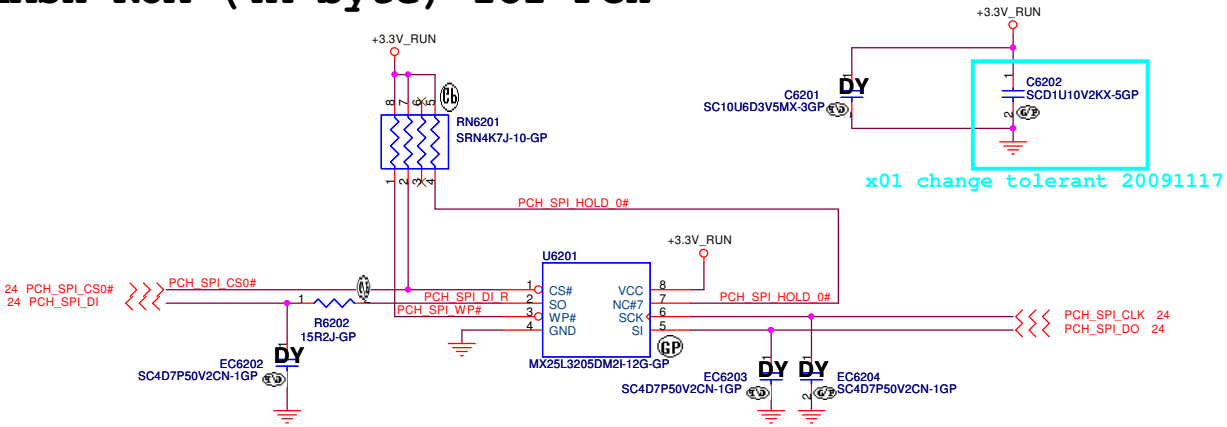
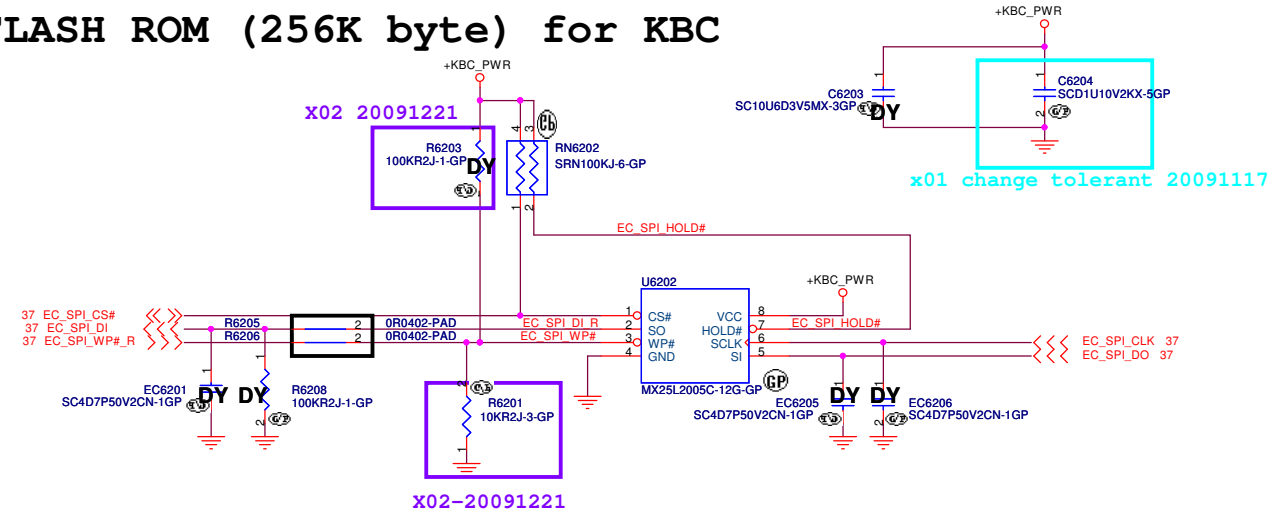
SSID = Flash.ROM

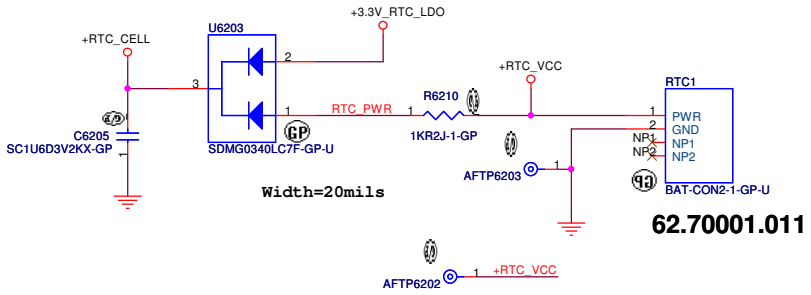
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

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Title: Flash/RTC

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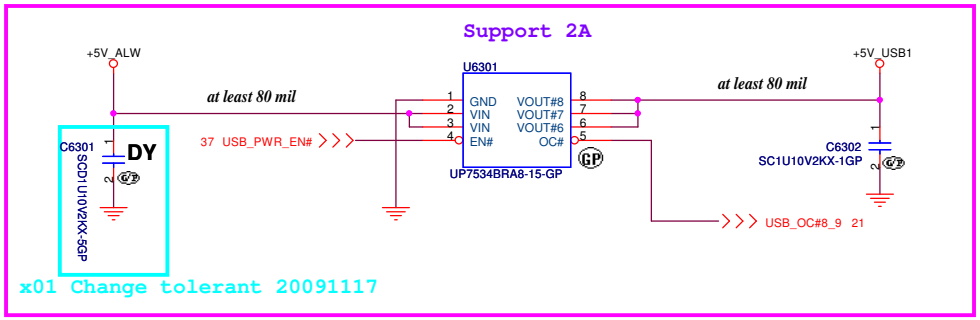
SSID = USB

IO Board USB Power

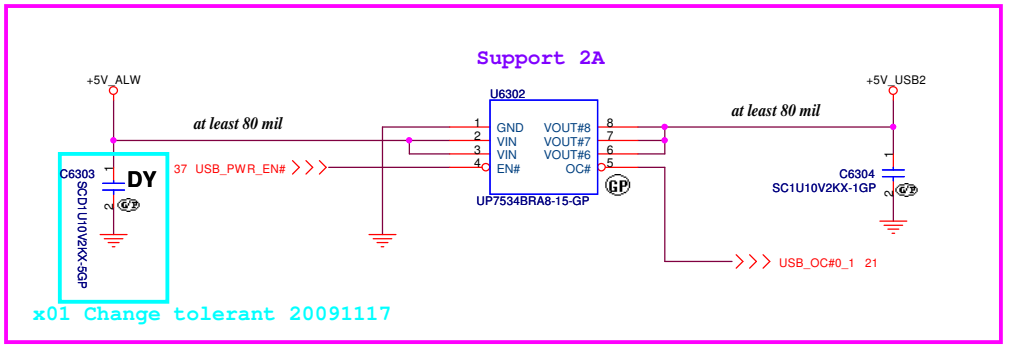
Close to I/O connector



USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079

CRT Board USB Power

Close to CRT Board connector



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	USB Power SW	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 63 of 92	

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<Core Design>

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Title
Reserved

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

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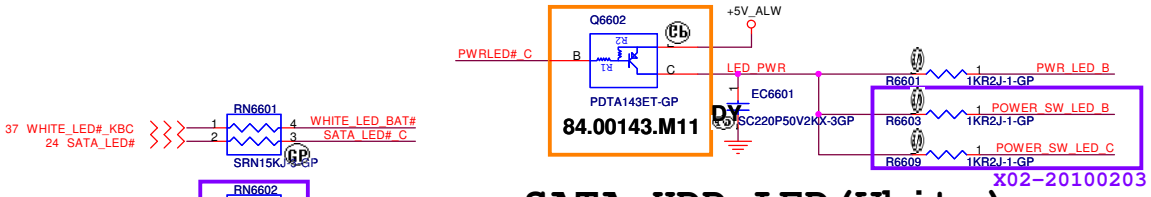
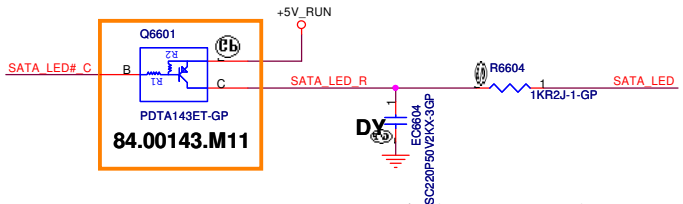
SSID = User.Interface

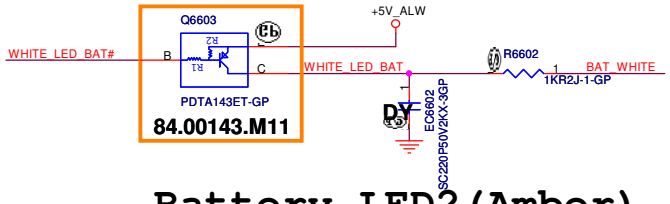
Power LED(White)

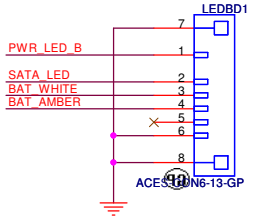


SATA HDD LED(White)

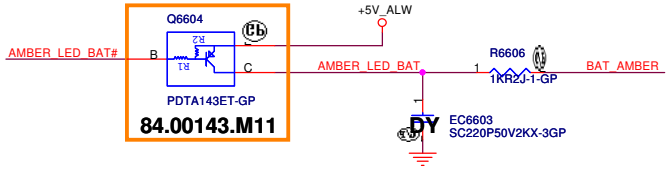


Battery LED1(White)

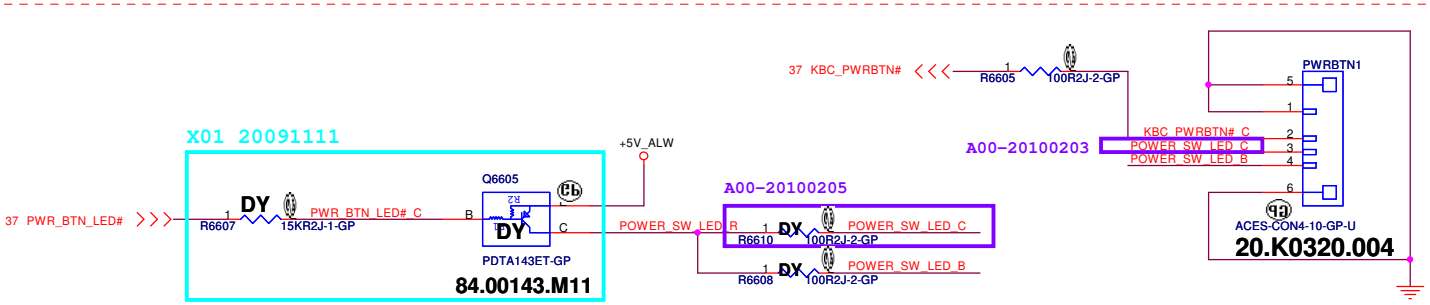




Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

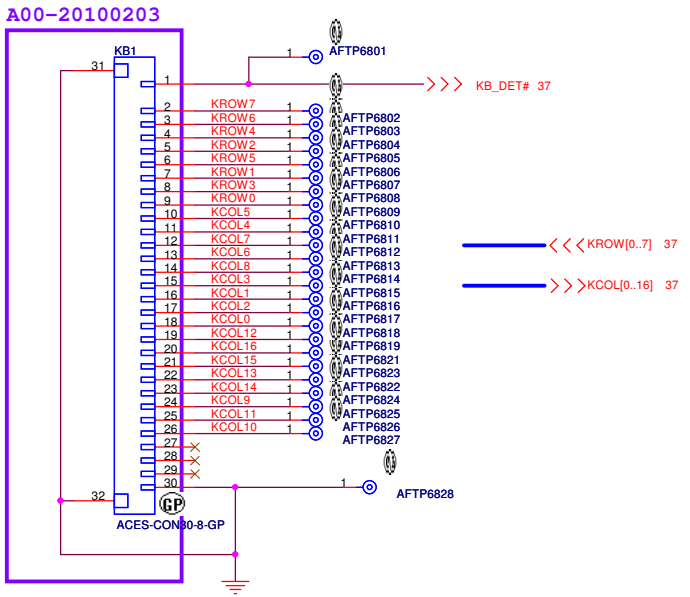
Title: *Reserved*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 67 of 92

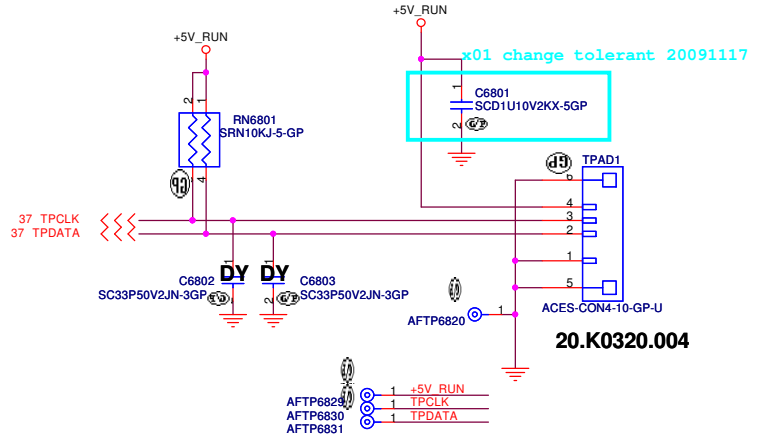
SSID = KBC

Internal KeyBoard Connector

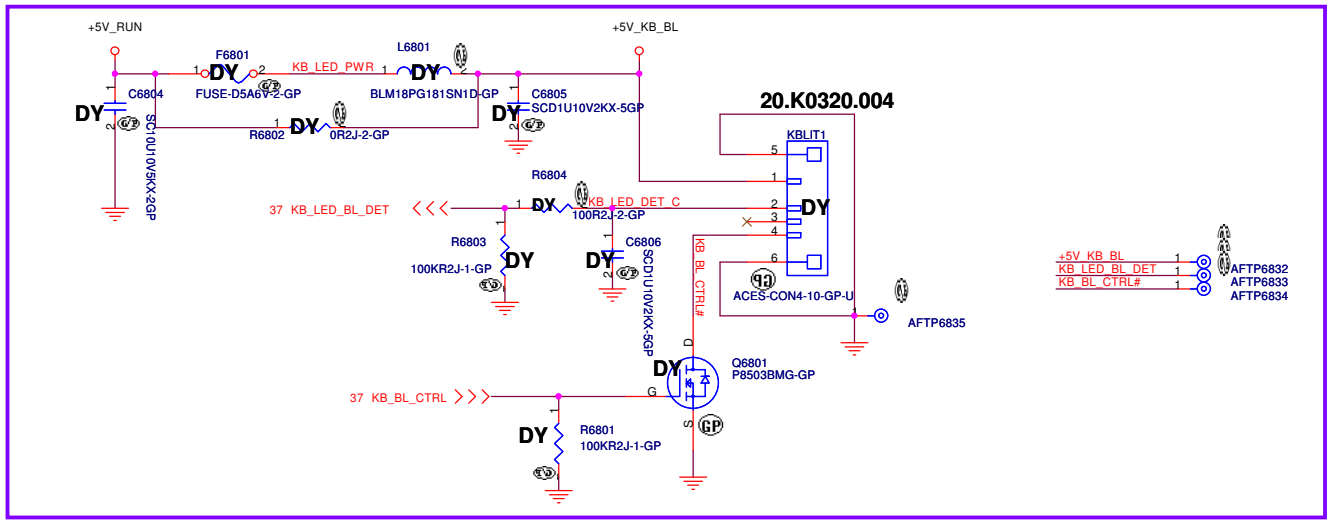


SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

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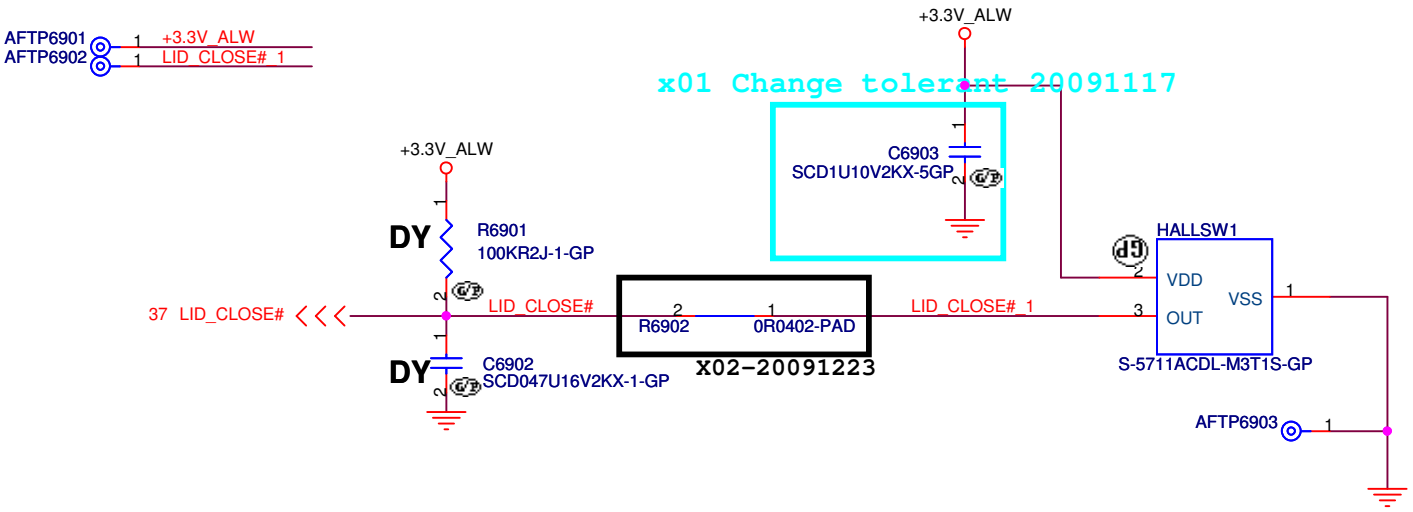

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

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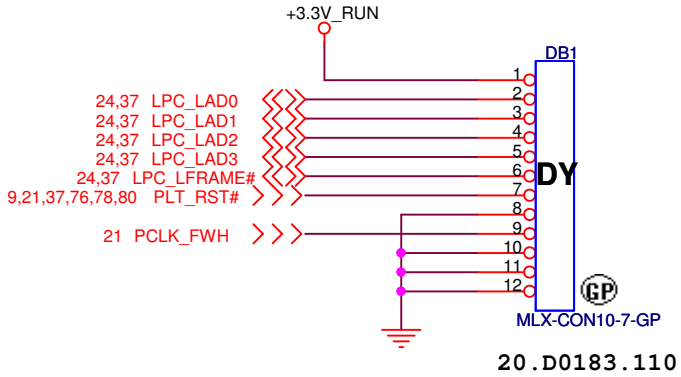

20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RESERVED***

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<Core Design>

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Title

RESERVED

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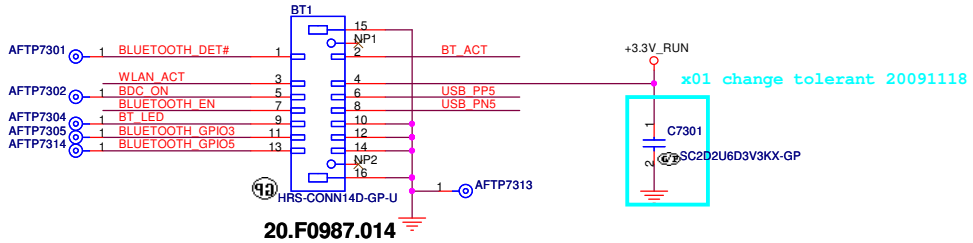
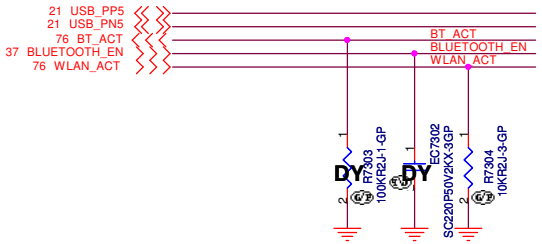
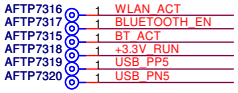
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size: A3 | Document Number: Berry | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*		
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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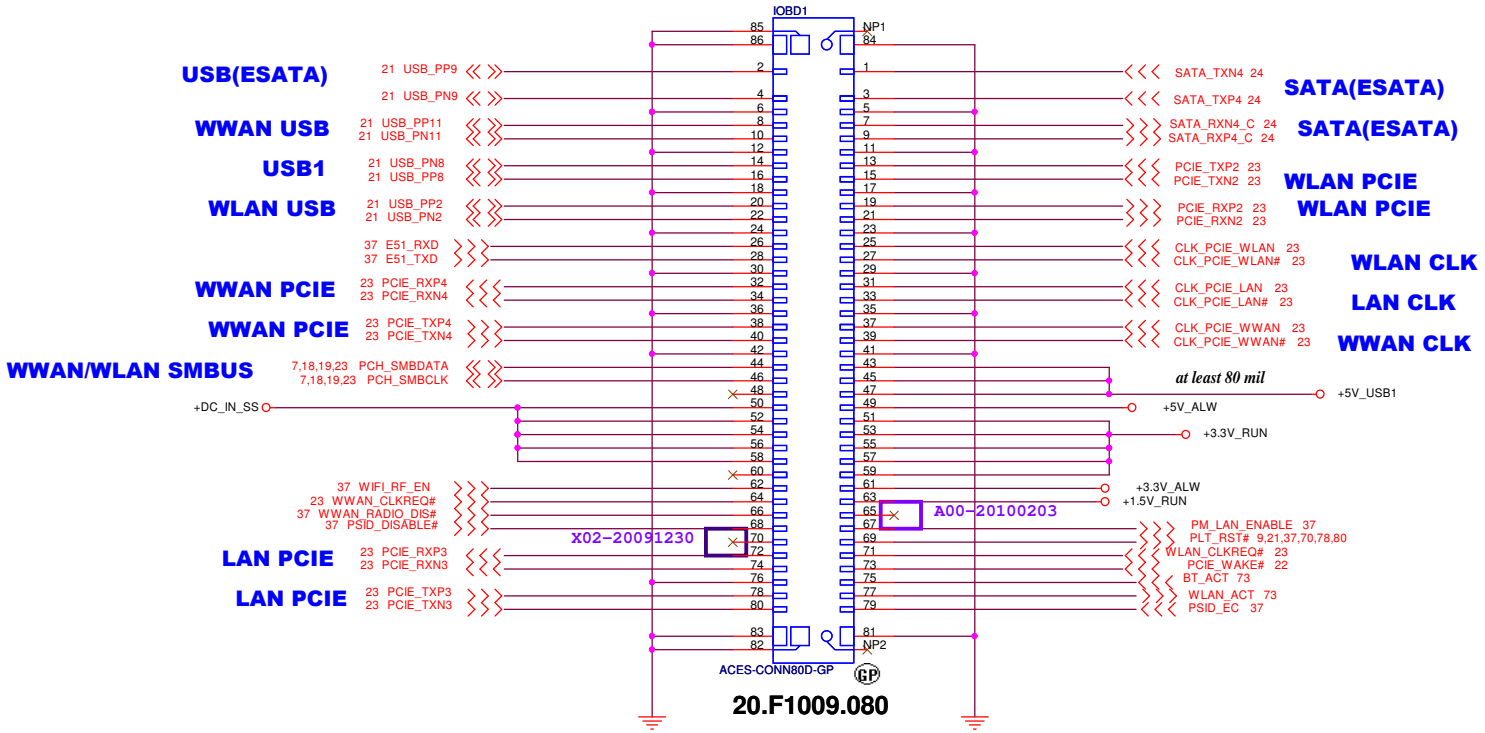
IO Board CONN 80 pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Berry | Rev: A00

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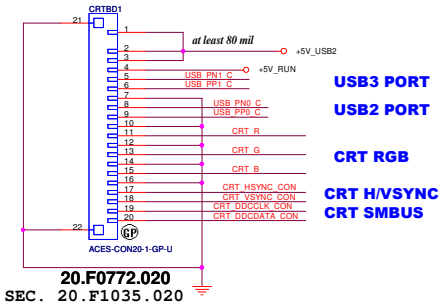
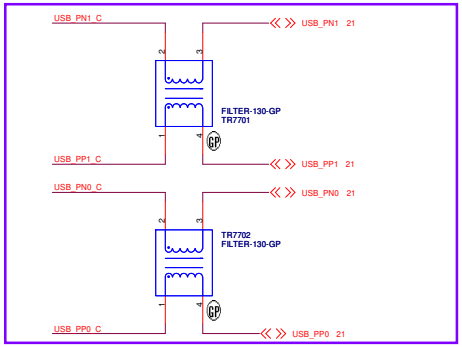
CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

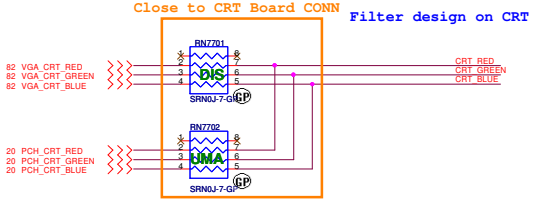
A00-20100120



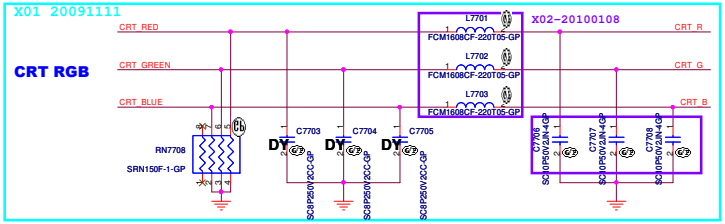
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

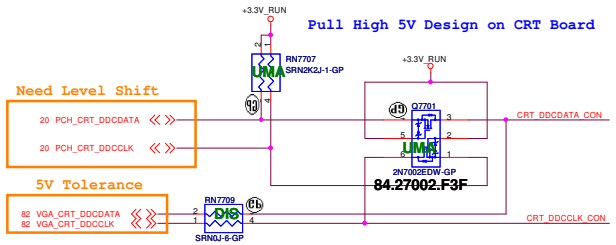


X01 20091111



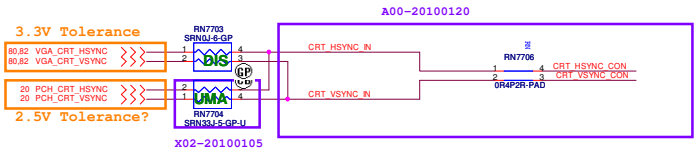
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CRT Board Connector
Size: A2	Document Number: Berry
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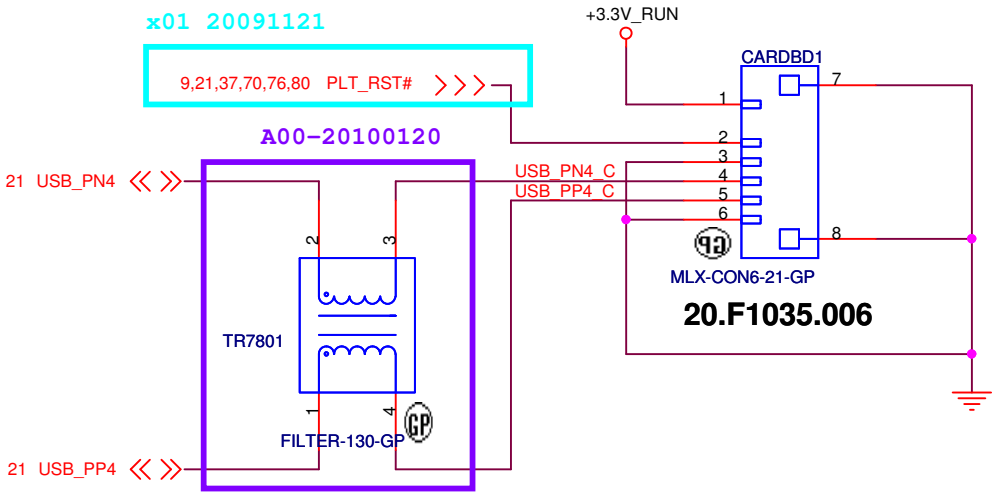
Date: Monday, March 29, 2010	Sheet 77 of 92

SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CARD Reader CONN*

Size	Document Number	Rev
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H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP

H10 HOLE335R115-GP
H11 HOLE256R111-GP

CPU Thermal module hole

HTML1 HOLE197R166-GP
HTML2 HOLE197R166-GP
HTML3 HOLE197R166-GP
DY DY DY

GPU Thermal module hole

HGPU1 STF237R117H83-1-GP

stand off

HBT1 STF237R117H123-GP

EMI Reserve

+PWR_SRC
X01 stuff 20091119
EC7901 EC7902 EC7904 EC7903 EC7905 EC7907 EC7909 SCD1U25V2KX-GP
DY EC7942 EC7940 EC7941 EC7939 EC7943 EC7938 SCD1U25V2KX-GP

+VGFXCORE_PWR_SRC
EC7906 DY SCD1U25V2KX-GP

+PWR_SRC_VTT
EC7911 SCD1U25V2KX-GP
X01 stuff 20091118

+PWR_SRC_1D5V
EC7916 DY SCD1U25V2KX-GP

EMI Reserve
SPR1 SPRING-58-GP DY

X01 RF Reserved-20091118

+PWR_SRC_1D5V 56pF*1
EC7908 DY SC68P50V2JN-2GP

+PWR_SRC 56pF*7
EC7912 EC7913 EC7917 EC7919 EC7920 EC7922 EC7925 DY SC68P50V2JN-2GP

+PWR_SRC +1.5V_SUS 0.1uF*2
EC7921 EC7933 SCD1U25V2KX-GP

+1.05V_VTT X02-20100208
EC7923 DY EC7924 UMA EC7926 UMA EC7927 UMA SCD1U25V2KX-GP

+1.5V_SUS
EC7945 DY EC7929 DY EC7936 DY EC7944 DY SCD1U25V2KX-GP

A00-20100204

+CPU_GFX_CORE 0.1uF*2
EC7946 DY EC7947 DY SCD1U25V2KX-GP

+VGA_CORE 56pF*1
EC7928 DY SC56P50V2JN-2GP

+1.5V_SUS 56pF*3
EC7930 DY EC7931 DY EC7932 DY SC56P50V2JN-2GP

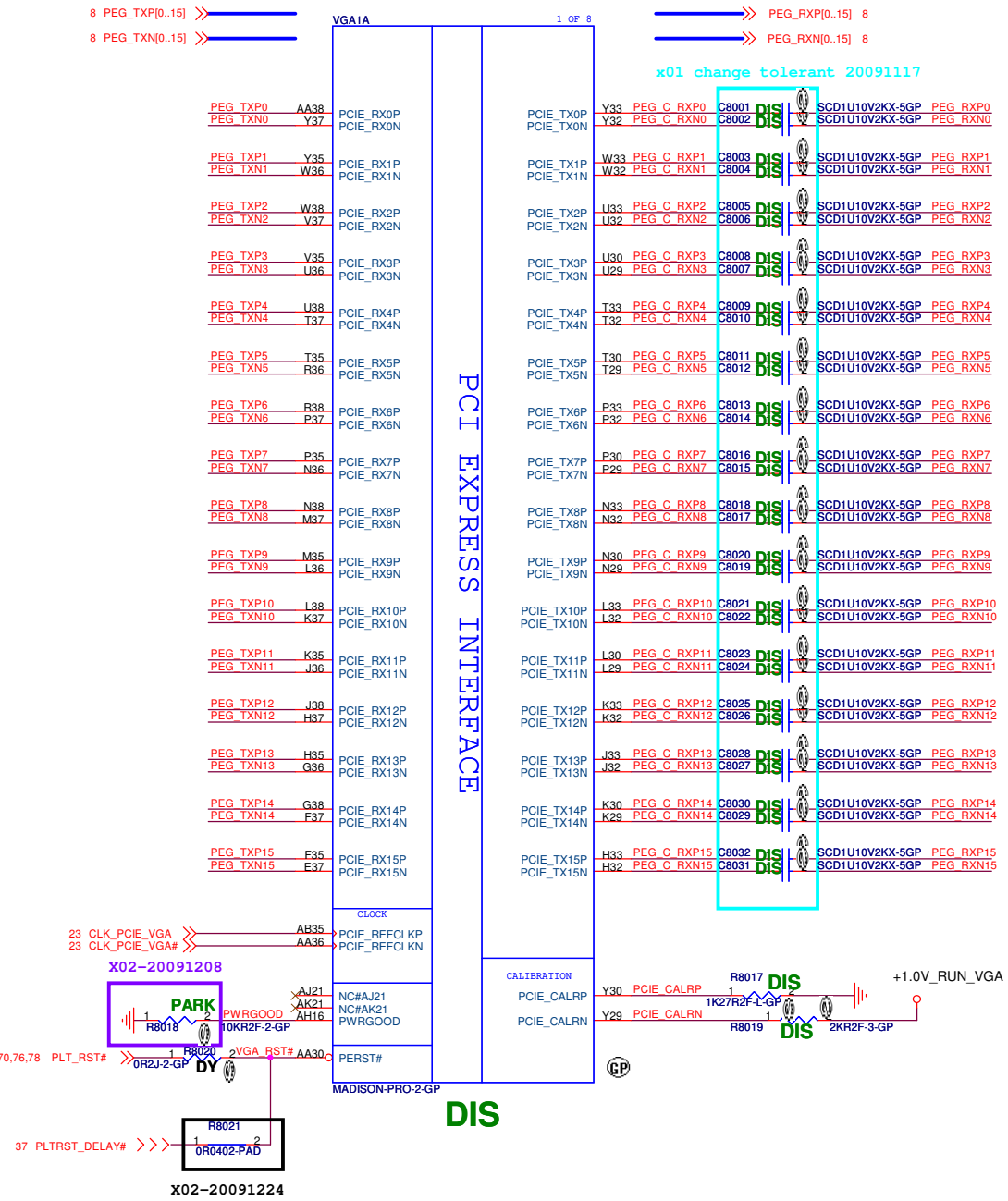
+VCC_CORE 56pF*2
EC7934 UMA EC7935 DY SC56P50V2JN-2GP
X02-20100209

+5V_RUN 56pF
EC7937 DY SC56P50V2JN-2GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: Berry | Rev: A00
Date: Wednesday, February 10, 2010 | Sheet 79 of 92



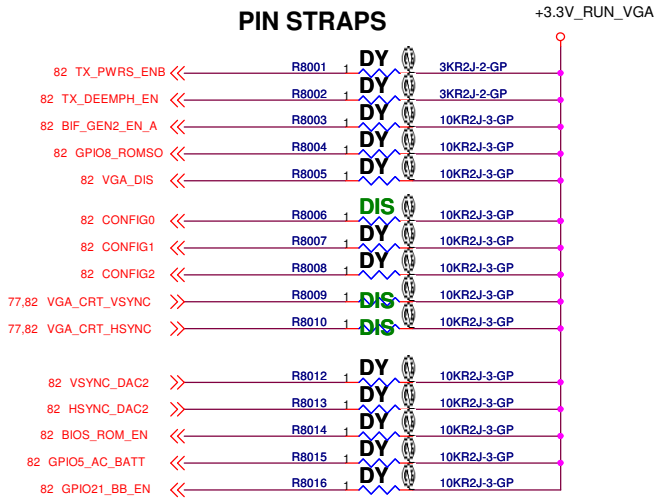
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	Berry	A00

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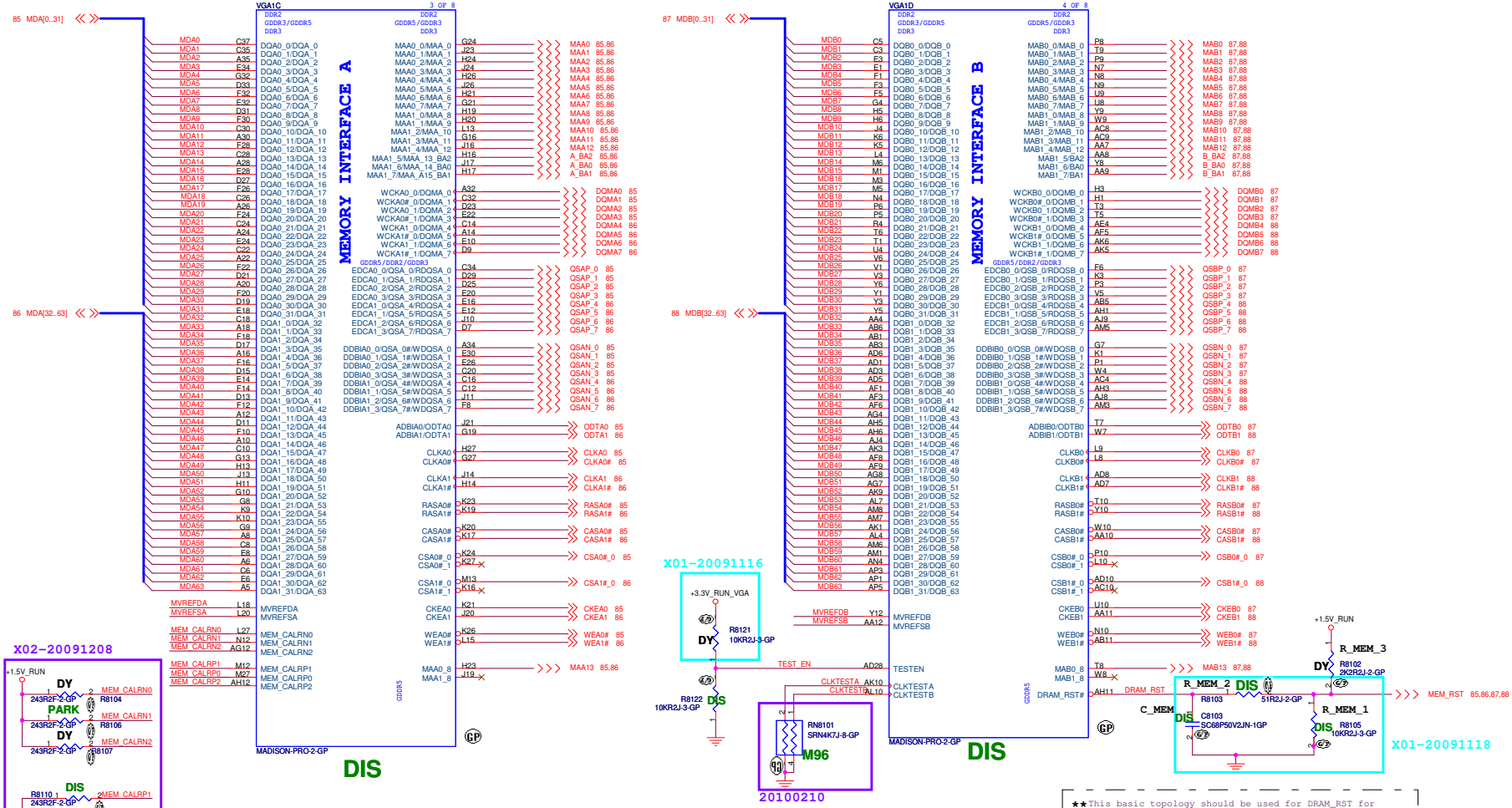


Designator	For Mannhatton	For M96-M2/M92-M2
R_MEM_1	10K	2.2nF
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	68pF	10K

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU Memory(2/5)
Size: C | Document Number: Berry | Rev: A00
Date: Monday, March 29, 2010 | Sheet 81 of 92

MEMORY ID Table

DVPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVPDATA[0:3] Default:Pull down

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

LVDS Interface

MEM_ID Control
X02-20091222

X02-20100104
84.27002.F3F

X02-20100104
84.2N702.D31

I2C Bus for LVDS

Straps

JTAG SIGNAL OPTION

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

X02-20091210
Voltage Swing:1.8V

X02 20091208

DDC1 channel for CRT

DDC2 channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

x01 Change tolerant 20091117

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

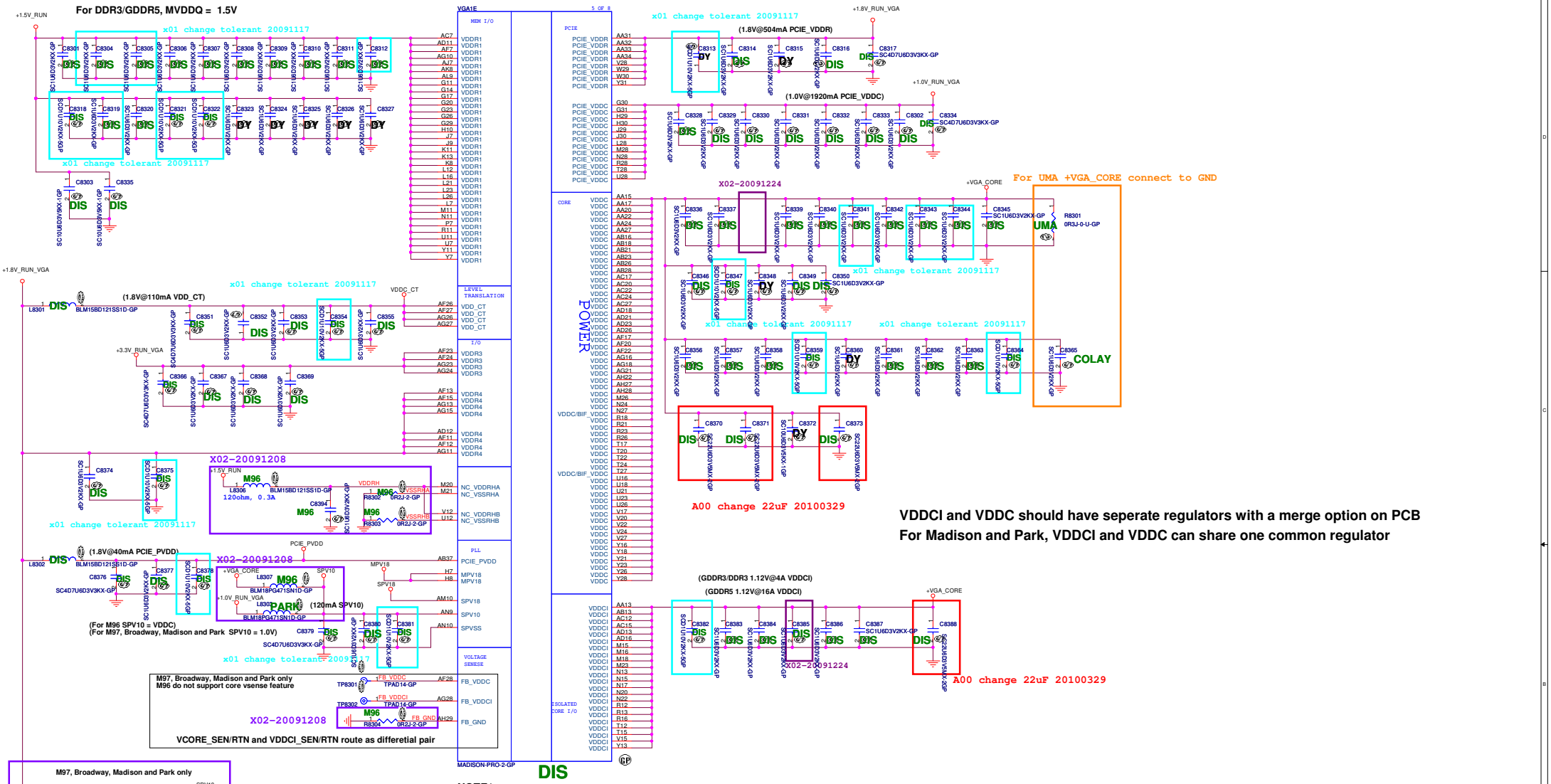
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 82 of 92



NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	Berry	A00

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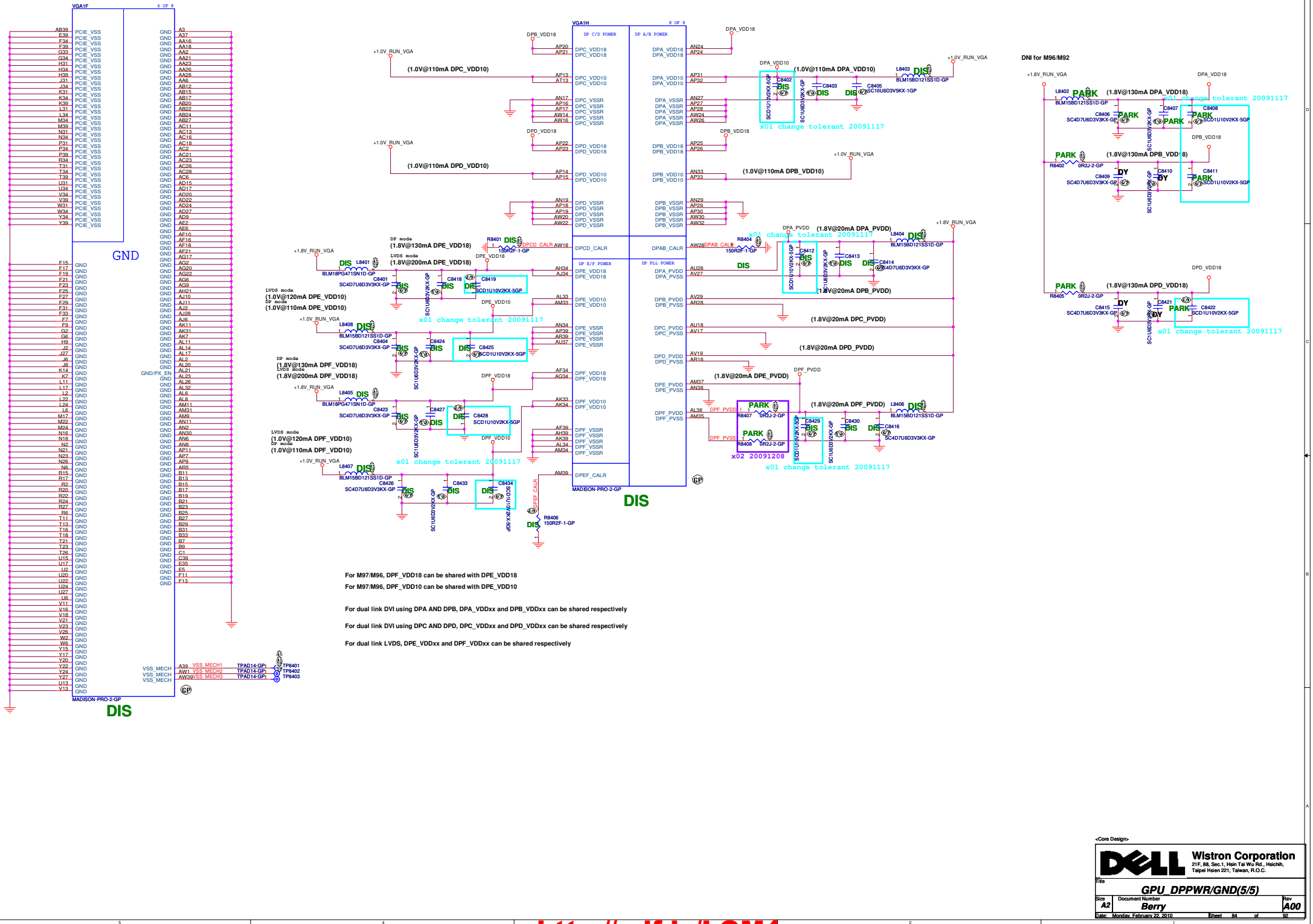

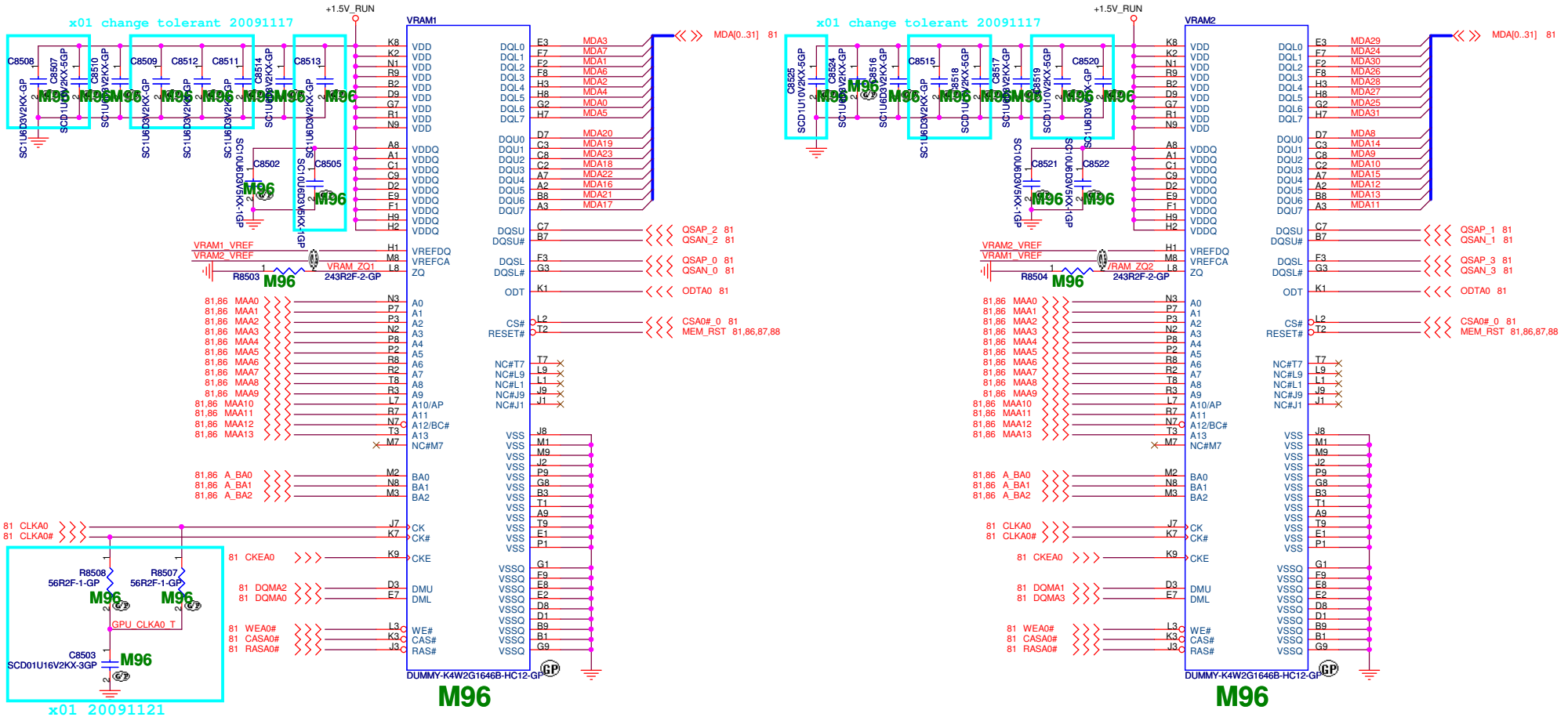

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Berry	A00

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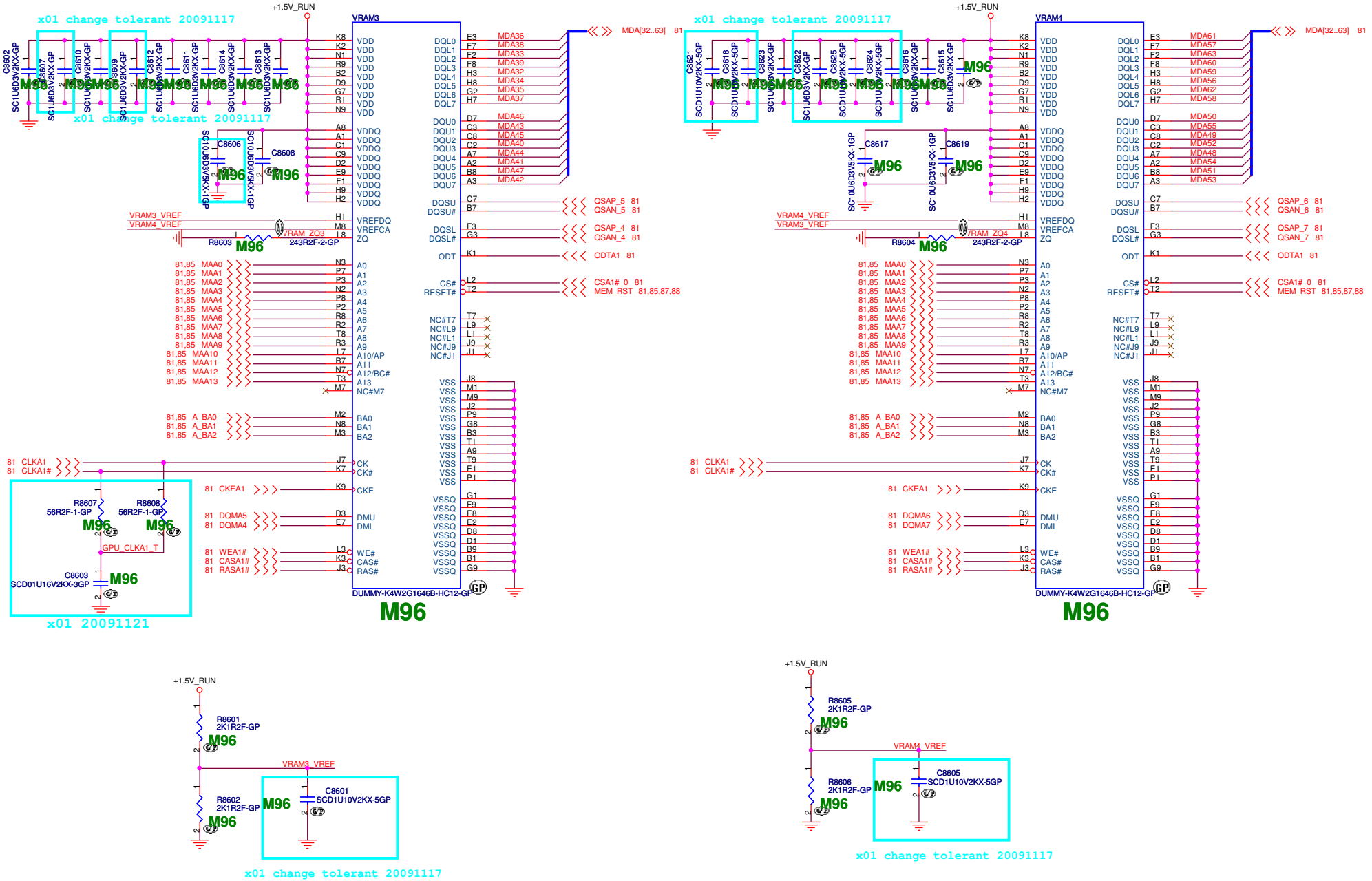

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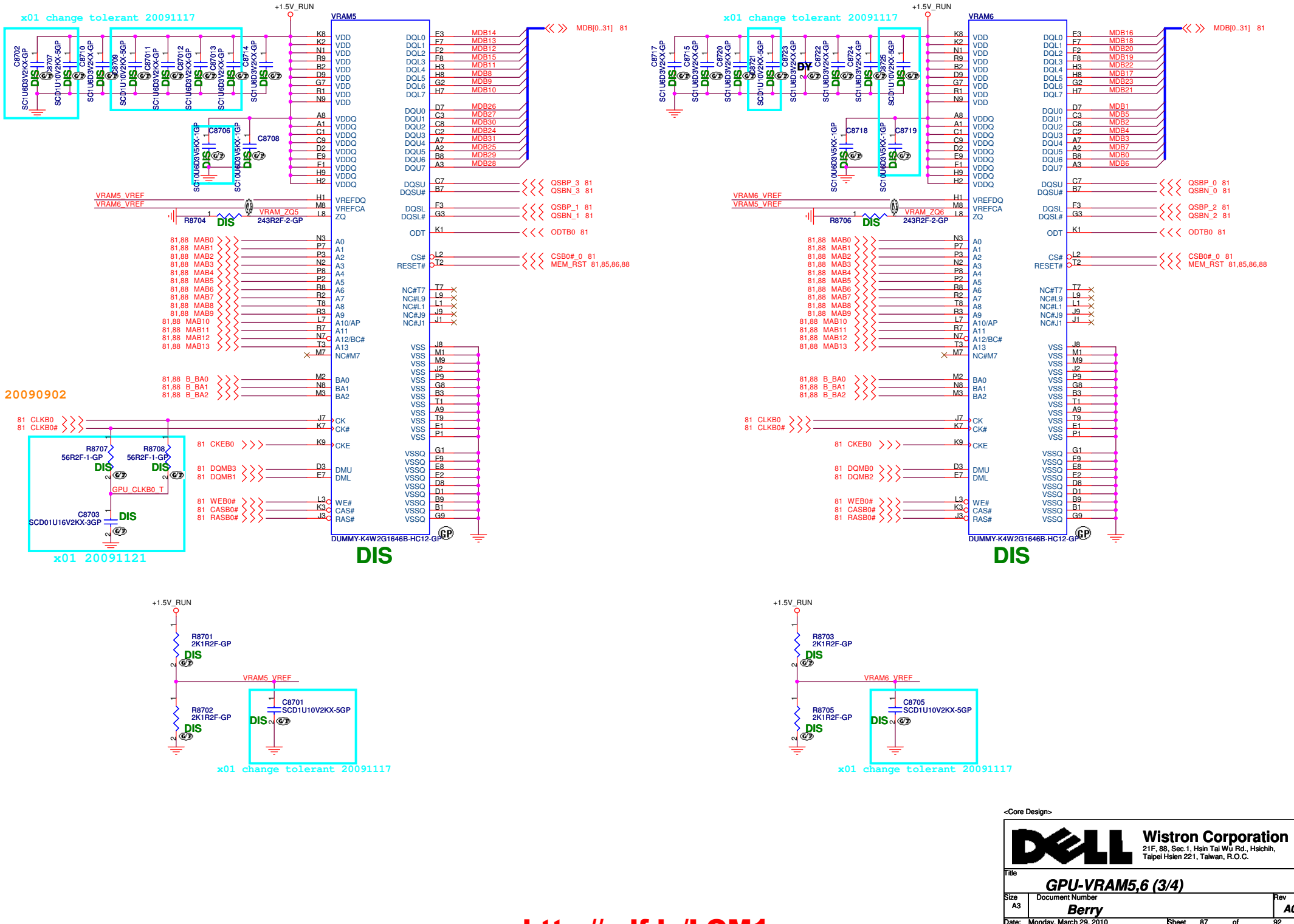
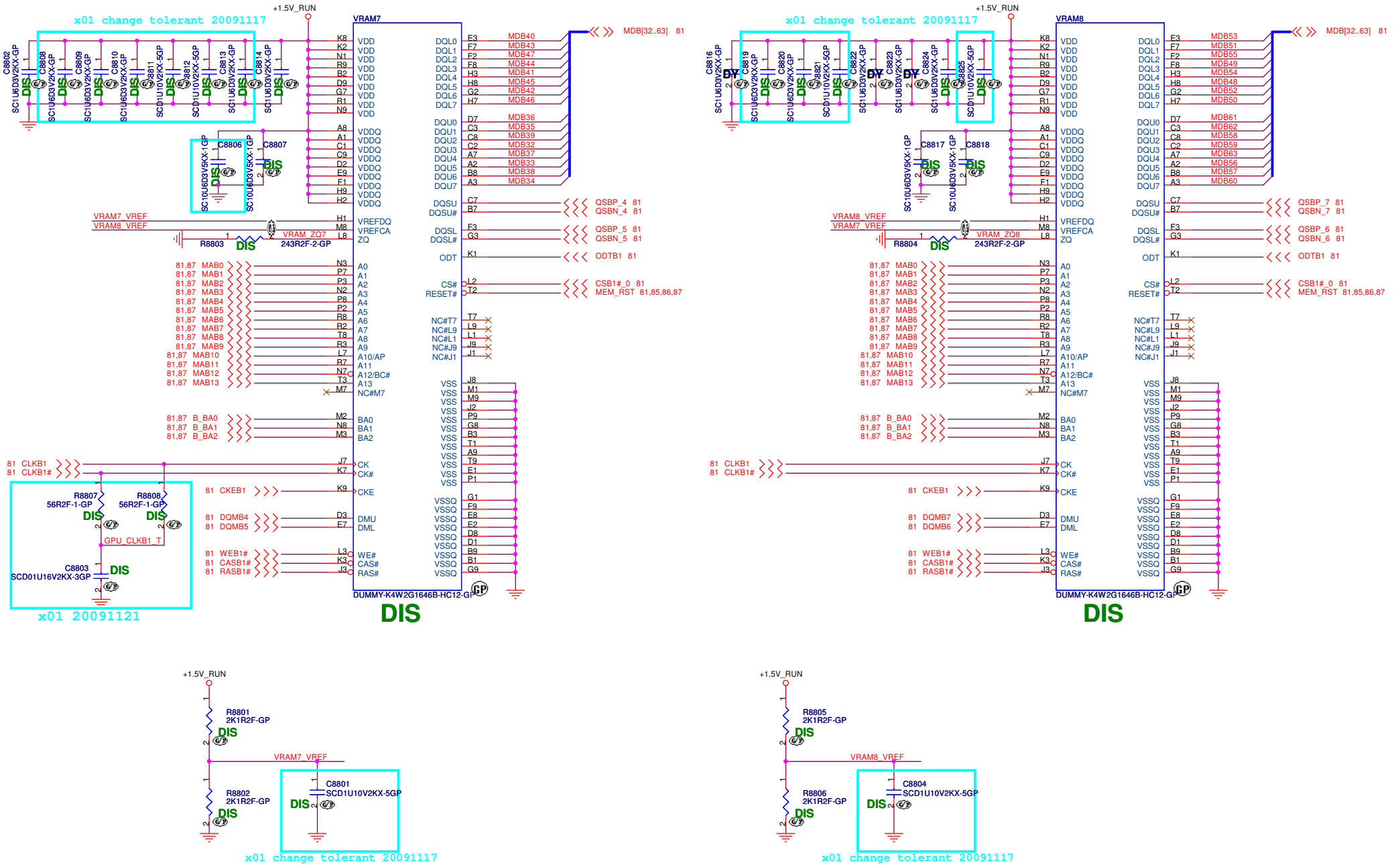
Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Berry | Rev: A00

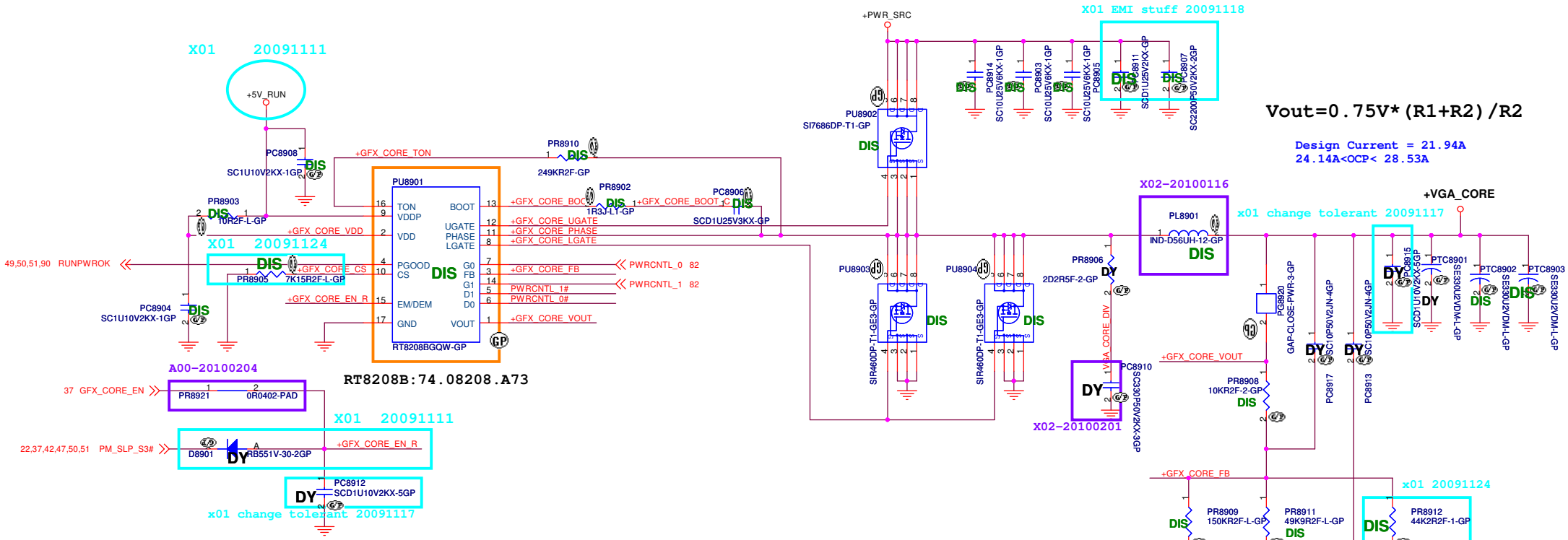
Date: Monday, March 29, 2010 | Sheet 86 of 92





SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



Park-XT

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

Madison-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.12V

M96-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.0V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size: A3 | Document Number: Arsenal DJ1 Discrete | Rev: A00

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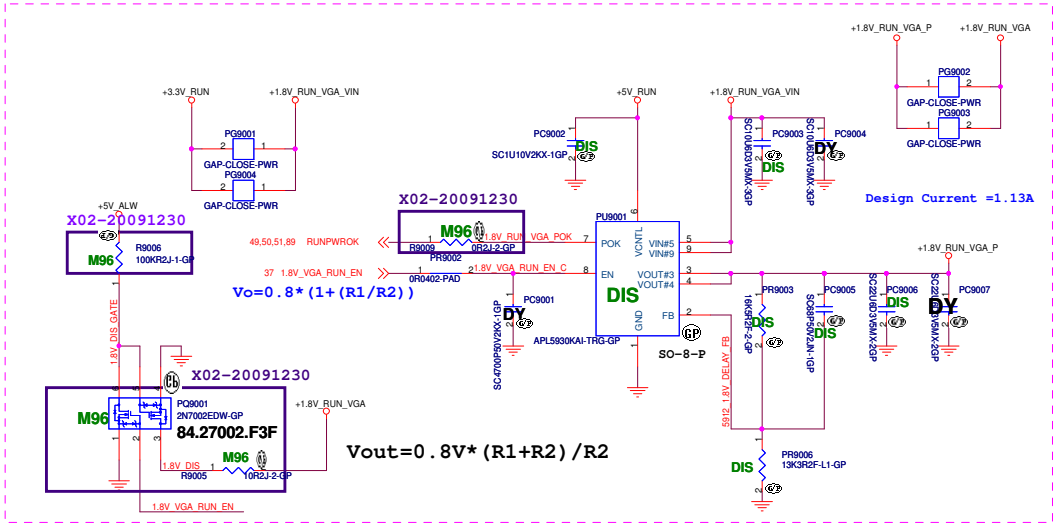
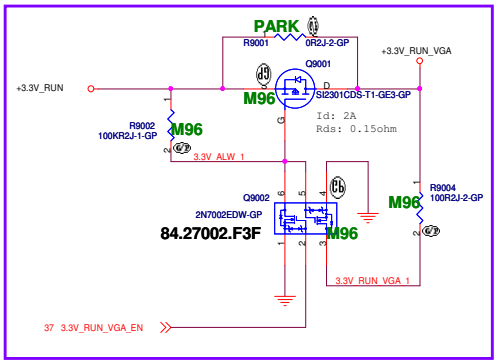
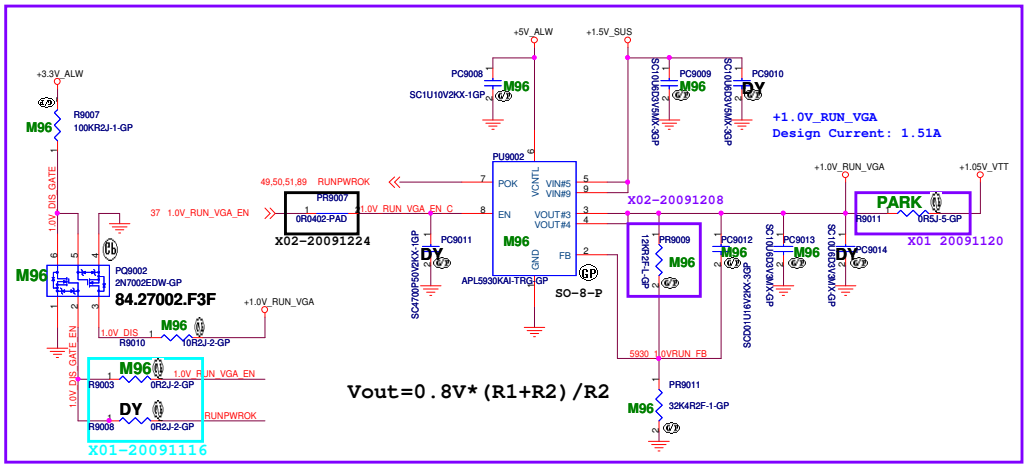
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



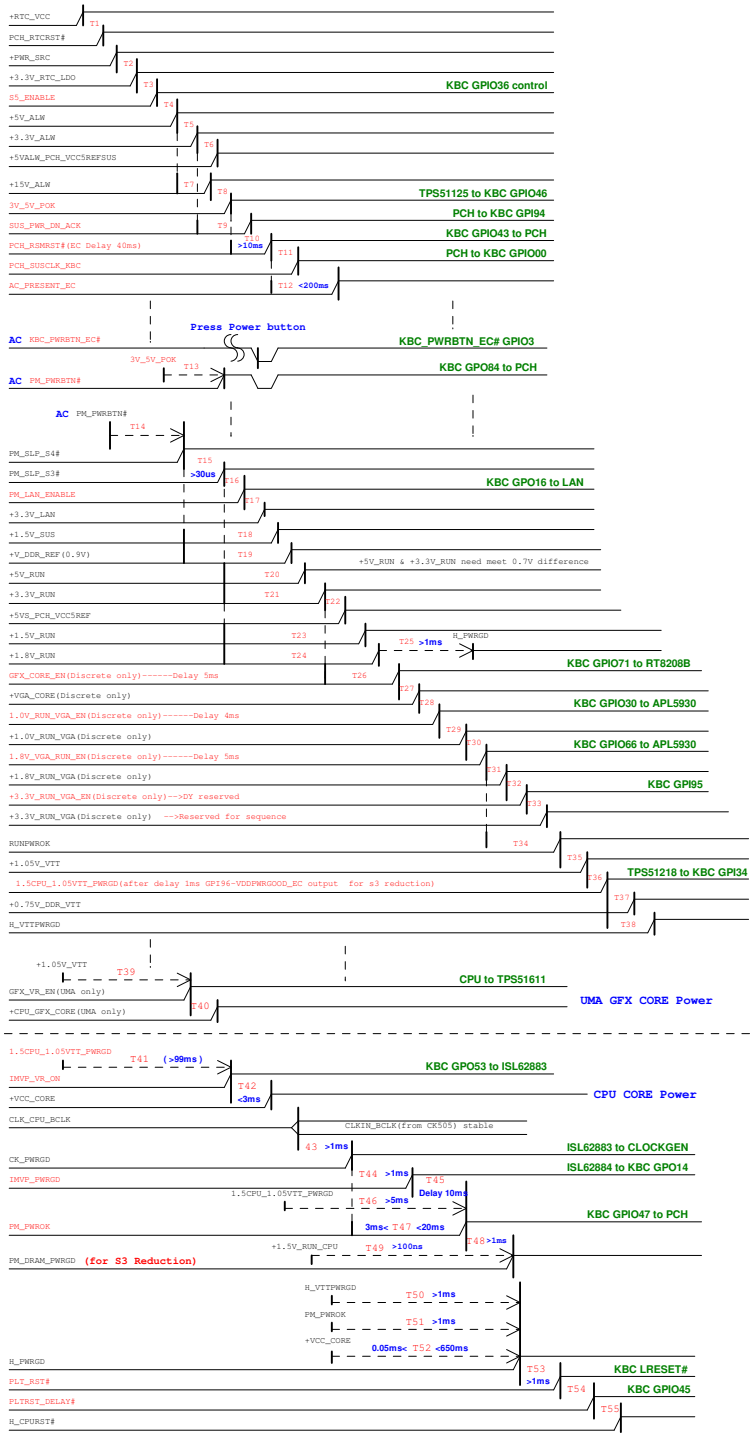
APL5930KAI for +1.0V_RUN_VGA



D15 Intel-Power Up Sequence

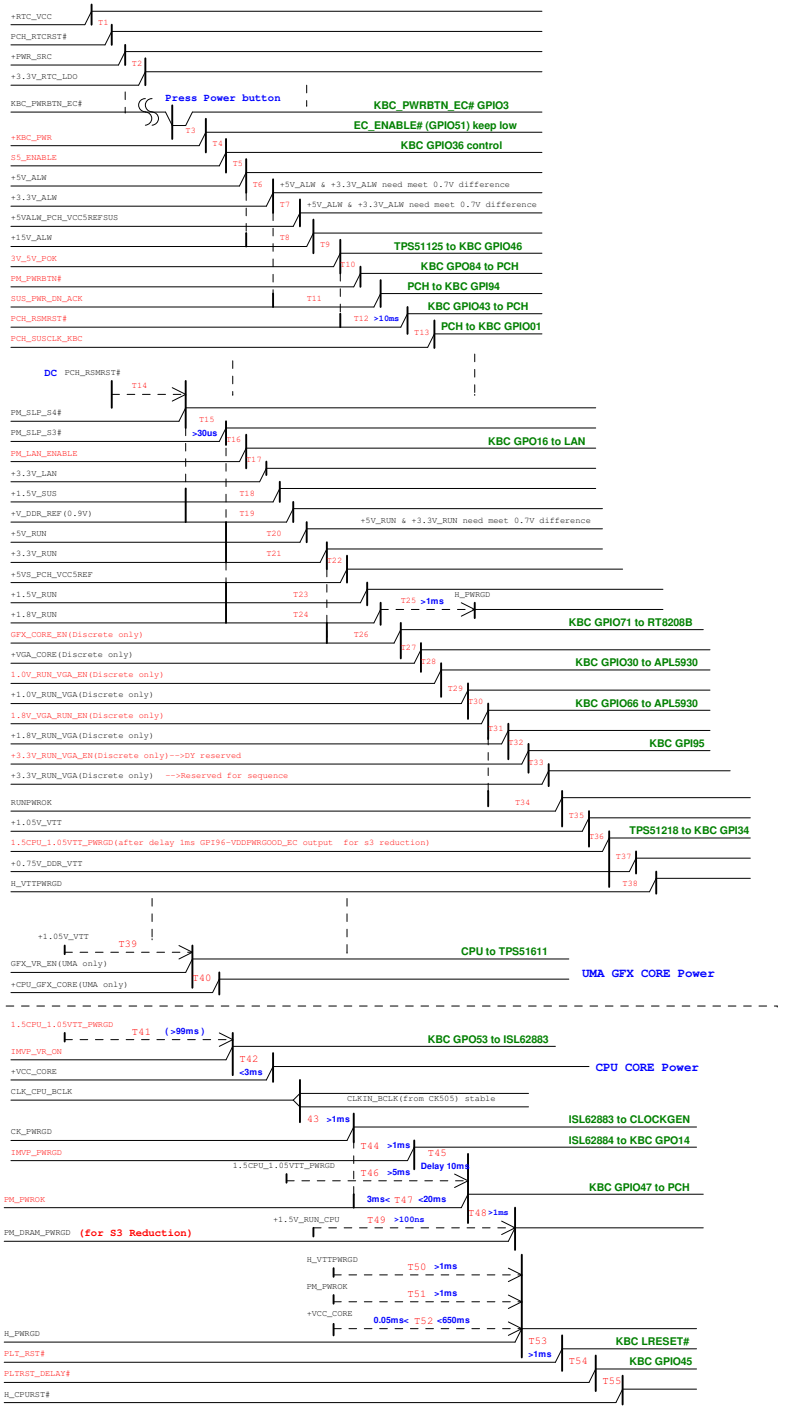
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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File: Power Sequence
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Date: Tuesday, March 09, 2010 | Sheet 51 of 90

(Blanking)

<Core Design>

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Title: *Change History*

Size: A3 | Document Number: *Berry* | Rev: *A00*

Date: Wednesday, February 10, 2010 | Sheet 92 of 92