

Berry AMD IO Board Schematics Document

2010-02-24

REV : A00

DY : Nopop Component

<Core Design>



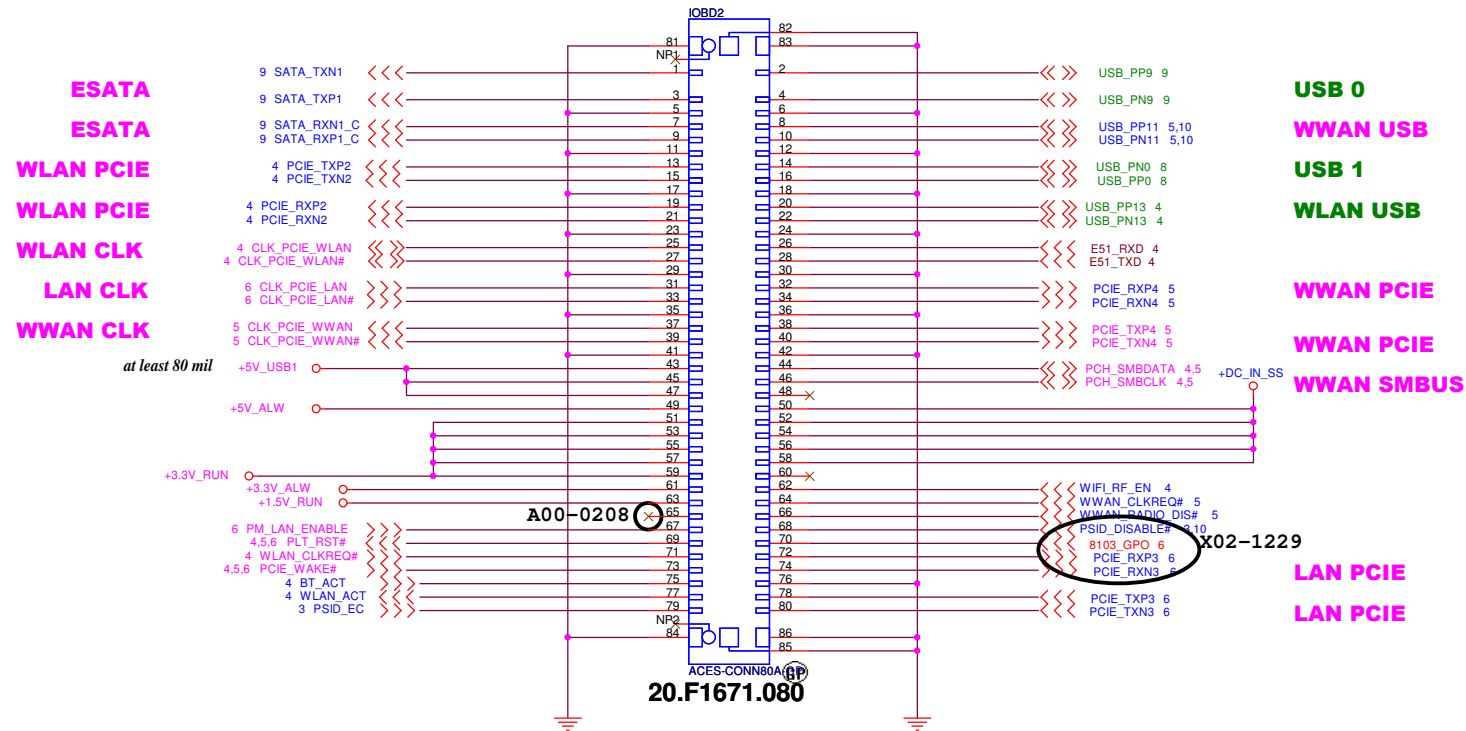
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Cover Page		
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Berry IO Board

Project code: 91.4HH01.001

PCB P/N : 09697-SC

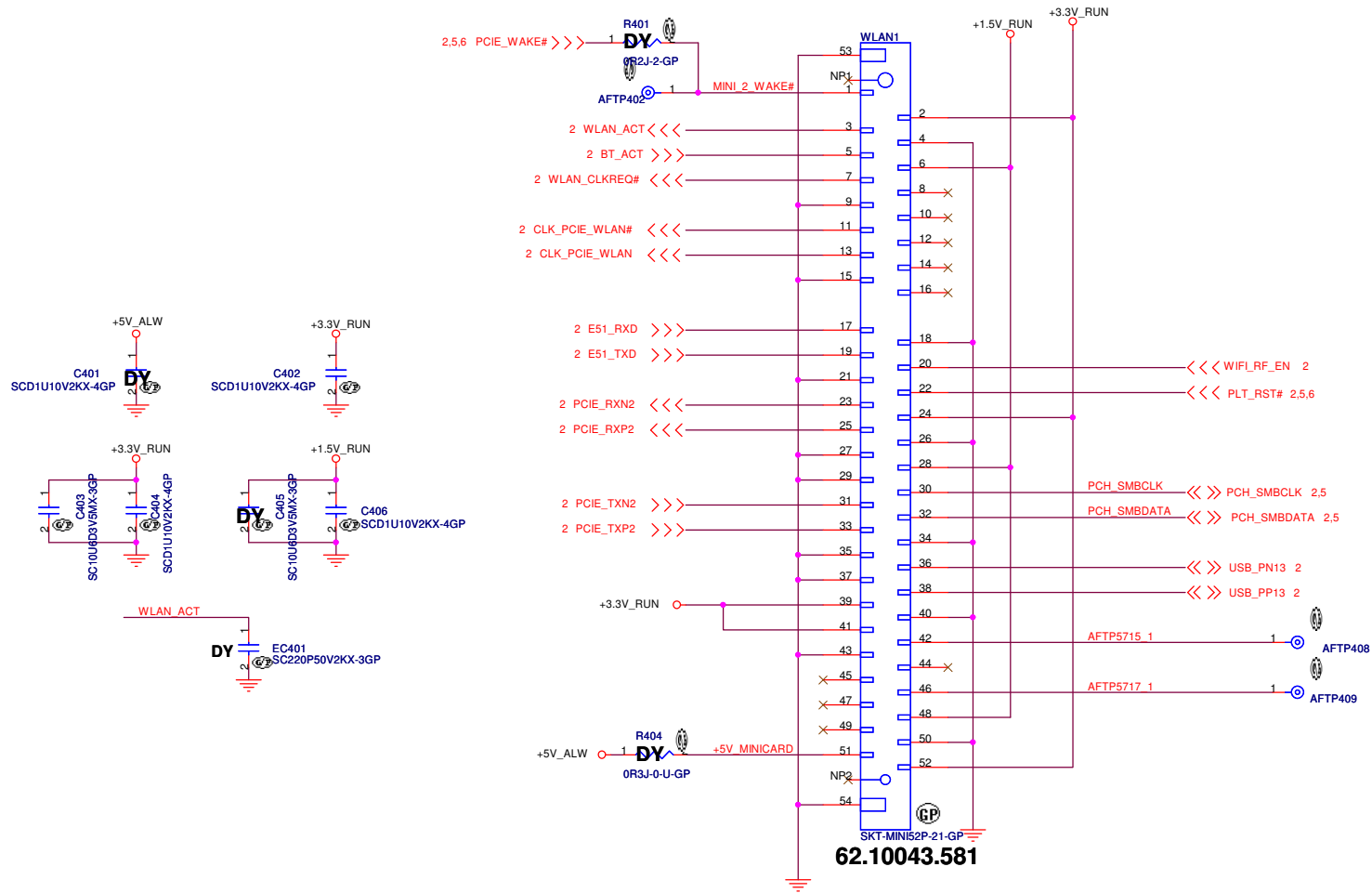
REVISION : SC



PCIE_RX Decoupling Capacitor near LAN Chip

SSID = Wireless

Mini Card Connector(802.11a/b/g)

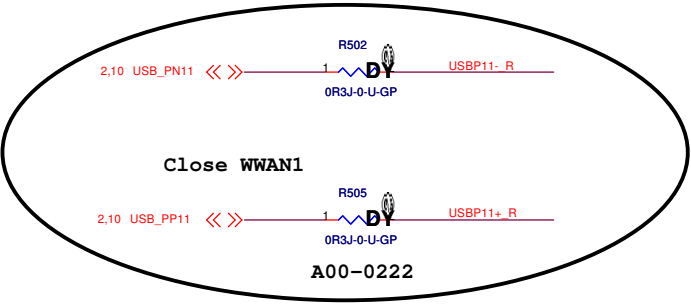


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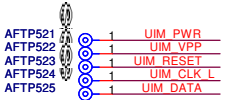
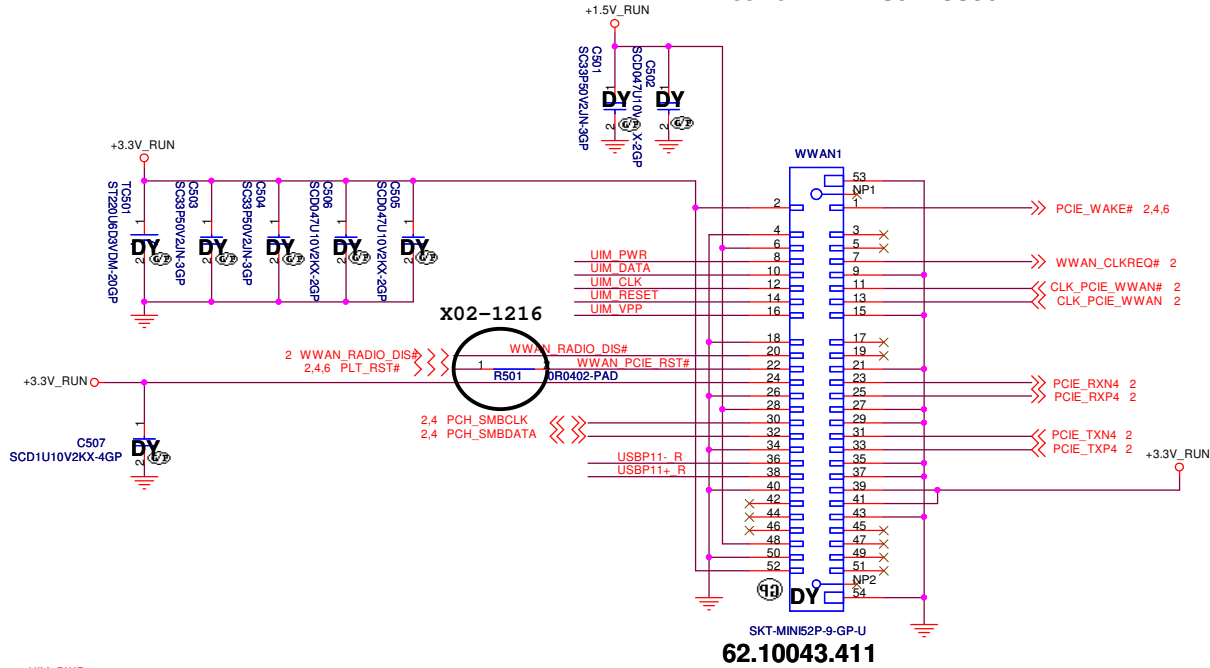
Title			BATT CONN		
Size	Document Number	Berry IO Board		Rev	X02
A3					
Date:	Wednesday, December 30, 2009	Sheet	4	of	12

Layout note: Place caps C401~C407 close WWAN1 connector.

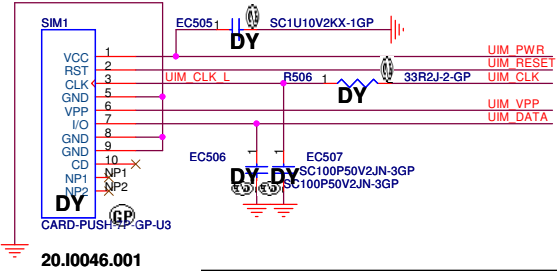
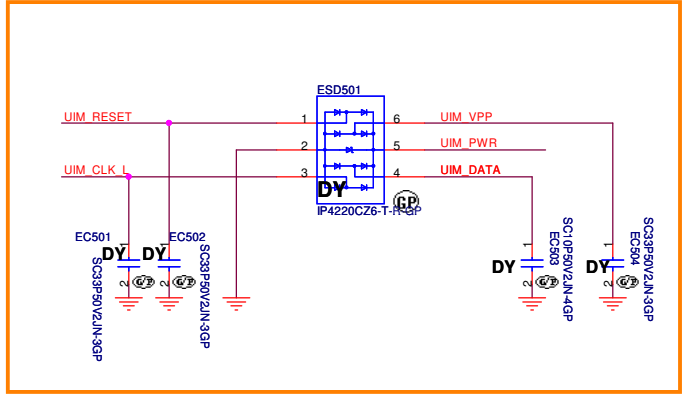


C901 Please near WWAN1

MiniCard WWAN connector



Close to SIM1



Place caps EC806, EC807 closest to SIM1

DATA and CLK need keep away about 12mil

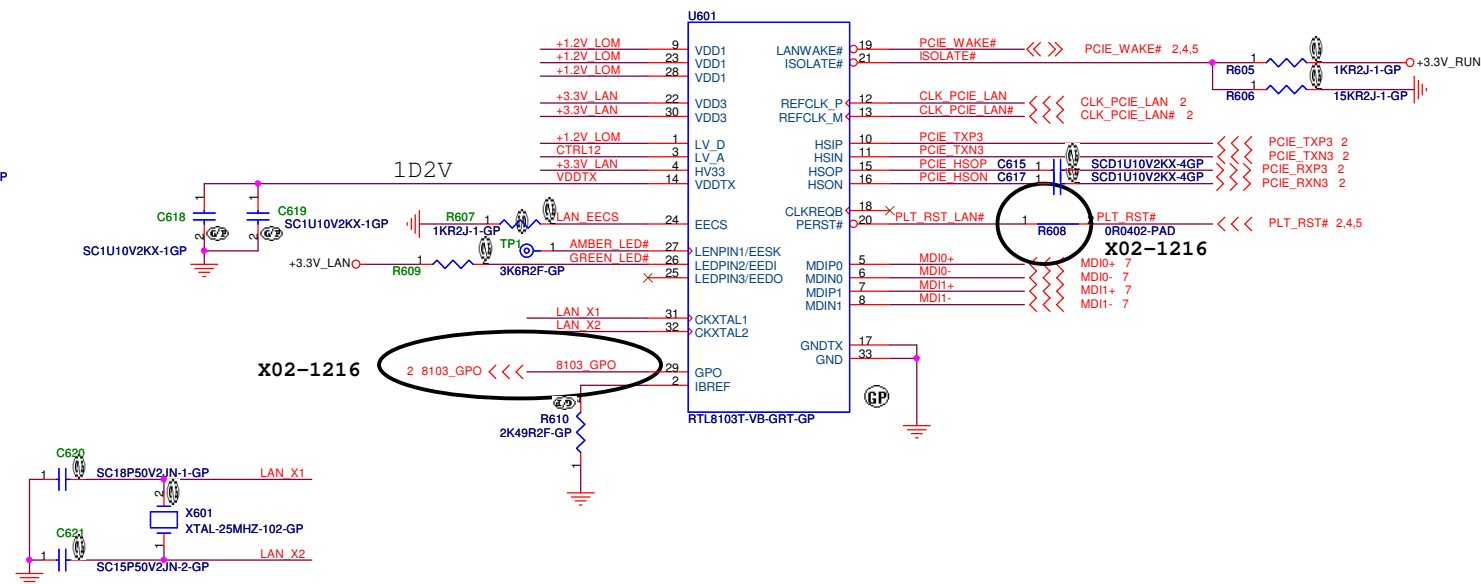
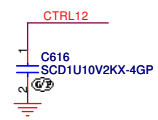
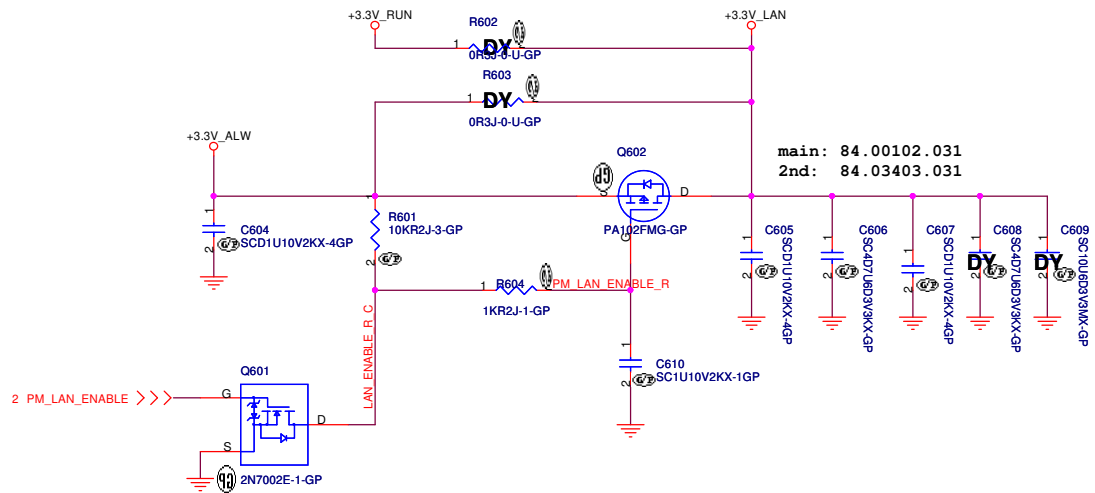
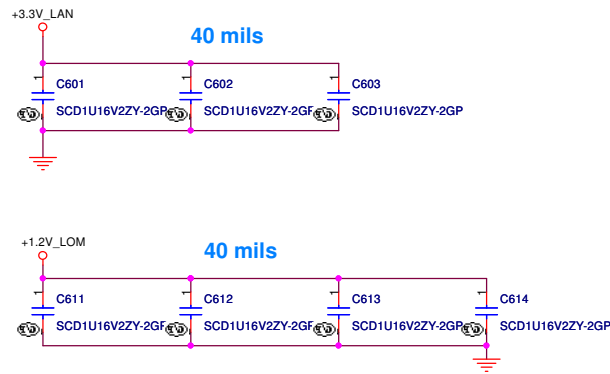
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Title: **WWAN/SIM Card**

Size: **A3** Document Number: **Berry IO Board** Rev: **X02**

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X02-1216 2 8103_GPO <<< 8103_GPO

Main: 82.30020.851
2nd : 82.30020.791

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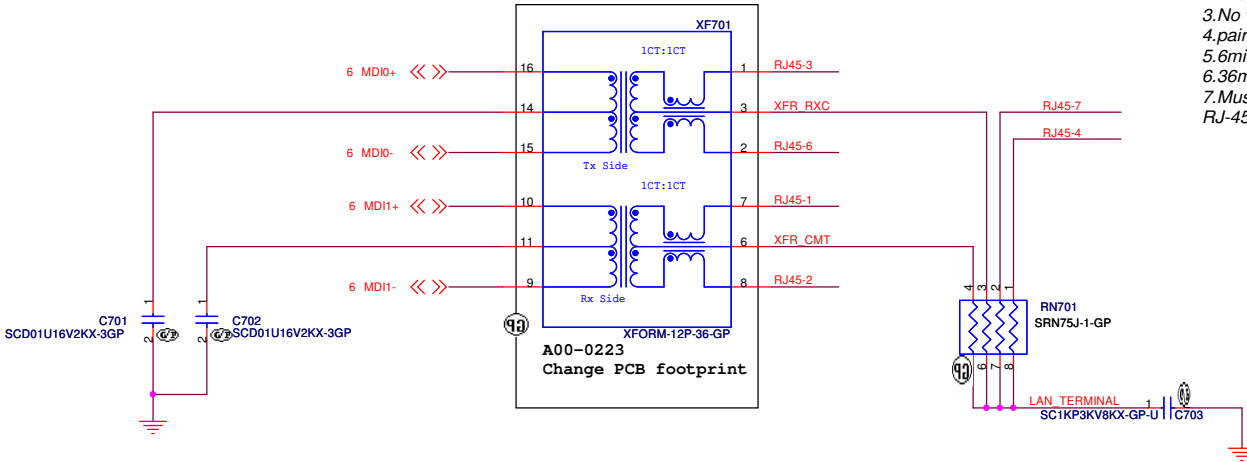
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Title: **LAN RTL8103T**

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		X02

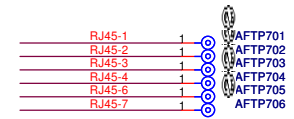
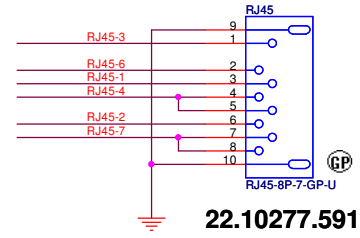
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10/100M Lan Transformer



1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ45 Connector



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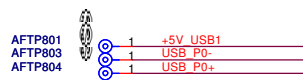
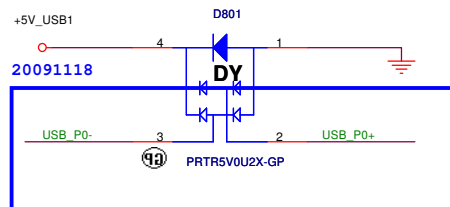
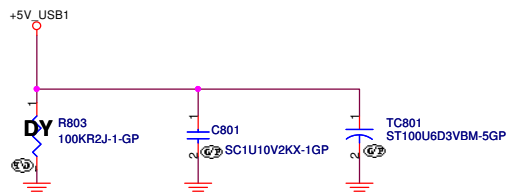
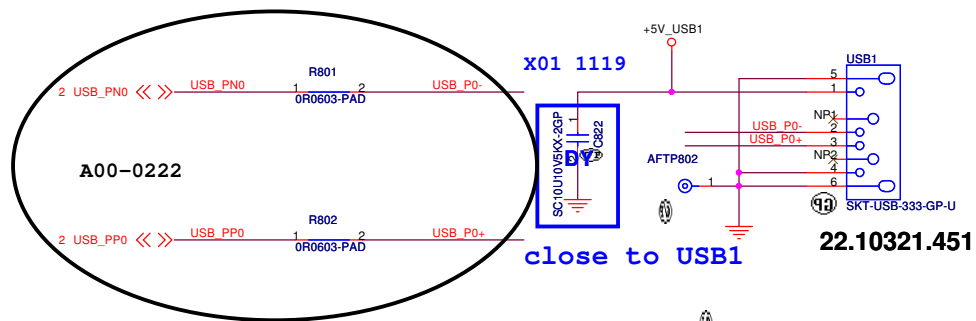
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XFORM

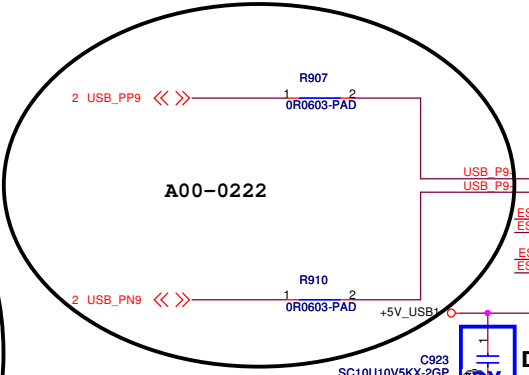
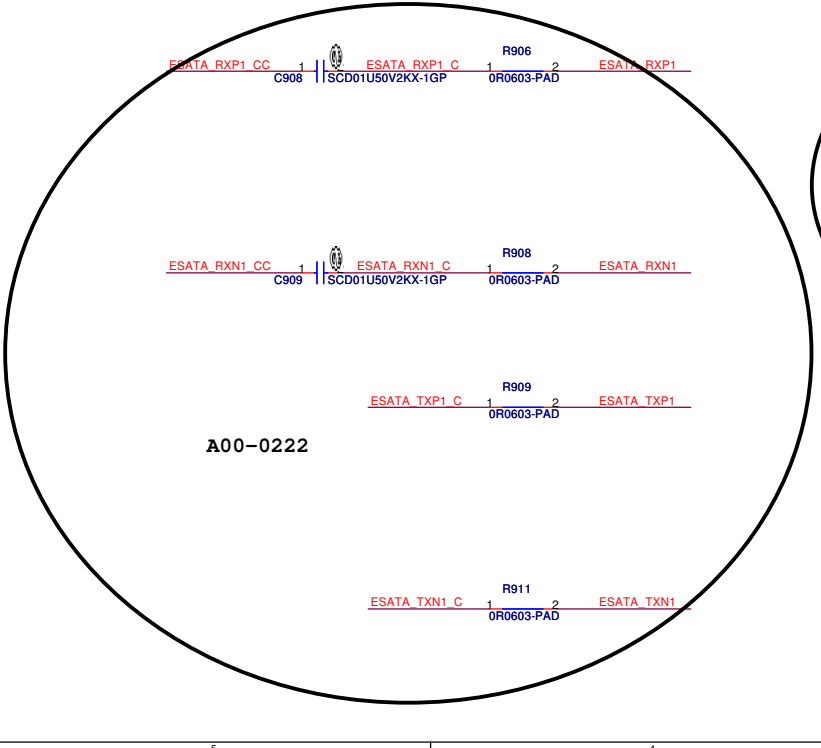
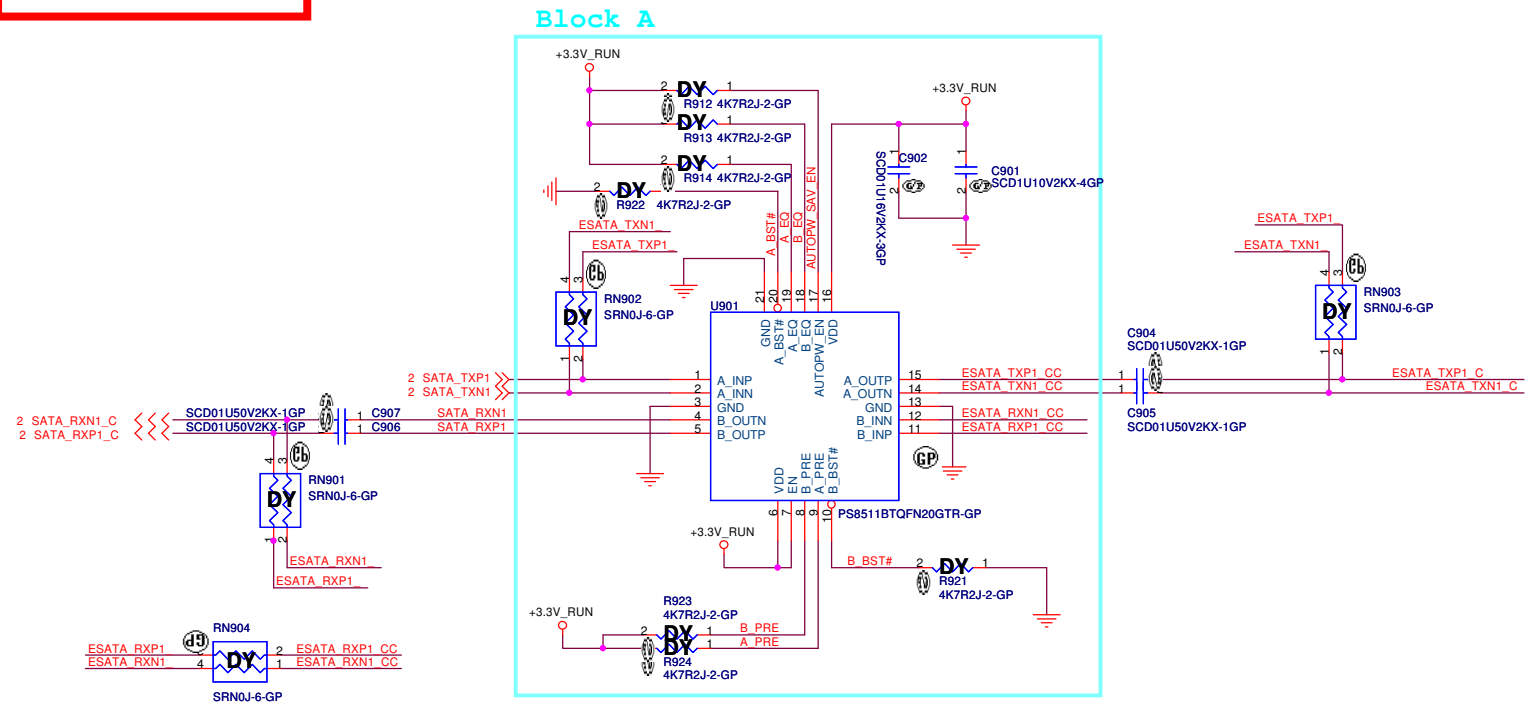
Berry IO Board

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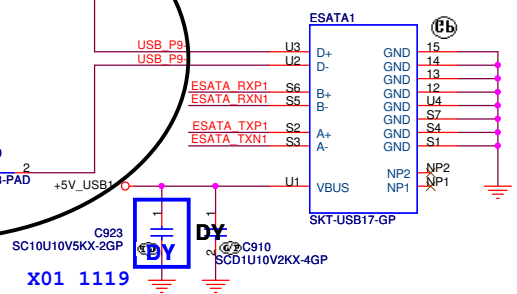
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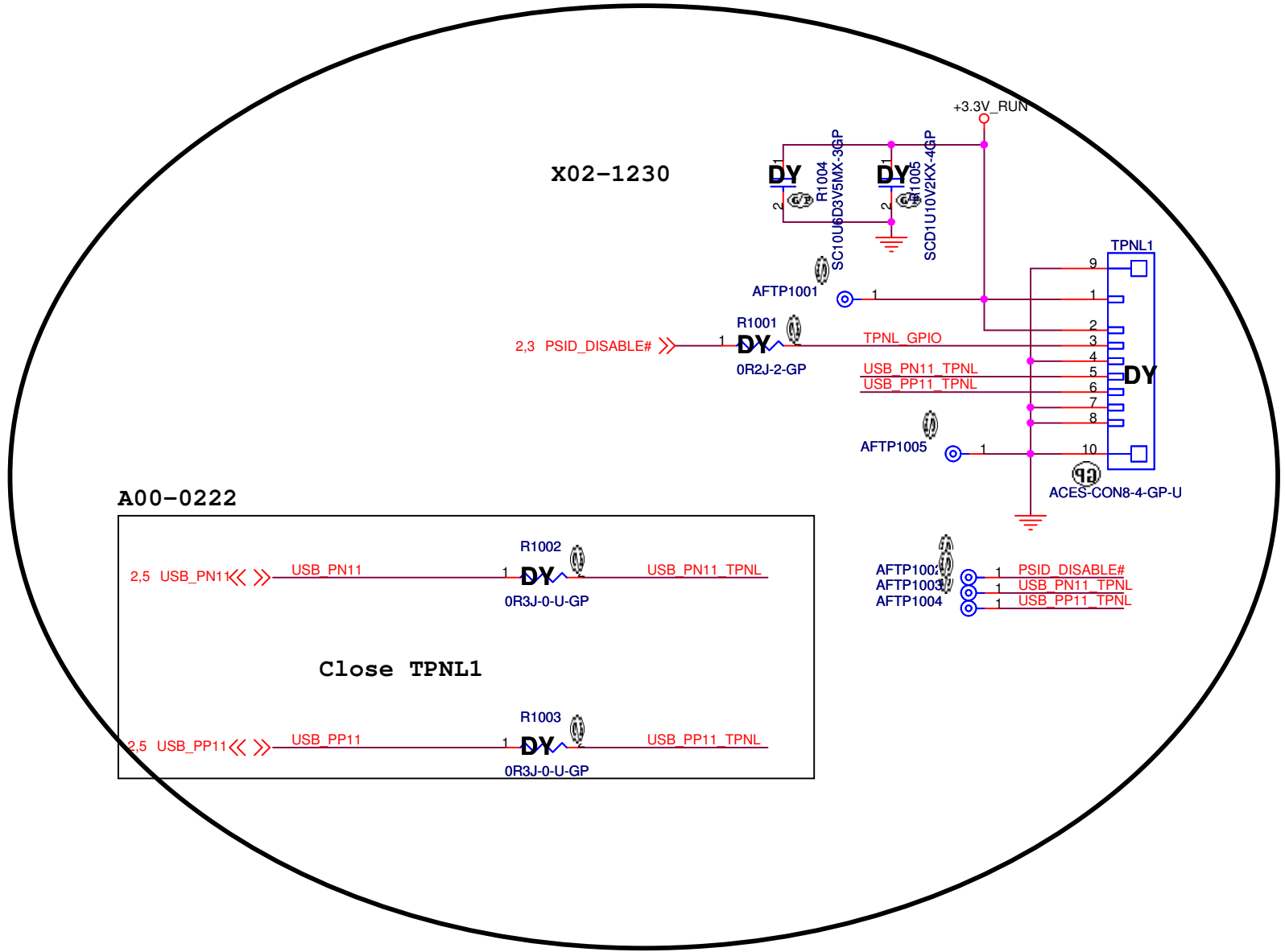
SSID = ESATA



ESATA CONN

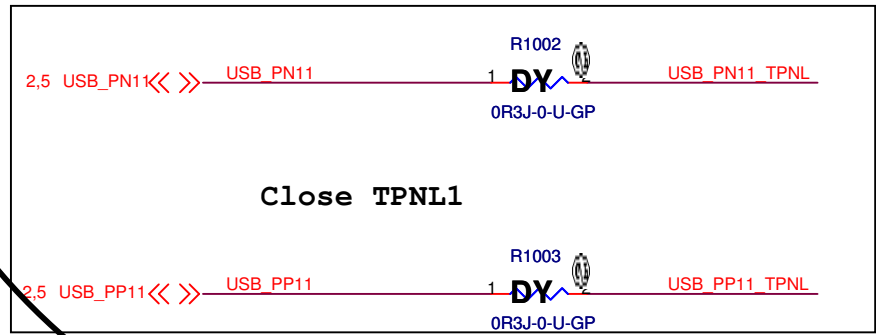


close to ESATA1



X02-1230

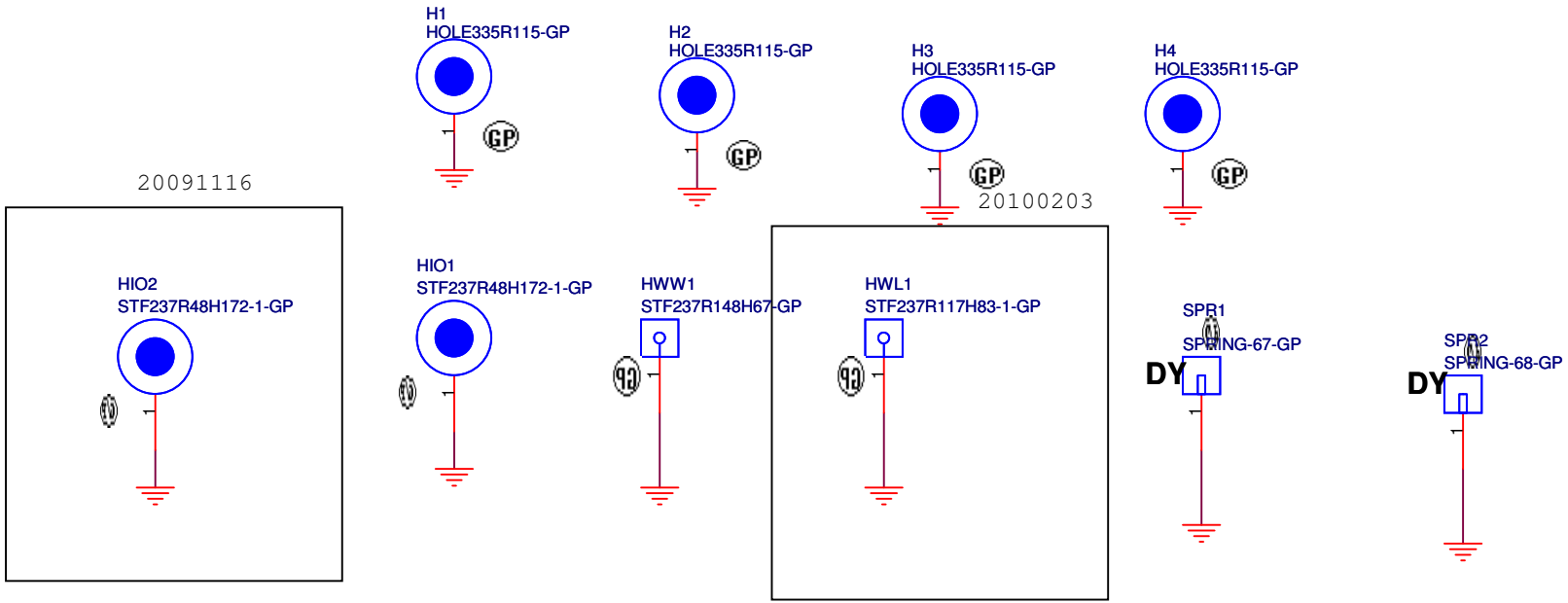
A00-0222



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Title		
Touch Panel Conn		
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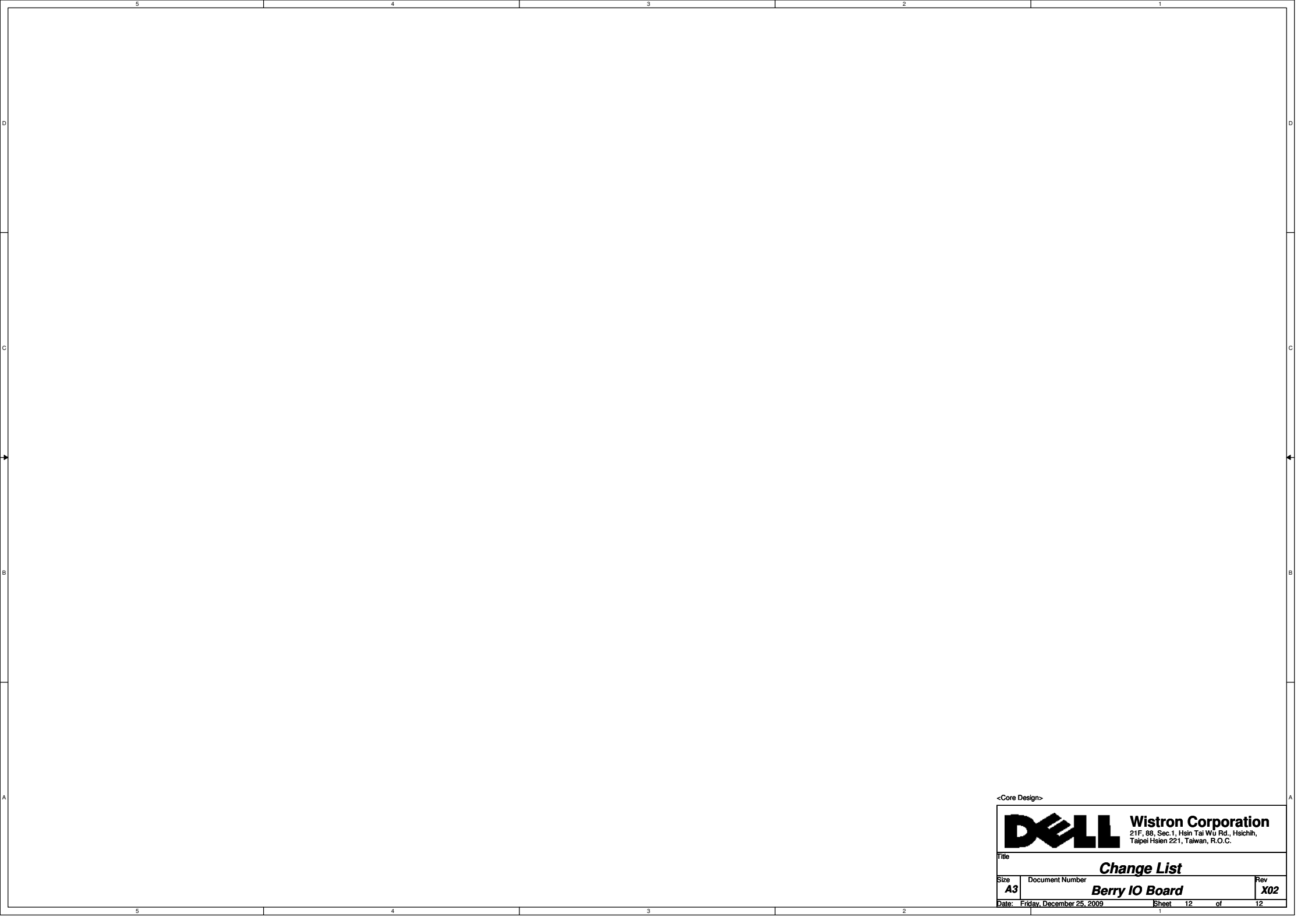


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Title **RESERVED**

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Change List		
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