V02A/R01A DIS BLOCK DIAGRAM

PCB STACK UP

8L DIS

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT

DDRIII-SODIMM1 (H=4mm) PAGE 16 — DDRIII 1333 MT/s

DDRIII-SODIMM2 (H=8mm) PAGE 17 — DDRIII 1333 MT/s

CPU
Sandy Bridge 35W
PGA 988
PAGE 4~8

PCIEx16

ATI
Robson XT(64bit)
Seymour XT (64bit)
Whistler LP (128bit)
29mm X 29mm
BGA 969
PAGE 18~22

DDR3 2GB
128Mx16bitx8
PG 23,24

FDI LINK 2.5GT /s

DMI LINK 2.5GT /s

INT HDMI — LEVEL SHIFTER PAGE 27 — HDMI CONN PAGE 27

INT CRT — CRT Board PAGE 26

INT Single CHANNEL LVDS — LCD CONN 1366 x 768 (HD) PAGE 25

iGFX Interfaces

E-SATA PAGE 28 — SATA4 3G /S

SATA -HDD PAGE 31 — SATA0 6G /S

ODD PAGE 36 — SATA1 6G /S

3-axis Fall Sensor PAGE 31 — SMBUS

Mobile Intel Series 6 Chipset

PCH

HM67
Couger Point

BGA 989
25 mm X 25 mm

PAGE 9~15

ESATA+USB2.0 PAGE 35 — USB[0]

USB Port x1 PAGE 29 — USB[2]

USB2.0

USB[11] — Camera PAGE 30

USB[8] — Card Reader RTL5128-GR PAGE 30

USB[4] — WLAN PAGE 34 — PCIE[1]

USB[5] — WWAN PAGE 35 — PCIE[2]

PCI-E

PCIE[5] — LAN Realtek RTL8111EL PAGE 39 — 25MHz

PCIE[3] — USB3.0 Controller PAGE 36 — USB3.0 Ports x2 PAGE 37

IHDA

IHDA — RJ45 PAGE 39

IO Board PAGE 33

Audio Codec ALC 269 PAGE 38

Speaker MB Side PAGE 38

Jack X2 PAGE 38

Digital-MIC PAGE 38

Keyboard Conn. PAGE 42

Touch Pad PAGE 42

KBC ITE 8518 PAGE 32 — LPC

PWM FAN &Thermal PAGE 45

SPI ROM 512KB PAGE 41

SPI

SPI ROM 4MB PAGE 41

25MHz

32.768KHz

Charger PAGE 49

3/5V PAGE 50

1.5V_SUS/0.75V_DDR PAGE 51

1.8V_RUN PAGE 52

1.05V_VTT/PCH PAGE 53

VCCSA PAGE 54

DGFX_CORE PAGE 55

CPU_CORE PAGE 56

Quanta Computer Inc.
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	BLOCK DIAGRAM	1A

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power / State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	Power Rails	1A

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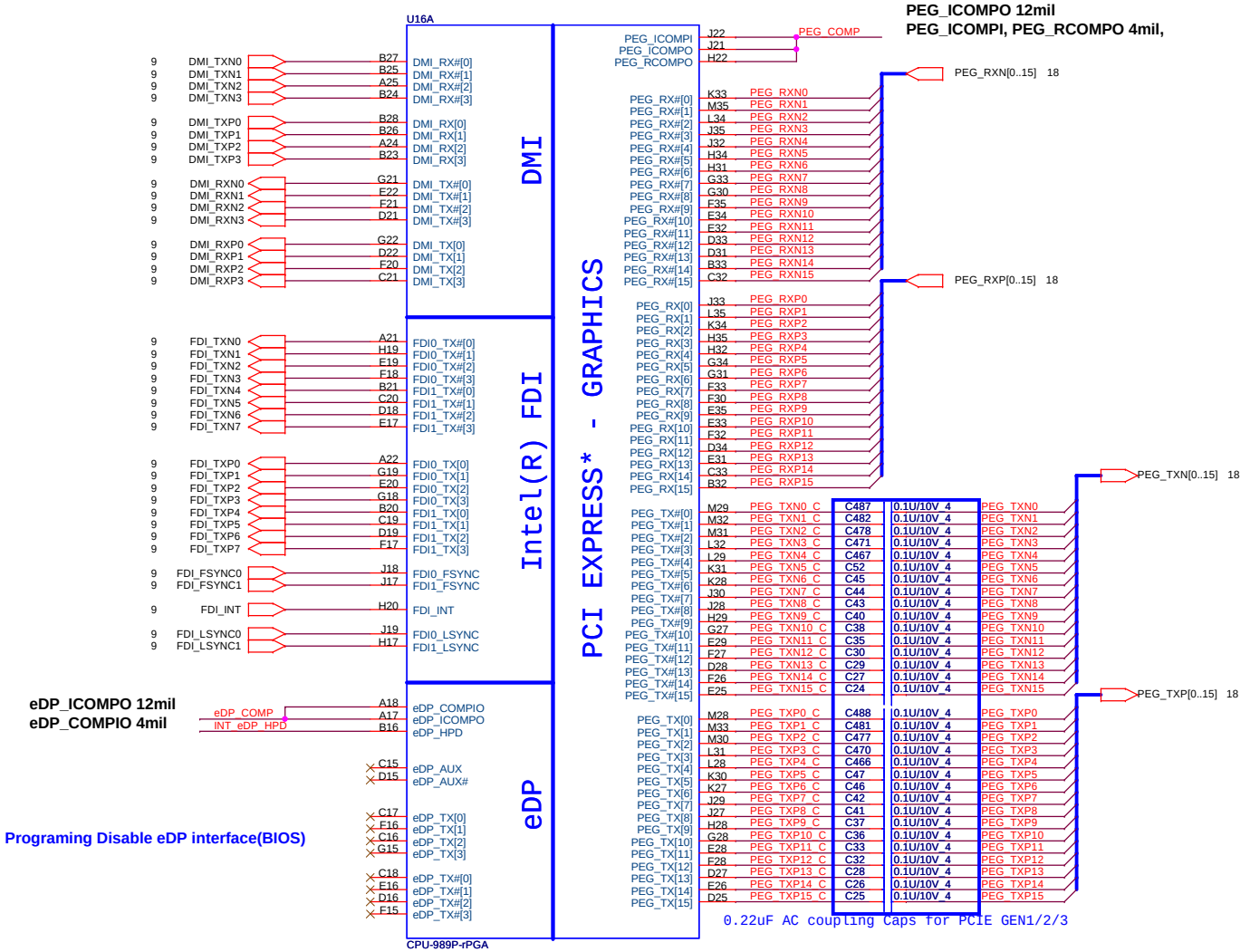
Quanta Computer Inc.

PROJECT : V02A/R01A

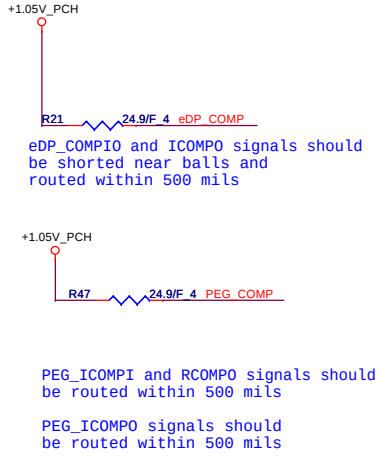
Size	Document Number	Rev
	BLANK	1A

Date: Wednesday, January 19, 2011 Sheet 3 of 61

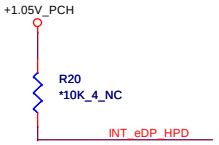
Sandy Bridge Processor (DMI,PEG,FDI)



DP & PEG Compensation



eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

Quanta Computer Inc.			
PROJECT : V02A/R01A			
Size	Document Number: Sandy Bridge 1/5		Rev: 1A
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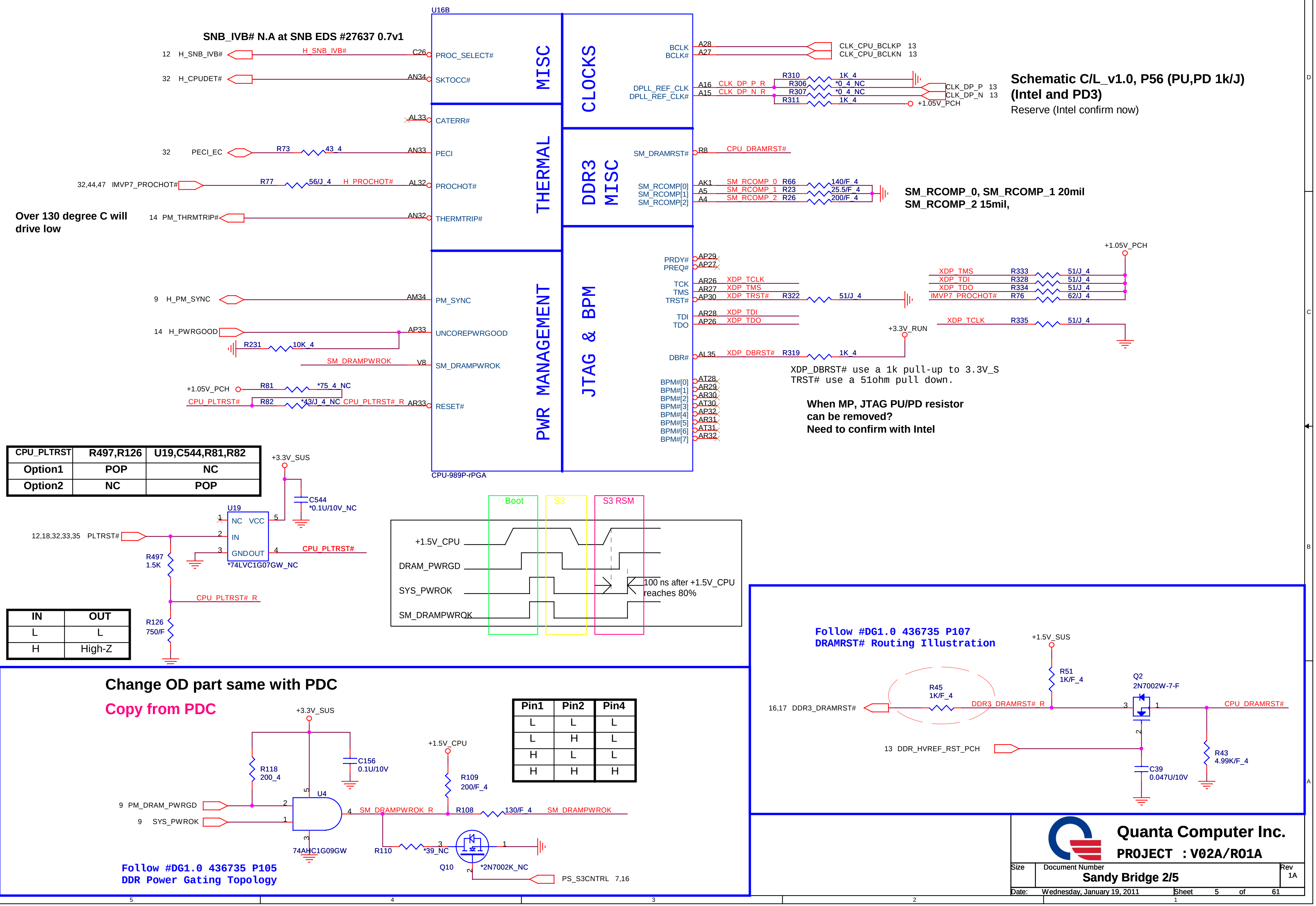
Sandy Bridge Processor (CLK,MISC,JTAG)


U16B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
CPU-989P-rPGA
PROC_SELECT#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
12 H_SNB_IVB#
32 H_CPUDET#
32 PECI_EC
32,44,47 IMVP7_PROCHOT#
14 PM_THRMTRIP#
9 H_PM_SYNC
14 H_PWRGOOD
CLK_CPU_BCLKP 13
CLK_CPU_BCLKN 13
CLK_DP_P 13
CLK_DP_N 13
+1.05V_PCH
CPU_DRAMRST#
+3.3V_RUN
+3.3V_SUS
12,18,32,33,35 PLTRST#
U19
*74LVC1G07GW_NC
C544 *0.1U/10V_NC
R497 1.5K
R126 750/F
CPU_PLTRST#
CPU_PLTRST#_R
Boot
S3
S3 RSM
+1.5V_CPU
DRAM_PWRGD
SYS_PWROK
SM_DRAMPWROK
100 ns after +1.5V_CPU reaches 80%
16,17 DDR3_DRAMRST#
13 DDR_HVREF_RST_PCH
R45 1K/F_4
R51 1K/F_4
Q2 2N7002W-7-F
R43 4.99K/F_4
C39 0.047U/10V
9 PM_DRAM_PWRGD
9 SYS_PWROK
U4 74AHC1G09GW
R118 200_4
C156 0.1U/10V
R109 200/F_4
R108 130/F_4
R110 *39_NC
Q10 *2N7002K_NC
PS_S3CNTRL 7,16

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Over 130 degree C will drive low

Schematic C/L_v1.0, P56 (PU,PD 1k/J) (Intel and PD3)

Reserve (Intel confirm now)

SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor can be removed?
Need to confirm with Intel

CPU_PLTRST	R497,R126	U19,C544,R81,R82
Option1	POP	NC
Option2	NC	POP

IN	OUT
L	L
H	High-Z

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration

Change OD part same with PDC

Copy from PDC

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	H

Follow #DG1.0 436735 P105
DDR Power Gating Topology

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PROJECT : V02A/R01A

Size | Document Number: Sandy Bridge 2/5 | Rev 1A

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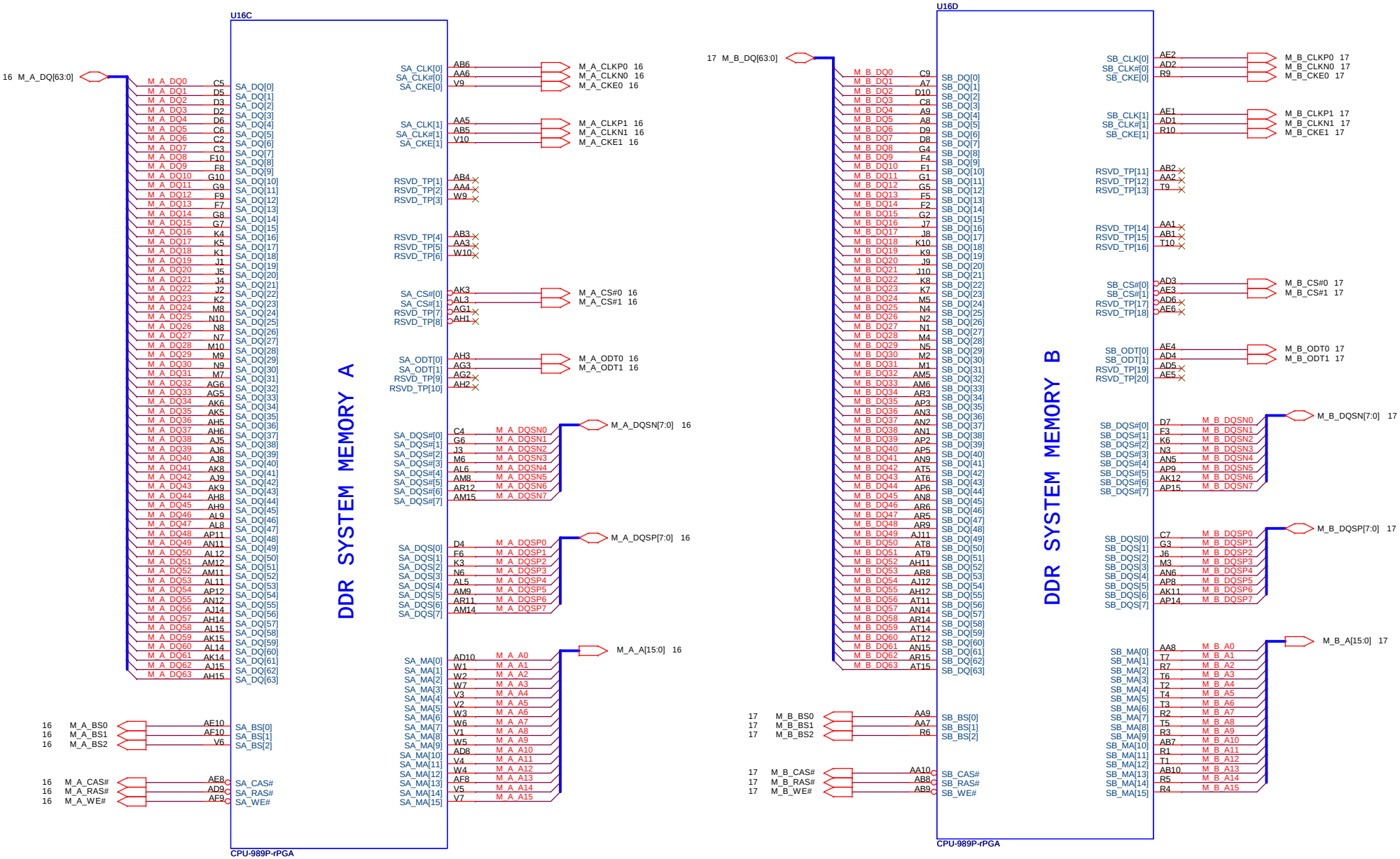
Sandy Bridge Processor (DDR3)



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PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 3/5	1A
Date: Wednesday, January 19, 2011	Sheet 6 of 61	

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

POWER

CPU Core Power
SNB 35W:55A
10uF x 24

CPU VTT
SNB 35W:8.5A
10F x12

CPU VGT
SNB 35W:22A
10uF x 12

CPU MCH
SNB 35W: 5A
10uF x 6

CPU SA
SNB35W: 6A
10uF x 3

CPU VCCPL
SNB 35W:3A
10uF x 1
1uF x 2

CPU-989P-rPGA

CORE SUPPLY
PEG AND DDR
SVID
SENSE LINES
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
SENSE LINES
VREF
MISC

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

S3 Power reduce

Q3 FDMS7670 10A
Q7 2N7002W-7-F
Q6 2N7002W-7-F
Q4 *2N7002W-7-F_NC
Q5 *2N7002W-7-F_NC

Take care Q3509 Vgs(MAX)=2.5

Change R8281,R8285, R8704,R8329 to +/-5%
54.9 ohm has no 5%

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK — Close to VR — R89 54.9/F_4 — R90
Place PU resistor close to CPU — R96 130_4 — R97
SVID DATA — Close to VR — R101 130_4
Place PU resistor close to CPU — R93 75_4 — R94 43_4
SVID ALERT

Quanta Computer Inc.
PROJECT :V02A/R01A

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	Sandy Bridge 4/5	1A
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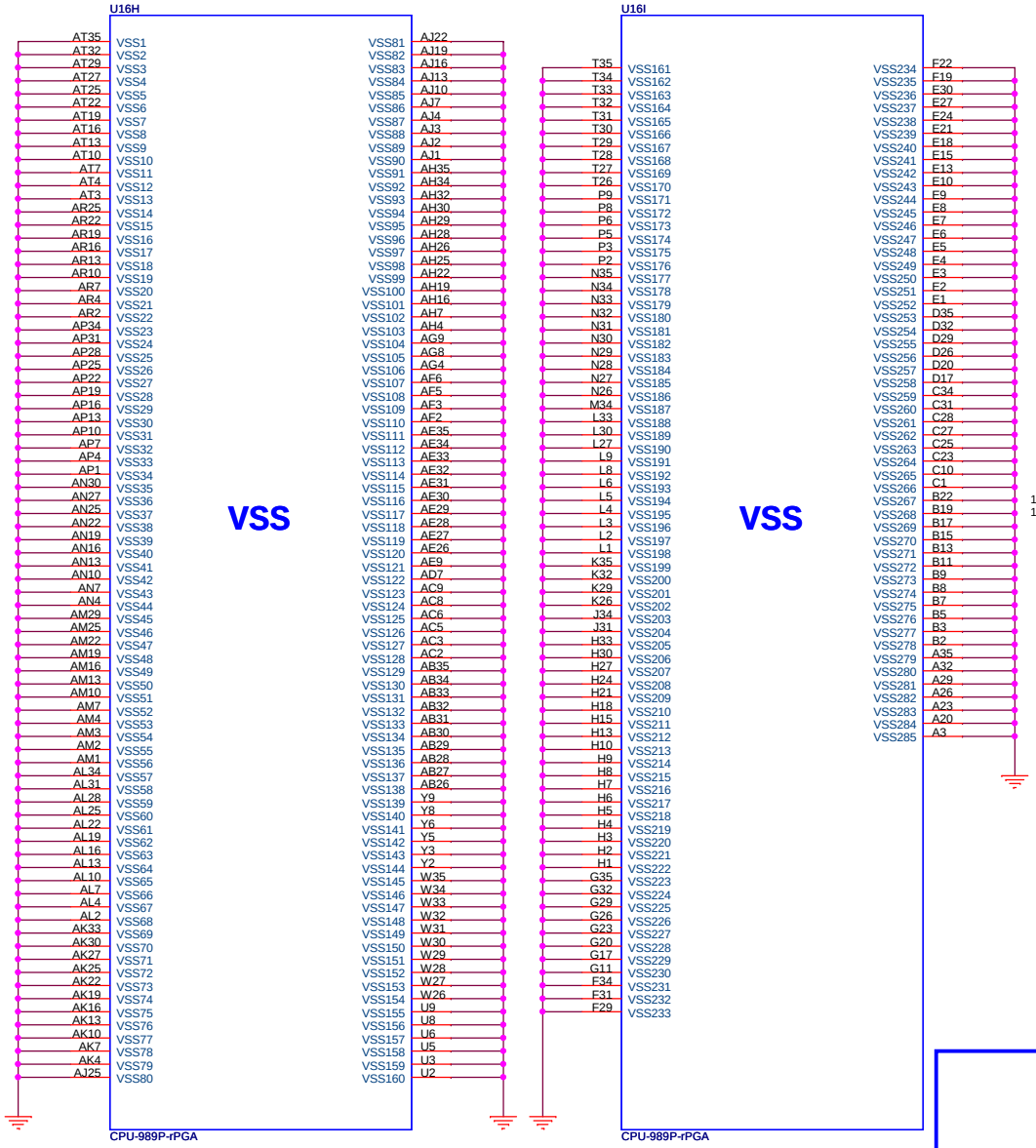
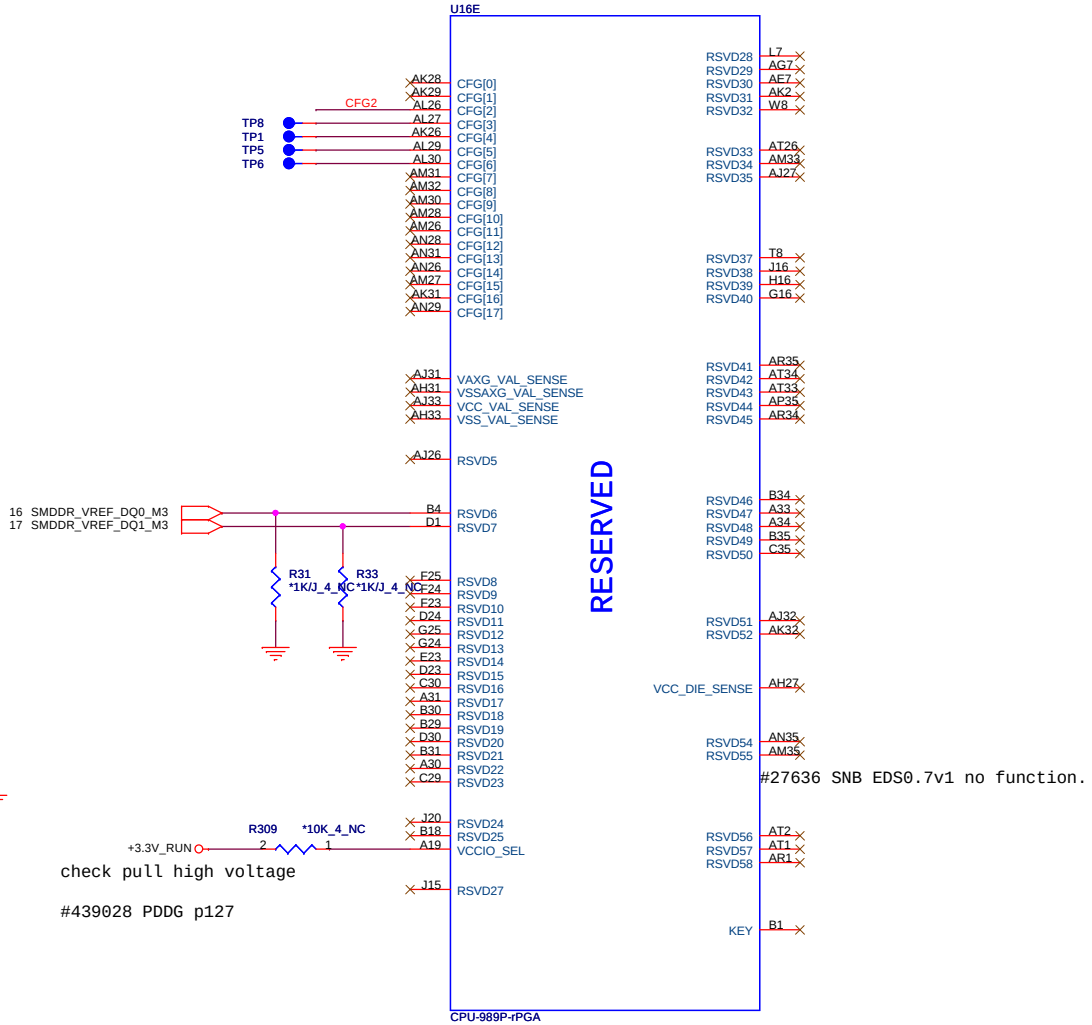
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



For rPGA socket, RSVD59 pin should be left NC

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R106 1K/F_4

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 5/5	1A
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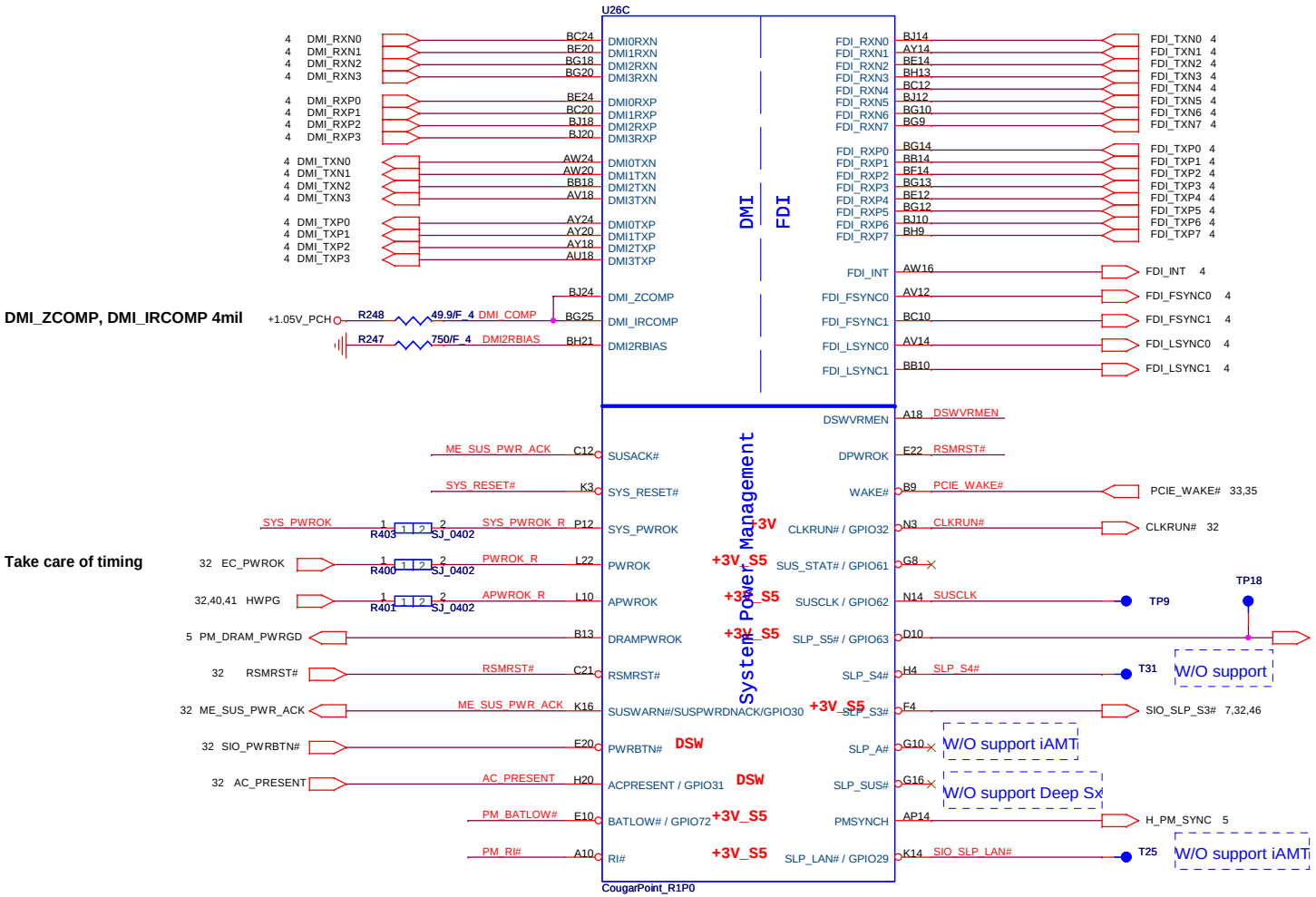
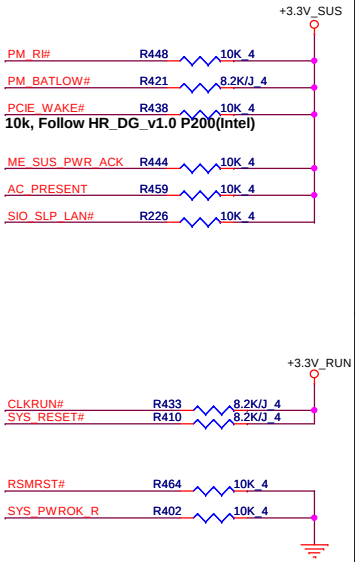
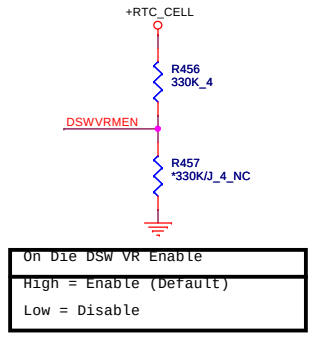
Cougar Point (DMI,FDI,PM)

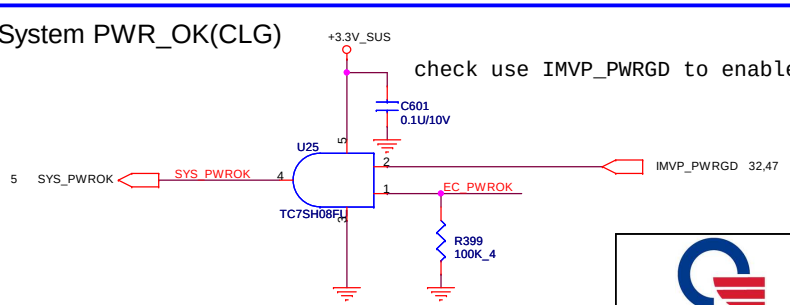


PCH Pull-high/low(CLG)





System PWR_OK(CLG)



Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: Cougar Point 1/7	Rev: 1A
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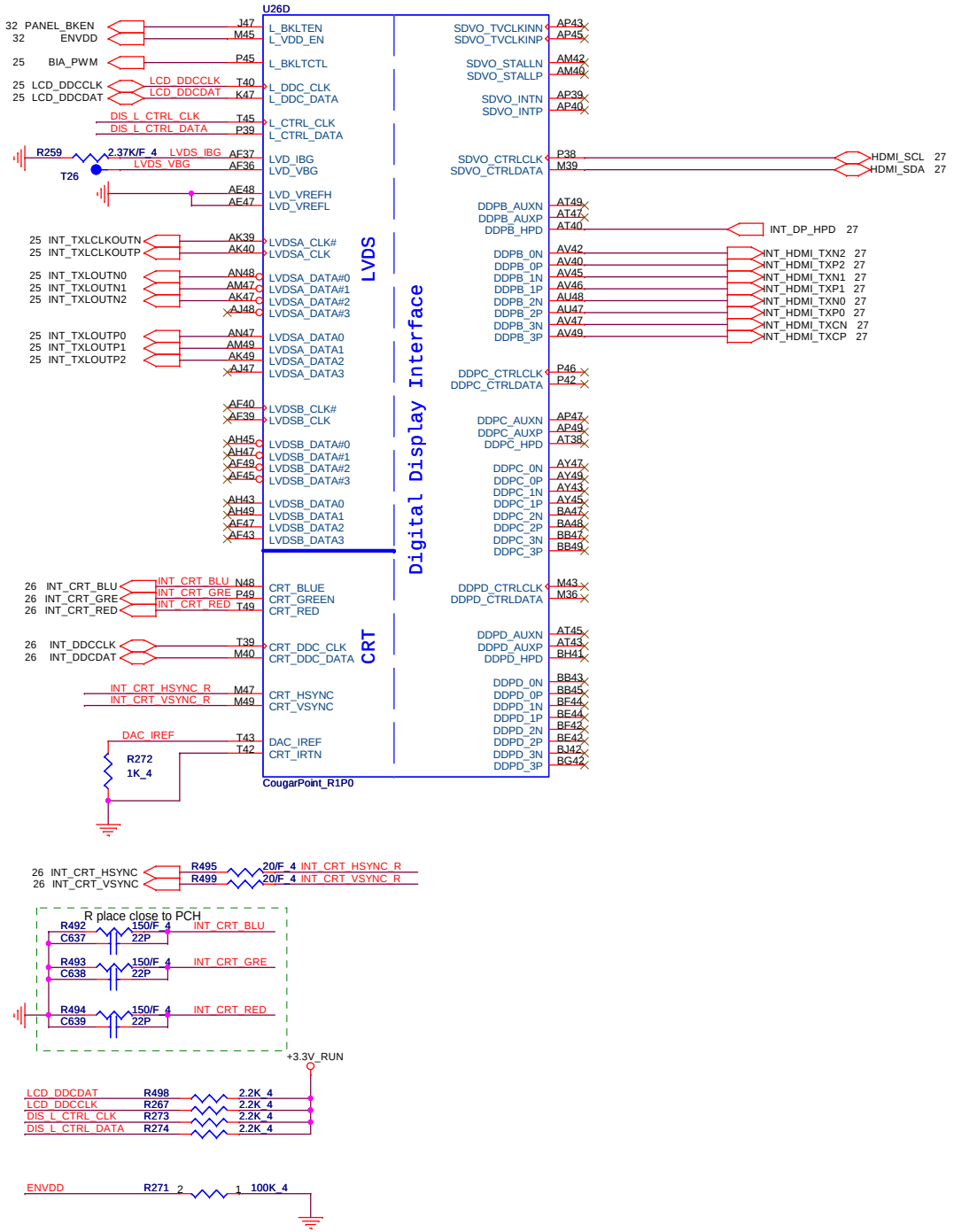
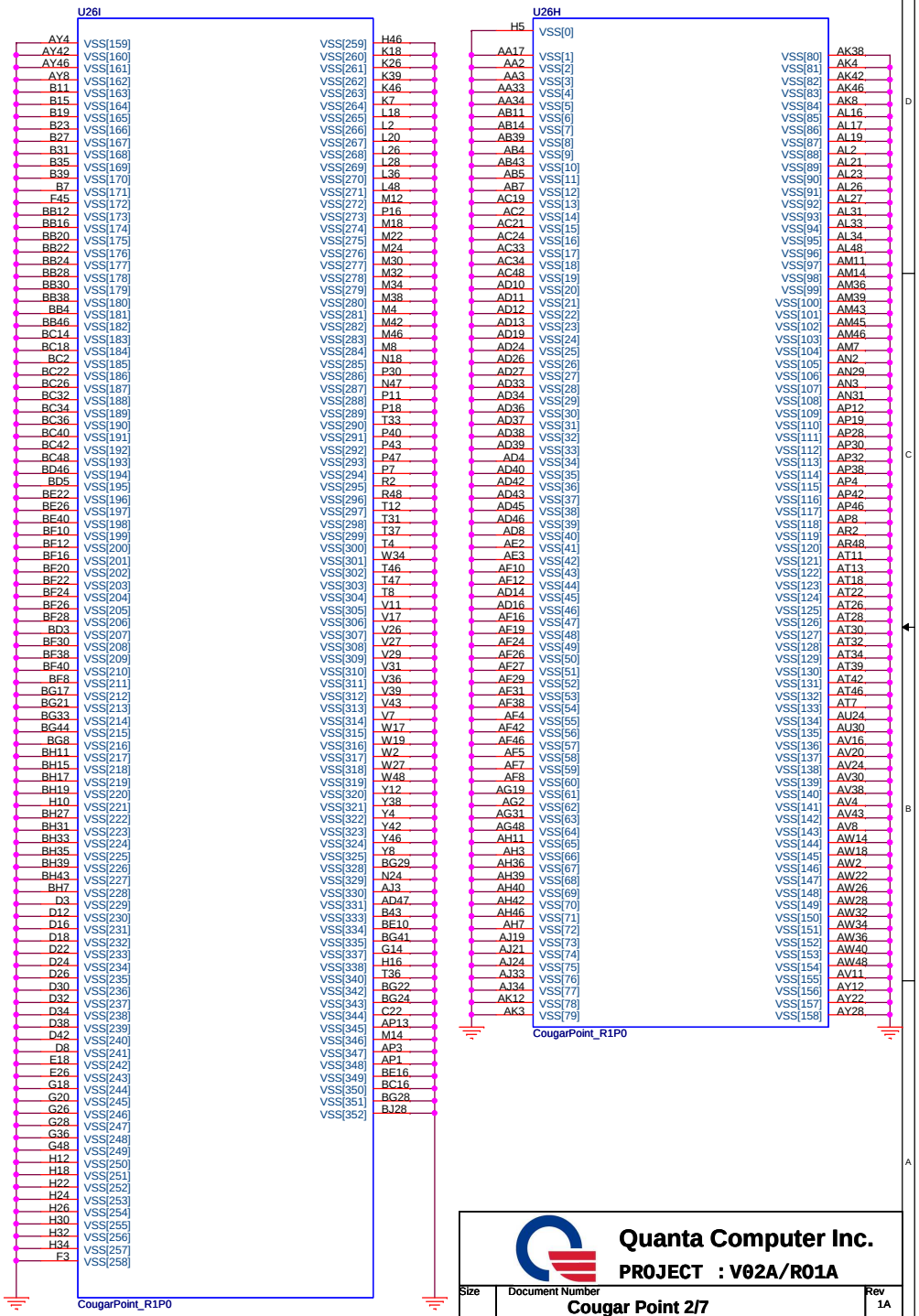
Cougar Point (LVDS,DDI)



Cougar Point (GND)



Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 2/7	1A

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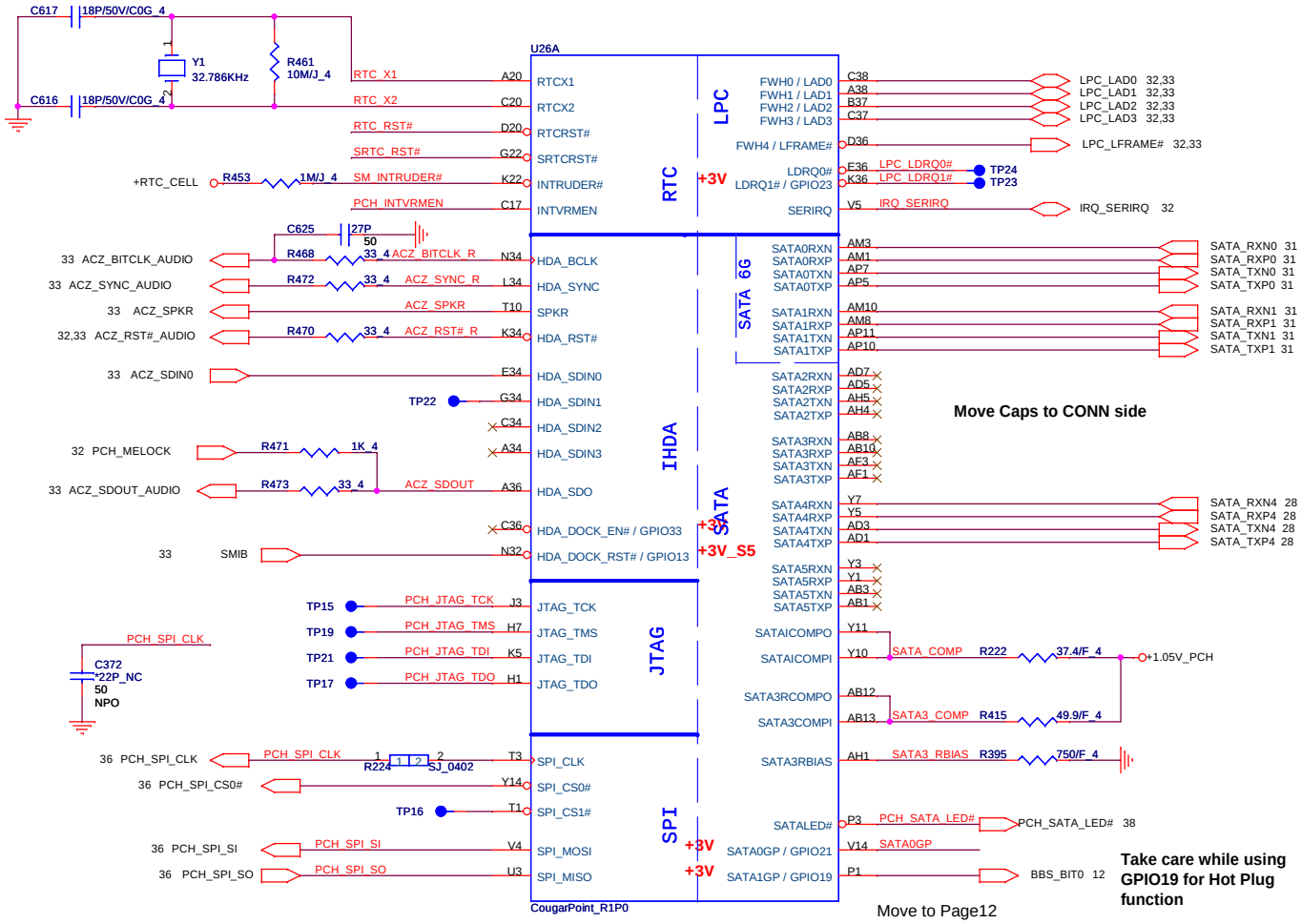
Cougar Point (HDA,JTAG,SATA)



SATA HDD/SSD

SATA ODD

ESATA

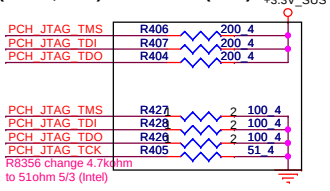
Move Caps to CONN side

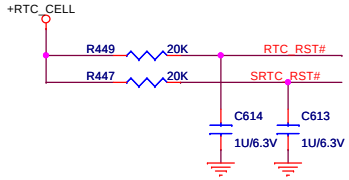
Take care while using GPIO19 for Hot Plug function

Move to Page12

PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)





PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS R413 *1K_4_NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R474 *1K_4_NC ACZ_SDOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R455 330K_4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R469 1K_4 ACZ_SYNC_R

Quanta Computer Inc.
PROJECT : V02A/R01A

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	Cougar Point 3/7	1A

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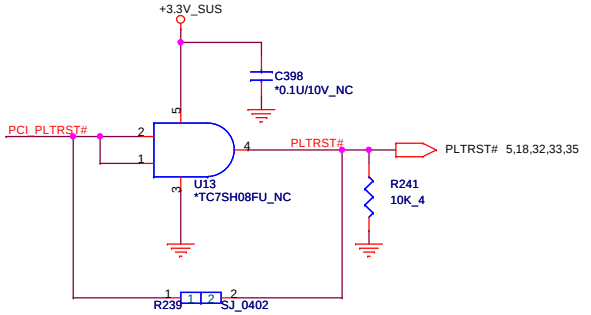
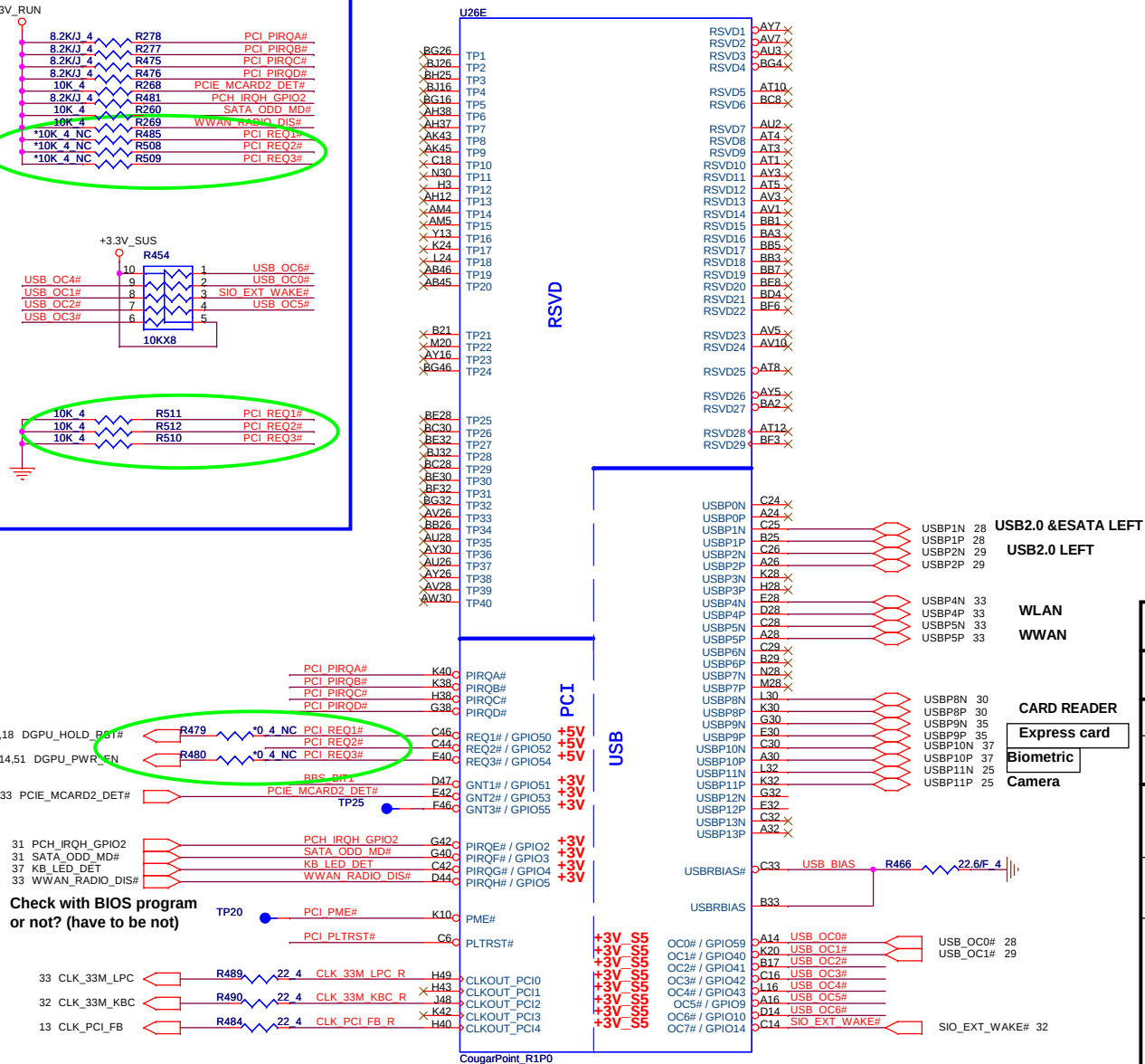
Cougar Point-M (PCI,USB,NVRAM)

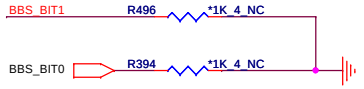
PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

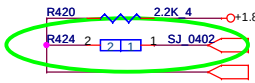




Pin Name	Strap description	Sampled	Configuration
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Bit 0 / Bit 1 / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm



Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]



CheckList_1.0 p58; HR_v1.0 p450

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 4/7	1A
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Cougar Point-M (PCI-E,SMBUS,CLK)

U26B

WLAN
WWAN
USB 3.0
LAN
Express card
Card reader
XDP

PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS

CougarPoint_R1P0

	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 /GPIO64	• 33 /27 /48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 /GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 /GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 /GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 5/7	1A
Date: Wednesday, January 19, 2011	Sheet 13 of 61	

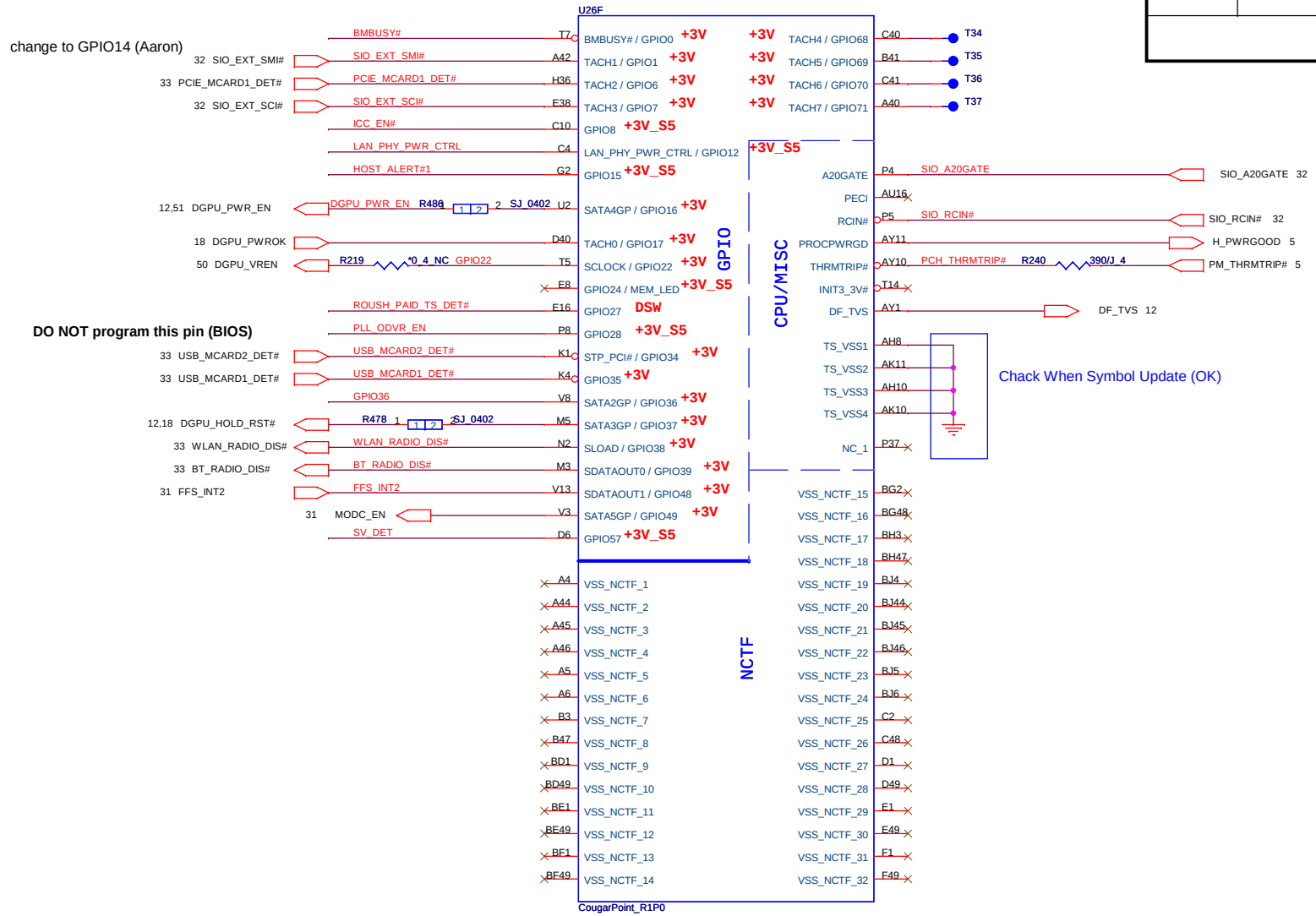
Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

R214 *1K_4_NC PLL_ODVR_EN

change to GPIO14 (Aaron)

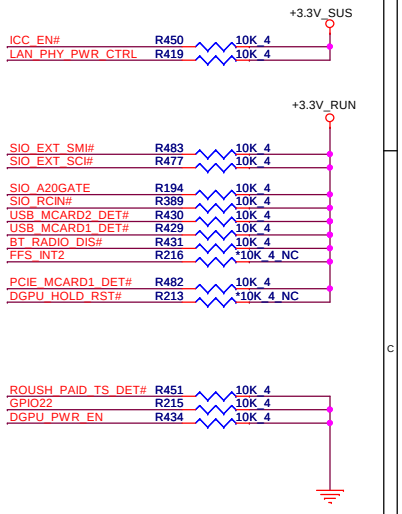
DO NOT program this pin (BIOS)



Chack When Symbol Update (OK)

Add Description in EC GPIO table (keyboard controller reset)

GPIO Pull-up/Pull-down(CLG)



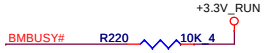
Can be del

Have to Reserve

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO Confirm with Intel



BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

MFG-TEST

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 6/7	1A
Date: Wednesday, January 19, 2011	Sheet 14 of 61	

COUGAR POINT (POWER)

Cougar Point (POWER)

VccCORE =1.14A(50mils)

need 1206?

+1.05V_PCH_VCC

VccADAC =1mA(8mils)

Cost Down Point

Tie to 3.3V_SUS, when don't support Deep SX CP_v1.0 p88

VccDSW3_3= 3mA(8mil)

VccALVDS=1mA (8mils)

+VCCALVDS

VccTX_LVDS=60mA (10mils)

+1.05V_PCH_VCCDPLL_EXP

VccIO =2.925 A(120mils)

+1.05V_VCCIO

walt over limit change PD3 use

Vcc3_3 = 0.266A (15mils)

+3V_VCC_GIO

VccASW =1.01A (50mils)

VccDMI = 80mA (20mils)

+1.1V_VCC_DMI_CCI

VccCLKDMI = 20mA (8mils)

+3V_VCC_EXP

VccVRM(1.5V) =0.16 A(10mils)

VccDMI =0.042 A(10mils)

+VCCP_NAND

VCCPNAND = 190 mA(15mils)

+3V_VCCME_SPI

VCCSPI = 20mA(8mils)

Intel

80mA(10mils)

80mA(10mils)

VCCDIFFCLKN= 55mA(10mils)

VCCSSC= 95mA(10mils)

1mA(8mils)

VCCRTC<1mA(8mils)

VCCRTC =1.8V (Destop) 07/20 del for Pre-ES1
1.5V (Mobile)

Ask PD3, Why leave so many 0 ohm for VCCIO?

11

11

Ask PD3 or Intel, why need 1ohm change to +/-5%

Change size to 0603

+1.05V_VCCUSBCORE

VCCSUS3_3 = 119mA (15mils)

VCC5REFSUS=1mA(8mil)

V5REF= 1mA(8mil)

VCCSUS3_3 = 119mA (15mils)

VCCPCORE = 28mA(10mils)

VCCVRM= 114mA(15mils)

VCCSUSHDA= 10mA(8mils)

POWER

VCC CORE | CRT | LVDS | HVCMOS | VCCIO | DMI | DFT / SPI | FDI

USB | Clock and Miscellaneous | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

CougarPoint_R1P0

Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: Cougar Point 7/7	Rev: 1A
Date: Friday, January 21, 2011	Sheet 15 of 61	

H=8mm,RVS

SO-DIMMA_SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
Still Support?

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

S3 Power reduce

M1 VREF

Place these Caps near So-Dimm0.

Some Projects replace 10UF 0805 by 4.7UF 0603 11/6

It can cost down 30%

For RF noise

For RF noise

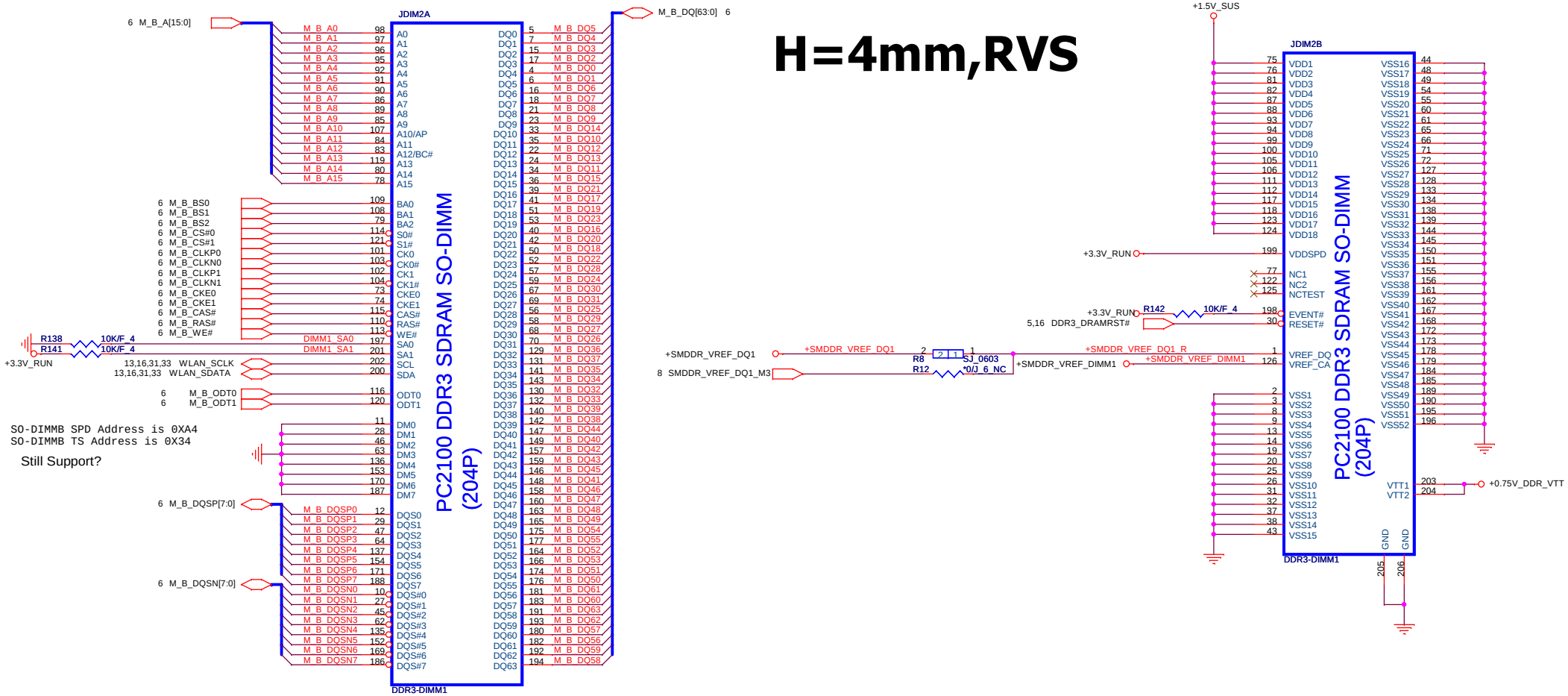
Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	DDR3 DIMM-0	1A

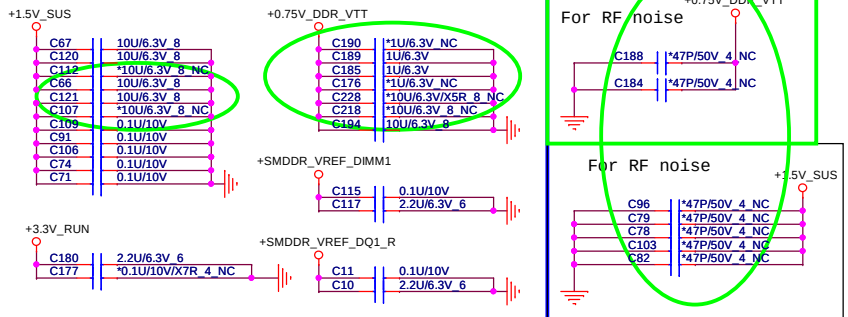
Date: Wednesday, January 19, 2011 Sheet 16 of 61

H=4mm,RVS

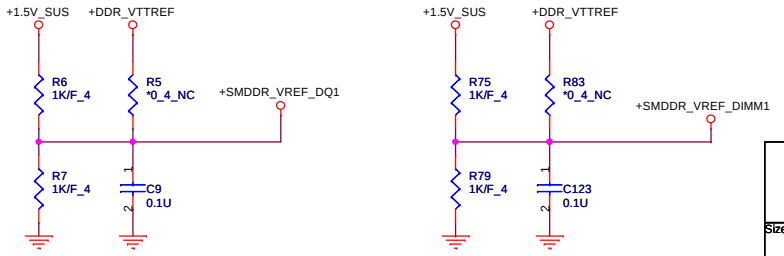


Place these Caps near So-Dimm1.

Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%

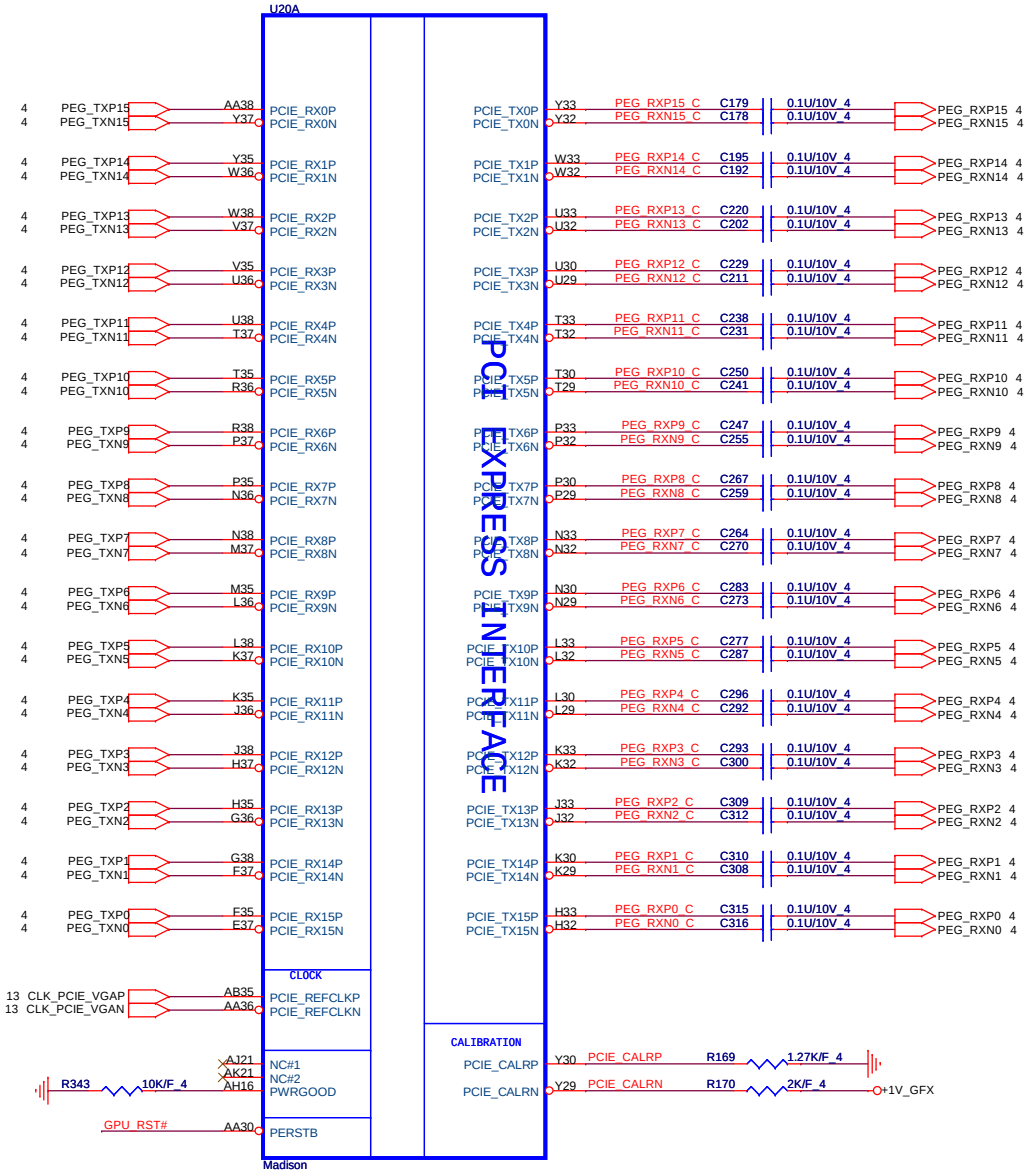


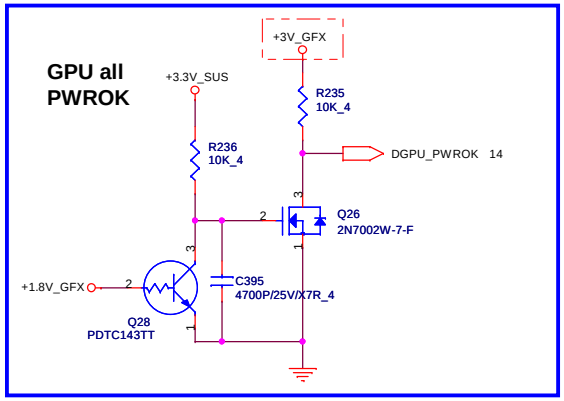
M1 VREF

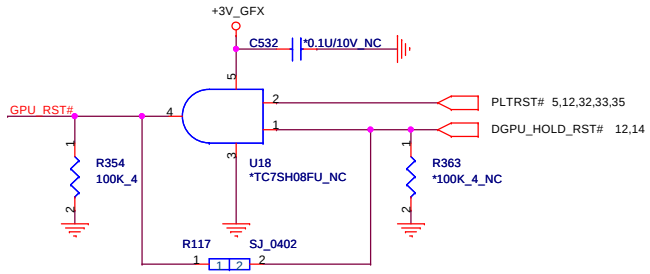


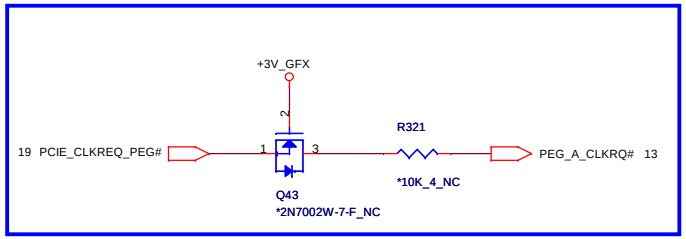
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	DDR3 DIMM-1	1A
Date: Wednesday, January 19, 2011	Sheet 17 of 61	









Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	N11M-GE2 (PCIE I/F) 1/5	1A

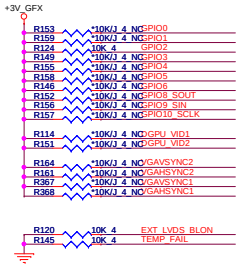
Date: Wednesday, January 19, 2011 Sheet 18 of 61

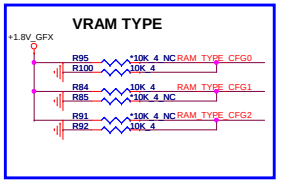
CONFIGURATION STRAPS

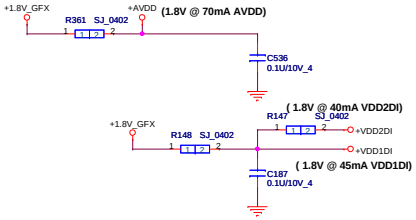
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

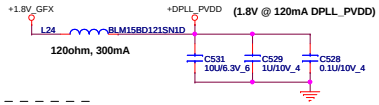
APERTURE SIZE

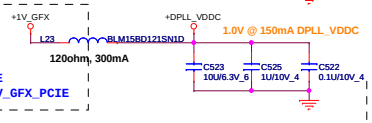
MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0



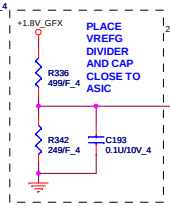


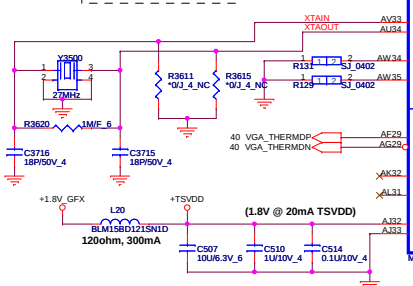


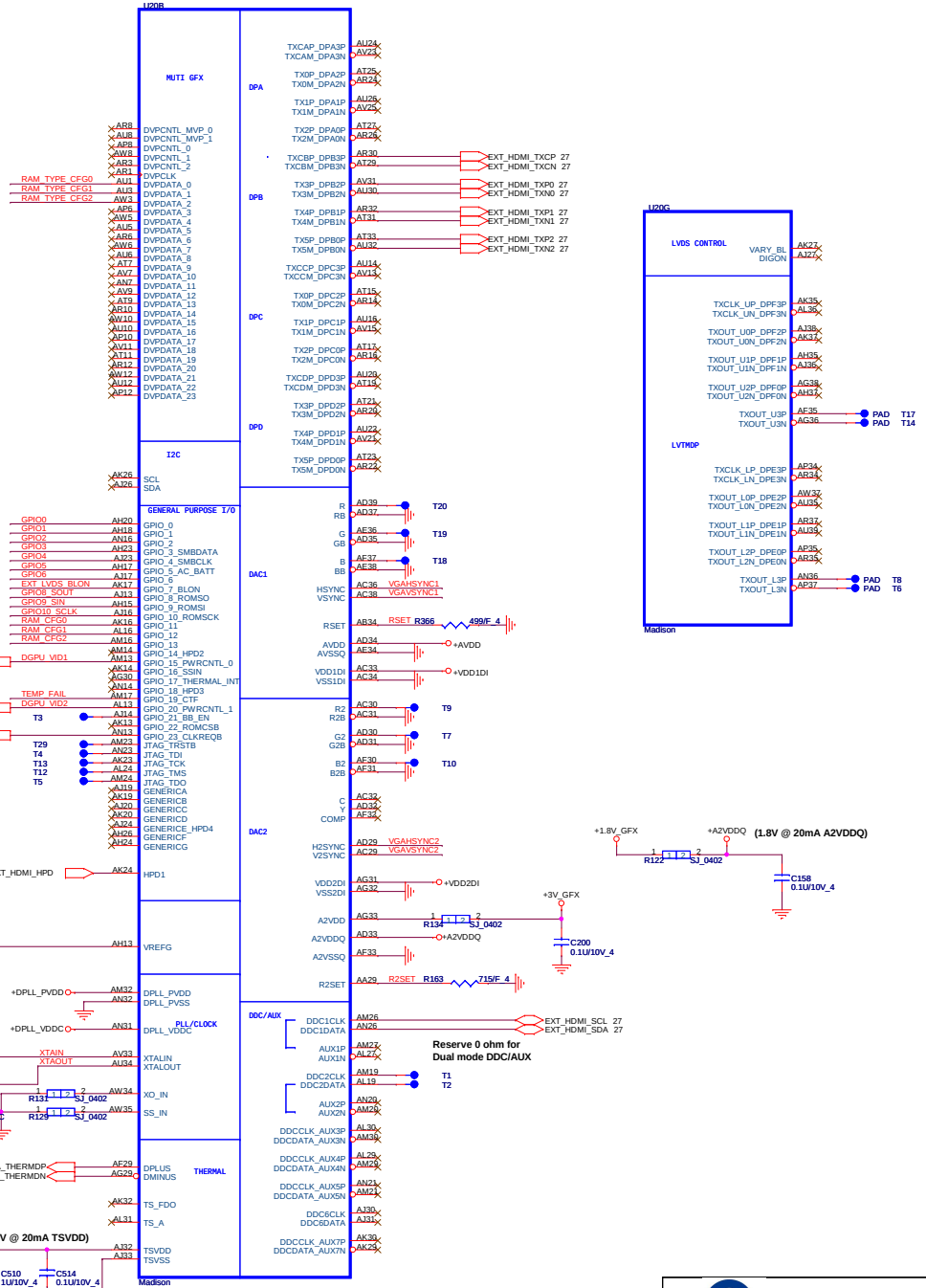




M96 => +1.1V_GFX_PCIE
Park, Madison=> +1.0V_GFX_PCIE



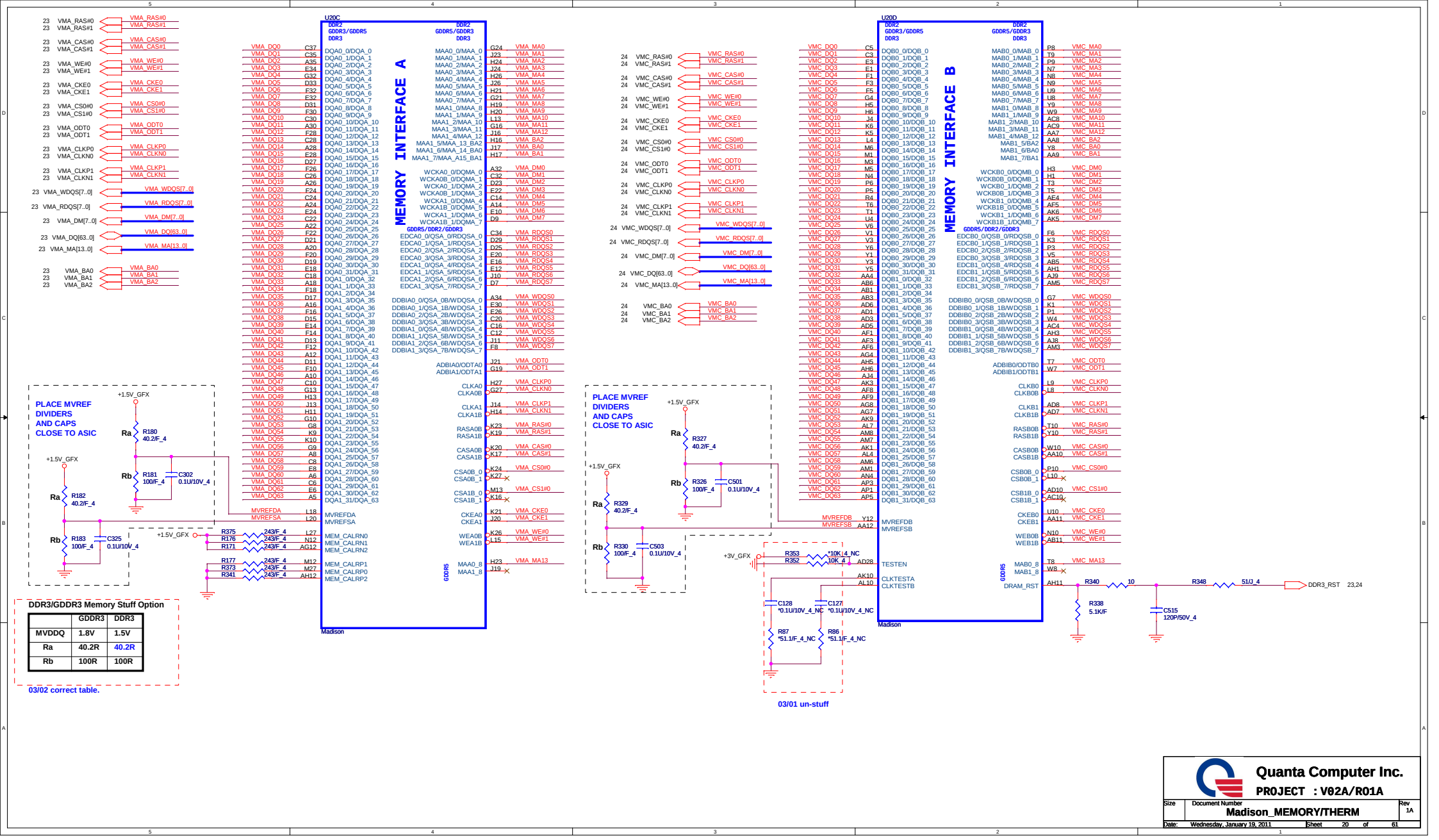




Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(128M*16*4pcs)	0	0	1	AKD5MGWT507	K4W2G1646C-HC11	For Robson XT (Only Channel B)
900MHz Hynix 1GB(128M*16*4pcs)	0	1	0	AKD5MGWTW06	H5TQ2G63BFR-11C	For Robson XT (Only Channel B)

Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5LGHT505	K4W1G1646E-HC11	For Whisler-LP
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZWTW07	H5TQ1G63DFR-11C	For Whisler-LP
900MHz Samsung 1GB(64M*16*8pcs)	1	0	0	AKD5EGGT500	K4W1G1646G-BC11	For Whisler-LP

Quanta Computer Inc.
PROJECT : V02A/R01A
Size | Document Number: Madison_IO&STRAP | Rev 1A
Date: Wednesday, January 19, 2011 | Sheet 19 of 61



	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Madison_MEMORY/THERM	1A

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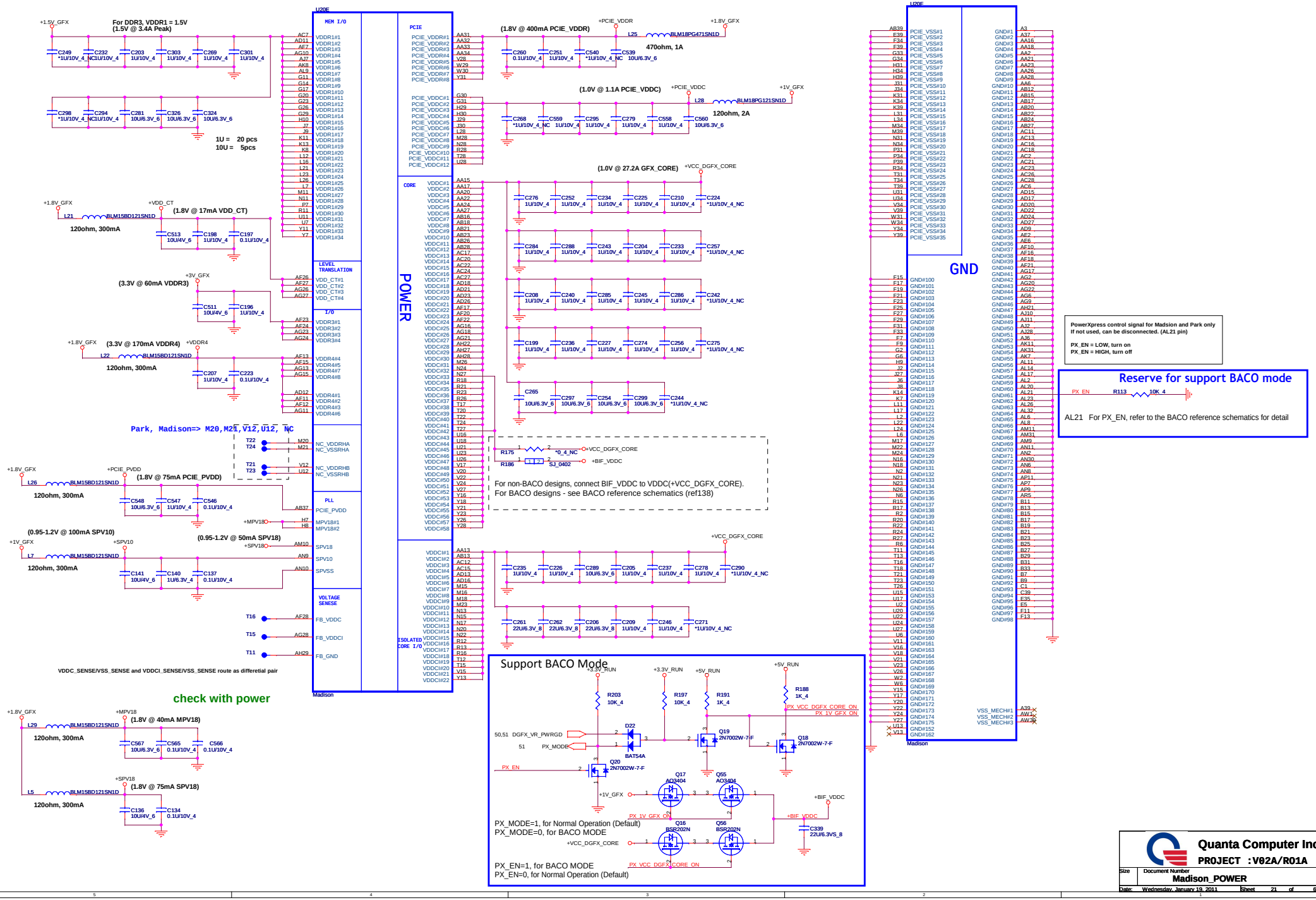
U20E
POWER
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
ISOLATED CORE I/O
For DDR3, VDDR1 = 1.5V
(1.5V @ 3.4A Peak)
1U = 20 pcs
10U = 5pcs
(1.8V @ 17mA VDD_CT)
120ohm, 300mA
(3.3V @ 60mA VDDR3)
(3.3V @ 170mA VDDR4)
Park, Madison=> M20,M21,V12,U12, NC
(1.8V @ 75mA PCIE_PVDD)
(0.95-1.2V @ 100mA SPV10)
(0.95-1.2V @ 50mA SPV18)
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
check with power
(1.8V @ 40mA MPV18)
(1.8V @ 75mA SPV18)
(1.8V @ 400mA PCIE_VDDR)
470ohm, 1A
(1.0V @ 1.1A PCIE_VDDC)
120ohm, 2A
(1.0V @ 27.2A GFX_CORE)
For non-BACO designs, connect BIF_VDDC to VDDC(+VCC_DGFX_CORE).
For BACO designs - see BACO reference schematics (ref138)
Support BACO Mode
PX_MODE=1, for Normal Operation (Default)
PX_MODE=0, for BACO MODE
PX_EN=1, for BACO MODE
PX_EN=0, for Normal Operation (Default)
GND
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected. (AL21 pin)
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
Reserve for support BACO mode
AL21 For PX_EN, refer to the BACO reference schematics for detail
Quanta Computer Inc.
PROJECT : V02A/R01A
Madison_POWER
Wednesday, January 19, 2011
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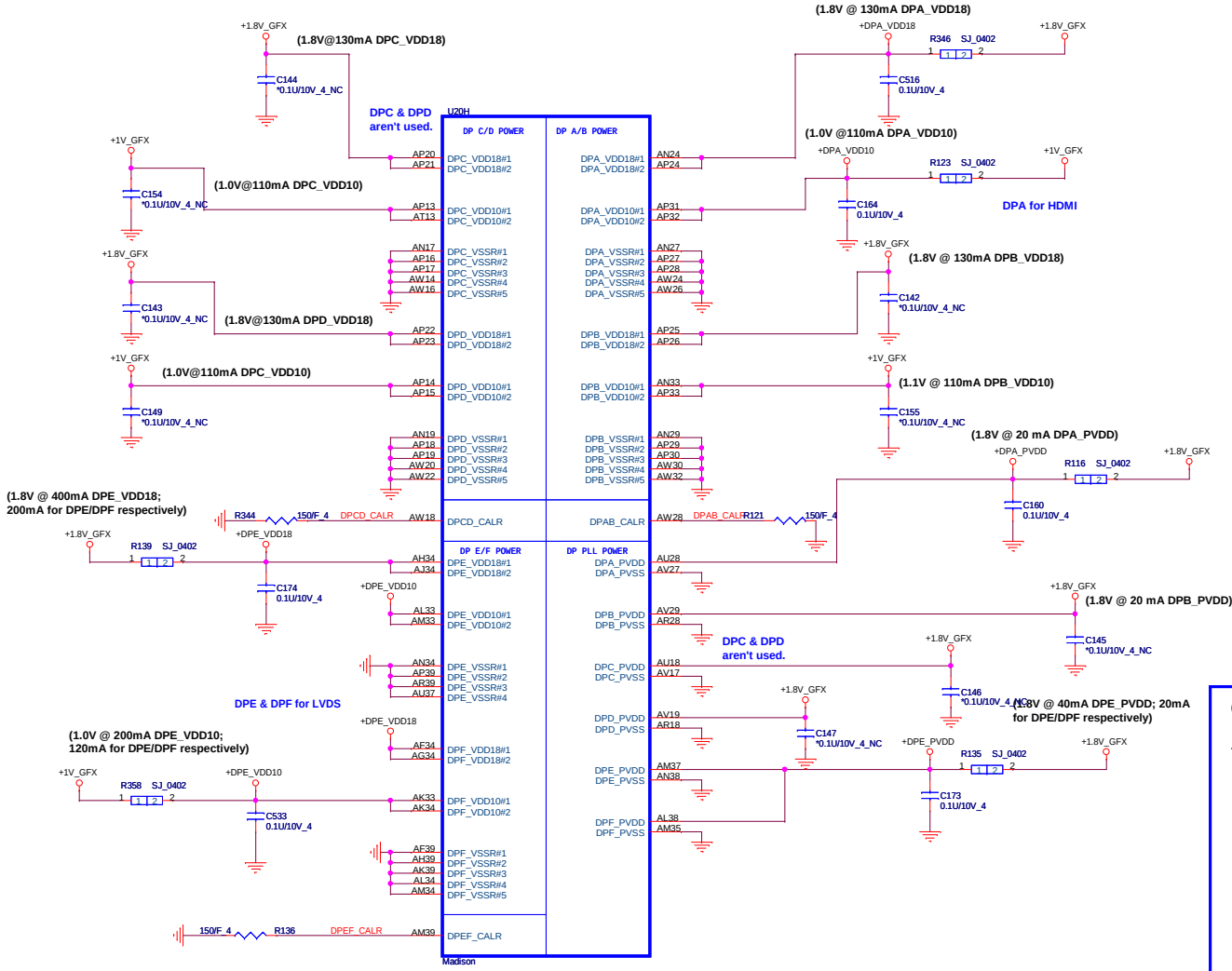

GPU Power Rail List

+1V_GFX=>
- +DPA_VDD10
- +SPV10
- +DPE_VDD10
- +DPLL_VDDC
- +PCIE_VDDC

+1.8V_GPU=>
- +A2VDDQ
- +AVDD
- +DPA_PVDD
- +DPA_VDD18
- +DPE_PVDD
- +DPE_VDD18
- +DPLL_PVDD
- +MPV18
- +PCIE_PVDD
- +PCIE_VDDR
- +SPV18
- +TSVDD
- +VDD1DI
- +VDD2DI
- +VDD_CT
- +VDDR4

GPU Power-on sequence

1 => +3V_GFX
2 => +VCC_DGFX_CORE
3 => +1V_GFX
4 => +1.5V_GFX
5 => +1.8V_GFX
6 => dGPU_PWROK

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Madison_DP_POWER	1A

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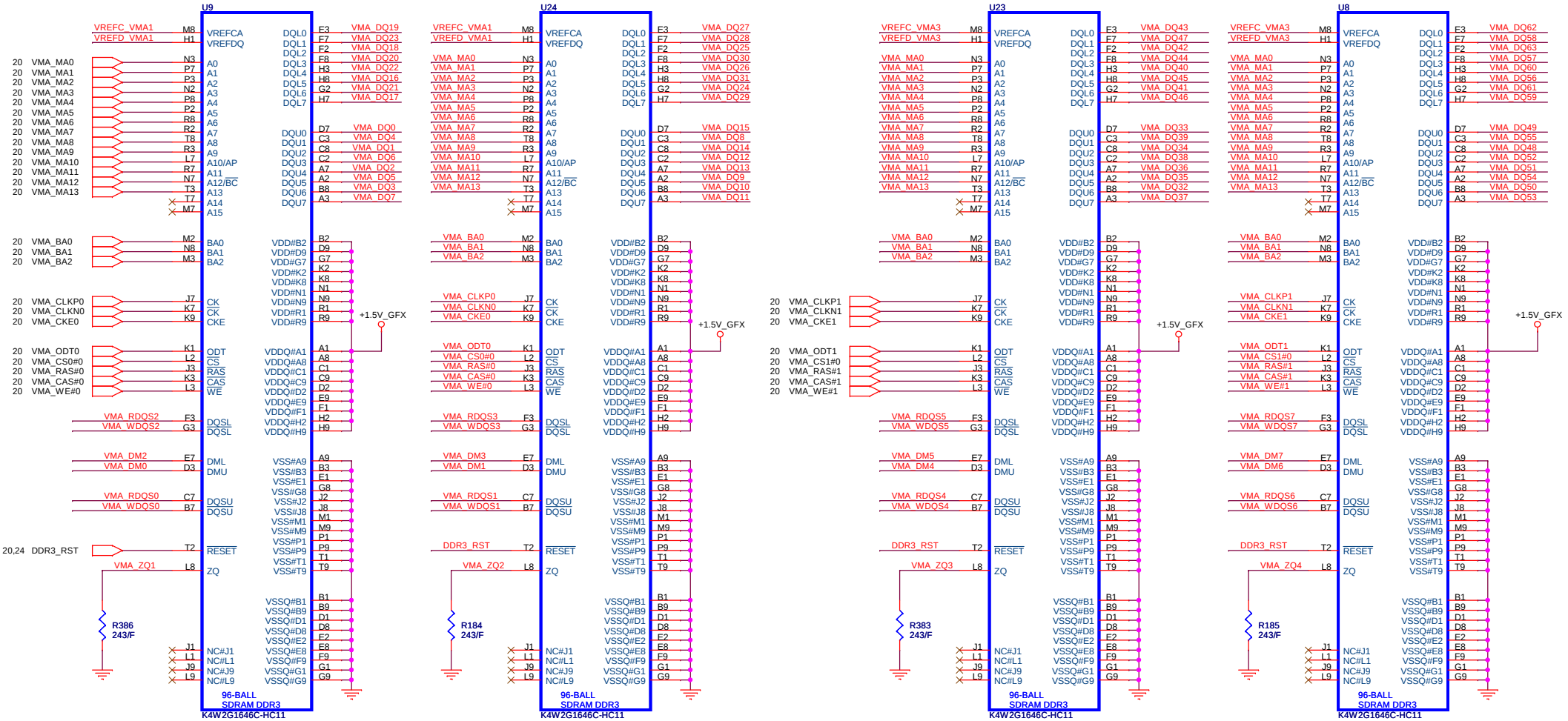
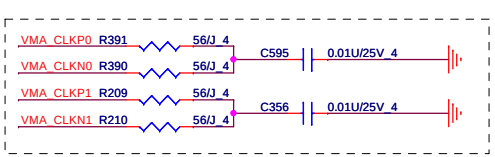
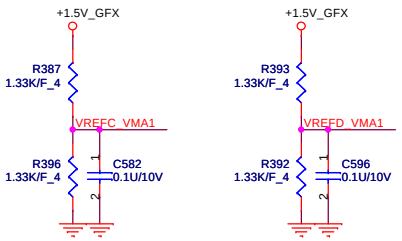
CHANNEL A: 1024MB DDR3

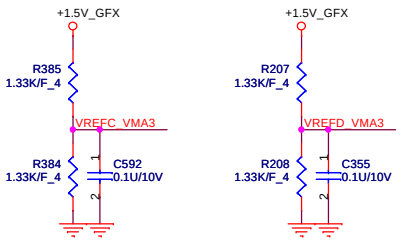
20 VMA_DQ[63..0]
20 VMA_DM[7..0]
20 VMA_WDQS[7..0]
20 VMA_RDQS[7..0]

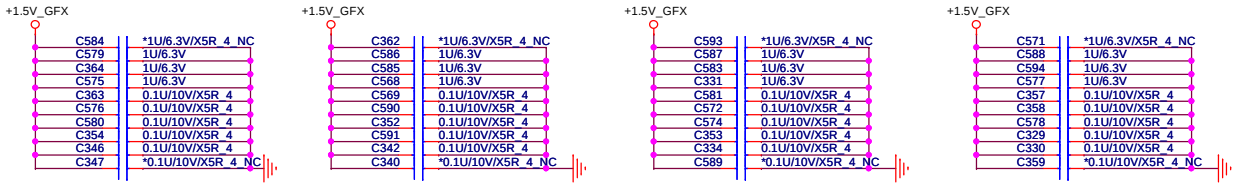


Placement has to be close to VRAM









Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	N11M-GE2 VRAM-1(DDR3 BGA96)	1A

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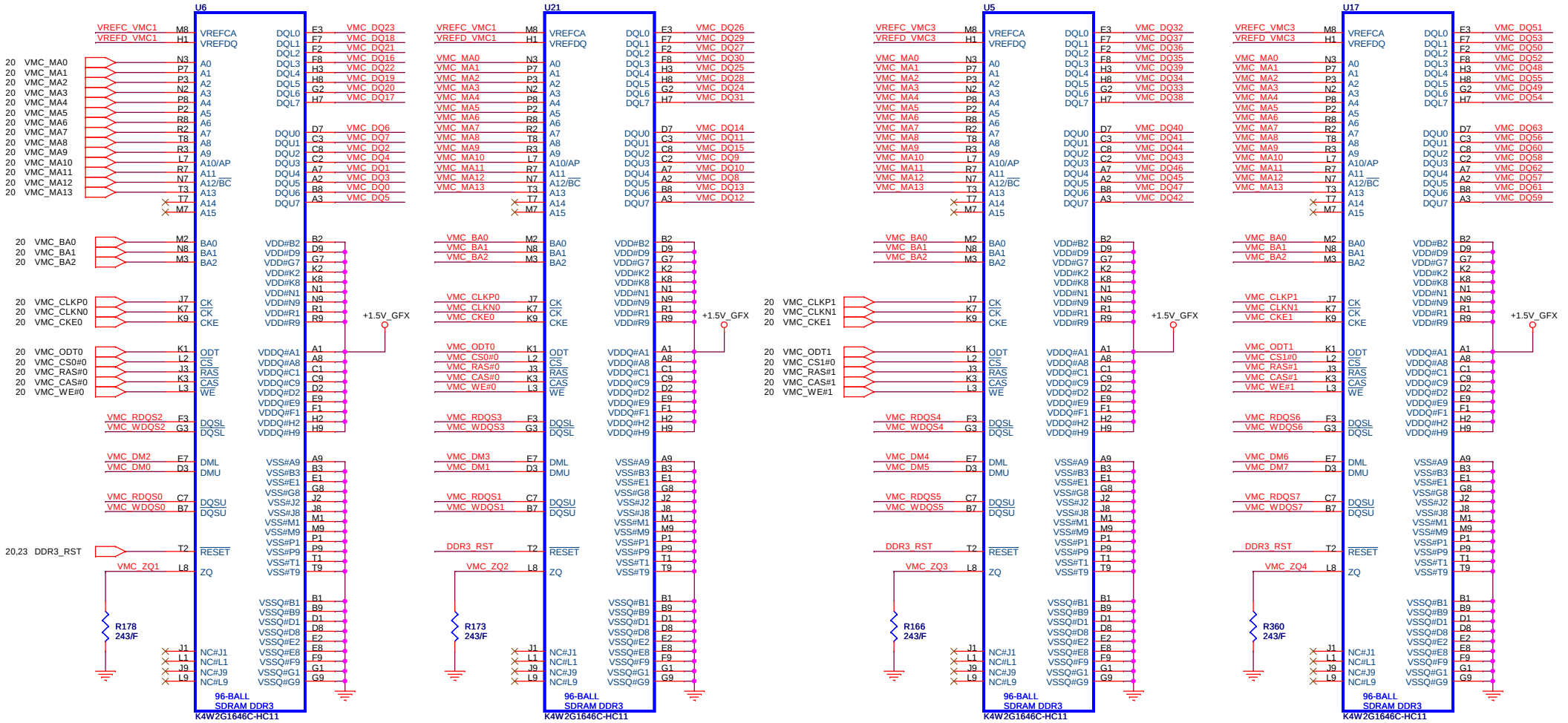
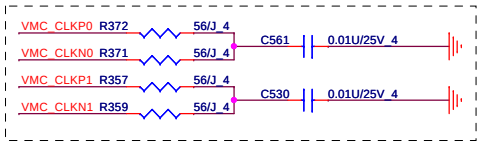
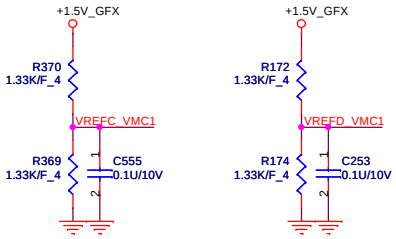
CHANNEL B: 1024MB DDR3

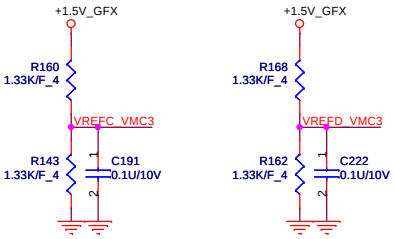
20 VMC_DQ[63..0]
20 VMC_DM[7..0]
20 VMC_WDQS[7..0]
20 VMC_RDQS[7..0]

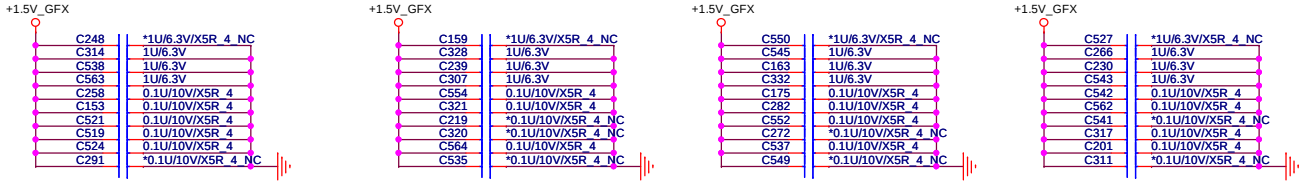


Placement has to be close to VRAM





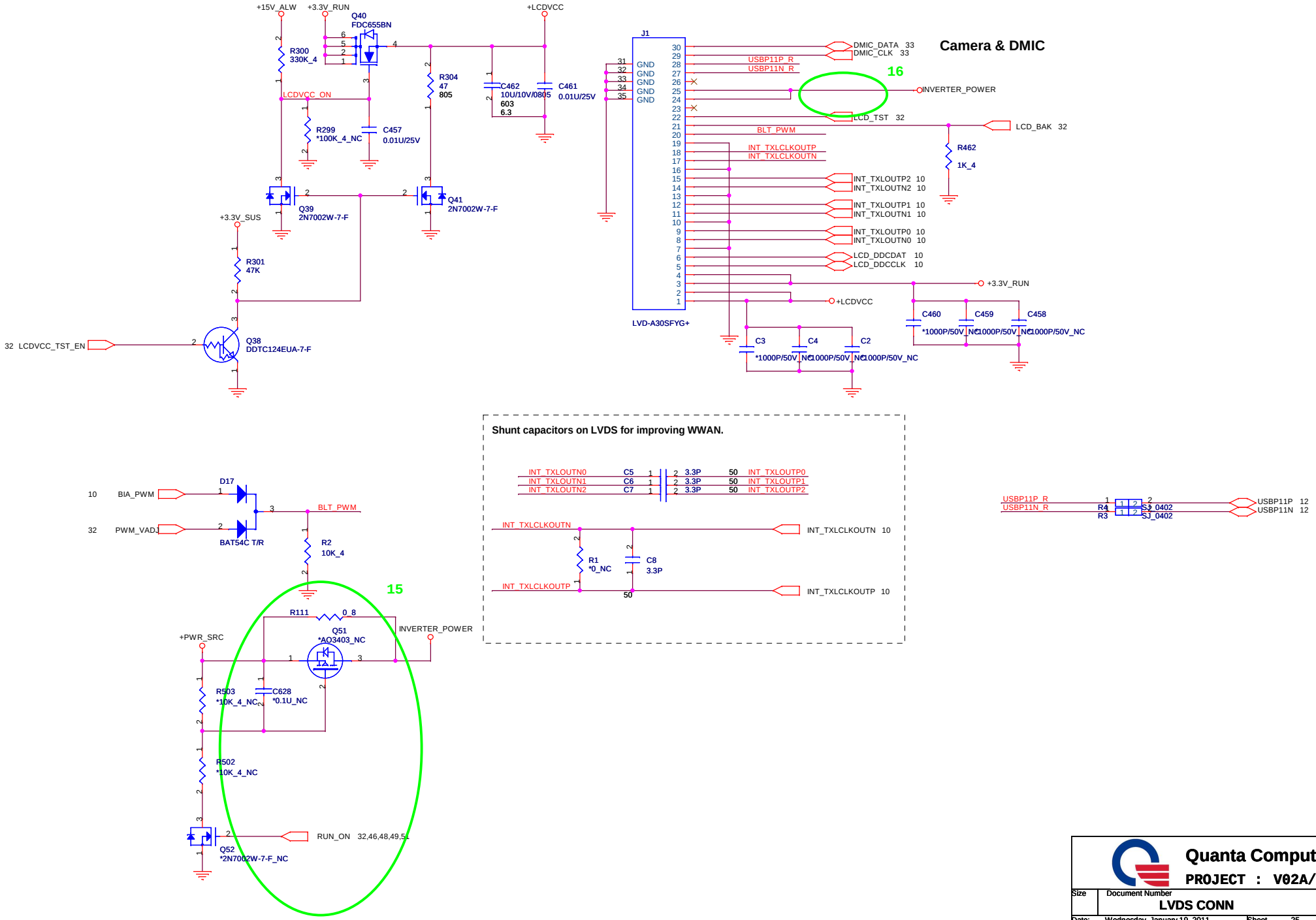




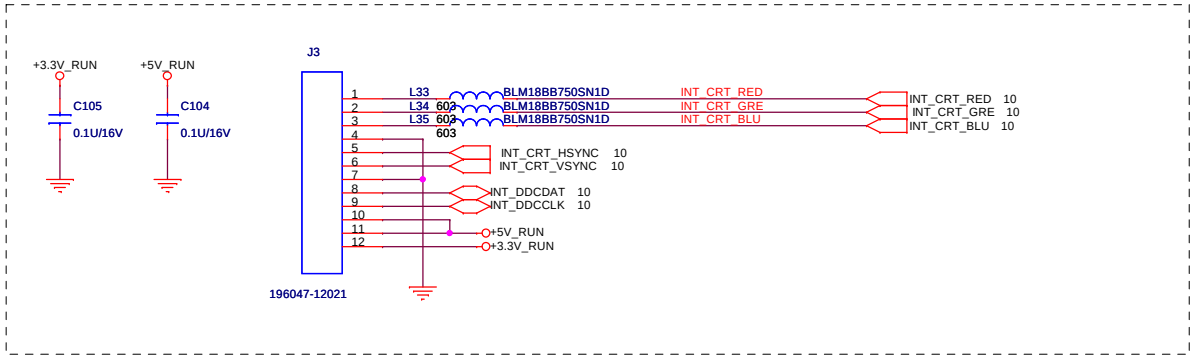
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	N11M-GE2 VRAM-2(DDR3 BGA96)	1A

Date: Wednesday, January 19, 2011 Sheet 24 of 61



Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: LVDS CONN	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 25 of 61	



Quanta Computer Inc.		
PROJECT : V02A/RO1A		
Size	Document Number: BLANK	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 26 of 61	

UMA HDMI

10 INT_HDMI_TXP2	C157	0.1U/10V	HDMI_TX2+_R
10 INT_HDMI_TXN2	C151	0.1U/10V	HDMI_TX2-_R
10 INT_HDMI_TXP1	C148	0.1U/10V	HDMI_TX1+_R
10 INT_HDMI_TXN1	C138	0.1U/10V	HDMI_TX1-_R
10 INT_HDMI_TXP0	C162	0.1U/10V	HDMI_TX0+_R
10 INT_HDMI_TXN0	C170	0.1U/10V	HDMI_TX0-_R
10 INT_HDMI_TXCP	C133	0.1U/10V	HDMI_CLK+_R
10 INT_HDMI_TXCN	C132	0.1U/10V	HDMI_CLK-_R
10 HDMI_SCL	R104	0_4	HDMI_SCL_R
10 HDMI_SDA	R102	0_4	HDMI_SDA_R
10 INT_DP_HPD	R325	0_4	HDMI_HPD_3V

DIS HDMI

19 EXT_HDMI_TXP2	C517	*0.1U/10V_NC	HDMI_TX2+_R
19 EXT_HDMI_TXN2	C512	*0.1U/10V_NC	HDMI_TX2-_R
19 EXT_HDMI_TXP1	C509	*0.1U/10V_NC	HDMI_TX1+_R
19 EXT_HDMI_TXN1	C508	*0.1U/10V_NC	HDMI_TX1-_R
19 EXT_HDMI_TXP0	C518	*0.1U/10V_NC	HDMI_TX0+_R
19 EXT_HDMI_TXN0	C520	*0.1U/10V_NC	HDMI_TX0-_R
19 EXT_HDMI_TXCP	C506	*0.1U/10V_NC	HDMI_CLK+_R
19 EXT_HDMI_TXCN	C504	*0.1U/10V_NC	HDMI_CLK-_R
19 EXT_HDMI_SCL	R105	*0_4_NC	HDMI_SCL_R
19 EXT_HDMI_SDA	R103	*0_4_NC	HDMI_SDA_R
19 EXT_HDMI_HPD	R150	*0_4_NC	HDMI_HPD_3V

Reserve for EMI and close to HDMI CONN

9

HDMI_TX2+_R — R276 — SJ_0402 — HDMI_TX2+_C
HDMI_TX2-_R — R282 — SJ_0402 — HDMI_TX2-_C
HDMI_TX0+_R — R285 — SJ_0402 — HDMI_TX0+_C
HDMI_TX0-_R — R293 — SJ_0402 — HDMI_TX0-_C
HDMI_TX1+_R — R314 — SJ_0402 — HDMI_TX1+_C
HDMI_TX1-_R — R377 — SJ_0402 — HDMI_TX1-_C
HDMI_CLK+_R — R432 — SJ_0402 — HDMI_CLK+_C
HDMI_CLK-_R — R504 — SJ_0402 — HDMI_CLK-_C

HDMI HPD

+3.3V_RUN
Q50 MMST3904-7-F
R491 200K
HDMI_HPD
R246 200K
HDMI_HPD_3V — R501 — SJ_0402
R324 10K_4

R347/R345 680/F HDMI_TX2+_R / HDMI_TX2-_R
R339/R337 680/F HDMI_TX1+_R / HDMI_TX1-_R
R349/R350 680/F HDMI_TX0+_R / HDMI_TX0-_R
R332/R331 680/F HDMI_CLK+_R / HDMI_CLK-_R
+5V_RUN — Q44 2N7002W-7-F

HDMI Conn.

CN6 DFHS19FR015 Female TYPE A

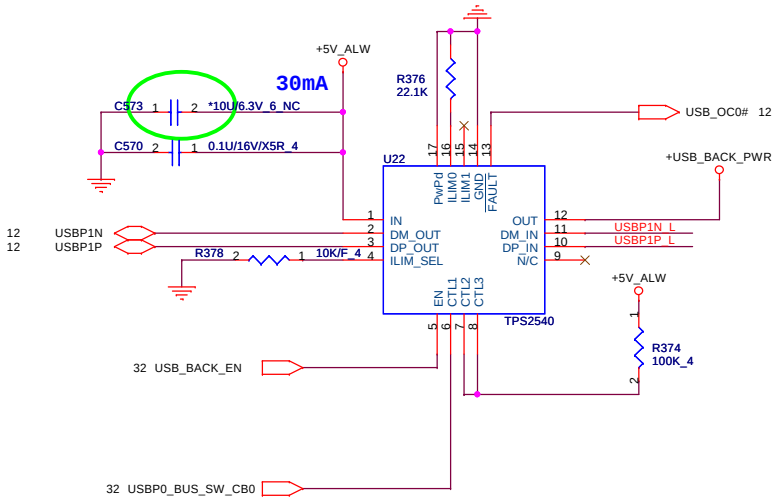
+3.3V_RUN — R99 4.7K, R98 4.7K
HDMI_SCL_R — Q9 FDV301N — HDMI_CLK
HDMI_SDA_R — Q8 FDV301N — HDMI_DAT
+5V_RUN — R320 2.2K_4, R323 2.2K_4
C126 *0.1U_NC 16

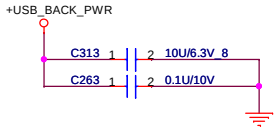
HDMI_TX2+_C, HDMI_TX2-_C, HDMI_TX1+_C, HDMI_TX1-_C, HDMI_TX0+_C, HDMI_TX0-_C, HDMI_CLK+_C, HDMI_CLK-_C, HDMI_HPD

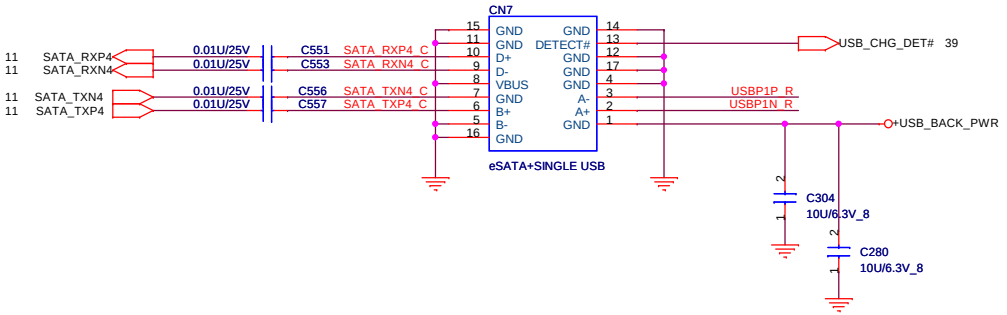
Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: HDMI CONN	Rev 1A
Date: Wednesday, January 19, 2011	Sheet 27 of 61	

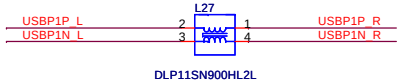
ESATA + USB Conn + Power share

S3/S5 USB charging circuit









USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

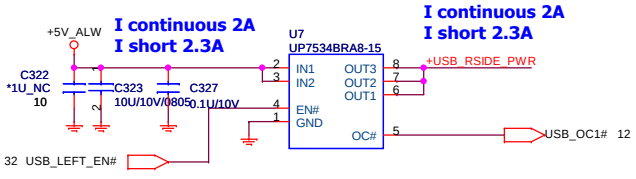
	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

Quanta Computer Inc.
PROJECT : V02A/R01A

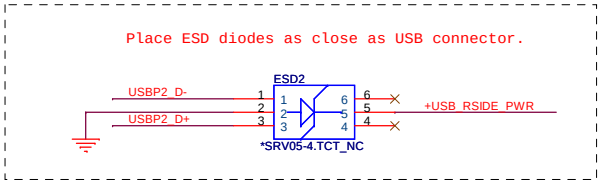
Size	Document Number	Rev
	PUSB / ESATA	1A

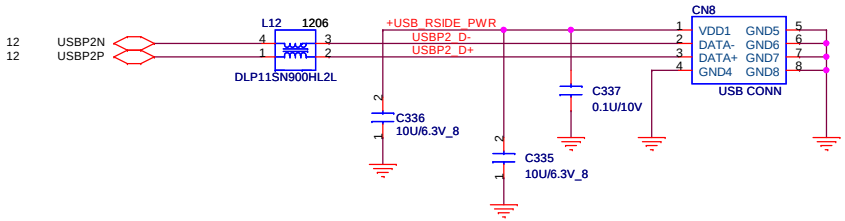
Date: Wednesday, January 19, 2011 Sheet 28 of 61

UPI power switch



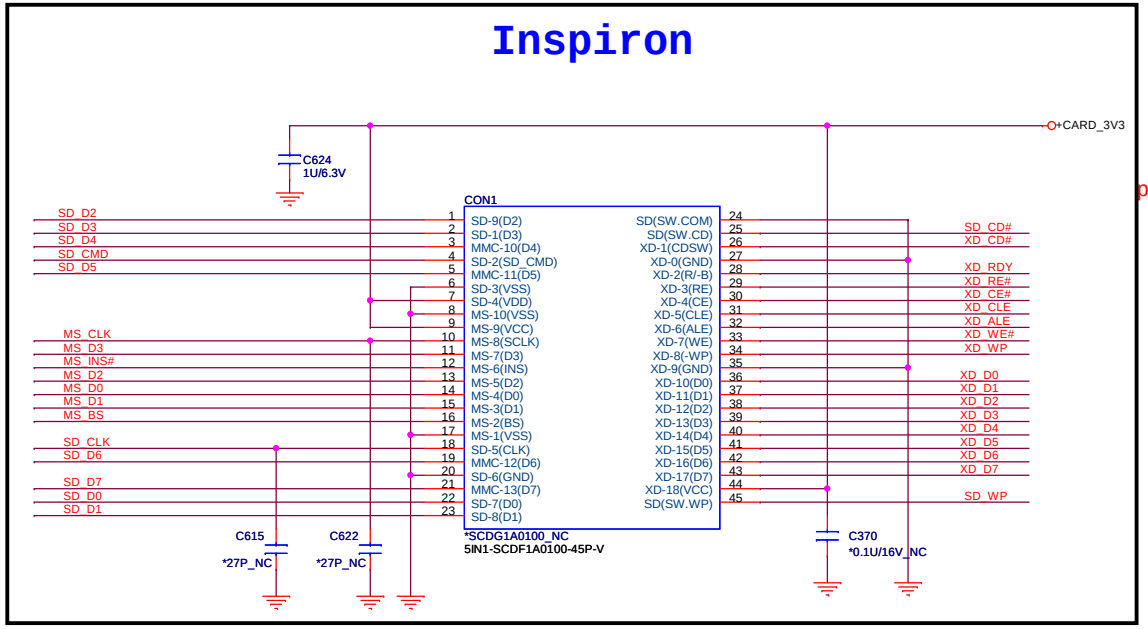
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

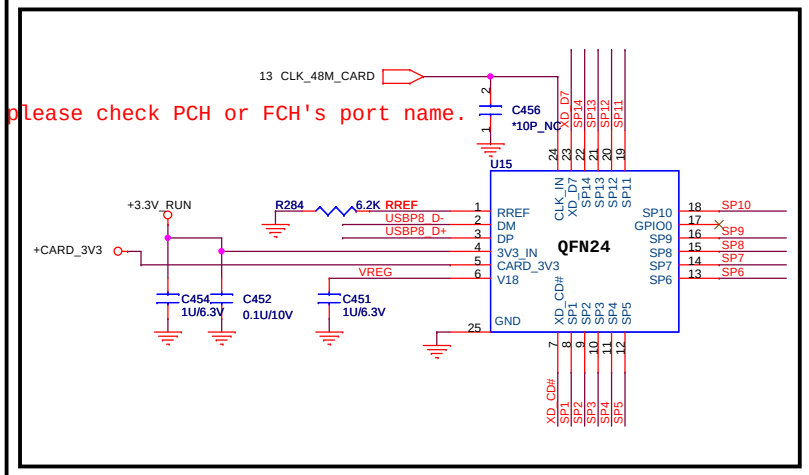




Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: USB 2.0	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 29 of 61	

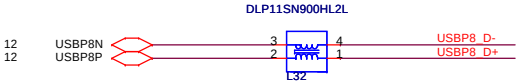
Inspiron



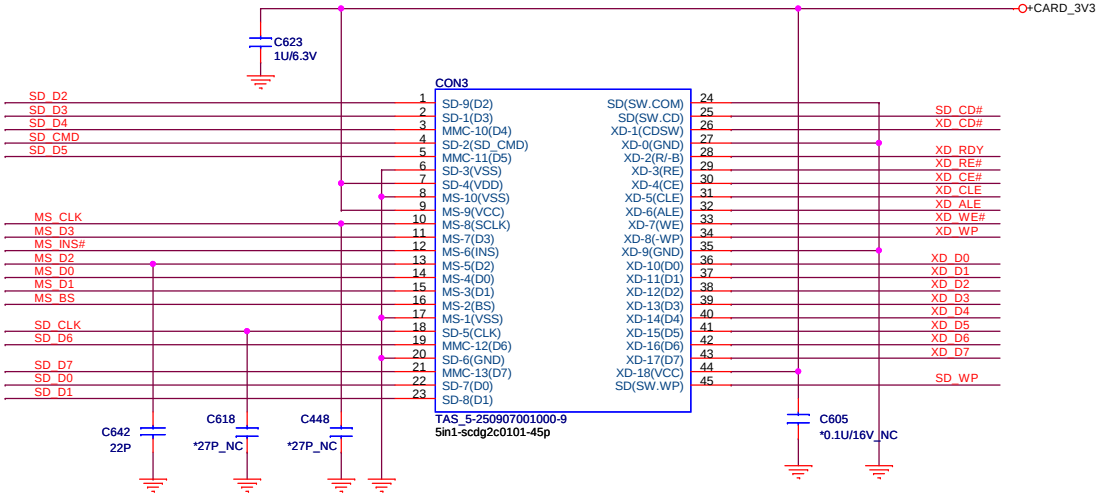


SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS

Share Pin



VOSTOR



Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1

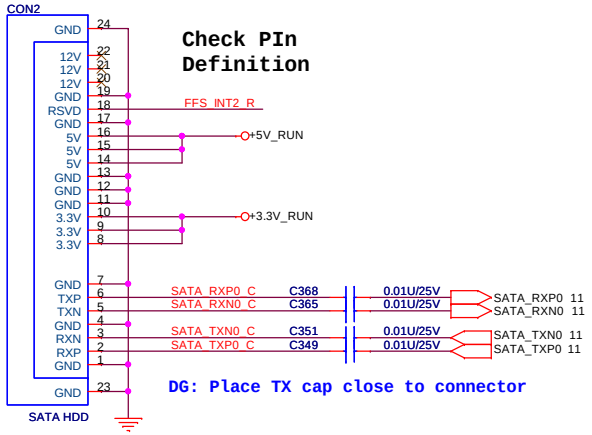
Quanta Computer Inc.

PROJECT : V02A/R01A

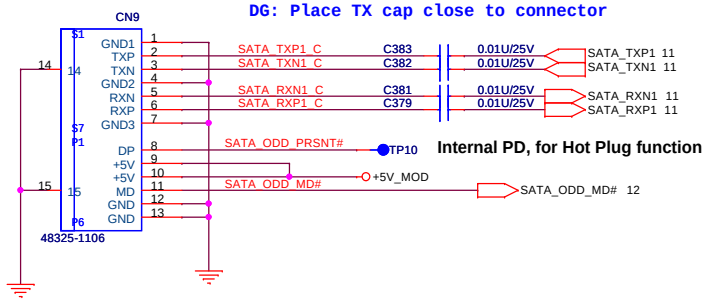
Size	Document Number	Rev
	Cardreader (RTS5128)	1A

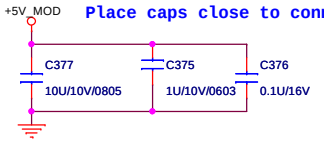
Date: Wednesday, January 19, 2011 Sheet 30 of 61

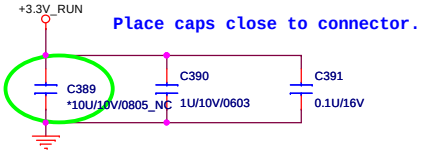
SATA Connector UM8

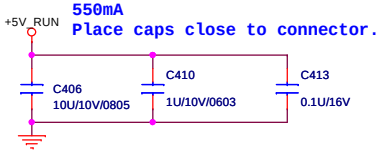


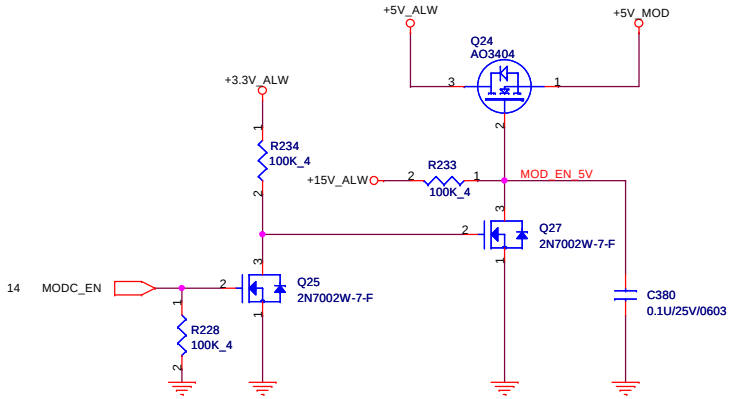
ODD Connector

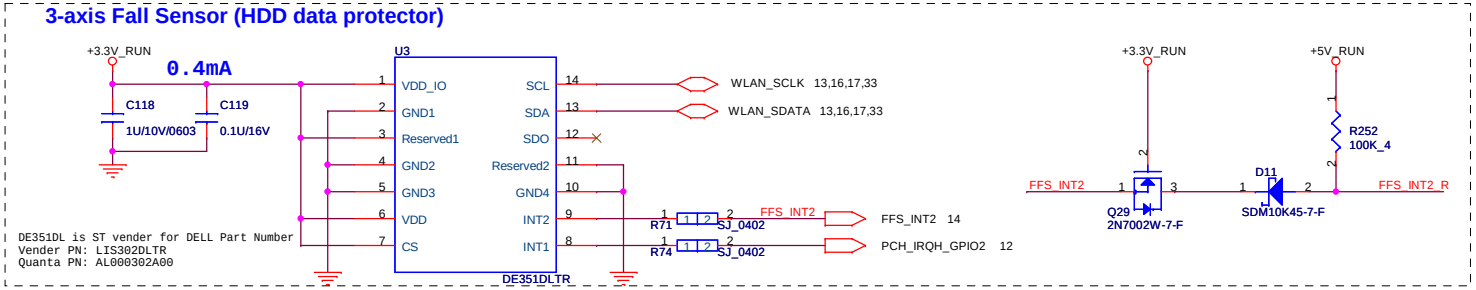








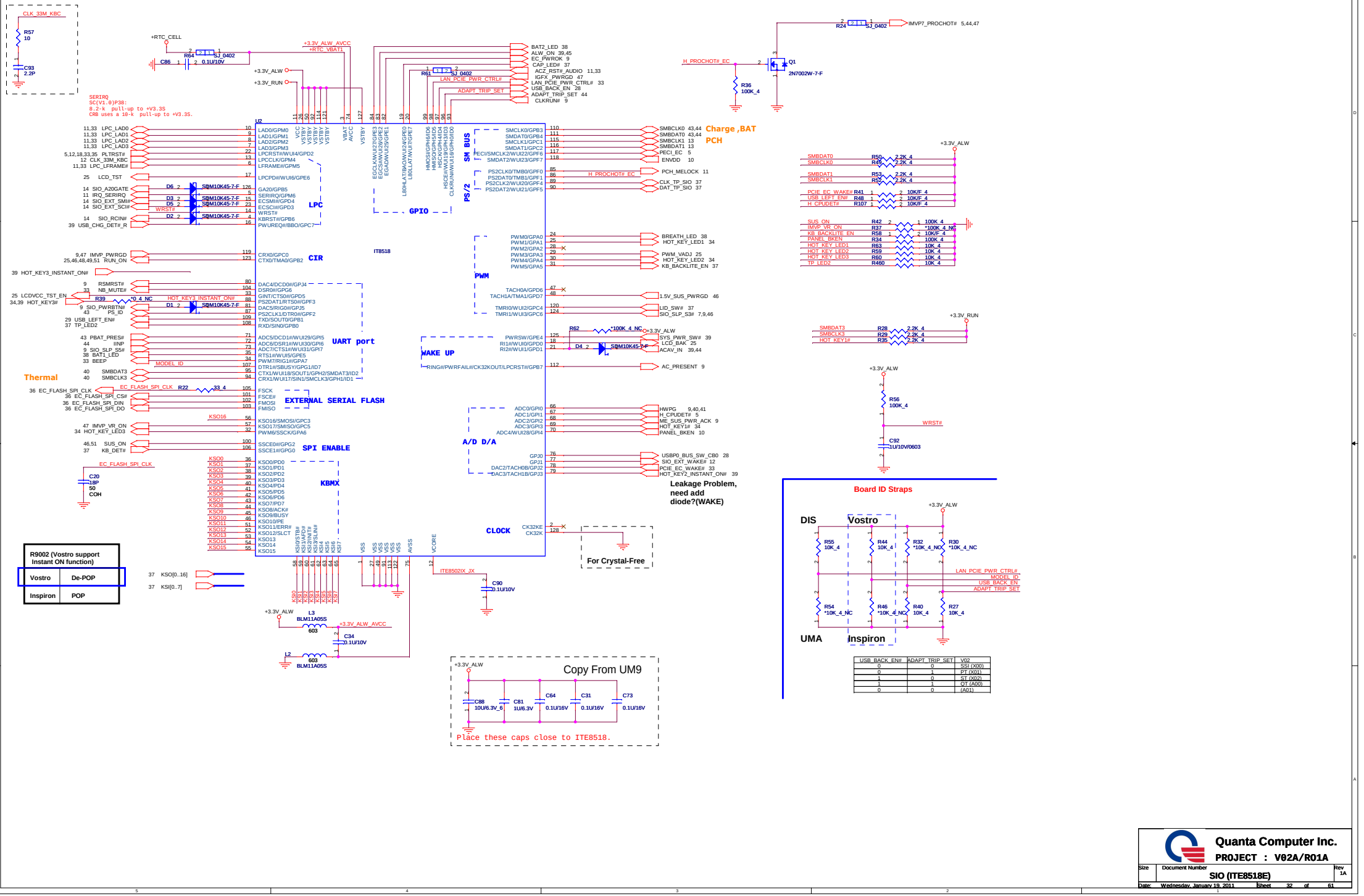


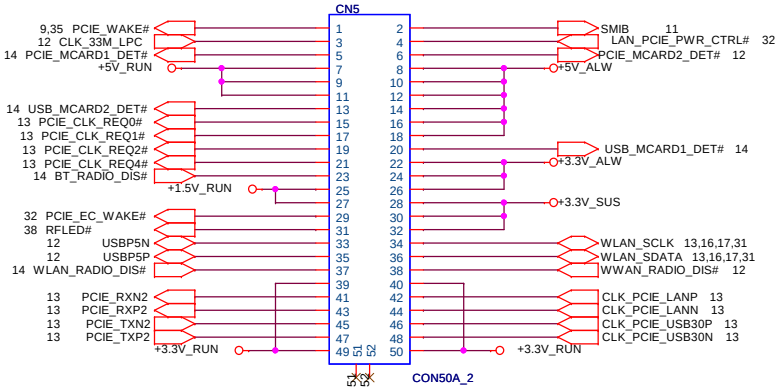


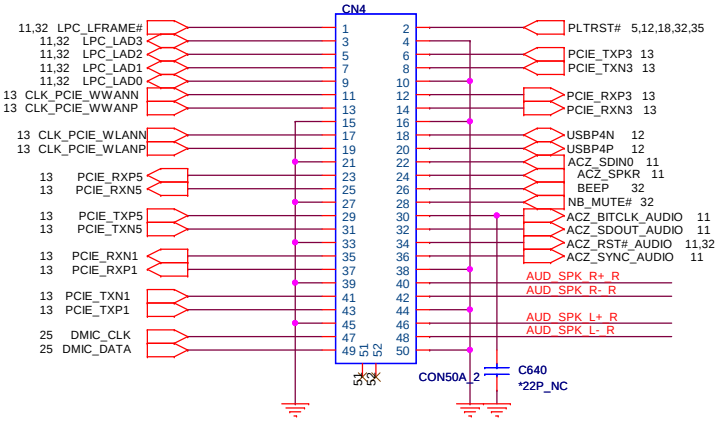
3-axis Fall Sensor	VOSTOR	Inspiron
U3,Q29,D11 R71,R74,R252 C118,C119	POP	NC

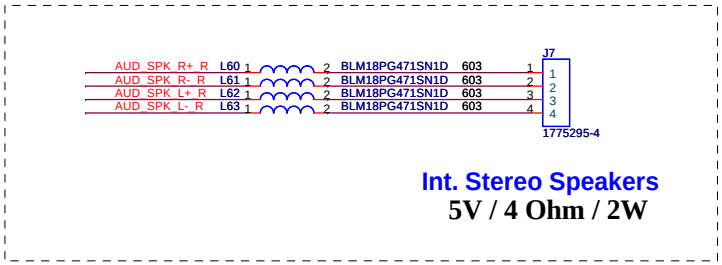
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	SATA HDD/ODD	1A
Date: Wednesday, January 19, 2011	Sheet 31 of 61	


U2
IT8518
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Thermal
Charge ,BAT
PCH
Leakage Problem, need add diode?(WAKE)
For Crystal-Free
Board ID Straps
DIS
Vostro
UMA
Inspiron
Copy From UM9
Place these caps close to ITE8518.
R9002 (Vostro support Instant ON function)
Vostro De-POP
Inspiron POP
Quanta Computer Inc.
PROJECT : V02A/R01A
SIO (ITE8518E)
Wednesday, January 19, 2011





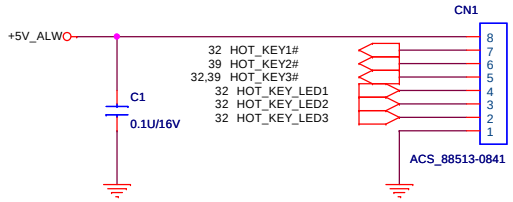


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	SIO (ITE8518E)	1A

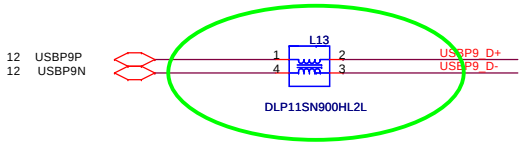
Date: Wednesday, January 19, 2011 Sheet 33 of 61

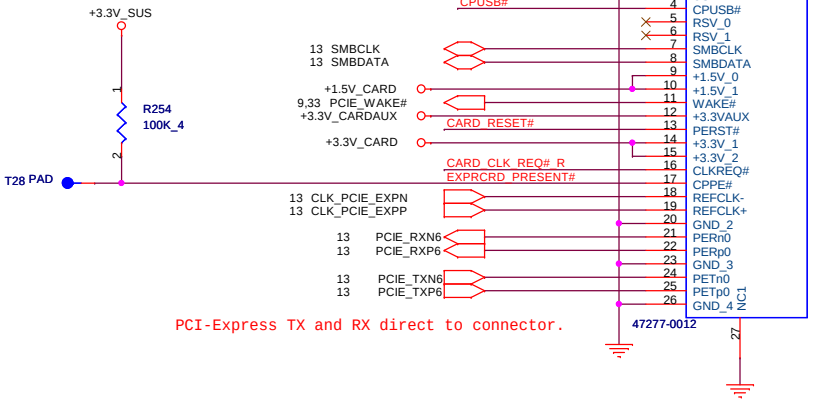


HOTKEY CON

Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: MINI-PCI (WLAN/WPAN)	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 34 of 61	

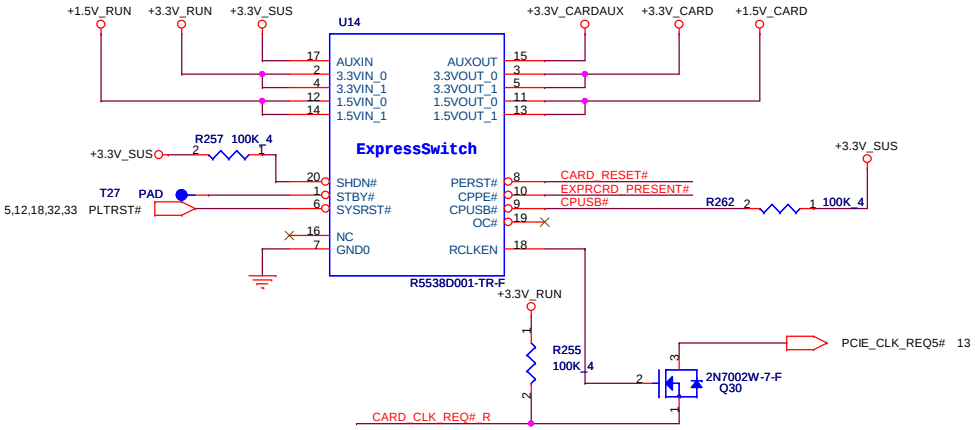
Express Card

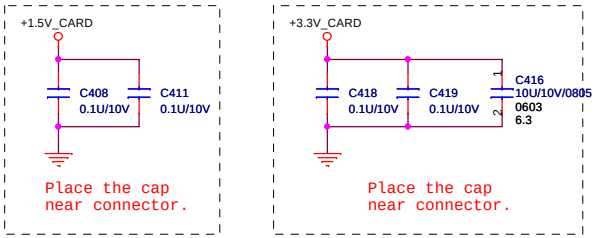




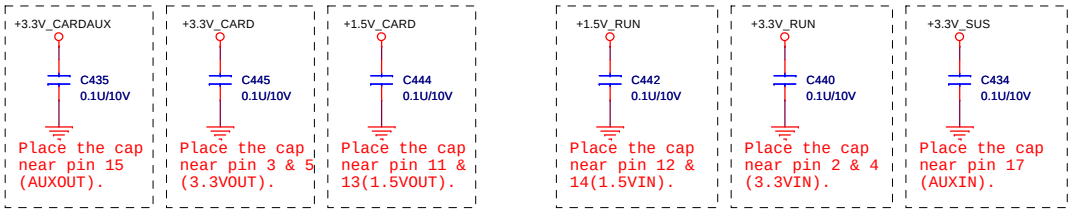
PCI-Express TX and RX direct to connector.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.





If close enough, could combine



Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	LAN (RTL8111EL)	1A
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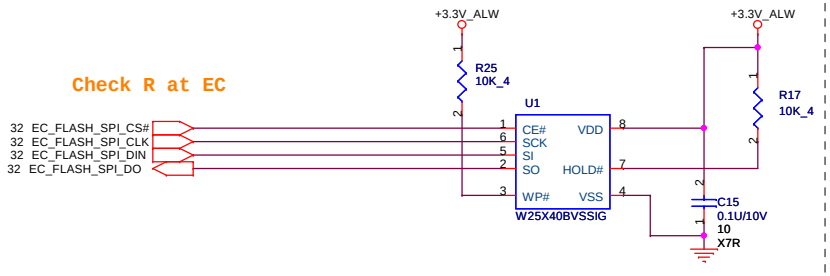
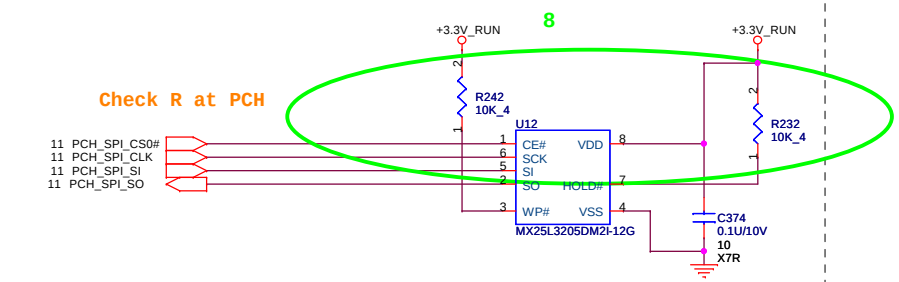
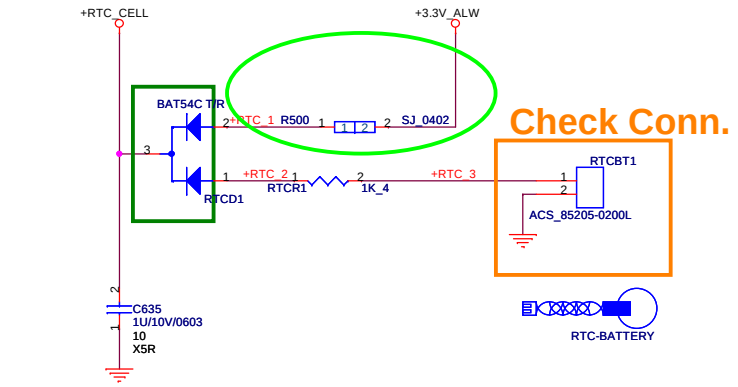
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC



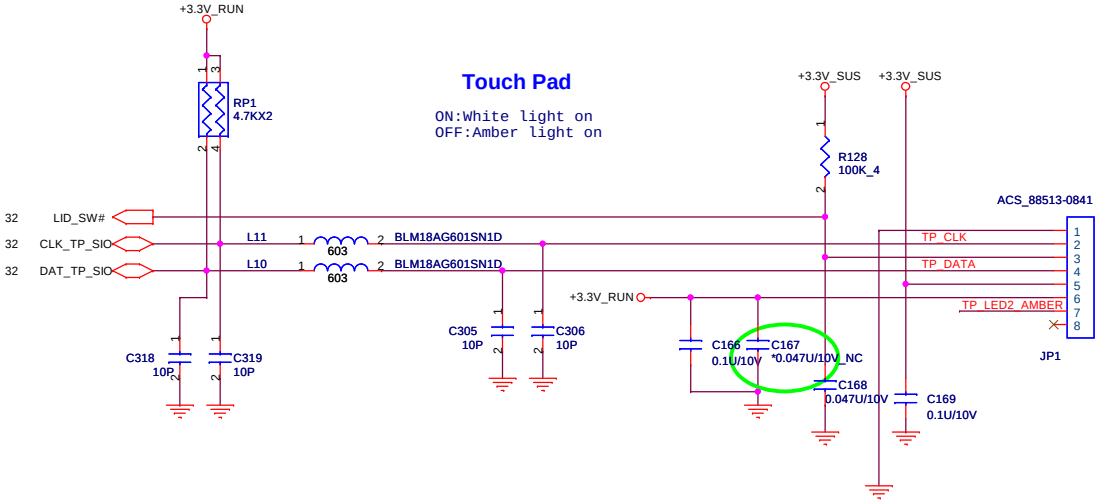
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: FLASH / RTC	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 36 of 61	

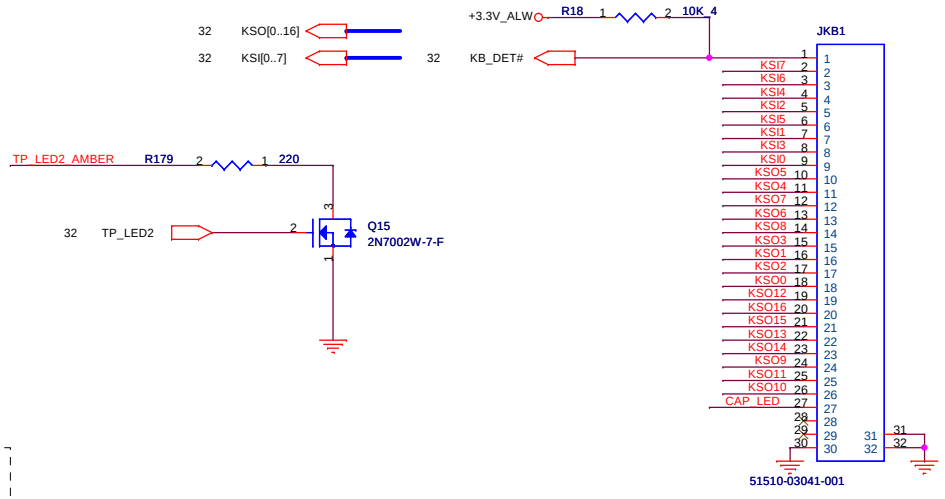
copy GM6

Touch Pad

ON:White light on
OFF:Amber light on

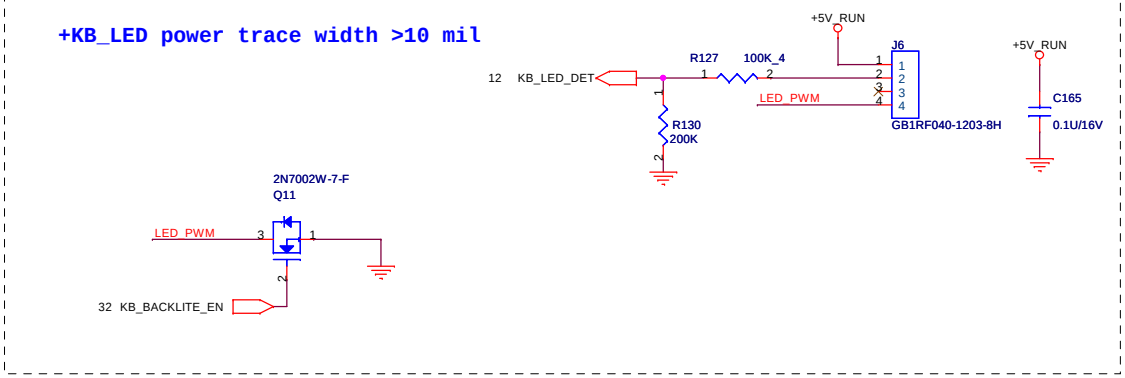


KEYBOARD CONNECTOR



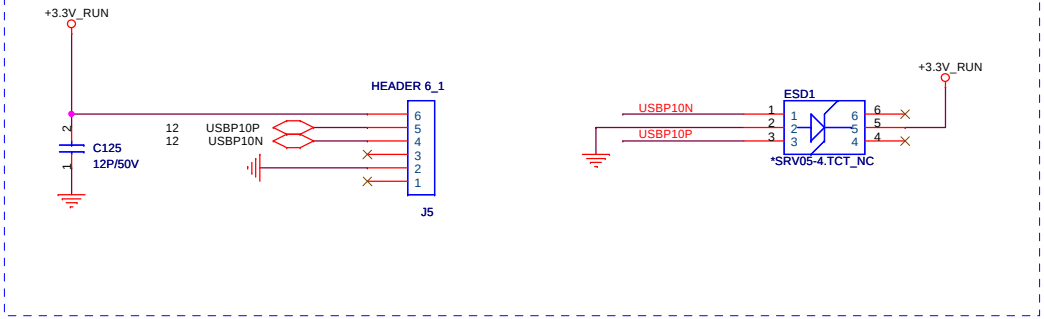
Key board illumination

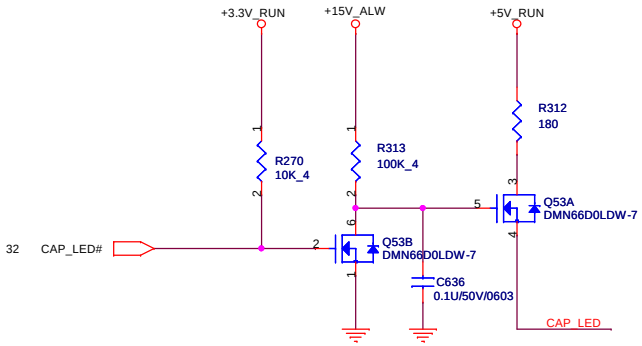
+KB_LED power trace width >10 mil



13

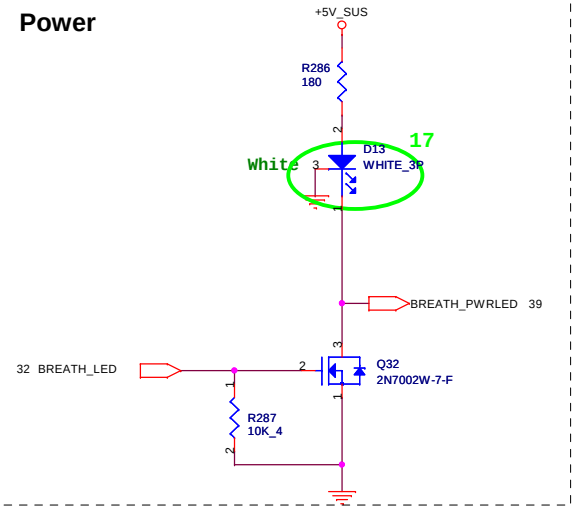
Biometric



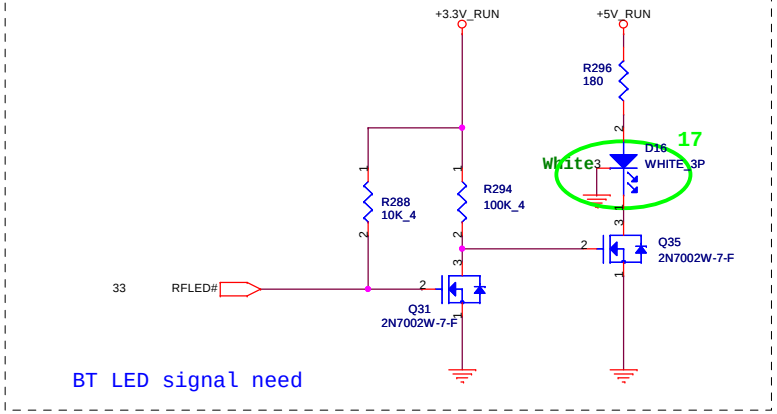


Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: TP / KB	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 37 of 61	

Power

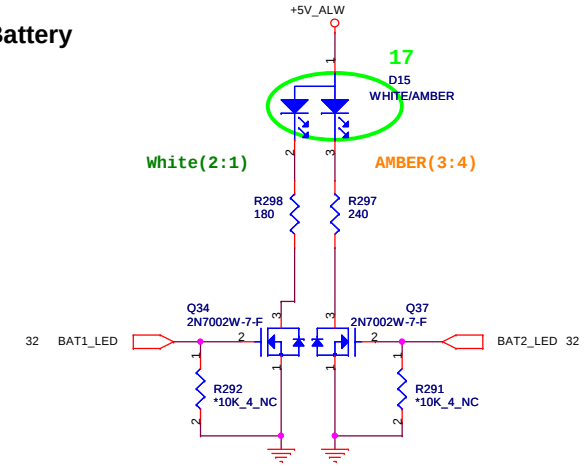


Bluetooth / WLAN on/off LED

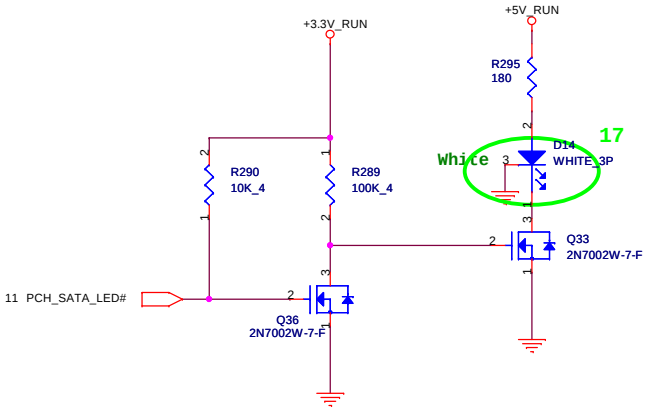


BT LED signal need

Battery



HDD activity LED.



VOSTOR	R286,R295,R296,R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286,R295,R296,R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21

Quanta Computer Inc.
PROJECT : V02A/RO1A

Size	Document Number	Rev
	LED	1A
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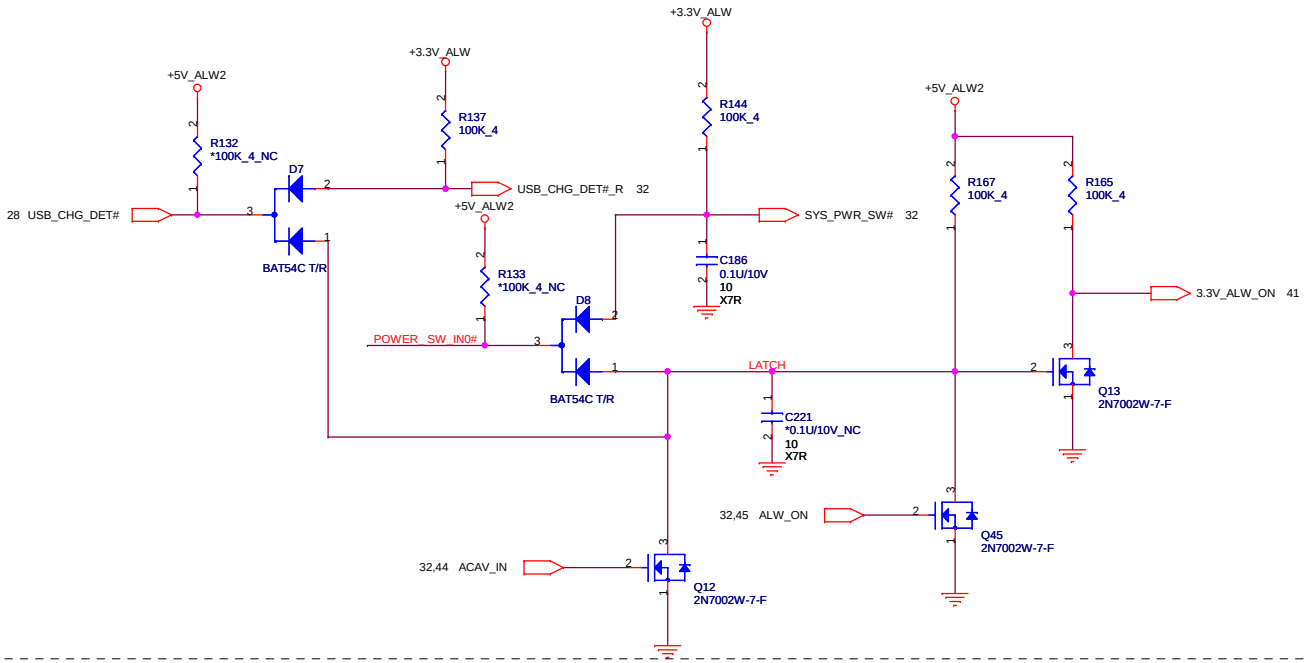
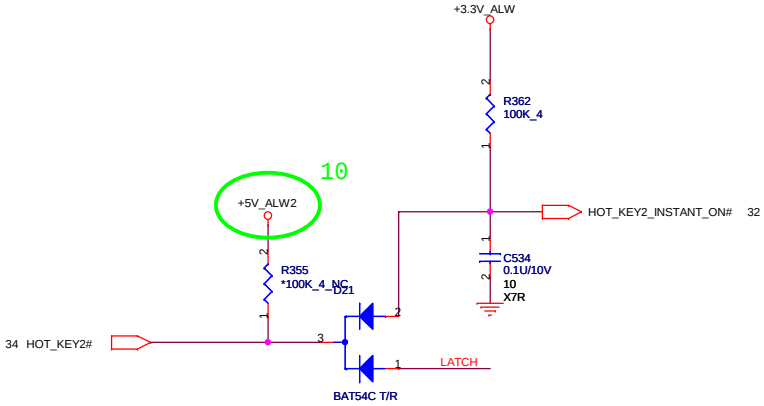
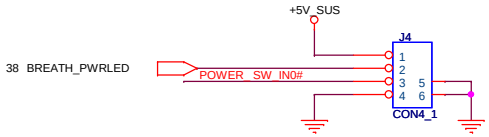
3VALW ON POWER LOGIC



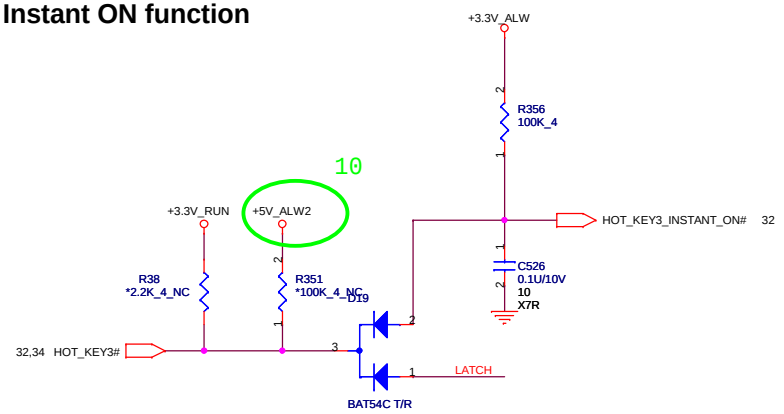


Vostro pop D19,C526,R356 depop R38,R39
Inspiron depop D19,C526,R356 pop R38,R39

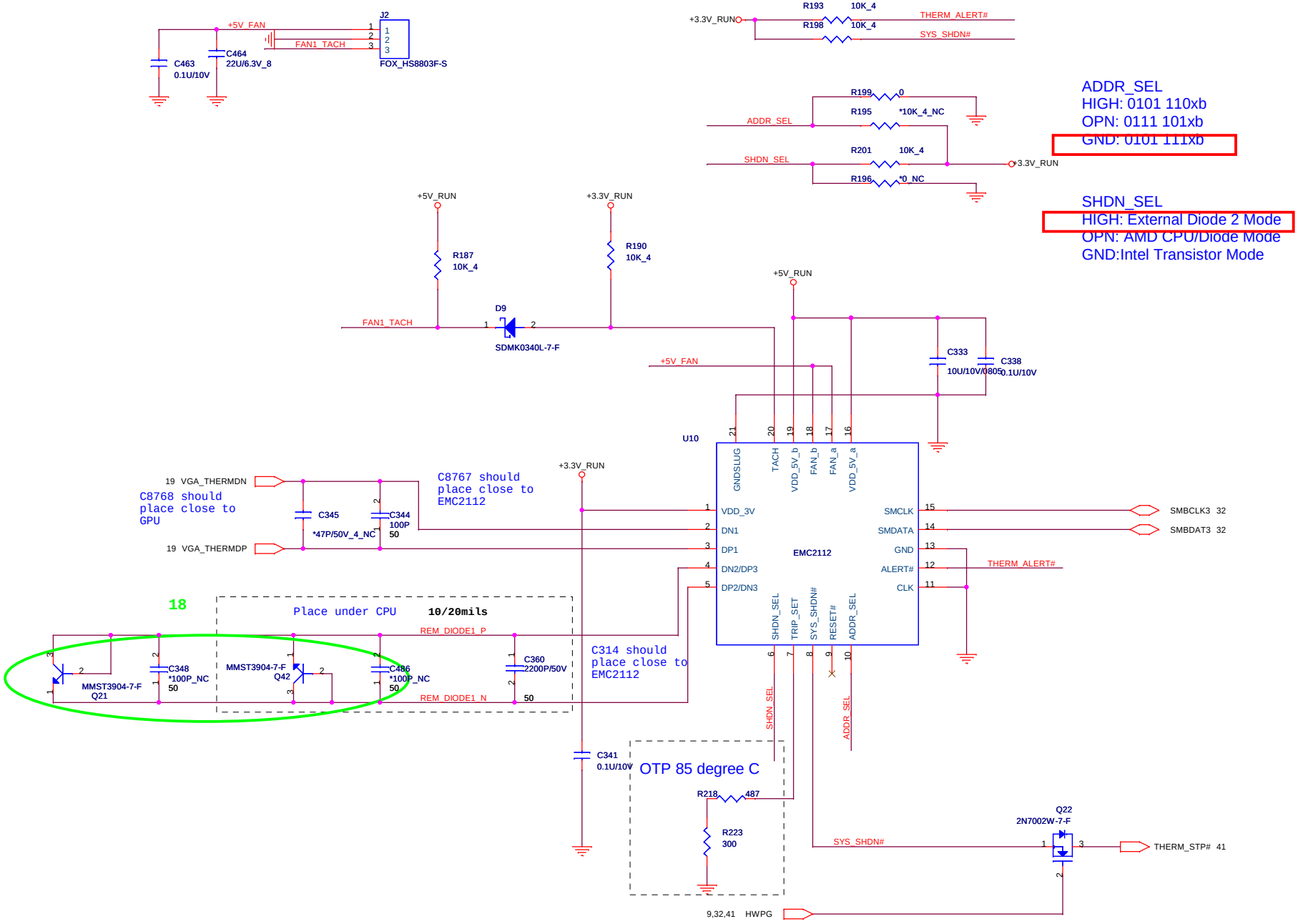
PWR button board

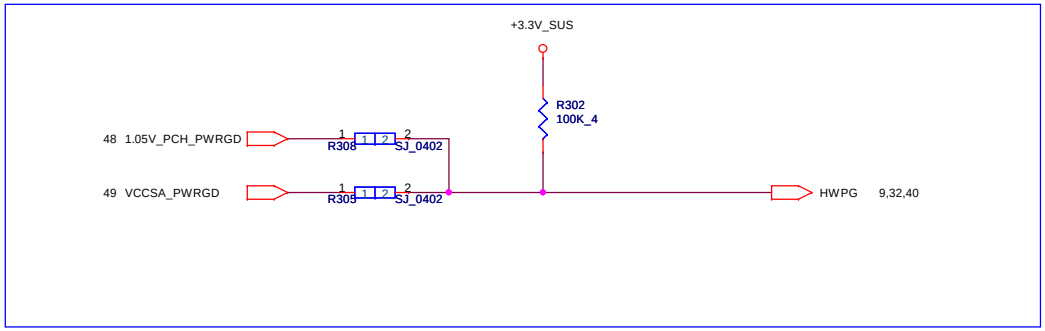


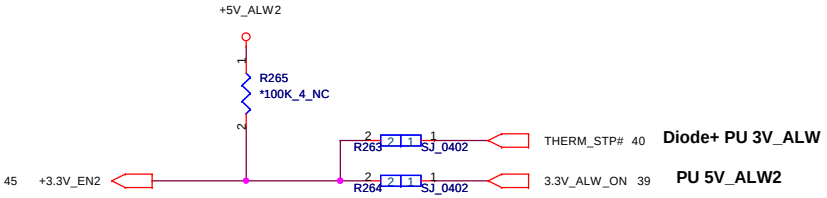
Instant ON function



Quanta Computer Inc.		
PROJECT : V02A/R01A		
Size	Document Number: PWR SW/LED	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 39 of 61	


+5V_FAN
C463
0.1U/10V
C464
22U/6.3V_8
FAN1_TACH
J2
FOX_HS8803F-S
+3.3V_RUN
R193
10K_4
R198
10K_4
THERM_ALERT#
SYS_SHDN#
ADDR_SEL
R199
0
R195
*10K_4_NC
SHDN_SEL
R201
10K_4
R196
*0_NC
ADDR_SEL
HIGH: 0101 110xb
OPN: 0111 101xb
GND: 0101 111xb
SHDN_SEL
HIGH: External Diode 2 Mode
OPN: AMD CPU/Diode Mode
GND:Intel Transistor Mode
+5V_RUN
+3.3V_RUN
R187
10K_4
R190
10K_4
D9
SDMK0340L-7-F
FAN1_TACH
+5V_FAN
C333
10U/10V/0805
C338
0.1U/10V
U10
EMC2112
GNDSLUG
TACH
VDD_5V_b
FAN_b
FAN_a
VDD_5V_a
VDD_3V
DN1
DP1
DN2/DP3
DP2/DN3
SMCLK
SMDATA
GND
ALERT#
CLK
SHDN_SEL
TRIP_SET
SYS_SHDN#
RESET#
ADDR_SEL
SMBCLK3 32
SMBDAT3 32
THERM_ALERT#
19 VGA_THERMDN
19 VGA_THERMDP
C8768 should
place close to
GPU
C345
*47P/50V_4_NC
C344
100P
50
C8767 should
place close to
EMC2112
C314 should
place close to
EMC2112
18
Place under CPU 10/20mils
REM_DIODE1_P
REM_DIODE1_N
MMST3904-7-F
Q21
C348
*100P_NC
50
MMST3904-7-F
Q42
C486
*100P_NC
50
C360
2200P/50V
50
C341
0.1U/10V
OTP 85 degree C
R218
487
R223
300
Q22
2N7002W-7-F
SYS_SHDN#
THERM_STP# 41
9,32,41 HWPG
Quanta Computer Inc.
PROJECT : V02A/R01A
Size
Document Number
FAN & THERMAL
Rev
1A
Date: Wednesday, January 19, 2011
Sheet 40 of 61

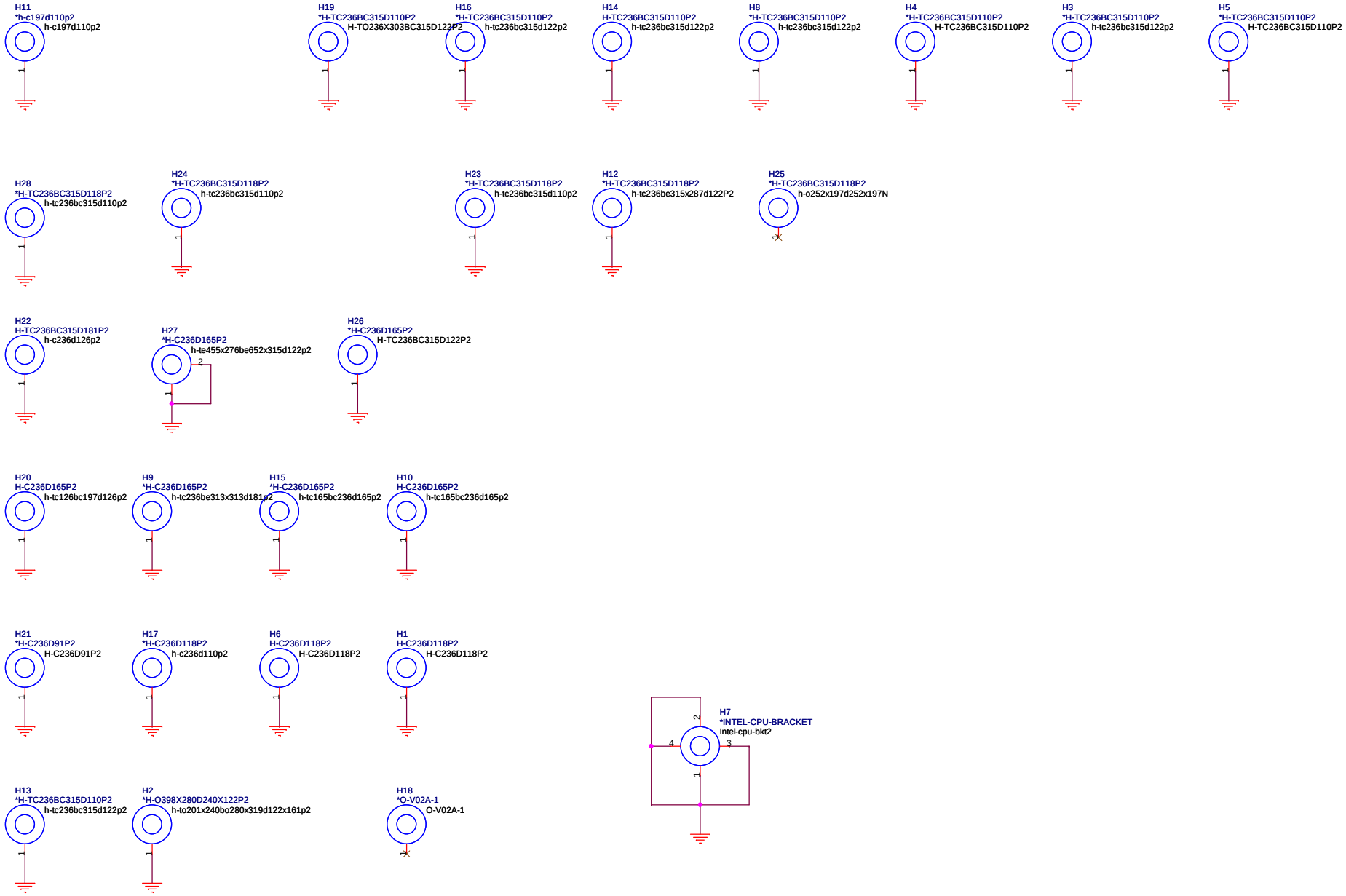




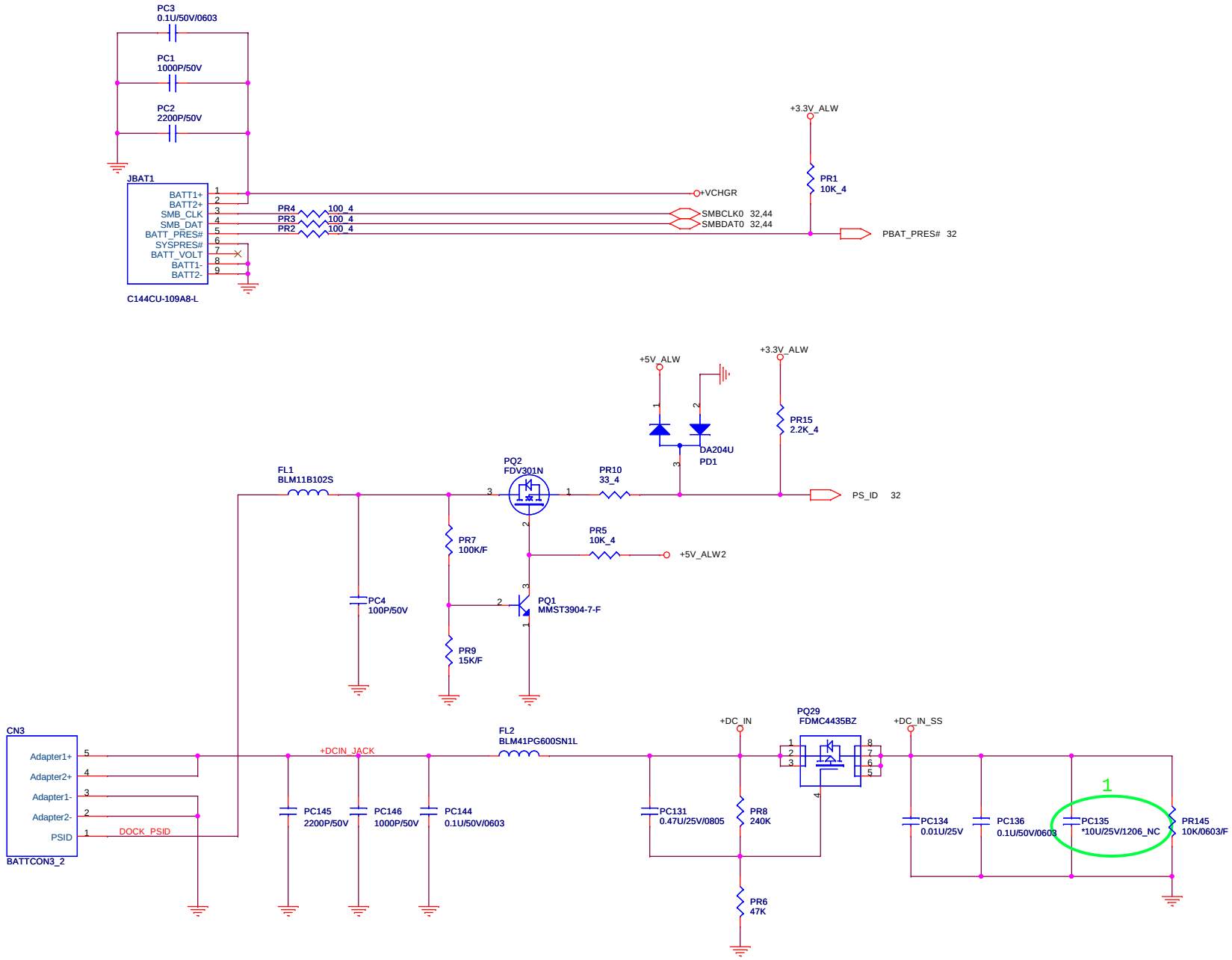
Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	System Reset Circuit	1A
Date: Wednesday, January 19, 2011	Sheet 41 of 61	



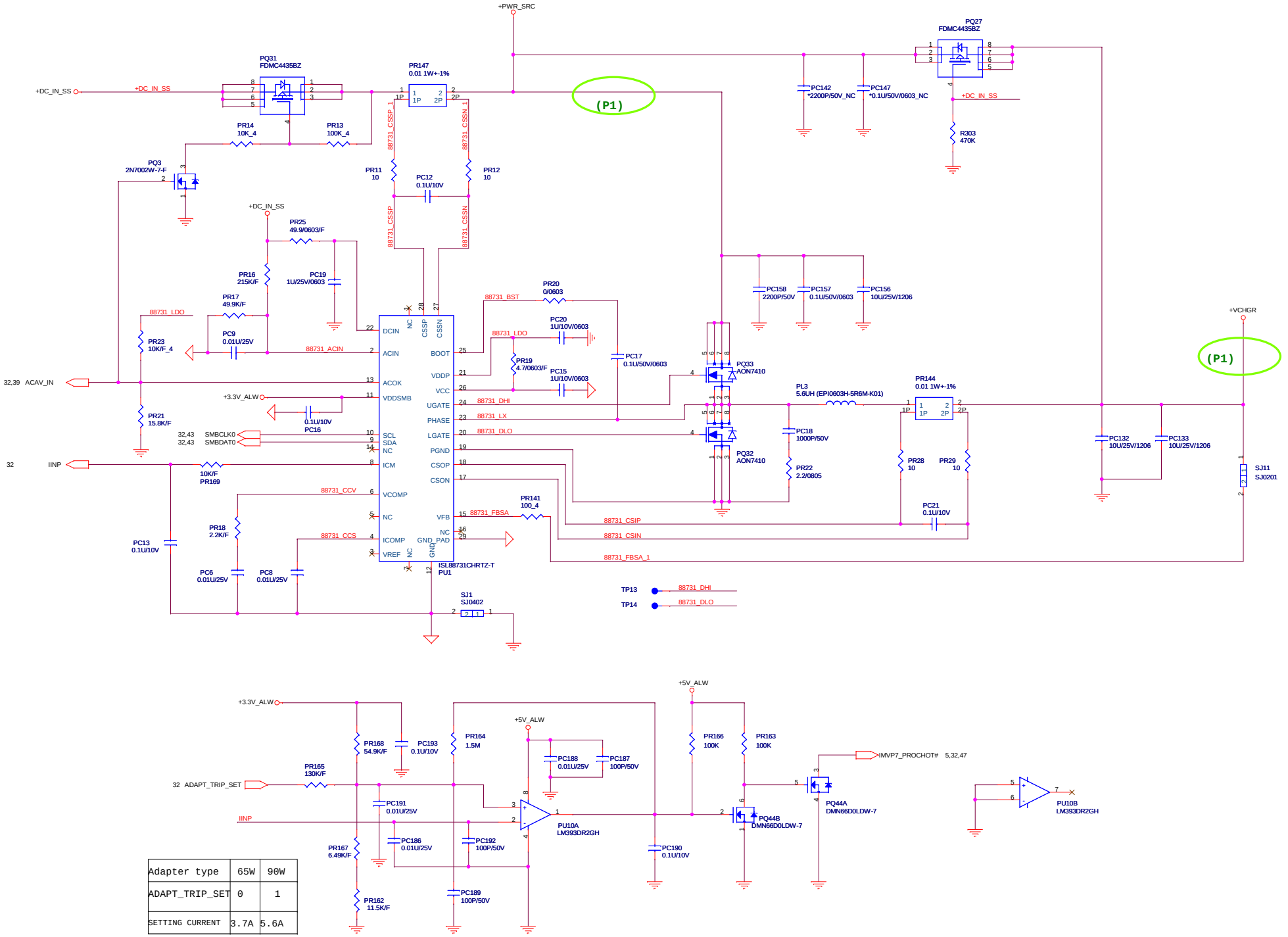
Quanta Computer Inc.		
PROJECT : V02A/RO1A		
Size	Document Number: SCREW PAD	Rev: 1A
Date: Wednesday, January 19, 2011	Sheet 42 of 61	



Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	DC IN / BATT	1A
Date: Wednesday, January 19, 2011	Sheet 43 of 61	



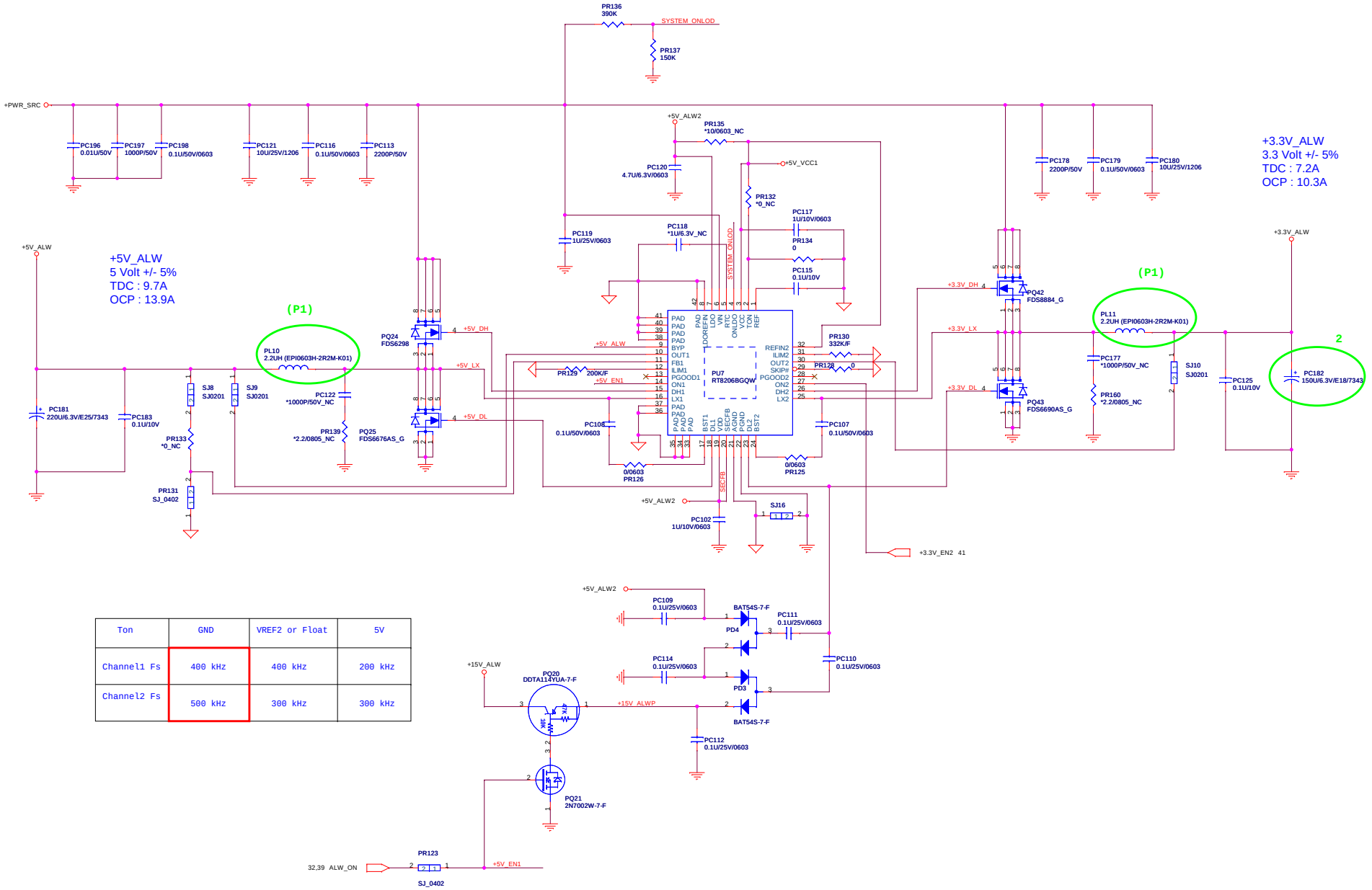
Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	Charger (BQ24765RUVR)	1A

Date: Wednesday, January 19, 2011 Sheet 44 of 61



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51427ARHBR)	1A

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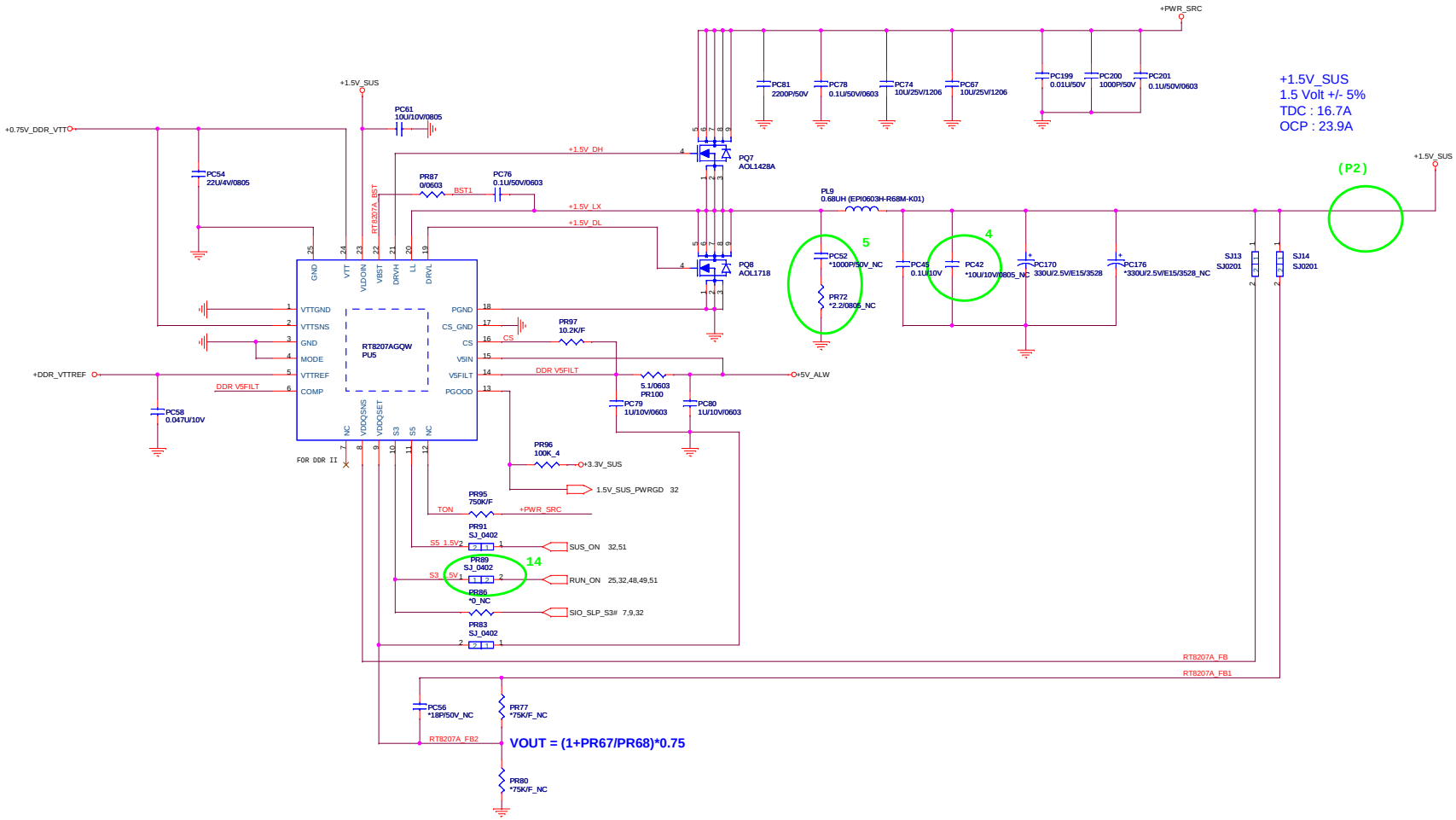


VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

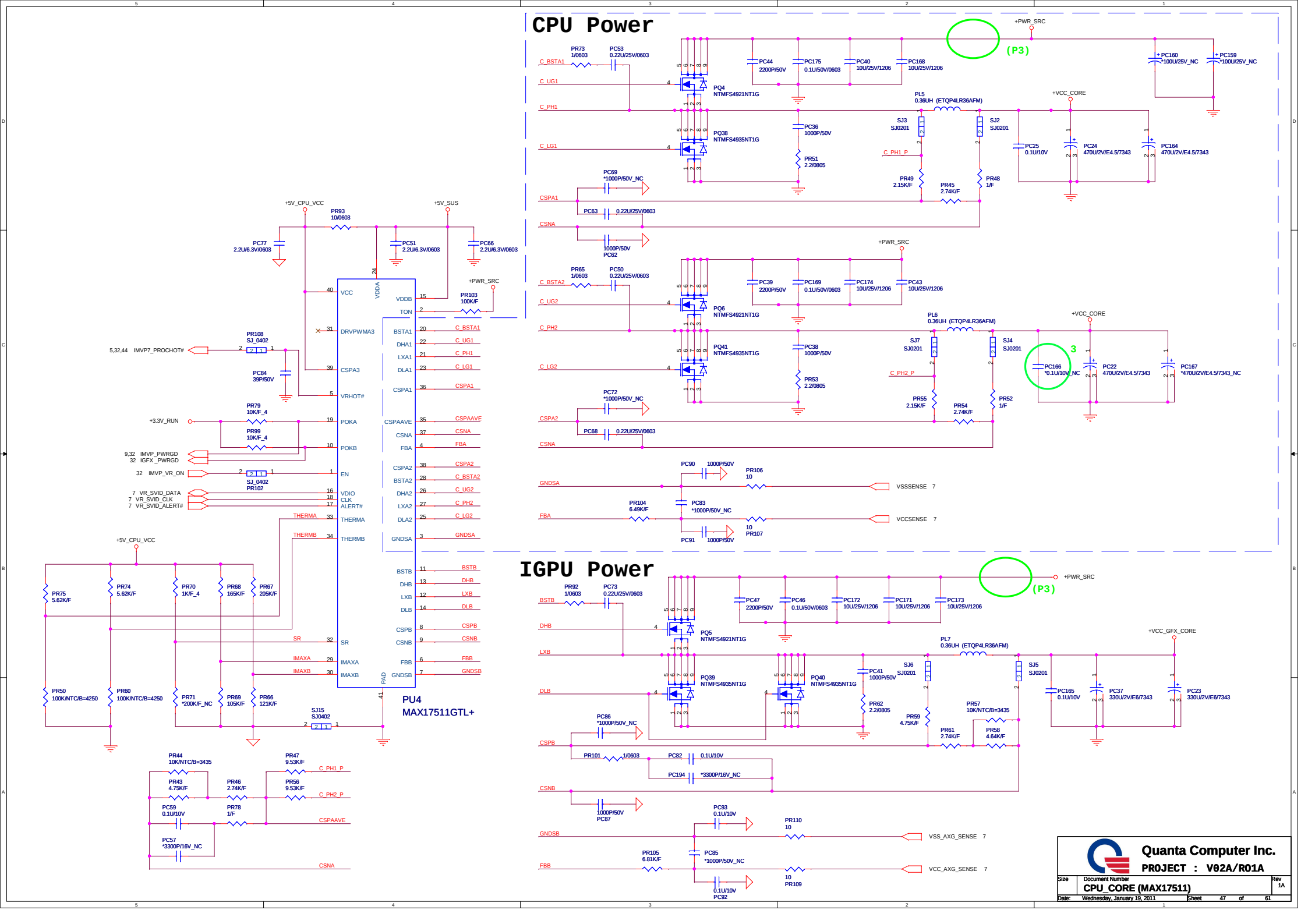
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : V02A/R01A
Size | Document Number: 1.5_SUS/0.75_DDR_VTT (RT8207AGQW) | Rev 1A
Date: Wednesday, January 19, 2011 | Sheet 46 of 61


CPU Power
IGPU Power
PU4
MAX17511GTL+
+5V_CPU_VCC
+5V_SUS
+PWR_SRC
+VCC_CORE
+VCC_GFX_CORE
(P3)
Quanta Computer Inc.
PROJECT : V02A/R01A
CPU_CORE (MAX17511)
Size
Document Number
Rev
1A
Date: Wednesday, January 19, 2011
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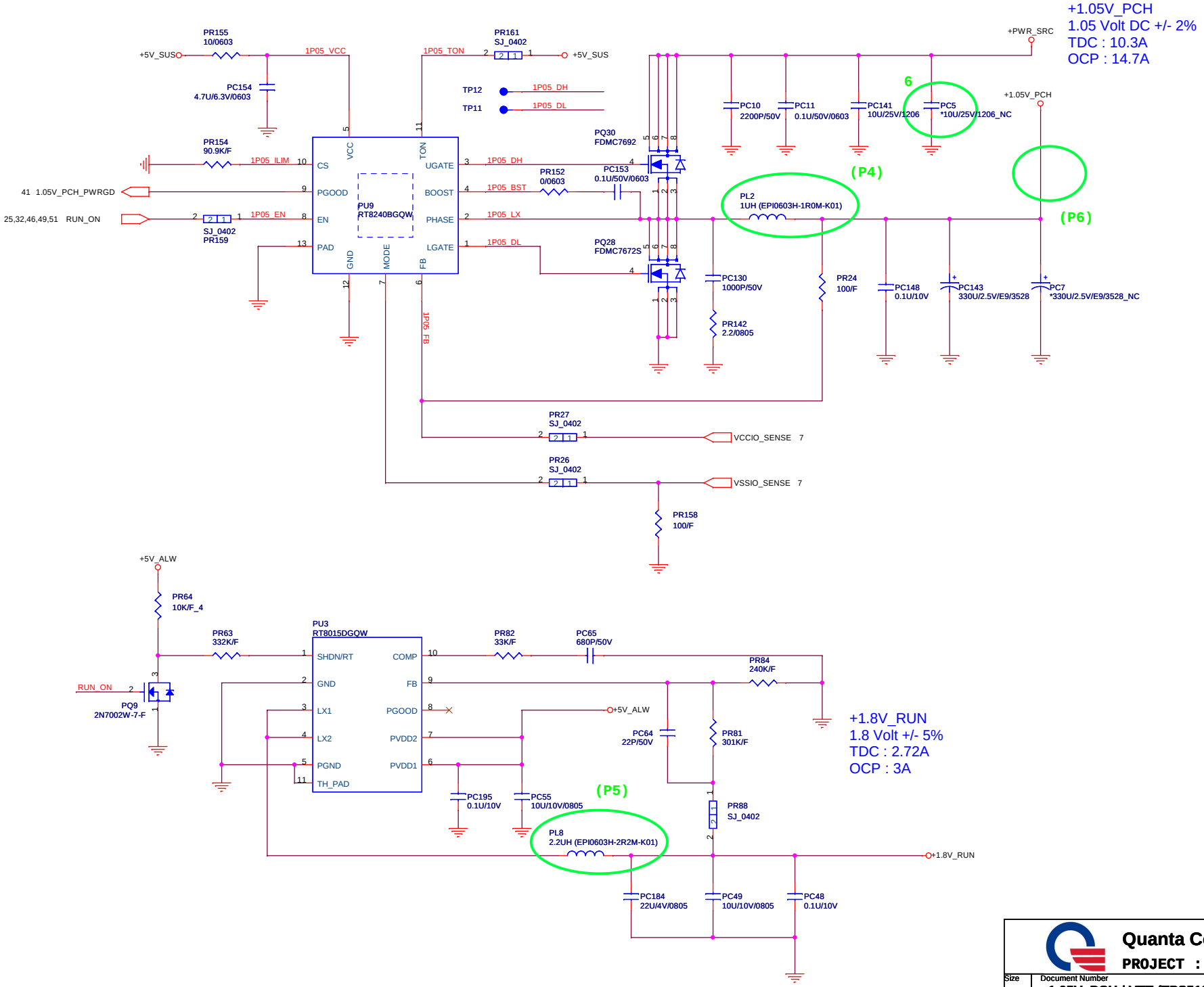
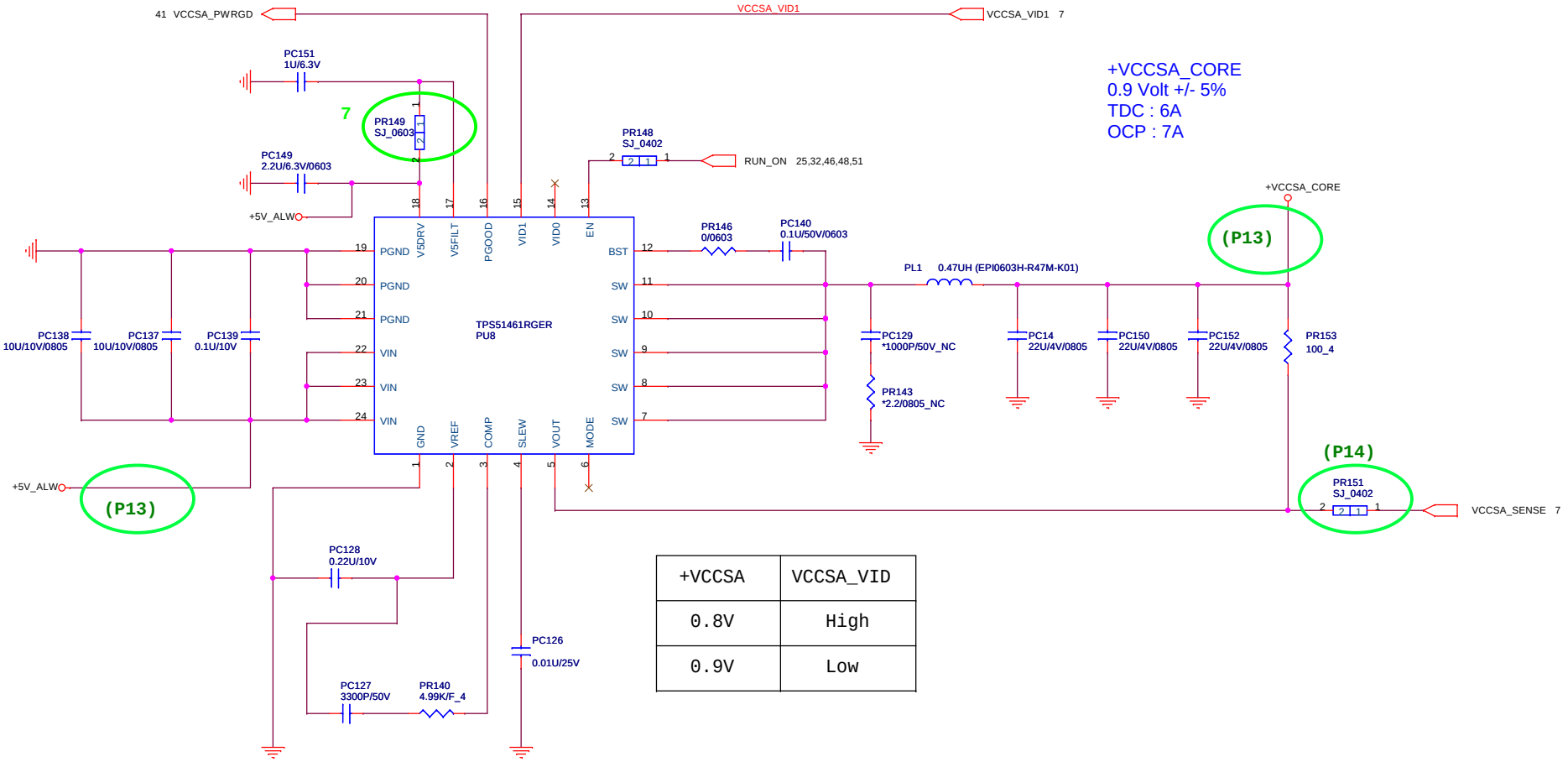


Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	+1.05V_PCH / VTT (TPS51218DSCR)	1A

Date: Wednesday, January 19, 2011 Sheet 48 of 61



+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

PROJECT : V02A/R01A

Size	Document Number	Rev
	VCCSA (ISL95870A)	1A

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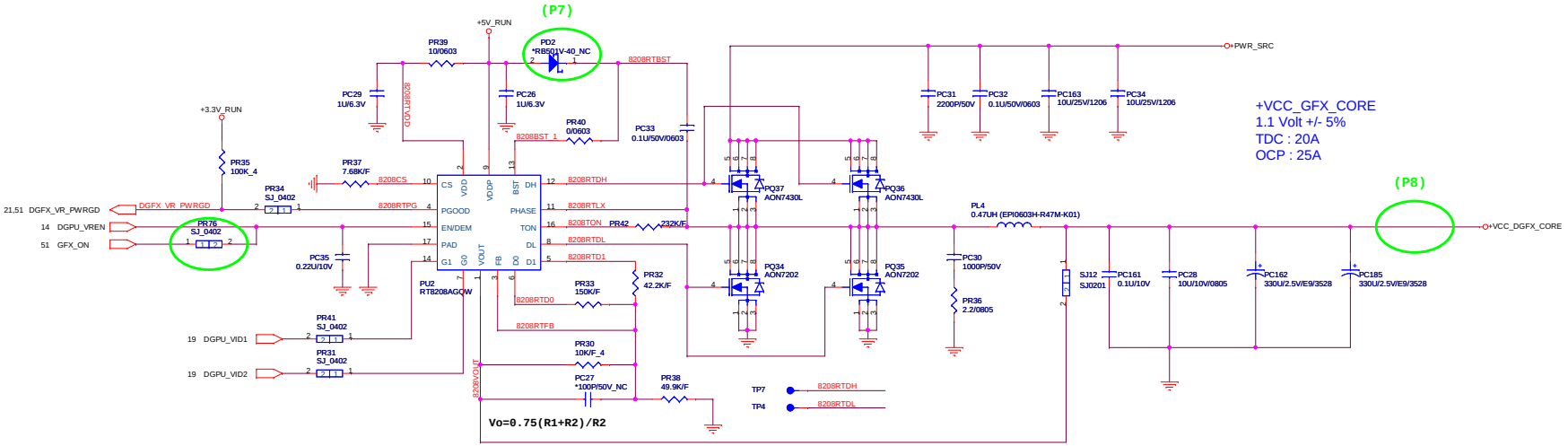


Robson_XT

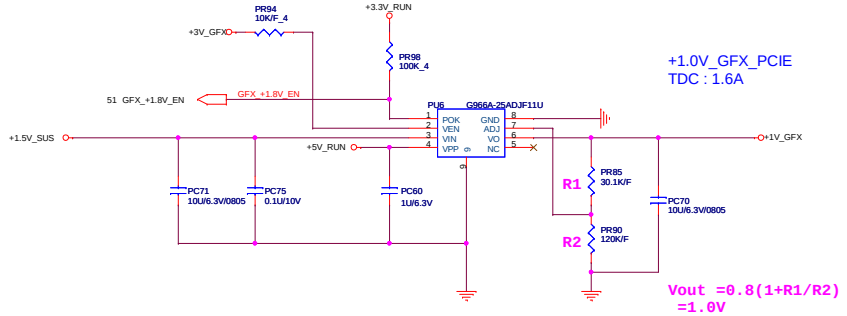
DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

Whistler_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

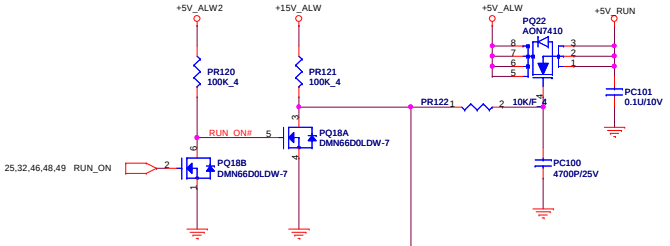
Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	**Part No.**	**Value**
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K

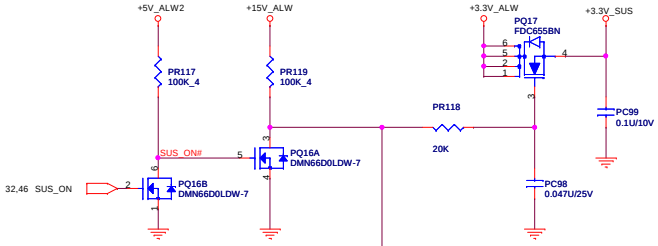


Quanta Computer Inc.
PROJECT : V02A/R01A
Size | Document Number: dGFX_CORE (RT8208A) | Rev 1A
Date: Wednesday, January 19, 2011 | Sheet 50 of 61

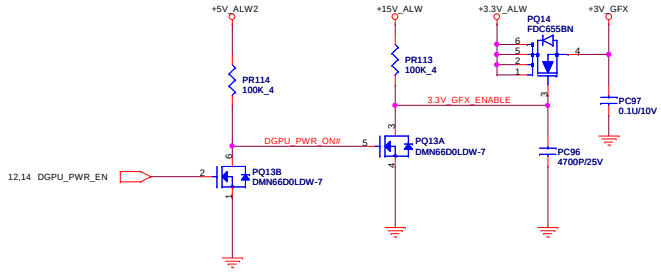
+5V_RUN
Max Current : 2.69A



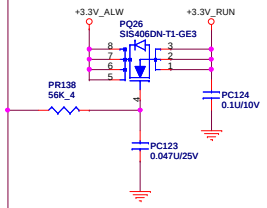
+3.3V_SUS
Max Current : 1.28A



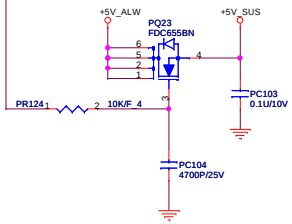
+3V_GFX
Max Current : 60mA



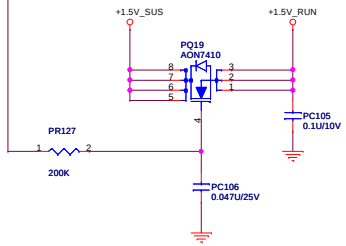
+3.3V_RUN
Max Current : 4.32A



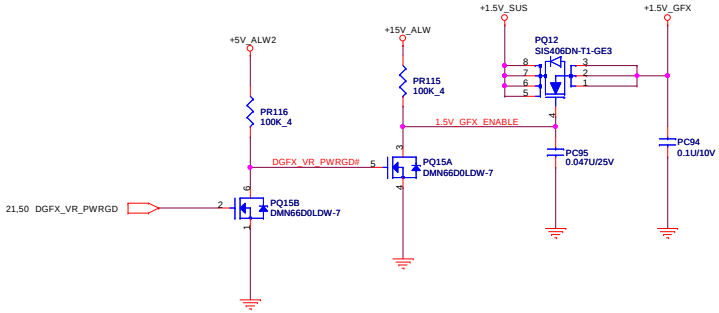
+5V_SUS
Max Current : 0.1A



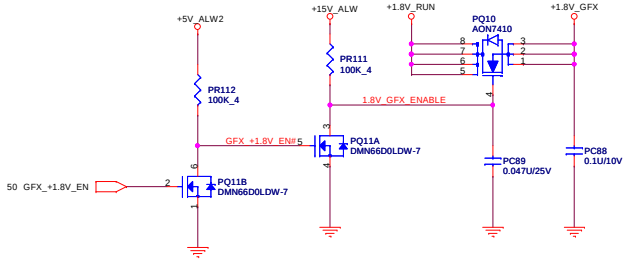
+1.5V_RUN
Max Current : 1.16A

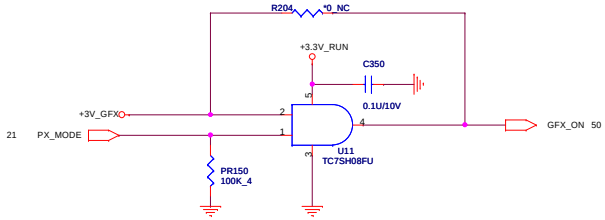


+1.5V_GFX
Max Current : 3.6A



+1.8V_GFX
Max Current : 2.5A





Reserve for support BACO mode
Power sequence control +3V_GFX>+VCC_DGFX_CORE

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Load Switch	1A

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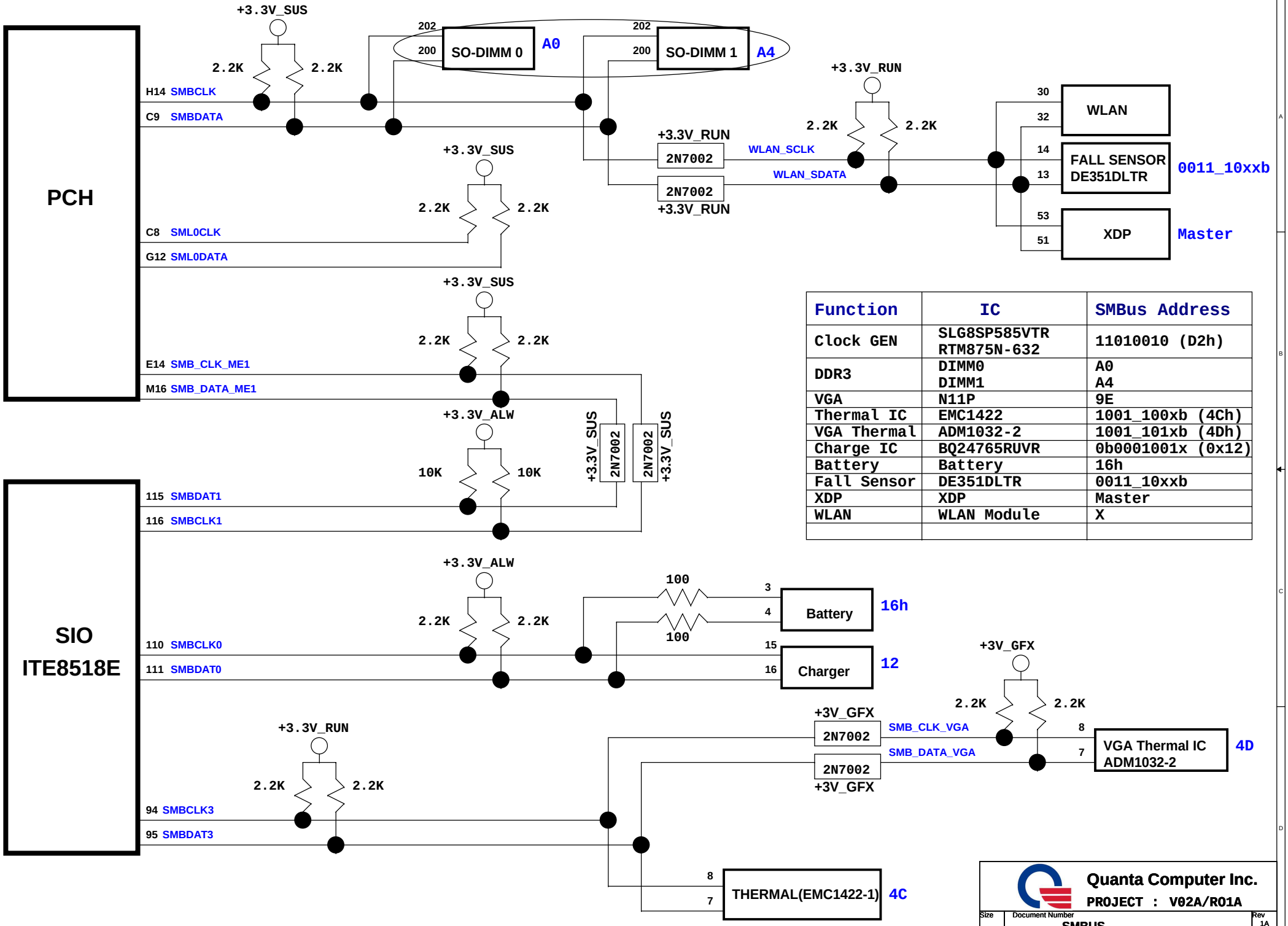

Function	IC	SMBus Address
Clock GEN	SLG8SP585VTR RTM875N-632	11010010 (D2h)
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC1422	1001_100xb (4Ch)
VGA Thermal	ADM1032-2	1001_101xb (4Dh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011_10xxb
XDP	XDP	Master
WLAN	WLAN Module	X

Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	SMBUS	1A

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