

DQDN15 AMD QUEEN M12 Muxless /UMA Schematics Document

AMD LIANO APU FS1 AMD GPU Seymour XT

FCH HUDSON M3 PCB 10246-1 2011-05-28 REV : A00

*DY :None Installed
UMA_PX:UMA and Muxless platform installed
DIS_PX:DIS and Muxless platform installed
PX:Muxless platform installed
FCH_UMA_PX:UMA_PX CRT FCH output
Whistler: For 8 X Vram
DN15: For DN15*

DQ15 AMD DIS SAMSUNG TI

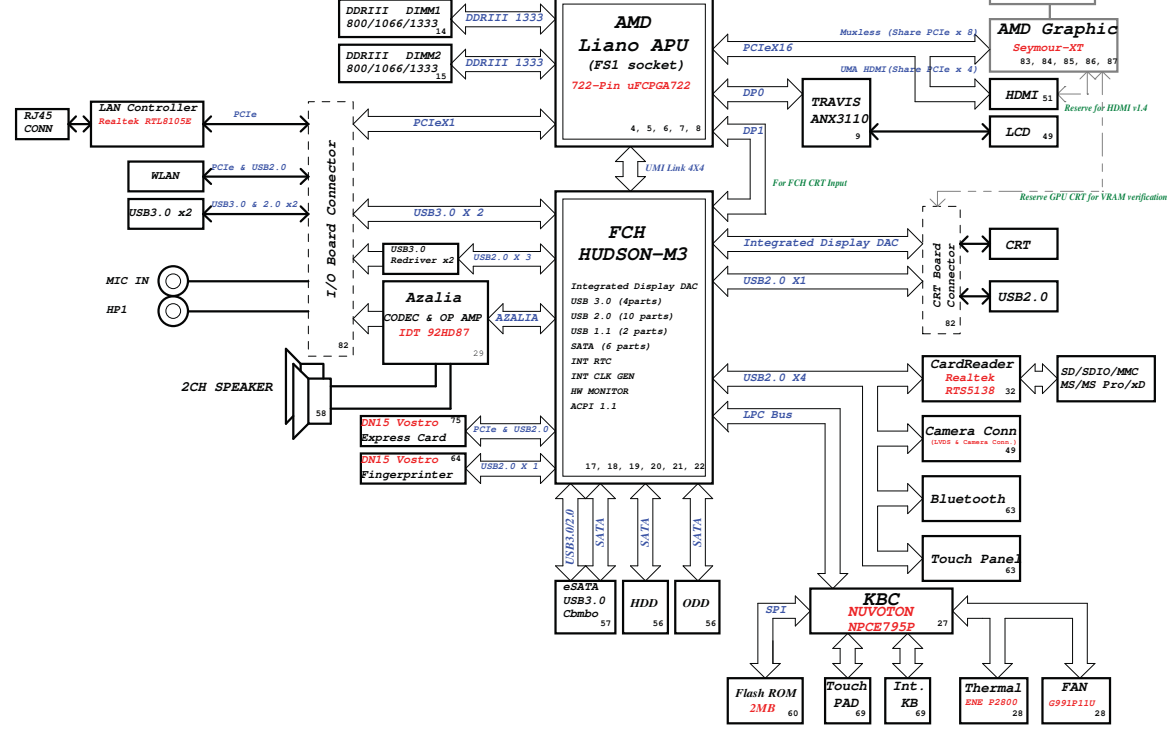


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Project code : 91.4IE01.001
 Part Number : 48.4IE04.0SA DQDN15 QUEEN AMD M12 UMA/Muxless DIS 15'
 PCB P/N : 10246-SB
 Revision : SB



CHARGER	
BQ24745	40
INPUTS	OUTPUTS
AD+	DCBATOUT
SYSTEM DC/DC	
TPS51123	
INPUTS	OUTPUTS
DCBATOUT	3D3V AUX S5 5V AUX S5 5V S5 3D3V S5
APU Core/NB Power	
ISL6267HRT-T	
INPUTS	OUTPUTS
DCBATOUT	APU VDD APU VDDNB
DDRIII SUS	
TPS51116RGER	
INPUTS	OUTPUTS
DCBATOUT	1D5V S3
DDRIII VTT	
TPS51116RGER	
INPUTS	OUTPUTS
DCBATOUT	0D75V S0
APU VDDR/VDDP	
RT8209	
INPUTS	OUTPUTS
DCBATOUT	1D2V S0
AMD FCH CORE Power	
RT8209	
INPUTS	OUTPUTS
DCBATOUT	1D1V S5
AMD GPU CORE	
RT8208B	
INPUTS	OUTPUTS
DCBATOUT	VGA CORE PWR
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Bottom	

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File: **Block Diagram**

Doc: Custom Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**

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Strapping

No Fusion Config, Strap Not needed, but reserve

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM	Allow PCIe GEN2 DEFAULT	SS_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM DEFAULT	Force PCIe GEN1	SS_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB Debug Port / CRT USB 2.0
1	Mini Card (WLAN)
2	Fingerprint
3	WWAN
4	Bluetooth
5	Touch Panel
6	eSATA/USB-Charger
7	CCD Camera
8	New Card
9	CardReader
10	USB 3.0 port 1
11	USB 3.0 port 2
12	USB 3.0 port 3
13	USB 3.0 port 4

PCIe Routing

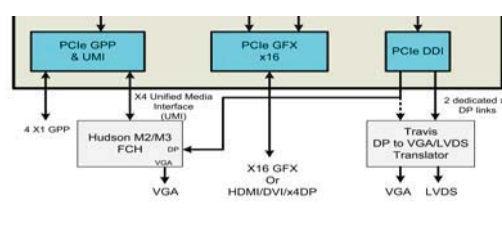
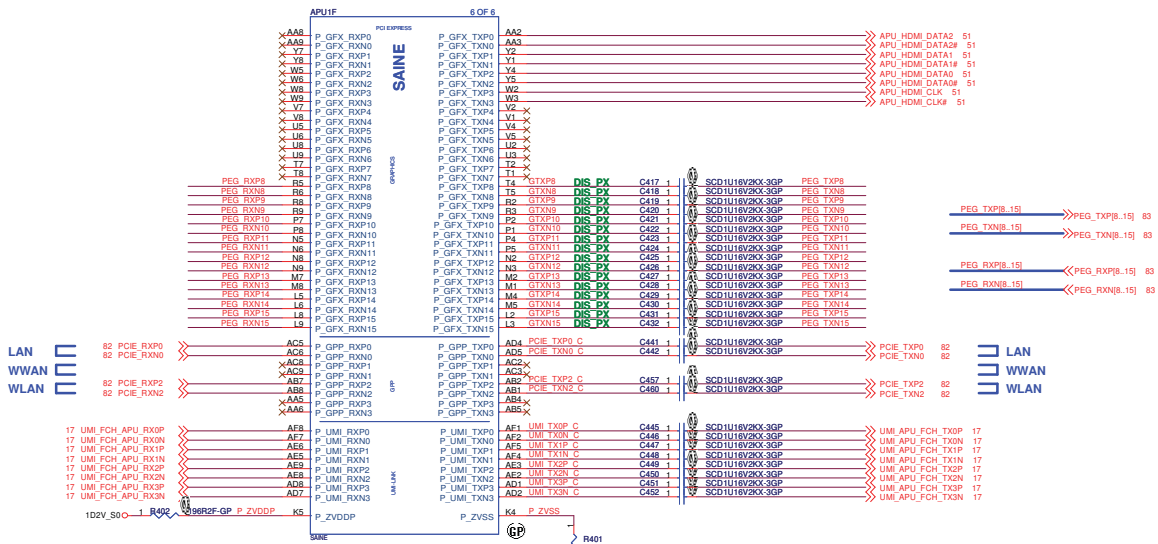
APU	
LANE0	LAN
LANE1	WWAN
LANE2	WLAN
LANE3	CardReader

FCH	
LANE0	
LANE1	Express-Card
LANE2	
LANE3	

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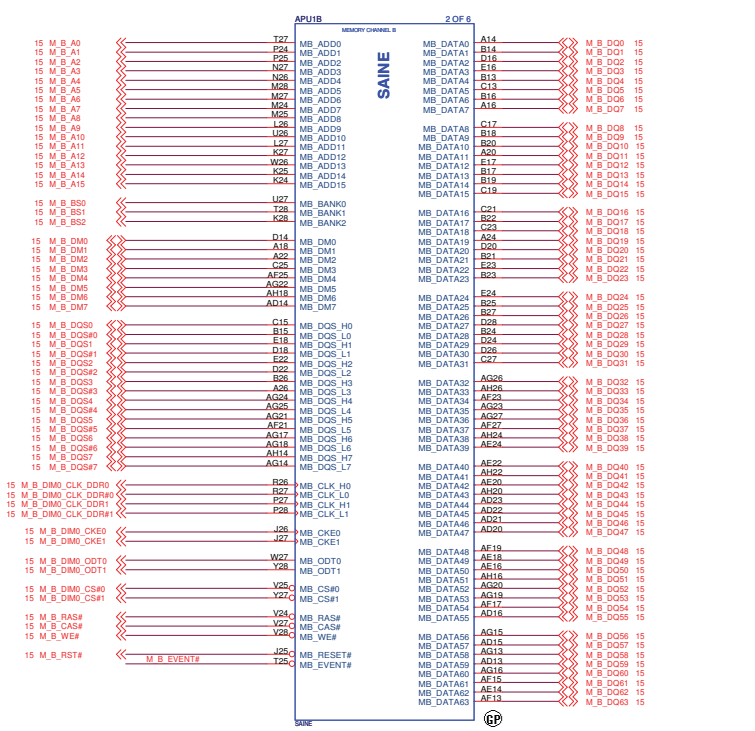
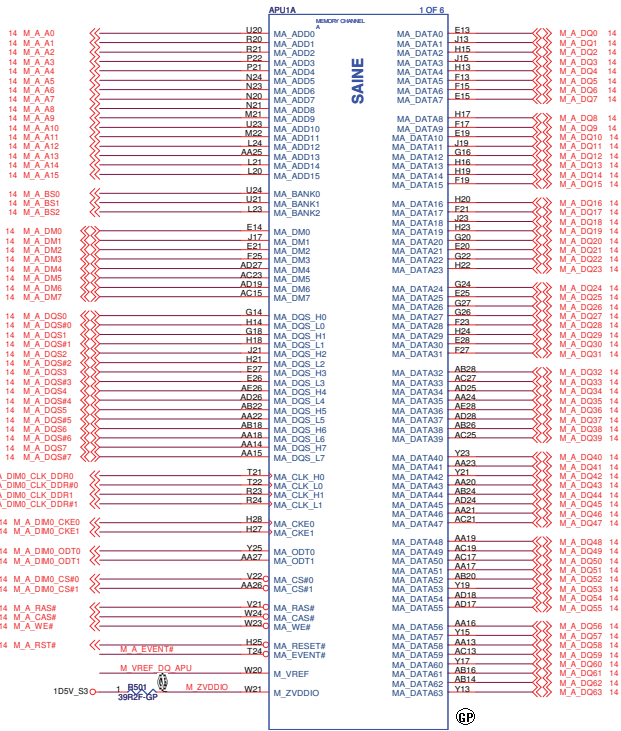
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Rev: **QUEEN AMD Muxless/UMA00**

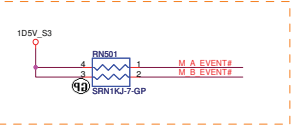
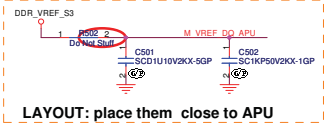
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APU_VREF_DQ



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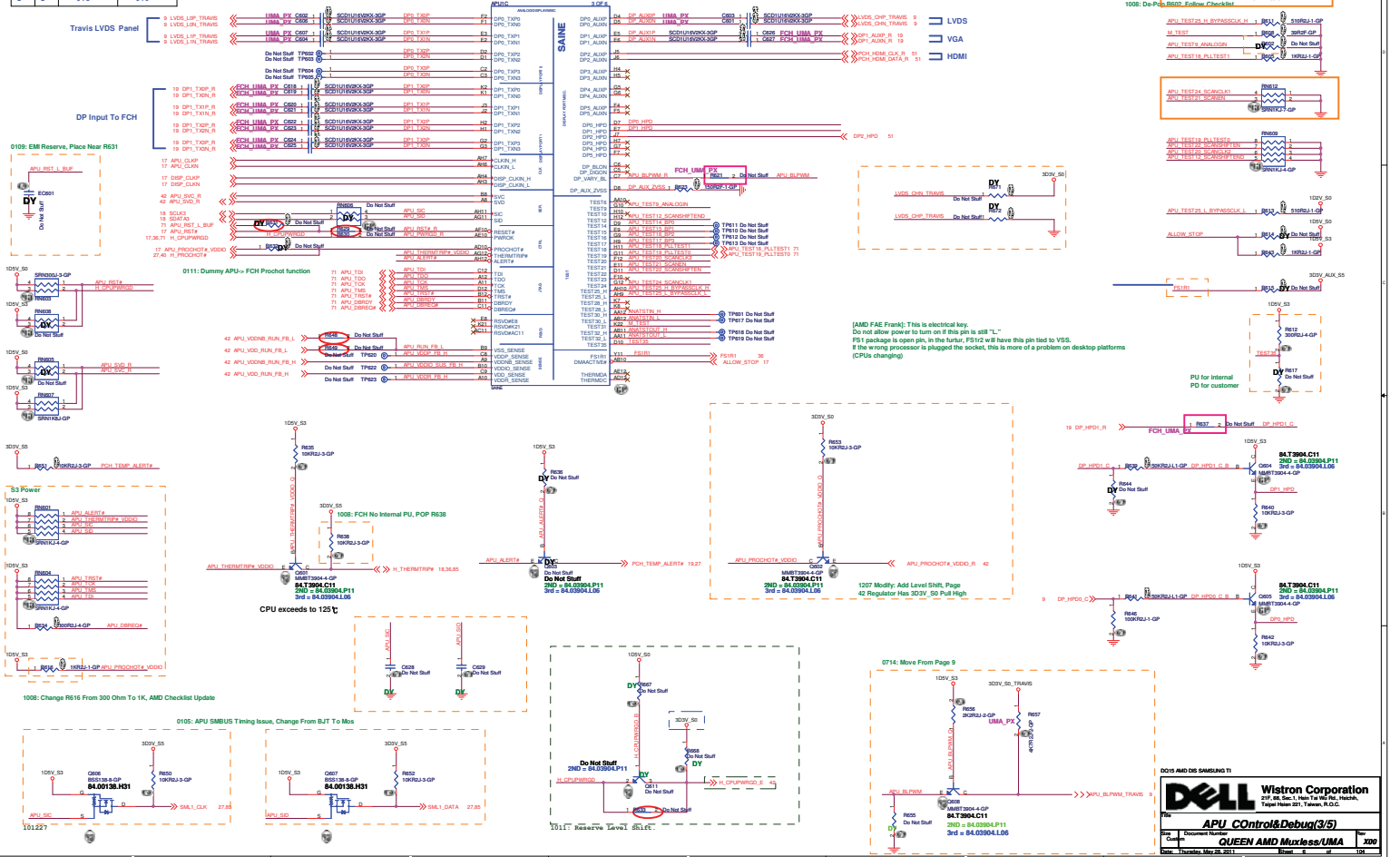
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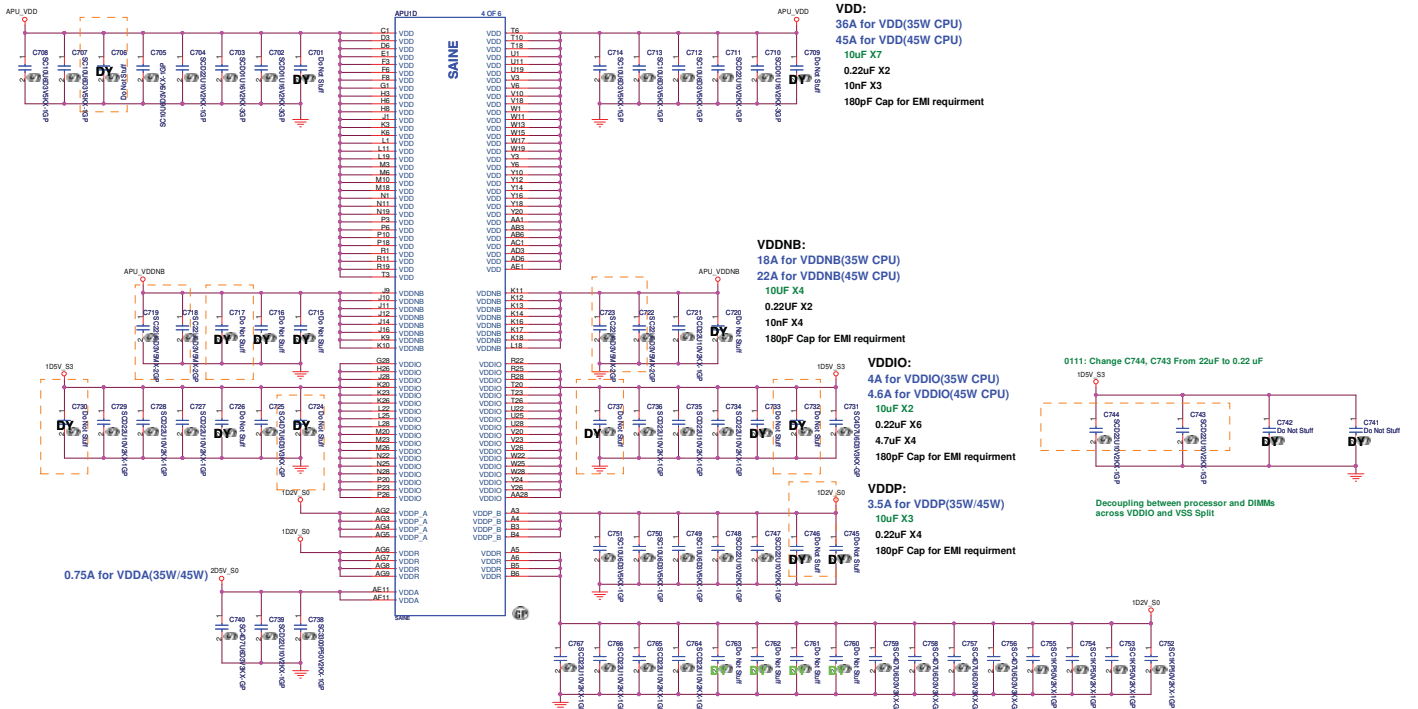
SVC	SVD	Boot Voltage (VDD)	Boot Voltage (VDD)
0	0	1.1	1.1
0	1	1.15	1.2
1	0	0.9	0.9
1	1	0.8	0.9

G112: Change To 2 Single 1.8K 0402 for layout routing.



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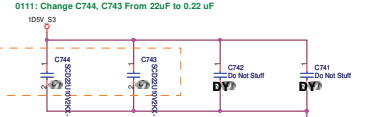
DELL W1000 Corporation
 217 St. Clair, New York, N.Y. 14856
 T800-347-4643
APU Control & Debug (3/5)
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VDD:
 36A for VDD(35W CPU)
 45A for VDD(45W CPU)
 10uF X7
 0.22uF X2
 10nF X3
 180pF Cap for EMI requirement

VDDNB:
 18A for VDDNB(35W CPU)
 22A for VDDNB(45W CPU)
 10uF X4
 0.22uF X2
 10nF X4
 180pF Cap for EMI requirement

VDDIO:
 4A for VDDIO(35W CPU)
 4.6A for VDDIO(45W CPU)
 10uF X2
 0.22uF X6
 4.7uF X4
 180pF Cap for EMI requirement



Decoupling between processor and DIMMs across VDDIO and VSS Split

VDDP:
 3.5A for VDDP(35W/45W)
 10uF X3
 0.22uF X4
 180pF Cap for EMI requirement

VDDR:
 3A for VDDR(35W)
 3.5A for VDDR(45W)
 4.7uF X4
 0.22uF X4
 1nF X4
 180pF Cap for EMI requirement

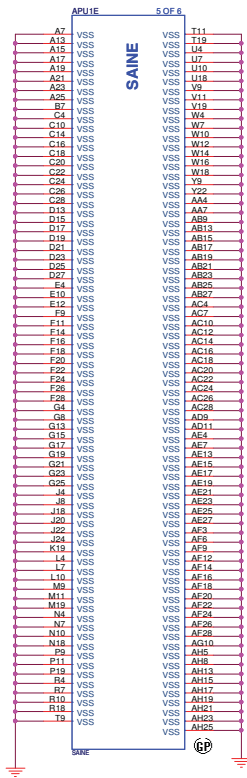
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Rev: **APU Power(4/5)**

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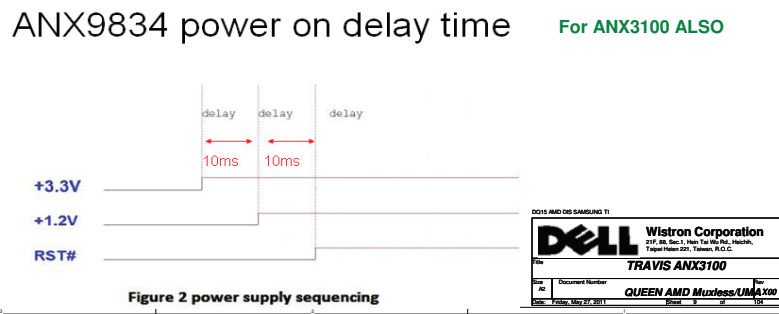
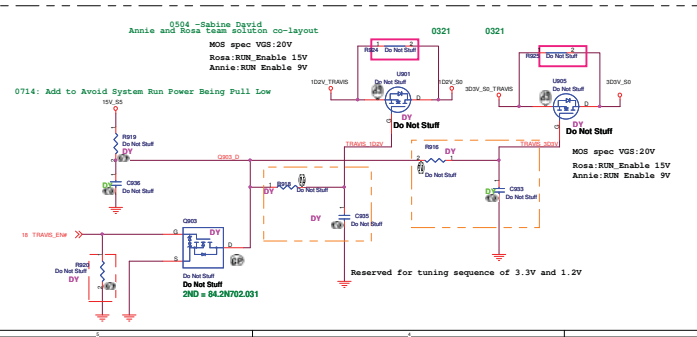
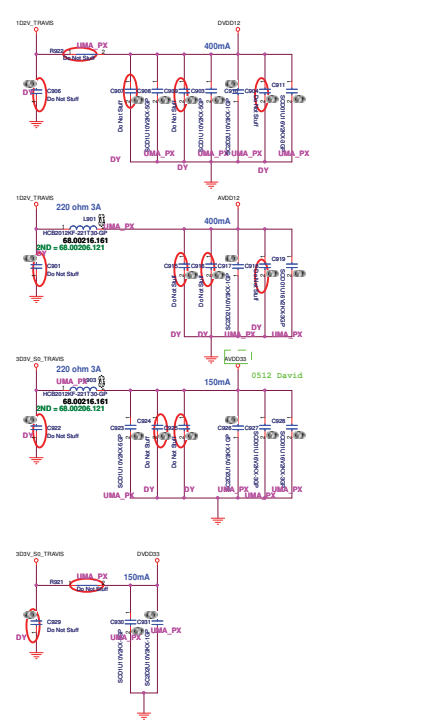
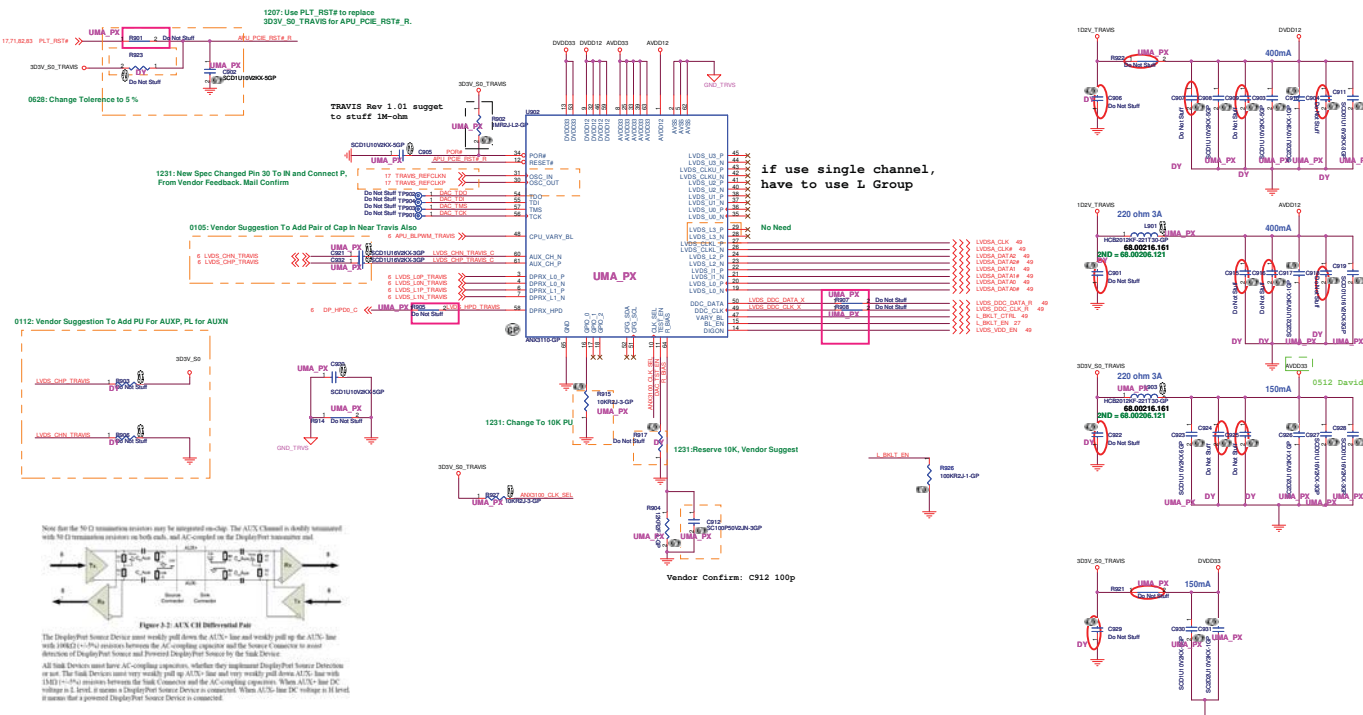
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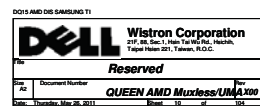
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		APU VSS(5/5)	
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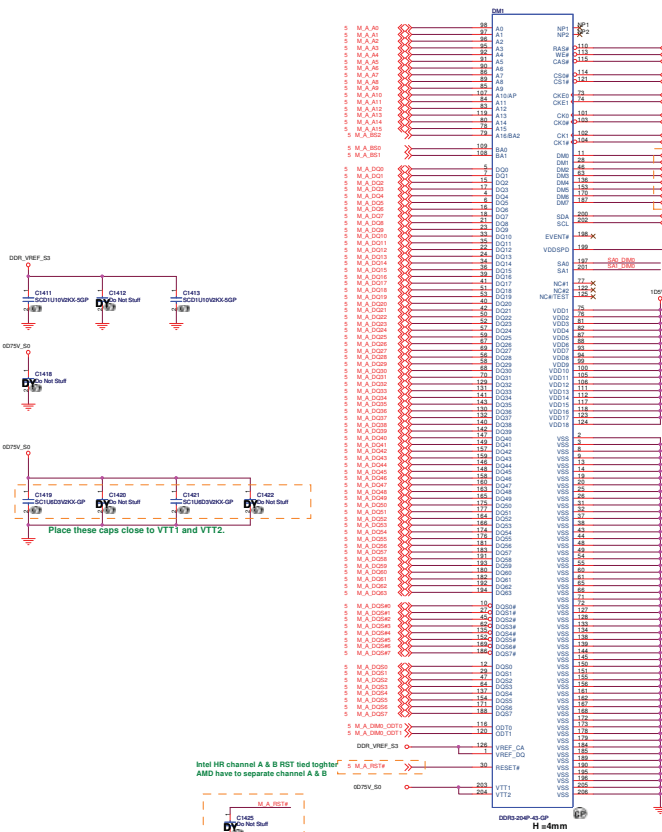
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SSID = MEMORY



Signal	Pin	Signal	Pin
M.A.A0	1	M.A.A0	1
M.A.A1	2	M.A.A1	2
M.A.A2	3	M.A.A2	3
M.A.A3	4	M.A.A3	4
M.A.A4	5	M.A.A4	5
M.A.A5	6	M.A.A5	6
M.A.A6	7	M.A.A6	7
M.A.A7	8	M.A.A7	8
M.A.A8	9	M.A.A8	9
M.A.A9	10	M.A.A9	10
M.A.A10	11	M.A.A10	11
M.A.A11	12	M.A.A11	12
M.A.A12	13	M.A.A12	13
M.A.A13	14	M.A.A13	14
M.A.A14	15	M.A.A14	15
M.A.A15	16	M.A.A15	16
M.A.A16	17	M.A.A16	17
M.A.A17	18	M.A.A17	18
M.A.A18	19	M.A.A18	19
M.A.A19	20	M.A.A19	20
M.A.A20	21	M.A.A20	21
M.A.A21	22	M.A.A21	22
M.A.A22	23	M.A.A22	23
M.A.A23	24	M.A.A23	24
M.A.A24	25	M.A.A24	25
M.A.A25	26	M.A.A25	26
M.A.A26	27	M.A.A26	27
M.A.A27	28	M.A.A27	28
M.A.A28	29	M.A.A28	29
M.A.A29	30	M.A.A29	30
M.A.A30	31	M.A.A30	31
M.A.A31	32	M.A.A31	32
M.A.A32	33	M.A.A32	33
M.A.A33	34	M.A.A33	34
M.A.A34	35	M.A.A34	35
M.A.A35	36	M.A.A35	36
M.A.A36	37	M.A.A36	37
M.A.A37	38	M.A.A37	38
M.A.A38	39	M.A.A38	39
M.A.A39	40	M.A.A39	40
M.A.A40	41	M.A.A40	41
M.A.A41	42	M.A.A41	42
M.A.A42	43	M.A.A42	43
M.A.A43	44	M.A.A43	44
M.A.A44	45	M.A.A44	45
M.A.A45	46	M.A.A45	46
M.A.A46	47	M.A.A46	47
M.A.A47	48	M.A.A47	48
M.A.A48	49	M.A.A48	49
M.A.A49	50	M.A.A49	50
M.A.A50	51	M.A.A50	51
M.A.A51	52	M.A.A51	52
M.A.A52	53	M.A.A52	53
M.A.A53	54	M.A.A53	54
M.A.A54	55	M.A.A54	55
M.A.A55	56	M.A.A55	56
M.A.A56	57	M.A.A56	57
M.A.A57	58	M.A.A57	58
M.A.A58	59	M.A.A58	59
M.A.A59	60	M.A.A59	60
M.A.A60	61	M.A.A60	61
M.A.A61	62	M.A.A61	62
M.A.A62	63	M.A.A62	63
M.A.A63	64	M.A.A63	64
M.A.A64	65	M.A.A64	65
M.A.A65	66	M.A.A65	66
M.A.A66	67	M.A.A66	67
M.A.A67	68	M.A.A67	68
M.A.A68	69	M.A.A68	69
M.A.A69	70	M.A.A69	70
M.A.A70	71	M.A.A70	71
M.A.A71	72	M.A.A71	72
M.A.A72	73	M.A.A72	73
M.A.A73	74	M.A.A73	74
M.A.A74	75	M.A.A74	75
M.A.A75	76	M.A.A75	76
M.A.A76	77	M.A.A76	77
M.A.A77	78	M.A.A77	78
M.A.A78	79	M.A.A78	79
M.A.A79	80	M.A.A79	80
M.A.A80	81	M.A.A80	81
M.A.A81	82	M.A.A81	82
M.A.A82	83	M.A.A82	83
M.A.A83	84	M.A.A83	84
M.A.A84	85	M.A.A84	85
M.A.A85	86	M.A.A85	86
M.A.A86	87	M.A.A86	87
M.A.A87	88	M.A.A87	88
M.A.A88	89	M.A.A88	89
M.A.A89	90	M.A.A89	90
M.A.A90	91	M.A.A90	91
M.A.A91	92	M.A.A91	92
M.A.A92	93	M.A.A92	93
M.A.A93	94	M.A.A93	94
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M.A.A95	96	M.A.A95	96
M.A.A96	97	M.A.A96	97
M.A.A97	98	M.A.A97	98
M.A.A98	99	M.A.A98	99
M.A.A99	100	M.A.A99	100
M.A.A100	101	M.A.A100	101
M.A.A101	102	M.A.A101	102
M.A.A102	103	M.A.A102	103
M.A.A103	104	M.A.A103	104
M.A.A104	105	M.A.A104	105
M.A.A105	106	M.A.A105	106
M.A.A106	107	M.A.A106	107
M.A.A107	108	M.A.A107	108
M.A.A108	109	M.A.A108	109
M.A.A109	110	M.A.A109	110
M.A.A110	111	M.A.A110	111
M.A.A111	112	M.A.A111	112
M.A.A112	113	M.A.A112	113
M.A.A113	114	M.A.A113	114
M.A.A114	115	M.A.A114	115
M.A.A115	116	M.A.A115	116
M.A.A116	117	M.A.A116	117
M.A.A117	118	M.A.A117	118
M.A.A118	119	M.A.A118	119
M.A.A119	120	M.A.A119	120
M.A.A120	121	M.A.A120	121
M.A.A121	122	M.A.A121	122
M.A.A122	123	M.A.A122	123
M.A.A123	124	M.A.A123	124
M.A.A124	125	M.A.A124	125
M.A.A125	126	M.A.A125	126
M.A.A126	127	M.A.A126	127
M.A.A127	128	M.A.A127	128
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M.A.A129	130	M.A.A129	130
M.A.A130	131	M.A.A130	131
M.A.A131	132	M.A.A131	132
M.A.A132	133	M.A.A132	133
M.A.A133	134	M.A.A133	134
M.A.A134	135	M.A.A134	135
M.A.A135	136	M.A.A135	136
M.A.A136	137	M.A.A136	137
M.A.A137	138	M.A.A137	138
M.A.A138	139	M.A.A138	139
M.A.A139	140	M.A.A139	140
M.A.A140	141	M.A.A140	141
M.A.A141	142	M.A.A141	142
M.A.A142	143	M.A.A142	143
M.A.A143	144	M.A.A143	144
M.A.A144	145	M.A.A144	145
M.A.A145	146	M.A.A145	146
M.A.A146	147	M.A.A146	147
M.A.A147	148	M.A.A147	148
M.A.A148	149	M.A.A148	149
M.A.A149	150	M.A.A149	150
M.A.A150	151	M.A.A150	151
M.A.A151	152	M.A.A151	152
M.A.A152	153	M.A.A152	153
M.A.A153	154	M.A.A153	154
M.A.A154	155	M.A.A154	155
M.A.A155	156	M.A.A155	156
M.A.A156	157	M.A.A156	157
M.A.A157	158	M.A.A157	158
M.A.A158	159	M.A.A158	159
M.A.A159	160	M.A.A159	160
M.A.A160	161	M.A.A160	161
M.A.A161	162	M.A.A161	162
M.A.A162	163	M.A.A162	163
M.A.A163	164	M.A.A163	164
M.A.A164	165	M.A.A164	165
M.A.A165	166	M.A.A165	166
M.A.A166	167	M.A.A166	167
M.A.A167	168	M.A.A167	168
M.A.A168	169	M.A.A168	169
M.A.A169	170	M.A.A169	170
M.A.A170	171	M.A.A170	171
M.A.A171	172	M.A.A171	172
M.A.A172	173	M.A.A172	173
M.A.A173	174	M.A.A173	174
M.A.A174	175	M.A.A174	175
M.A.A175	176	M.A.A175	176
M.A.A176	177	M.A.A176	177
M.A.A177	178	M.A.A177	178
M.A.A178	179	M.A.A178	179
M.A.A179	180	M.A.A179	180
M.A.A180	181	M.A.A180	181
M.A.A181	182	M.A.A181	182
M.A.A182	183	M.A.A182	183
M.A.A183	184	M.A.A183	184
M.A.A184	185	M.A.A184	185
M.A.A185	186	M.A.A185	186
M.A.A186	187	M.A.A186	187
M.A.A187	188	M.A.A187	188
M.A.A188	189	M.A.A188	189
M.A.A189	190	M.A.A189	190
M.A.A190	191	M.A.A190	191
M.A.A191	192	M.A.A191	192
M.A.A192	193	M.A.A192	193
M.A.A193	194	M.A.A193	194
M.A.A194	195	M.A.A194	195
M.A.A195	196	M.A.A195	196
M.A.A196	197	M.A.A196	197
M.A.A197	198	M.A.A197	198
M.A.A198	199	M.A.A198	199
M.A.A199	200	M.A.A199	200

0019 AMD DS 54830G 11

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21F, 8F, 5th Fl., Hsin Tai Hsiung Rd., Hsinchu, Taiwan, R.O.C.


Part Number: **QUEEN AMD Muxless/UMA**

Doc: **QUEEN AMD Muxless/UMA**

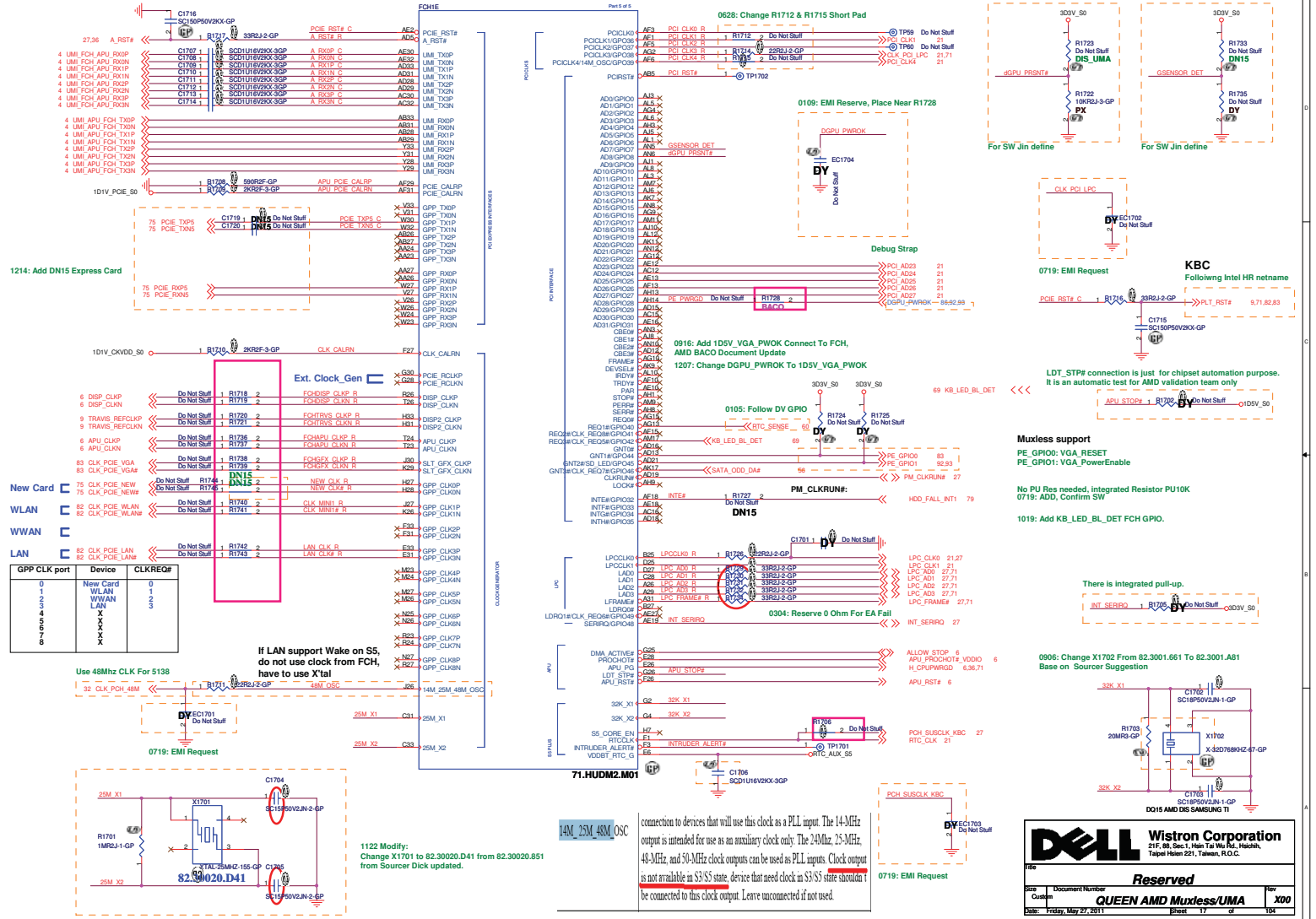
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DQ15 AMD DIS SAMSUNG TI

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Title		Reserved
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
Date:	Thursday, May 26, 2011	Sheet 18 of 104

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21F, 88, Sec.1, Hsin 14th Rd., Hsueh, Taipei 10821, Taiwan, R.O.C.

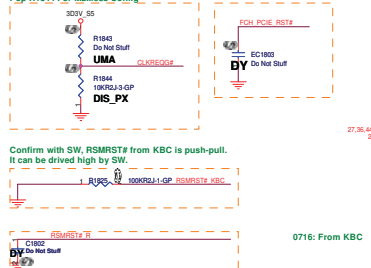
Reserved

Doc# **QUEEN AMD Muxless/UMA** Rev **X00**
Date: Friday, May 27, 2011

0909: Modify Pop R1843 For UMA Config Pop R1844 For Muxless Config

0109: EMI Reserve, Place Near R1810

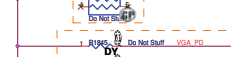
Remove PCIE2_RST, Did Not Use FCH GPP



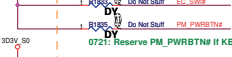
Confirm with SW, RSMRST# from KBC is push-pull. It can be driven high by SW.



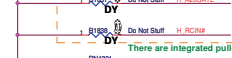
Travis_EN# : Base on AMD suggestion, use the GPIO66 same the CRB first. If it work normally, ask BIOS to re-program to GPIO55 to double verify.



0719: Change From 2.2k and POP



0721: Reserve PIM_PWRBTN# If KBC Change To OD



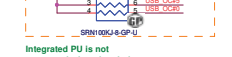
There are integrated pull-up.



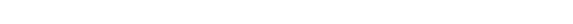
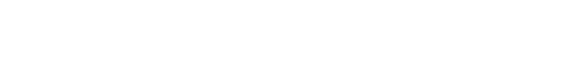
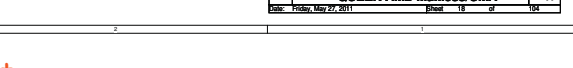
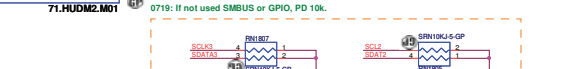
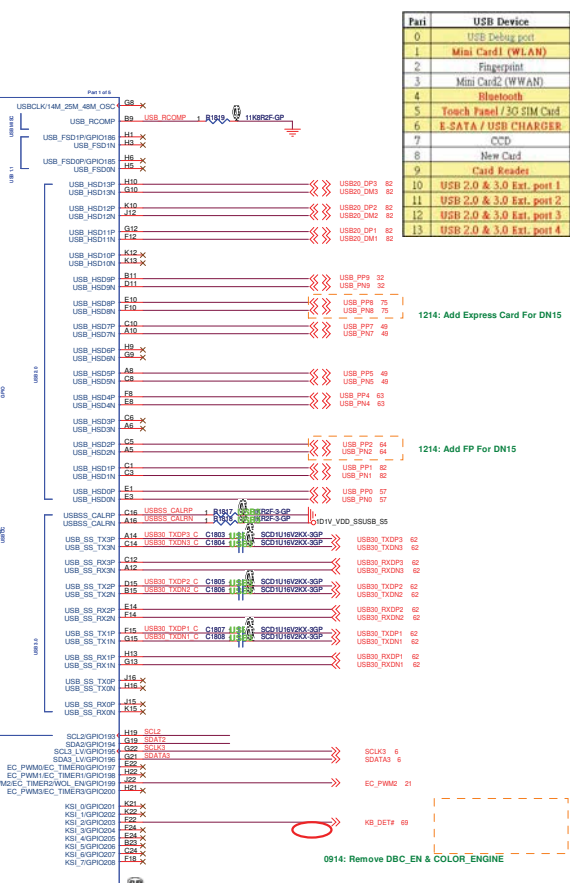
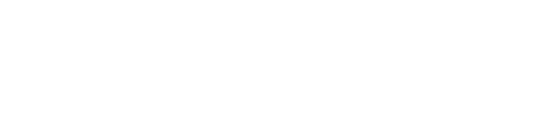
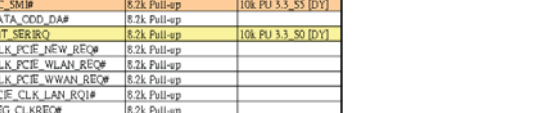
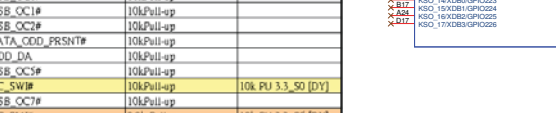
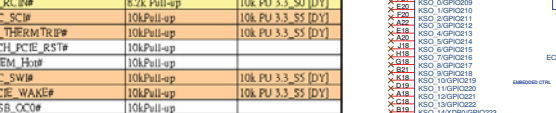
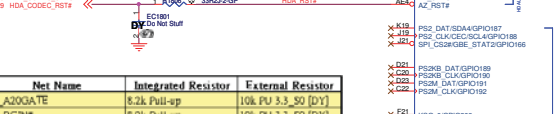
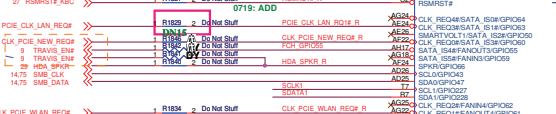
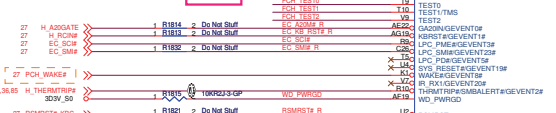
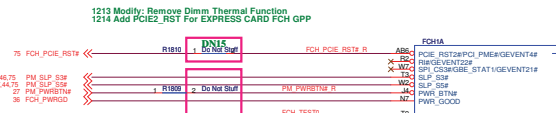
Modify Zero Power ODD circuit by Annie team suggestion.



Checklist suggestion: Don't stuff for default



Integrated PU is not supported when the pin is configured for USB over current function.

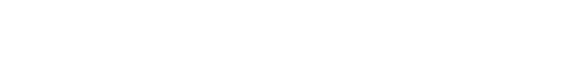
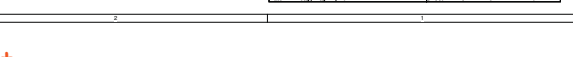
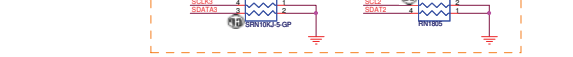
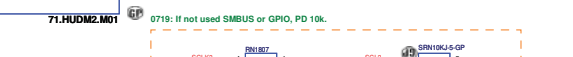


Part	USB Device
0	USB Hub
1	Mini Card1 (WLAN)
2	Fingerprint
3	Mini Card2 (WLAN)
4	Bluetooth
5	Touch Panel / 3G SIM Card
6	E-SATA / USB CHARGER
7	CCD
8	New Card
9	Card Reader
10	USB 2.0 & 3.0 Ext. port 1
11	USB 2.0 & 3.0 Ext. port 2
12	USB 2.0 & 3.0 Ext. port 3
13	USB 2.0 & 3.0 Ext. port 4

1214: Add Express Card For DN15

1214: Add FP For DN15

0914: Remove DBC_EN & COLOR_ENGINE



Function	Net Name	Integrated Resistor	External Resistor
GAZON	H_A20GATE	8.2k Pull-up	10k PU 3.3_30 [DY]
KBRST#	H_RCMP#	8.2k Pull-up	10k PU 3.3_30 [DY]
PWR#	EC_SW#	10k Pull-up	10k PU 3.3_30 [DY]
TRIP_RST#	H_THERMTRIP#	10k Pull-up	10k PU 3.3_30 [DY]
PCIE_RST#	FCH_PCIE_RST#	10k Pull-up	10k PU 3.3_30 [DY]
Event5	MEM_H#	10k Pull-up	
Event6	EC_SW#	10k Pull-up	10k PU 3.3_30 [DY]
WAKE#	PCIE_WAKE#	10k Pull-up	10k PU 3.3_30 [DY]
USB_OC0#	USB_OC0#	10k Pull-up	
USB_OC1#	USB_OC1#	10k Pull-up	
USB_OC2#	USB_OC2#	10k Pull-up	
Event15#	SATA_ODD_PRSNT#	10k Pull-up	
Event16#	ODD_DA	10k Pull-up	
USB_OC3#	USB_OC3#	10k Pull-up	
Event17#	EC_SW#	10k Pull-up	10k PU 3.3_30 [DY]
USB_OC7#	USB_OC7#	10k Pull-up	
LPC_SMI#	EC_SMI#	8.2k Pull-up	10k PU 3.3_30 [DY]
GPIO55	SATA_ODD_DA#	8.2k Pull-up	
SERIRQ	INT_SERIRQ	8.2k Pull-up	10k PU 3.3_30 [DY]
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2k Pull-up	
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2k Pull-up	
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2k Pull-up	
CLK_REQ3	PCIE_CLK_LAN_REQ#	8.2k Pull-up	
CLK_REQ0	PEG_CLKREQ#	8.2k Pull-up	

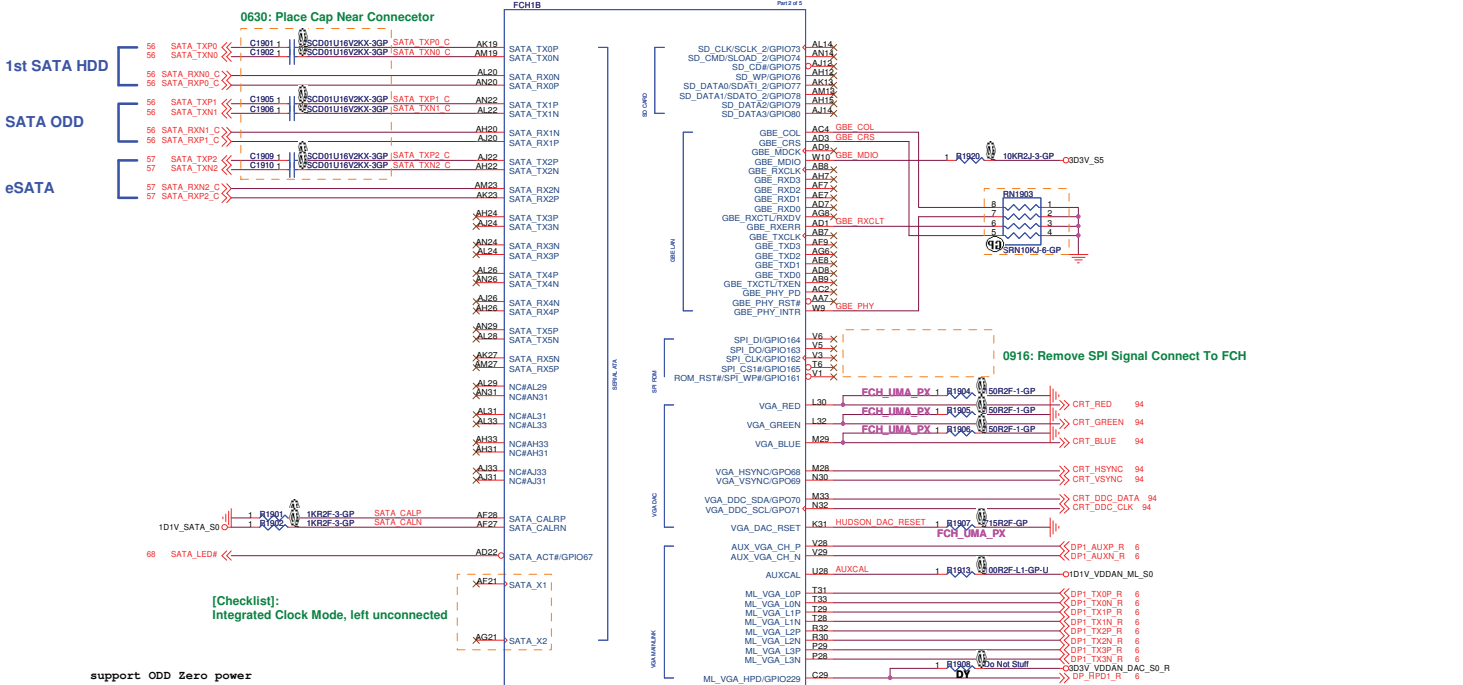
0015 AMD DIS SAMSUNG TI

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Part: **HUDSON-M2(2/6)**

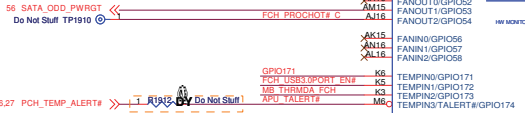
Doc: **QUEEN AMD Muxless/UMA** Rev: **200**

Rev: **1.0** Date: **1/27/2011** Page: **18** of **19**

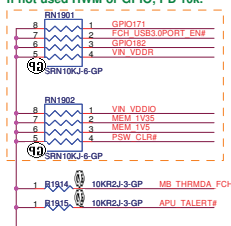


[Checklist]:
Integrated Clock Mode, left unconnected

support ODD Zero power



If not used HWM or GPIO, PD 10k.

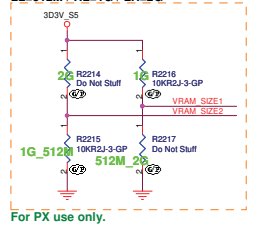


1213 Modify: Remove Dimm Thermal Function
Pop R1914 If function Not used.

71.HUDD2.M01

VDDIO	MEM_1V5	MEM_1V35
1.5V	H	Don't Care
1.35V	L	H

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G



For PX use only.

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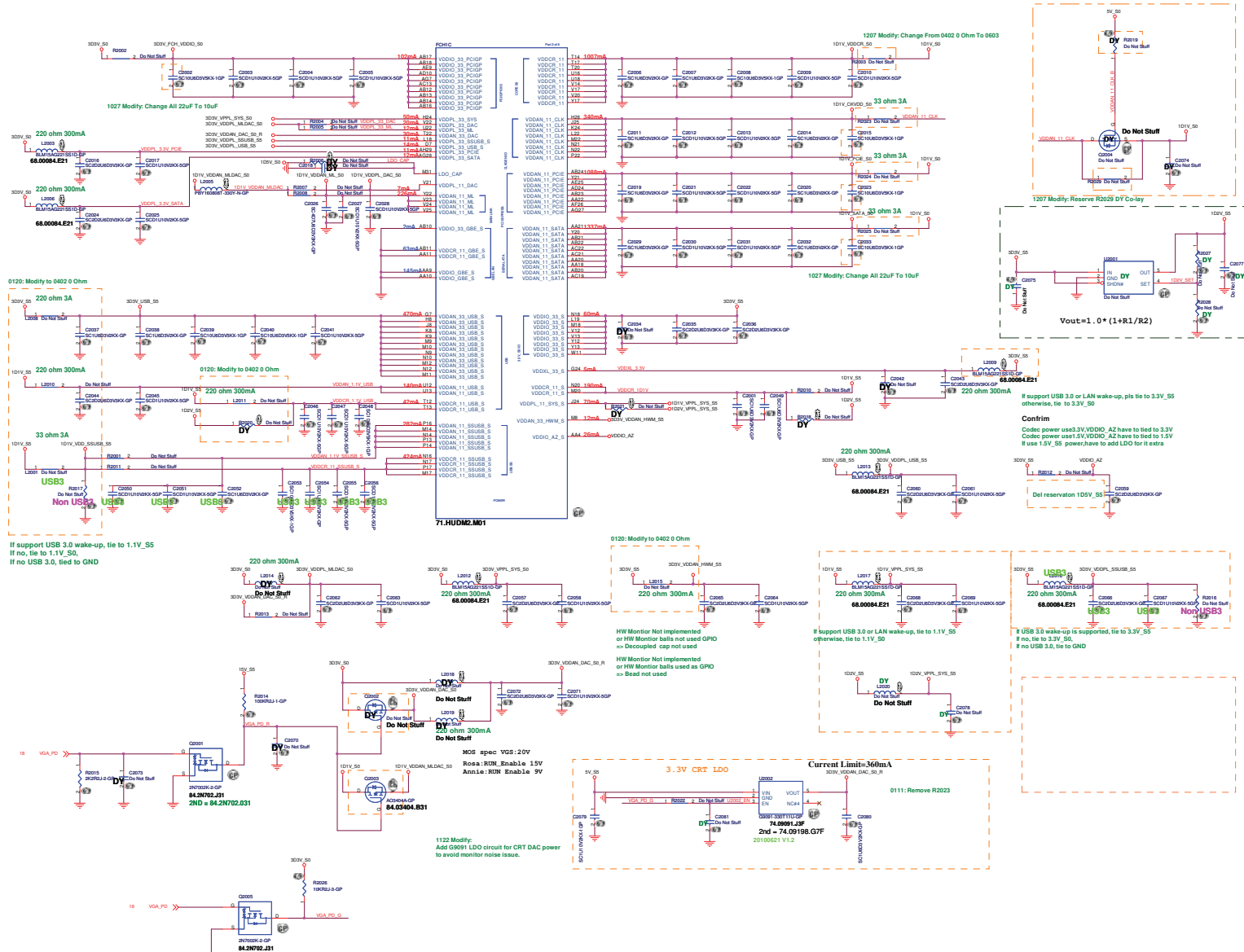
DQ15 AMD DIS SAMSUNG TI

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsein 221, Taiwan, R.O.C.

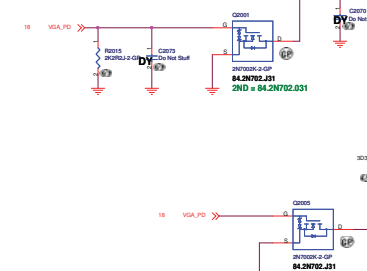
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Size: Document Number **QUEEN AMD Muxless/UMA** Rev **X00**

Date: Thursday, May 28, 2011 Sheet 19 of 104



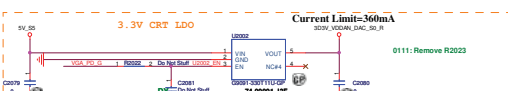
If support USB 3.0 wake-up, tie to 1.1V_SS
 If no, tie to 1.1V_SS
 If no USB 3.0, tied to GND



HW Monitor Not implemented or HW Monitor balls not used GPOD => Decoupled cap not used

If support USB 3.0 or LAN wake-up, pls tie to 3.3V_SS otherwise, tie to 1.1V_SS

If support USB 3.0 or LAN wake-up, pls tie to 3.3V_SS otherwise, tie to 3.3V_SS
 Confirm
 Codec power used 3V_VDDIO_AZ have to tied to 3.3V
 Codec power used 3V_VDDIO_AZ have to tied to 3.3V
 If use 1.5V_SS power, have to add LDO for it extra
 Del reservation 105V_SS



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0019 AMD OS SAMBUNG TI

Wistron Corporation
 21F, 38, Sec. 1, Neihu Tech. Hub,
 Taipei Hsinshui, Taiwan, R.O.C.

Model: **HUDSON-M2 Power(4/6)**

Document Name: **QUEEN AMD Muxless/UMA**

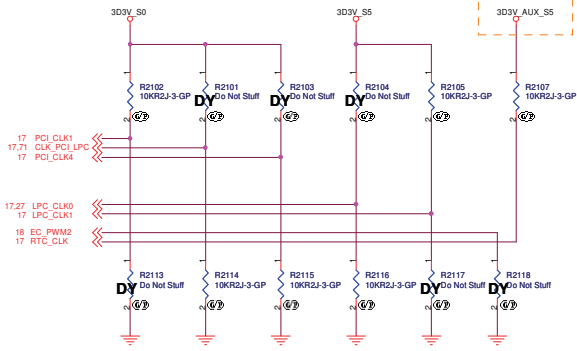
Rev: **XW**

Date: **2016/02/26**

SSID = S.B

REQUIRED STRAPS

CRB: PU to 3.3V_AUX_S5
 Checklist: PU to 3.3V_S5
 Confirm with AMD, follow CRB suggestion



REQUIRED SYSTEM STRAPS

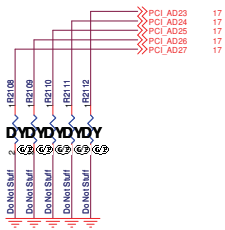
Use this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPIO199	PCI_CLK1	RTC_CLK	CLK_PCH_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	SS_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	SS_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS

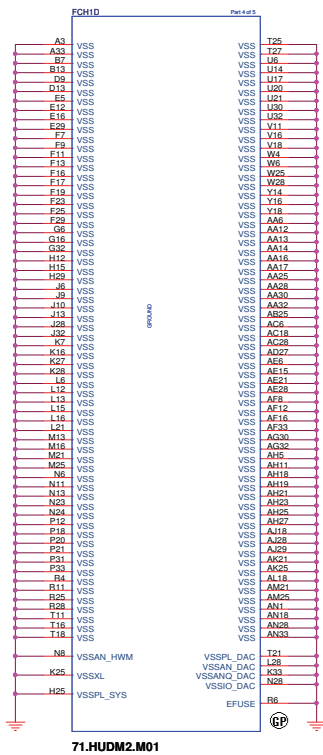


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable I/A AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable I/A AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

DQ15 AMD DIS SAMSUNG T1

DELL		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: SB820M_STRAPPING_(5/5)			
Size: A3	Document Number:	Rev:	X00
Date: Thursday, May 26, 2011		Sheet: 21	of 104



DD15 AMD DS SAMSUNG T1

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Reserved			
Site	Document Number	Rev	
A3		QUEEN AMD Muxless/UMA00	
Date:	Thursday, May 26, 2011	Sheet	22 of 104

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DQ15 AMD DS SAMSUNG T1




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Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMX00	
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Title		Reserved	
Size A3	Document Number	Rev	
Date: Thursday, May 26, 2011		Sheet 24	of 104

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DQ15 AMD DS SAMSUNG T1




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Title		
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Size	Document Number	Rev
NO	QUEEN AMD Muxless/UMX00	
Date: Thursday, May 26, 2011		Sheet 26 of 104

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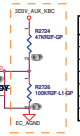
DD15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		Reserved
Size A3	Document Number	Rev
Date: Thursday, May 26, 2011		Sheet 26 of 104
QUEEN AMD Muxless/UMA00		

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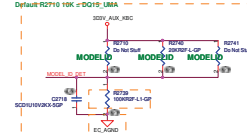
SSID = KBC

0107: Change R2724 & R2725 from 5% to 1% & resistor tolerance.



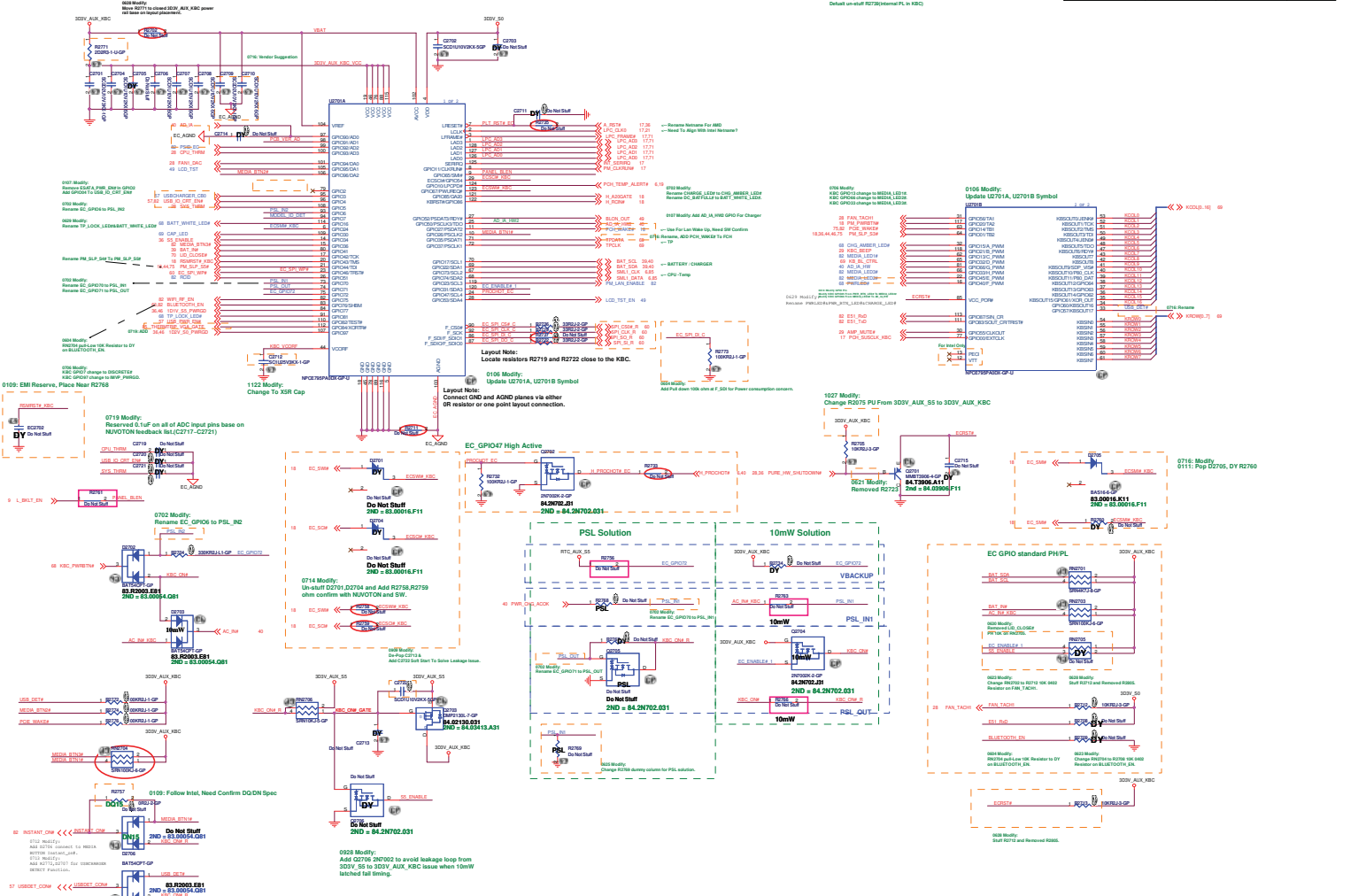
PCB VERSION A (D/P/N)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100K	100K	3.3V
SB	100K	200K	2.5V
SC	100K	230K	2.5V
-1	100K	270K	2.5V
Reserved	100K	645K	2.5V
Reserved	100K	76.5	1.8V
Reserved	100K	100K	1.8V

0107: POP C2718, R2739, Change to Voltage Divider

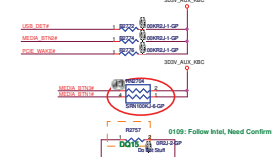
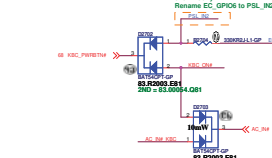


0107: Update Model_ID_DET

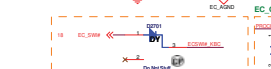
MODEL_ID_DET(C/P/D)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DN31_LMA	100K	100K/64.5K(2.5V)	3.3V
DN31_AMD_DS(PA)	100K	200K/64.5K(2.5V)	2.5V
DN31_LMA	100K	100K	2.5V
DN31_LMA	100K	470K/64.5K(2.5V)	2.5V
DN31_ATT	100K	645K/64.5K(2.5V)	2.5V
Reserved	100K	76.5	1.8V
Reserved	100K	100K	1.8V
DN31_LMA	100K	143.5K	1.5V
DN31_ATT	100K	174.5K	1.25V
DAQF_Veritas	100K	215.5K	1.8V



0109: EM Resistor, Place Near R2705



0719 Modify: Reserved 5% to all of ADD input pins base on NUVOTON feedback list(C2717-C2721)



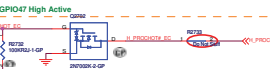
0714 Modify: Un-stuff D2701, D2706 and Add R2758, R2759 chain confirm with NUVOTON and SW.



0928 Modify: Add C2716 2N7002 to avoid leakage loop from 300V_SS to 300V_AUX_KBC when identity latched fail timing.



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



1027 Modify: Change R2075 PU from 300V_AUX_SS to 300V_AUX_KBC



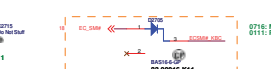
0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



0108 Modify: Update U2701A, U2701B Symbol



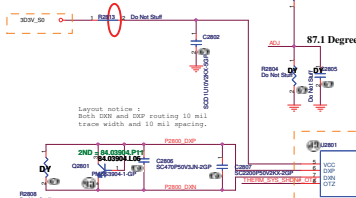
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0001 AMD DS PARTNO: 71

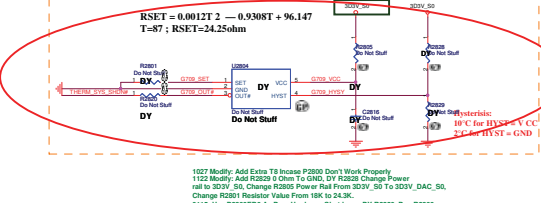
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 2/F, Dell Tower, No. 101, Sec. 2, Hsinchu, Taiwan, R.O.C.

KBC Navoton NPCE295
 QUEEN AMD Muxless/UMA
 Rev: 1.00 Date: 04/28/2011

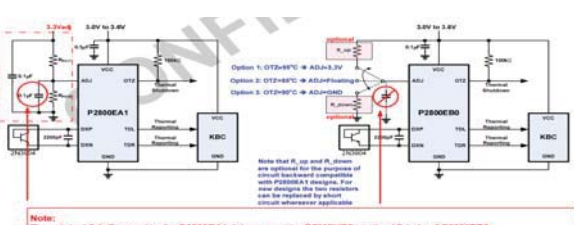
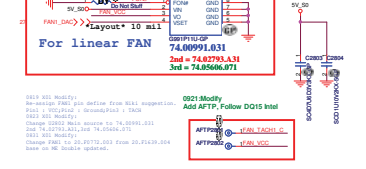
1122 Modify: AD1AAU1_VGA power source change to 3D3V_DAC_50 from 3D3V_50 to solve TS shut down issue.
 1123 Modify: Co lay 3D3V_DAC_50 & 3D3V_50 In Case LDO is Not Used
 0115: Remove R201 ADJ 3D3V_AUX_KBC Pull High



0105 Modify: Change P2800 To E80 Version
 1.8V/N TS Shutdown
 0117 Modify: Vendor Suggest, But will reserve first only, Place Near KBC is OK

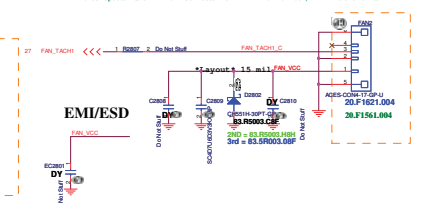
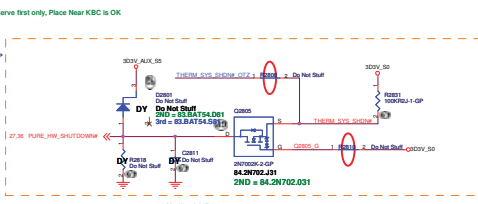


Fan controller P2793



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RAD1 (KΩ)	RAD2 (KΩ)	VAD2 (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



Pin	Pin-1	Definition
P2793A	FGM	Low (<0.4V): VOUT +Vin and the fan is fully on High (>1.6V): VOUT+L*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4V): IC in shutdown. High (>1.6V): VOUT+1.5*VSET This pin is internal Pull-High with ~500K ohm

1213 Modify: Remove Dim Thermal Function

0107: Remove VGA P2800, SW Does Not Use

0915 AMD DS SAMSUNG TI

Wistron Corporation
 2/F, 300 SMC1, Hsin-Tai HSIANG ROAD, Taipei, Taiwan, R.O.C.

Thermal/Fan Controller EMC2102
 QUEEN AMD Muxless/UMA

Doc. No. : EMC2102 Rev. 201101
 Date: 2011.01.22

AUDIO OP AMPLIFIER

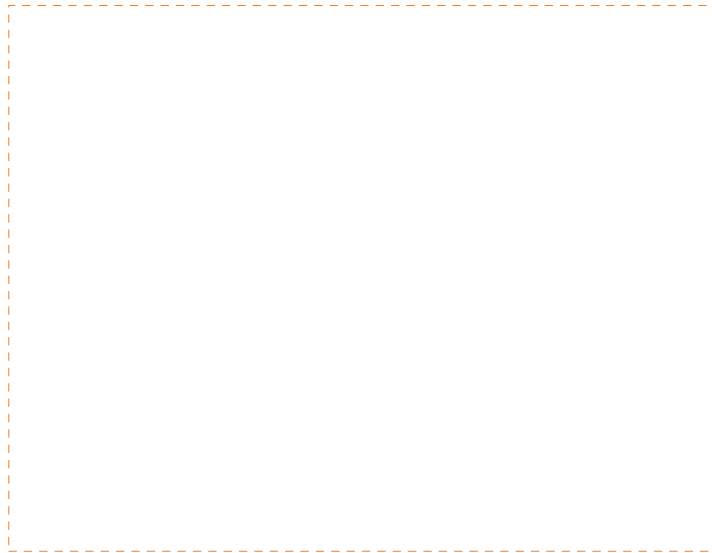
DQ15 AMD DIS SAMSUNG TI

	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	


Title	AMP	
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMX00	
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DG15 M12 In Daughter BD



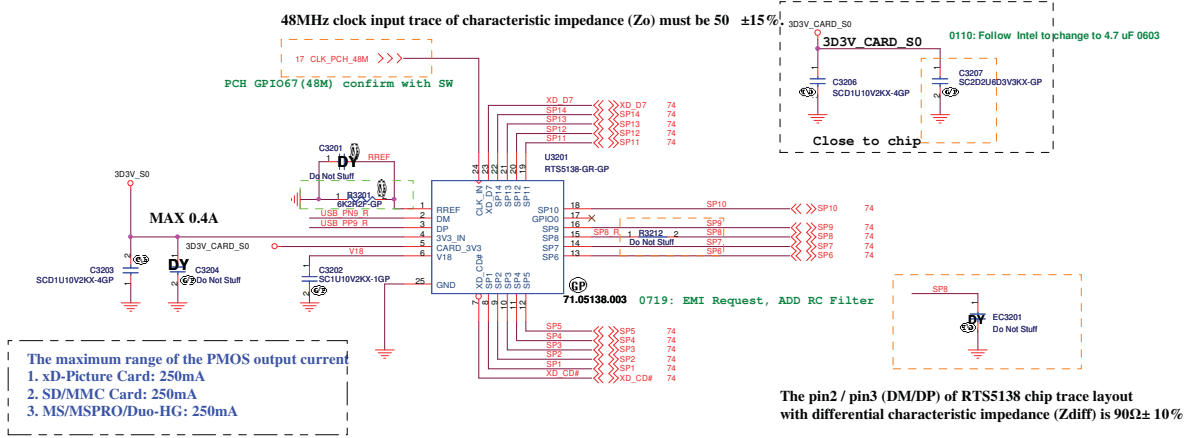
DQ15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LOM	
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA	X00	
Date:	Thursday, May 26, 2011	Sheet	31 of 104

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SSID = SDIO

48MHz clock input trace of characteristic impedance (Z_0) must be $50 \pm 15\%$



The maximum range of the PMOS output current
 1. xD-Picture Card: 250mA
 2. SD/MMC Card: 250mA
 3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE


- 1.RTSS138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
- 2.RTSS138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
- 3.RTSS138: pin 6 (V18) trace fixed width is 12 mils (minimum). Keep the trace routing lengths as short as possible.
- 4.RTSS138: pin 1(RREF) trace fixed width is 12 mils (minimum).
- 5.RTSS138: pin 1(RREF) trace must far away 48MHz clock trace.
- 6.De-coupling and Bulk capacitor should place near to RTSS138 chip and Combo Socket.
- 7.It is recommended that use of ferrites bead on power trace.
- 8.Via size: Pad=>32 mils, Finished hole=>16 mils.

- 0103 Modify: AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch
- 0118 Modify: Change TR3201 To 69.10118.001 due to layout limitation

DD15 AMD_DS_0AMSUNG T1

DELL		Wistron Corporation	
		21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Reserved	
Size	A3	Document Number	QUEEN AMD Muxless/UMA00
Date:	Friday, May 27, 2011	Sheet	02 of 104

DD15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		Reserved
Size A3	Document Number	Rev
Date: Thursday, May 26, 2011		Sheet 33 of 104
QUEEN AMD Muxless/UMA00		

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DQ15 AMD DIS SAMSUNG TI



Title	Reserved		Rev
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMX00		
Date: Thursday, May 28, 2011	Sheet	34	of 104

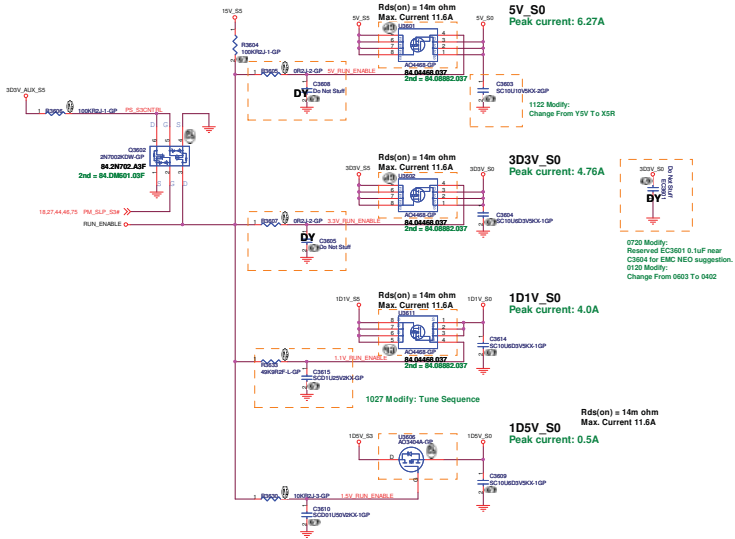
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DQ15 AMD DIS SAMSUNG TI

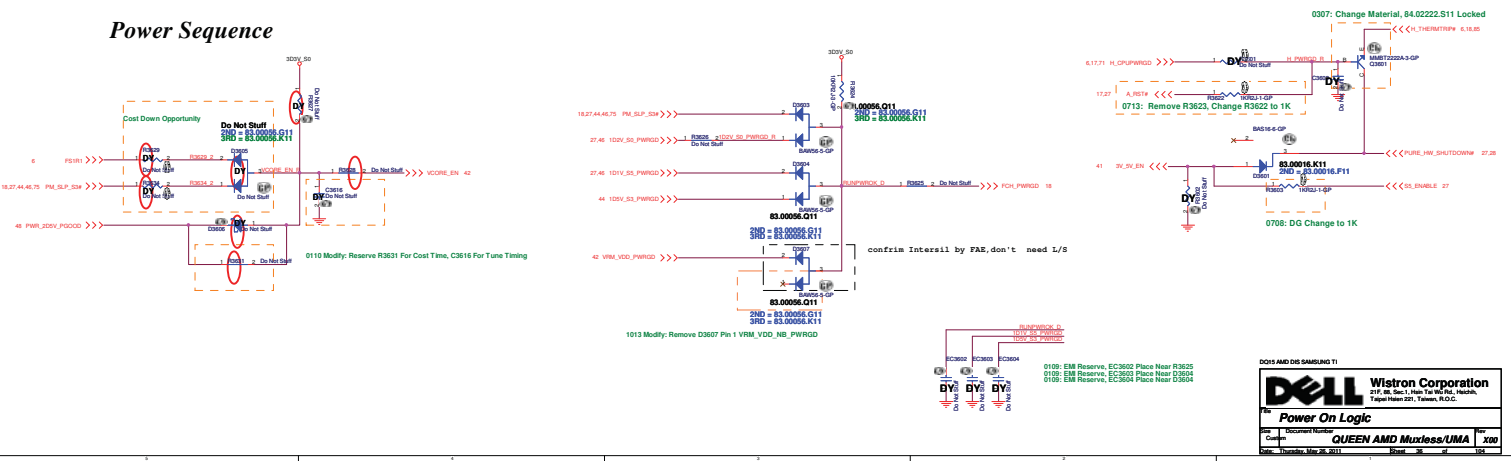
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Title		Reserved
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
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ROSA Run Power



Power Sequence



0019 AMD DG SAMPLING T1

DELL Wistron Corporation
 019, 020, 021, 022, 023, 024, 025, 026, 027, 028, 029, 030, 031, 032, 033, 034, 035, 036, 037, 038, 039, 040, 041, 042, 043, 044, 045, 046, 047, 048, 049, 050, 051, 052, 053, 054, 055, 056, 057, 058, 059, 060, 061, 062, 063, 064, 065, 066, 067, 068, 069, 070, 071, 072, 073, 074, 075, 076, 077, 078, 079, 080, 081, 082, 083, 084, 085, 086, 087, 088, 089, 090, 091, 092, 093, 094, 095, 096, 097, 098, 099, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000

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DQ15 AMD DIS SAMSUNG TI

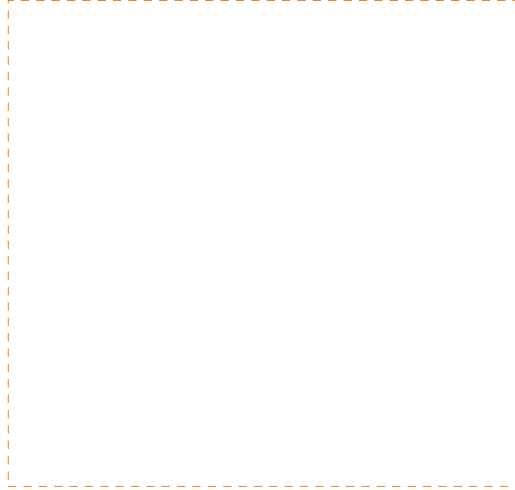
DELL **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
Date: Thursday, May 26, 2011	Sheet 37 of	104

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Move To CRT BD



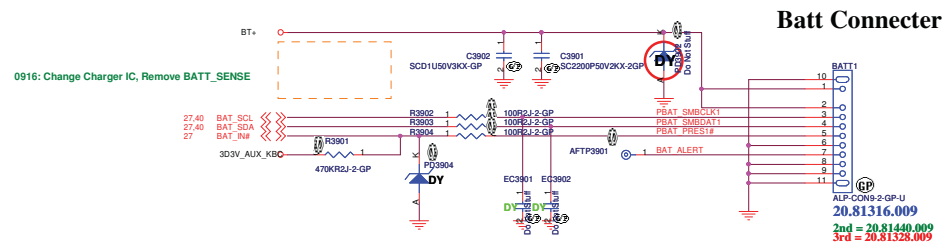
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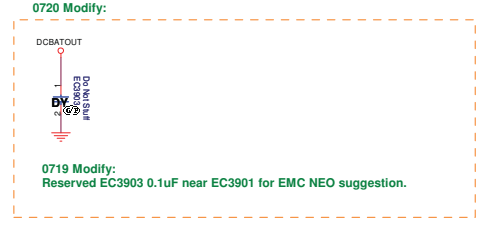
File	DCIN JACK	
Step	Document Number	Rev
1		
QUEEN AMD Muxless/UMAD0		
Date	Thursday, May 26, 2011	Page 38 of 105

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SSID = BATT CONN

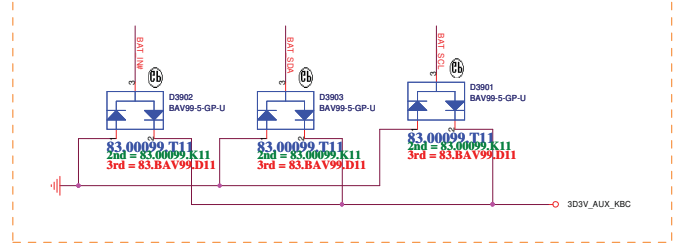


Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

BATT CONN

Size: A3 Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**
 Date: Thursday, May 28, 2011 Sheet: 39 of 104

SSID = Charger

EE need pull high and net name
0802 Rename H_PROCHOT#

6.27 H_PROCHOT#

X00 0415

X00 0415

X00 0415

EC code only BQ24707

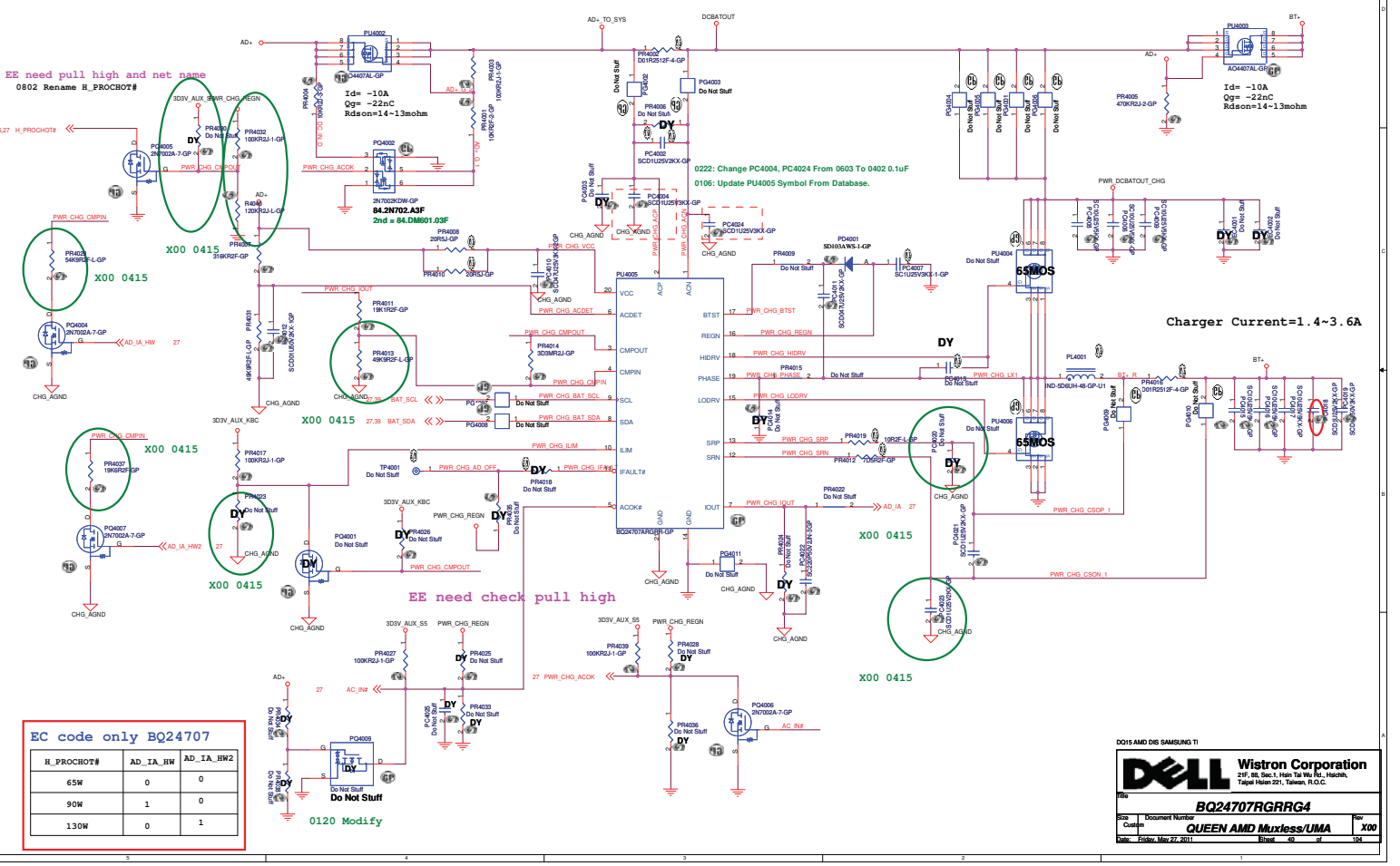
H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

0120 Modify

EE need check pull high

Q222: Change PC4004, PC4024 From 0503 To 0402 0.1uF
0105: Update PU4005 Symbol From Database.

Charger Current=1.4~3.6A



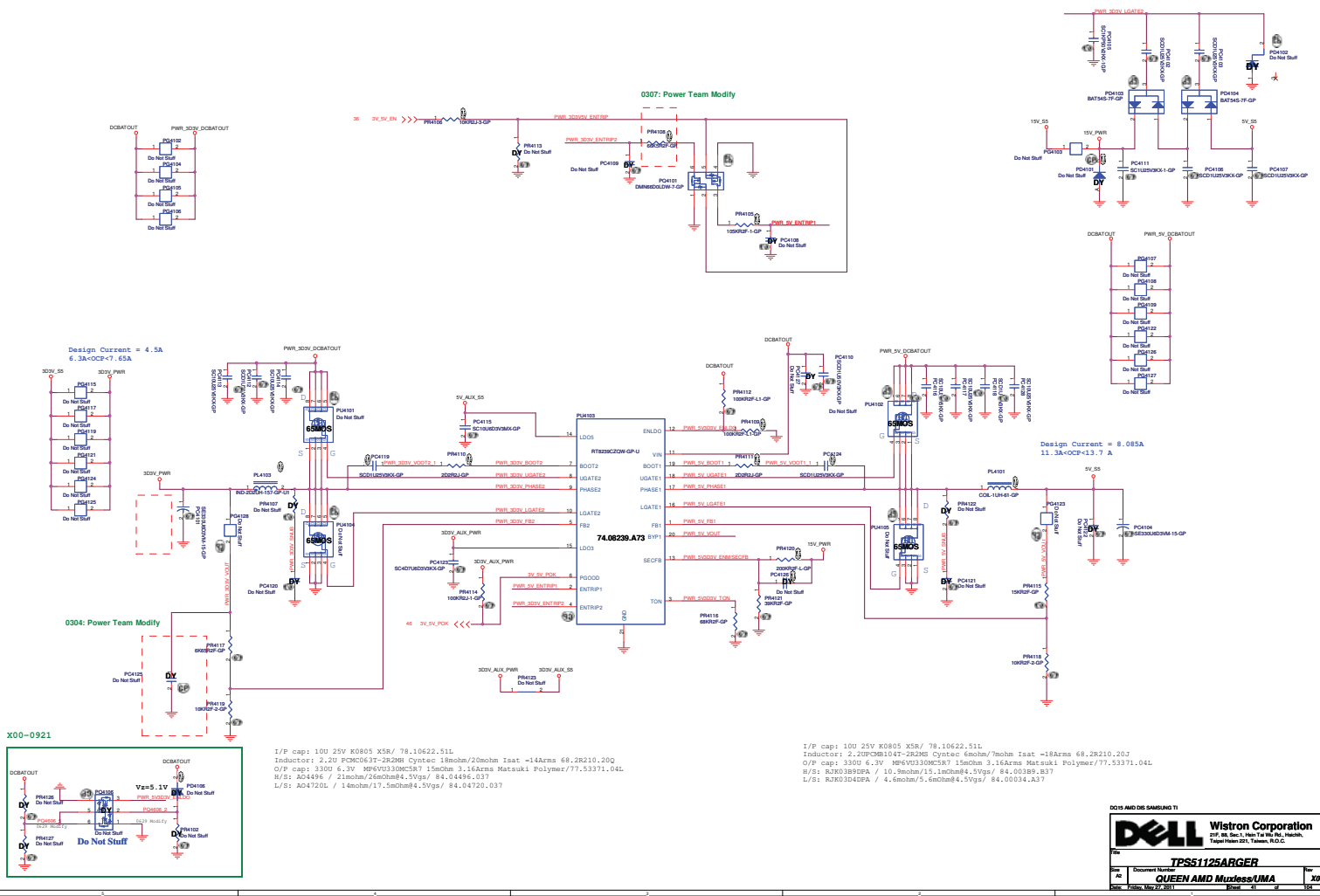
0015 AMD DIS SAMUNG TI

DELL Wistron Corporation
2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsueh,
Taipai Hsein 221, Taiwan, R.O.C.

Rev: **BQ24707RGRG4**

Doc: Document Number **QUEEN AMD Muxless/UMA** Rev **X00**

Size: 100x100mm, Mar 27, 2011



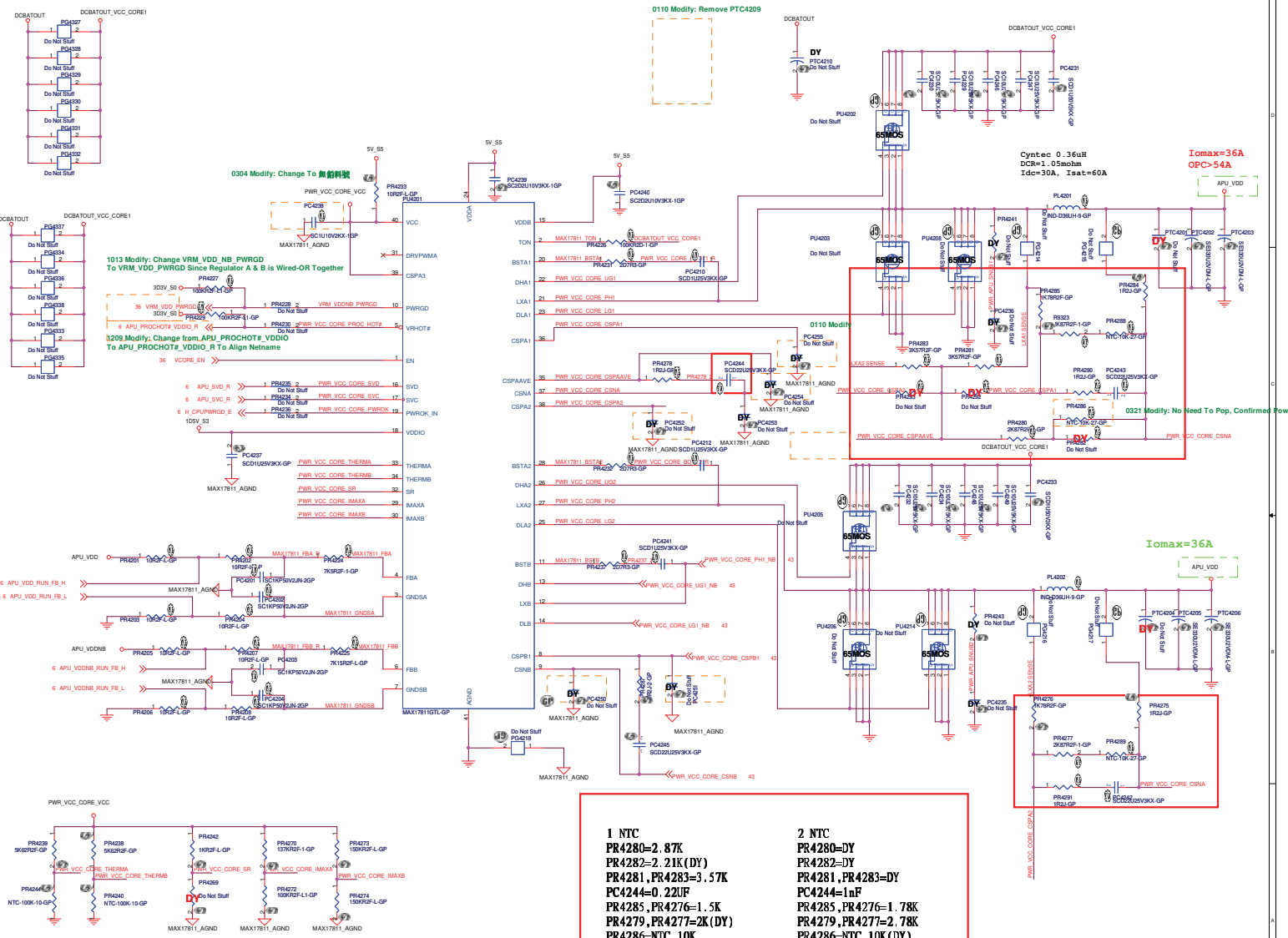
<http://hobi-elektronika.net>

DELL Wistron Corporation
 5/F, 2/F, 3/F, 4/F, 5/F, 6/F, 7/F, 8/F, 9/F, 10/F, 11/F, 12/F, 13/F, 14/F, 15/F, 16/F, 17/F, 18/F, 19/F, 20/F, 21/F, 22/F, 23/F, 24/F, 25/F, 26/F, 27/F, 28/F, 29/F, 30/F, 31/F, 32/F, 33/F, 34/F, 35/F, 36/F, 37/F, 38/F, 39/F, 40/F, 41/F, 42/F, 43/F, 44/F, 45/F, 46/F, 47/F, 48/F, 49/F, 50/F, 51/F, 52/F, 53/F, 54/F, 55/F, 56/F, 57/F, 58/F, 59/F, 60/F, 61/F, 62/F, 63/F, 64/F, 65/F, 66/F, 67/F, 68/F, 69/F, 70/F, 71/F, 72/F, 73/F, 74/F, 75/F, 76/F, 77/F, 78/F, 79/F, 80/F, 81/F, 82/F, 83/F, 84/F, 85/F, 86/F, 87/F, 88/F, 89/F, 90/F, 91/F, 92/F, 93/F, 94/F, 95/F, 96/F, 97/F, 98/F, 99/F, 100/F

TPSS112SARGER

QUEEN AND MURDER/UMA

X90



- | | |
|----------------------------|------------------------|
| 1 NTC | 2 NTC |
| PR4280=2.87K | PR4280=DY |
| PR4282=2.21K(DY) | PR4282=DY |
| PR4281, PR4283=3.57K | PR4281, PR4283=DY |
| PC4244=0.22uF | PC4244=1nF |
| PR4285, PR4276=1.5K | PR4285, PR4276=1.78K |
| PR4279, PR4277=2K(DY) | PR4279, PR4277=2.78K |
| PR4286=NTC 10K | PR4286=NTC 10K(DY) |
| PR4288, PR4289=NTC 10K(DY) | PR4288, PR4289=NTC 10K |
| PR4290, PR4291=0 ohm | PR4290, PR4291=1 ohm |
| PR4292, PR4393=100ohm (DY) | PR4292, PR4393=100 ohm |

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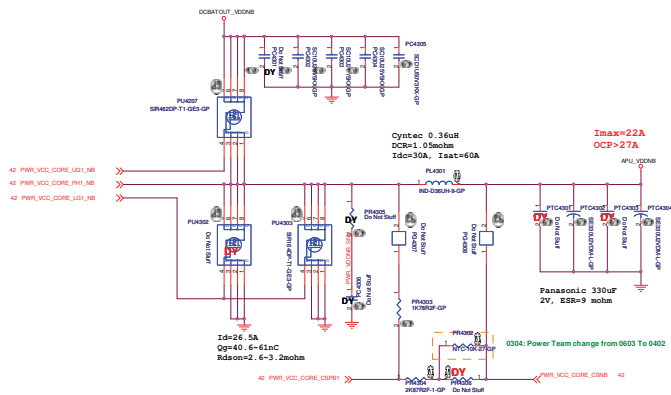
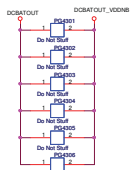
DO15 AMD DS SAMUNG TI

DELL Wistron Corporation
 2/F, 88, Sec 1, Hsin Tai Wu Rd, Hsinchu, Taipei Hsin 301, Taiwan, R.O.C.

Rev: **VREG : +VCC_CORE&+VDDNB**

Docu: **QUEEN AMD Muxless/UMA** Rev: **X00**

Date: **Friday, Mar 27, 2011** Sheet: **6** of **6**



0015 AND DC SAMUNG T1

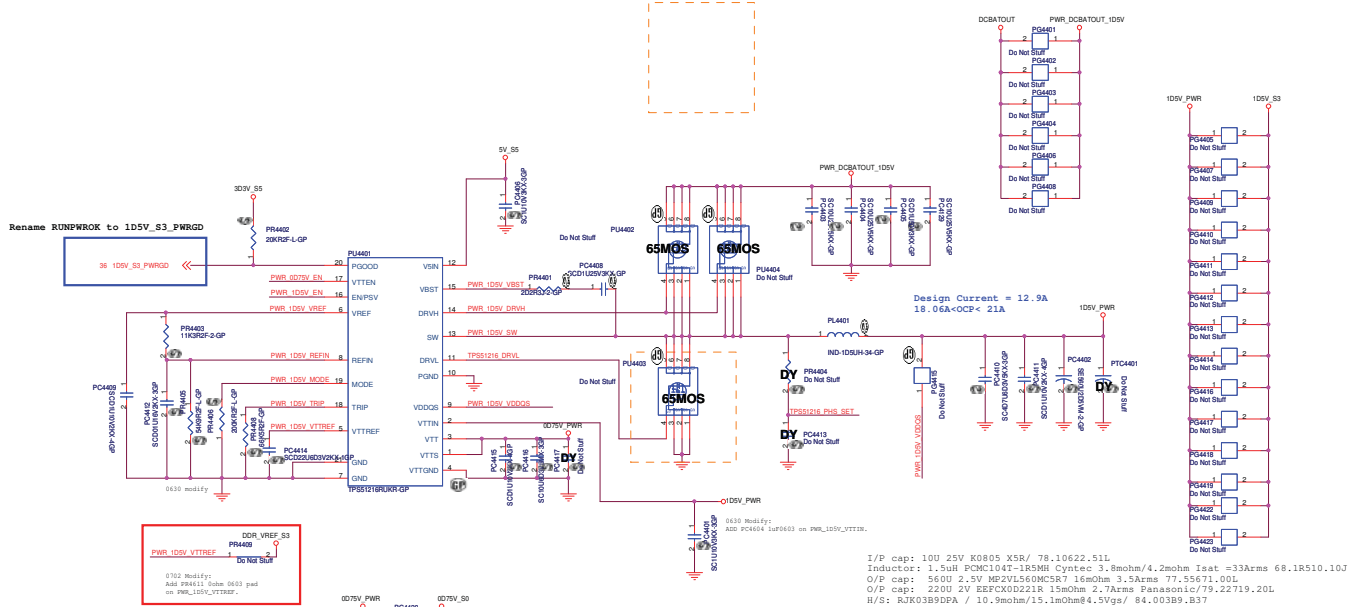
DELL Wistron Corporation
 5/F, No. 2, Lane 1, Ta Hsiung, Hsinchu, Taiwan, R.O.C.

Doc: **VDDNB**

Doc Number: **QUEEN AND Muxless/UMA** X10

Date: **Rev: 01**

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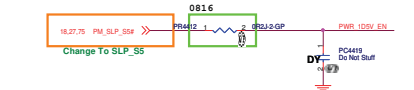
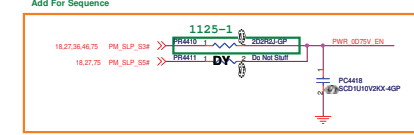


Design Current = 1.2 9A
1.8 0.6A <OCP< 21A

I/P cap: 10U 25V R0805 X5R/ 78.10622.51L
Inductor: 1.5uH PCW2104T-1R35MR Cynotec 3.3mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 560U 2.5V MP2VL56MCSR7 16mohm 3.5Arms 77.55671.00L
O/P cap: 220U 2V EEPFC02221R 15mohm 2.7Arms Panasonic/79.22719.20L
H/S: RJK039DPA / 10.3mohm/5.1mohm/4.5Vgs/ 84.00389.83T
L/S: RJK039DPA / 4.6mohm/5.6mohm/4.5Vgs/ 84.00034.A37

State	S3	S5	VDDR	VTTREF	VTT
S0	HL	HL	On	On	On
S3	Lo	HL	On	On	DEF (HL-Z)
S4/S5	Lo	Lo	OFF	OFF	DEF

MODE	FR4406	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge	
100k ohm	300kHz	Tracking Discharge	
68k ohm	300kHz	Non-tracking Discharge	
47k ohm	400kHz	Non-tracking Discharge	



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0015 AMD DIS SAMSUNG TI

Wistron Corporation
2/F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsinchu, Taiwan, R.O.C.


Rev: **TP551216 1D5V S3**

Doc No	Document Number	Rev
0000	0000	X00

Created: **QUEEN AMD Muxless/UMA**

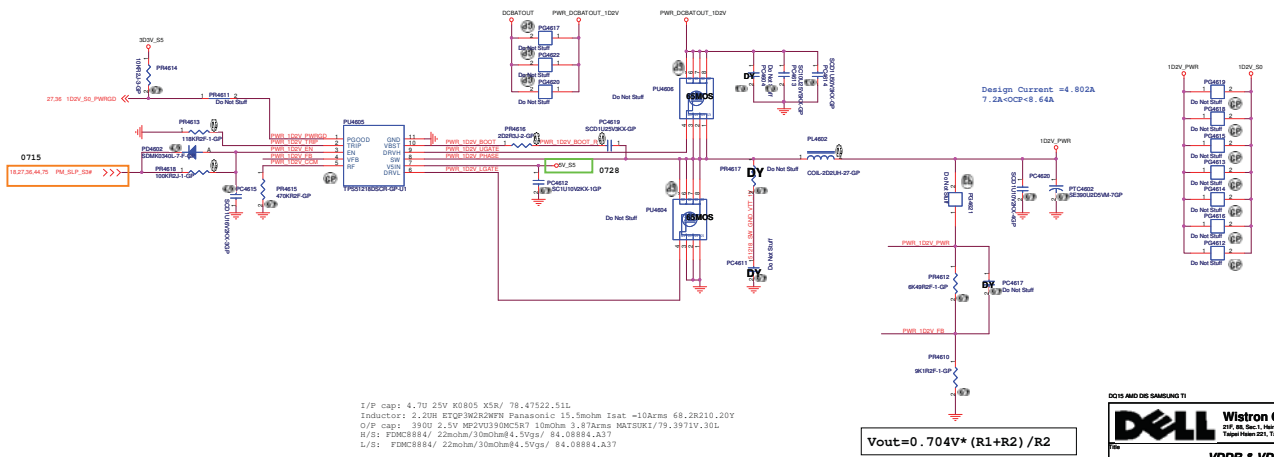
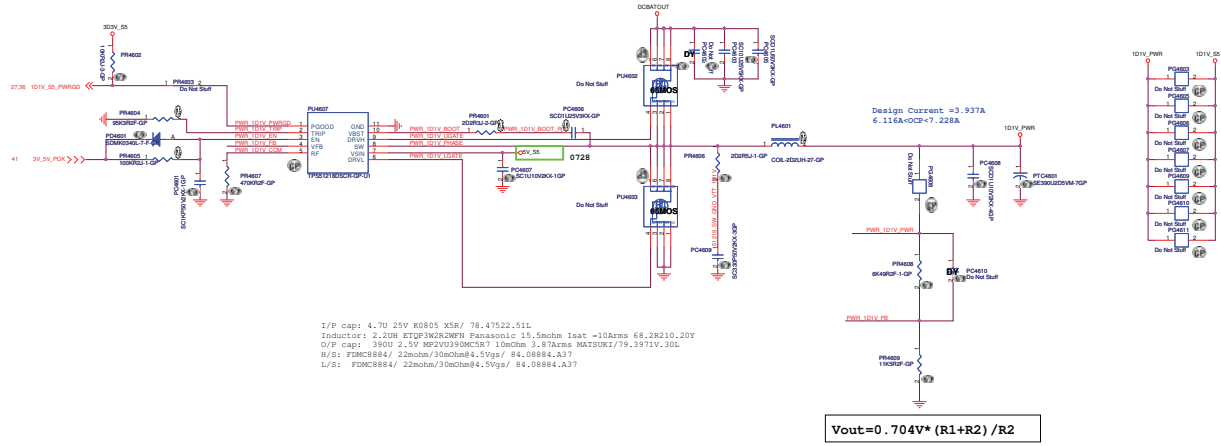
Rev: 1509, 1509, 1501

QUEEN AMD DIS SAMUNG T1

	Wistron Corporation <small>21F, 28, Sec. 1, Neihu Tech Rd, Neihu, Taipei, Taiwan, R.O.C.</small>
File	VDDR & VDDP
Part	QUEEN AMD Muxless UM&X0
Date	Rev. 01 <small>Rev. 01</small>

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SSID = PWR.Plane.Regulator_1D1V_S5



0015 AMD DG-SAMSUNG TI

DELL Wistron Corporation
 1/F, 3/F, 5/F, 6/F, 7/F, 8/F, 9/F, 10/F, 11/F, 12/F, 13/F, 14/F, 15/F, 16/F, 17/F, 18/F, 19/F, 20/F, 21/F, 22/F, 23/F, 24/F, 25/F, 26/F, 27/F, 28/F, 29/F, 30/F, 31/F, 32/F, 33/F, 34/F, 35/F, 36/F, 37/F, 38/F, 39/F, 40/F, 41/F, 42/F, 43/F, 44/F, 45/F, 46/F, 47/F, 48/F, 49/F, 50/F, 51/F, 52/F, 53/F, 54/F, 55/F, 56/F, 57/F, 58/F, 59/F, 60/F, 61/F, 62/F, 63/F, 64/F, 65/F, 66/F, 67/F, 68/F, 69/F, 70/F, 71/F, 72/F, 73/F, 74/F, 75/F, 76/F, 77/F, 78/F, 79/F, 80/F, 81/F, 82/F, 83/F, 84/F, 85/F, 86/F, 87/F, 88/F, 89/F, 90/F, 91/F, 92/F, 93/F, 94/F, 95/F, 96/F, 97/F, 98/F, 99/F, 100/F

Doc: VDDR & VDDP
 Document Number: QUEEN AMD Muxless UM&Xv
 Rev: 1.00, Mar 27, 2011

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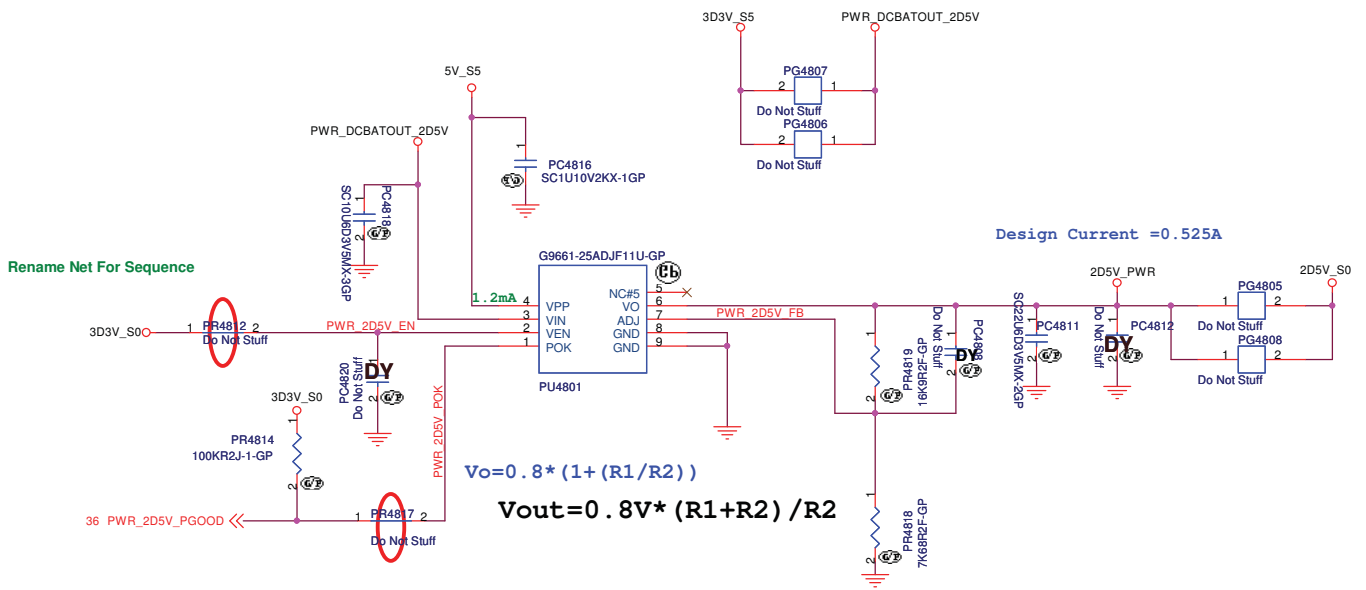
0010 AMD DS SAMUNG T1

		Wistron Corporation <small>2/F, 28, Sec. 1, Hsin-Tai Rd, Hsinchu, Taiwan 305, Taiwan, R.O.C.</small>
Reserved		
Part	Document Number	Part
At	QUEEN AMD Muxless/UMAX00	For
Date	Thursday, May 26, 2011	Rev
		of
		100

<http://hobi-elektronika.net>

SSID = PWR.Plane.Regulator_2p5v VGA 1V

G9661 for 2D5V_S0



DQ15 AMD DIS SAMSUNG TI



Title		2D5V_S0	
Size	Document Number	Rev	
A4	QUEEN AMD Muxless/UMA00		
Date: Thursday, May 26, 2011	Sheet 48	of	104

<http://hobi-elektronika.net>

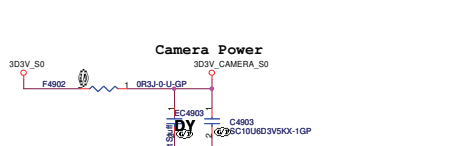
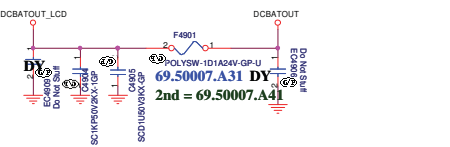
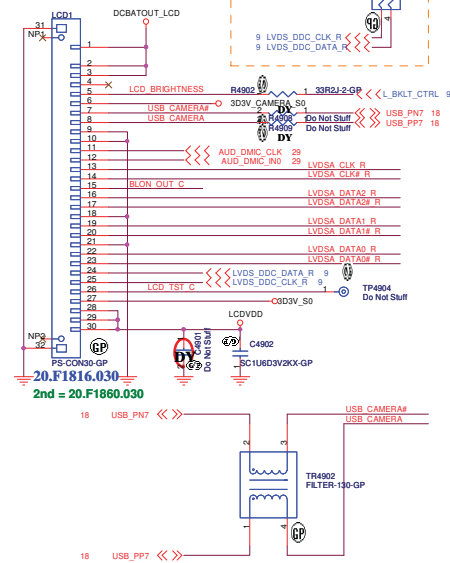
SSID = VIDEO

0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated
cable pin define list.

0914 Modify:
Change PU From Page 82 To Page 49

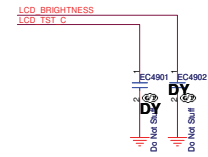
0921 Modify:
Change BLON_OUT_C to pin 15 and pin 4
to NC on LCD1.

LVDS CONNECTOR



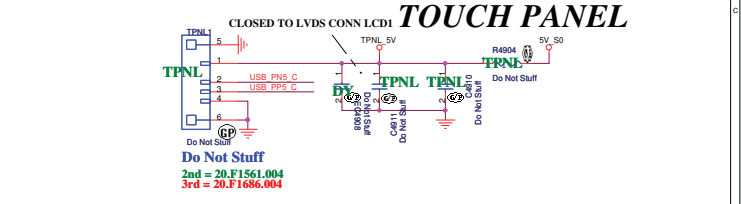
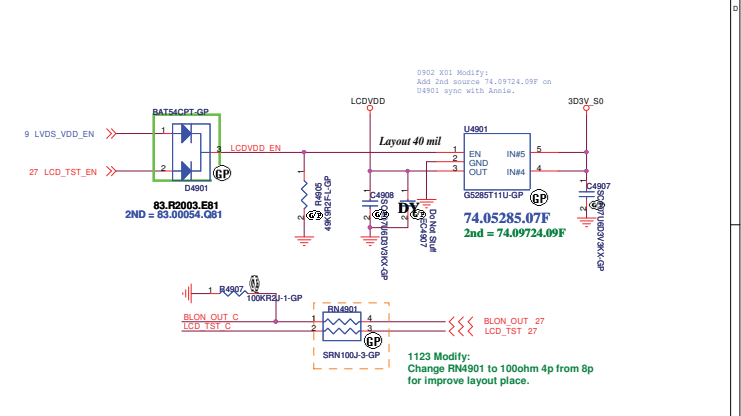
(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	BLON_OUT_C
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	LCD_DET_G
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

For EMI request
Close to LVDS connector



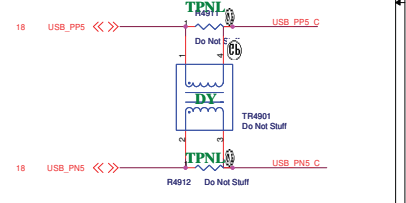
SSID = VIDEO

LCD POWER for ROSA

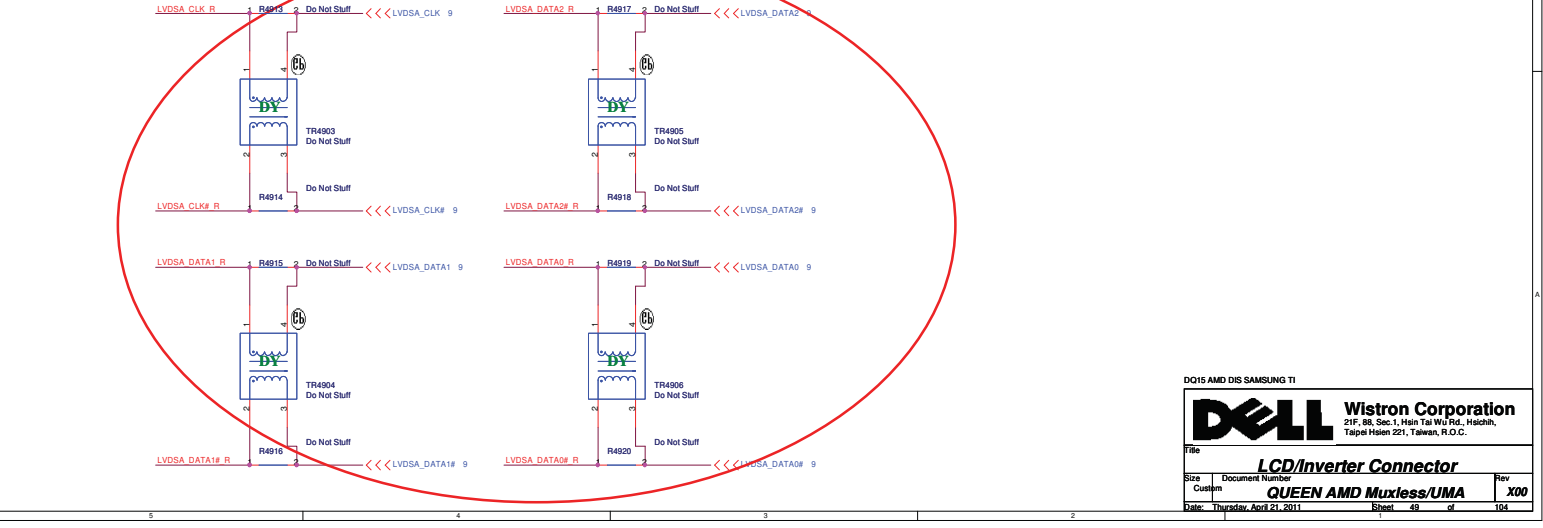


0909 Modify:
Add TP1 to touch panel solution 4pin connector.

0928 Modify:
Change to 20.F1621.004 on TP1 from updated
connector list.



<http://hobi-elektronika.net>



DDI5 AMD DIS SAMSUNG TI

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taippei Hsien 221, Taiwan, R.O.C.

File: **LCD/Inverter Connector**

Size: Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**

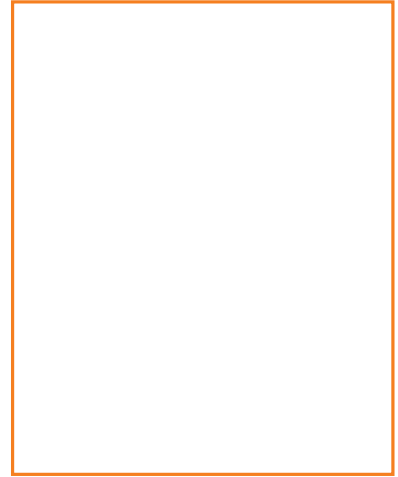
Customer: **QUEEN AMD Muxless/UMA**

Date: Thursday, April 21, 2011 10:41:49 AM

Remove For M12 Spec & Put In Daughter BD




Remove For M12 Spec & Put In Daughter BD



Remove For M12 Spec & Put In Daughter BD



DQ15 AMD DIS SAMSUNG TI

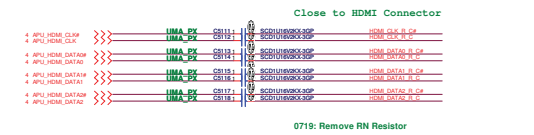
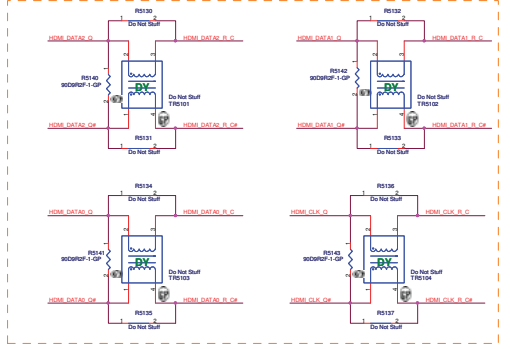
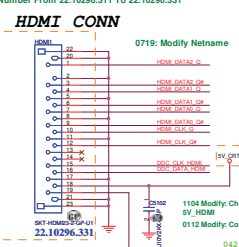
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		CRT Board Connector	
Size	Document Number	Rev	
Custom	QUEEN AMD Muxless/UMA	X00	
Date:	Thursday, May 26, 2011	Sheet	50 of 104

<http://hobi-elektronika.net>

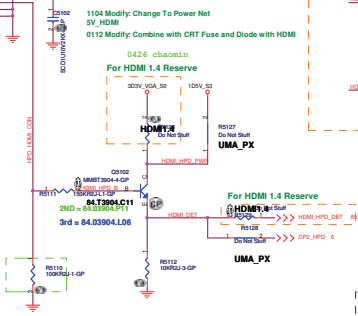
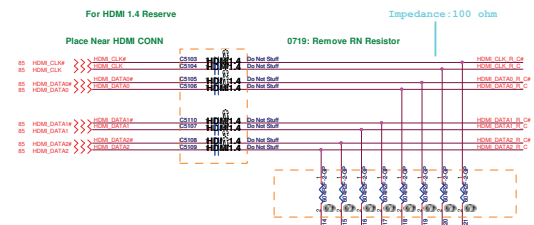
HDMI Level Shifter & CONNECTOR

0913: Modify Change HDMI1 Part Number From 22.10296.311 To 22.10296.331

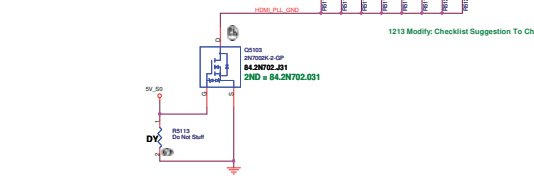
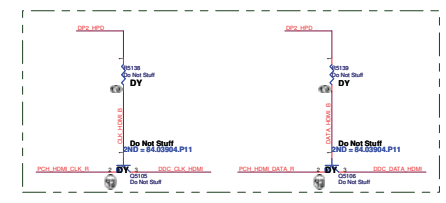
0719: Reserve For EM



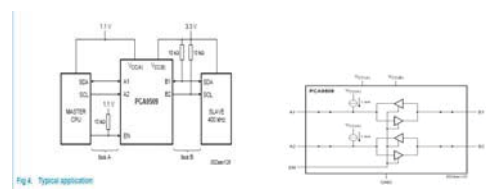
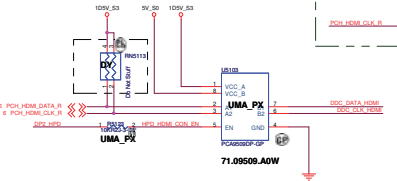
0719: Remove RN Resistor



0921: Modify Add ATTP, Follow DQ15 Intel



confirm by NXP FAE Do not need PU Res, Reserve PU Res for debug further



0015 AMD DCI SAMPLING TI

Wistron Corporation
 2100, 2101, 2102, 2103, 2104, 2105, 2106, 2107, 2108, 2109, 2110, 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, 2129, 2130, 2131, 2132, 2133, 2134, 2135, 2136, 2137, 2138, 2139, 2140, 2141, 2142, 2143, 2144, 2145, 2146, 2147, 2148, 2149, 2150, 2151, 2152, 2153, 2154, 2155, 2156, 2157, 2158, 2159, 2160, 2161, 2162, 2163, 2164, 2165, 2166, 2167, 2168, 2169, 2170, 2171, 2172, 2173, 2174, 2175, 2176, 2177, 2178, 2179, 2180, 2181, 2182, 2183, 2184, 2185, 2186, 2187, 2188, 2189, 2190, 2191, 2192, 2193, 2194, 2195, 2196, 2197, 2198, 2199, 2200

HDMI Level Shifter/Connector

Document Name: **QUEEN AMD Mixless/UMA**

Doc. No.: **X10**

Rev: **01**

Date: **2010.11.26**

<http://hobi-elektronika.net>

Remove EDP



LCD POWER CIRCUIT

Remove EDP




Rosa team

Remove EDP



<http://hobi-elektronika.net>

DD15 AMD DIS SAMSUNG T1

		Wistron Corporation	
		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title		eDP	
Size	Document Number	Rev	
Custom			
Date: Thursday, May 26, 2011		Sheet	52 of 104

DQ15 AMD DIS SAMSUNG TI



Title	Reserved		Rev
Size	Document Number		
A3	QUEEN AMD Muxless/UMX00		
Date: Thursday, May 26, 2011	Sheet	53	of 104

<http://hobi-elektronika.net>

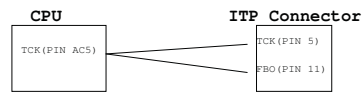
DQ15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File		Reserved
Size A3	Document Number	QUEEN AMD Muxless/UH/A00
Date: Thursday, May 26, 2011	Sheet	54 of 104

<http://hobi-elektronika.net>

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

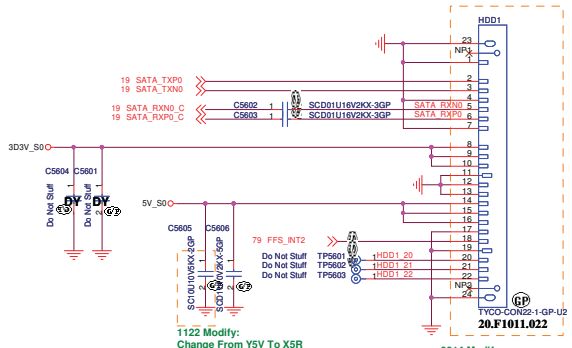


DQ15 AMD DIS SAMSUNG TI

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP			
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA	X00	
Date:	Thursday, May 26, 2011	Sheet	55 of 104

SSID = SATA

SATA HDD Connector



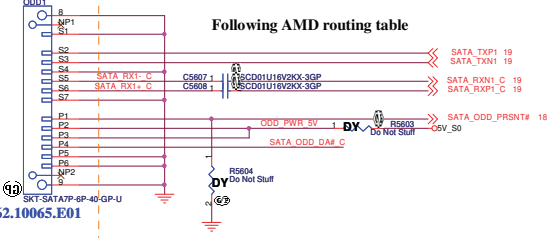
0614 Modify:
Change HDD1 connector part number to 20.F1011.022 base on ME EMM and DXF.

ODD Connector

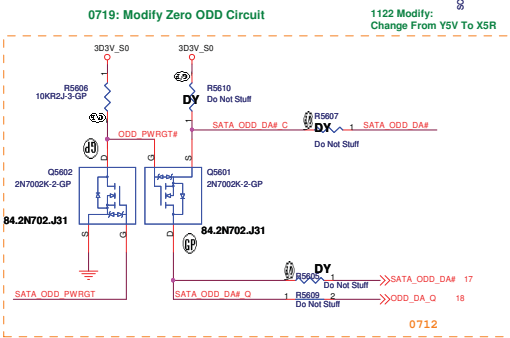
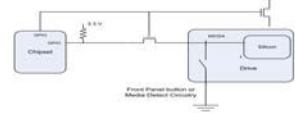
SATA_RX- and SATA_RX+ Trace Length match within 20 mil

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SUPPORT ZERO SATA ODD

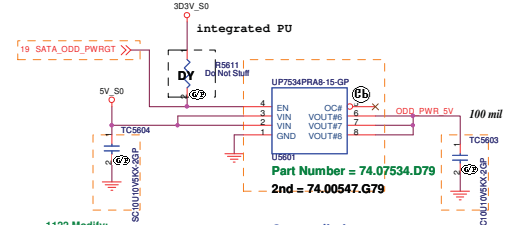


0914 Modify:
Change ODD Part number From 22.10300.421 To 62.10065.E01



0719: Modify Zero ODD Circuit

1122 Modify:
Change From Y5V To X5R



Current limit
Active High
typ => 2.5A

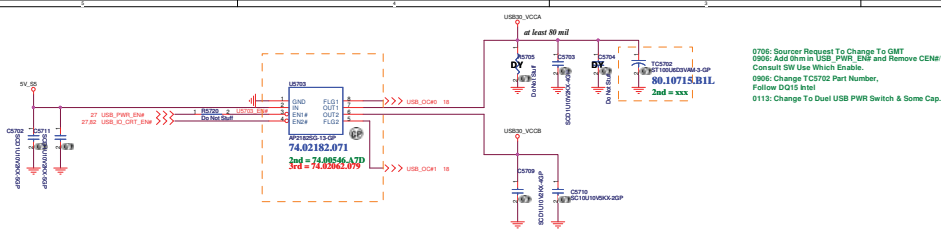
1122 Modify:
Change From Y5V To X5R

0109: EMI Request.

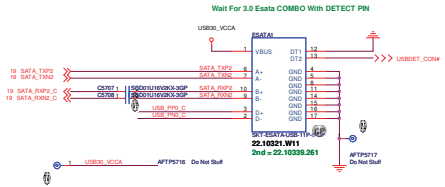
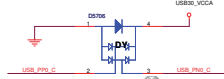
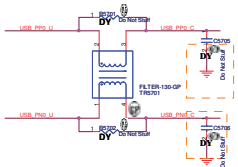
Q015 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

File	HDD/ODD	
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
Date: Thursday, May 26, 2011	Sheet 58 of 104	



0101: Change ESATA1 To 22.10290.271



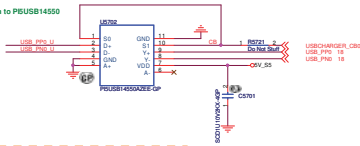
0706: Rename Netname

0112: Change To USB 2.0 ESD Diode X 2

0101: Reserve Common Mode Choke & ESD Diode.

USB CHARGER

0906: Modify: Change U5702 solution to PBU5B14550 from MAX14556



Switch Control Bit:
 CB=0 (AM): auto detection charger identification active.
 CB=1 (PM): connect DP/DM to TDP/TDM.

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0914: Remove Non Charger Co-ly Resistor.

0015 AMD DS SAMUNG T1

DELL Wistron Corporation
 210, St. Sec-1, Hsin-Tai Rd, Hsinchu, Taiwan, R.O.C.

ESATA/USB Charger

Doc: **QUEEN.AMD.Murice.LMA** Ver: **X00**

Date: **1/20/2010** By: **20100120**

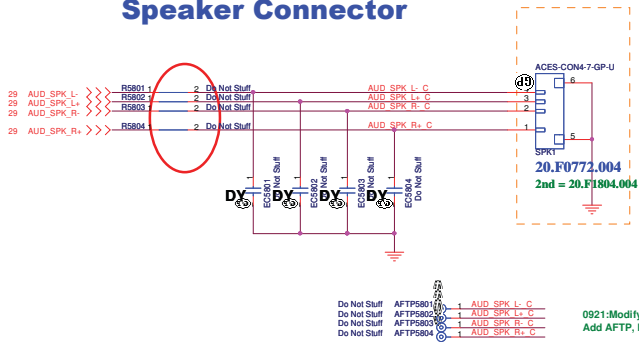
0715 Modify:
Change ECS801-ECS804 to 100p 0402
and default un-stuff.
Add R5801-R5804 between SPK signal and connector
for EMC NEO suggest.

0914 Modify:
Change SPK1 to 20.F0772.004 from
20.F1847.004 from Double updated.

0921 Modify:
Modify Pin Define Base On DQ15 Intel

1110 X02 Modify:
Add 2nd 20.F1804.004 on SPK1 from
ME updated connector list.

Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

DQ15 AMD DIS SAMSUNG TI

DELL	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title: Audio Jack		
Size: A3	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet: 08	of 104

LAN CONN in Daughtier BD



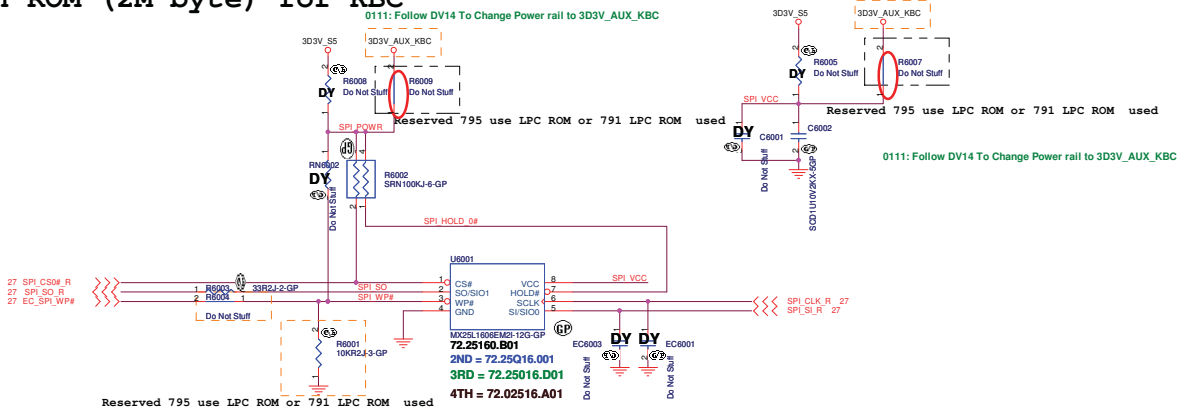
DQ15 AMD DIS SAMSUNG TI

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		LAN CONN	
Size A3	Document Number	Rev	
Date: Thursday, May 26, 2011		QUEEN AMD Muxless/UM/A00	
	Sheet	59	of 104

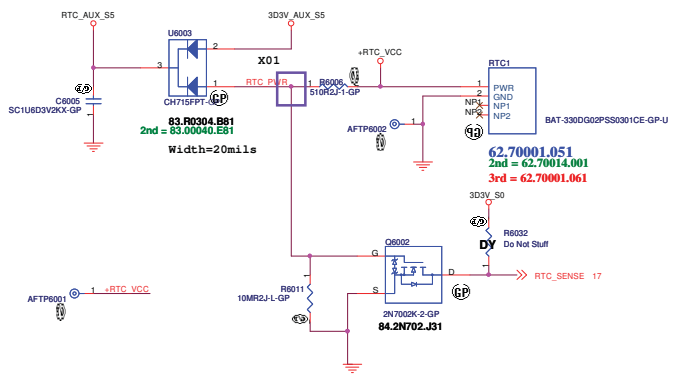
<http://hobi-elektronika.net>

SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



0105 Modify:
updated RTC1 symbol and footprint from
data base.
1122 Modify:
Add Q6002, R6010, R6011 for FACTORY RTC detect function.
0111: Change RTC Schematic As DV14 Brazo, SW Suggest.

DQ15 AMD DIS SAMSUNG TI

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: **Flash/RTC**

Size: A3	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet: 60	of 104

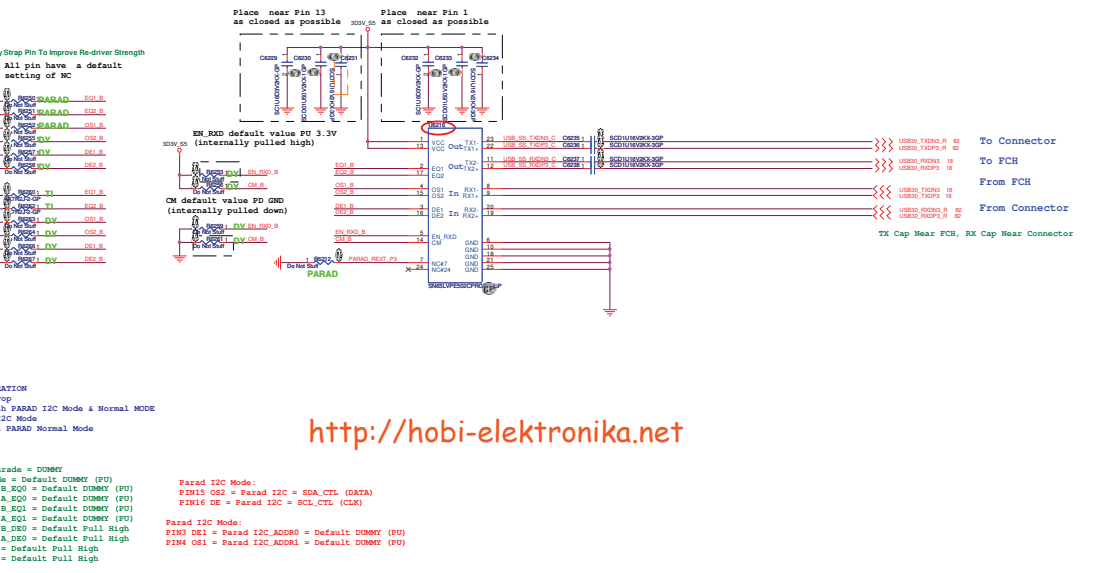
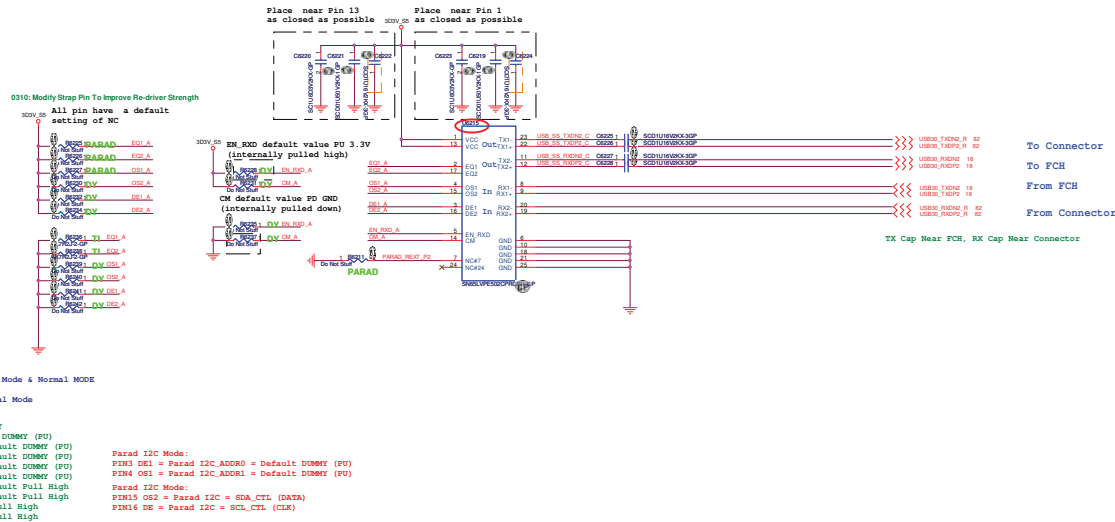
SSID = USB

DQ15 AMD DIS SAMSUNG T1

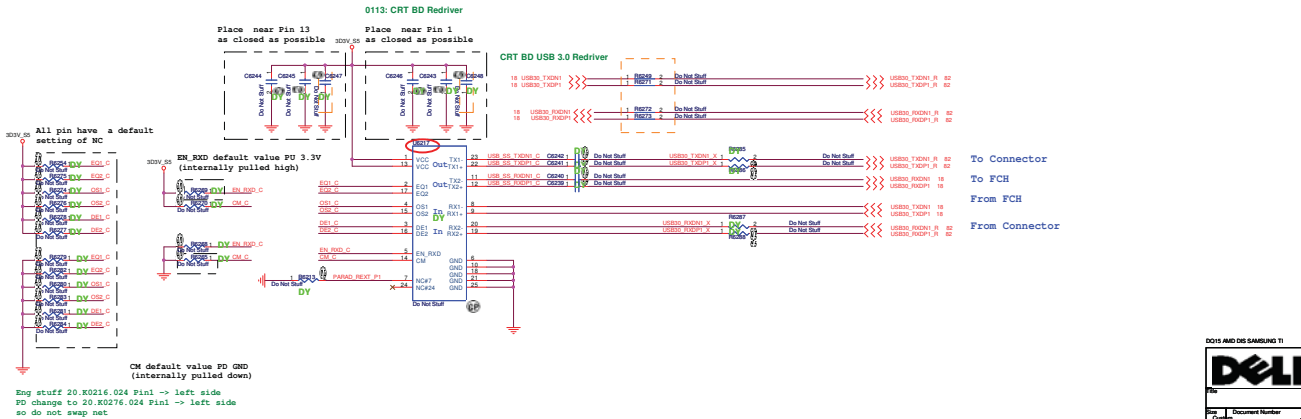


Title		
USB Power SW		
Size	Document Number	Rev
	QUEEN AMD Muxless/UMA	X00
Date:	Thursday, May 26, 2011	Sheet 61 of 104

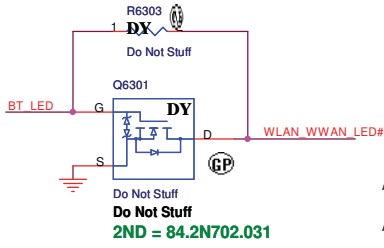
<http://hobi-elektronika.net>



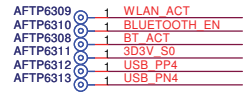
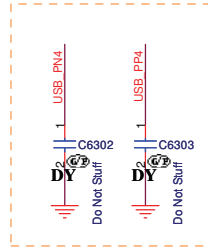
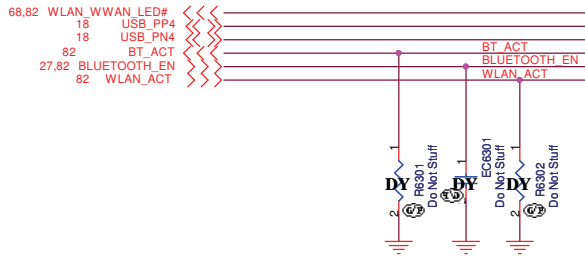
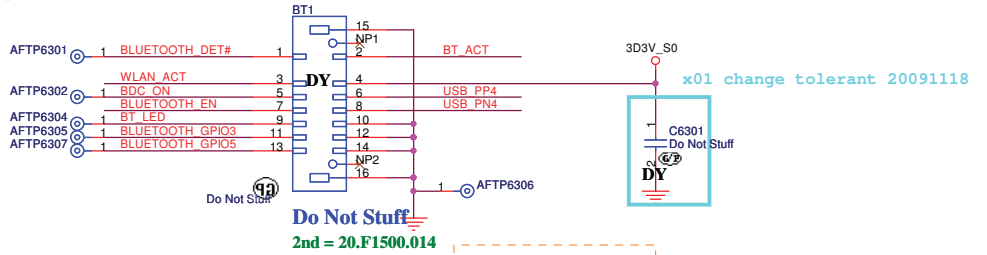
http://hobi-elektronika.net



SSID = User.Interface



Bluetooth Module conn.



0906 Modify:
 Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wireless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

0103 Modify:
 AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

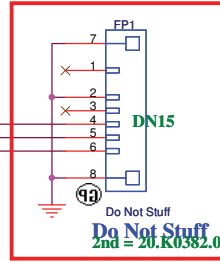
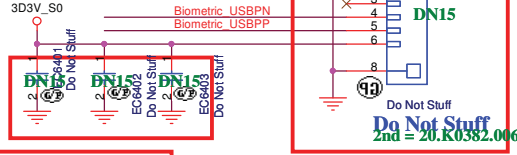
DQ15 AMD DIS SAMSUNG T1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Bluetooth	
Size A4	Document Number QUEEN AMD Muxless/UMA	Rev X00	
Date Thursday, May 26, 2011	Sheet 63	of 104	

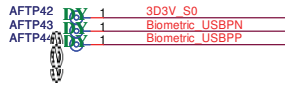
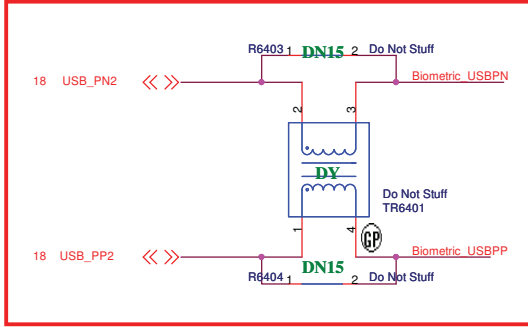
Finger Printer Connector

Finger Printer Connector

1124 X02 Modify:
 Add EC6402 0.1uF, EC6403 180pF and stuff EC6401
 47pF from RF fine tune result.



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0



DQ15 AMD DIS SAMSUNG T1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title: F/P	
Size: A4	Document Number:	Rev:	
Date: Thursday, May 26, 2011		QUEEN AMD Muxless/UMA00	
2	Sheet	64	of 104

WLAN CONN In Daughtter BD



DQ15 AMD DIS SAMSUNG T1



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

Title		WLAN	
Size	Document Number	Rev	
A0	QUEEN AMD Muxless/UMX00		
Date: Thursday, May 26, 2011		Sheet	65 of 104

<http://hobi-elektronika.net>

Remove For DG12 M12 SPEC




DD15 AMD DIS SAMSUNG TI

		Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		WWAN	
Size	Document Number	Rev	
A3	QUEEN AMD Muxless/UMA00		
Date: Thursday, May 26, 2011		Sheet	66 of 104

<http://hobi-elektronika.net>

(Blanking)

DQ15 AMD DIS SAMSUNG TI

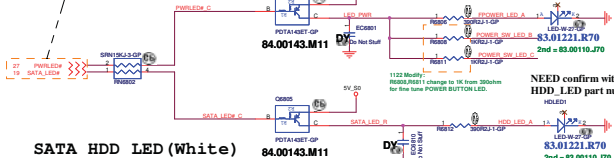
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		Reserved
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00
Date:	Thursday, May 26, 2011	Sheet 67 of 104

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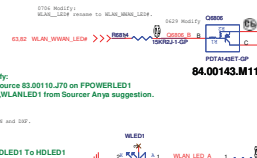
0928 Modify:
 Rename CHARGER_LED1 to CHARGERLED1.
 Rename FPOWER_LED1 to FPOWERLED1.
 Rename HDD_LED1 to HDDLED1.
 Rename TP_LOCK_LED1 to TPLOCKLED1.
 Rename TP_LOCK_LED2 to TPLOCKLED2.
 Rename WLAN_LED1 to WLANLED1
 0105 Modify:
 Change Part Reference FPOWERLED1 To FPLED1

FRONT POWER LED

Need change to LOW activated from KBC GPIO



WLAN_LED



SATA HDD LED (White)

NEED confirm with ME actual FPOWER_LED part number.



NEED confirm with ME actual HDD_LED part number.

Battery LED2 (WHITE_LED)

Need change to LOW activated from KBC GPIO



Battery LED1 (AMBER_LED)

Need change to LOW activated from KBC GPIO



TPLOCK LED

Need change to LOW activated from KBC GPIO



NEED confirm with ME actual HDD_LED part number.



SKEW	ITEM1	ITEM2
DQ15	PWRBTN1	TP_LOCK_LED1
DN15	PWRBTN2	TP_LOCK_LED2

0914 Modify:
 CORRECT PWR_BTN_LEDS SPEC.
 maybe by can combine with FPOWER_LED.
 Then PWR_BTN_LED can reserved for other function.



0105 Modify:
 ESM Request
 0304 Modify:
 ESM Request To Pop EC6808 83.M504A.AA0
 0321 Modify:
 Change EC6808 Source To 83.1040Z.0A0



0921 Modify:
 Add APTX Follow DQ15 Intel
 0921 Modify:
 Add 2nd source 83.00326.070 on CHARGER_LED from Sourcer Arjya suggestion.
 1122 Modify:
 Change R6813 to 1K from 390ohm for fine tune LED illumination
 0105 Modify:
 Change Part reference name From TPLOCKLED1/TPLOCKLED2 To TPLED1/TPLED2



DQ15 AMD DS SARGUNG T1

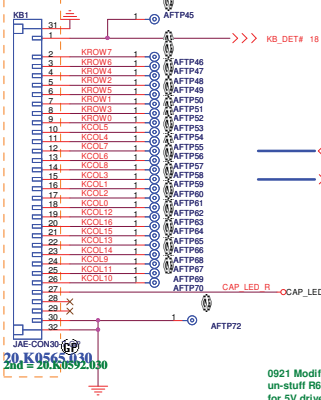
Wistron Corporation
 2/F, 8F, 9F, 11/F, 12/F, 13/F, 14/F, 15/F, 16/F, 17/F, 18/F, 19/F, 20/F, 21/F, 22/F, 23/F, 24/F, 25/F, 26/F, 27/F, 28/F, 29/F, 30/F, 31/F, 32/F, 33/F, 34/F, 35/F, 36/F, 37/F, 38/F, 39/F, 40/F, 41/F, 42/F, 43/F, 44/F, 45/F, 46/F, 47/F, 48/F, 49/F, 50/F, 51/F, 52/F, 53/F, 54/F, 55/F, 56/F, 57/F, 58/F, 59/F, 60/F, 61/F, 62/F, 63/F, 64/F, 65/F, 66/F, 67/F, 68/F, 69/F, 70/F, 71/F, 72/F, 73/F, 74/F, 75/F, 76/F, 77/F, 78/F, 79/F, 80/F, 81/F, 82/F, 83/F, 84/F, 85/F, 86/F, 87/F, 88/F, 89/F, 90/F, 91/F, 92/F, 93/F, 94/F, 95/F, 96/F, 97/F, 98/F, 99/F, 100/F

LED Bard/Power Button
 QUEEN AMD Muxless/UMA
 04/20/2011

1122 Modify:
Add 2nd 20.K0592.030 on KB1 from ME updated connector list.

Internal Keyboard Connector

0630 Modify:
Change KB1 part number to 20.K0565.030 base on ME updated KB1 and COV.

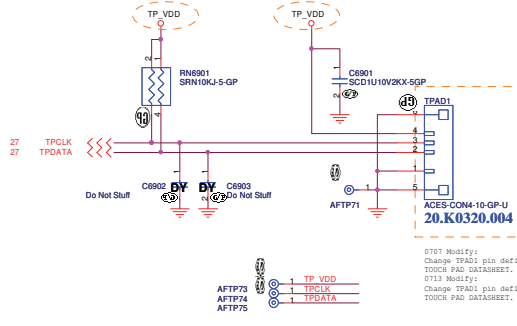


0921 Modify:
un-stuff R6907 and stuff R6905, Q6902, R6906
for SV drive CAP LED.
0109 Modify: CAP LED Change To Low Active From KBC GPIO
0109 Modify: R6906 Change To 1K

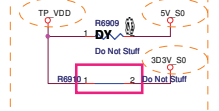
0624 Modify:
Add CAP LED Control circuit (Q6902, R6905, R6907)
and Connect CAP_LED_R control to KB1 pin27 from
KBC GPIO (High active).

SSID = Touch.Pad

0713 Modify:
Change TPAD1 power source to 3D3V_S0 from
5V_S0 base on DELL latest spec A02.
TouchPad Connector



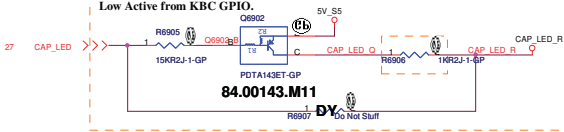
0715 Modify:
Add R6908, R6909 for TPAD1 co-lay power option.
0109 Modify:
Change TP_VDD To 3D3V_S0, Follow Intel



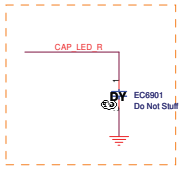
MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

CAP LED CONTROL

Low Active from KBC GPIO.

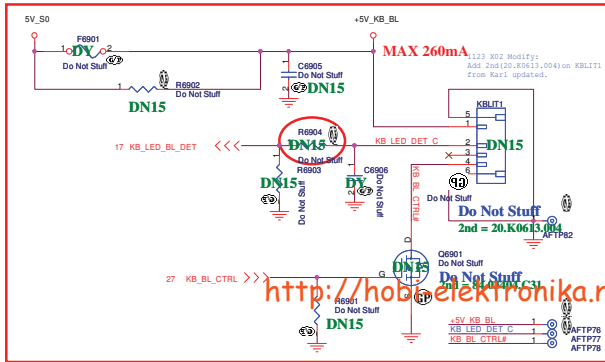


0719: EMI Request



MB CONN.	(FFC)
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

KB Backlight Connector



<http://hobbyelektronika.net>

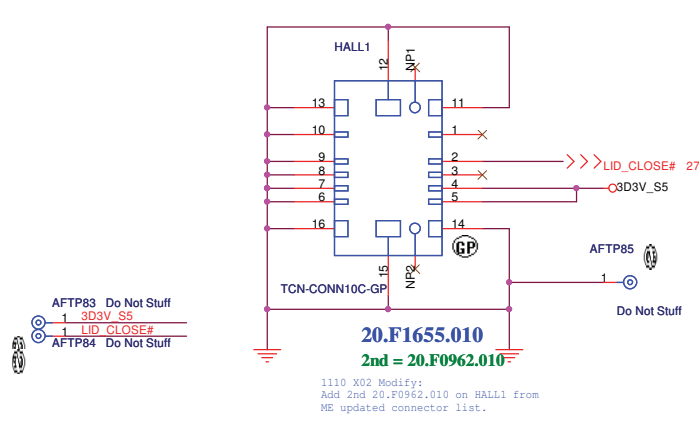
DQ15 AMD DIS SAMSUNG T1

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title		Key Board/Touch Pad	
Size	Document Number	Rev	
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SSID = Hall.Sensor

0906 Modify:
HALL SENSOR move to small board at X01 stage,so
Removed HALLSW1 related circuit and add HALL1
connector.
1122 Modify:
Add 2nd 20.F0962.010 on HALL1 from
ME updated connector list.

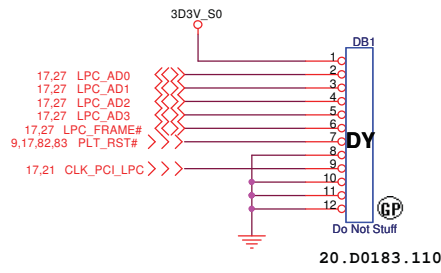


DQ15 AMD DIS SAMSUNG T1

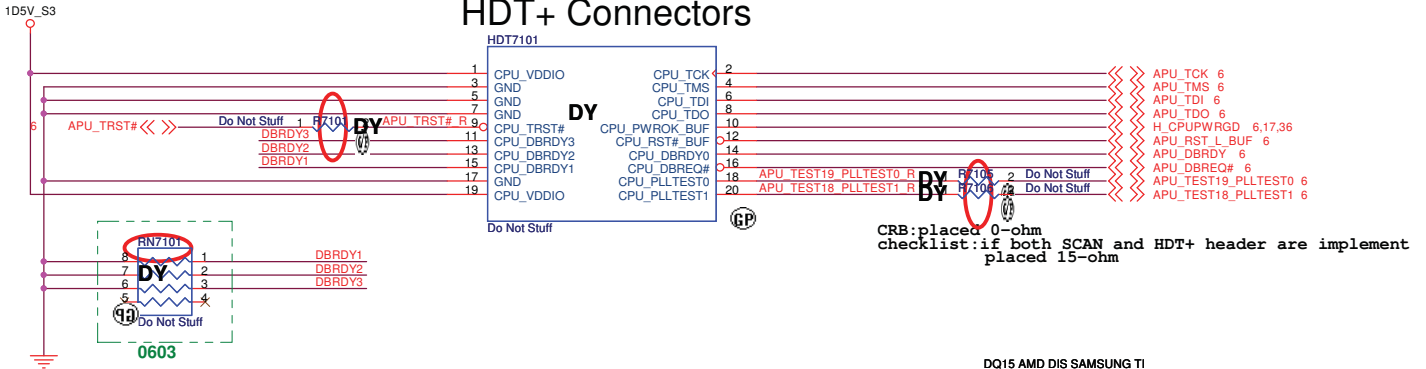
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Size A4	Document Number QUEEN AMD Muxless/UMA	Rev X00
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SSID = Debug



HDT+ Connectors




DQ15 AMD DIS SAMSUNG TI

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		Title Dubug connector	
Size A4	Document Number	Rev	
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DQ15 AMD DIS SAMSUNG TI

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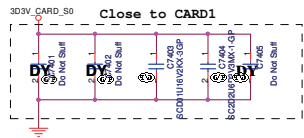
<http://hobi-elektronika.net>

DD15 AMD DIS SAMSUNG TI

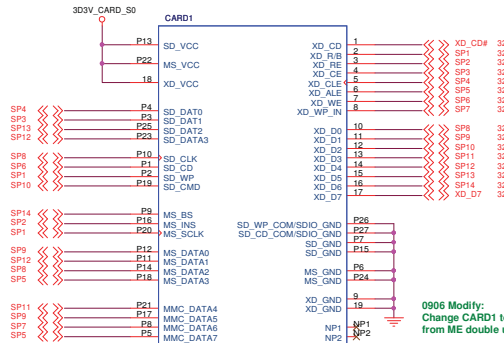
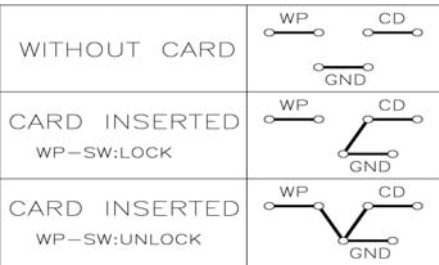
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Title		Reserved
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QUEEN AMD Muxless/UMA00		

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SSID = SDIO



SD/XD/MS/MMC+ Card Reader

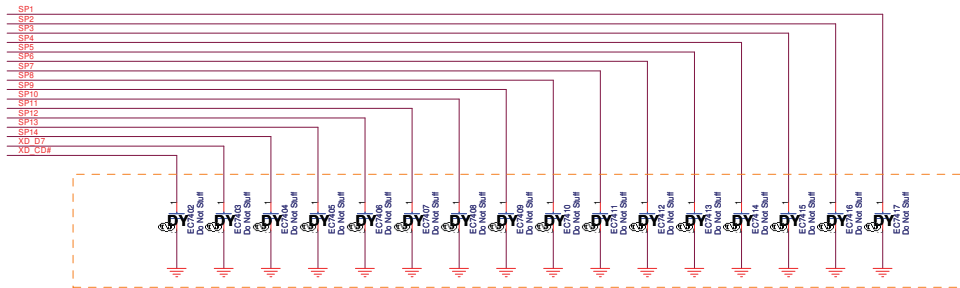


0906 Modify:
Change CARD1 to 20.10129.001 from 62.10051.931
from ME double updated latest DXF&EMN on X01.

0928 Modify:
Updated CARD1 footprint to R013-P12-HM-1
from data base updated footprint.

1122 Modify:
Add 2nd 20.10135.001 on CARD1 from
ME updated latest connector list.

For EMI Reserved



0913: Schematic Score Card Suggest Cap Less Than 10P

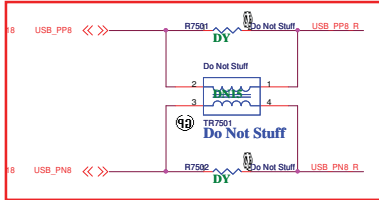
20.10129.001			
Pin	TYPE	FUNCTION	RTSS138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3DV_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	CARD_S0
P21	MMC PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3DV_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM	GND
P27	SD	SD-CD COM	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-RB	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3DV_CARD_S0
#19	XD	XD-GND	GND

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

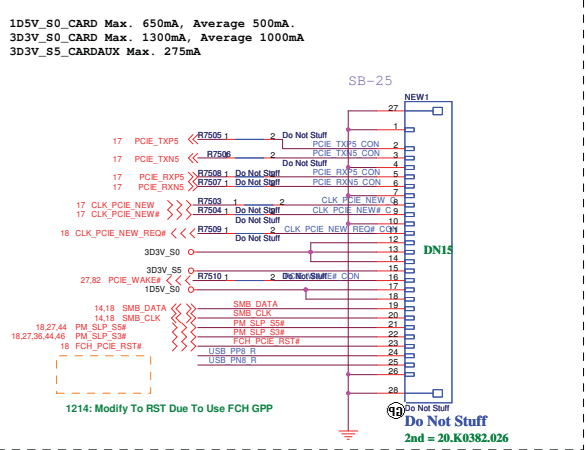
File: **CARD Reader CONN**
Size: A3 Document Number: **QUEEN AND Muxless/UMA** Rev: **X00**
Date: Thursday, May 26, 2011 Sheet: 74 of 104

SSID = ExpressCard

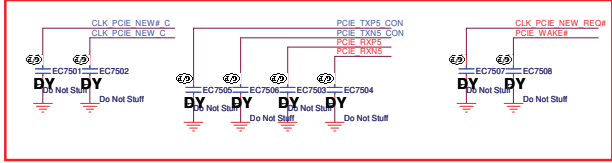
1123 302 Modify:
 Change TR7501 DM choke to 69.10103.043
 and un-stuff R7501, R7502 from BMC Neo Suggestion.
 Change R7501, R7502 to 0603 from 0402.
 1123 302 Modify:
 SWAP TR7501 pin1&4 and pin2&3 each other
 base on Chrome swmp report.



Do Not Stuff	AFTP107	1	3D3V_S5
Do Not Stuff	AFTP107	1	3D3V_S0
Do Not Stuff	AFTP107	1	1D5V_S0
Do Not Stuff	AFTP107	1	USB_PNB_R
Do Not Stuff	AFTP107	1	USB_PPB_R
Do Not Stuff	AFTP107	1	CLK_PCIE_NEW_REQ#_CON
Do Not Stuff	AFTP107	1	SMB_CLK
Do Not Stuff	AFTP107	1	SMB_DATA
Do Not Stuff	AFTP107	1	PM_SLP_SS#
Do Not Stuff	AFTP107	1	PM_SLP_SS#
Do Not Stuff	AFTP107	1	FCH_PCIE_RST#_C
Do Not Stuff	AFTP107	1	CLK_PCIE_NEW#_C
Do Not Stuff	AFTP107	1	CLK_PCIE_NEW#_C
Do Not Stuff	AFTP107	1	PCIE_TXNS_CON
Do Not Stuff	AFTP107	1	PCIE_TXNS_CON
Do Not Stuff	AFTP107	1	PCIE_RXPS_CON
Do Not Stuff	AFTP107	1	PCIE_RXPS_CON
Do Not Stuff	AFTP107	1	PCIE_WAKE#_CON
Do Not Stuff	AFTP107	1	PCIE_WAKE#_CON



For EMI



DD15 AMD DS SAMSUNG TI


DELL Wistron Corporation
 21F, 8th, Sect.1, Hsin Tai Wu Rd., Hsinchu,
 Taipei Hsien 321, Taiwan, R.O.C.

File: **Express Card**

Size: AS	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
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Reserved		
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A4		
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DD15 AMD DIS SAMSUNG TI

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Title		Reserved
Size A3	Document Number	Rev
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QUEEN AMD Muxless/UMA00		

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DQ15 AMD DIS SAMSUNG T1

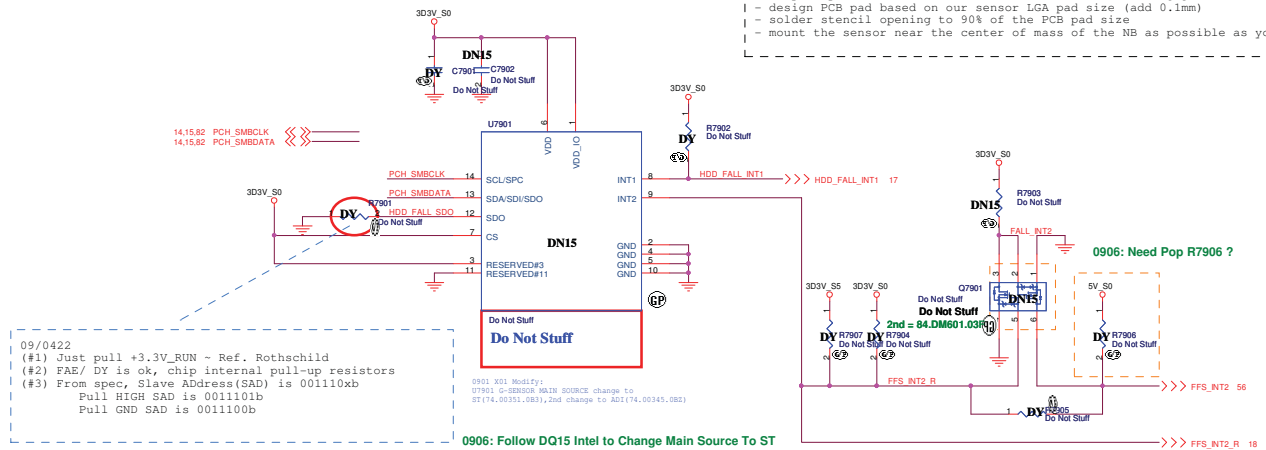


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<i>Reserved</i>		
Size	Document Number	Rev
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Free Fall Sensor

Note
 - no via, trace, under the sensor (keep out area around 2mm)
 - stay away from the screw hole or metal shield soldering joints
 - design PCB pad based on our sensor LGA pad size (add 0.1mm)
 - solder stencil opening to 90% of the PCB pad size
 - mount the sensor near the center of the mass of the NB as possible as you can



09/0422
 (#1) Just pull +3.3V_RUN ~ Ref. Rothschild
 (#2) FAE/ DY is ok, chip internal pull-up resistors
 (#3) From spec, Slave Address(SAD) is 001110xb
 Pull HIGH SAD is 0011101b
 Pull GND SAD is 0011100b

Note
 (1) Keep all signals are the same trace width. (included VDD, GND).
 (2) No VIA under IC bottom.

DO15 AMD DIS SAMSUNG TI

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Title: **Free Fall Sensor**

Size: A3 Document Number: **QUEEN AMD Muxless/UMX00** Rev: 1

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DQ15 AMD DIS SAMSUNG TI



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Title

Reserved

Size

Document Number

Rev

A

QUEEN AMD Muxless/UMAX00

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DQ15 AMD DIS SAMSUNG TI



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

UNUSED PARTS/EMI Capacitors

Size

Document Number

Rev

A4

QUEEN AMD Muxless/UMA

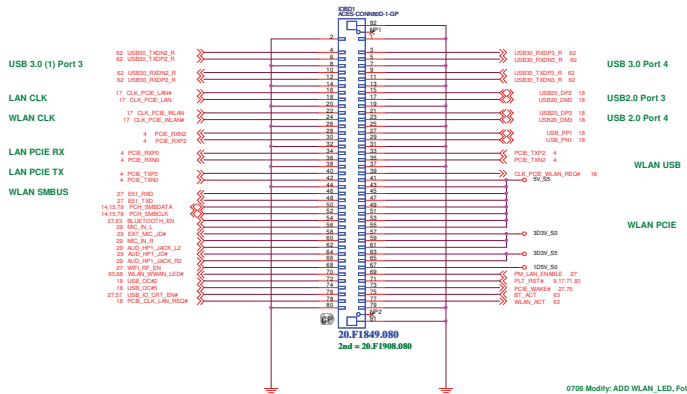
X00

Date: Thursday, May 26, 2011

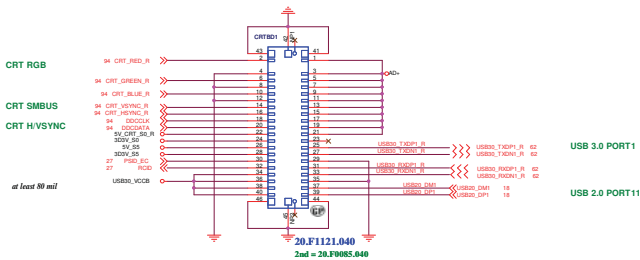
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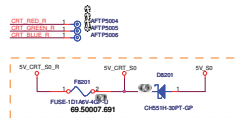
IO Board CONN 80 pin



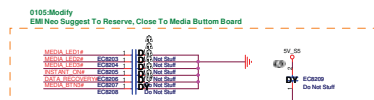
0706 Modify: ADD WLAN_LED, Follow Intel, AMD Dont have WLAN
 1123 Modify: Change Main Source To 20.F1849.080 & Add 2nd 20.F1908.080 on IOBD1 from ME updated latest connector list & Modify Pin Define So 4 corner pin are GND.



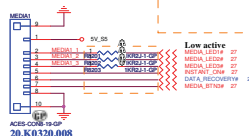
0914 Modify:
 Change BTB Connector To 20.F1121.040
 Follow ME Connector List
 1228 Modify:
 Remove USB 3.0 Signal and Re-arrange Pin-Define For Better Layout Routing
 1118 Modify:
 Modify Pin Define



0906 Modify:
 Change Part Number 20.K0422.010 To 30.K0320.008
 Base On ME Connector List
 0914 Modify:
 Change R2021 - R2023 to 470 ohm from 33ohm
 for fine tune MEDIA_LED Sink current
 0928 Modify:
 Change R2021 - R2023 to 430 ohm from 470 ohm
 for fine tune MEDIA_LED 5mA current.



0105 Modify:
 EMI Noo Suggest To Reserve, Close To Media Bottom Board



Low active



0921 Modify:
 Add AFP, Follow DQ15 Intel

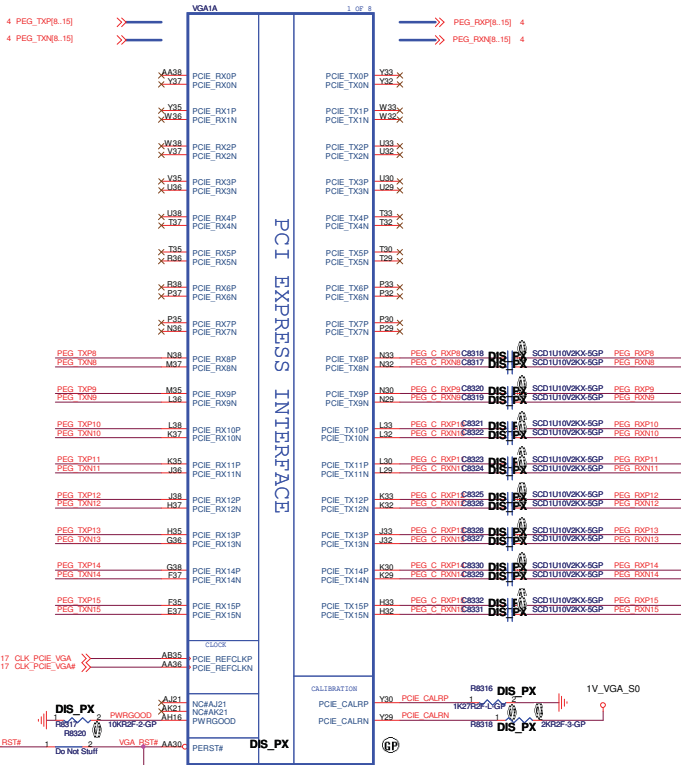


1122 Modify:
 change Media resistor from 430 ohm to 1K on both DQD15 (R2021, R2022, R2023) for Media button LED light spot lesse

DQ15 AND DQ16 SAMPLING TI

IO Board Connector
 QUEEN AMD Muxless/UMA
 Rev: 1.00
 Date: 11/25/2011

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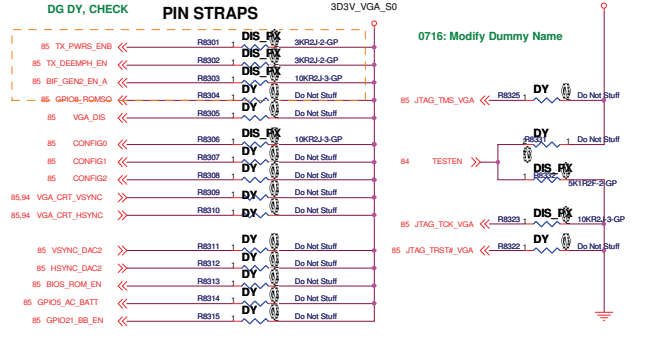


CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCIe device as 2.5GT/s capable at power on. 1: Advertises the PCIe device as 5.0GT/s capable at power on.	0	1
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1: Config[2:0] defines the ROM type BIOS_ROM_EN=0: Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0: Disable external BIOS ROM device 1: Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]: 1: Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSNC		X	1

Full Tx output swing. Must be pulled to 3.3 V at reset using ~3-K (5%) resistor.



JTAG SIGNAL OPTION - for option2

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC

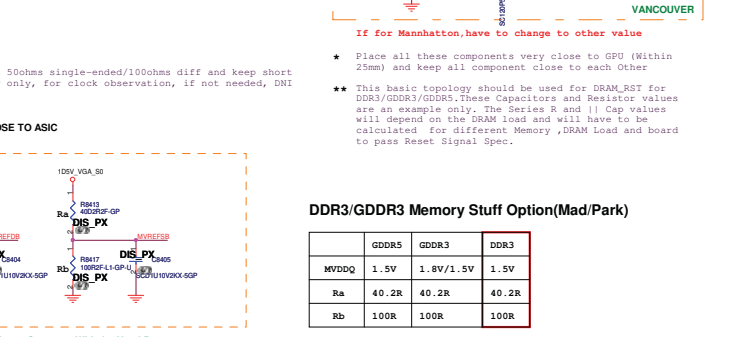
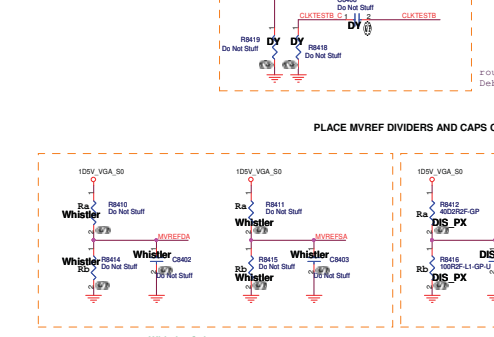
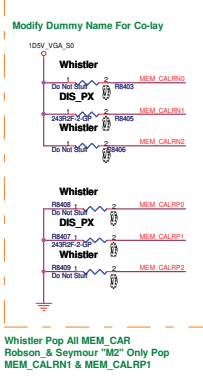
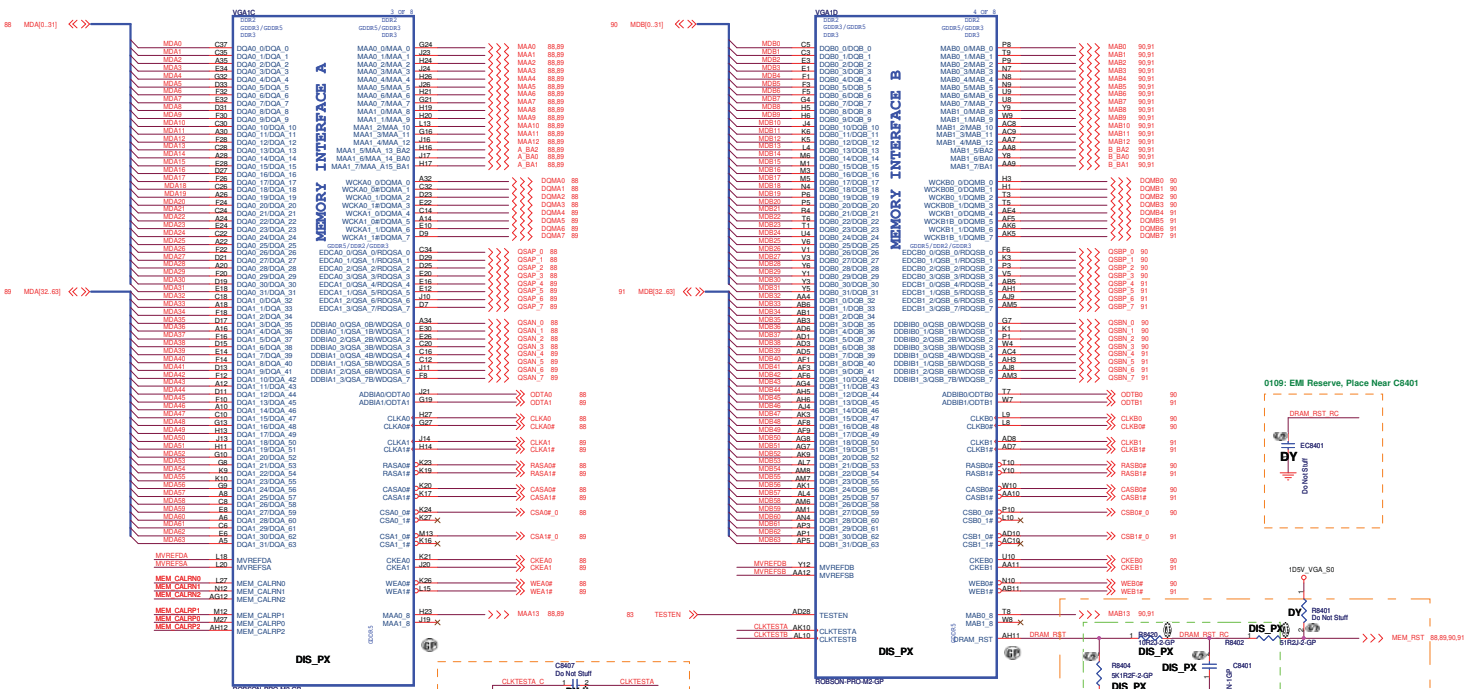
1008: Add Level Shift For APU_RST# To 3.3V

DQ15 AMD DIS SASLING T1



Doc	Document Number	Rev
GPU	GPU PCIe/STRAPPING(1/5)	1.0
Std	Custom	QUEEN AMD Muxless/UMA
Date	Thursday, May 26, 2011	Sheet 83 of 104

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Whistler Pop All MEM_CAR
Robson_ & Seymour "M2" Only Pop
MEM_CALRN1 & MEM_CALRP1

Whistler Only

Robson_Seymour_Whistler Need Pop

<http://hobi-elektronika.net>

0109: EM Reserve, Place Near C5401

DRAM_RST_PC

EC9401

105V_VGA_50

MEM_RST

MEM_RST_0

MEM_RST_1

MEM_RST_2

MEM_RST_3

MEM_RST_4

MEM_RST_5

MEM_RST_6

MEM_RST_7

MEM_RST_8

MEM_RST_9

MEM_RST_10

MEM_RST_11

MEM_RST_12

MEM_RST_13

MEM_RST_14

MEM_RST_15

MEM_RST_16

MEM_RST_17

MEM_RST_18

MEM_RST_19

MEM_RST_20

MEM_RST_21

MEM_RST_22

MEM_RST_23

MEM_RST_24

MEM_RST_25

MEM_RST_26

MEM_RST_27

MEM_RST_28

MEM_RST_29

MEM_RST_30

MEM_RST_31

MEM_RST_32

MEM_RST_33

MEM_RST_34

MEM_RST_35

MEM_RST_36

MEM_RST_37

MEM_RST_38

MEM_RST_39

MEM_RST_40

MEM_RST_41

MEM_RST_42

MEM_RST_43

MEM_RST_44

MEM_RST_45

MEM_RST_46

MEM_RST_47

MEM_RST_48

MEM_RST_49

MEM_RST_50

MEM_RST_51

MEM_RST_52

MEM_RST_53

MEM_RST_54

MEM_RST_55

MEM_RST_56

MEM_RST_57

MEM_RST_58

MEM_RST_59

MEM_RST_60

MEM_RST_61

MEM_RST_62

MEM_RST_63

MEM_RST_64

MEM_RST_65

MEM_RST_66

MEM_RST_67

MEM_RST_68

MEM_RST_69

MEM_RST_70

MEM_RST_71

MEM_RST_72

MEM_RST_73

MEM_RST_74

MEM_RST_75

MEM_RST_76

MEM_RST_77

MEM_RST_78

MEM_RST_79

MEM_RST_80

MEM_RST_81

MEM_RST_82

MEM_RST_83

MEM_RST_84

MEM_RST_85

MEM_RST_86

MEM_RST_87

MEM_RST_88

MEM_RST_89

MEM_RST_90

MEM_RST_91

MEM_RST_92

MEM_RST_93

MEM_RST_94

MEM_RST_95

MEM_RST_96

MEM_RST_97

MEM_RST_98

MEM_RST_99

MEM_RST_100

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

0105 AMD DIS SAMSUNG TI

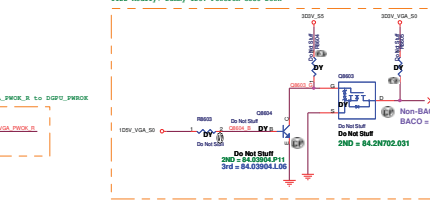
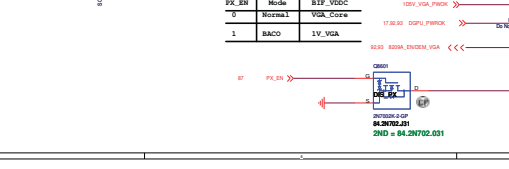
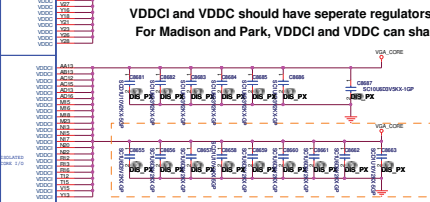
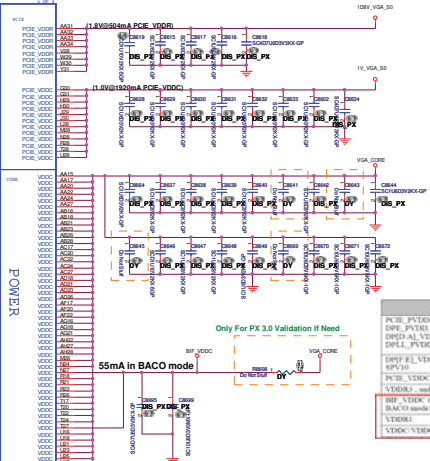
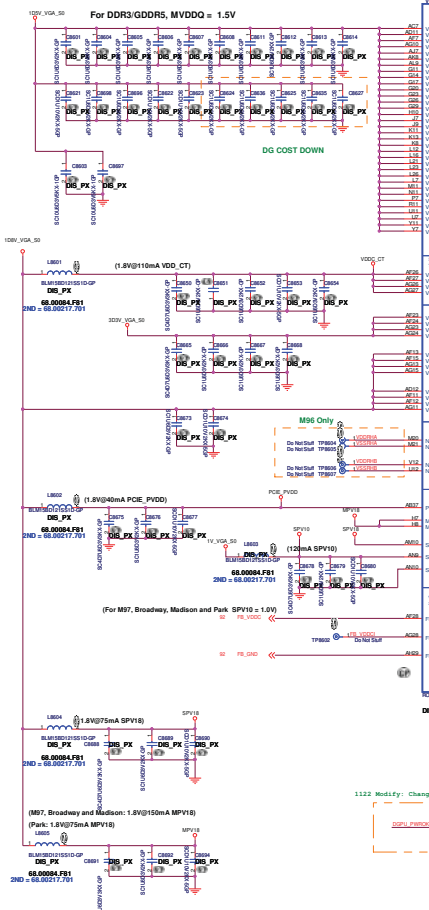
DELL Wistron Corporation
27F, 8F, 9F, 10F, 11F, 12F, 13F, 14F, 15F, 16F, 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 28F, 29F, 30F, 31F, 32F, 33F, 34F, 35F, 36F, 37F, 38F, 39F, 40F, 41F, 42F, 43F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F, 55F, 56F, 57F, 58F, 59F, 60F, 61F, 62F, 63F, 64F, 65F, 66F, 67F, 68F, 69F, 70F, 71F, 72F, 73F, 74F, 75F, 76F, 77F, 78F, 79F, 80F, 81F, 82F, 83F, 84F, 85F, 86F, 87F, 88F, 89F, 90F, 91F, 92F, 93F, 94F, 95F, 96F, 97F, 98F, 99F, 100F

GPU Memory(2/5)

Custom QUEEN AMD Muxless/UMA

Doc: Thursday, May 26, 2011

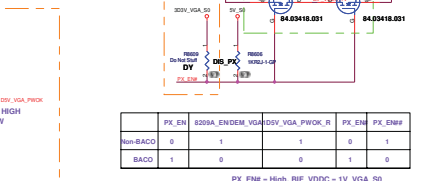
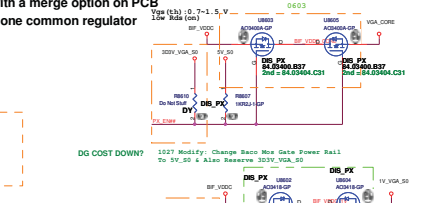
Rev: X00



SICPE Power Plan

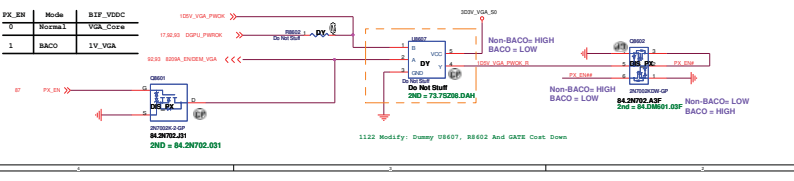
Regulator	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDQ, TVDD4, VDDA, VDD_C, DDP, PVDD, DPF1, VDD14, DPDA1, PVDD0, DPDA1_VDD10, AVDD, VDD10, AVDDQ, VDD10E, DPDA1_PVDD0, MPV18, and SPV18	1.8V	ON
DPDA1_VDD10, DPDA1_VDD10E, DPDA1_VDD10E, and SPV10	1.0V	ON
PCIE_VDDQ, VDD10, and AVDD0	1.0V	ON
VDD10E and AVDD0	2.5V	OFF
REG_VDDC (Output capacitance = 3µm, 1.1µV, 10	Same as VDDC	ON (Change to BACO mode)
VDD10E	1.8V/1.5V	OFF
VDD10E	0.8V/1.5V	OFF

VDDCI and VDDC should have separate regulators with a merge option on PCB. For Madison and Park, VDDCI and VDDC can share one common regulator.



	PX_EN	SDRA_EN/DEM_VDD_VGA_PWORK_R	PX_EN	PX_EN
Non-BACO	0	1	1	0
BACO	1	0	0	1

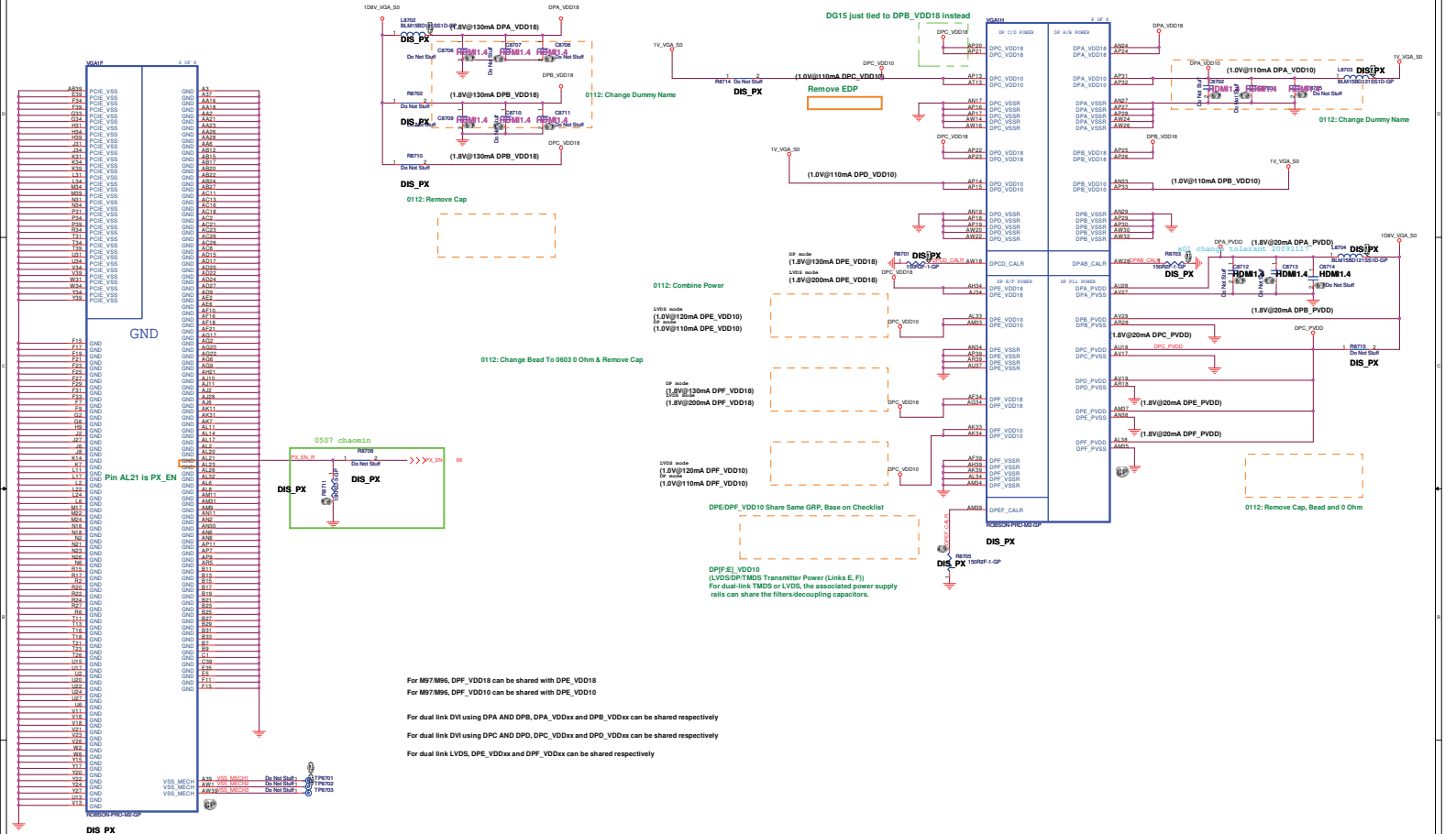
PX_EN# = High, BIF_VDDC = 1V, VGA_50
PX_EN# = High, BIF_VDDC = VGA_CORE



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GPU POWER(4/5)

QUEEN AMD Murresse/UMA

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<http://hobi-elektronika.net>

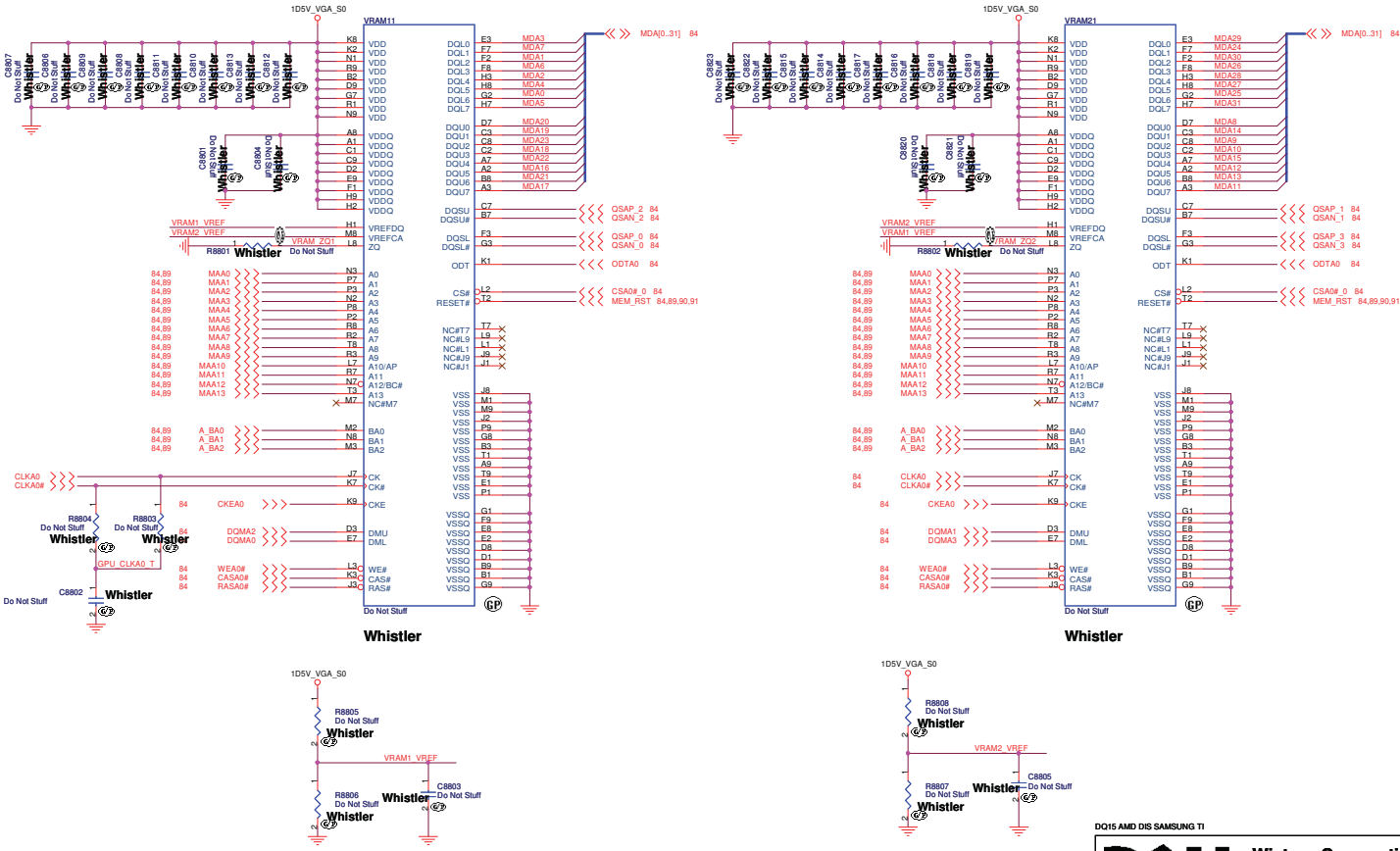
0015 AMD DES-SAMUNG T1

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 2/F, No. 261, Hsin-Tai Rd., Hsinchu, Taiwan, R.O.C.

GPU DPPWR/GND(S/S)

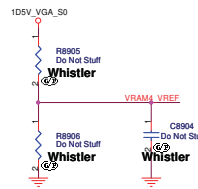
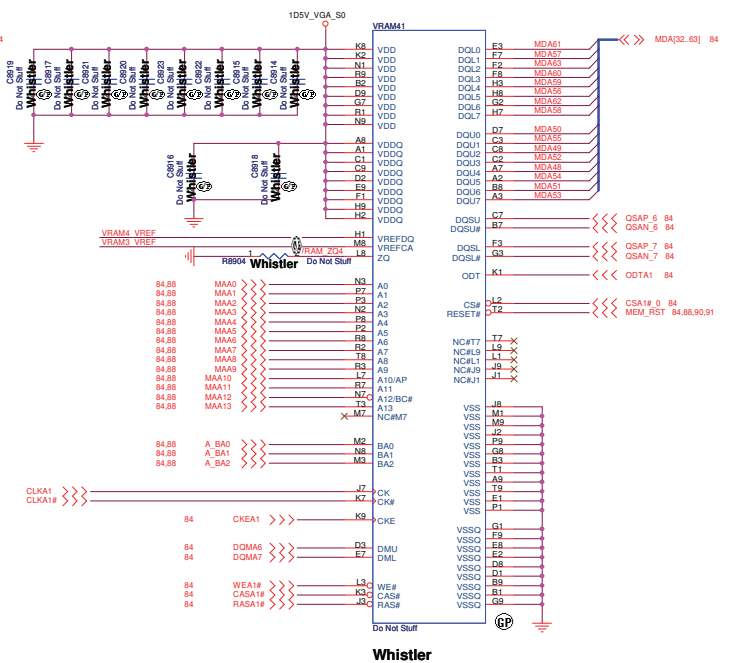
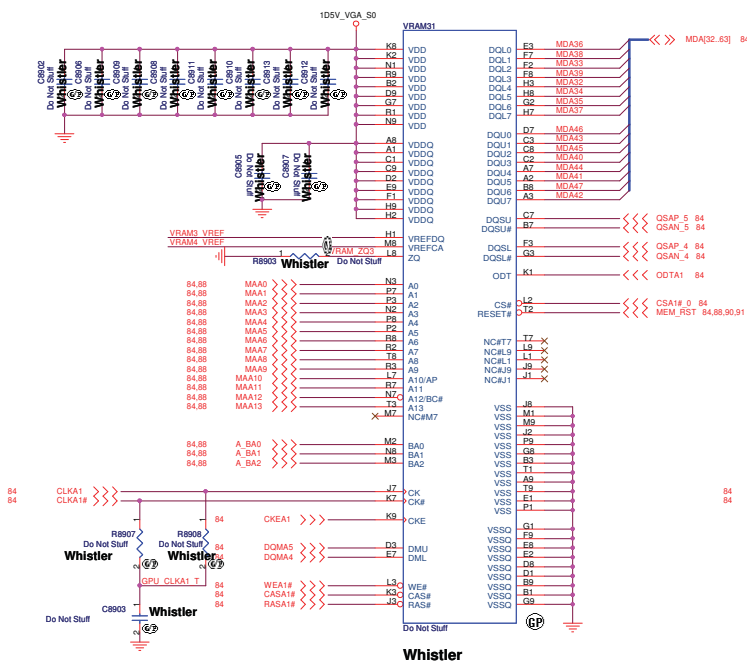
Document Name: QUEEN AMD Muxless/LMA

Doc No: 43, Rev: 01, Date: 2023.05.28



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File	GPU-VRAM1,2 (1/4)		
Size	Document Number	Rev	X00
A3		QUEEN AMD Muxless/UMA	
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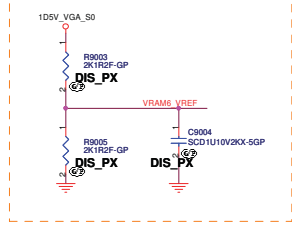
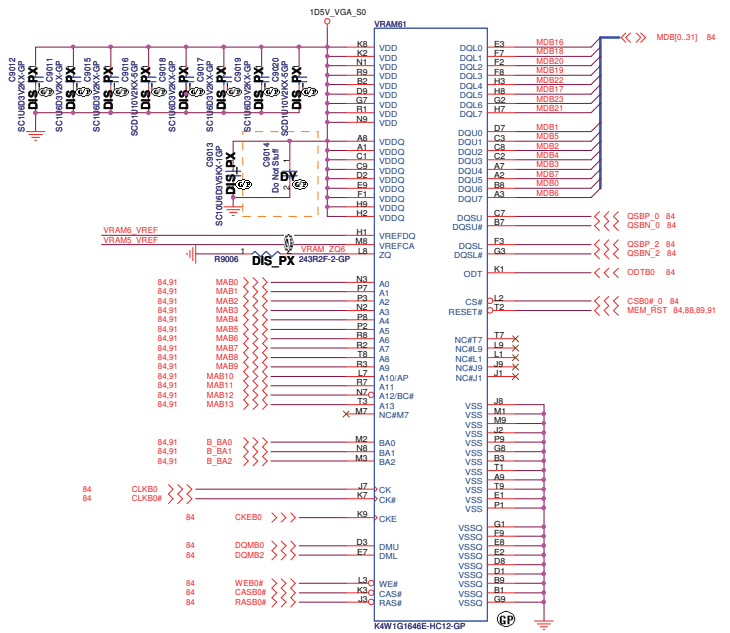
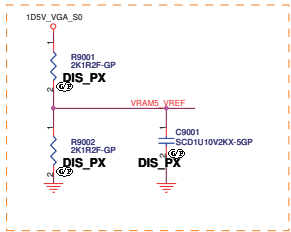
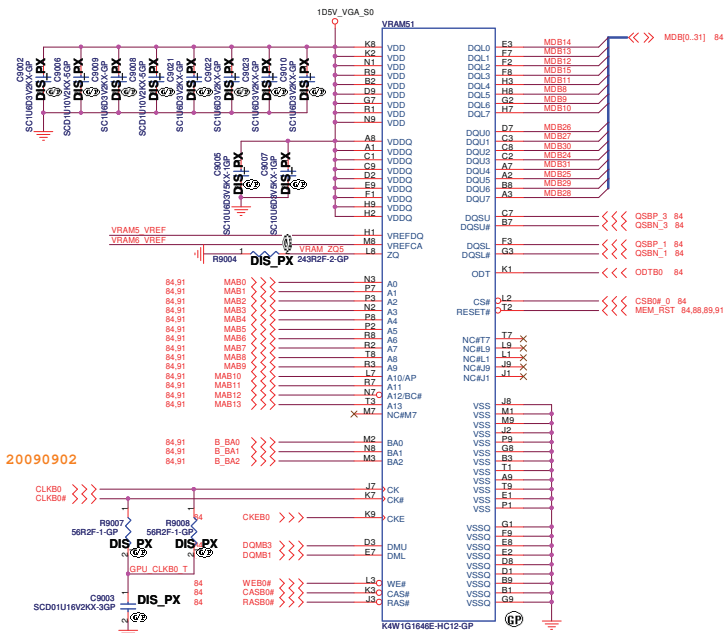


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File: **GPU-VRAM3,4 (2/4)**
 Size: A3 Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**
 Date: Thursday, May 28, 2010 Sheet: 89 of 104

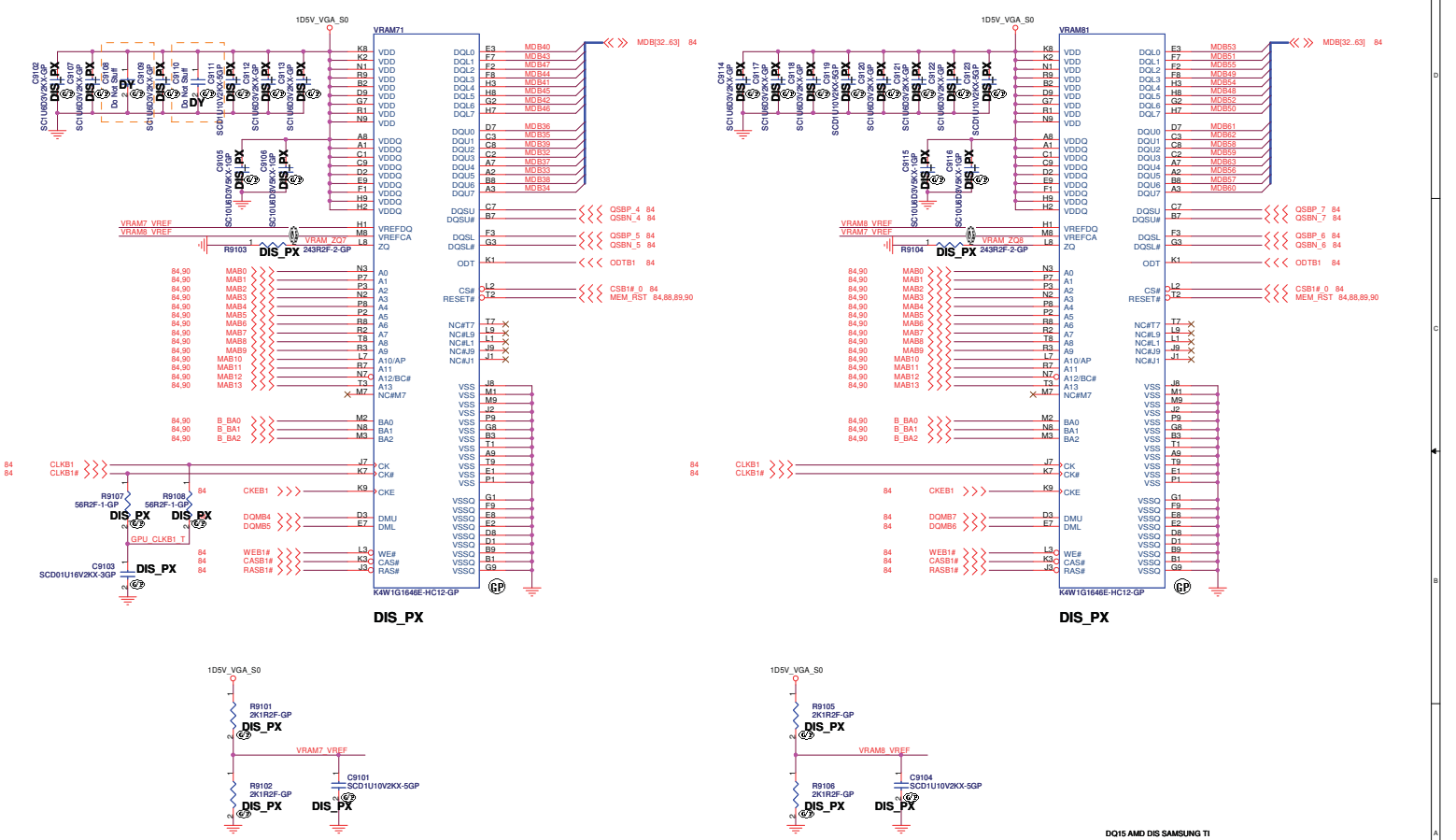
<http://hobi-elektronika.net>



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Taipei Hsien 221, Taiwan, R.O.C.

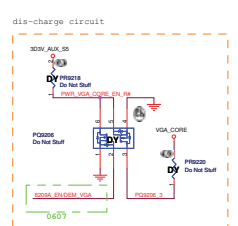
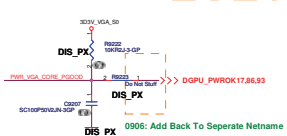
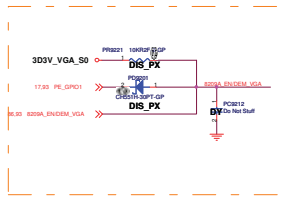
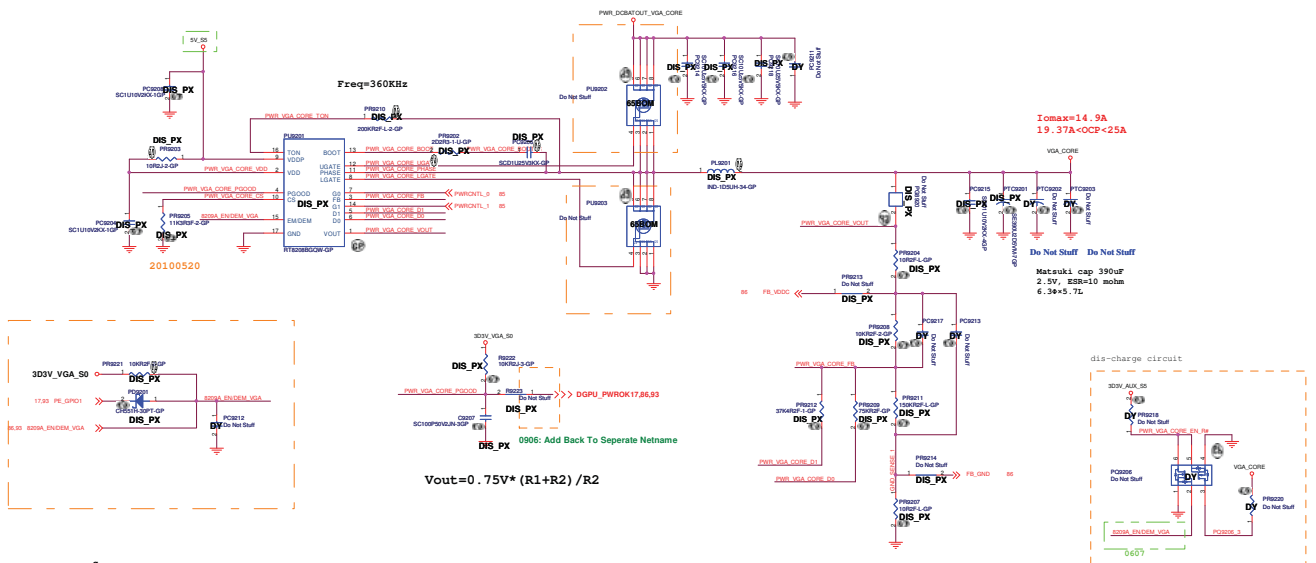
File: GPU-VRAM5.6 (3/4)
Size: A3 Document Number: QUEEN AMD Muxless/UMA Rev: X00
Date: Thursday, May 26, 2011 Sheet: 90 of 104



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 Taipei Hsien 221, Taiwan, R.O.C.

File: **GPU-VRAM7.8 (4/4)**
 Size: A3 Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**
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$V_{out} = 0.75V * (R1+R2) / R2$

Seymour:

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	R	1.0V
R	L	0.9V
R	H	X

Seymour	280208	280211	280209	280212
280212	280208	280211	280209	280212

Whistler:

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.0V
L	R	X
R	L	0.9V
R	H	X

I/P cap: 100 25V K0805 X5R/ 78.10622.51L
 Inductor: 1.5uH PCK1047-1R5MH Cynotec 3.8mOhm/4.2mOhm Isat =33Arms 68.1R510.10J
 O/P cap: 560U 2.5V M27V150MCM3K7 16mOhm 3.3Arms 77.95671.00J
 O/P cap: 220U 2V SEFCX0221R 15mOhm 2.7Arms Panasonic/79.22719.20L
 R/S: RJK03890RA / 10.9mOhm/15.1mOhm@4.5Vgs / 84.00389.837
 L/G: RJK03890RA / 4.6mOhm/5.6mOhm@4.5Vgs / 84.00389.837

DC15 AMD DIS SAMBA10

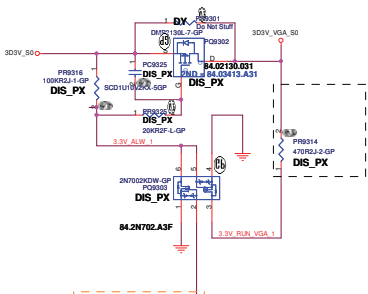
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RT8208B +VGA CORE

Document ID: **QUEEN AMD Muxless/UMA**

Rev: 1.00
 Date: 10/27/2011

+3VS to 3.3V_DELAY Transfer



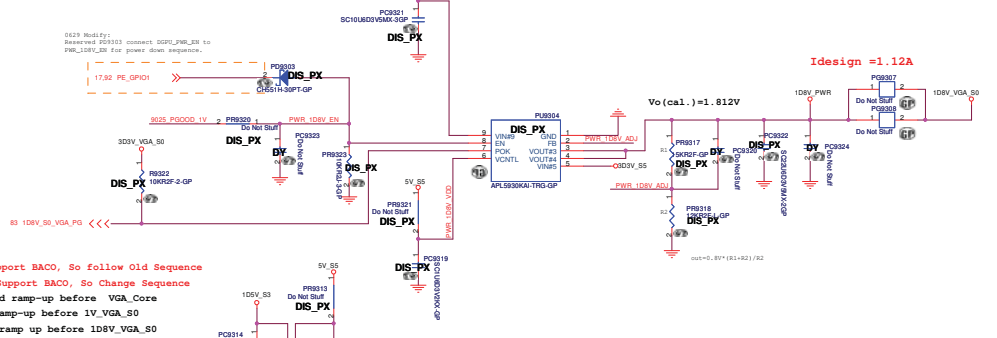
Different To Intel, AMD Is High Active

Park_Madison Does Not Support BACO, So follow Old Sequence
 Seymour_Whistler_Robson Support BACO, So Change Sequence
 3DV_VGA_S0 should ramp-up before VGA_Core
 VGA_Coresould ramp-up before 1V_VGA_S0
 1V_VGA_S0 should ramp up before 1D8V_S0
 so 1V_VGA_S0 EN have to fine tune R0C085505M3GP
 after VGA_Core

FE_GP101	PX3_0	PX4_0
I_GPU	L	H
DGPU	H	H

2nd = 84.DM601.03F

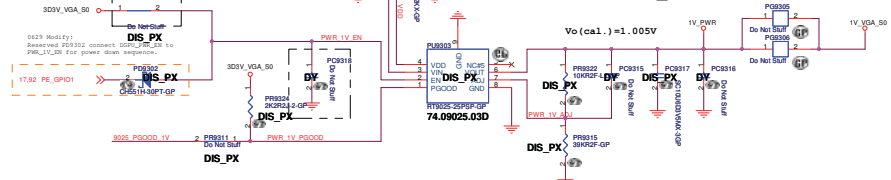
APL5930KAI for 1D8V_S0



I_{design} = 1.12A

Vo (ca1.) = 1.812V

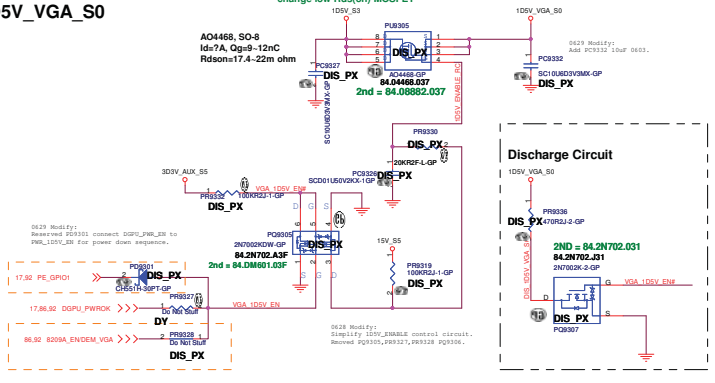
RT9025 for 1V_S0



I_{design} = 1.2A

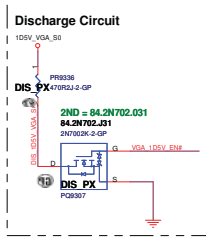
Vo (ca1.) = 1.005V

1D5V_VGA_S0



change low R_{ds(on)} MOSFET

AD4468-50-8
 Id=7A, Qg=8-12nC
 R_{ds(on)}=17.4-22mhm
 2nd = 84.08882.037

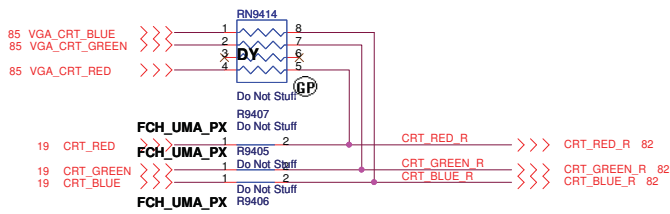
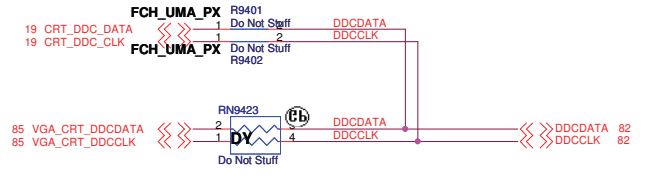
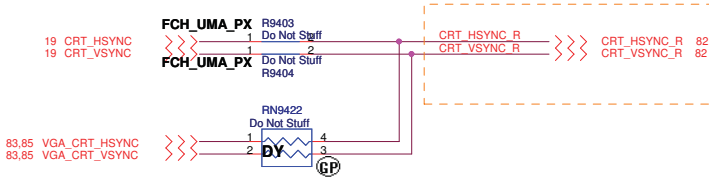


Discharge Circuit

2ND = 84.2N702.031

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SSID = VIDEO



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		Title LVDS VGA Switch	
Size	Document Number	Rev	
QUEEN AMD Muxless/UMA		x00	
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DQ15 AMD DIS SAMSUNG T1



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Title

Reserved

Size

Document Number

Rev

A

QUEEN AMD Muxless/UMAX00

Date: Thursday, May 26, 2011

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TOUCH PANEL connector



0707: Move To Page 49, Touch Panel Combine With LVDS

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Title

Touch Panel

Size

Document Number

Rev

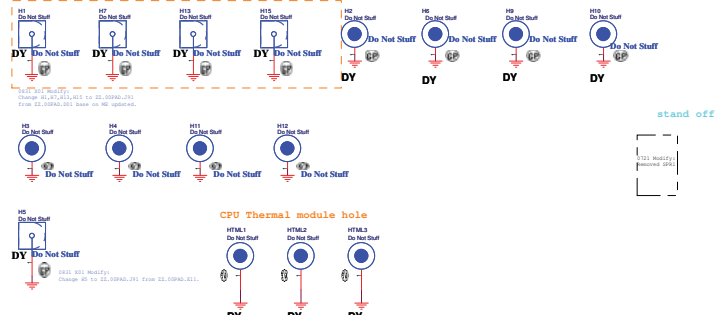
A

QUEEN AMD Muxless/UMAX00

Date: Thursday, May 26, 2011

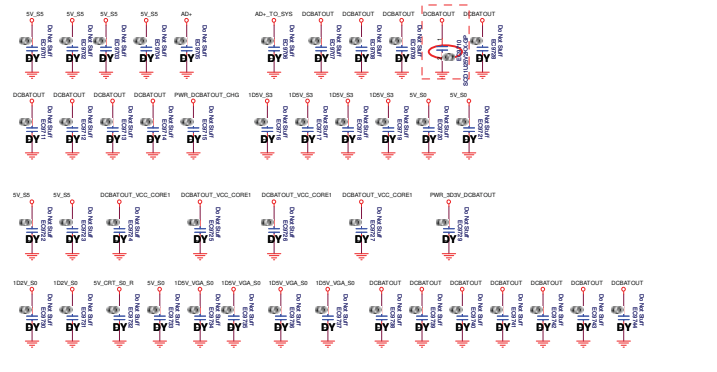
Sheet 96 of 104

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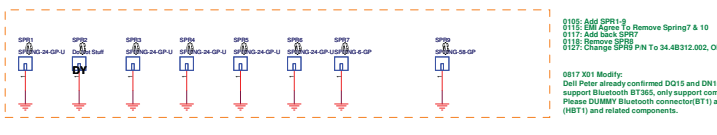
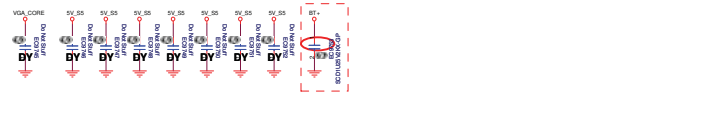


Check test point

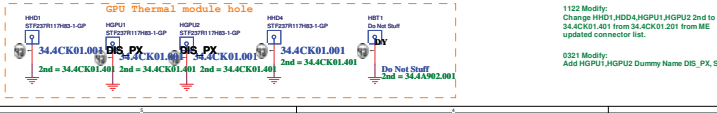
8624 Modify:
Revised A1F1,A1F7-A1F1A



- 0109: EMI Reserve EC9701-EC9704 Place: (870, 7875) Top near C3702 Bottom near FT C2033 Bottom near H15 Bottom
- 0109: EMI Reserve EC9705 Place: near P44002 Top
- 0109: EMI Reserve EC9706 Place: near C3604 Top near PR4002 Top
- 0109: EMI Reserve EC9707-EC9714,EC9728 Place: near LCD1 Top (8900, 7815) Top (8275, 7290) Top near PR4003 Top near PC4016 Top near F6003 Top (7600, 6015) Top near PC4117 Top near PC4301 Top
- 0109: EMI Reserve EC9715 Place: near PR4002 Top
- 0109: EMI Reserve EC9716-EC9719 Place: (8785, 3415) Top (8785, 2090) Top
- 0109: EMI Reserve EC9716-EC9719 Place: (8785, 3410) Top (8785, 2090) Top
- 0109: EMI Reserve EC9720-EC9721 Place: near C3604 Top near PR4002 Top
- 0109: EMI Reserve EC9722-EC9723 Place: near D3604 Top near D3604 Top
- 0109: EMI Reserve EC9724-EC9727 Place: near PC4246 Top (4300, 3985) Bottom near PC4246 Top (4300, 3985) Bottom
- 0109: EMI Reserve EC9729 Place: near PC4114 Top
- 0109: EMI Reserve EC9730-EC9731 Place: near C765 Top near PTC4203 Top



- 0110: Add SPR1-8
- 0111: EMI Agmt: To Remove Spring7 & 10
- 0112: Add back SPR7
- 0113: Remove SPR9
- 0127: Change SPR9 P/N To 34.4B312.002, Old P/N No Block
- 0817 X01 Modify: Dell Peter already confirmed Q015 and DN15 will not support Bluetooth BT365, only support combo Wireless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (BRT1) and related components.



- 1122 Modify: Change H8D1,H8D4,H8D11,H8D12 to 34.4CK01.001 from 34.4CK01.001 from ME updated connector list.
- 0321 Modify: Add H8D1,H8D2 Dummy Name DIS_PX, So UMA Wort Pop

0015 AMD DIS SAMUNG TI

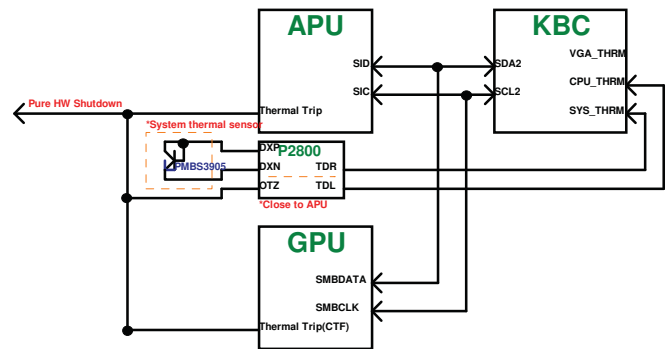
DELL Wistron Corporation
217, 26, Sec. 2, Hsin Tai Hsiang Rd., Hsinchu, Taiwan, R.O.C.

Document Number: **UNUSED PARTS/CAP**

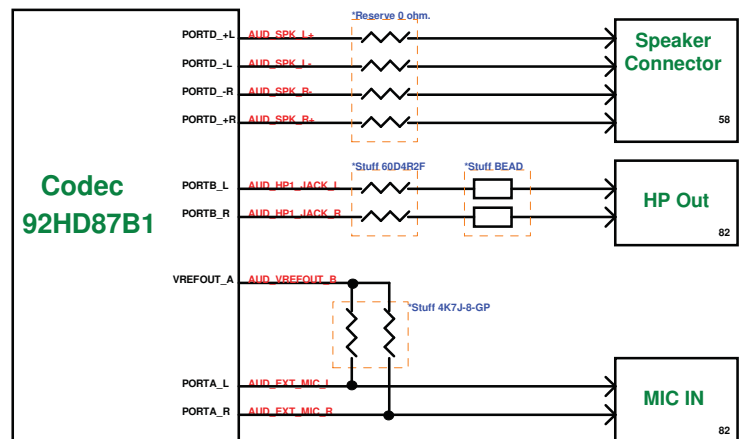
QUEEN AMD Wireless/UMA X001

Date: November, May 26, 2011

Thermal Block Diagram

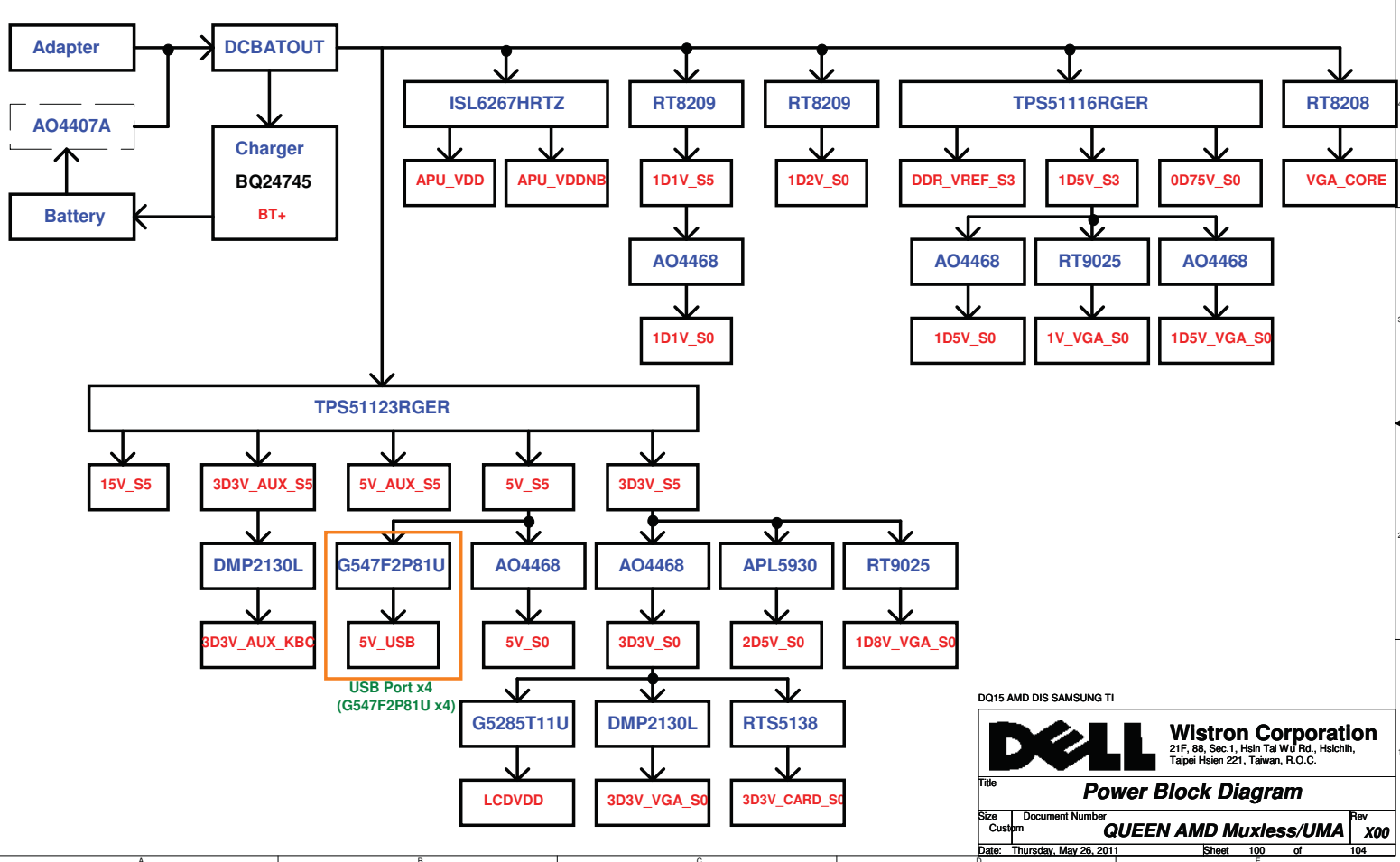


Audio Block Diagram



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 Title: **THERMAL/AUDIO BLOCK DIAGRAM**
 Size: A3 Document Number: **QUEEN AMD Muxless/UMA** Rev: **X00**
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DQ15 AMD DIS SAMSUNG TI

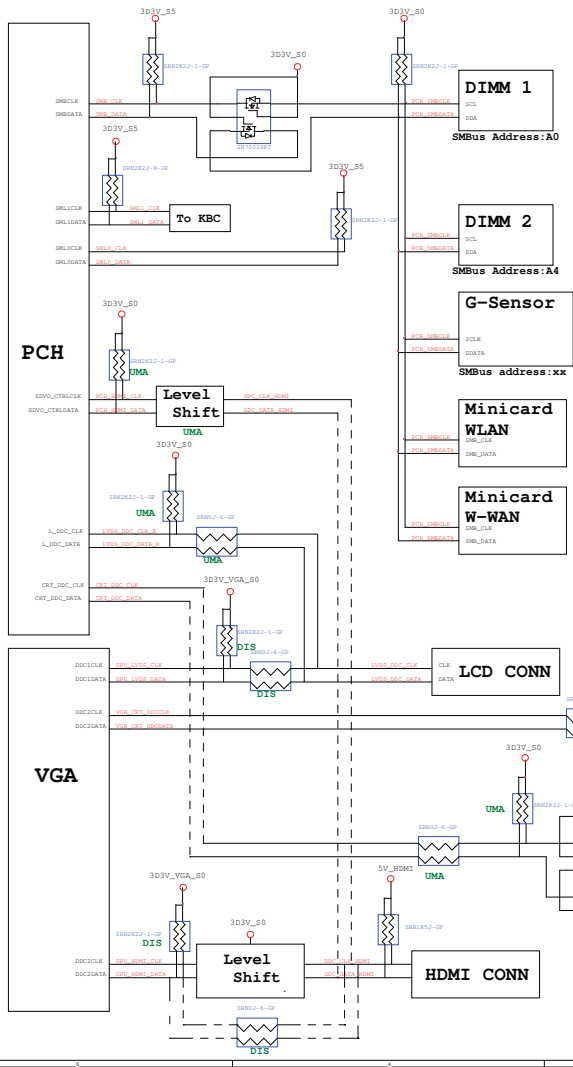
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

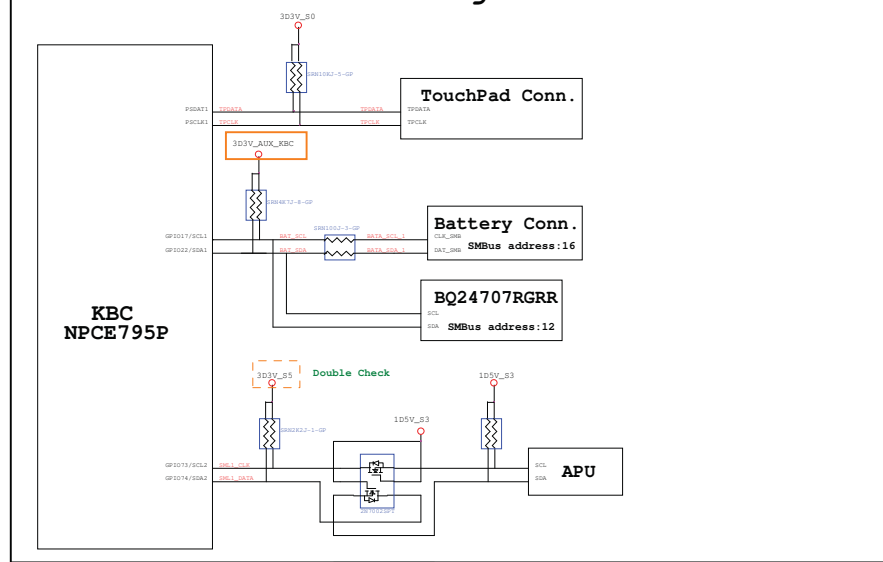
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PCH SMBus Block Diagram



KBC SMBus Block Diagram



0015 AND DIS SAMSIANG TI

DELL Wistron Corporation
 5/F, 35, Sec. 1, Ring 1st Rd, Hsinchu, Taiwan, R.O.C.

Doc: **SMBUS BLOCK DIAGRAM**

Part: **QUEEN AMD Muxless/UMA** X90

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VERSION	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER	
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE	
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE	
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE	
	01/11	1	68	Change KB1 P/N.	According ME request.	ME	
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE	
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE	
		2	10	Add R1041 OR.	Add OR for level shift off.	EE	
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE	
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power	
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE	
	A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
			2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
			3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
			4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
02/10		1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power	
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME	
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE	
02/22		1	54	Remove co-layout pad.	As factory request.	EE	
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE	
		3	48	Delete Power Gap.	Request by Power Team.	Power	
02/23		1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE	
02/24		1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC	
02/25		1	13	Add TP1309.	As factory request to add.	Factory	
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE	
	3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power		
	4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE		
	5	79	Remove EC7928.	Layout space limitation.	EE		
02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE		
03/03	1	60	Change SPK1 part number.	Request by ME.	ME		
03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE		

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