DQDN15 AMD QUEEN M12
Muxless /UMA Schematics Document

AMD LIANO APU FS1
AMD GPU Seymour XT

FCH HUDSON M3
PCB 10246-1
2011-05-28
REV : A00

DY :None Installed
UMA_PX:UMA and Muxless platform installed
DIS_PX:DIS and Muxless platform installed
PX:Muxless platform installed
FCH_UMA_PX:UMA_PX CRT FCH output
Whistler: For 8 X Vram
DN15: For DN15

DQ15 AMD DIS SAMSUNG TI

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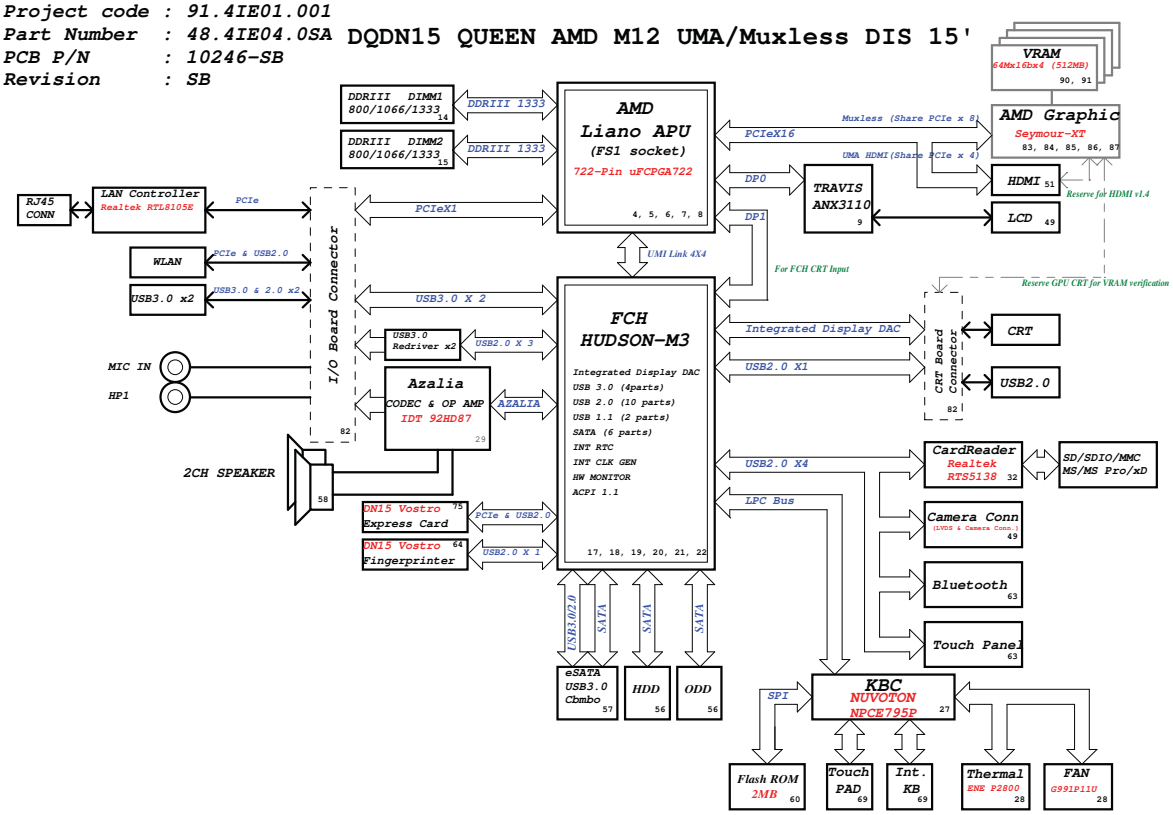
Title: Cover Page		
Size: Custom	Document Number: DQDN15 AMD QUEEN M12	Rev: X00
Date: Friday, May 27, 2011	Sheet 1 of 104	

Project code : 91.4IE01.001
Part Number : 48.4IE04.0SA
PCB P/N : 10246-SB
Revision : SB

DQDN15 QUEEN AMD M12 UMA/Muxless DIS 15'



CHARGER	
BQ24745	40
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC	
TPS51123	41
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5

APU Core/NB Power	
ISL6267HRTZ-T	42, 43
INPUTS	OUTPUTS
DCBATOUT	APU_VDD APU_VDDNB

DDRIII SUS	
TPS51116RGER	44
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

DDRIII VTT	
TPS51116RGER	44
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0

APU VDDR/VDDP	
RT8209	46
INPUTS	OUTPUTS
DCBATOUT	1D2V_S0

AMD FCH CORE Power	
RT8209	46
INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

AMD GPU CORE	
RT8208B	92
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_PWR

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

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Strapping

No Fusion Config, Strap Not needed, but reserve

REQUIRED SYSTEM STRAPS

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM DEFAULT	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB Debug Port / CRT USB 2.0
1	Mini Card (WLAN)
2	Fingerprint
3	~~WWAN~~
4	Bluetooth
5	Touch Panel
6	~~eSATA/USB Charger~~
7	CCD Camera
8	~~New Card~~
9	CardReader
10	USB 3.0 port 1
11	USB 3.0 port 2
12	USB 3.0 port 3
13	USB 3.0 port 4

PCIe Routing

	APU
LANE0	LAN
LANE1	~~WWAN~~
LANE2	WLAN
LANE3	~~CardReader~~

	FCH
LANE0	
LANE1	~~Express Card~~
LANE2	
LANE3	

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Title: Table of Content

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A3	QUEEN AMD Muxless/UMA	X00

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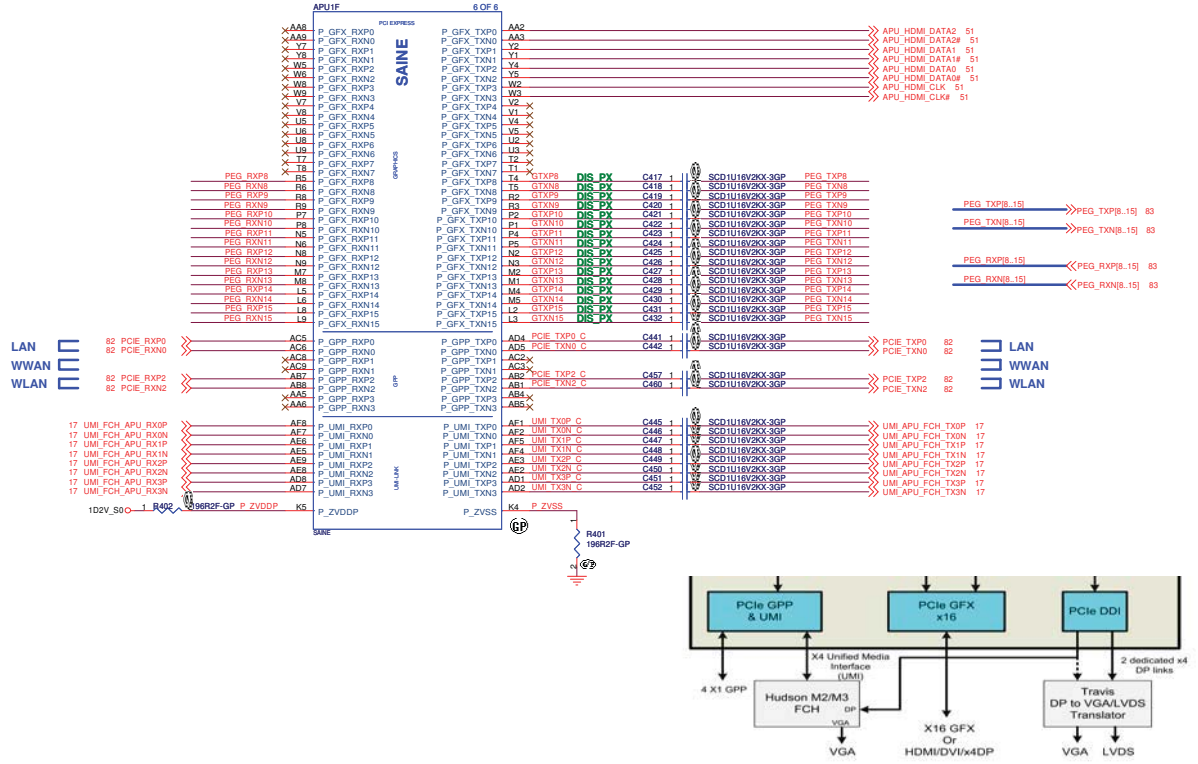

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Title	APU_PCIE(1/5)	
Size: A3	Document Number: QUEEN AMD Muxless/UMA	Rev: 1.00
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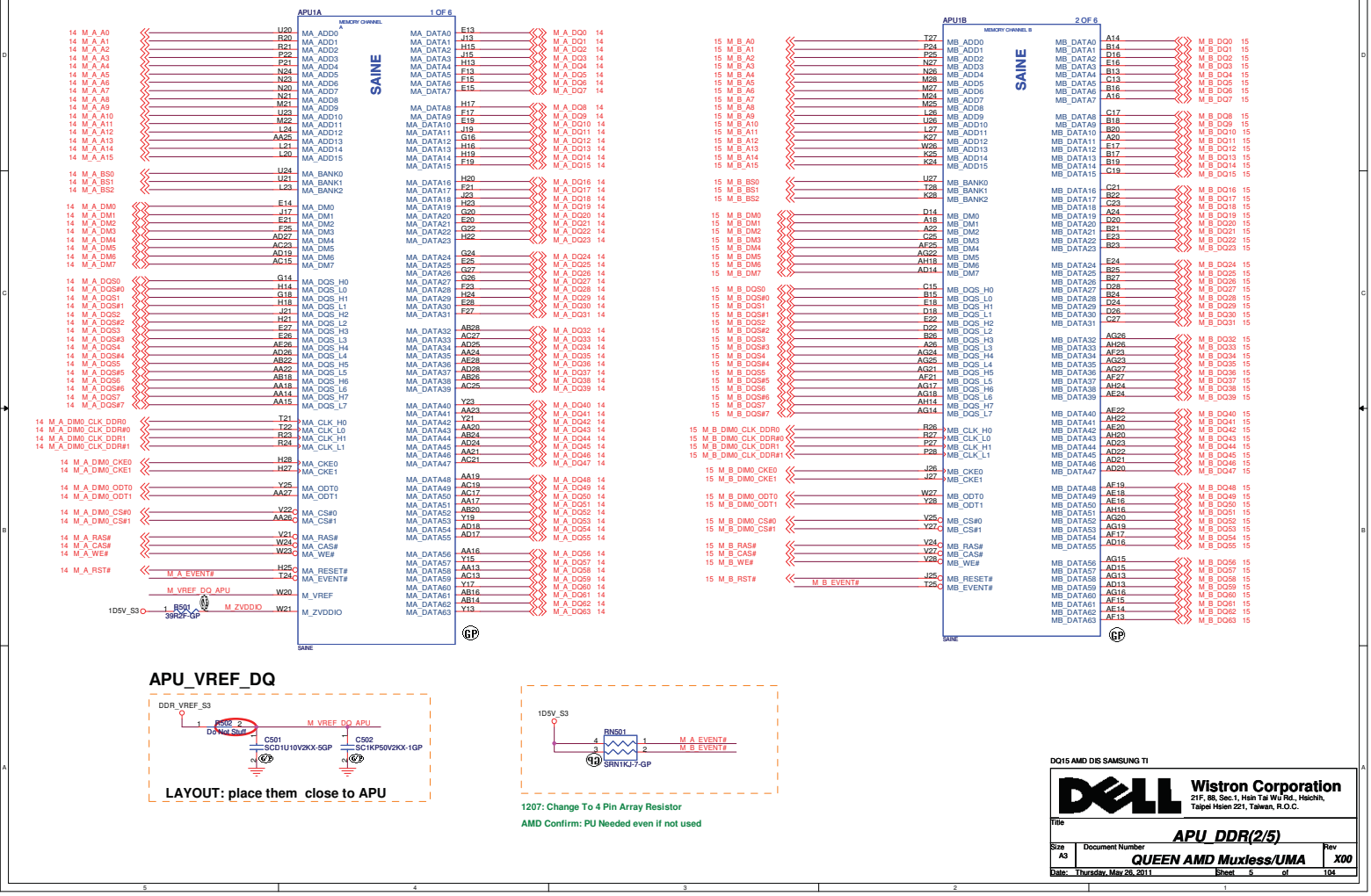

APU_VREF_DQ

1207: Change To 4 Pin Array Resistor

AMD Confirm: PU Needed even if not used

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Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

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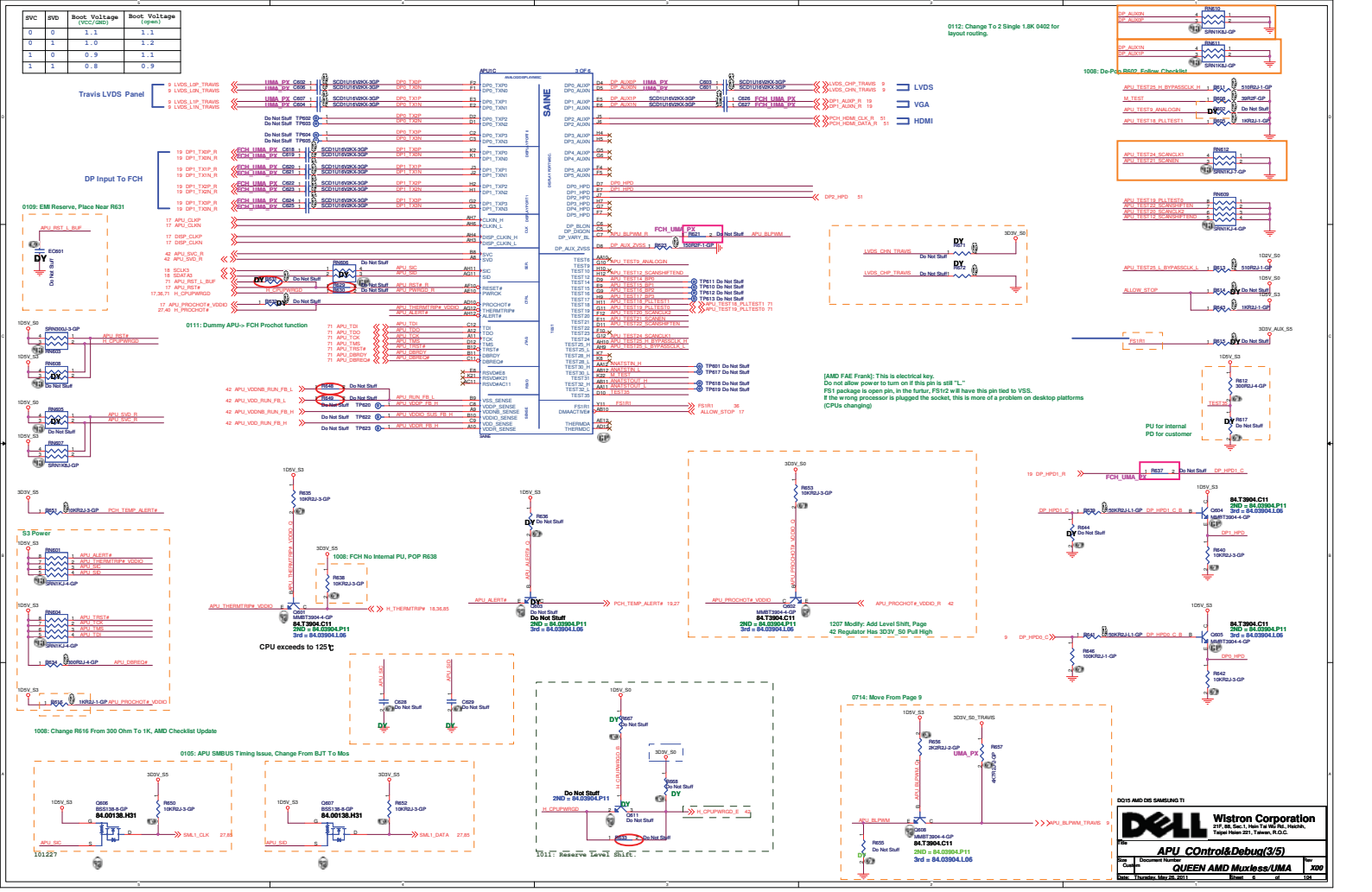

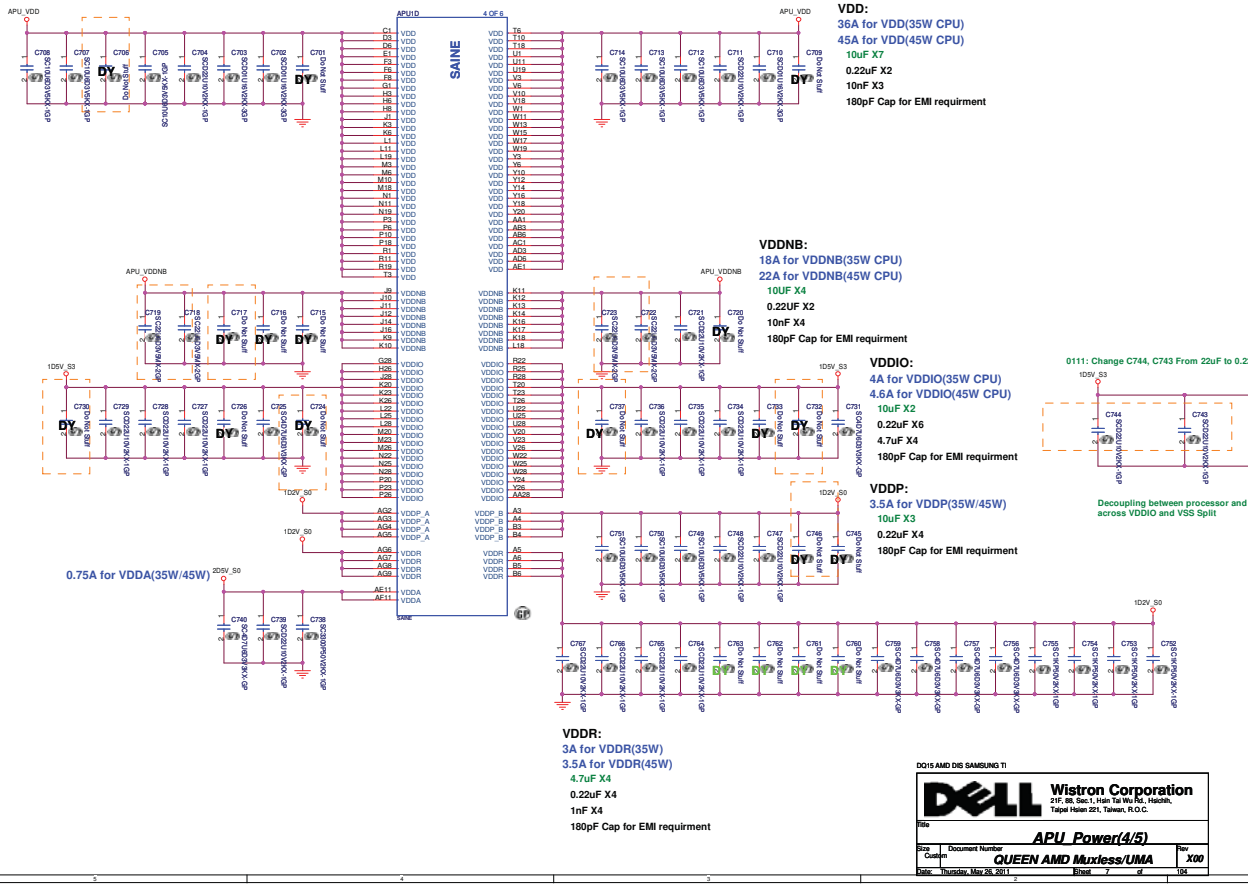

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Title: APU_Power(4/5)

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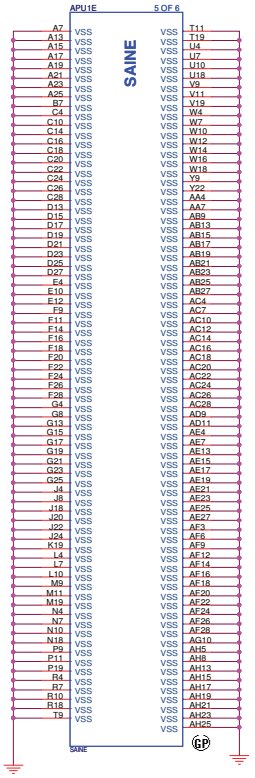

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Title: APU_VSS(5/5)

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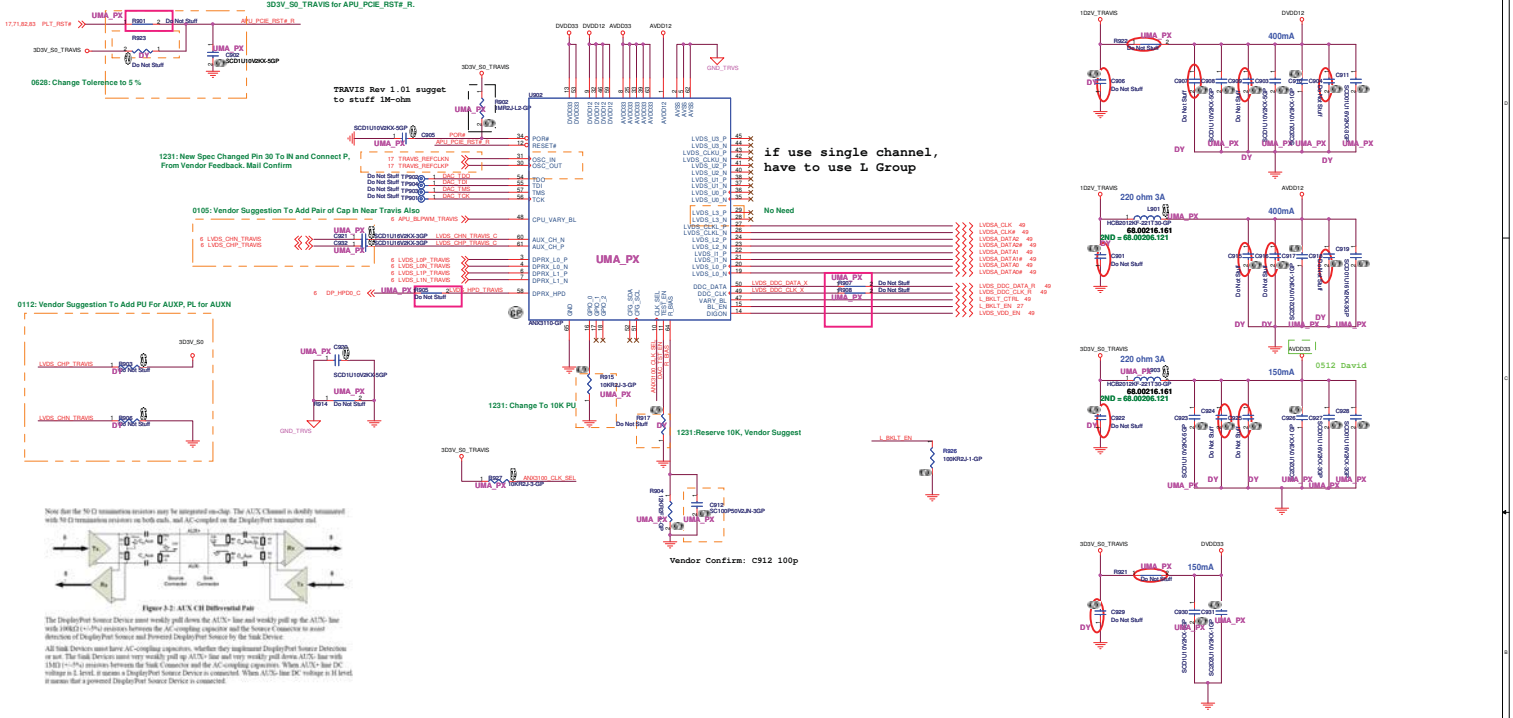
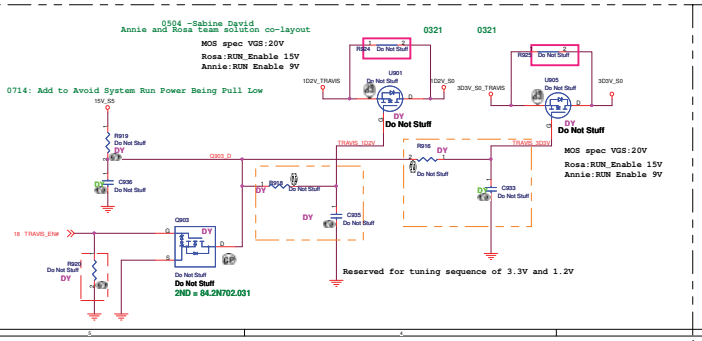


Figure 3-2: AUX CH Differential Pair

The DisplayPort Source Device must weakly pull down the AUX+ line and weakly pull up the AUX- line with 100KΩ (+/-5%) resistors between the AC coupling capacitor and the Source Connector to assist detection of DisplayPort Source and Powered DisplayPort Source by the Sink Device.

All Sink Devices must have AC-coupling capacitors, whether they implement DisplayPort Source Detection or not. The Sink Devices must very weakly pull up AUX+ line and very weakly pull down AUX- line with 1MΩ (+/-5%) resistors between the Sink Connector and the AC-coupling capacitors. When AUX+ line DC voltage is L level, it means a DisplayPort Source Device is connected. When AUX- line DC voltage is H level, it means that a powered DisplayPort Source Device is connected.



ANX9834 power on delay time

For ANX3100 ALSO

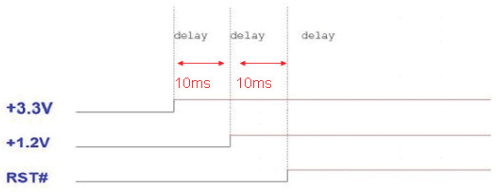


Figure 2 power supply sequencing

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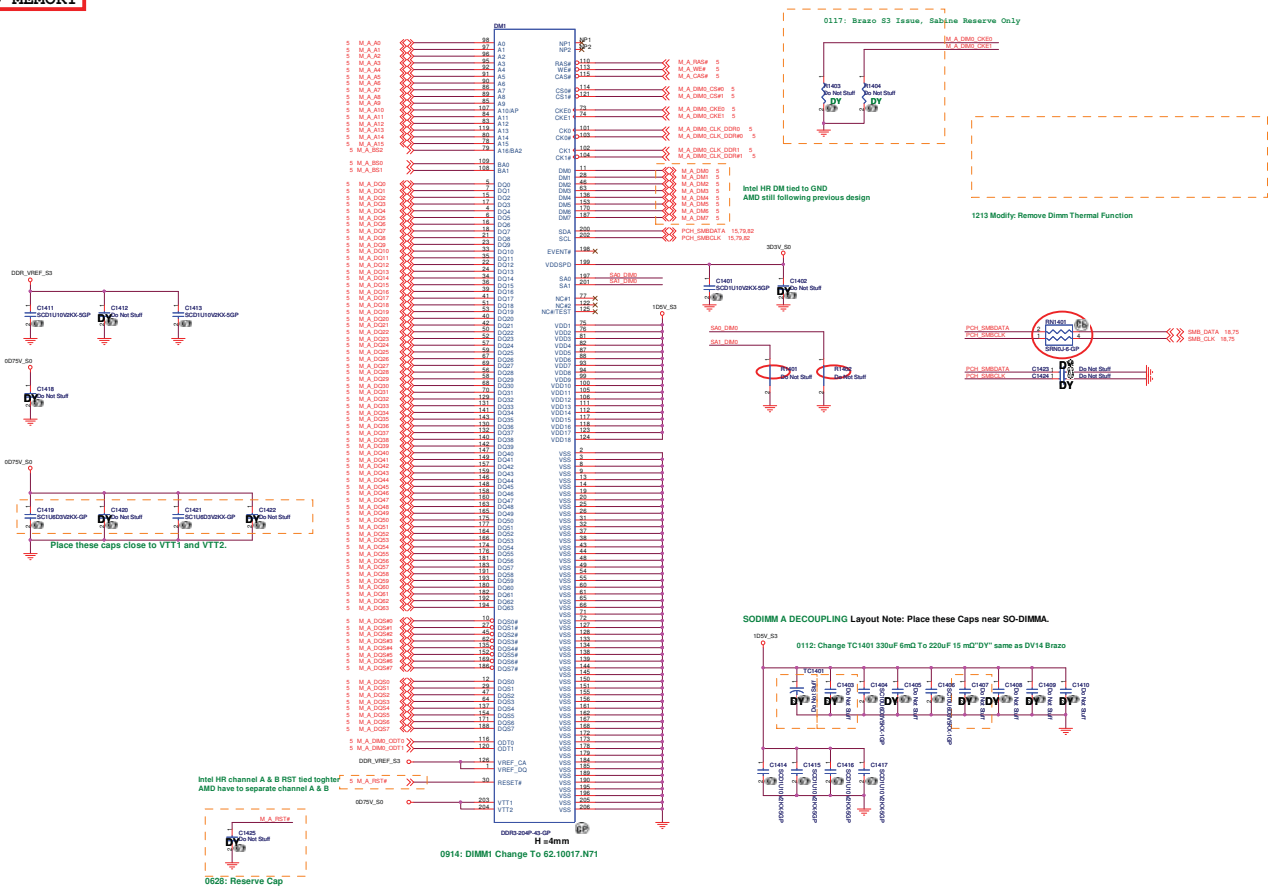
SSID = MEMORY



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File: DDR3-SODIMM1

Size	Document Number	Rev
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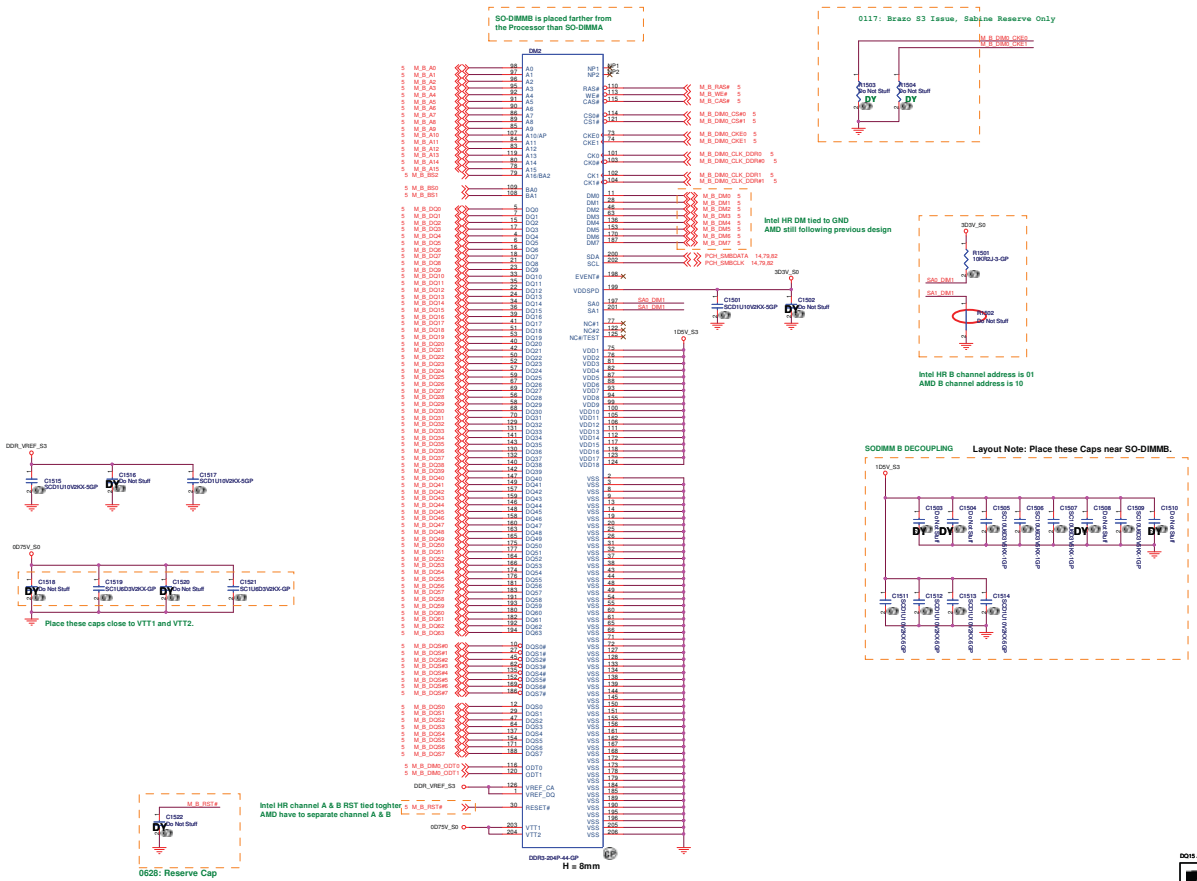
SSID = MEMORY



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Title: DDR3-SODIMM2

Size	Document Number	Rev
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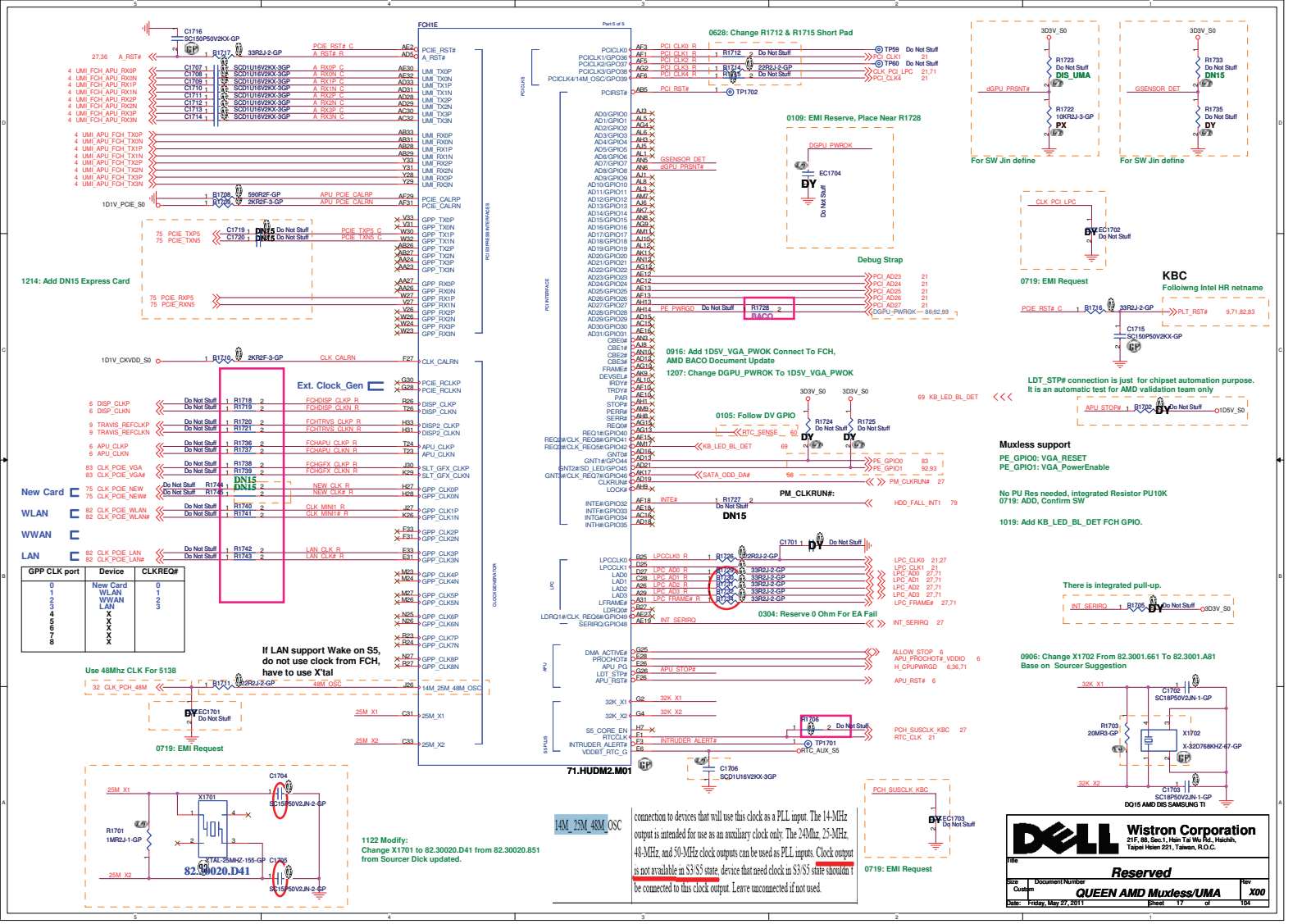

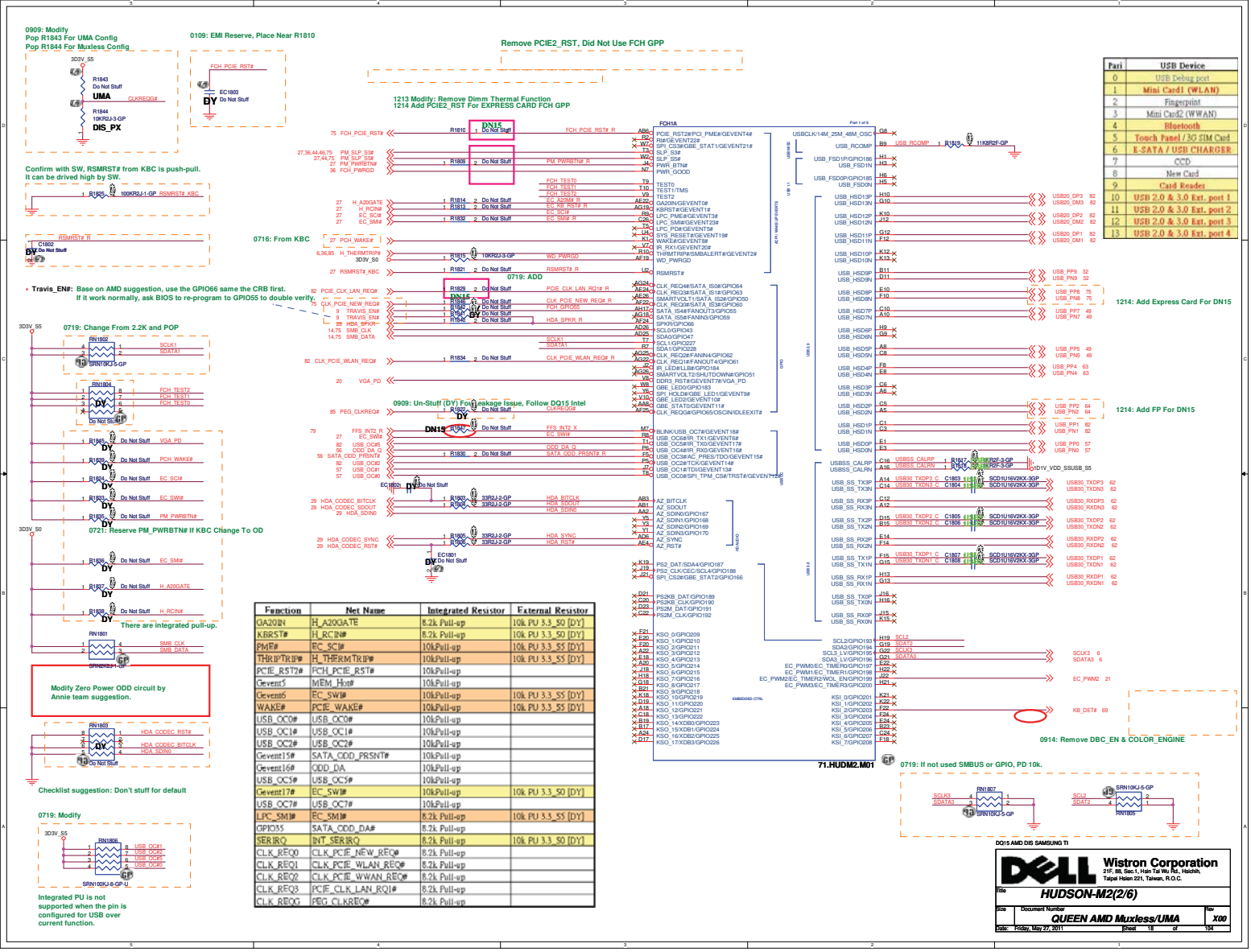

Function	Net Name	Integrated Resistor	External Resistor
GA20IN	H_A20GATE	8.2k Pull-up	10k PU 3.3_S0 [DY]
KBRST#	H_RCIN#	8.2k Pull-up	10k PU 3.3_S0 [DY]
PME#	EC_SCI#	10kPull-up	10k PU 3.3_S5 [DY]
THRMTRIP#	H_THRMTRIP#	10kPull-up	10k PU 3.3_S5 [DY]
PCIE_RST7#	FCH_PCIE_RST#	10kPull-up	
Gevent5	MEM_Hot#	10kPull-up	
Gevent6	EC_SWI#	10kPull-up	10k PU 3.3_S5 [DY]
WAKE#	PCIE_WAKE#	10kPull-up	10k PU 3.3_S5 [DY]
USB_OC0#	USB_OC0#	10kPull-up	
USB_OC1#	USB_OC1#	10kPull-up	
USB_OC2#	USB_OC2#	10kPull-up	
Gevent15#	SATA_ODD_PRSNT#	10kPull-up	
Gevent16#	ODD_DA	10kPull-up	
USB_OC5#	USB_OC5#	10kPull-up	
Gevent17#	EC_SWI#	10kPull-up	10k PU 3.3_S0 [DY]
USB_OC7#	USB_OC7#	10kPull-up	
LPC_SMI#	EC_SMI#	8.2k Pull-up	10k PU 3.3_S5 [DY]
GPIO35	SATA_ODD_DA#	8.2k Pull-up	
SERIRQ	INT_SERIRQ	8.2k Pull-up	10k PU 3.3_S0 [DY]
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2k Pull-up	
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2k Pull-up	
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2k Pull-up	
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2k Pull-up	
CLK_REQ5	PEG_CLKREQ#	8.2k Pull-up	

Pari	USB Device
0	USB Debug port
1	Mini Card1 (WLAN)
2	Fingerprint
3	Mini Card2 (WWAN)
4	Bluetooth
5	Touch Panel / 3G SIM Card
6	E-SATA / USB CHARGER
7	CCD
8	New Card
9	Card Reader
10	USB 2.0 & 3.0 Ext. port 1
11	USB 2.0 & 3.0 Ext. port 2
12	USB 2.0 & 3.0 Ext. port 3
13	USB 2.0 & 3.0 Ext. port 4

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Title: HUDSON-M2(2/6)
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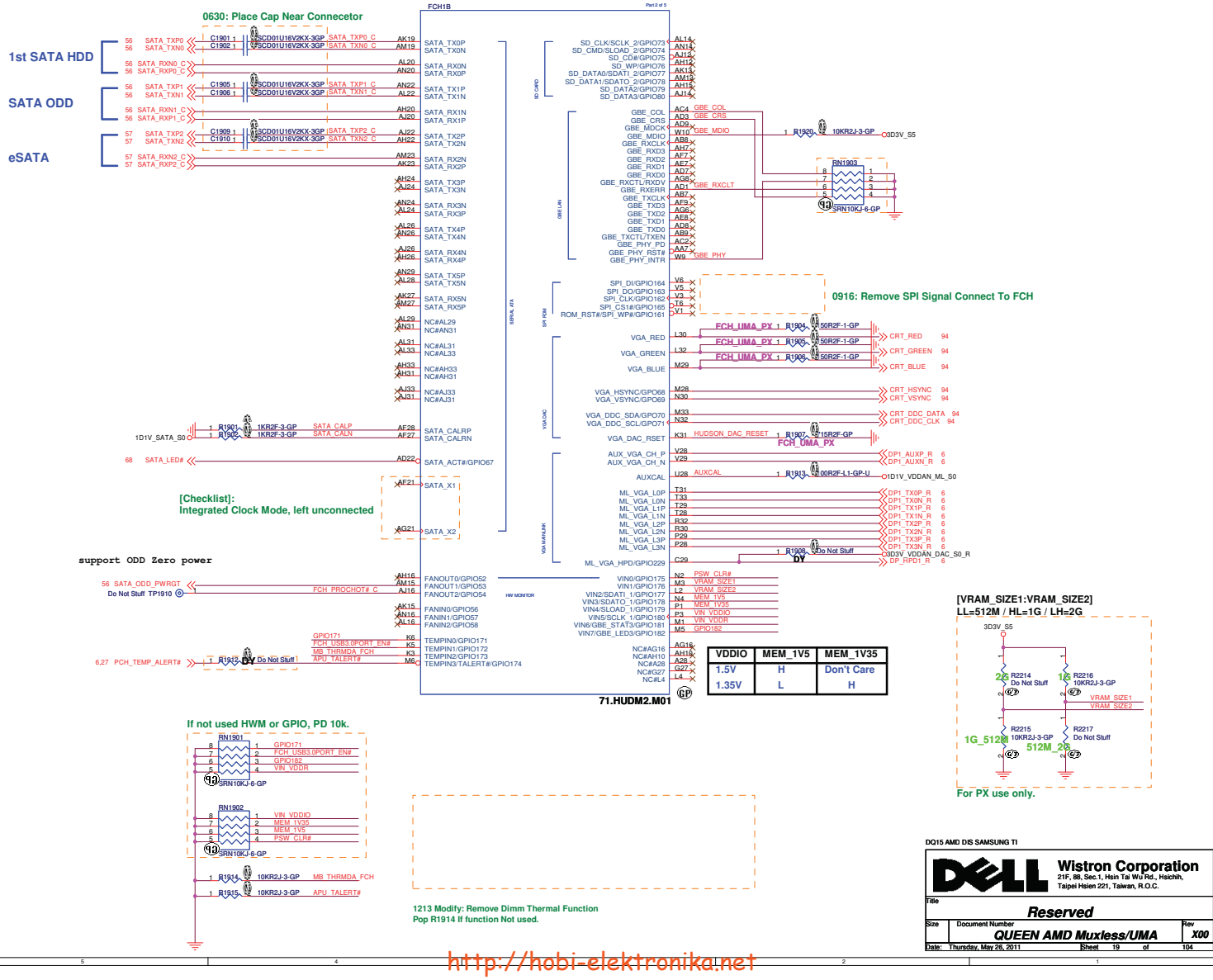

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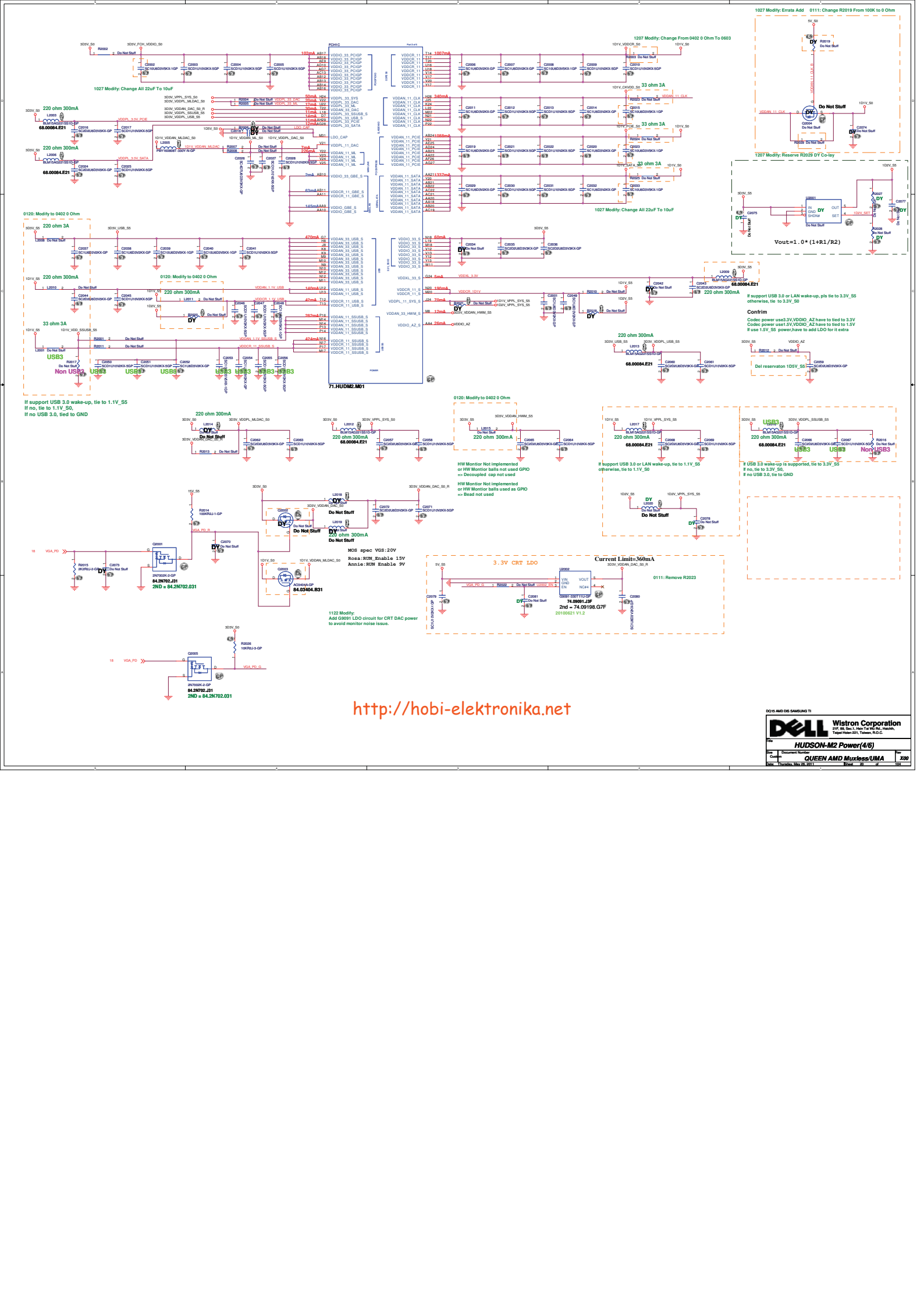
1027 Modify: Errata Add 0111: Change R2019 From 100K to 0 Ohm
1207 Modify: Change From 0402 0 Ohm To 0603
1027 Modify: Change All 22uF To 10uF
1027 Modify: Change All 22uF To 10uF
1207 Modify: Reserve R2029 DY Co-lay
0120: Modify to 0402 0 Ohm
0120: Modify to 0402 0 Ohm
0120: Modify to 0402 0 Ohm
0120: Modify to 0402 0 Ohm
Vout=1.0*(1+R1/R2)
If support USB 3.0 or LAN wake-up, pls tie to 3.3V_S5 otherwise, tie to 3.3V_S0
Confirm
Codec power use3.3V,VDDIO_AZ have to tied to 3.3V
Codec power use1.5V,VDDIO_AZ have to tied to 1.5V
If use 1.5V_S5 power,have to add LDO for it extra
If support USB 3.0 wake-up, tie to 1.1V_S5
If no, tie to 1.1V_S0,
If no USB 3.0, tied to GND
If support USB 3.0 or LAN wake-up, tie to 1.1V_S5 otherwise, tie to 1.1V_S0
If USB 3.0 wake-up is supported, tie to 3.3V_S5
If no, tie to 3.3V_S0,
If no USB 3.0, tie to GND
HW Montior Not implemented or HW Montior balls not used GPIO => Decoupled cap not used
HW Montior Not implemented or HW Montior balls used as GPIO => Bead not used
MOS spec VGS:20V
Rosa:RUN_Enable 15V
Annie:RUN Enable 9V
1122 Modify: Add G9091 LDO circuit for CRT DAC power to avoid monitor noise issue.
3.3V CRT LDO
Current Limit=360mA
0111: Remove R2023
Del reservaton 1D5V_S5
71.HUDM2.M01
84.2N702.J31
2ND = 84.2N702.031
84.03404.B31
68.00084.E21
74.09091.J3F
2nd = 74.09198.G7F
http://hobi-elektronika.net
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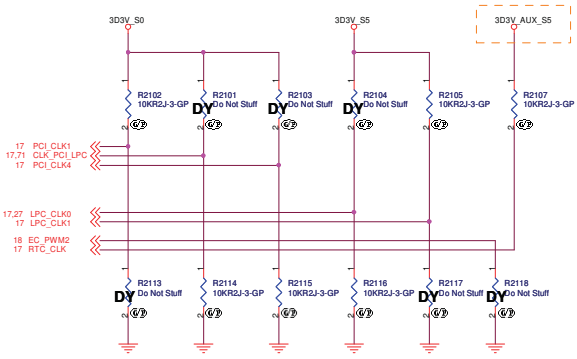
HUDSON-M2 Power(4/6)
QUEEN AMD Muxless/UMA
X00
Thursday, May 26, 2011

SSID = S.B

REQUIRED STRAPS

CRB: PU to 3.3V_AUX_S5
Checklist: PU to 3.3V_S5
Confirm with AMD, follow CRB suggestion



REQUIRED SYSTEM STRAPS

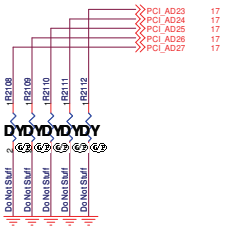
Use this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

No Fusion Config, Strap Not needed, but reserve

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

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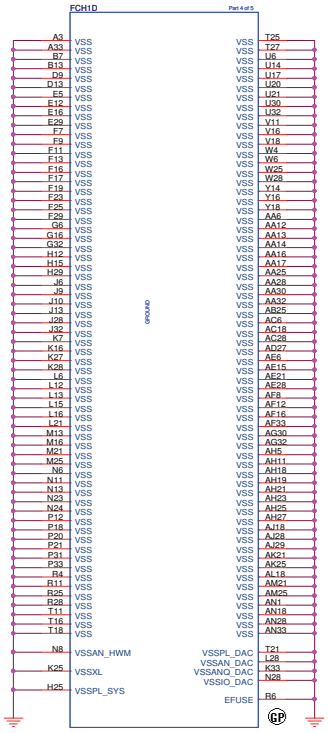

71.HUDM2.M01

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SSID = KBC

0107: Change R2724 & R2726 from 5 % To 1 & Resistor tolerance.

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

0107: POP C2718, R2739, Change To Voltage Divider
** BOM Control For R2710 Value.
Default R2710 10K = DQ15_UMA

0702 Modify:
Default un-stuff R2736(internal PL in KBC)

0107: Update Model_ID_DET
Table,
DQ15_AMD_UMA
DQ15_AMD_DIS (PX)
DN15_AMD_DIS (PX)

MODEL_ID_DET(GPIO97)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DQ15_ATI	100.0K	20.0K(64.20025.6DL)	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K(64.47025.6DL)	2.24V
DN15_ATI	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

0628 Modify:
Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.

0716: Vendor Suggestion

0107: Modify:
Remove EAIE/A_PWR_EN#1b GPIO2
Add GPO94 To USB_IO_CRT_EN#

0702 Modify:
Rename EC_GPIO6 to PSL_IN2

0629 Modify:
Rename TP_LOCK_LED#/BATT_WHITE_LED#

Rename PM_SLP_S4# To PM_SLP_S5#

0702 Modify:
Rename EC_GPIO70 to PSL_IN1
Rename EC_GPIO71 to PSL_OUT

0604 Modify:
RN2704 pull-5 use 10K Resistor to DY on BLUETOOTH_EN.

0706 Modify:
KBC GPIO47 change to MKP_PWRGD.
KBC GPO07 change to MKP_PWRGD.

0109: EMI Reserve, Place Near R2768

0719 Modify:
Reserved 0.1uF on all of ADC input pins base on NUVOTON feedback list.(C2717~C2721)

0702 Modify:
Rename EC_GPIO6 to PSL_IN2

0714 Modify:
Un-stuff D2701,D2704 and Add R2758,R2759 ohm confirm with NUVOTON and SW.

0928 Modify:
Add Q2706 2N7002 to avoid leakage loop from 3D3V_S5 to 3D3V_AUX_KBC issue when 10mW latched fail timing.

0109: Follow Intel, Need Confirm DQ/DN Spec

1122 Modify:
Change To X5R Cap

Layout Note:
Locate resistors R2719 and R2722 close to the KBC.

0106 Modify:
Update U2701A, U2701B Symbol

Layout Note:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

EC_GPIO47 High Active

0621 Modify:
Removed R2723

1027 Modify:
Change R2075 PU From 3D3V_AUX_S5 to 3D3V_AUX_KBC

0716: Modify
0111: Pop D2705, DY R2760

PSL Solution

10mW Solution

EC GPIO standard PH/PL

0109: EMI Reserve, Place Near R2768

0719: EMI Reserve, Place Near R2768

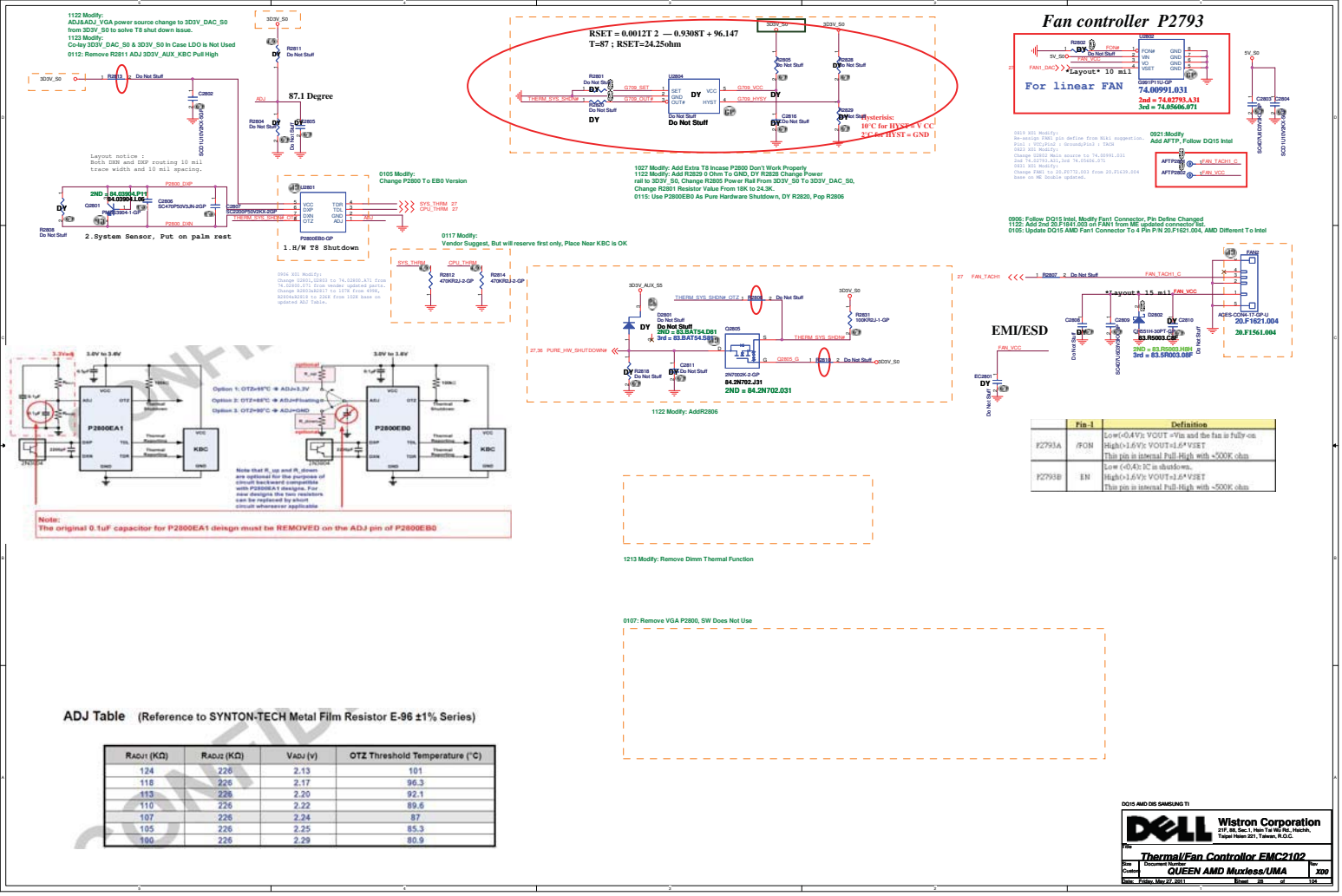
DQ15 AMD DIS SAMSUNG T1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 37 of 104



	Pin 1	Definition
F2793A	/FON	Low (<0.4V): VOUT =Vin and the fan is fully-on High (>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
F2793B	EN	Low (<0.4): IC in shutdown. High (>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: Thermal/Fan Controllor EMC2102

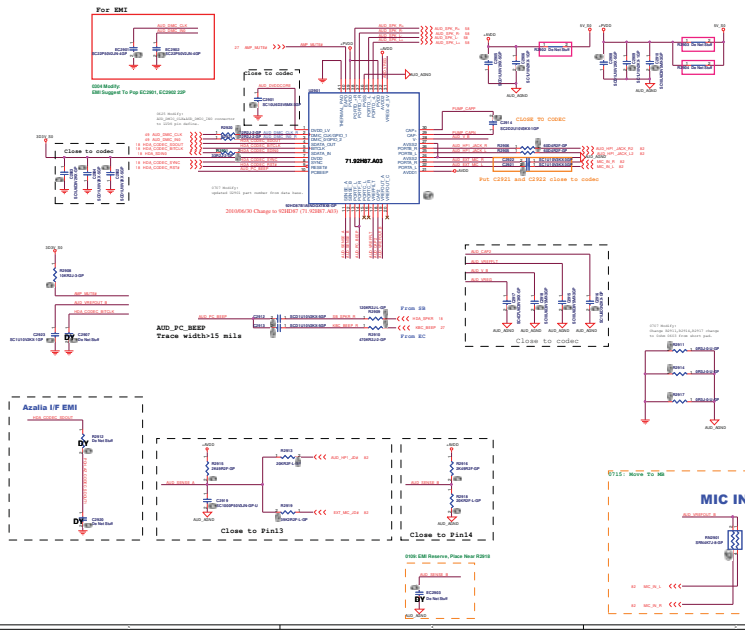
Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Friday, May 27, 2011 | Sheet 29 of 104

SSID = AUDIO

ANNIE Audio solution

Remove Annie Audio



Audio Codec 92HD79B1

CUCEN AMD Mullins/IMA

AUDIO OP AMPLIFIER

DQ15 AMD DIS SAMSUNG TI

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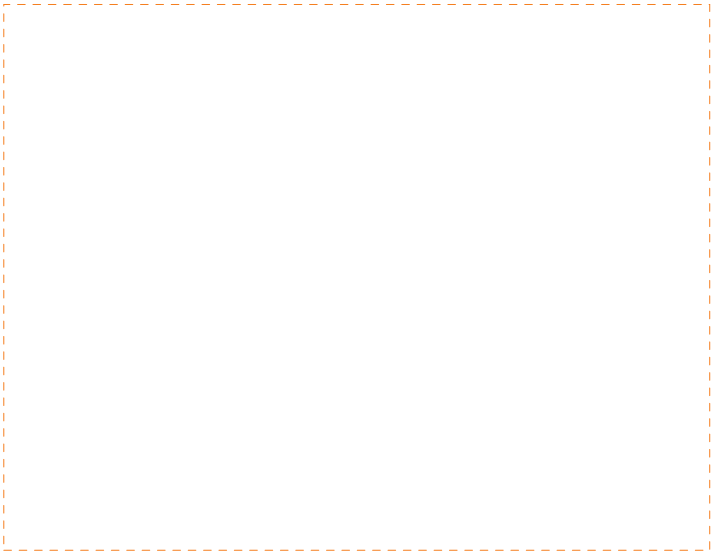
Taipei Hsien 221, Taiwan, R.O.C.

Title: AMP

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 30 of 104

DG15 M12 In Daughter BD



DQ15 AMD DIS SAMSUNG TI

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Taipei Hsien 221, Taiwan, R.O.C.

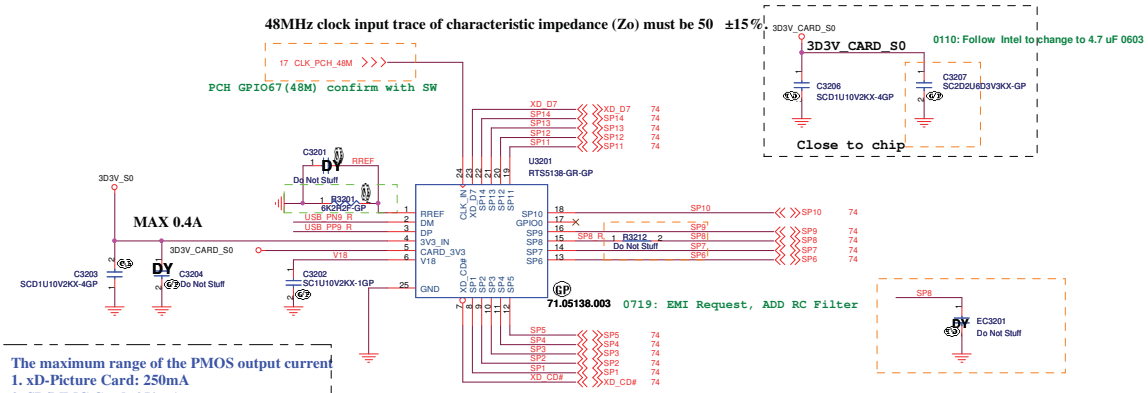
Title: LOM

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 31 of 104

SSID = SDIO

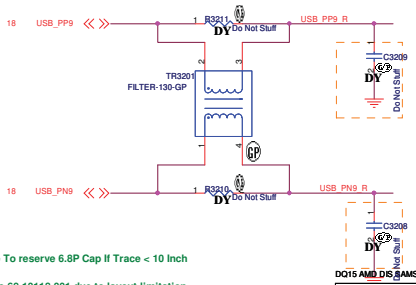
48MHz clock input trace of characteristic impedance (Zo) must be 50 ±15%.



The maximum range of the PMOS output current
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Zdiff) is 90Ω± 10%

POWER TRACE
1.RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2.RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7.It is recommended that use of ferrites bead on power trace.
8.Via size: Pad>=32 mils, Finished hole>=16 mils.



0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch
0118 Modify:
Change TR3201 To 69.10118.001 due to layout limitation

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: 1.00

Date: Friday, May 27, 2011 | Sheet 32 of 104

DO15 AMD DIS SAMSUNG TI

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Title: Reserved

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	1.00

Date: Thursday, May 26, 2011 Sheet 33 of 104

DQ15 AMD DIS SAMSUNG TI

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Title

Reserved

Size	Document Number	Rev
A3	***QUEEN AMD Muxless/UMA***	***1A00***

Date: Thursday, May 26, 2011 Sheet 34 of 104

DQ15 AMD DIS SAMSUNG TI

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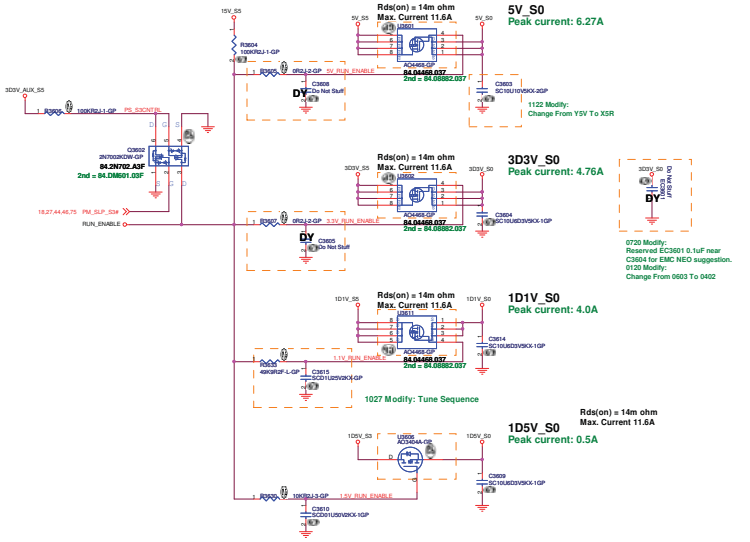
Title: Reserved

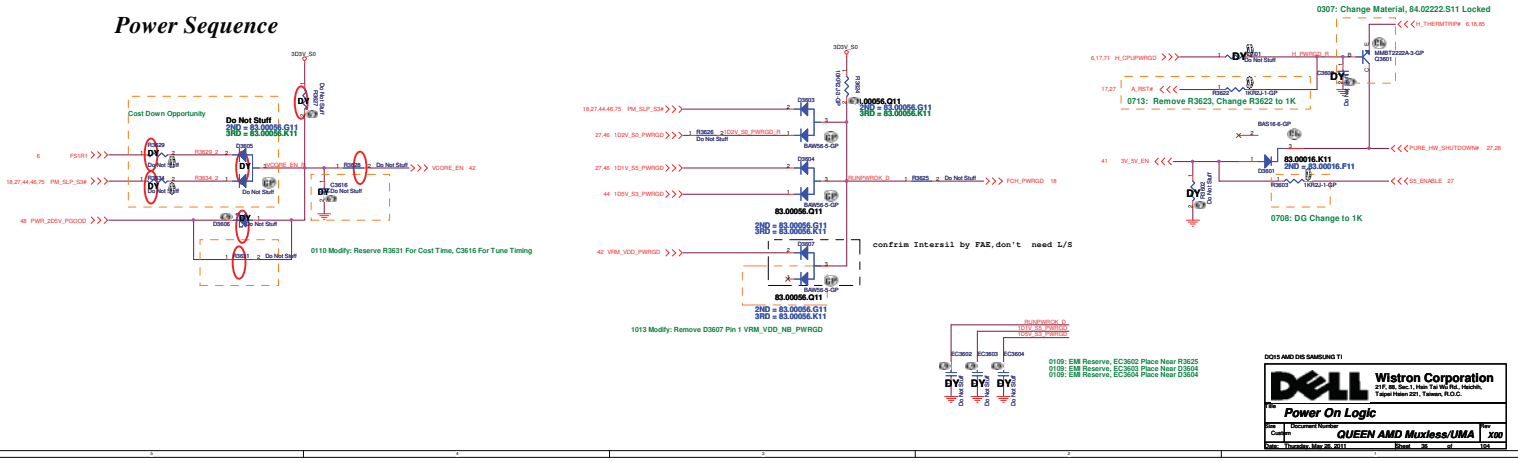
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 35 of 104

ROSA Run Power



Power Sequence



DDR3 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 36 of 104

DQ15 AMD DIS SAMSUNG TI

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Title

Power Plane Enable

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

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Move To CRT BD

DQ15 AMD DIS SAMSUNG TI

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Title: DCIN_JACK

Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	1.00

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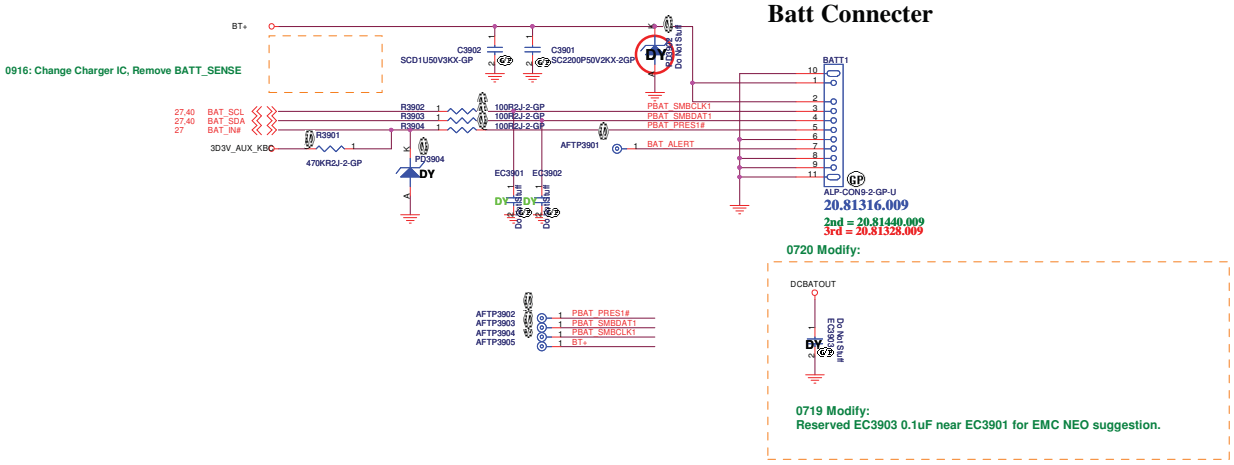
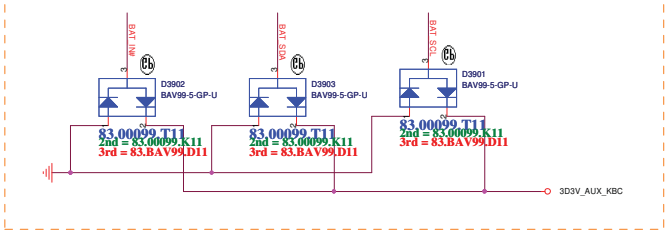
SSID = BATT CONN

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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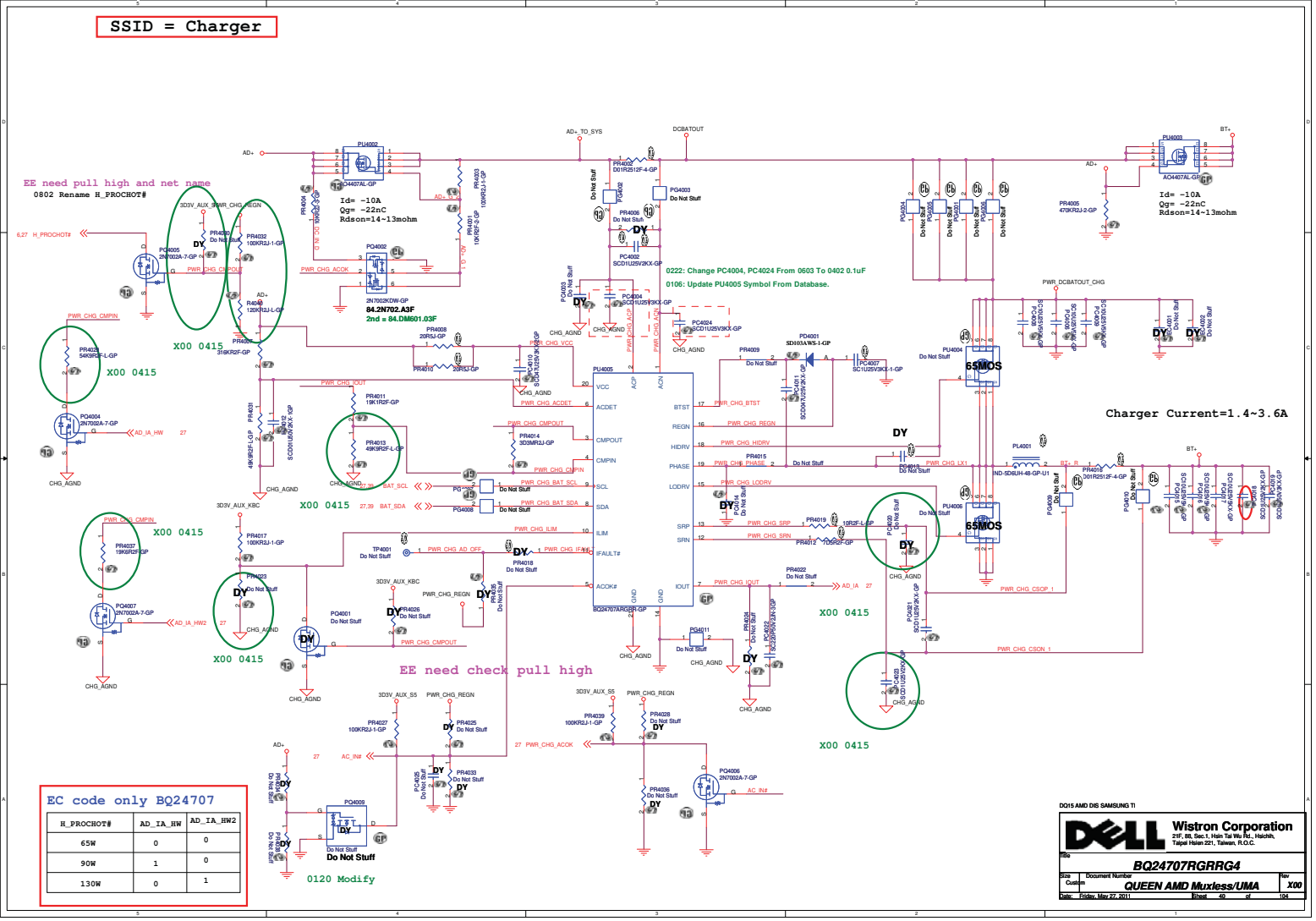
Taipei Hsien 221, Taiwan, R.O.C.

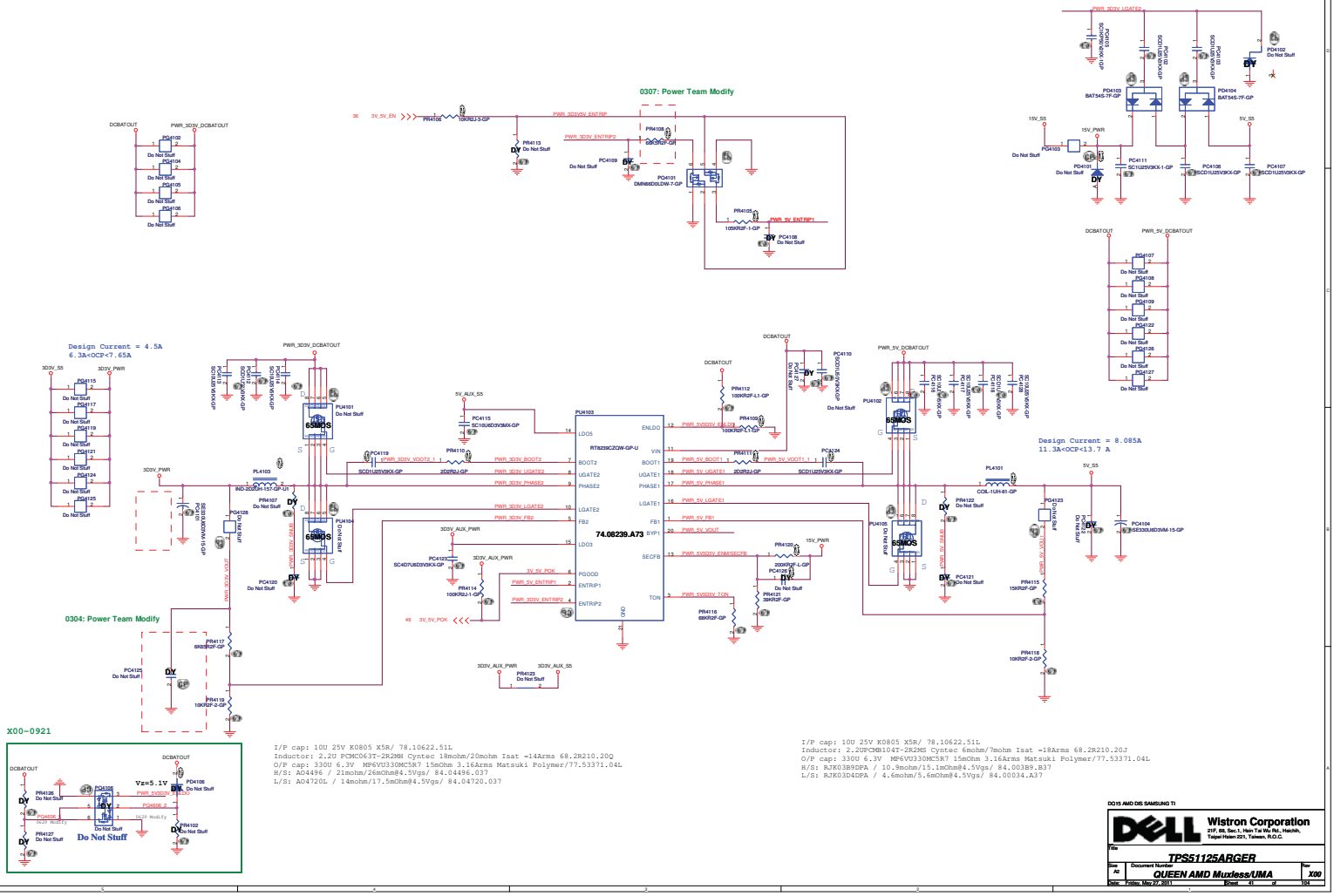
Title: BATT CONN

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 39 of 104



SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20Q
O/P cap: 330U 6.3V MP6VU330M5R7 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
H/S: AO4496 / 21mohm/26mOhm@4.5Vgs/ 84.04496.037
L/S: AO4720L / 14mohm/17.5mOhm@4.5Vgs/ 84.04720.037

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2UPCMB104T-2R2MS Cyntec 6mohm/7mohm Isat =18Arms 68.2R210.20J
O/P cap: 330U 6.3V MP6VU330M5R7 15mOhm 3.16Arms Matsuki Polymer/77.53371.04L
H/S: RJK03B9DPA / 10.9mohm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA / 4.6mohm/5.6mOhm@4.5Vgs/ 84.00034.A37

DCIS AMD DIS SAMSUNG TI

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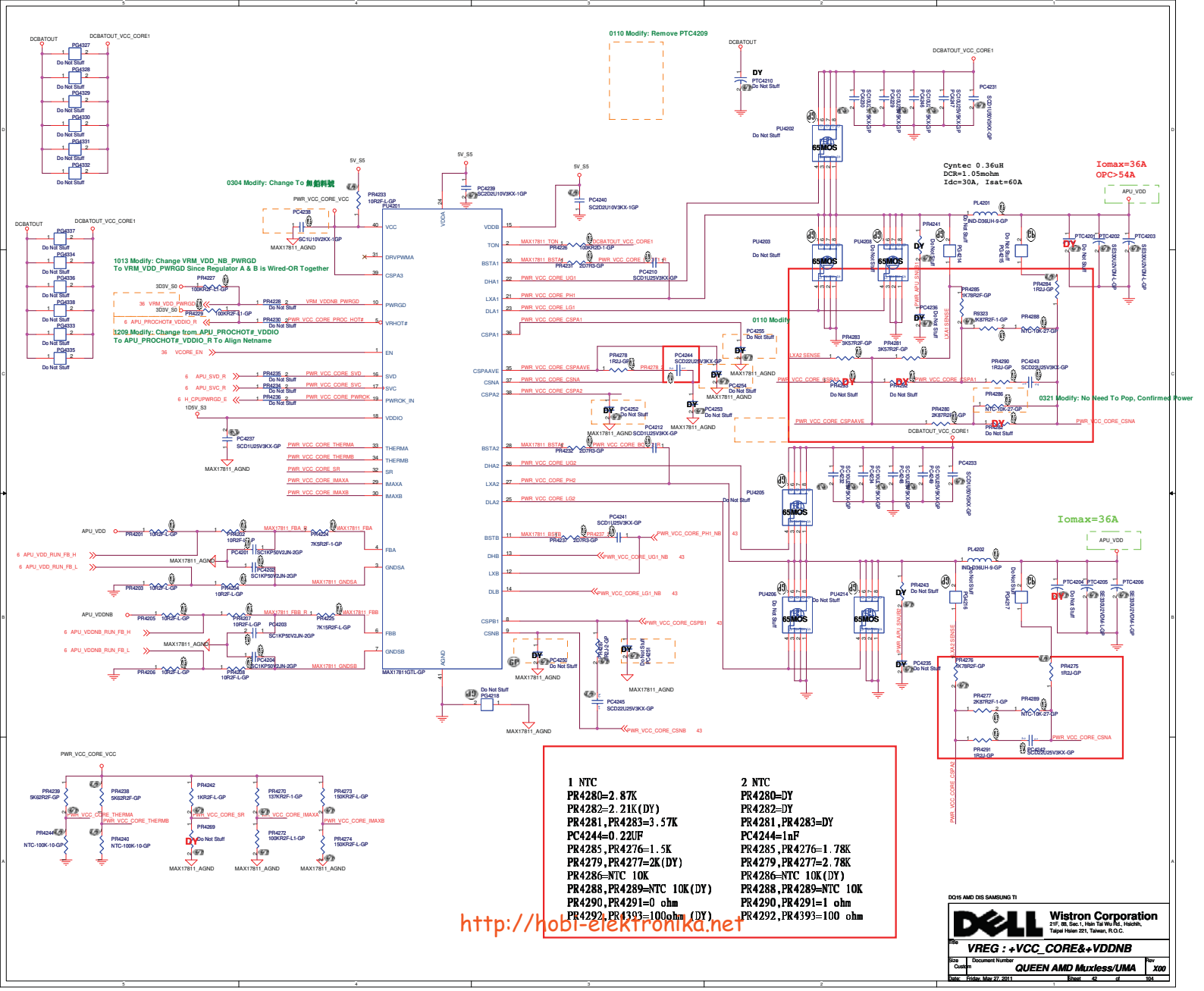
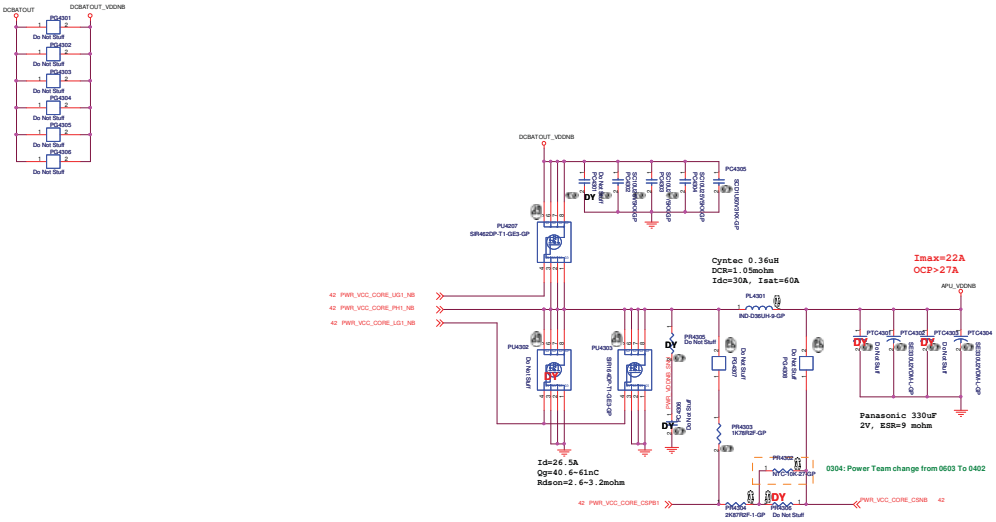
File: TPS51125ARGER

Size	Document Number	Rev
A0	QUEEN AMD Mudless/UMA	X00
Date: Friday, May 27, 2011	Sheet 41 of 104	





DC15 AMD DIS SAMSUNG TI

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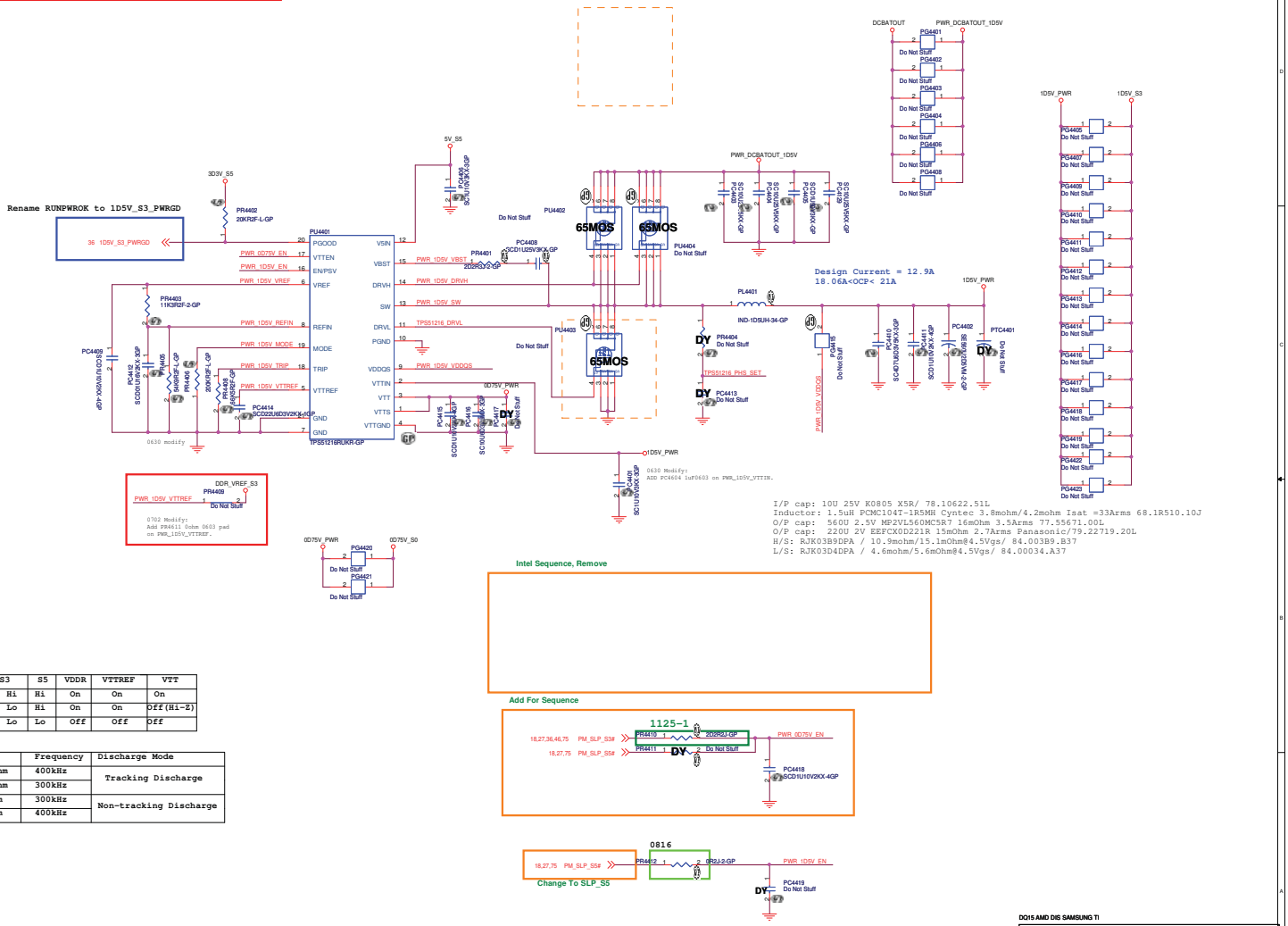
Taipei Hsien 221, Taiwan, R.O.C.

File: VDDNB

Size	Document Number	Rev
A0	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 43 of 104

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4406	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216 1D5V S3

Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Friday, May 27, 2011 Sheet 44 of 104

DC1S AMD DIS SAMSUNG TI

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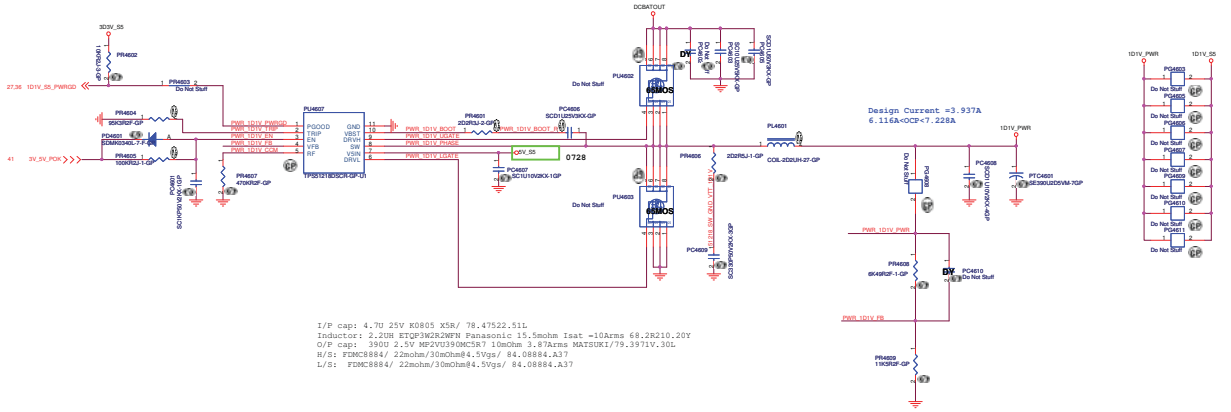
File: VDDR & VDDP

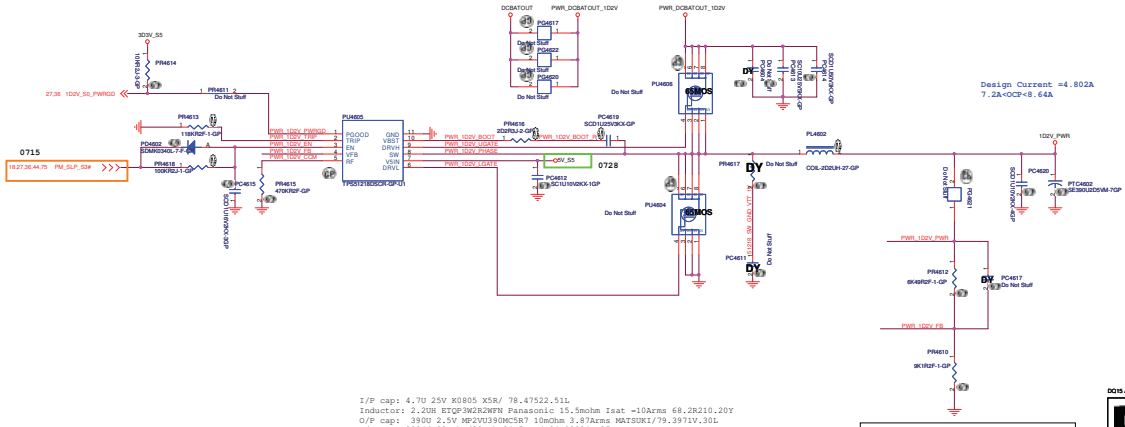
Size: A0 | Document Number: | Rev: QUEEN AMD Muxless/UMA X00

Date: Thursday, May 26, 2011 | Sheet 45 of 53

SSID = PWR.Plane.Regulator_1D1V_S5



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2UH ETQP3W2R2WFN Panasonic 15.5mohm Isat =10Arms 68.2R210.20Y
O/P cap: 390U 2.5V MP2VU390MC5R7 10mOhm 3.87Arms MATSUKI/79.3971V.30L
H/S: FDMC8884/ 22mohm/30mOhm@4.5Vgs/ 84.08884.A37
L/S: FDMC8884/ 22mohm/30mOhm@4.5Vgs/ 84.08884.A37



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2UH ETQP3W2R2WFN Panasonic 15.5mohm Isat =10Arms 68.2R210.20Y
O/P cap: 390U 2.5V MP2VU390MC5R7 10mOhm 3.87Arms MATSUKI/79.3971V.30L
H/S: FDMC8884/ 22mohm/30mOhm@4.5Vgs/ 84.08884.A37
L/S: FDMC8884/ 22mohm/30mOhm@4.5Vgs/ 84.08884.A37

DC1S AMD DIS SAMSUNG TI

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File: VDDR & VDDP

Size	Document Number	Rev
A6	QUEEN AMD Muxless/UMA X09	

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DQ15 AMD DIS SAMSUNG TI

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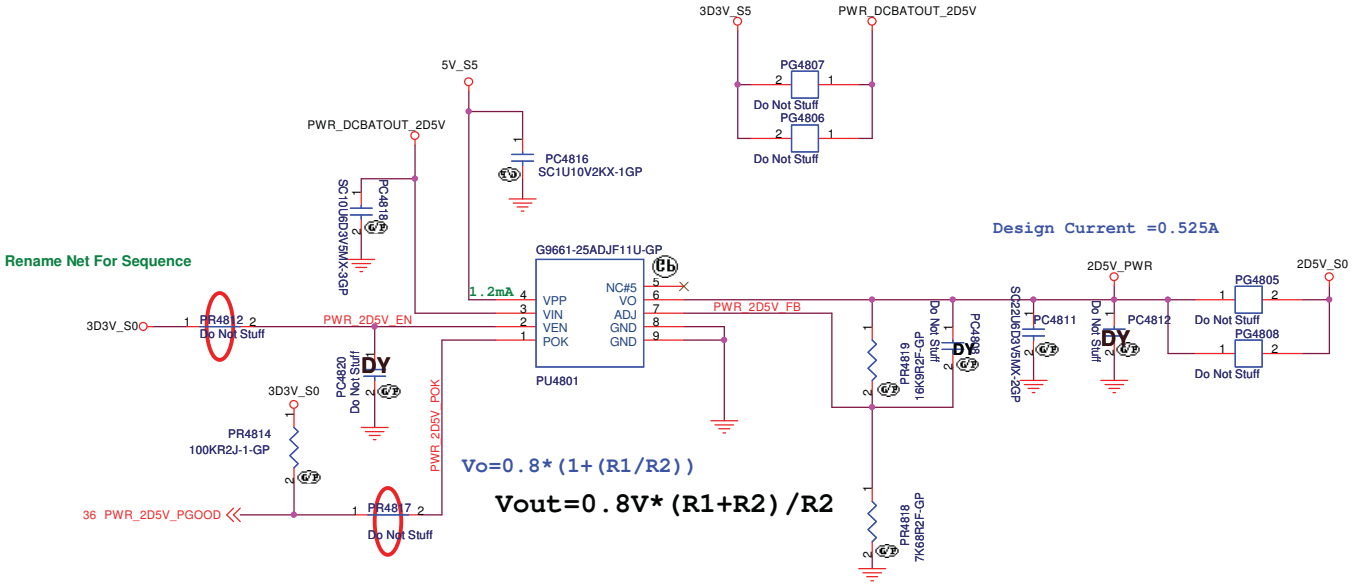
Title: Reserved

Size	Document Number	Rev
A2	QUEEN AMD Muxless/UMA	AX00

Date: Thursday, May 26, 2011 Sheet 47 of 104

SSID = PWR.Plane.Regulator_2p5v VGA 1V

G9661 for 2D5V_S0



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	2D5V_S0	
Size A4	Document Number QUEEN AMD Muxless/UMA	Rev X00
Date: Thursday, May 26, 2011	Sheet 48 of 104	

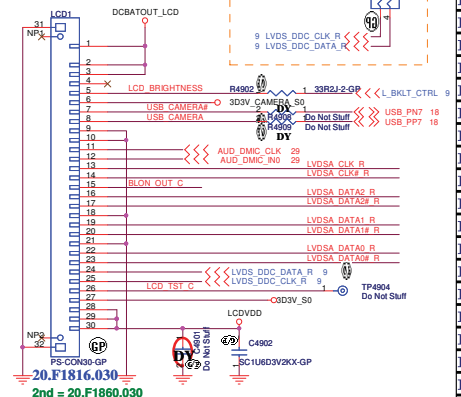
SSID = VIDEO

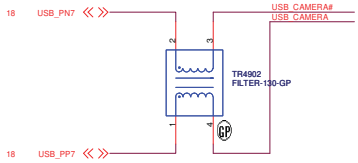
0909 X01 Modify:
Change LCD1 to 20.F1816.030 for 30pin
Re-assign LCD1 pin define base on Roy updated cable pin define list.

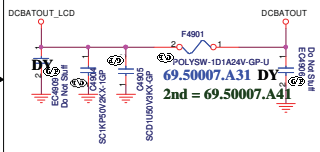
0921Modify:
Change BLON_OUT_C to pin 15 and pin 4 to NC on LCD1.

0914 Modify:
Change PU From Page 82 To Page 49

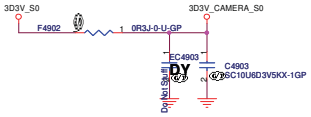
LVDS CONNECTOR





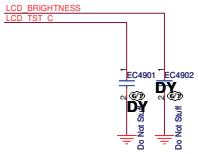


Camera Power



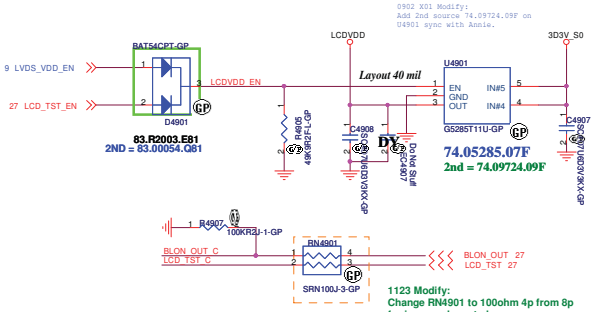
(MB Pin Define)	
MB CONN. (WIRE)	
Pin 1	DCBATOUT_LCD
Pin 2	DCBATOUT_LCD
Pin 3	DCBATOUT_LCD
Pin 4	BLON_OUT_C
Pin 5	LCD_BRIGHTNESS
Pin 6	3D3V_CAMERA_S0
Pin 7	USB_CAMERA#
Pin 8	USB_CAMERA
Pin 9	GND
Pin 10	GND
Pin 11	AUD_DMIC_CLK
Pin 12	AUD_DMIC_IN0
Pin 13	LVDSA_CLK
Pin 14	LVDSA_CLK#
Pin 15	LCD_DET_G
Pin 16	LVDSA_DATA2
Pin 17	LVDSA_DATA2#
Pin 18	GND
Pin 19	LVDSA_DATA1
Pin 20	LVDSA_DATA1#
Pin 21	GND
Pin 22	LVDSA_DATA0
Pin 23	LVDSA_DATA0#
Pin 24	LVDS_DDC_DATA_R
Pin 25	LVDS_DDC_CLK_R
Pin 26	LCD_TST_C
Pin 27	3D3V_S0
Pin 28	LCDVDD
Pin 29	LCDVDD
Pin 30	LCDVDD

For EMI request
Close to LVDS connector



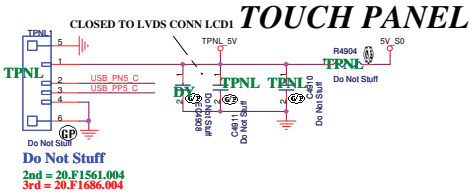
SSID = VIDEO

LCD POWER for ROSA



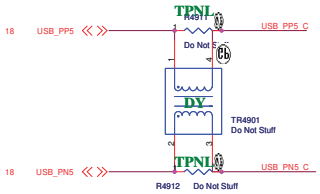
1123 Modify:
Change RN4901 to 100ohm 4p from 8p for improve layout place.

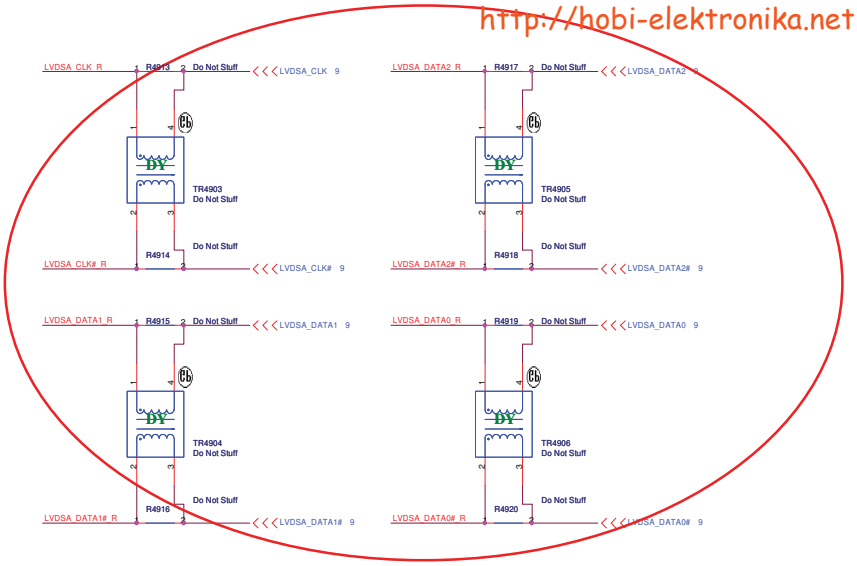
TOUCH PANEL



0909 Modify:
Add TPNL1 for touch panel solution 4pin connector.

0928 Modify:
Change To 20.F1621.004 on TPNL1 from updated connector list.





DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Thursday, April 21, 2011 Sheet 49 of 104

Remove For M12 Spec & Put In Daughter BD

Remove For M12 Spec & Put In Daughter BD

Remove For M12 Spec & Put In Daughter BD

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Board Connector

Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 50 of 104

HDMI Level Shifter & CONNECTOR

0913: Modify
Change HDMI1 Part Number From 22.10296.311 To 22.10296.331

0719: Reserve For EMI

HDMI_CONN

0719: Modify Netname

HDMI1
SKT-HDMI20-S1GP-U1
22.10296.331

1104 Modify: Change To Power Net
5V_HDMI
0112 Modify: Combine with CRT Fuse and Diode with HDMI

0426 chaomin
For HDMI 1.4 Reserve

Close to HDMI Connector

0719: Remove RN Resistor

For HDMI 1.4 Reserve

Impedance:100 ohm

Place Near HDMI CONN

0719: Remove RN Resistor

1213 Modify: Checklist Suggestion To Change To 604 Ohm

confirm by NXP FAE
Do not need PU Res,
Reserve PU Res for debug furtur

0921:Modify
Add AFTP, Follow DQ15 Intel

Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.

DC IS AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A0 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 51 of 104

Remove EDP

LCD POWER CIRCUIT

Remove EDP

Rosa team

Remove EDP

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: eDP		
Size: Custom	Document Number: QUEEN AMD Muxless/UMA	Rev: 1.00
Date: Thursday, May 26, 2011	Sheet 52 of 104	

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A3	***QUEEN AMD Muxless/UMA***	***1A00***

Date: Thursday, May 26, 2011 Sheet 53 of 104

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

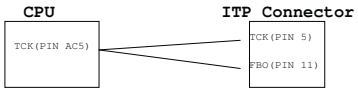
Size	Document Number	Rev
A3	*QUEEN AMD Muxless/UMA*	*X00*

Date: Thursday, May 26, 2011 Sheet 54 of 104

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

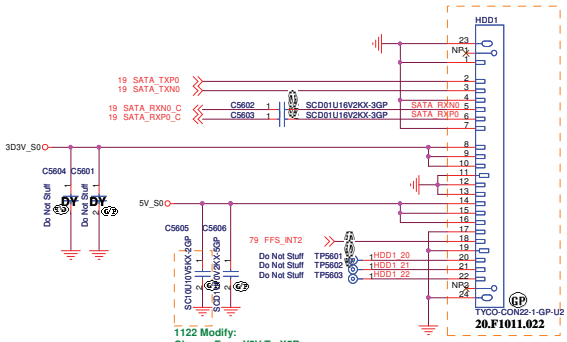
Title: ITP

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 55 of 104

SSID = SATA

SATA HDD Connector



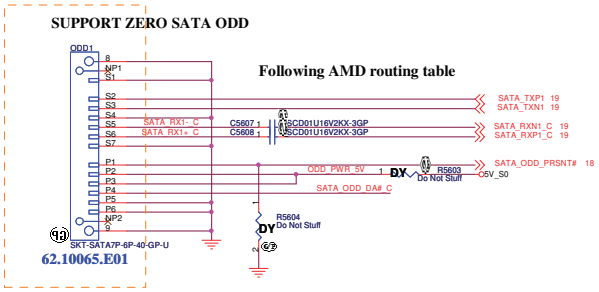
1122 Modify:
Change From Y5V To X5R

0614 Modify:
Change HDD1 connector part number to
20.F1011.022 base on ME EMN and DXF.

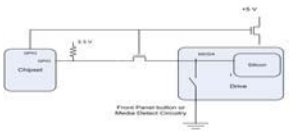
ODD Connector

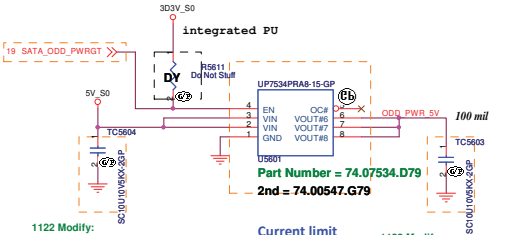
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



0914 Modify:
Change ODD Part number From 22.10300.421 To 62.10065.E01



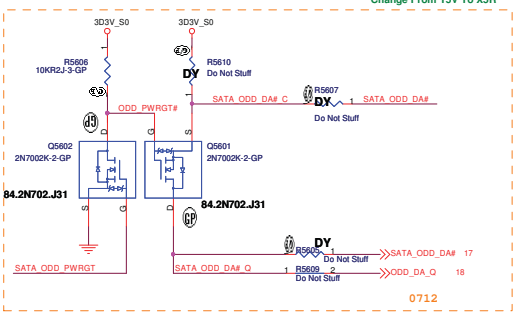


1122 Modify:
Change From Y5V To X5R

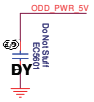
Current limit
Active High
typ =>2.5A

1122 Modify:
Change From Y5V To X5R

0719: Modify Zero ODD Circuit



0109: EMI Request.



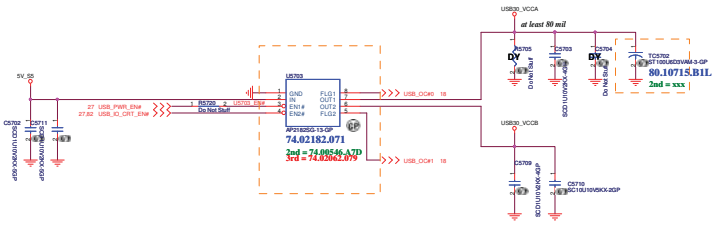
DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

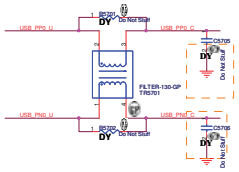
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

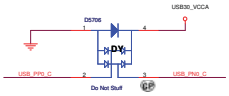
Date: Thursday, May 26, 2011 Sheet 56 of 104



0706: Sourcer Request To Change To GMT
0906: Add 0hm in USB_PWR_EN# and Remove CEN#/
Consult SW Use Which Enable.
0906: Change TC5702 Part Number,
Follow DQ15 Intel
0113: Change To Duel USB PWR Switch & Some Cap.

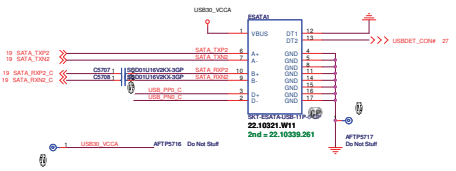
0101: Change ESATA1 To 22.10290.271





0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

Wait For 3.0 Esata COMBO With DETECT PIN



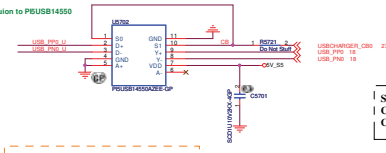
0706: Rename Netname

0101: Reserve Common Mode Choke & ESD Diode.

0112: Change To USB 2.0 ESD Diode X 2

USB CHARGER

0906: Modify:
Change US702 soltuion to PSUSB14550
from MAX14566



Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

D	Size	Title
C		
B		
A		Error comments to Vivi

0914: Remove Non Charger Co-lay Resistor.

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA/USB Charger

Size	Document Number	Rev
A2	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 28, 2015 Sheet 37 of 104

SSID = AUDIO

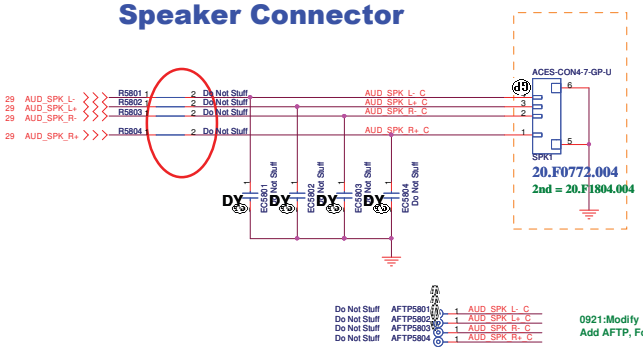
0715 Modify:
Change EC5801~EC5804 to 100p 0402
and default un-stuff.
Add R5801~R5804 between SPK signal and connector
for EMC NEO suggest.

0914 Modify:
Change SPK1 to 20.F0772.004 from
20.F1647.004 from Double updated.

0921 Modify:
Modify Pin Define Base On DQ15 Intel

1110 X02 Modify:
Add 2nd 20.F1804.004 on SPK1 from
ME updated connector list.

Speaker Connector



MB CONN. (WIRE)	
Pin 4	AUD_SPK_L-C
Pin 3	AUD_SPK_L+C
Pin 2	AUD_SPK_R-C
Pin 1	AUD_SPK_R+C

0921:Modify
Add AFTP, Follow DQ15 Intel

DQ15 AMD DIS SAMSUNG TI

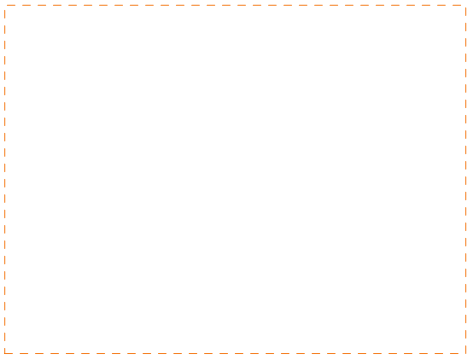
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 58 of 104

LAN CONN In Daugthter BD

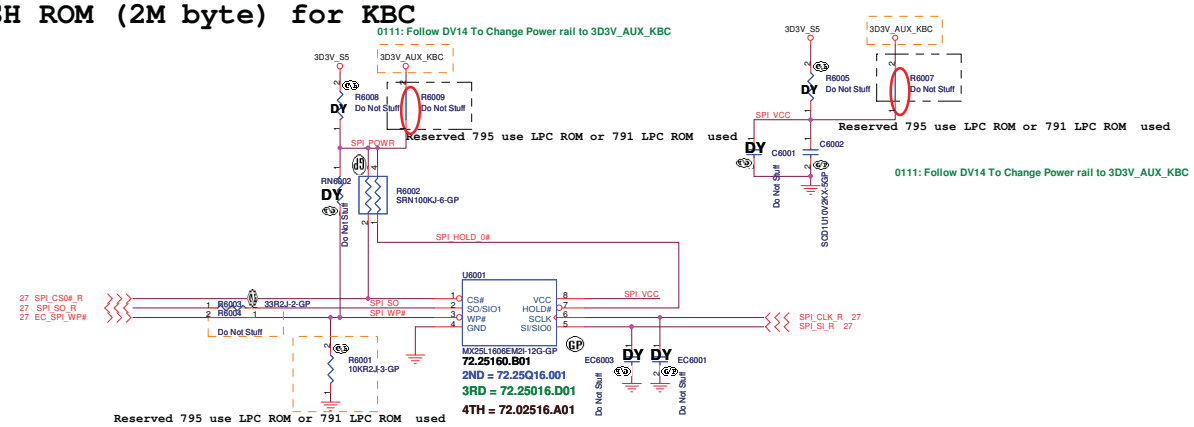


DQ15 AMD DIS SAMSUNG TI

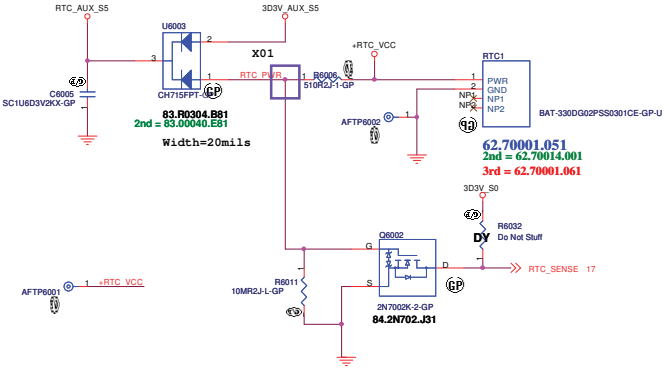
DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONN	
Size: A3	Document Number: QUEEN AMD Muxless/UMA	Rev: 1A00
Date: Thursday, May 26, 2011	Sheet 59 of 104	

SSID = Flash.ROM

SPI FLASH ROM (2M byte) for KBC



SSID = RBATT



0105 Modify:
updated RTC1 symbol and footprint from data base.
1122 Modify:
Add Q6002, R6010, R6011 for FACTORY RTC detect function.

0111: Change RTC Schematic As DV14 Brazo, SW Suggest.

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 60 of 104

SSID = USB

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

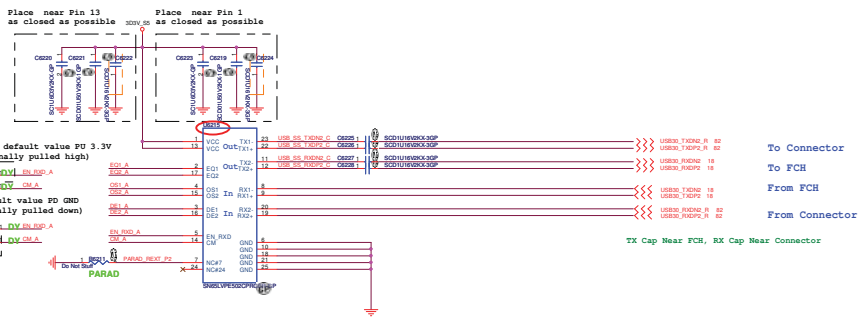
Title: USB Power SW

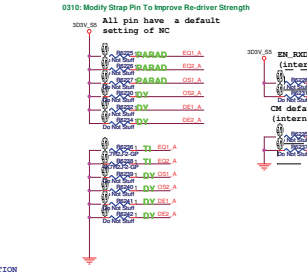
Size | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 61 of 104

1222 Modify:
C6222,C6224, C6231, C6234 Change Y5V To X7R

0916: Move From IO Board To Main Board



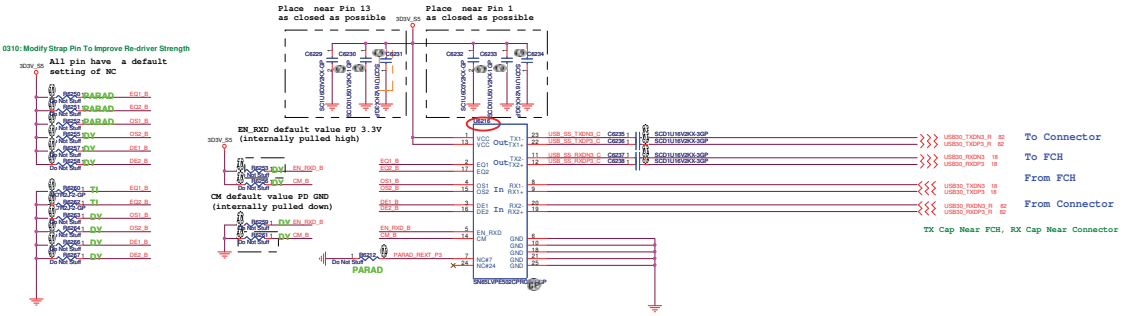


DUMMY NAME CONFIGURATION
TI = TI 502R Need Pop
PARAD_ALL = For Both PARAD I2C Mode & Normal MODE
PARAD_I2C = Parad I2C Mode
TI_PARAD= Both TI & PARAD Normal Mode

Pin5 EN_RX_A = Parade = DUMMY
Pin14 CM_A = Parade = Default DUMMY (PU)
Pin2 EQ1 = Parad B_EQ0 = Default DUMMY (PU)
Pin17 EQ2 = Parad A_EQ0 = Default DUMMY (PU)
Pin4 OS1 = Parad B_EQ1 = Default DUMMY (PU)
Pin15 OS2 = Parad A_EQ1 = Default DUMMY (PU)
Pin3 DE1 = Parad B_DE0 = Default Pull High
PIN16 DE2 = Parad A_DE0 = Default Pull High
GND6 = Parad B_DE1 = Default Pull High
GND18= Parad A_DE1 = Default Pull High

Parad I2C Mode:
PIN3 DE1 = Parad I2C_ADDR0 = Default DUMMY (PU)
PIN4 OS1 = Parad I2C_ADDR1 = Default DUMMY (PU)

Parad I2C Mode:
PIN15 OS2 = Parad I2C = SDA_CTL (DATA)
PIN16 DE = Parad I2C = SCL_CTL (CLK)



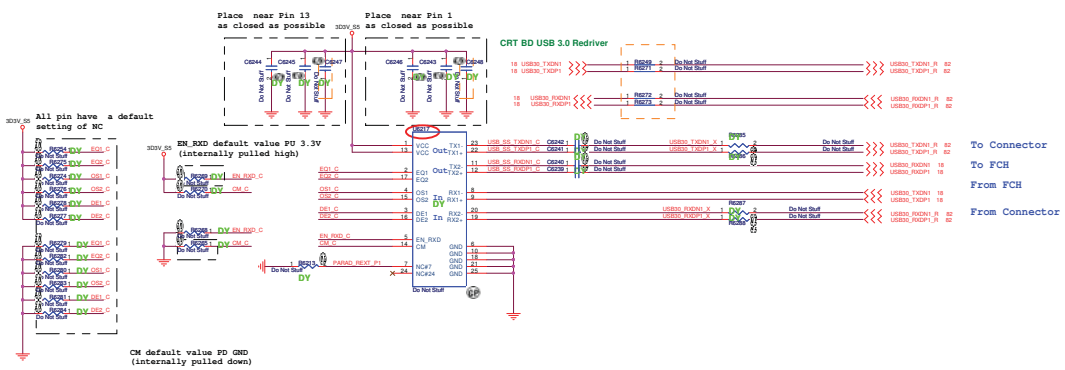
DUMMY NAME CONFIGURATION
TI = TI 502R Need Pop
PARAD_ALL = For Both PARAD I2C Mode & Normal MODE
PARAD_I2C = Parad I2C Mode
TI_PARAD= Both TI & PARAD Normal Mode

Pin5 EN_RX_A = Parade = DUMMY
Pin14 CM_A = Parade = Default DUMMY (PU)
Pin2 EQ1 = Parad B_EQ0 = Default DUMMY (PU)
Pin17 EQ2 = Parad A_EQ0 = Default DUMMY (PU)
Pin4 OS1 = Parad B_EQ1 = Default DUMMY (PU)
Pin15 OS2 = Parad A_EQ1 = Default DUMMY (PU)
Pin3 DE1 = Parad B_DE0 = Default Pull High
PIN16 DE2 = Parad A_DE0 = Default Pull High
GND6 = Parad B_DE1 = Default Pull High
GND18= Parad A_DE1 = Default Pull High

Parad I2C Mode:
PIN15 OS2 = Parad I2C = SDA_CTL (DATA)
PIN16 DE = Parad I2C = SCL_CTL (CLK)

Parad I2C Mode:
PIN3 DE1 = Parad I2C_ADDR0 = Default DUMMY (PU)
PIN4 OS1 = Parad I2C_ADDR1 = Default DUMMY (PU)

0113: CRT BD Redriver



Eng stuff 20.K0216.024 Pin1 -> left side
PD change to 20.K0276.024 Pin1 -> left side
so do not swap net

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

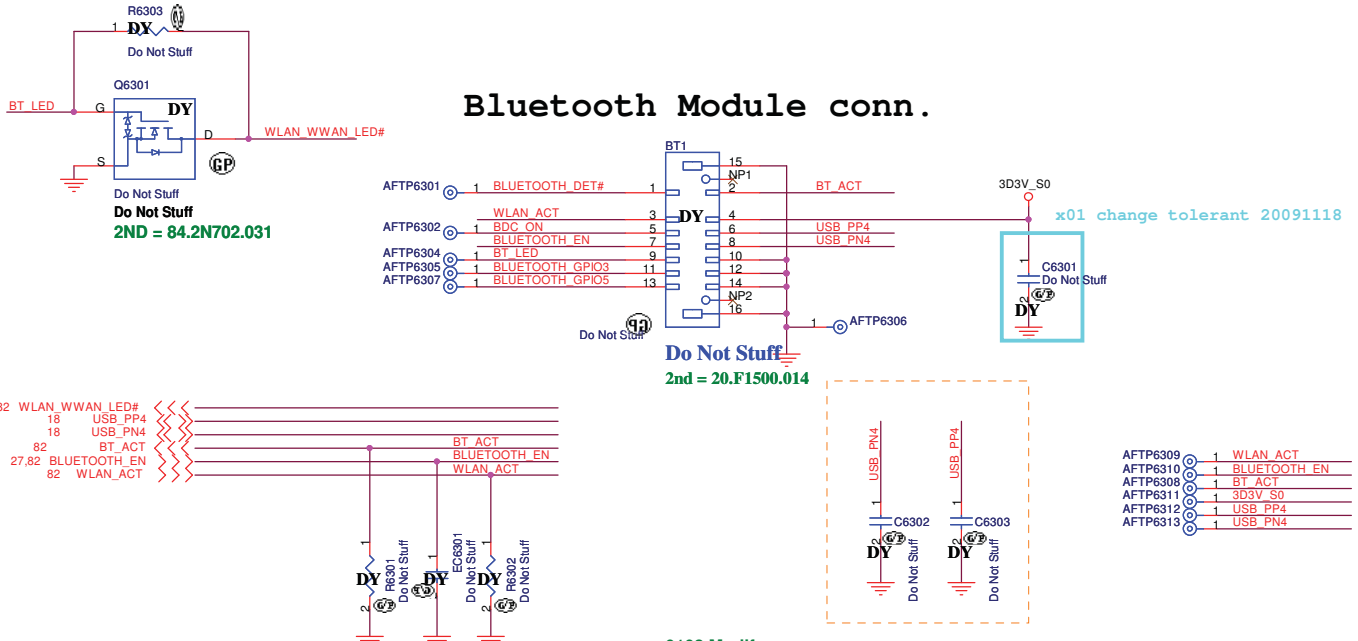
Title: USB 3.0

Size: C | Document Number: QUEEN AMD Muxless/UMA X00 | Rev: Custom

Date: Friday, May 27, 2011 | Sheet 42 of 104

SSID = User.Interface

Bluetooth Module conn.



0103 Modify:
AMD Spec Update To reserve 6.8P Cap If Trace < 10 Inch

0906 Modify:
Dell Peter already confirmed DQ15 and DN15 will not support Bluetooth BT365, only support combo Wirless+BT. Please DUMMY Bluetooth connector(BT1) and stand off (HBT1) and related components.

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

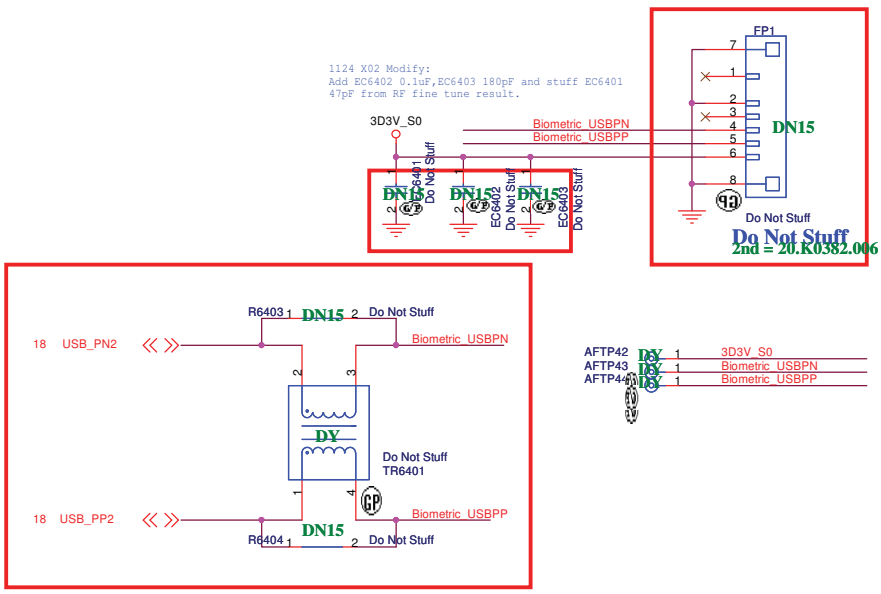
Title: Bluetooth

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 63 of 104

Finger Printer Connector

Finger Printer Connector



MB CONN.(FFC)	
Pin1	NC
Pin2	GND
Pin3	NC
Pin4	Biometric_USBPN
Pin5	Biometric_USBPP
Pin6	3D3V_S0

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: F/P

Size: A4 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 64 of 104

WLAN CONN In Daugthter BD

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	1.00

Date: Thursday, May 26, 2011 Sheet 65 of 104

Remove For DG12 M12 SPEC

DO15 AMD DIS SAMSUNG TI

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WWAN	
Size: A3	Document Number: QUEEN AMD Muxless/UMA	Rev: X00
Date: Thursday, May 26, 2011	Sheet 66 of 104	

(Blanking)

DQ15 AMD DIS SAMSUNG TI

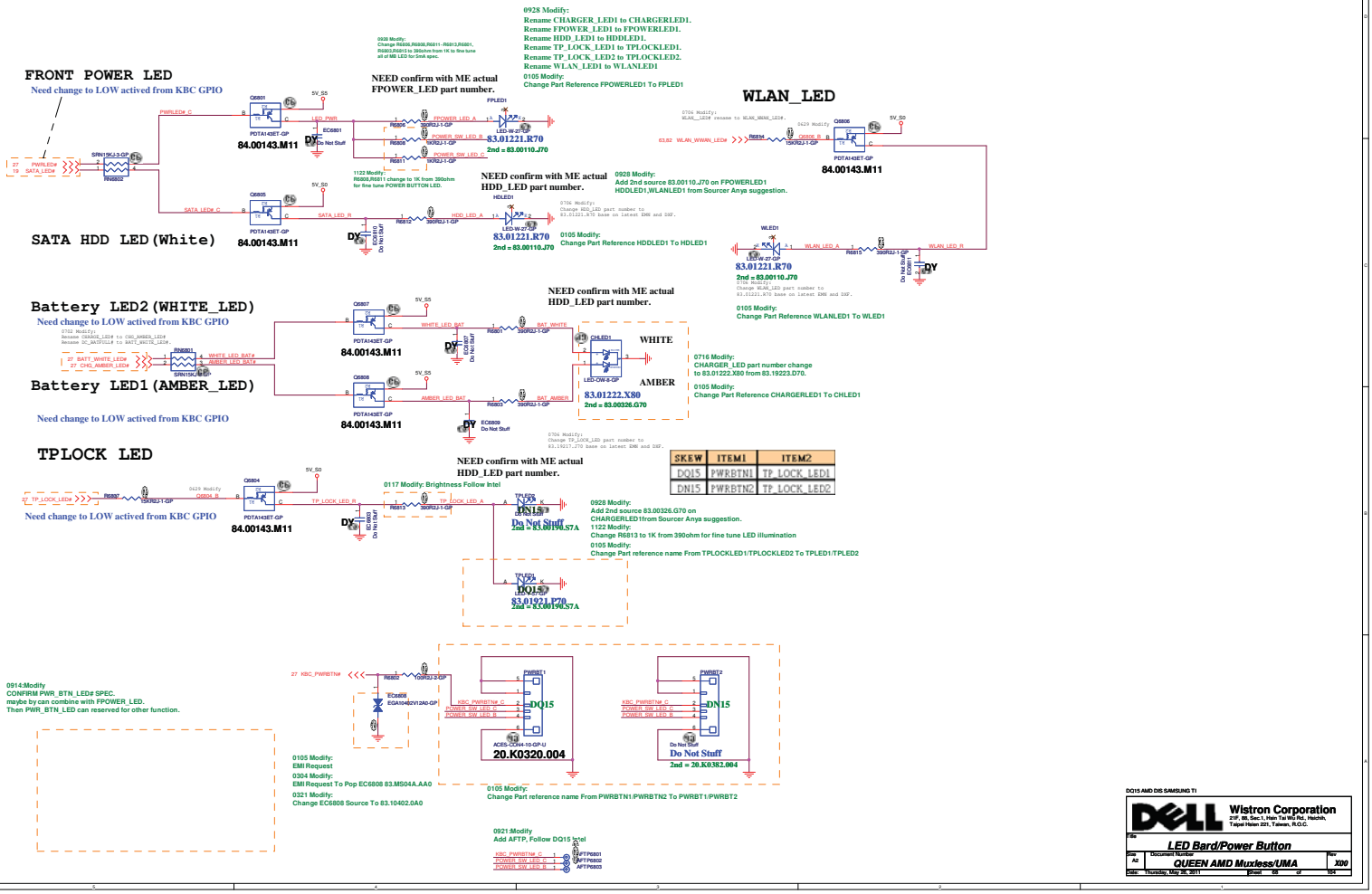
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 67 of 104

SSID = User.Interface



DQ15 AMD DIS SAMSUNG TI

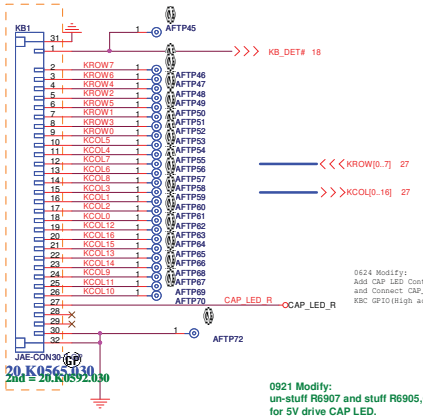
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button
Size: A2 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00
Date: Thursday, May 26, 2011 | Sheet 68 of 104

1122 Modify:
Add 2nd 20.K0592.030 on KB1 from ME
updated connector list.

Internal KeyBoard Connector

0630 Modify:
Change KB1 part number to 20.K0565.030
base on ME updated EMN and DXF.

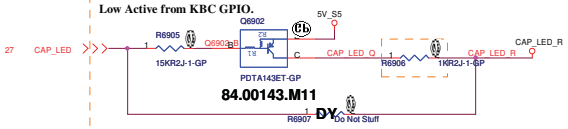


0624 Modify:
Add CAP LED Control circuit(Q6902,R6906,R6907)
and Connect CAP_LED_R control to KB1 pin27 from
KBC GPIO(High active).

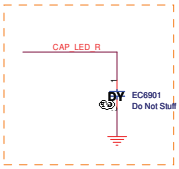
0921 Modify:
un-stuff R6907 and stuff R6905,Q6902,R6906
for 5V drive CAP LED.
0109 Modify: CAP_LED Change To Low Active From KBC GPIO
0109 Modify: R6906 Change To 1K

CAP LED CONTROL

Low Active from KBC GPIO.

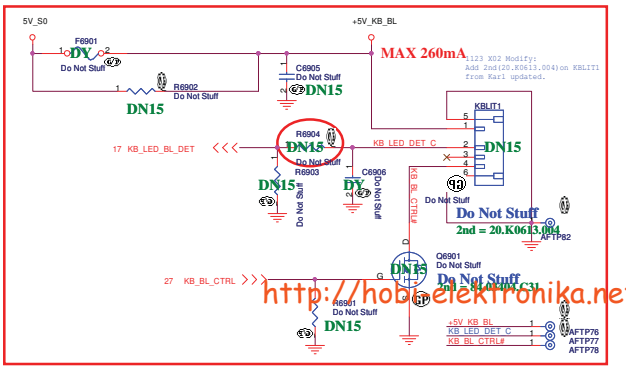


0719: EMI Request



KB Backlight Connector

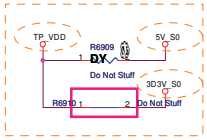
MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#



SSID = Touch.Pad

0624 Modify:
Removed TP_LOCKED CONTROL combin
with KEYBOARD Function KEY.

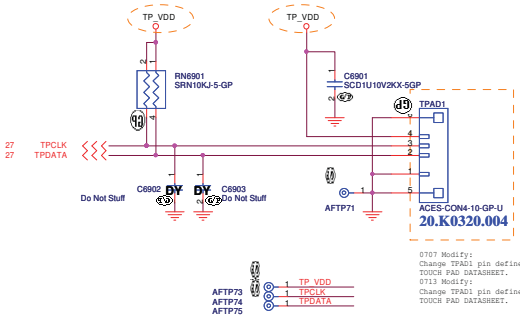
0715 Modify:
Add R6908,R6909 for TPAD1 co-lay power option.
0109 Modify:
Change TP_VDD To 3D3V_S0, Follow Intel



0713 Modify:
Change TPAD1 power source to 3D3V_S0 from
5V_S0 base on DELL latest spec A02.

0630 Modify:
Change TPAD1 part number to 20.K0320.006
base on ME updated EMN&DXF.
0712 Modify:
Change TPAD1 part number to 20.K0320.004
from 20.K0320.006.

TouchPad Connector



MB CONN.	(FFC)
Pin 4	TP_VDD
Pin 3	TPCLK
Pin 2	TPDATA
Pin 1	GND

0707 Modify:
Change TPAD1 pin define to follow
TOUCH PAD DATASHEET.
0713 Modify:
Change TPAD1 pin define to follow
TOUCH PAD DATASHEET.

DQ15 AMD DIS SAMSUNG TI

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Title: Key Board/Touch Pad

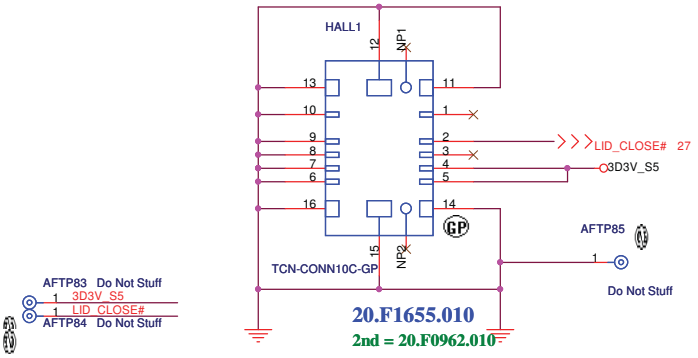
Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 69 of 104

SSID = Hall.Sensor

0906 Modify:
HALL SENSOR move to small board at X01 stage,so
Removed HALLSW1 related circuit and add HALL1
connector.

1122 Modify:
Add 2nd 20.F0962.010 on HALL1 from
ME updated connector list.



DQ15 AMD DIS SAMSUNG TI

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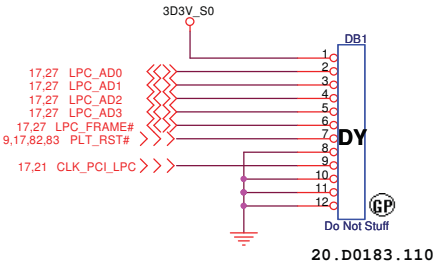
Title: Hall Effect Sensor

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

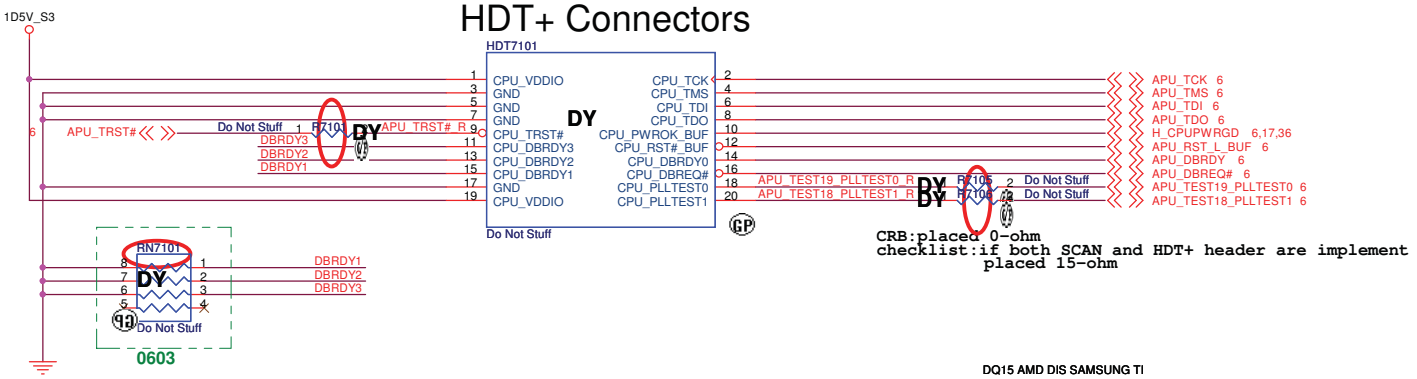
Date: Thursday, May 26, 2011 Sheet 70 of 104

SSID = Debug



20.D0183.110

HDT+ Connectors



CRB:placed 0-ohm
checklist:if both SCAN and HDT+ header are implement
placed 15-ohm

DQ15 AMD DIS SAMSUNG TI

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Title: Dubug connector

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 71 of 104

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DQ15 AMD DIS SAMSUNG TI

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Title: RESERVED

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 72 of 104

DC15 AMD DIS SAMSUNG TI

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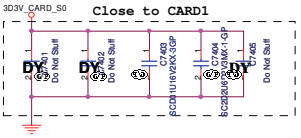
Title: Reserved

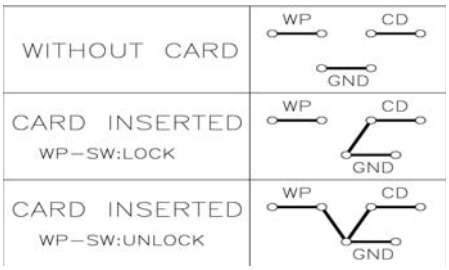
Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	1.00

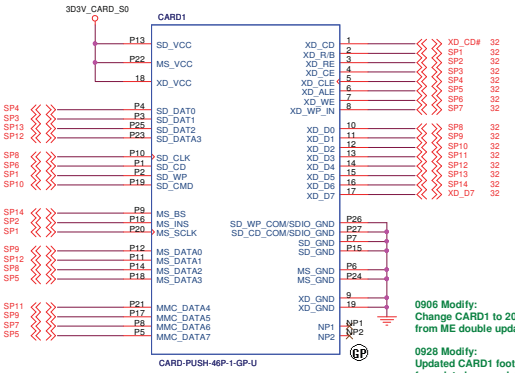
Date: Thursday, May 26, 2011 Sheet 73 of 104

SSID = SDIO



SD/XD/MS/MMC+ Card Reader





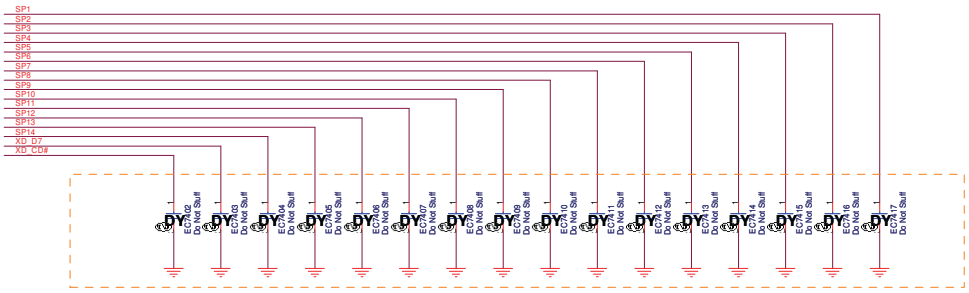
20.I0129.001
2nd = 20.I0135.001
PCB Footprint = R013-P12-HM-1

0906 Modify:
Change CARD1 to 20.I0129.001 from 62.10051.931 from ME double updated latest DXF&EMN on X01.

0928 Modify:
Updated CARD1 footprint to R013-P12-HM-1 from data base updated footprint.

1122 Modify:
Add 2nd 20.I0135.001 on CARD1 from ME updated latest connector list.

For EMI Reserved



0913: Schematic Score Card Suggest Cap Less Than 10P

20.I0129.001

PIN	TYPE	FUNCTION	RTS5138 NET
P1	SD	SD-CD	SP6
P2	SD	SD-WP	SP1
P3	SD	SD-DAT1	SP3
P4	SD	SD-DAT0	SP4
P5	MMC_PLUS	MMC-DATA7	SP5
P6	MemoryStick	MS-GND	GND
P7	SD	SD-GND	GND
P8	MMC_PLUS	MMC-DATA6	SP7
P9	MemoryStick	MS-BS	SP14
P10	SD	SD-CLK	SP8
P11	MemoryStick	MS-DATA1	SP12
P12	MemoryStick	MS-DATA0	SP9
P13	SD	SD-VCC	3D3V_CARD_S0
P14	MemoryStick	MS-DATA2	SP8
P15	SD	SD-GND	GND
P16	MemoryStick	MS-INS	SP2
P17	MMC_PLUS	MMC-DATA5	SP9
P18	MemoryStick	MS-DATA3	SP5
P19	SD	SD-CMD	SP10
P20	MemoryStick	MS-SCLK	SP1
P21	MMC_PLUS	MMC-DATA4	SP11
P22	MemoryStick	MS-VCC	3D3V_CARD_S0
P23	SD	SD-DATA3	SP12
P24	MemoryStick	MS-GND	GND
P25	SD	SD-DAT2	SP13
P26	SD	SD-WP COM /SDIO GND	GND
P27	SD	SD-CD COM /SDIO GND	GND
#1	XD	XD-CD	XD_CD#
#2	XD	XD-R/B	SP1
#3	XD	XD-RE	SP2
#4	XD	XD-CE	SP3
#5	XD	XD-CLE	SP4
#6	XD	XD-ALE	SP5
#7	XD	XD-WE	SP6
#8	XD	XD-WP-IN	SP7
#9	XD	XD-GND	GND
#10	XD	XD-D0	SP8
#11	XD	XD-D1	SP9
#12	XD	XD-D2	SP10
#13	XD	XD-D3	SP11
#14	XD	XD-D4	SP12
#15	XD	XD-D5	SP13
#16	XD	XD-D6	SP14
#17	XD	XD-D7	XD-D7
#18	XD	XD-VCC	3D3V_CARD_S0
#19	XD	XD-GND	GND

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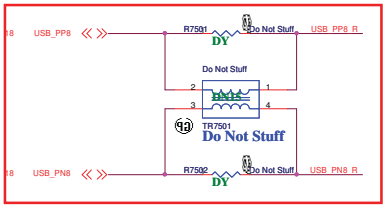
Title: CARD Reader CONN

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

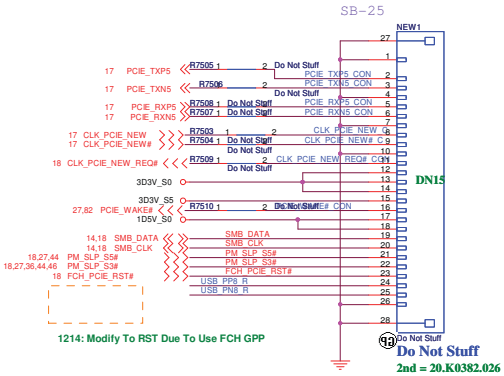
Date: Thursday, May 26, 2011 | Sheet 74 of 104

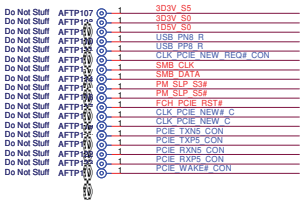
SSID = ExpressCard

1122 X02 Modify:
Change TR7501 CM choke to 69.10103.041
and un-stuff R7501,R7502 from EMC Neo Suggestion.
Change R7501,R7502 to 0603 from 0402.
1123 X02 Modify:
SWAP TR7501 pin1&4 and pin2&3 each other
base on Connie swap report.

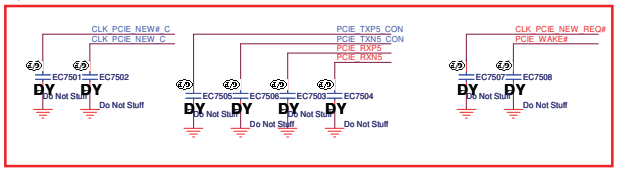


1D5V_S0_CARD Max. 650mA, Average 500mA.
3D3V_S0_CARD Max. 1300mA, Average 1000mA
3D3V_S5_CARDAUX Max. 275mA





For EMI



DQ15 AMD DIS SAMSUNG TI

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Title: Express Card

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 75 of 104

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Title: Reserved

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	1.00

Date: Thursday, May 26, 2011 Sheet 76 of 104

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Title: Reserved

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	1.00

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DQ15 AMD DIS SAMSUNG TI

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Title: Reserved

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

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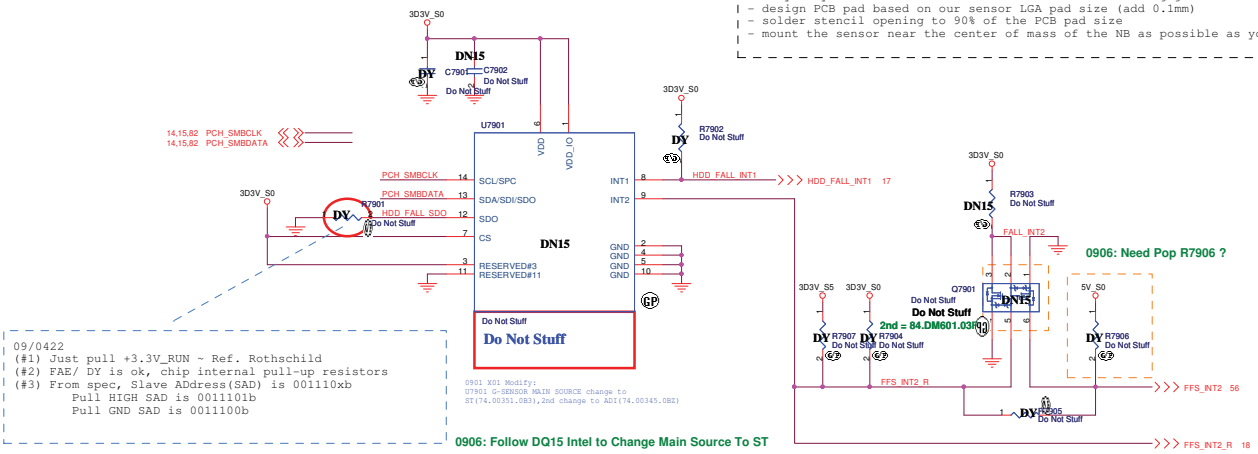
SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

DQ15 AMD DIS SAMSUNG TI

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Title: Free Fall Sensor

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	1.00

Date: Thursday, May 26, 2011 Sheet 79 of 104

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Title: ***Reserved***

Size	Document Number	Rev
A	***QUEEN AMD Muxless/UMA***	***1.00***

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DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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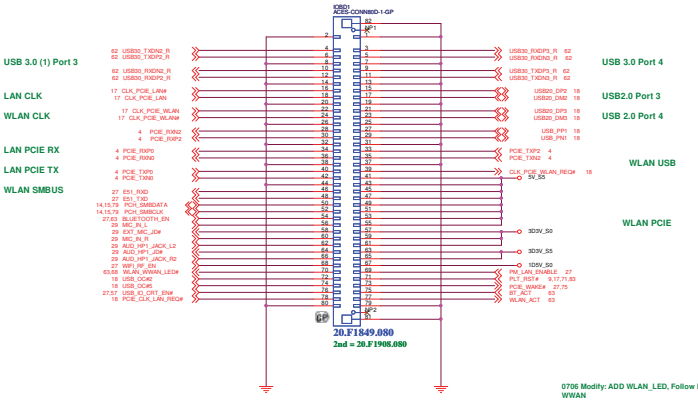
Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A4	QUEEN AMD Muxless/UMA	X00

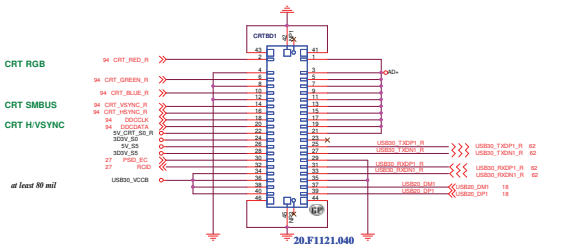
Date: Thursday, May 26, 2011 Sheet 81 of 104

IO Board CONN 80 pin

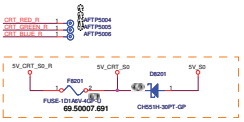


0706 Modify: ADD WLAN_LED, Follow Intel, AMD Dont have WWAN

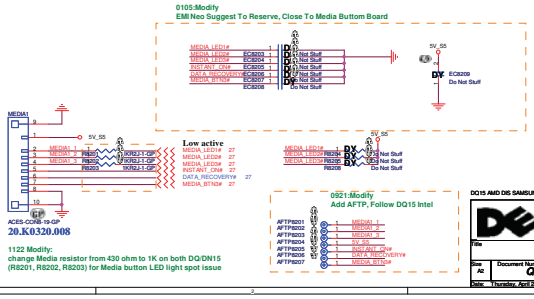
1123 Modify: Change Main Source To 20.F1849.080 & Add 2nd 20.F1908.080 on IOBD1 from ME updated latest connector list & Modify Pin Define So 4 corner pin are GND.



0914 Modify:
Change BTB Connector To 20.F1121.040
Follow ME Connector List
1228 Modify:
Remove USB 3.0 Signal and Re-arrange Pin-Define For Better Layout Routing
1118 Modify:
Modify Pin Define



0906 Modify:
Change Part Number 20.K0422.010 To20.K0320.008
Base On ME Connector List
0914 Modify:
Change R8201 ~R8203 to 470 ohm from 33ohm
for fine tune MEDIA LED 5mA current.
0928 Modify:
Change R8201 ~R8203 to 430 ohm from 470 ohm
for fine tune MEDIA LED 5mA current.



1122 Modify:
change Media resistor from 430 ohm to 1K on both DQ/DN15
(R8201, R8202, R8203) for Media button LED light spot issue

0921:Modify
Add AFTP, Follow DQ15 Intel

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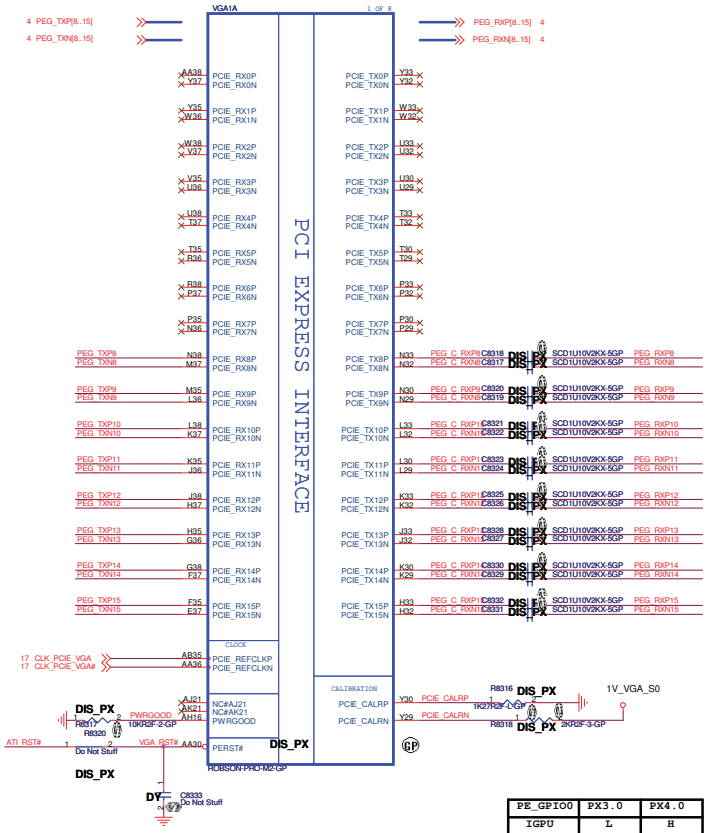
Title: IO Board Connector
Size: A0 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00
Date: Thursday, April 21, 2011 | Sheet 80 of 104



PE_GPIO0	PX3.0	PX4.0
IGPU	L	H
DGPU	H	H

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

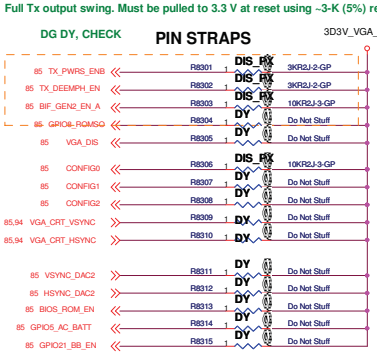
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	1
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

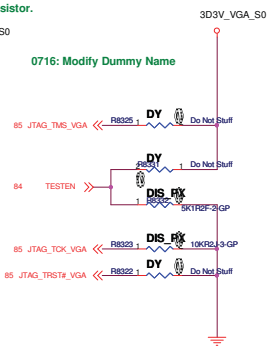
Full Tx output swing. Must be pulled to 3.3 V at reset using ~3-K (5%) resistor.

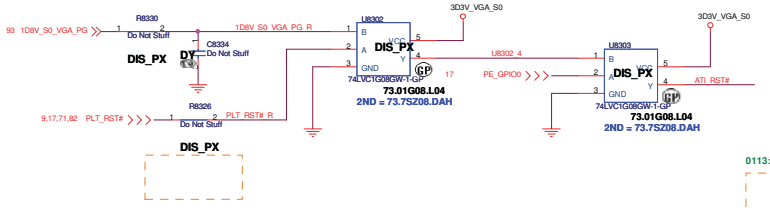
DG DY, CHECK

PIN STRAPS

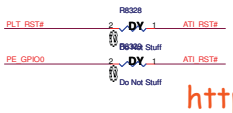


0716: Modify Dummy Name





0113: Remove APU_RST# Colay



JTAG SIGNAL OPTION – for option2

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

0113: Remove APU_RST# Level Shift

1008: Add Level Shift For APU_RST# To 3.3V

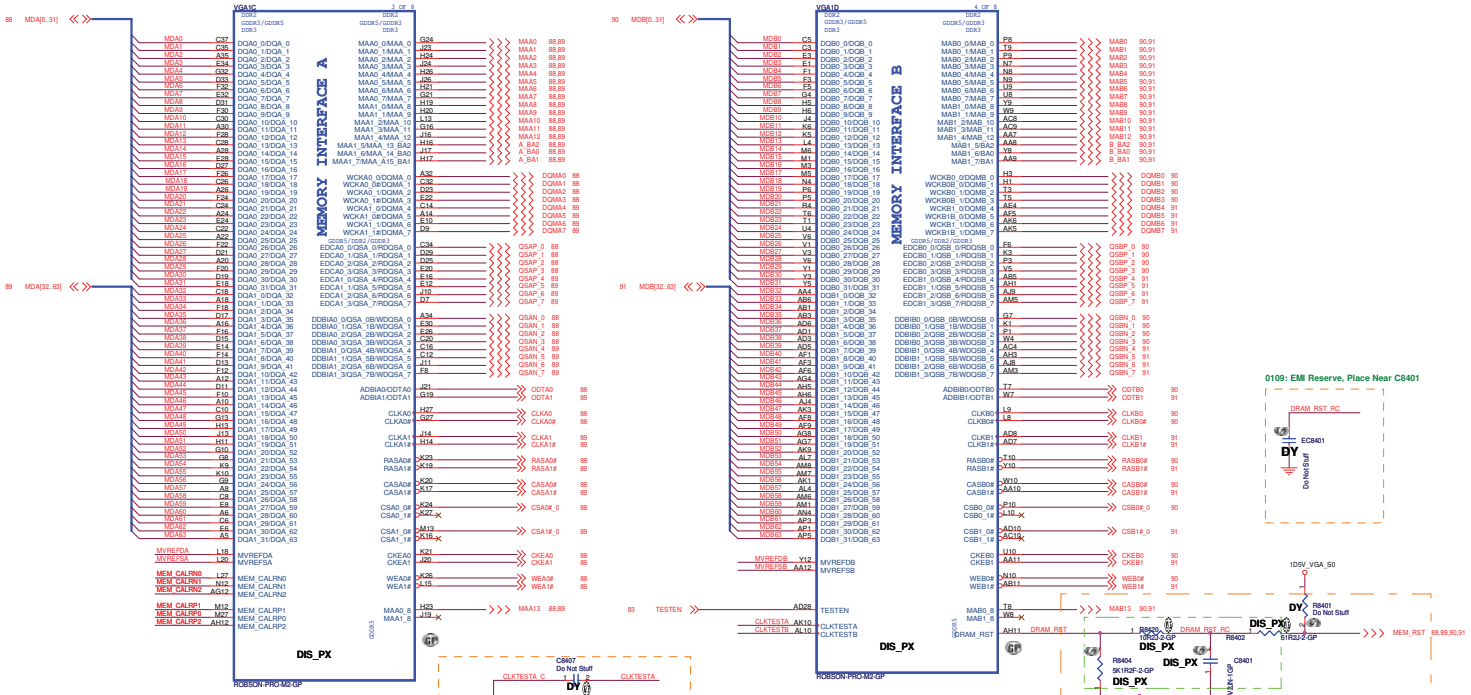
DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: Custom | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 83 of 104



DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size	Document Number	Rev
Custom	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 | Sheet 84 of 104

1228: Modify Table

Default 1G + Hynix Vram, 0011 72.52G63.A0U

MEMORY ID Table

DVPDATA[3:0]	Description	PN
0001	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16	72.52G63.A0U
0011	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16	72.51G63.H0U
0010	DDR3 SAMSUNG-K4W2G1646C-HC11(900MHz) 128M*16	72.42164.D0U
0000	DDR3 SAMSUNG-K4W1G1646G-BC11 (900MHz) 64M*16	72.41646.Q0U

0914: Change R8518 Part Reference To HYNIX
For Hynix + Vram 1G, Pop R8518, Pop R8519
For Hynix + Vram 512M, Pop R8518, De-pop R8519
For Samsung+Vram1G, De-pop R8518, Pop R8519
For Samsung+Vram512M, De-pop R8518, De-POP R8519

0708: Need To Pick GPIO
0708: Add Thermal Shutdown Circuit
0107: SW Will Not Use This Function, DY For Reserve Only

I2C Bus for LVDS

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

0107 Modify:
Removed P2800 Circuit , So does C8523.

FOR HDMI 1.4

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

1027 Modify: Use VGA Smbus Instead of use another P2800

0112: Dummy Cap

0112: Remove Cap

LVDS Interface

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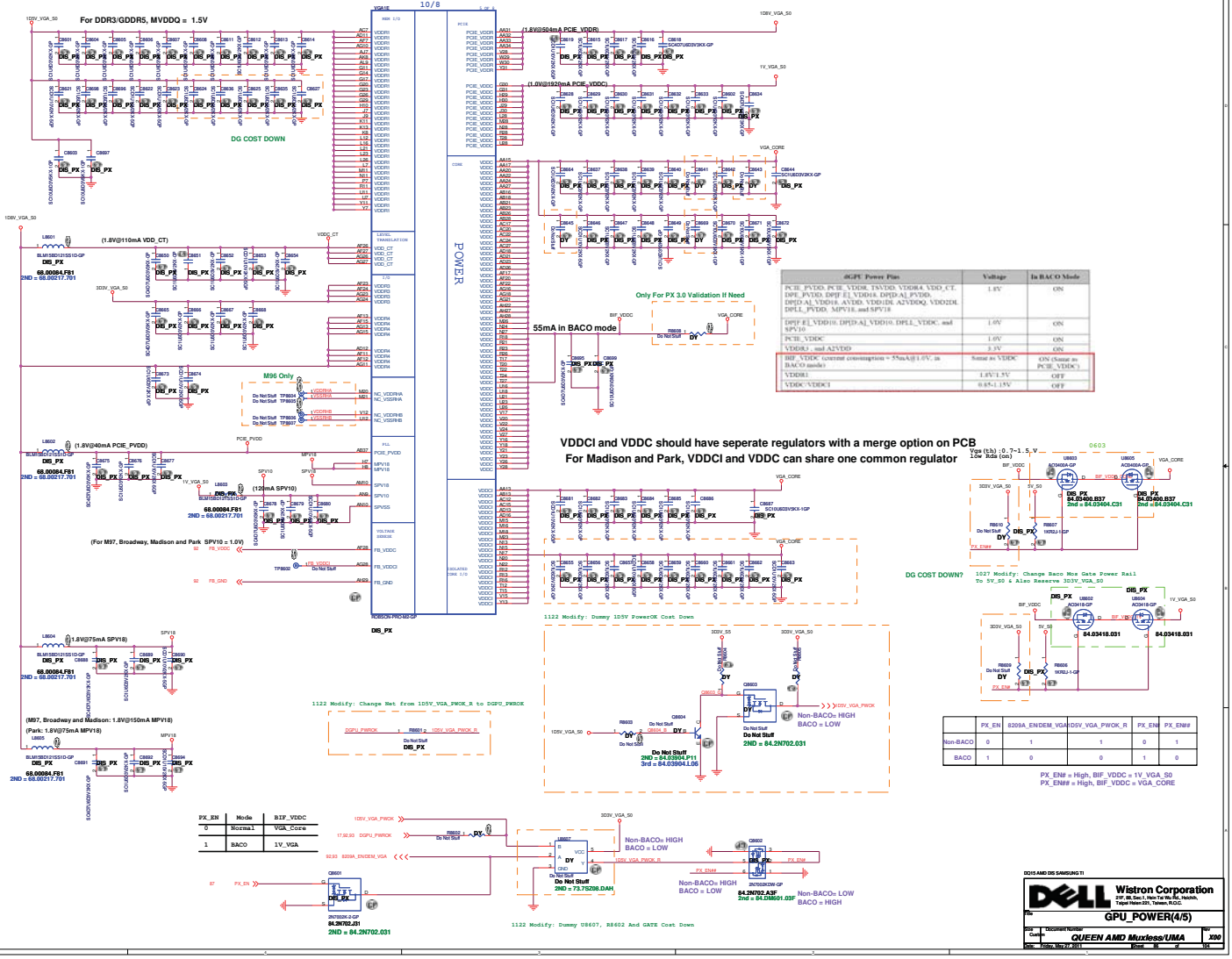
Title	GPU_DP/LVDS/CRT/GPIO(3/5)
Size	A0
Document Number	QUEEN AMD Muxless/UMA
Rev	X00
Date	Thursday, May 26, 2011
Sheet	18 of 104



.GPU Power Plan	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDDR4_CT, DPE_PVDD, DPIT_E1, VDDI18, DPD[A]_PVDD, DPD[A]_VDDI18, AVDD, VDDPDB, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DPIT_E1_VDDI18, DPD[A]_VDDI18, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 , and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC, VDDCI	0.85-1.15V	OFF

	PX_EN	8209A_ENDEM_VGA	1D5V_VGA_PWOK_R	PX_EN	PX_EN#
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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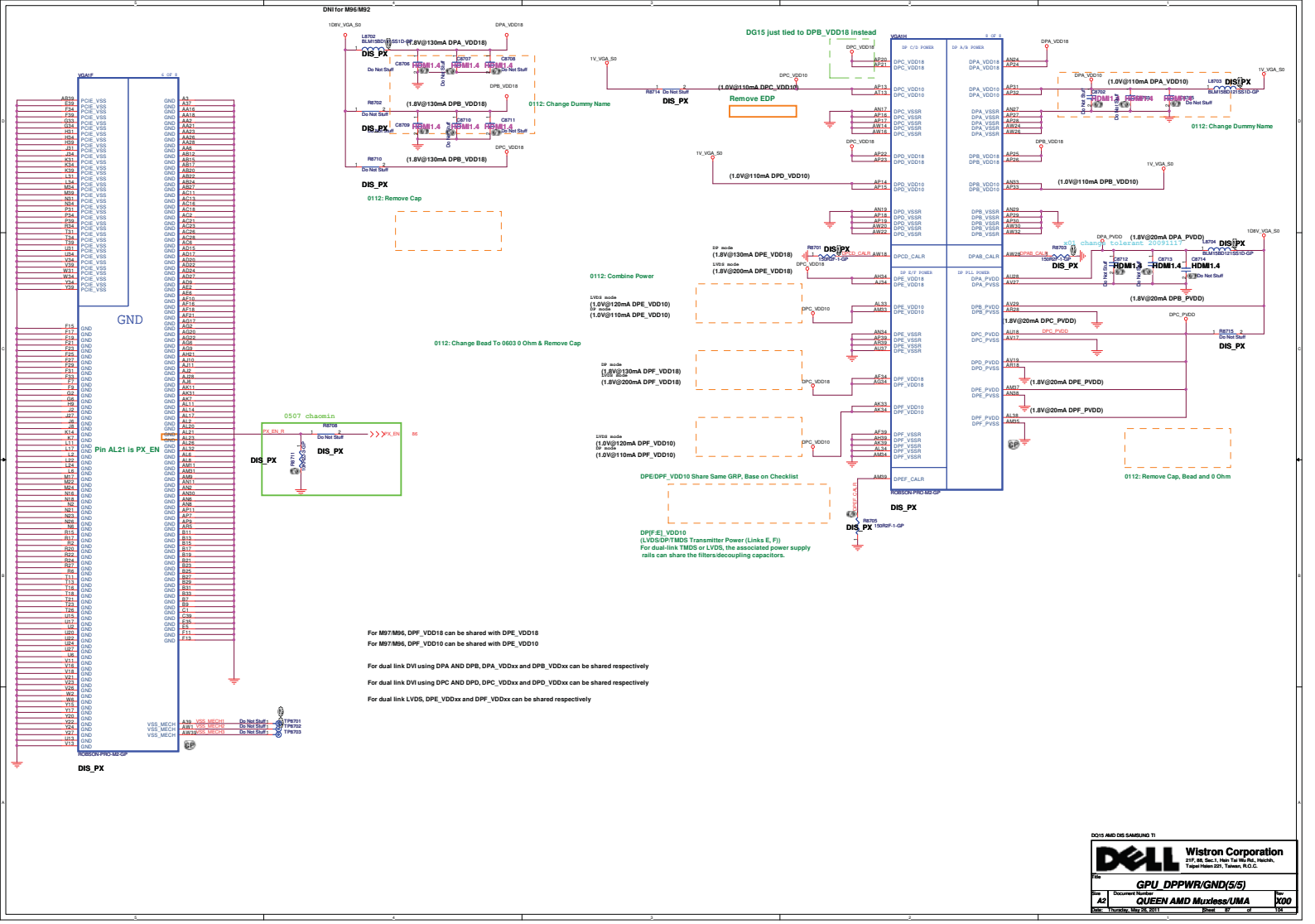
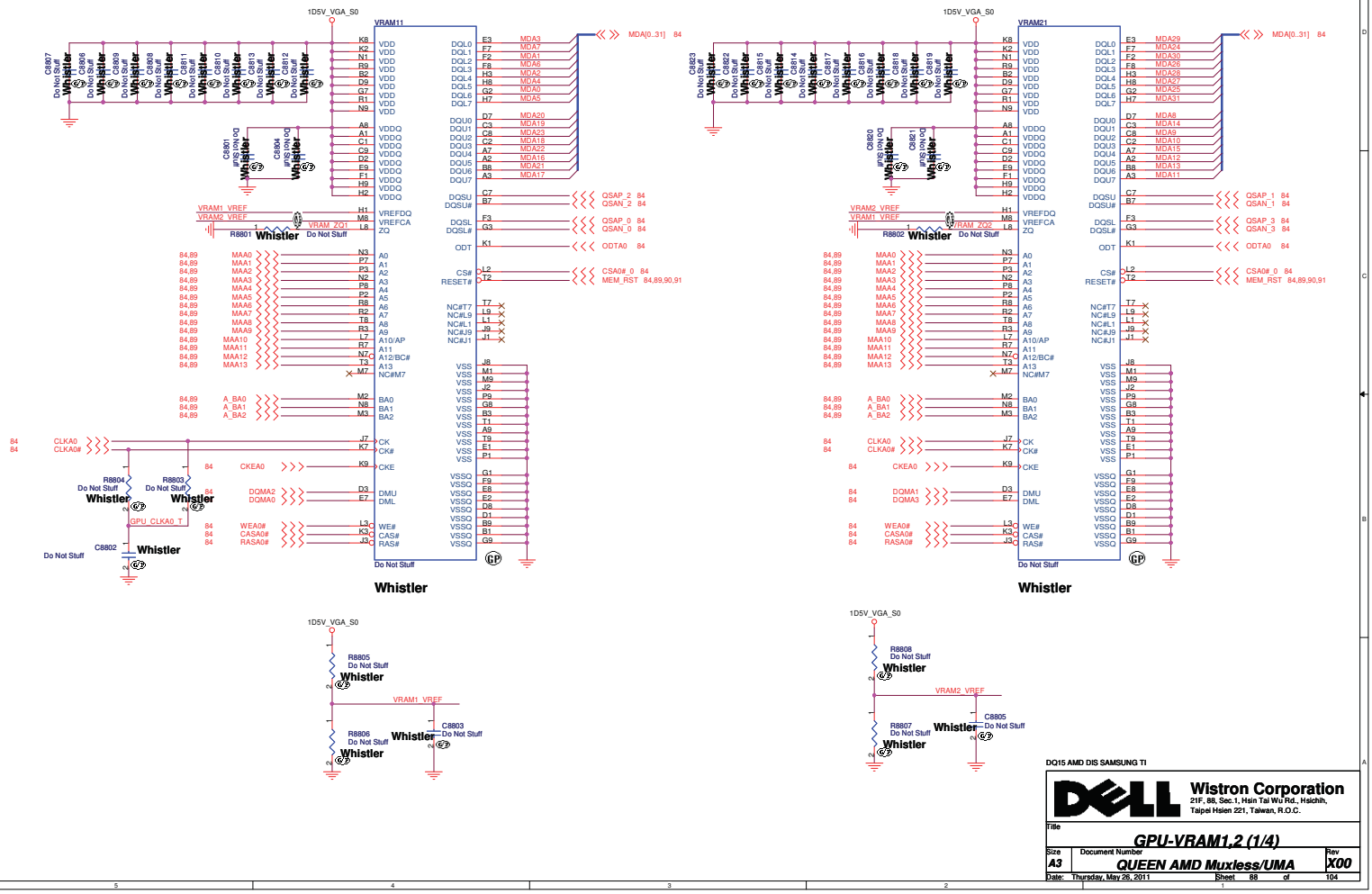
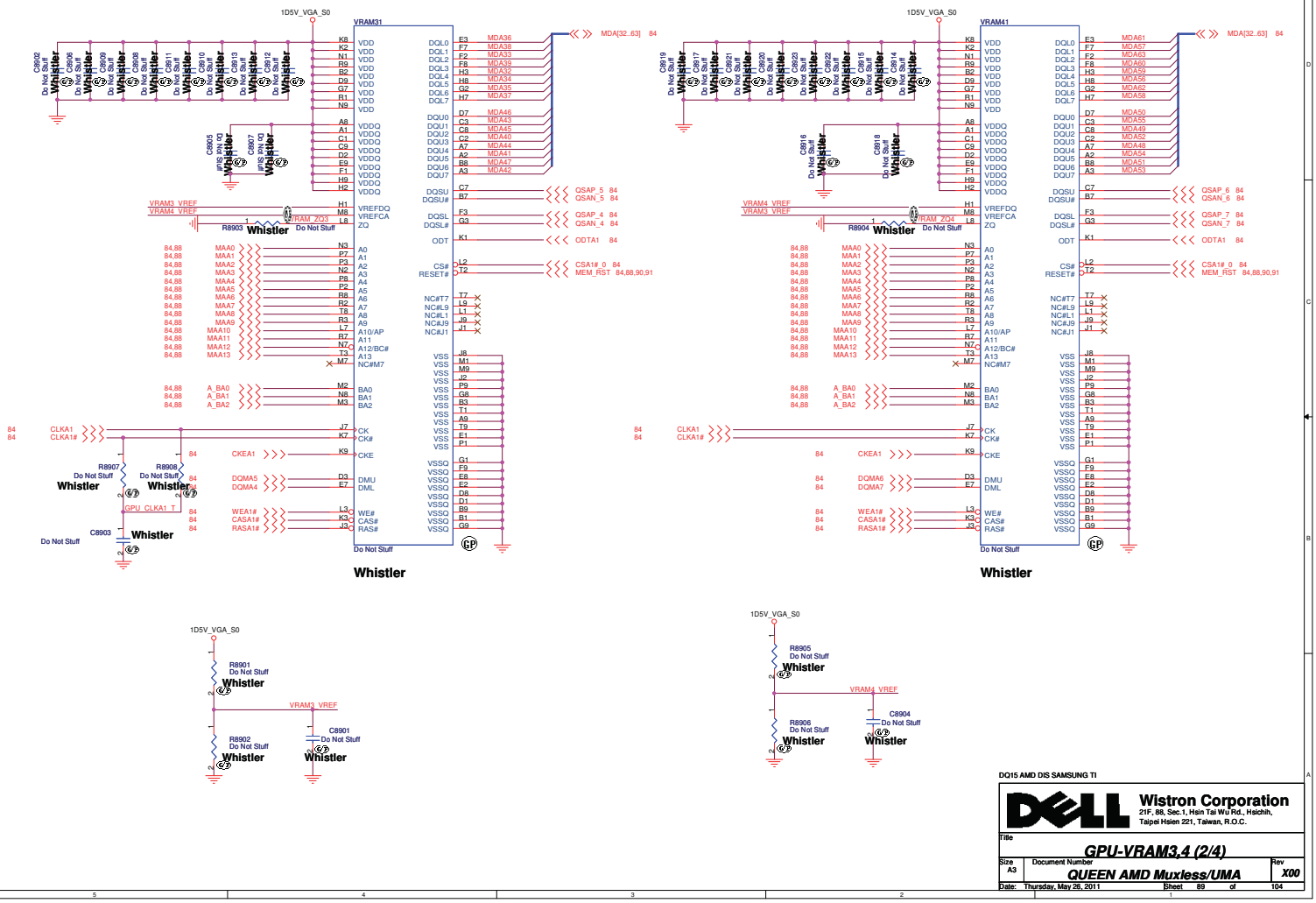
Title	GPU_POWER(4/5)
Size: Custom	Document Number: QUEEN AMD Muxless/UMA
Rev: X00
Date: Friday, May 07, 2010	Sheet 36 of 45







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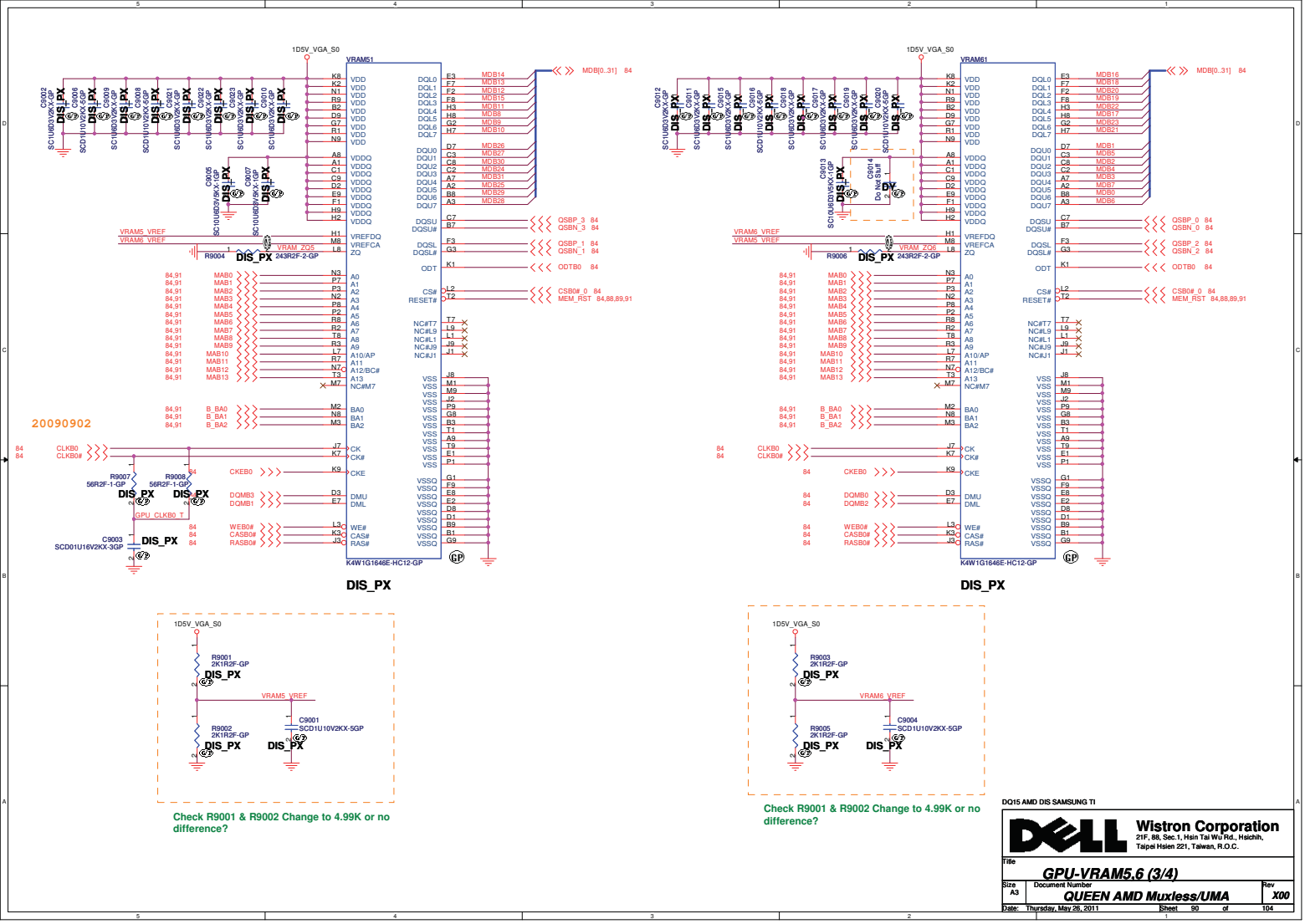
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM3,4 (2/4)**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 89 of 104



Check R9001 & R9002 Change to 4.99K or no difference?

Check R9001 & R9002 Change to 4.99K or no difference?

DQ15 AMD DIS SAMSUNG TI

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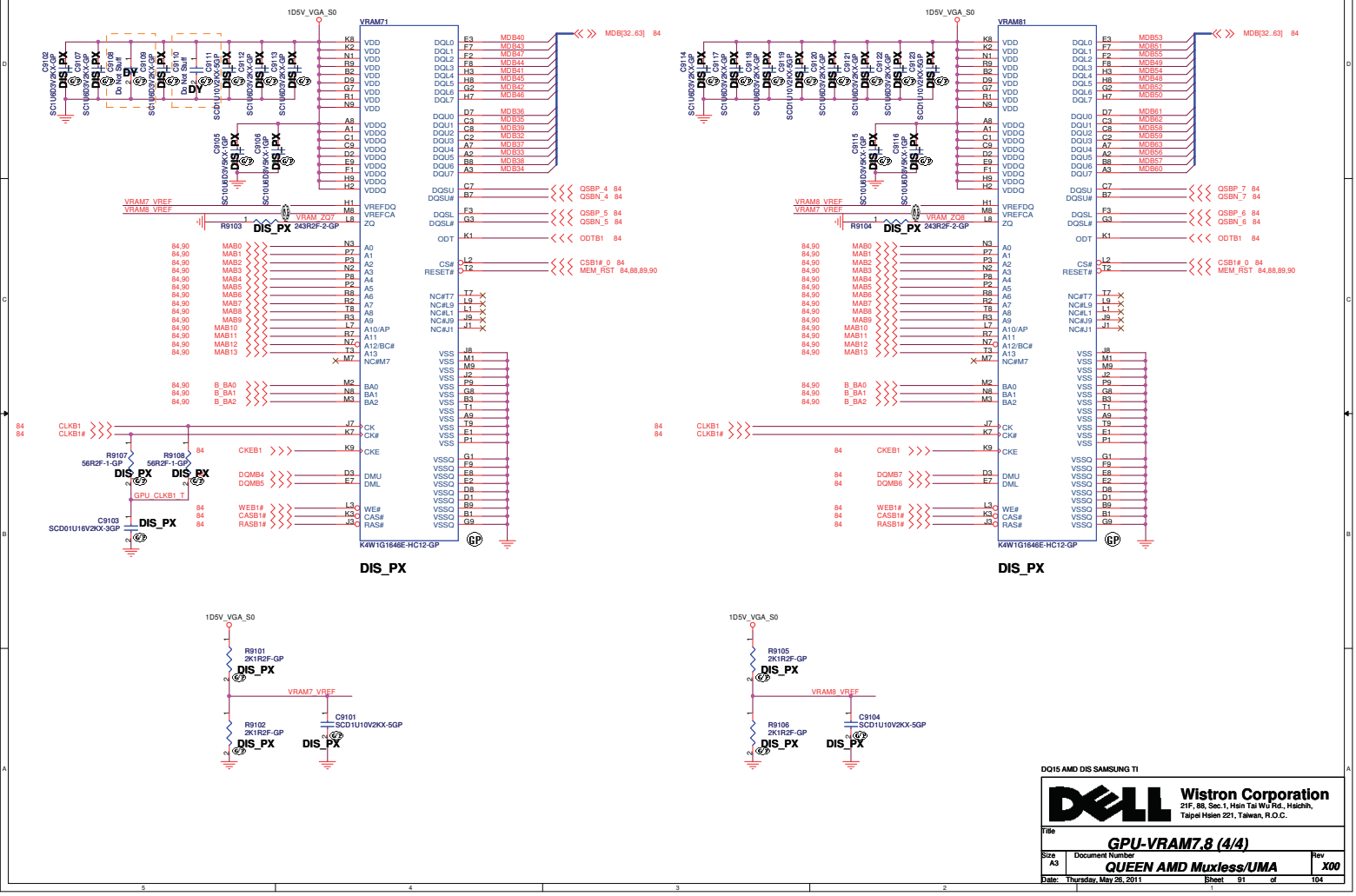
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU-VRAM5,6 (3/4)**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 90 of 104



DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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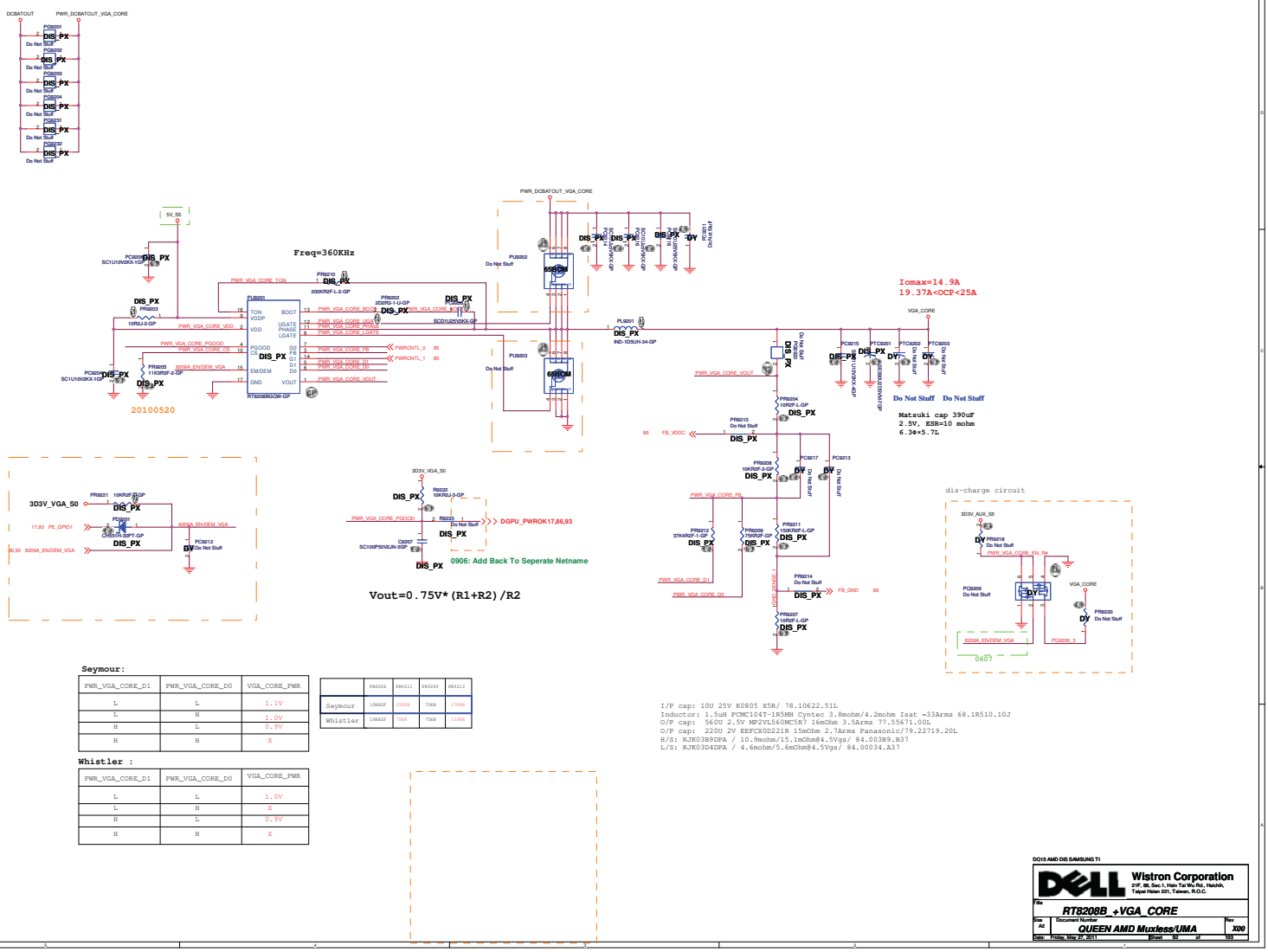
Title: **GPU-VRAM7,8 (4/4)**

Size	Document Number	Rev
A3	QUEEN AMD Muxless/UMA	X00

Date: Thursday, May 26, 2011 Sheet 91 of 104



Seymour:

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.1V
L	H	1.0V
H	L	0.9V
H	H	X

	PR8208	PR8211	PR8209	PR8212
Seymour	10K82F	150K5	75K5	37K4
Whistler	10K82F	75K5	75K5	150K5

Whistler :

PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
L	L	1.0V
L	H	X
H	L	0.9V
H	H	X

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5uH PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 560U 2.5V MP2VL560M2SR7 16mOhm 3.5Arms 77.55671.00L
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms Panasonic/79.22719.20L
H/S: RJK03B9DPA / 10.9mohm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA / 4.6mohm/5.6mOhm@4.5Vgs/ 84.00034.A37

DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
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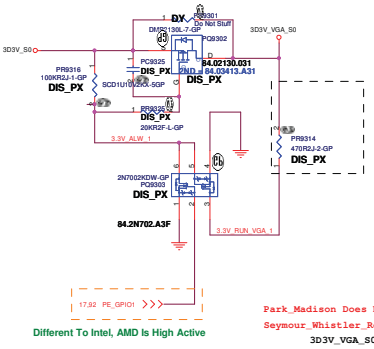
Title: RT8208B +VGA_CORE

Size	Document Number	Rev
A2	QUEEN AMD Muxless/UMA	X00

Date: Friday, May 27, 2011 Sheet 50 of 53

+3VS to 3.3V_DELAY Transfer



Different To Intel, AMD Is High Active

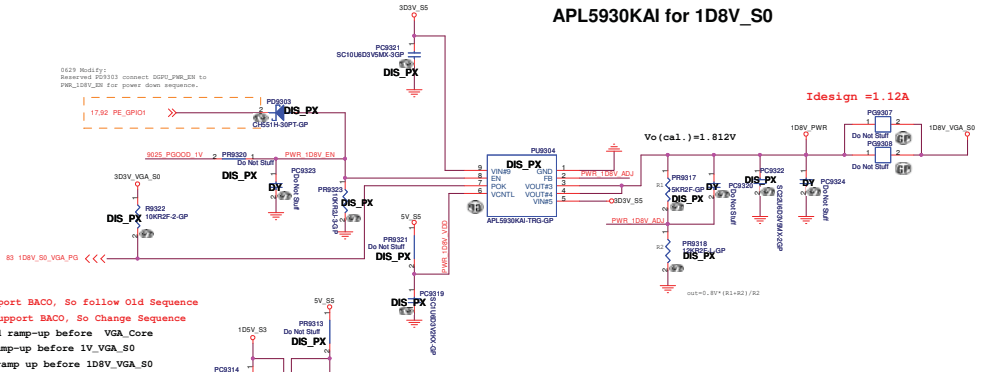
PE_GPIO1	PX3.0	PX4.0
IGPU	L	H
DGPU	H	H

2nd = 84.DM601.03F

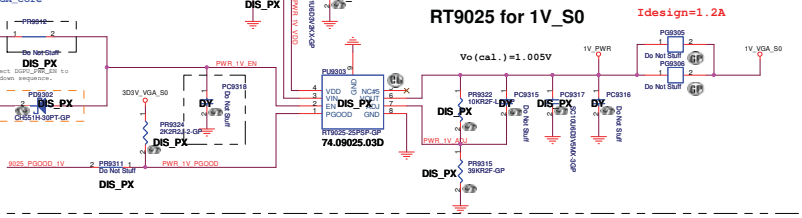
Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Coreshould ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

so 1V_VGA_S0 EN have to fine tune RC after VGA_Core

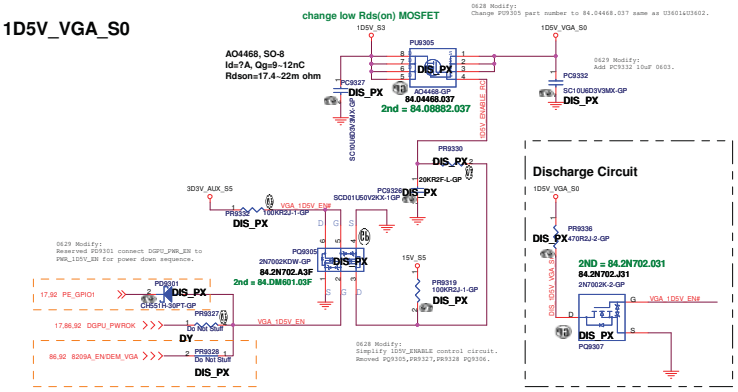
APL5930KAI for 1D8V_S0



RT9025 for 1V_S0



1D5V_VGA_S0



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Title: DISCRETE VGA POWER

Size	Document Number	Rev
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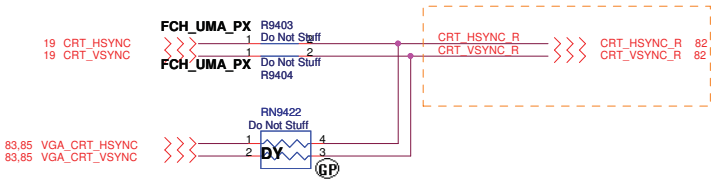
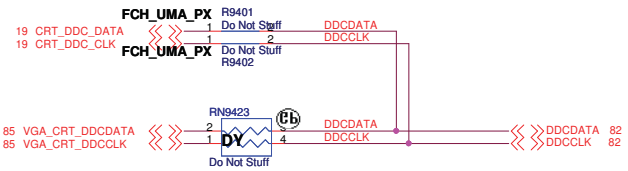
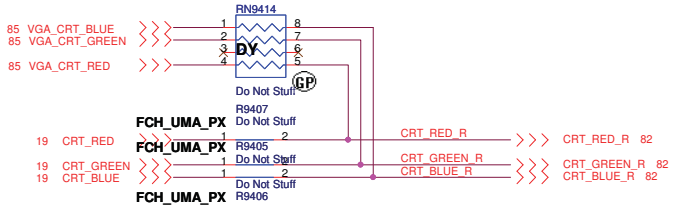
SSID = VIDEO







DQ15 AMD DIS SAMSUNG TI

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_VGA_Switch

Size | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

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DQ15 AMD DIS SAMSUNG TI

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Title

Reserved

Size	Document Number	Rev
A	***QUEEN AMD Muxless/UMA***	***1.00***
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TOUCH PANEL connector

0707: Move To Page 49, Touch Panel Combine With LVDS

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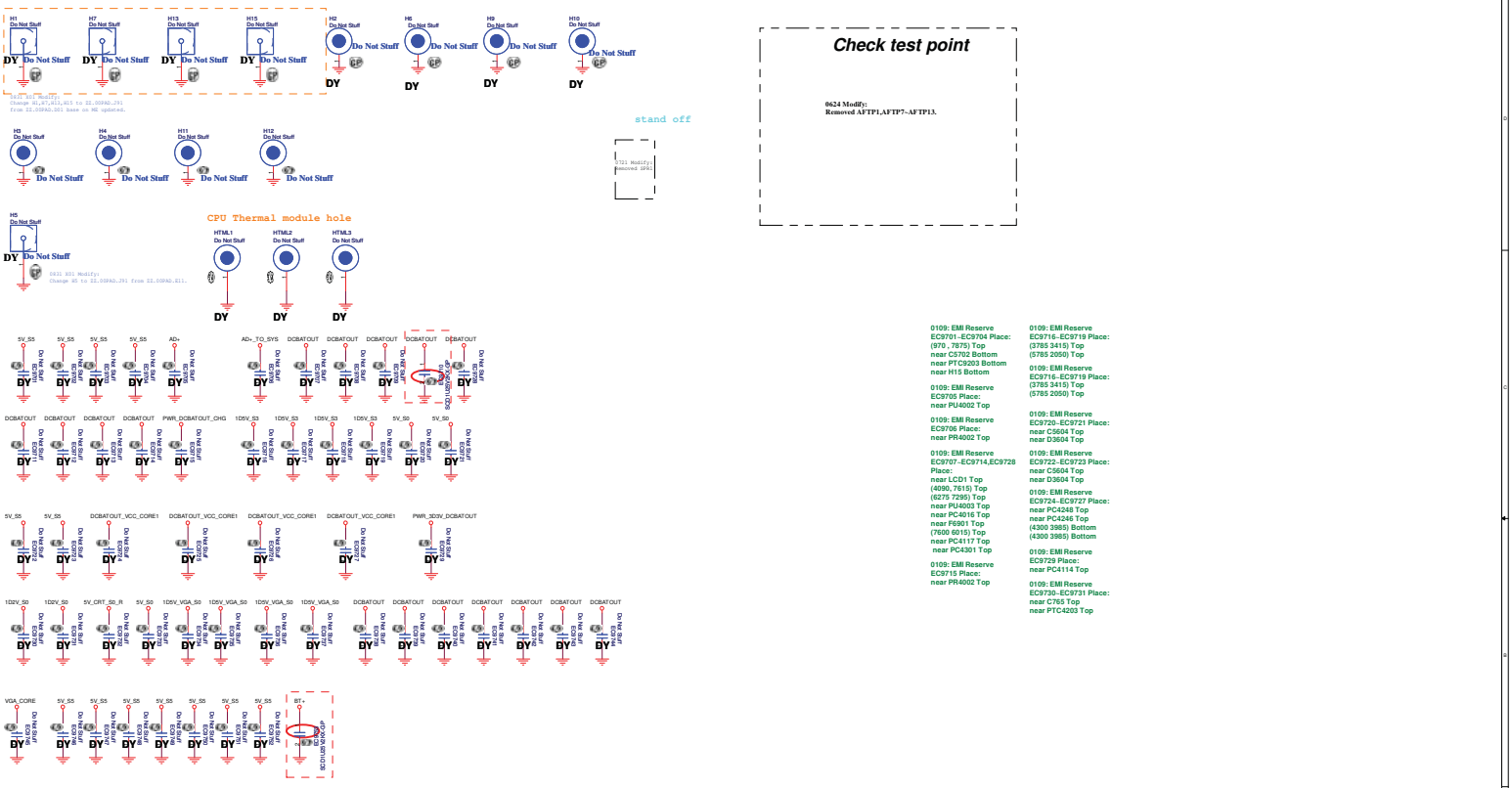
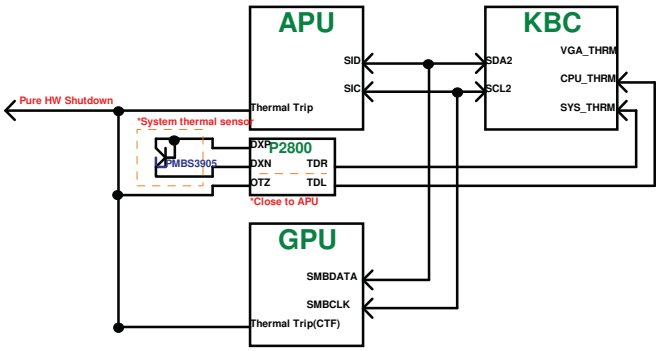
Title: Touch Panel

Size: A | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

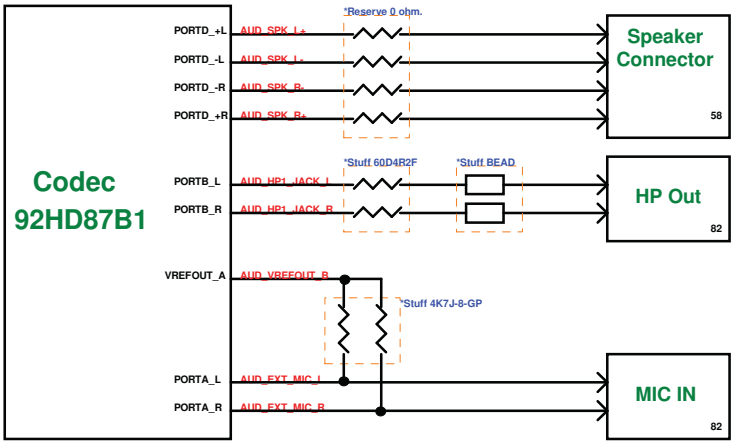
Date: Thursday, May 26, 2011 | Sheet 96 of 104



Thermal Block Diagram



Audio Block Diagram



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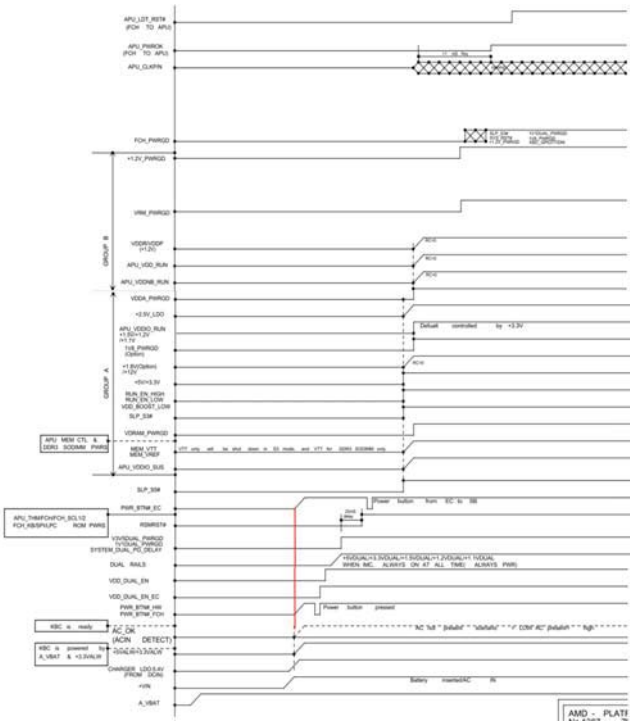
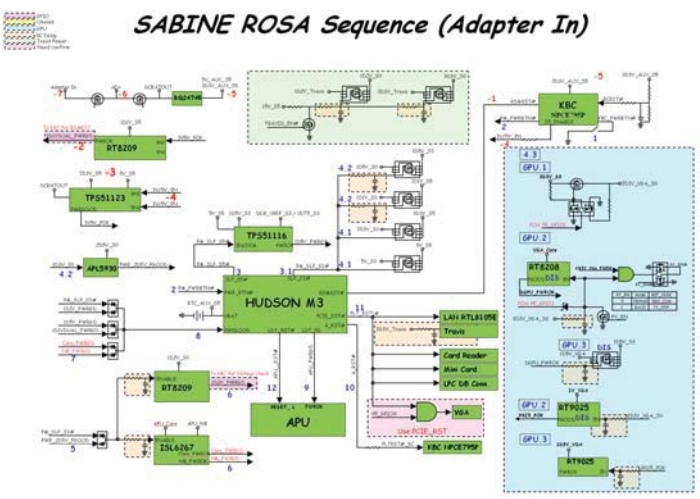
Title	THERMAL/AUDIO BLOCK DIAGRAM	
Size A3	Document Number QUEEN AMD Muxless/UMA	Rev X00
Date: Thursday, May 26, 2011	Sheet 98 of 104	

POWER SEQUENCE

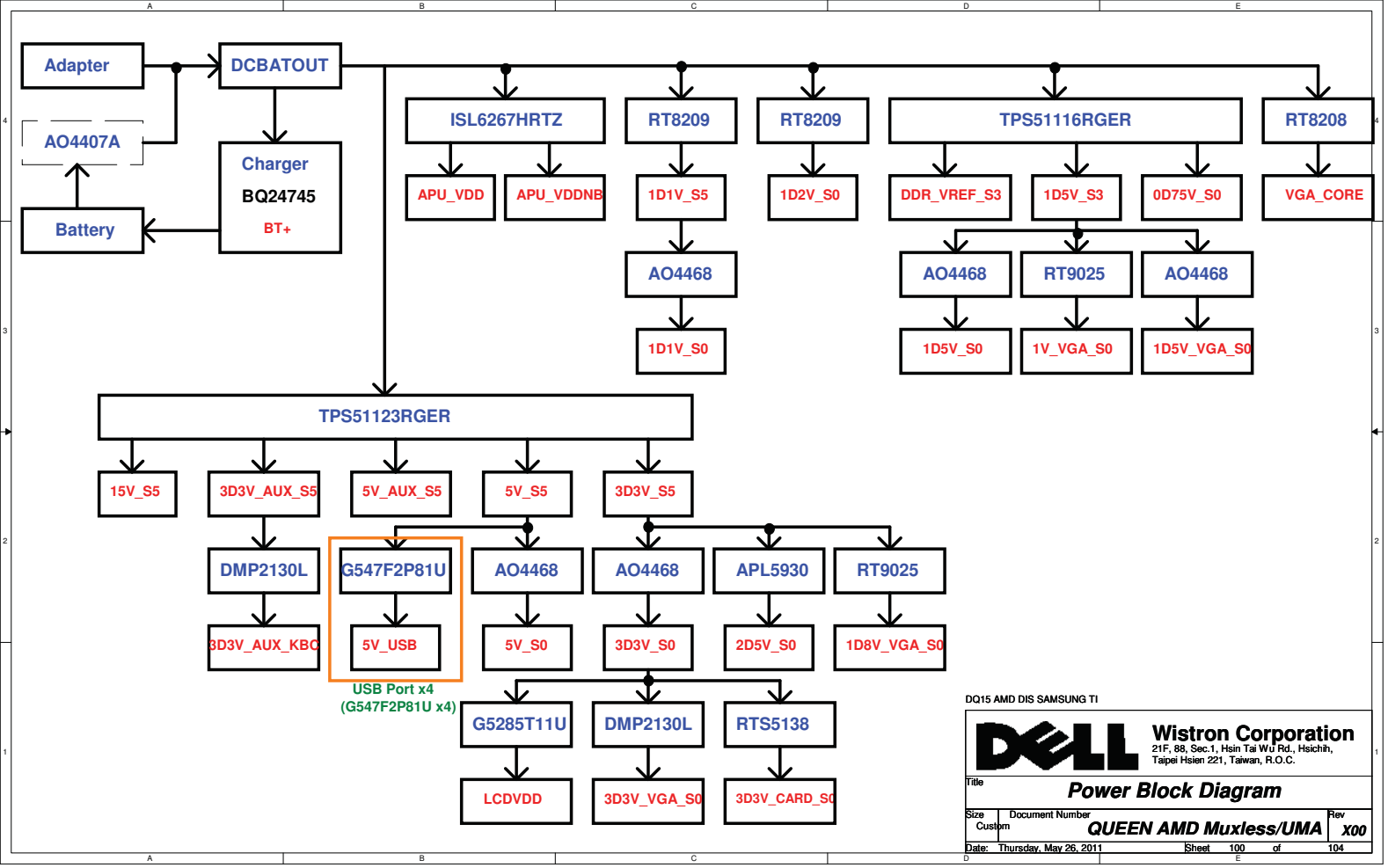


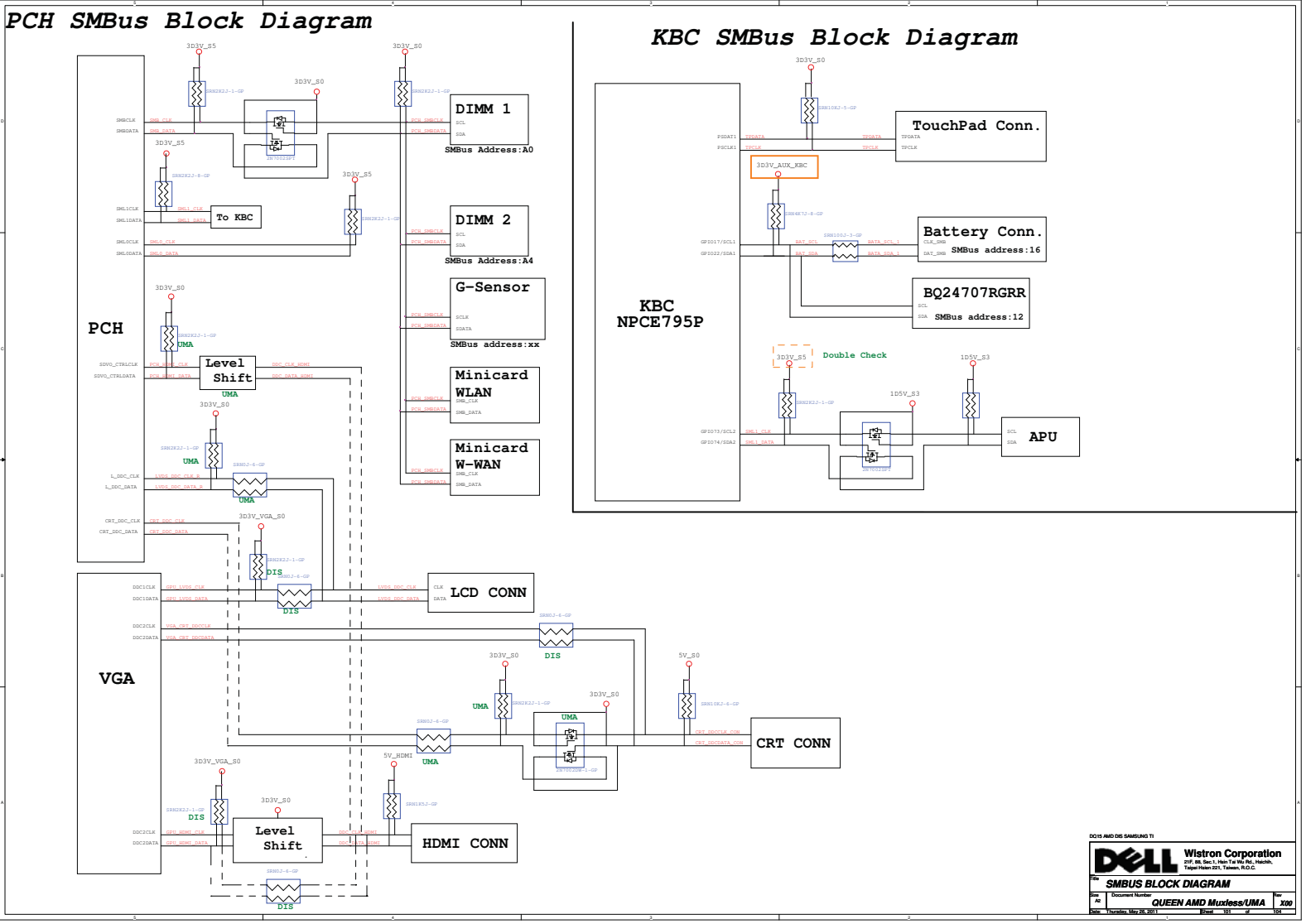


DELL Wistron Corporation

POWER SEQUENCE

QUEEN AMD Muxless/UMA





Change notes -

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Title: *Change notes*

Size	Document Number	Rev
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Change notes – Page 4

VERSON	DATE	ITEM	PAGE	Modify List	Issue Description	OWNER
X02	01/08	3	18,19	Add C1825,C1922.	Reduce V_REF ripple by EA team result.	EE
		4	37	Reserve C3721,C3722.	Prevent signal cross talk.	EE
		5	ALL	Change capacitors value and add C3723.	Ensure signal quality.	EE
	01/11	1	68	Change KB1 P/N.	According ME request.	ME
		2	66	Change R6601,R6602,R6604,R6606 to 1KR, R6603 to 470R.	Decrease LED brightness.	EE
	01/12	1	37	Add C3724, R3757.	To set accurate current detection in EC.	EE
		2	10	Add R1041 0R.	Add 0R for level shift off.	EE
	01/13	1	21,37	Add C3725, C2105.	Reserve for singal quality.	EE
	01/14	1	Power	Modify power team componets.	Request by Power Team.	Power
		2	7	Change RN712 to 22R.	Fine tuned damping resistor value.	EE
A00	02/08	1	66	Reserve R6609, R6610 1KR.	Add for future LED brightness balance.	EE
		2	68	Add keyboard back light circuit, remove R5403.	Add for keyboard with back light module.	EE
		3	69	Change HALLSW1 footprint for co-layout.	Change for co-layout different kind of HALLSW1.	EE
		4	77	Add AFTP7701, AFTP7702, AFTP7703.	Add AFTP test point for factory test.	EE
	02/10	1	Power	Update Obsolete parts.	Update obsolete parts due to policy.	Power
		2	79	Change HBT1 part number.	Change HBT1 part number to match ME EMN file.	ME
		3	47	Add PTC4710.	Add to solve board accoustic issue.	EE
	02/22	1	54	Remove co-layout pad.	As factory requst.	EE
		2	42	Add C4217, C4401, C4402.	Ensure signal quality.	EE
		3	48	Delete Power Gap.	Request by Power Team.	Power
	02/23	1	ALL	Change to short pad.	Change most of 0-ohm resistors to short pad.	EE
	02/24	1	7,68,79	Reserve C724, C725, C6806, C6807, EC7928-EC7932.	As EMC team request.	EMC
	02/25	1	13	Add TP1309.	As factory requset to add.	Factory
		2	7,68	Rename EMC capacitor to EC704,EC705,EC6801,EC6802.	Meet schematic standardization.	EE
		3	49,89	Change PR4913 to 3.9R, PR8905 to 6.98KR.	PR4913 for snubber, PR8905 for OCP.	Power
		4	21	Change R2133 to 0R.	Set GPIO input level from 0.5V to 0V.	EE
		5	79	Remove EC7928.	Layout space limitation.	EE
	02/26	1	39,42	Empty R3906 and Change R4202 from 0R to 1KR.	It is for solving T8 shutdown issue.	EE
	03/03	1	60	Change SPK1 part number.	Request by ME.	ME
	03/05	1	20,24,37	Empty R2029,R2404,R3751.	Saving unused components.	EE

0303-1

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Title: Change notes

Size: A3 | Document Number: QUEEN AMD Muxless/UMA | Rev: X00

Date: Thursday, May 26, 2011 | Sheet 103 of 104