

MODEL NAME: *NAP10*
PCB NAME: *LA-5812P MB*
COMPAL P/N:

Dell/Compal confidential

Schematics Document

Phantom Calpella

Arrandale ULV BGA + Ibex PCH

DISCRETE VGA N11P-GS1 (Switchable Graphics)

2010-04-19

Rev: 1.0

Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>		
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				Custom	<i>LA-5812P</i>	1.0
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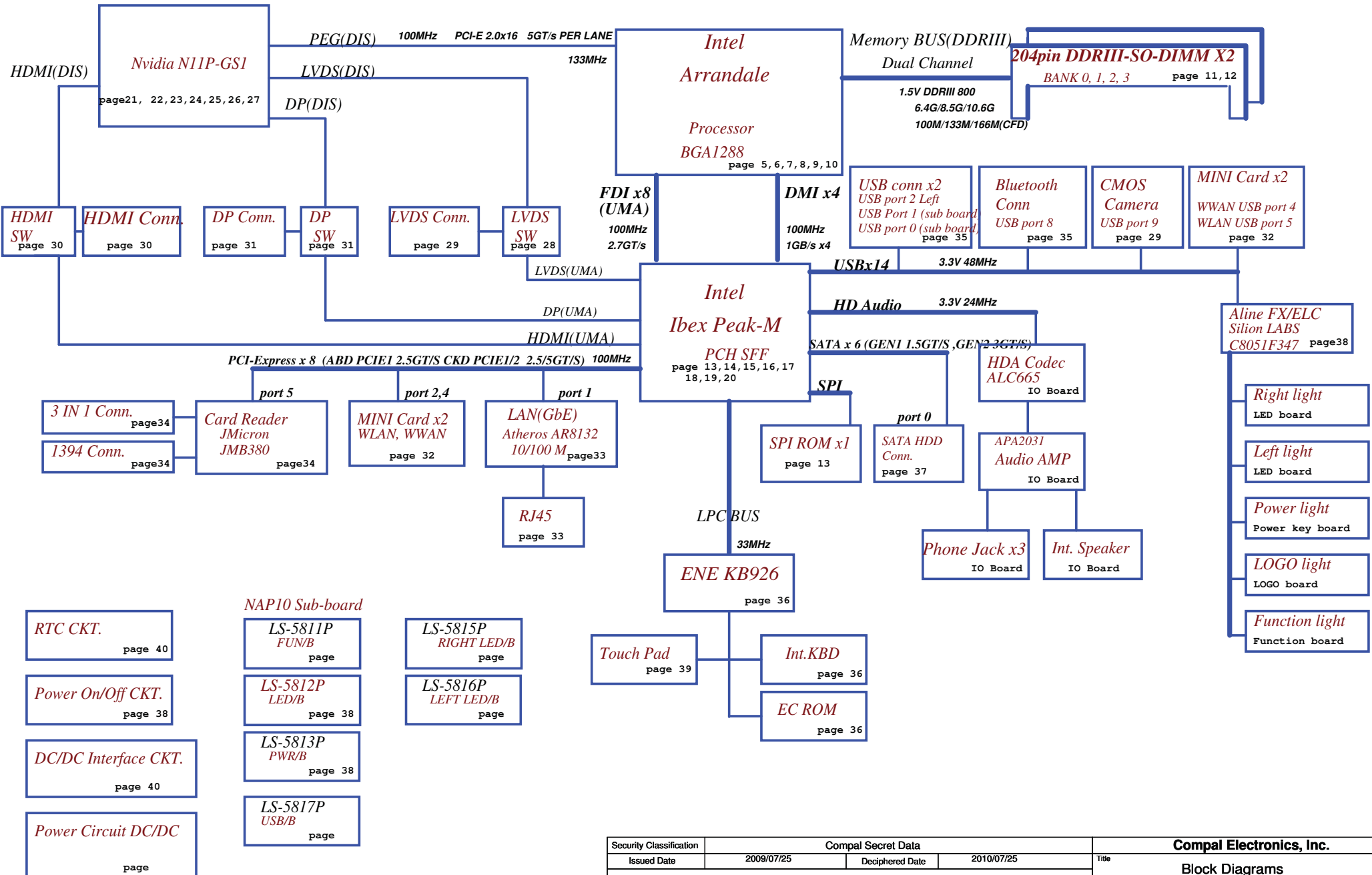
Compal Confidential

Model Name NAP10

File Name : LA5812P

Clock Generator
 IDT: 9LRS3199AKLFT
 SILEGO: SLG8SP587
 133/120/100/96/14.318MHZ to PCH
 27MHZ to N11P
 page 4

Fan Control
 page 37



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Voltage Rails (O MEANS ON X MEANS OFF)

power plane / State	B+	+5VALW +3VALW VL	+1.5V	+5VS +3VS +0.75VS +1.05VS +1.05VS_VTT +VCC_CORE +VCC_GFXCORE +1.5V_CPU_VDDQ +1.8VS +3VS_DELAY +1.8VSDGPU +1.05VSDGPU +1.5VSDGPU +VGA_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

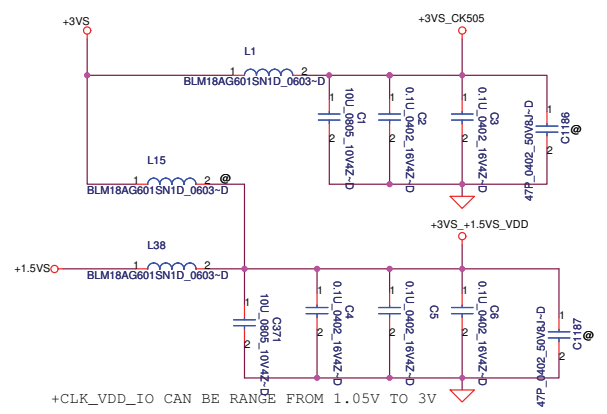
CONN@ : means ME part.

45@ : means install after SMT.

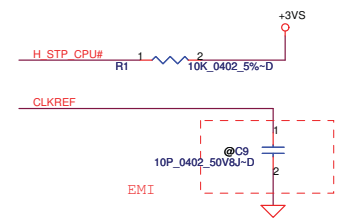
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
EC_SMB_CK1 EC_SMB_DA1	Battery	16 00010110
EC_SMB_CK2 EC_SMB_DA2	CPU THERMAL SENSOR (EMC1412A-1-ACZL)	F8 11111000
	CPU(PCH)INTERNAL THERMAL SENSOR	96 10010110
	CPU(PCH)INTERNAL THERMAL SENSOR	98 10011000
(PCH_SML1BCLK) (PCH_SML1DATA)	GPU THERMAL SENSOR (ADM1032ARMZ)	9A 10011010
	GPU INTERNAL THERMAL SENSOR	9E 10011110
	WWAN	
	WLAN	
PCH_SMBCLK PCH_SMBDATA	CLOCK GENERATOR (EXT.)	D2 11010010
	DDR Memory	
	Free Fall sensor	38 00111000

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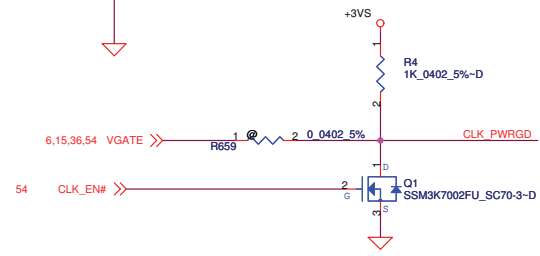
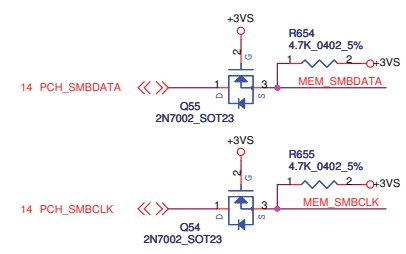
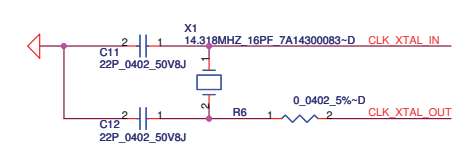
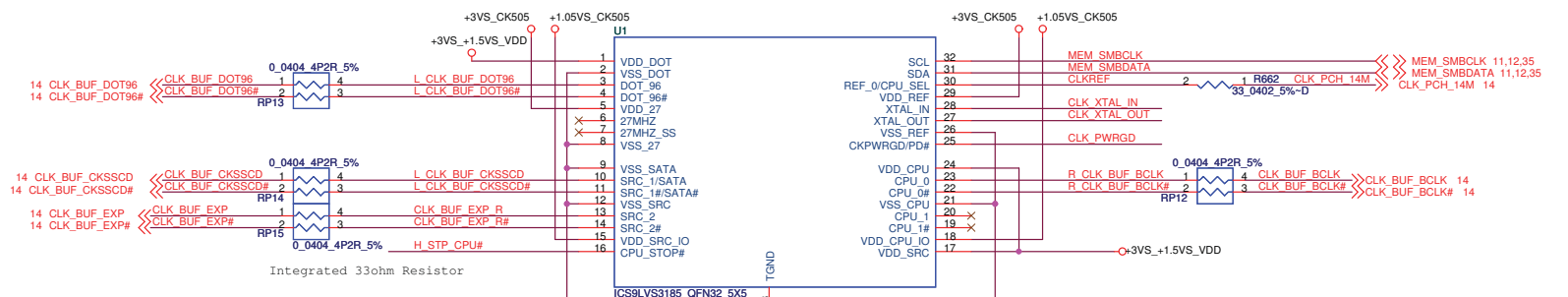
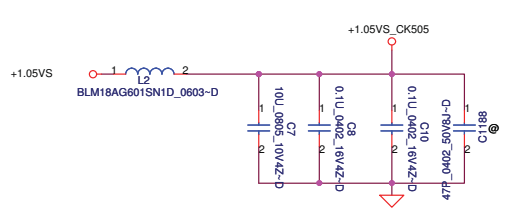
+CLK_VDD_IO CAN BE RANGE FROM 1.05V TO 3V



REF_O/CPU_SEL CLKREF

PIN 30	CPU0	CPU1
1 (0.7~1.5v)	100MHz	100MHz
0 (DEFAULT)	133MHz	133MHz

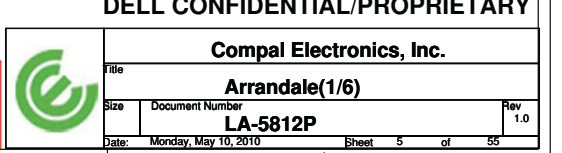
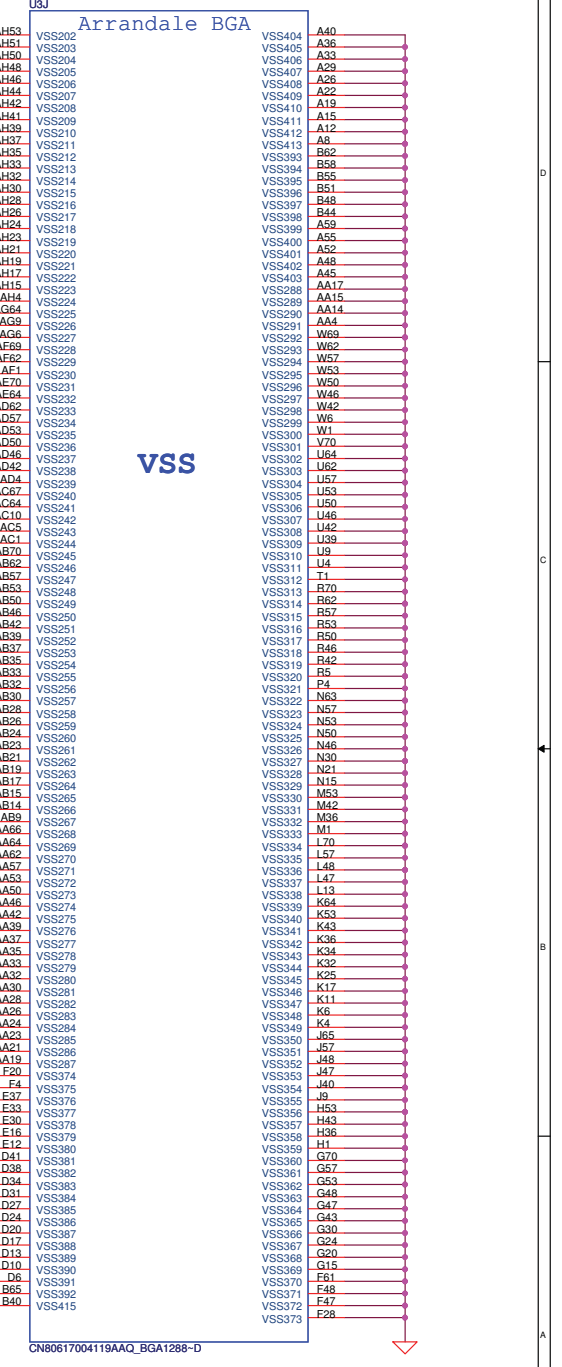
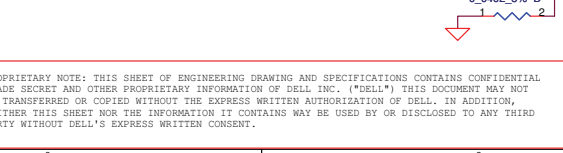
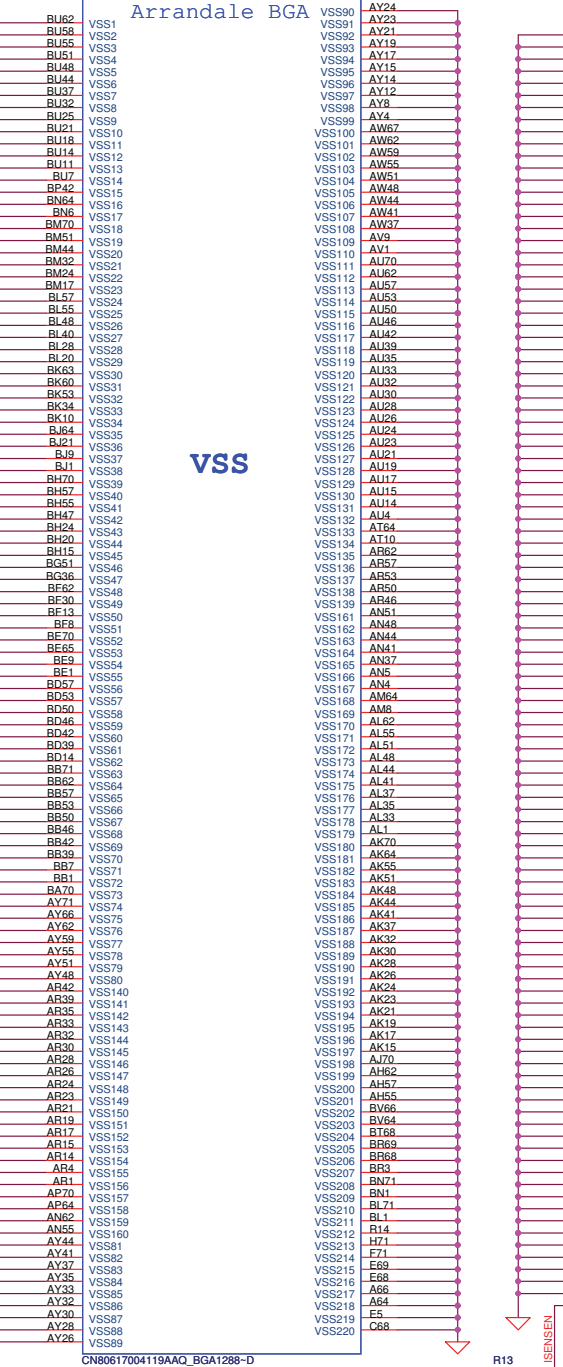
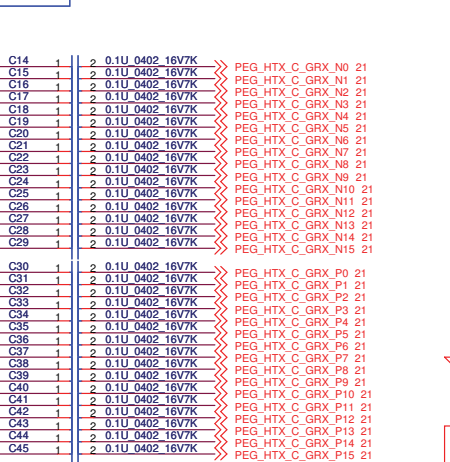
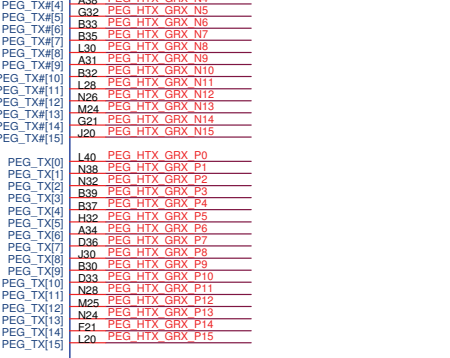
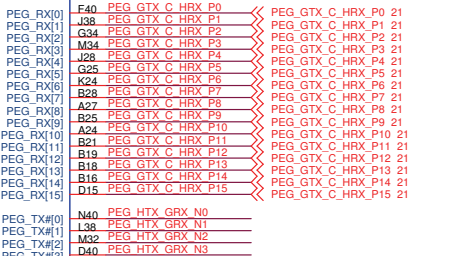
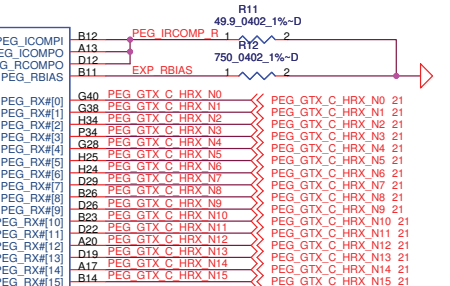
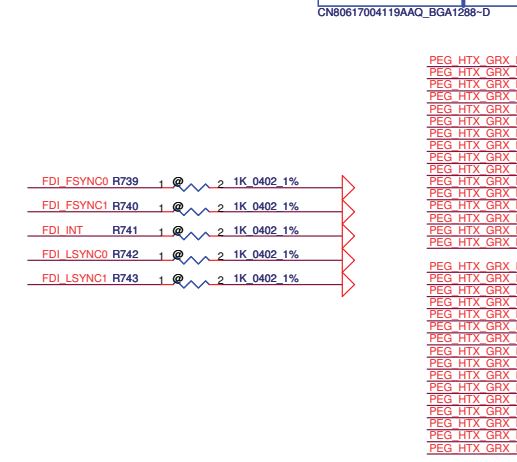
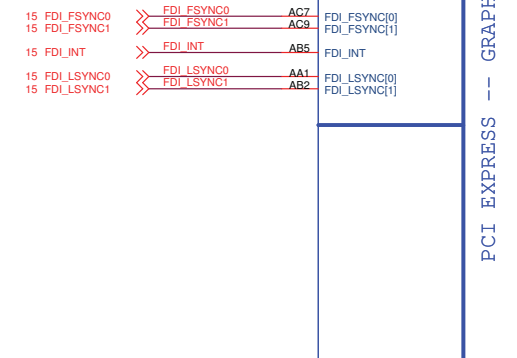
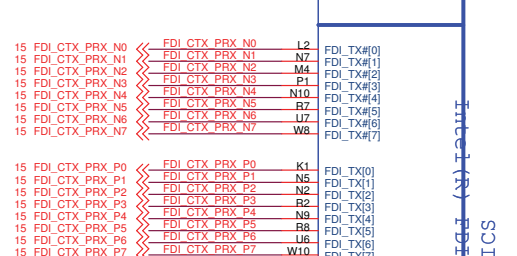
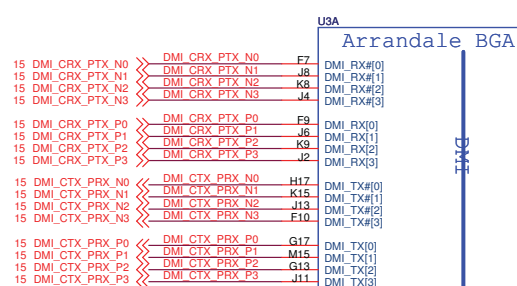
R8 4.7K_0402_5%-D
R10 10K_0402_5%-D



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Clock Generator			
LA-5812P	1.0		
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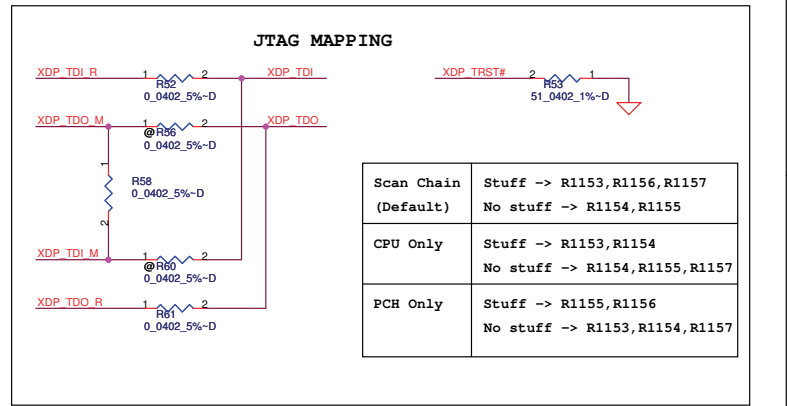
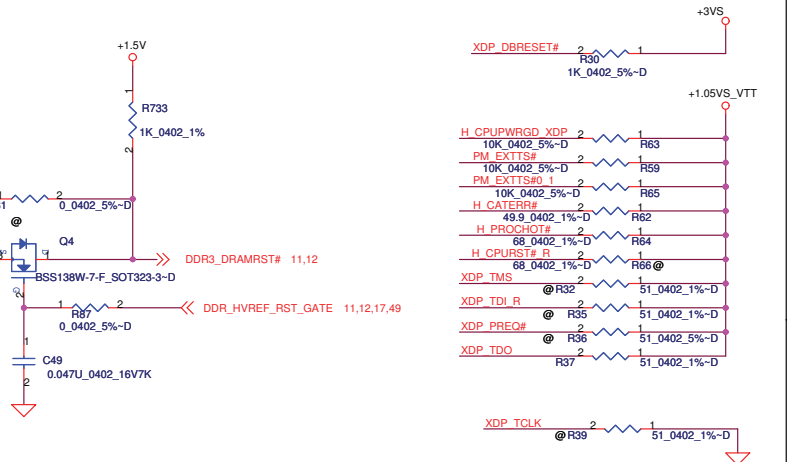
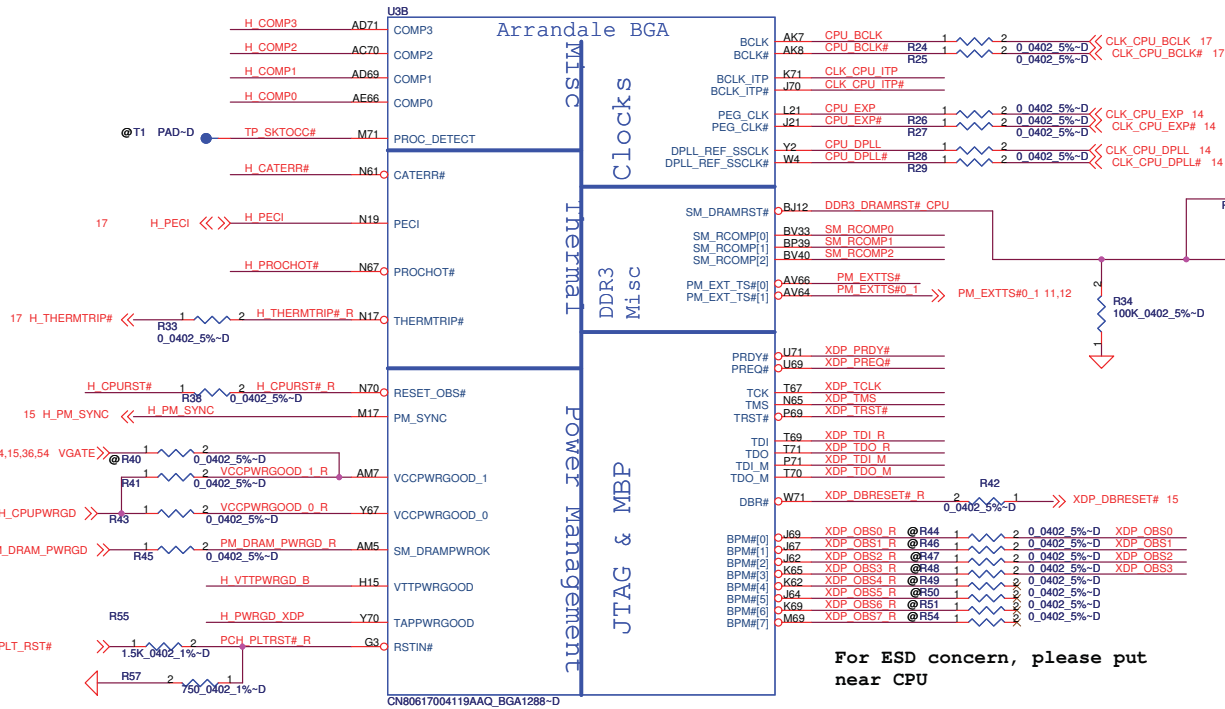
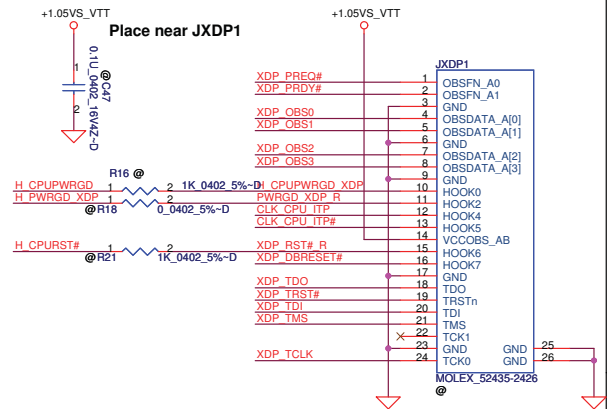
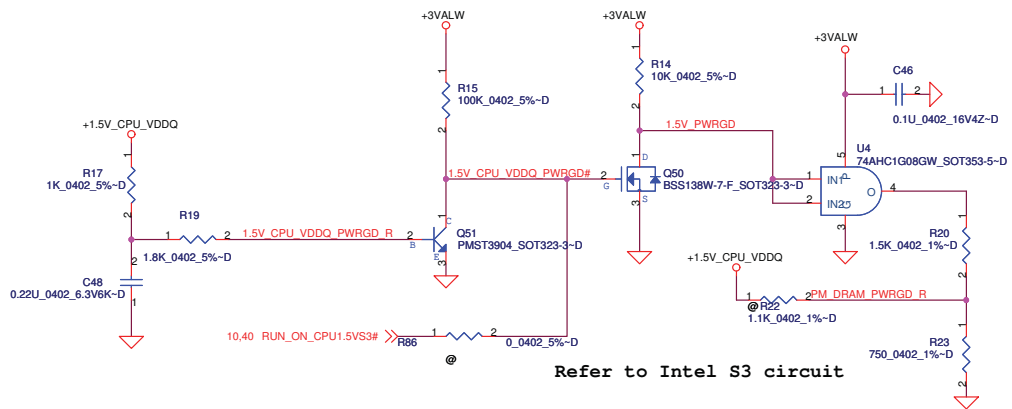
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Arrandale(1/6)

LA-5812P

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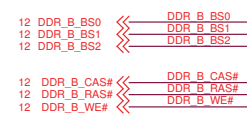
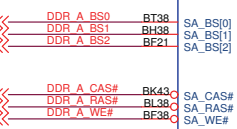
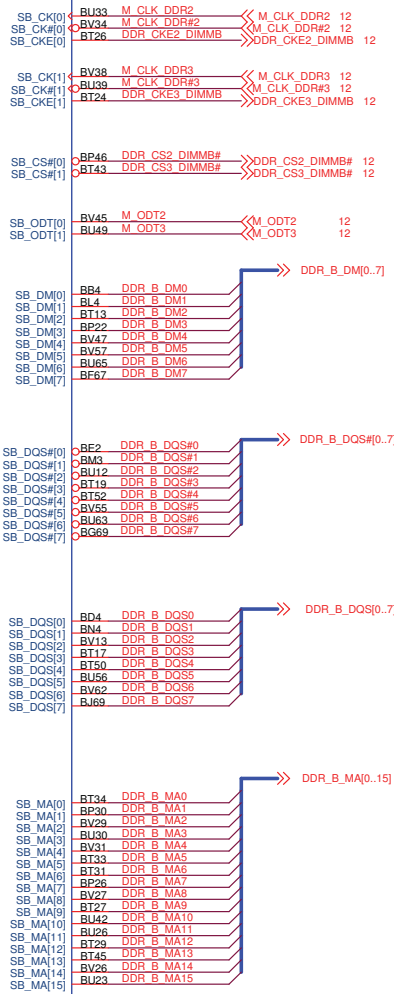
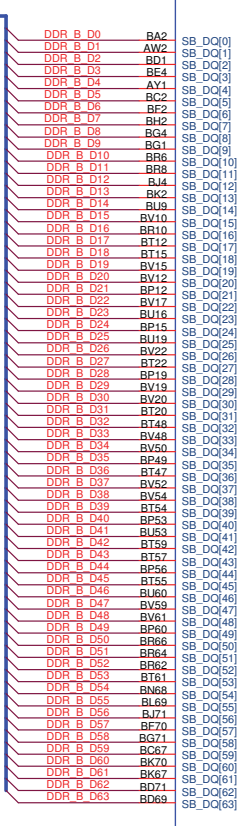
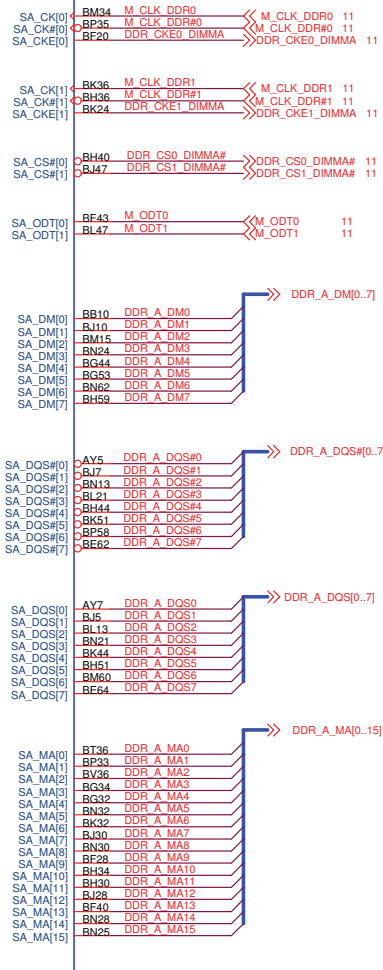
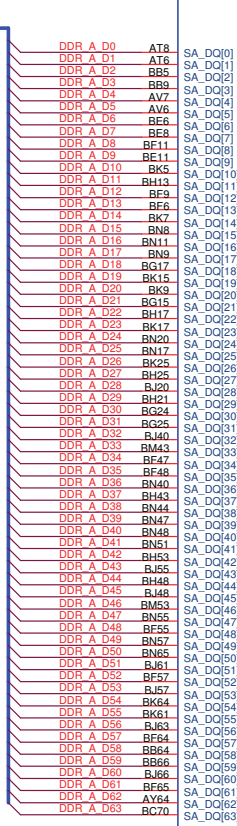
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U3C
Arrandale BGA

U3D
Arrandale BGA

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY - B



CN80617004119AAQ_BGA1288-D

CN80617004119AAQ_BGA1288-D

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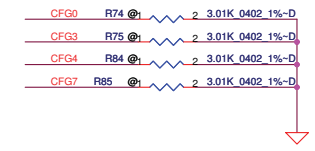
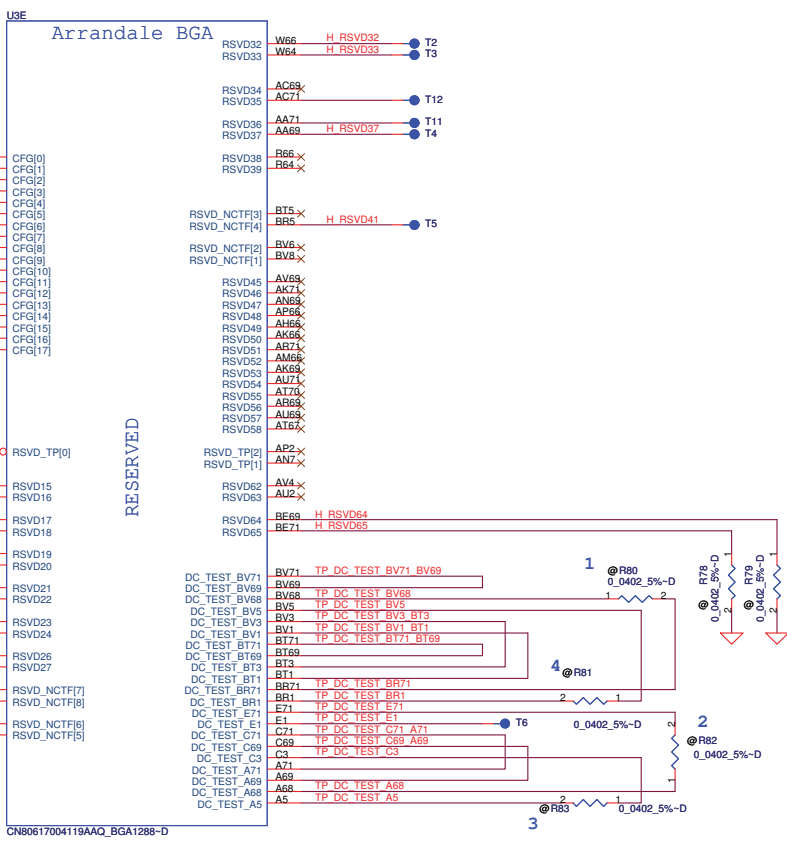
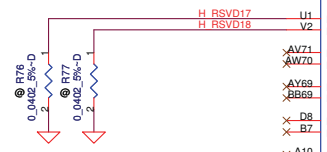
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Arrandale(3/6)

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Reserve VIA on PCB

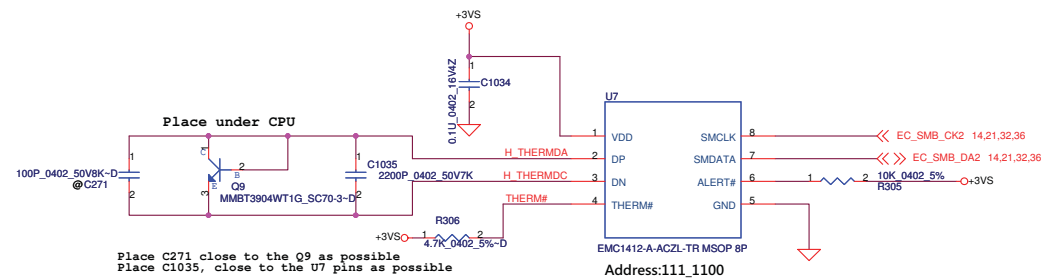


Margaux Intel review change to 3.3K ohm

PCI-Express Configuration Select	
CFG0	1 : Single PEG 0 : Bifurcation enable
PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Number Reversed 15->0, 14->1 ...
Display Port Presence	
CFG4 *	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

- Package Daisy Chain:**
- 1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68
 - 2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71
 - 3: A5 - pkg - C3
 - 4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5

CPU Thermal Sensor ADM1032ARMZ



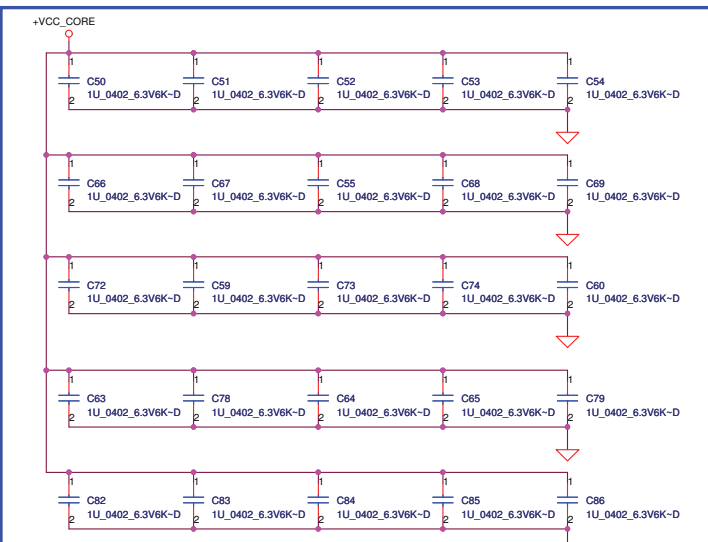
Place C271 close to the Q9 as possible
Place C1035, close to the U7 pins as possible

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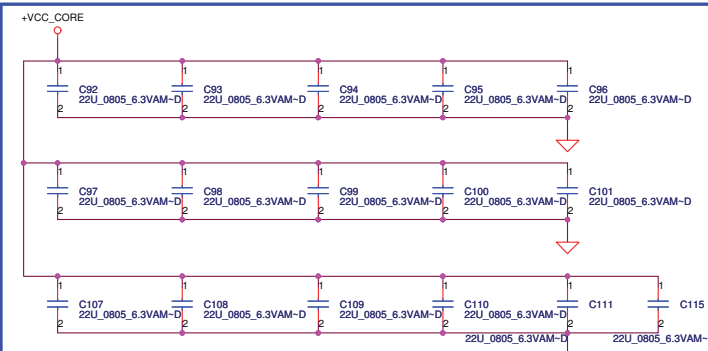
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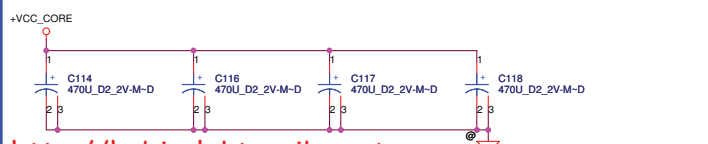
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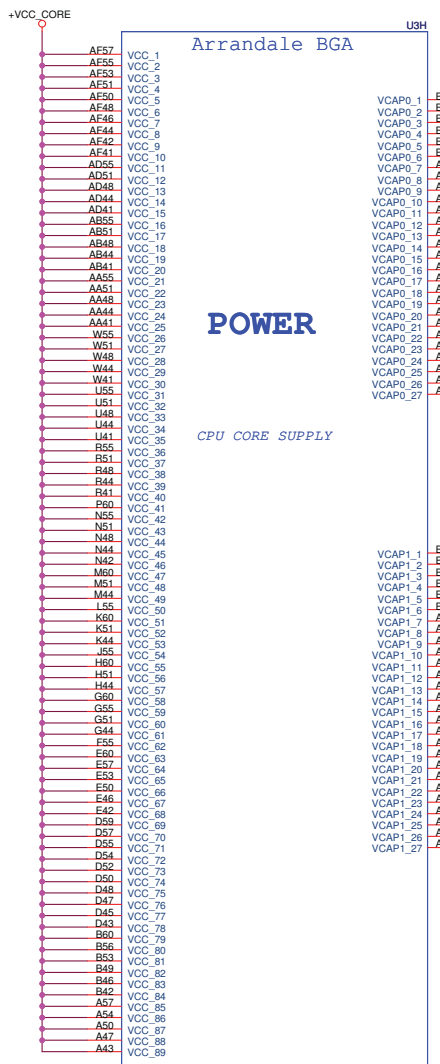
High-Frequency Decoupling 25x on Top Side



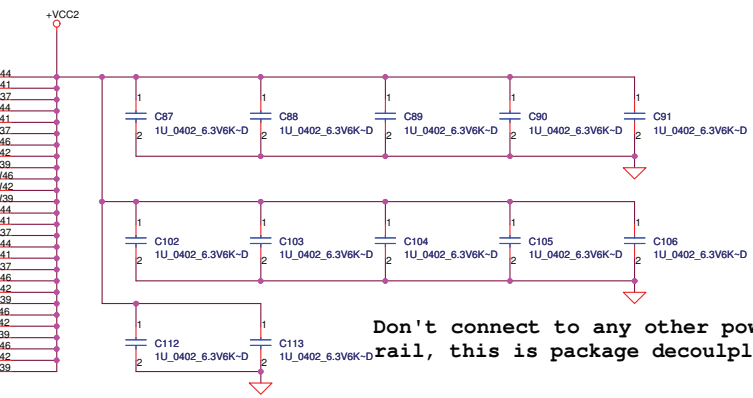
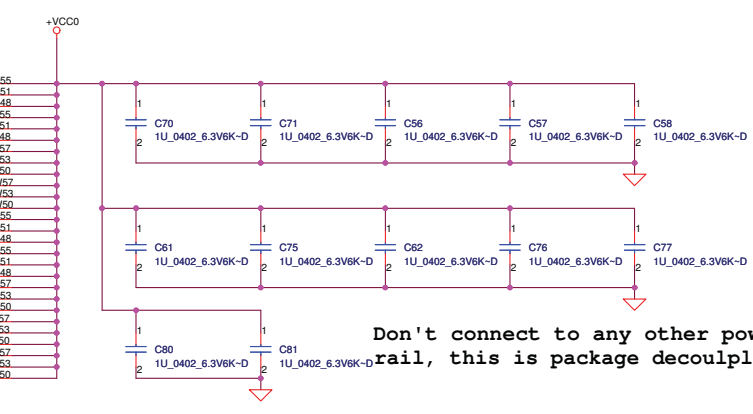
Mid-Frequency Decoupling 15x on Bottom Side between inductors and package



Current = 48A



CN80617004119AAQ_BGA1288-D



PROCESSOR Power Rail Table (EDS V1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VXNG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

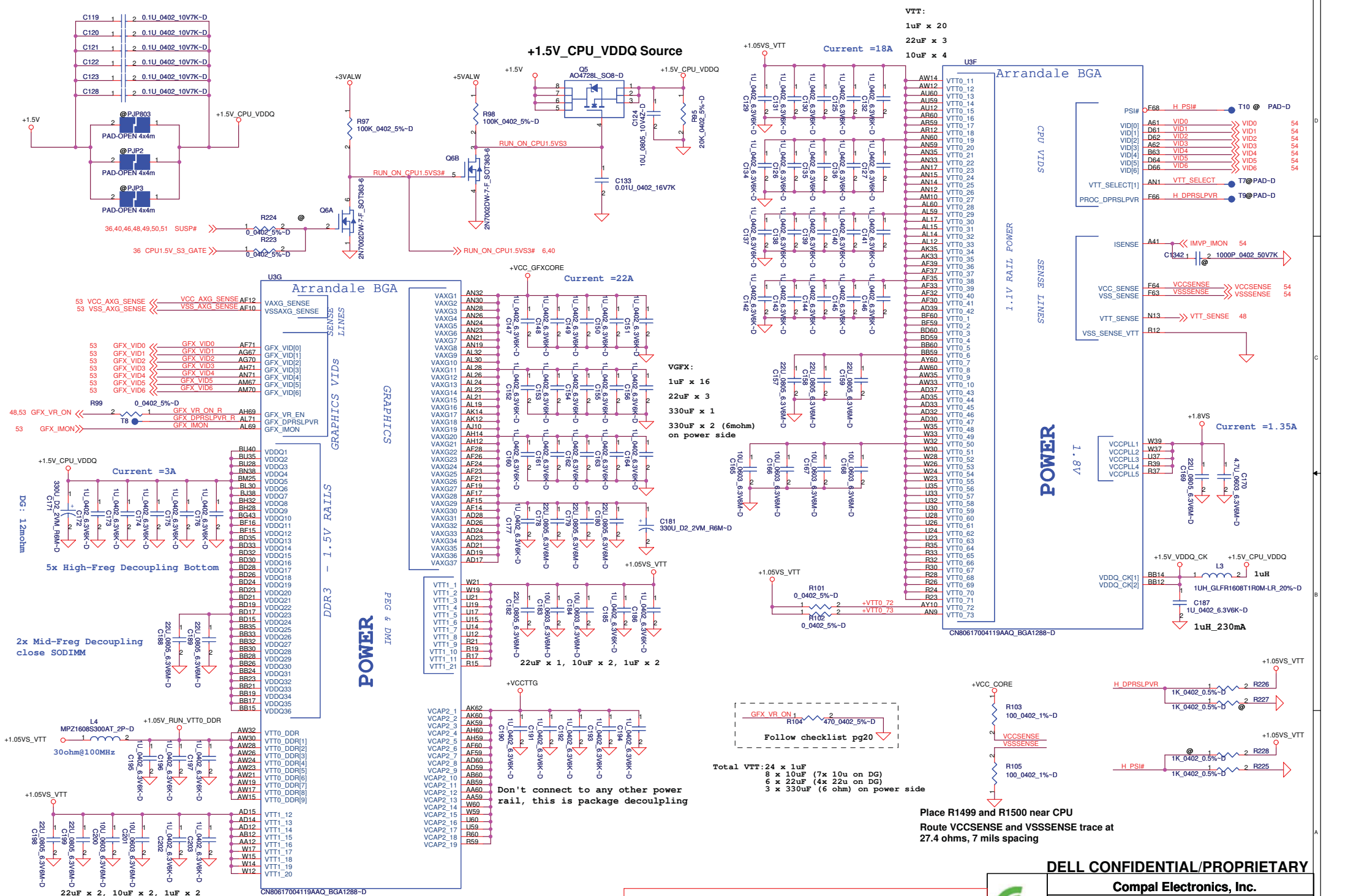
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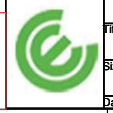
Arrandale(5/6)

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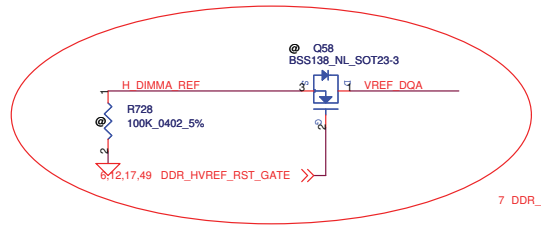
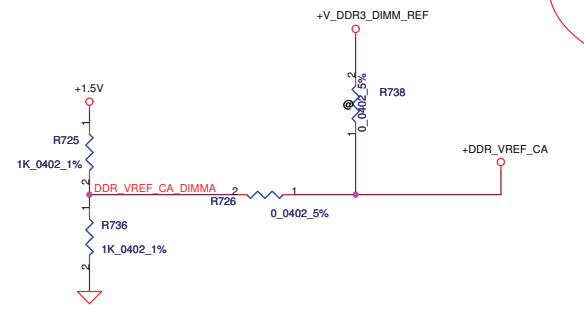
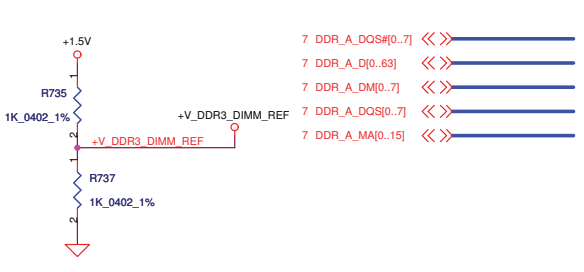


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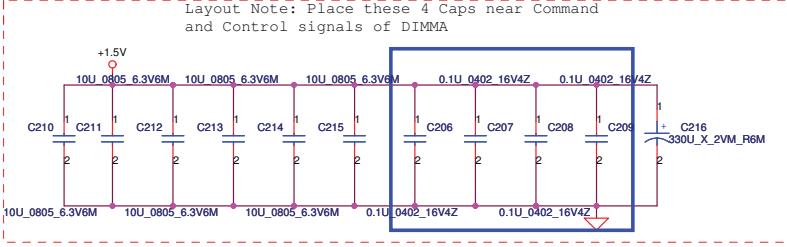


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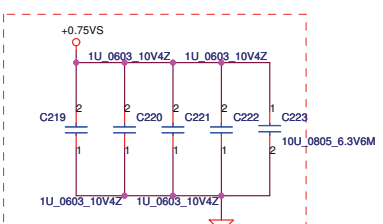
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Arrandale(6/6)			
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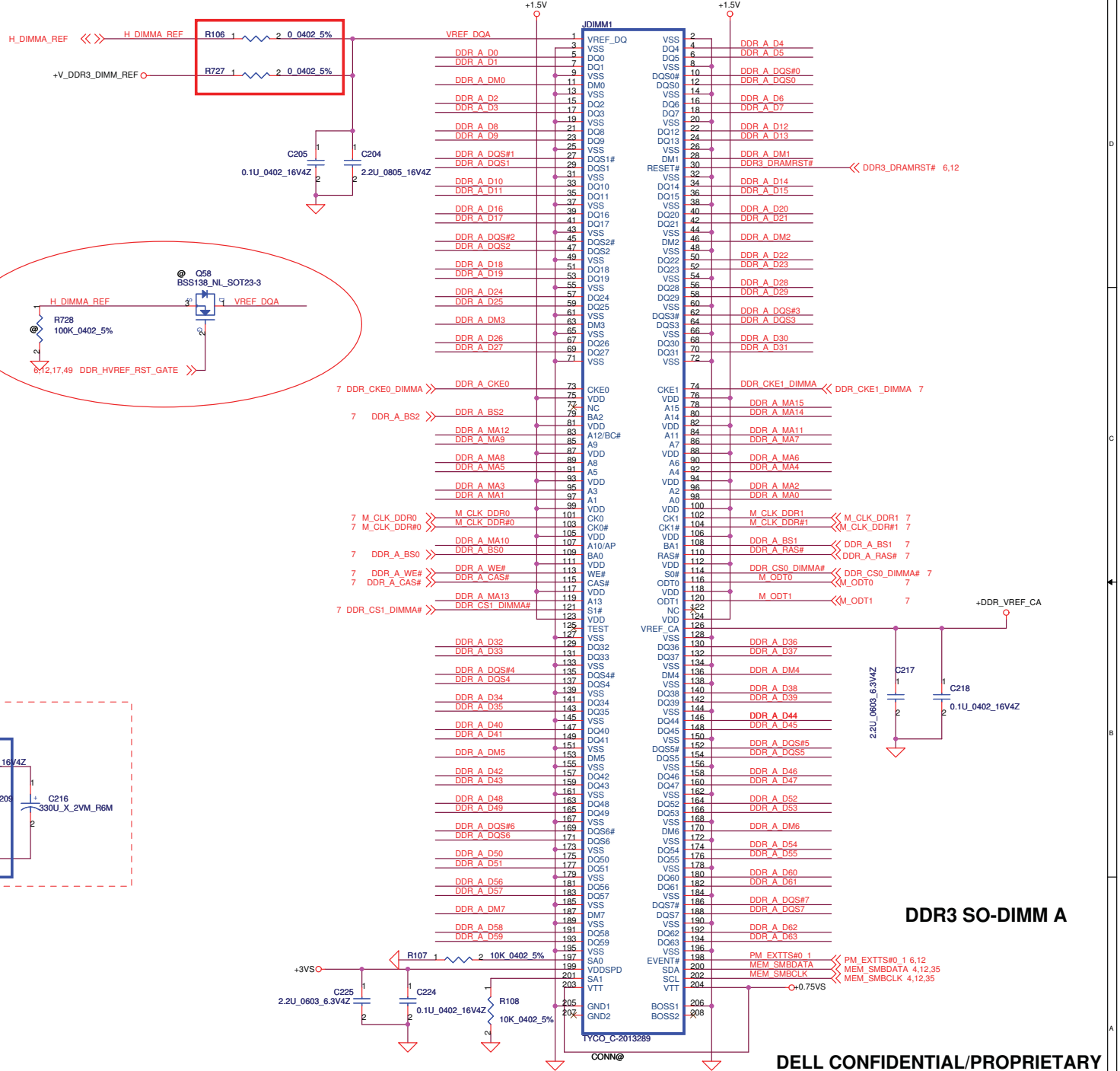
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



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DDR3 SO-DIMM A

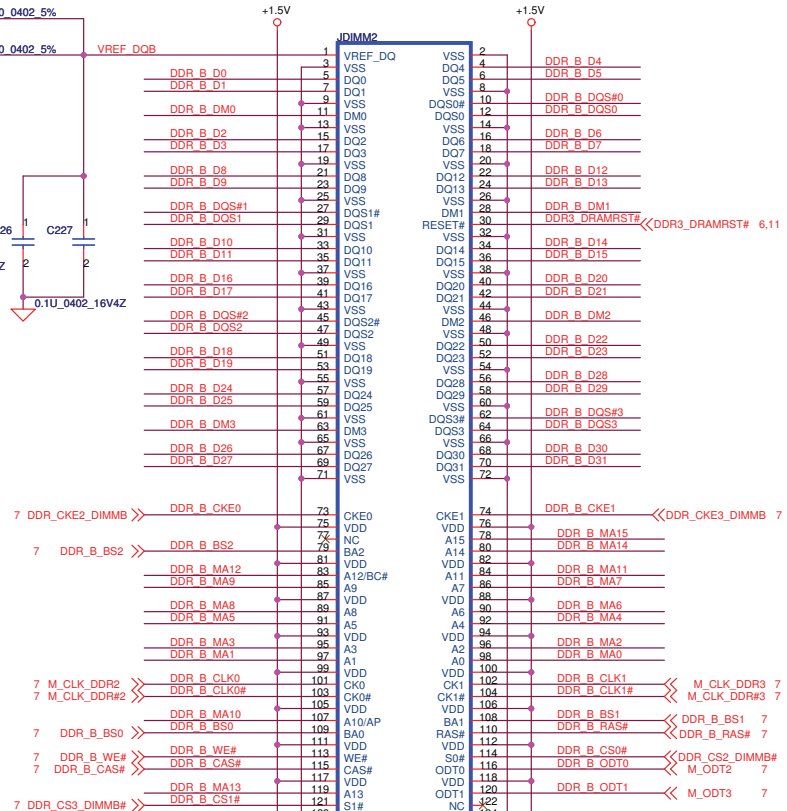
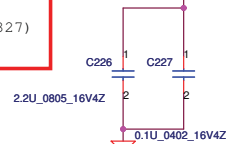
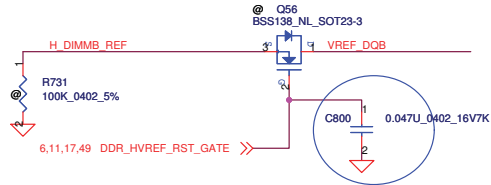
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				DDR3-SODIMM SLOT1	
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- 7 DDR_B_DQS#[0..7] <<>>
- 7 DDR_B_DQ[0..63] <<>>
- 7 DDR_B_DM[0..7] <<>>
- 7 DDR_B_DQS[0..7] <<>>
- 7 DDR_B_MA[0..15] <<>>

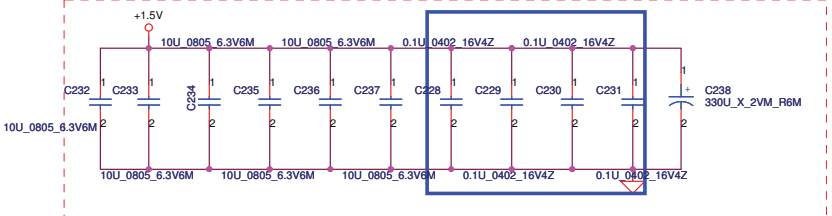
2008/9/8 #400755
 Calpella Clarksfield
 DDR3 SO-DIMM
 VREFDQ Platform
 Design Guide Change Details

2009/04/13
 For Arrandale ,it should be use M1 Circuit (pop R328)
 For Clarksfield ,it should be use M3 Circuit (pop R327)
 DG V1.52

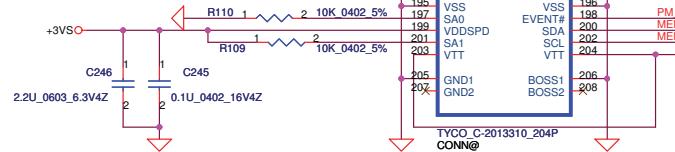
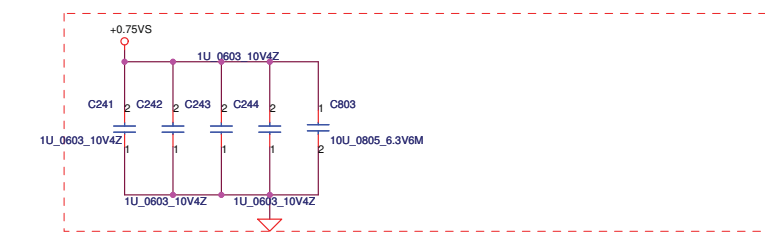


Layout Note:
 Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
 Place near JDIMM2.203 & JDIMM2.204



DDR3 SO-DIMM B

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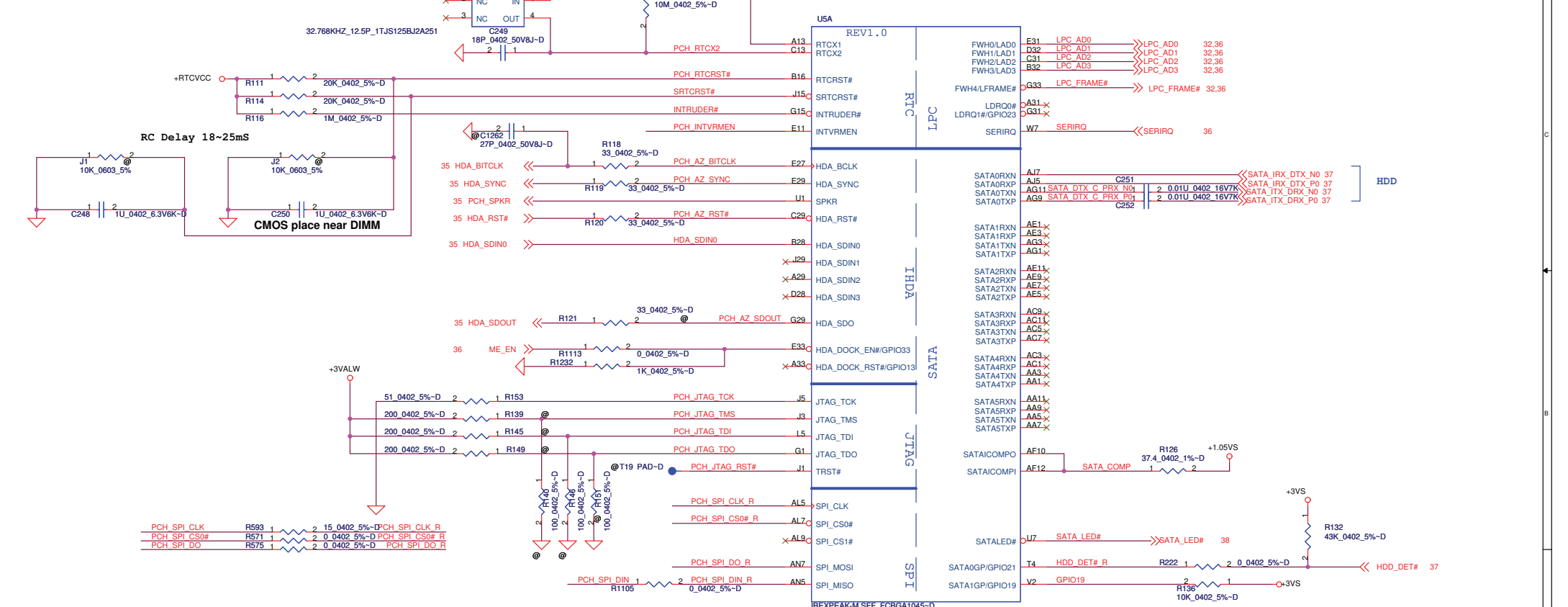
Security Classification	Compal Secret Data		Title	
Issued Date	2009/5/12	Deciphered Date	2010/04/15	MEM_EXTTSH#0_1 6,11 MEM_SMBDATA 4,11,35 MEM_SMBCLK 4,11,35
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Compal Electronics, Inc. DDR3II-SODIMM SLOT2 LA-5812P Rev 1.0
Date: Monday, May 10, 2010				Sheet 12 of 55

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

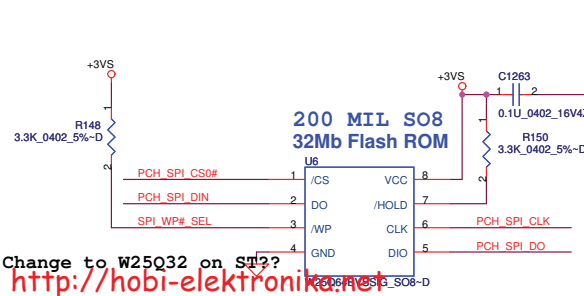
ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable Internal VRs

On Die PLL VR is supplied by
1.5V when sampled high, 1.8 V when sampled low



No Reboot Strap	
SPKR	Low = Default
	High = No Reboot



PCH Pin	Ref.	PCH JTAG Enable		PCH JTAG Disable		Production
		ES1	ES2	ES1	ES2	
TDO	R149	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R151	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R139	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R140	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R145	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R146	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R153	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm
		20K ohm	20K ohm	No Stuff	No Stuff	No Stuff
TRST#		10K ohm	10K ohm	No Stuff	No Stuff	No Stuff



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PCH (1/8)	
File	
Size	Document Number
	LA-5812P
Date	Monday, May 10, 2010
Sheet	13 of 55
Rev	1.0

Change to W25Q32 on ST??
<http://hobi-elektronika.net>

For PCIE LAN

33 PCIE_IRX_LANTX_N1
33 PCIE_IRX_LANTX_P1
33 PCIE_ITX_LANRX_N1
33 PCIE_ITX_LANRX_P1

For Wireless LAN

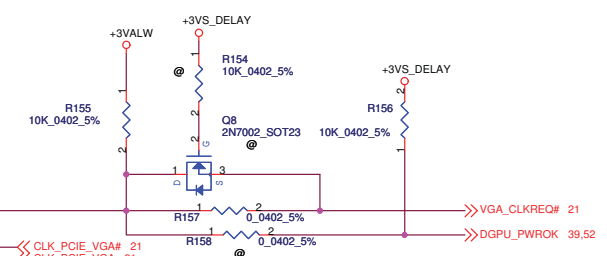
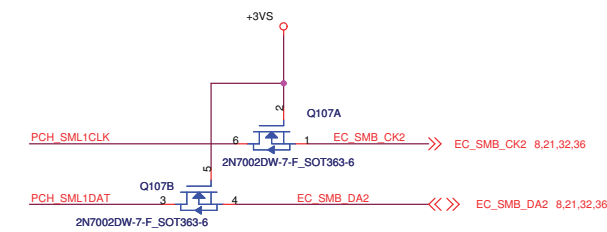
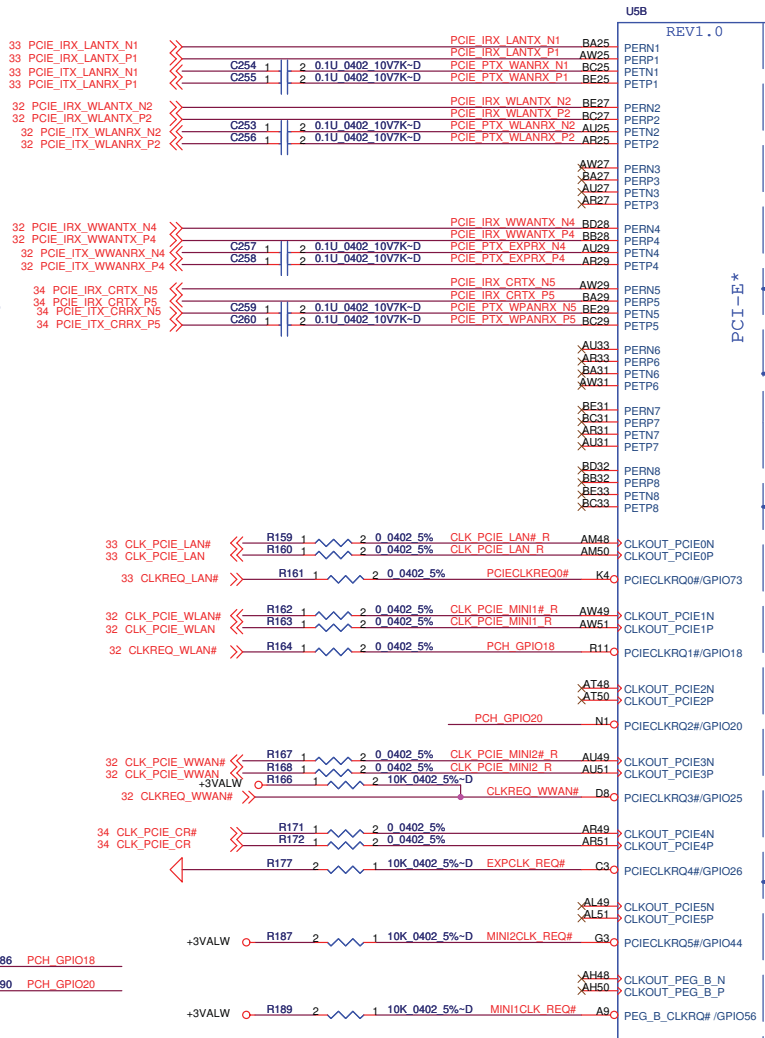
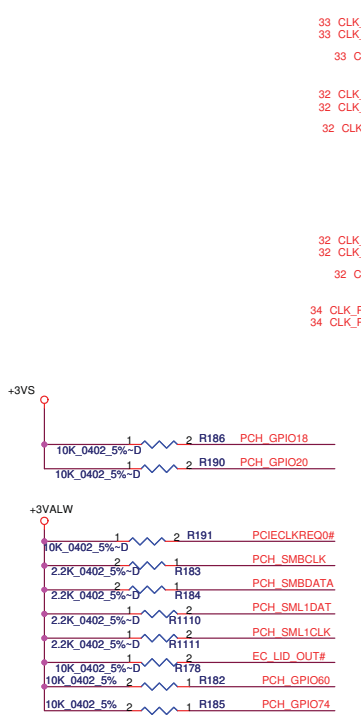
32 PCIE_IRX_WLANTX_N2
32 PCIE_IRX_WLANTX_P2
32 PCIE_ITX_WLANRX_N2
32 PCIE_ITX_WLANRX_P2

For WWAN

32 PCIE_IRX_WWANTX_N4
32 PCIE_IRX_WWANTX_P4
32 PCIE_ITX_WWANRX_N4
32 PCIE_ITX_WWANRX_P4

For 1394/Card Reader

34 PCIE_IRX_CRTX_N5
34 PCIE_IRX_CRTX_P5
34 PCIE_ITX_CRRX_N5
34 PCIE_ITX_CRRX_P5



Project ID		
ID1	ID0	Project
1	0	
1	1	

Project Port ID

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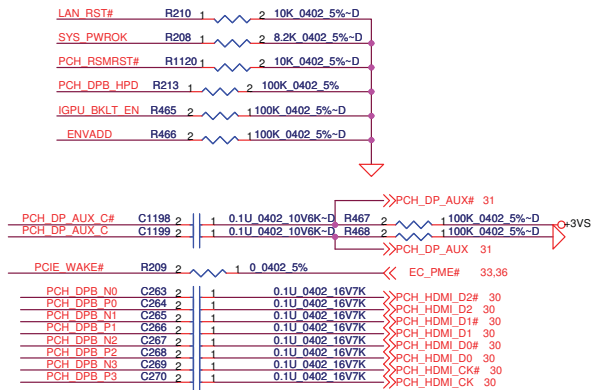
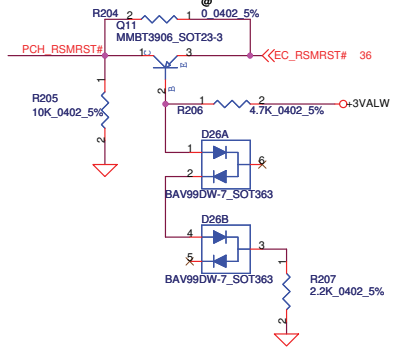
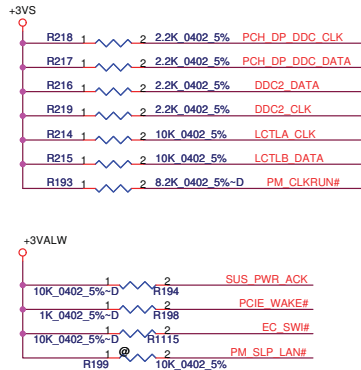
Compal Electronics, Inc.

PCH (2/8)

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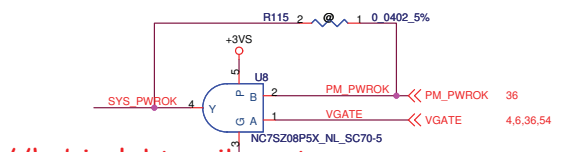
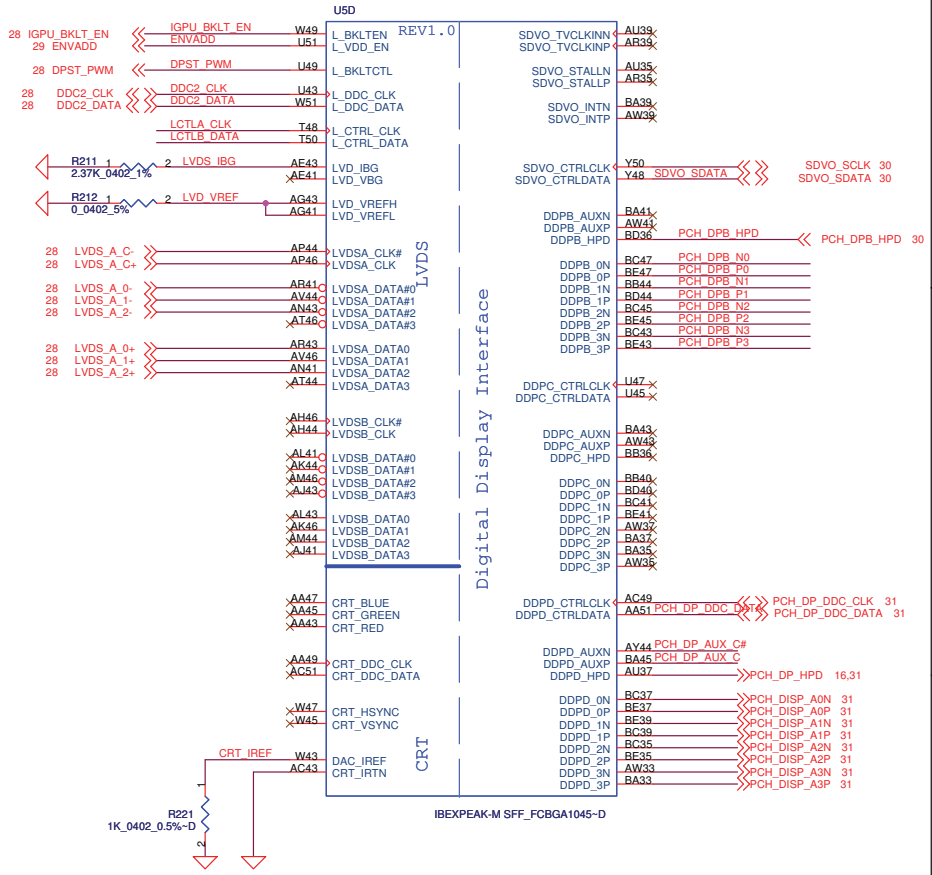
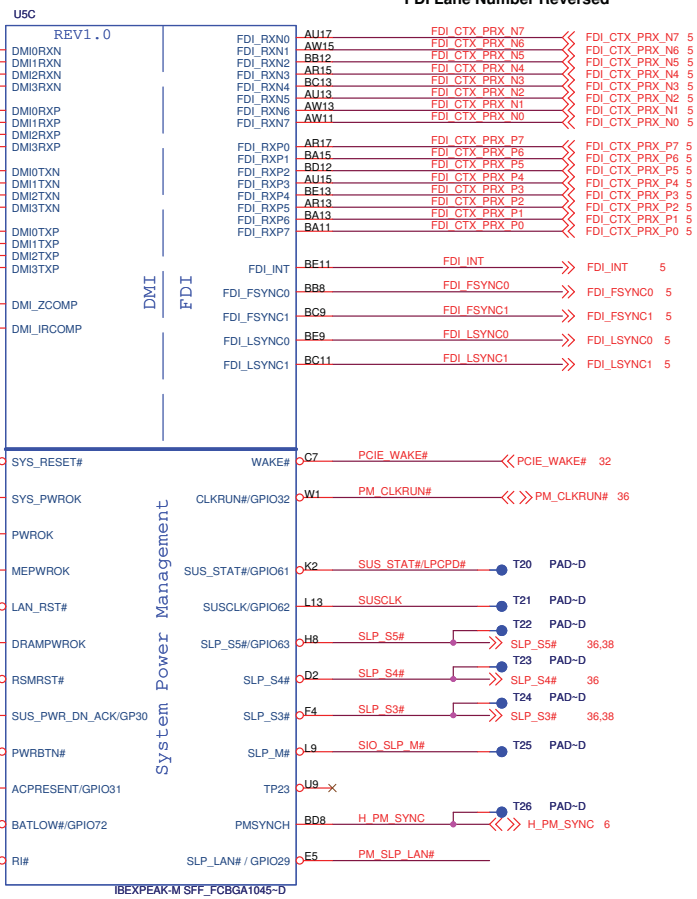
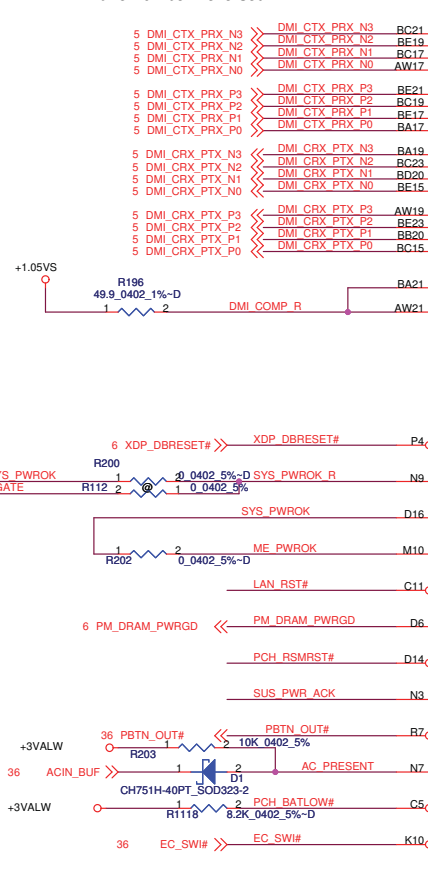
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Date: Monday, May 10, 2010 Sheet: 14 of 55



DMI Lane Number Reversed

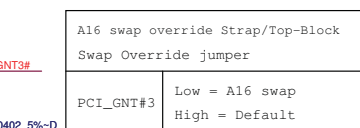
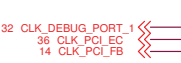
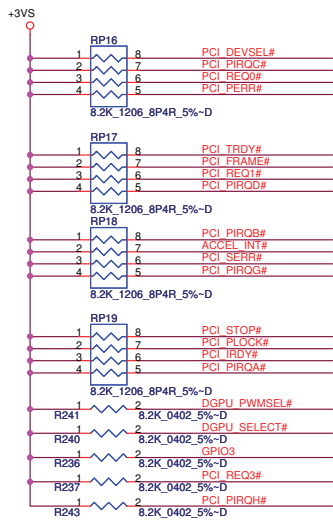
FDI Lane Number Reversed



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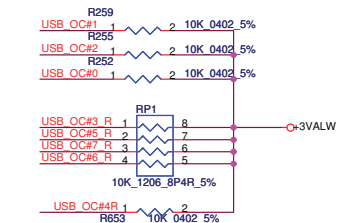
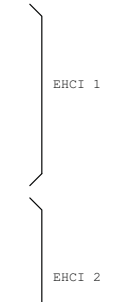
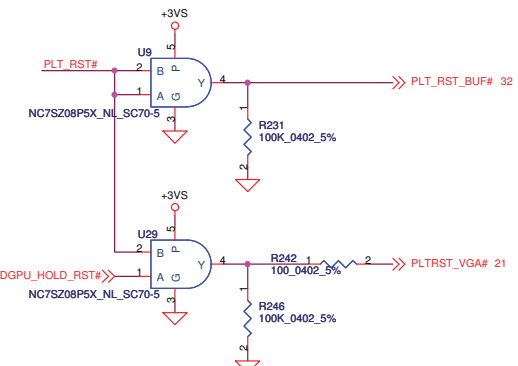
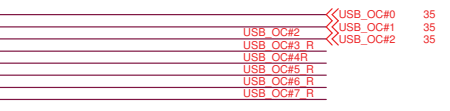
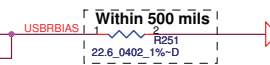
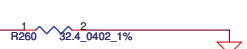
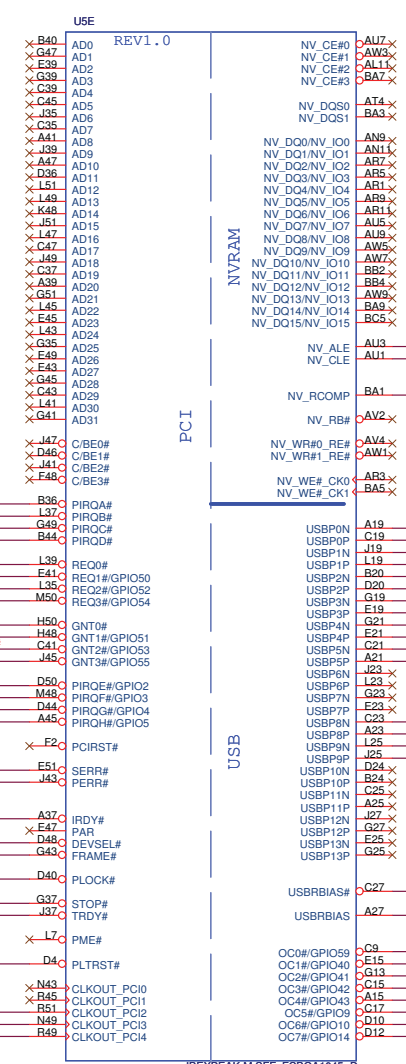
Compal Electronics, Inc.	
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File	
Size	Document Number
	LA-5812P
Date	Monday, May 10, 2010
Sheet	15 of 55
	Rev 1.0

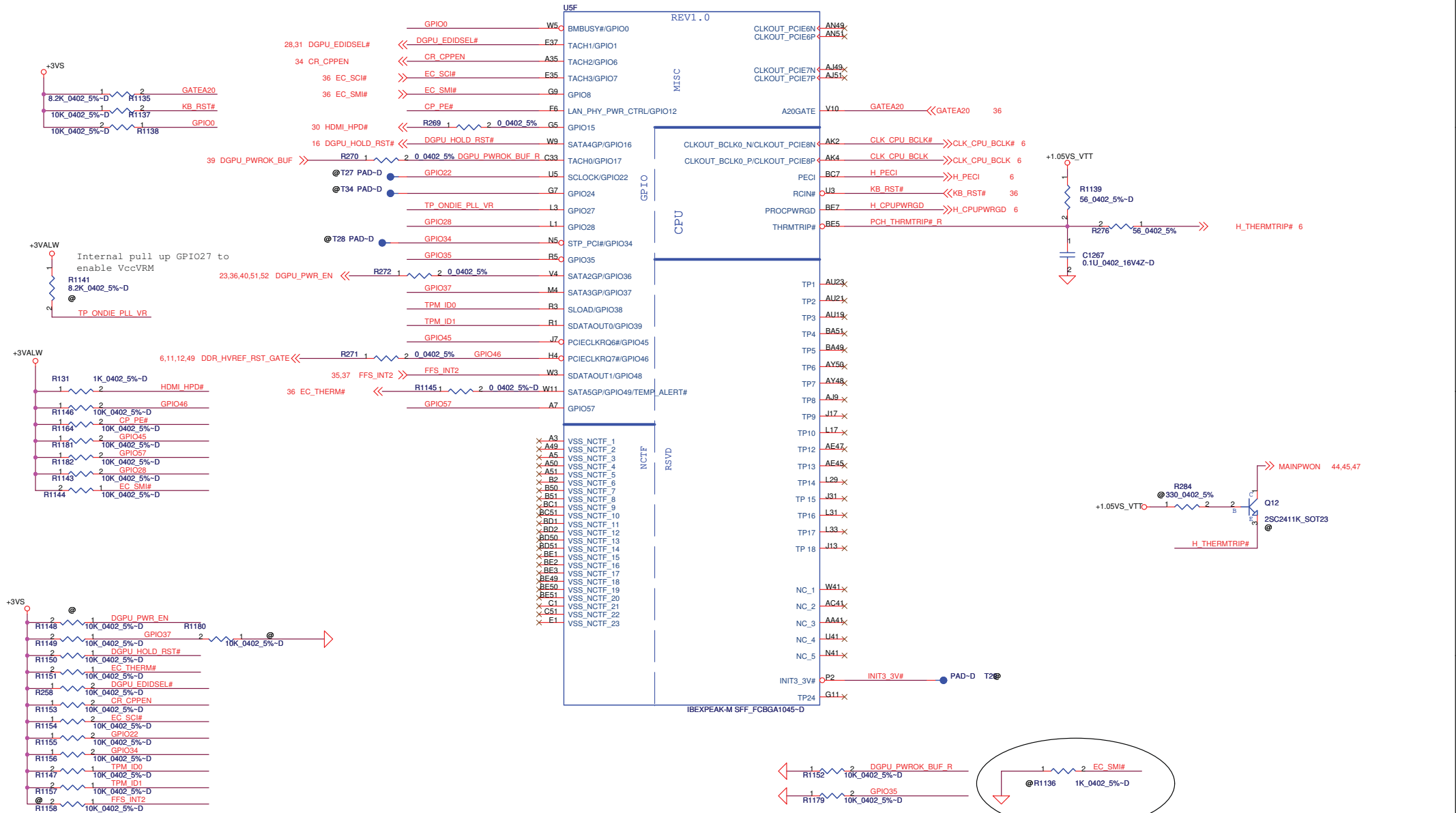


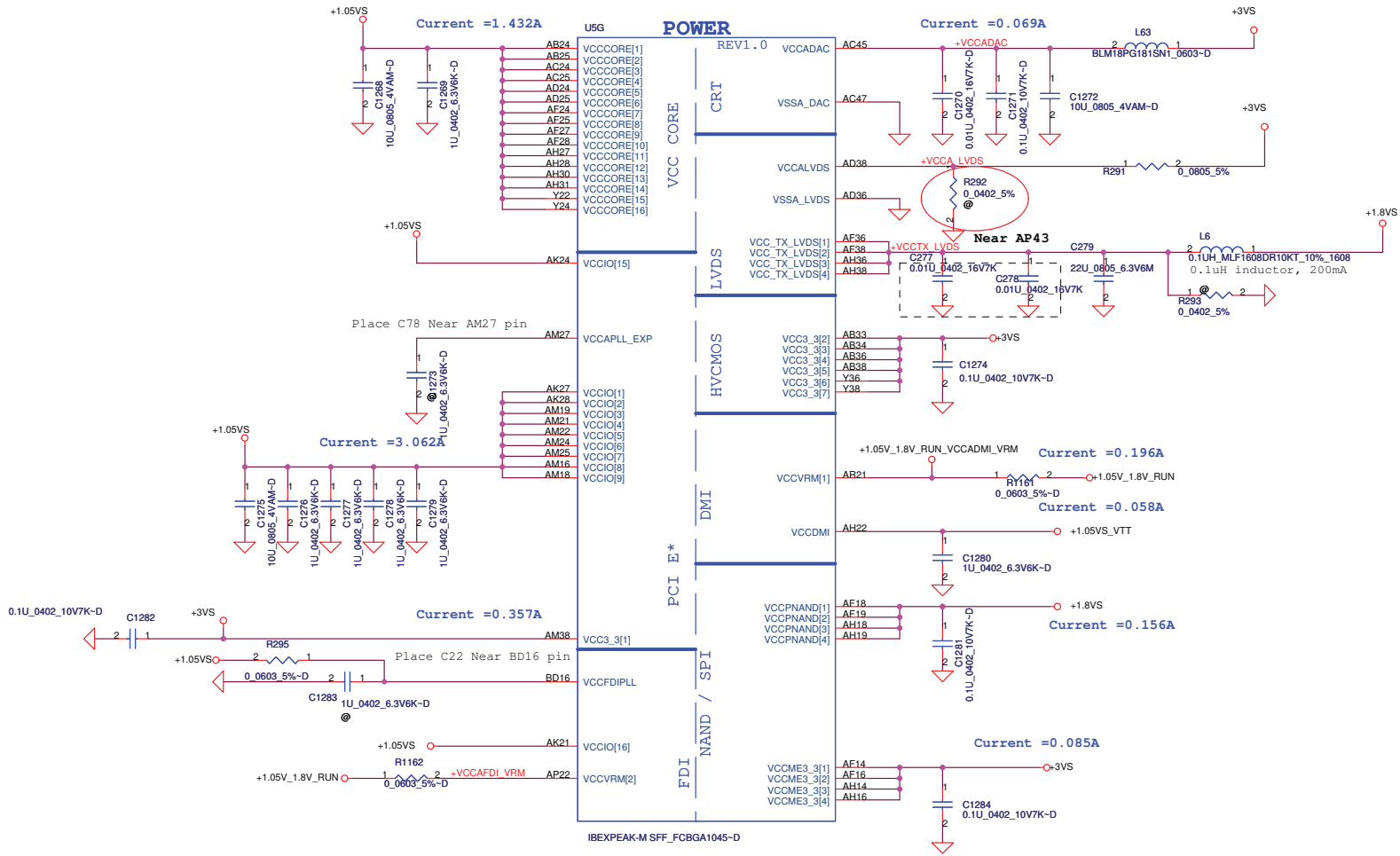
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap
PCI_GNT#3	High = Default

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

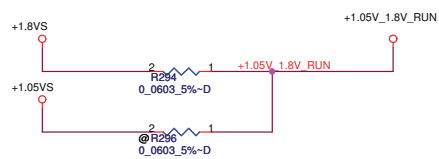
Danbury Technology Enabled	
NV_ALE	High = Enabled (Default) Low = Disabled
DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH







PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_CPU_IO	1.1/1.05	< 1 (mA)
V5REF	5	< 1 (mA)
V5REF_Sus	5	< 1 (mA)
Vcc3_3	3.3	0.357
VccAC1k	1.1	0.052
VccADAC	3.3	0.069
VccADPLLA	1.1	0.068
VccADPLLB	1.1	0.069
Vccap11EXP	1.1	0.04
VccCore	1.1	1.432
VccDMI	1.1	0.058
VccDMI	1.1	0.061
VccFDIPLL	1.1	0.037
VccIO	1.1	3.062
VccLAN	1.1	0.32
VccME	1.1	1.849
VccME3_3	3.3	0.085
VccpNAND	1.8	0.156
VccSATAPLL	1.1	0.031
VccSus3_3	3.3	0.163
VccSusHDA	3.3	0.006
VccVRM	1.8 / 1.5	0.196
VccALVDS	3.3	< 1 (mA)
VccTX_LVDS	1.8	0.059

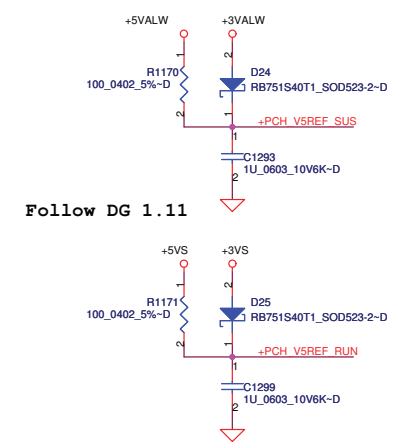
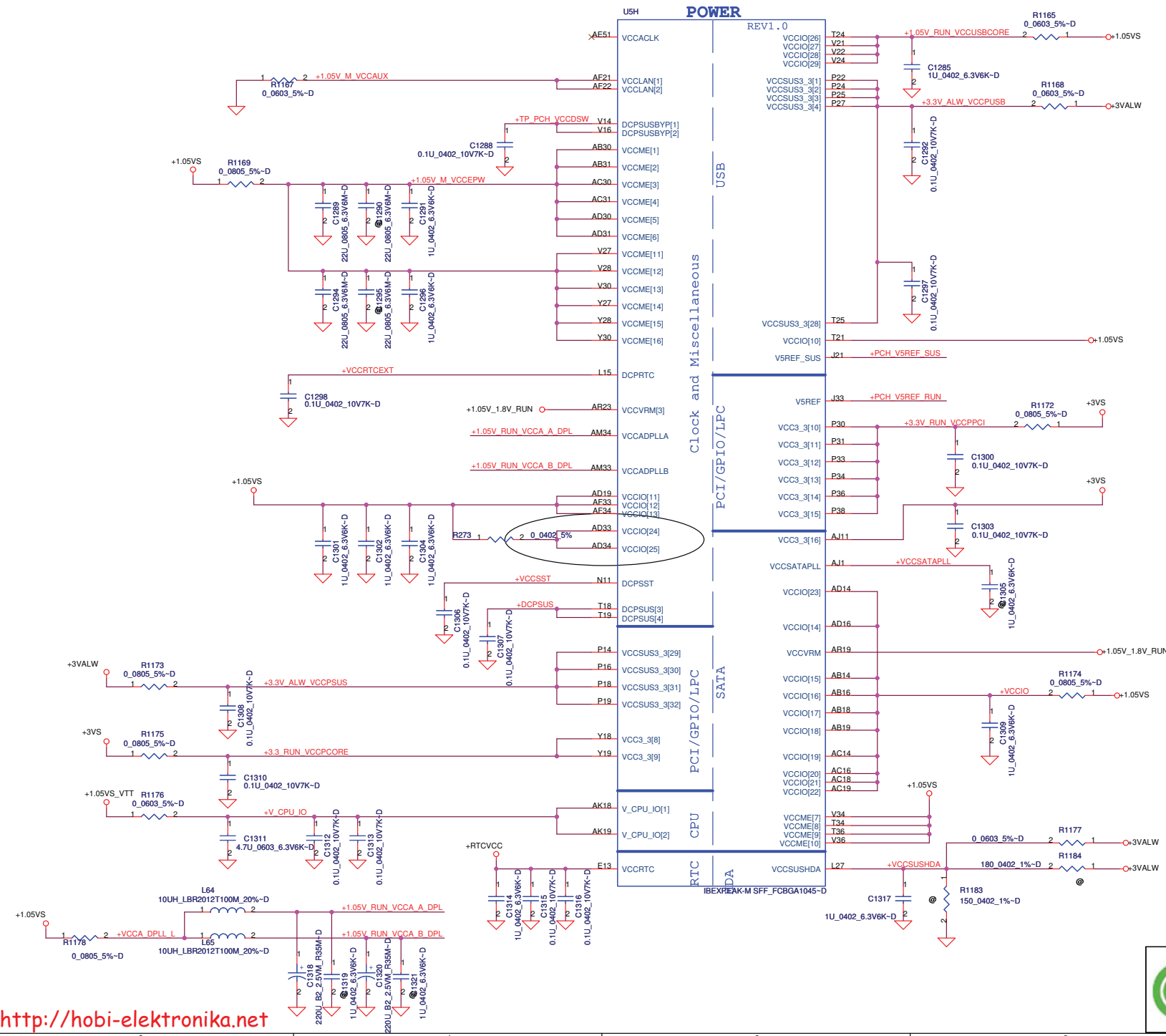


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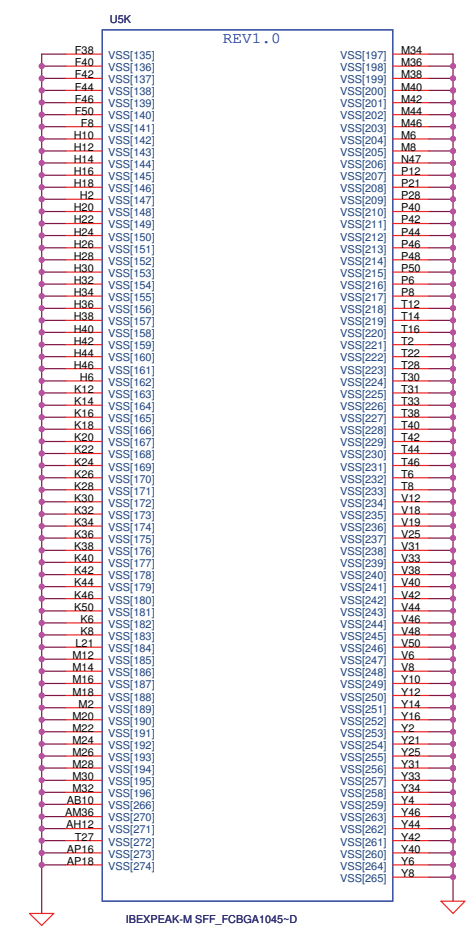
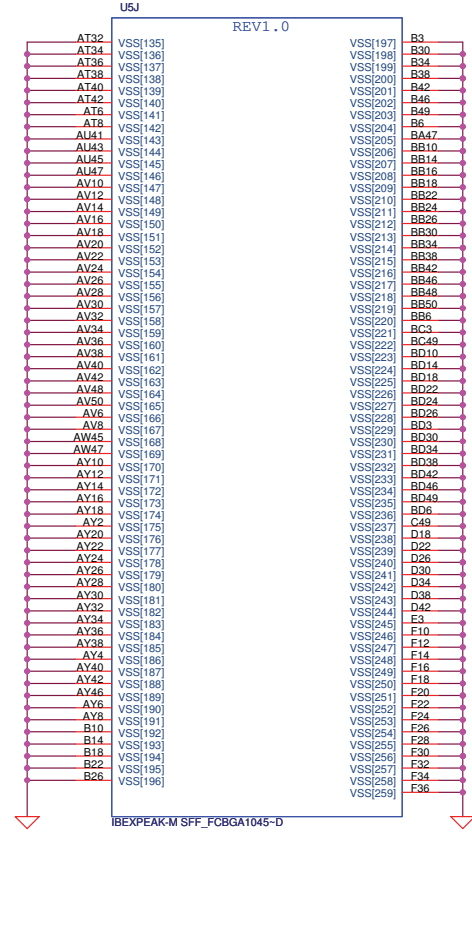
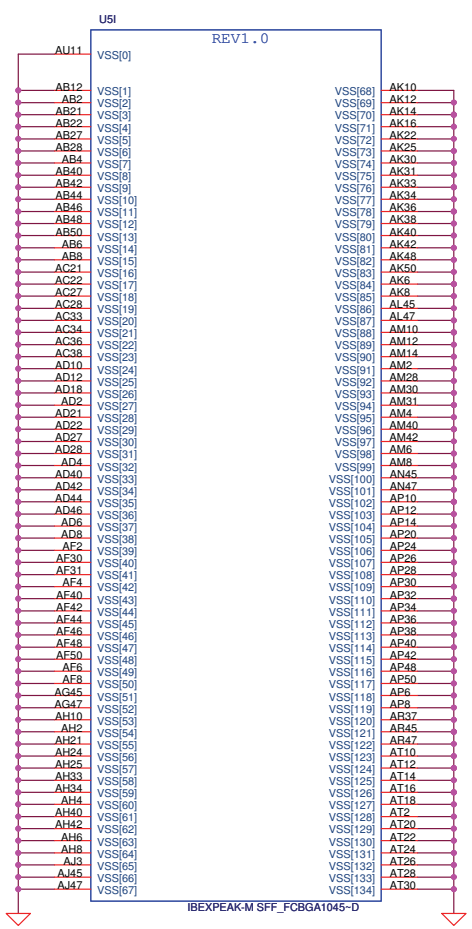
Compal Electronics, Inc.



File		PCH (6/8)		Rev	1.0
Size	Document Number	LA-5812P		Date	Monday, May 10, 2010
Date		Monday, May 10, 2010	Sheet	18	of 55

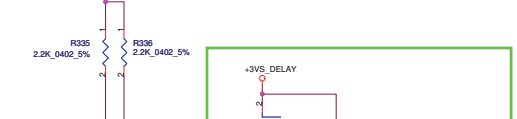
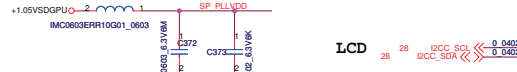
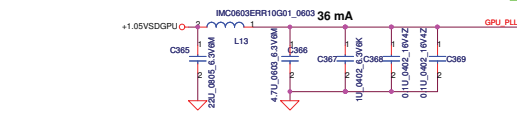


Follow DG 1.11



- 5 PEG GTX_C_HRX_N0_15] PEG GTX_C_HRX_N0_15]
- 5 PEG GTX_C_HRX_P0_15] PEG GTX_C_HRX_P0_15]
- 5 PEG GTX_C_HRX_N0_15] PEG GTX_C_HRX_N0_15]
- 5 PEG GTX_C_HRX_P0_15] PEG GTX_C_HRX_P0_15]

PEG GTX_C_HRX_P0	AP17	PEG GTX_C_HRX_P0	AL17
PEG GTX_C_HRX_N0	AP17	PEG GTX_C_HRX_N0	AL17
PEG GTX_C_HRX_P1	AP19	PEG GTX_C_HRX_P1	AM17
PEG GTX_C_HRX_N1	AP19	PEG GTX_C_HRX_N1	AM19
PEG GTX_C_HRX_P2	AP20	PEG GTX_C_HRX_P2	AL19
PEG GTX_C_HRX_N2	AP20	PEG GTX_C_HRX_N2	AL19
PEG GTX_C_HRX_P3	AP22	PEG GTX_C_HRX_P3	AM20
PEG GTX_C_HRX_N3	AP22	PEG GTX_C_HRX_N3	AM21
PEG GTX_C_HRX_P4	AP22	PEG GTX_C_HRX_P4	AM21
PEG GTX_C_HRX_N4	AP22	PEG GTX_C_HRX_N4	AM22
PEG GTX_C_HRX_P5	AP22	PEG GTX_C_HRX_P5	AM22
PEG GTX_C_HRX_N5	AP22	PEG GTX_C_HRX_N5	AM22
PEG GTX_C_HRX_P6	AP23	PEG GTX_C_HRX_P6	AM23
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PEG GTX_C_HRX_N7	AP25	PEG GTX_C_HRX_N7	AM25
PEG GTX_C_HRX_P8	AP26	PEG GTX_C_HRX_P8	AM26
PEG GTX_C_HRX_N8	AP26	PEG GTX_C_HRX_N8	AM26
PEG GTX_C_HRX_P9	AP26	PEG GTX_C_HRX_P9	AM26
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PEG GTX_C_HRX_P10	AP28	PEG GTX_C_HRX_P10	AM28
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PEG GTX_C_HRX_P11	AP28	PEG GTX_C_HRX_P11	AM28
PEG GTX_C_HRX_N11	AP28	PEG GTX_C_HRX_N11	AM28
PEG GTX_C_HRX_P12	AP29	PEG GTX_C_HRX_P12	AM29
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PEG GTX_C_HRX_N13	AP31	PEG GTX_C_HRX_N13	AM31
PEG GTX_C_HRX_P14	AP32	PEG GTX_C_HRX_P14	AM32
PEG GTX_C_HRX_N14	AP32	PEG GTX_C_HRX_N14	AM32
PEG GTX_C_HRX_P15	AP34	PEG GTX_C_HRX_P15	AM34
PEG GTX_C_HRX_N15	AP34	PEG GTX_C_HRX_N15	AM34



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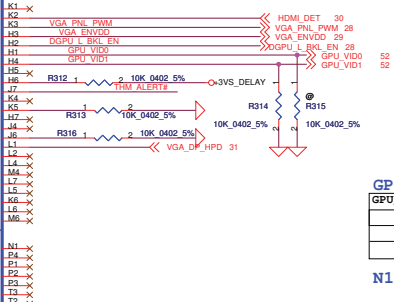
U11A Part 1 of 7

GPIO

PCI EXPRESS DVO

CLK

I2C DACs

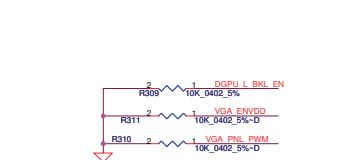
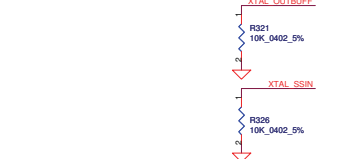
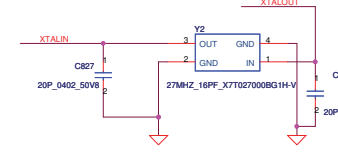


GPIO6 GPIO5

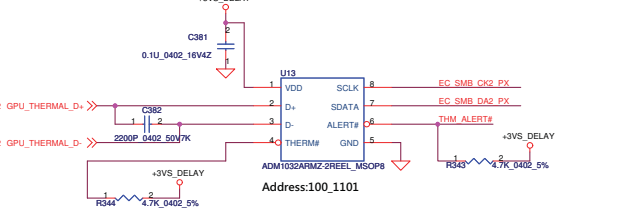
GPU_VID1	GPU_VID0	VGA_CORE
0	0	0.85V
0	1	0.85V
1	1	0.95V

N11P-GS1

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	H	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	IN	L	N/A
GPIO8	IN	L	N/A
GPIO9	IN	L	THM_ALERT#
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A
GPIO15	IN	H	DP Hot-plug

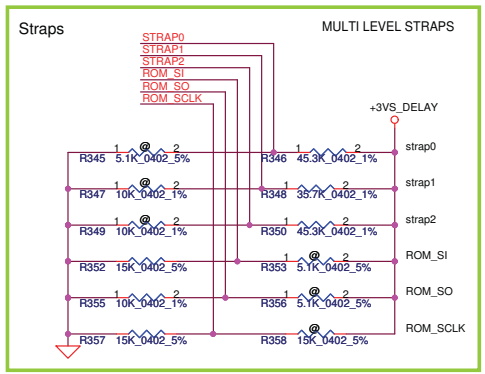
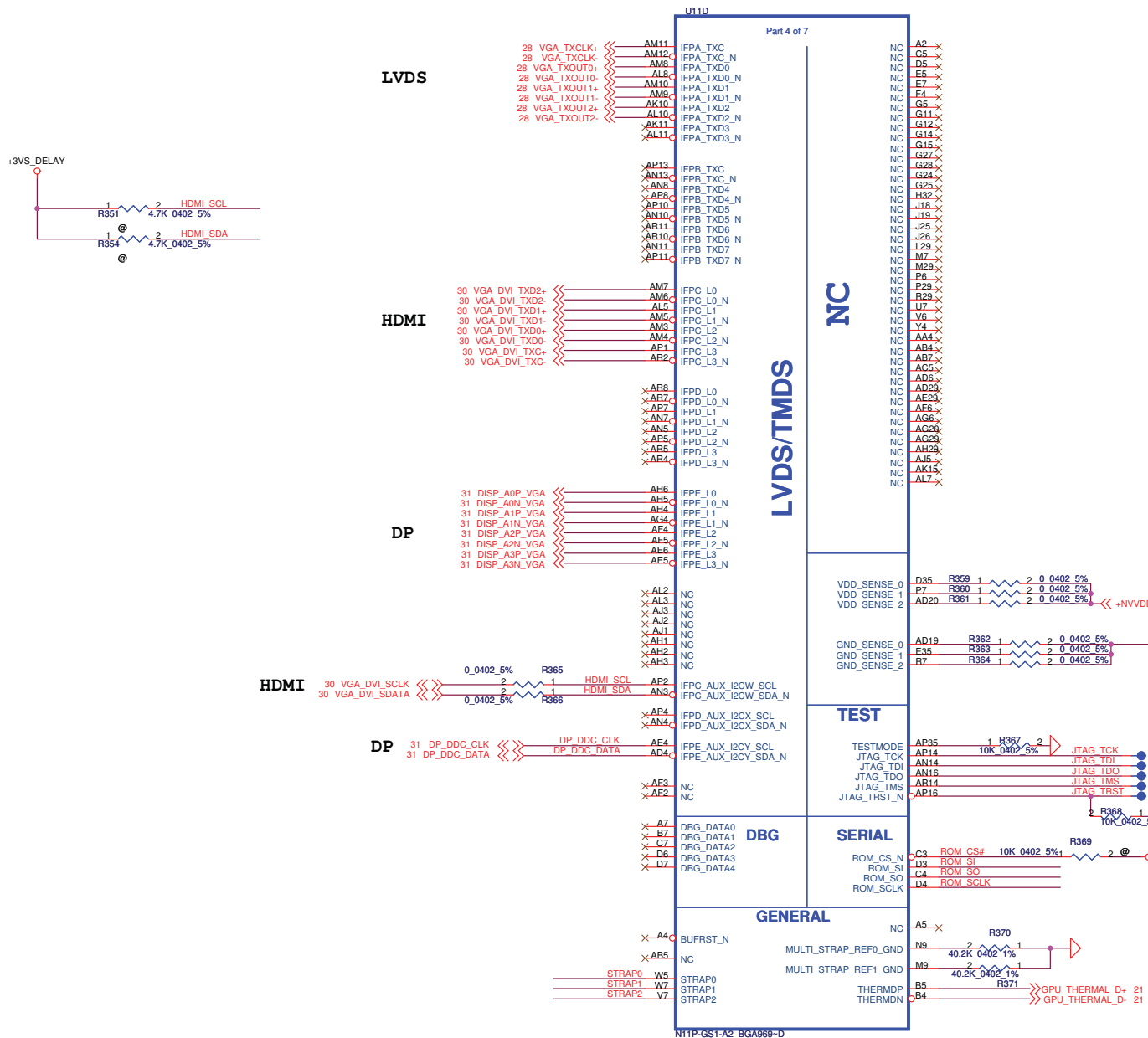


VGA Thermal Sensor ADM1032ARMZ



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Security Classification	Compal Secret Data	Title	
Issued Date	2009/07/25	N11P-GS1(1/5)PCIE/STRAPS/THERM	
Deciphered Date	2010/07/25	Size	Document Number
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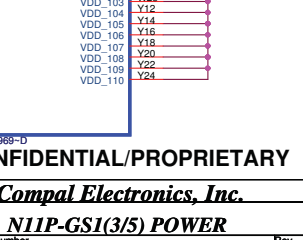
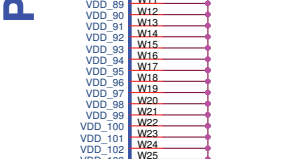
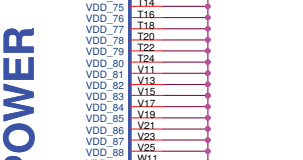
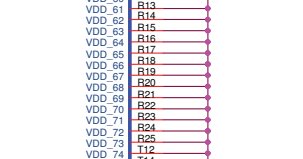
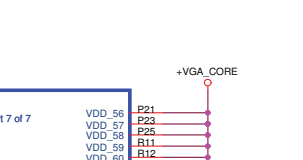
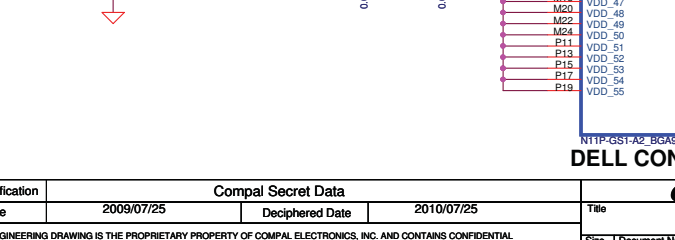
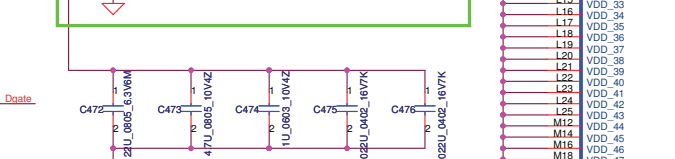
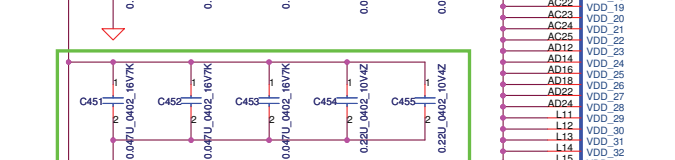
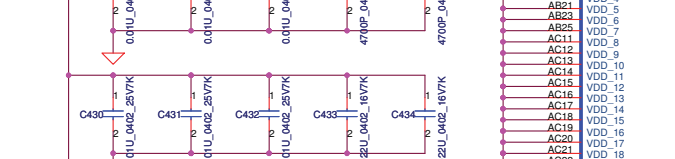
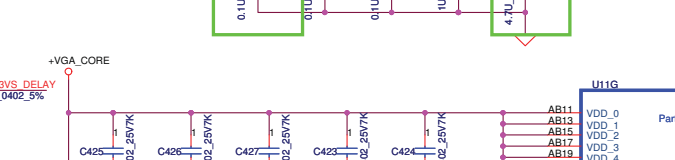
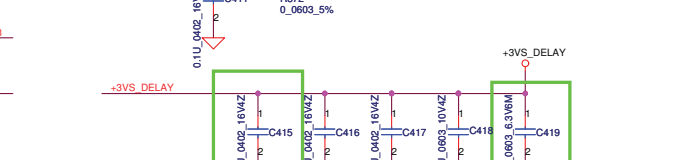
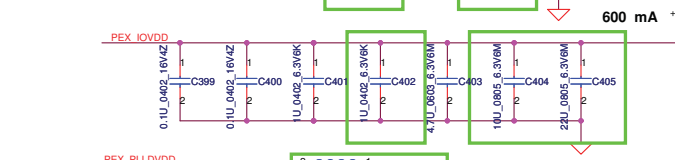
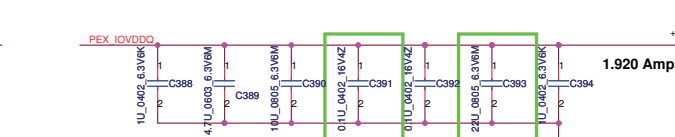
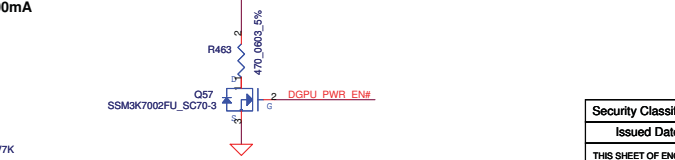
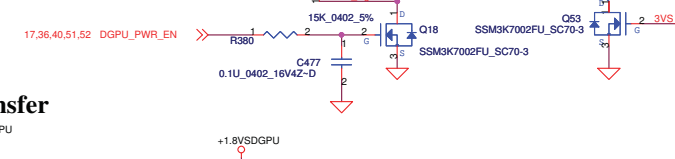
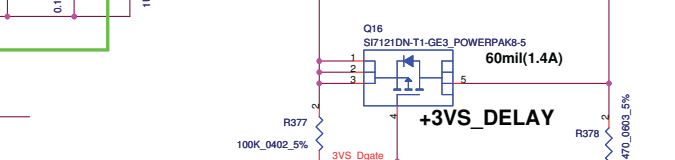
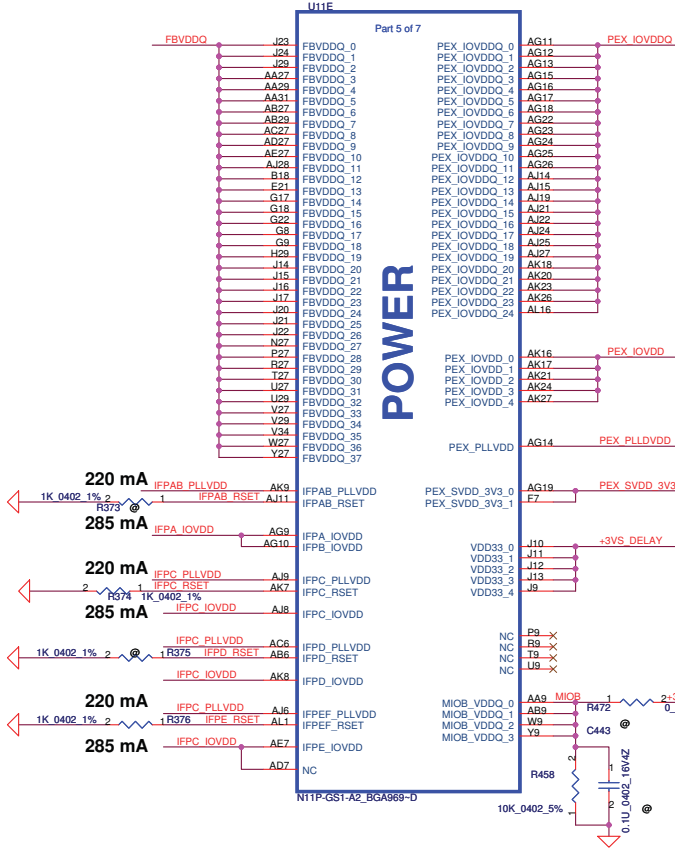
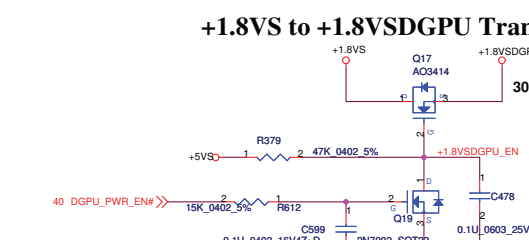
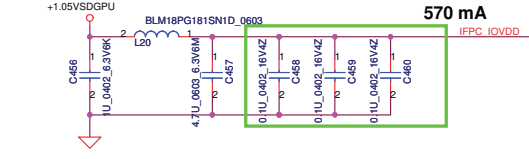
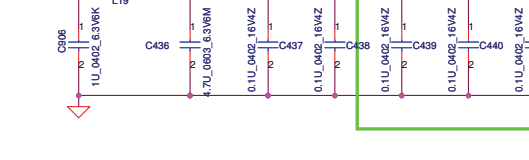
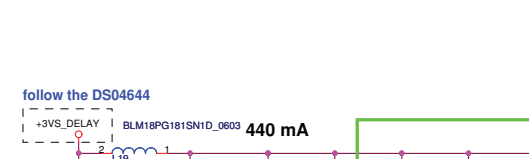
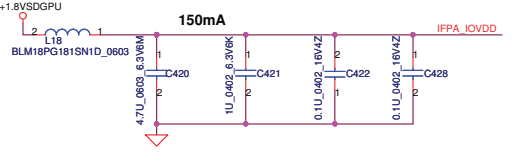
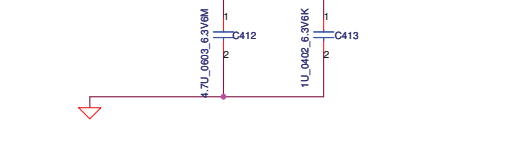
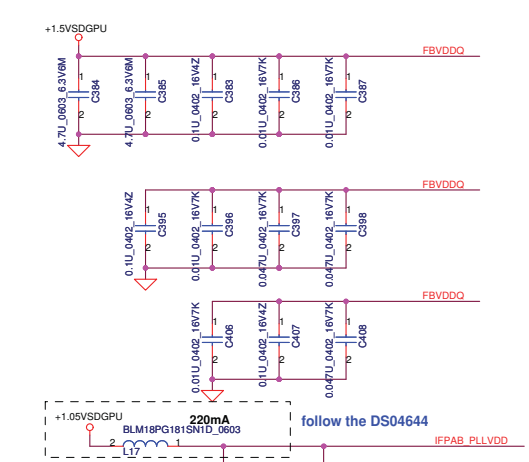


	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung	H 45K	H 35K	L 30K	L 20K	L 10K	H 15K
64MX16 Hynix	H 45K	H 35K	H 45.3K	L 15K	L 10K	H 15K

SSI --> Hynix

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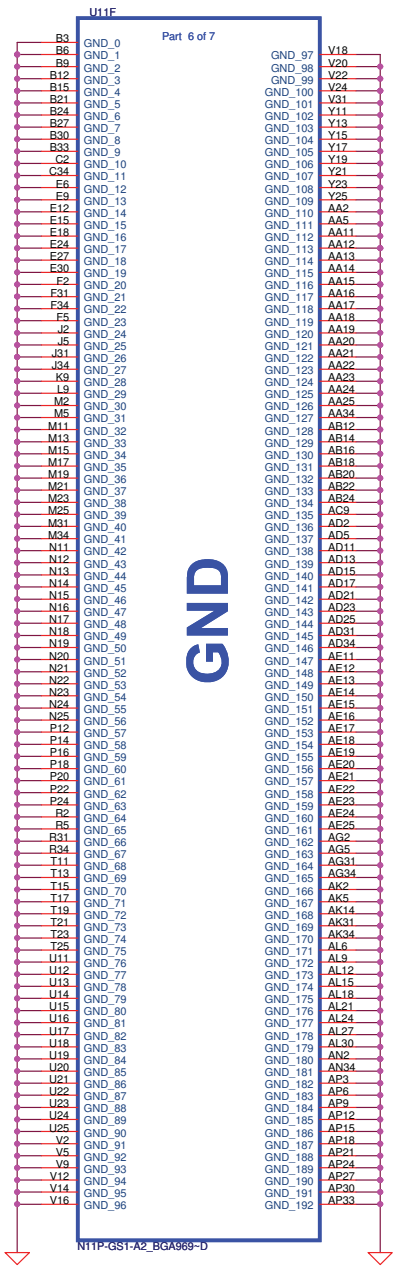
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N11P-GS1(2/5) 10			
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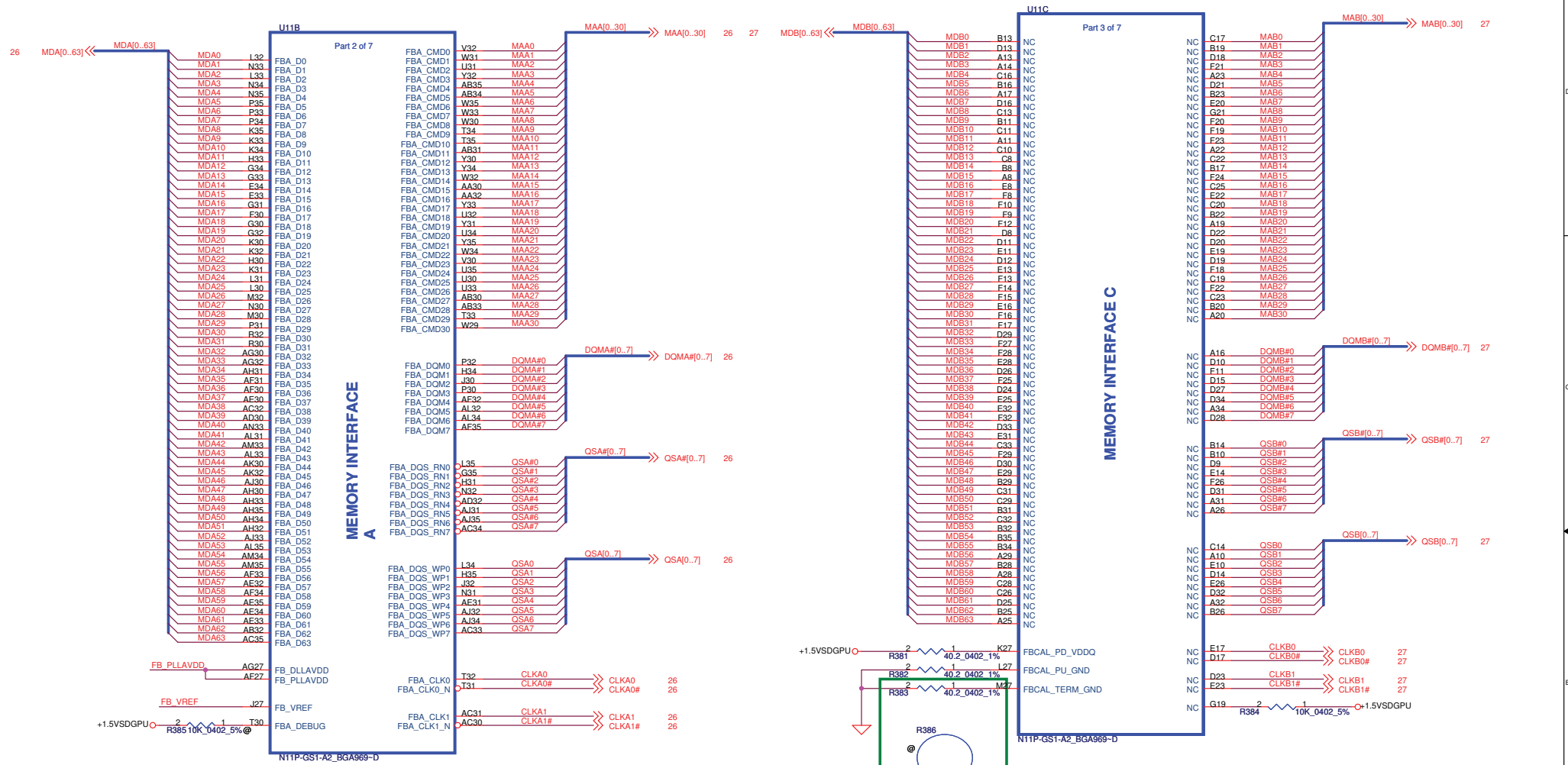
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Compal Electronics, Inc.			
N1IP-GS1(3/5) POWER			
Title			
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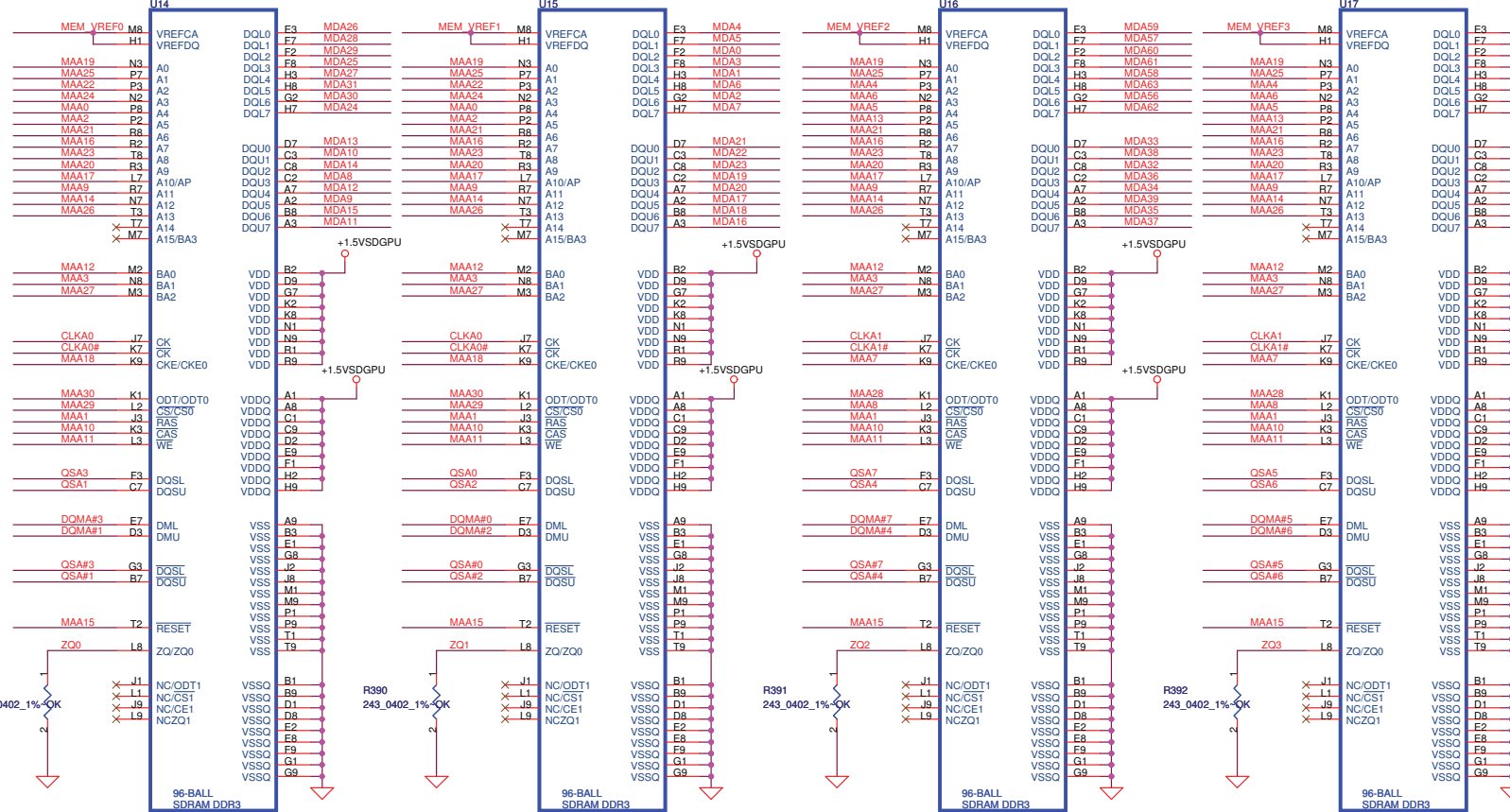
Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3 (11P)	+1.5VS	40.2 ohm	40.2 ohm	40.2 ohm

Must be used 1% resistor for driver calibration

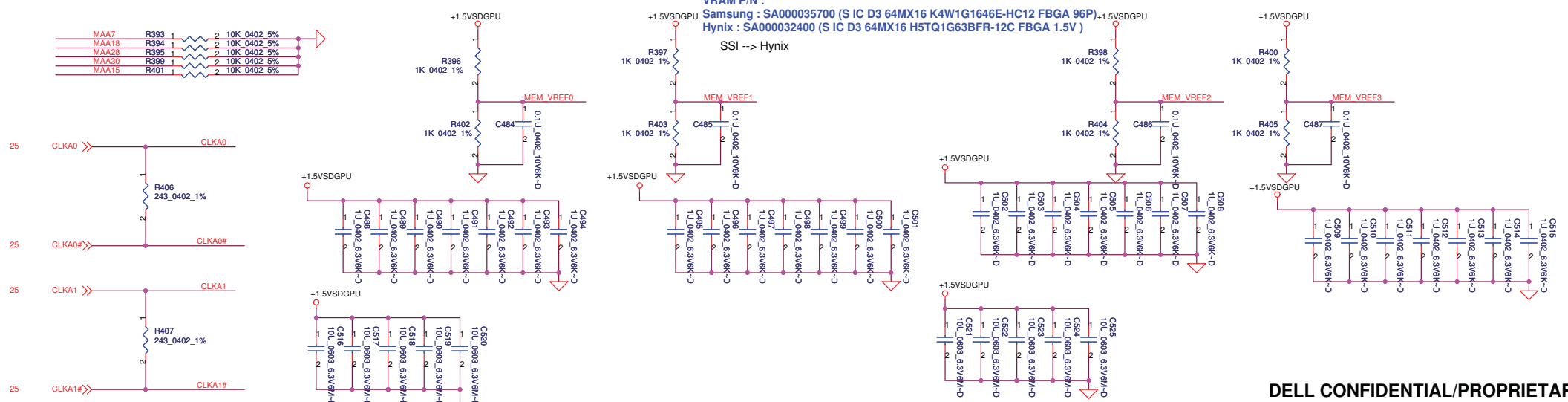
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				N11P-GS1(5/5) MEMORY	
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VRAM P/N : Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
 Hynix : SA000032400 (S IC D3 64MX16 H5TG1G63BFR-12C FBGA 1.5V)

SSI -> Hynix



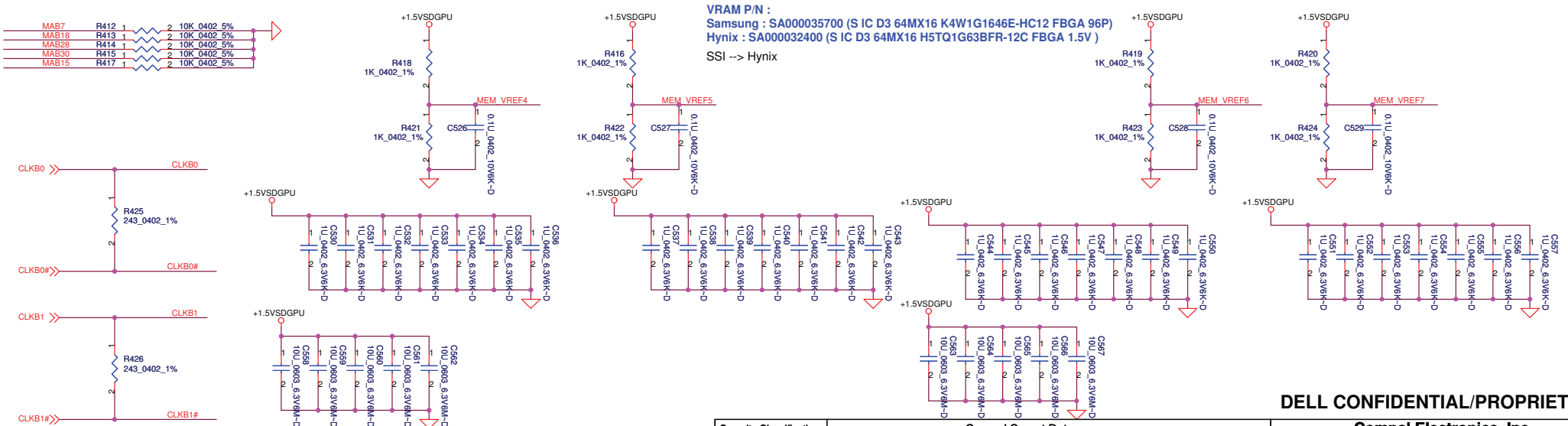
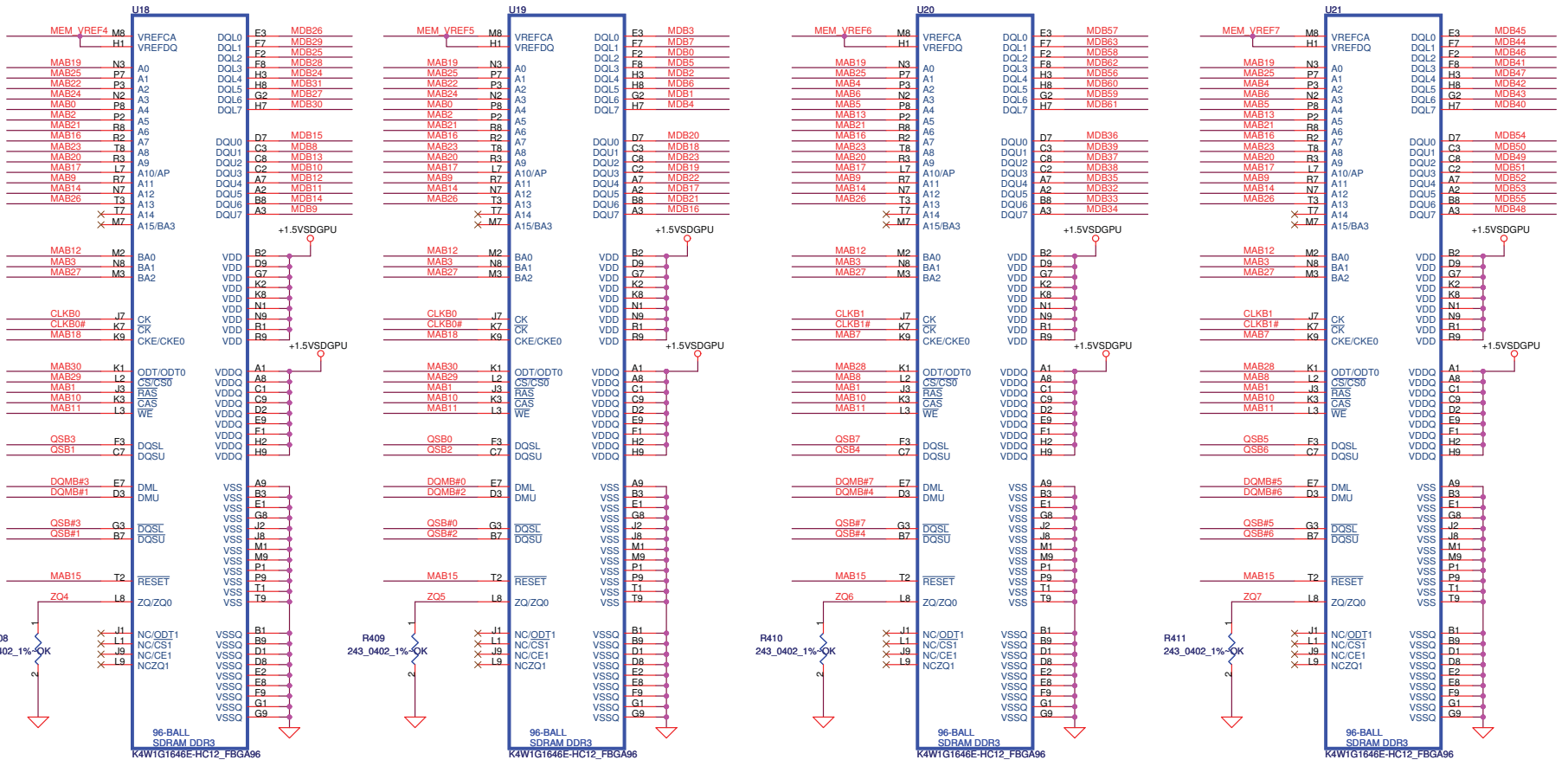
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		2010/07/25

Title
VRAM DDR3 / Channel A

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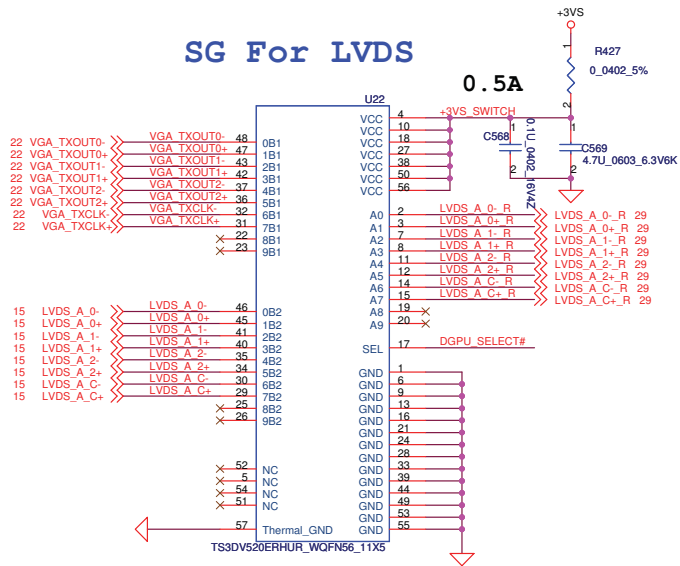
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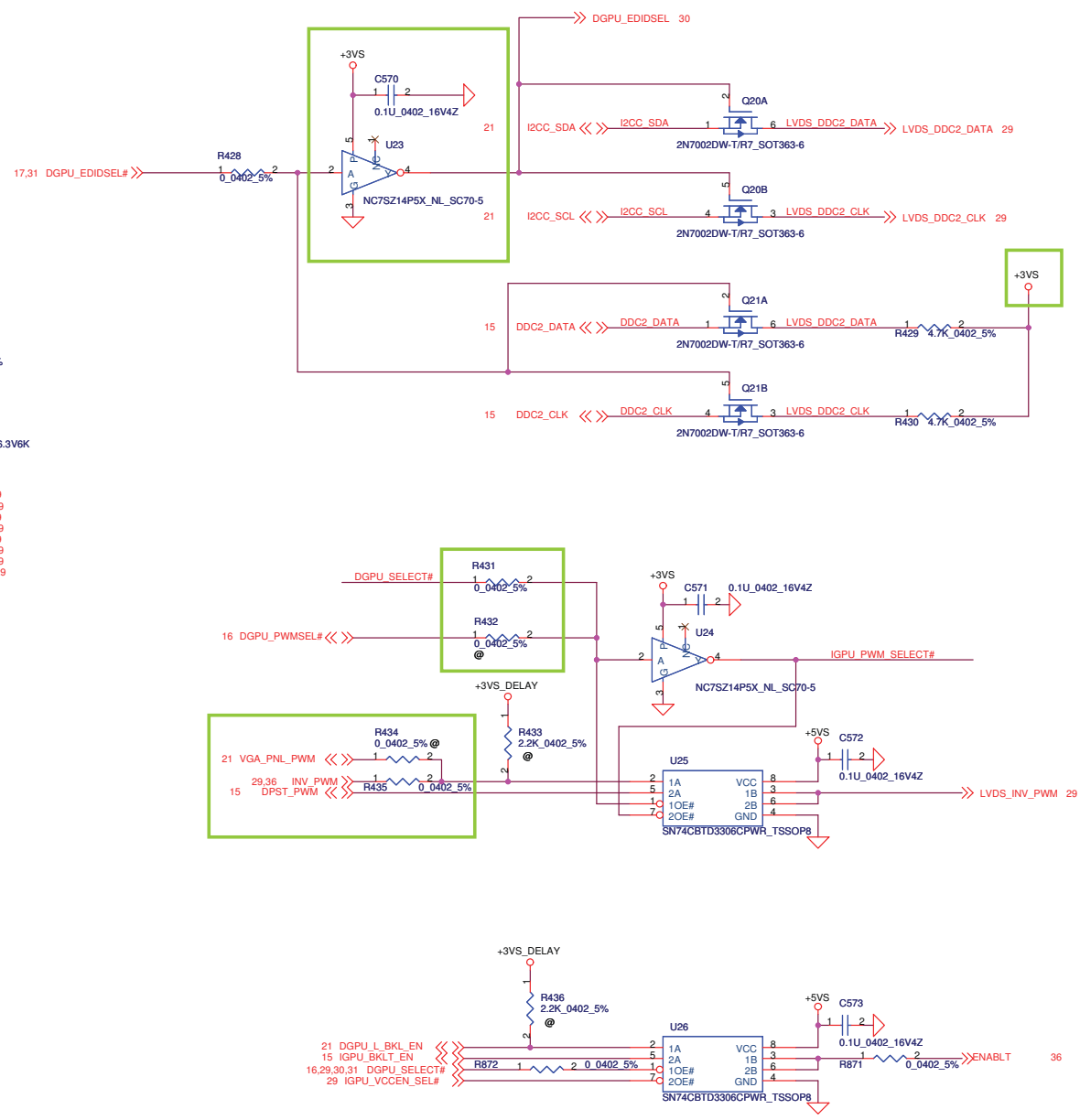
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Size	Document Number	VRAM DDR3 / Channel B		Rev	1.0			
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SG For LVDS

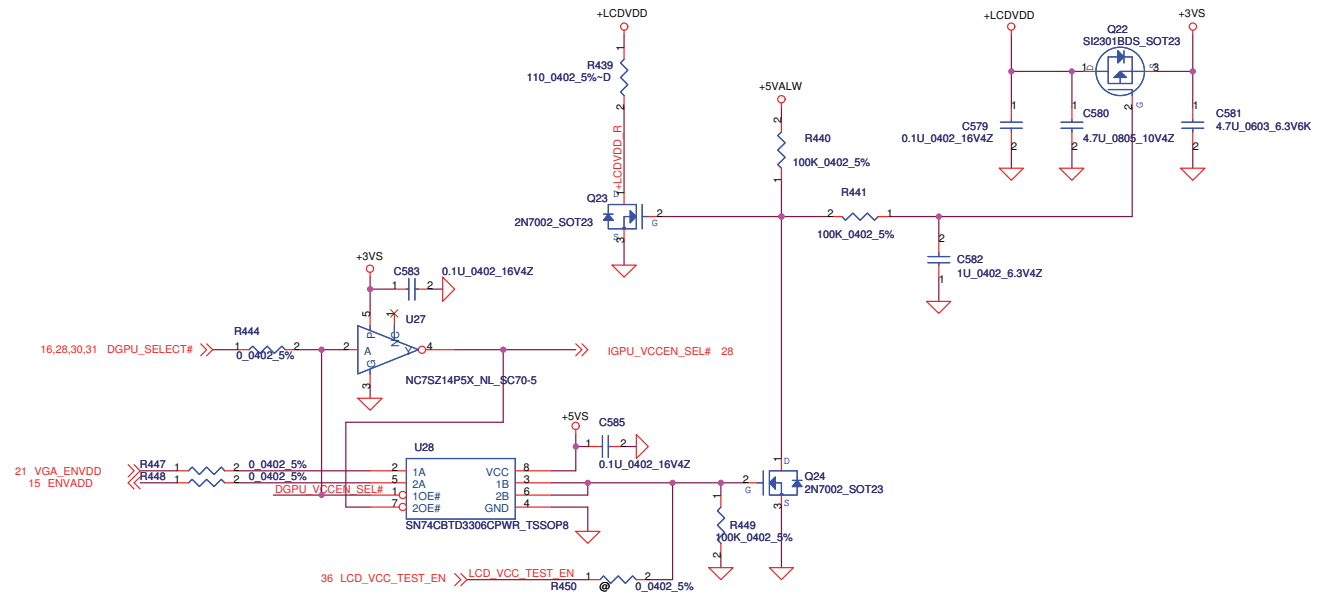
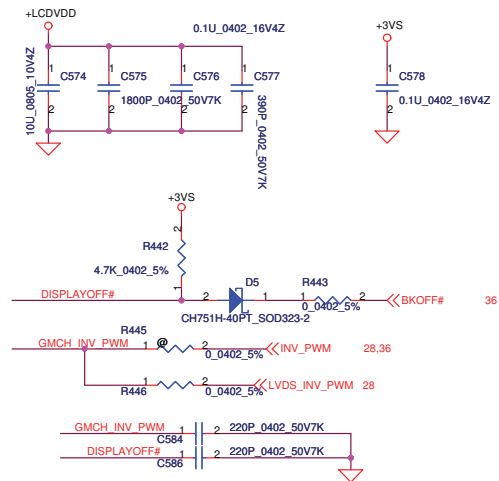


For SSI shortage issue
P/N from SA00001RM00 change to SA00001RM0L

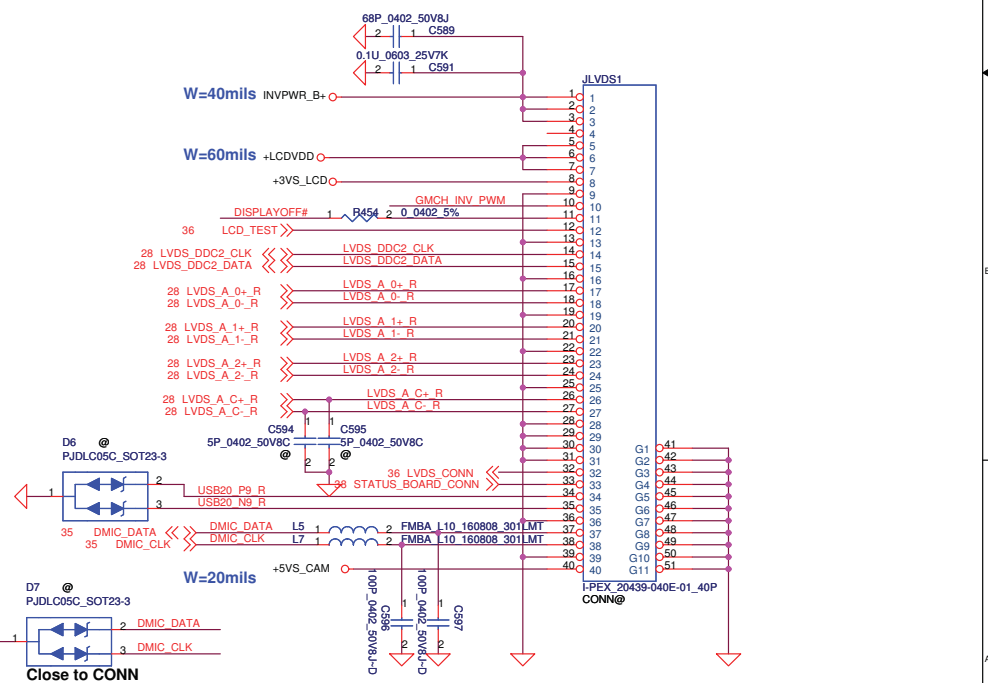
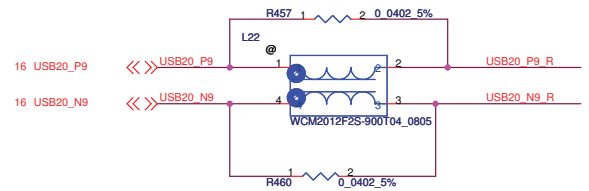
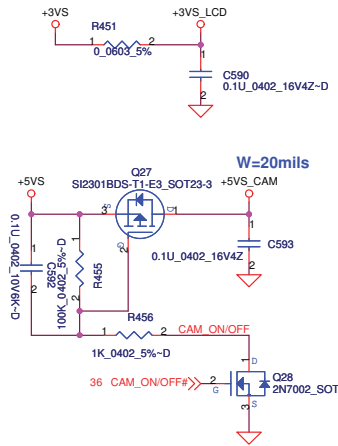
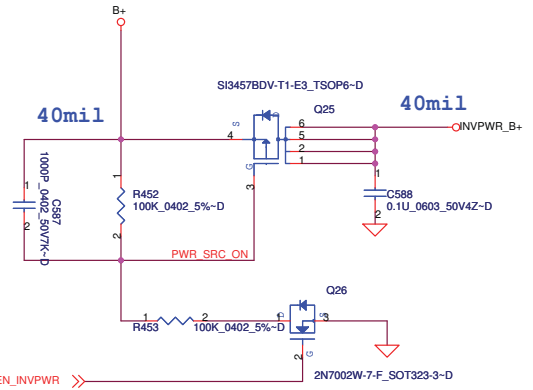


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				LVDS Switch	
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				Custom	1.0
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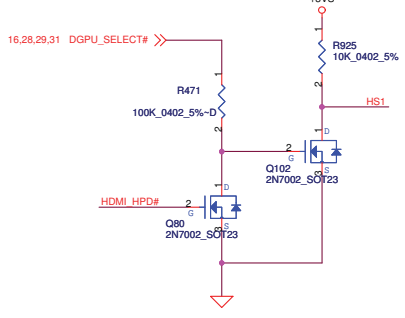
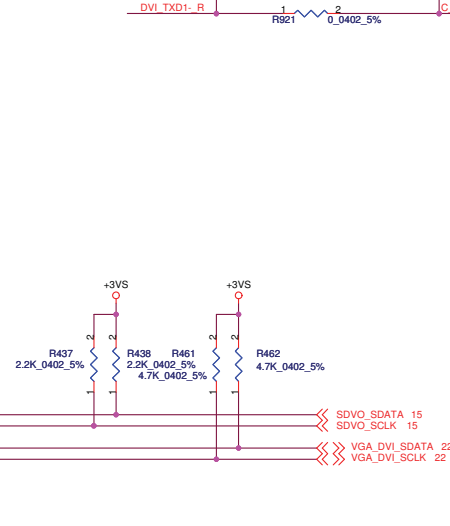
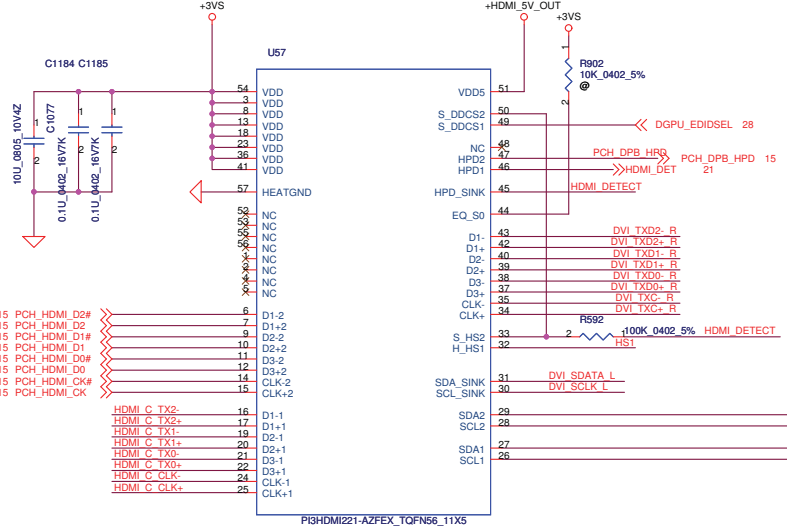
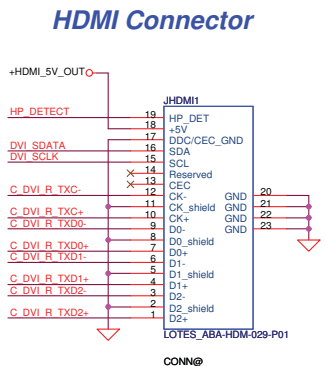
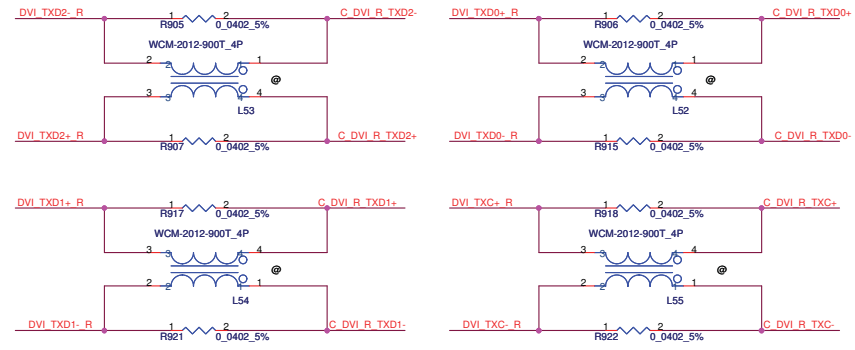
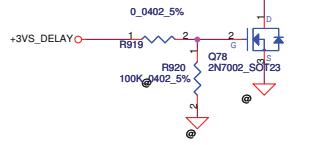
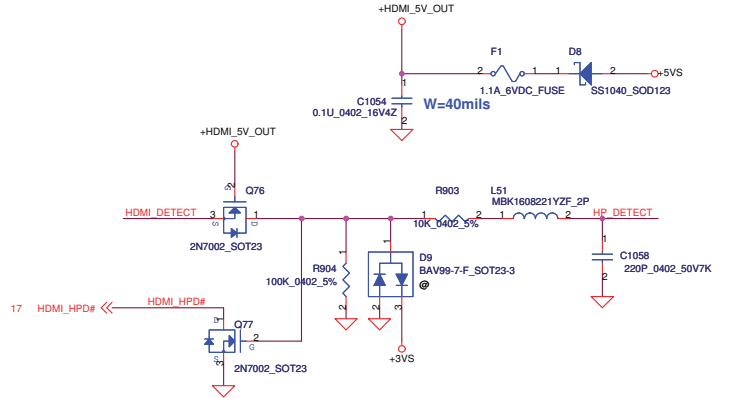
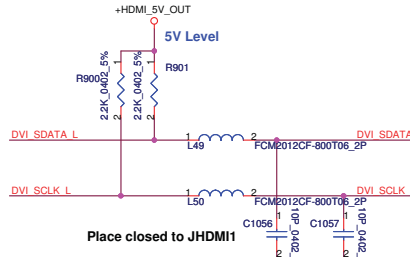
LVDS and USB CAM connector



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22	VGA_DVI_TXD2-	VGA_DVI_TXD2-	C1059	2	1	0.1U_0402_16V7K	HDMI C_TX2-
22	VGA_DVI_TXD2+	VGA_DVI_TXD2+	C1060	2	1	0.1U_0402_16V7K	HDMI C_TX2+
22	VGA_DVI_TXD1-	VGA_DVI_TXD1-	C1061	2	1	0.1U_0402_16V7K	HDMI C_TX1-
22	VGA_DVI_TXD1+	VGA_DVI_TXD1+	C1062	2	1	0.1U_0402_16V7K	HDMI C_TX1+
22	VGA_DVI_TXD0-	VGA_DVI_TXD0-	C1063	2	1	0.1U_0402_16V7K	HDMI C_TX0-
22	VGA_DVI_TXD0+	VGA_DVI_TXD0+	C1064	2	1	0.1U_0402_16V7K	HDMI C_TX0+
22	VGA_DVI_TXC-	VGA_DVI_TXC-	C1065	2	1	0.1U_0402_16V7K	HDMI C_CLK-
22	VGA_DVI_TXC+	VGA_DVI_TXC+	C1066	2	1	0.1U_0402_16V7K	HDMI C_CLK+



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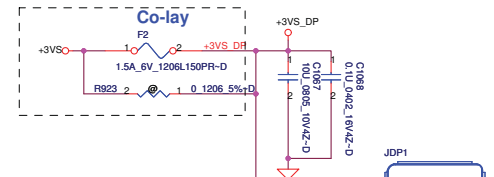
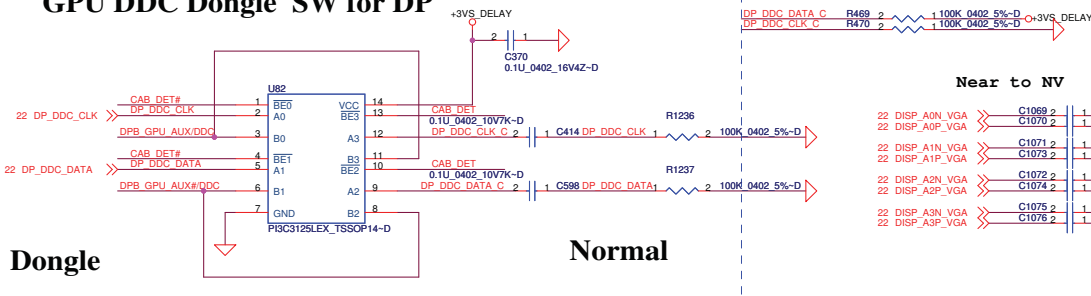
HDMI

Size: Custom, Document Number: LA-5812P, Rev: 1.0

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GPU DDC Dongle SW for DP



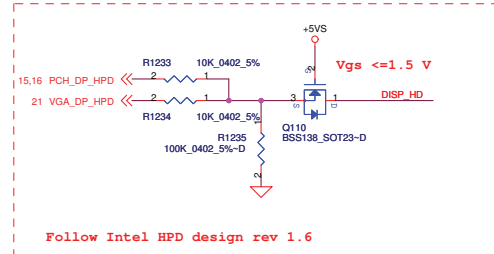
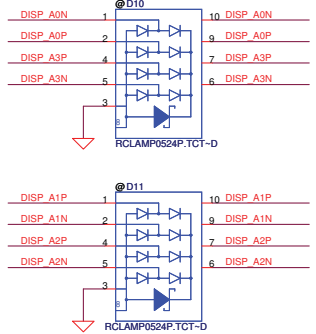
Near to NV

22 DISP_A0N_VGA	C1069 2	1	0.1U 0402 10V6K-D	DISP_C_A0N
22 DISP_A0P_VGA	C1070 2	1	0.1U 0402 10V6K-D	DISP_C_A0P
22 DISP_A1N_VGA	C1071 2	1	0.1U 0402 10V6K-D	DISP_C_A1N
22 DISP_A1P_VGA	C1072 2	1	0.1U 0402 10V6K-D	DISP_C_A1P
22 DISP_A2N_VGA	C1072 2	1	0.1U 0402 10V6K-D	DISP_C_A2N
22 DISP_A2P_VGA	C1074 2	1	0.1U 0402 10V6K-D	DISP_C_A2P
22 DISP_A3N_VGA	C1075 2	1	0.1U 0402 10V6K-D	DISP_C_A3N
22 DISP_A3P_VGA	C1076 2	1	0.1U 0402 10V6K-D	DISP_C_A3P

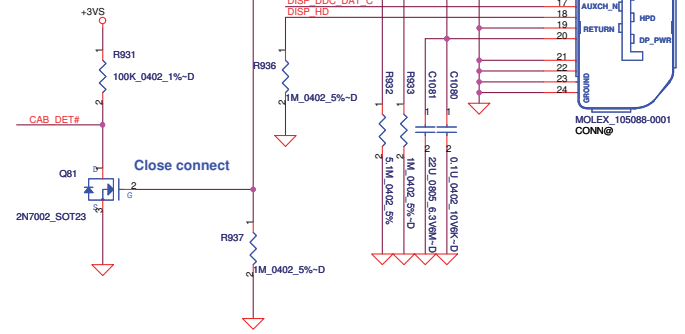
Dongle

Normal

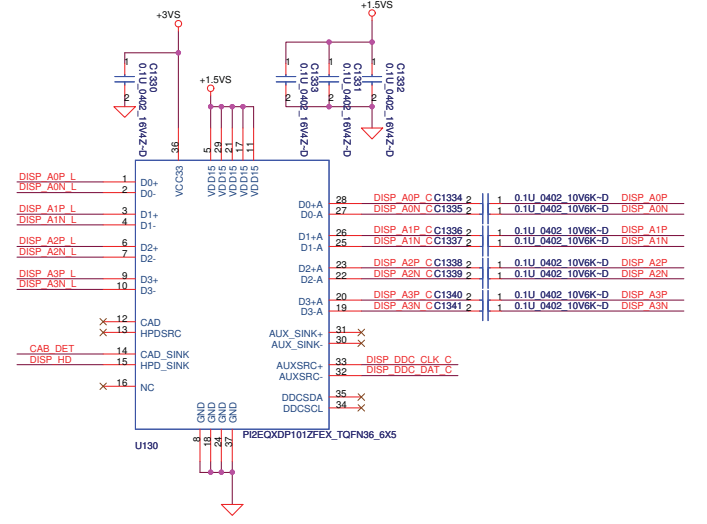
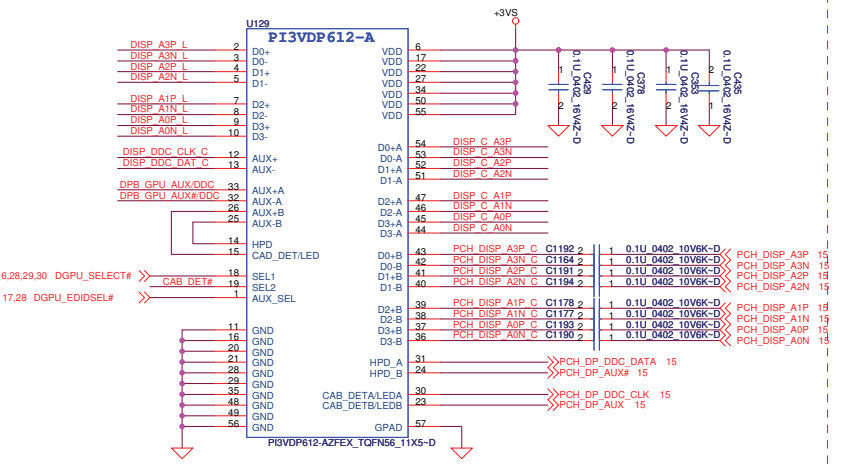
Place close JDP1



Follow Intel HPD design rev 1.6



PCH/GPU AUX&LANE SW for DPB



Truth Table (SEL control)

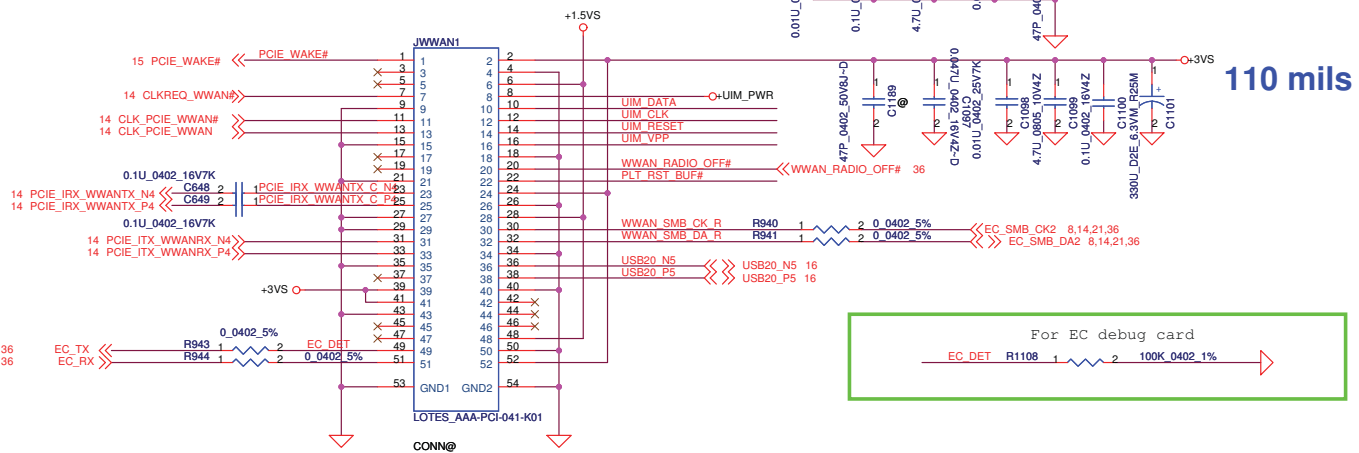
Function	SEL 1/SEL2/AUX_SEL
Port A is active	L
Port B is active	H

Notes:
 SEL1 is only for DP lanes
 SEL2 is only for HPD/CAB_DET signals
 AUX_SEL is only for AUX path

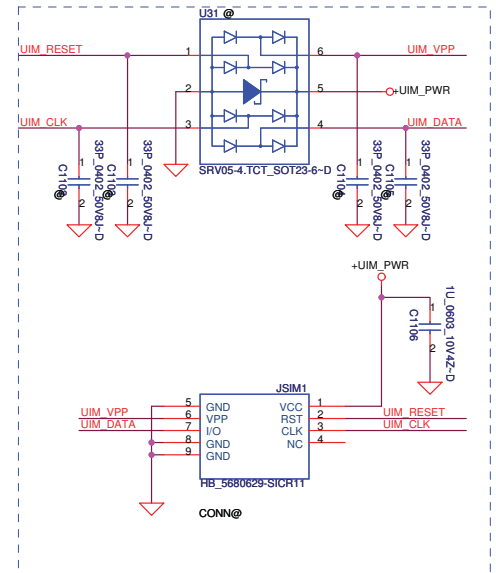
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Size	Document Number	Rev		
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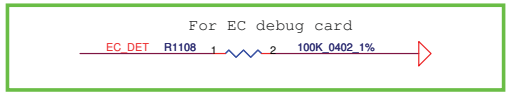
WWAN PCIE MiniCard



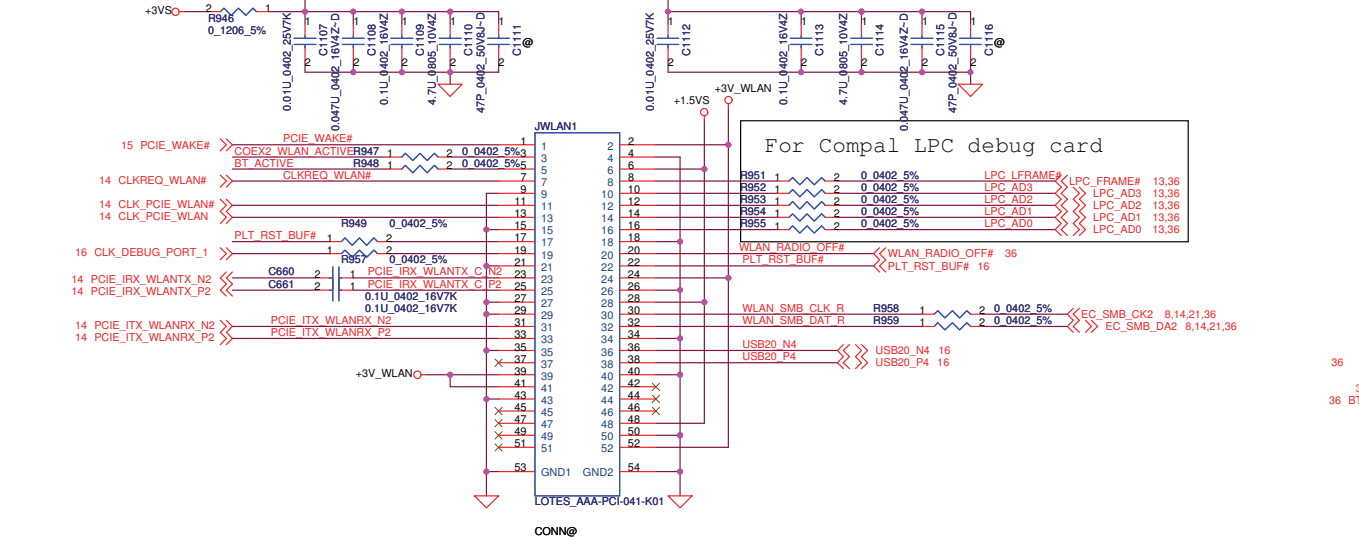
SIM Card



110 mils

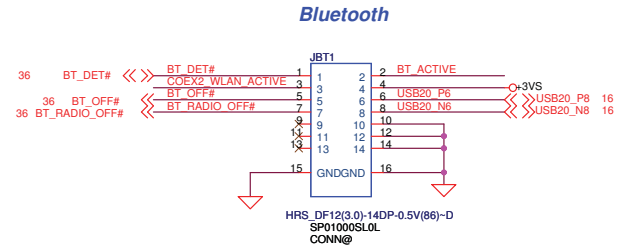


40 mils WLAN/WIMAX PCIE Mini Card



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA

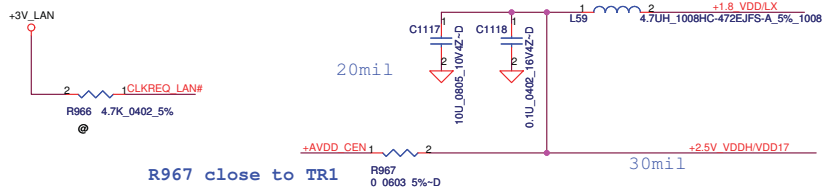
For Compal LPC debug card



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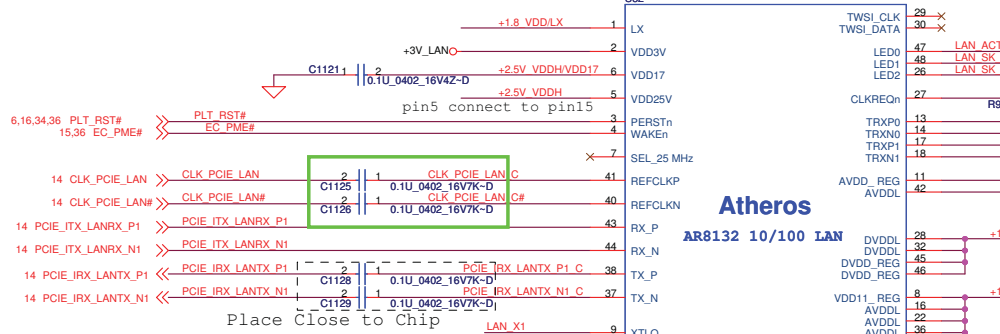
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Size	Document Number	Date	Rev
Custom	LA-5812P	Monday, May 10, 2010	1.0
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C1117, C1118, L59 Close to pin 1 60mil



R967 close to TR1

the common mode voltage of the input pcie clock must be lower than 0.5V

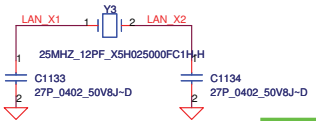


Atheros

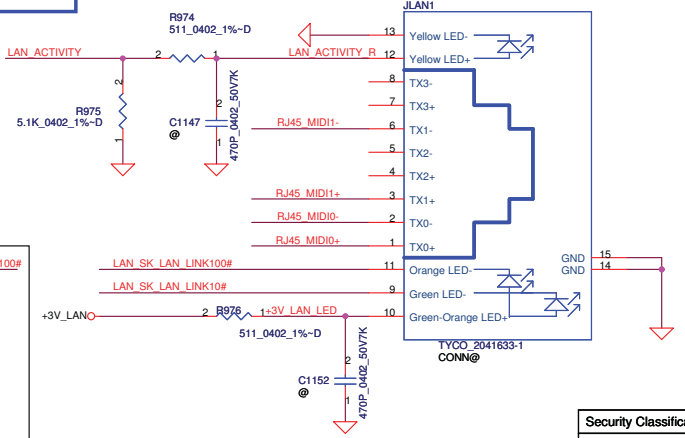
AR8132 10/100 LAN

Place Close to Chip

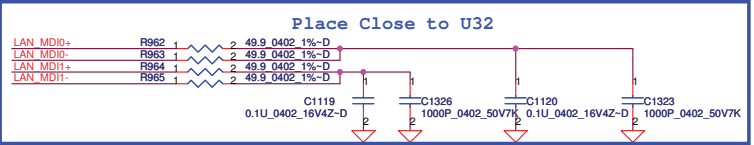
All Cap close to TR1



Pull down circuit:
more power saving in no-overclocking mode
vendor suggestion

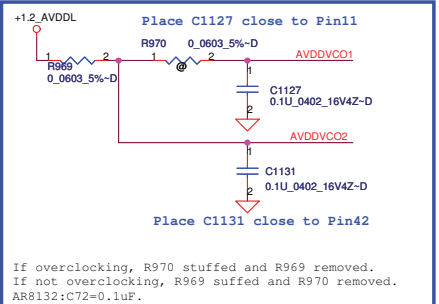
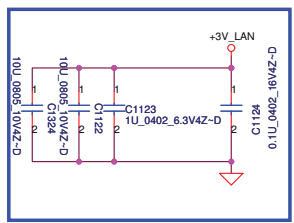


C1322, C1325 close to JLAN1



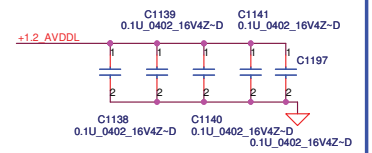
Place Close to U32

Layout Notice : Place as close
c hip U32 PIN5

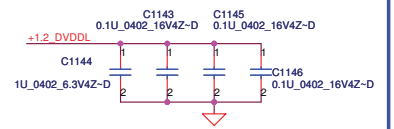


If overclocking, R970 stuffed and R969 removed.
If not overclocking, R969 suffed and R970 removed.
AR8132:C72=0.1uF.

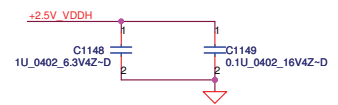
Place C1138 close to Pin8. C1139,C1141,C1140,C1197close to Pin16, Pin36, Pin39,Pin22



Place C1144 close to Pin46. C1143,C1145,C1146 close to Pin45, Pin28, Pin32



Place C1148 close to Pin15, C1149 close to Pin25



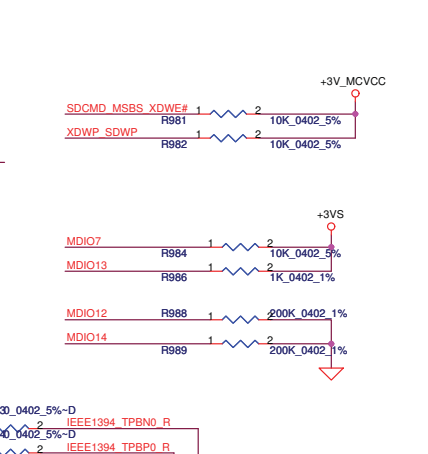
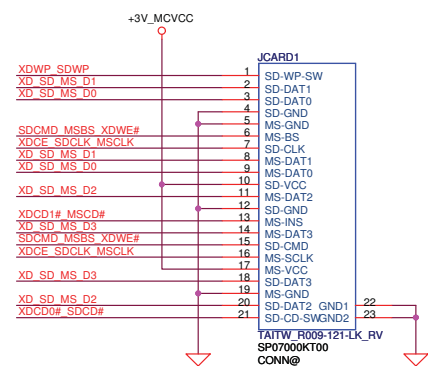
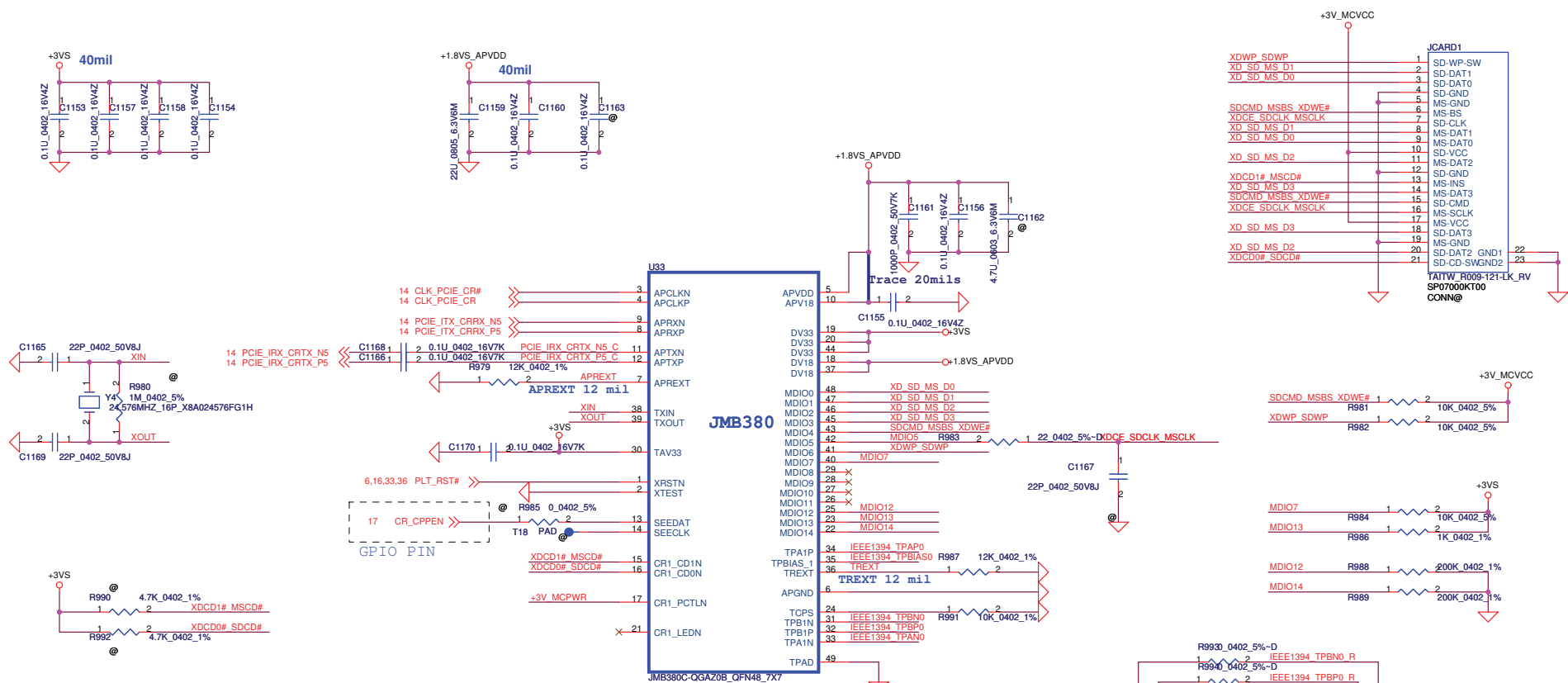
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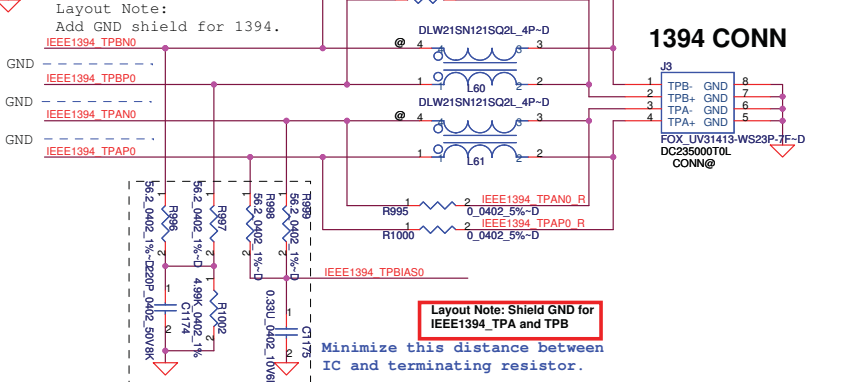
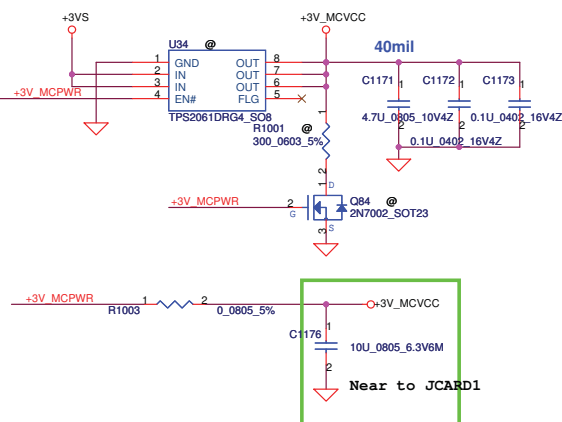
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3 in 1 Card Reader CONN



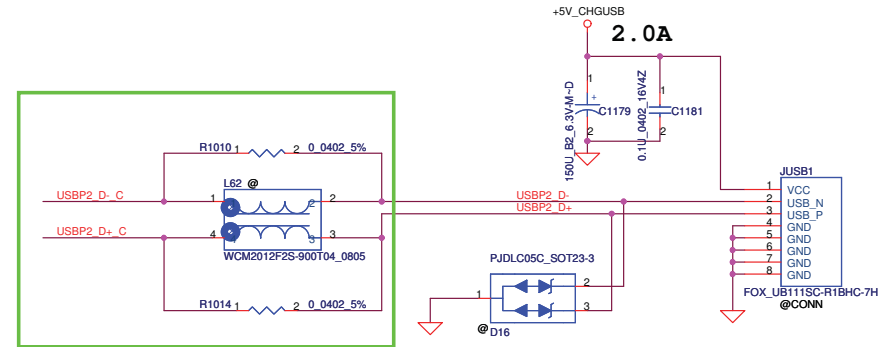
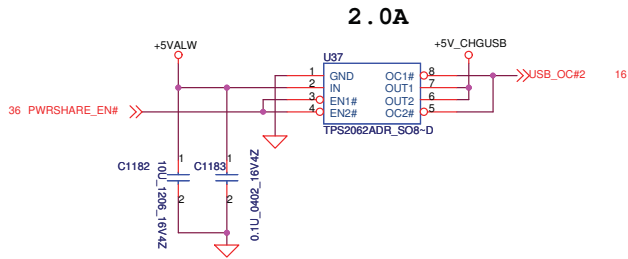
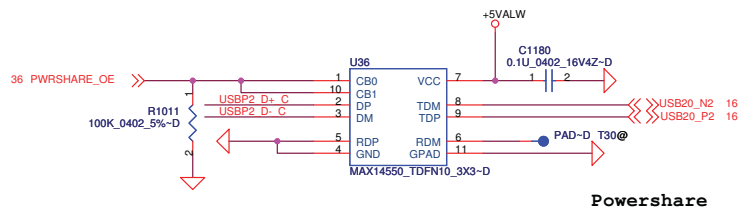
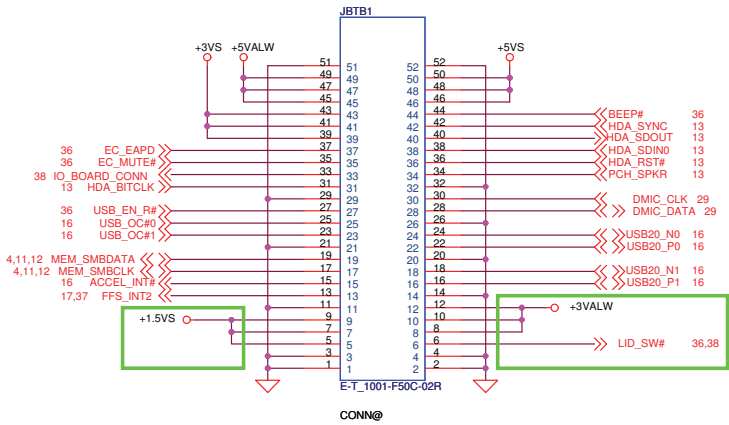
Memory Card Power Switch



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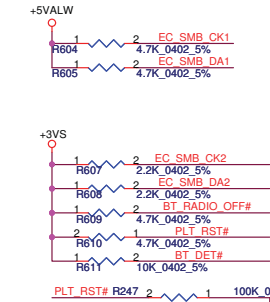
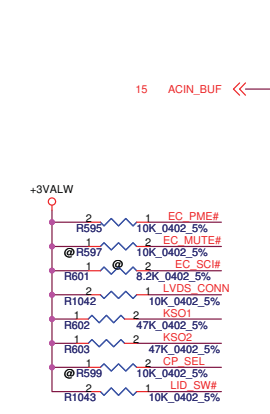
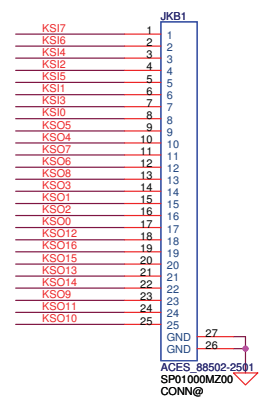
IO Board CONN



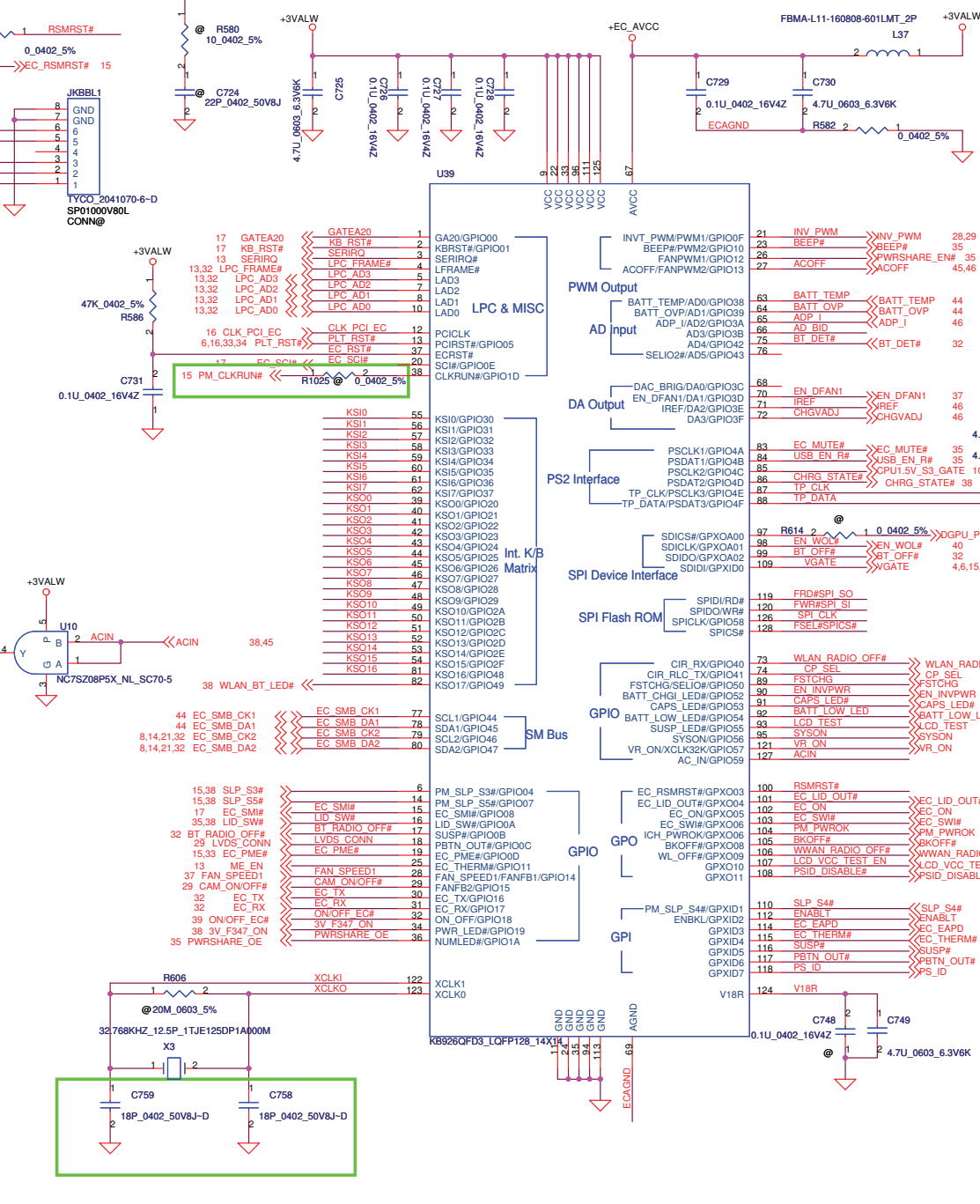
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				USB/LID SW/IO CONN		
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RSMRST circuit

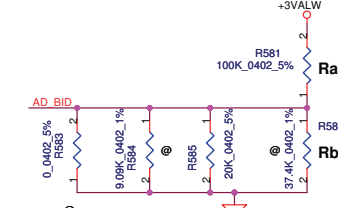
KEYBOARD CONN.



<http://hobi-elektronika.net>

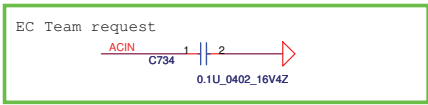


Board ID

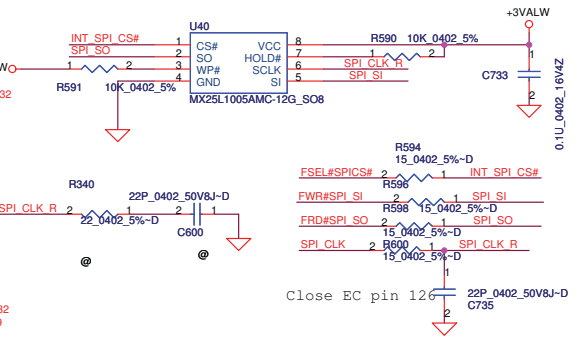


BOARD ID Table

ID	BOARD ID	Ra	Rb	Vab
0	0.1(X00)	NC	0	0V
1	0.2(X01)	100K	9.09K	0.25V
2	0.3(X02)	100K	20K	0.50V
3	1.0(A00)	100K	37.4K	0.82V

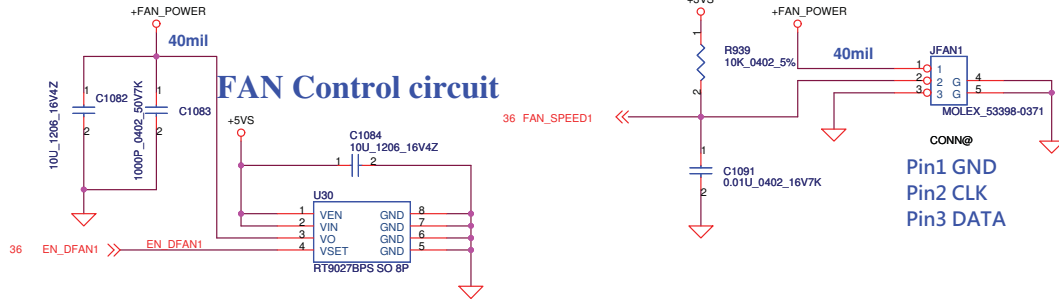


System SPI Flash ROM (1Mb)



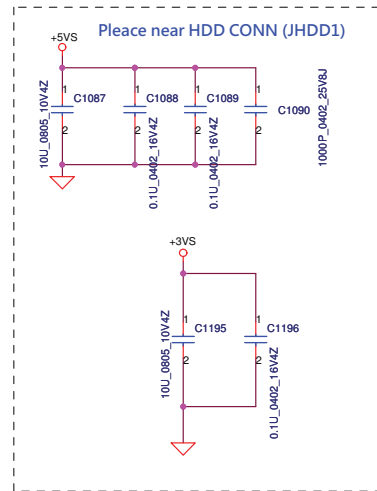
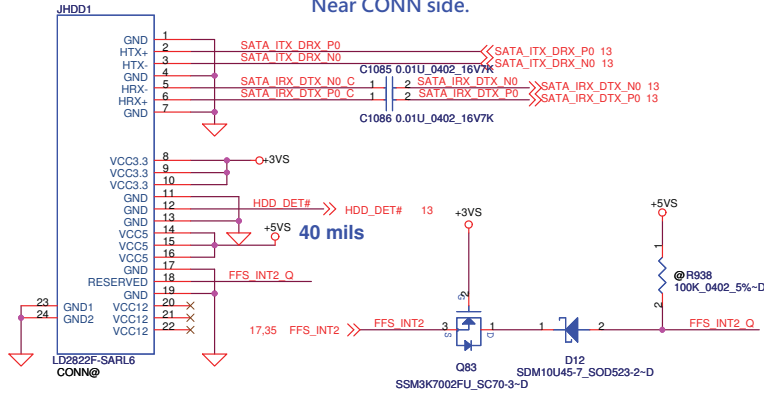
KSO8 @C736	100P_0402_25V8K	100P_0402_25V8K	C737@	KSI7
KSI3 @C738	100P_0402_25V8K	100P_0402_25V8K	C739@	KSI6
KSO9 @C740	100P_0402_25V8K	100P_0402_25V8K	C741@	KSI5
KSI2 @C742	100P_0402_25V8K	100P_0402_25V8K	C743@	KSO0
KSI1 @C744	100P_0402_25V8K	100P_0402_25V8K	C745@	KSO1
KSO10 @C746	100P_0402_25V8K	100P_0402_25V8K	C747@	KSO2
KSO11 @C750	100P_0402_25V8K	100P_0402_25V8K	C751@	KSI4
KSO12 @C752	100P_0402_25V8K	100P_0402_25V8K	C753@	KSO3
KSO13 @C756	100P_0402_25V8K	100P_0402_25V8K	C757@	KSO5
KSO14 @C760	100P_0402_25V8K	100P_0402_25V8K	C761@	KSO6
KSO15 @C762	100P_0402_25V8K	100P_0402_25V8K	C763@	KSO7
KSO16 @C764	100P_0402_25V8K	100P_0402_25V8K		

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HDD Connector

Near CONN side.



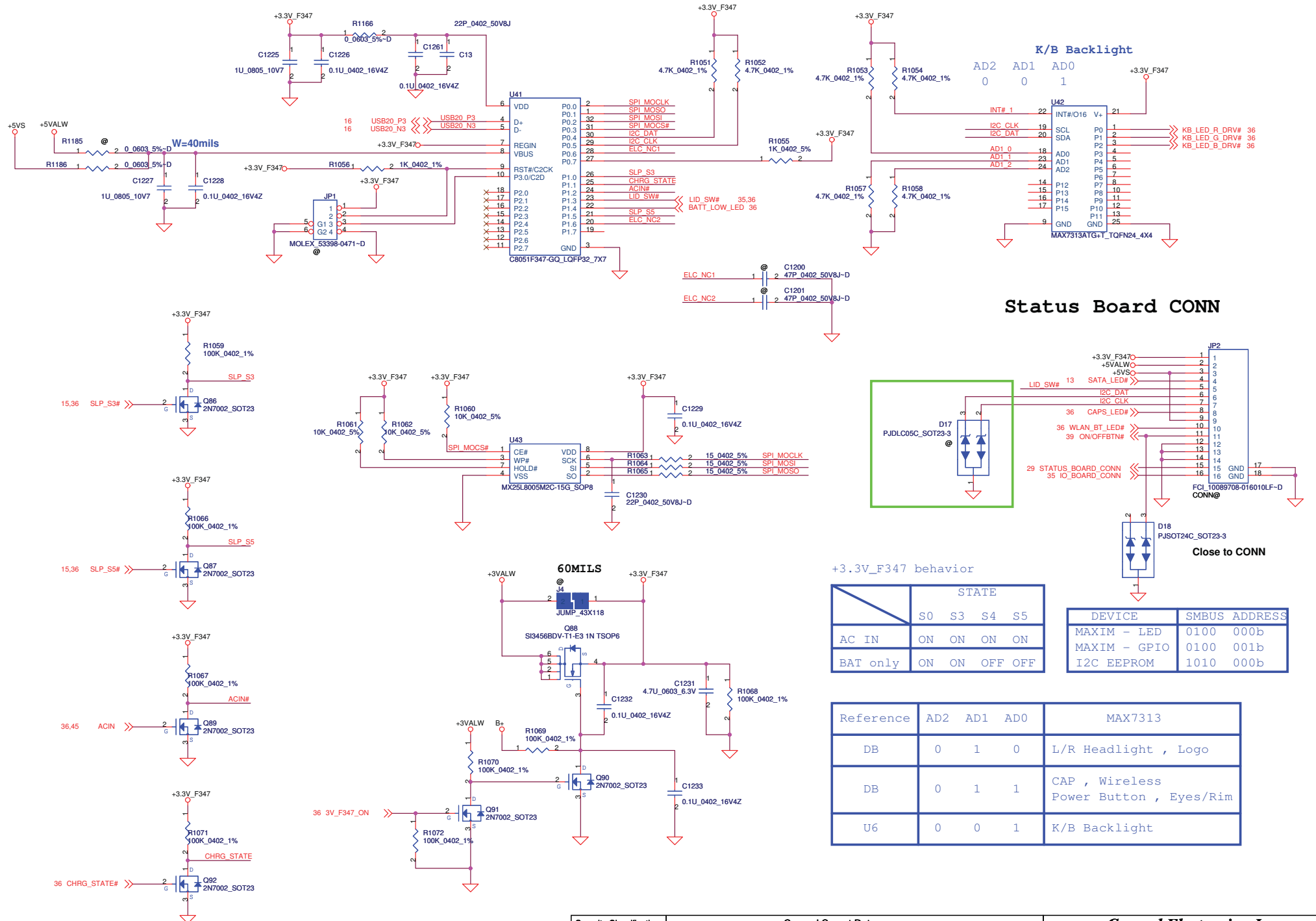
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File	FAN & Thermal Sensor		Rev	1.0
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K/B Backlight

Status Board CONN

+3.3V_F347 behavior

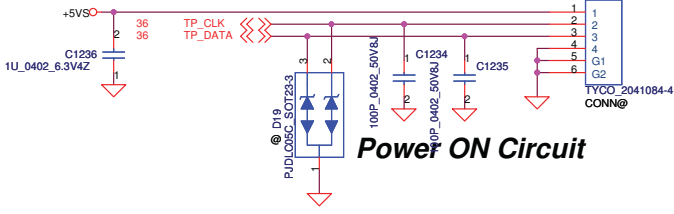
	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

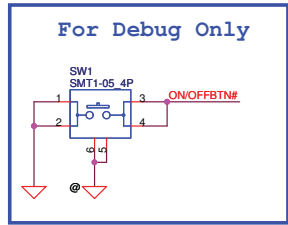
Reference	AD2	AD1	AD0	MAX7313
DB	0	1	0	L/R Headlight , Logo
DB	0	1	1	CAP , Wireless Power Button , Eyes/Rim
U6	0	0	1	K/B Backlight

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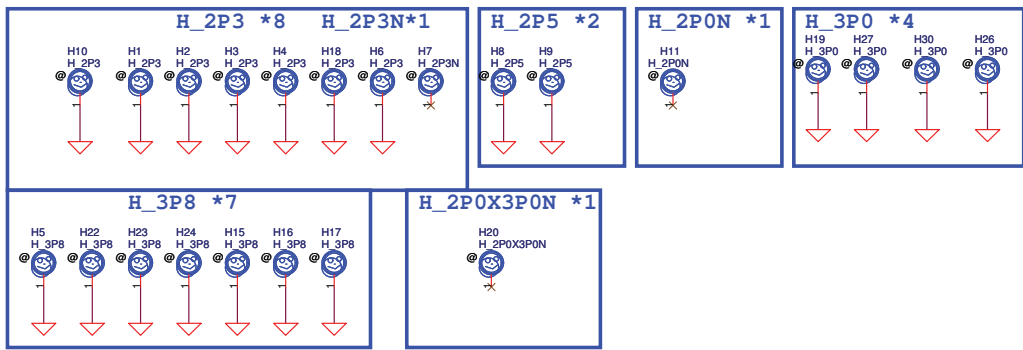
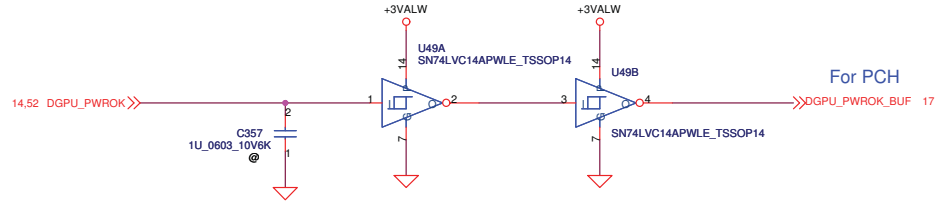
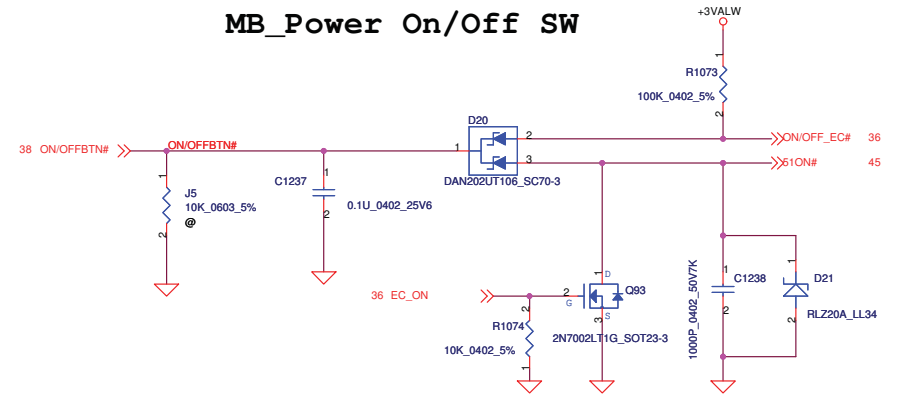
Touch pad Connector



Power ON Circuit

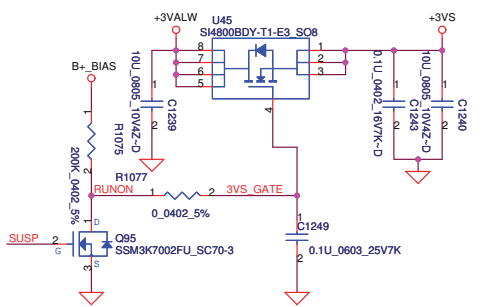


MB_Power On/Off SW

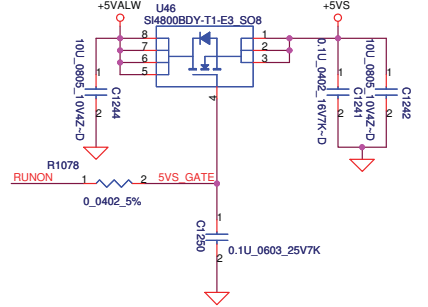


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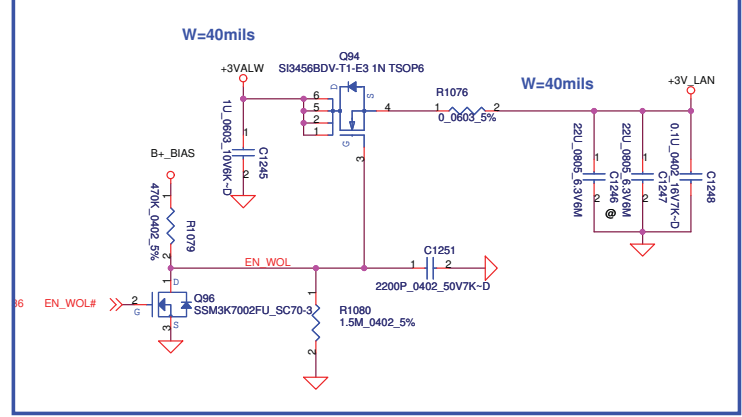
+3VALW to +3VS Transfer



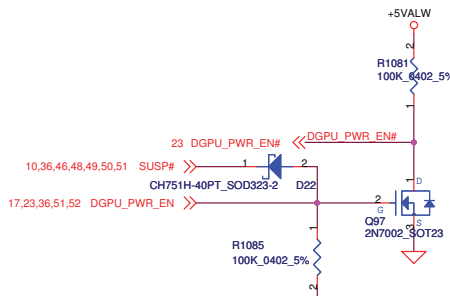
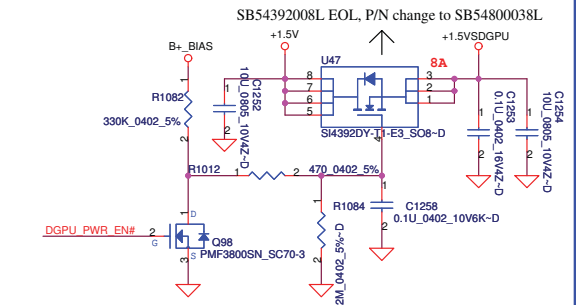
+5VALW to +5VS Transfer



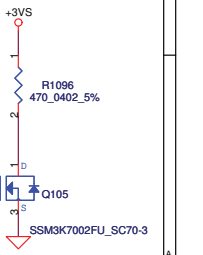
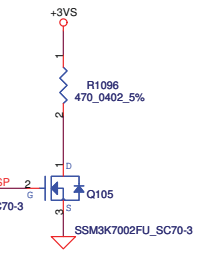
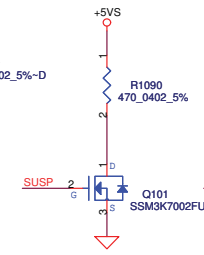
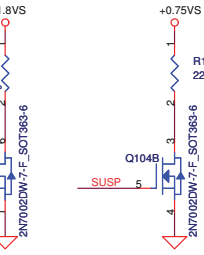
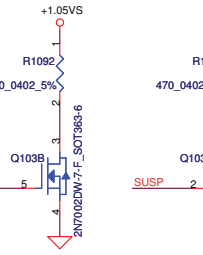
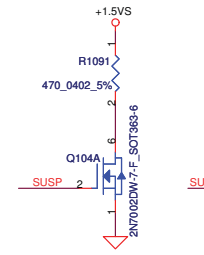
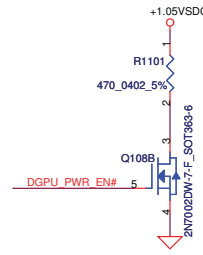
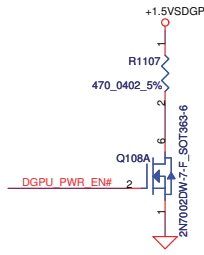
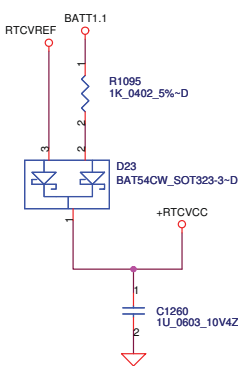
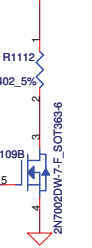
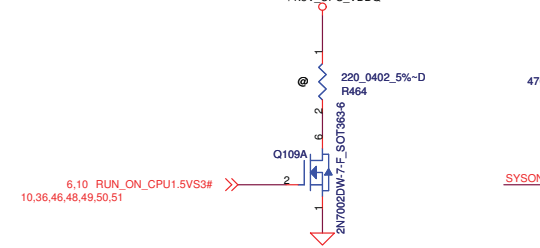
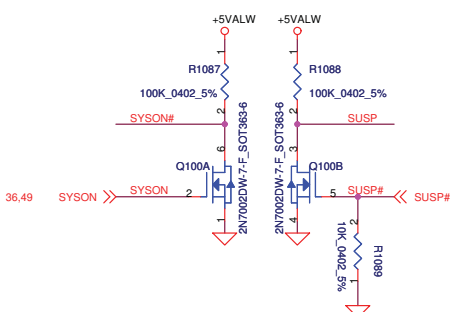
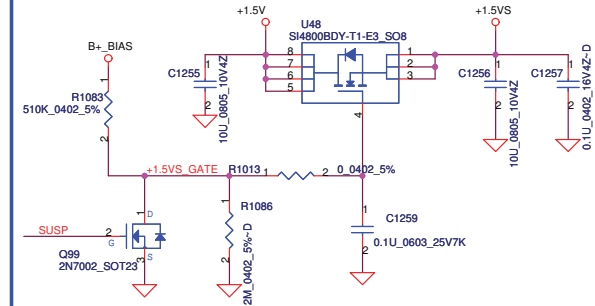
+3VALW to +3LAN Transfer



+1.5V to +1.5VSDGPU Transfer



+1.5V to +1.5VS Transfer



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Title	DC/DC INTERFACE		
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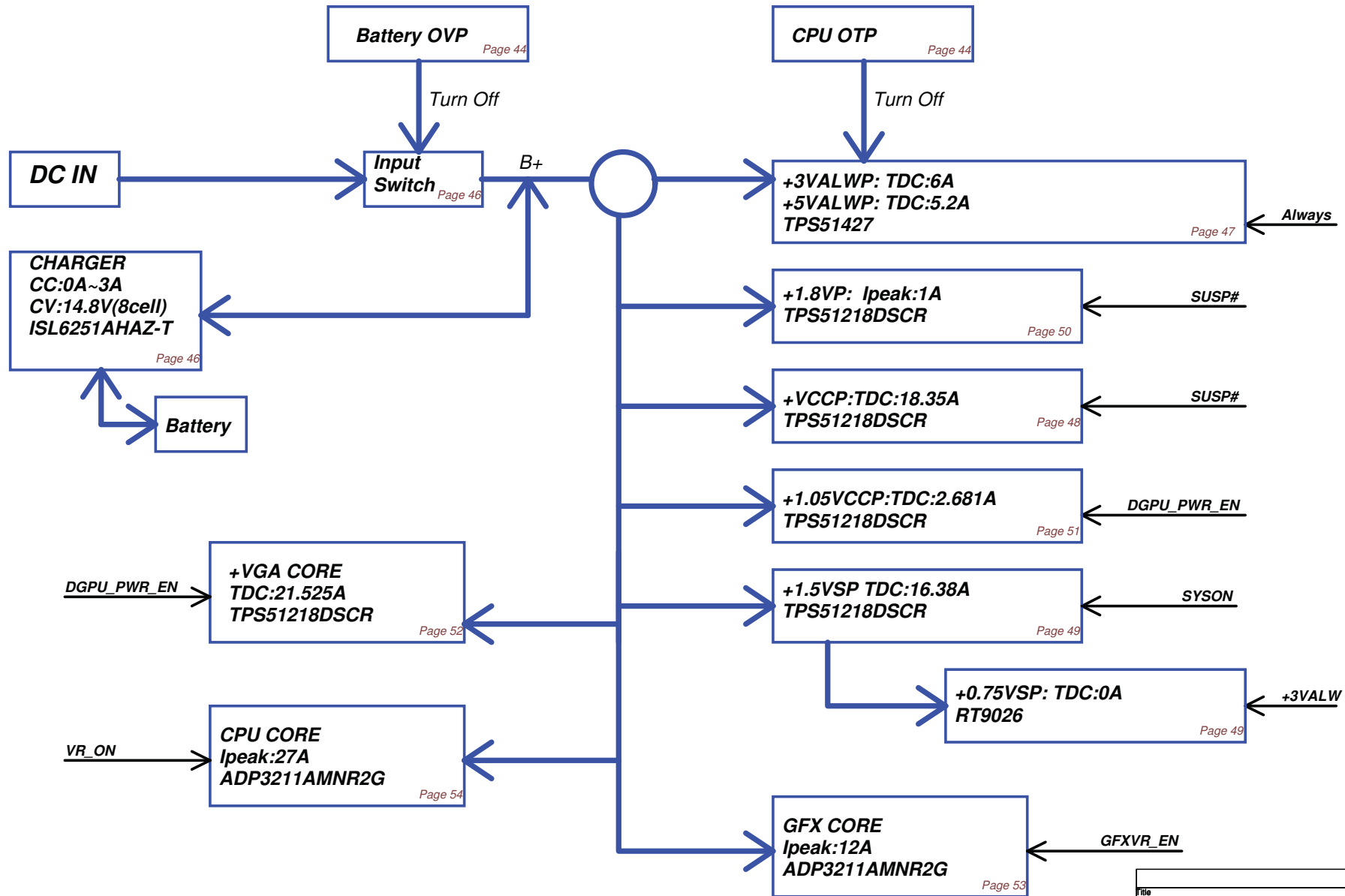
Item	Reason for change	PG#	Modify List	Date	Phase
1	The S3 status power +3VS leakage	17	Change C1151 to +3VS	2009/12/17	PT
2	The NV vender request	23	Add R472 to link +3Vs_Delay and U11 pin AA9,AB9,W9,Y9	2009/12/17	PT
3	The NV vender request	23	Add C443	2009/12/17	PT
4	The power +VCC_CORE can't up	10	Add R226,R227 H_DPRSLEVR Pull up,Pull down	2009/12/17	PT
5	The power +VCC_CORE can't up	10	Add R225,R228 H_PSI# Pull up,Pull down	2009/12/17	PT
6	The EA LVDS Part	29	Change BOM R439 from 330ohm to 110ohm	2009/12/21	PT
7	The DGPU_PWR_EN signal to PCH	36	Add R614 to U39	2009/12/21	PT
8	WLAN can't detect	14	Change BOM R186 from 10Kohm to reserve	2009/12/21	PT
9	Audio can't detect	19	Add R184,R183	2009/12/21	PT
10	Signal GFX_VR_ON spike noise	10	Change BOM R104 from 10Kohm to 470ohm	2009/12/21	PT
11	The power request MAINPWON del EC control	36	Del MAINPWON FOR EC Command	2009/12/21	PT
12	Add CP_SEL Function decter for 65W or 90W adapter	36	Add CP_SEL link to U39	2009/12/21	PT
13	Intel request 10uf need to 16 pice	9	Add C115	2009/12/21	PT
14	SUS_PWR_ACK signal double Pull high	15	Del R195	2009/12/21	PT
15	DP power change +3vs_delay	31	Change +3vs_delay to R469 pin1 ,U82 Pin14	2009/12/21	PT
16	Intel request PCH check list need to pull high	15	ADD R218 for PCH_DP_DDC_CLK signal,	2009/12/24	PT
17	Intel request PCH check list need to pull high	15	ADD R219 for DDC2_CLK signal	2009/12/24	PT
18	Intel request PCH check list DP solution	15	Change R467 to +3vs ,R468 to GND	2009/12/24	PT
19	PCH Check list TPM_ID0,TPM_ID1 pull high to +3ALW -->+3VS	17	Change R1147 pin 2 ,R1157 to +3VS	2009/12/24	PT
20	Modify screw H5,H10,H27,H30,H19,H26,H18,H25,H31,H32 for ME request	39	change H5,H10,H27,H30,H19,H26,H18,H25,H32,H31	2009/12/24	PT
21	The power +1.5V_CPU_VDDQ change to EC control	6	Change 0ohm from R223 to R224	2009/12/24	PT
22	The signal VGA_CLKREQ# double control	12	Change BOM R154,Q8 to reserve	2009/12/24	PT
23	The DP vendor request	31	Add R1236,R1237	2009/12/24	PT
24	The EC_SMI# signal double pull up	36	Del R599	2009/12/24	PT
25	The VGA_CLKREQ#_R signal double pull up	11	Del R339	2009/12/24	PT
26	The PCH_RSMRST# signal double diod	15	Del D2 change to D26	2009/12/24	PT
27	The discharge +1.8Vs and +1.5vs change	40	Change Q103A and Q104A location	2009/12/24	PT
28	The ACIN function leakage	36	Del R613,D3	2009/12/24	PT
29	The ACIN function leakage	36	Add Q10	2009/12/24	PT
30	The RF request	4	Add C1186,C1187,C1188 for 47PF to CLK power	2009/12/30	PT
31	The RF request	14	Add C1078 10PF to CLK_PCI_FB signal	2009/12/30	PT
32	The RF request	16	Add C1079 10PF to PCI_MEC(CLK_PCI_EC) signal	2009/12/30	PT
33	The RF request	32	Add C1189 for 47PF to +3VS JWWANI,but notice to JWWANI connector space	2009/12/30	PT
34	The RF request	38	Add C1200,C1201 to U41 Dummy pin	2009/12/30	PT
35	The BIOS request	36	Add R1113 for PCH_GPI033 to EC pin25	2009/12/30	PT
36	The EA SPI Fail	13	Change R593 15ohm for PCH_SPI_CLK	2009/12/30	PT
37	The EMI request	29	Change R458,R459 to L5,L7 sm01001710	2009/12/30	PT
38	ADD R599 to CP_SEL signal pull high	36	ADD R599 to CP_SEL signal	2010/01/04	PT
39	The NV vender request	23	ADD R458 pull down	2010/01/04	PT
40	The NAP10 Request	38	The ELC chip U41 pin8 select +5vs and +5VALW ADD R1185,R1186	2010/01/04	PT
41	The EC part need board ID	36	Change BOM R581 to 100Kohm	2010/01/04	PT
42	The EC part need board ID	36	Change BOM R584 to 9.09Kohm	2010/01/04	PT
43	The EC part need board ID	36	Change BOM R583 from 0ohm to reserve	2010/01/04	PT
44	The power +VCC_CORE add bulk for power request	10	Change BOM C117 add 470uF	2010/01/04	PT
45	The power +VCC_GFXCORE add bulk for power request	9	Change BOM C181 add 330uF	2010/01/04	PT
46	Audio S3/S4 resum fail	13	Change BOM C1262 from 27PF to reserve	2010/01/04	PT
47	H_VITTPWRGD_B Signal	6	add R88,Change R747 connection ,and R746,R747 Change BOM reserve	2010/01/24	PT
48	Leakage +3vs	33	Change BOM R966 to Reserve	2010/02/02	PT
49	The EC part need board ID	36	Change BOM R584 to Reserve	2010/02/05	PT
50	The EC part need board ID	36	Change BOM R585 to 20Kohm	2010/02/05	PT
51	Signal DGPU_PWR_EN two level	17	Change BOM R1148 to reserve	2010/02/10	ST
52	Signal EC_SCI# Pull high	36	Change BOM R601 to Reserve	2010/02/10	ST
53	Signal GPIO0 dual Pull high	17	Remove R1163	2010/02/10	ST
54	HDMI EA TEST	30	Change BOM D8 3CS00004000	2010/02/10	ST
				2010/02/22	ST

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Issued Date	2009/07/25	Deciphered Date	2010/07/25			
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					LA-5812P	1.0
Date:				Monday, May 10, 2010	Sheet	41 of 55

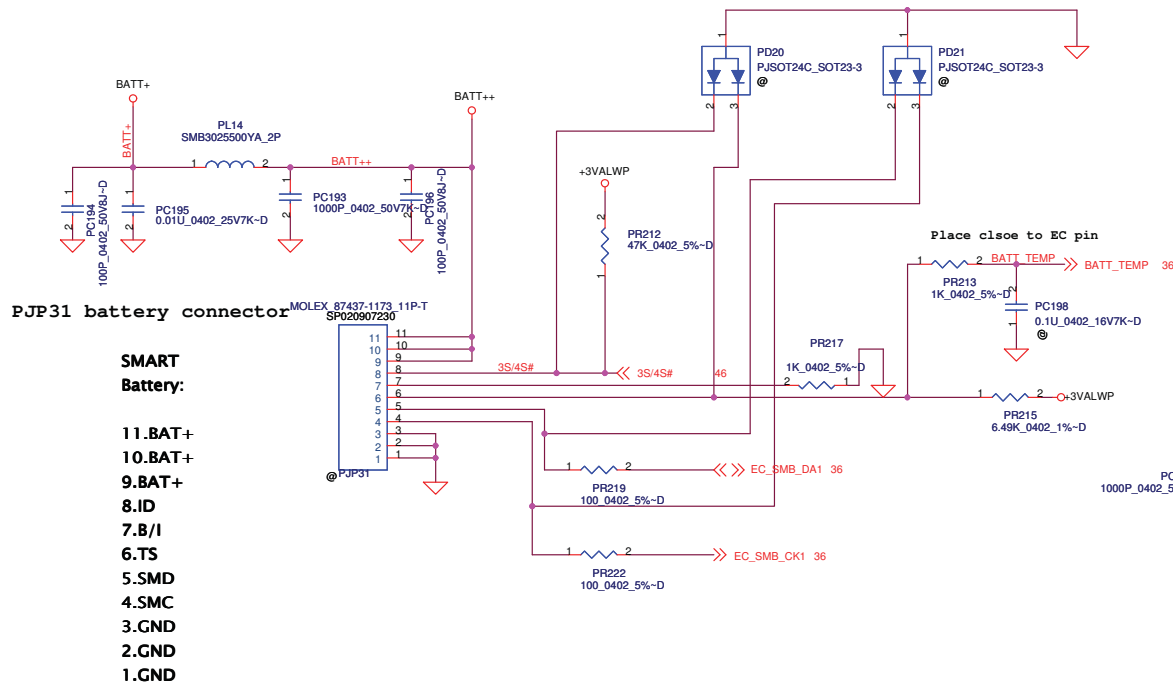
Item	Reason for change	PG#	Modify List	Date	Phase
55	HDMI detector low	17	Add R131 1Kohm	2010/02/22	ST
56	The 1394 and card reader function change to JMB380C	34	Change BOM U33 to SA000023A20	2010/02/23	ST
57	The 1394 and card reader function change to JMB380C	34	Change BOM R980, R990, R992 to reserve	2010/02/23	ST
58	The 1394 and card reader function change to JMB380C	34	Change BOM R979 from 8.2k to 12k	2010/02/23	ST
59	SMBUS Address conflict	8	Change BOM U7 to SA00003YA0L	2010/02/26	ST
60	SMBUS Address conflict	8	Change BOM R306 to 4.7Kohm	2010/02/26	ST
61	Add Power jump to open door	39	Add J5	2010/03/01	ST
62	Detect DP type	16	Add R274	2010/03/01	ST
63	Detect DP type	16	Change BOM 243 to reserve	2010/03/02	ST
64	FFS_INT2 pull up	17	Add R158	2010/03/03	ST
65	Cost issue	33	Del C1150, C1151	2010/03/04	ST
66	Deep Green	14	Change BOM R186 to 10K	2010/03/09	ST
67	Change Q16 to SI7121DN for +3VS_DELAY 1380mA	23	Change Q16 from SB923010020 to SB00000KI00	2010/04/15	X-build
68	NV Fimming	23	Change R380 from SD028000080 to SD028150280	2010/05/10	X-build
69	NV Fimming	23	Change C477 to SE07010428L	2010/05/10	X-build
70	NV Fimming	23	Change R612 from SD028100180 to SD028150280	2010/05/10	X-build

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				Size	Document Number
Date: Monday, May 10, 2010				Sheet	42 of 55

Power block

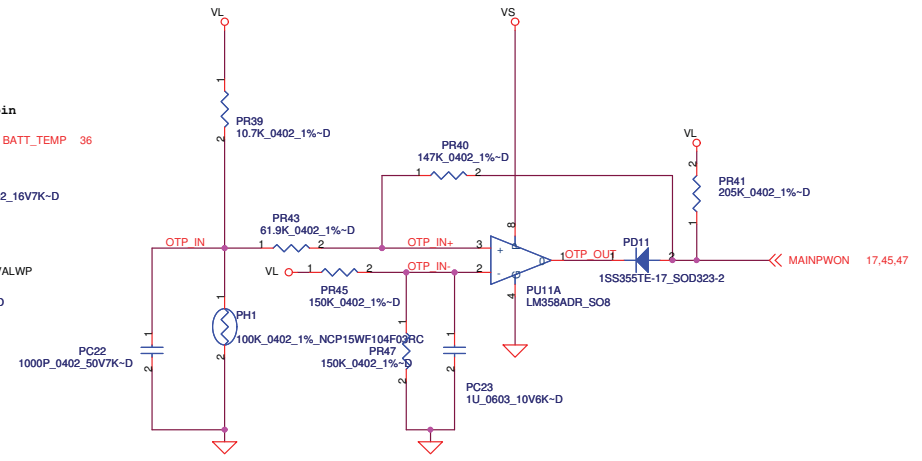


File		
POWER BLOCK DIAGRAM		
Size	Document Number	Rev
Date:	Monday, May 10, 2010	Sheet 43 of 55

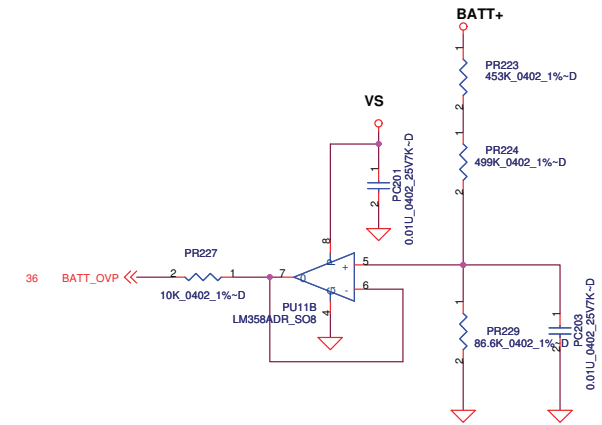
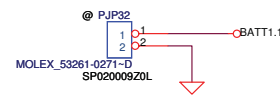
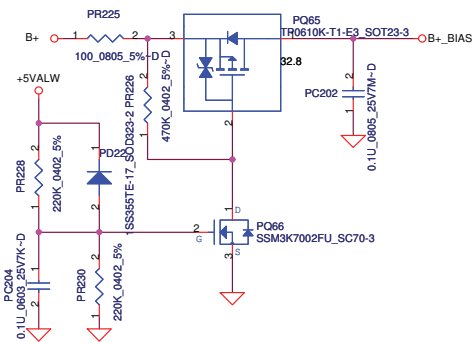


CPU OTP

PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C

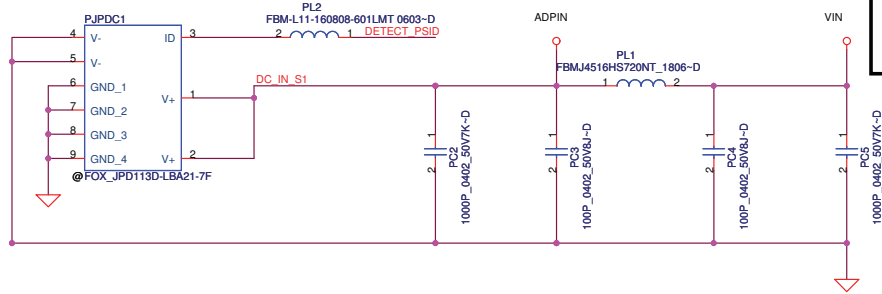


COIN RTC Battery



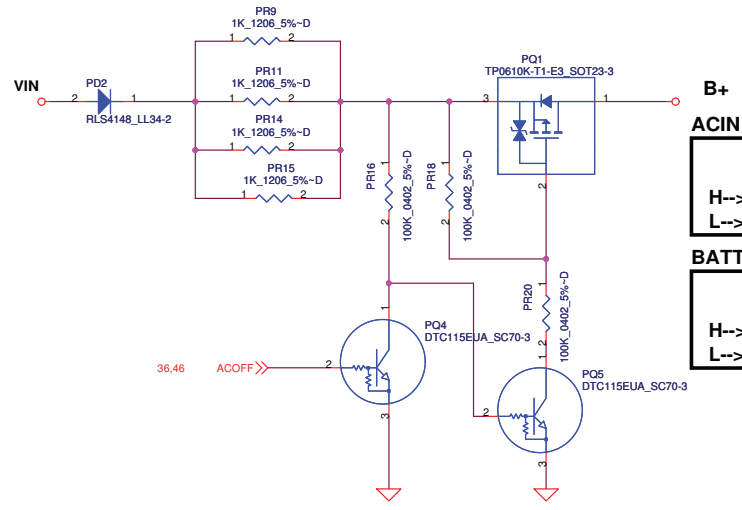
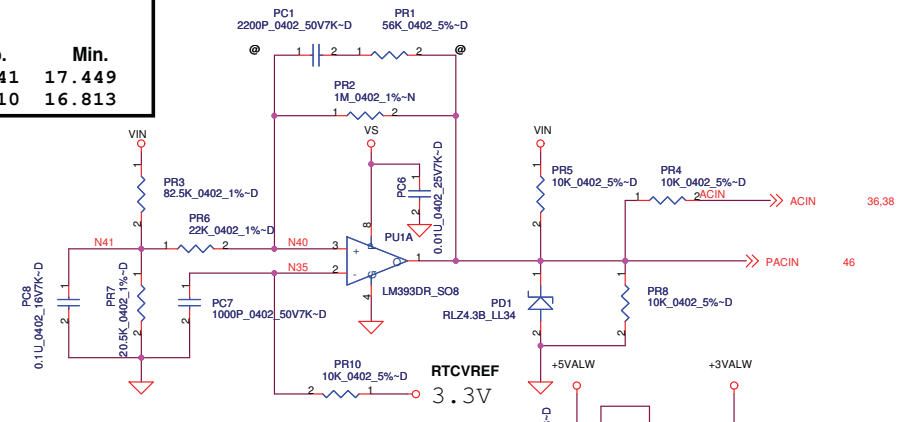
LI-3S : 13.5V----BATT-OVP=1.126V
LI-4S : 18V----BATT-OVP=1.5V
BATT-OVP=0.08338*BATT+

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Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

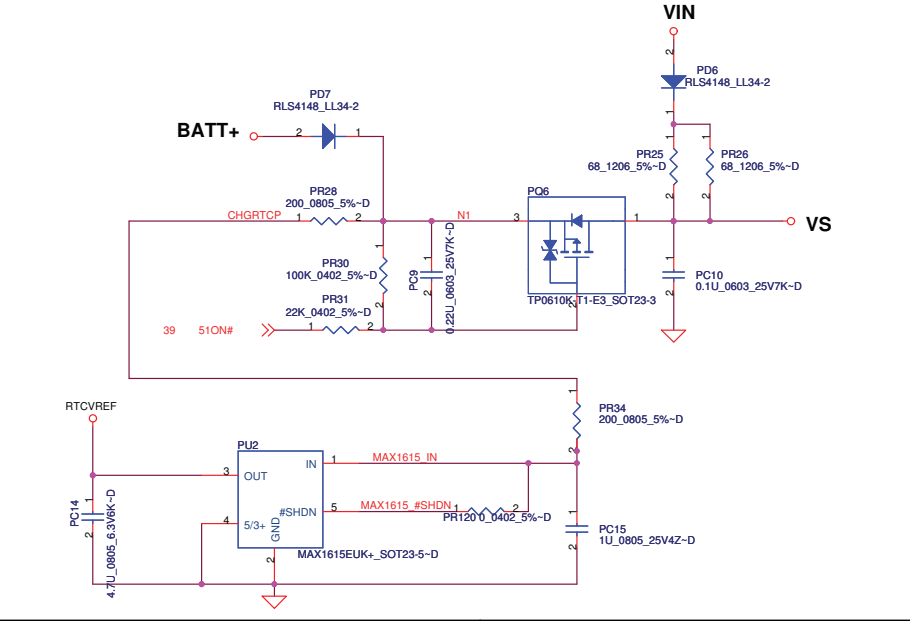
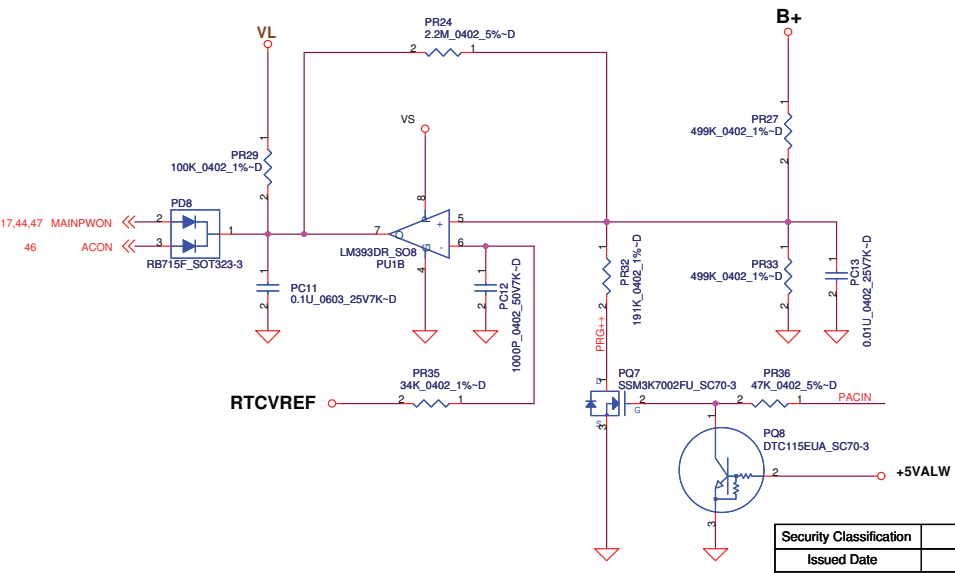
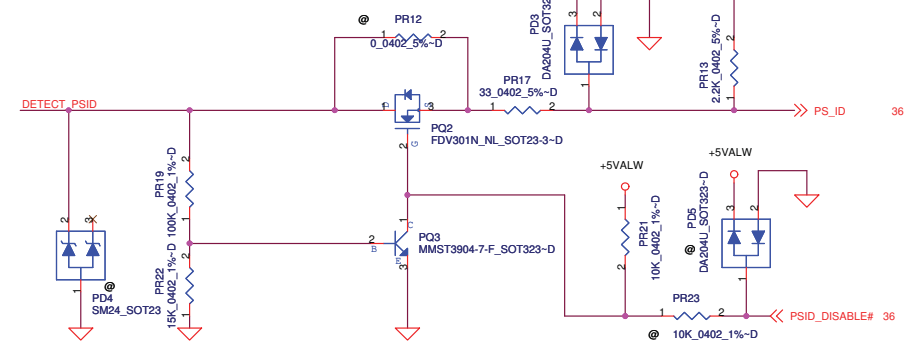


ACIN

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

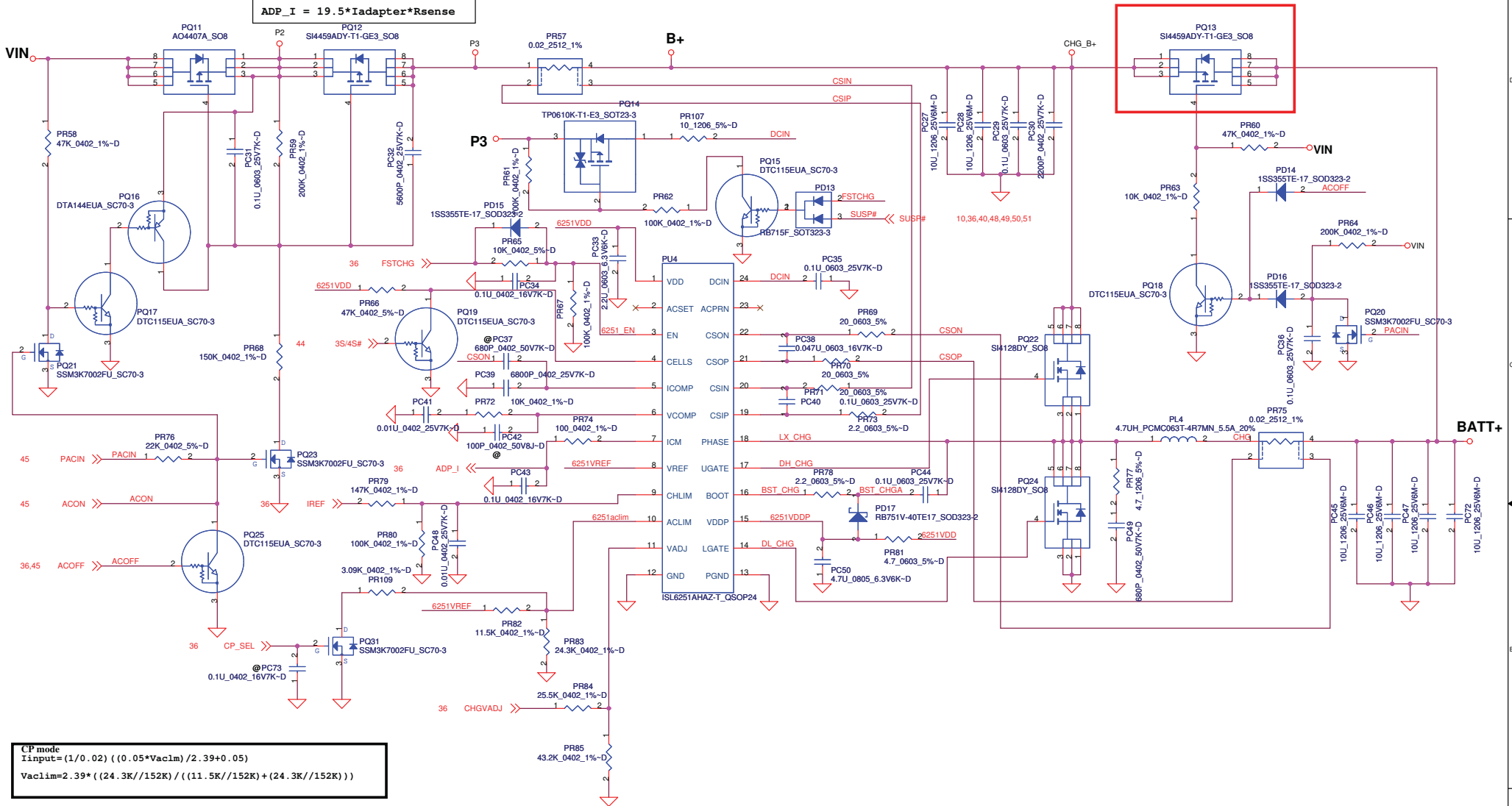
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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				DCIN & DETECTOR		
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				Customer		
Date:	Monday, May 10, 2010	Sheet	45	of 55		

Iada=0~4.62A (90W)

$$ADP_I = 19.5 * I_{adapter} * R_{sense}$$

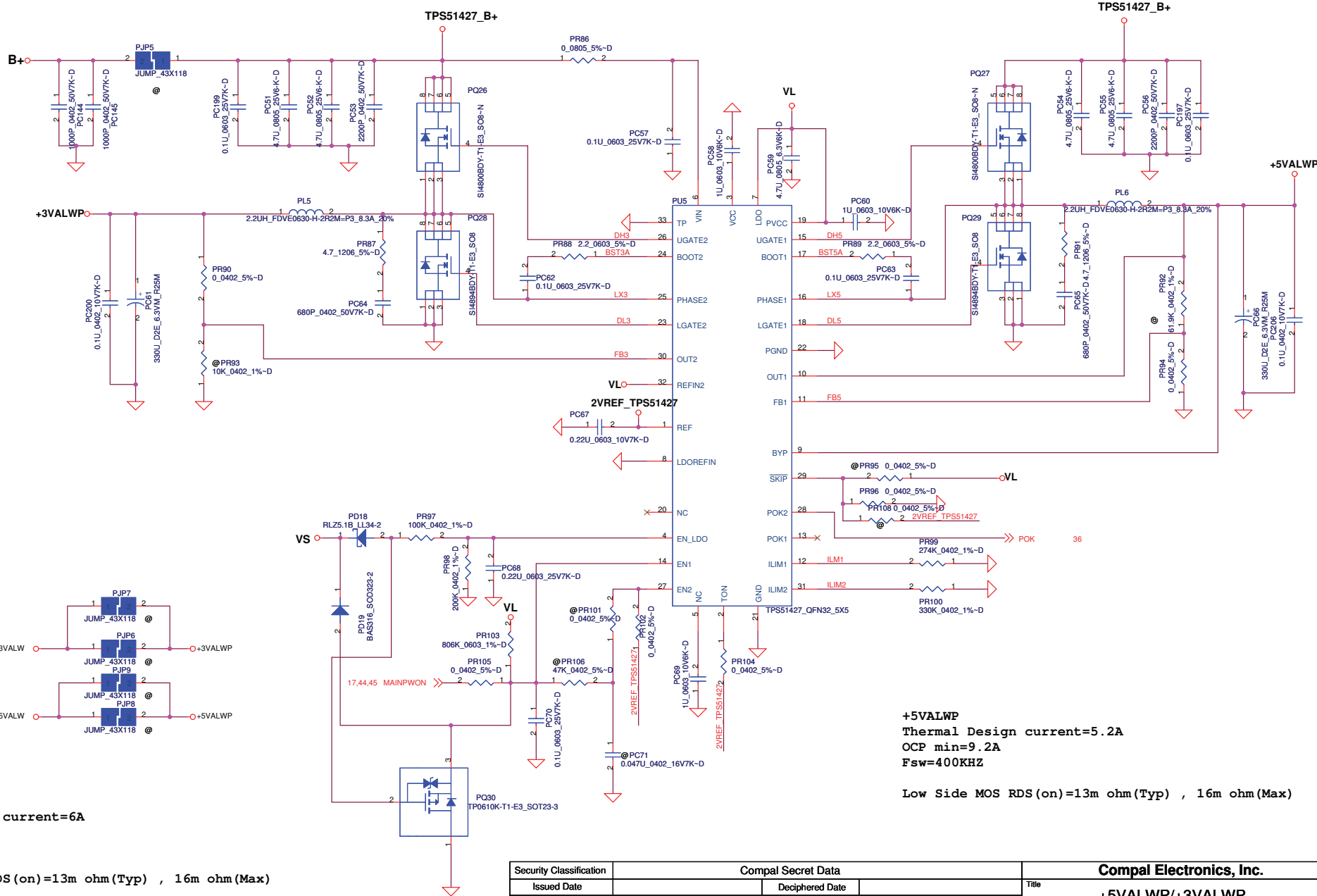


CP mode
 $I_{input} = (1/0.02) * ((0.05 * V_{acim}) / 2.39 + 0.05)$
 $V_{acim} = 2.39 * ((24.3K / 152K) / ((11.5K / 152K) + (24.3K / 152K)))$

CC=3.3A
 IREF=1*Icharge
 IREF=0.25V~3.3V

CHGVADJ	CV mode
0V	3.99V per cell
1.93V	4.2V per cell
3.3V	4.35V per cell

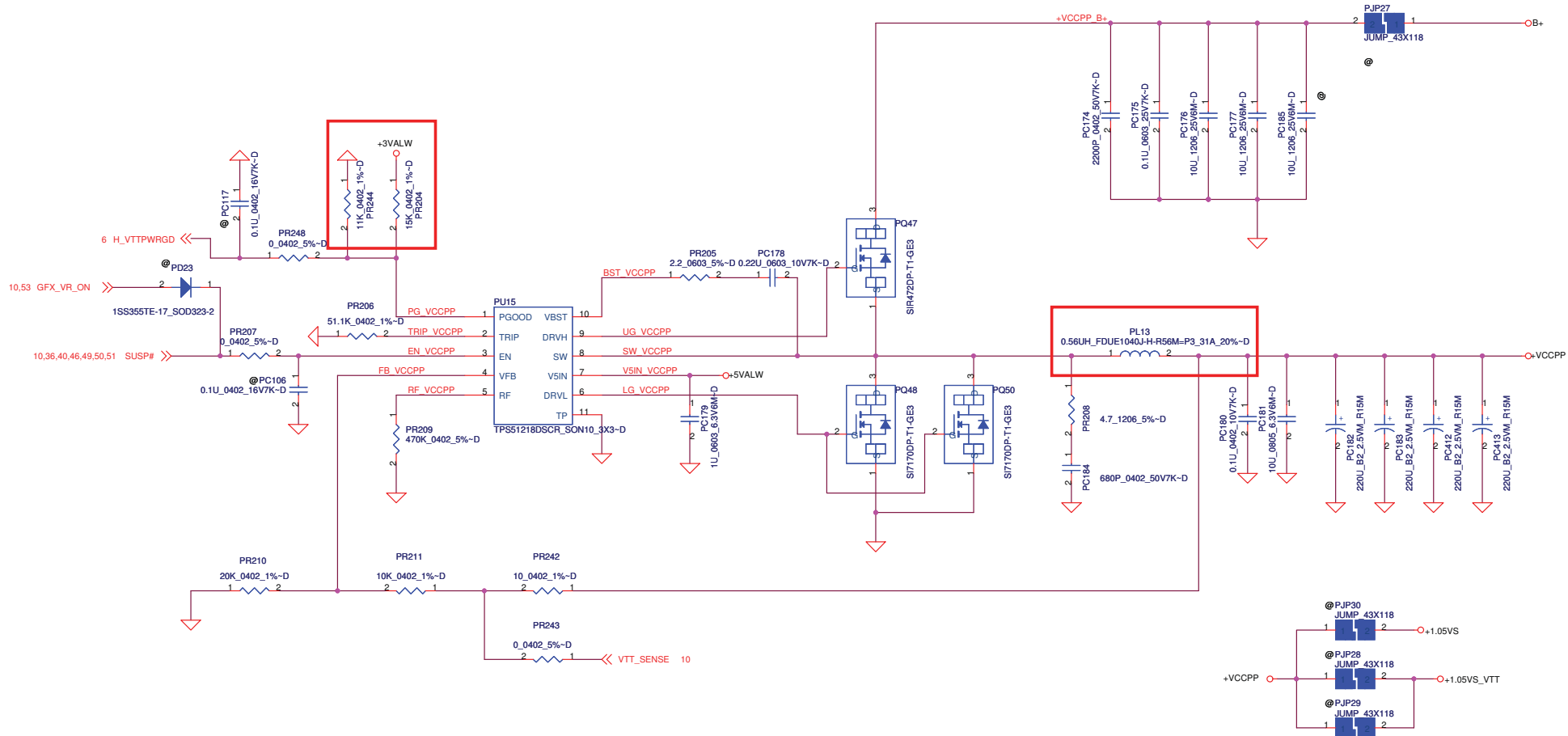
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Issued Date	Deciphered Date		Title CHARGER	
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+3.3VALWP
 Thermal Design current=6A
 OCP min=11A
 Fsw=300KHZ
 Low Side MOS RDS(on)=13m ohm(Typ) , 16m ohm(Max)

+5VALWP
 Thermal Design current=5.2A
 OCP min=9.2A
 Fsw=400KHZ
 Low Side MOS RDS(on)=13m ohm(Typ) , 16m ohm(Max)

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Date: Monday, May 10, 2010		Sheet 47 of 55		Size	Document Number	Rev
				Custom		



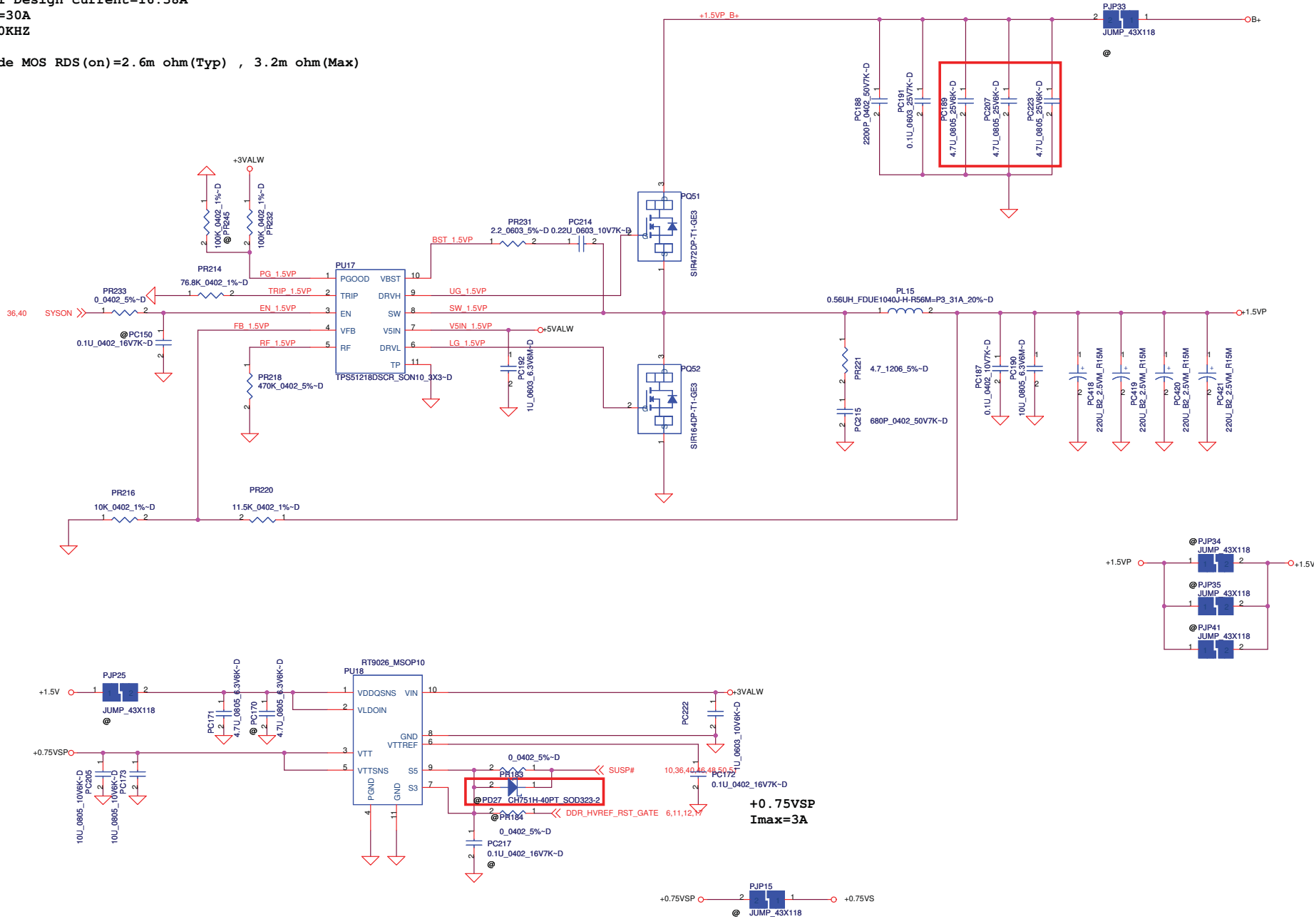
+VCCPP
 Thermal Design current=18.35A
 OCPmin=27.5A
 Fsw=290KHZ

Low Side MOS RDS(on)=1.8m ohm(Typ) , 2.25m ohm(Max)

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Issued Date		Deciphered Date		+VCCPP		
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				Custom		
				Date:	Monday, May 10, 2010	Sheet 48 of 55

+1.5VP
Thermal Design current=16.38A
OCPmin=30A
Fsw=290KHZ

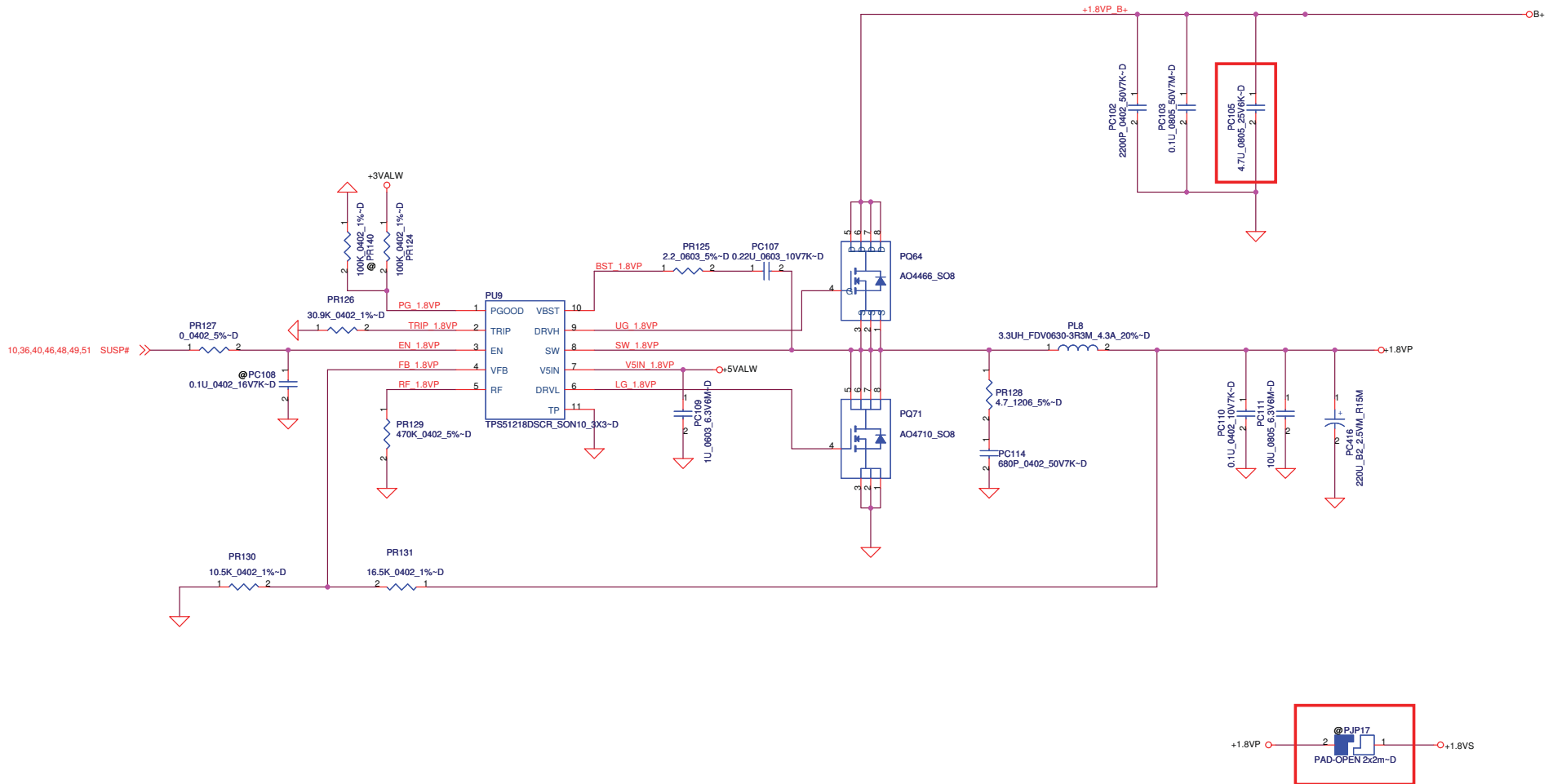
Low Side MOS RDS(on)=2.6m ohm(Typ) , 3.2m ohm(Max)



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				Date:	Monday, May 10, 2010	Sheet 49 of 55

+1.8VP
 Thermal Design current=1A
 OCPmin=3A
 Fsw=290KHZ

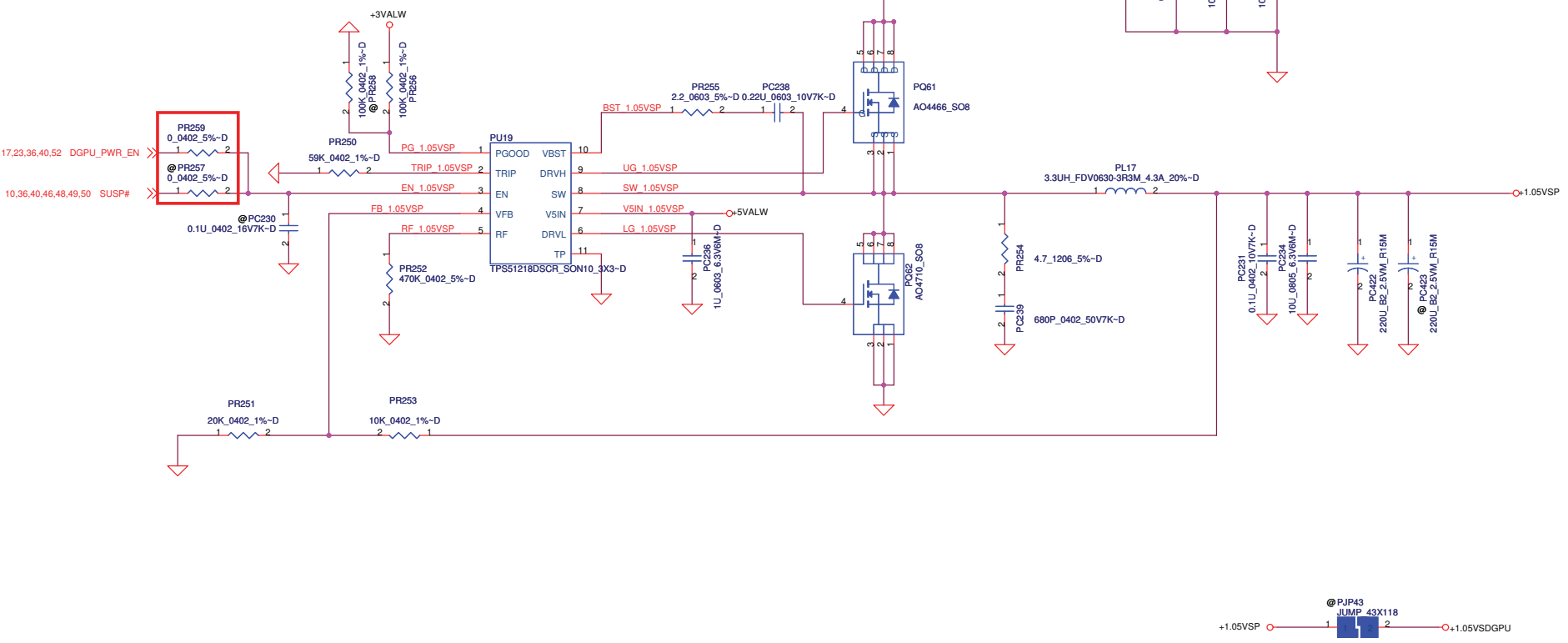
Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)



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Size	Document Number	Rev			
Date:	Monday, May 10, 2010	Sheet	50	of	55

+1.05VSP
 Thermal Design current=2.681A
 OCPmin=5A
 Fsw=290KHZ

Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)

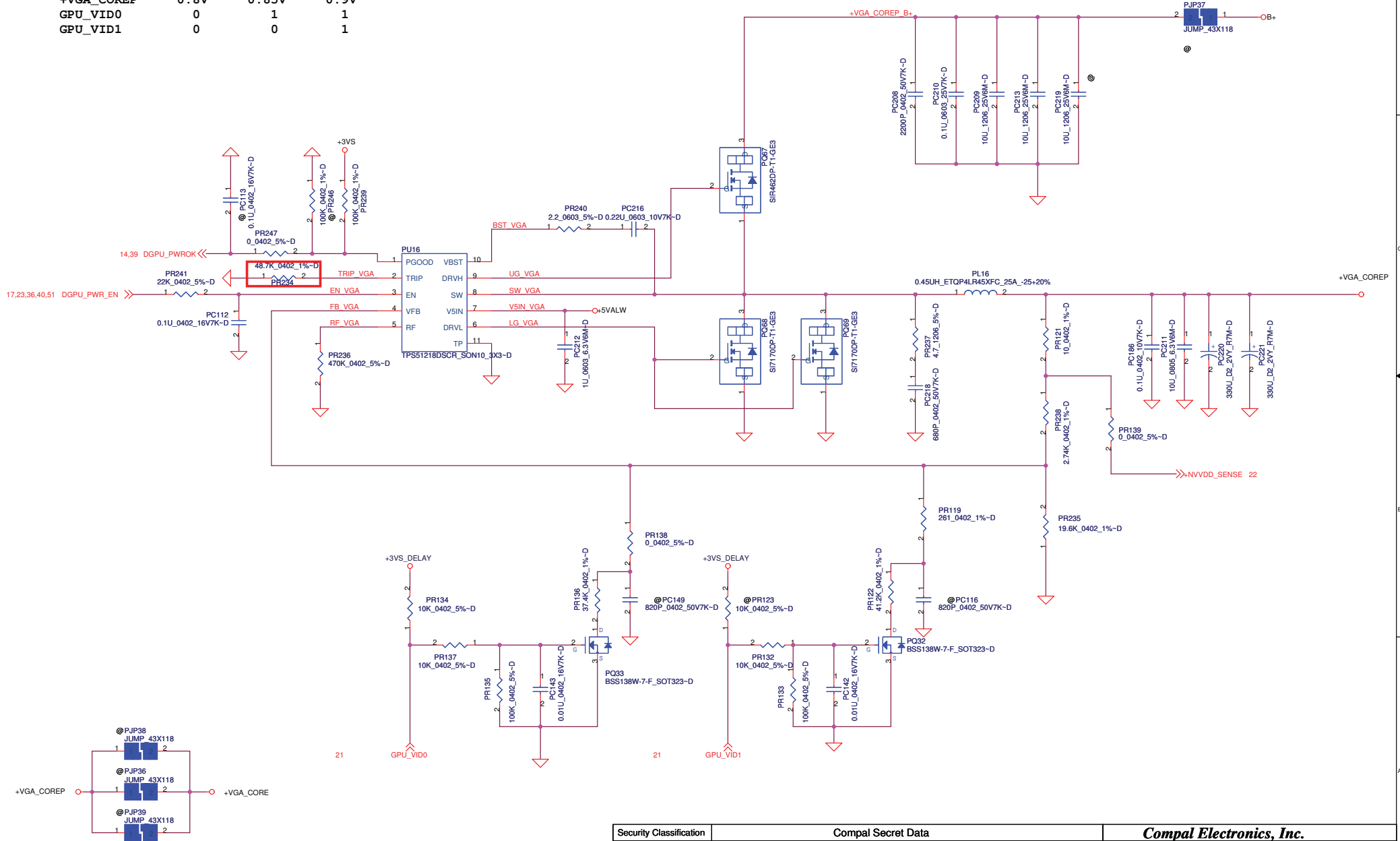


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+VGA_COREP
 ThermalDesignCurrent=21.525A
 OCPmin=36.9A
 Fsw=290KHZ
 Low Side MOS RDS(on)=1.8m ohm(Typ) , 2.25m ohm(Max)

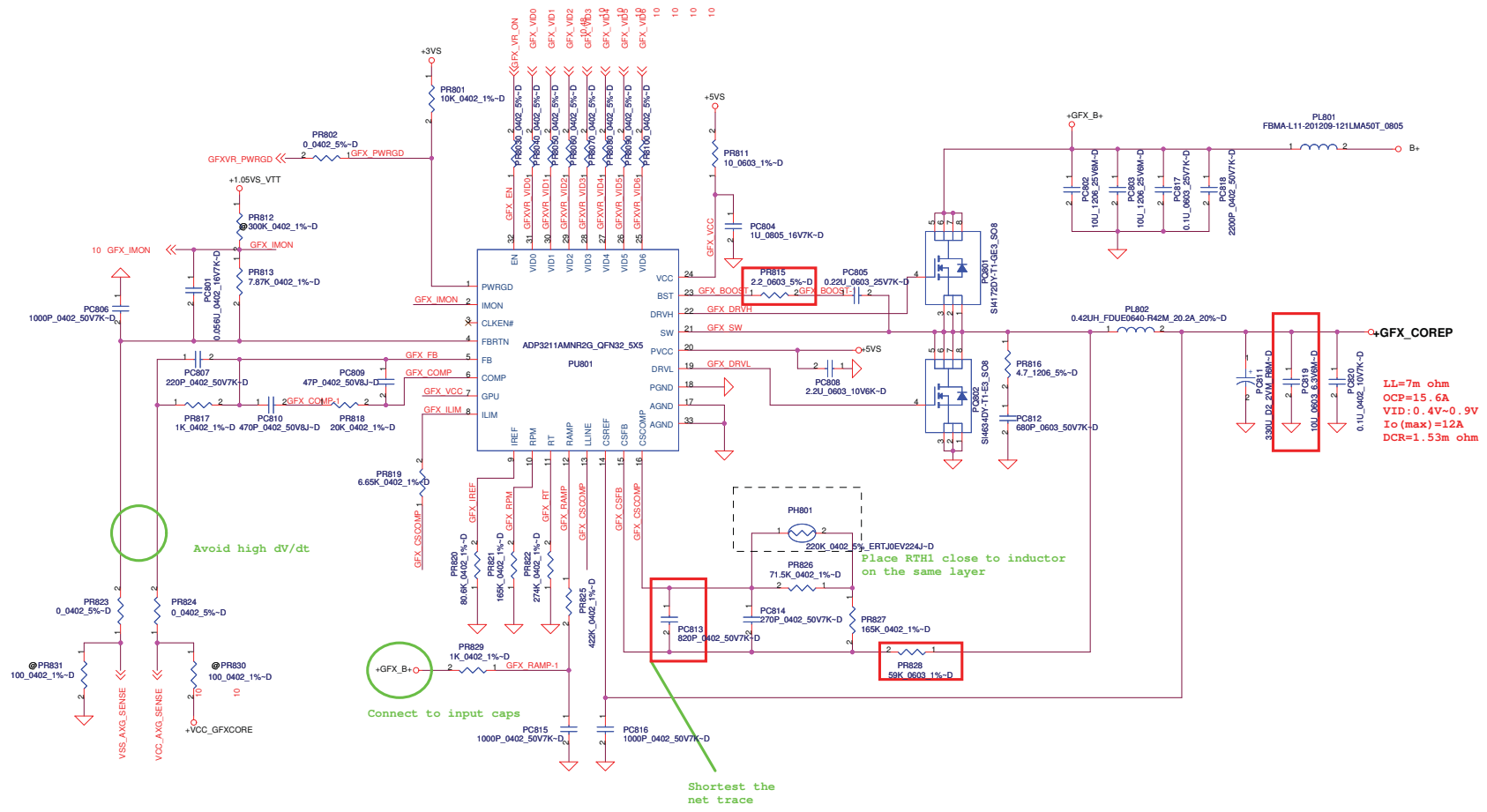
+VGA_COREP (N11P_GS1) PR122=41.2K ohm

+VGA_COREP	0.8V	0.85V	0.9V
GPU_VID0	0	1	1
GPU_VID1	0	0	1

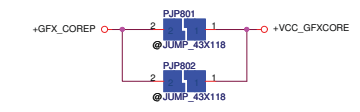


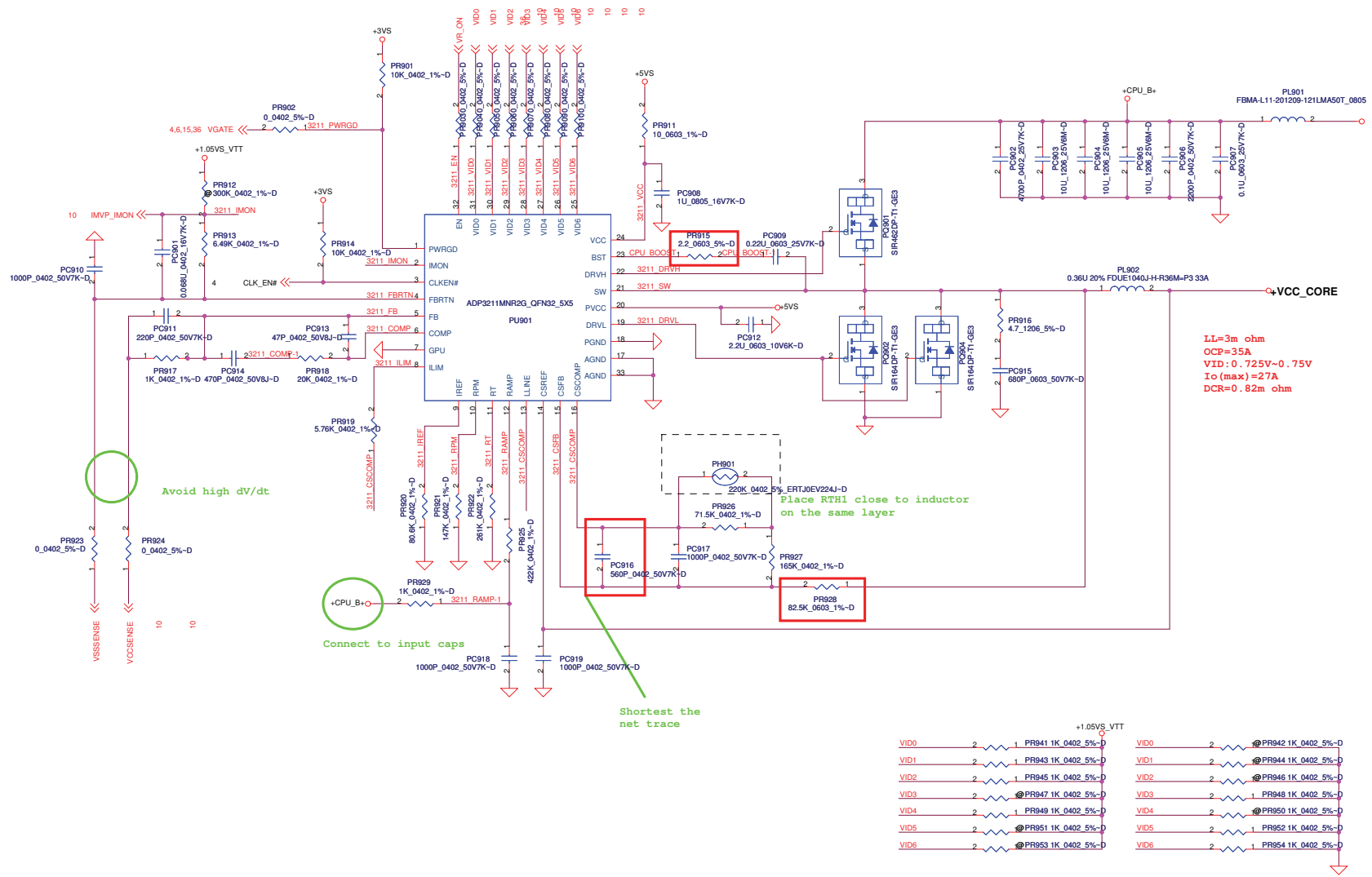
<http://hobi-elektronika.net>

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$L_L = 7m\ \text{ohm}$
 $OCP = 15.6A$
 $VID = 0.4V - 0.9V$
 $I_o(\text{max}) = 12A$
 $DCR = 1.53m\ \text{ohm}$





Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	CHARGER	09/12/16	COMPAL	add current rating	change PQ13 from SB00000DL00 to SB00000I600	0.2
2	48	+VCCPP	09/12/16	COMPAL	adjust VTPWRGD voltage rating	change PR204 from 100k to 15k and PR244 from 100k to 11k	0.2
3	53	GFX_CORE	09/12/16	COMPAL	adjust apposite MLCC size	change PC819 from SE153106K8L to SE000005T8L	0.2
4	51	+1.05VP	09/12/26	COMPAL	change enable signal for HW request	del PR257, add PR259 0 ohm	0.2
5	53	GFX_CORE	09/12/28	COMPAL	change resister for RF request	change PR815 from 0 to 2.2	0.2
6	54	CPU_CORE	09/12/28	COMPAL	change resister for RF request	change PR915 from 0 to 2.2	0.2
7	52	VGA_CORE	10/01/04	COMPAL	adjust VGA OCP point	change PR234 from 69.8k to 48.7k	0.2
8	54	CPU_CORE	10/01/04	COMPAL	adjust loadline	change PR928 from 60.4k to 82.5k	0.2
			10/01/04	COMPAL	adjust time-constant	change PC916 from 1000p to 560p	0.2
9	53	GFX_CORE	10/01/04	COMPAL	adjust loadline	change PR828 from 47.5k to 59k	0.2
			10/01/04	COMPAL	adjust time-constant	change PC813 from 1000p to 820p	0.2
10	48	+VCCPP	10/02/04	COMPAL	raise choke current rating	change PL13 from SH05056BM00 to SH00000I20L	0.3
11	49	+1.5VP/+0.75VSP	10/02/04	COMPAL	raise choke current rating	change PL15 from SH05056BM00 to SH00000I20L	0.3
12	49	+1.5VP/+0.75VSP	10/02/25	COMPAL	speaker interfere	change PC189 PC207 from SE142106M8L to SE000006R8L and add PC223	0.3
13	50	+1.8VP	10/02/26	COMPAL	HDD connect interfere	change PC105 from SE142106M8L to SE000006R8L and del PC115	0.3
14	44	BATTERY CONN/OTP	10/04/12	COMPAL	adjust OTP trigger point for thermal request	change PR39 from SD03410728L to SD03480618L	0.4
15	52	VGA_CORE	10/05/10	COMPAL	adjust time sequence for EE request	change PR241 from 220 to 22k	

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				PWR-PIR		
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