

Key West Block Diagram

Project code: 91.4D901.001
 PCB P/N : 48.4D901.0SD
 REVISION : 05209-SD

CLK GEN³
 ICS954226AG

SB

4,5
Mobile CPU
 Celeron/Dothan

6,7,8,9,10
Alviso
 GML

15,16,17,18
ICH6-M

DDRII*2
 400MHz
 11,12

LVDS
 LCD¹³

RGB CRT
 CRT¹⁴

25
 Mini-PCI
 802.11a/b/g

22
 RJ45
 CONN

21
 10/100 BCM4401

22
 RJ11
 CONN

26
 MODEM
 MDC 1.5 Card

SB

AZALIA

24
 LINE OUT

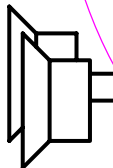
24
 OP AMP
 MAX4411

24
 MIC IN

23
 AC'97 CODEC
 STAC9200

24
 OP AMP
 TPA6017

SB



2CH SPEAKER

27
 KBC
 H8S/RE144AV
 SC

29
 FlashRom
 4Mb
 (S12kB)

19
 Thermal Sensor
 & Fan
 ENC 6N300
 SB

28
 Touch
 Pad

28
 Int.
 KB

SYSTEM DC/DC MAX8734A ³³	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S3

SYSTEM DC/DC TPS5130 ^{34,35}	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 1D8V_S3

MAXIM CHARGER MAX1909 ³¹	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A 5V 100mA

CPU DC/DC MAX1907 ³²	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Title: **Block Diagram**

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ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

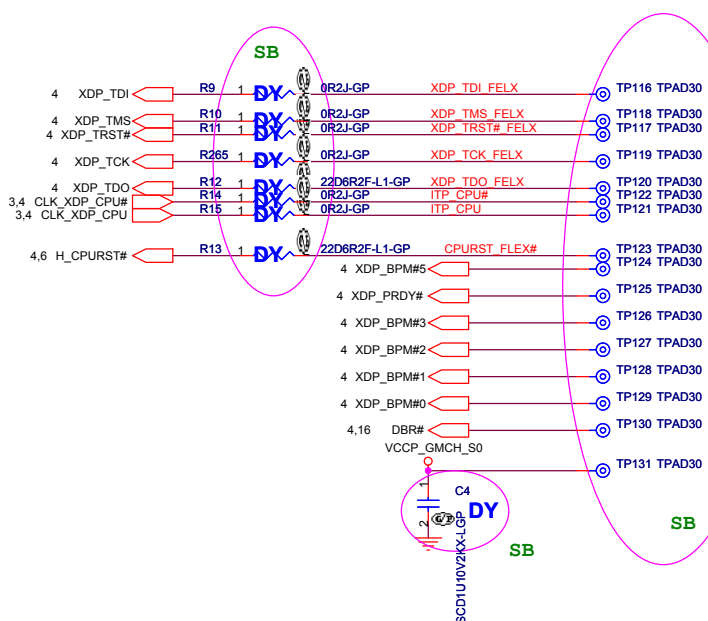
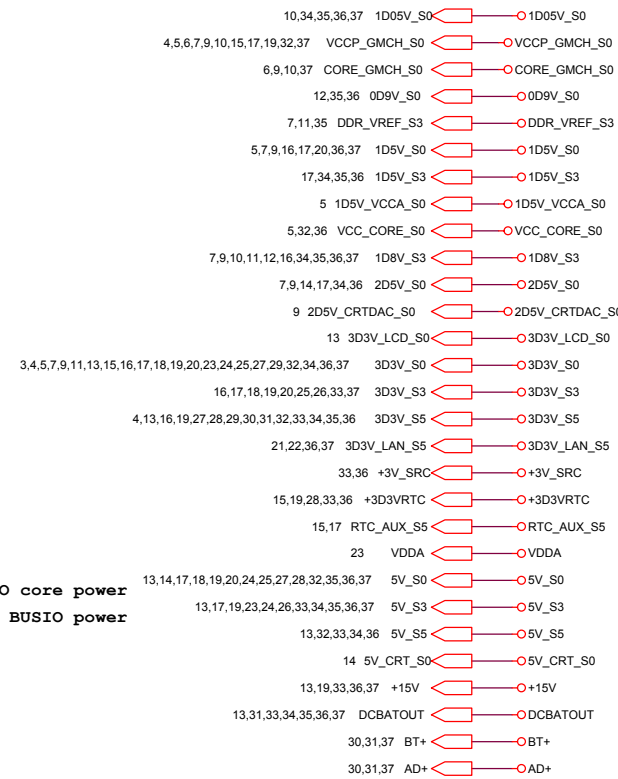
ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
 5V_S3= 5 Voltage suspend to RAM(S3 state)
 5V_S5= 5 Voltage soft off(S5 state)
 3D3V_S0= 3.3 Voltage power up on system work(S0 state)
 3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
 3D3V_S5= 3.3 Voltage soft off(S5 state)
 LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
 1D8V_S3= 1.8 Voltage suspend to RAM(S3 state)
 2D5V_S0= 2.5 Voltage power up on system work(S0 state)
 VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
 1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S0= 1.5 Voltage power up on system work(S0 state)
 1D5V_S5= 1.5 Voltage soft off(S5 state)
 DDR_VREF_S3= 0.9 Voltage suspend to RAM(S3 state)
 0D9V_S0= 0.9 Voltage power up on system work(S0 state)
 1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
 1D05V_S0= 1.05 Voltage power up on system work(S0 state)
 CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
 VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO BUSIO power



Device	SMBus addr.
Clock Gen.	D2
DDR Module 1	A0
DDR Module 2	A4
LCD	58
Guardian	5E
Battery	16
EEPROM	A2

USB Port	Key West Define
USBP[0]	USB1 Up connector
USBP[1]	New card used
USBP[2]	USB1 Down connector
USBP[3]	NC
USBP[4]	USB2 connector
USBP[5]	NC
USBP[6]	NC
USBP[7]	NC

PCIE Port	Key West Define
PE[1]	NC
PE[2]	NC
PE[3]	NC
PE[4]	New card used

PCI RESOURCE TABLE

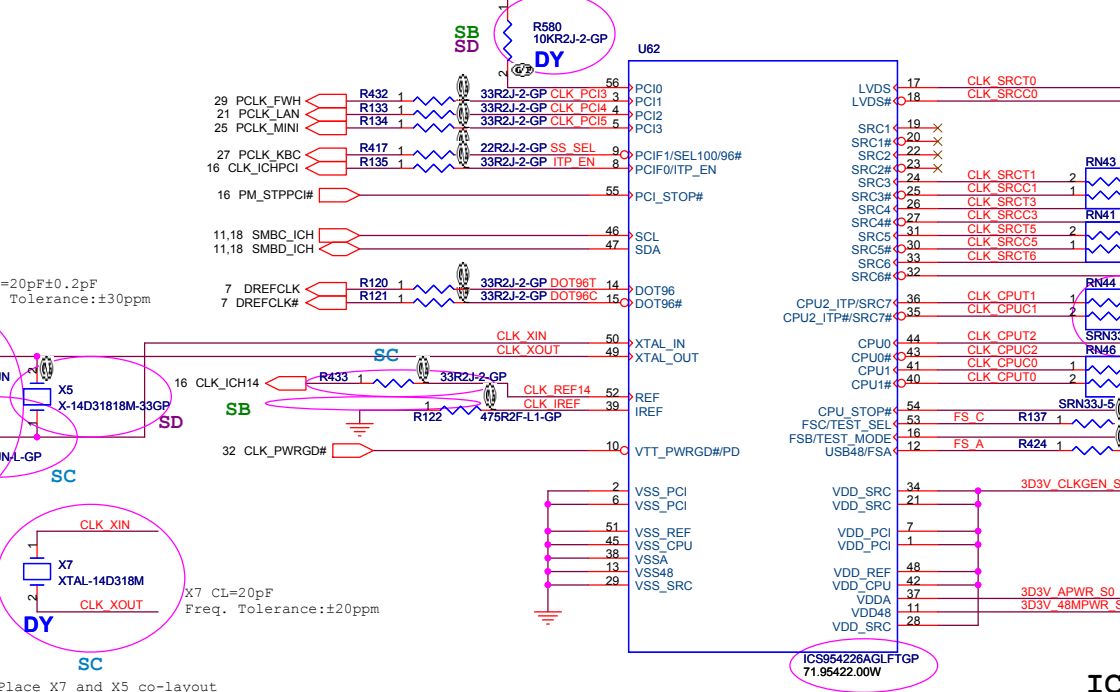
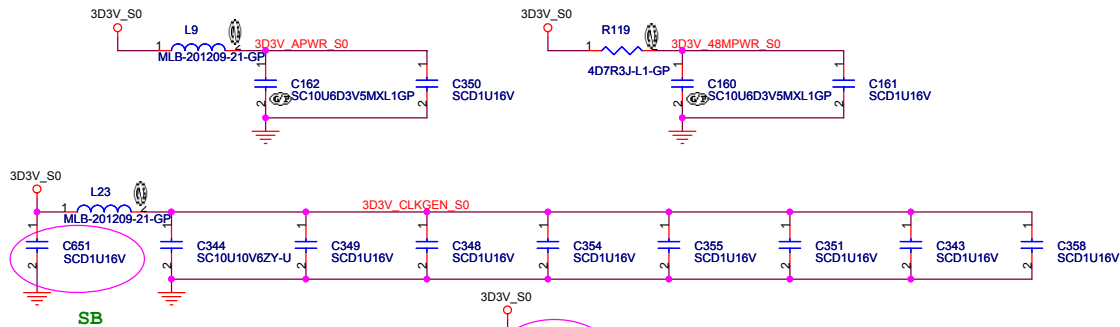
DEVICE	IDSEL	PCI IRQ	REQ#/GNT#
Mini-PCI	AD19	P_INTB# / P_INTD#	REQ3#/GNT3#
LAN	AD16	P_INTC#	REQ4#/GNT4#

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Title: **ITP**

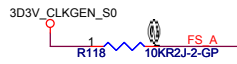
Size A3 Document Number: **KeyWest** Rev: **SD**

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Place X7 and X5 co-layout

NEAR CLKGEN



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

- 1st source: 71.95422.00W (ICS954226AGLFTGP)
- 2nd source: 71.00140.00W (IDTCV140PAG-GP)
- 3rd source: 71.28442.00W (CY28442ZXC-2T-GP)

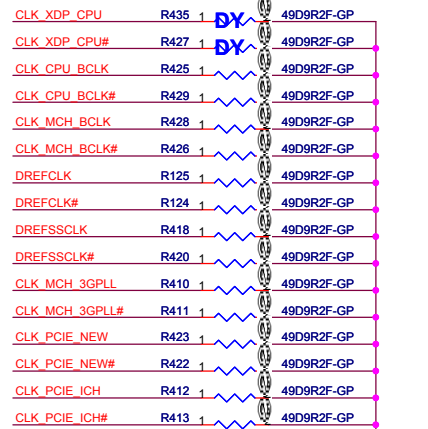
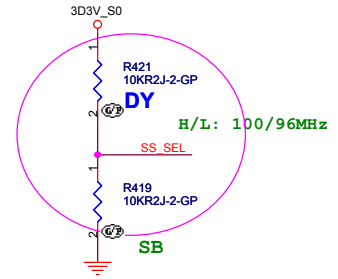
ICS954226AG Spread Spectrum Select

S3	S2	S1	S0	Spread Amount%
0	0	0	0	-0.8
0	0	0	1	-1.0
0	0	1	0	-1.25
0	0	1	1	-1.5
0	1	0	0	-1.75
0	1	0	1	-2.0
0	1	1	0	-2.5
0	1	1	1	-3.0
1	0	0	0	+/-0.3
1	0	0	1	+/-0.4
1	0	1	0	+/-0.5
1	0	1	1	+/-0.6
1	1	0	0	+/-0.8
1	1	0	1	+/-1.0
1	1	1	0	+/-1.25
1	1	1	1	+/-1.5

4.5,7,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0

Dummy R123 (up side), Mounting R136 (down side)
--SRC7 on

Mounting R136 (up side), Dummy R123 (down side)
--CPU2_ITP on



<Variant Name>

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Title: Clock Generator (ICS954226AG)		
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6 H_A#[31..3]

VCCP_GMCH_S0
2,5,6,7,9,10,15,17,19,32,37 VCCP_GMCH_S0

1st source: 62.10079.001
2nd source: 62.10053.341

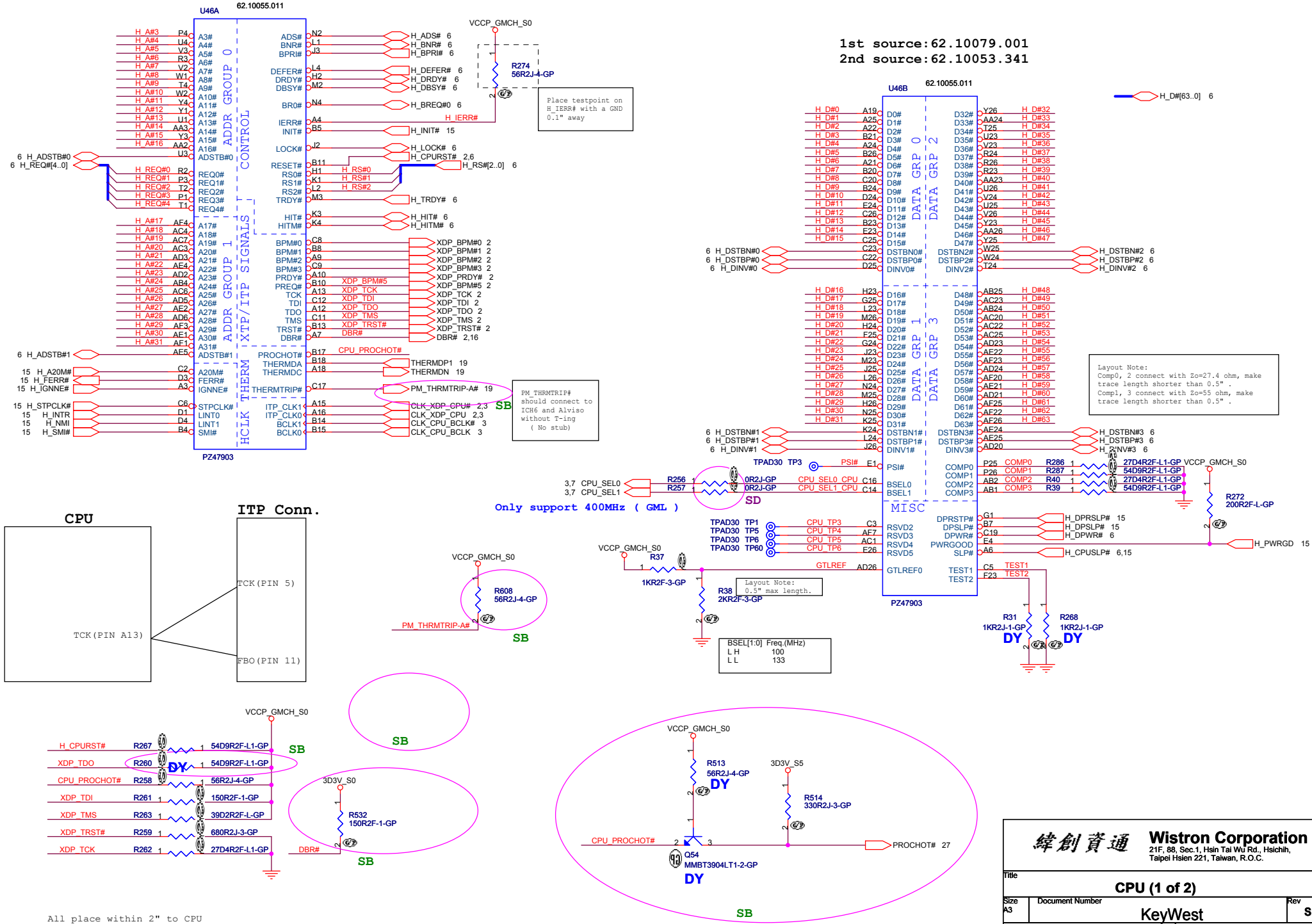
Place testpoint on H_IERR# with a GND 0.1" away

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Only support 400MHz (GML)

Layout Note:
0.5" max length.

BSEL[1:0] Freq.(MHz)	
LH	100
LL	133



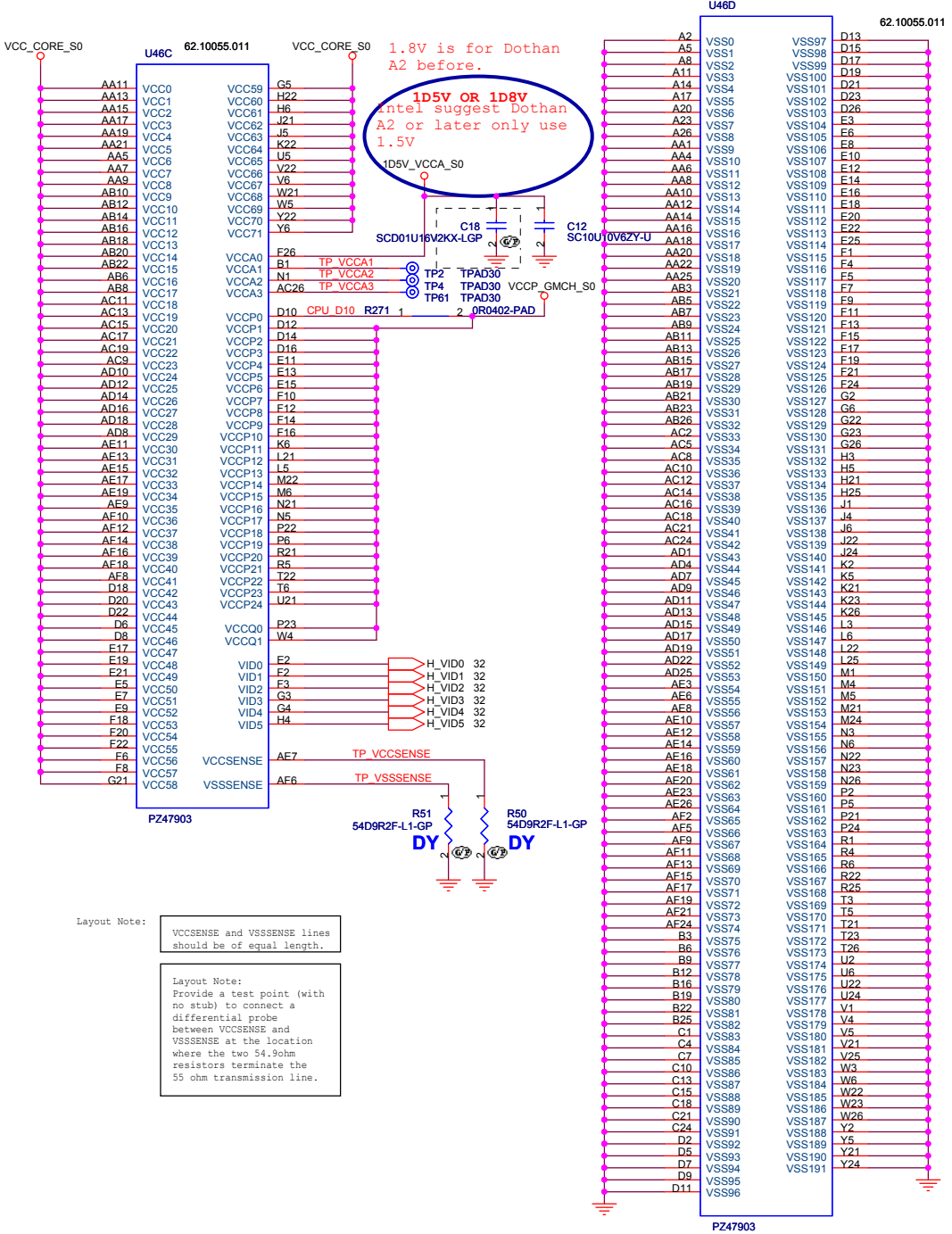
All place within 2" to CPU

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CPU (1 of 2)

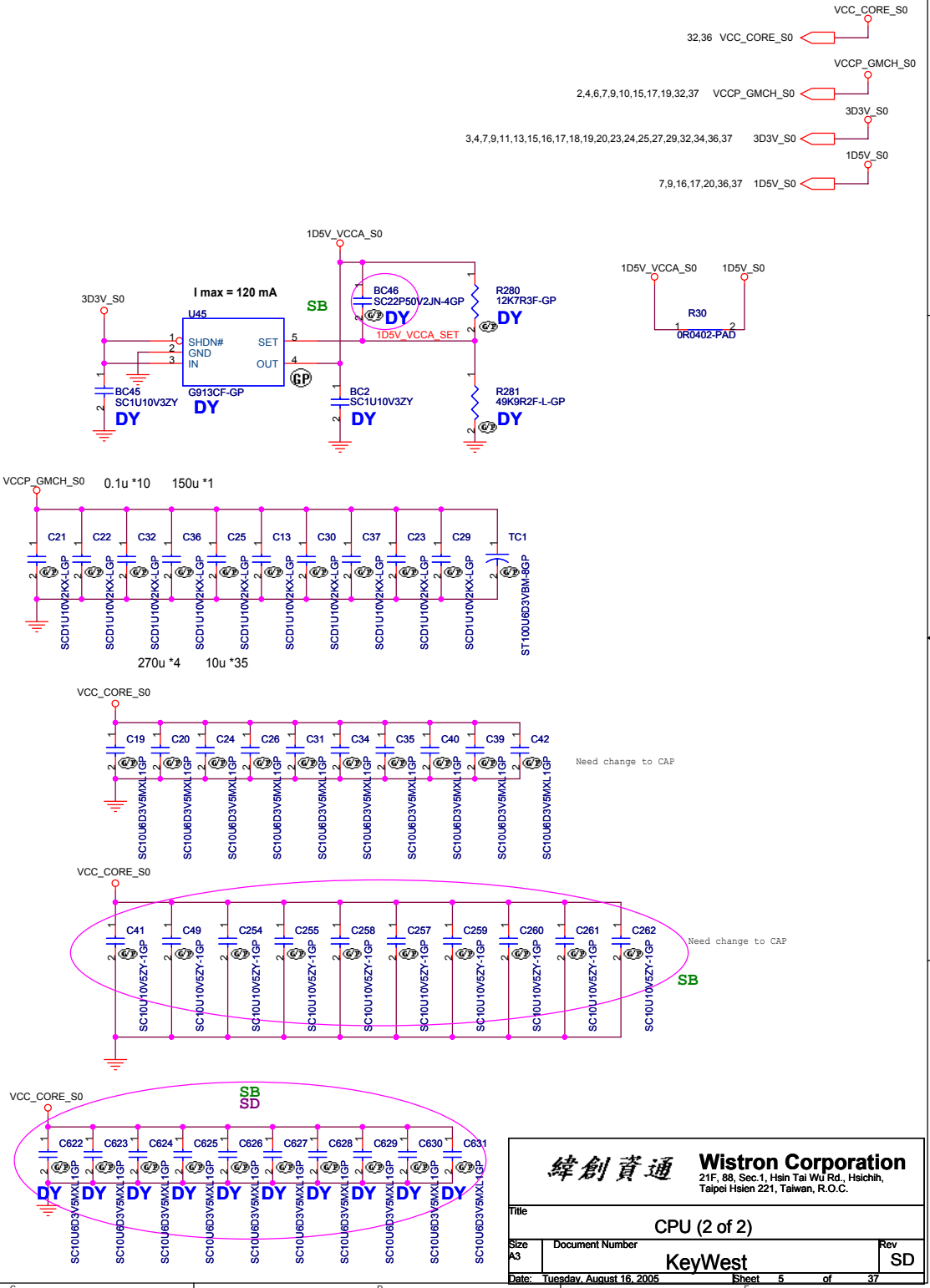
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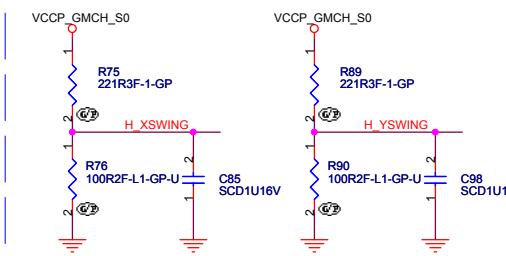
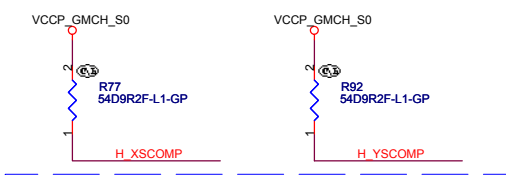
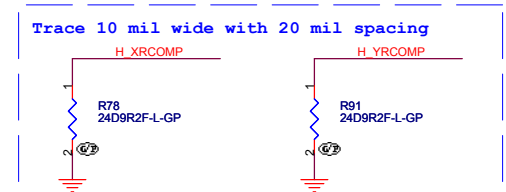


Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

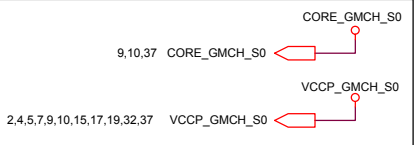
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.



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Trace 10 mil wide with 20 mil spacing

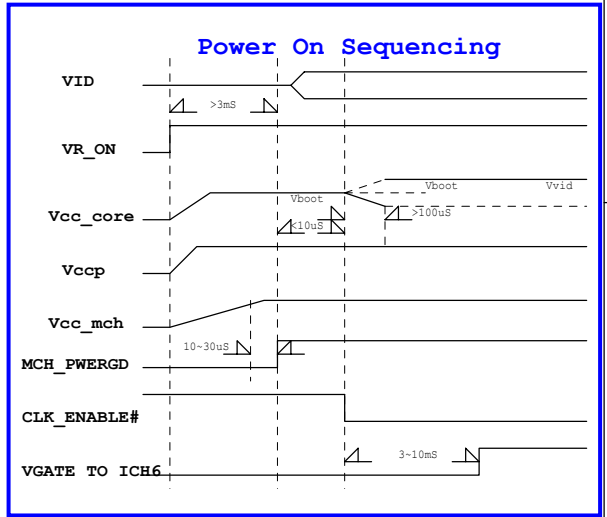
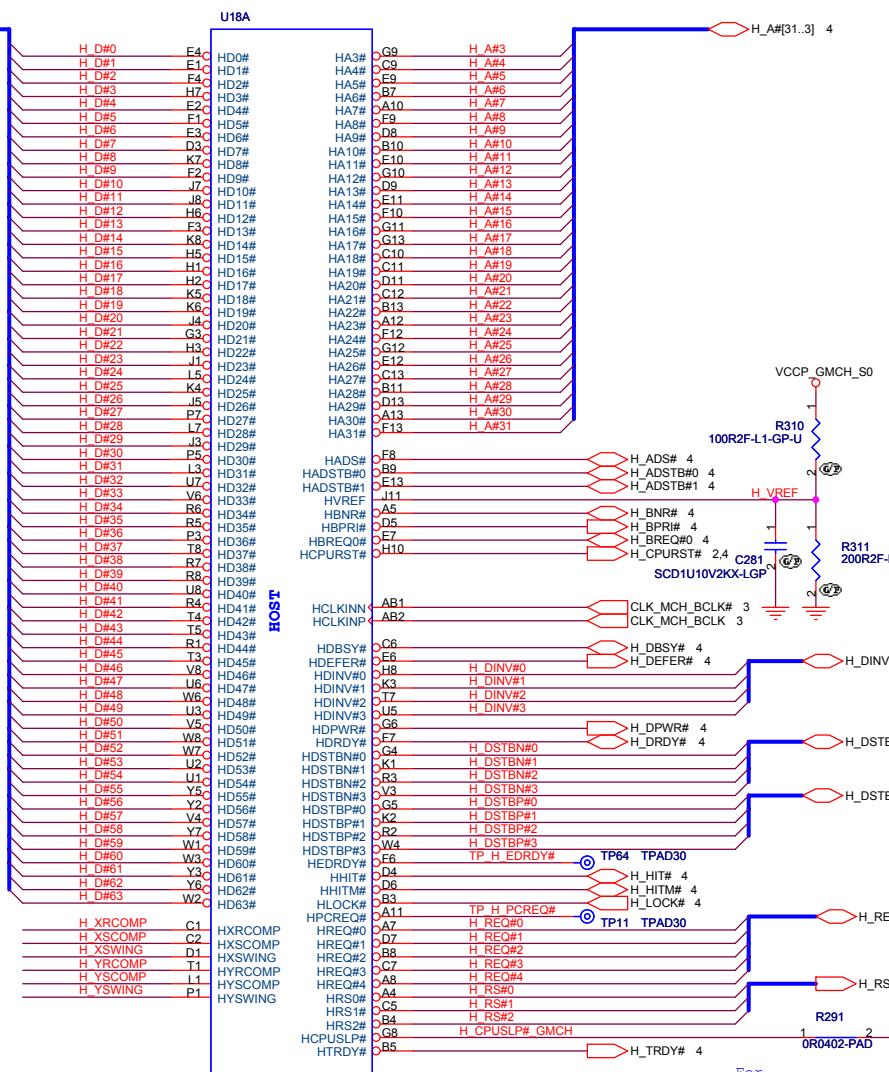


Alviso Strapping Signals and Configuration

REV. NO. 1.0
REF. NO. 15577 page 183

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 101 = FSB400 others = Reversed
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	0 = DDR2 (Default) 1 = DDR1
CFG7	CPU Strap	0 = Reserved 1 = Dothan (Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes 1 = Normal (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reserved	
CFG18	GMCH core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reserved	
SDVOCRTL_DATA	SDVO Present	0 = No SDVO device present (Default) 1 = SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORX In signal.



71.0GMCH.0J1
910GML (LF C1) : 71.0GMCH.M28
915GM (LF C1) : 71.0GMCH.M27

For Banias/Celeron-M: R291=DUMMY
For Dothan A: R291=DUMMY
For Dothan B: R291=0R

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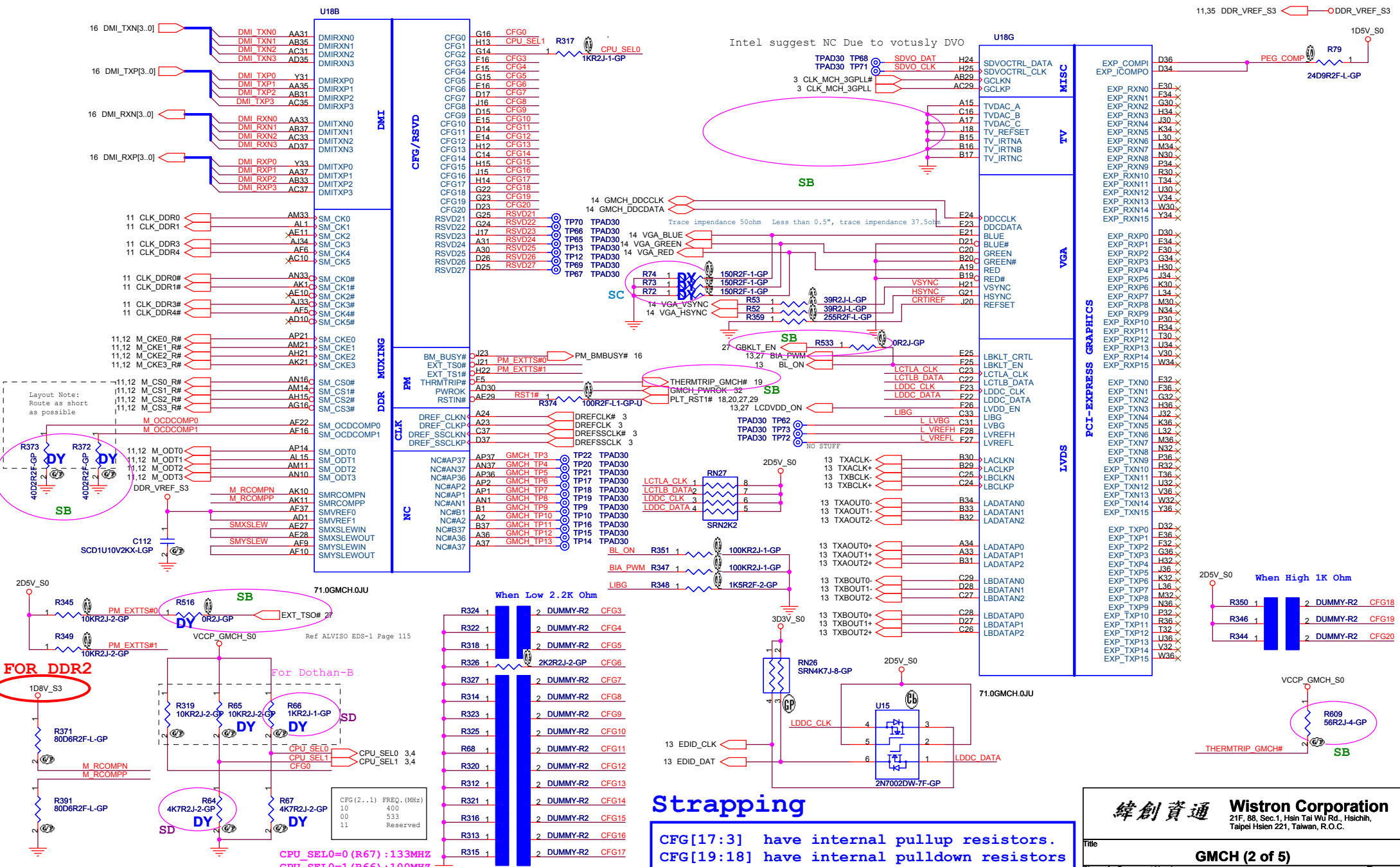
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Size A3 Document Number KeyWest Rev SD

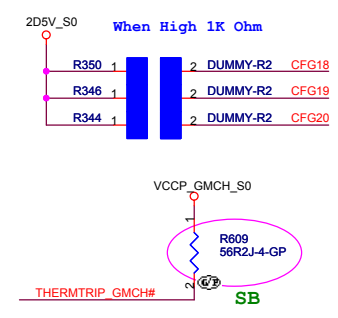
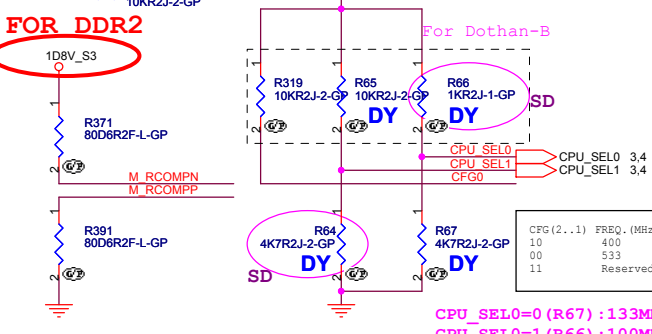
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3,4,5,9,11,13,15,16,17,18,19,20,23,24,25,27,29,32,34,36,37 3D3V_S0
 9,14,17,34,36 2D5V_S0
 9,10,11,12,16,34,35,36,37 1D8V_S3
 5,9,16,17,20,36,37 1D5V_S0
 2,4,5,6,9,10,15,17,19,32,37 VCCP_GMCH_S0
 11,35 DDR_VREF_S3

Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die



Strapping
 CFG[17:3] have internal pullup resistors.
 CFG[19:18] have internal pulldown resistors



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Title: **GMCH (2 of 5)**

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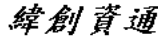
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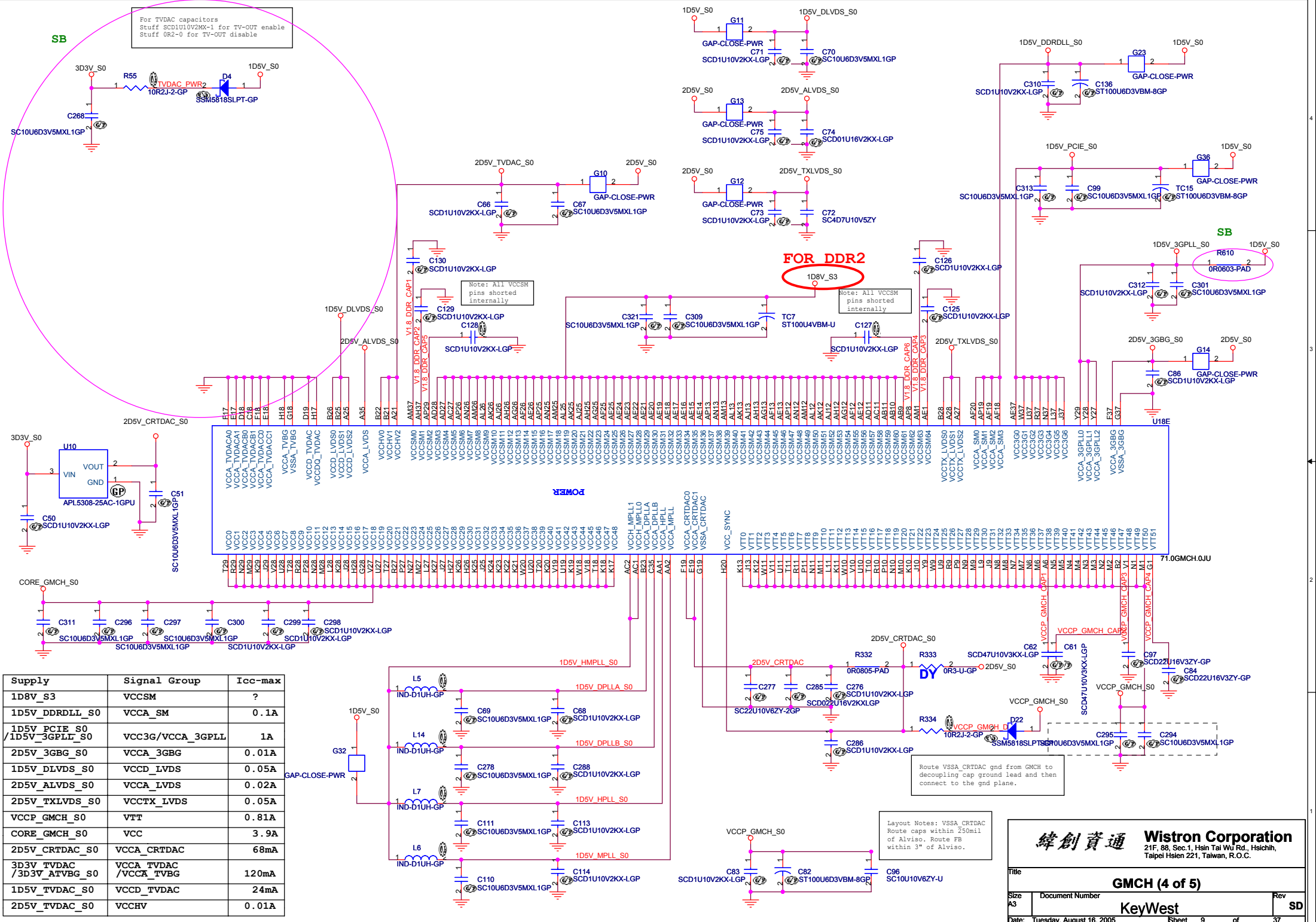
SUPPORT DDRII 400



71.0GMCH.0JU

71.0GMCH.0JU

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GMCH (3 of 5)	
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Supply	Signal Group	Icc-max
1D8V_S3	VCCSM	?
1D5V_DDRDLL_S0	VCCA_SM	0.1A
1D5V_PCIE_S0 /1D5V_3GPLL_S0	VCC3G/VCCA_3GPLL	1A
2D5V_3GBG_S0	VCCA_3GBG	0.01A
1D5V_DLVDS_S0	VCCD_LVDS	0.05A
2D5V_ALVDS_S0	VCCA_LVDS	0.02A
2D5V_TXLVDS_S0	VCCTX_LVDS	0.05A
VCCP_GMCH_S0	VTT	0.81A
CORE_GMCH_S0	VCC	3.9A
2D5V_CRTDAC_S0	VCCA_CRTDAC	68mA
3D3V_TVDAC /3D3V_ATVBS_S0	VCCA_TVDAC /VCCA_TVBS	120mA
1D5V_TVDAC_S0	VCDD_TVDAC	24mA
2D5V_TVDAC_S0	VCCHV	0.01A

For TVDAC capacitors
 Stuff SCD1U10V2MX-1 for TV-OUT enable
 Stuff 0R2-0 for TV-OUT disable

Note: All VCCSM pins shorted internally

Note: All VCCSM pins shorted internally

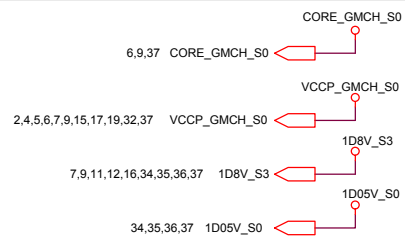
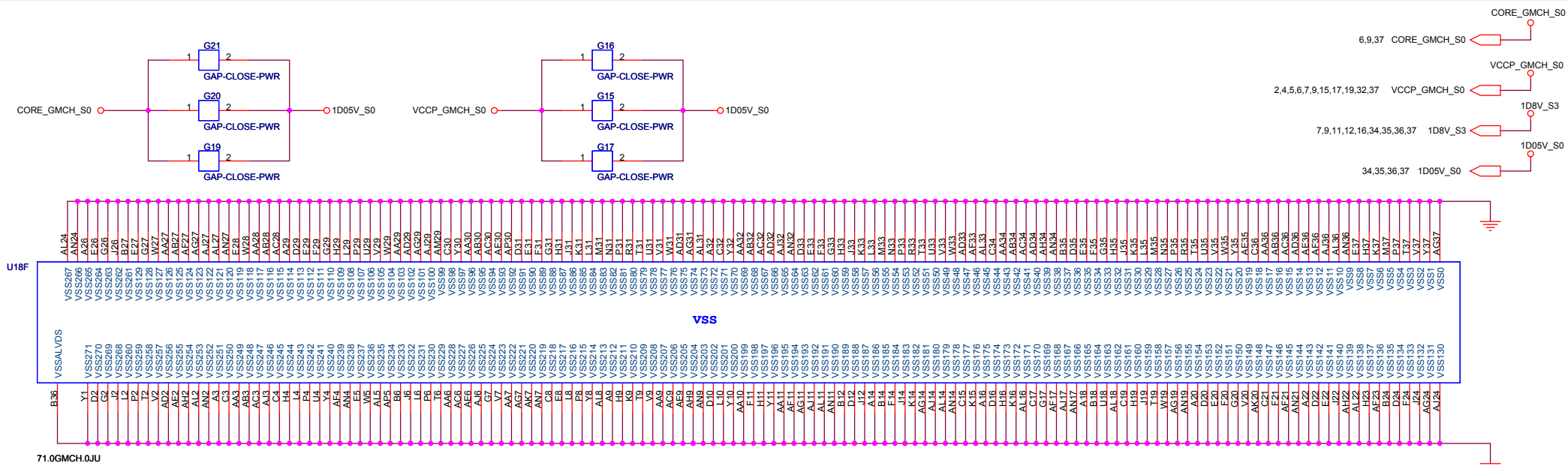
Layout Notes: VSSA_CRTDAC
 Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

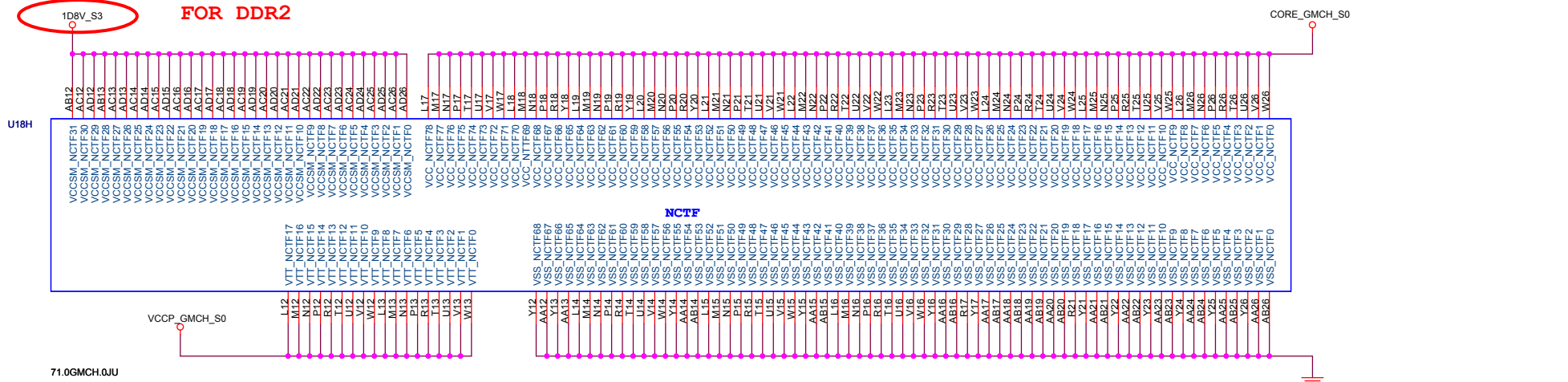
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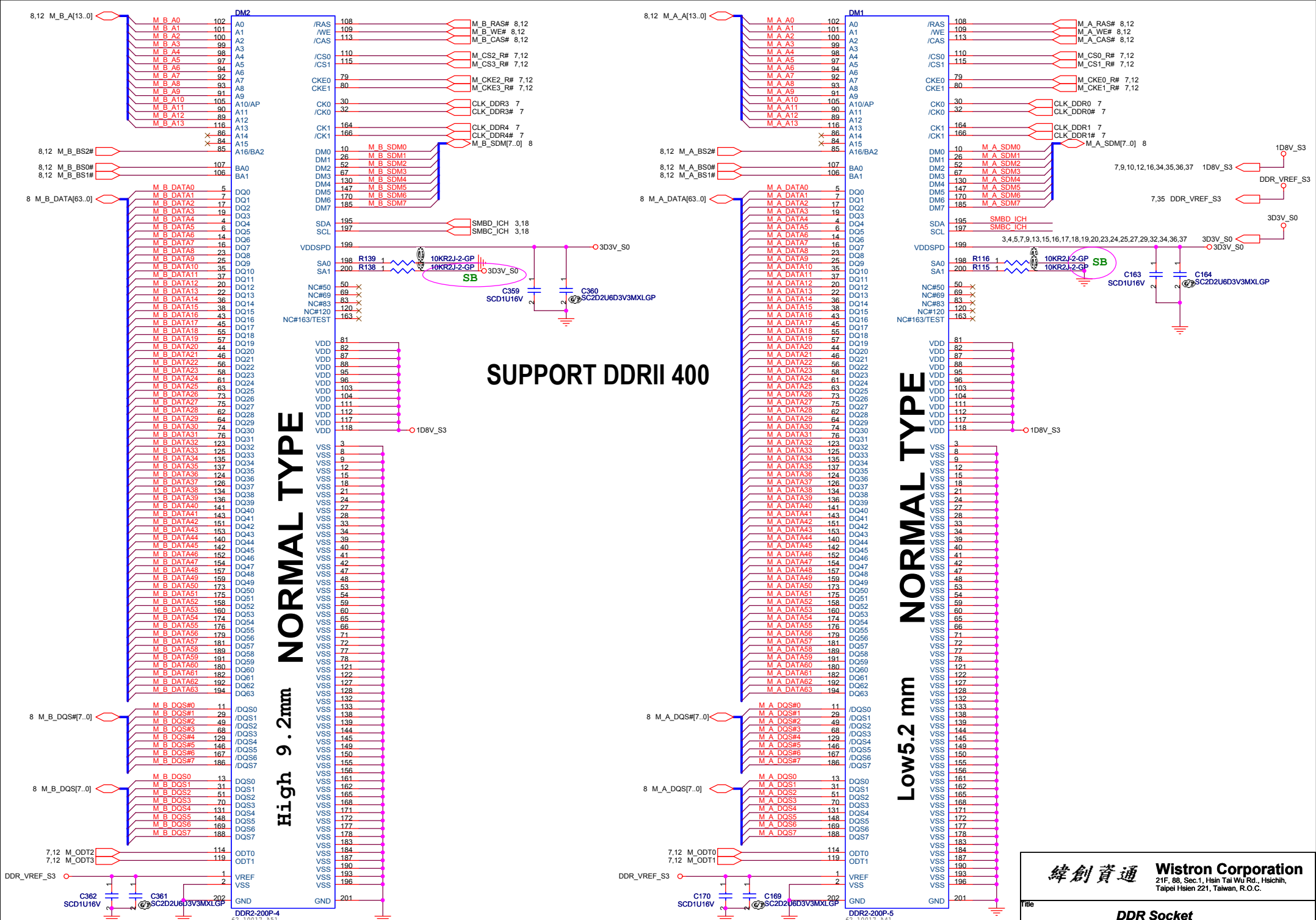
GMCH (4 of 5)

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FOR DDR2





SUPPORT DDRII 400

High 9.2mm
NORMAL TYPE

Low5.2 mm
NORMAL TYPE

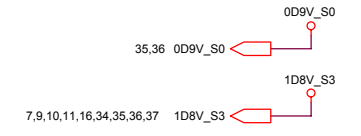
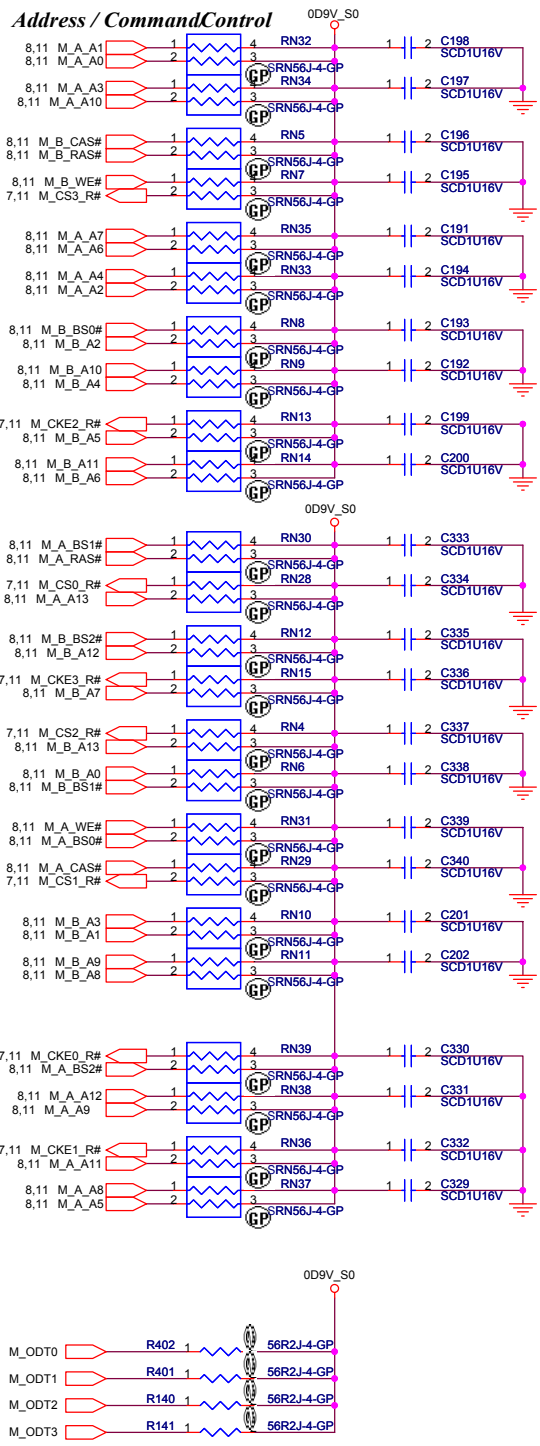
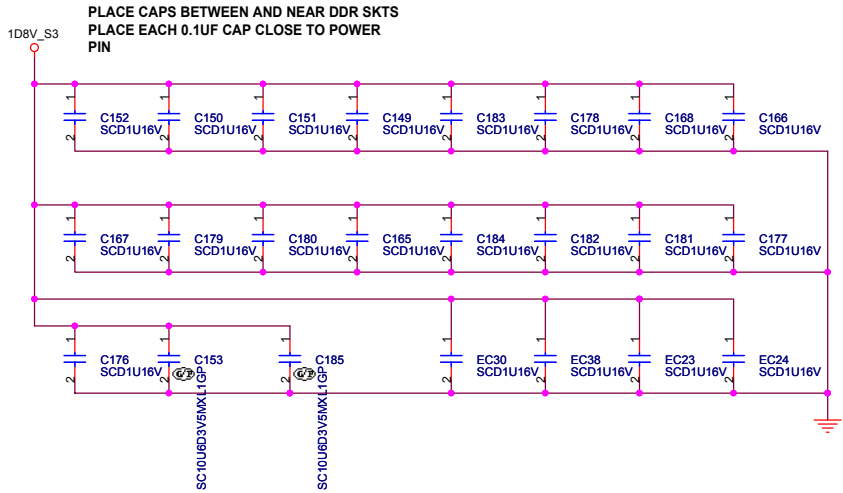
Hi 9.2mm 1st source:62.10017.A51
2nd source:62.10017.A61

1st source:62.10017.A41
2nd source:62.10017.661

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File: **DDR Socket**

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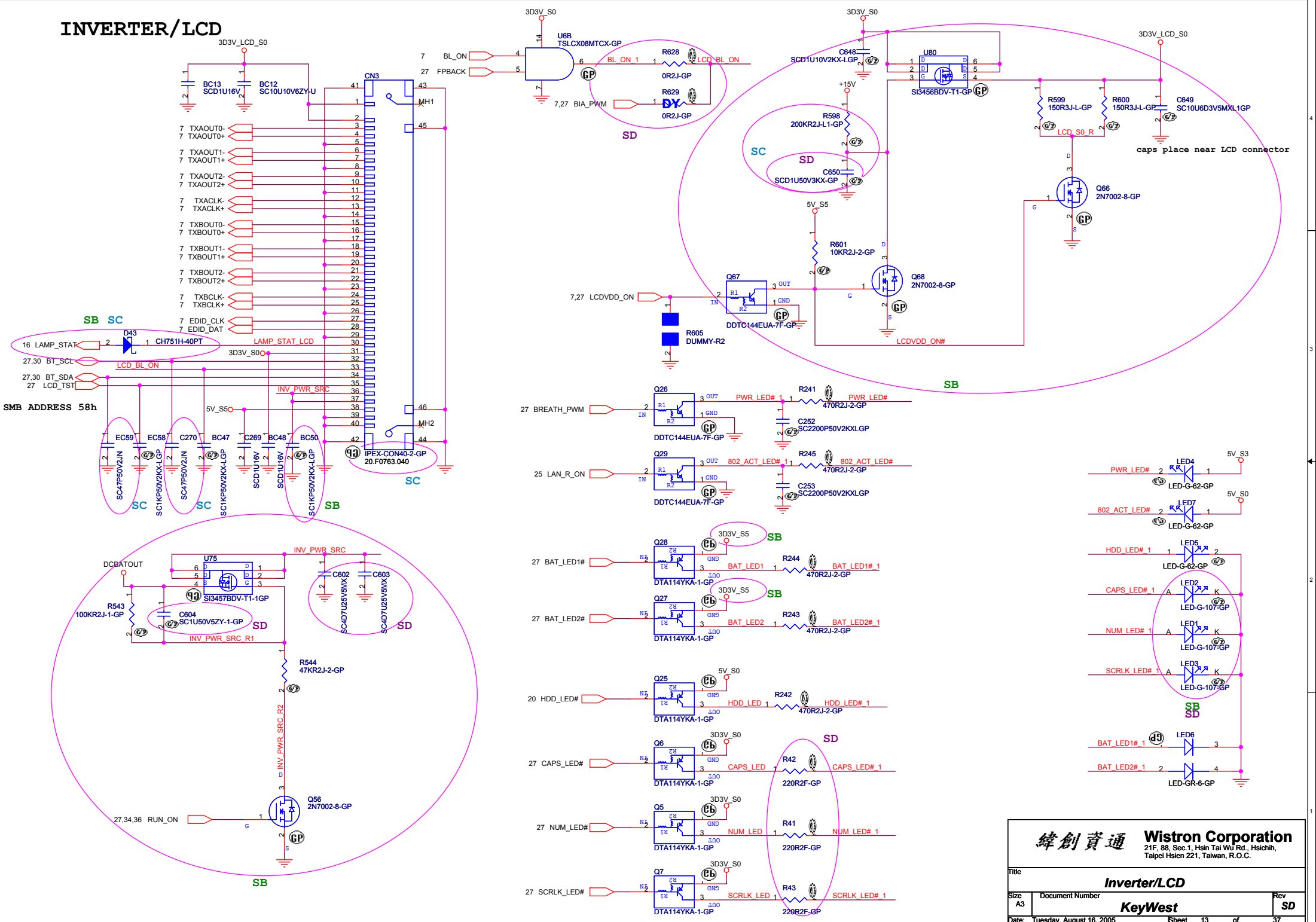


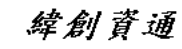
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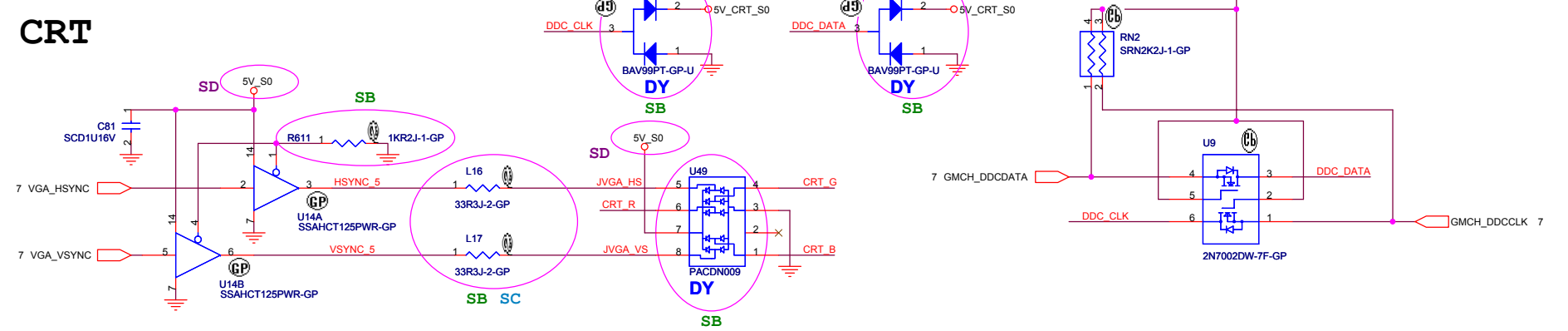
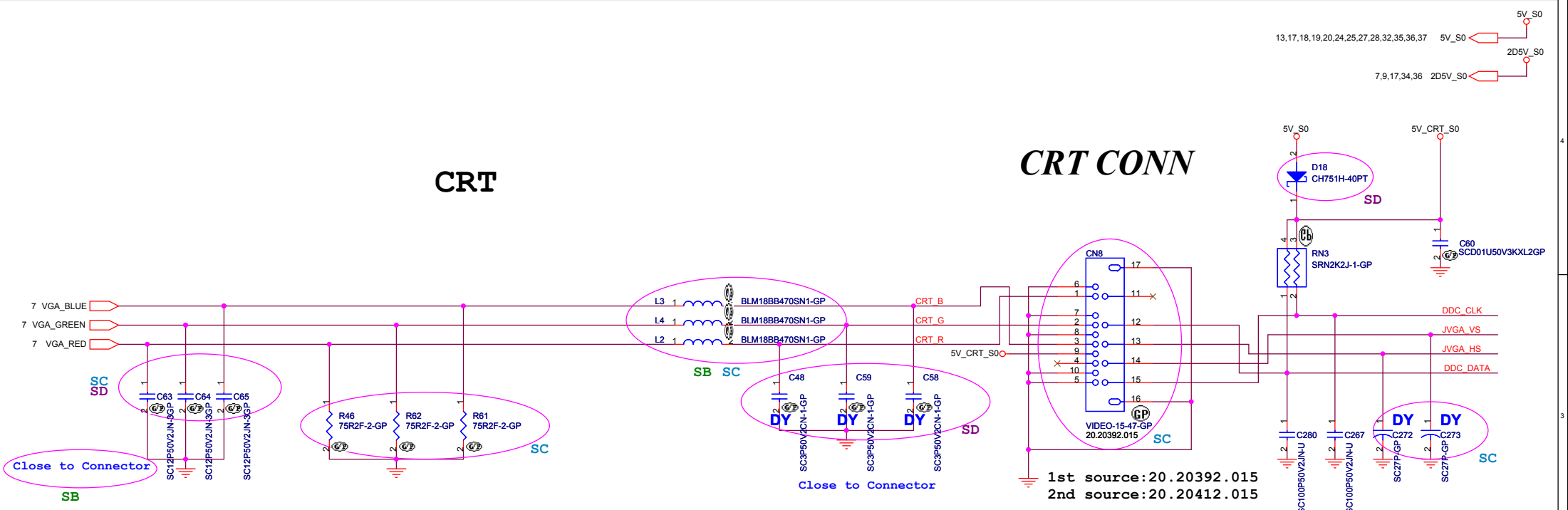
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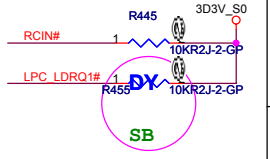
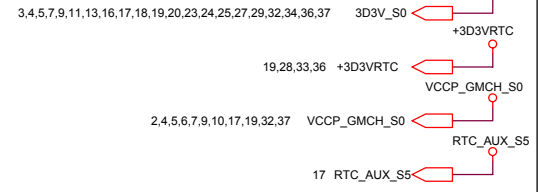
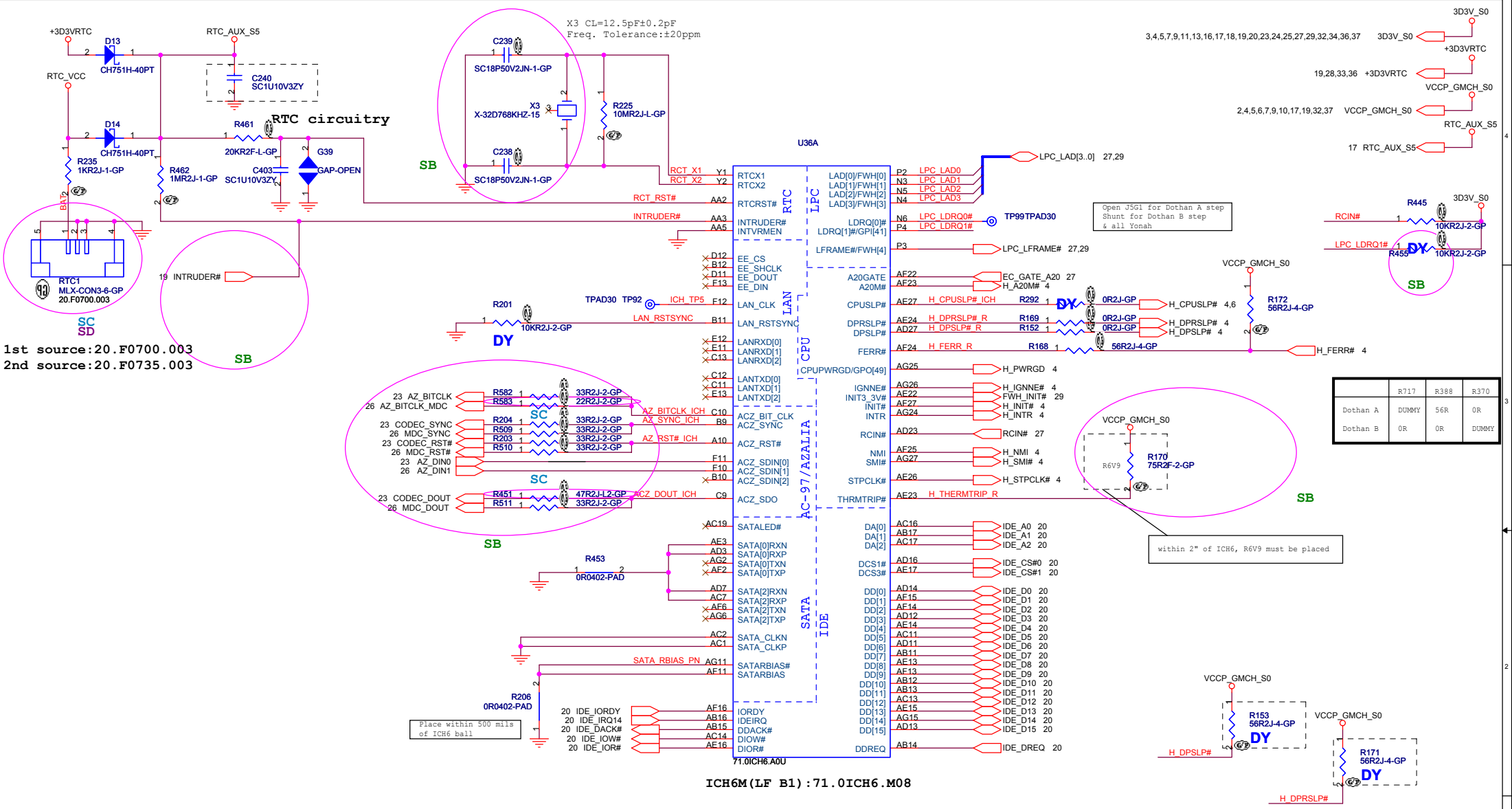
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INVERTER/LCD

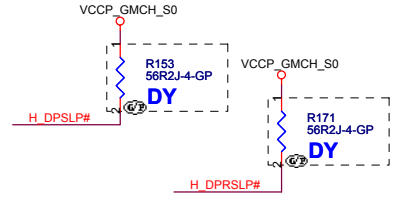
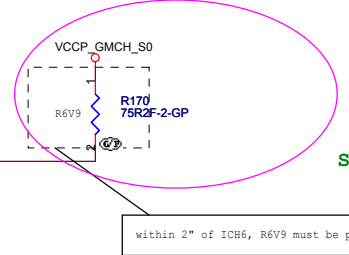


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Inverter/LCD	
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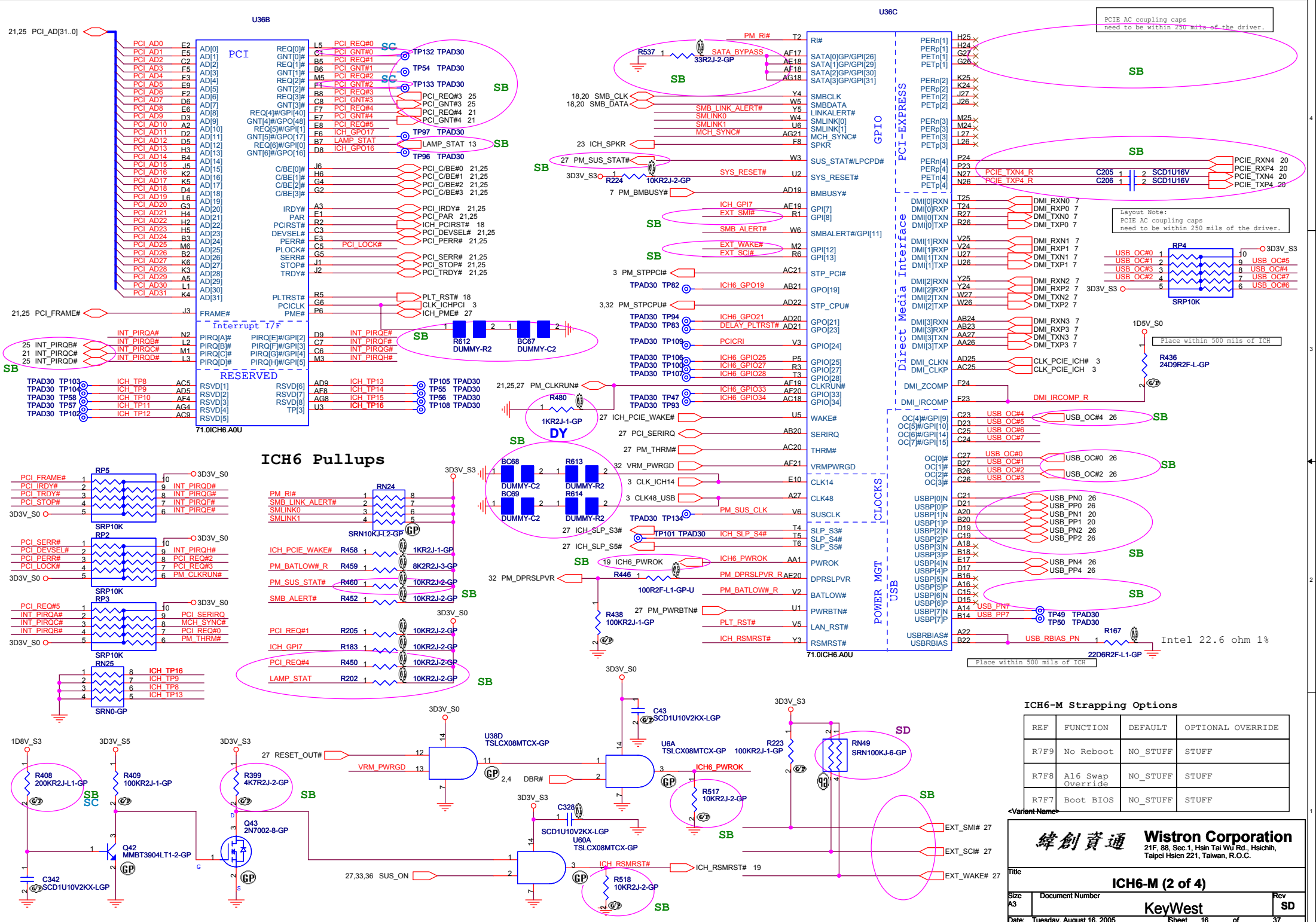




	R717	R388	R370
Dothan A	DUMMY	56R	0R
Dothan B	0R	0R	DUMMY

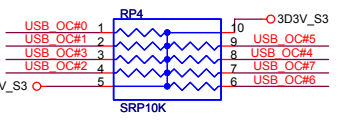


ICH6M (LF B1) : 71.0 ICH6.M08



PCIe AC coupling caps need to be within 250 mils of the driver.

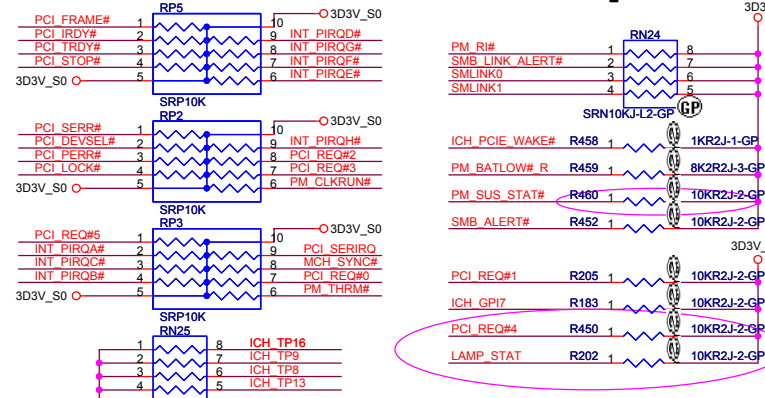
Layout Note: PCIe AC coupling caps need to be within 250 mils of the driver.



Place within 500 mils of ICH

Place within 500 mils of ICH

ICH6 Pullups



ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

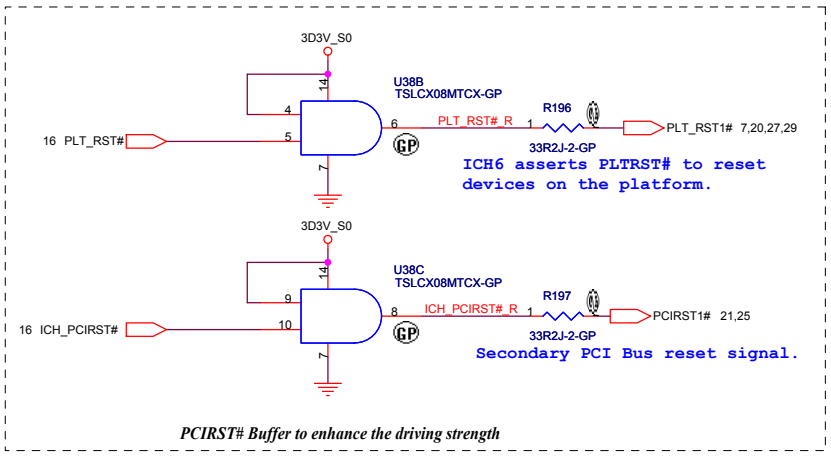
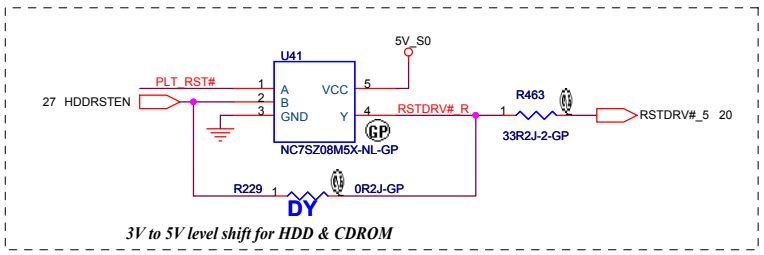
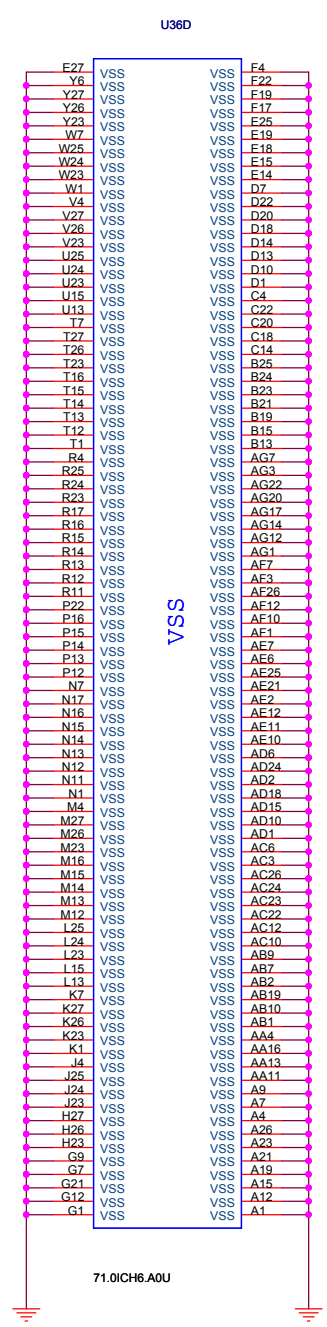
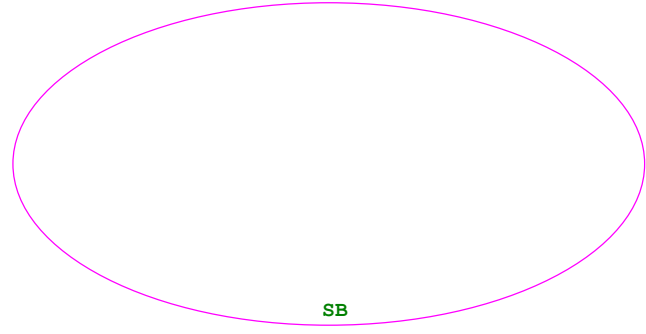
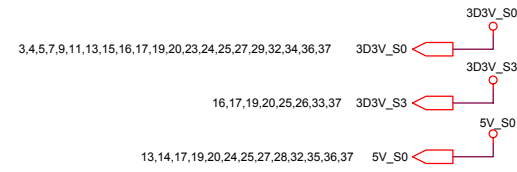
<Variant Name>

緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

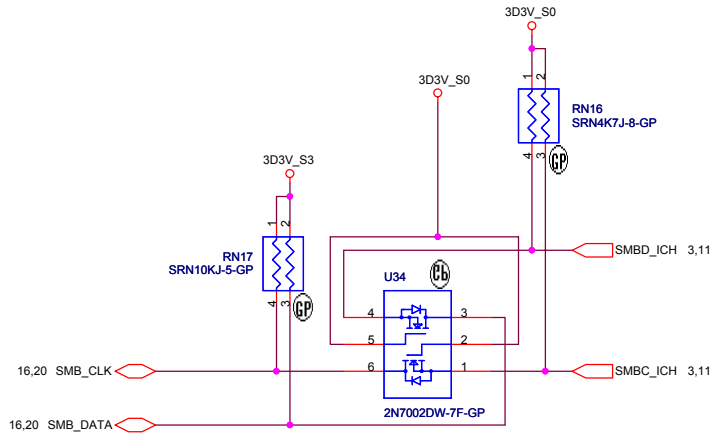
ICH6-M (2 of 4)

KeyWest

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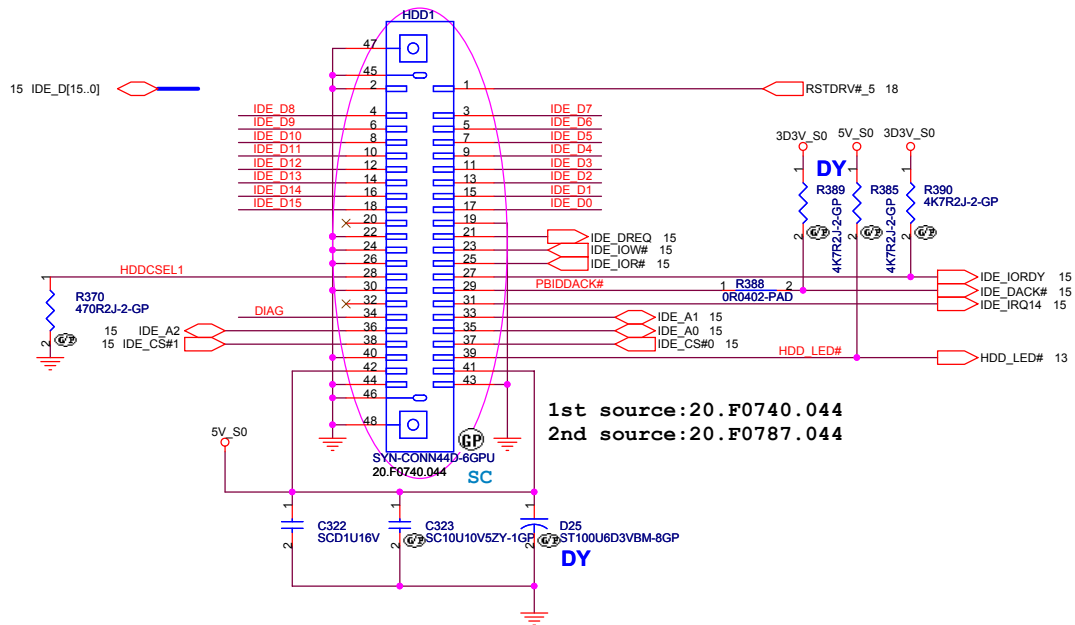
SMBUS (ICH6 ---> SODIMM, CLKGEN)



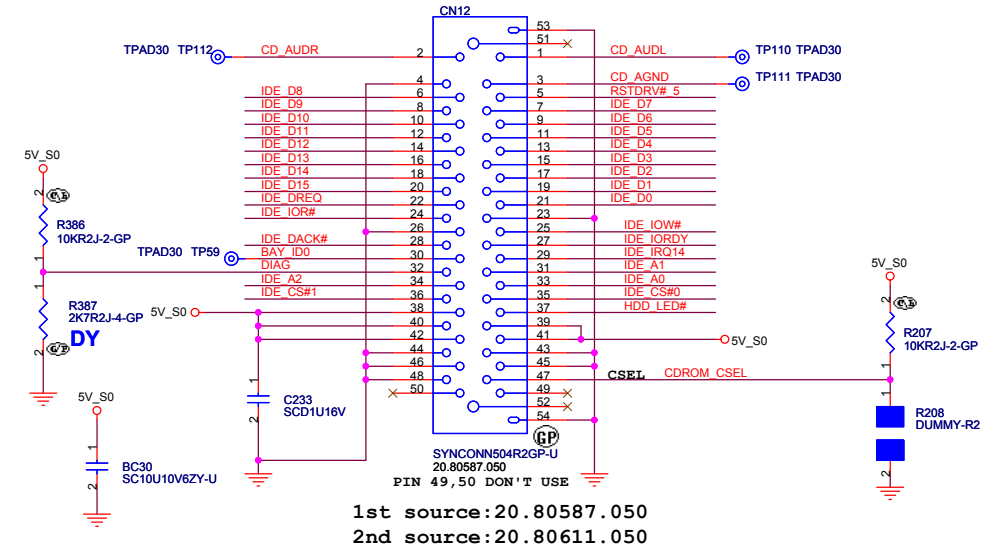
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH6-M (4 of 4)**
 Size: A3 Document Number: KeyWest Rev: SD
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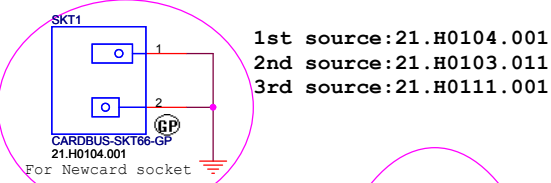
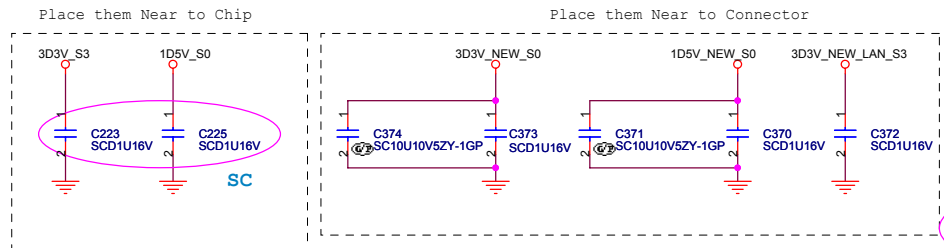
HDD Connector



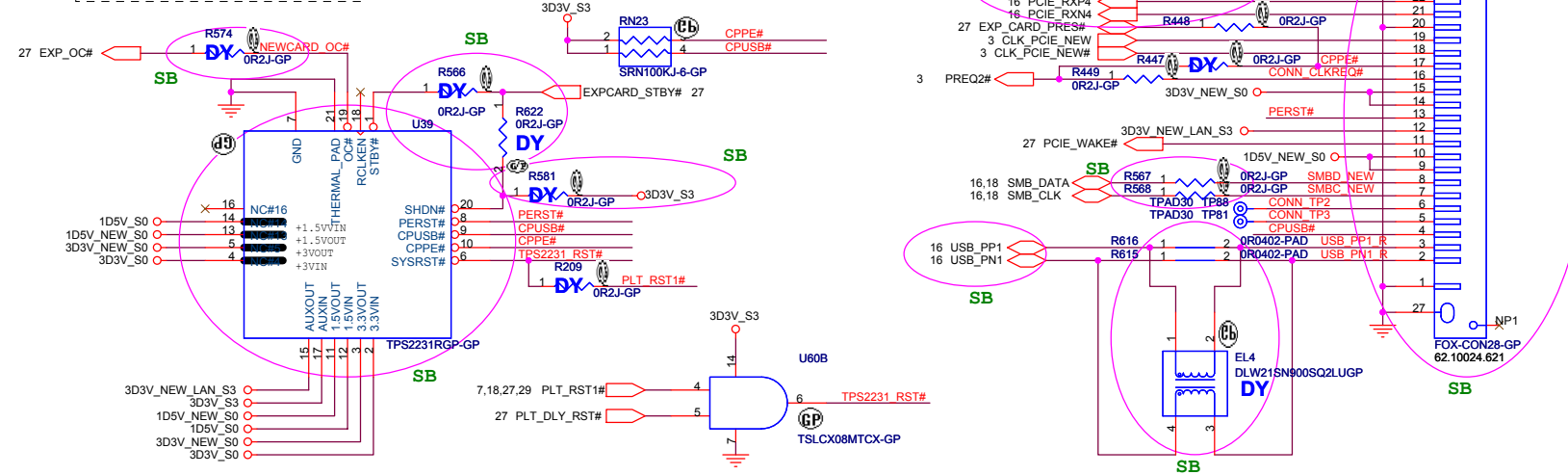
CDROM



NEWCARD Connector



SMBUS (ICH6--NEWCARD, LAN)



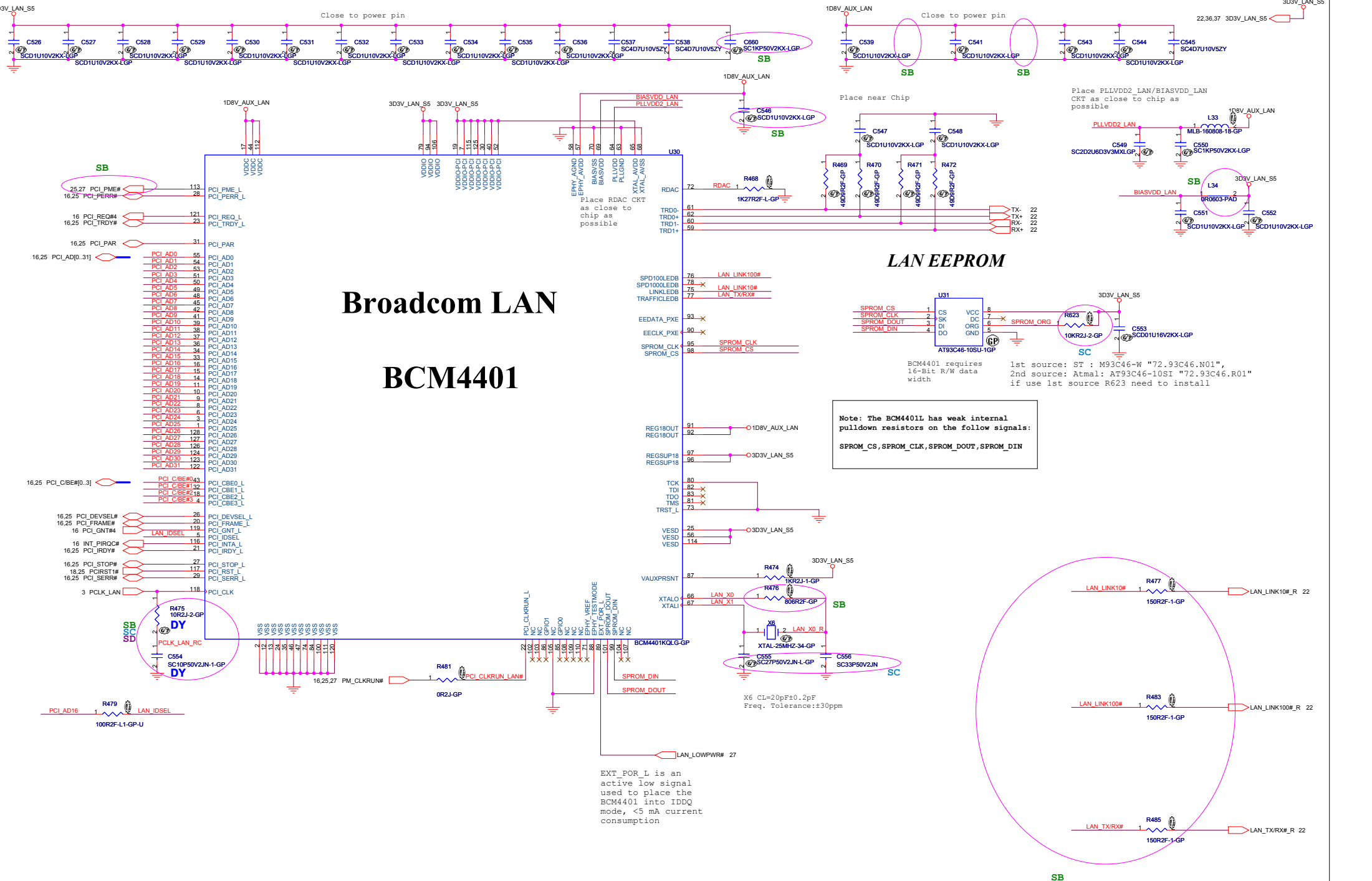
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM / NEW CARD**

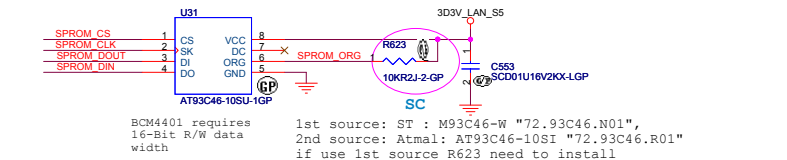
Size: A3 Document Number: 62.10024.621 Rev: **SD**

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Broadcom LAN BCM4401



LAN EEPROM



BCM4401 requires 16-Bit R/W data width

1st source: ST : M93C46-W "72.93C46.N01",
2nd source: Atmel: AT93C46-10SI "72.93C46.R01"
if use 1st source R623 need to install

Note: The BCM4401 has weak internal pulldown resistors on the follow signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title		LAN BCM4401	
Size	Document Number	KeyWest	
Customer		Rev SD	
Date: Wednesday, August 17, 2005	Sheet 21	of 37	

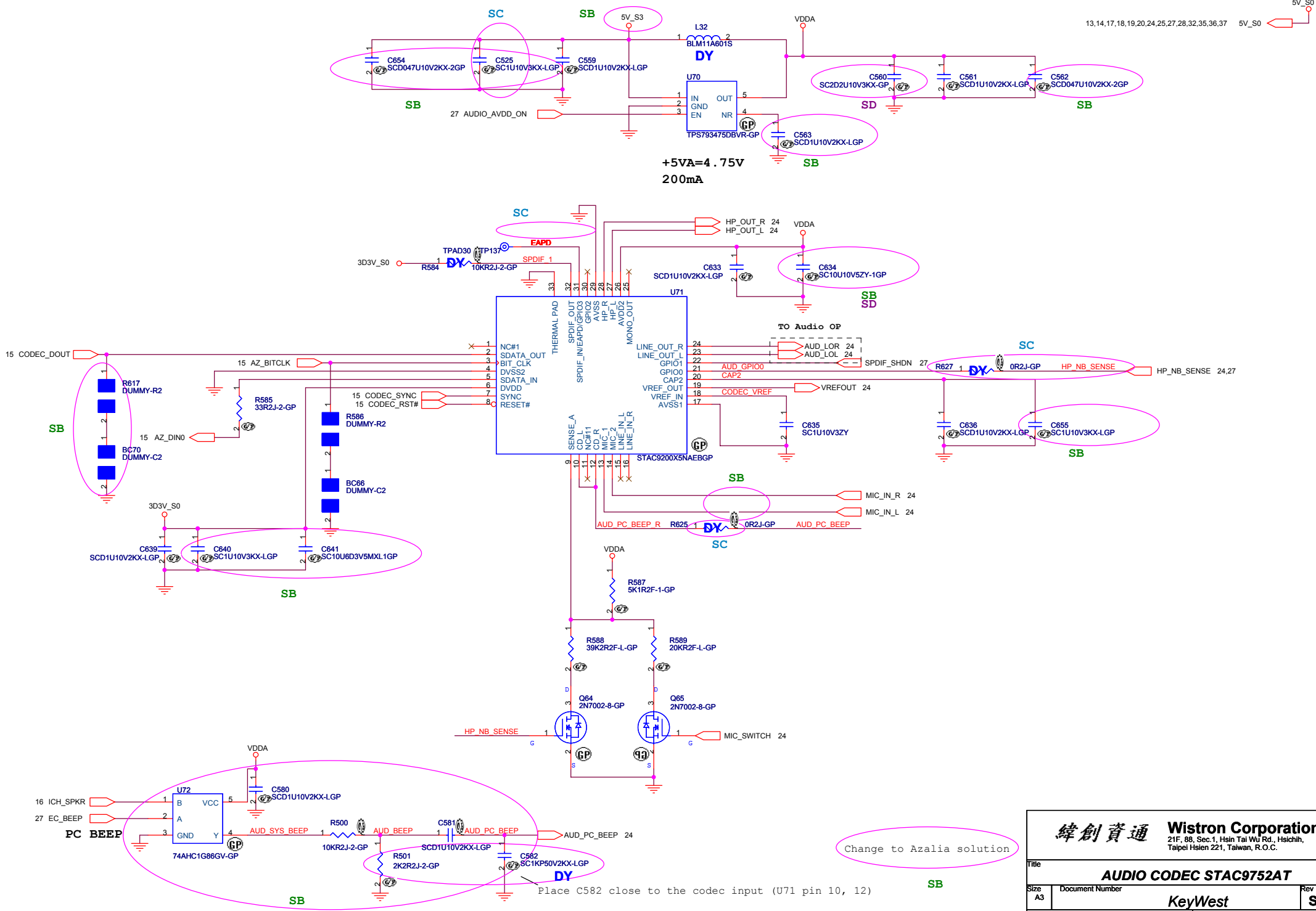
Change LAN solution

+5VA

3,4,5,7,9,11,13,15,16,17,18,19,20,24,25,27,29,32,34,36,37 3D3V_S0

5V_S0

13,14,17,18,19,20,24,25,27,28,32,35,36,37 5V_S0



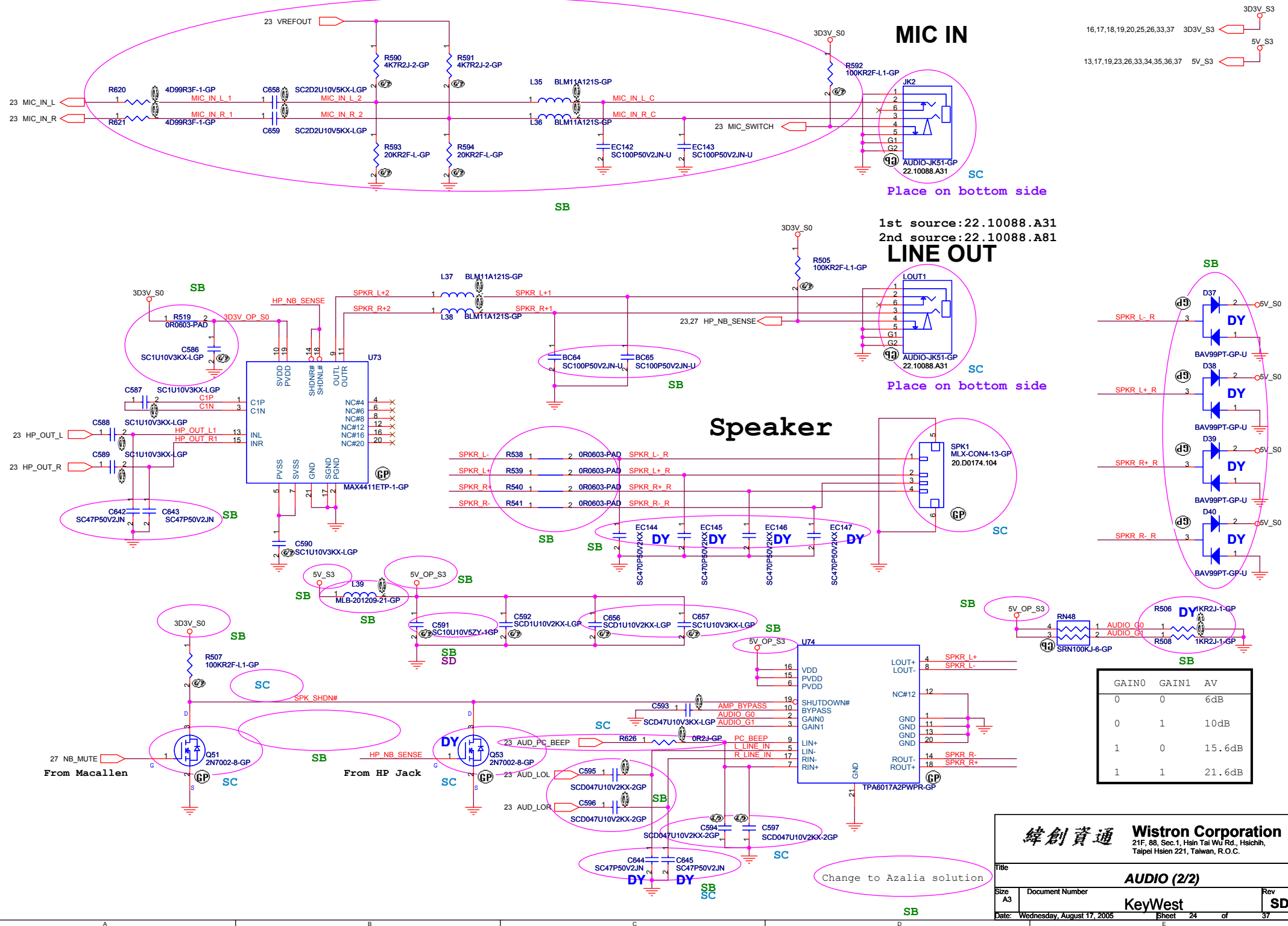
Change to Azalia solution

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

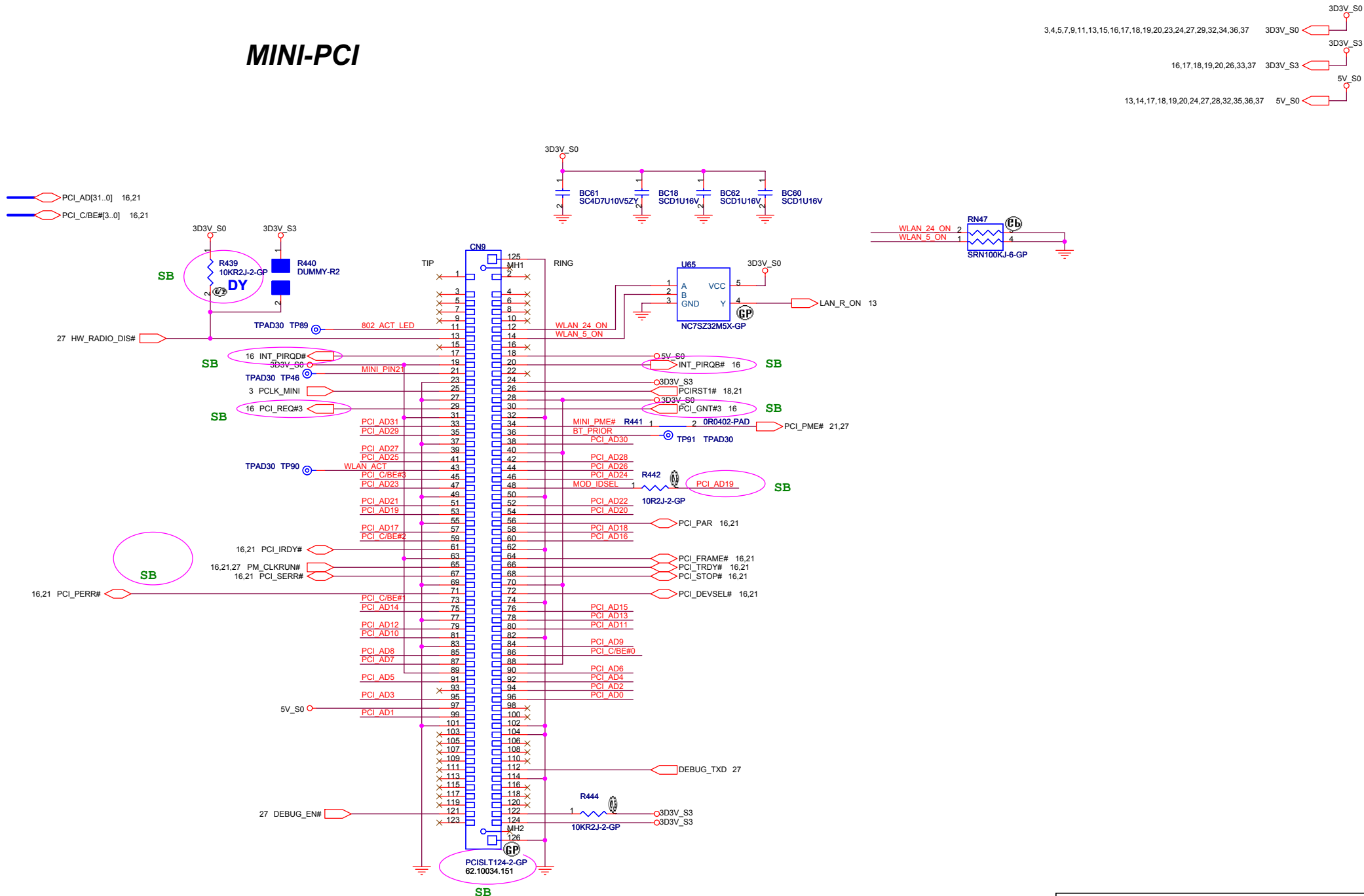
AUDIO CODEC STAC9752AT

Size A3	Document Number	Rev
	KeyWest	SD
Date: Tuesday, August 16, 2005		Sheet 23 of 37

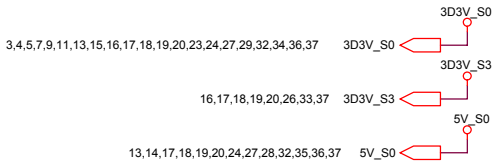
Place C582 close to the codec input (U71 pin 10, 12)



MINI-PCI

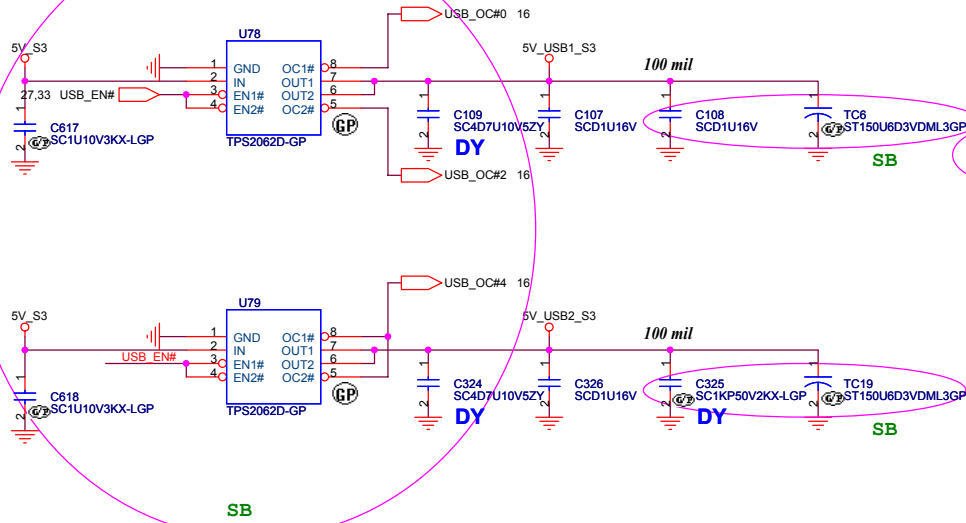


1st source: 62.10034.151
2nd source: 62.10043.151

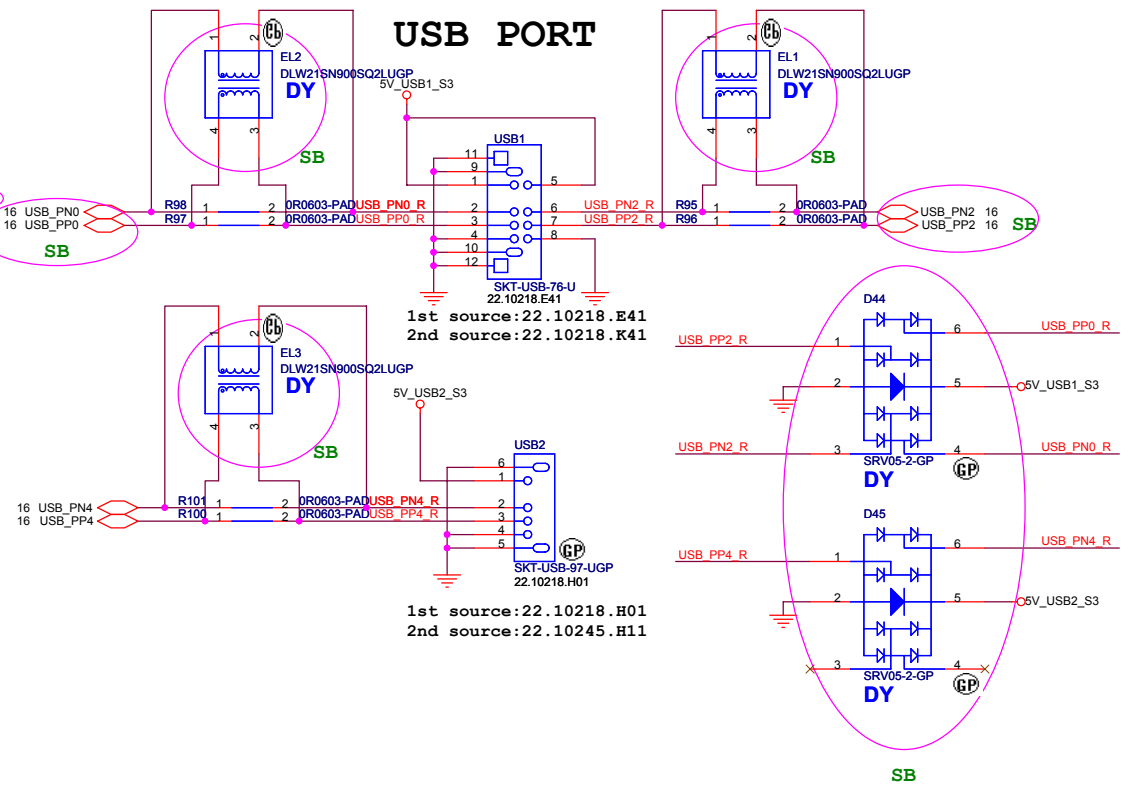


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI-PCI	
Size: A3	Document Number: KeyWest
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Rev: SD	

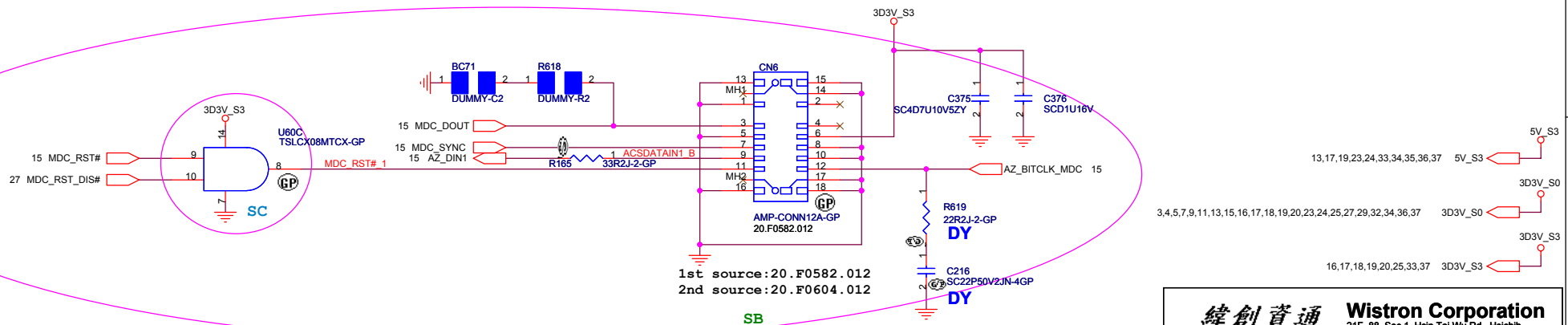
USB POWER



USB PORT

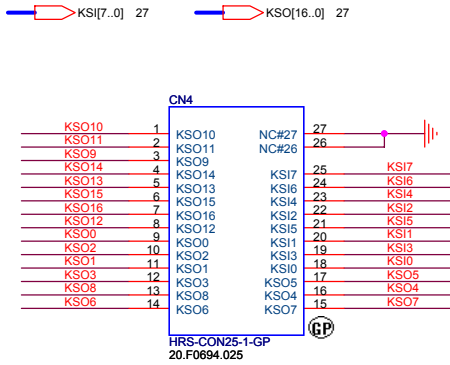


MDC Connector



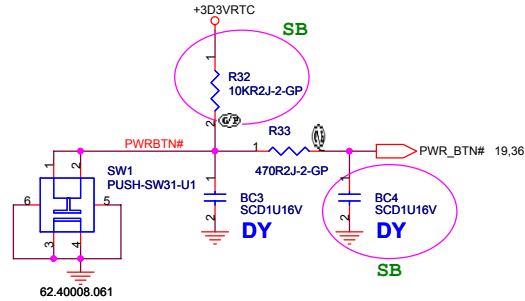
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB / MDC CONN.	
Title	SD
Size A3	Rev
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INTERNAL KEYBOARD CONNECTOR

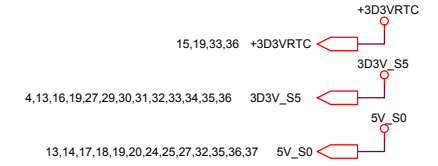


1st source : 20.F0694.025
2nd source : 20.F0642.025

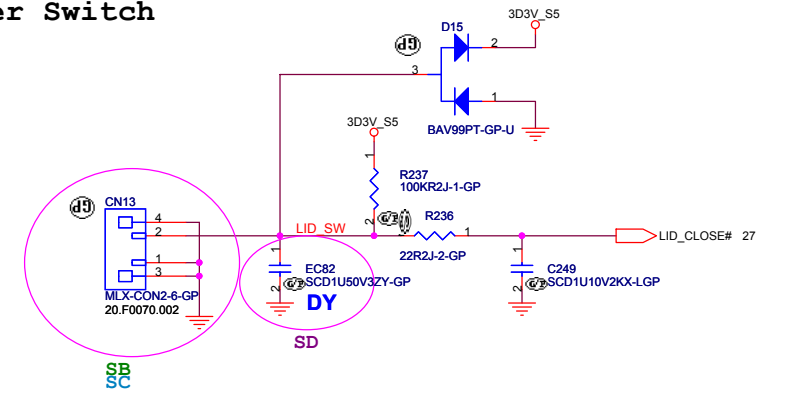
POWER BUTTON



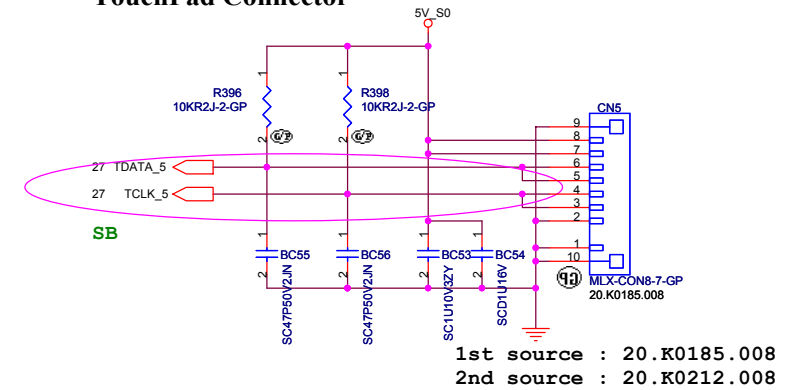
1st source : 62.40008.061
2nd source : 62.40009.191



Cover Switch



TouchPad Connector



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KB / TPAD / LID SW / PWR BTN**

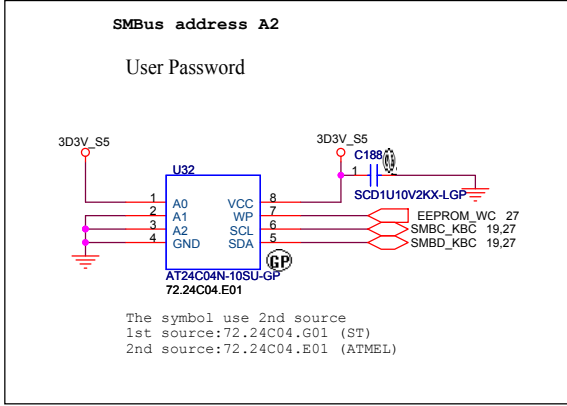
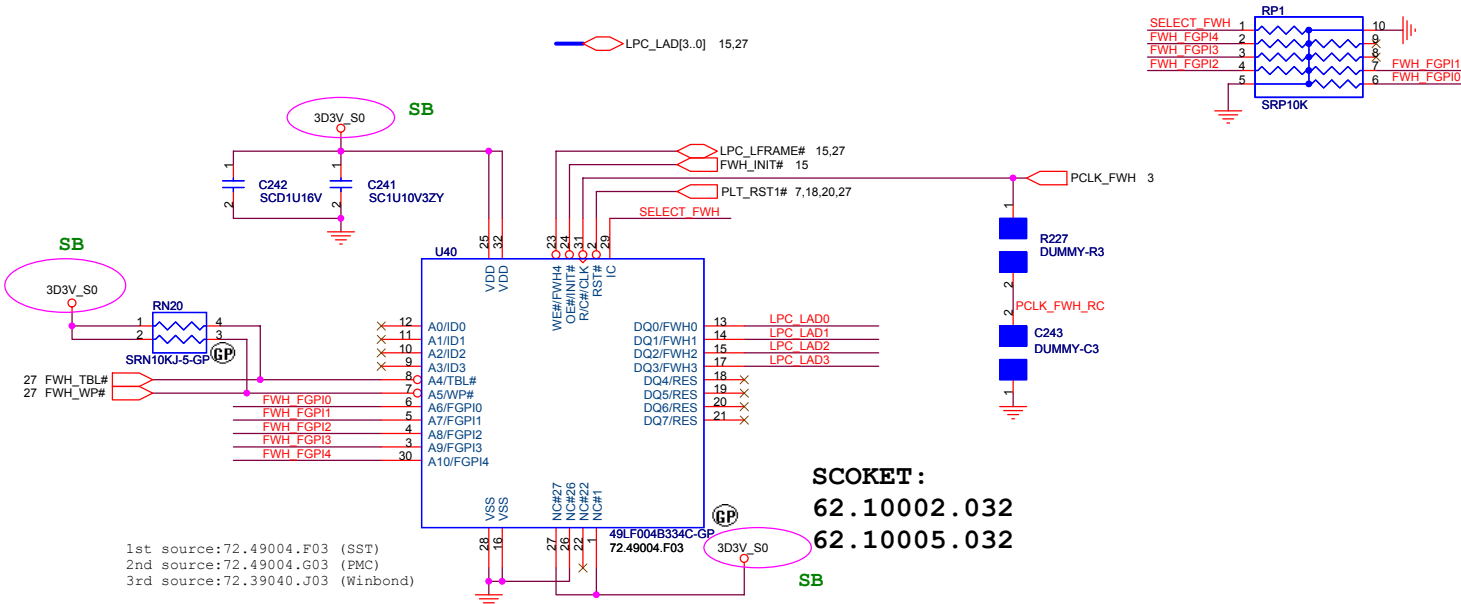
Size: A3	Document Number	Rev: SD
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for EMI

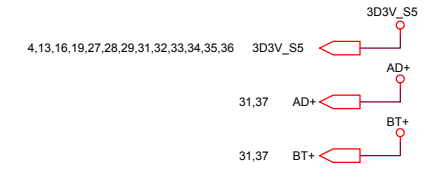
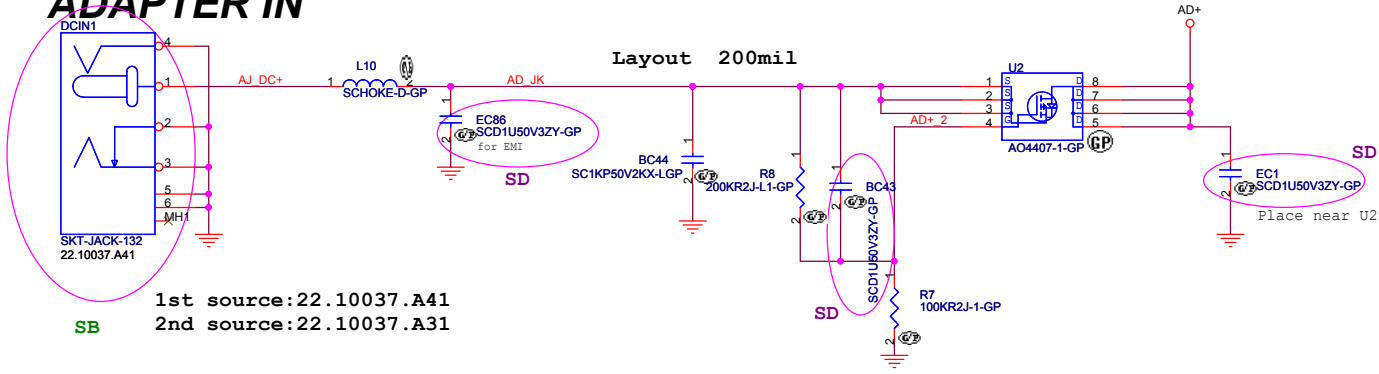
512KB Flash

Unused FGPI pins must not be float

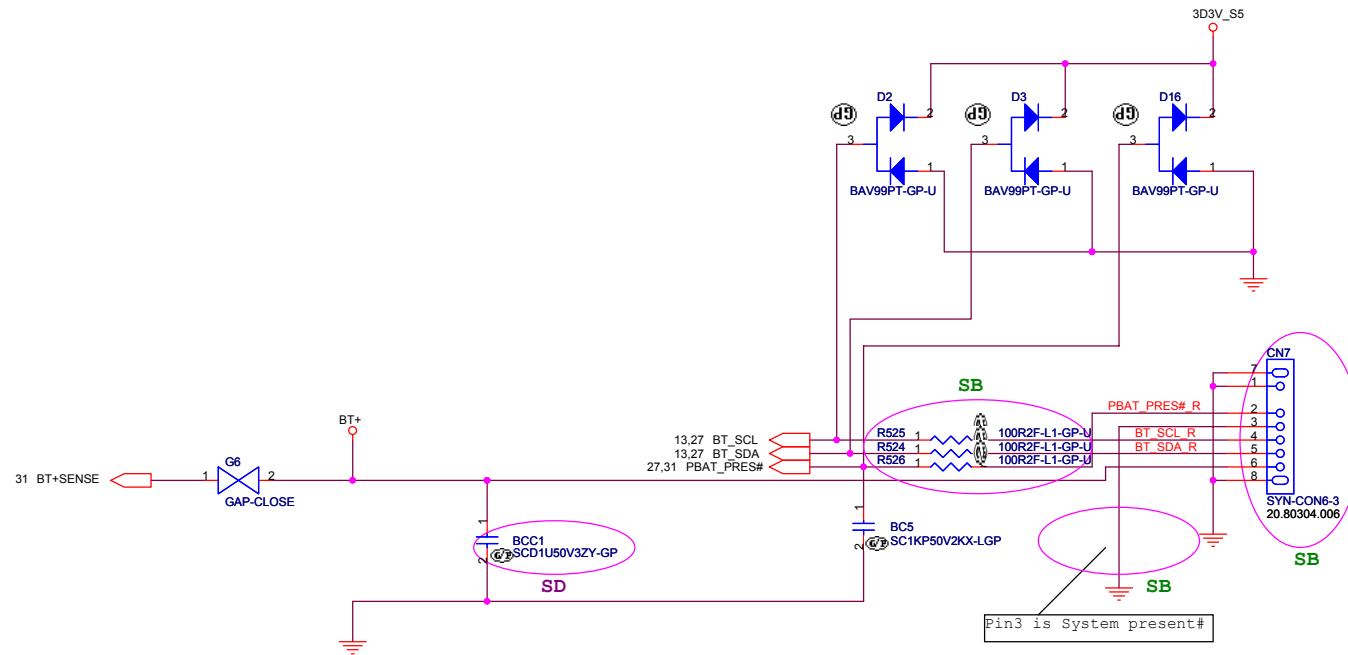


Adaptor in to generate DCBATOUT

ADAPTER IN



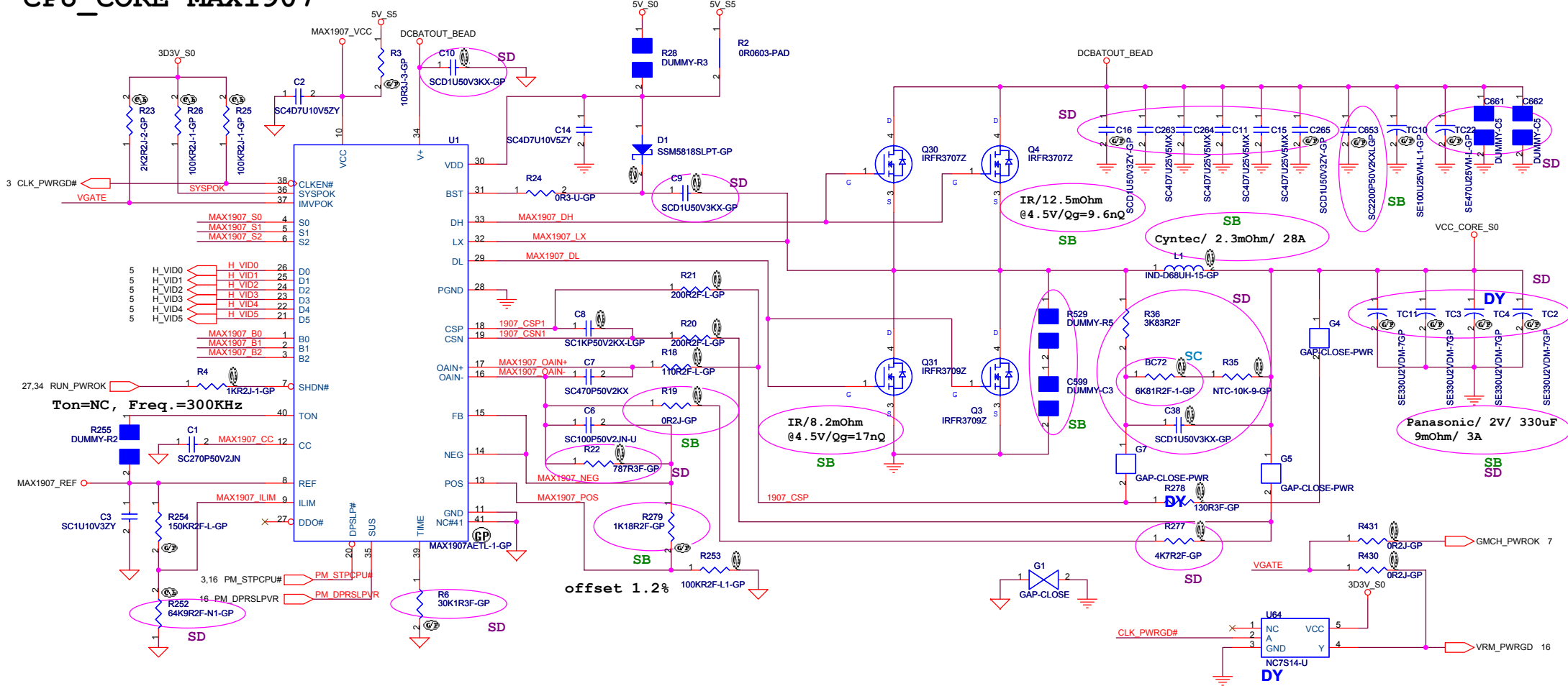
BATTERY CONNECTOR



1st source: 20.80304.006
2nd source: 20.80385.006

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Adaptor/ Battery conn.	
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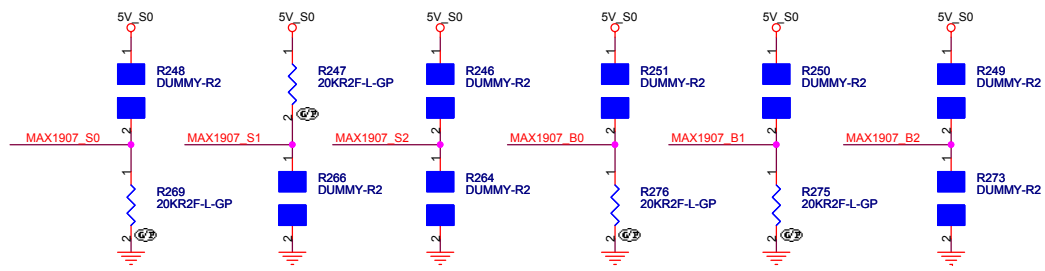
CPU_CORE-MAX1907



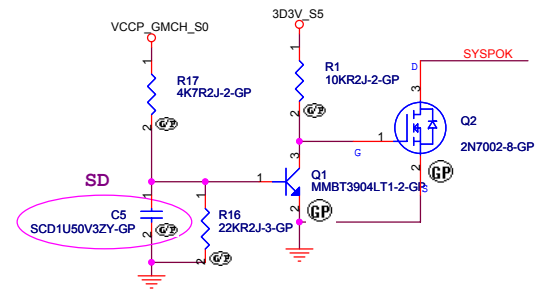
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID					Vcore	
VID5	VID4	VID3	VID2	VID1	VID0	v
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940



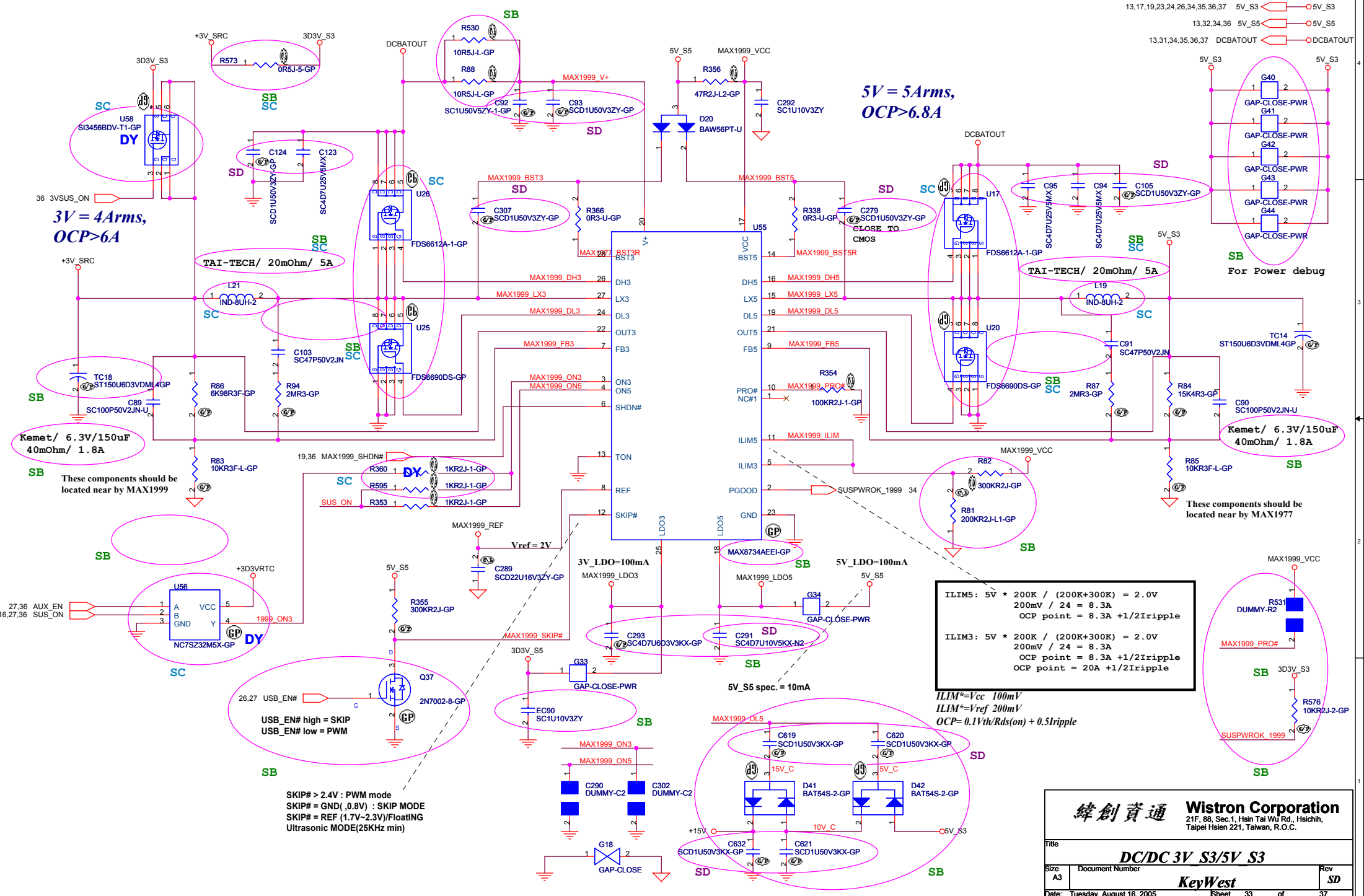
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **IMVP IV-CPU POWER-MAX1907**

Size: A3 Document Number: **KeyWest** Rev: **SD**

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SYSTEM DC/DC 3D3V_S3 / 5V_S3



**3V = 4Arms,
OCP > 6A**

**5V = 5Arms,
OCP > 6.8A**

Kemet / 6.3V/150uF
40mOhm / 1.8A

Kemet / 6.3V/150uF
40mOhm / 1.8A

These components should be located near by MAX1999

These components should be located near by MAX1977

$ILIM5: 5V * 200K / (200K+300K) = 2.0V$
 $200mV / 24 = 8.3A$
 $OCP \text{ point} = 8.3A + 1/2 I_{ripple}$
 $ILIM3: 5V * 200K / (200K+300K) = 2.0V$
 $200mV / 24 = 8.3A$
 $OCP \text{ point} = 8.3A + 1/2 I_{ripple}$
 $OCP = 0.1V_{th}/R_{ds(on)} + 0.5I_{ripple}$

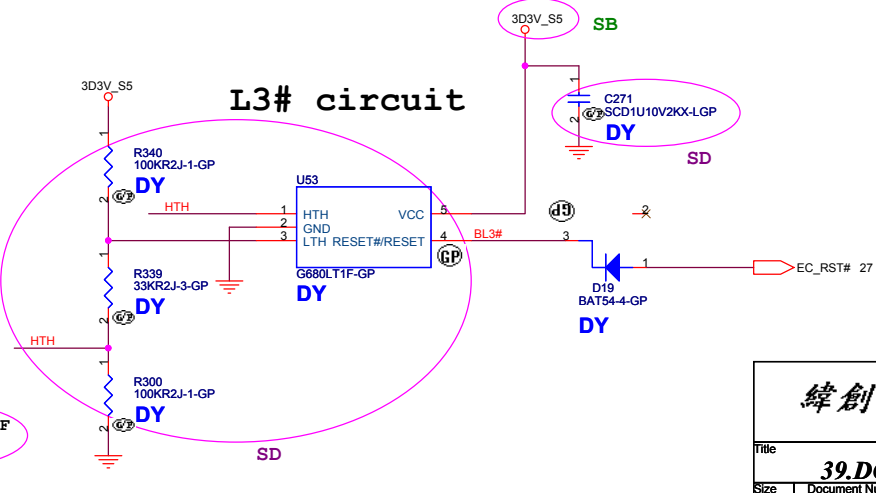
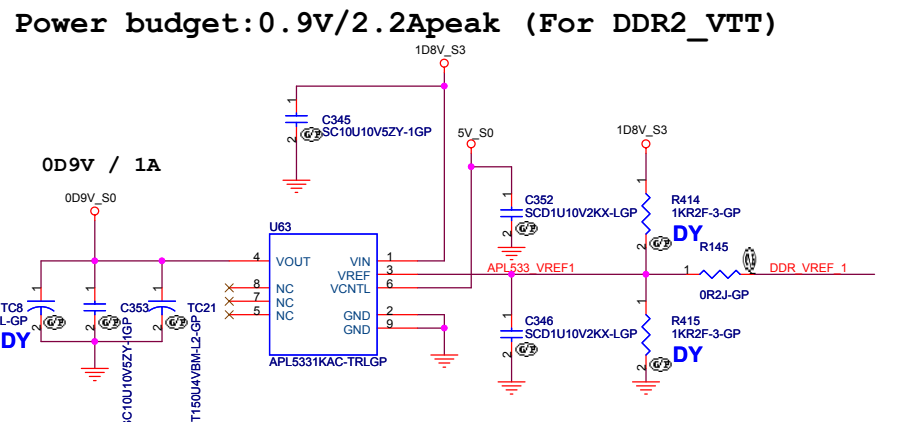
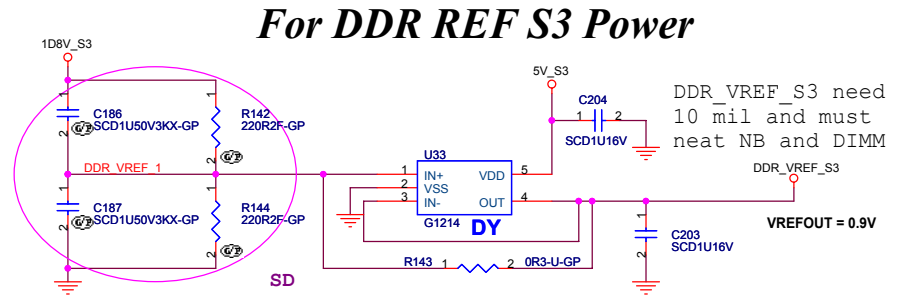
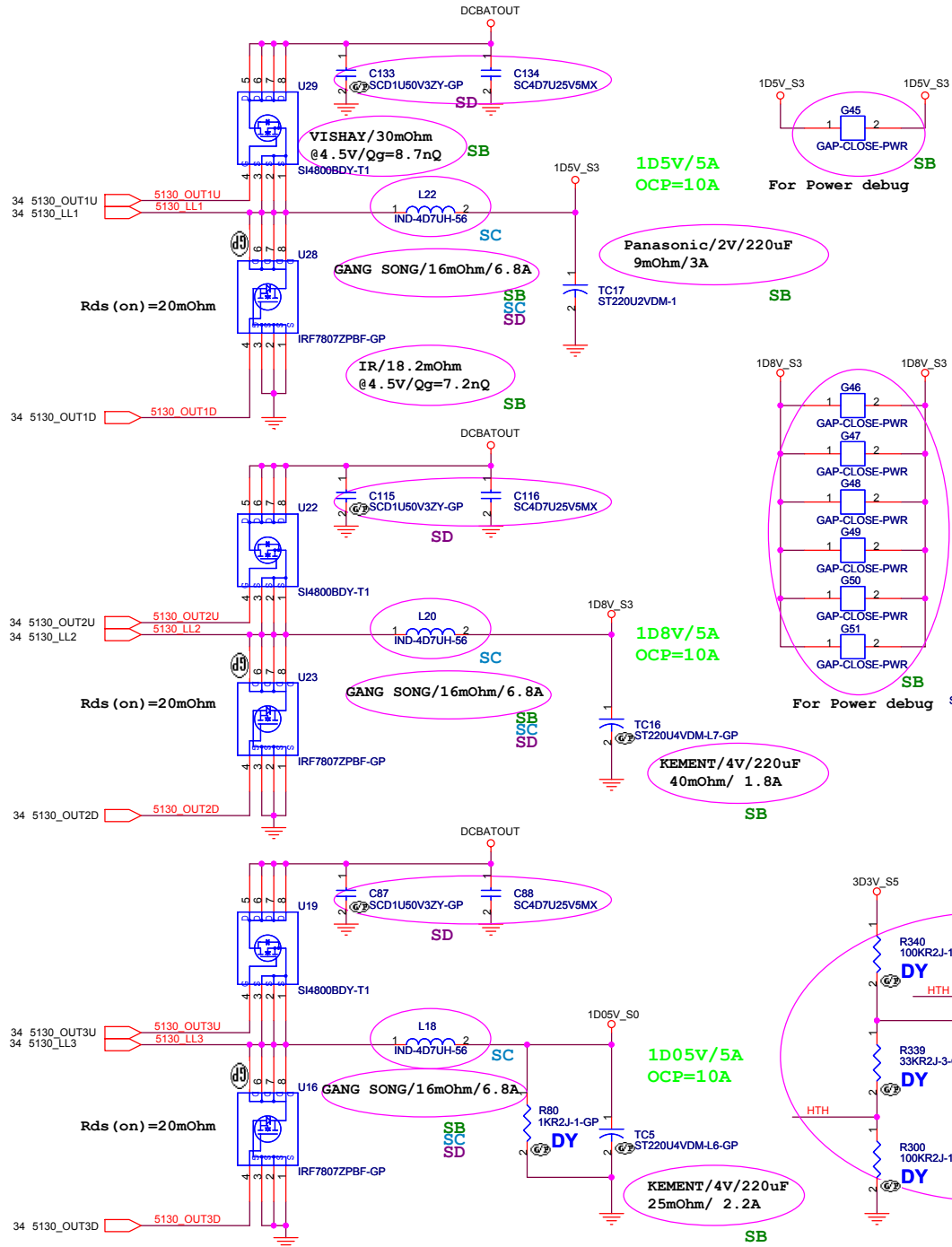
SKIP# > 2.4V : PWM mode
 SKIP# = GND(,0.8V) : SKIP MODE
 SKIP# = REF (1.7V-2.3V)/Floating
 Ultrasonic MODE(25KHz min)

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsein 221, Taiwan, R.O.C.

Title: **DC/DC 3V S3/5V S3**
 Size A3 Document Number
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 Rev SD
KeyWest

TI TPS5130 for 1.5V, 1.8V, 1.05V

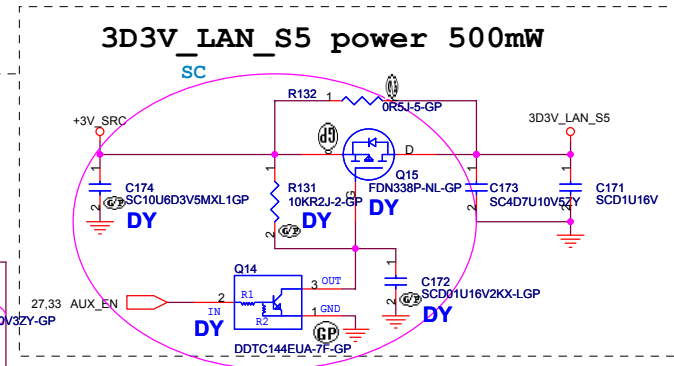
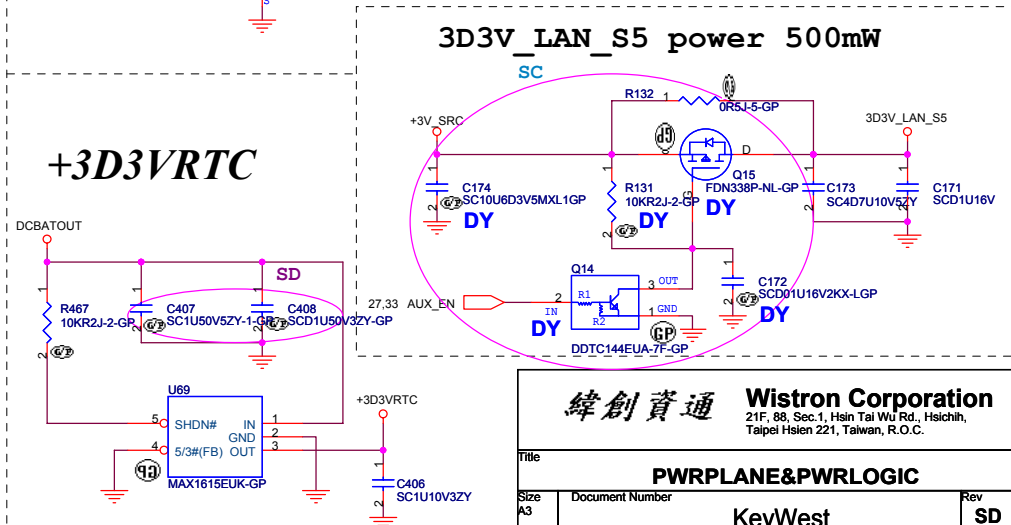
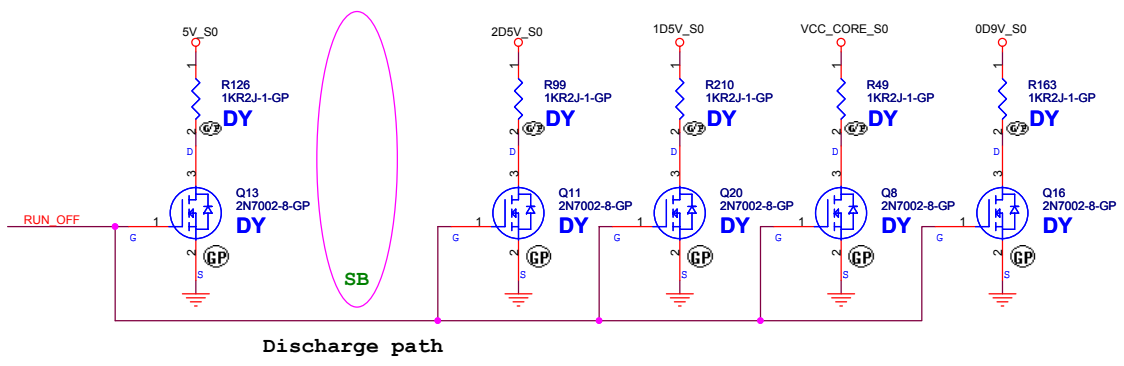
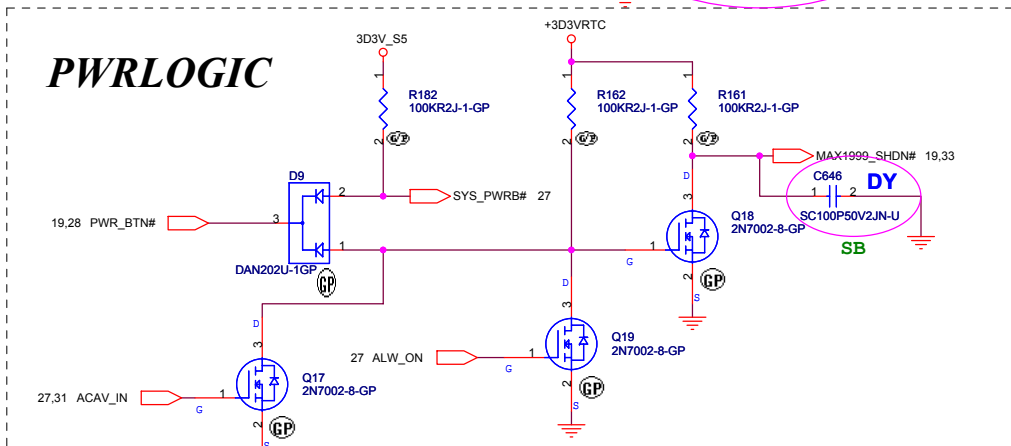
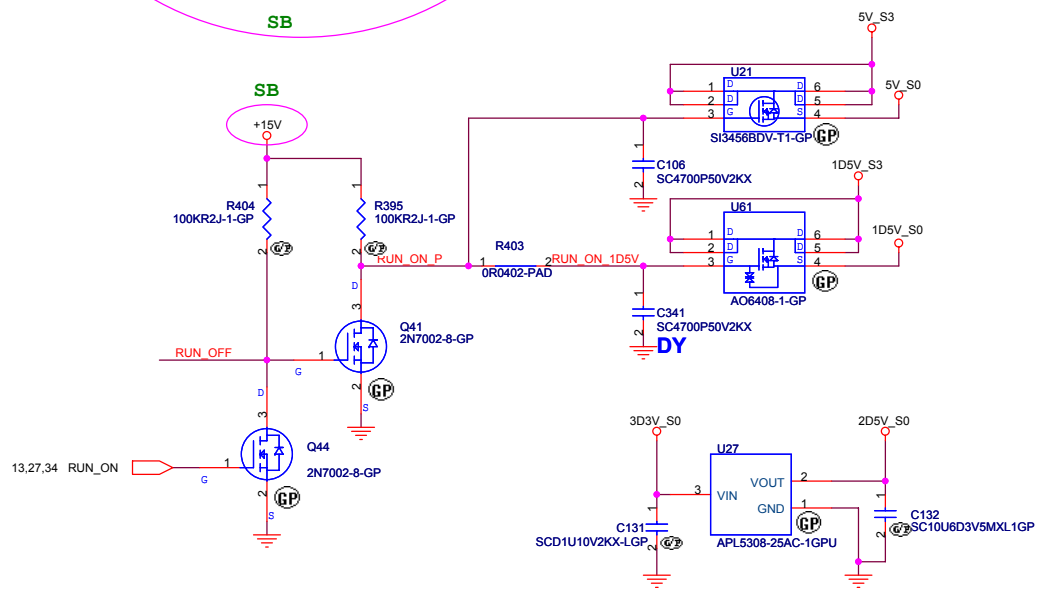
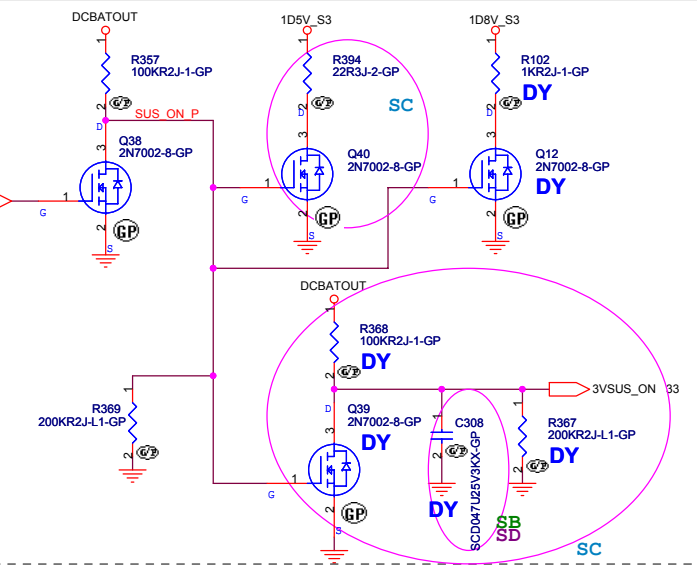
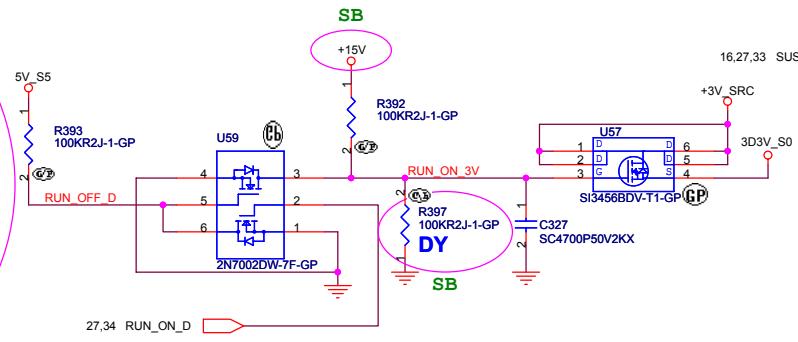
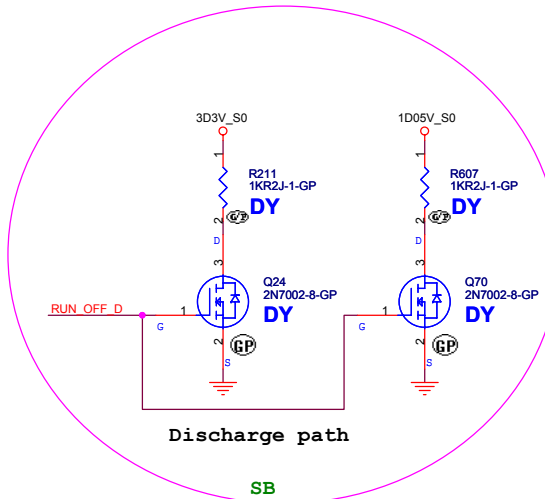
(1D5V=>CH1 , 1D8V=>CH2 , 1D05V =>CH3)



- 13,31,33,34,36,37 DCBATOUT
- 13,32,33,34,36 5V_S5
- 10,34,36,37 1D05V_S0
- 7,9,10,11,12,16,34,36,37 1D8V_S3
- 13,14,17,18,19,20,24,25,27,28,32,36,37 5V_S0
- 12,36 0D9V_S0
- 17,34,36 1D5V_S3

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 39.DC/DC 1D8V/1D5V/1D05V-2	
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Run Power



緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title PWRPLANE&PWRLOGIC
Size A3
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