

Compal Confidential

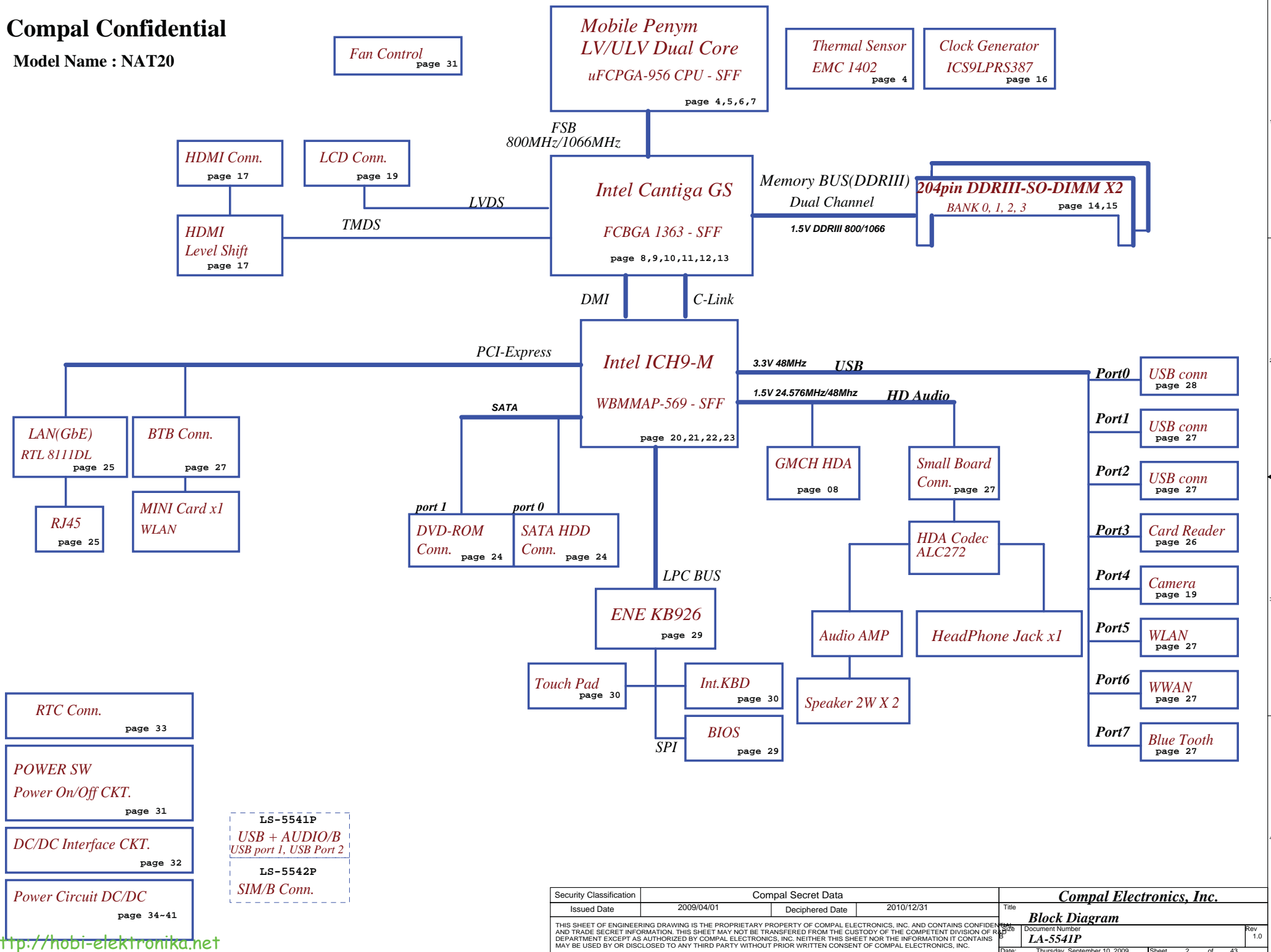
Schematic Document

Rev: 1.0
2009.09.10

Security Classification		Compal Secret Data		Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	Cover Sheet	
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Model Name : NAT20



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Issued Date	2009/04/01	Deciphered Date	2010/12/31	Block Diagram	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	18K +/- 5%	0.436 V	0.503 V	0.538 V
2	33K +/- 5%	0.712 V	0.819 V	0.875 V
3	56K +/- 5%	1.036 V	1.185 V	1.264 V
4	100K +/- 5%	1.453 V	1.650 V	1.759 V
5	200K +/- 5%	1.935 V	2.200 V	2.341 V
6	NC	2.500 V	3.300 V	3.300 V
7				

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	
5	
6	
7	

Symbol Note :



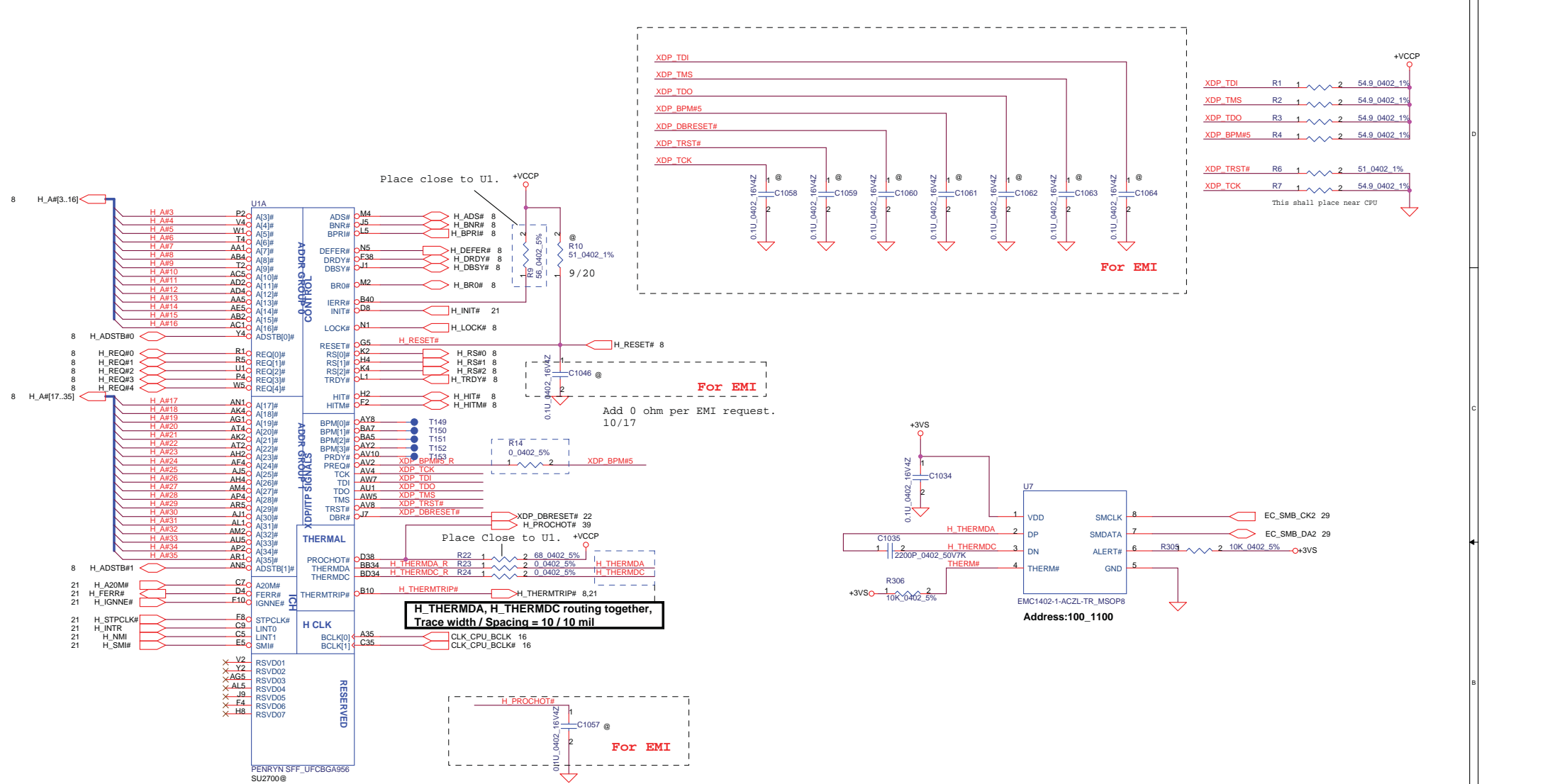
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM
EC_SMB_CLK1 EC_SMB_DA1	KB926	X	V	X	X	X
EC_SMB_CLK2 EC_SMB_DA2	KB926	X	X	X	V	X
ICH_SMBCLK ICH_SMBDATA	ICH9	X	X	X	X	V
MCP_SMB_CLK MCP_SMB_DATA	ICH9	X	X	X	X	X

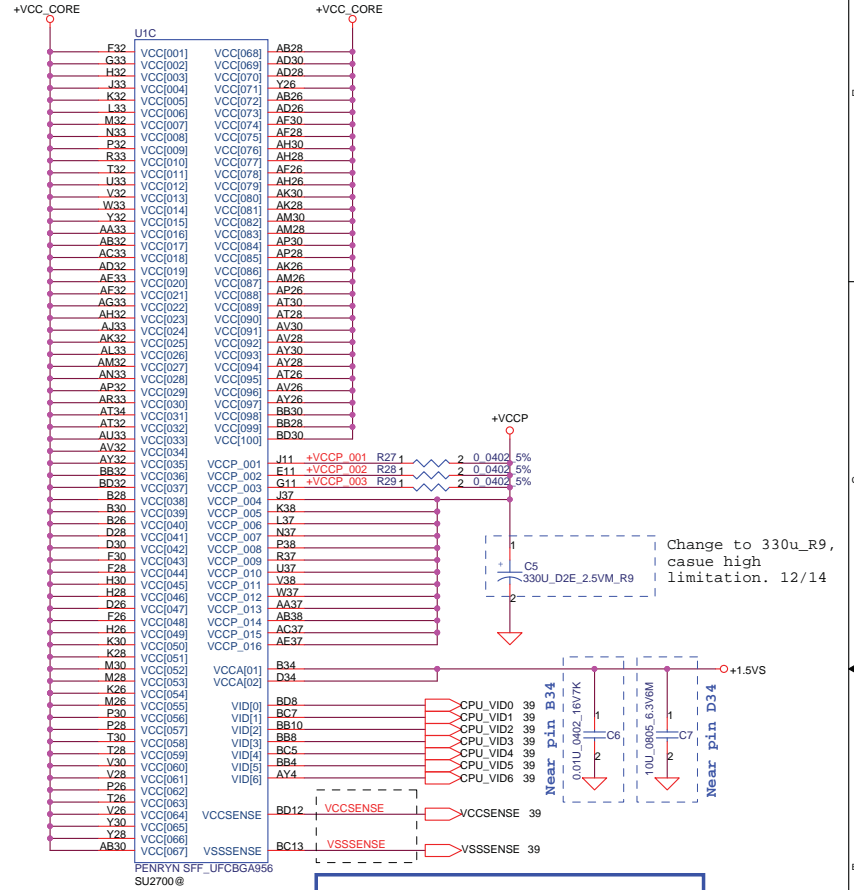
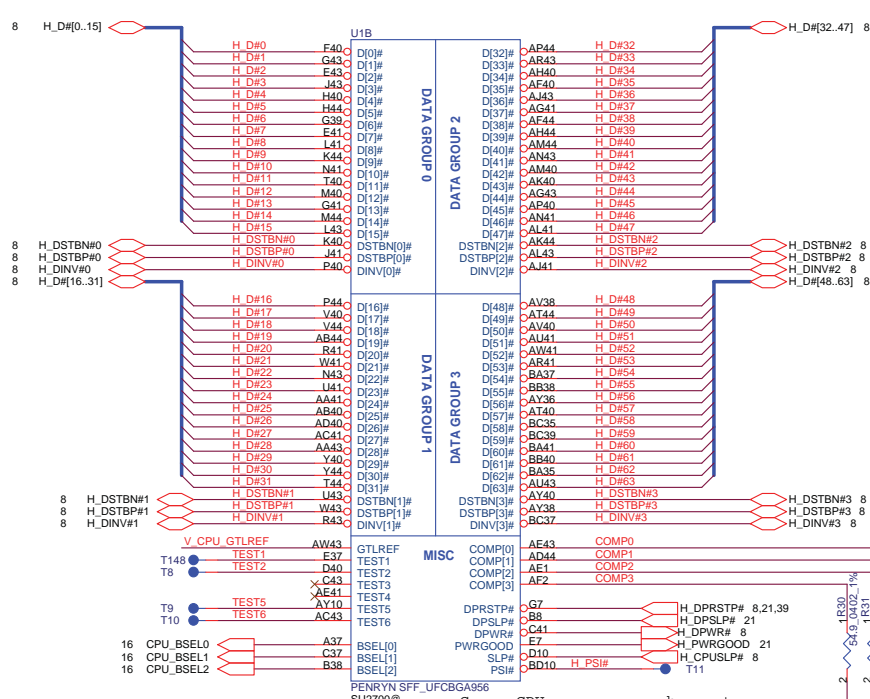
MINI CARD 1 RESERVED +3VALW TO PULL HIGH

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010



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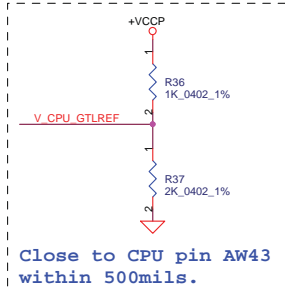
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TFS

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

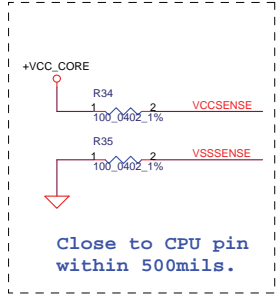
Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

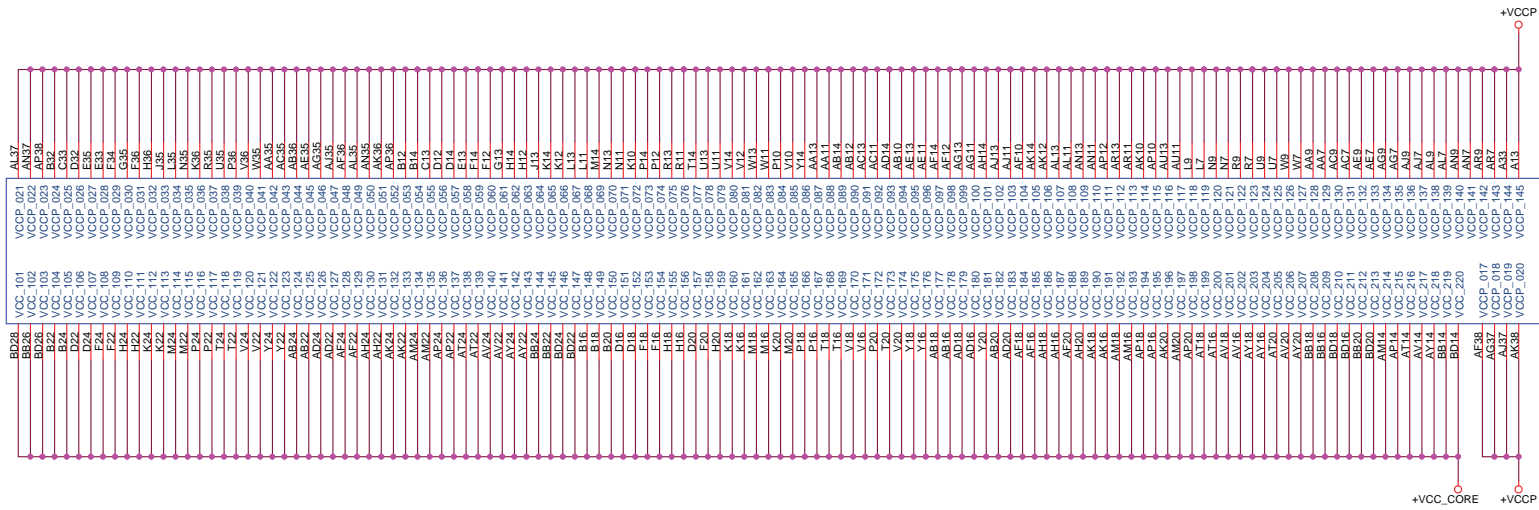
Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AW43 within 500mils.



Close to CPU pin within 500mils.



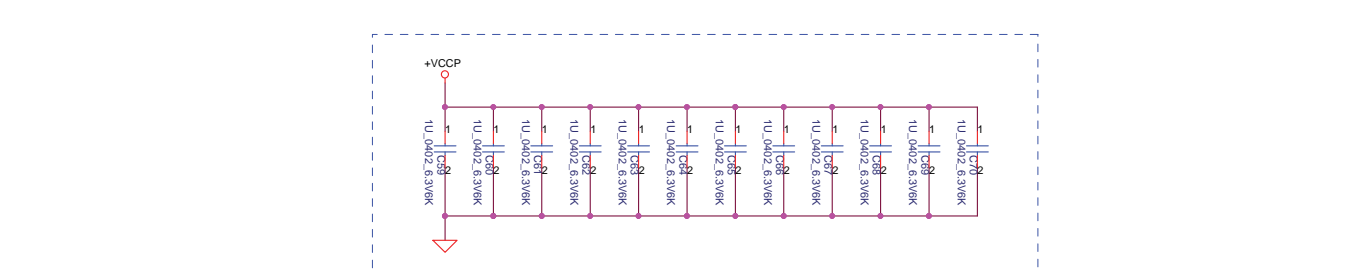
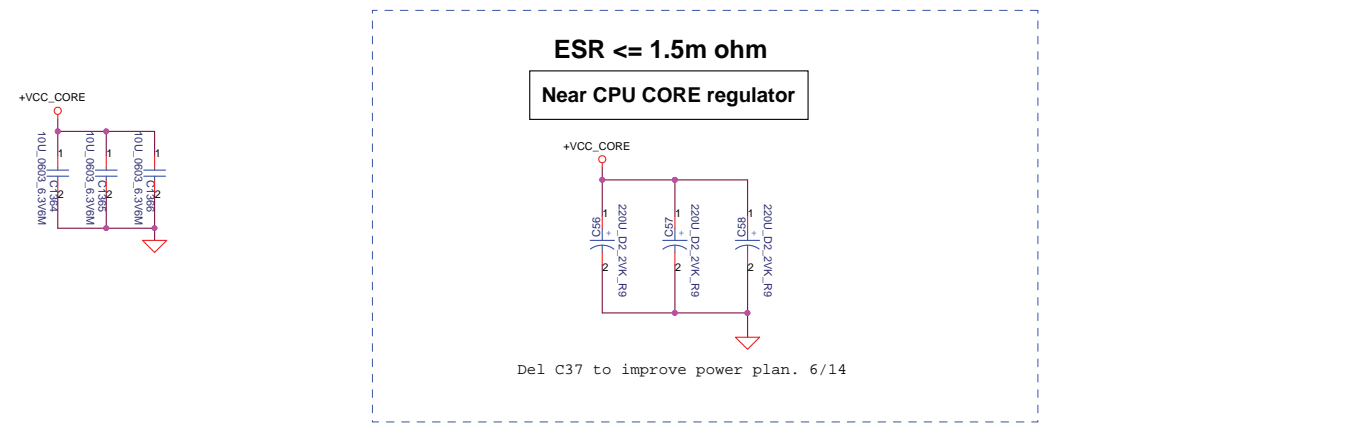
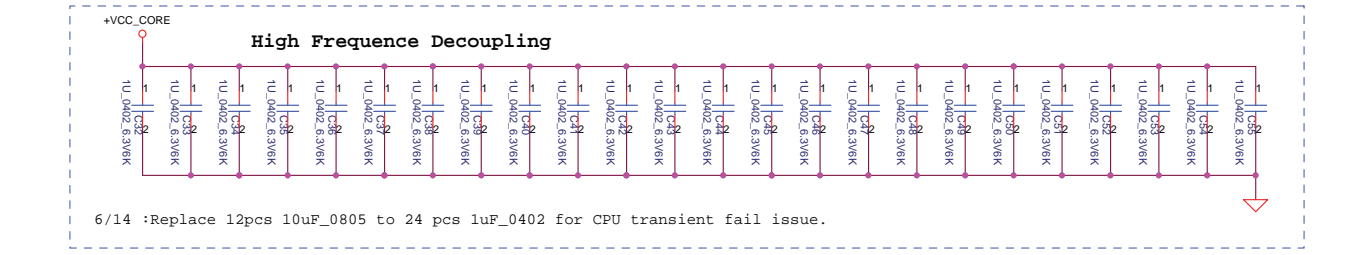
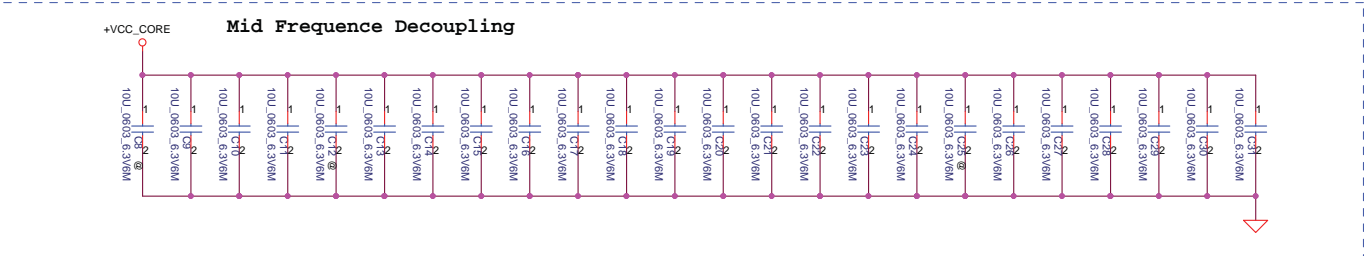
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U1D			
B42	VSS001	VSS082	AM36
F44	VSS002	VSS083	AR35
D42	VSS003	VSS084	AV35
F42	VSS005	VSS086	AW35
H42	VSS006	VSS087	AW33
K42	VSS007	VSS088	AX34
M42	VSS009	VSS090	AV36
P42	VSS010	VSS091	BA33
T42	VSS011	VSS092	BB36
Y42	VSS012	VSS093	BC33
AB42	VSS013	VSS094	BD36
AD42	VSS014	VSS095	CE27
AF42	VSS015	VSS096	CF29
AH42	VSS016	VSS097	CG29
AK42	VSS017	VSS098	CH29
AM42	VSS018	VSS099	CH29
AP42	VSS019	VSS100	CH29
AY44	VSS020	VSS101	CH29
AV44	VSS021	VSS102	CH29
AT42	VSS022	VSS103	CH29
AV42	VSS023	VSS104	CH29
BA43	VSS024	VSS105	CH29
BB42	VSS026	VSS107	CH29
C49	VSS027	VSS108	CH29
G37	VSS028	VSS109	CH29
H38	VSS030	VSS111	CH29
J39	VSS031	VSS112	CH29
M38	VSS032	VSS113	CH29
L39	VSS033	VSS114	CH29
N39	VSS034	VSS115	CH29
R39	VSS035	VSS116	CH29
T38	VSS036	VSS117	CH29
U39	VSS037	VSS118	CH29
W39	VSS038	VSS119	CH29
Y38	VSS039	VSS120	CH29
AC39	VSS040	VSS121	CH29
AD38	VSS041	VSS122	CH29
AE39	VSS043	VSS124	CH29
AG39	VSS044	VSS125	CH29
AH38	VSS045	VSS126	CH29
AJ39	VSS046	VSS127	CH29
AL39	VSS047	VSS128	CH29
AM38	VSS048	VSS129	CH29
AN39	VSS049	VSS130	CH29
AR39	VSS050	VSS131	CH29
AS37	VSS051	VSS132	CH29
AT38	VSS052	VSS133	CH29
AU39	VSS053	VSS134	CH29
AW39	VSS054	VSS135	CH29
AX37	VSS055	VSS136	CH29
AY37	VSS056	VSS137	CH29
BA39	VSS057	VSS138	CH29
BC41	VSS058	VSS139	CH29
BD40	VSS059	VSS140	CH29
BE40	VSS060	VSS141	CH29
BG40	VSS061	VSS142	CH29
BH40	VSS062	VSS143	CH29
BI40	VSS063	VSS144	CH29
BK40	VSS064	VSS145	CH29
BL40	VSS065	VSS146	CH29
BM40	VSS066	VSS147	CH29
BN40	VSS067	VSS148	CH29
BP40	VSS068	VSS149	CH29
BQ40	VSS069	VSS150	CH29
BR40	VSS070	VSS151	CH29
BS40	VSS071	VSS152	CH29
BT40	VSS072	VSS153	CH29
BV40	VSS073	VSS154	CH29
BW40	VSS074	VSS155	CH29
BX40	VSS075	VSS156	CH29
BY40	VSS076	VSS157	CH29
CA40	VSS077	VSS158	CH29
CB40	VSS078	VSS159	CH29
CC40	VSS079	VSS160	CH29
CD40	VSS080	VSS161	CH29
CE40	VSS081	VSS162	CH29
CF40		VSS163	CH29

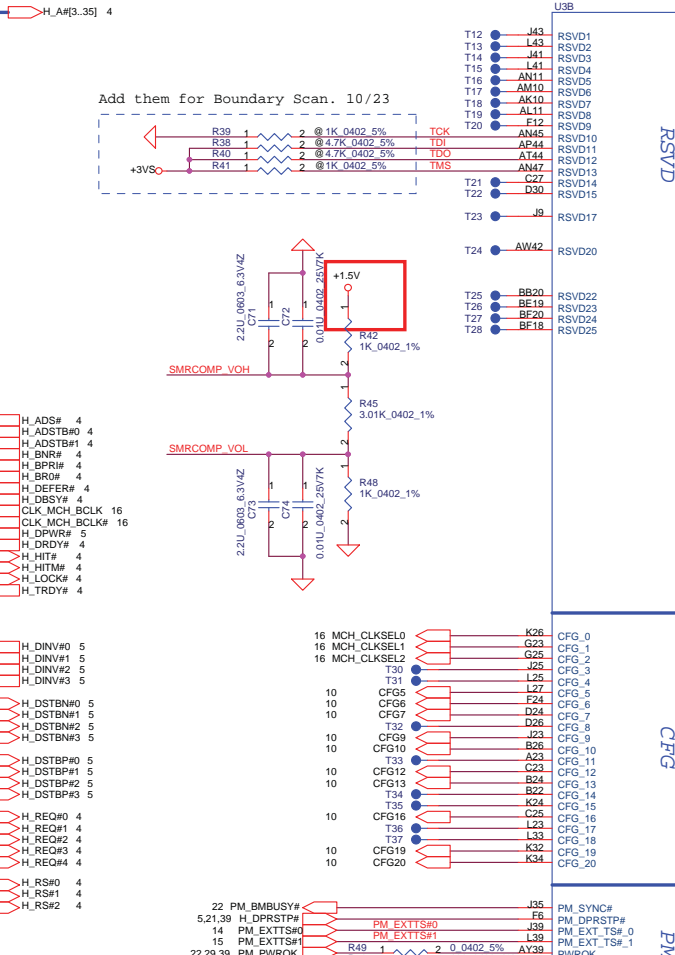
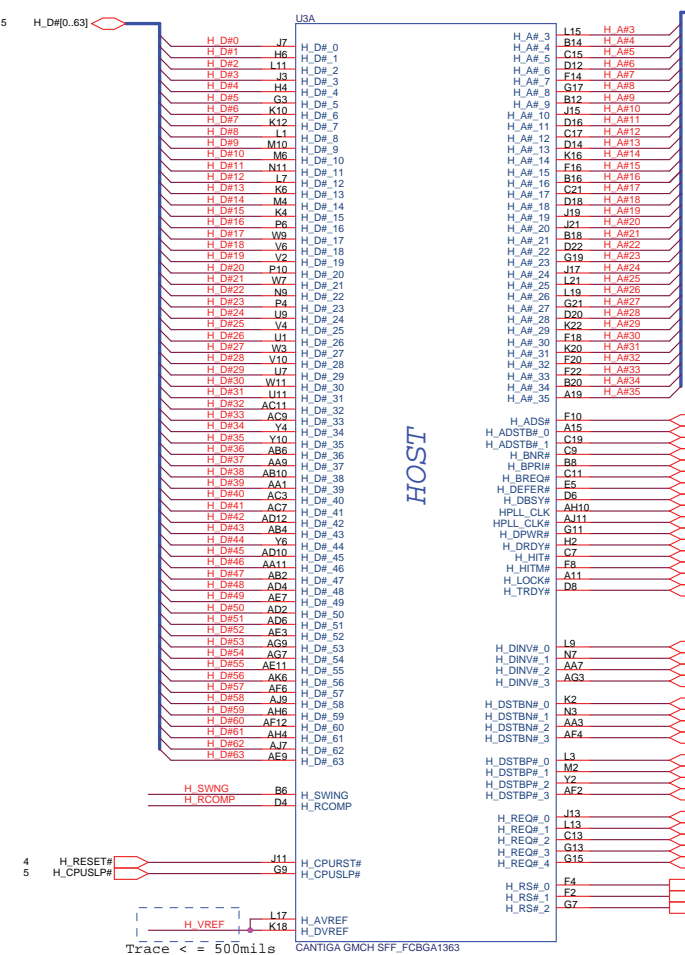
PENRYN SFF_UFCBGA956
SU2700®

U1E			
G25	VSS_164	VSS_280	AA15
G23	VSS_165	VSS_281	AC15
J25	VSS_166	VSS_282	AD10
K25	VSS_167	VSS_283	AE15
L25	VSS_168	VSS_284	AH12
M25	VSS_169	VSS_285	AI15
N25	VSS_170	VSS_286	AJ15
O25	VSS_171	VSS_287	AK15
P25	VSS_172	VSS_288	AL15
Q25	VSS_173	VSS_289	AM12
R25	VSS_174	VSS_290	AN15
S25	VSS_175	VSS_291	AR15
T25	VSS_176	VSS_292	AM10
U25	VSS_177	VSS_293	AT12
V25	VSS_178	VSS_294	AV12
W25	VSS_179	VSS_295	AW13
X25	VSS_180	VSS_296	AW11
Y25	VSS_181	VSS_297	AX12
Z25	VSS_182	VSS_298	AU15
AA25	VSS_183	VSS_299	AW15
AB25	VSS_184	VSS_300	AT10
AC25	VSS_185	VSS_301	BA13
AD25	VSS_186	VSS_302	BA11
AE25	VSS_187	VSS_303	BB12
AF25	VSS_188	VSS_304	BC11
AG25	VSS_189	VSS_305	BA15
AH25	VSS_190	VSS_306	BD15
AI25	VSS_191	VSS_307	BE
AJ25	VSS_192	VSS_308	D6
AK25	VSS_193	VSS_309	D9
AL25	VSS_194	VSS_310	E6
AM25	VSS_195	VSS_311	G9
AN25	VSS_196	VSS_312	H6
AO25	VSS_197	VSS_313	K8
AP25	VSS_198	VSS_314	L6
AQ25	VSS_199	VSS_315	M8
AR25	VSS_200	VSS_316	M6
AS25	VSS_201	VSS_317	PA
AT25	VSS_202	VSS_318	PA
AV25	VSS_203	VSS_319	PA
AW25	VSS_204	VSS_320	TA
AX25	VSS_205	VSS_321	V8
AY25	VSS_206	VSS_322	V8
AZ25	VSS_207	VSS_323	V8
BA25	VSS_208	VSS_324	Y8
BB25	VSS_209	VSS_325	Y6
BC25	VSS_210	VSS_326	Y6
BD25	VSS_211	VSS_327	ABR
BE25	VSS_212	VSS_328	ABE
BF25	VSS_213	VSS_329	AD8
BG25	VSS_214	VSS_330	AD6
BH25	VSS_215	VSS_331	AF8
BI25	VSS_216	VSS_332	AF6
BJ25	VSS_217	VSS_333	AH8
BK25	VSS_218	VSS_334	AH6
BL25	VSS_219	VSS_335	AK8
BM25	VSS_220	VSS_336	AK6
BN25	VSS_221	VSS_337	AM8
BO25	VSS_222	VSS_338	AM6
BP25	VSS_223	VSS_339	AP8
BQ25	VSS_224	VSS_340	AP6
BR25	VSS_225	VSS_341	AT8
BS25	VSS_226	VSS_342	AT6
BT25	VSS_227	VSS_343	AU9
BU25	VSS_228	VSS_344	AV6
BV25	VSS_229	VSS_345	AV7
BW25	VSS_230	VSS_346	AW9
BX25	VSS_231	VSS_347	AY6
BY25	VSS_232	VSS_348	BA9
BZ25	VSS_233	VSS_349	BB6
CA25	VSS_234	VSS_350	BC9
CB25	VSS_235	VSS_351	BD6
CC25	VSS_236	VSS_352	B4
CD25	VSS_237	VSS_353	C3
CE25	VSS_238	VSS_354	E3
CF25	VSS_239	VSS_355	G3
CG25	VSS_240	VSS_356	J3
CH25	VSS_241	VSS_357	L3
CI25	VSS_242	VSS_358	N3
CJ25	VSS_243	VSS_359	R3
CK25	VSS_244	VSS_360	U3
CL25	VSS_245	VSS_361	VA
CM25	VSS_246	VSS_362	AA3
CN25	VSS_247	VSS_363	AC3
CO25	VSS_248	VSS_364	AE3
CP25	VSS_249	VSS_365	AG3
CQ25	VSS_250	VSS_366	AJ3
CR25	VSS_251	VSS_367	AL3
CS25	VSS_252	VSS_368	AN3
CT25	VSS_253	VSS_369	AR3
CU25	VSS_254	VSS_370	AU3
CV25	VSS_255	VSS_371	AW3
CA25	VSS_256	VSS_372	BA3
CB25	VSS_257	VSS_373	BC3
CC25	VSS_258	VSS_374	E1
CD25	VSS_259	VSS_375	G1
CE25	VSS_260	VSS_376	AW1
CF25	VSS_261	VSS_377	BA1
CG25	VSS_262	VSS_378	BB2
CH25	VSS_263	VSS_379	A41
CI25	VSS_264	VSS_380	A39
CJ25	VSS_265	VSS_381	A29
CK25	VSS_266	VSS_382	A27
CL25	VSS_267	VSS_383	A31
CM25	VSS_268	VSS_384	A25
CN25	VSS_269	VSS_385	A23
CO25	VSS_270	VSS_386	A21
CP25	VSS_271	VSS_387	A19
CQ25	VSS_272	VSS_388	A17
CR25	VSS_273	VSS_389	A11
CS25	VSS_274	VSS_390	A15
CT25	VSS_275	VSS_391	A7
CU25	VSS_276	VSS_392	A5
CV25	VSS_277	VSS_393	A9
CA25	VSS_278	VSS_394	BD4
CB25	VSS_279	VSS_395	

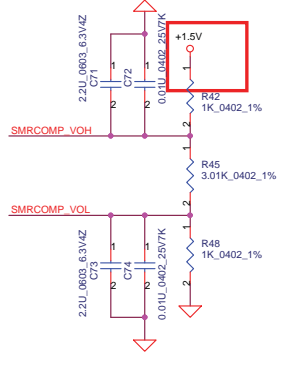
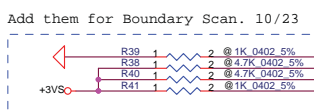
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SU2700®



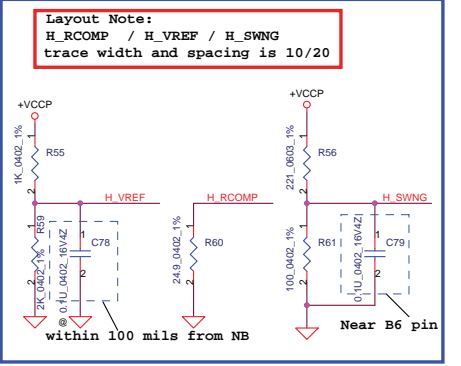
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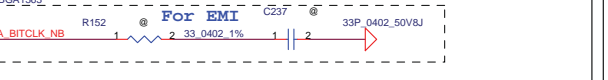
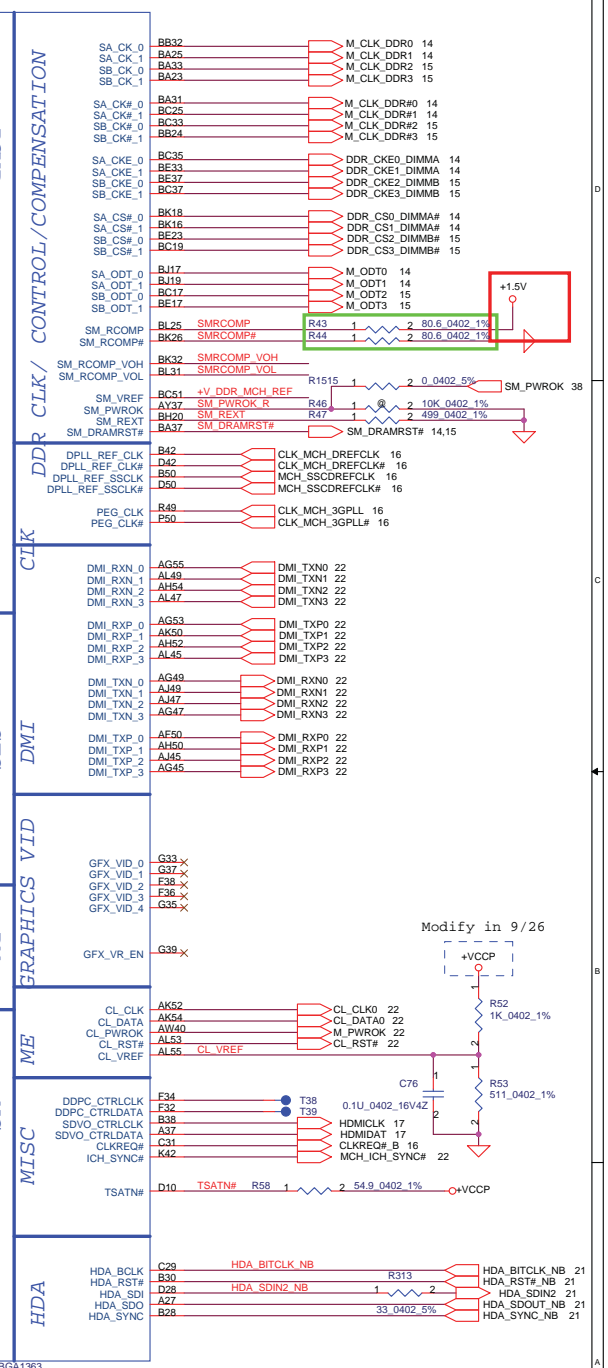
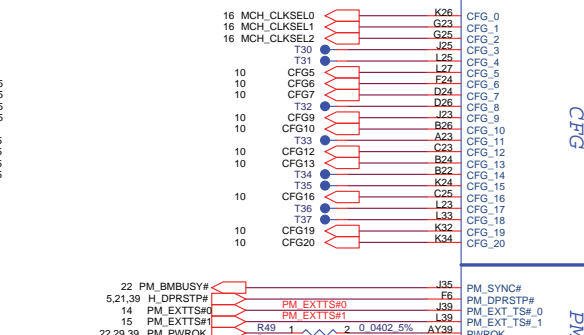
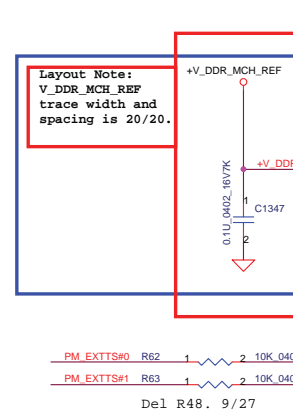
HOST

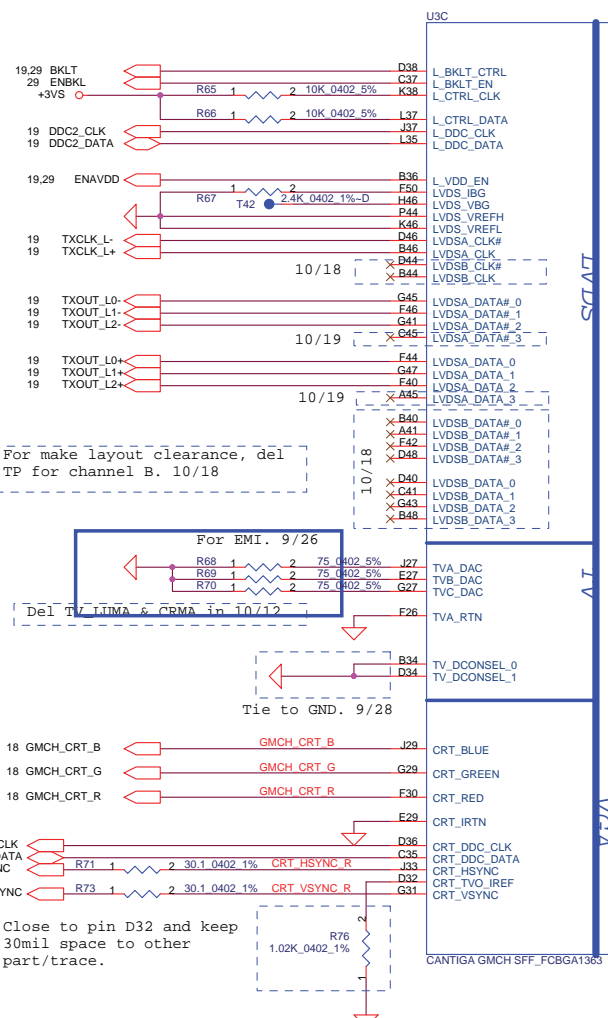


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



layout note:
Place them close to U3 pin BC51.





For make layout clearance, del TP for channel B. 10/18

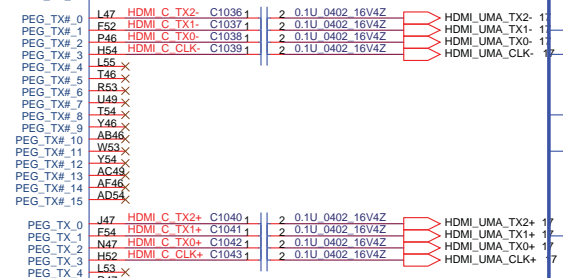
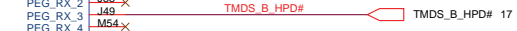
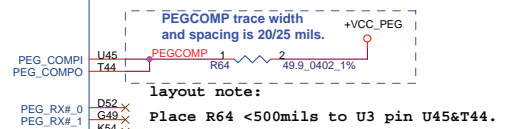
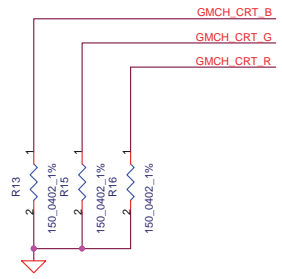
For EMI. 9/26
Del TV IITMA & CRMA in 10/12

Tie to GND. 9/28

Close to pin D32 and keep 30mil space to other part/trace.

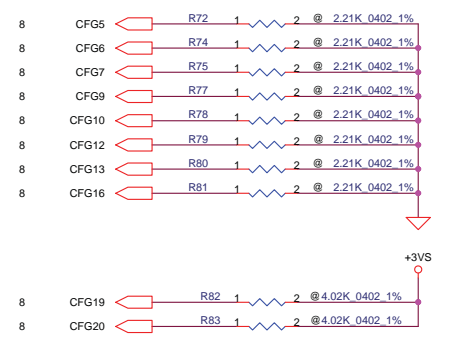
Del R82, R83. 10/18

Remove R84 ~ R86 since already have 75ohm of page17. 10/27



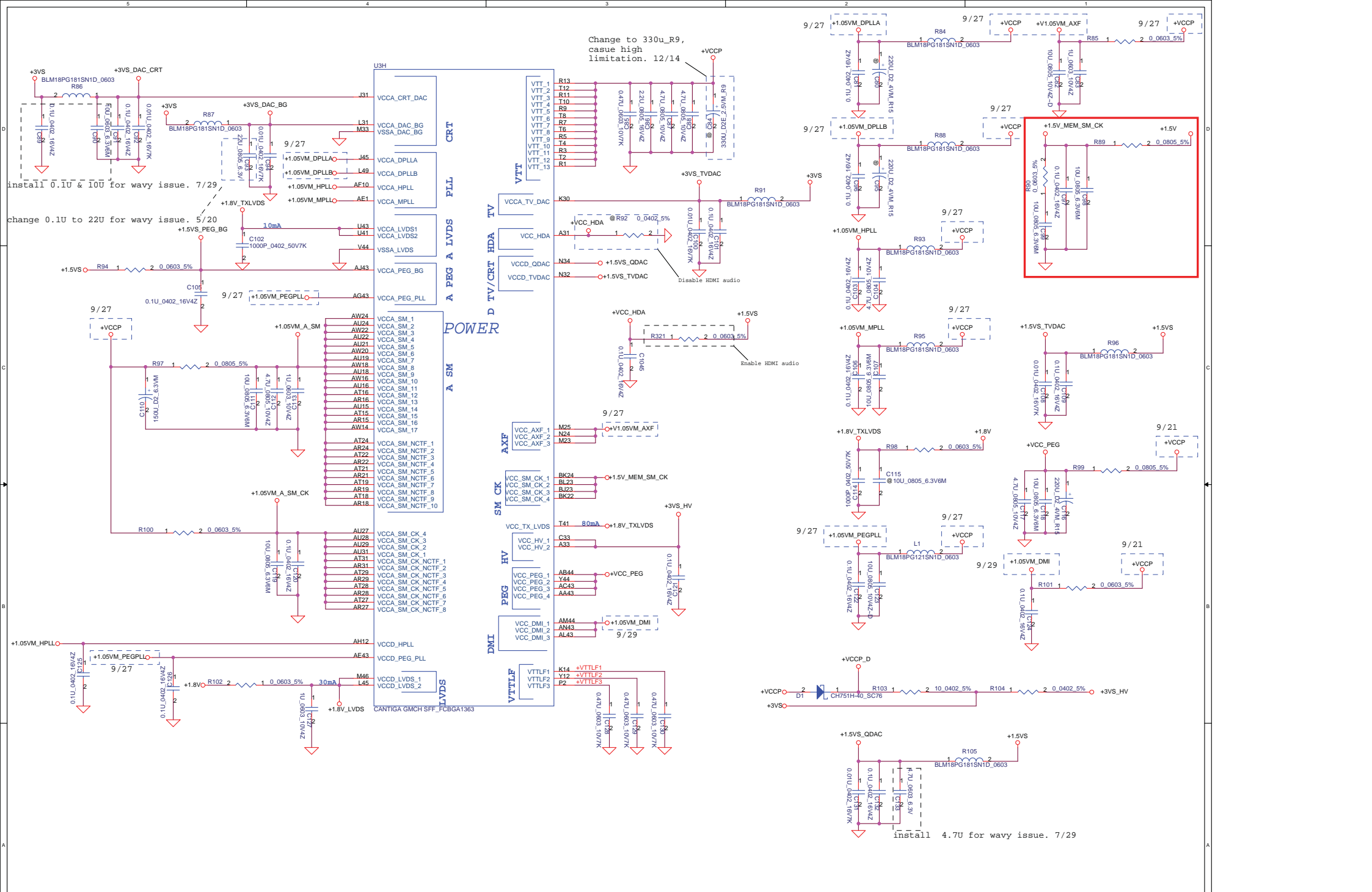
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * 1 = Reverse Lane (Lane number in Order)
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



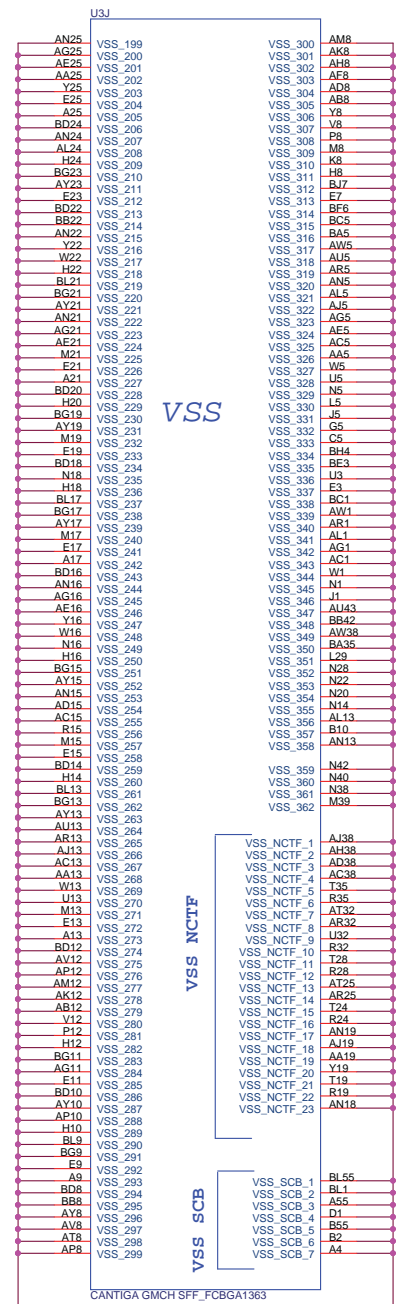
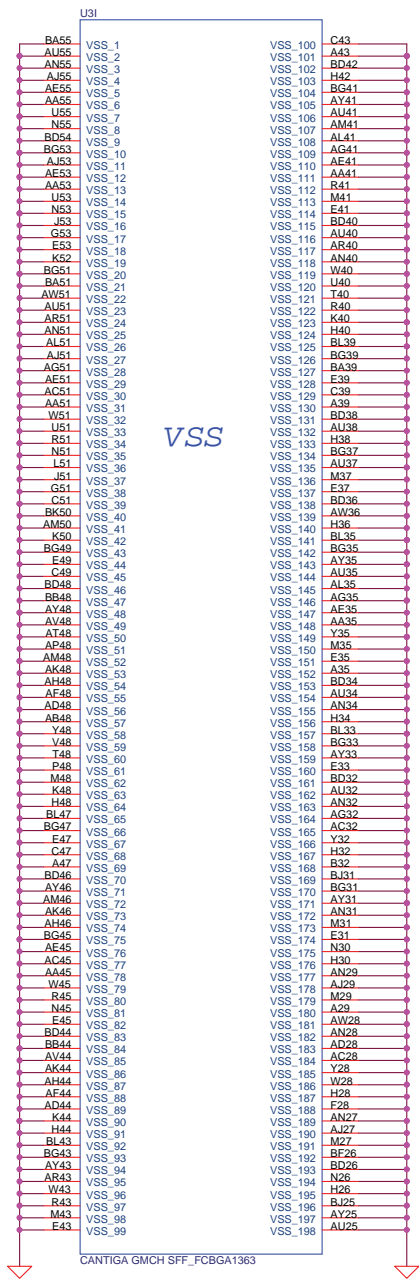
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Title		Compal Electronics, Inc.	
Product		Cantiga(3/6)-LVDS/TV/CRT	
Document Number	LA-5541P	Rev	1.0
Date:	Thursday, September 10, 2009	Sheet	10 of 43

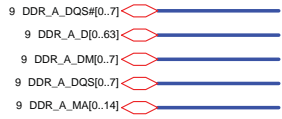


<http://hobi-elektronika.net>

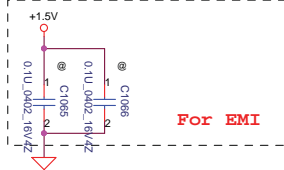
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	Title
				Cantiga(4/6)-PWR
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				LA-5541P
Date:	Thursday, September 10, 2009	Sheet	11	Rev 1.0
			of	43



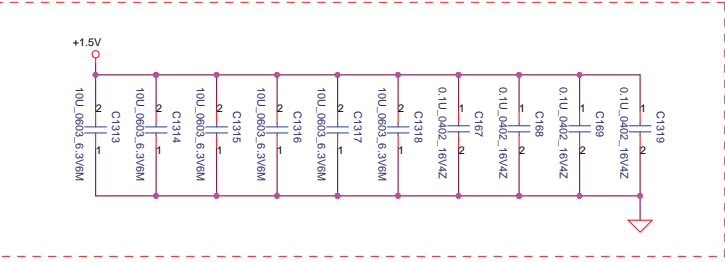
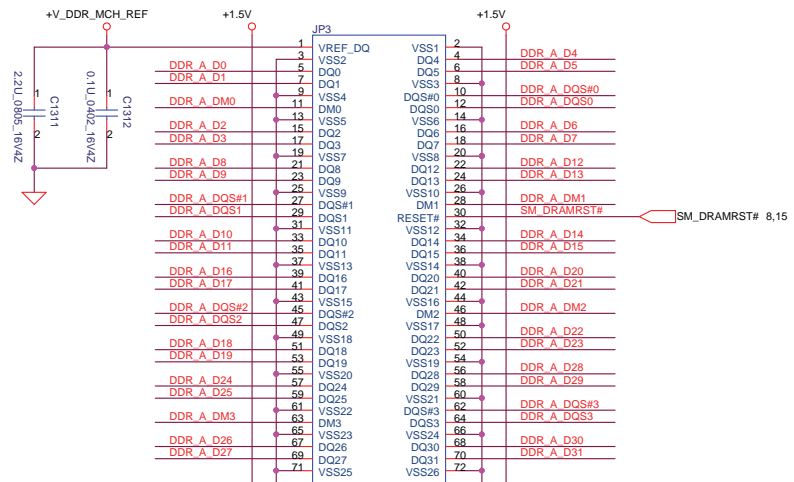
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Date:	Thursday, September 10, 2009	Sheet	13	of 43



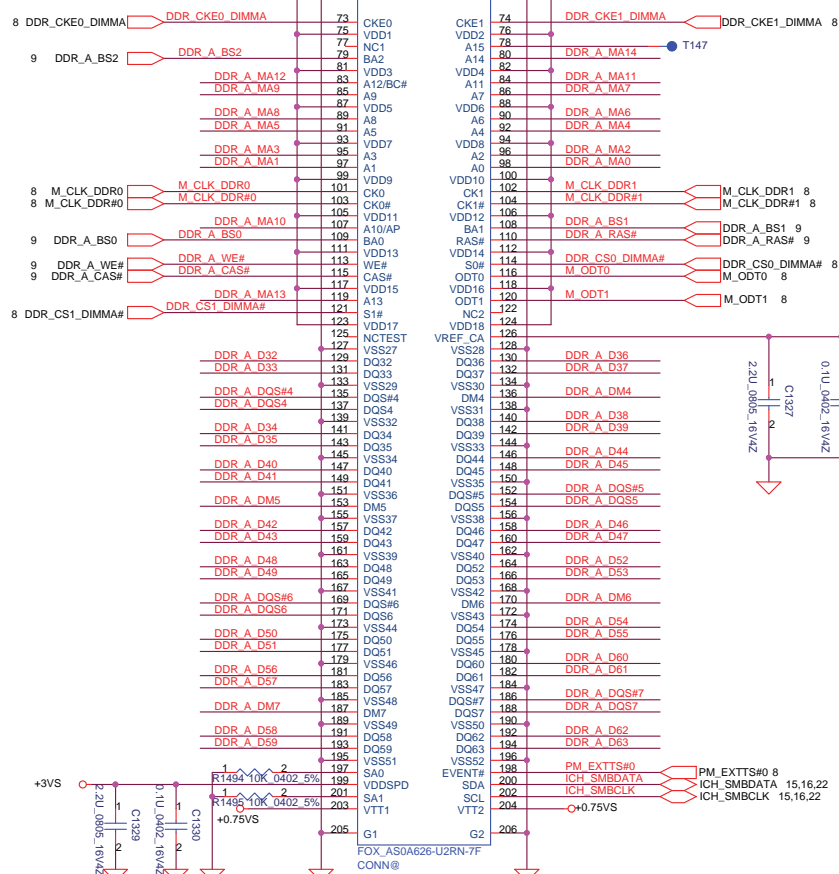
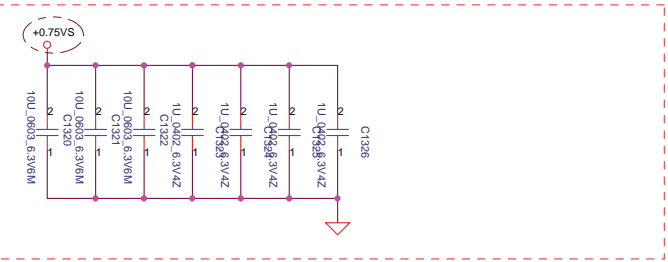
Layout Note:
Place near JP3



For EMI

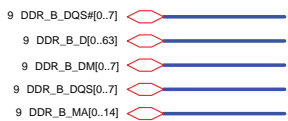


Layout Note:
Place near JP3.203,204

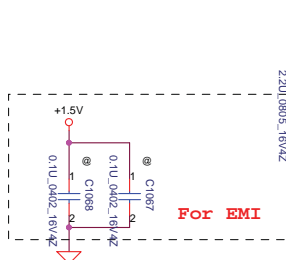


Top side

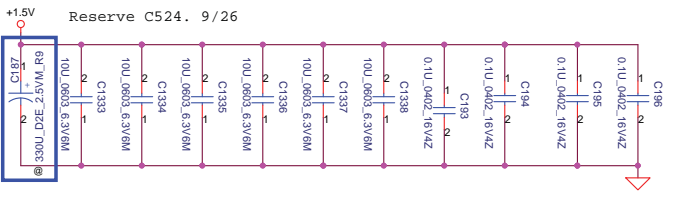
Security Classification	Compal Secret Data		Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	Compal Electronics, Inc.
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Date: Thursday, September 10, 2009				Sheet 14 of 43



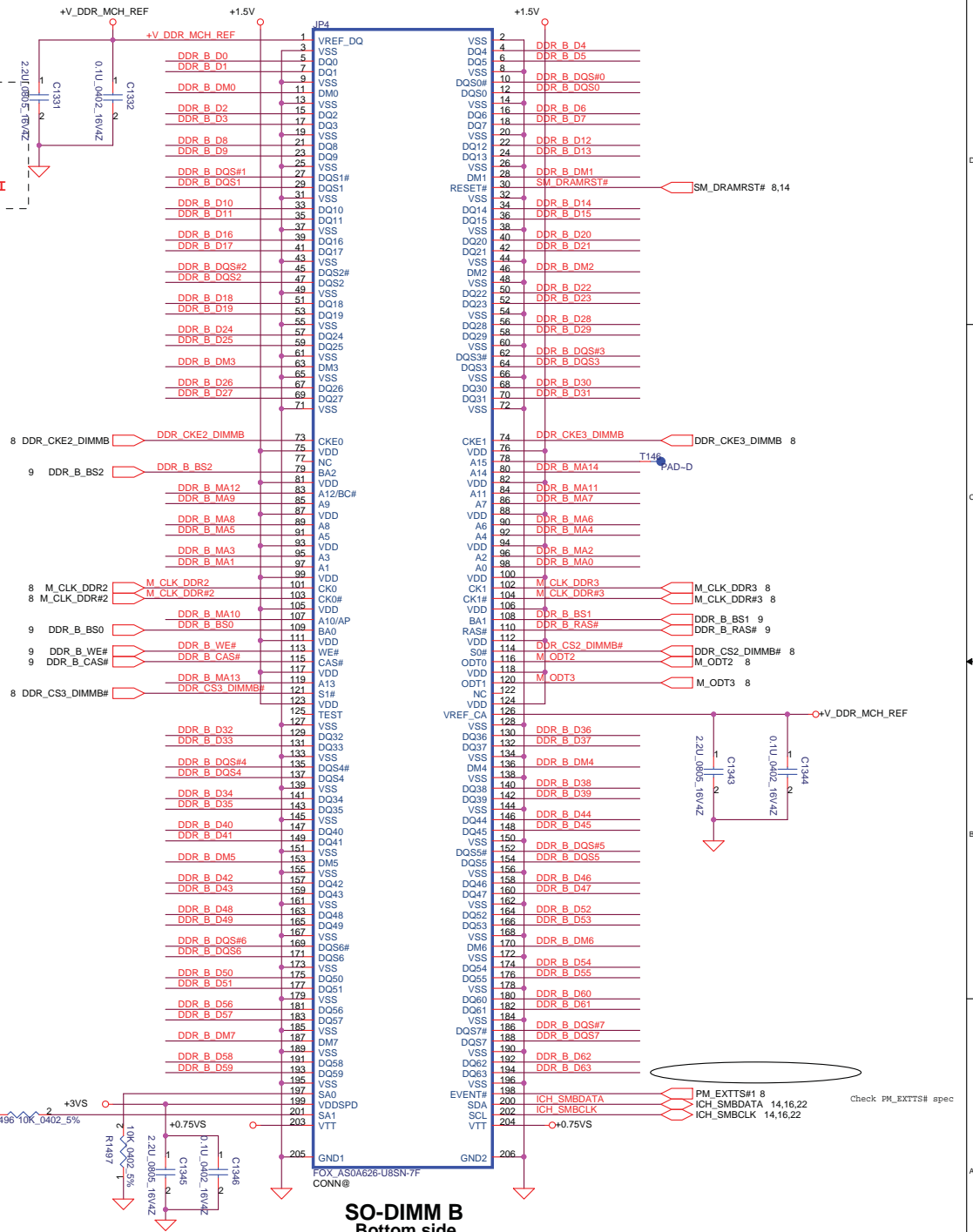
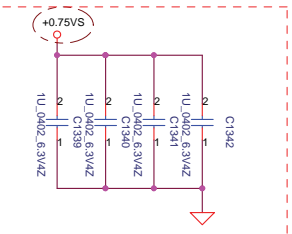
Layout Note:
Place near JP4



For EMI



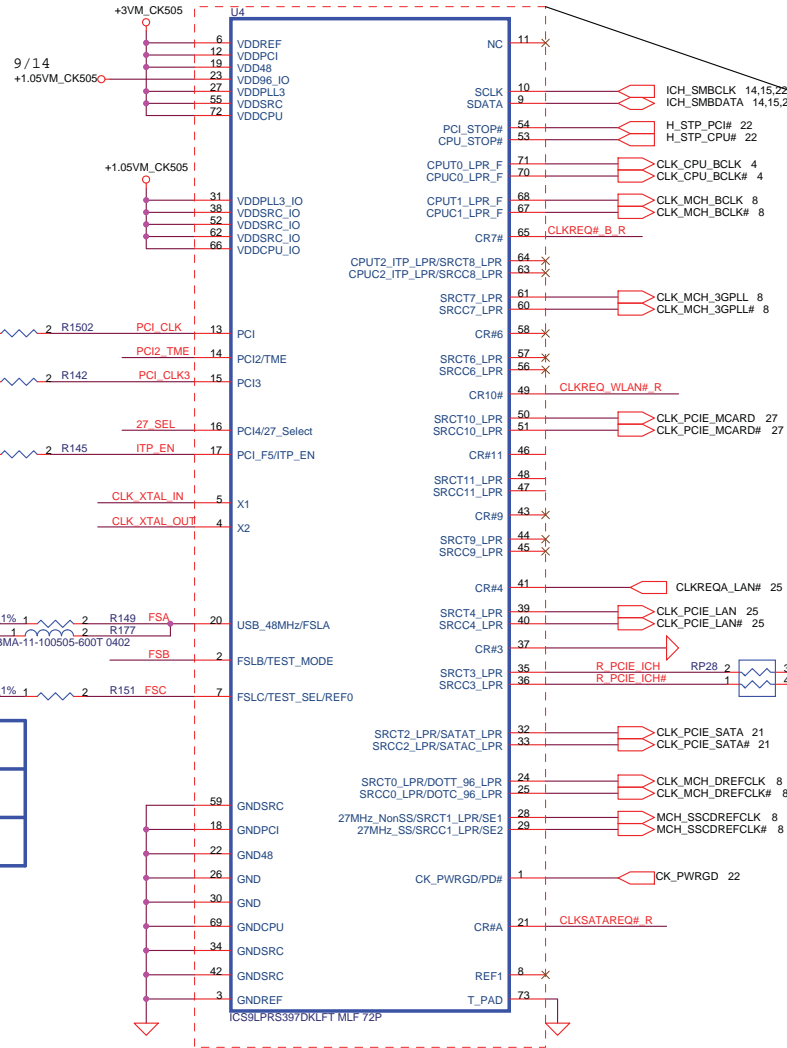
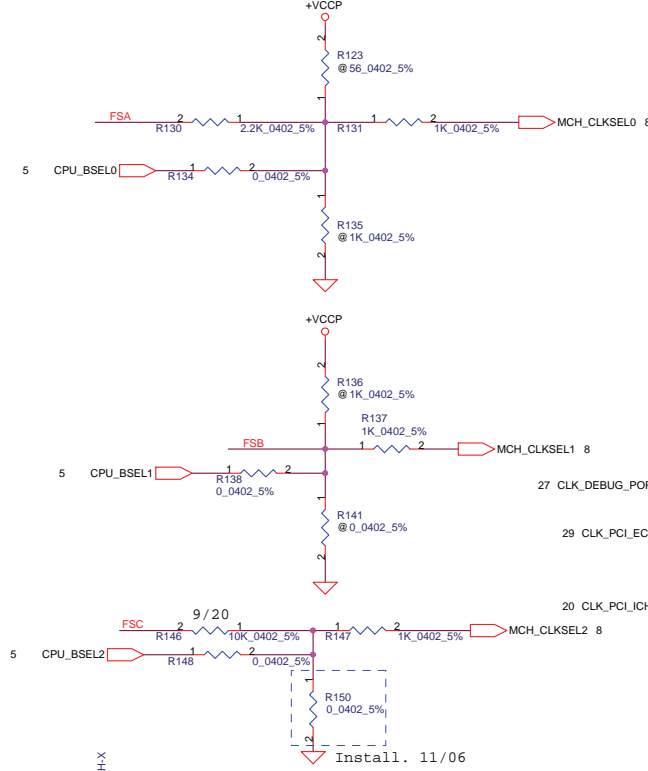
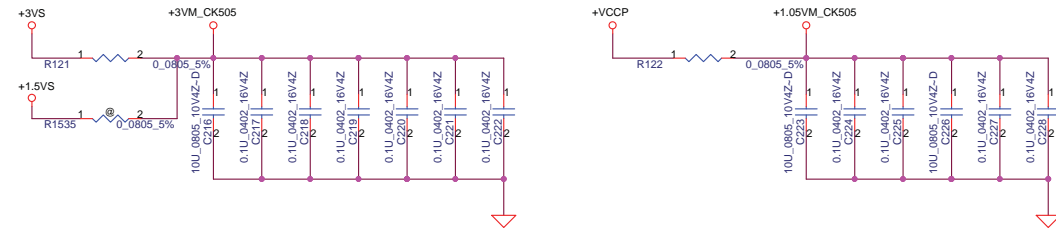
Layout Note:
Place near JP4.203,204



**SO-DIMM B
Bottom side**

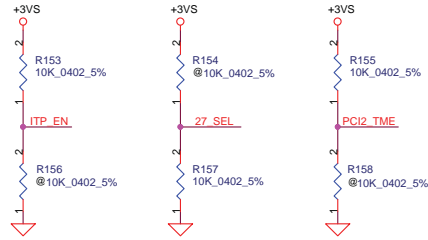
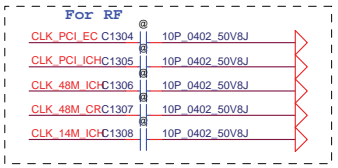
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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	FSB MHz	SRC MHz	PCI MHz
0	0	0	266	1066	100	33.3
0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3



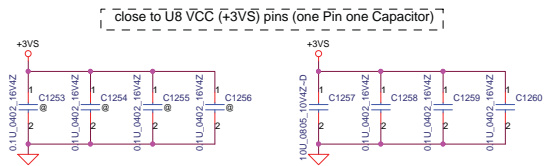
SA00020H10 for Compal
SA00001YJ20 for HP

ITP_EN	0 = SRC8/SRC8# *1 = ITP/ITP#
27_SEL	*0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed



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Compal Electronics, Inc.	
Title	Clock Generator CK505
Document Number	LA-554IP
Rev	1.0
Date:	Thursday, September 10, 2009
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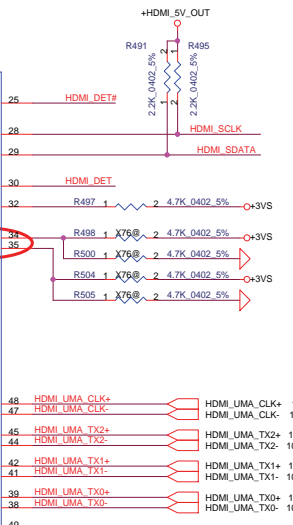
Intel Cantiga TMD5 Pin Definition

TMD5_B_CLK	PEG_TXP_3
TMD5_B_CLK#	PEG_TXN_3
TMD5_B_DATA0	PEG_TXP_2
TMD5_B_DATA0#	PEG_TXN_2
TMD5_B_DATA1	PEG_TXP_1
TMD5_B_DATA1#	PEG_TXN_1
TMD5_B_DATA2	PEG_TXP_0
TMD5_B_DATA2#	PEG_TXN_0
TMD5_B_HPD#	PEG_RXP_3

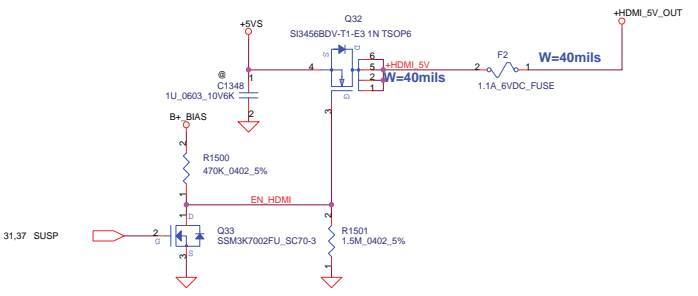


Trace AS Short PASS

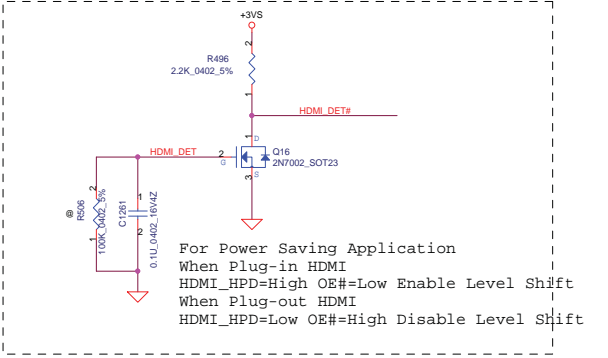
DP139 need stuff R492,R494, R498 and change R503 value to 3.9K
ASM1442T need stuff R503 value 3.6K



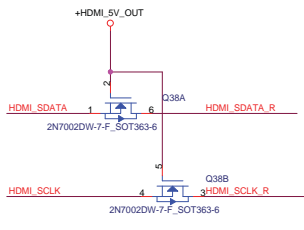
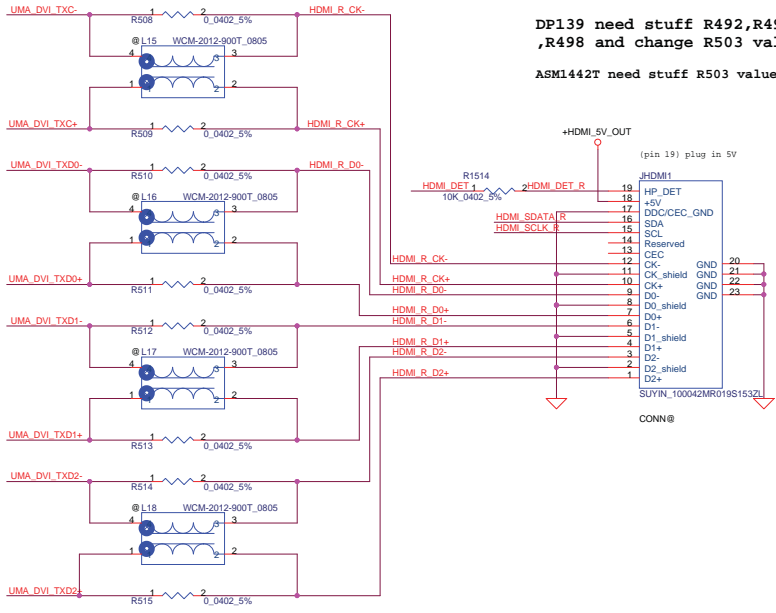
20071031:
Add U1.49 (THERMAL_GND) to GND Plane



Pin34	Pin35	Equalization	Default
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	*

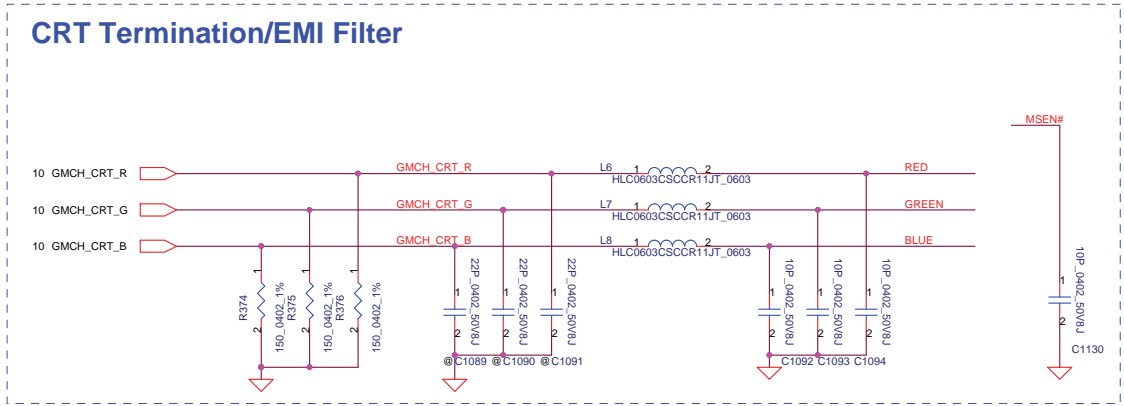
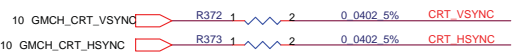
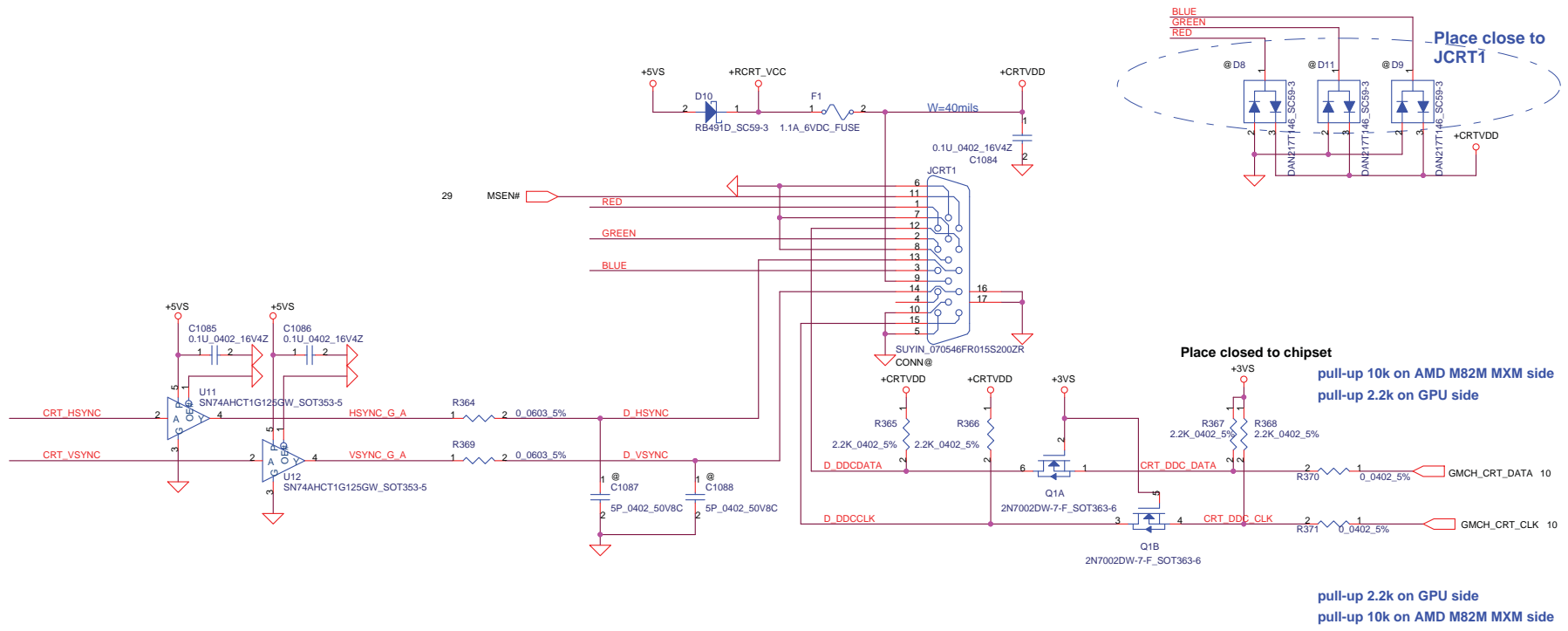


For Power Saving Application
 When Plug-in HDMI
 HDMI_HPD=High OE#=Low Enable Level Shift
 When Plug-out HDMI
 HDMI_HPD=Low OE#=High Disable Level Shift

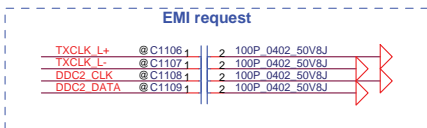
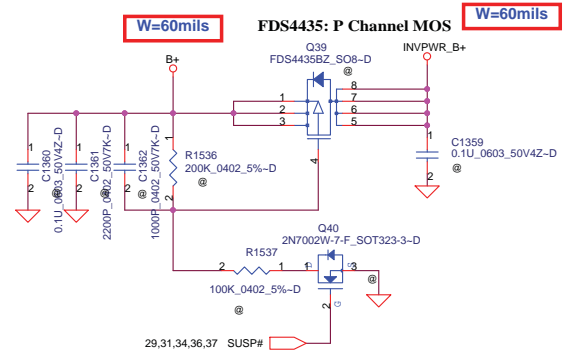
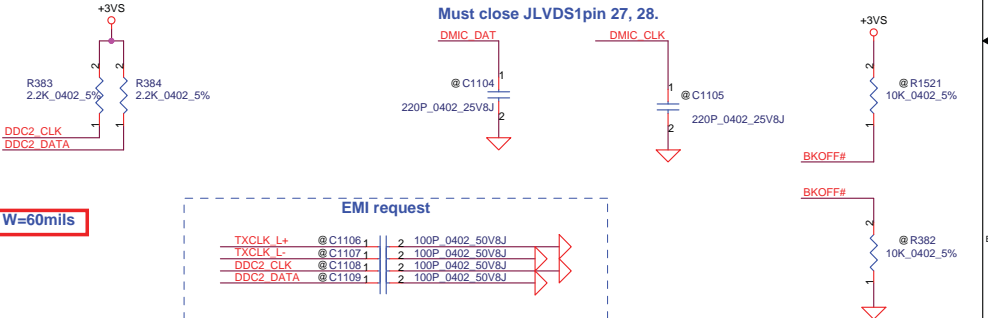
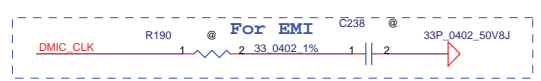
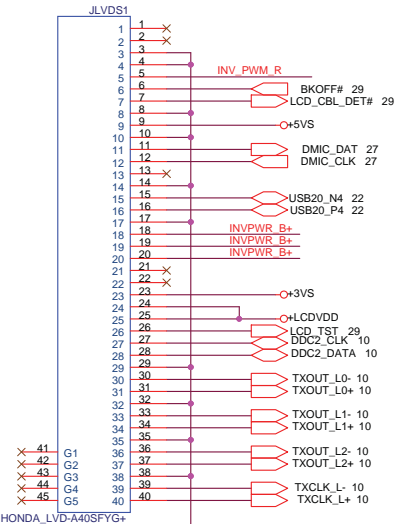
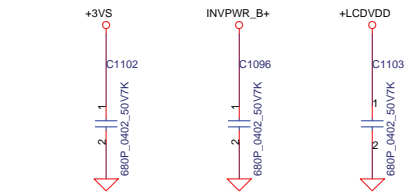
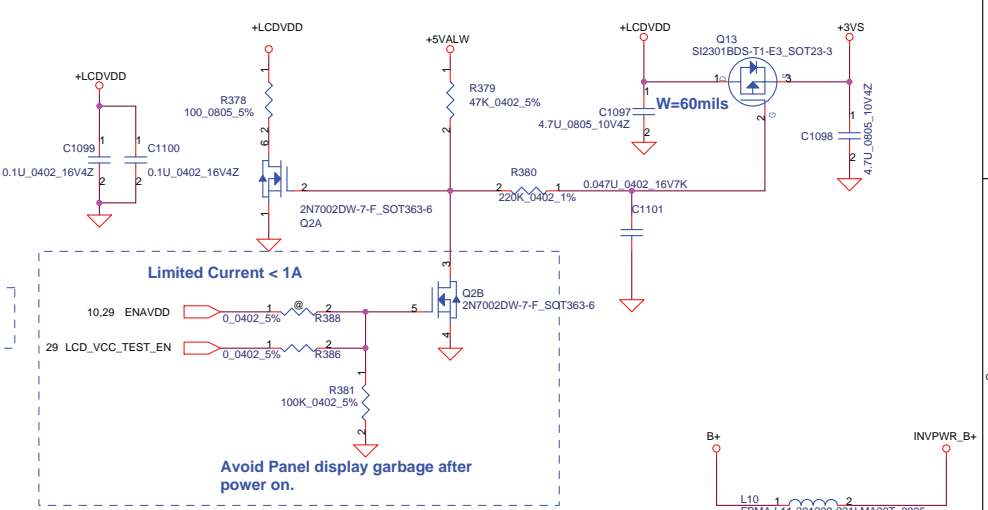
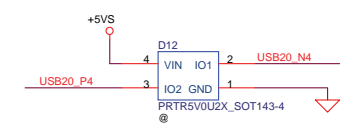
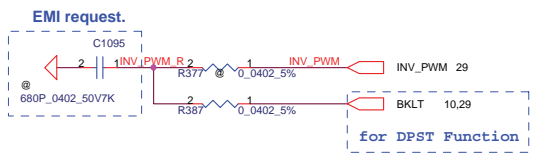


Q38 Please close to JHDMI1

Pin 10	Pin 4	Pin 3	Swing	Pre-amp	Slew-rate	Default
0	0	0	450	0	0	
0	0	1	420	0	0	
0	1	0	450	0	0	
0	1	1	460	0	-4dB	*
1	0	0	340	0	0	
1	0	1	400	2dB	0	
1	1	0	400	2dB	0	
1	1	1	420	0	0	

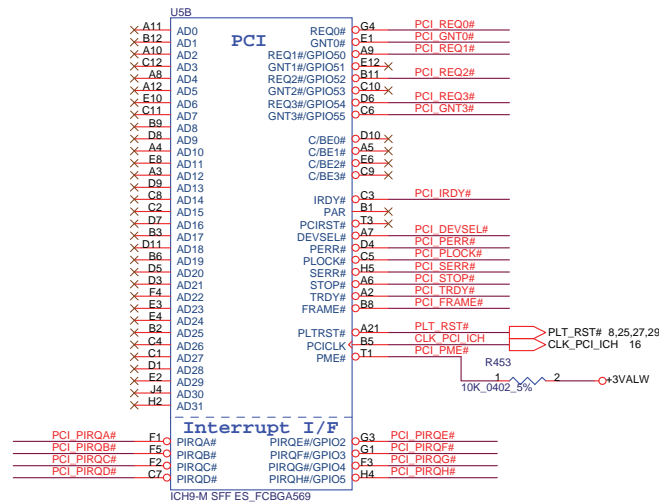
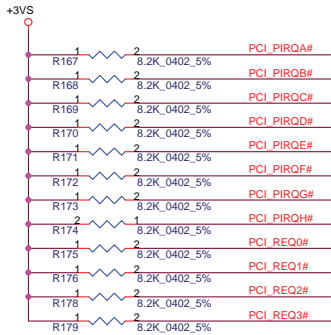
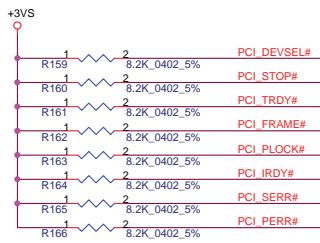


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Date: Thursday, September 10, 2009				Sheet 18 of 43	

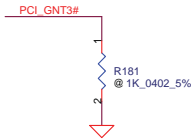


LVDS CONN & USB Camera + Dig Mic

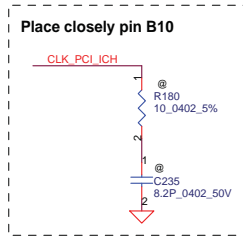
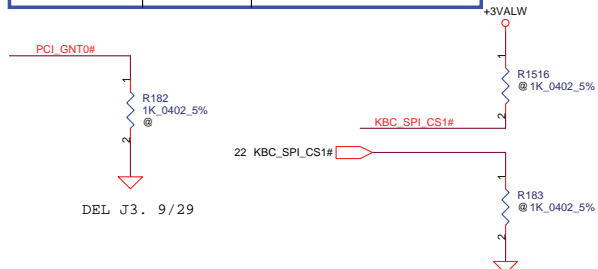
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				Date:	Thursday, September 10, 2009	Sheet 19 of 43



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

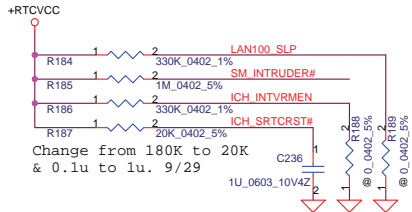


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

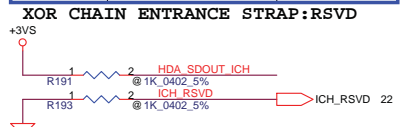


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Compal Electronics, Inc.	
Title	ICH9M(I/4)-PCI/INT
Document Number	LA-5541P
Date	Thursday, September 10, 2009
Sheet	20 of 43

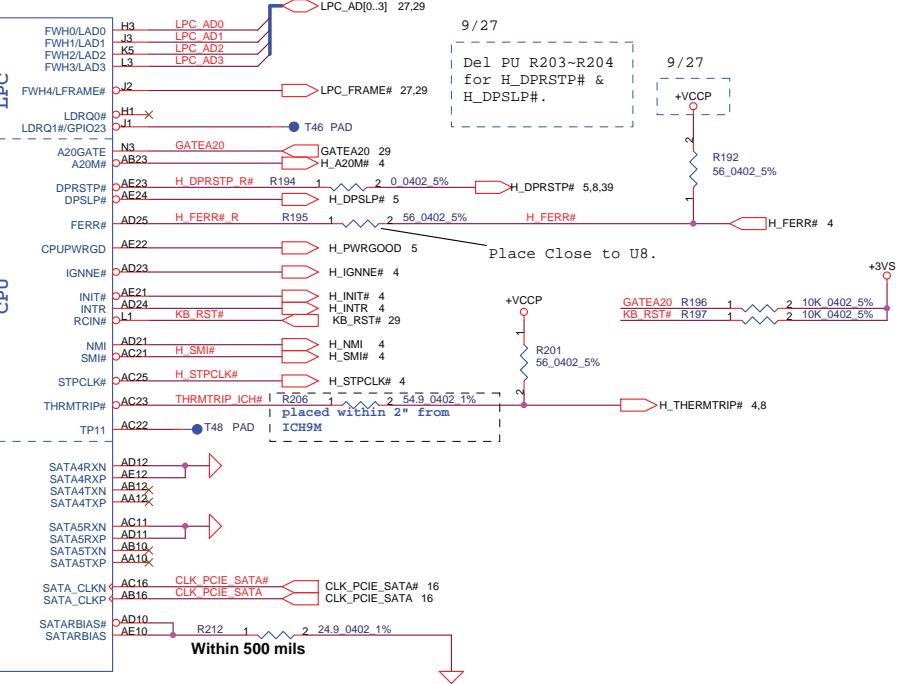
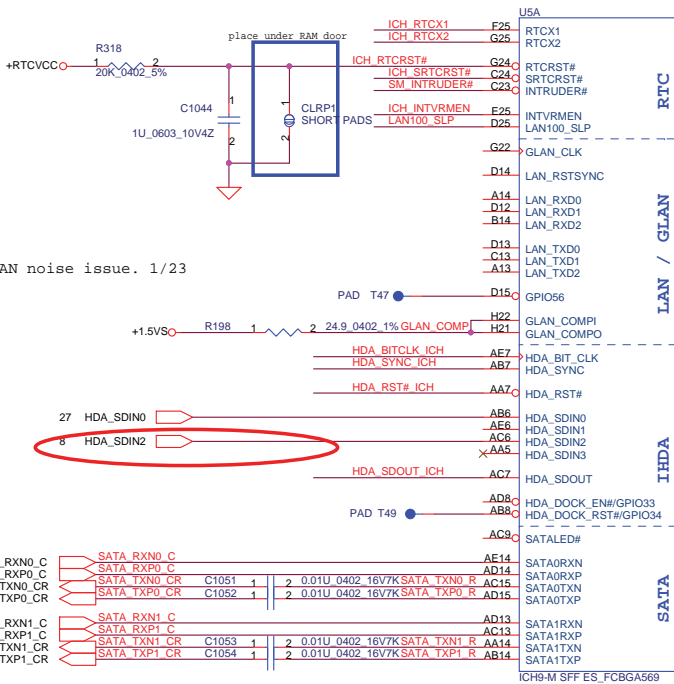


ICH_RSVD	HDA_SDOUT_CODEC	Description
0	0	RV
0	1	XOR
1	0	Normal (D)
1	1	PCIE Bit



Add C599 ~ C602 to solve WWAN noise issue. 1/23

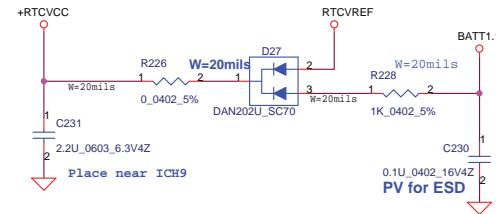
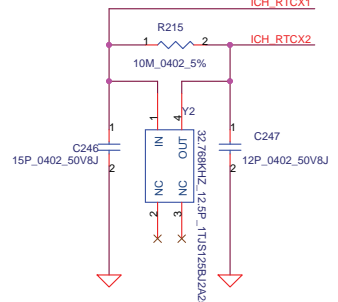
Remove R227 & C199



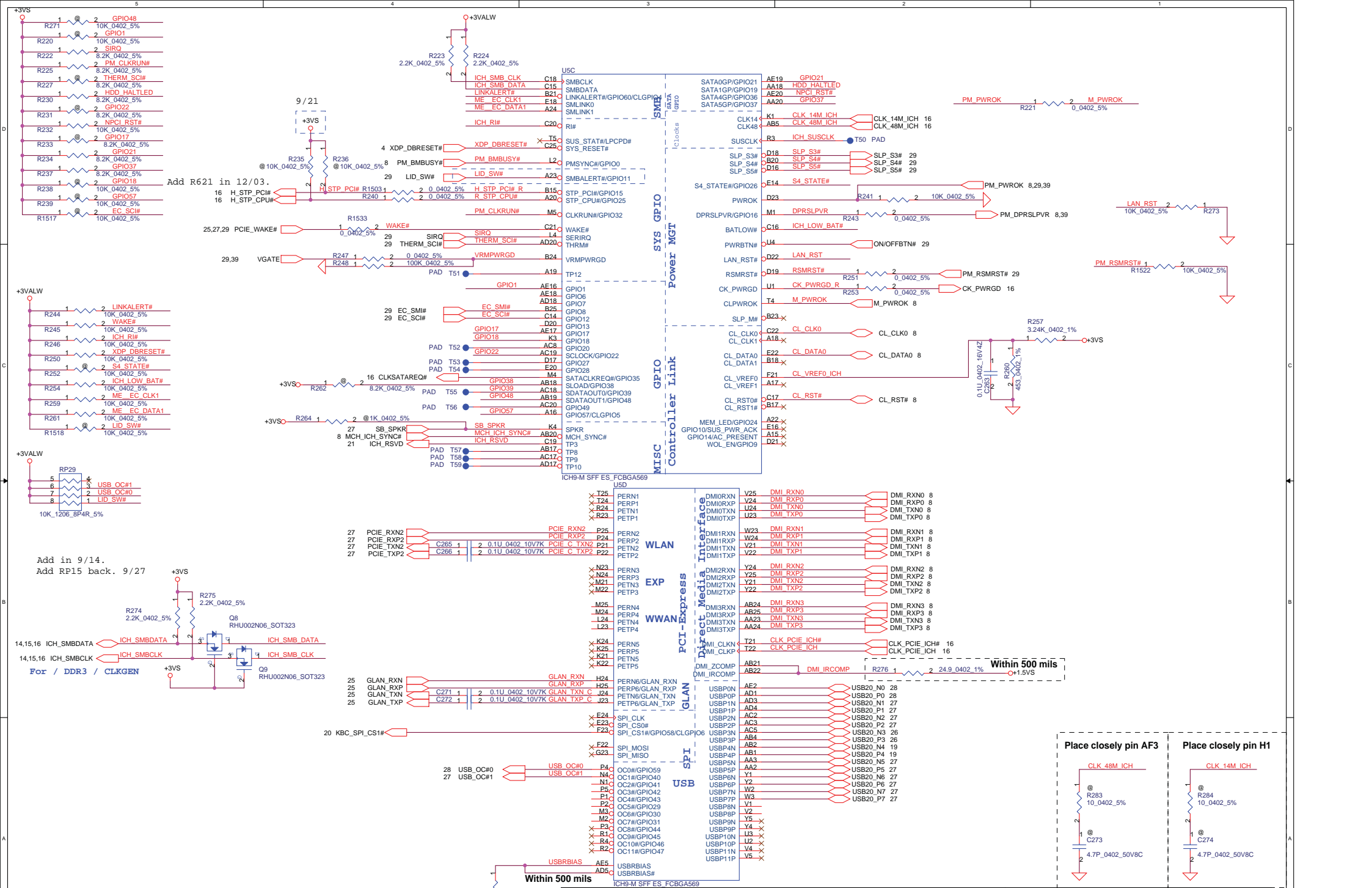
9/27
Del PU R203-R204 for H_DPRSTP# & H_DPSLP#.

Place Close to U8.

Within 500 mils



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Add R621 in 12/03.

Add in 9/14.
Add RP15 back. 9/27

Within 500 mils

Place closely pin AF3 Place closely pin H1

Security Classification	Issued Date	Deciphered Date	2010/12/31
	2009/04/01		

Compal Secret Data

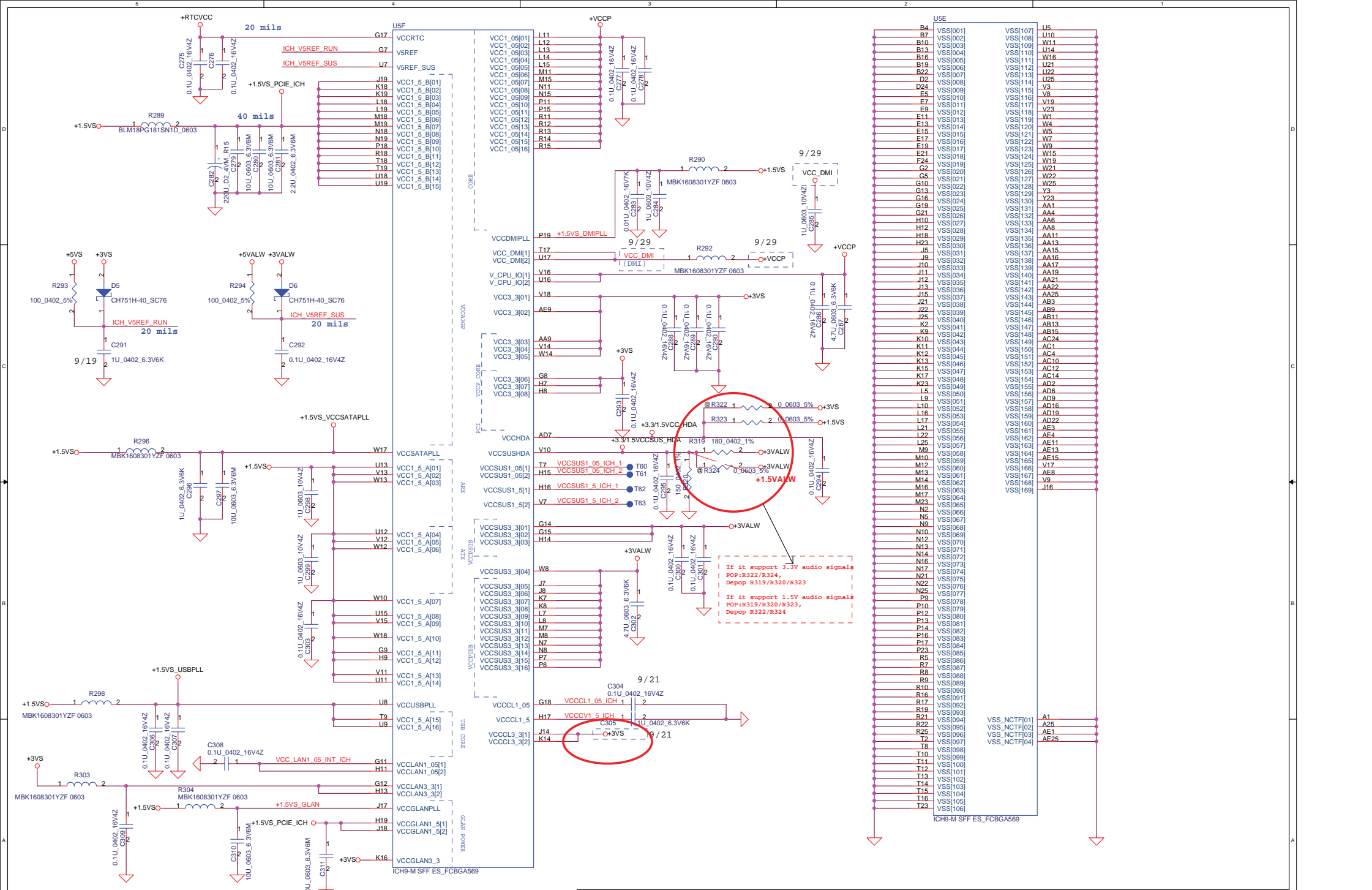
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Compal Electronics, Inc.

ICH9M(3/4)-DMI/USB/GPIO/PCIE

Document Number
LA-5541P

Date: Thursday, September 10, 2009 Sheet 22 of 43 Rev 1.0

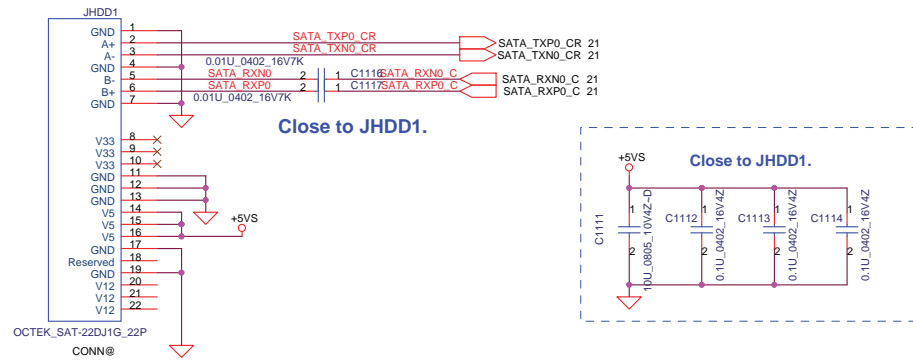


Security Classification	Compal Secret Data	
Issued Date	2009/04/01	Deciphered Date
		2010/12/31

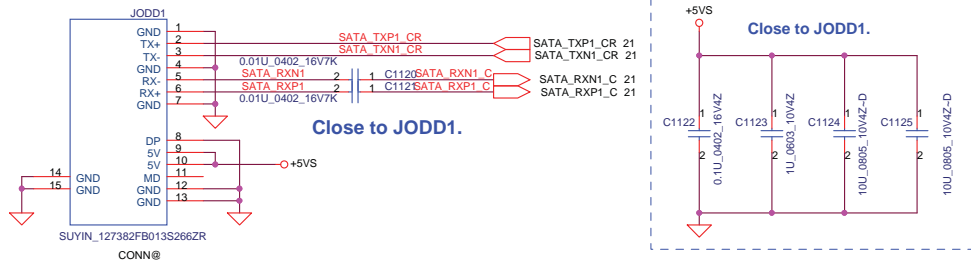
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Compal Electronics, Inc.	
ICH9M(4/4)-PWR/GND	
Document Number	LA-5541P
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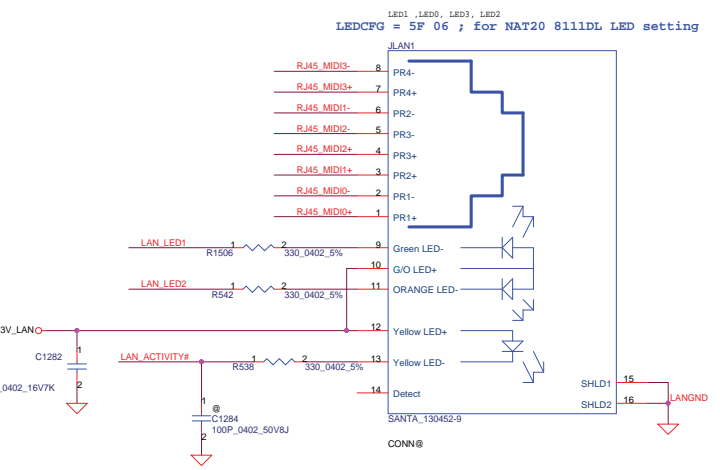
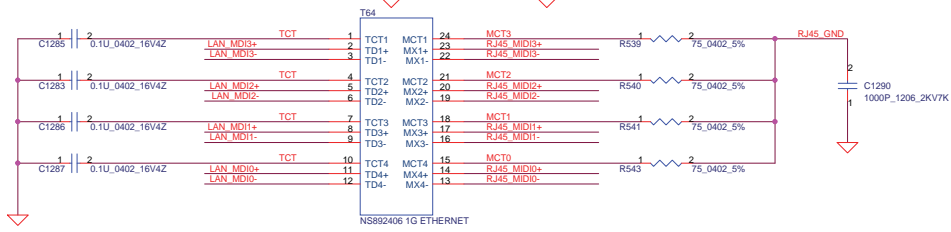
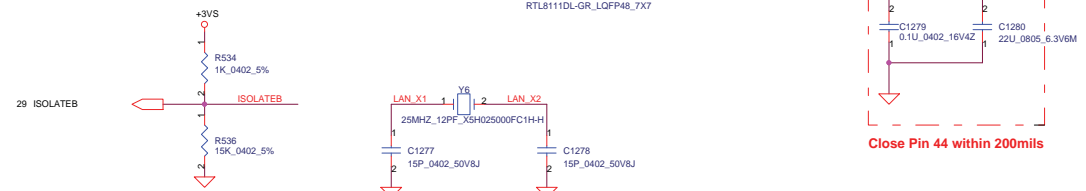
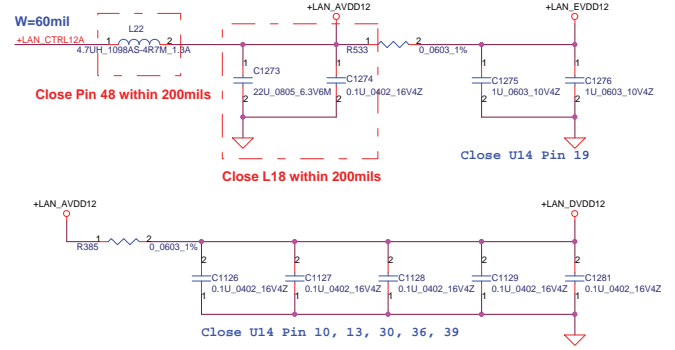
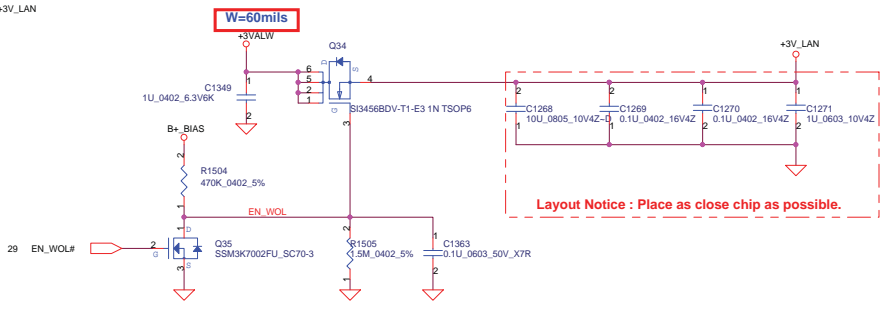
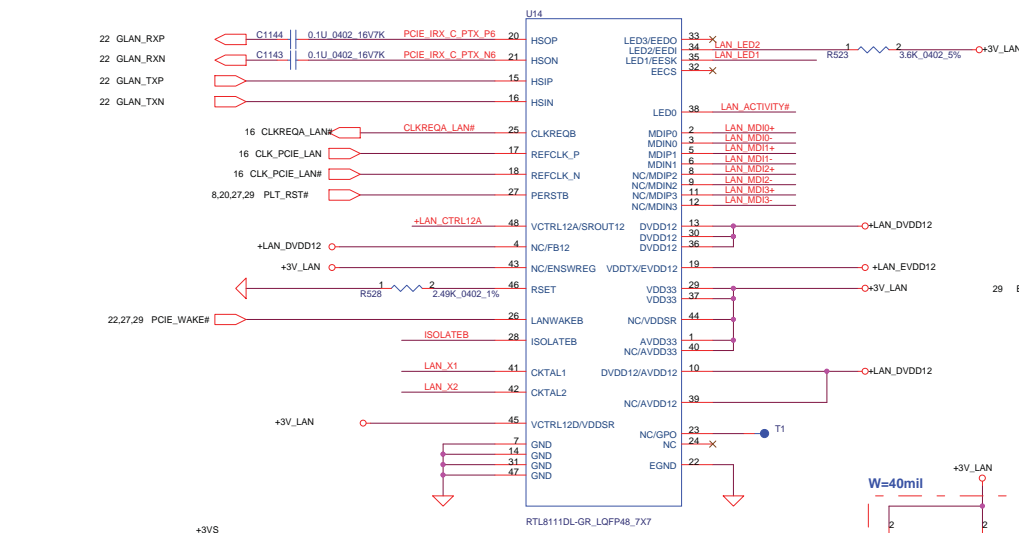
HDD Connector

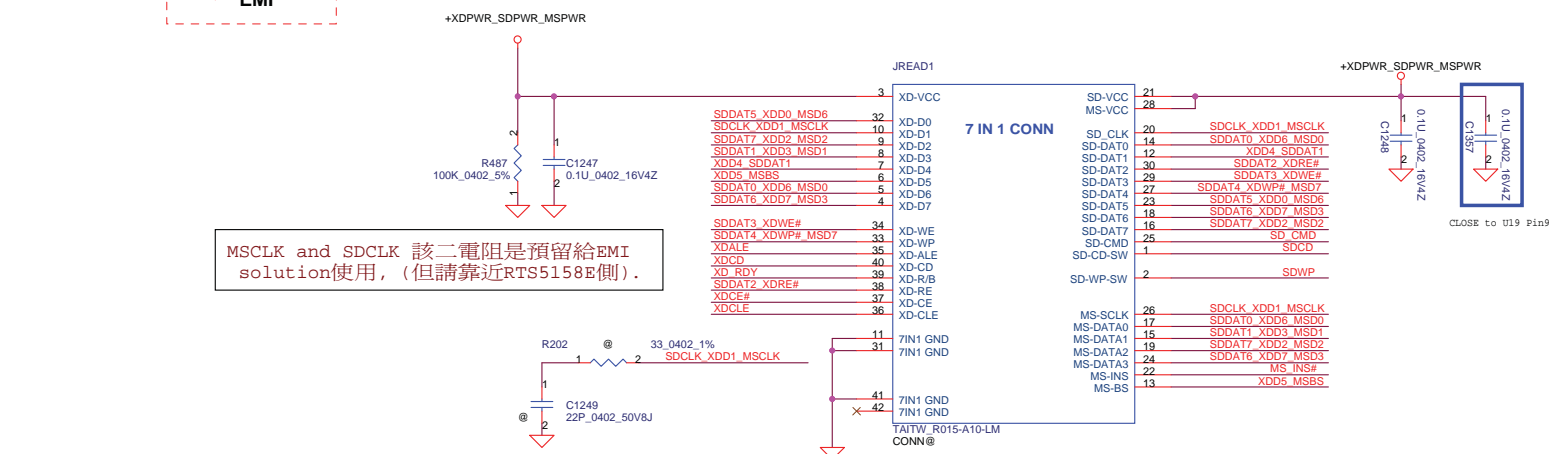
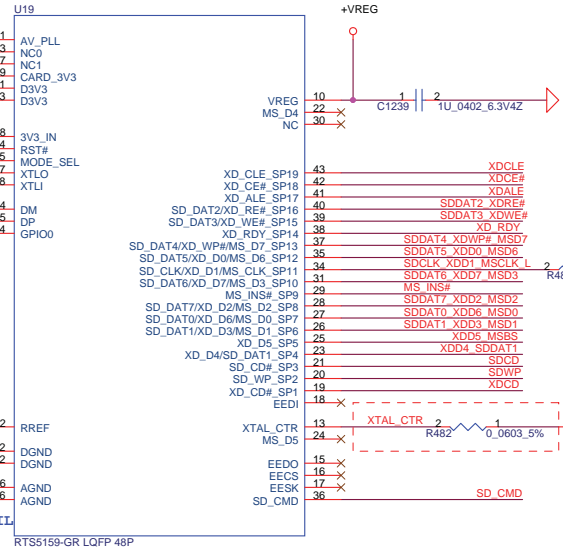
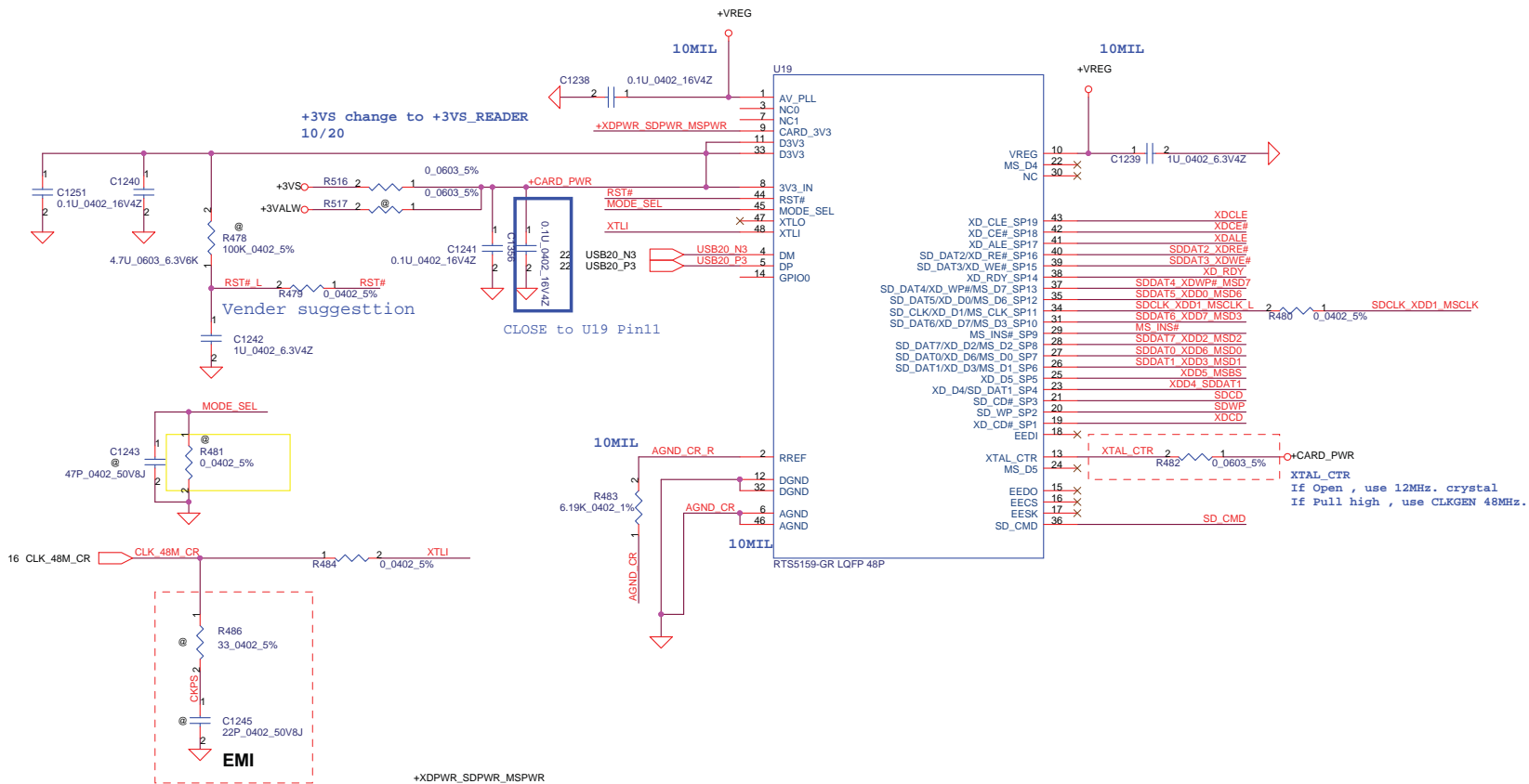


DVD-ROM Connector



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Issued Date	2009/04/01	Deciphered Date	2010/12/31	HDD/ODD Connector	
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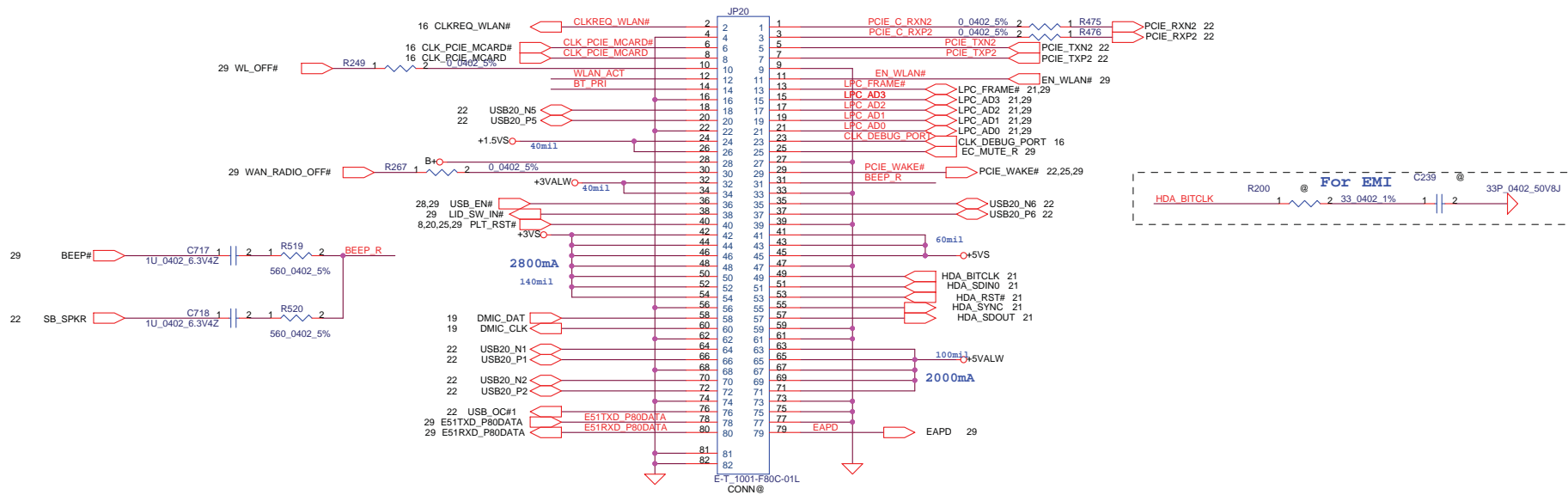


MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS15158B側).

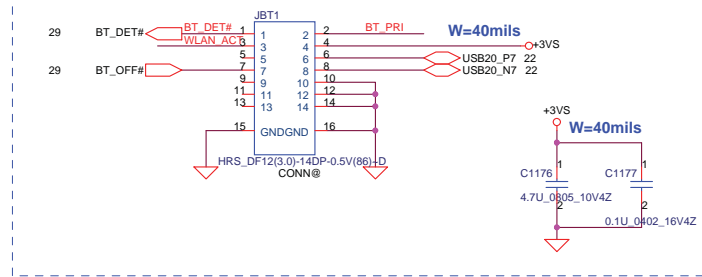
Security Classification	Compal Secret Data	
Issued Date	2009/04/01	Deciphered Date
		2010/12/31
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Compal Electronics, Inc.	
Title	Card Reader RTL5159-GR
Document Number	LA-5541P
Date	Thursday, September 10, 2009
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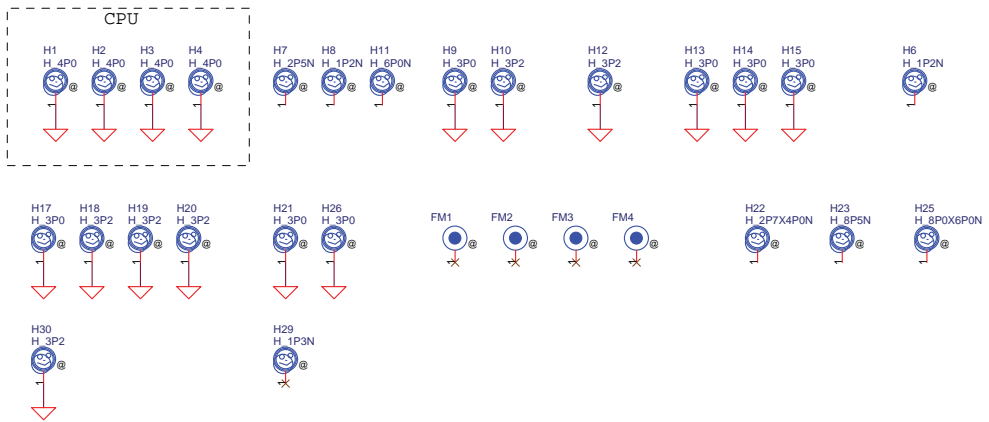
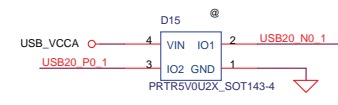
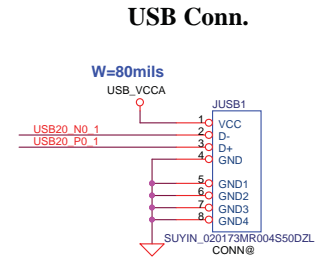
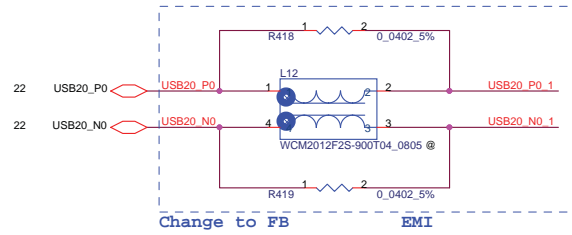
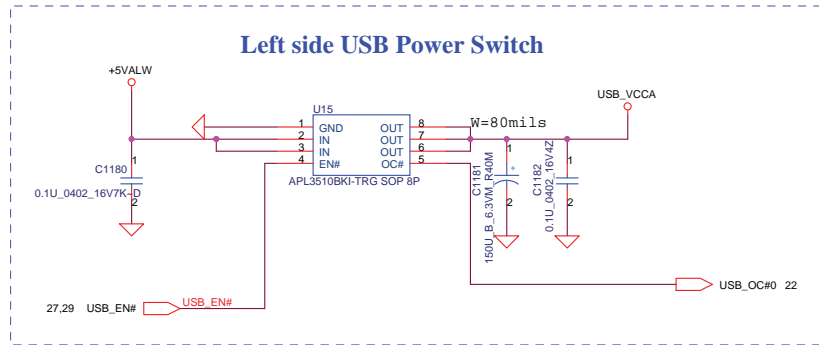
BTB Conn.



Blue Tooth Conn.

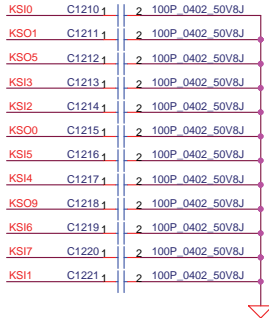
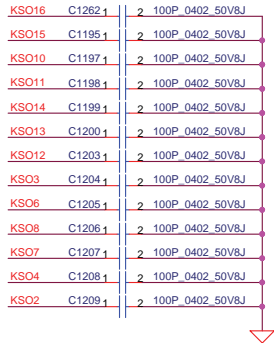


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Issued Date	2009/04/01	Deciphered Date	2010/12/31	Compal Electronics, Inc.	
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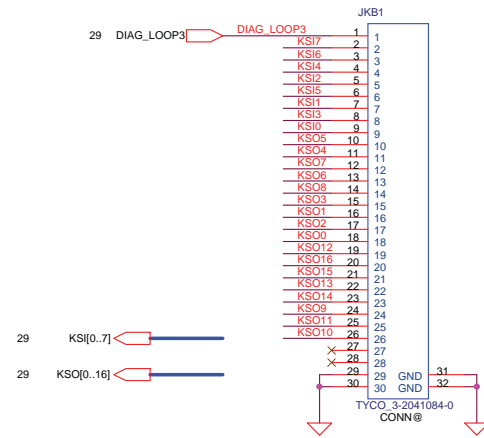


Security Classification	Compal Secret Data			Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	USB/Screws	
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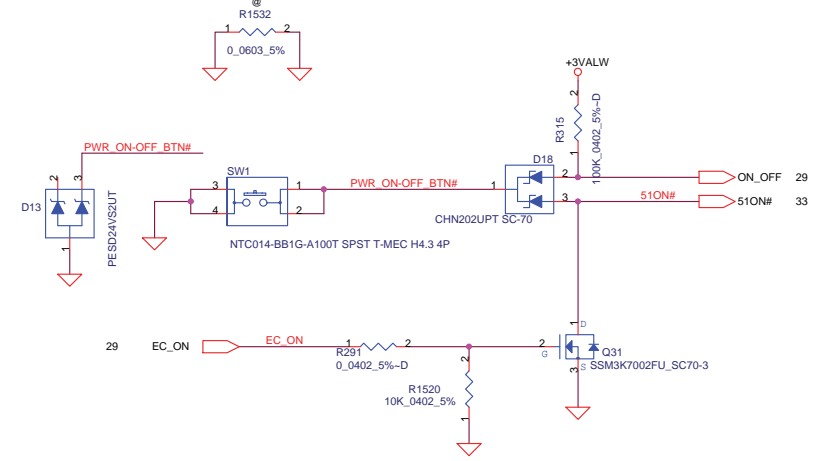
For EMI



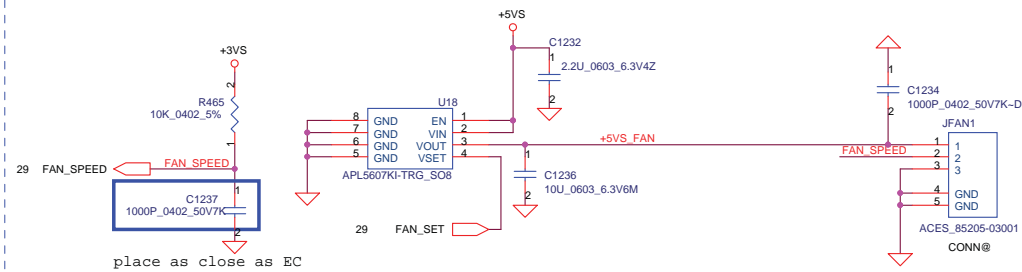
INT KBD Conn.



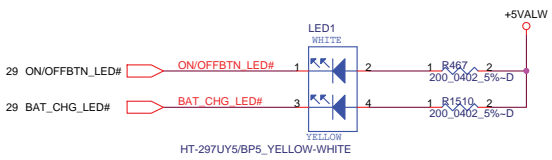
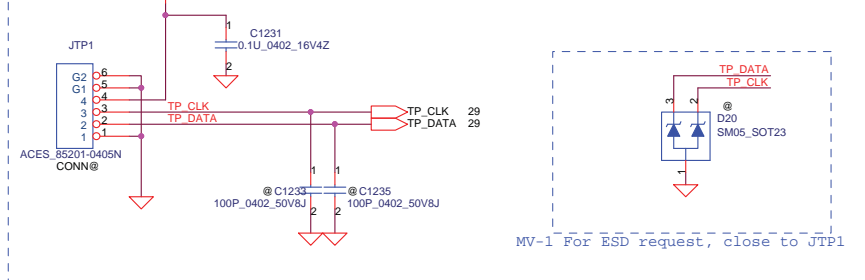
Power Button



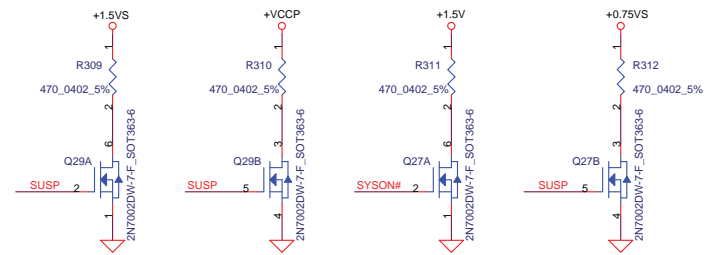
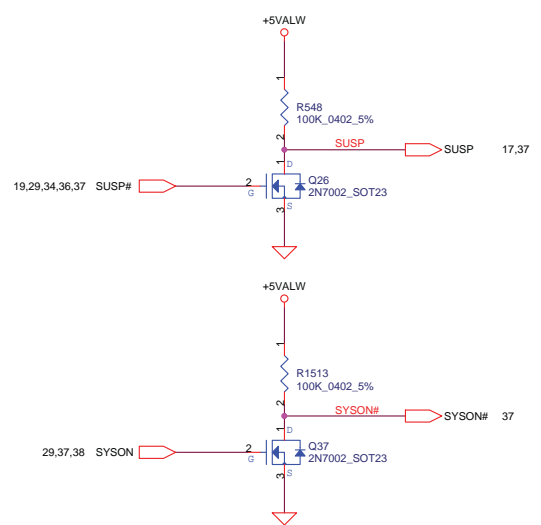
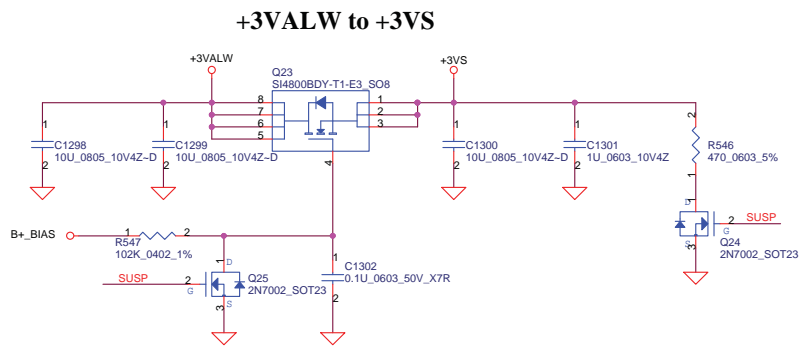
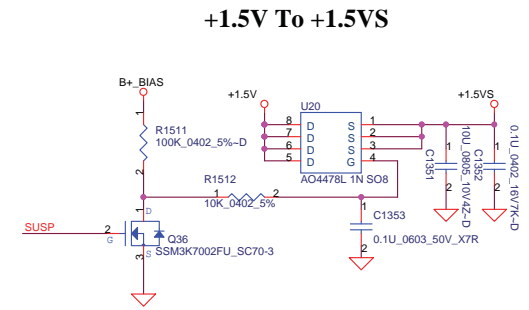
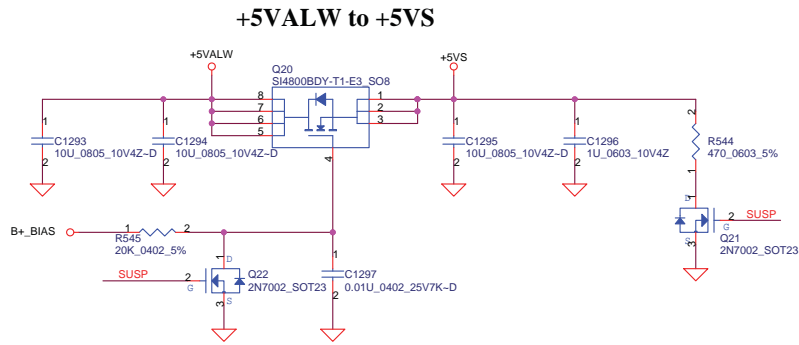
Fan Control Circuit



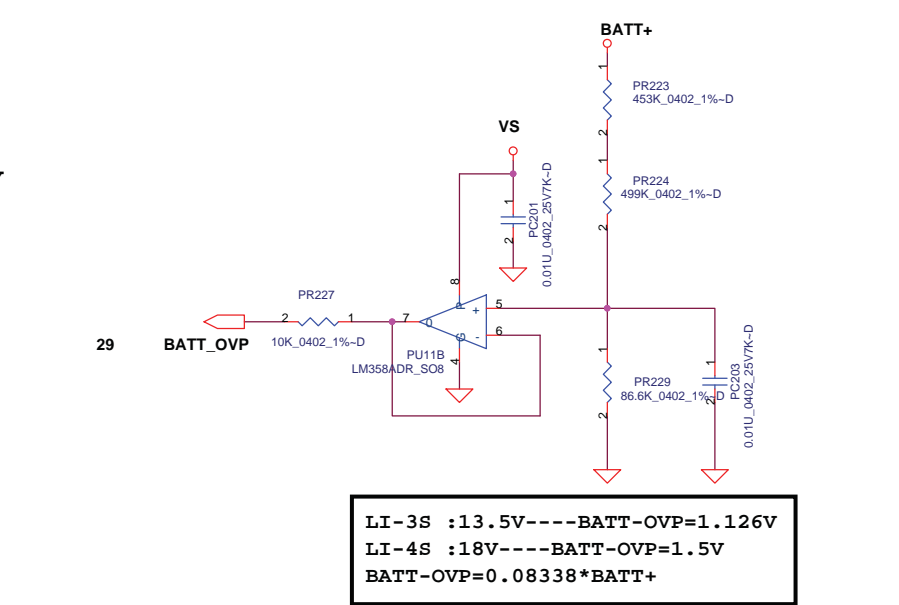
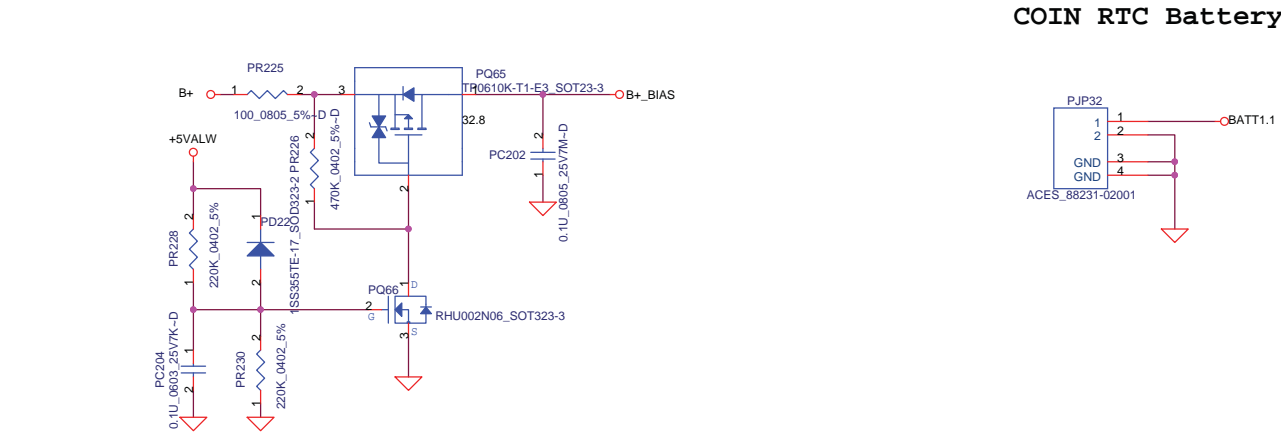
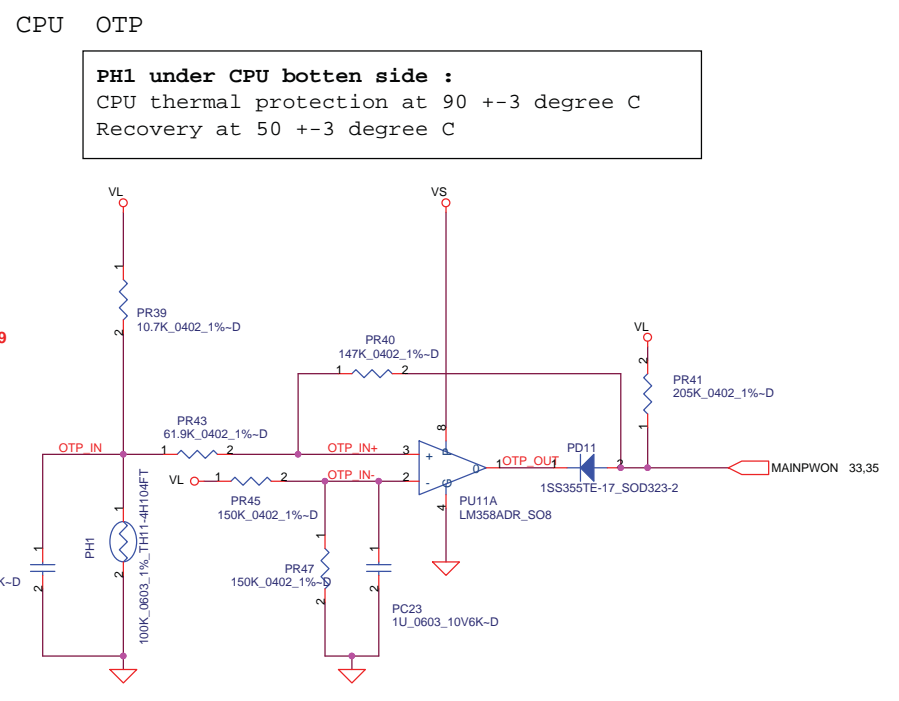
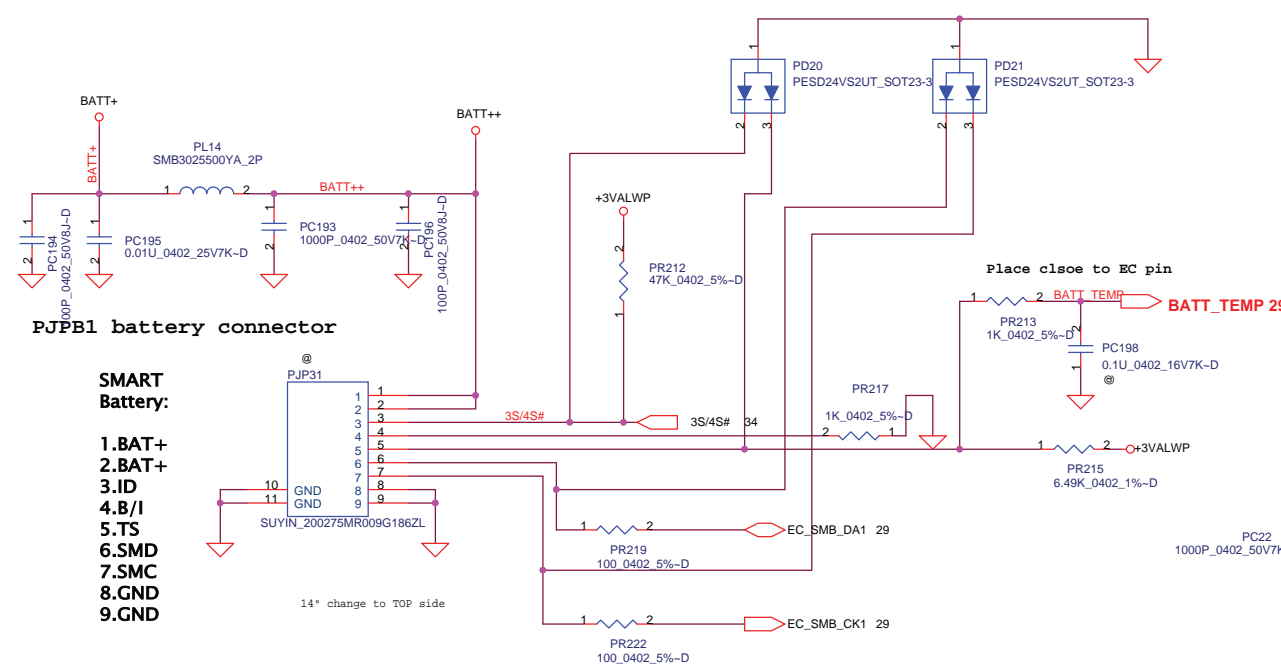
Touch Pad Connector



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Issued Date	2009/04/01	Deciphered Date	2010/12/31	KB/BTN/FAN/TP	
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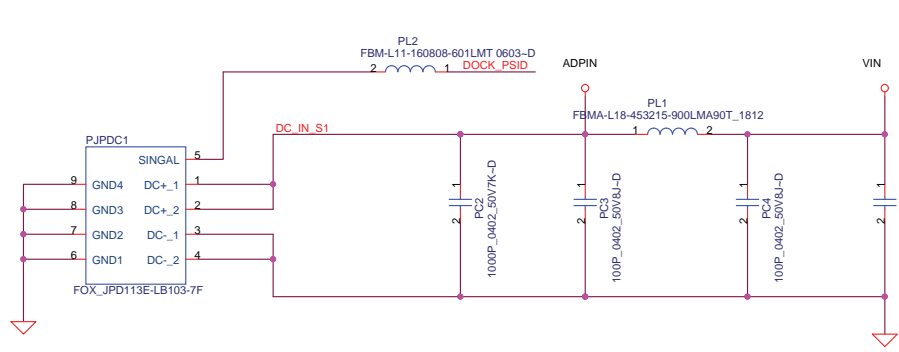


Security Classification	Compal Secret Data			Title	
Issued Date	2009/04/01	Deciphered Date	2010/12/31	DC/DC Interface	
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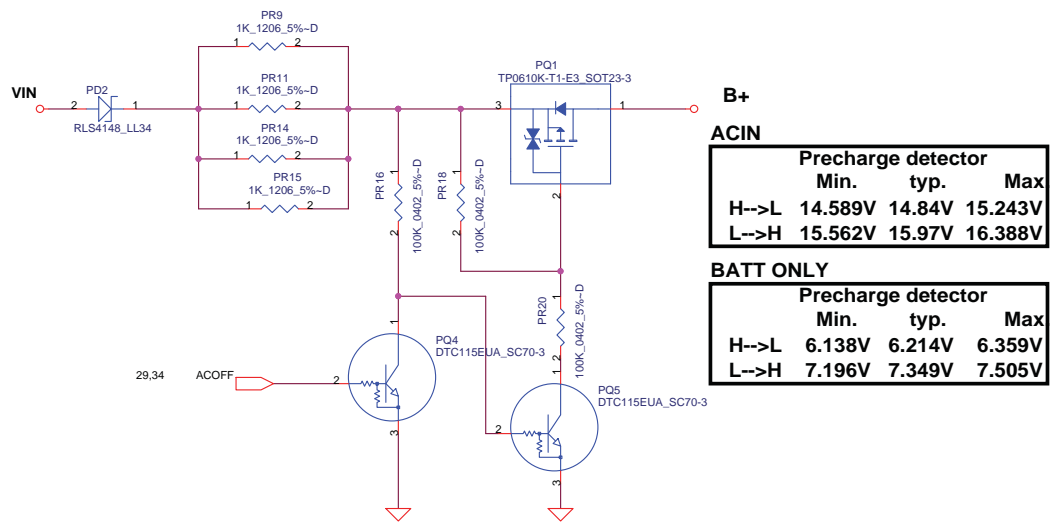
LI-3S :13.5V----BATT-OVP=1.126V
 LI-4S :18V----BATT-OVP=1.5V
 BATT-OVP=0.08338*BATT+

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Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

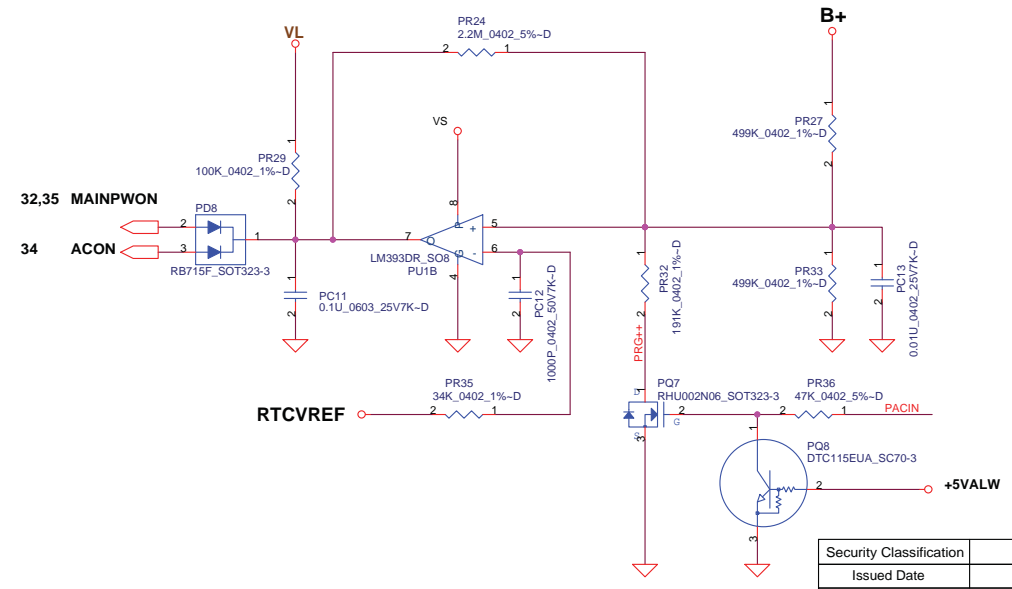
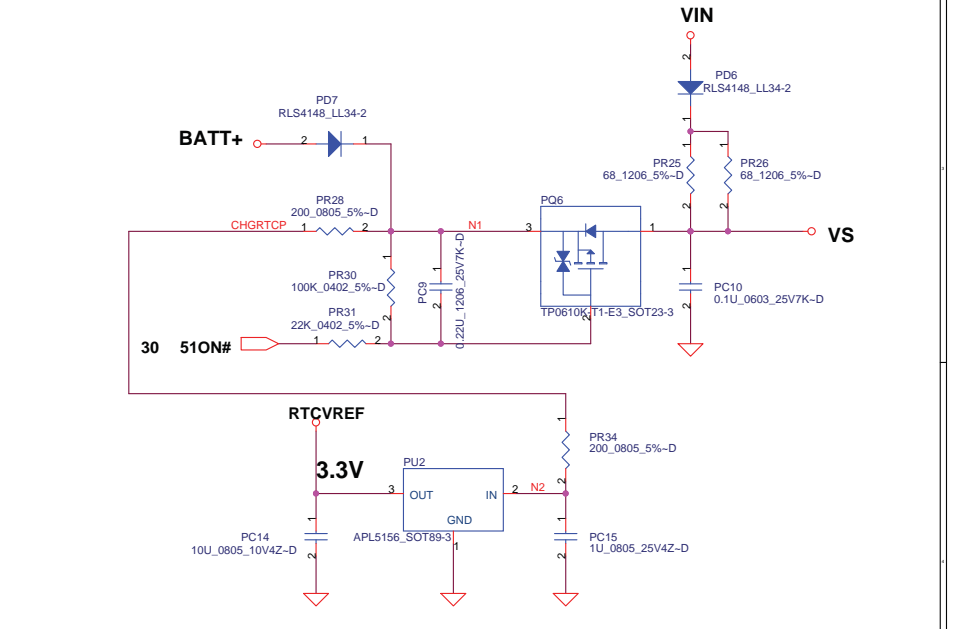
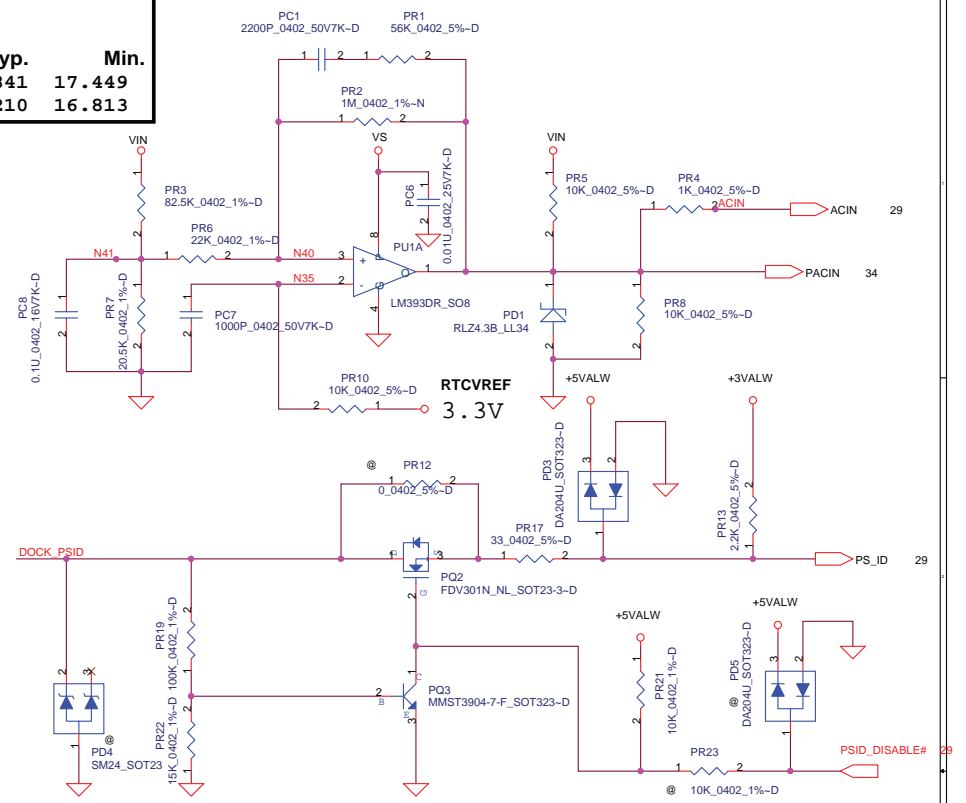


ACIN Precharge detector

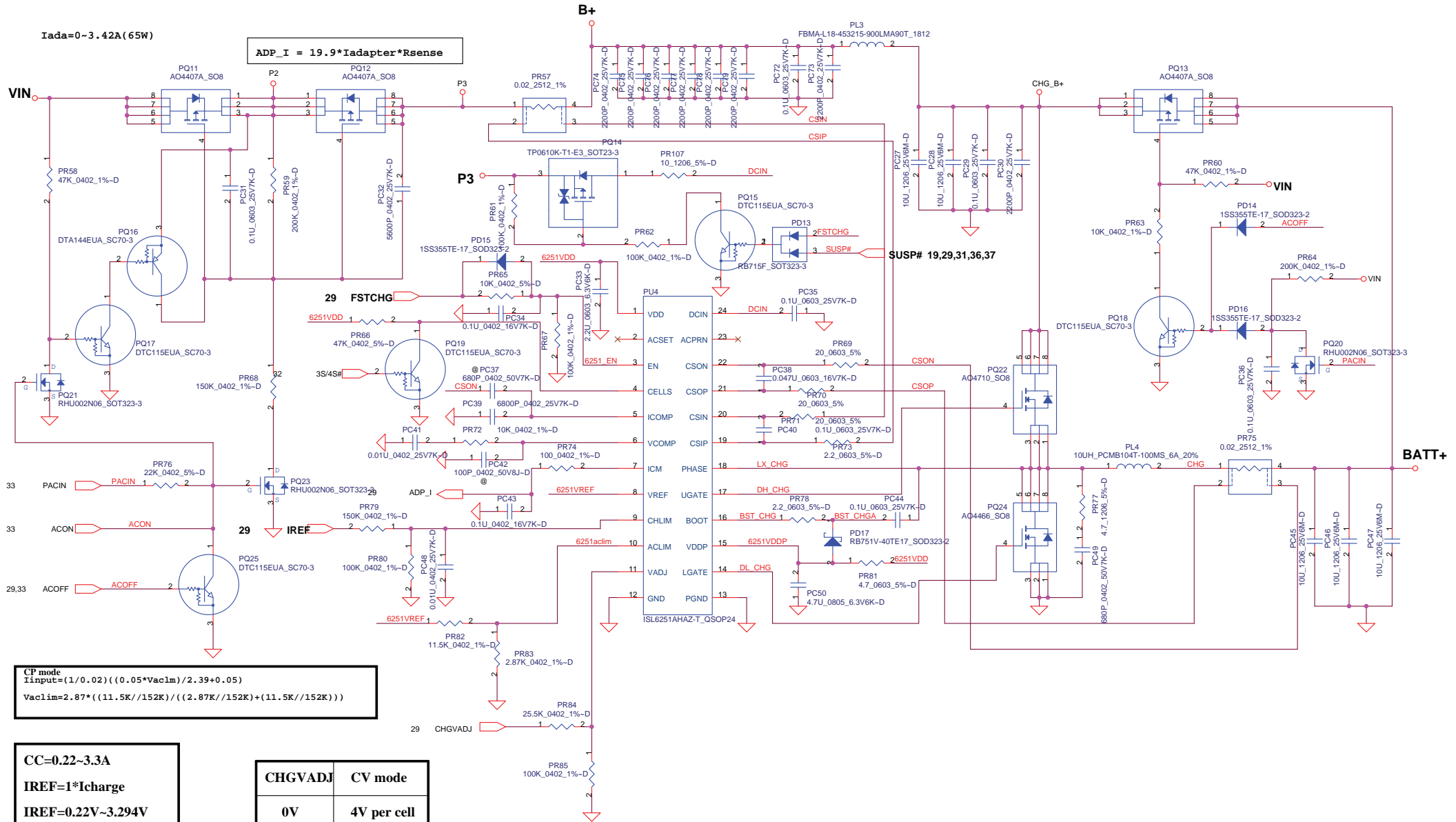
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY Precharge detector

	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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Iada=0~3.42A(65W)

$$ADP_I = 19.9 * I_{adapter} * R_{sense}$$

CP mode
 $I_{input} = (1/0.02) * ((0.05 * V_{ac1m}) / 2.39 + 0.05)$
 $V_{ac1m} = 2.87 * ((11.5K // 152K) / ((2.87K // 152K) + (11.5K // 152K)))$

CC=0.22~3.3A
 IREF=1*Icharge
 IREF=0.22V~3.294V

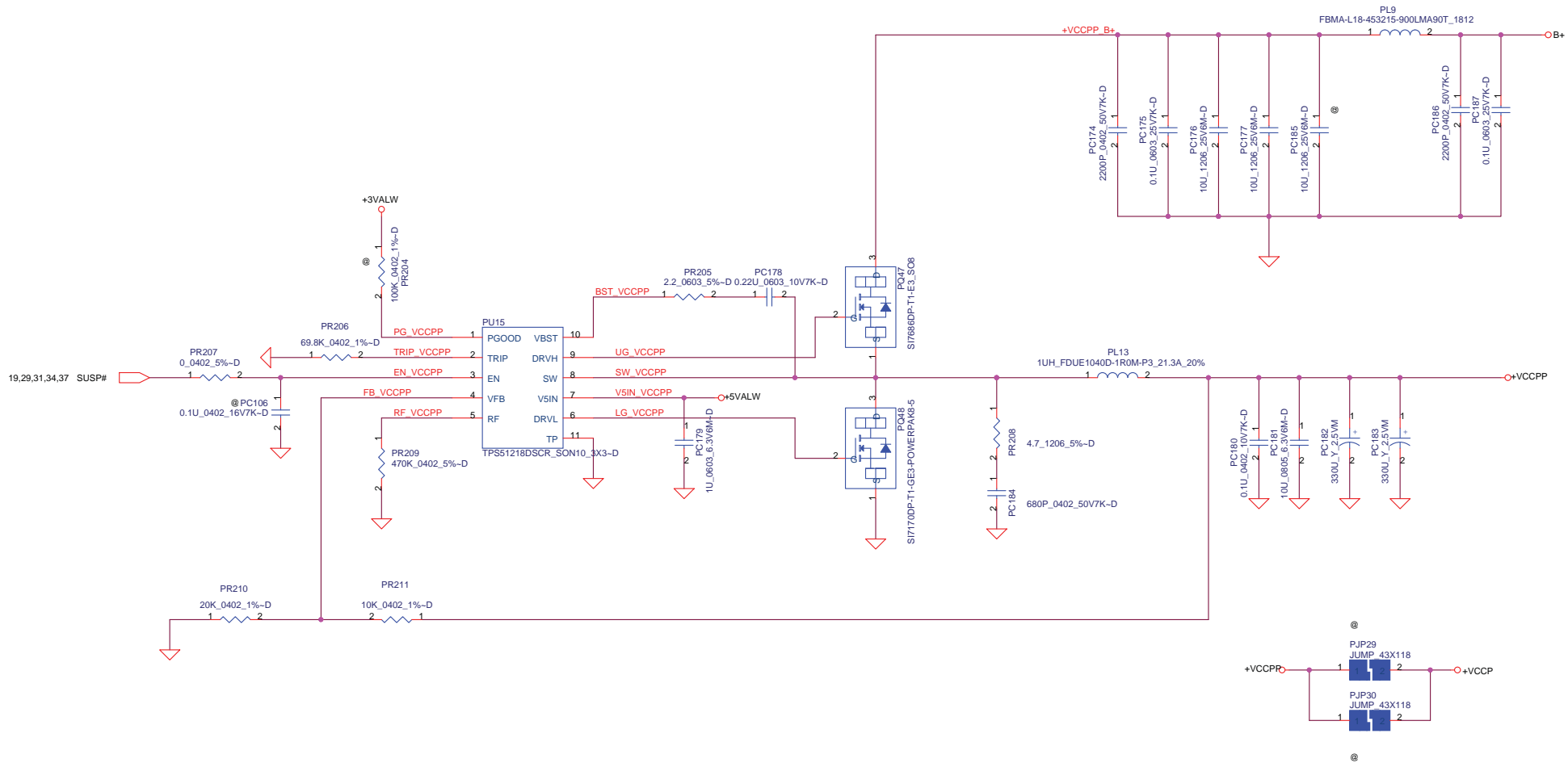
CHGVADJ	CV mode
0V	4V per cell
1.882V	4.2V per cell
3.294V	4.45V per cell

+VCCPP

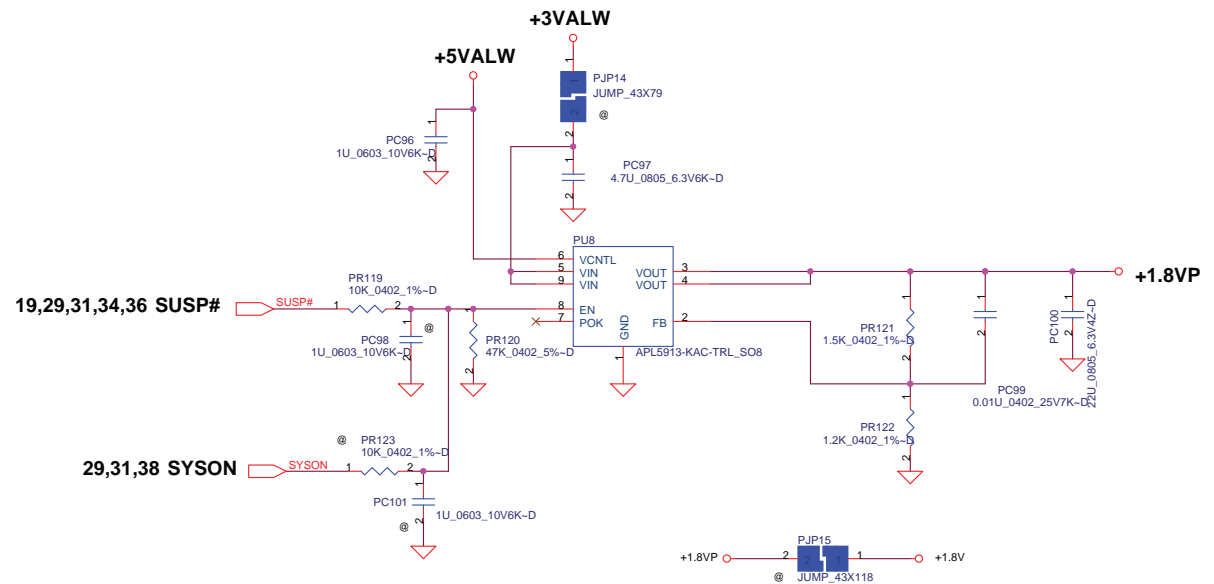
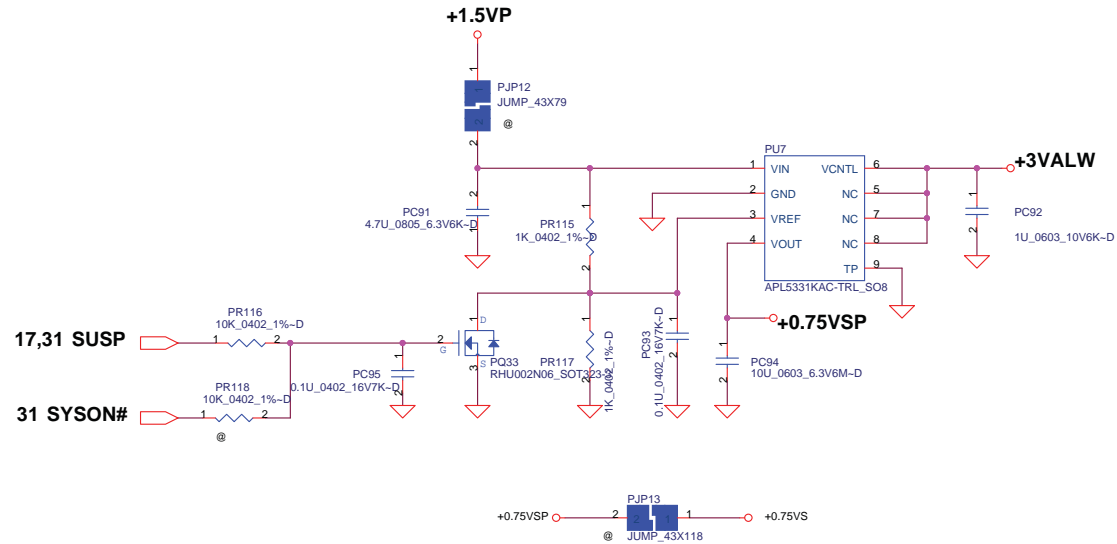
Thermal Design current=11.5A

OCP min=19.5A

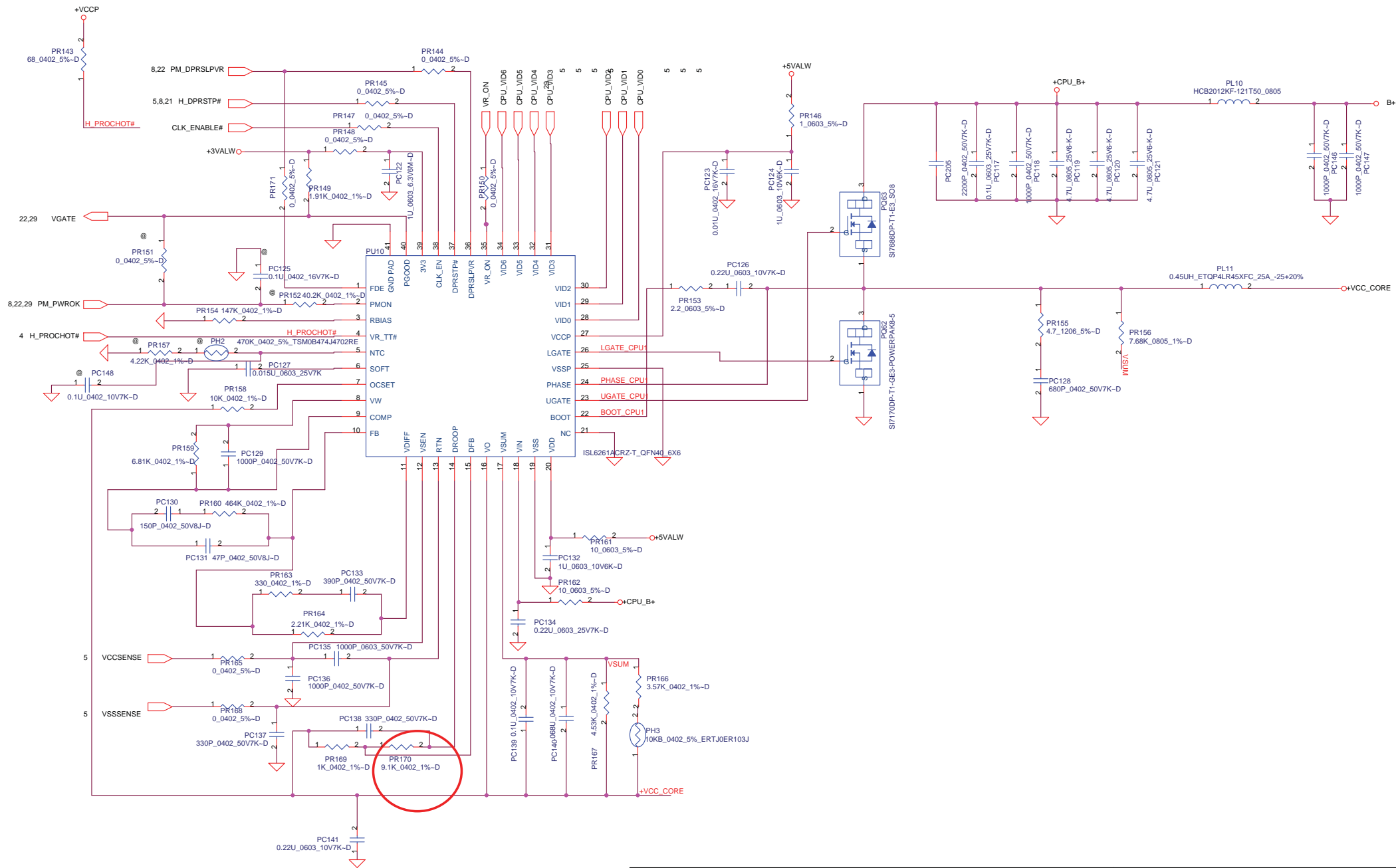
Fsw=290KHZ



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Issued Date	2008/2/5	Deciphered Date	2010/12/31	Title
				+1.8VP / +0.75VP
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Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/23	Deciphered Date	2010/12/31	CPU_CORE	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	CPU_CORE	09' 09/09	Compal_Will	Modify CPU load line	PR170 change 6.65K_1%_0402 to 9.1K_1%_0402	0.5

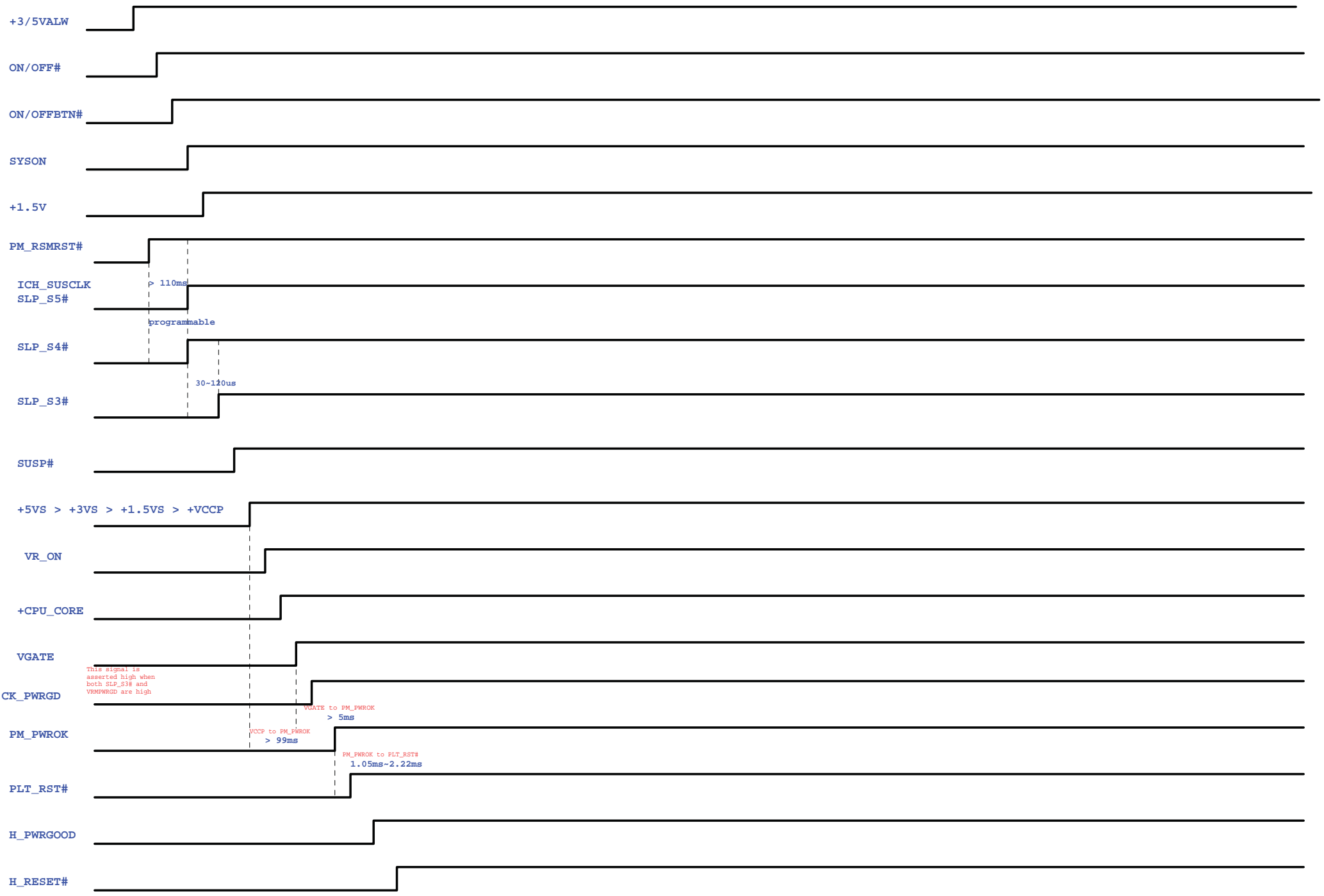
Compal Electronics, Inc.	
Title PWR-PIR	Revision Number
Part Number LA-5541P	Rev 1.0
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21, 23		2009/06/05	Compal	HDMI NO SOUND	ADD R319, R320, R323, R321 DEL R322, R324, R92	0.2
2	29, 30		2009/06/05	Compal	Battery LED can't work	ADD NET BAT_CHG_LED#	0.2
3	19		2009/06/05	Compal		Change JLVDS connect	0.2
4	24		2009/06/05	Compal		Change JODD1 connect	0.2
5	17		2009/06/05	Compal		Change Level shift IC to ASMEDIA	0.2
6	16		2009/06/18	Compal		reserve R1535 to using LOW POWER CLK GEN RTM890-397	0.3
7	26		2009/06/24	Compal		DEL Y5 C1244, C1246	0.3
8	19		2009/07/08	Compal		reserve Q39,Q40,R1536, R1537, C1359, C1360, C1361, C1362	0.3
9	30		2009/07/08	Compal		Del C313 D14	0.3
10	29,30		2009/07/08	Compal		Add EAPD trace	0.3
11	25		2009/07/23	Compal		Add C1363	1.0
12	30		2009/07/23	Compal		Change Keyboard footprint	1.0
13							
14							
15							
16							
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Issued Date	2009/04/01	Deciphered Date	2010/12/31	EE PIR-1	
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This signal is asserted high when both SLP_S3# and VPM_PWRGD are high

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