

# Compal Confidential

## HBL51 Schematics Document

Intel Yonah Processor with 945GM/940GML + DDRII + ICH7M

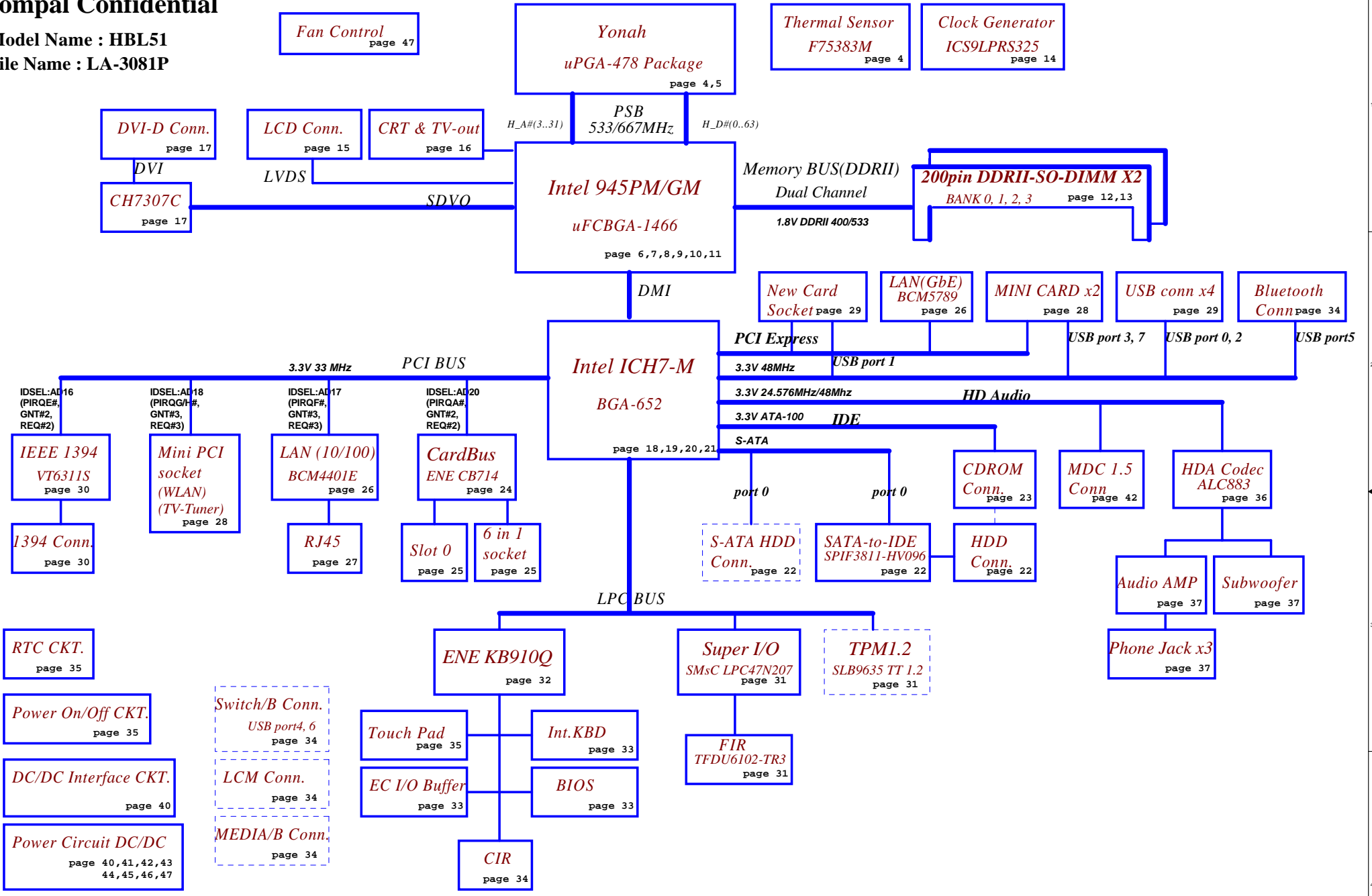
2006-10-04

REV: 5.0

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Model Name : HBL51  
File Name : LA-3081P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

## EC SM Bus2 address

## ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

## SKU ID Table

SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

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<6> H\_A# [3..31] H\_A# [3..31]

<6> H\_REQ# [0..4] H\_REQ# [0..4]

<6> H\_RS# [0..2] H\_RS# [0..2]

<6> H\_ADSTB#0 ADSTB0#  
<6> H\_ADSTB#1 ADSTB1#

<14> CLK\_CPU\_BCLK BCLK0  
<14> CLK\_CPU\_BCLK# BCLK1

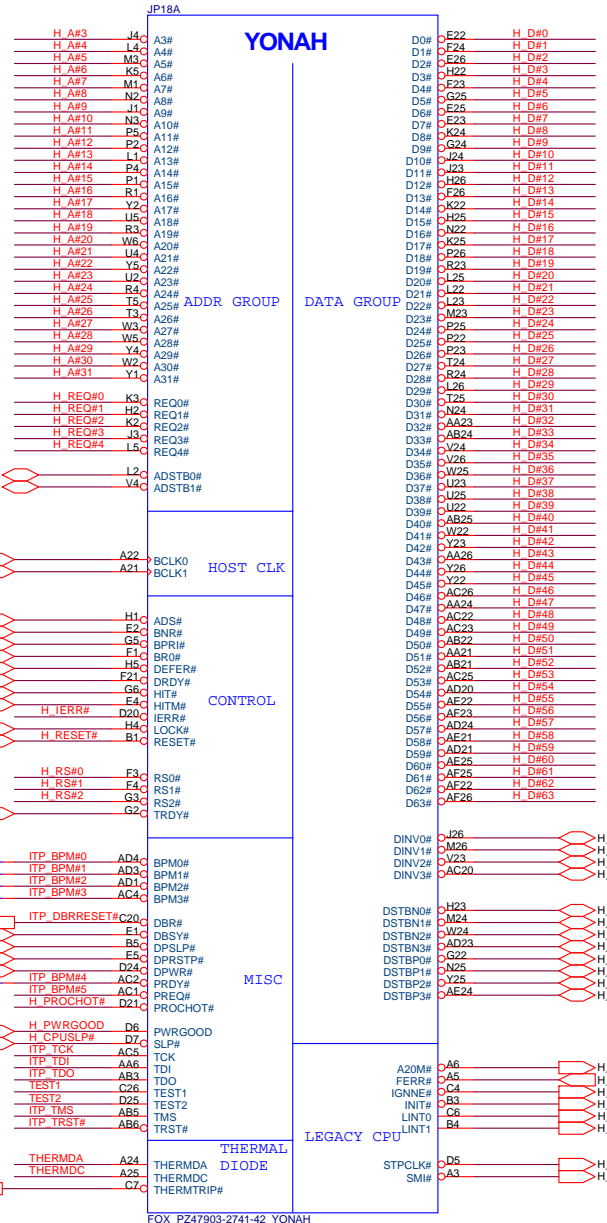
<6> H\_ADS# ADS#  
<6> H\_BNR# BNR#  
<6> H\_BRPR# BRPR#  
<6> H\_BR0# BR0#  
<6> H\_DEFER# DEFER#  
<6> H\_DRDY# DRDY#  
<6> H\_HIT# HIT#  
<6> H\_HITM# HITM#  
<6> H\_IERR# IERR#  
<6> H\_LOCK# LOCK#  
<6> H\_RESET# RESET#

H\_RS#0 RS0#  
H\_RS#1 RS1#  
H\_RS#2 RS2#  
<6> H\_TRDY# TRDY#

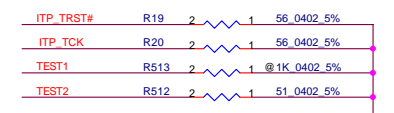
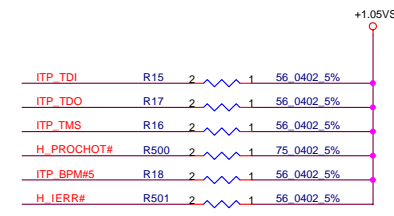
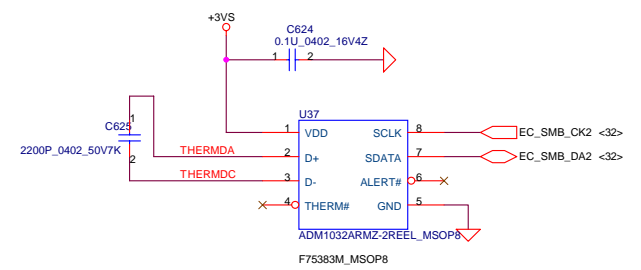
T5 PAD ITP\_BPM#0 AD4 BPM0#  
T3 PAD ITP\_BPM#1 AD3 BPM1#  
T1 PAD ITP\_BPM#2 AD2 BPM2#  
T4 PAD ITP\_BPM#3 AD1 BPM3#  
<20> ITP\_DBRRESET# C20 DBR#  
<6> H\_DBSY# E1 DBSY#  
<19> H\_DPSLP# E5 DPSLP#  
<19,47> H\_DPRSTP# E5 DPRSTP#  
<6> H\_DPWR# D24 DPWR#  
T2 PAD ITP\_BPM#4 AC2 PRDY#  
ITP\_BPM#5 AC1 PREQ#  
H\_PROCHOT# D21 PROCHOT#

<19> H\_PWRGOOD D6 PWRGOOD  
<6> H\_CPUSLP# D7 SLP#  
ITP\_TCK AC5 TCK  
ITP\_TDI AA6 TDI  
ITP\_TDO AB3 TDO  
TEST1 C26 TEST1  
TEST2 D25 TEST2  
ITP\_TMS AB5 TMS  
ITP\_TRST# AB6 TRST#

<6,19> H\_THERMTRIP# THERMDA A24 THERMDA  
THERMDC A25 THERMDC  
THERMTRIP# C7 THERMTRIP#



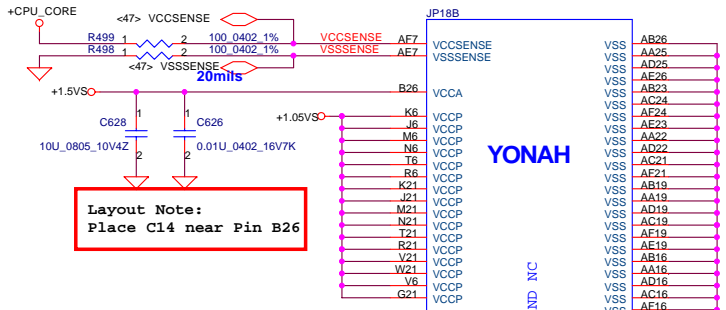
H\_D# [0..63] H\_D# [0..63]



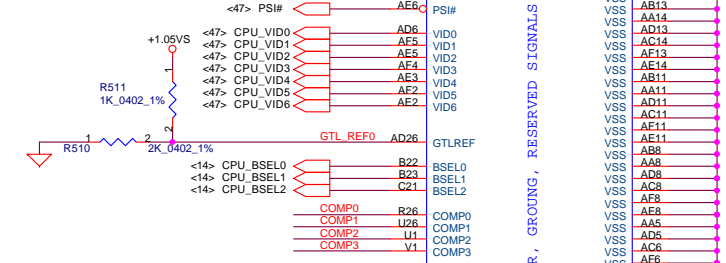
**Layout Note:**  
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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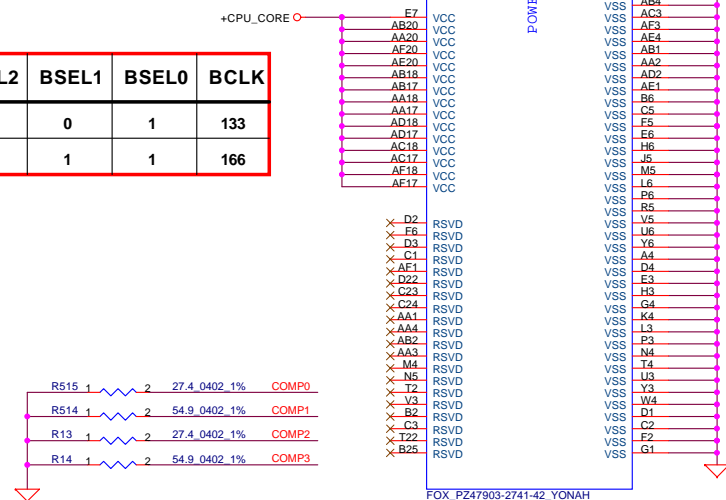
**Layout Note:**  
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.



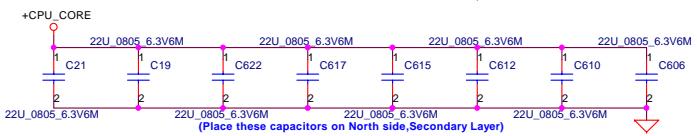
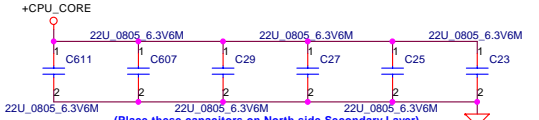
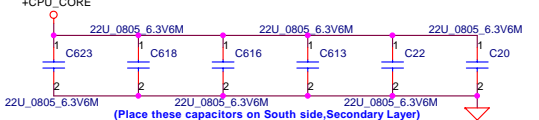
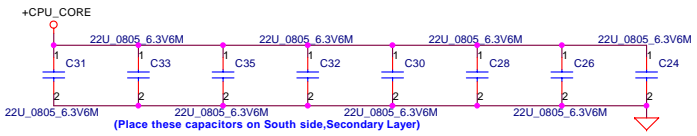
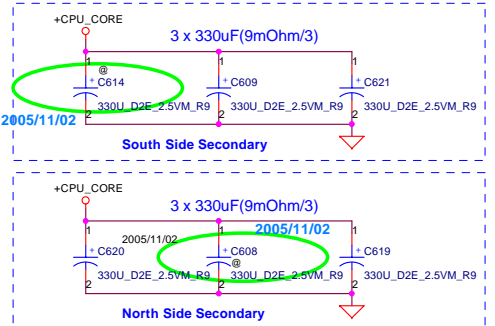
**Layout Note:**  
Place C14 near Pin B26



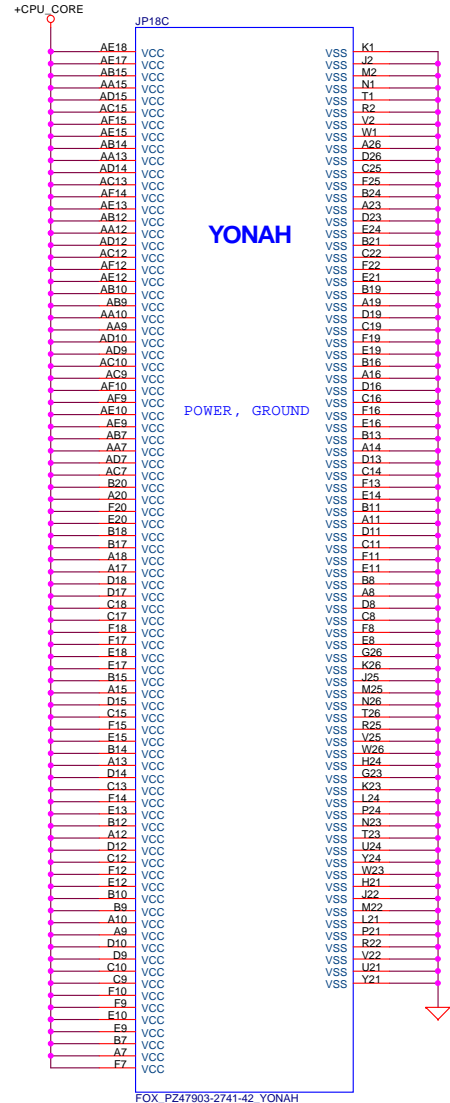
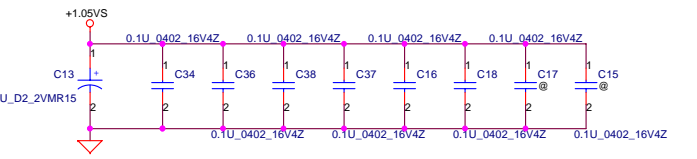
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166



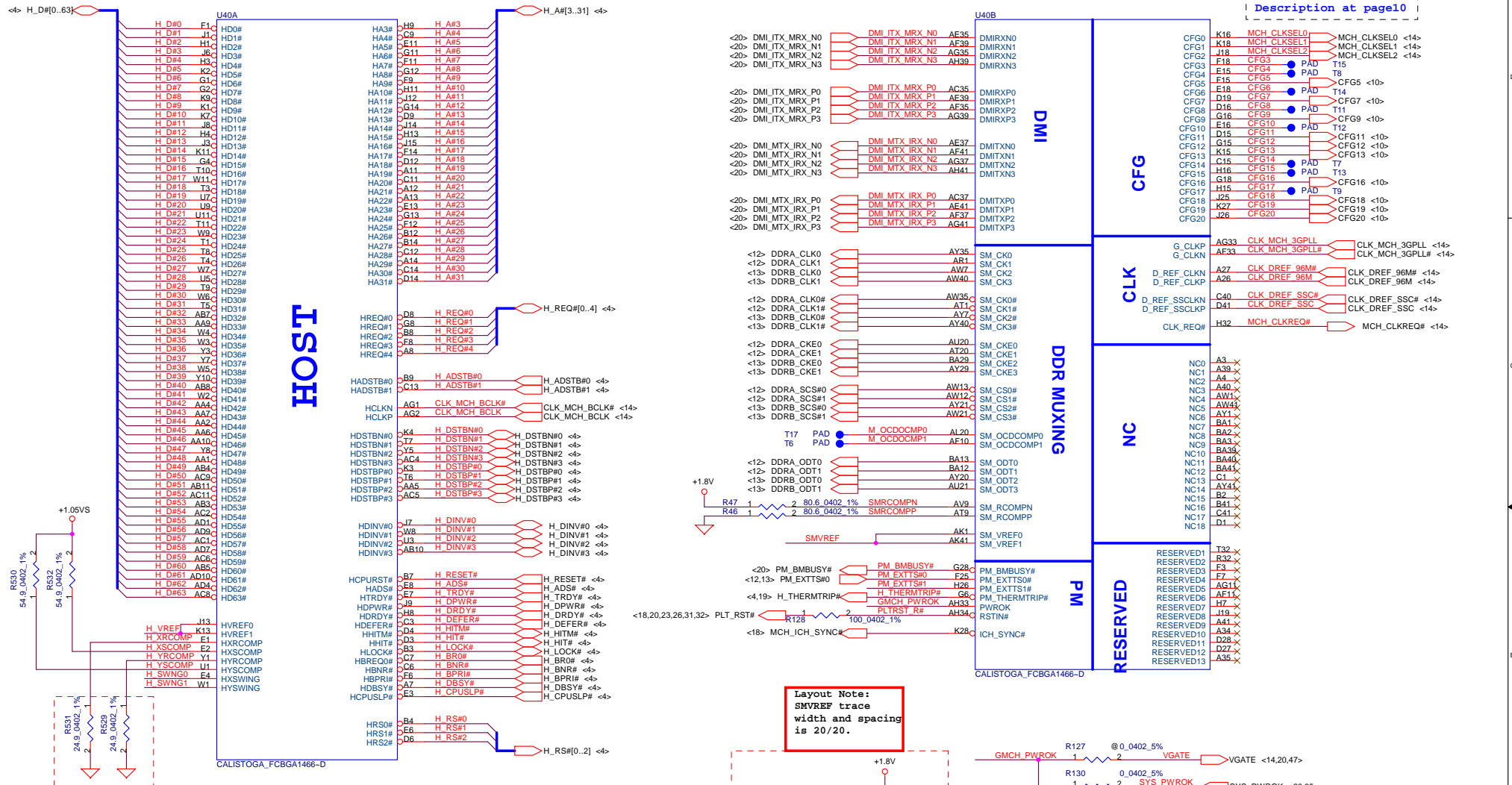
**TRACE CLOSELY CPU < 0.5'**  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)  
COMP1, COMP3 layout : Space 25mils (55ohms)



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32



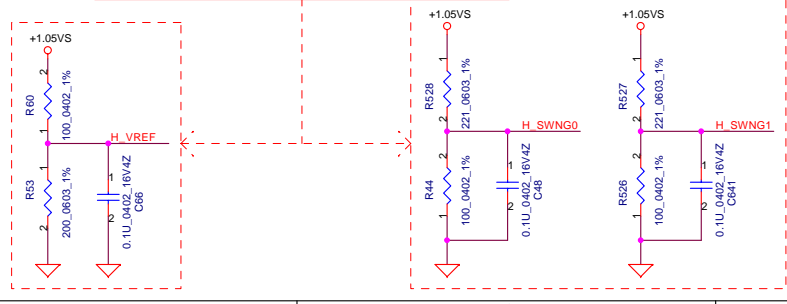
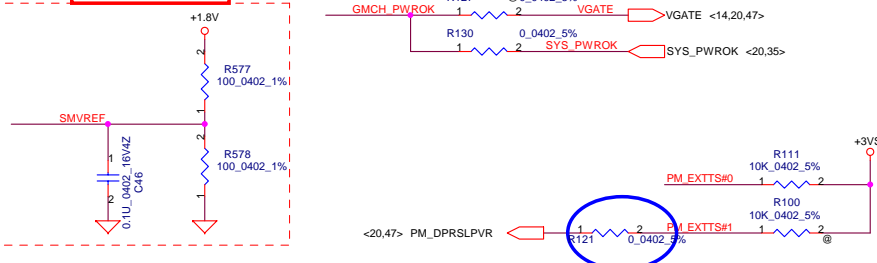
945GM(A-1)(QJ15)[ES2]: SA000005970  
 945GM(A-2)(QK44)[ES3]: SA000005980  
 945PM(A-2)(QK46)[ES3]: SA00000UV10



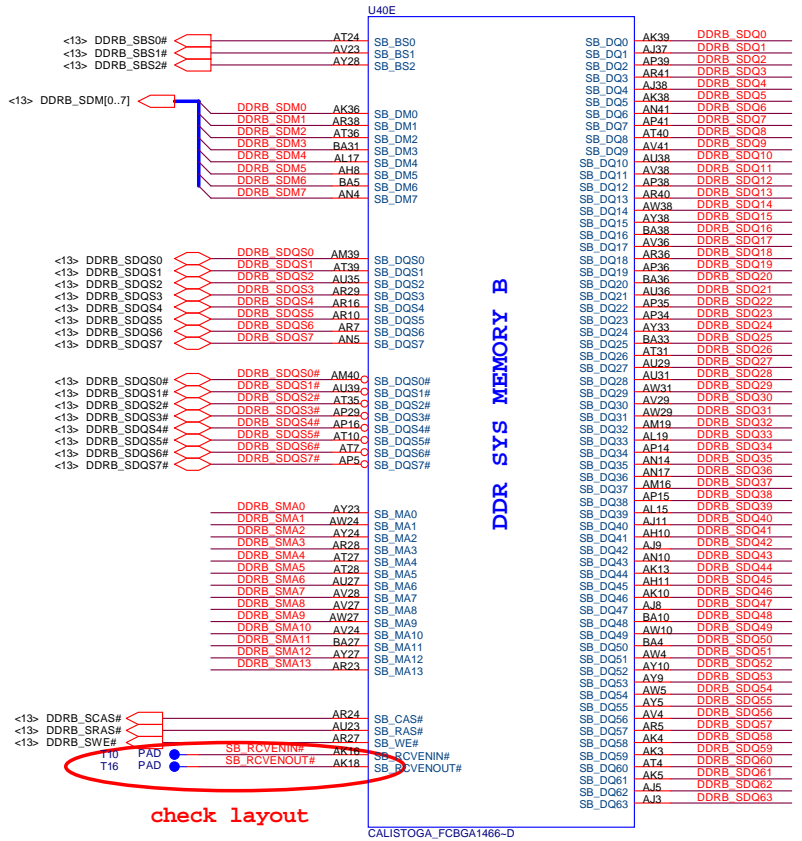
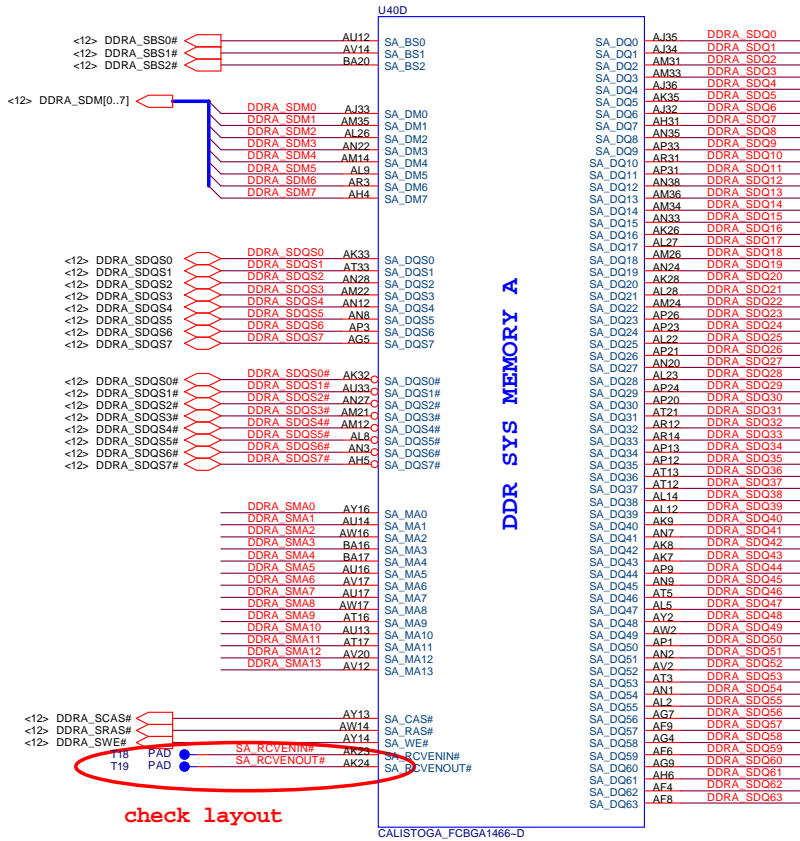
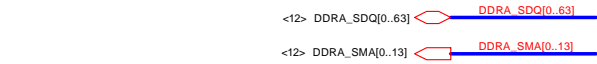
HOST

**Layout Note:**  
 SMVREF trace width and spacing is 20/20.

**Layout Note:**  
 H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.



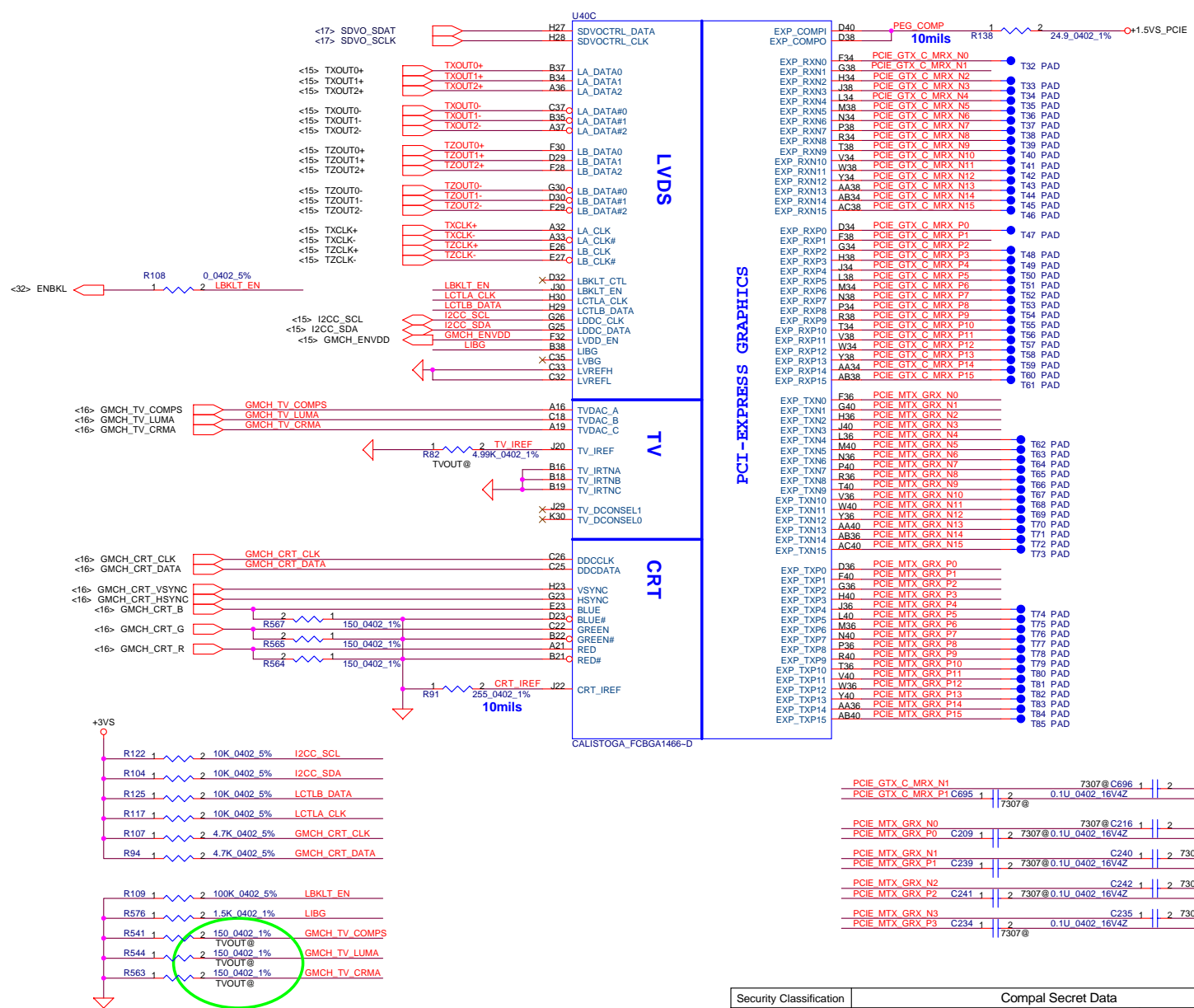
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PCIE GTX C MRX N1	7307@C696	1	2	0.1U 0402 16V4Z	SDVO_INT# <17>
PCIE GTX C MRX P1	C695	1	2	0.1U 0402 16V4Z	SDVO_INT <17>
PCIE MTX GRX N0	7307@C216	1	2	0.1U 0402 16V4Z	SDVOB_R# <17>
PCIE MTX GRX P0	C209	1	2	7307@0.1U 0402 16V4Z	SDVOB_R <17>
PCIE MTX GRX N1	C240	1	2	7307@0.1U 0402 16V4Z	SDVOB_G# <17>
PCIE MTX GRX P1	C239	1	2	7307@0.1U 0402 16V4Z	SDVOB_G <17>
PCIE MTX GRX N2	C242	1	2	7307@0.1U 0402 16V4Z	SDVOB_B# <17>
PCIE MTX GRX P2	C241	1	2	7307@0.1U 0402 16V4Z	SDVOB_B <17>
PCIE MTX GRX N3	C235	1	2	7307@0.1U 0402 16V4Z	SDVOB_CLK# <17>
PCIE MTX GRX P3	C234	1	2	0.1U 0402 16V4Z	SDVOB_CLK <17>

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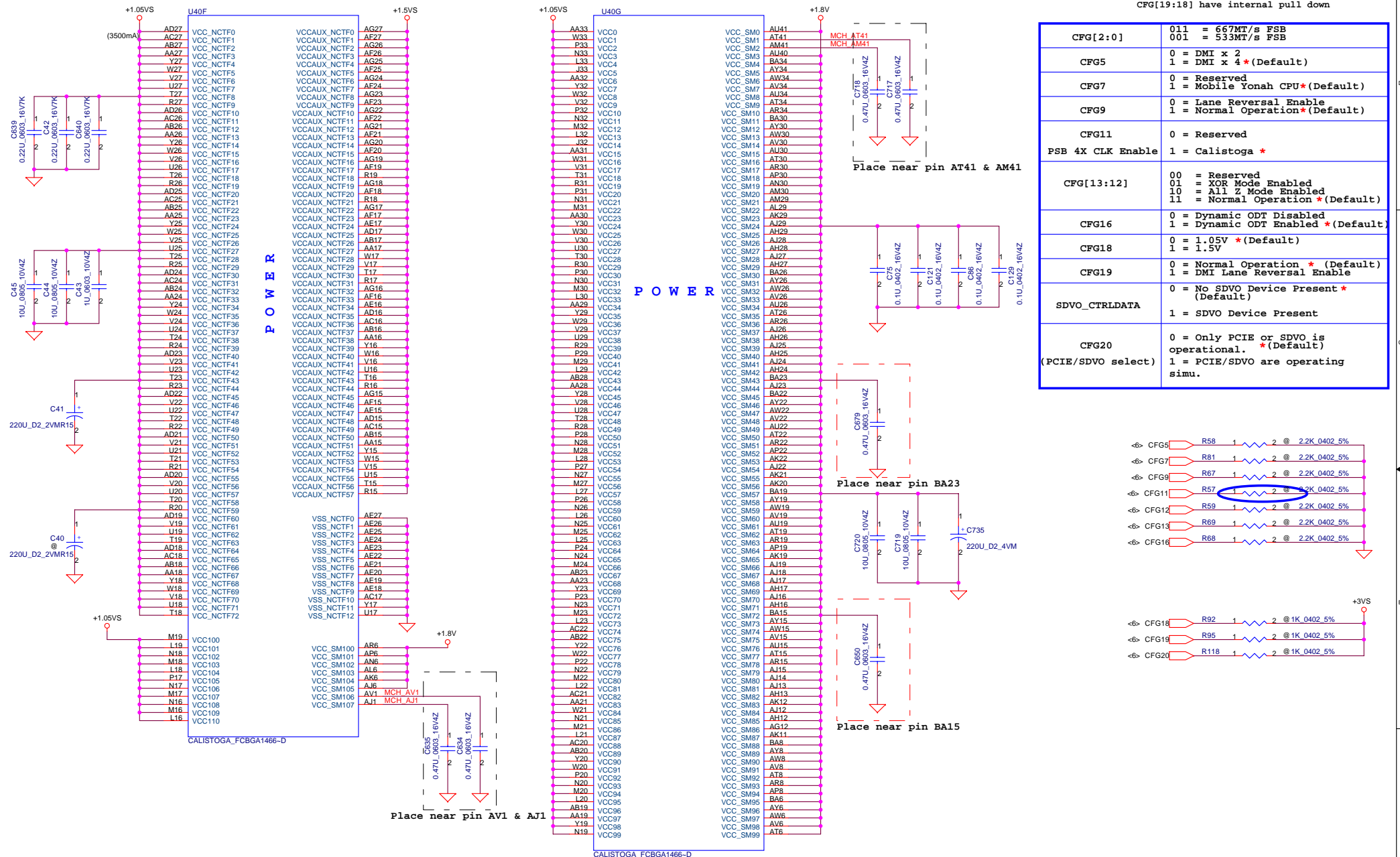


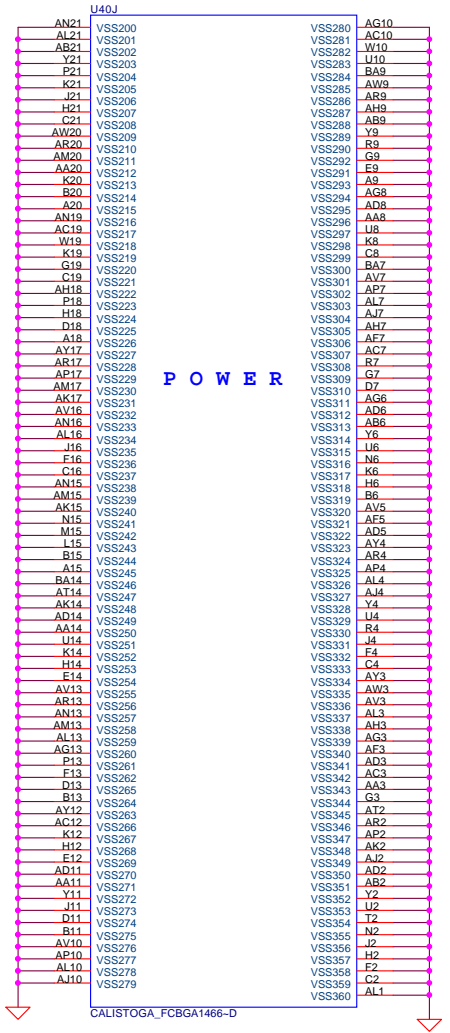
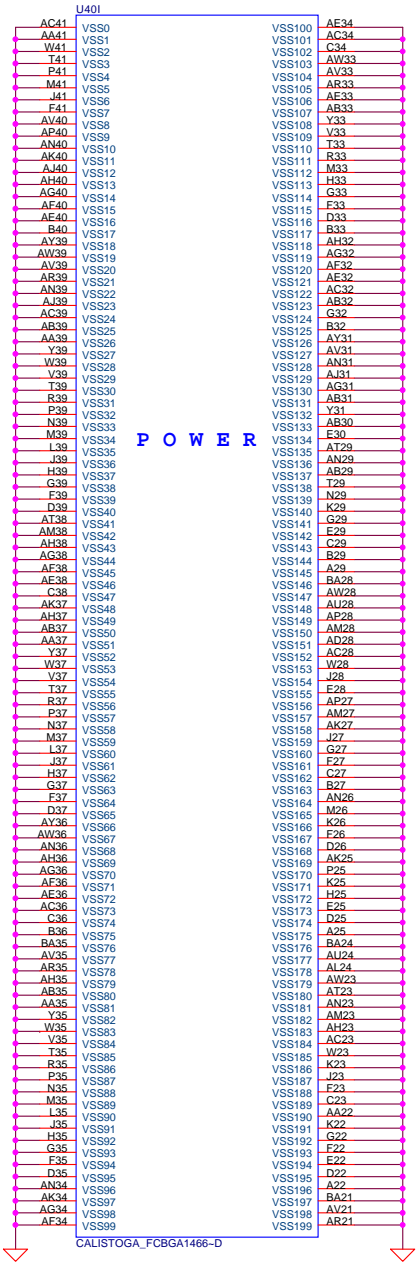


# Strap Pin Table

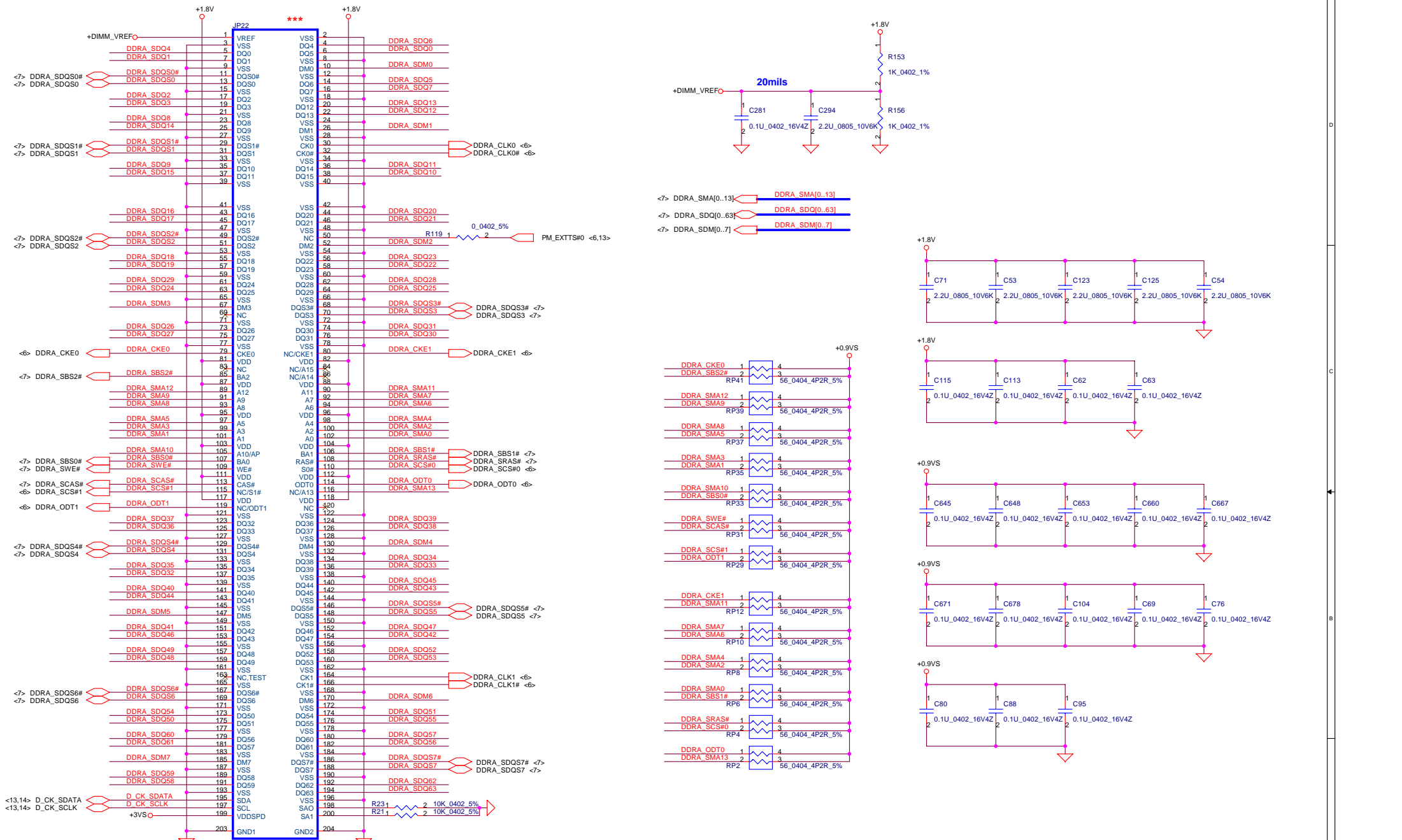
CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.





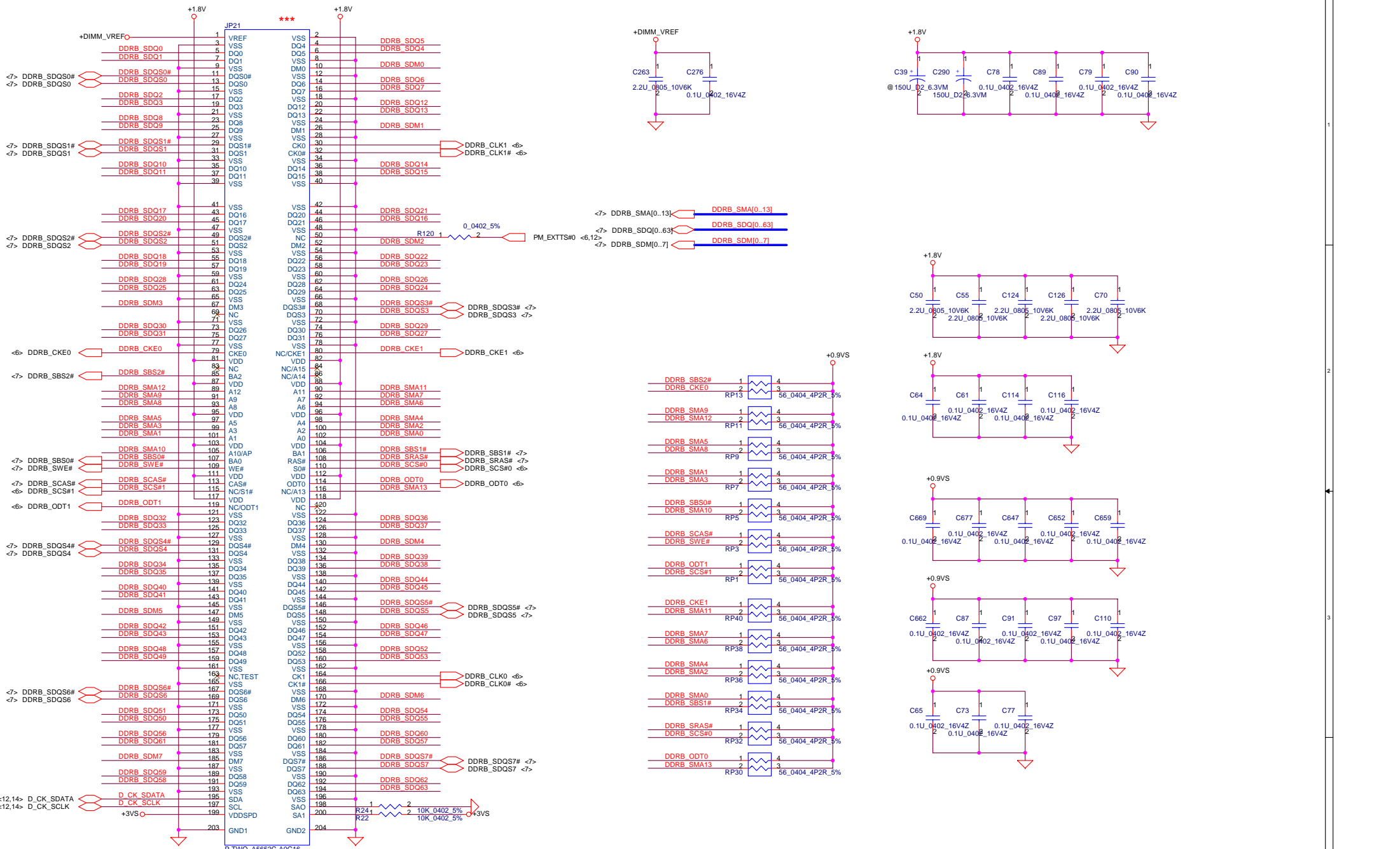
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**DIMM0 STD H:9.2mm (BOT)**

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**DIMM1 STD H:5.2mm (BOT)**

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FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

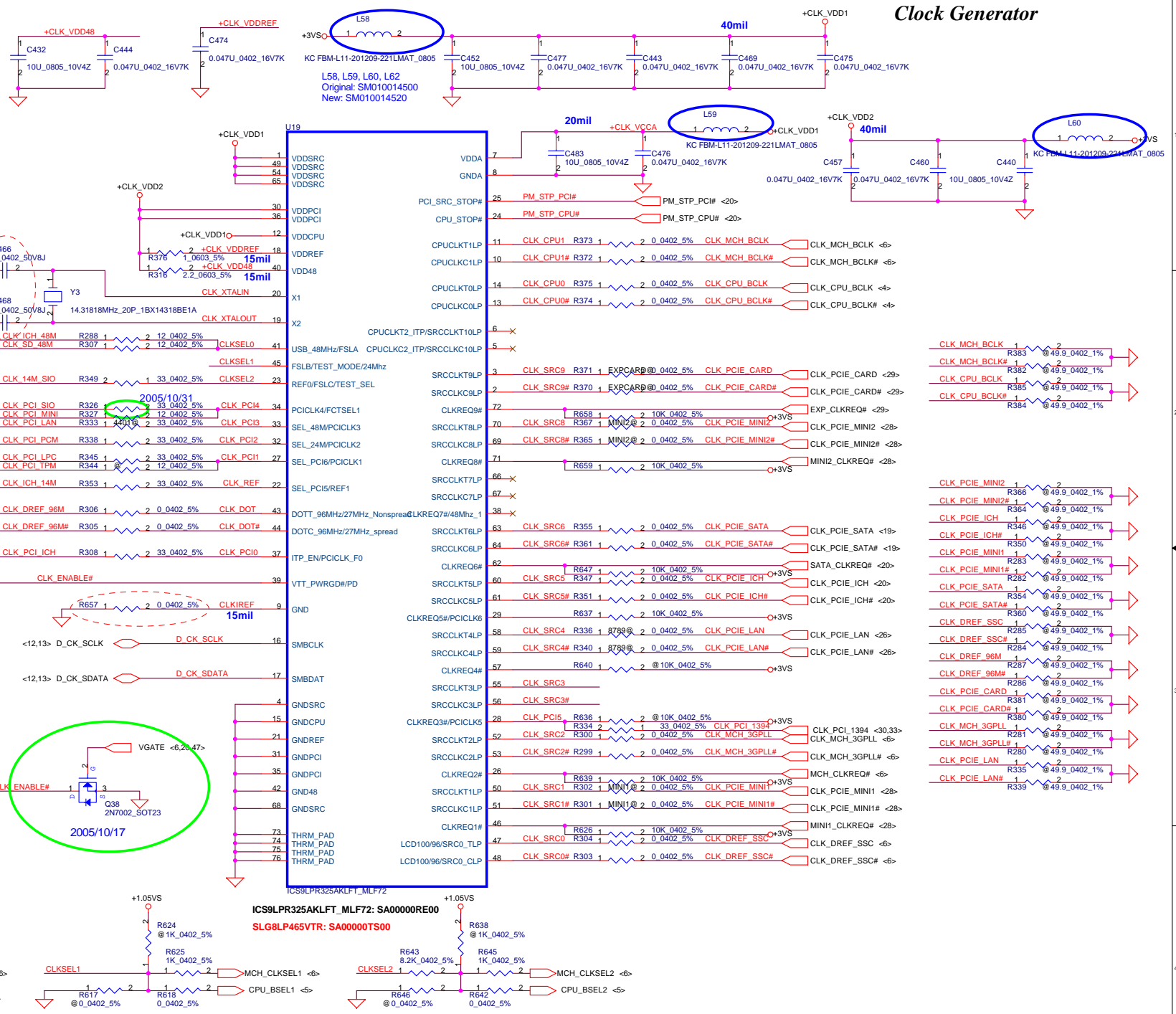
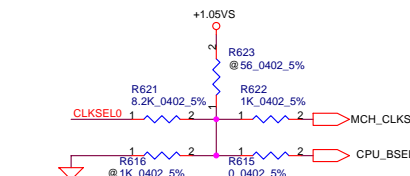
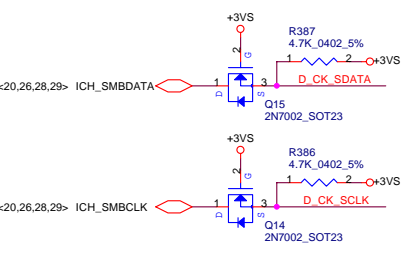
\*\*SEL\_24M/PCICLK2=0=TESTMODE  
\*\*SEL\_PCI6/PCICLK1=0=CLKREQ5#

\*\*SEL\_PCI5=1=PCICLK5  
ITP\_EN/PCICLK\_F0=0=SRC pair

CLK PCIO  
R619 10K\_0402\_5%  
ITP\_EN/PCICLK\_F0=0=SRC pair

CLK PC14  
R713 10K\_0402\_5%  
08/29 add

CLK ENABLE#  
R620 10K\_0402\_5%  
2005/10/17



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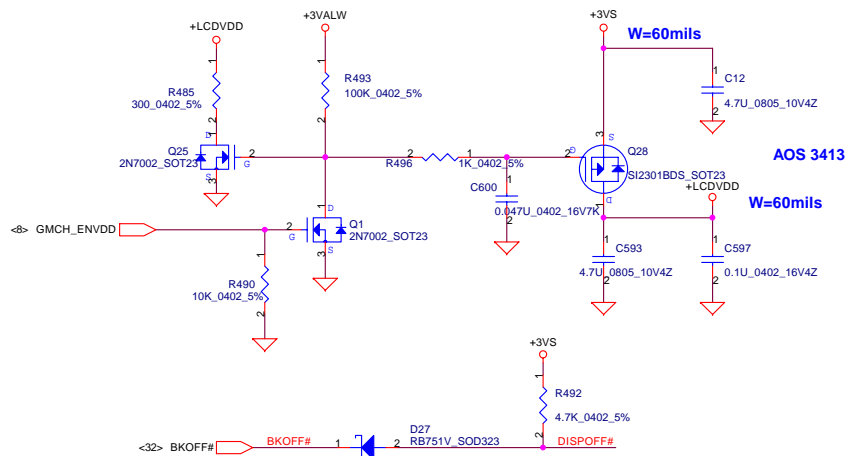
## Clock Generator

**Compal Electronics, Inc.**

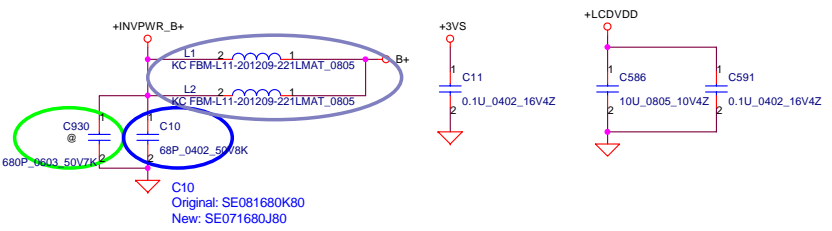
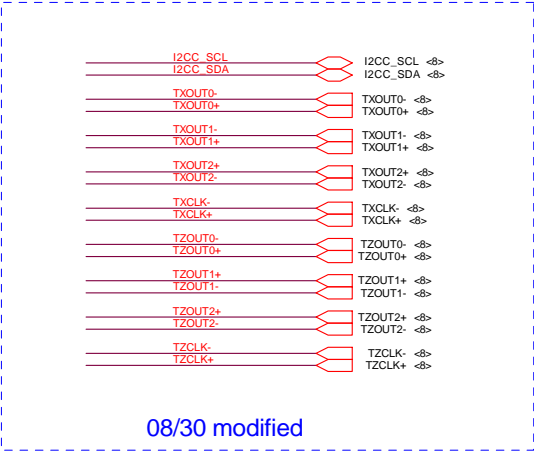
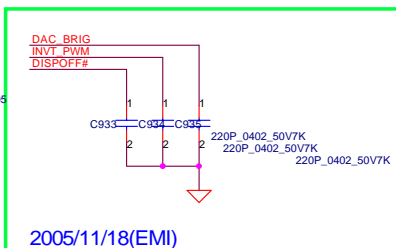
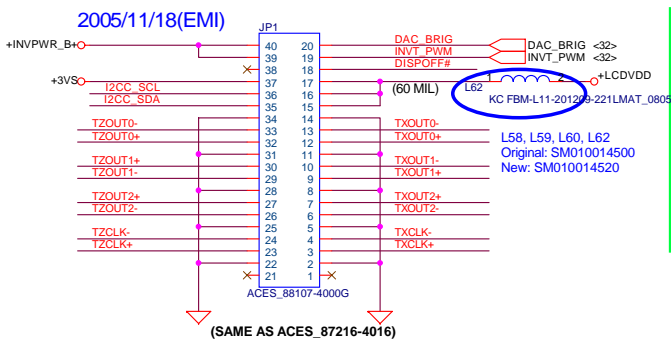
**SCHEMATIC, M/B LA-3081P**

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# LCD POWER CIRCUIT

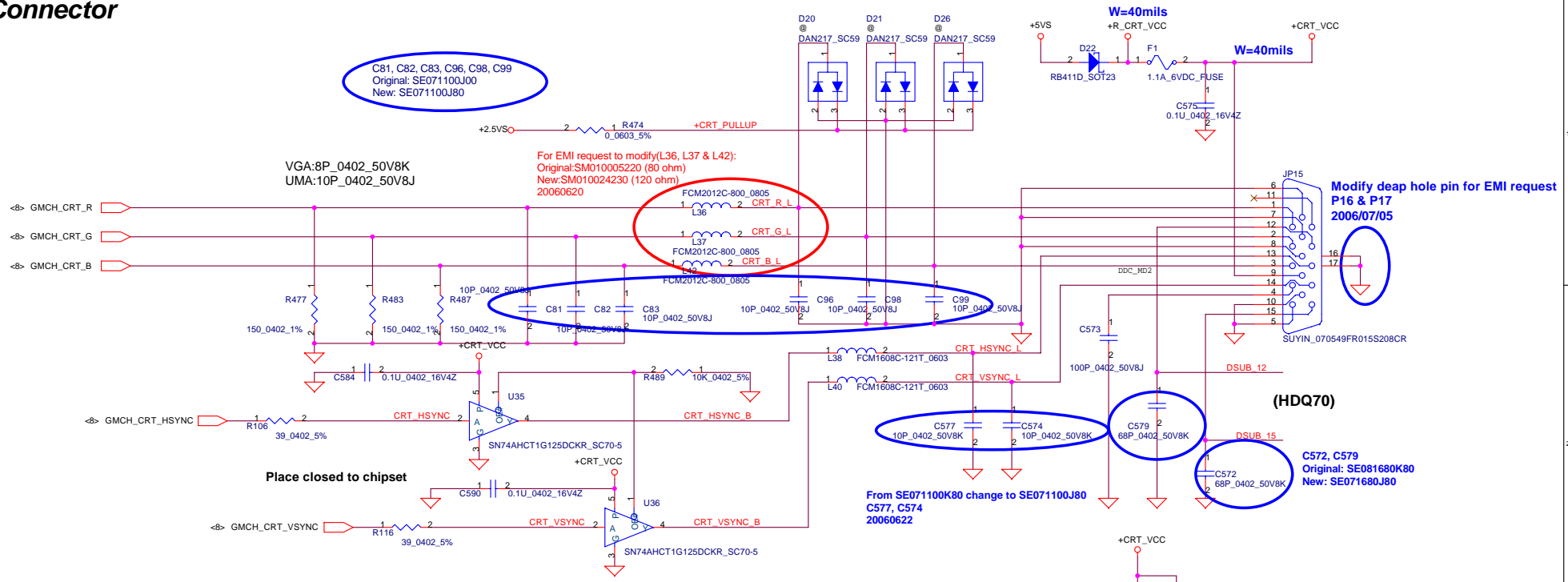


## LCD/PANEL BD. Conn.

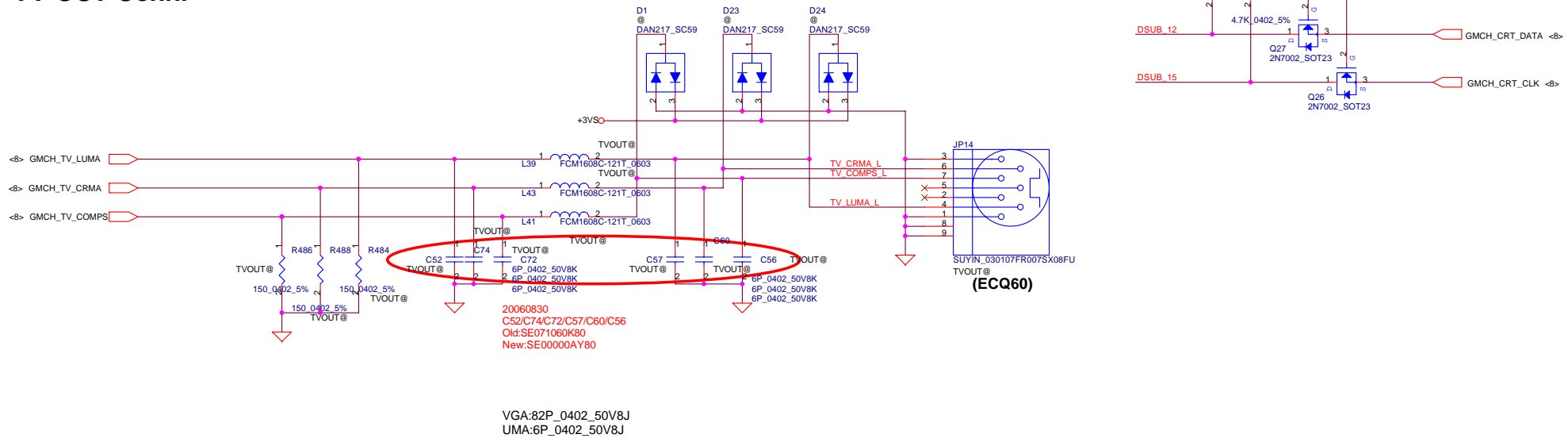


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# CRT Connector

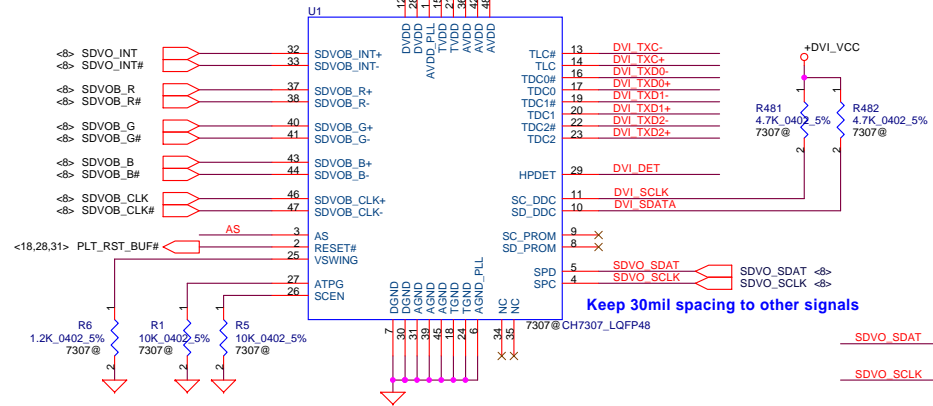
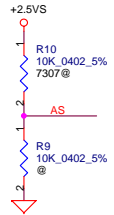
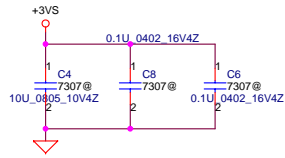
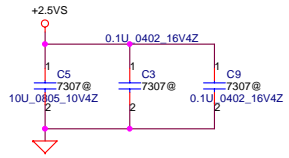


# TV-OUT Conn.



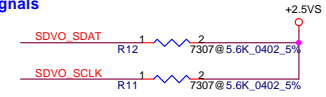
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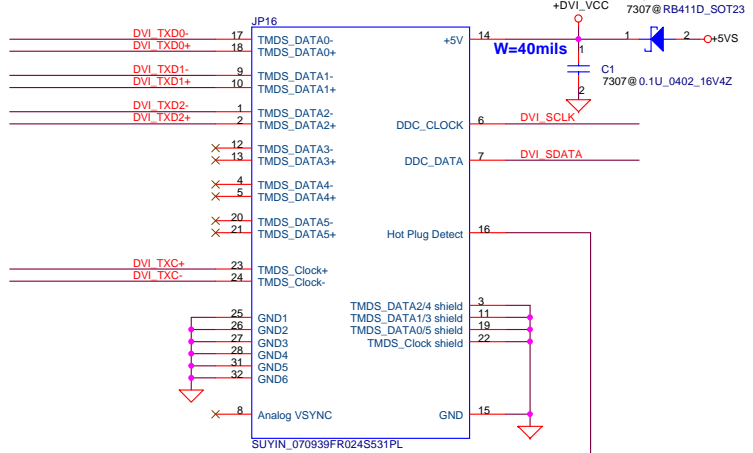


BOM structure	DVI from SDVO
7307@	Stuff
@	No_Stuff

Keep 30mil spacing to other signals



### DVI-D Connector



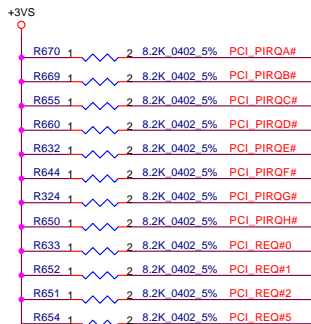
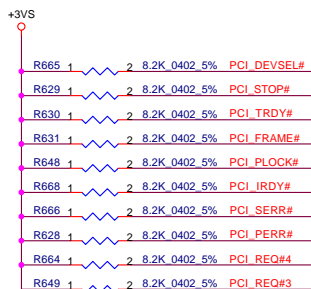
(HDQ70)

Security Classification	Compal Secret Data	
Issued Date	2006/10/4	Deciphered Date
		2007/10/4

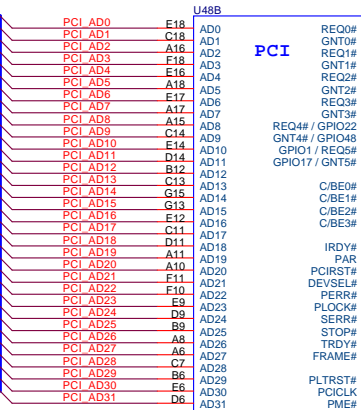
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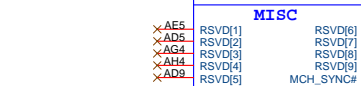
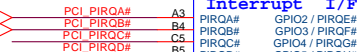
ICH7M(B-0) (QK17) [ES3] : SA00000JK30



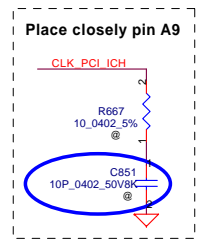
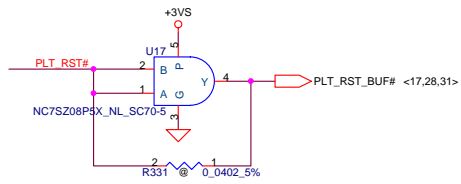
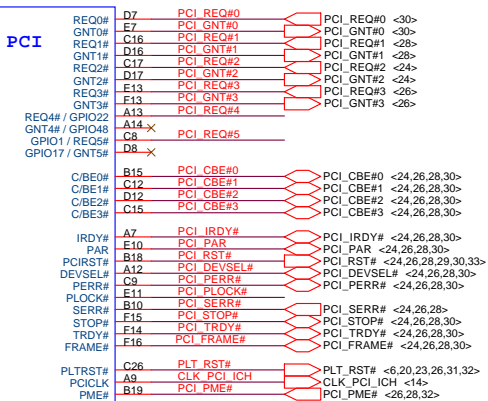
<24,26,28,30> PCI\_AD[0..31]



<24> PCI\_PIRQA#  
<24> PCI\_PIRQB#

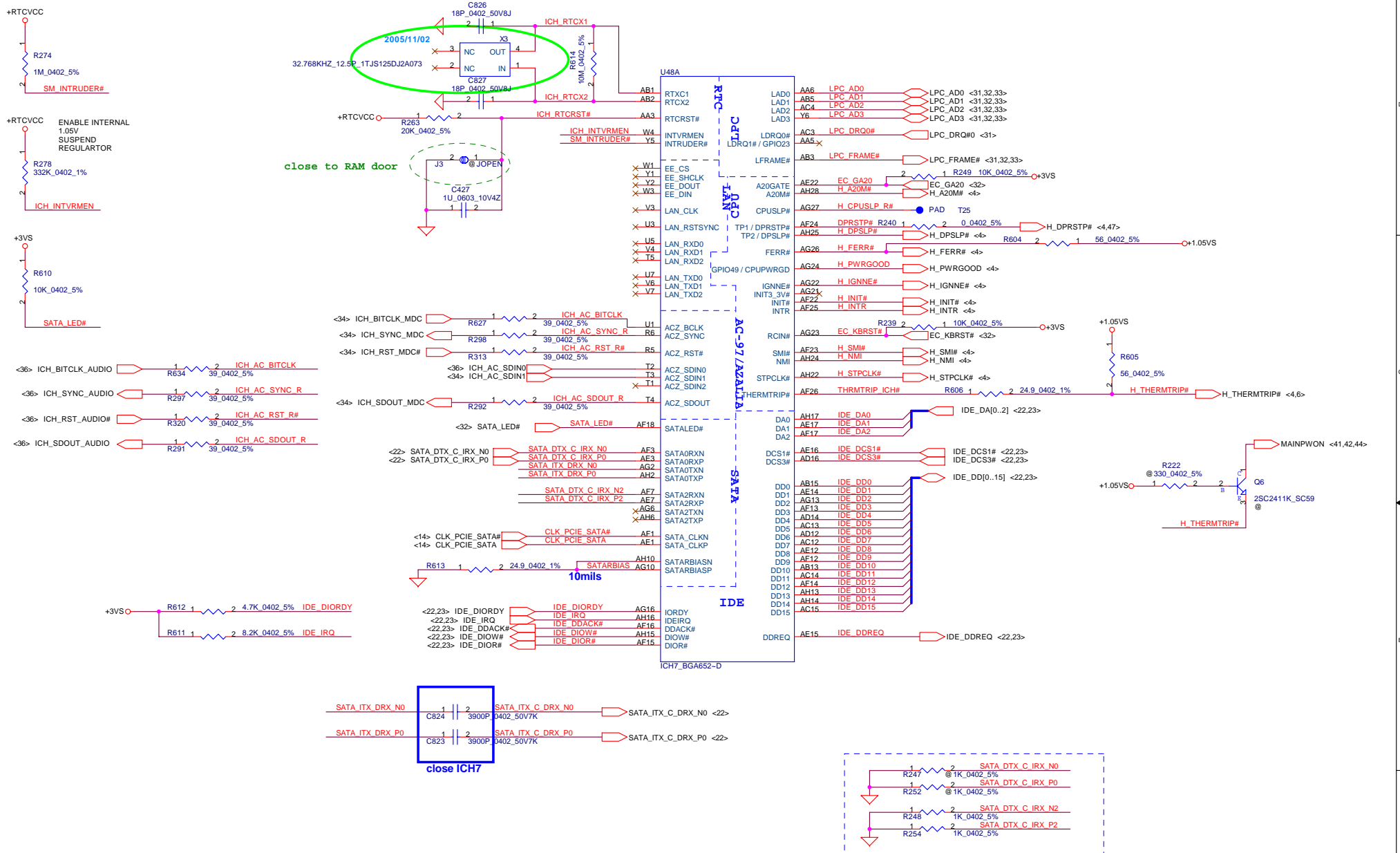


CH7\_BGA652-D



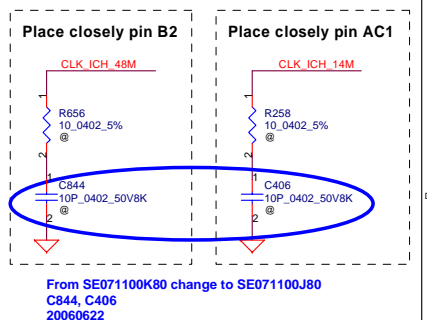
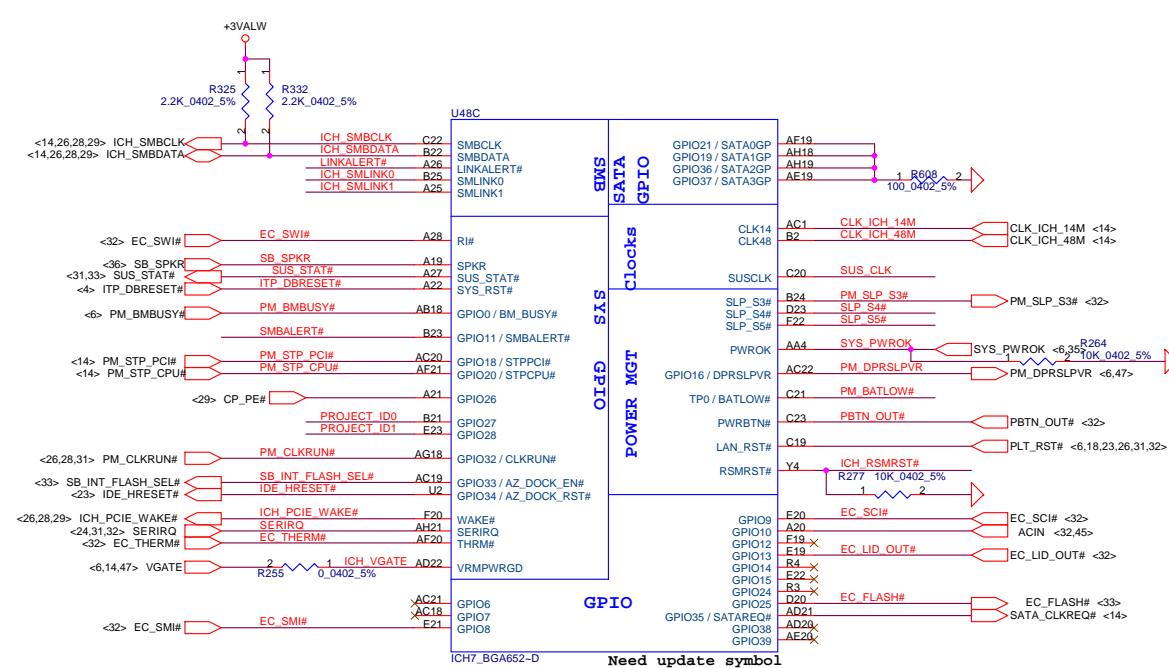
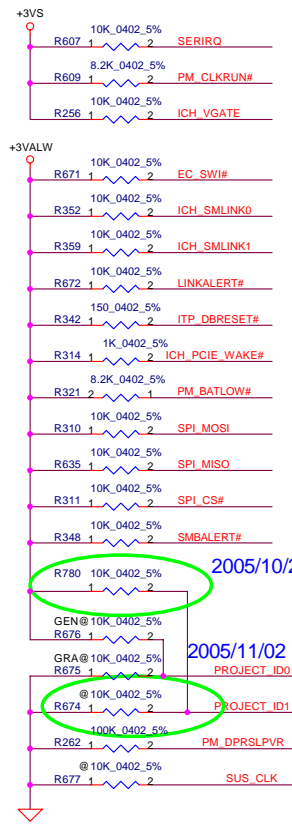
From SE071100K80 change to SE071100J80 20060622

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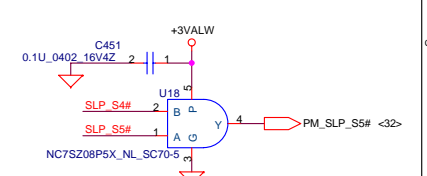
SATA\_Rx/n/p need tie to ground when SATA port no used

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From SE071100K80 change to SE071100J80  
C844, C406  
20060622

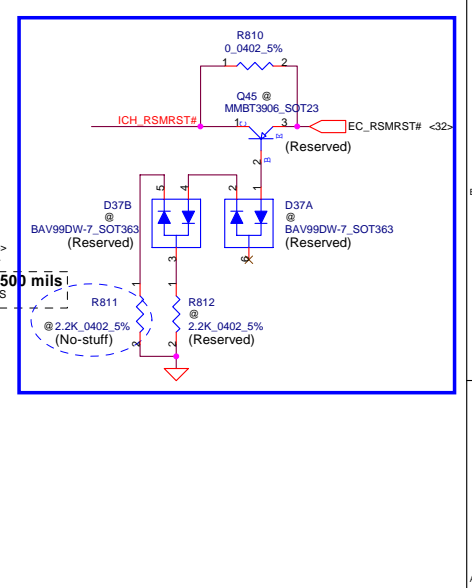
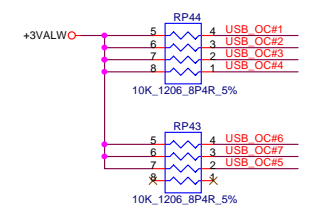
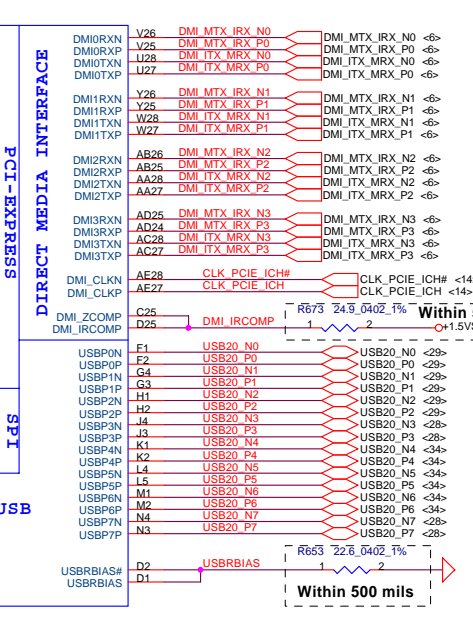
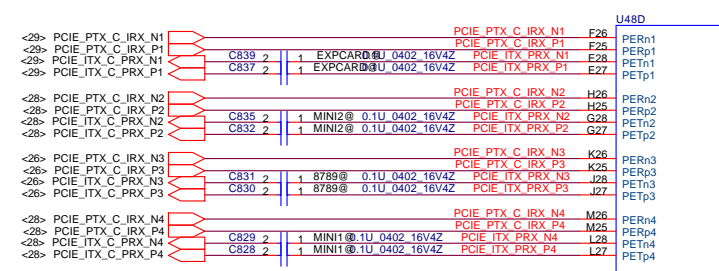
PM\_DPRSPLVPR : Need to series  
a 500Ohm resistor to IMVP6



2005/10/27

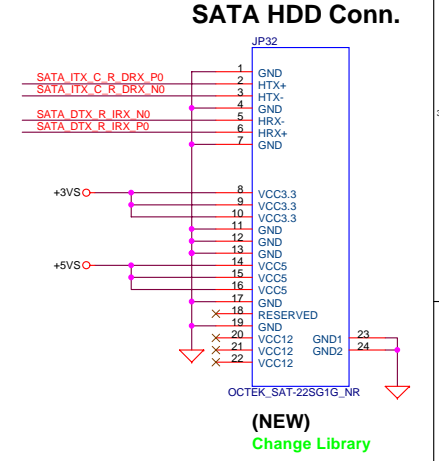
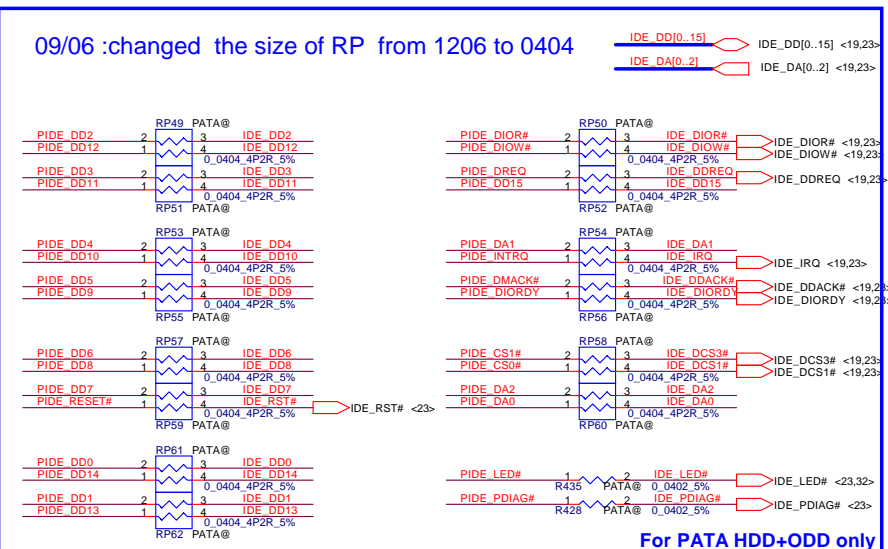
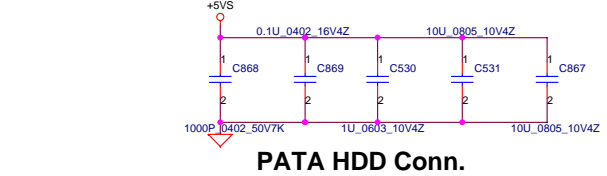
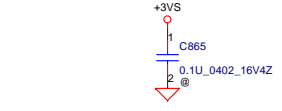
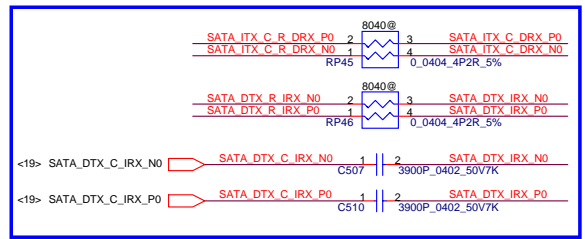
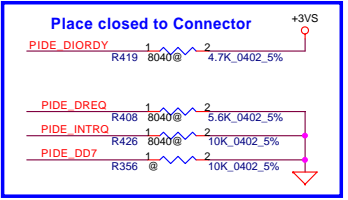
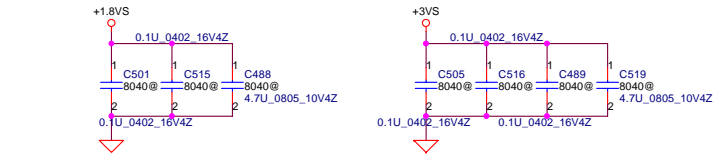
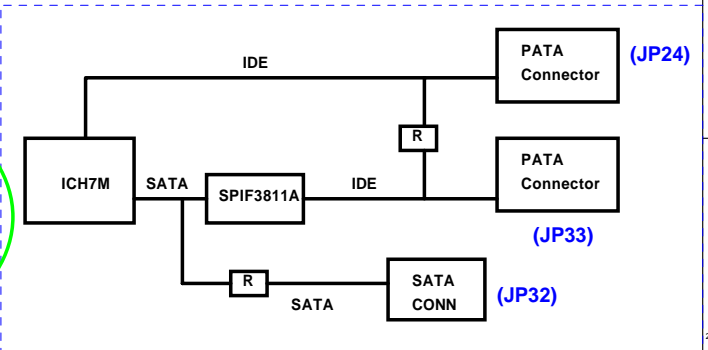
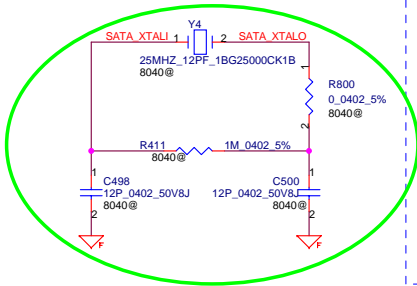
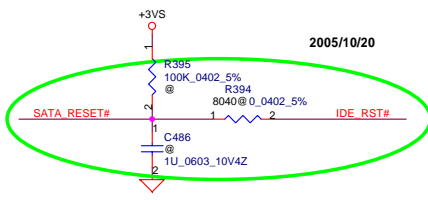
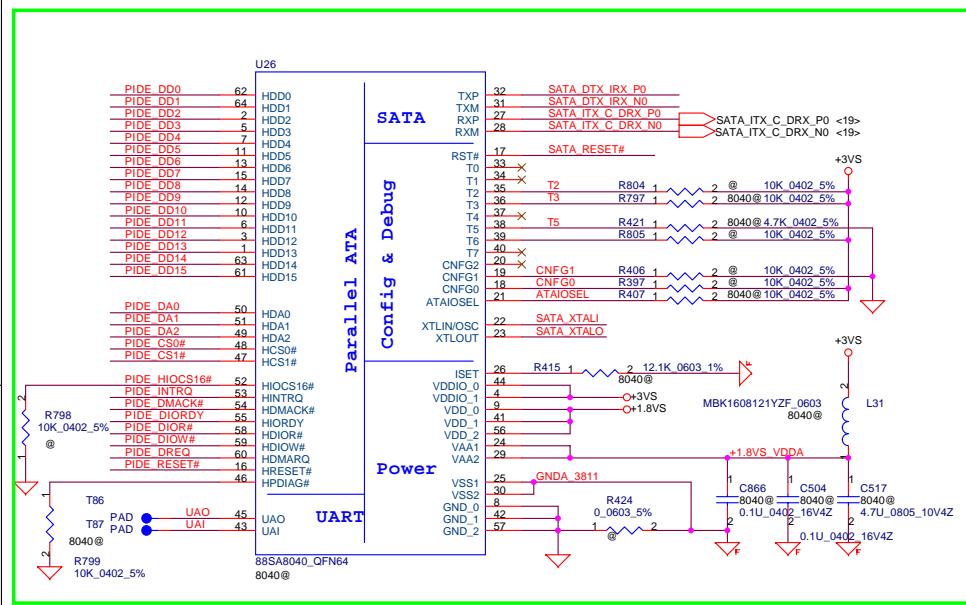
2005/11/02

PROJECT_ID[1:0]	
00	= Grapevine
01	= Geneva
10	= HBL51_PATA



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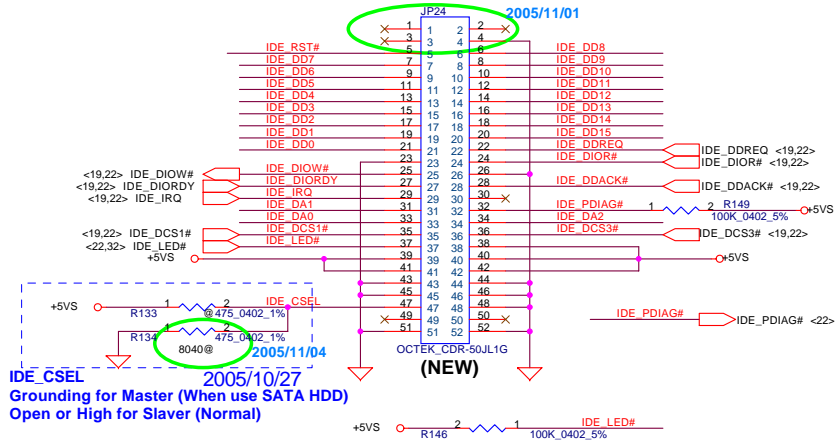
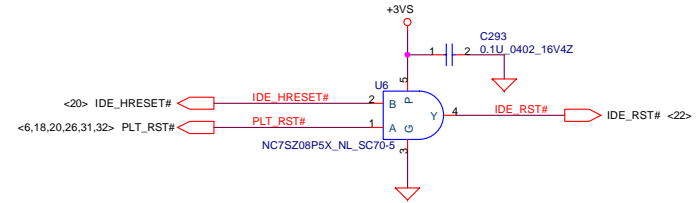
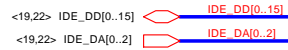
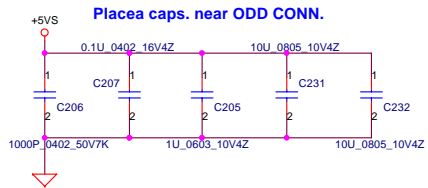




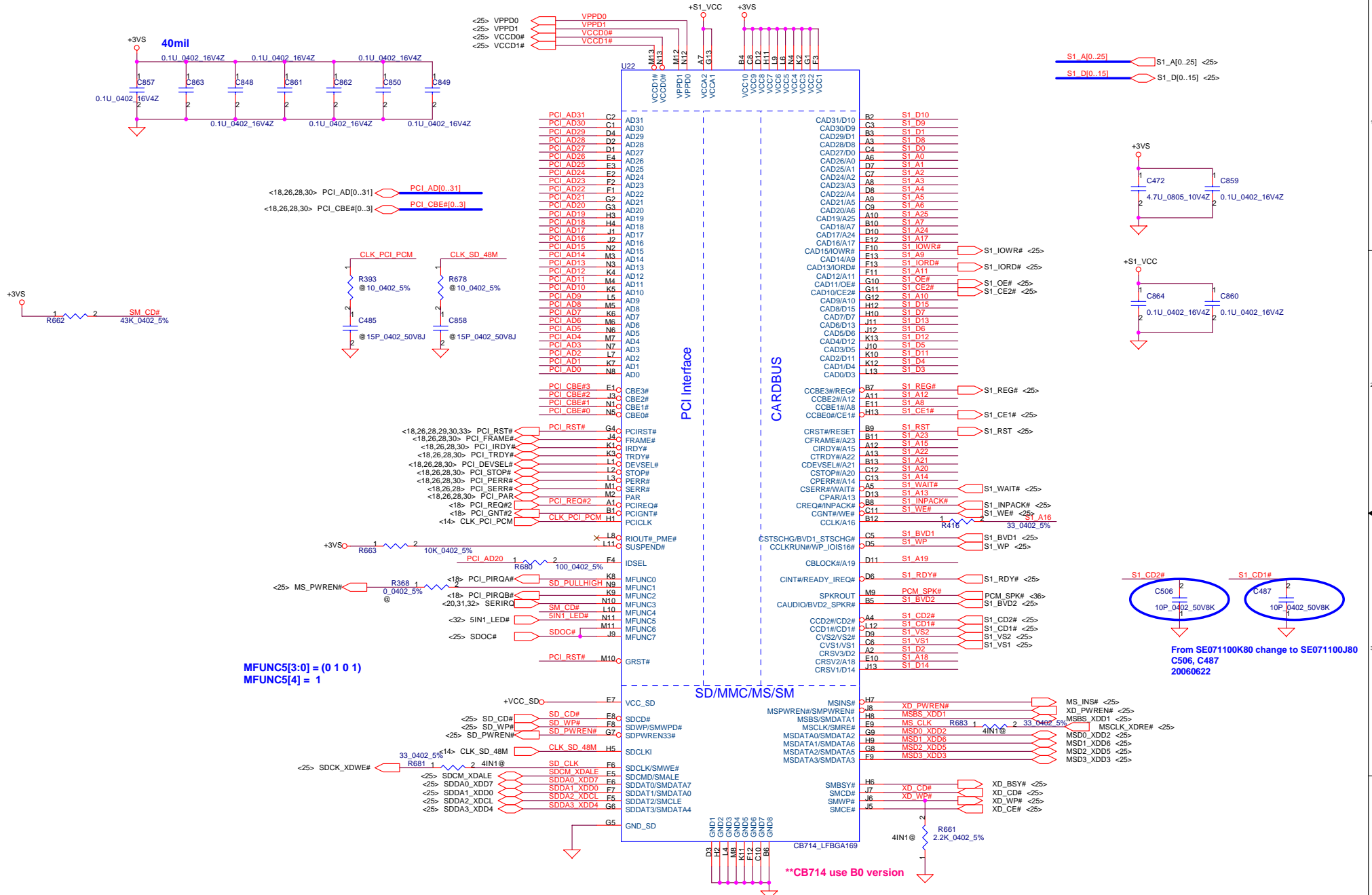
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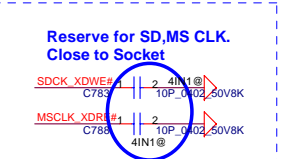
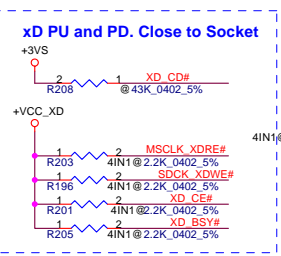
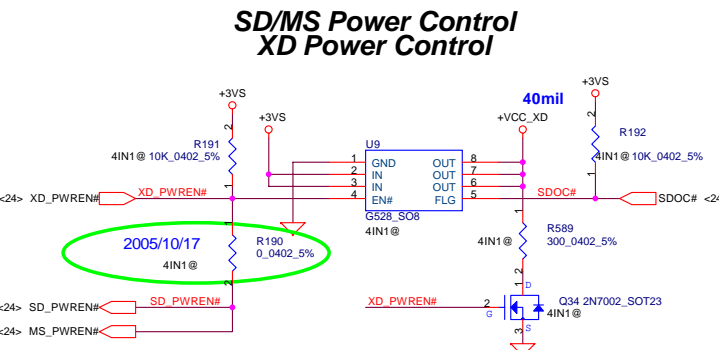
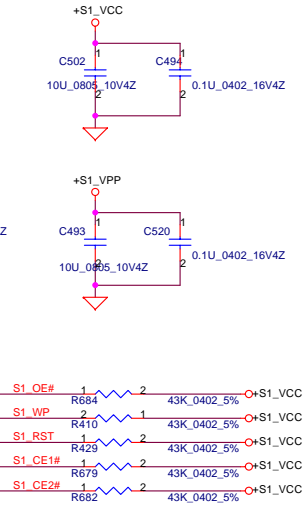
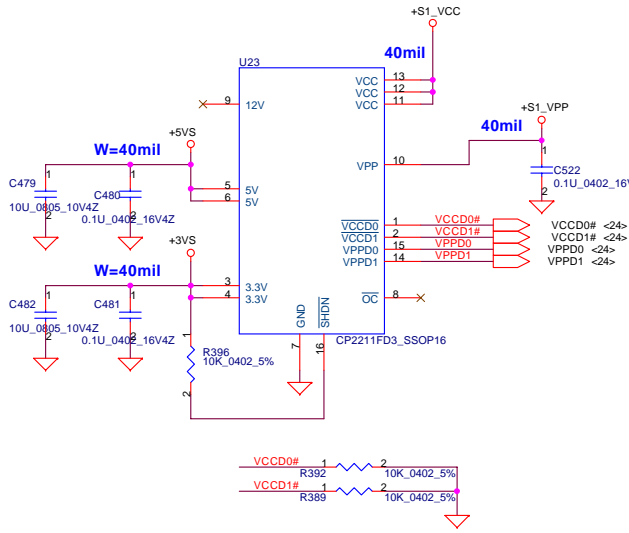
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MFUNC5[4] = 1

From SE071100K80 change to SE071100J80  
C506, C487  
20060622

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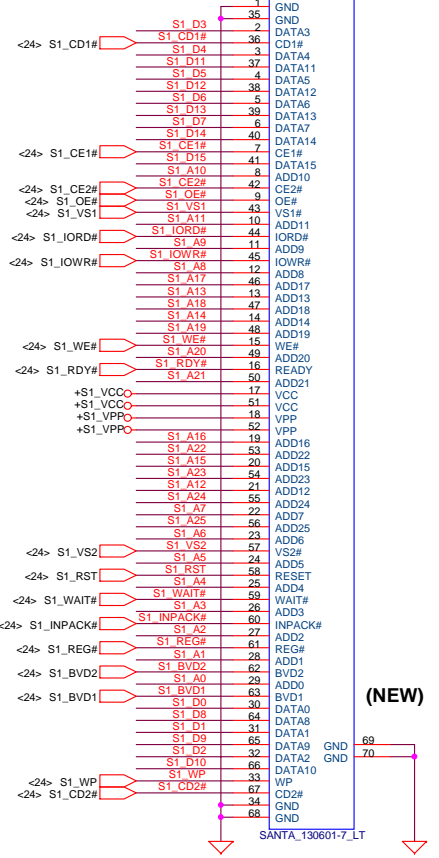


### PCMCIA Power Control



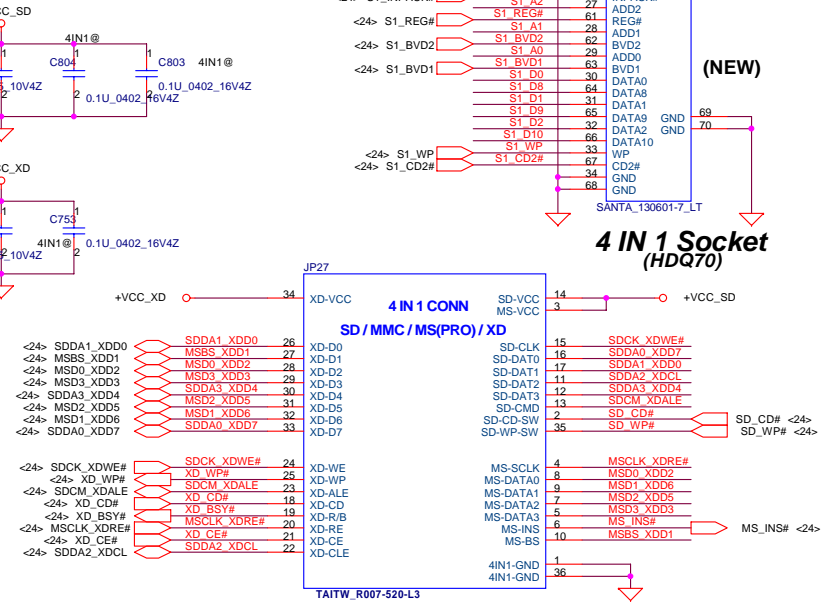
From SE071100K80 change to SE071100J80  
C783, C788  
20060622

### PCMCIA Socket



(NEW)

### 4 IN 1 Socket (HDQ70)

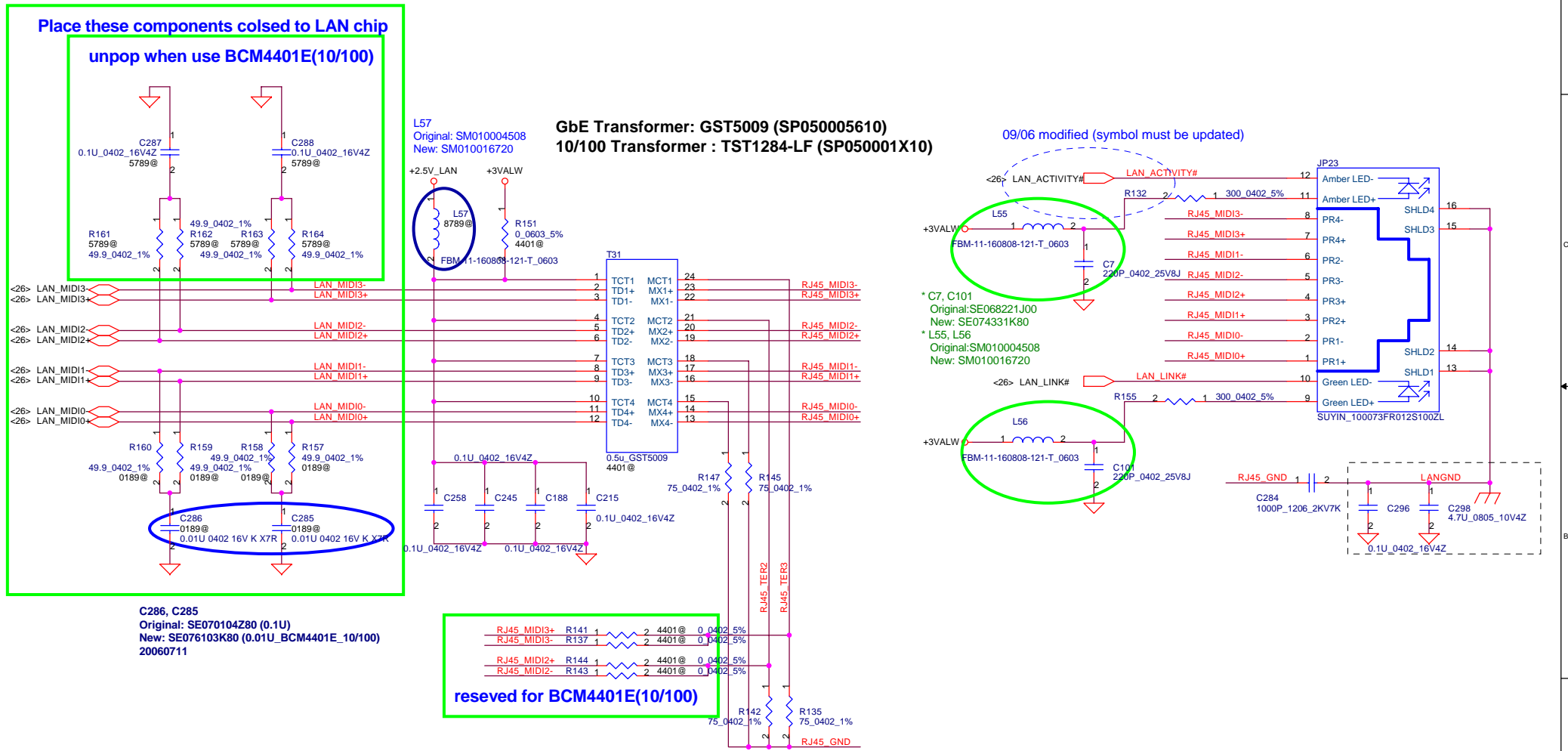


Security Classification	Compal Secret Data		Title	Schematic, M/B LA-3081P	
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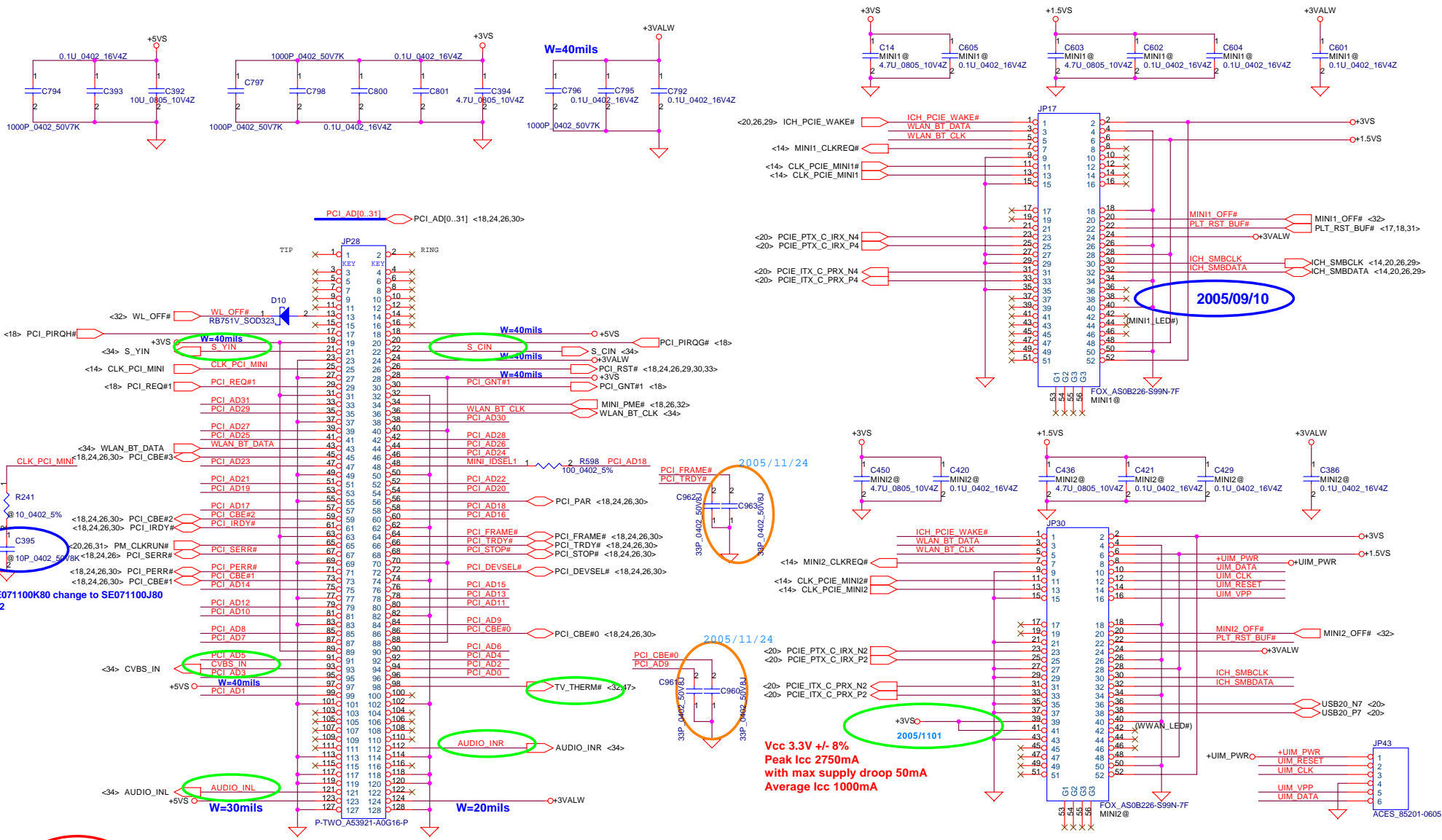
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# LAN BCM4401E/ BCM5789



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From SE071100K80 change to SE071100J80  
20060622

2006/03/01  
C895 change BOM structure to \*  
20060713

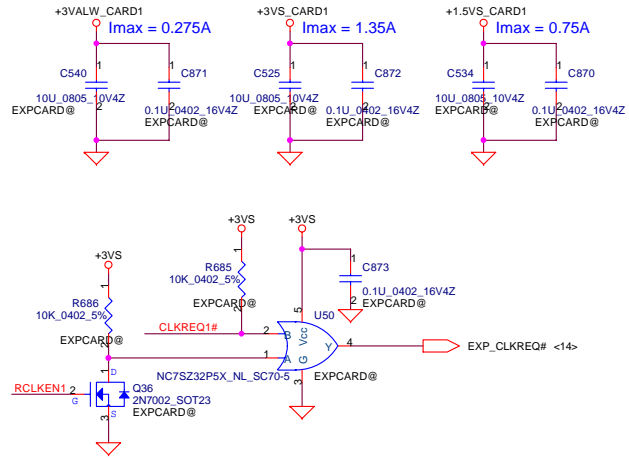
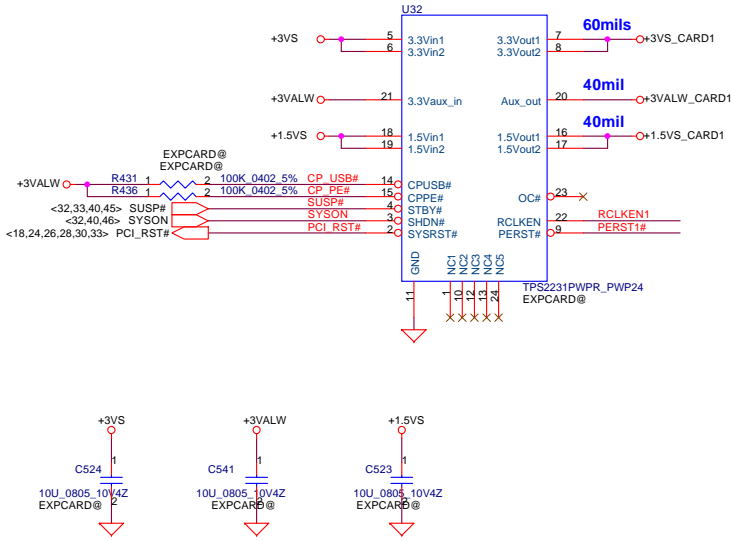
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data	
Issued Date	2006/10/4	Deciphered Date
		2007/10/4

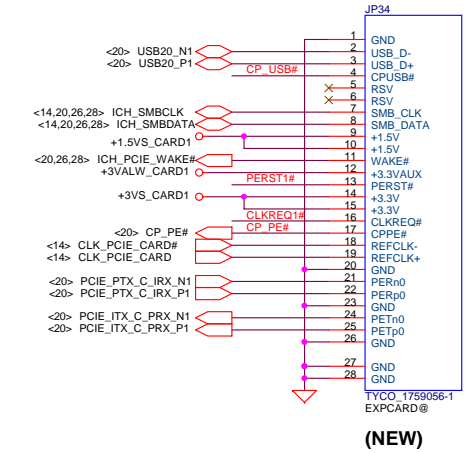
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SCHEMATIC, M/B LA-3081P			
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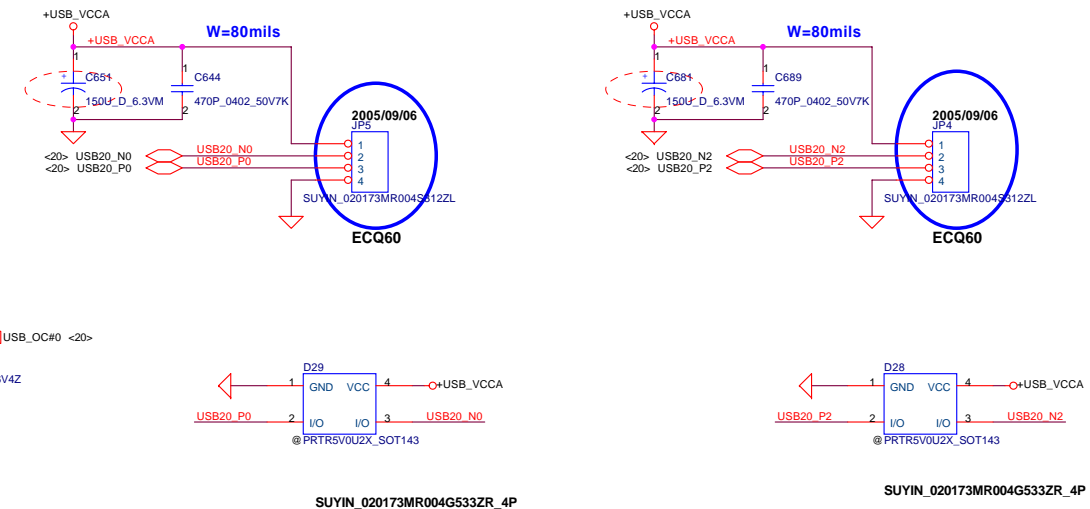
# New Card Power Switch



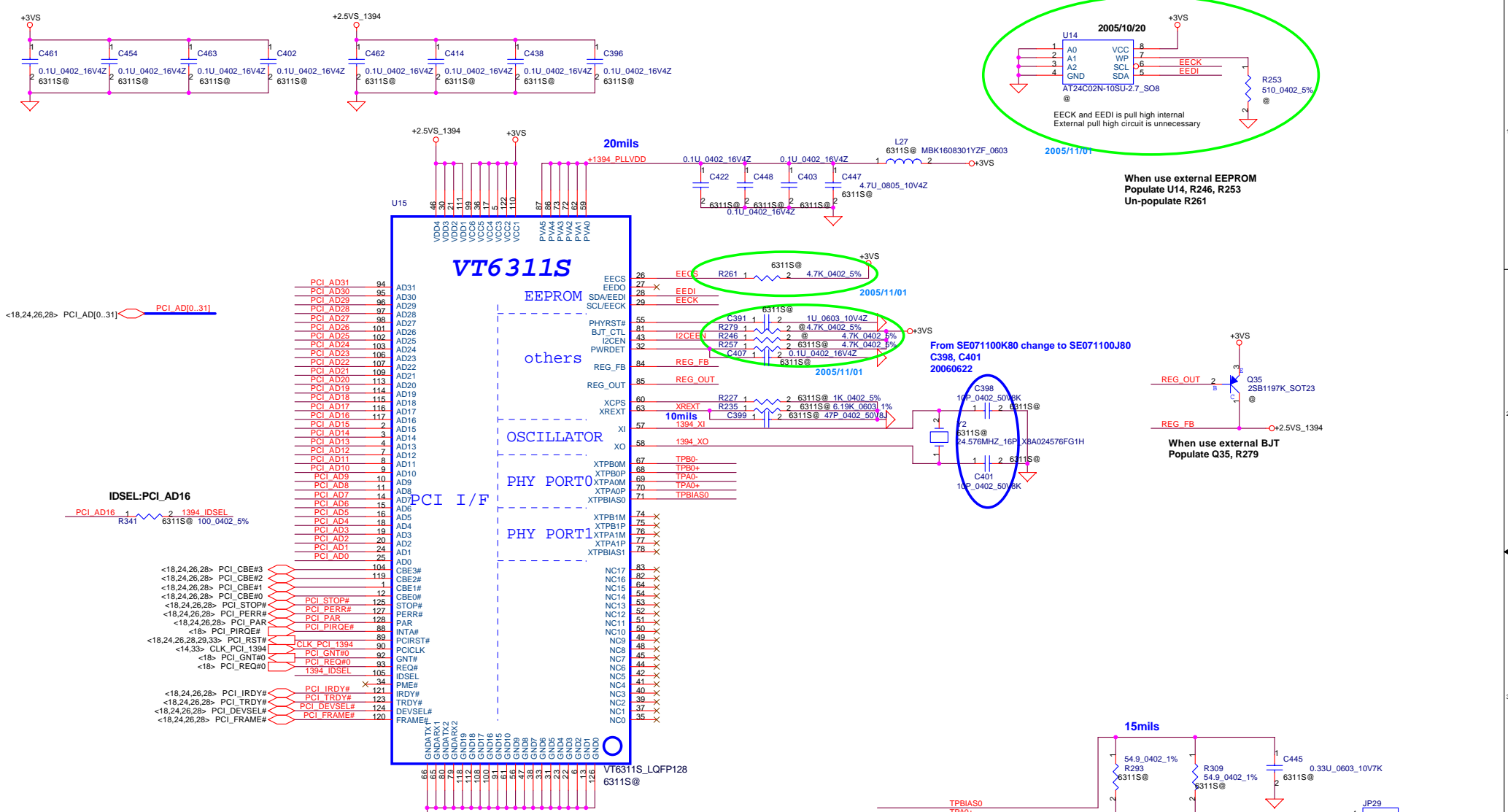
# New Card Socket (Left)



# USB CONN. 1 & 2



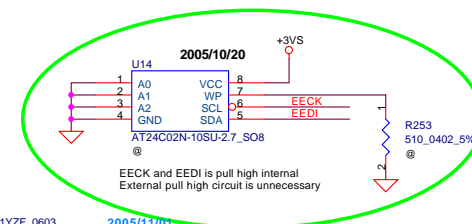
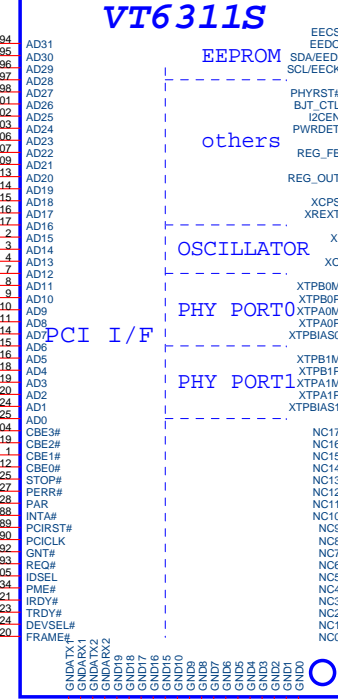
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Size B	Document Number	Date: 星期四, 十月 05, 2006		Sheet	29 of 47
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<18,24,26,28> PCI\_AD[0..31]

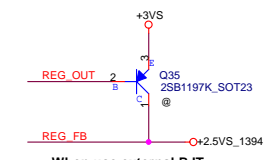
IDSEL:PCI\_AD16

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 <18,24,26,28> PCI\_STOP#  
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 <18,24,26,28> PCI\_PAR#  
 <18> PCI\_PIRQE#  
 <18,24,26,28,29,33> PCI\_RST#  
 <14,33> CLK PCI\_1394  
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 <18,24,26,28> PCI\_FRAME#

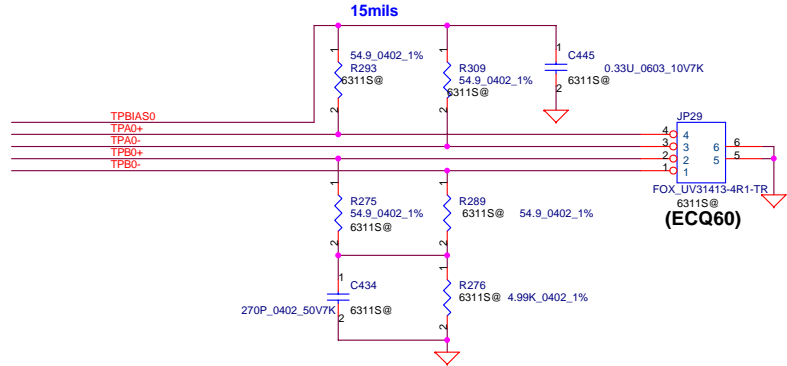


When use external EEPROM  
 Populate U14, R246, R253  
 Un-populate R261

From SE071100K80 change to SE071100J80  
 C398, C401  
 20060622



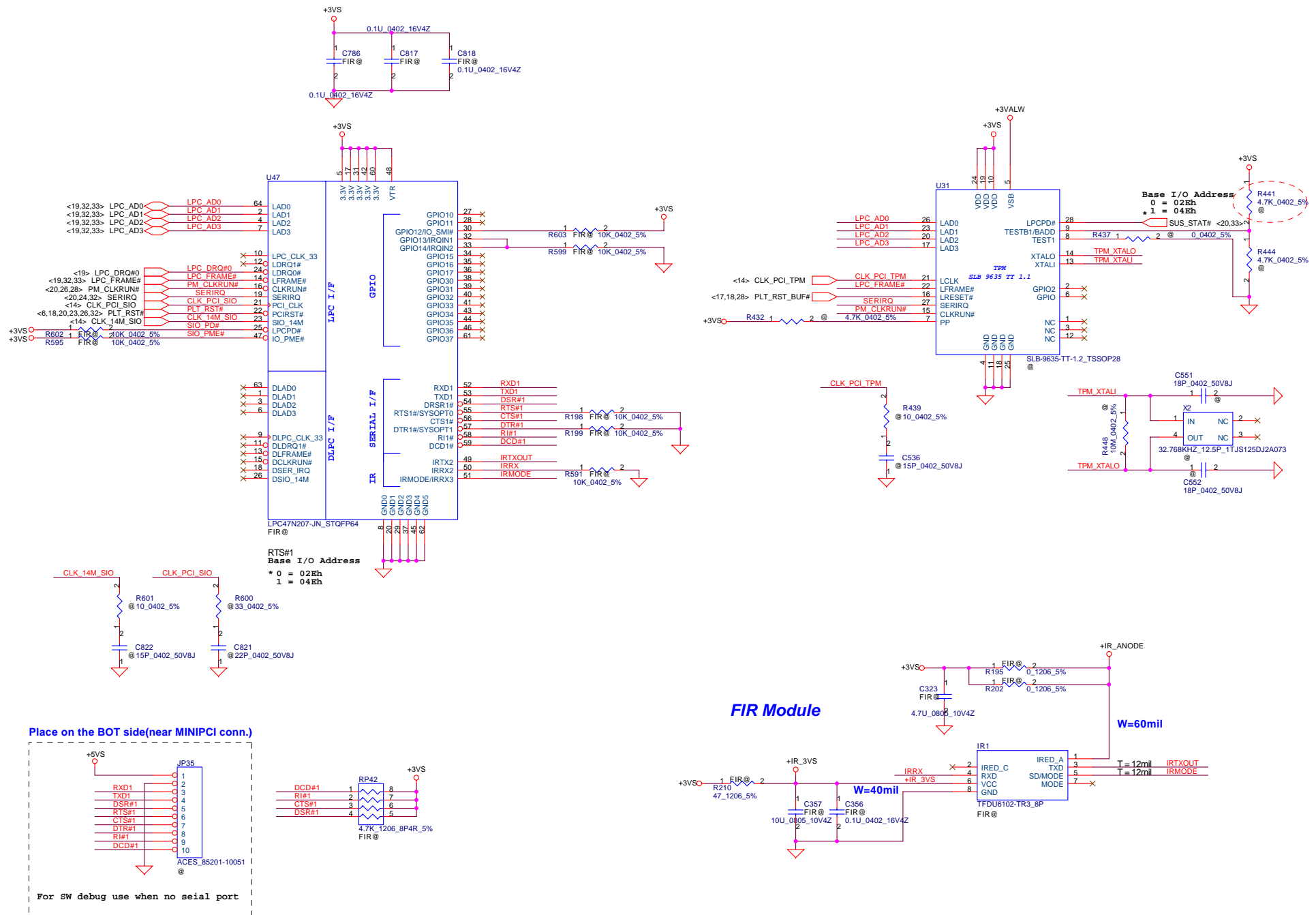
When use external BJT  
 Populate Q35, R279



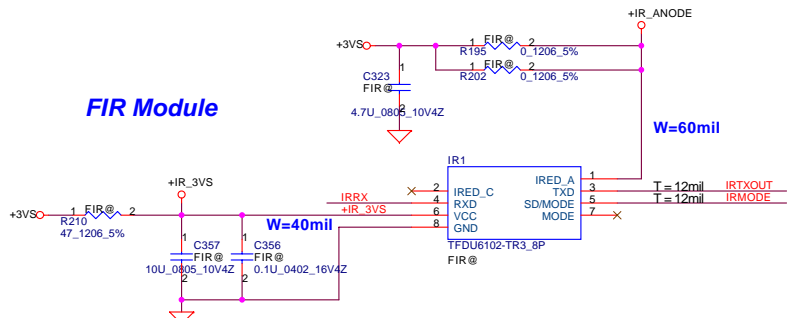
(ECQ60)

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SHEMATIC, M/B LA-3081P				Sheet 30 of 47 Rev G

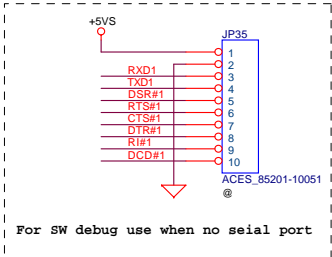
# SUPER I/O SMsC LPC47N207



## FIR Module

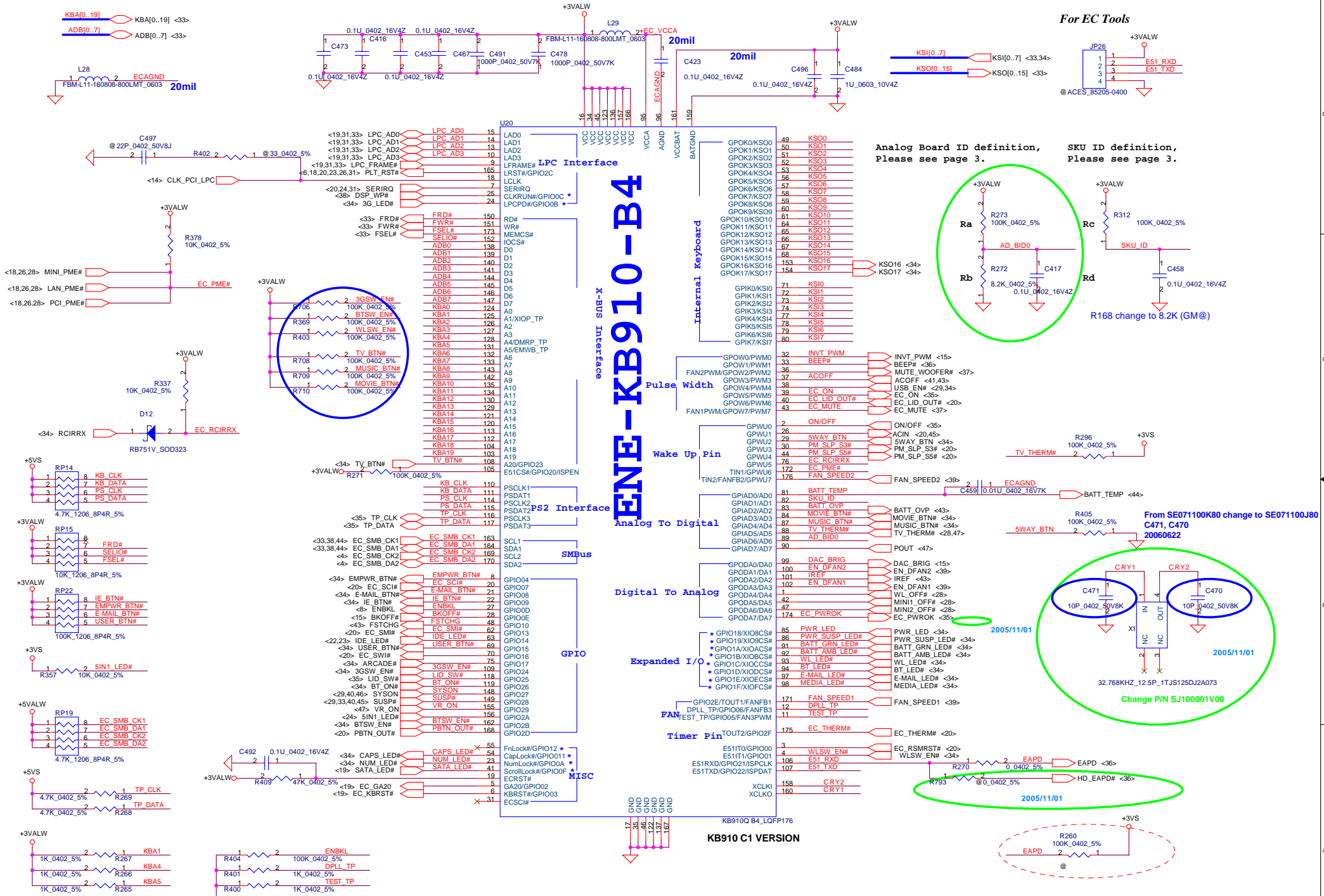


Place on the BOT side (near MINIPCI conn.)



For SW debug use when no serial port

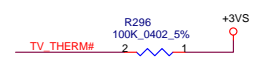
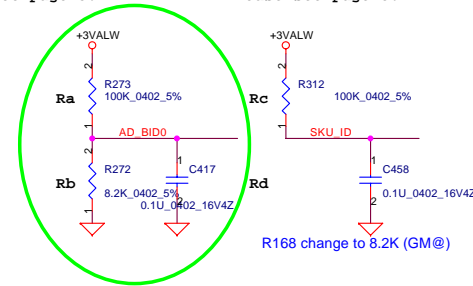
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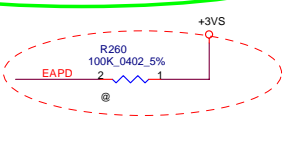
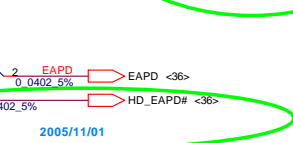
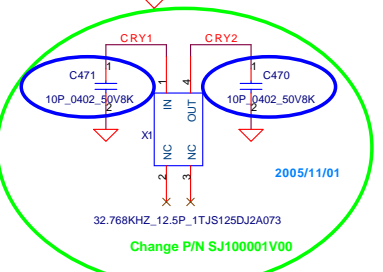
For EC Tools

Analog Board ID definition, Please see page 3.

SKU ID definition, Please see page 3.

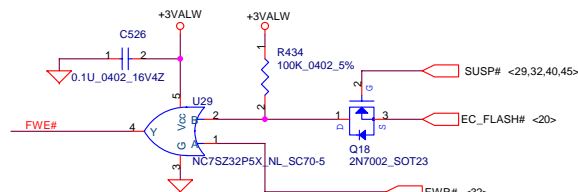


From SE071100K80 change to SE071100J80 C471, C470 20060622

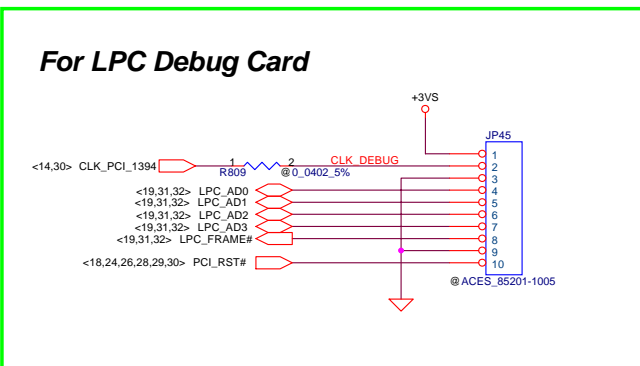
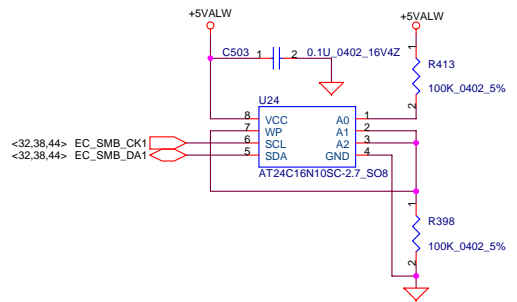


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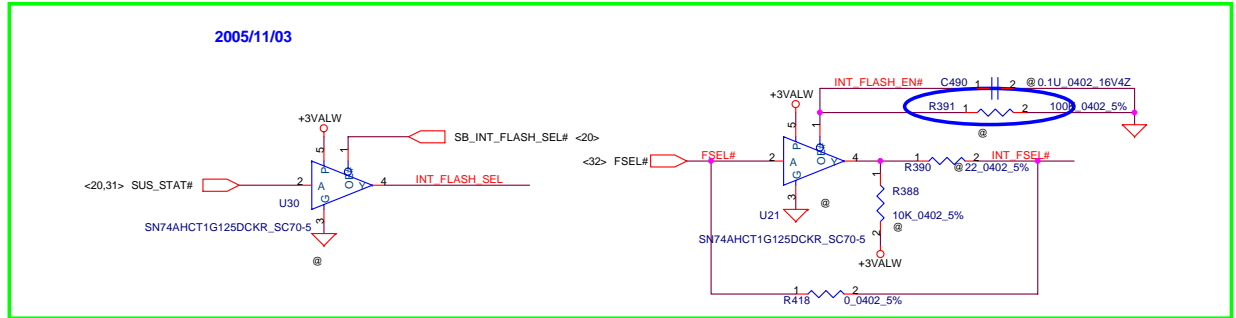
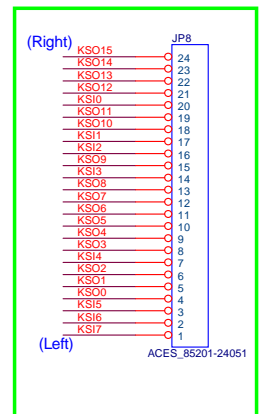
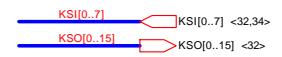




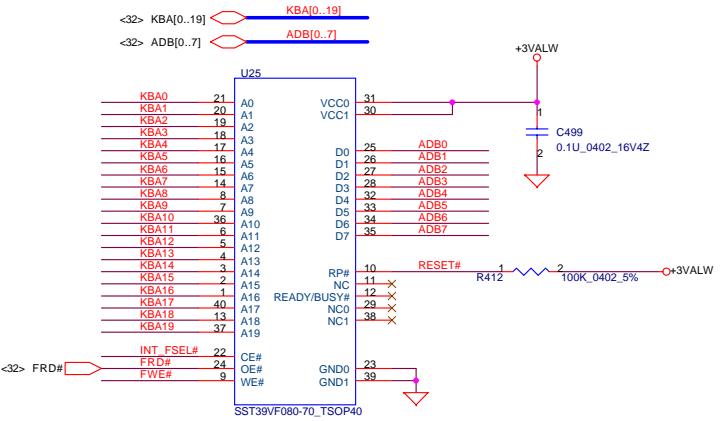
Check PCB Footprint



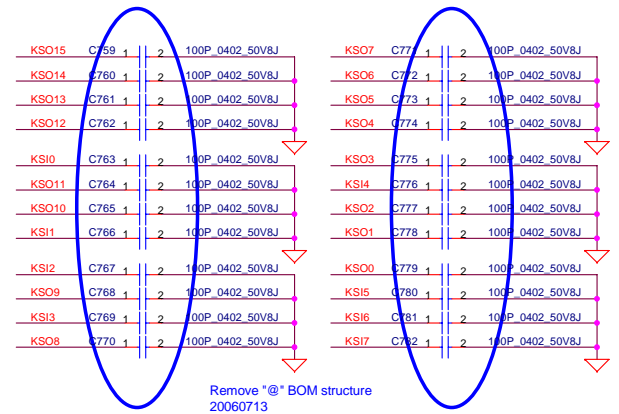
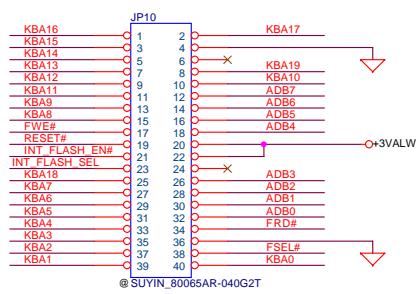
INT\_KBD Conn.



1MB Flash ROM

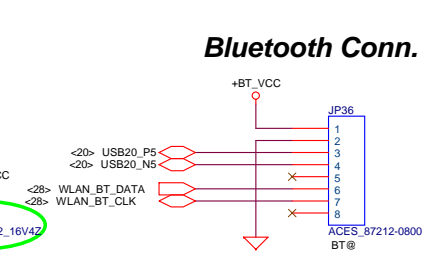
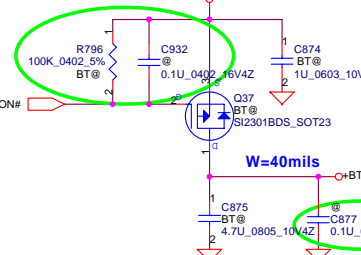
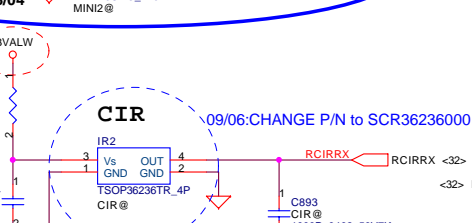
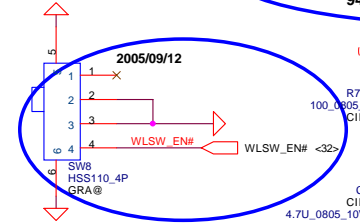
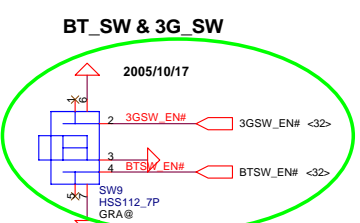
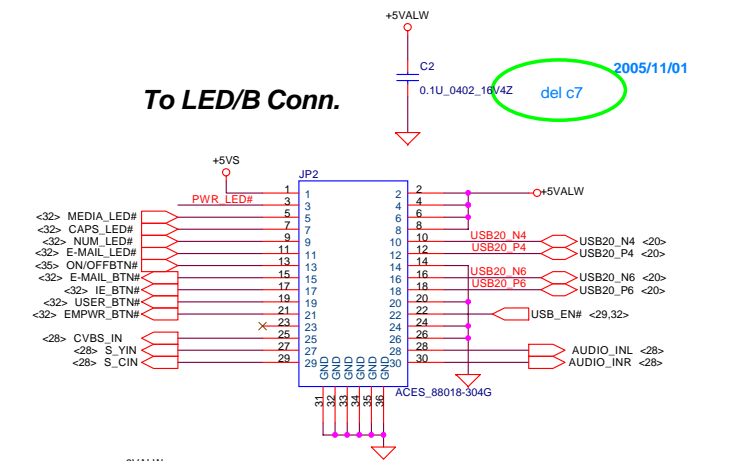
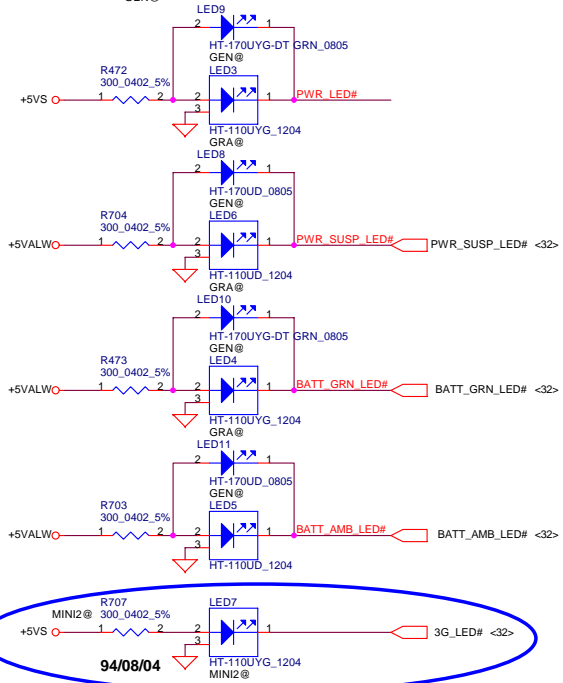
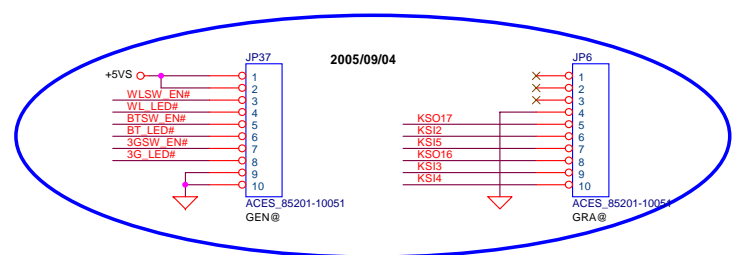
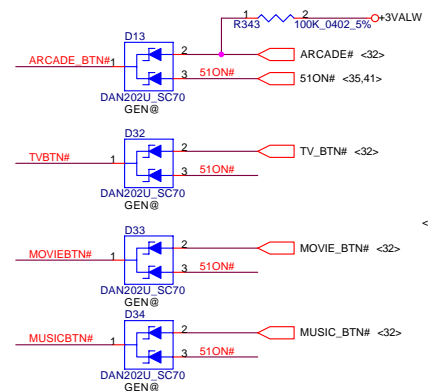
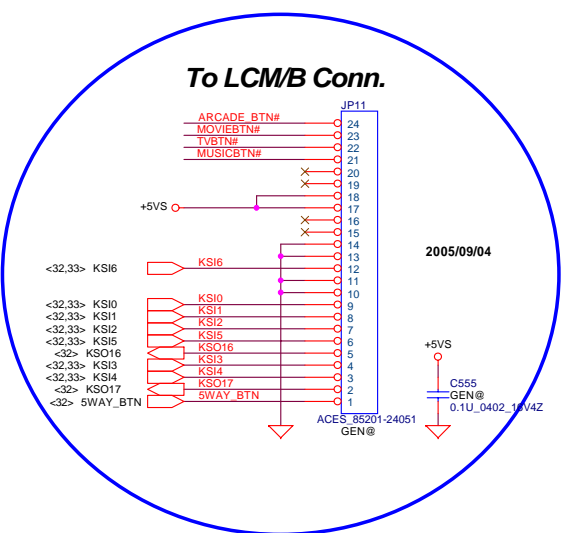


1MB ROM Socket



Remove @\* BOM structure 20060713

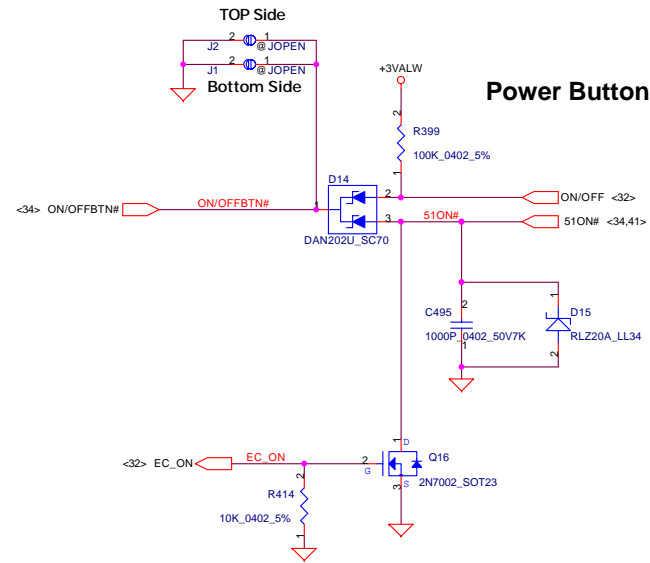
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Size B	Document Number	Rev G	401405		
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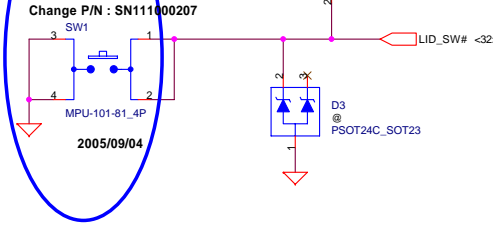
Geneva		Grapevine	
	KSO16	KSO17	
KSI0	VOL_UP	LEFT	
KSI1	RIGHT	VOL_DOWN	
KSI2	PLAY	ENTER	
KSI3	STOP		
KSI4	NEXT	VOL_UP	
KSI5	REV	VOL_DOWN	
KSI6		RECORD	ARCADE_TV

Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)

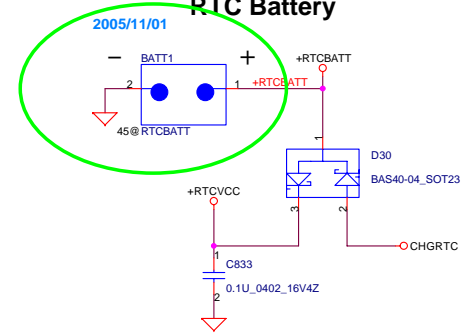
### ON/OFF switch



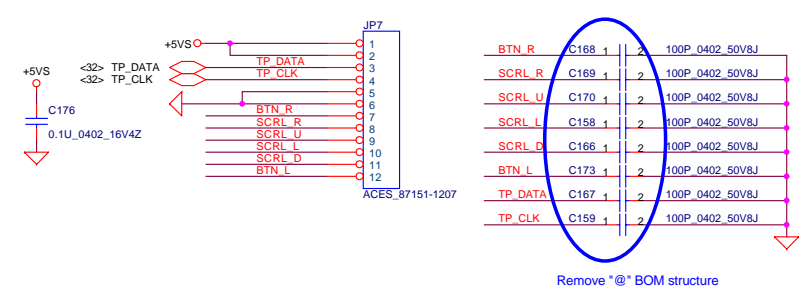
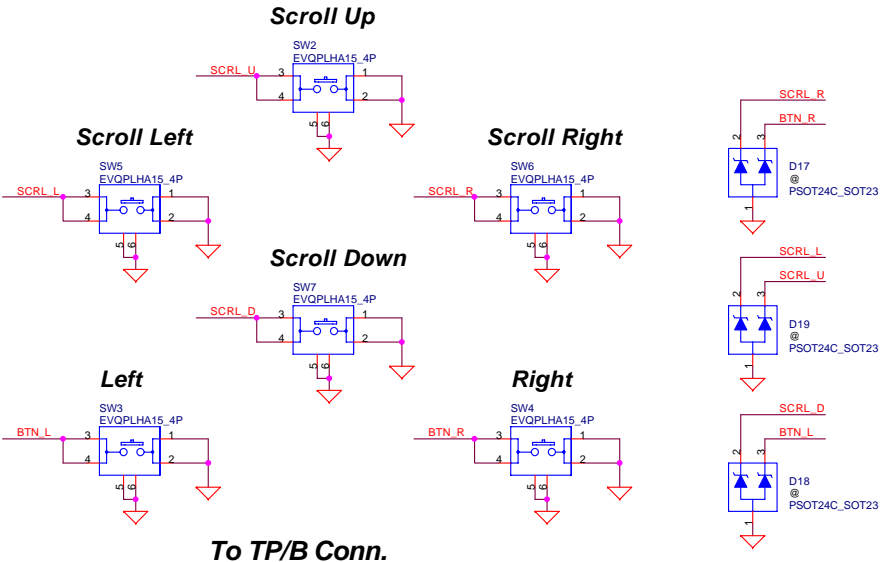
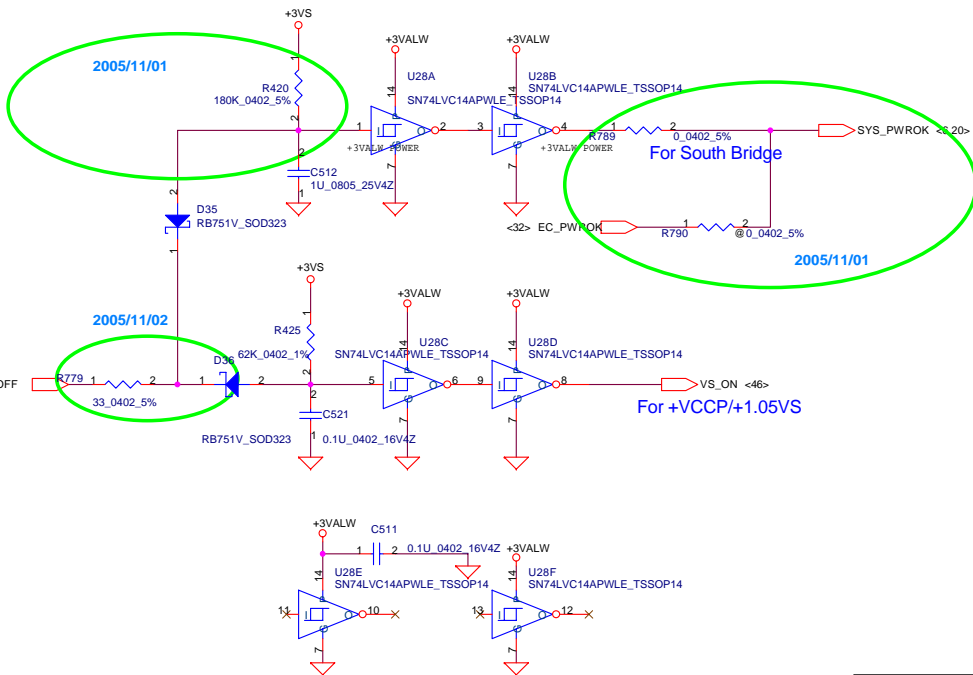
### Lid Switch



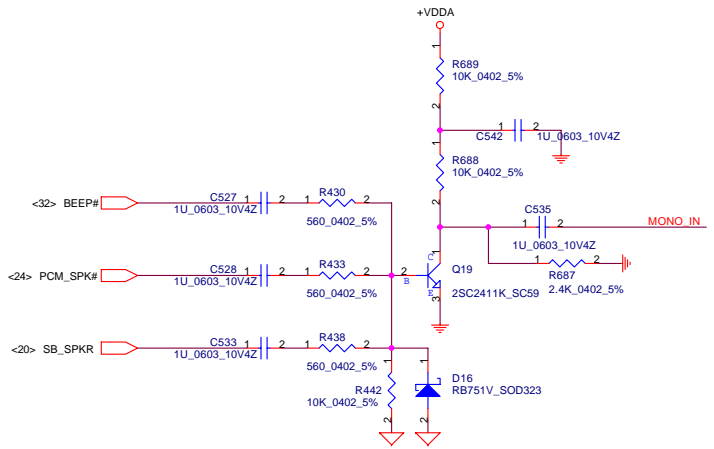
### RTC Battery



### Power ON Circuit



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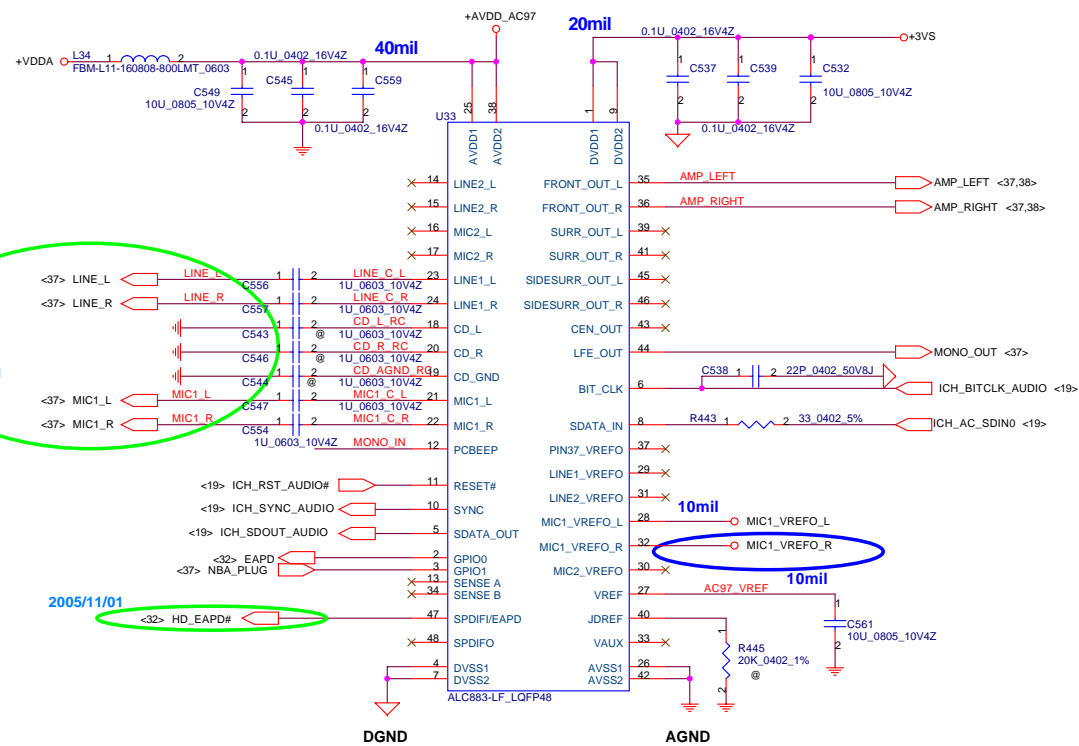


L32, L33  
Original: SM010014520  
New: SM010014500

28.7K for Module Design (VDDA = 4.702)

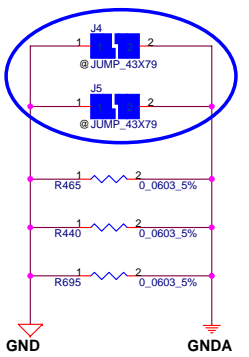
(output = 250 mA)

### HD Audio Codec



2005/11/01

2005/11/01

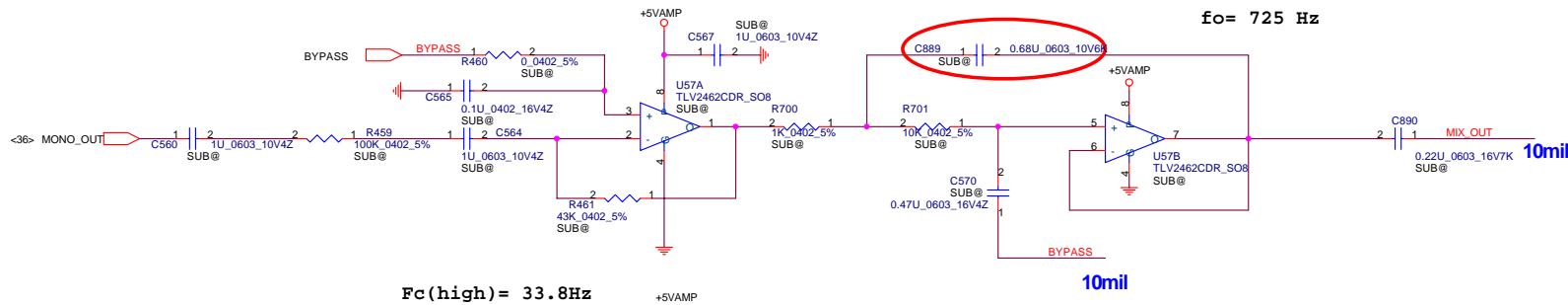


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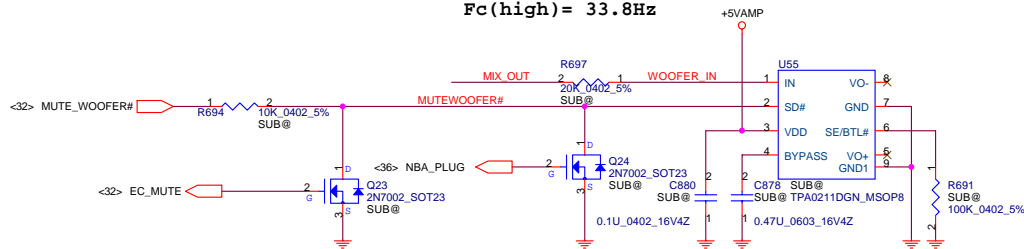
# Subwoofer

$f_o = 725 \text{ Hz}$

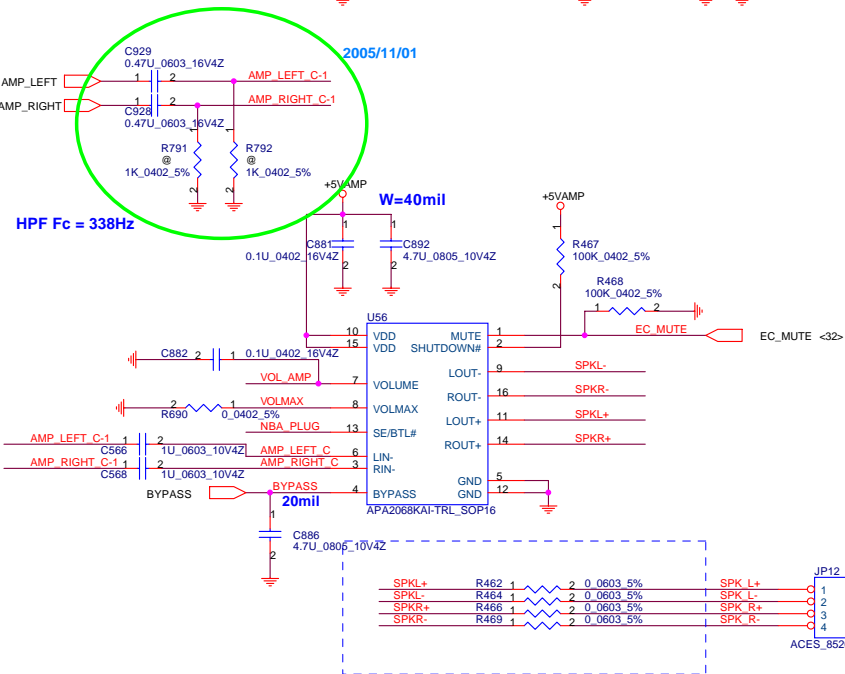


$F_c(\text{high}) = 33.8 \text{ Hz}$

10mil



HP Out JACK  
Original: DC230002H00  
New: DC230001G00

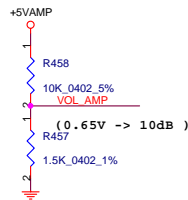


HPF  $F_c = 338 \text{ Hz}$

2005/11/01

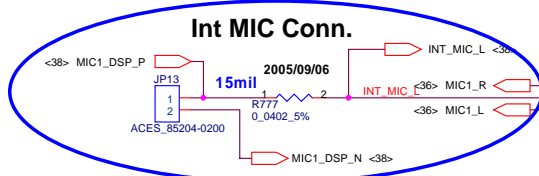
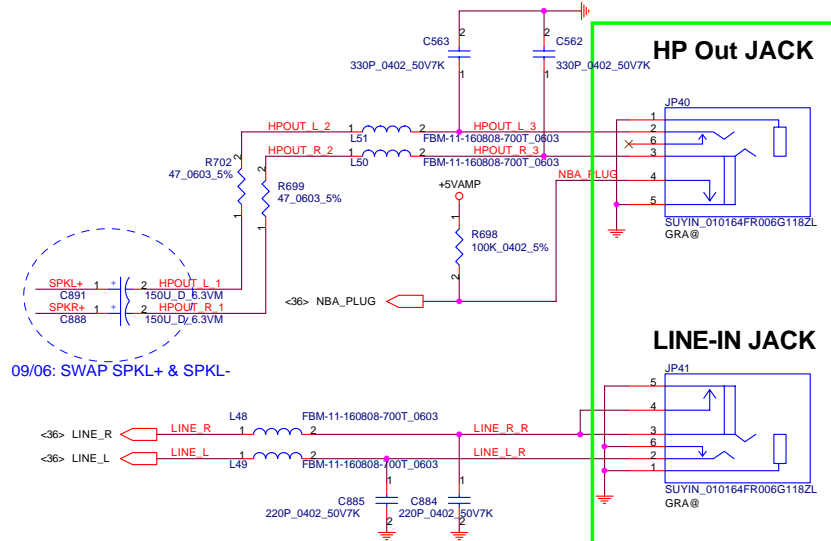
$W = 40 \text{ mil}$

20mil Speaker Conn.



(0.65V -> 10dB)

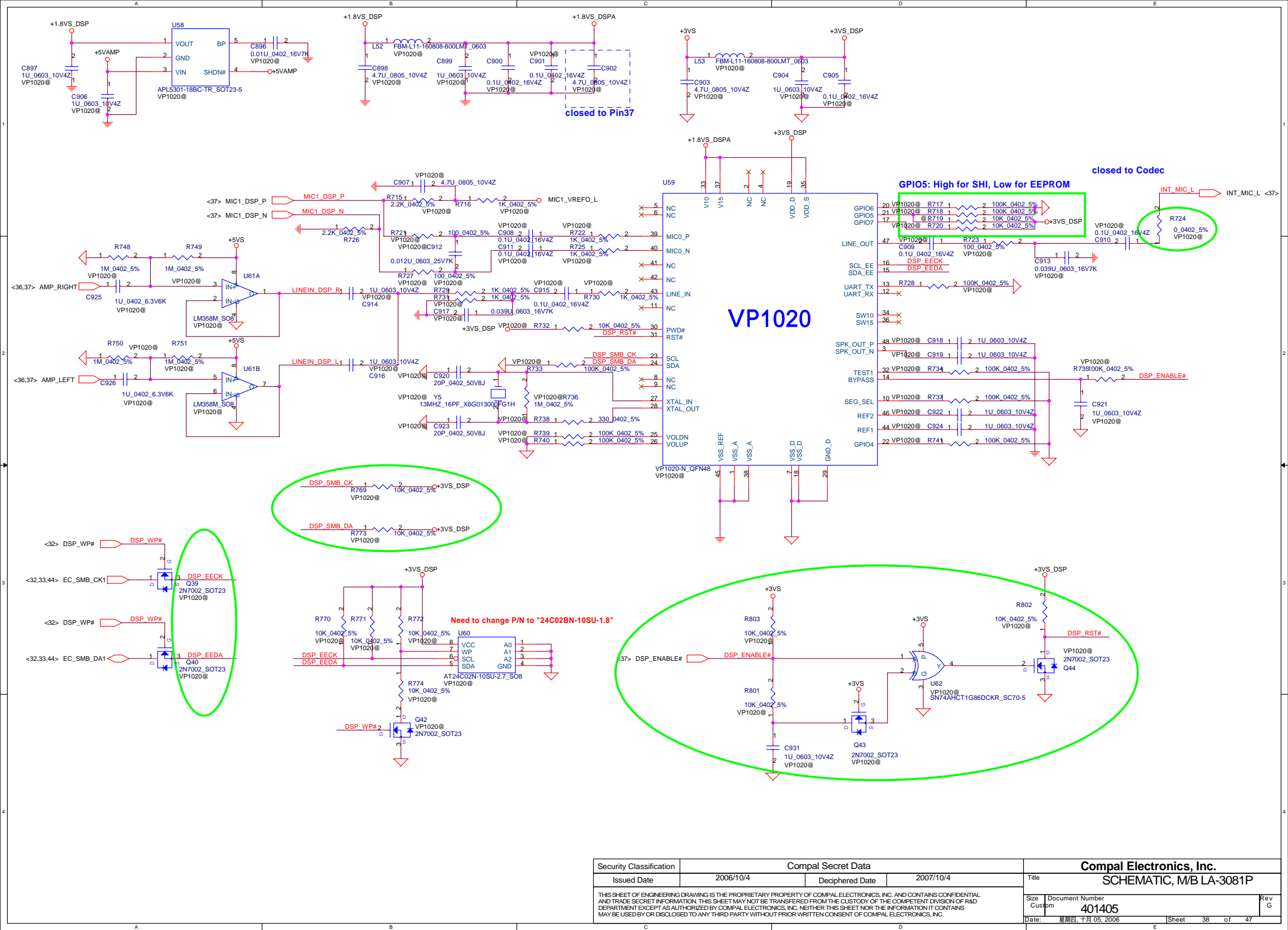
09/06: SWAP SPKL+ & SPKL-



Int MIC Conn.

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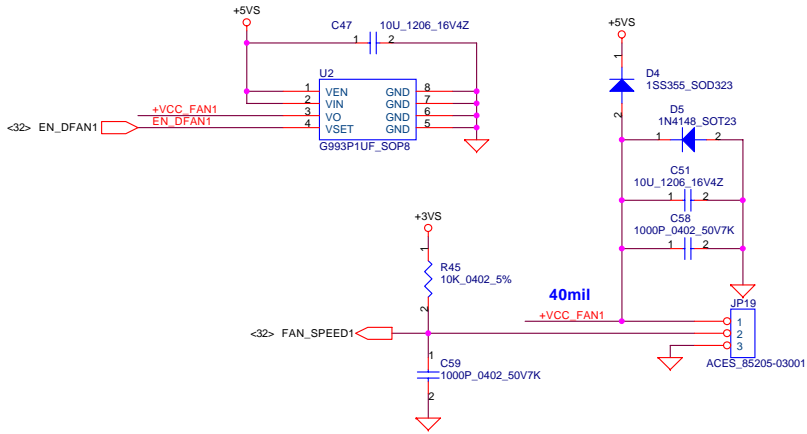


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		2007/10/4

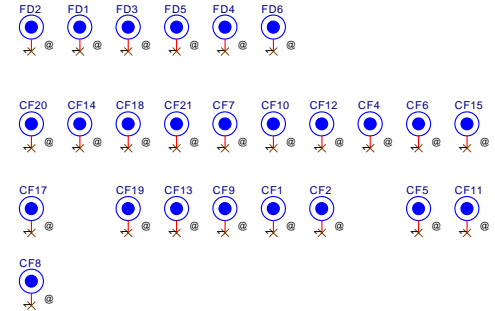
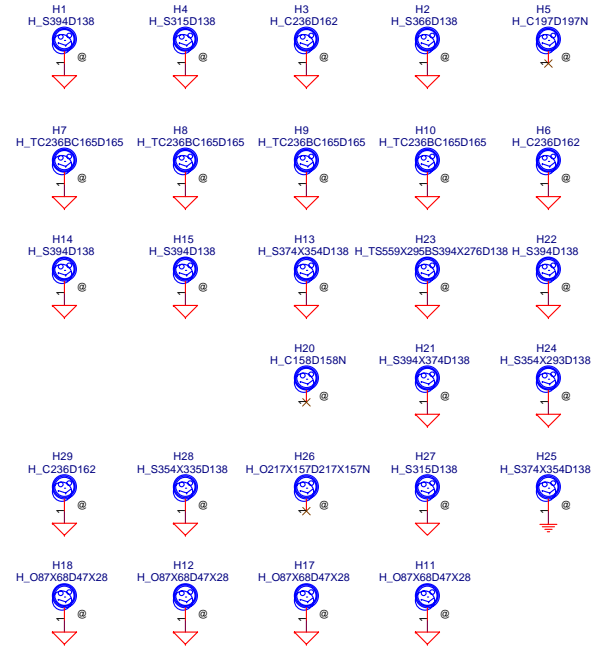
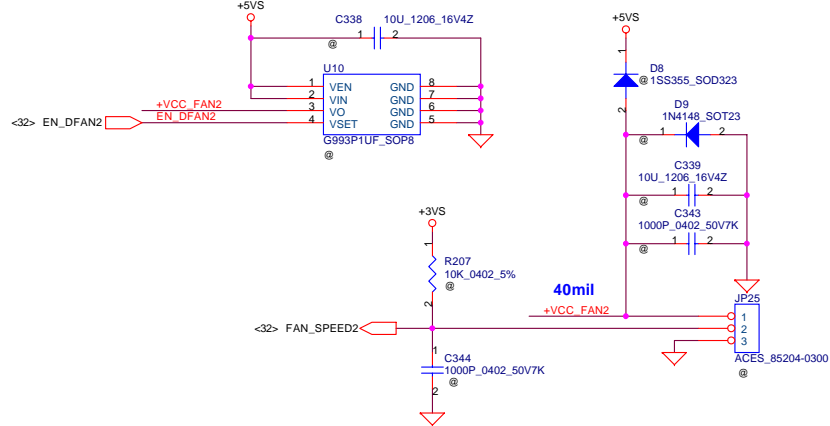
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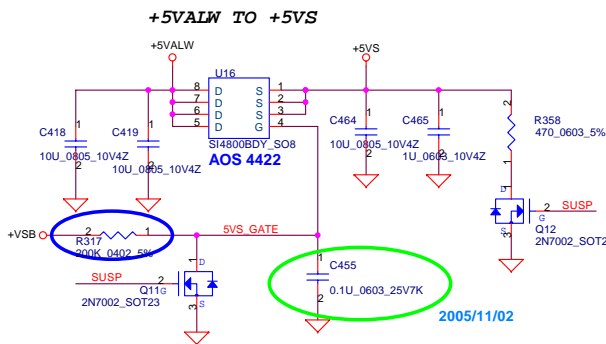
### FAN1 Conn



### FAN2 Conn

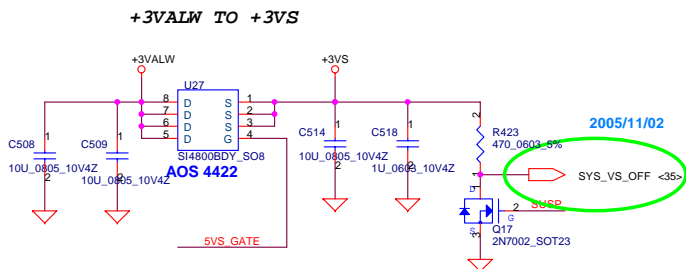
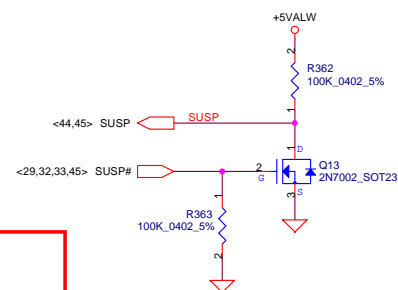
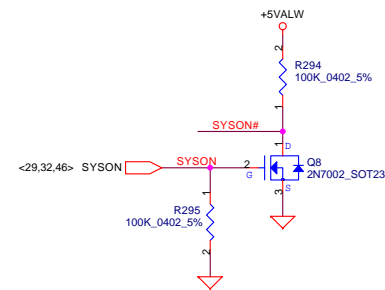
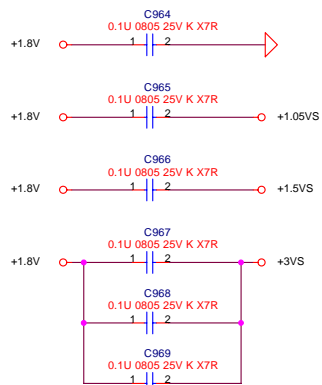


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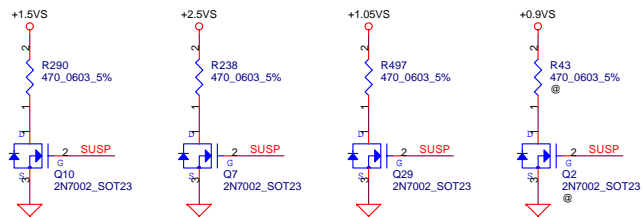
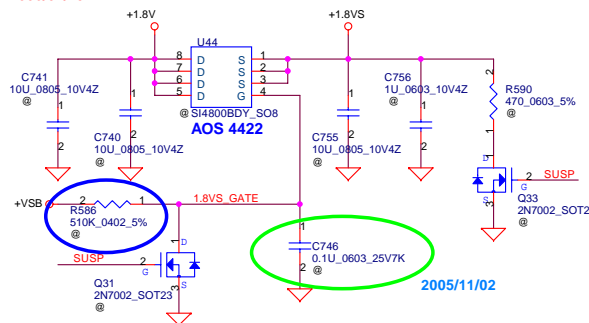
**For EMI Request to add:**

2006/7/05



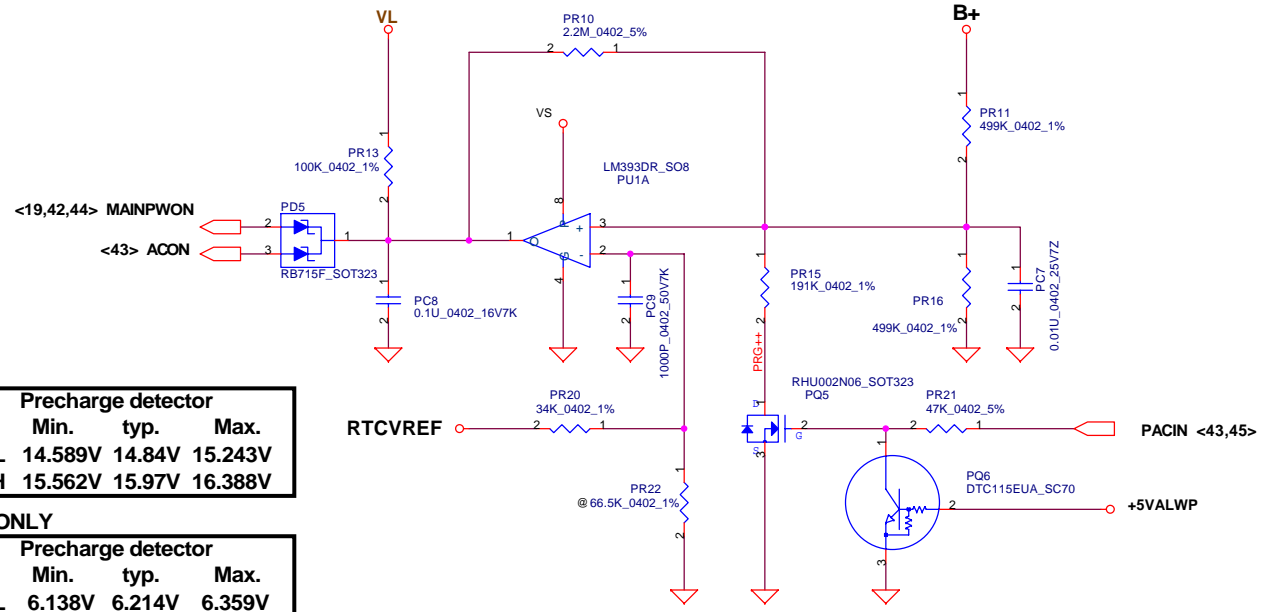
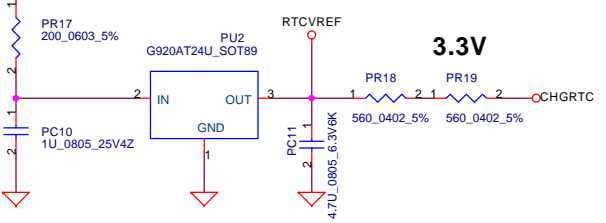
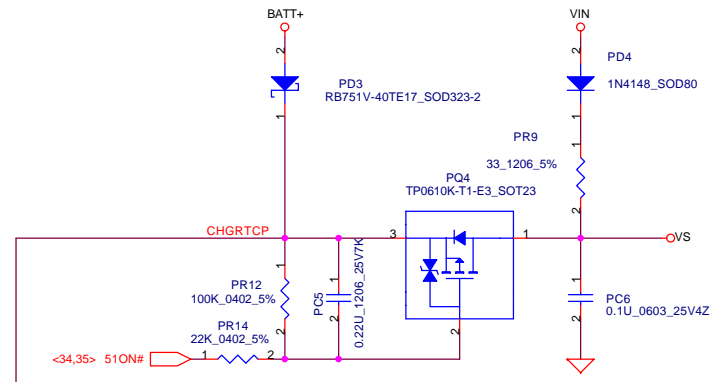
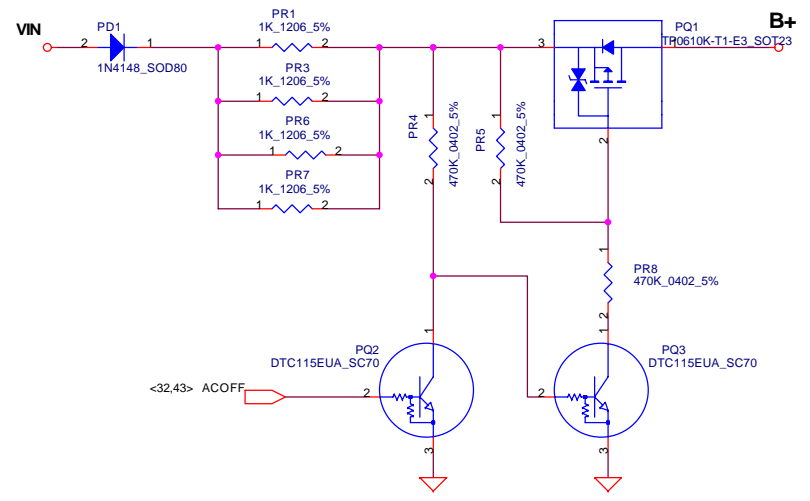
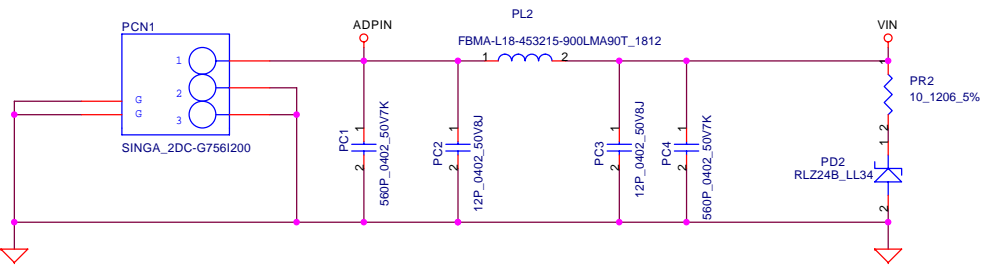
**+1.8V to +1.8VS**  
(change BOM structure to "@")

2006/04/19



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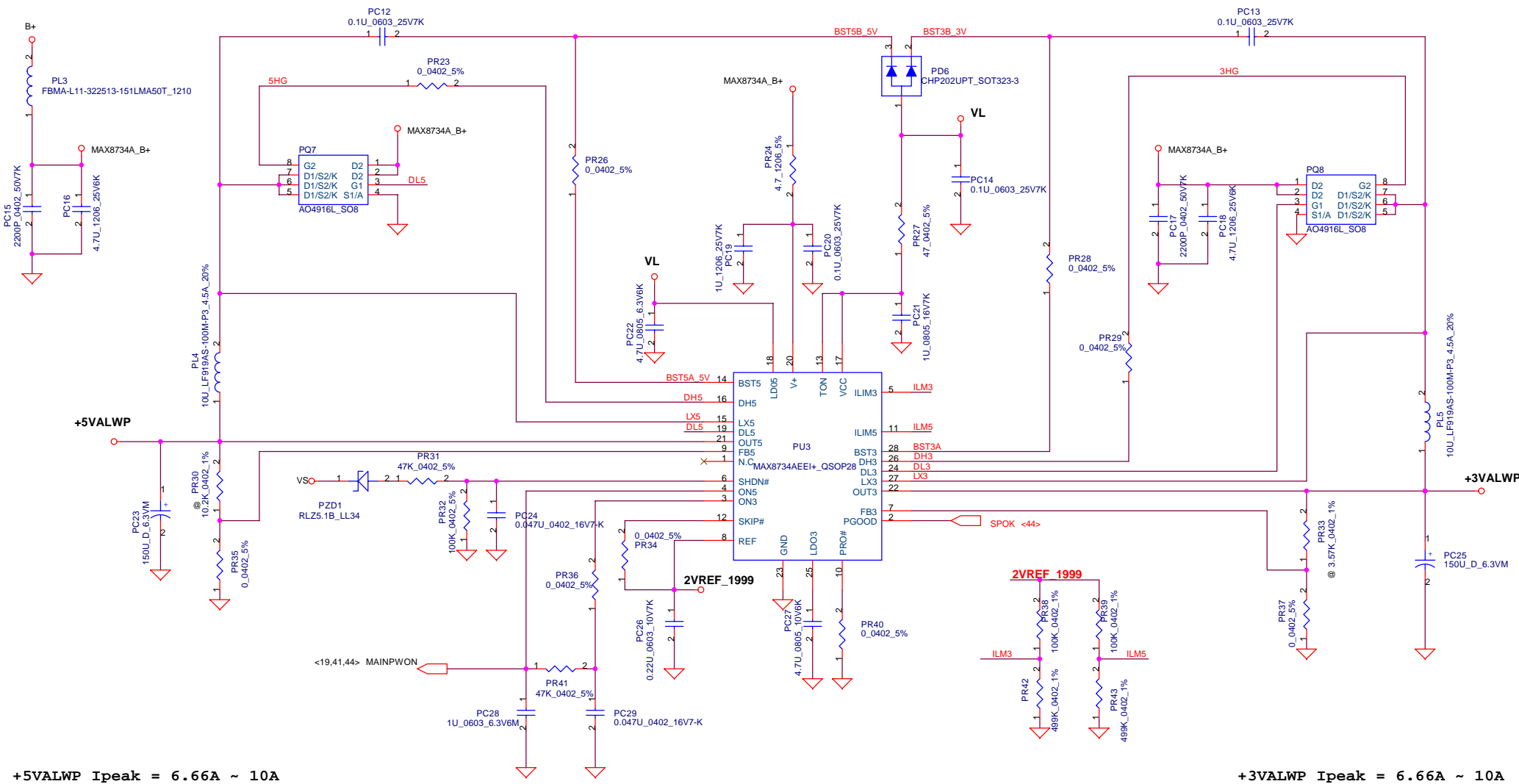


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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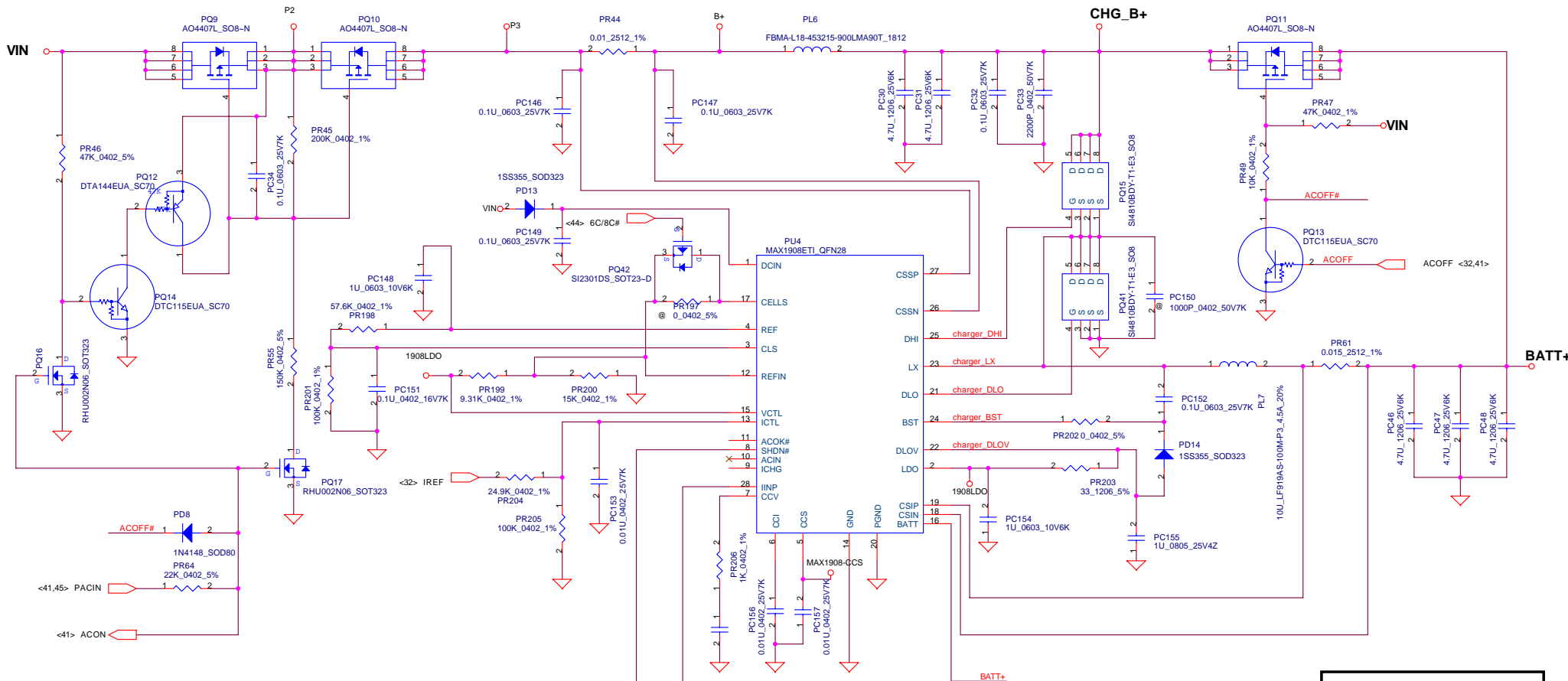


**+5VALWP Ipeak = 6.66A ~ 10A**

**+3VALWP Ipeak = 6.66A ~ 10A**

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I<sub>adp</sub>=0~4.74A(90W)



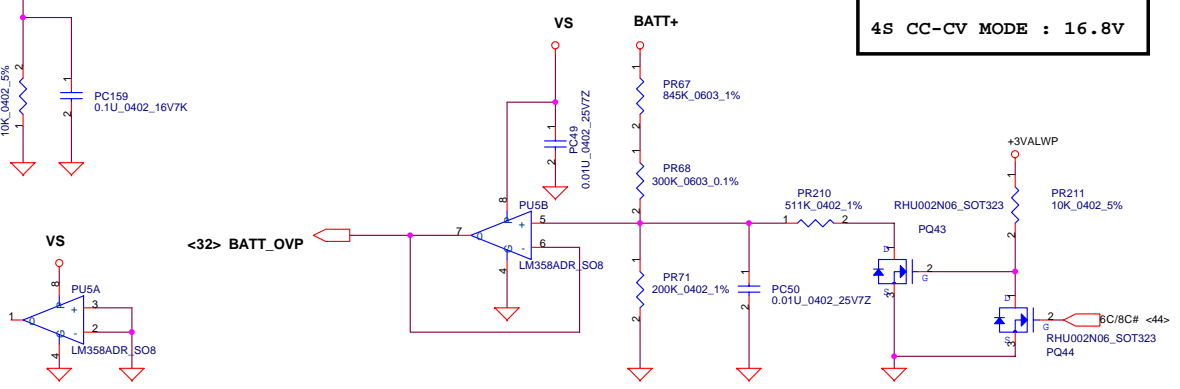
Charge voltage  
4S CC-CV MODE : 16.8V

LI-4S : 17.8V--BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

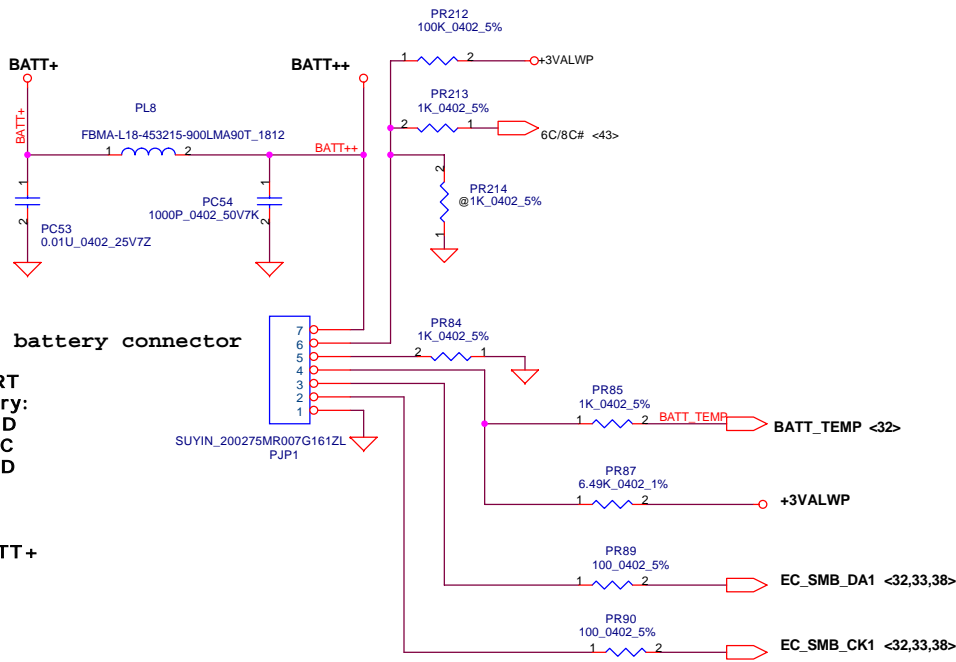
IREF=0.832\*Icharge  
IREF=0.73~3.3V

2P4S:4800mAh/cell  
0.8C=3.84A

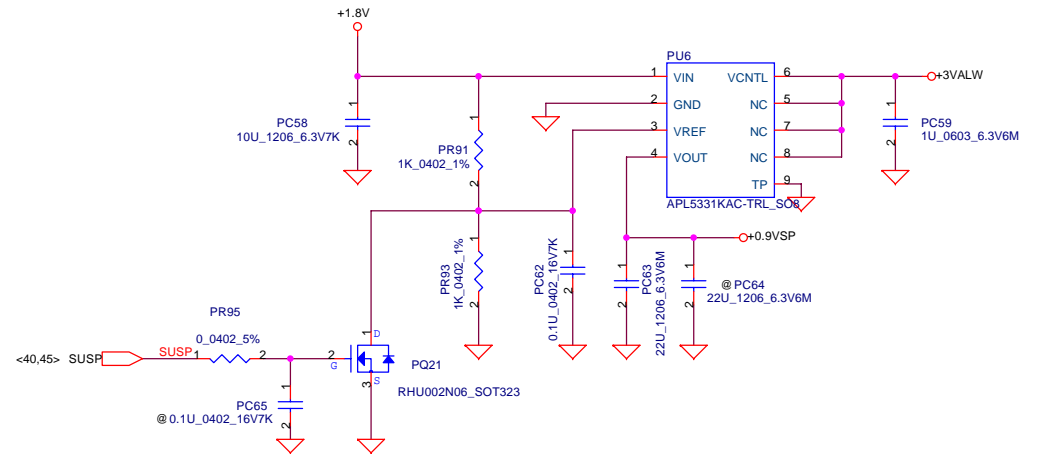
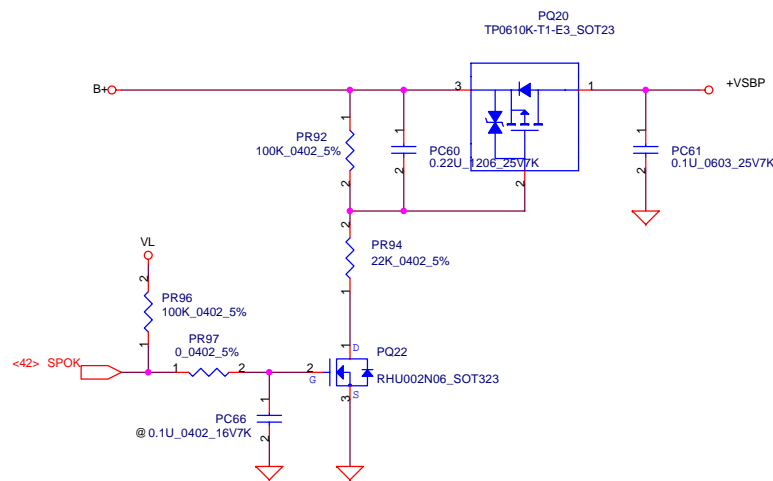
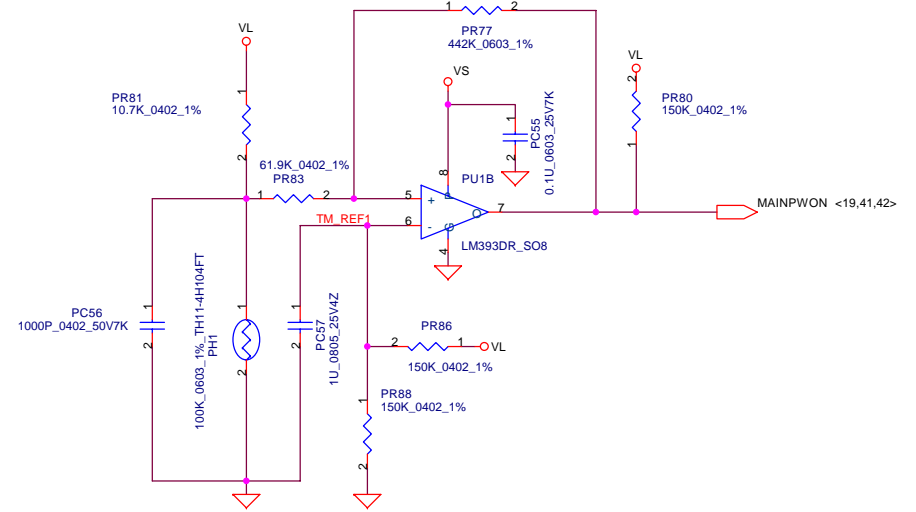
OVP voltage :  
LI-3S : 17.8V---BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+



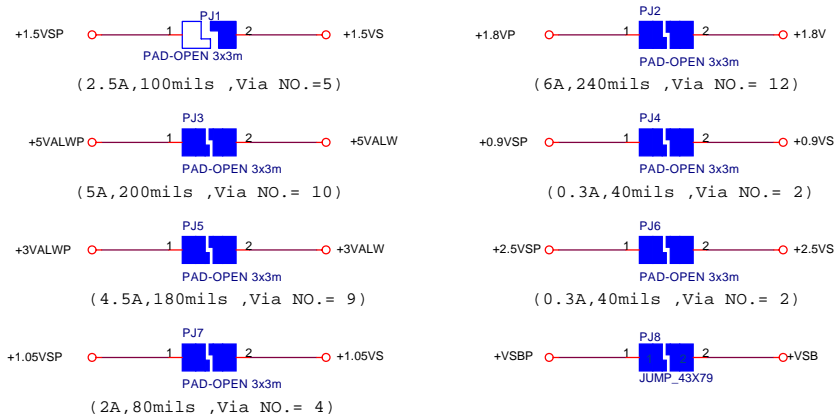
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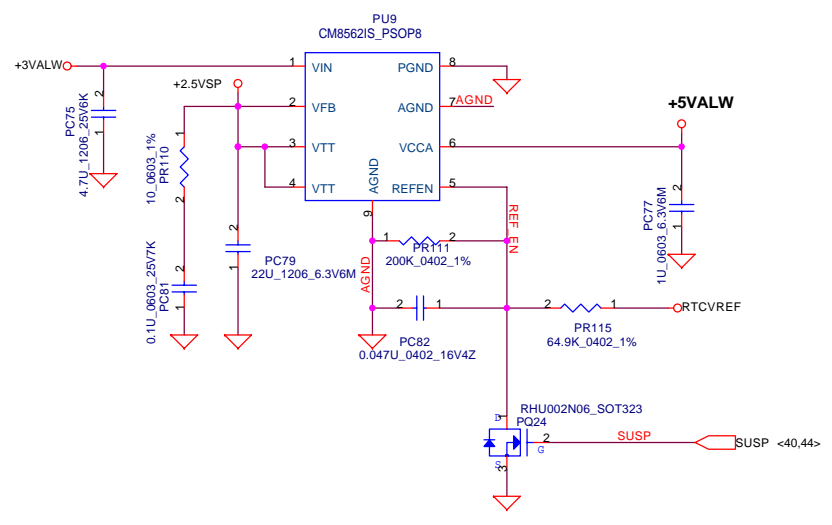
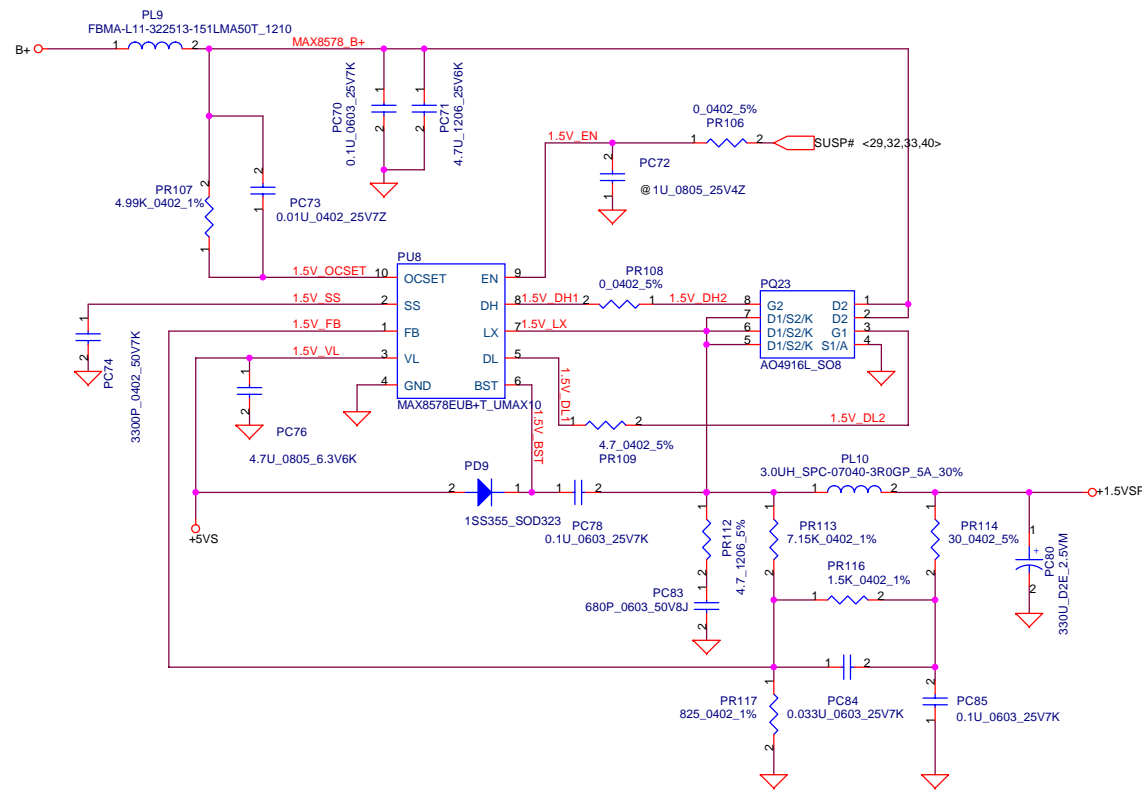
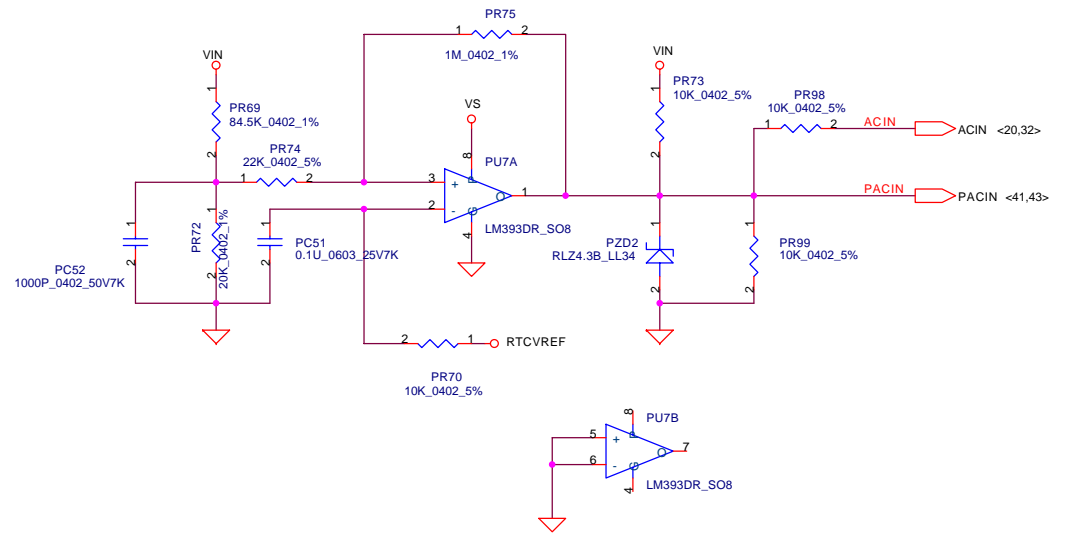
**PH1 under CPU botten side :**  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C



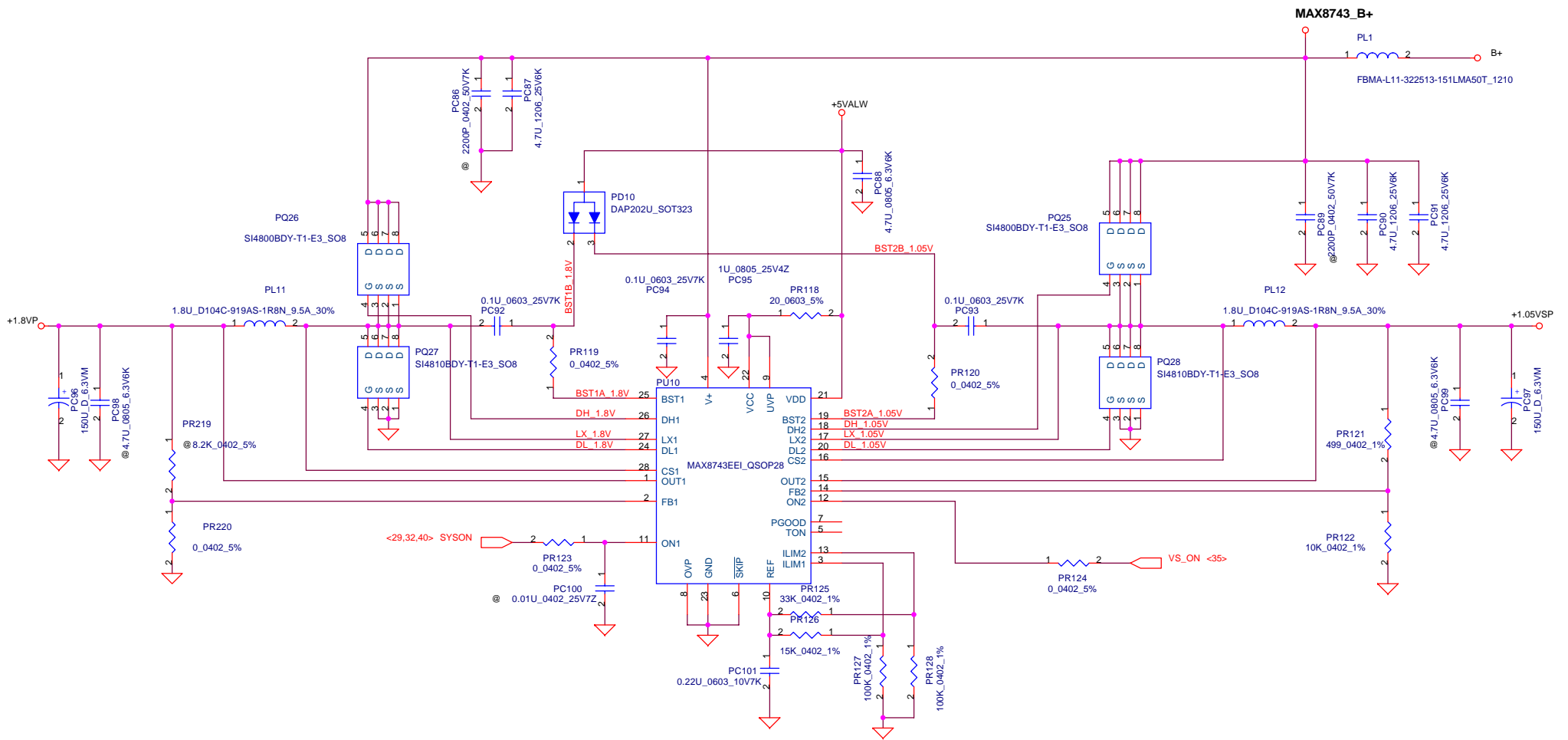
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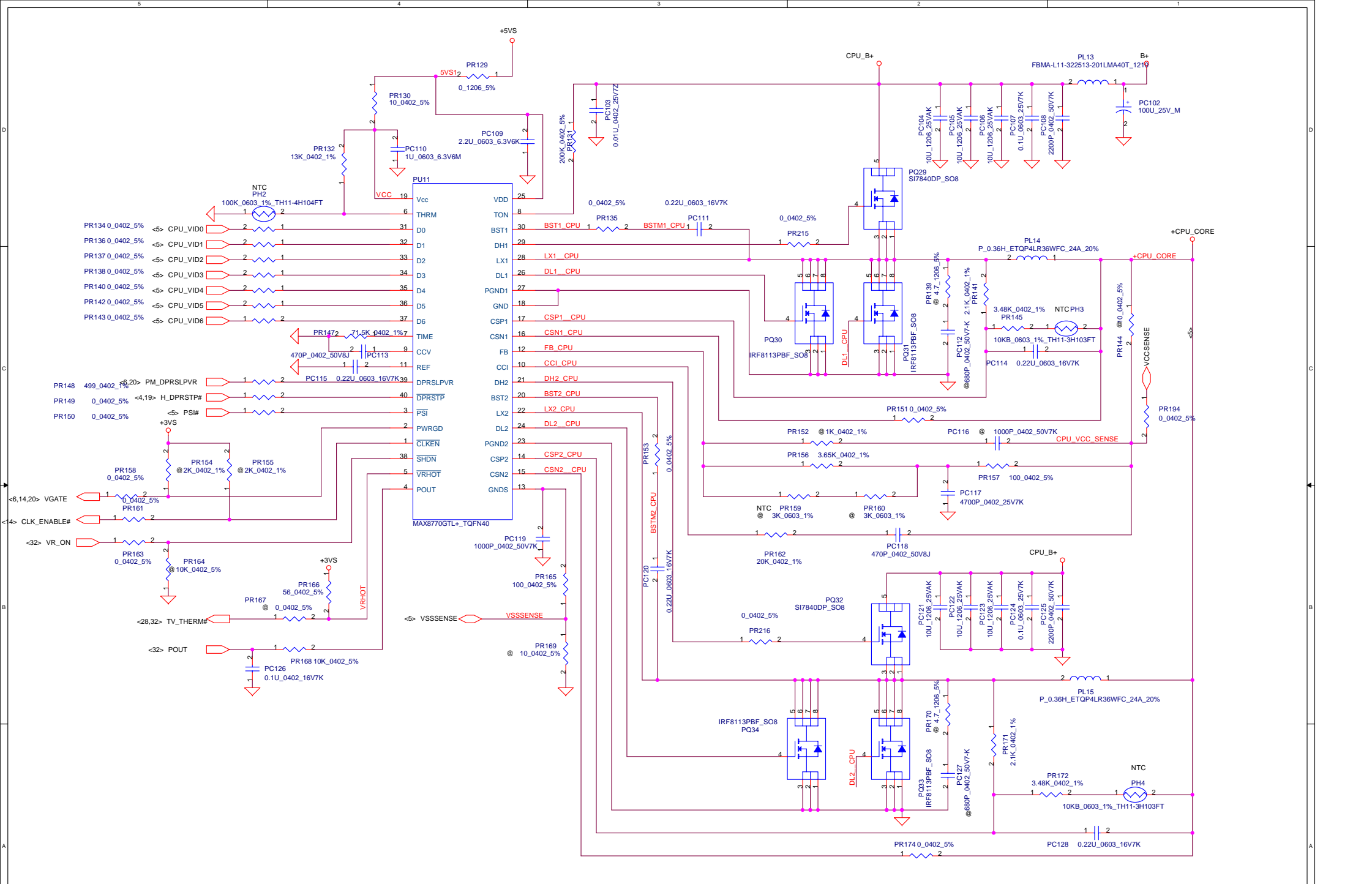
**Vin Detector**  
17.90V/17.24V



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