

MODEL NAME : *PAP00*  
PCB NO : *LA-6961P ( DA\*\*\*\*\* )*  
BOM P/N : *TBD*

# Dell/Compal Confidential

## Schematic Document

Phantom (Huron River)

Sandy Bridge (BGA1023) + Cougar Point (SFF)

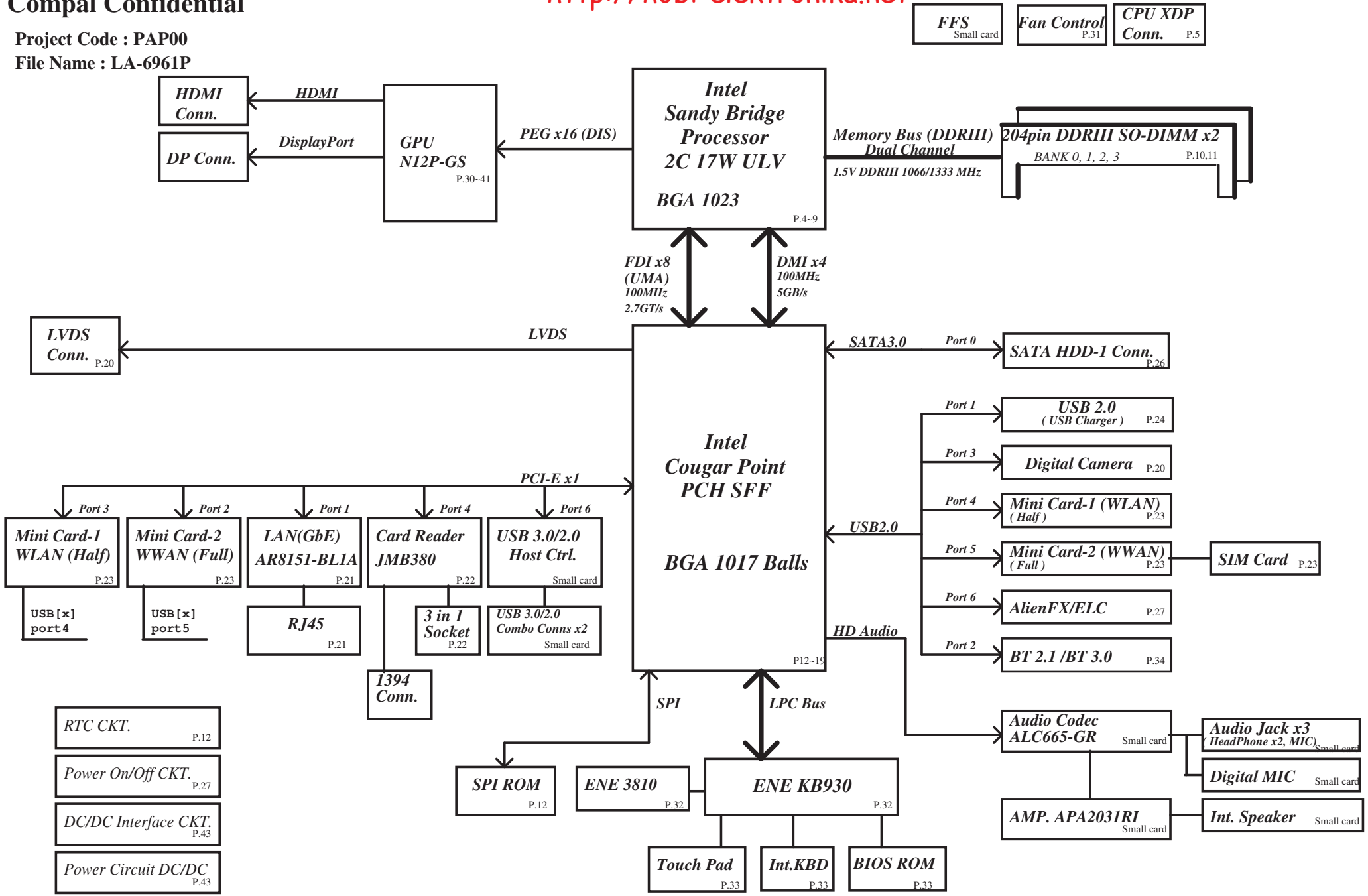
DISCRETE VGA N12P-GS (optimus)

2010-11-29

Rev: 0.4

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Project Code : PAP00  
File Name : LA-6961P



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Issued Date	2010/06/10	Deciphered Date	2011/07/06	Title	PCH (6/8) PWR	
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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>AD_BID min</sub>	V <sub>AD_BID typ</sub>	V <sub>AD_BID max</sub>	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

<http://hobi-elektronika.net>

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

PCH	USB PORT#	DESTINATION
	0	None
	1	JUSB1 (Ext Left Side)
	2	Bluetooth
	3	CAMERA
	4	JMINI1 (WLAN)
	5	JMINI2 (WWAN)
	6	ELC
	7	None
	8	None
	9	None
	10	None
	11	None
	12	None
13	None	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	FFS	VGA Thermal Sensor	SMSC
EC_SMB_CK1 EC_SMB_DA1	KB930			V					
EC_SMB_CK2 EC_SMB_DA2	KB930								
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH	V	V			V		V	V
MEM_SMBCLK MEM_SMBDATA	PCH				V		V		

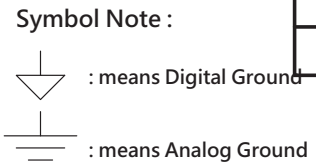


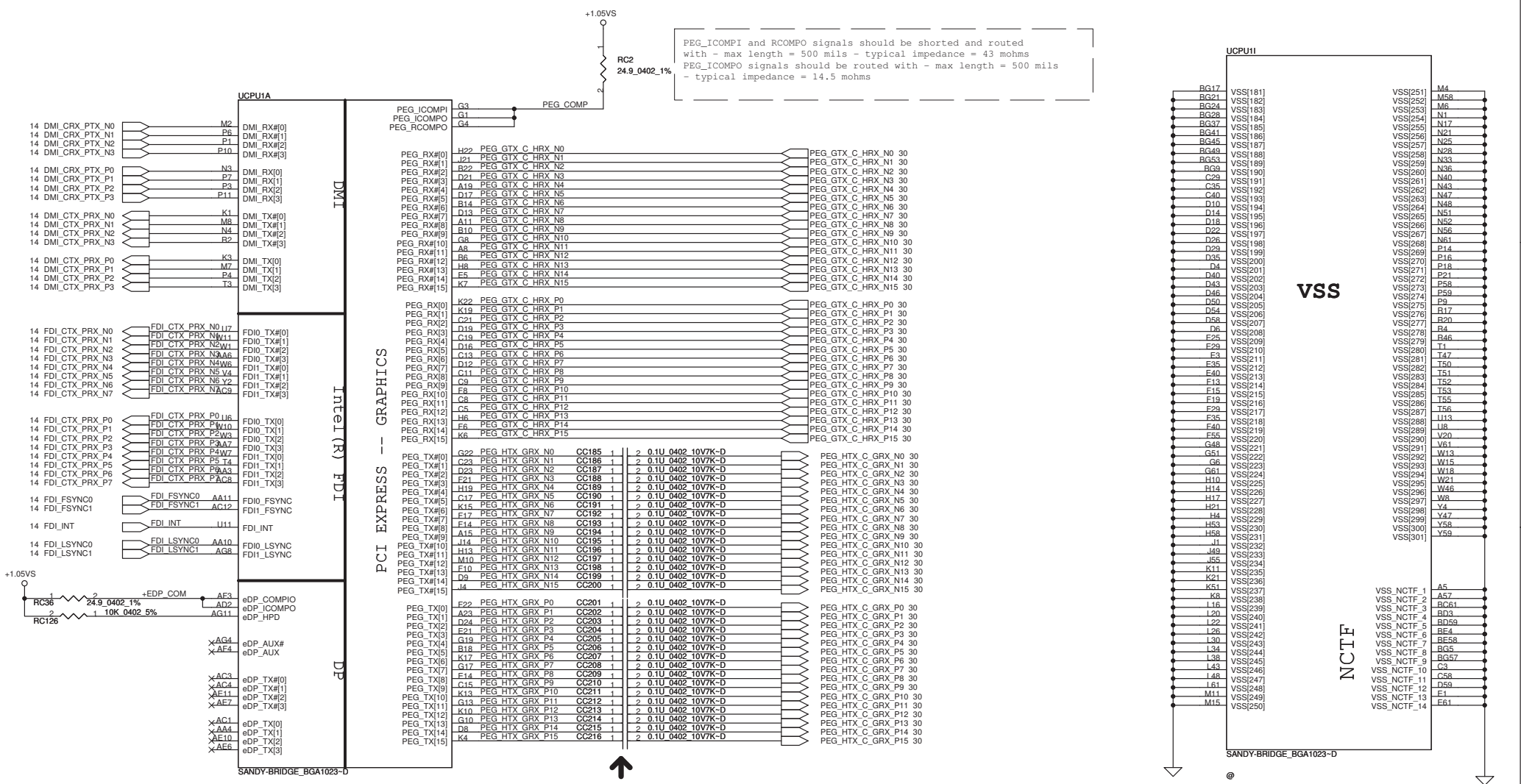
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	None
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER and 1394
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

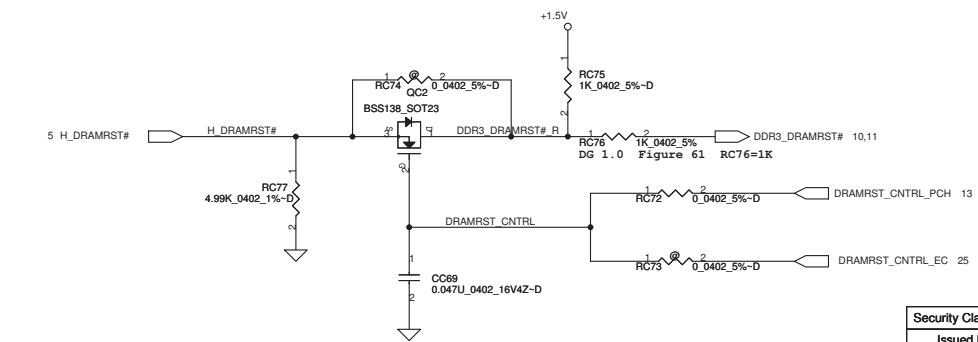
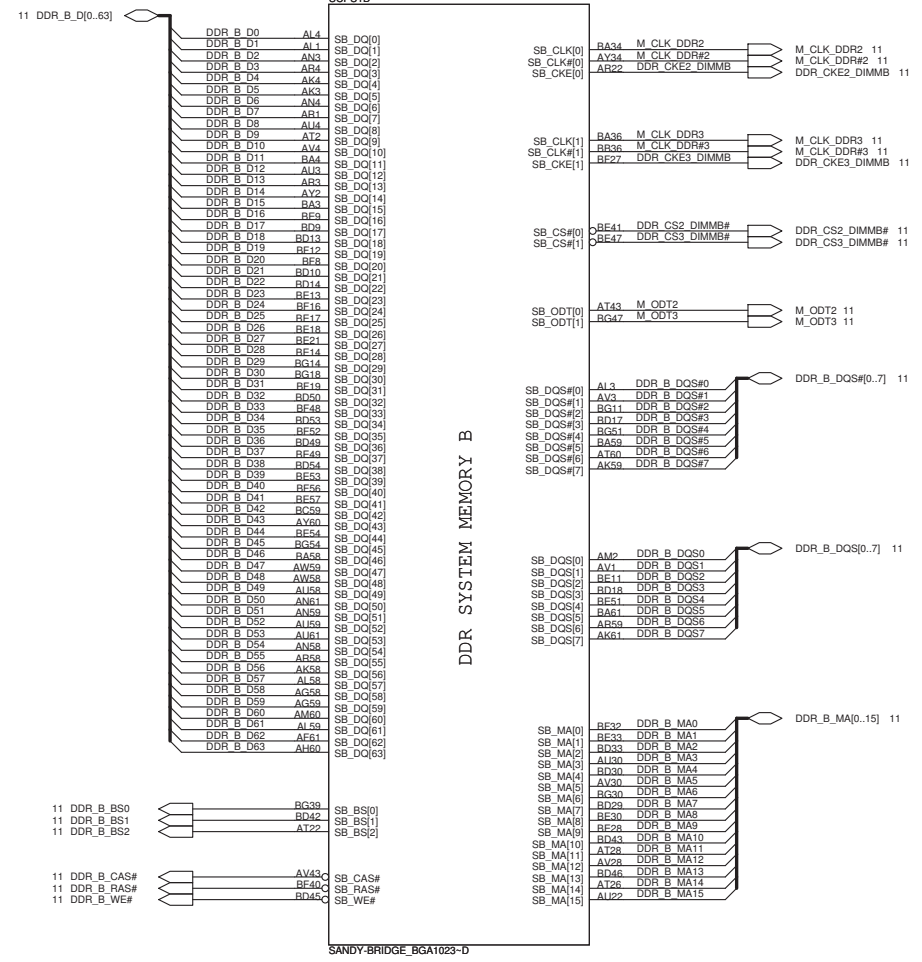
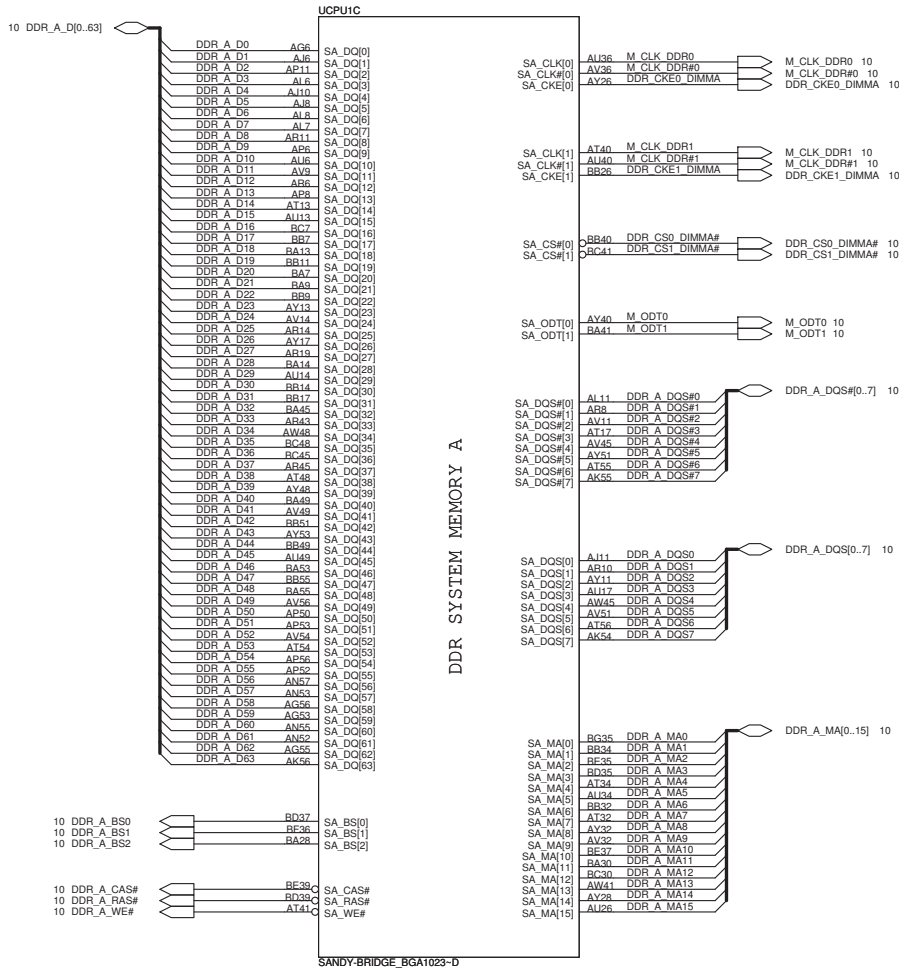




Typ-suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

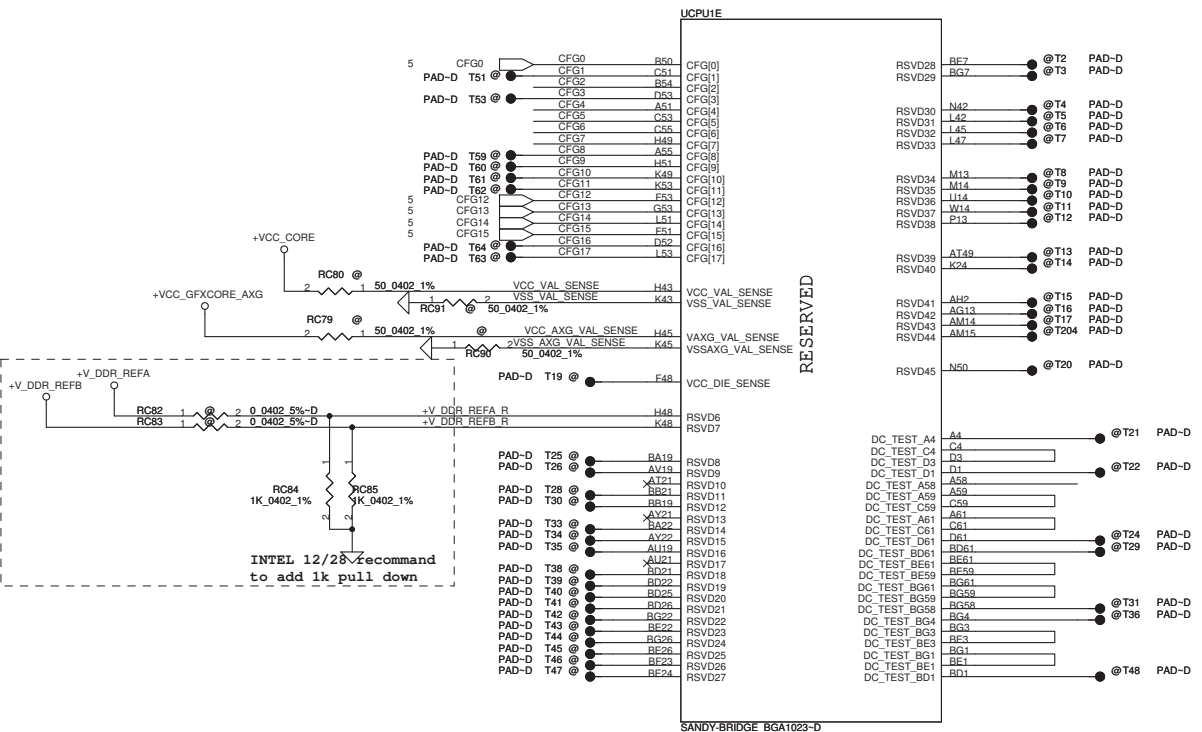
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Compal Electronics, Inc.			PROCESSOR(1/6) DMI,FDI,PEG	
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Issued Date	2010/07/06	Deciphered Date	2011/07/06	PROCESSOR(3/6) DDRIII
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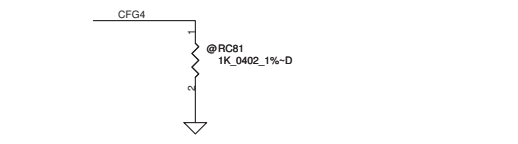
CFG Straps for Processor



**PEG Static Lane Reversal - CFG2 is for the 16x**

CFG2

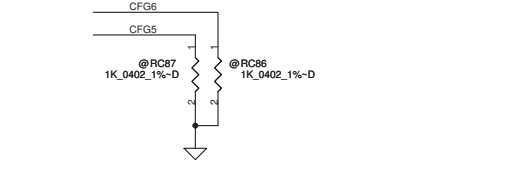
- \*1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed



**Display Port Presence Strap**

CFG4

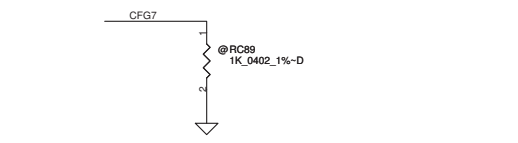
- \*1 : Disabled; No Physical Display Port attached to Embedded Display Port
- 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



**PCIe Port Bifurcation Straps**

CFG[6:5]

- \*11: (Default) x16 - Device 1 functions 1 and 2 disabled
- 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
- 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
- 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

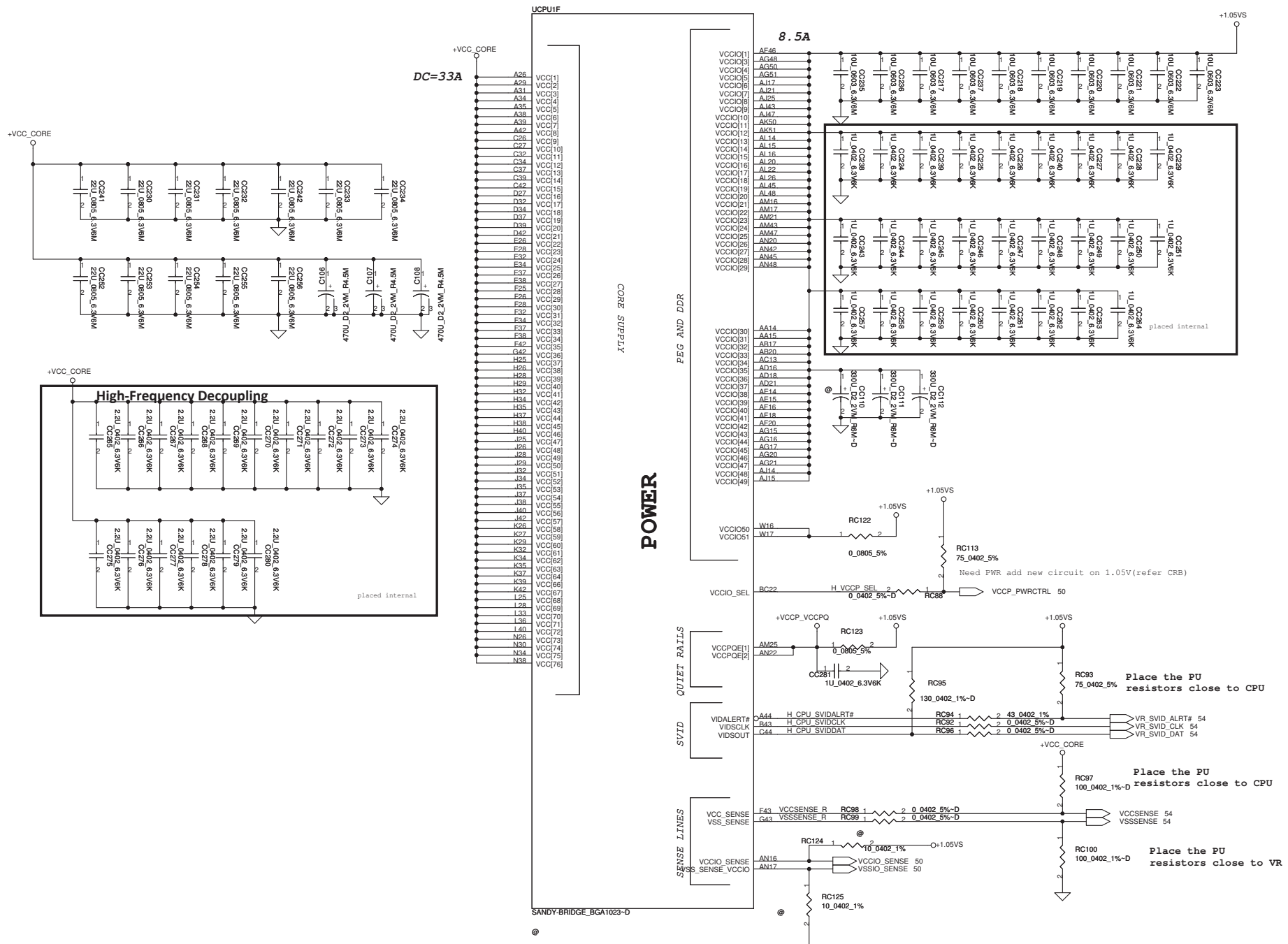


**PEG DEFER TRAINING**

CFG7

- \*1: (Default) PEG Train immediately following xRESET# de assertion
- 0: PEG Wait for BIOS for training

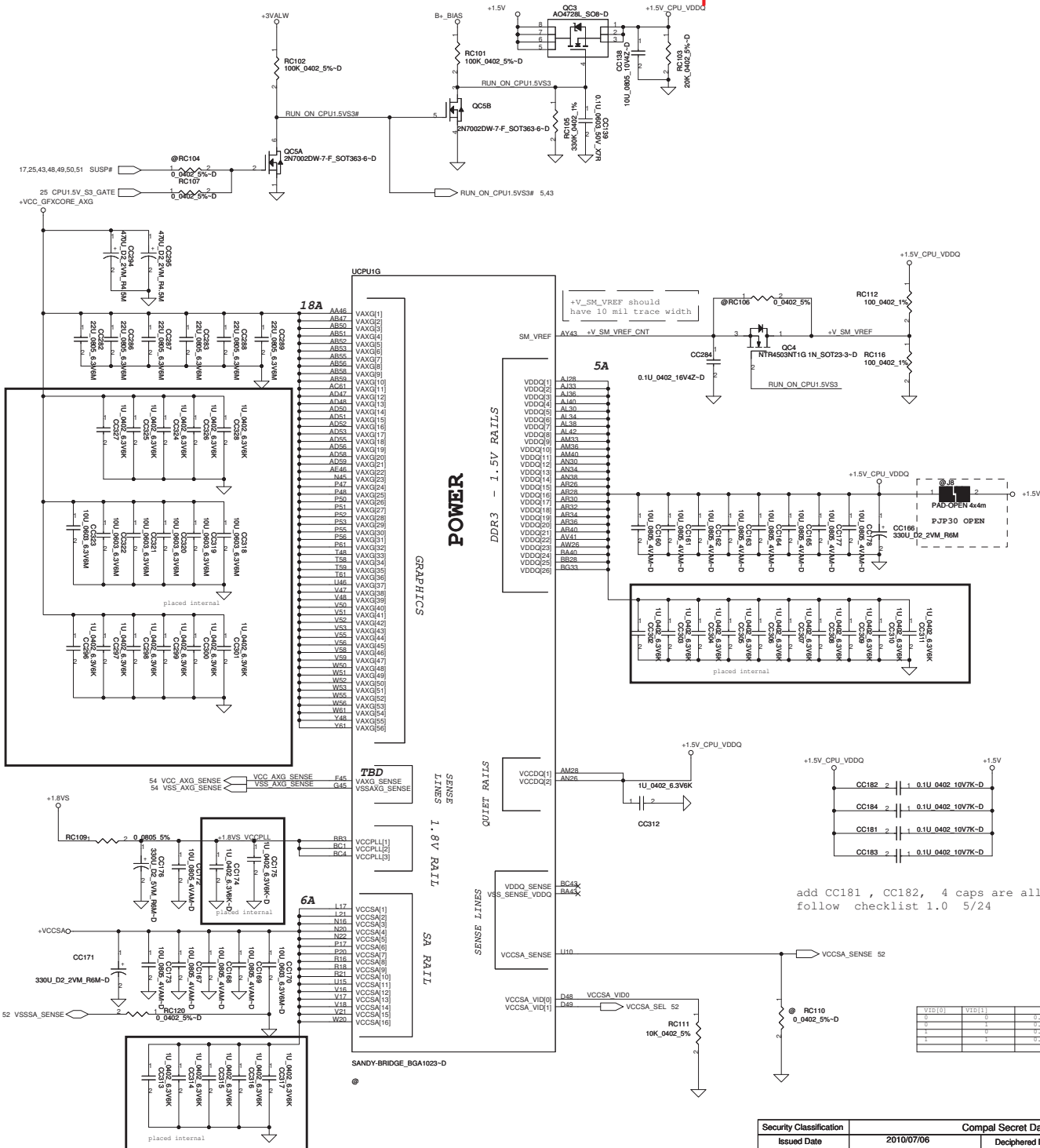




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**+1.5V\_CPU\_VDDQ Source**



**UCPU1H**

A11	VSS[11]	AM38
A17	VSS[2]	AM4
A21	VSS[3]	AM44
VSS[4]	VSS[4]	AM45
A28	VSS[5]	AM43
VSS[6]	VSS[6]	AM58
A37	VSS[7]	AN1
AM1	VSS[8]	AN21
VSS[9]	VSS[9]	AN28
AM4	VSS[10]	AN29
VSS[100]	VSS[10]	AN36
AM10	VSS[11]	AN38
VSS[102]	VSS[11]	AN40
AM13	VSS[13]	AN43
VSS[104]	VSS[14]	AN47
AM50	VSS[15]	AN50
VSS[106]	VSS[16]	AN54
VSS[107]	VSS[17]	AN59
AM51	VSS[18]	AN60
VSS[109]	VSS[19]	AN62
AM56	VSS[20]	AN65
VSS[110]	VSS[21]	AN67
AM6	VSS[22]	AN68
VSS[112]	VSS[22]	AN71
AM16	VSS[23]	AN72
VSS[113]	VSS[23]	AN73
AM8	VSS[24]	AN74
VSS[114]	VSS[24]	AN75
AM20	VSS[25]	AN76
VSS[115]	VSS[25]	AN77
AM26	VSS[26]	AN78
VSS[116]	VSS[26]	AN79
AM32	VSS[27]	AN80
VSS[117]	VSS[27]	AN81
AM37	VSS[28]	AN82
VSS[118]	VSS[28]	AN83
AM42	VSS[29]	AN84
VSS[119]	VSS[29]	AN85
AM47	VSS[30]	AN86
VSS[120]	VSS[30]	AN87
AM52	VSS[31]	AN88
VSS[121]	VSS[31]	AN89
AM57	VSS[32]	AN90
VSS[122]	VSS[32]	AN91
AM62	VSS[33]	AN92
VSS[123]	VSS[33]	AN93
AM67	VSS[34]	AN94
VSS[124]	VSS[34]	AN95
AM72	VSS[35]	AN96
VSS[125]	VSS[35]	AN97
AM77	VSS[36]	AN98
VSS[126]	VSS[36]	AN99
AM82	VSS[37]	AN100
VSS[127]	VSS[37]	AN101
AM87	VSS[38]	AN102
VSS[128]	VSS[38]	AN103
AM92	VSS[39]	AN104
VSS[129]	VSS[39]	AN105
AM97	VSS[40]	AN106
VSS[130]	VSS[40]	AN107
AM102	VSS[41]	AN108
VSS[131]	VSS[41]	AN109
AM107	VSS[42]	AN110
VSS[132]	VSS[42]	AN111
AM112	VSS[43]	AN112
VSS[133]	VSS[43]	AN113
AM117	VSS[44]	AN114
VSS[134]	VSS[44]	AN115
AM122	VSS[45]	AN116
VSS[135]	VSS[45]	AN117
AM127	VSS[46]	AN118
VSS[136]	VSS[46]	AN119
AM132	VSS[47]	AN120
VSS[137]	VSS[47]	AN121
AM137	VSS[48]	AN122
VSS[138]	VSS[48]	AN123
AM142	VSS[49]	AN124
VSS[139]	VSS[49]	AN125
AM147	VSS[50]	AN126
VSS[140]	VSS[50]	AN127
AM152	VSS[51]	AN128
VSS[141]	VSS[51]	AN129
AM157	VSS[52]	AN130
VSS[142]	VSS[52]	AN131
AM162	VSS[53]	AN132
VSS[143]	VSS[53]	AN133
AM167	VSS[54]	AN134
VSS[144]	VSS[54]	AN135
AM172	VSS[55]	AN136
VSS[145]	VSS[55]	AN137
AM177	VSS[56]	AN138
VSS[146]	VSS[56]	AN139
AM182	VSS[57]	AN140
VSS[147]	VSS[57]	AN141
AM187	VSS[58]	AN142
VSS[148]	VSS[58]	AN143
AM192	VSS[59]	AN144
VSS[149]	VSS[59]	AN145
AM197	VSS[60]	AN146
VSS[150]	VSS[60]	AN147
AM202	VSS[61]	AN148
VSS[151]	VSS[61]	AN149
AM207	VSS[62]	AN150
VSS[152]	VSS[62]	AN151
AM212	VSS[63]	AN152
VSS[153]	VSS[63]	AN153
AM217	VSS[64]	AN154
VSS[154]	VSS[64]	AN155
AM222	VSS[65]	AN156
VSS[155]	VSS[65]	AN157
AM227	VSS[66]	AN158
VSS[156]	VSS[66]	AN159
AM232	VSS[67]	AN160
VSS[157]	VSS[67]	AN161
AM237	VSS[68]	AN162
VSS[158]	VSS[68]	AN163
AM242	VSS[69]	AN164
VSS[159]	VSS[69]	AN165
AM247	VSS[70]	AN166
VSS[160]	VSS[70]	AN167
AM252	VSS[71]	AN168
VSS[161]	VSS[71]	AN169
AM257	VSS[72]	AN170
VSS[162]	VSS[72]	AN171
AM262	VSS[73]	AN172
VSS[163]	VSS[73]	AN173
AM267	VSS[74]	AN174
VSS[164]	VSS[74]	AN175
AM272	VSS[75]	AN176
VSS[165]	VSS[75]	AN177
AM277	VSS[76]	AN178
VSS[166]	VSS[76]	AN179
AM282	VSS[77]	AN180
VSS[167]	VSS[77]	AN181
AM287	VSS[78]	AN182
VSS[168]	VSS[78]	AN183
AM292	VSS[79]	AN184
VSS[169]	VSS[79]	AN185
AM297	VSS[80]	AN186
VSS[170]	VSS[80]	AN187
AM302	VSS[81]	AN188
VSS[171]	VSS[81]	AN189
AM307	VSS[82]	AN190
VSS[172]	VSS[82]	AN191
AM312	VSS[83]	AN192
VSS[173]	VSS[83]	AN193
AM317	VSS[84]	AN194
VSS[174]	VSS[84]	AN195
AM322	VSS[85]	AN196
VSS[175]	VSS[85]	AN197
AM327	VSS[86]	AN198
VSS[176]	VSS[86]	AN199
AM332	VSS[87]	AN200
VSS[177]	VSS[87]	AN201
AM337	VSS[88]	AN202
VSS[178]	VSS[88]	AN203
AM342	VSS[89]	AN204
VSS[179]	VSS[89]	AN205
AM347	VSS[90]	AN206
VSS[180]	VSS[90]	AN207

**VSS**

**POWER**

**GRAPHICS**

**TBD**

**1.0V RAIL**

**SA RAIL**

**UCPU1G**

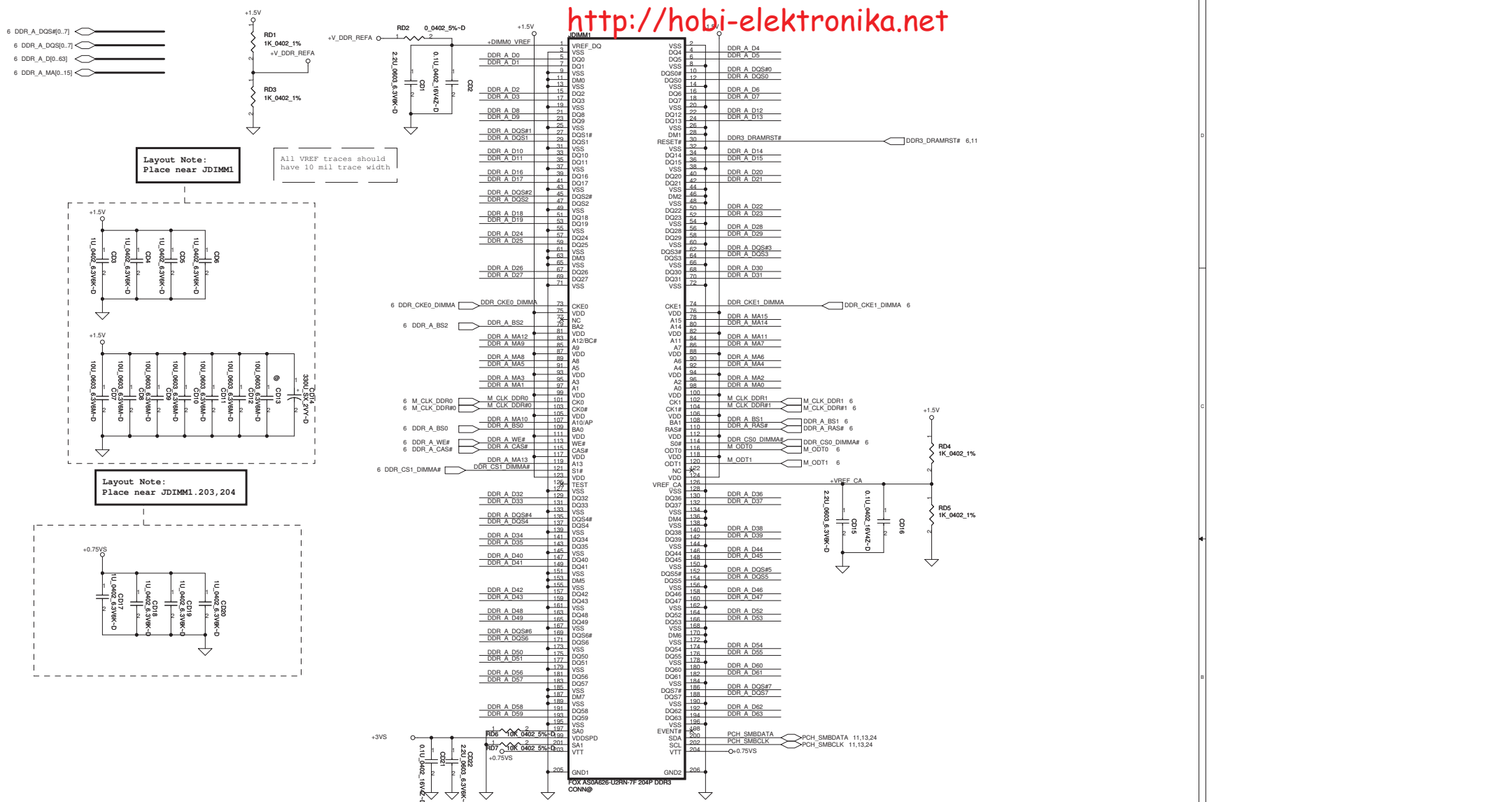
**18A**

**5A**

**6A**

add CC181 , CC182 , 4 caps are all pop.  
follow checklist 1.0 5/24

V2D[0]	V2D[1]	2011	2012
1	1	0.90 V	Yes
1	1	0.80 V	Yes
1	1	0.75 V	Yes
1	1	0.675 V	No



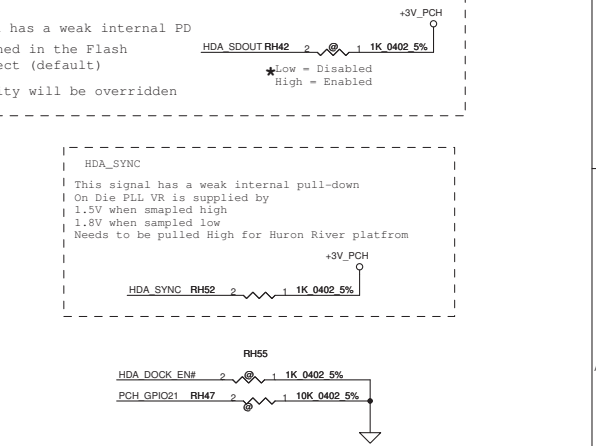
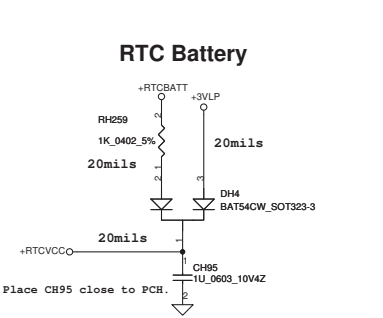
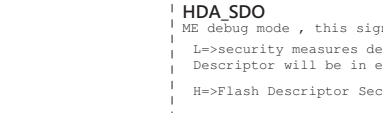
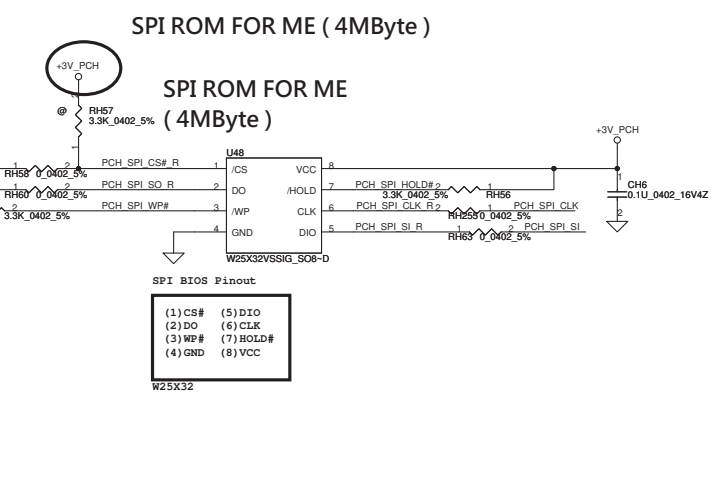
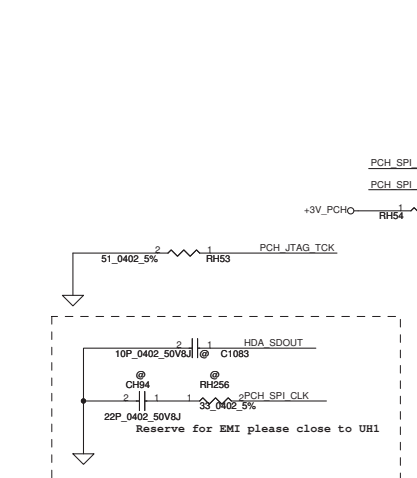
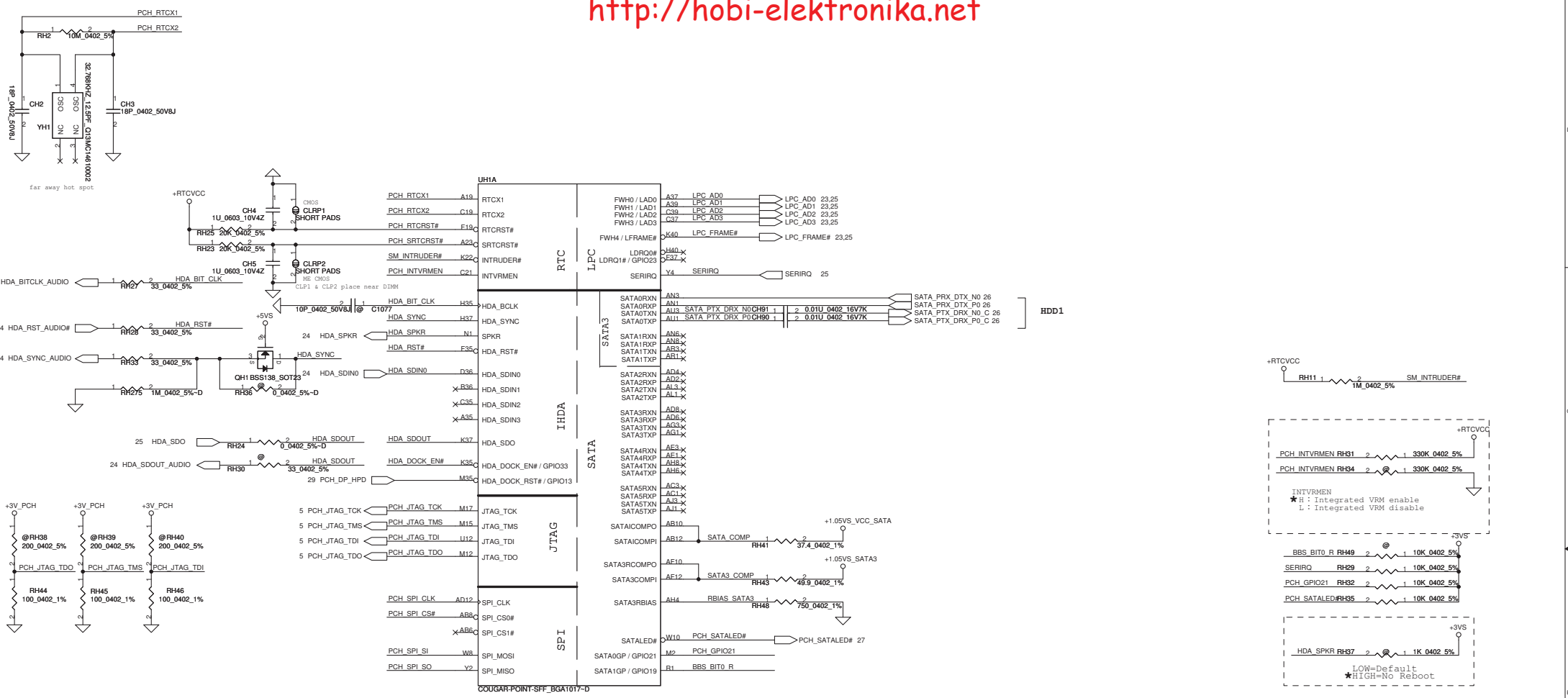
**Layout Note:**  
Place near JDIMM1

**Layout Note:**  
Place near JDIMM1.203,204

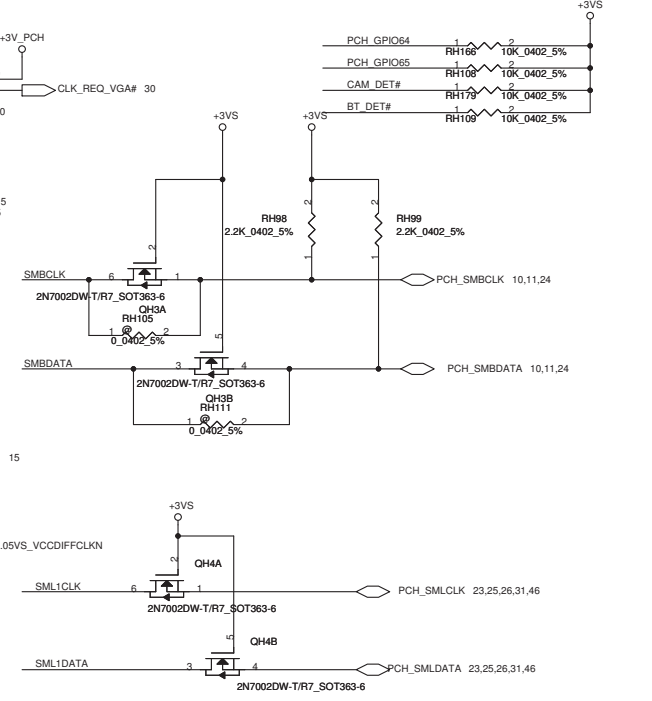
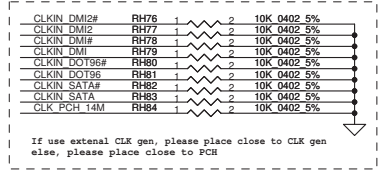
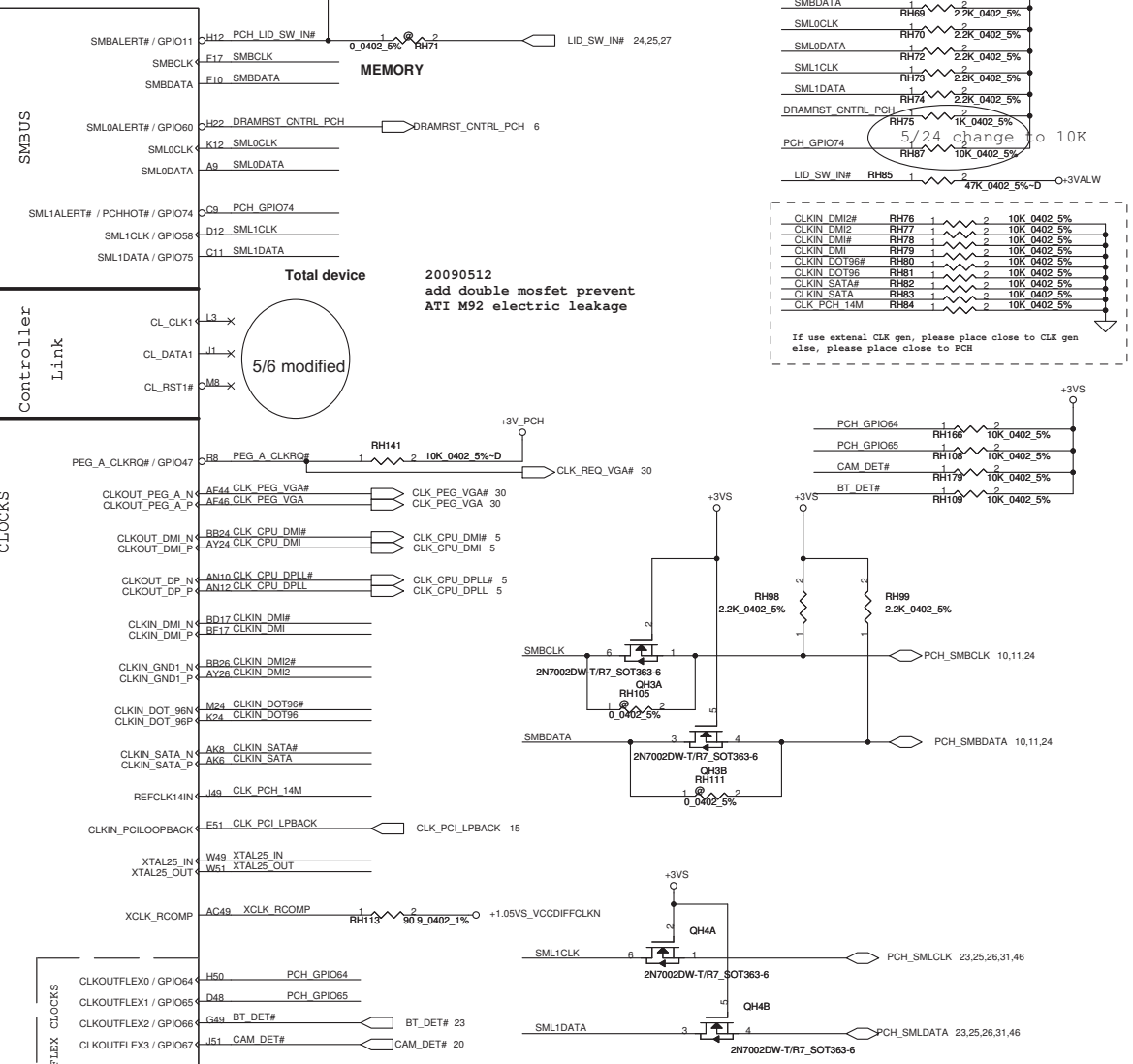
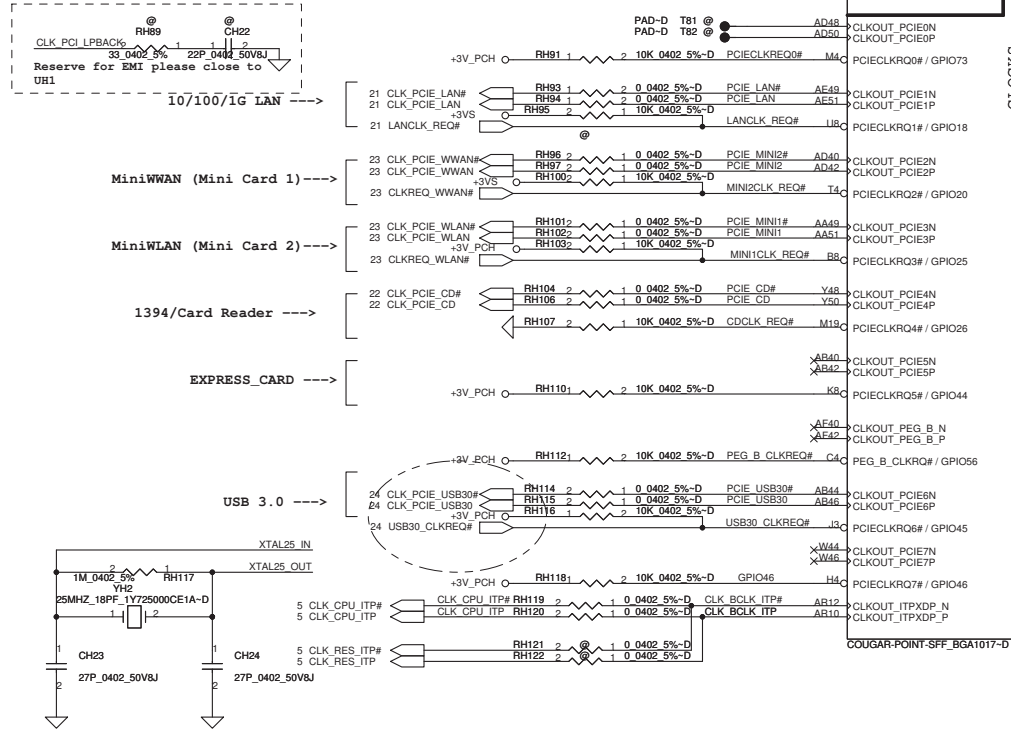
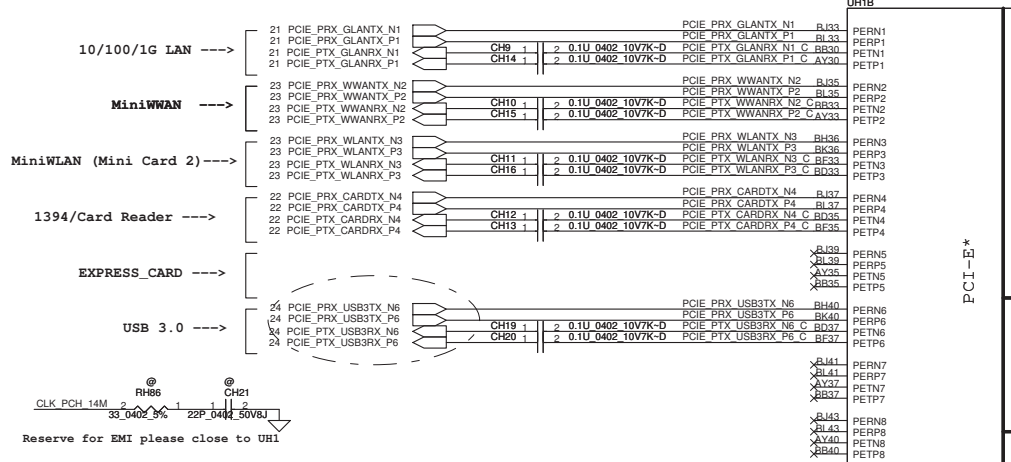
**Layout Note:**  
Place near JDIMM1.203,204

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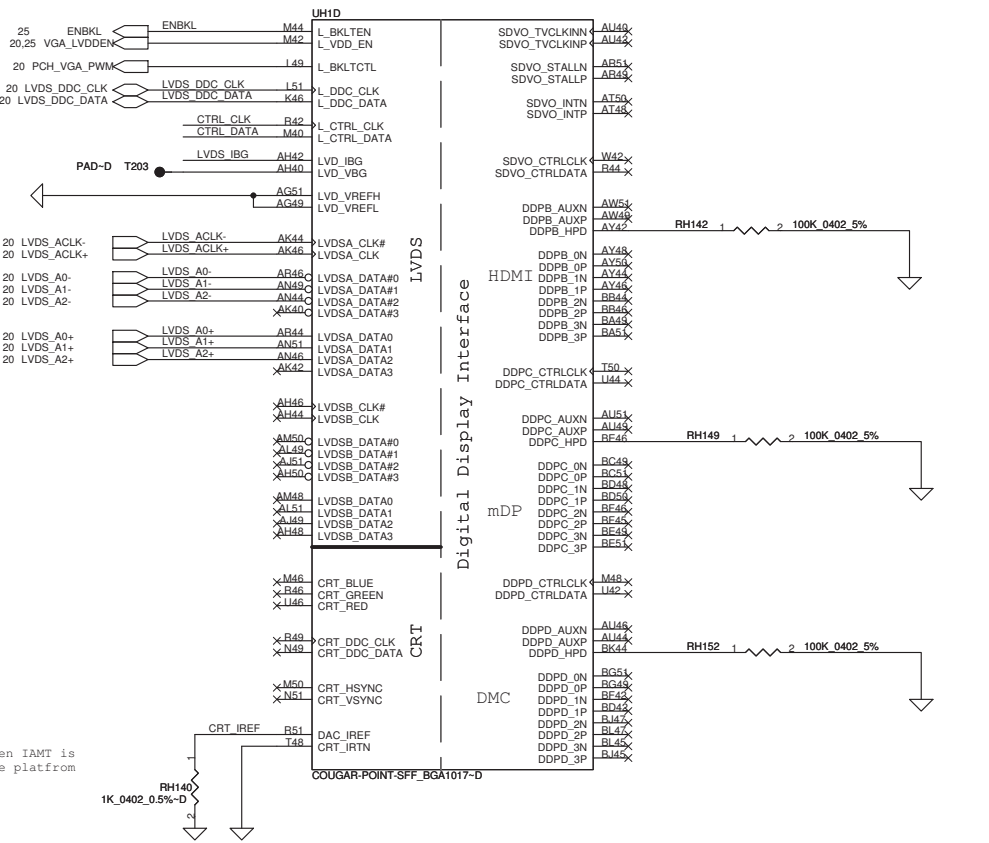
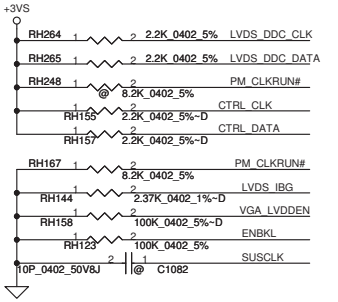
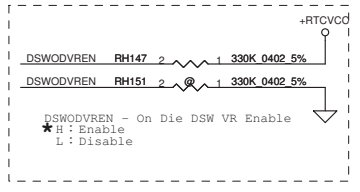
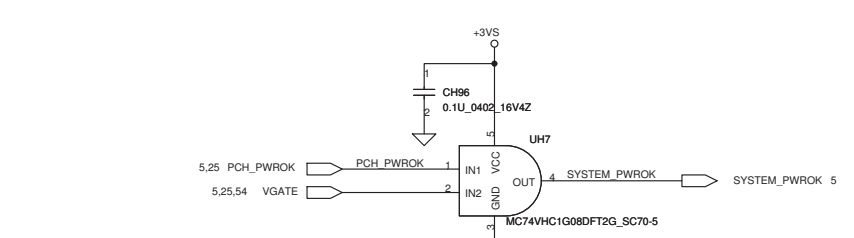
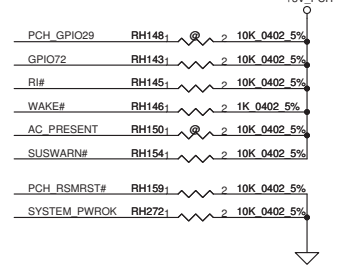
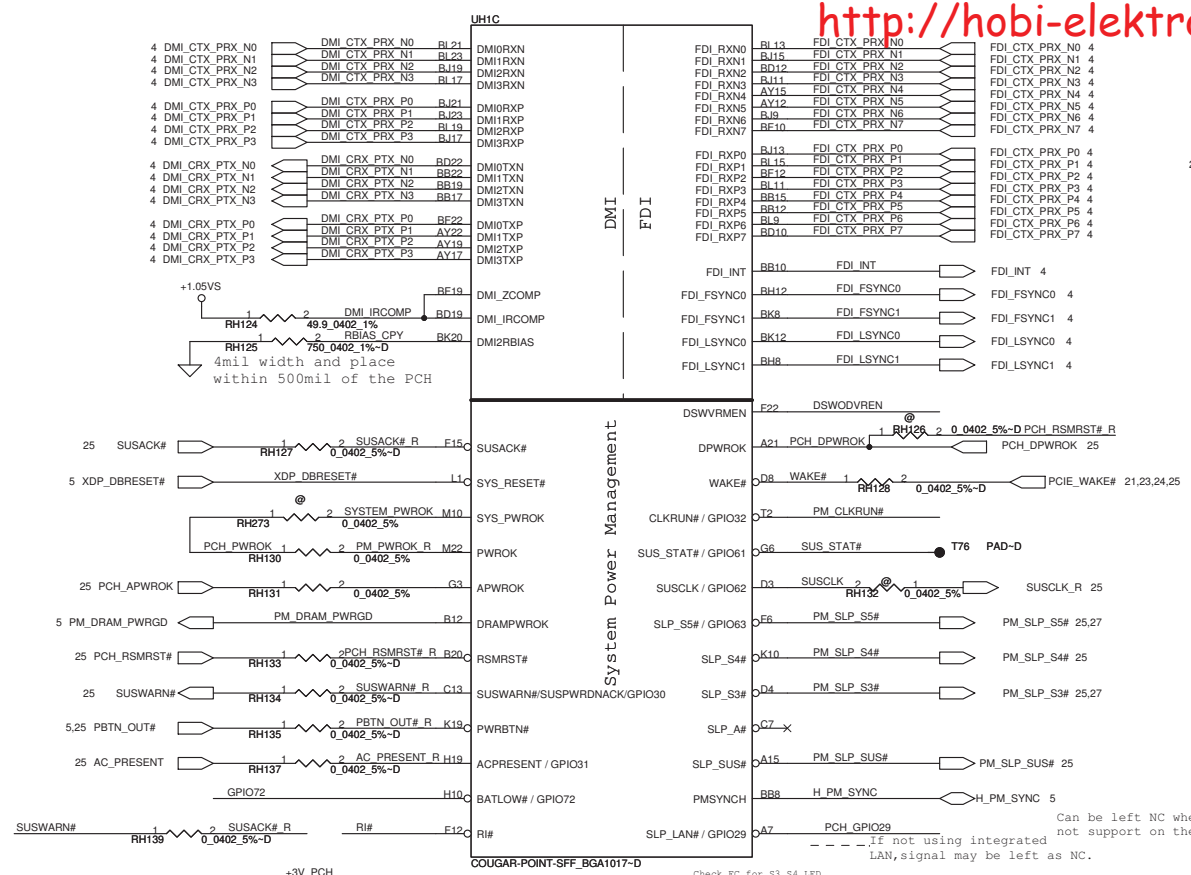




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HDA_SYNC This signal has a weak internal pull-down On Die PLL VR is supplied by 1.5V when sampled high 1.8V when sampled low Needs to be pulled High for Huron River platform				Rev 0.4
HDA_SDO ME debug mode , this signal has a weak internal PD L=>security measures defined in the Flash Descriptor will be in effect (default) H=>Flash Descriptor Security will be overridden				Sheet 12 of 54

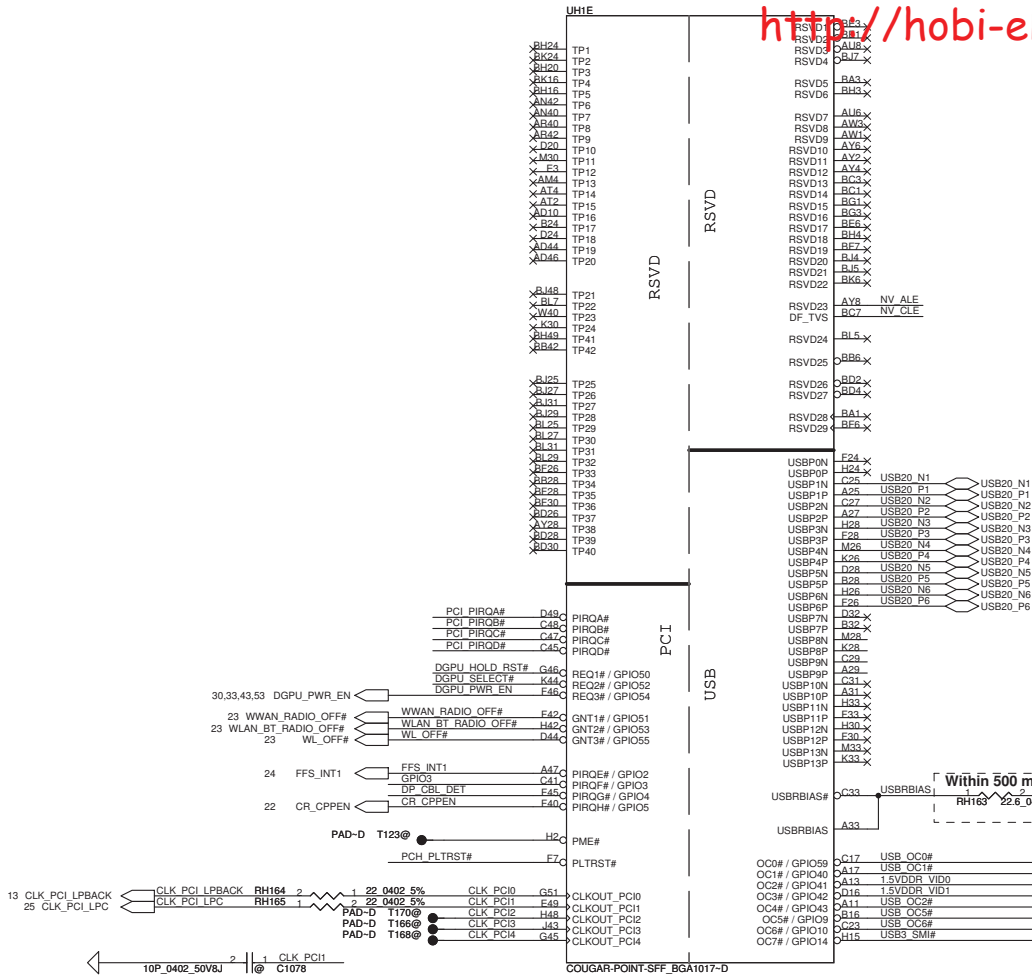


Security Classification	Compal Secret Data		Title <b>PCH (2/8) PCIE, SMBUS, CLK</b>
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Size	Document Number <b>LA-6961P</b>	Sheet	Rev 0.4
Date	Monday, January 24, 2011	13	of 54

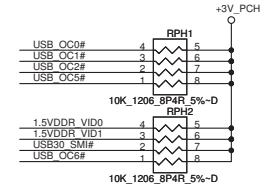
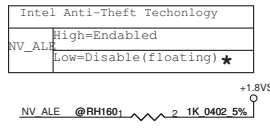
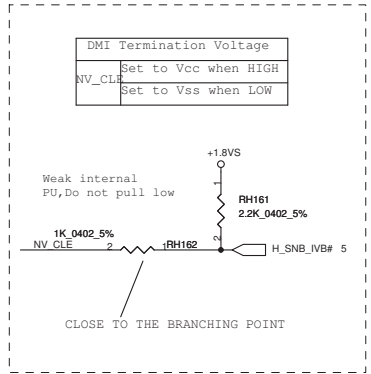


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Document Number				LA-6961P
Date:	Monday, January 24, 2011	Sheet	14	of 54



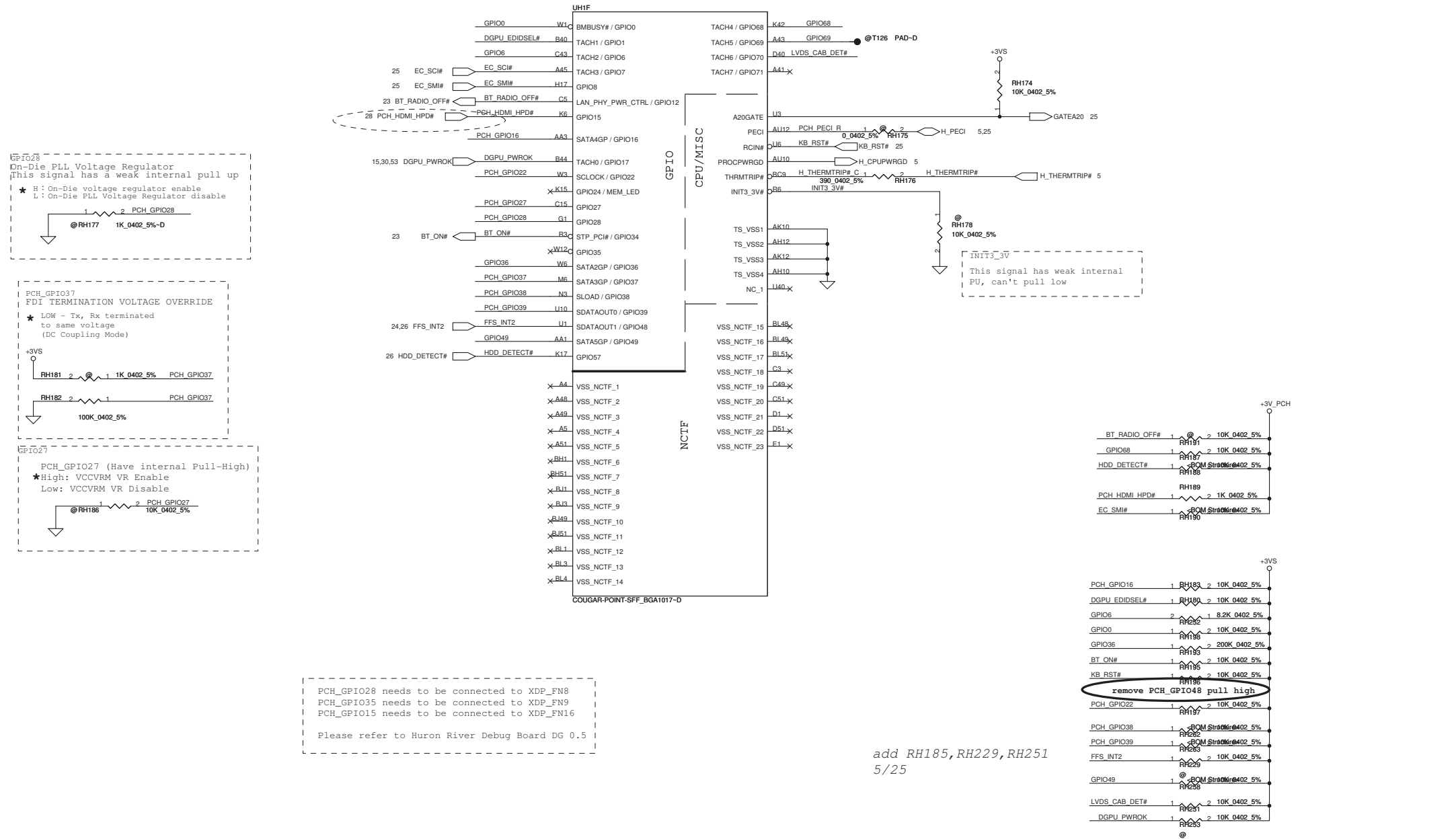


- USB/Left
- Bluetooth
- Camera
- Mini Card(WLAN)
- Mini Card(WWAN)
- ELC LED



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Date:	Tuesday, January 25, 2011	Sheet	15	of 54

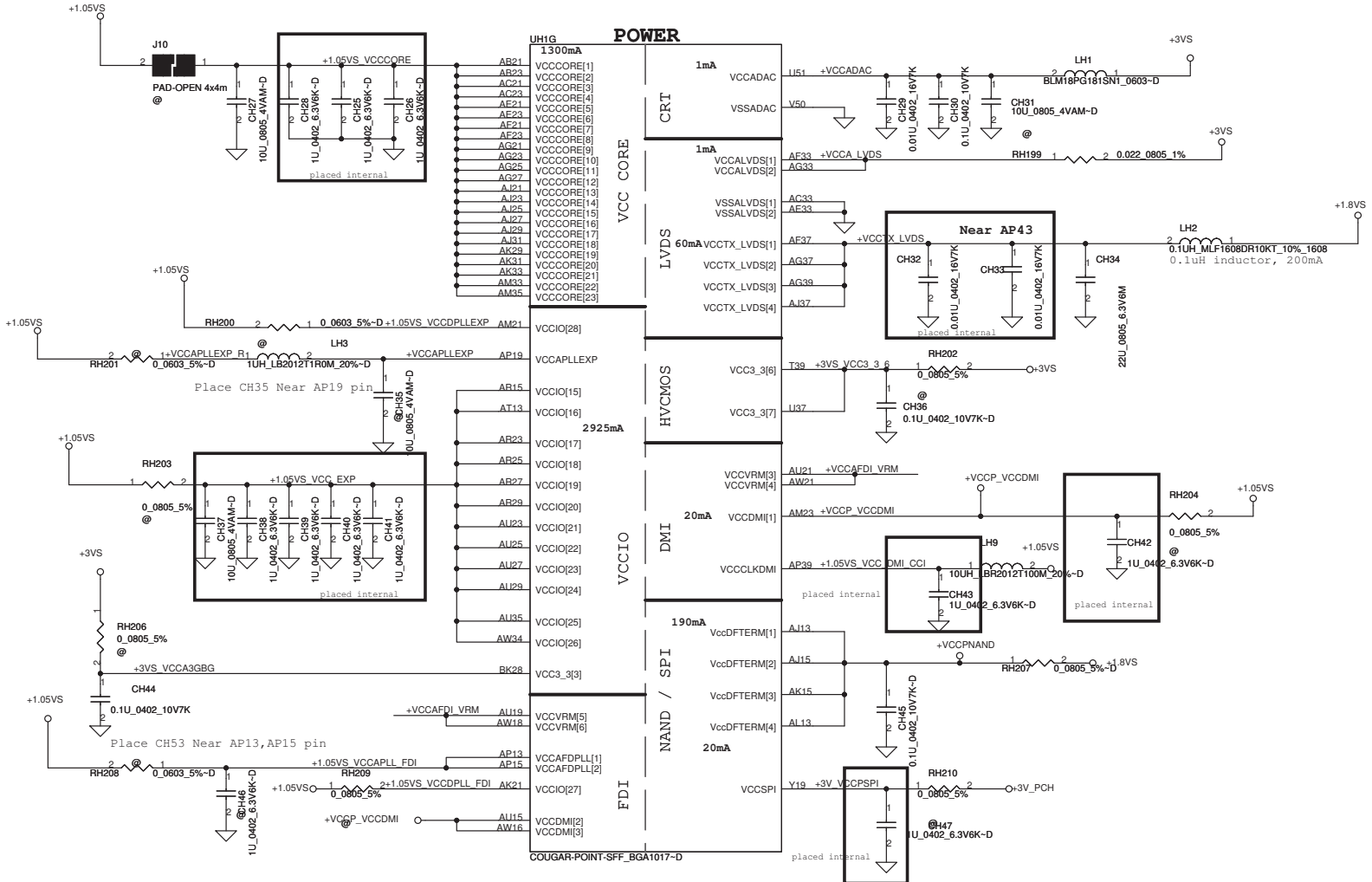




PCH\_GPIO28 needs to be connected to XDP\_FN8  
 PCH\_GPIO35 needs to be connected to XDP\_FN9  
 PCH\_GPIO15 needs to be connected to XDP\_FN16  
 Please refer to Huron River Debug Board DG 0.5

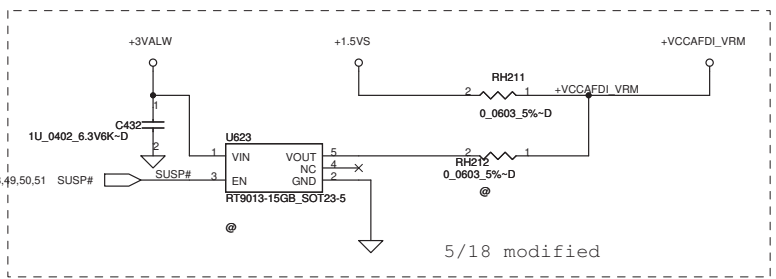
add RH185, RH229, RH251  
 5/25

Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	PCH (5/8) GPIO, CPU, MISC	
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Size	Document Number	Date		Sheet	Rev
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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

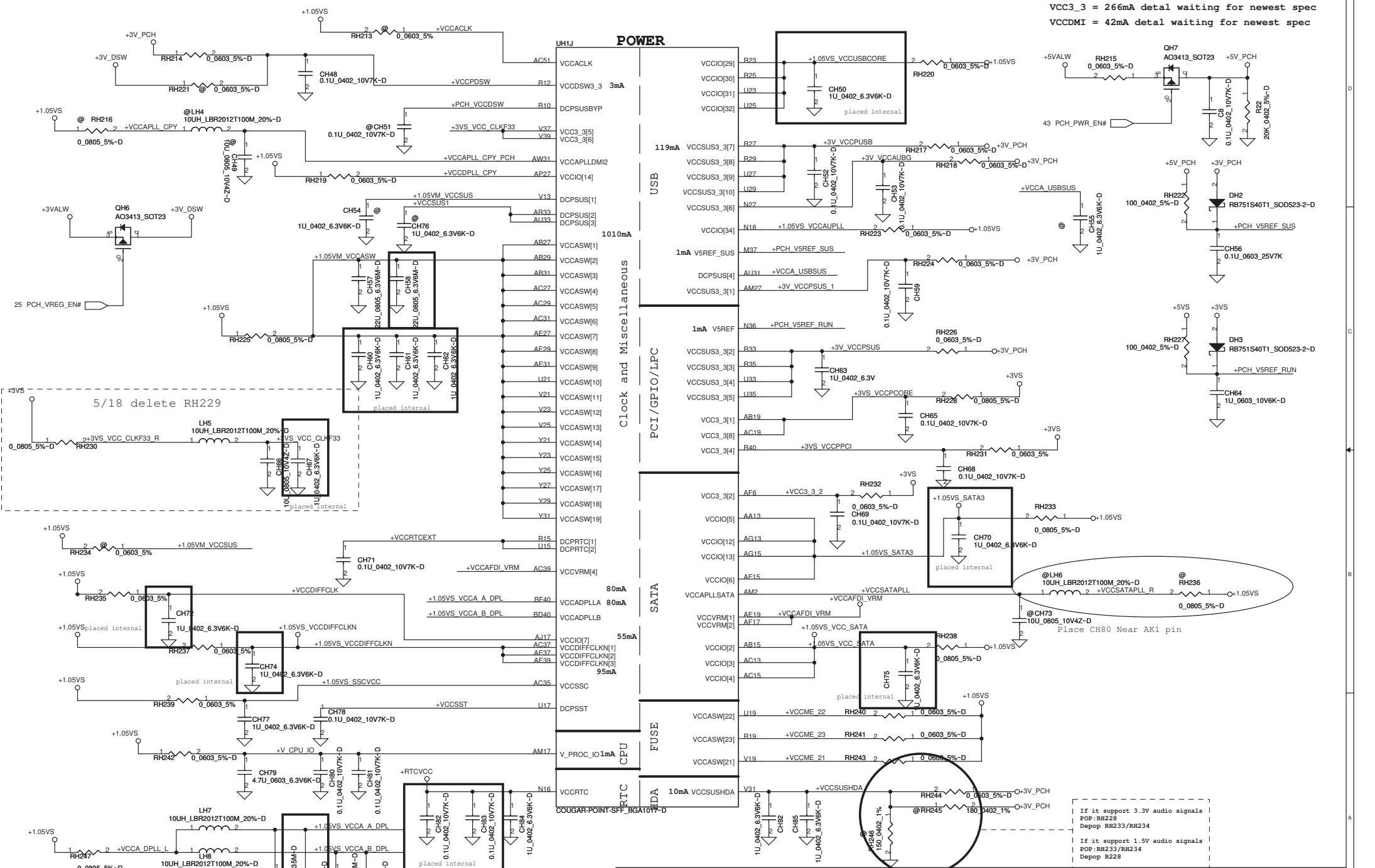
VCCVRM = 160mA detail waiting for newest spec



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<b>Compal Electronics, Inc.</b>		
<b>PCH (6/8) PWR</b>		
Size	Document Number	Rev
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VCC3\_3 = 266mA detal waiting for newest spec  
 VCCDMI = 42mA detal waiting for newest spec

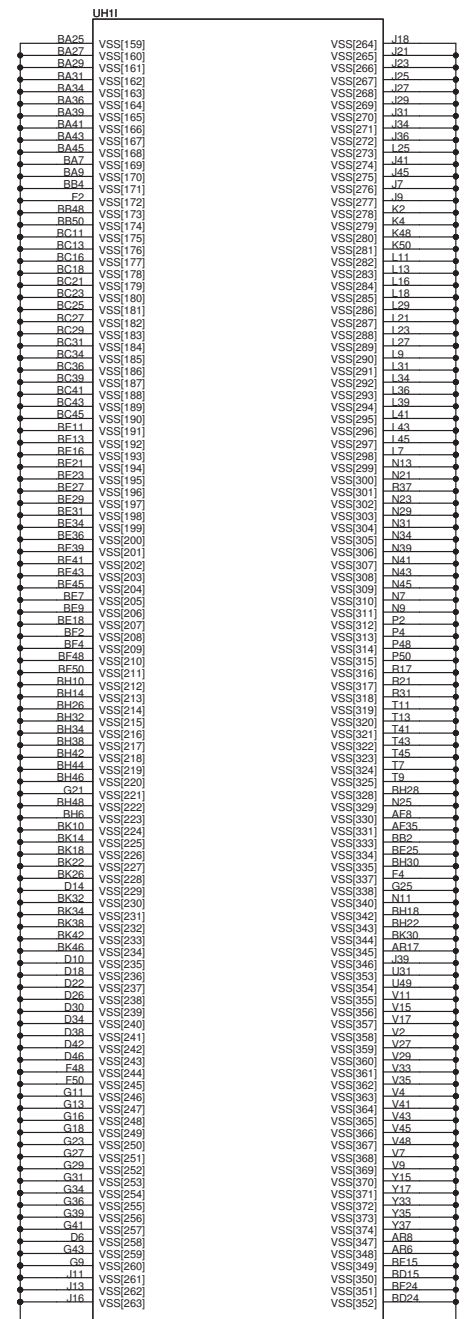
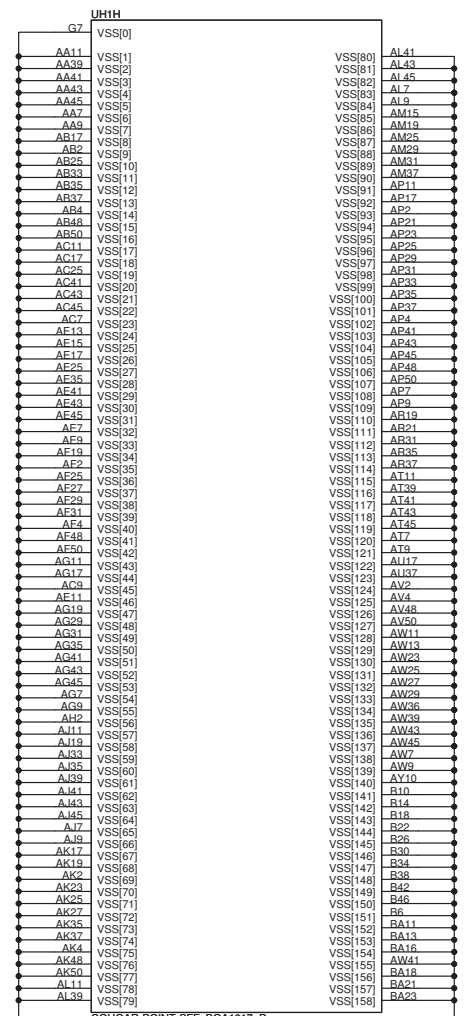


If it support 3.3V audio signals  
 POP: RH228  
 Depop: RH233/RH234

If it support 1.5V audio signals  
 POP: RH233/RH234  
 Depop: R228

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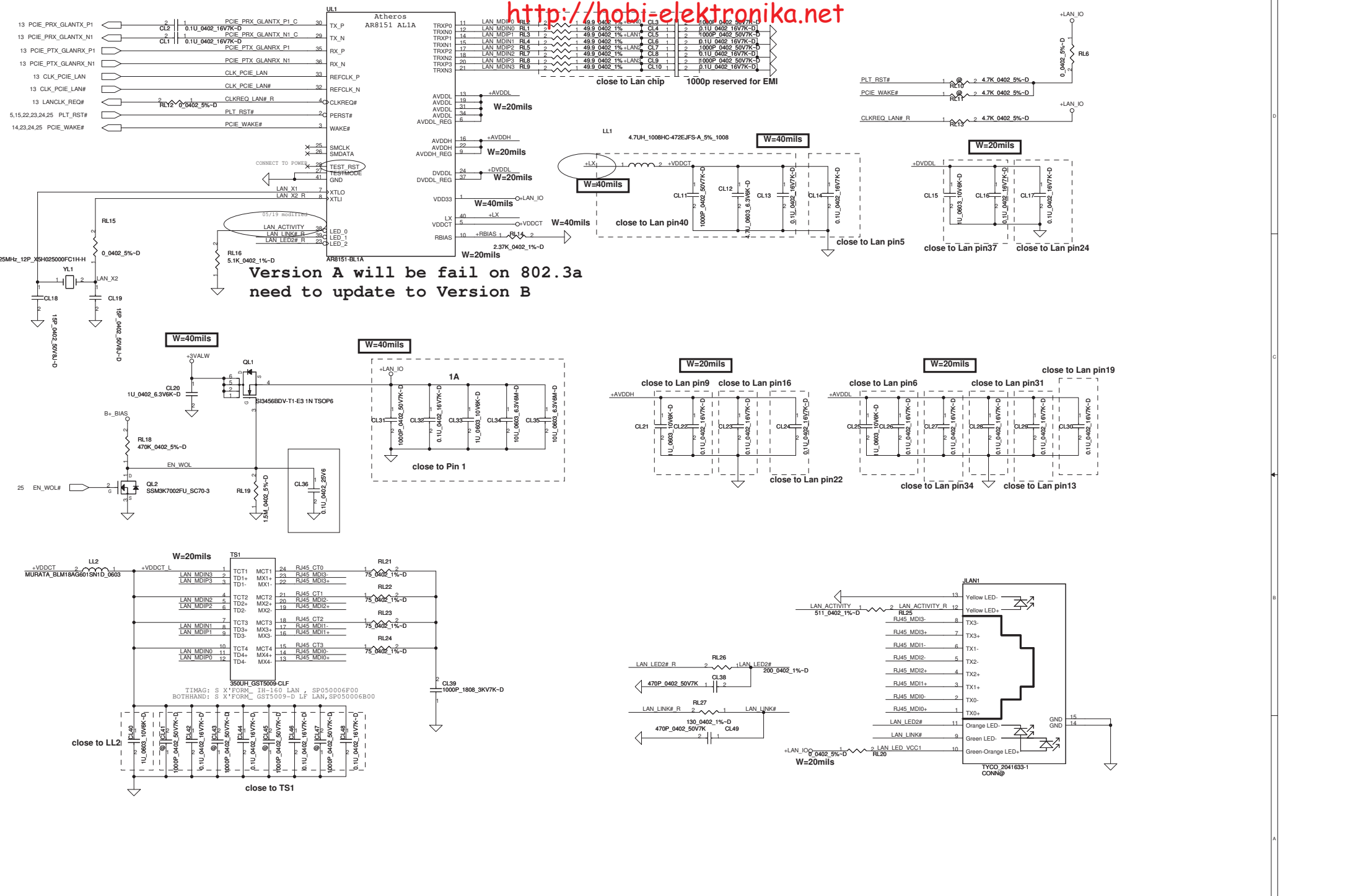
Compal Electronics, Inc.			
Title <b>PCH (7/8) PWR</b>			
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Issued Date	2010/07/06	Deciphered Date	2011/07/06	Compal Electronics, Inc.
				<b>PCH (8/8) VSS</b>
				Size Document Number
				<b>LA-6961P</b>
				Rev 0.4
				Date: Monday, January 24, 2011
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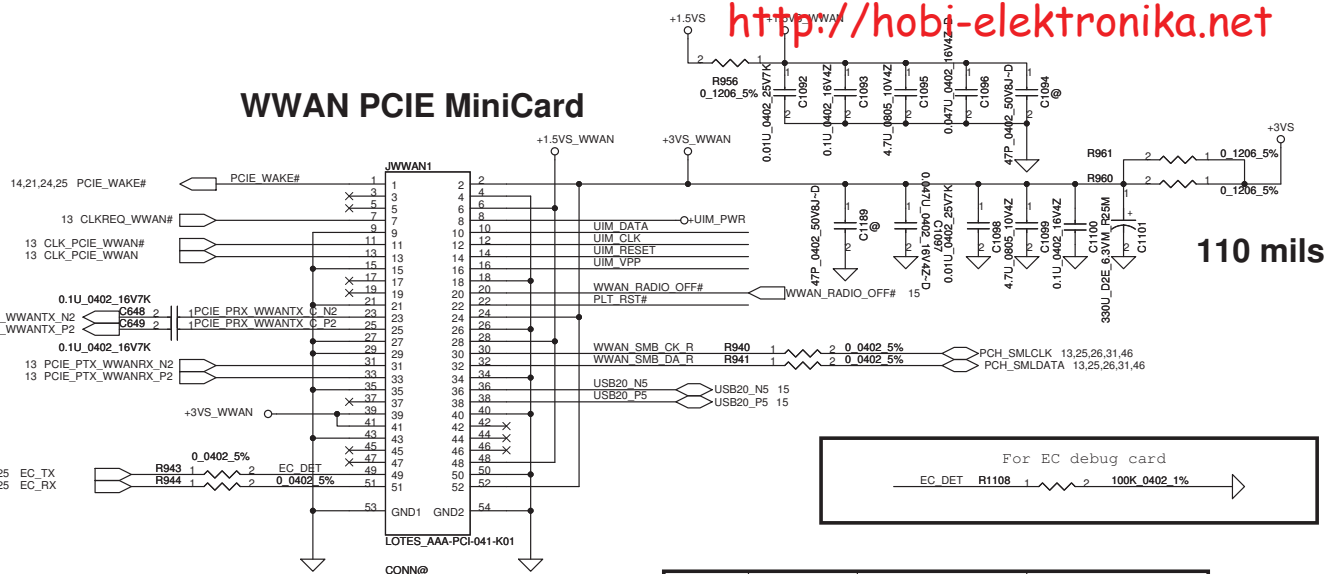
Version A will fail on 802.3a  
need to update to Version B

Security Classification	Compal Secret Data		Title <b>GLAN AR8151 AL1A/RJ45</b>
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Size	Document Number	Rev	Sheet
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Date:	Tuesday, January 25, 2011		

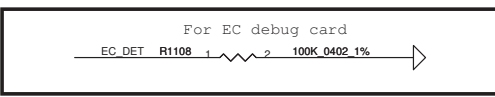




### WWAN PCIE MiniCard



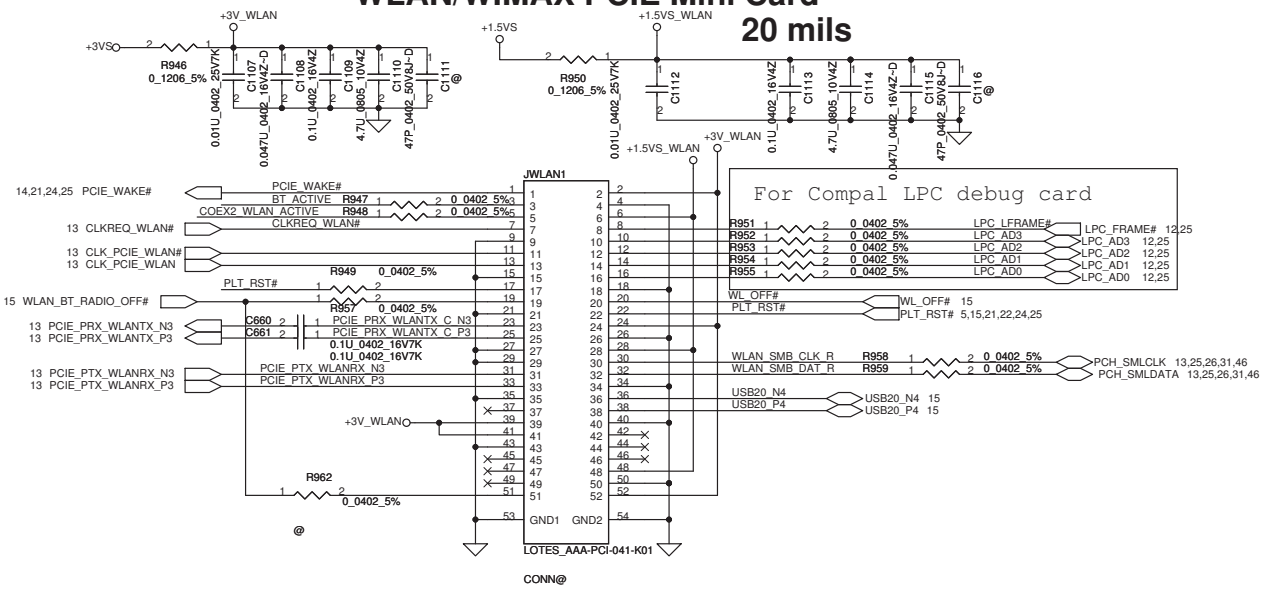
110 mils



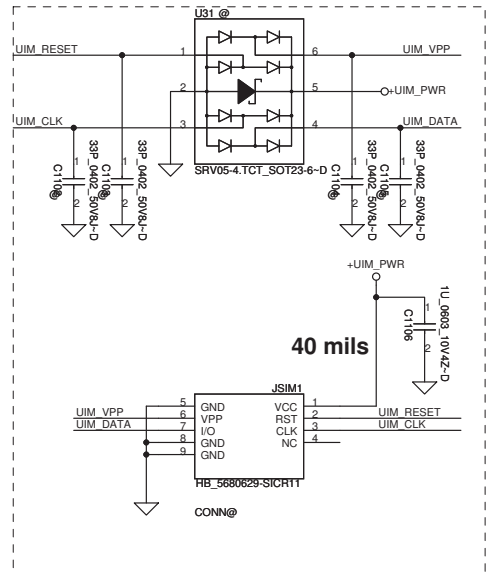
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+/-9%	1000	750	
+3.3Vaux	+/-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+/-5%	500	375	NA

### WLAN/WIMAX PCIE Mini Card

40 mils 20 mils

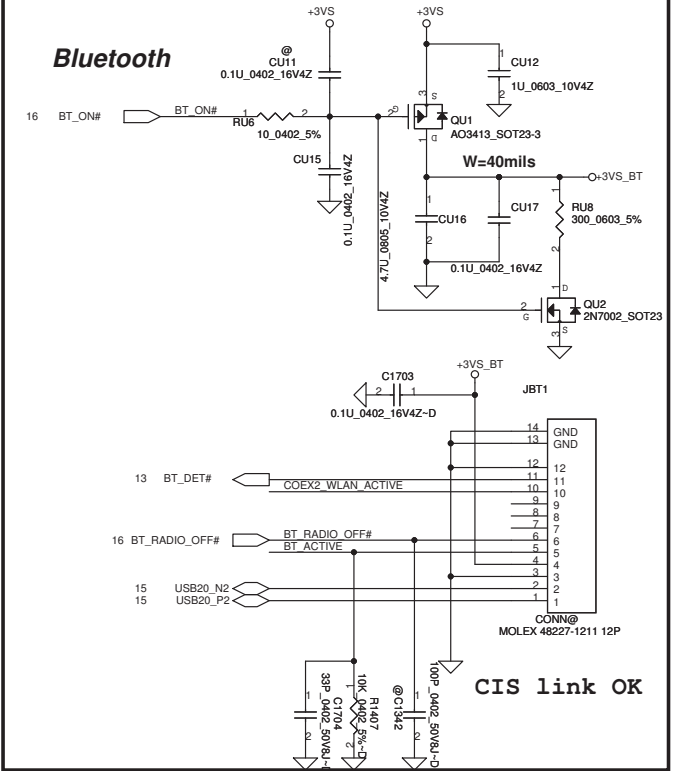


### SIM Card



40 mils

### Bluetooth



CIS link OK

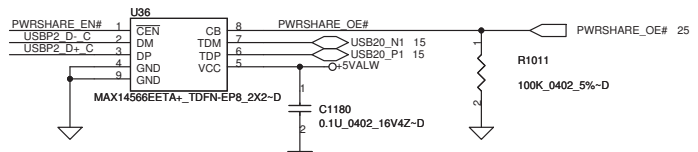
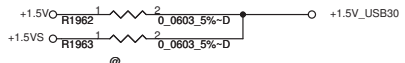
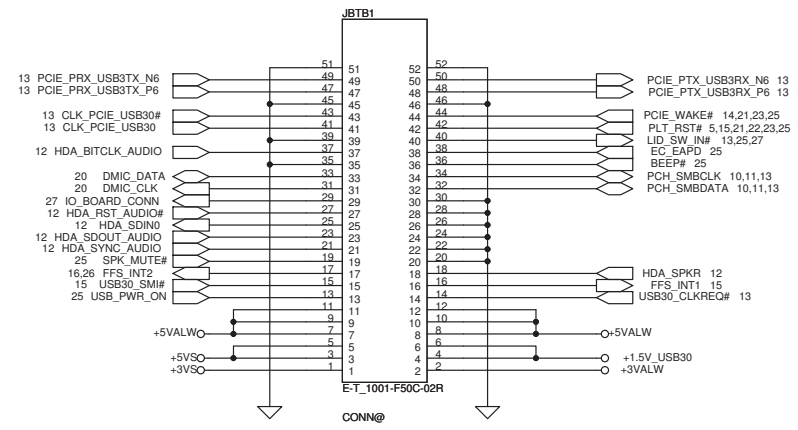
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Issued Date	2009/07/25	Deciphered Date
		2011/07/06

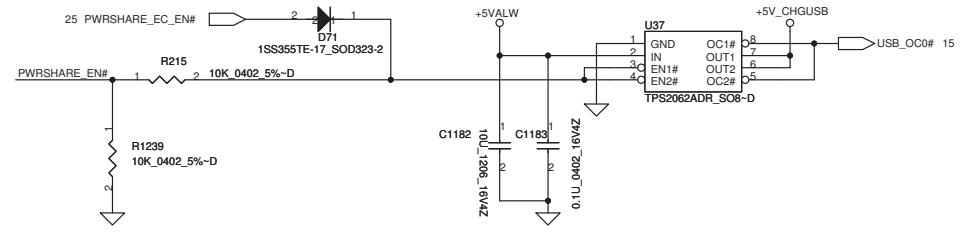
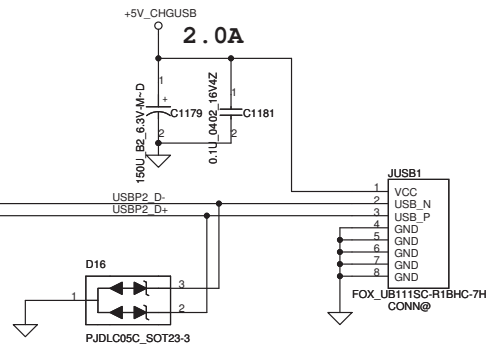
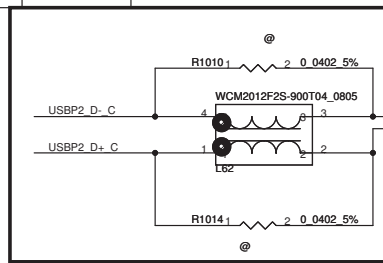
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Size			<b>WLAN/WWAN/SIM/BT</b>	
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IO Board CONN



OE#	Function
L	Dect charger
H	D=1D



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Issued Date	2009/07/25	Deciphered Date
		2011/07/06

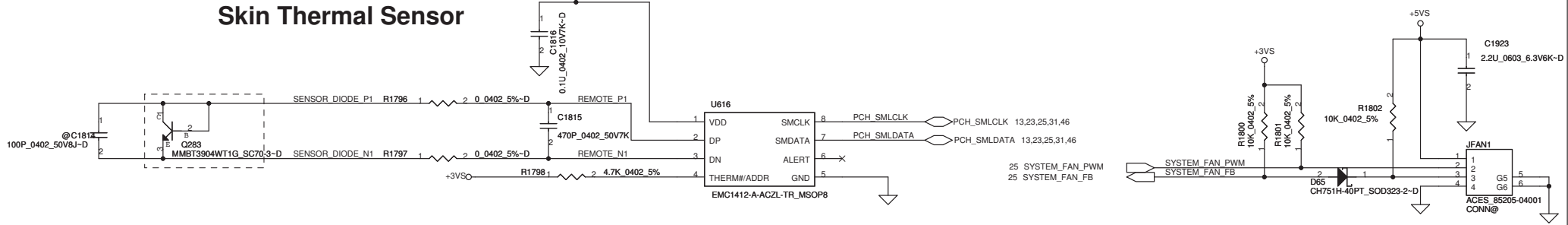
Title		
Compal Electronics, Inc.		
USB/LID SW/IO CONN		

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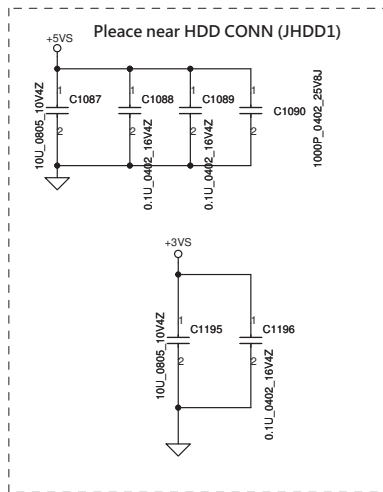
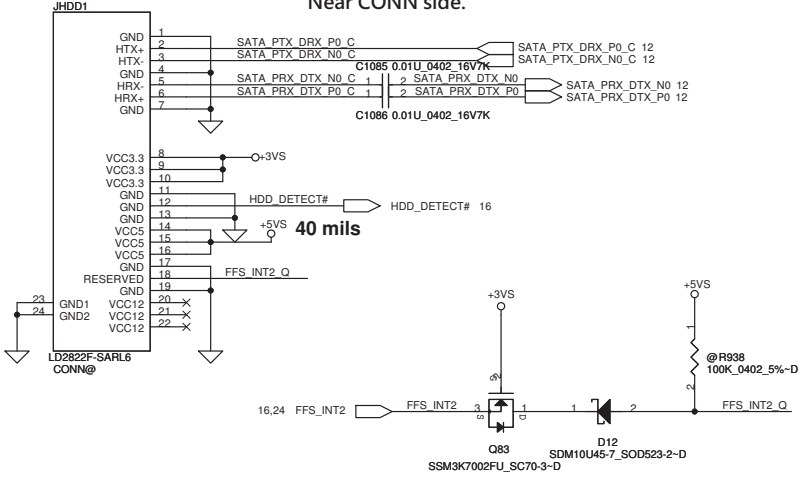


### Skin Thermal Sensor



### HDD Connector

Near CONN side.



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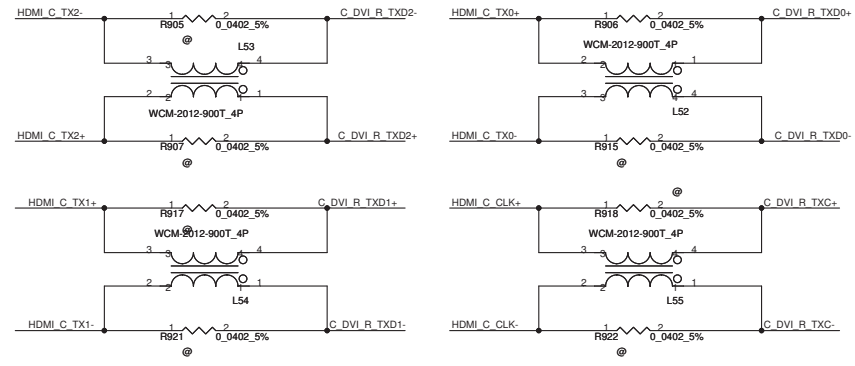
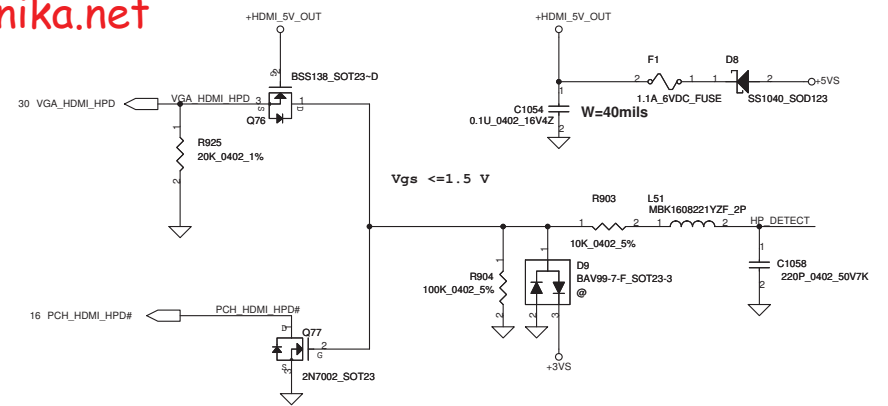
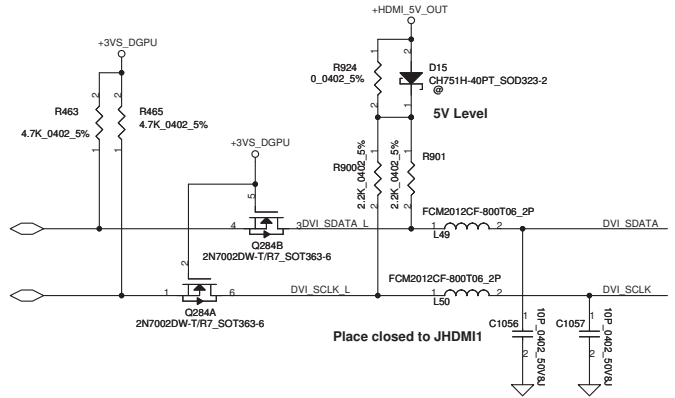
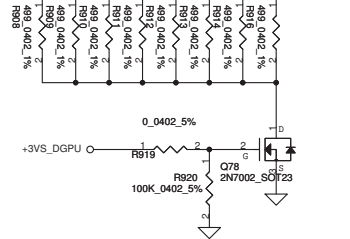


Title		
FAN & Thermal Sensor		
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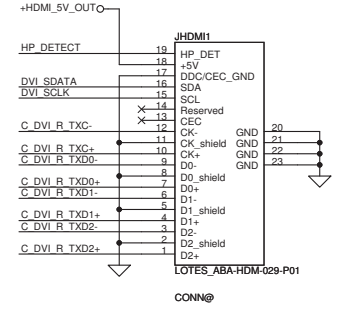
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31	VGA_HDMI_TX2-	VGA_HDMI_TX2-	C1059	2	1	0.1U_0402_16V7K	HDMI C_TX2-
31	VGA_HDMI_TX2+	VGA_HDMI_TX2+	C1060	2	1	0.1U_0402_16V7K	HDMI C_TX2+
31	VGA_HDMI_TX1-	VGA_HDMI_TX1-	C1061	2	1	0.1U_0402_16V7K	HDMI C_TX1-
31	VGA_HDMI_TX1+	VGA_HDMI_TX1+	C1062	2	1	0.1U_0402_16V7K	HDMI C_TX1+
31	VGA_HDMI_TX0-	VGA_HDMI_TX0-	C1063	2	1	0.1U_0402_16V7K	HDMI C_TX0-
31	VGA_HDMI_TX0+	VGA_HDMI_TX0+	C1064	2	1	0.1U_0402_16V7K	HDMI C_TX0+
31	VGA_HDMI_CLK-	VGA_HDMI_CLK-	C1065	2	1	0.1U_0402_16V7K	HDMI C_CLK-
31	VGA_HDMI_CLK+	VGA_HDMI_CLK+	C1066	2	1	0.1U_0402_16V7K	HDMI C_CLK+



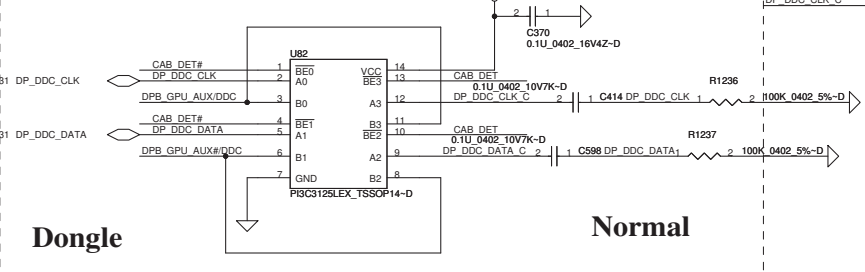
**HDMI Connector**



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Issued Date	2009/07/25	Deciphered Date	2011/07/06	<b>HDMI</b>
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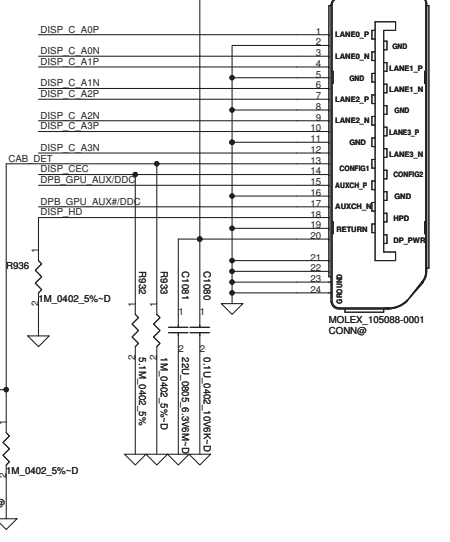
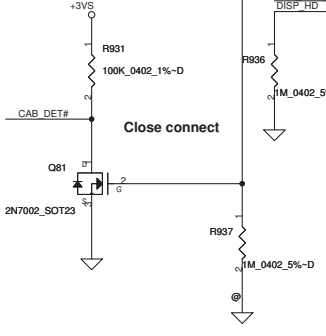
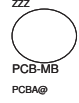
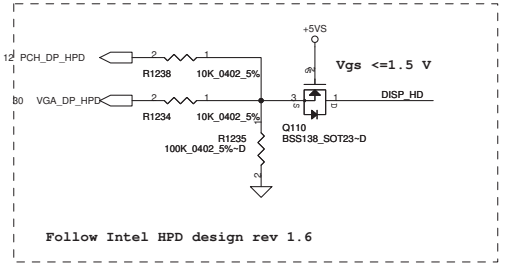
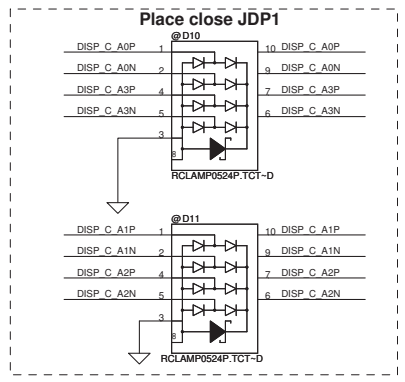
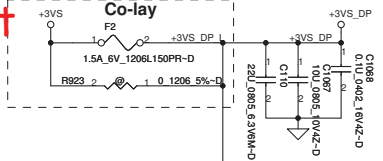
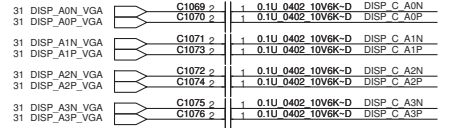
# GPU DDC Dongle SW for DP



Dongle

Normal

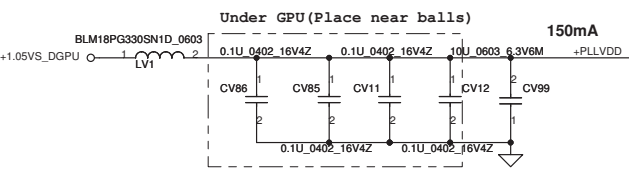
## Near to NV



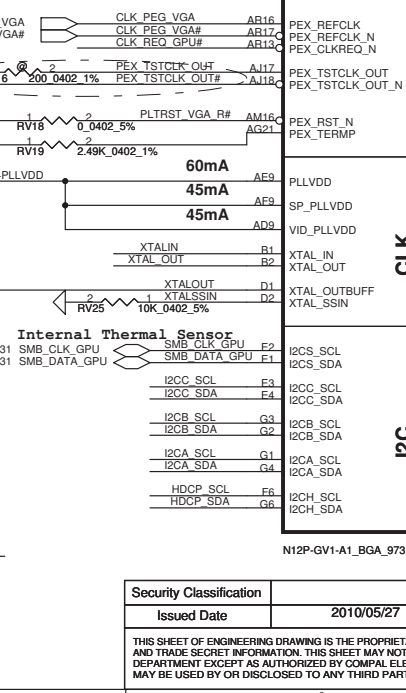
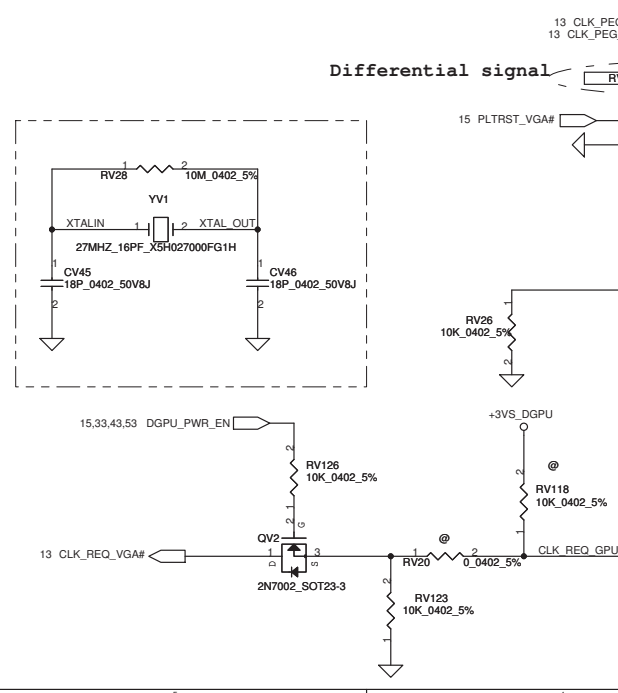
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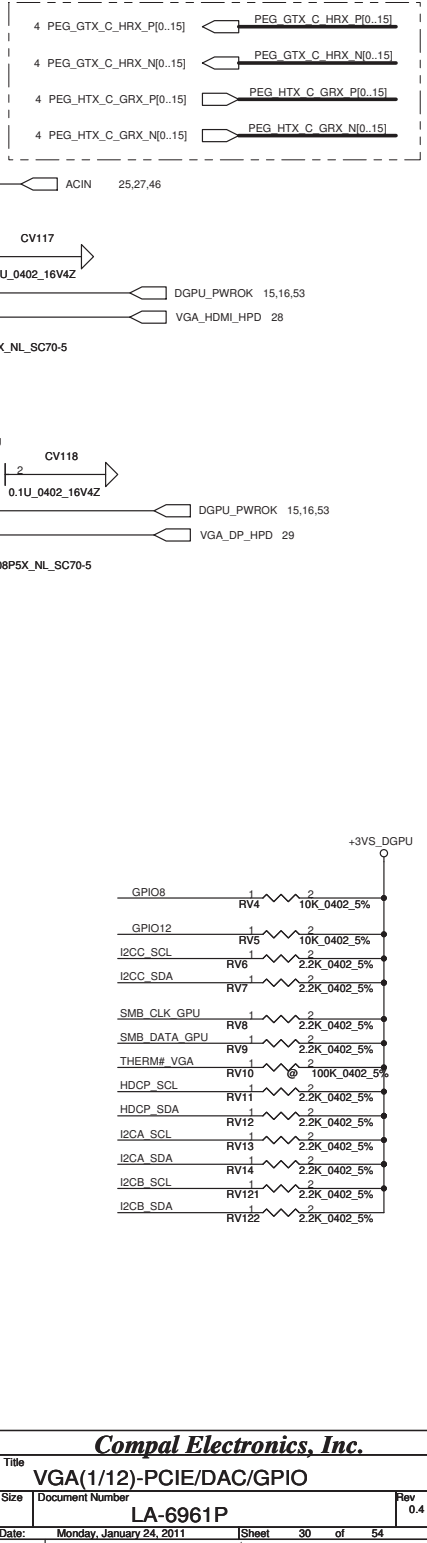




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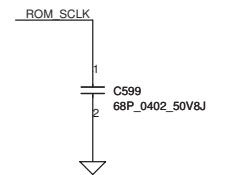
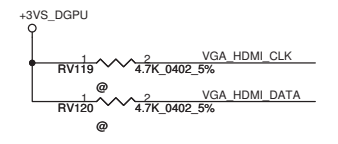
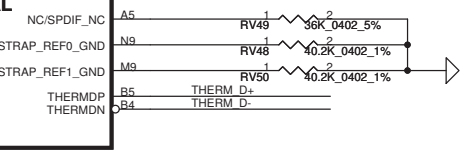
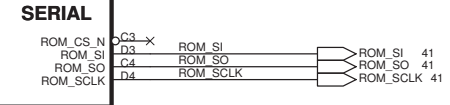
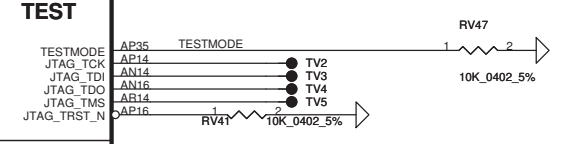
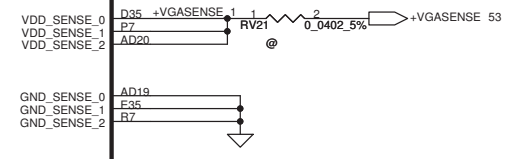
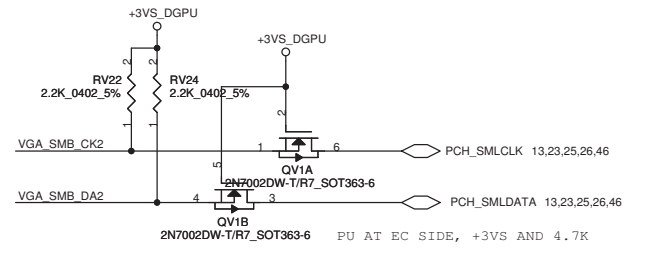
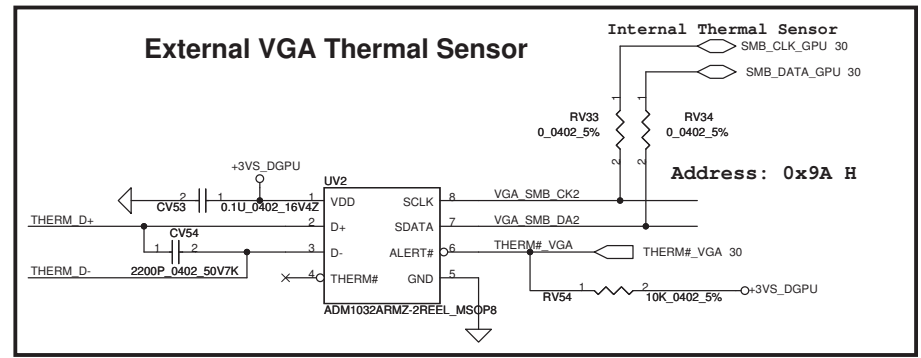
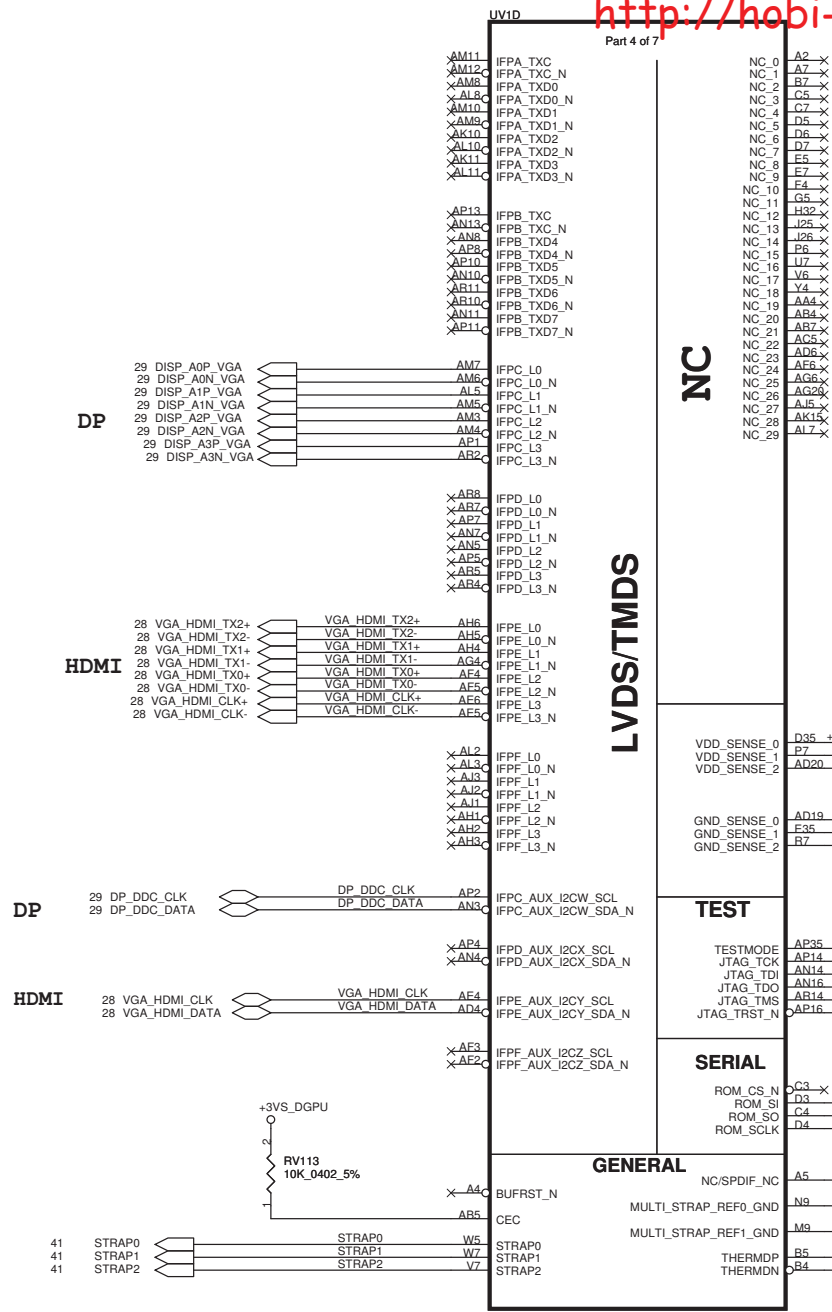


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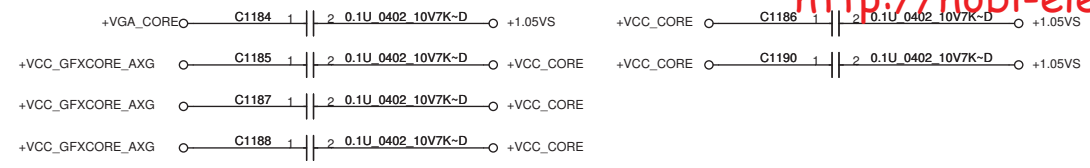
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Title VGA(1/12)-PCIE/DAC/GPIO			
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Date	Monday, January 24, 2011	Sheet	30 of 54

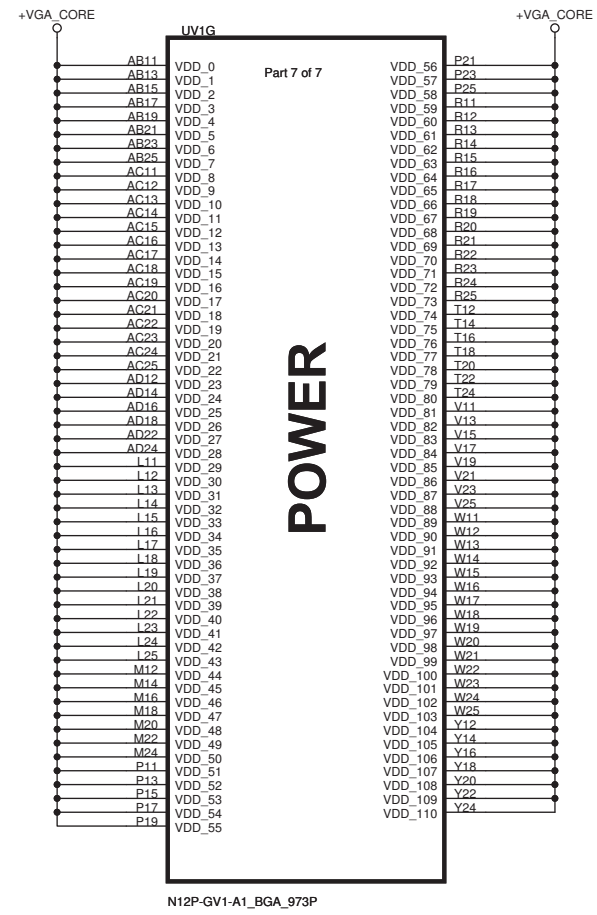


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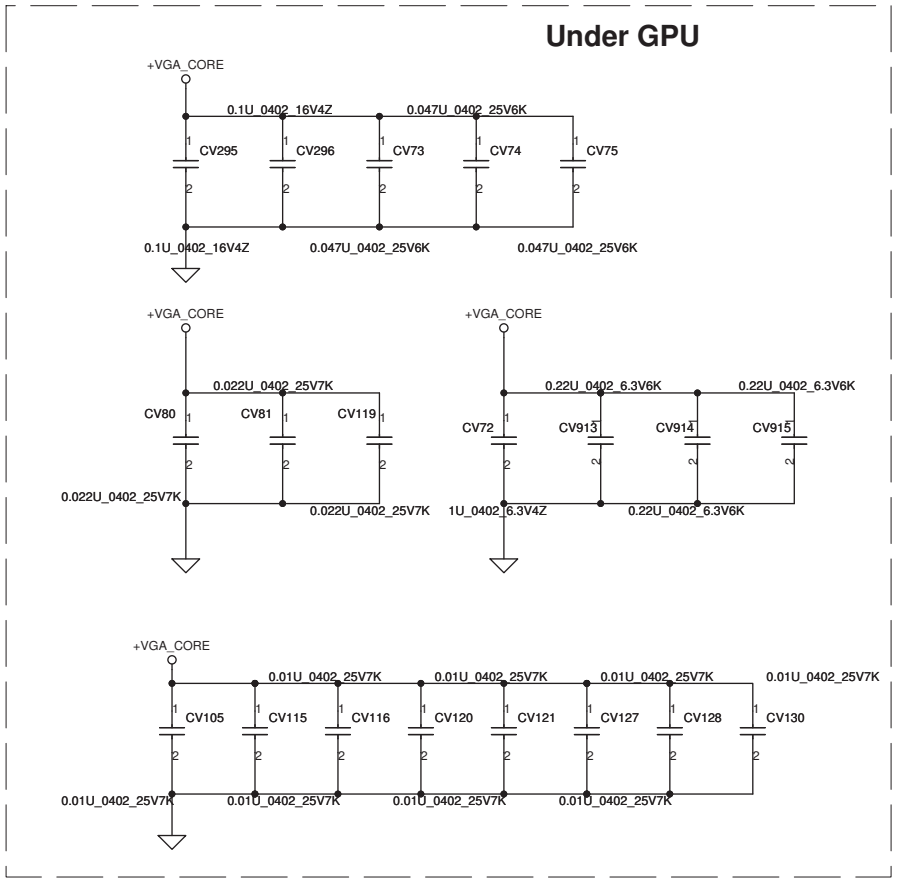
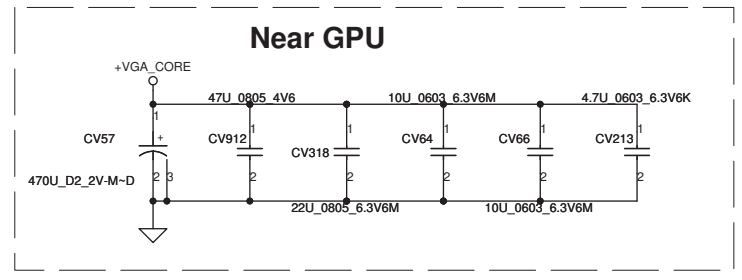
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Size		Document Number		Rev	
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Date:		Tuesday, January 25, 2011		Sheet 31 of 54	



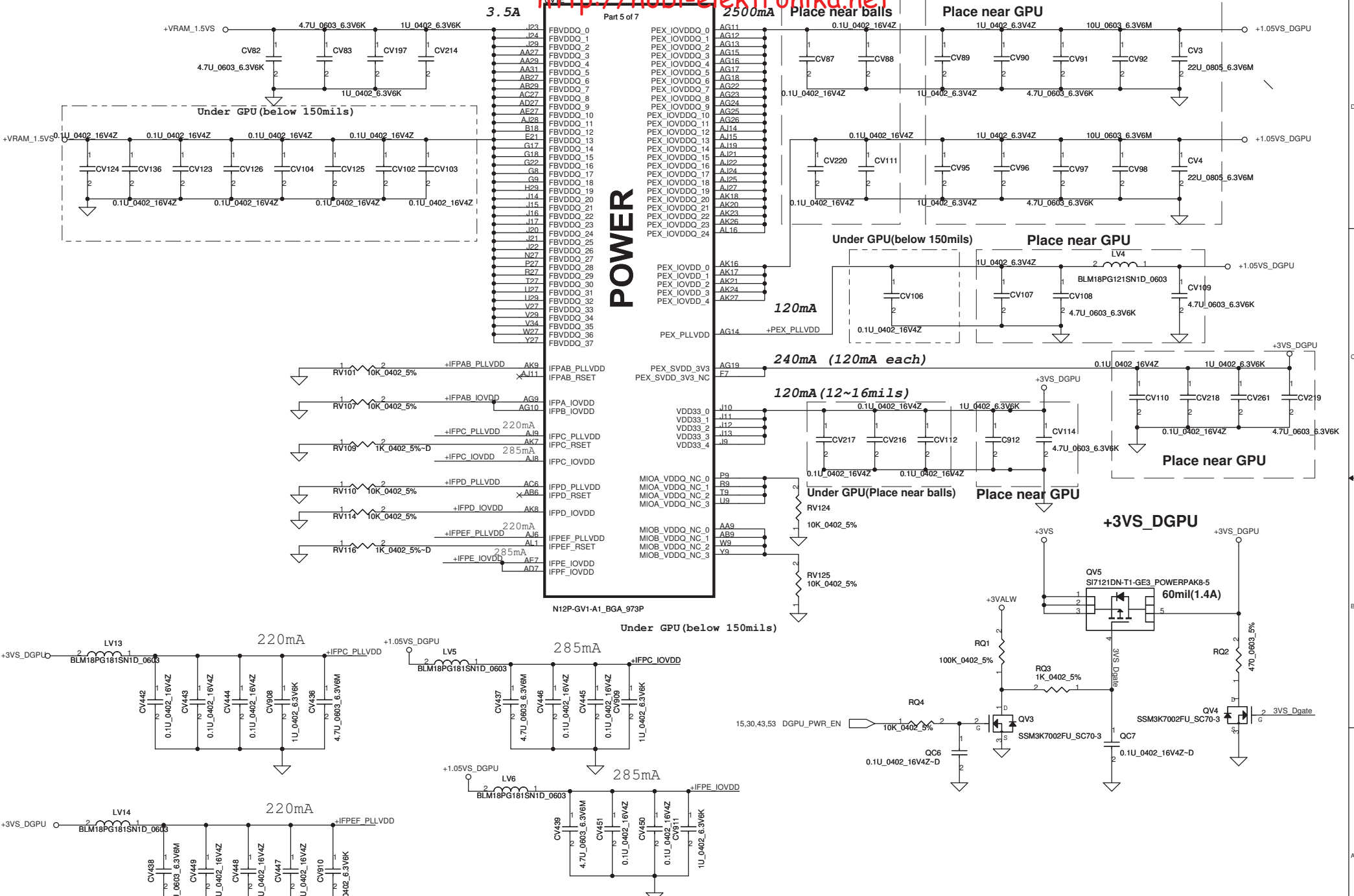
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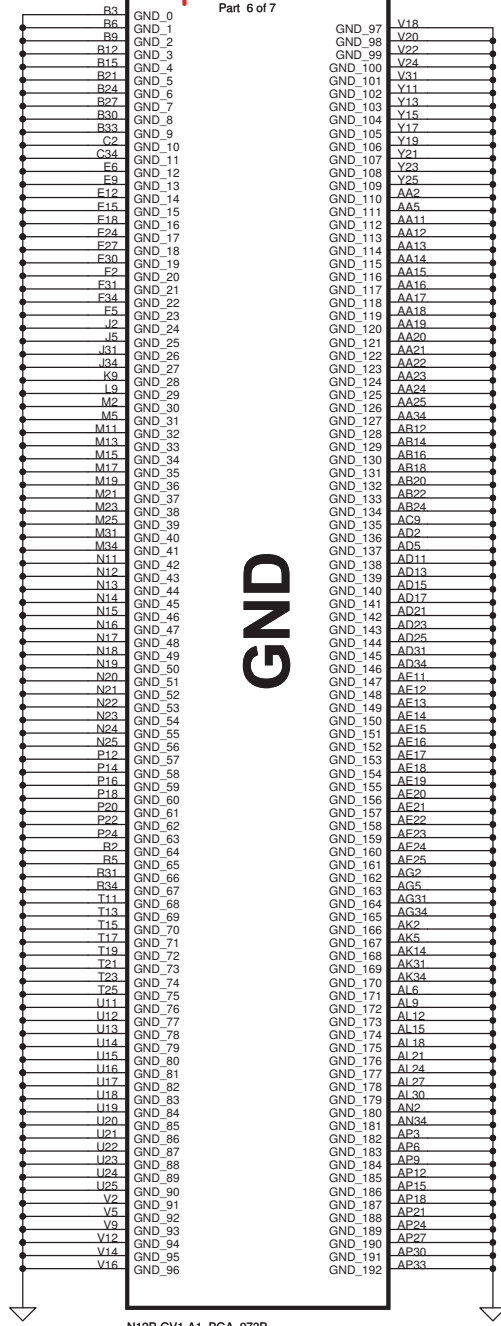


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<b>VGA(4/12)-POWER</b>		
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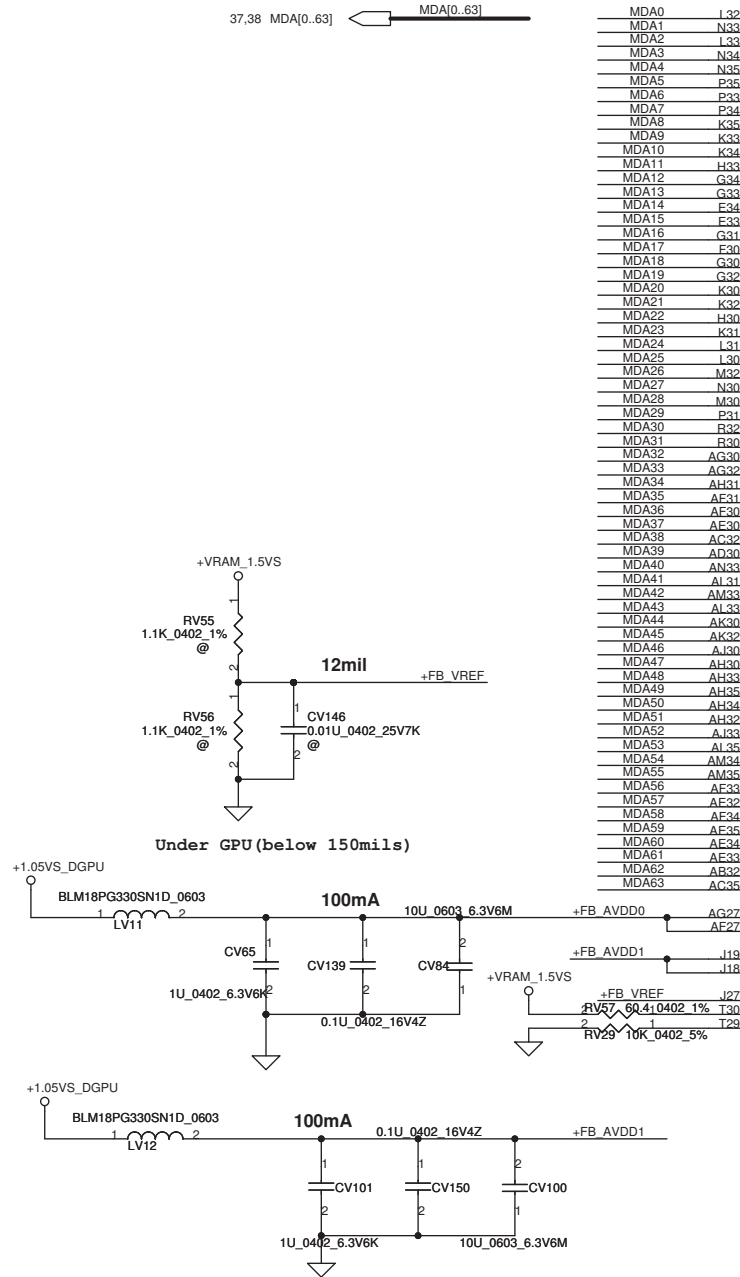
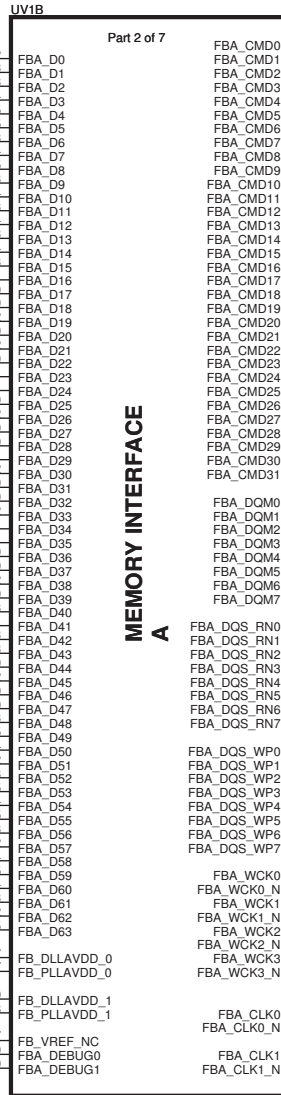
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Issued Date	2010/05/27	Deciphered Date	2011/07/06
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<b>Compal Electronics, Inc.</b>			
Title <b>VGA(5/12)-GND</b>			
Size	Document Number	Rev	
	<b>LA-6961P</b>	0.4	
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Mode E - Mirror Mode Mapping

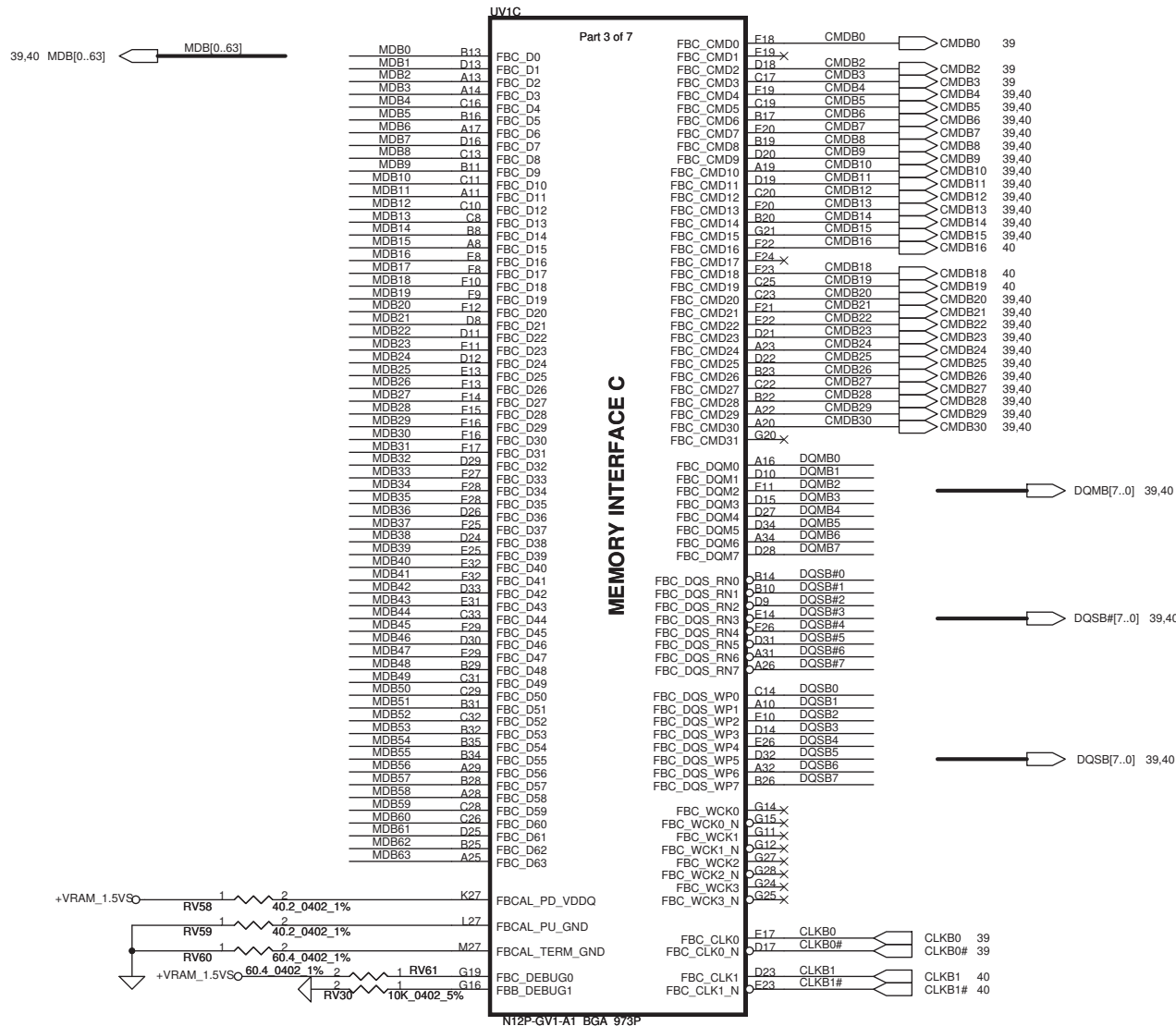
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CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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Compal Electronics, Inc.			
Title VGA(6/12)-MEM Interface A			
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Mode E - Mirror Mode Mapping

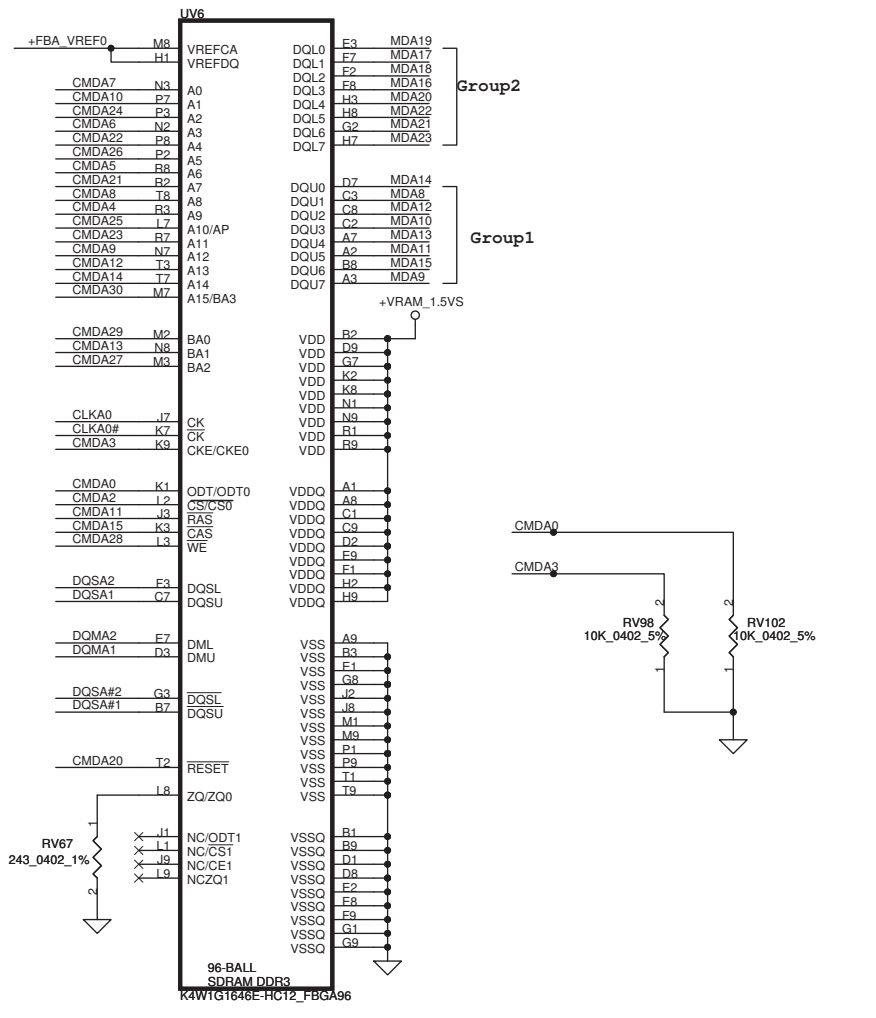
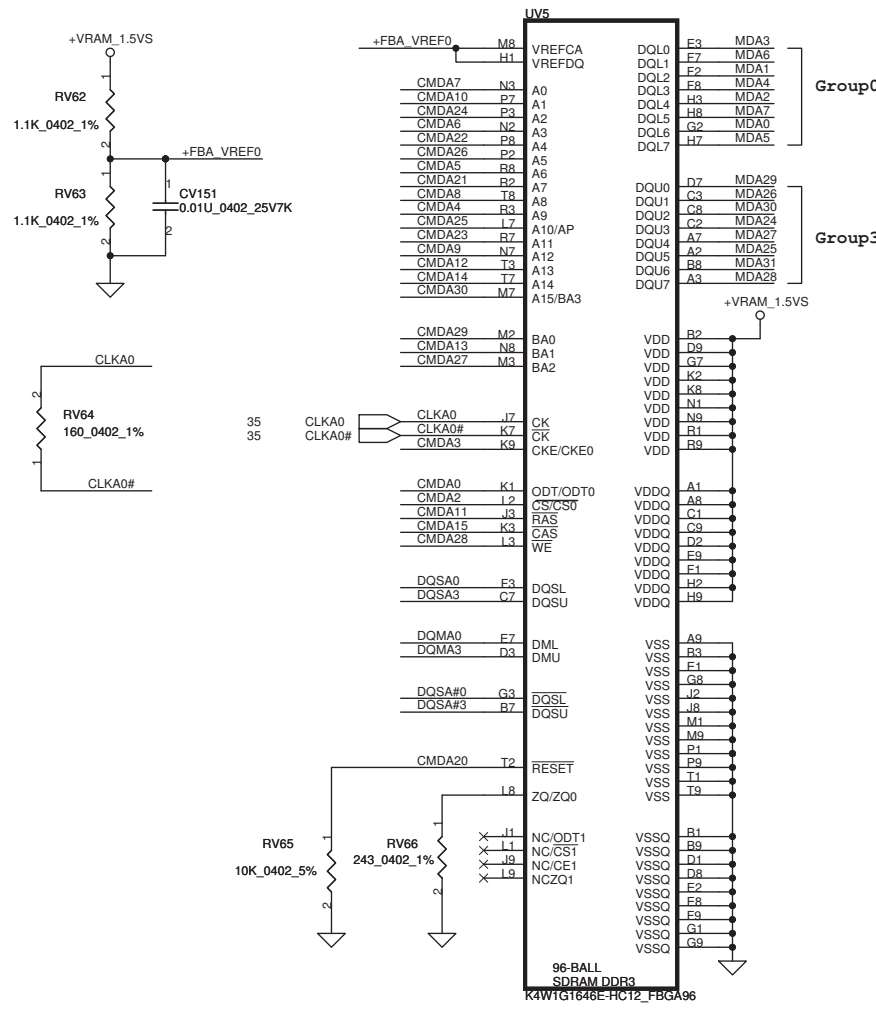
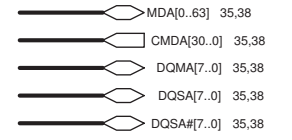
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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Title			<b>Compal Electronics, Inc.</b>	
Title			VGA(7/12)-MEM Interface C	
Size	Document Number	Rev		0.4
	LA-6961P			
Date:	Monday, January 24, 2011	Sheet	36	of 54

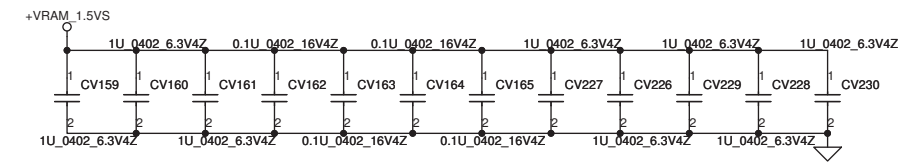
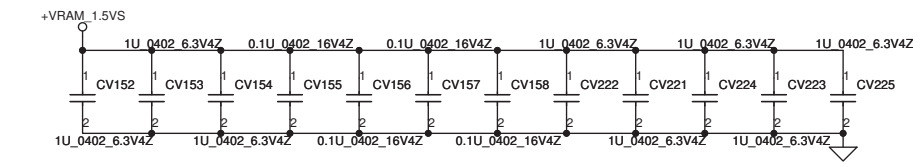


# Memory Partition A - Lower 32 bits



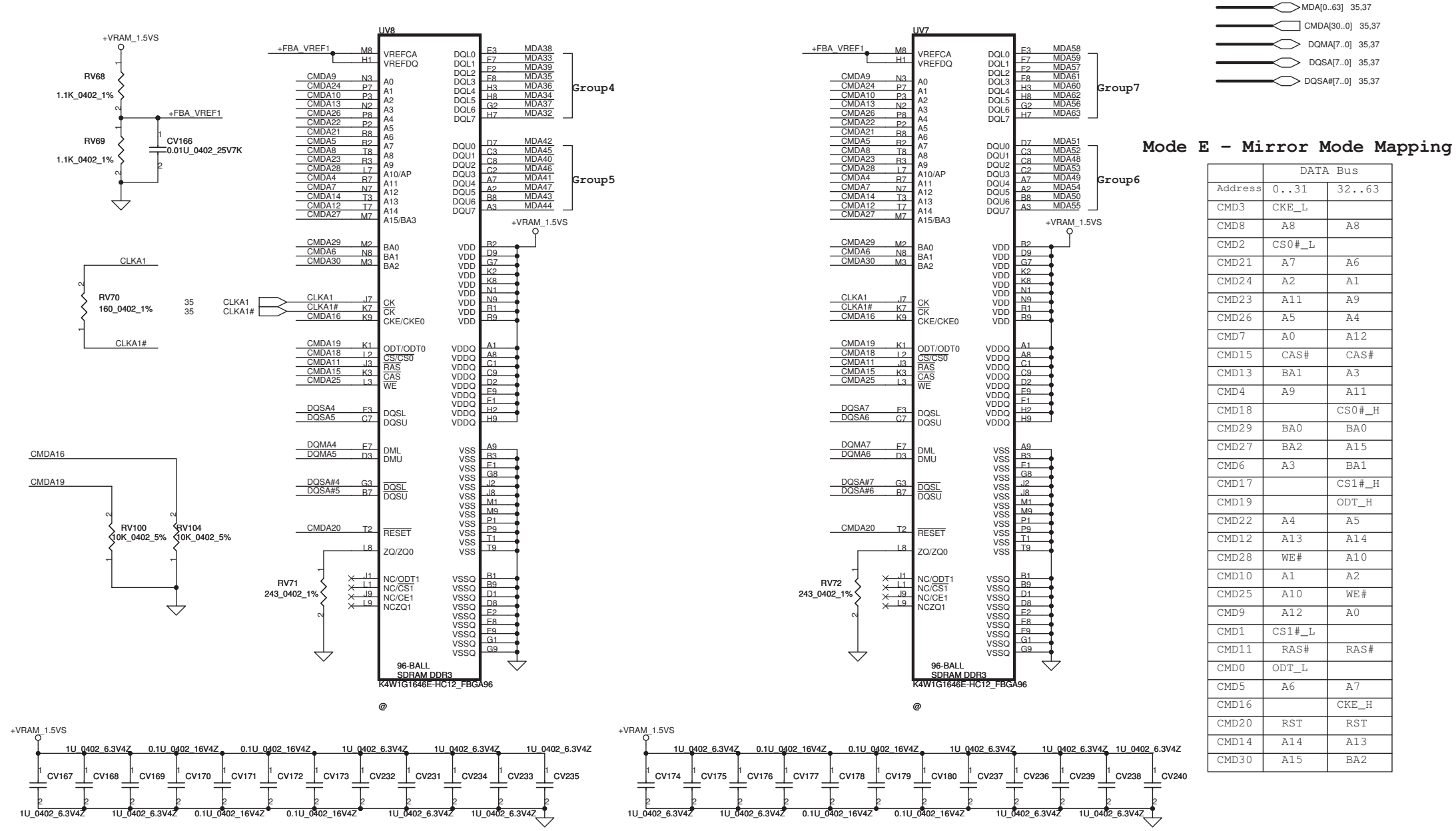
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Address	DATA Bus	
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CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



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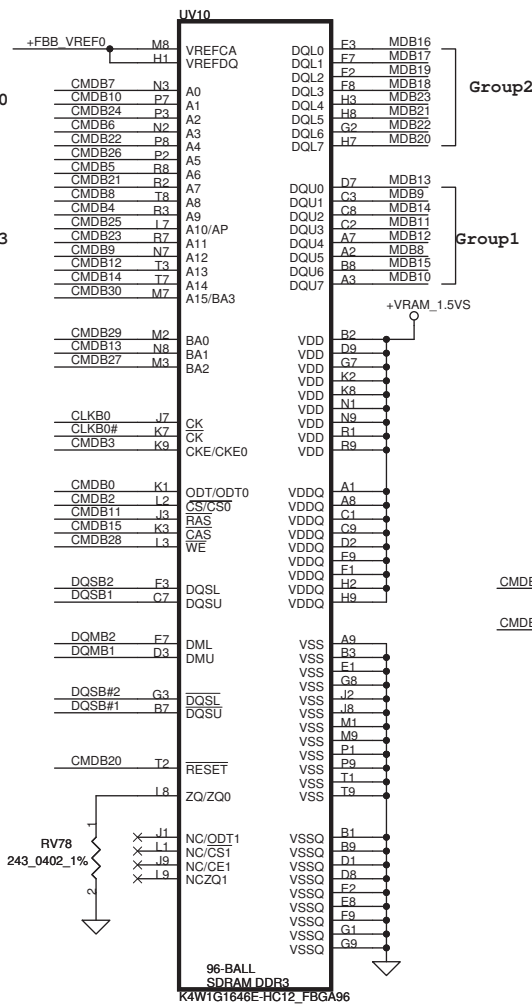
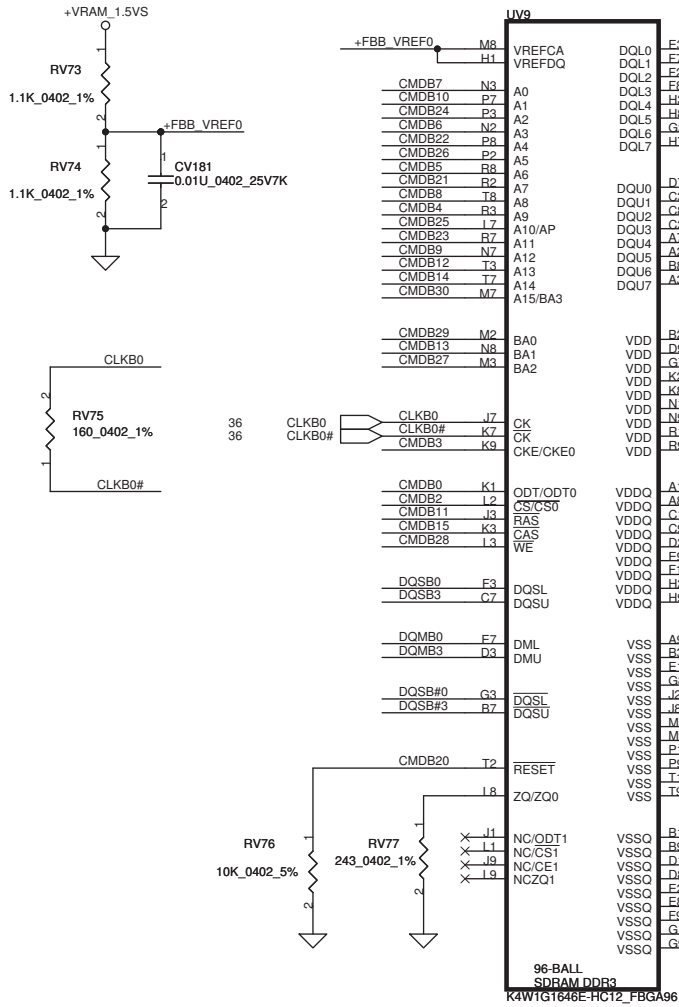
# Memory Partition A - Upper 32 bits <http://hobi-elektronika.net>



Security Classification		Compal Secret Data		Title <b>VGA(9/12)-VRAM A Upper</b>	
Issued Date	2010/05/27	Deciphered Date	2011/07/06		
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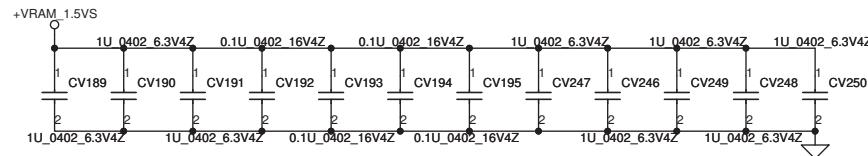
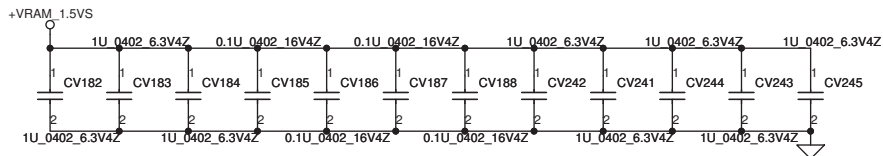
# Memory Partition C - Lower 32 bits

<http://hobi-elektronika.net>



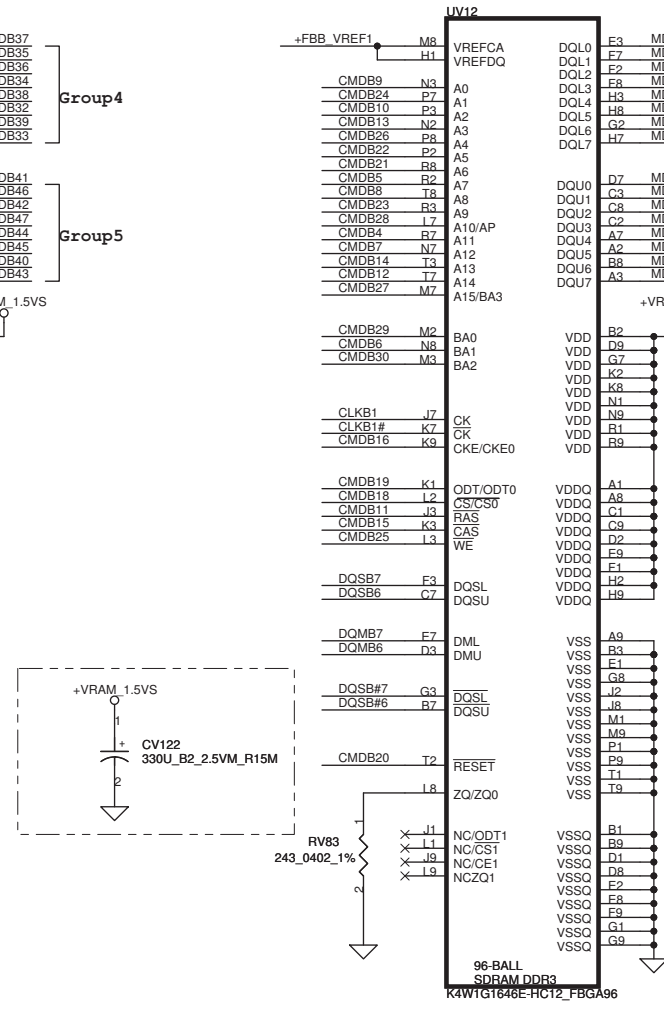
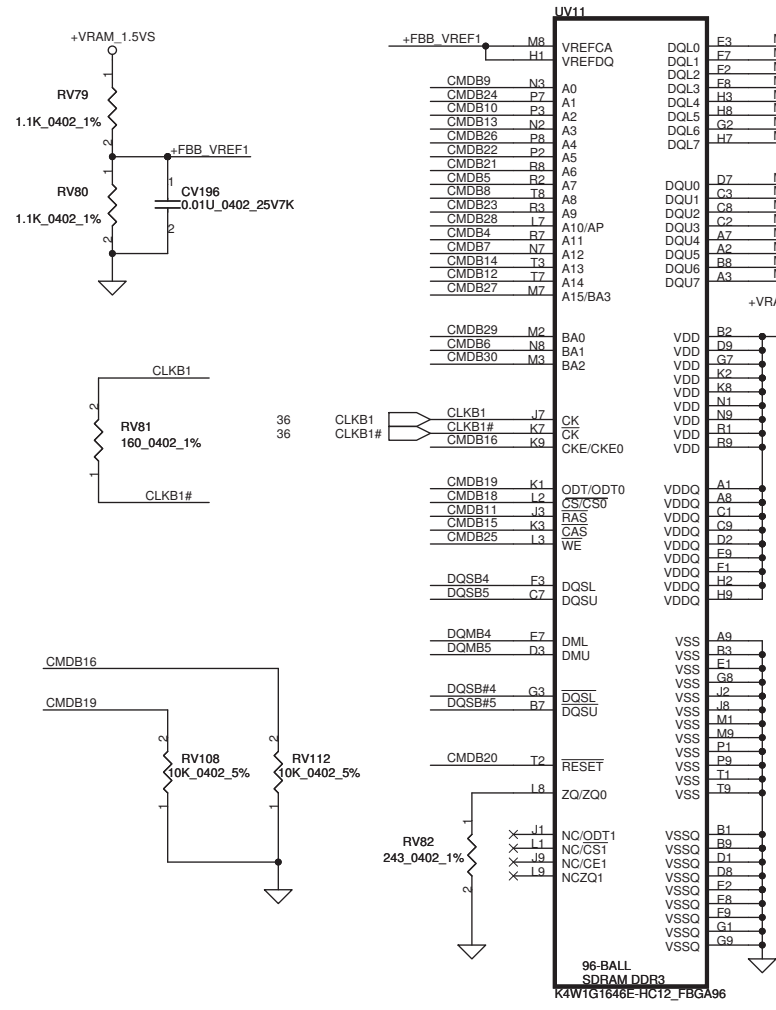
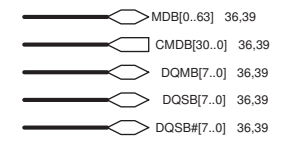
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Address	DATA Bus	
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CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



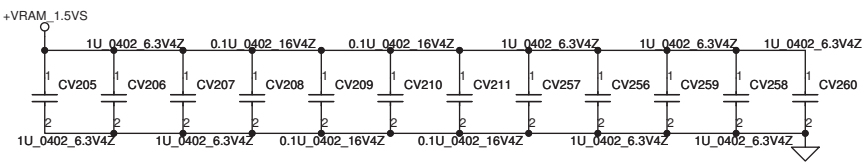
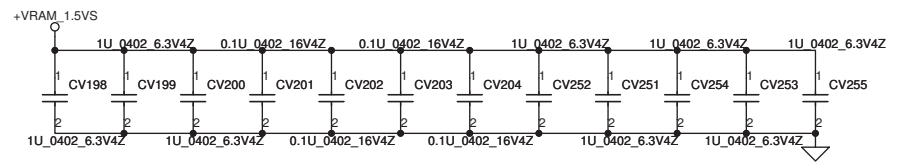
Security Classification		Compal Secret Data		Title	
Issued Date	2010/05/27	Deciphered Date	2011/07/06	VGA(10/12)-VRAM C Lower	
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				Custom	LA-6961P
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				Rev	0.4

# Memory Partition C - Upper 32 bits



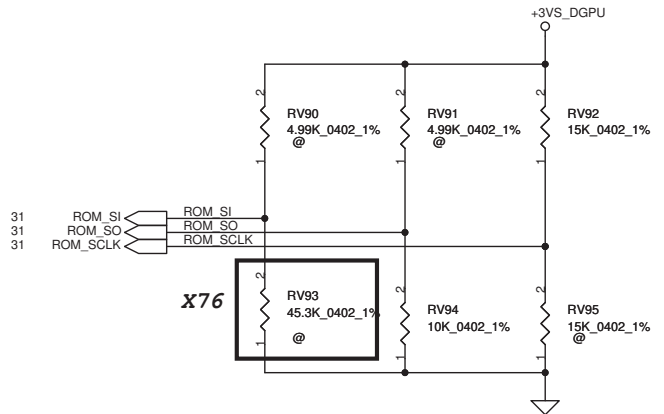
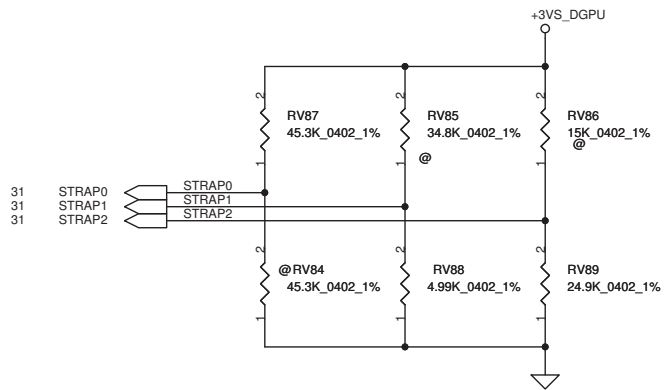
## Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD24	A7	A6
CMD4	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



Security Classification		Compal Secret Data		Title <b>VGA(11/12)-VRAM C Upper</b>	
Issued Date	2010/05/27	Deciphered Date	2011/07/06		
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Physical Strapping pin	Physical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]
				USER[0]



Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12M-GE	0x0A7A	Pull up 15K	Pull up 15K
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K

N12P-GS-A1 :  
 ROM\_SO : PL-10K  
 ROM\_CLK : PH-15K  
 ROM\_SI : PL45.3K (Samsung 2GB)  
 Strap 2 : PL-5K  
 Strap 1 : PH-35K  
 Strap 0 : PH-45K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S20	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646E-HC11 SA000041T00	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q00	2GB	0111	PD 45.3K(SD034453280)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG		
3GIO_PADCFG[3:0]		
0110	Notebook Default	

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

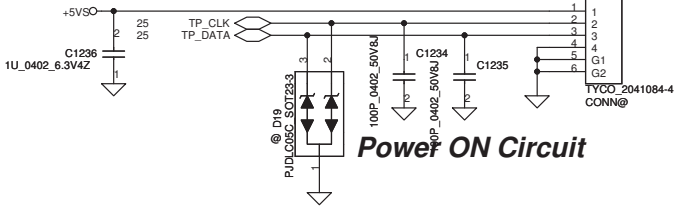
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

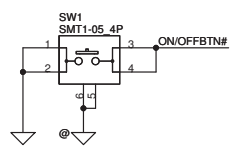
Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> Title <b>VGA(12/12)-MISC</b>	
Issued Date	2010/05/27	Deciphered Date	2011/07/06		
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**Touch pad Connector**

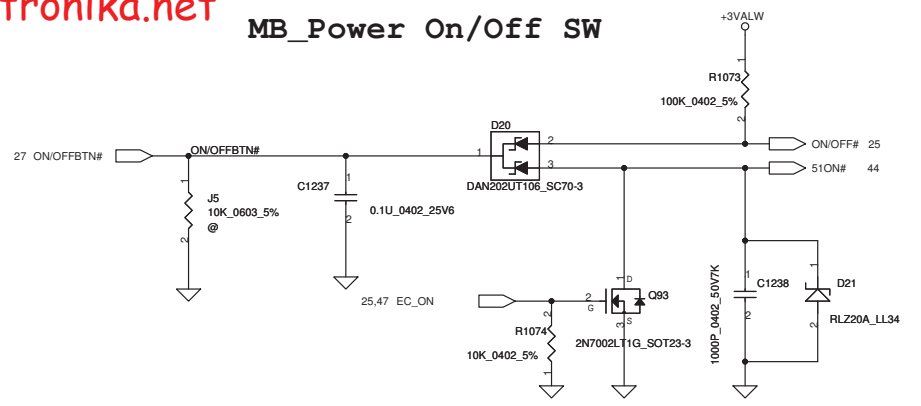


**Power ON Circuit**

**For Debug Only**

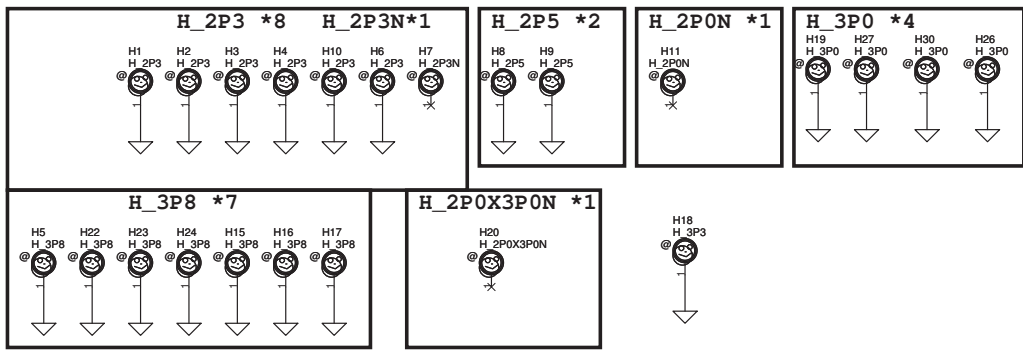
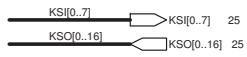
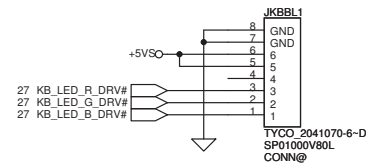


**MB\_Power On/Off SW**

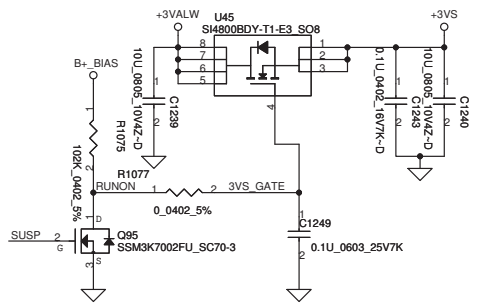


KSO8 @C736	100P_0402_25V8K	100P_0402_25V8K	C737@	KSI7
KSI3 @C738	100P_0402_25V8K	100P_0402_25V8K	C739@	KSI6
KSO9 @C740	100P_0402_25V8K	100P_0402_25V8K	C741@	KSI5
KSI2 @C742	100P_0402_25V8K	100P_0402_25V8K	C743@	KSO0
KSI1 @C744	100P_0402_25V8K	100P_0402_25V8K	C745@	KSO1
KSO10 @C746	100P_0402_25V8K	100P_0402_25V8K	C747@	KSO2
KSO11 @C750	100P_0402_25V8K	100P_0402_25V8K	C751@	KSI4
KSI0 @C752	100P_0402_25V8K	100P_0402_25V8K	C753@	KSO3
KSO12 @C754	100P_0402_25V8K	100P_0402_25V8K	C755@	KSO4
KSO13 @C756	100P_0402_25V8K	100P_0402_25V8K	C757@	KSO5
KSO14 @C760	100P_0402_25V8K	100P_0402_25V8K	C761@	KSO6
KSO15 @C762	100P_0402_25V8K	100P_0402_25V8K	C763@	KSO7
KSO16 @C764	100P_0402_25V8K			

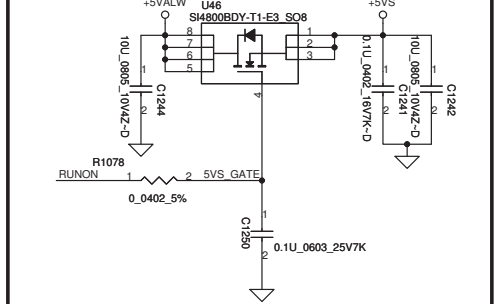
KSI7	1
KSI6	2
KSI4	3
KSI2	4
KSI5	5
KSI1	6
KSI3	7
KSI0	8
KSO5	9
KSO4	10
KSO7	11
KSO6	12
KSO8	13
KSO3	14
KSO1	15
KSO2	16
KSO0	17
KSO12	18
KSO13	19
KSO15	20
KSO13	21
KSO14	22
KSO9	23
KSO11	24
KSO10	25



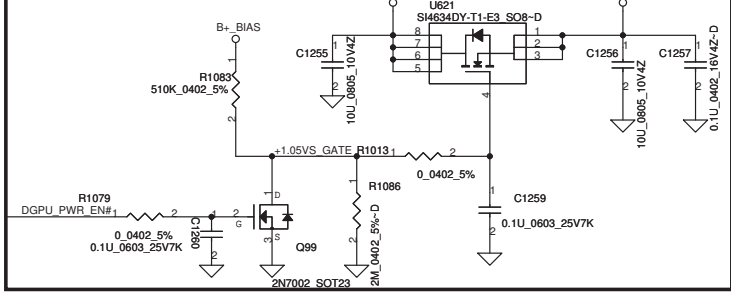
### +3VALW to +3VS Transfer



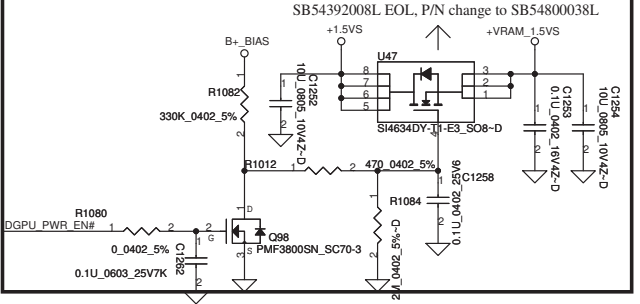
### +5VALW to +5VS Transfer



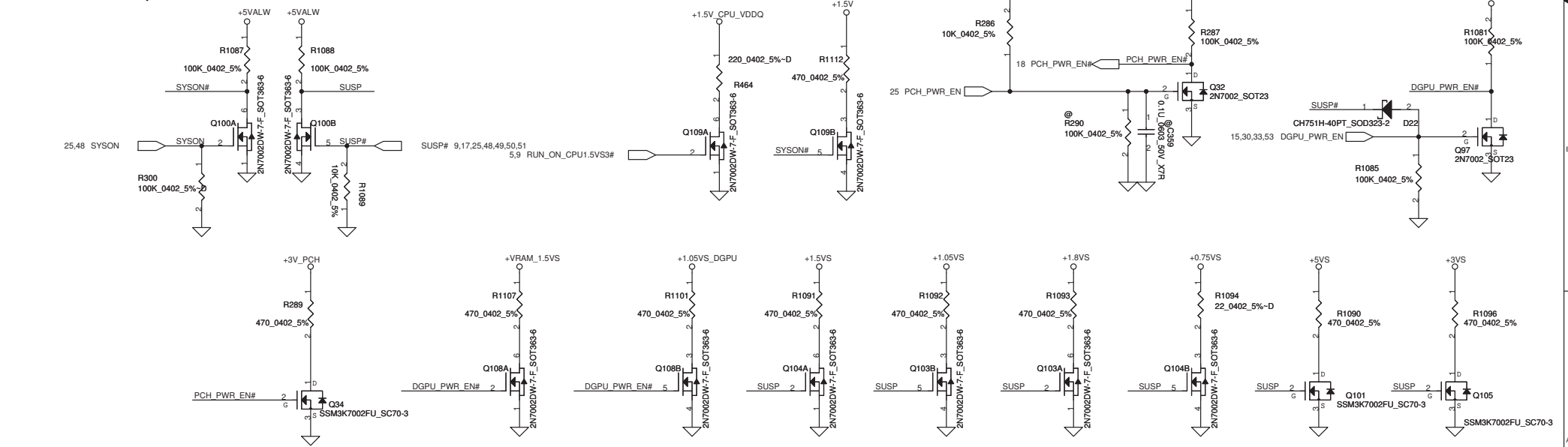
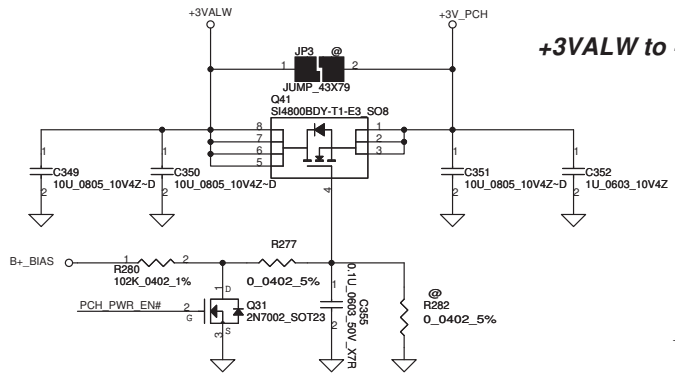
### +1.05V to +1.05VS\_DGPU Transfer



### +1.5VS to +1.5VSDGPU Transfer



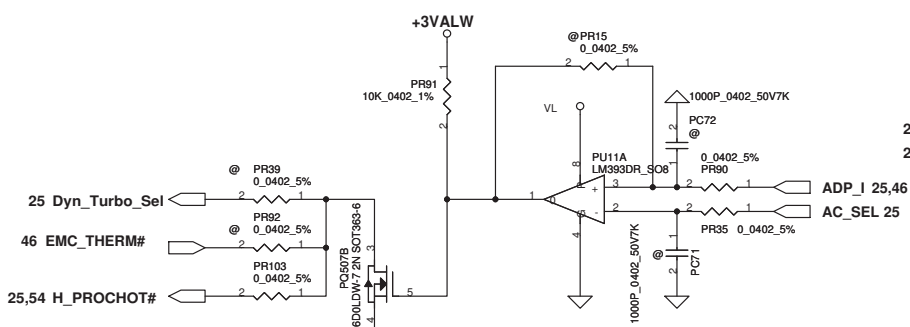
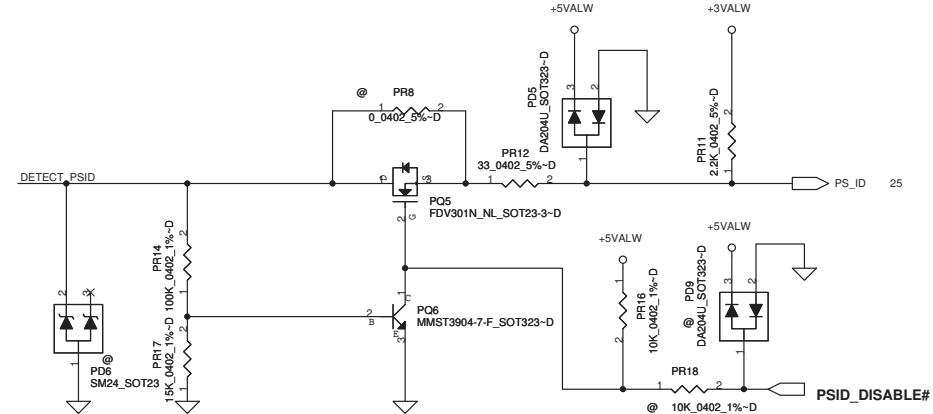
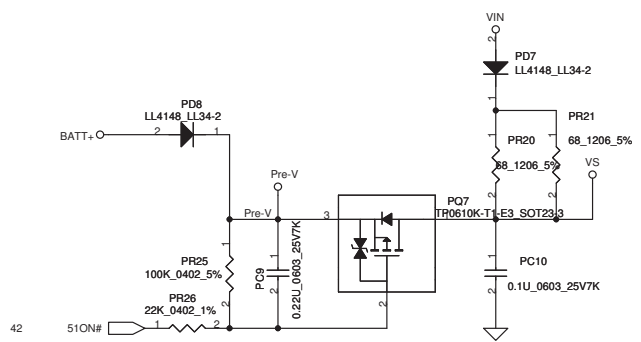
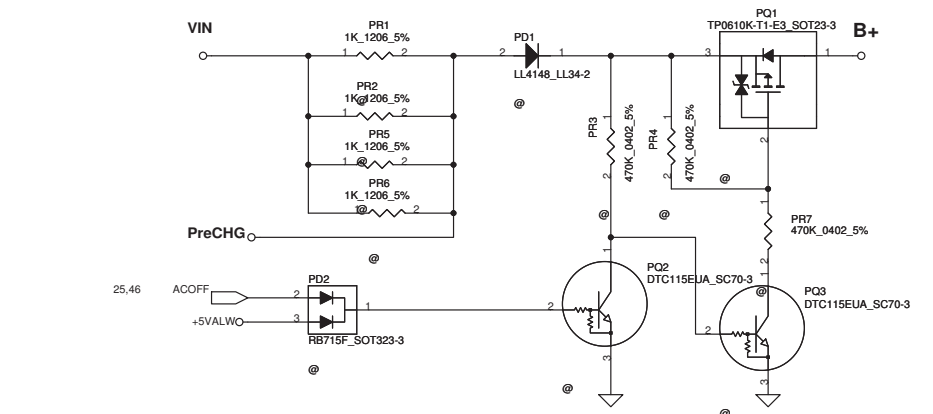
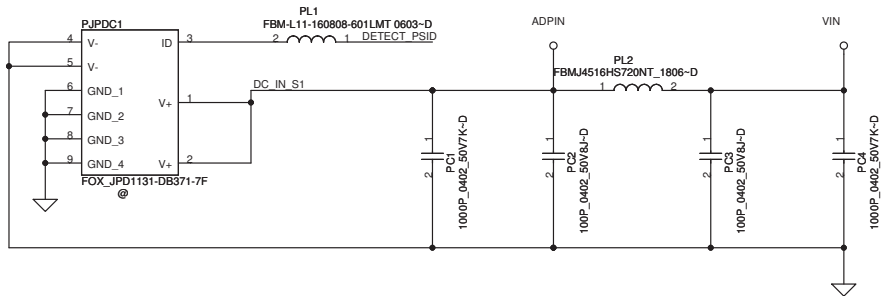
### +3VALW to +3V\_PCH Transfer



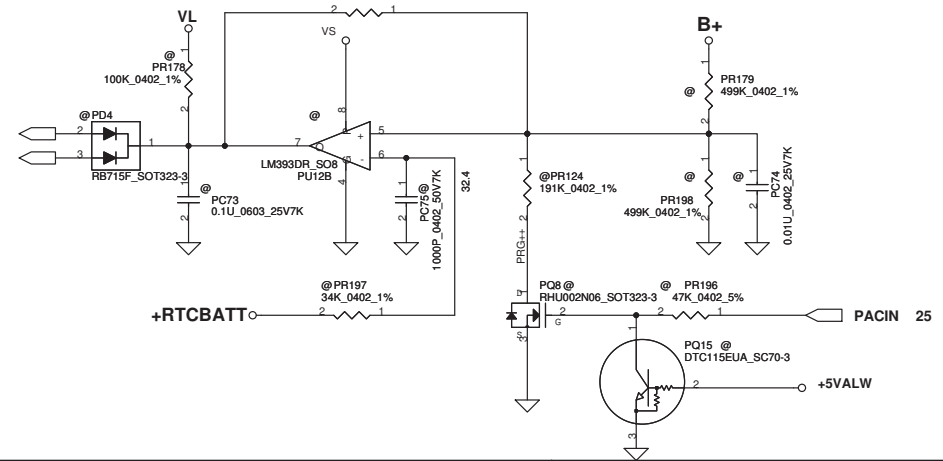
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Issued Date	2009/07/25	Deciphered Date	2011/07/06
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<b>DC/DC INTERFACE</b>			
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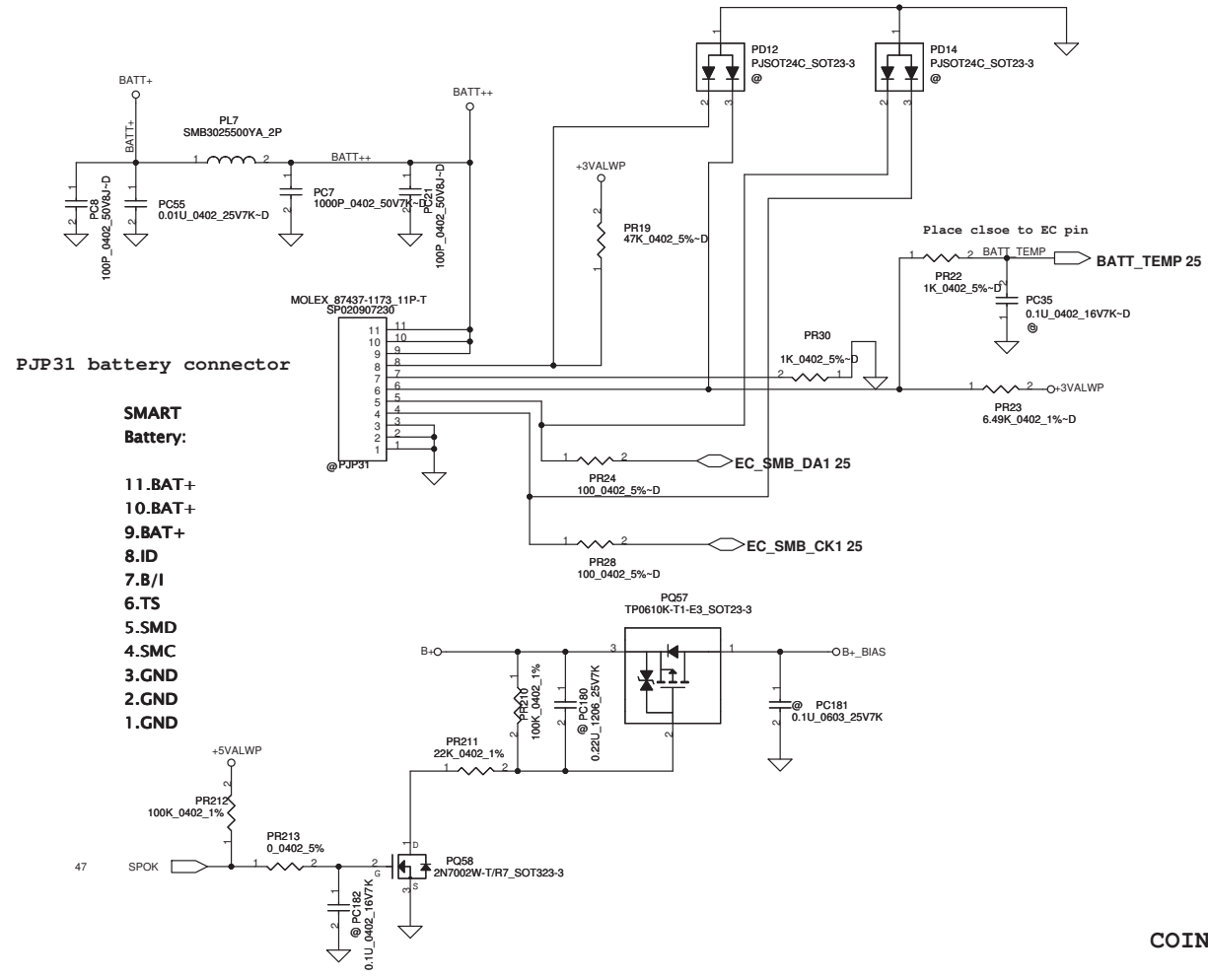




25,54 MAINPWN  
25,54 ACON



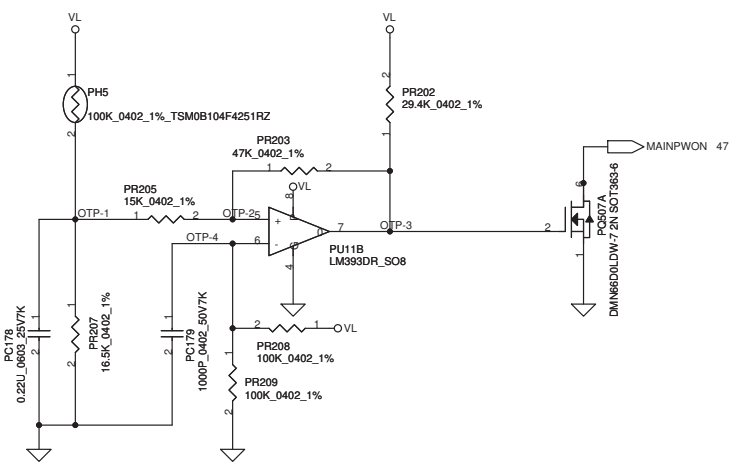
Security Classification		Compal Secret Data		Title	
Issued Date	2009/12/01	Deciphered Date	2010/05/28	PWR-DCIN / Vin Detector	
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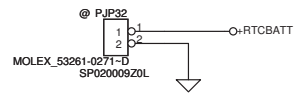
- SMART Battery:**
- 11.BAT+
  - 10.BAT+
  - 9.BAT+
  - 8.ID
  - 7.B/I
  - 6.TS
  - 5.SMD
  - 4.SMC
  - 3.GND
  - 2.GND
  - 1.GND

**Battery Connect/OTP**

PH3 under CPU bottom side :  
CPU thermal protection at 90 degree C  
Recovery at 50 degree C



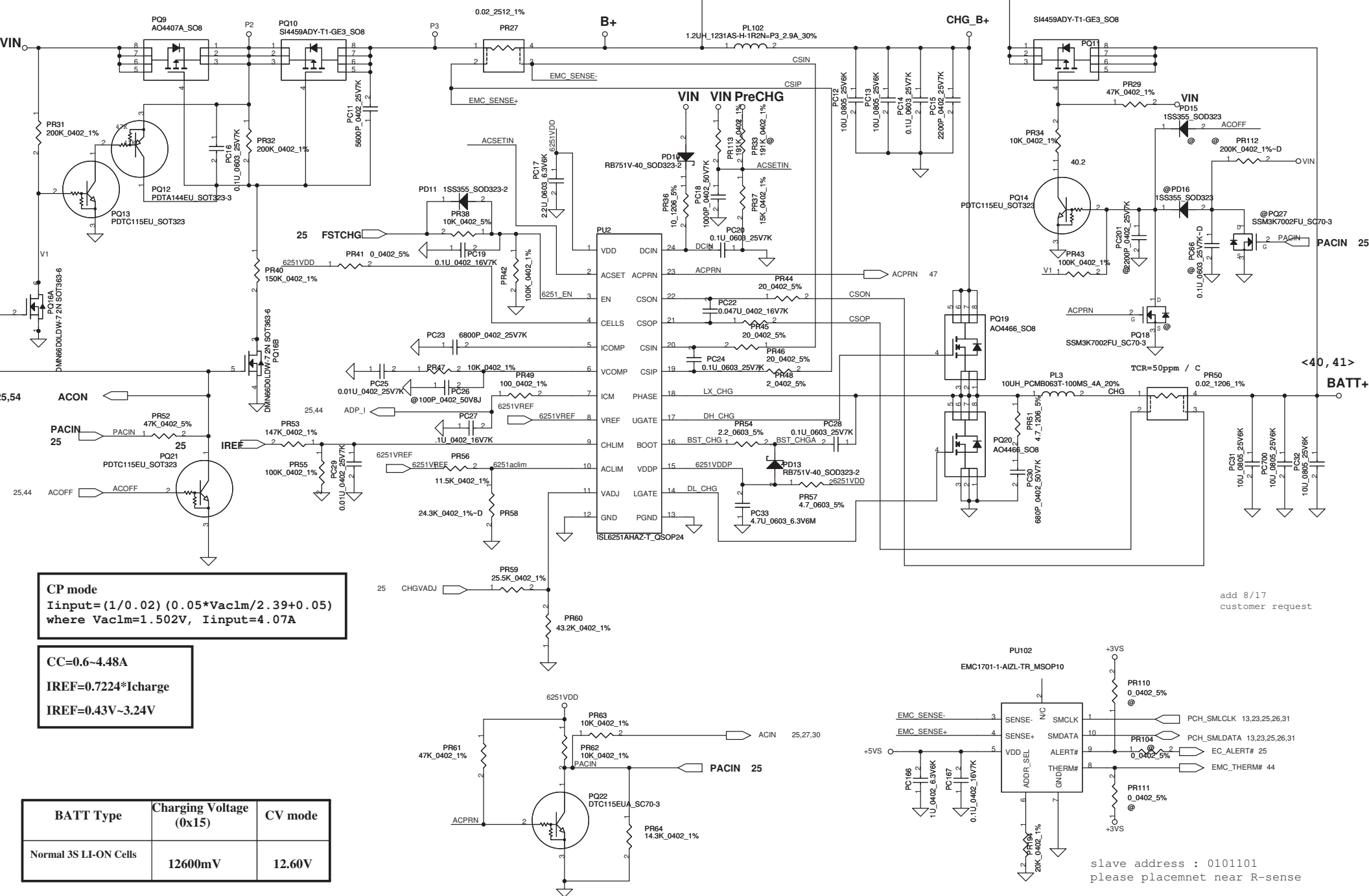
**COIN RTC Battery**



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				<b>PWR-BATTERY CONN</b>
				Size
				Custom
				Customer
				Rev
				0.1
				Date
				Monday, January 24, 2011
				Sheet
				45 of 54

Iada=0~4.74A (90W/19V=4.736A)

ADP\_I = 19.9 \* Iadapter \* Rsense

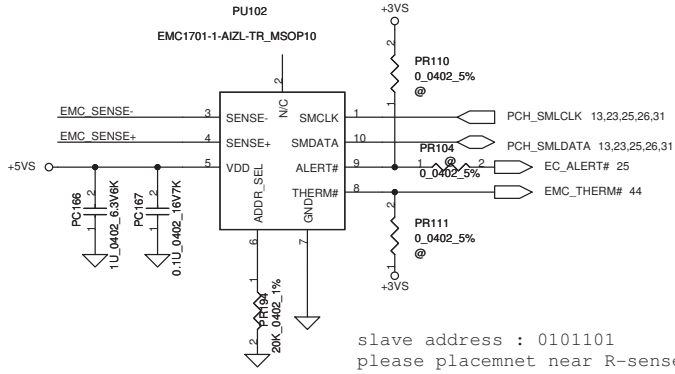


**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 1.502V$ ,  $I_{input} = 4.07A$

**CC=0.6-4.48A**  
 $I_{REF} = 0.7224 * I_{charge}$   
 $I_{REF} = 0.43V - 3.24V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

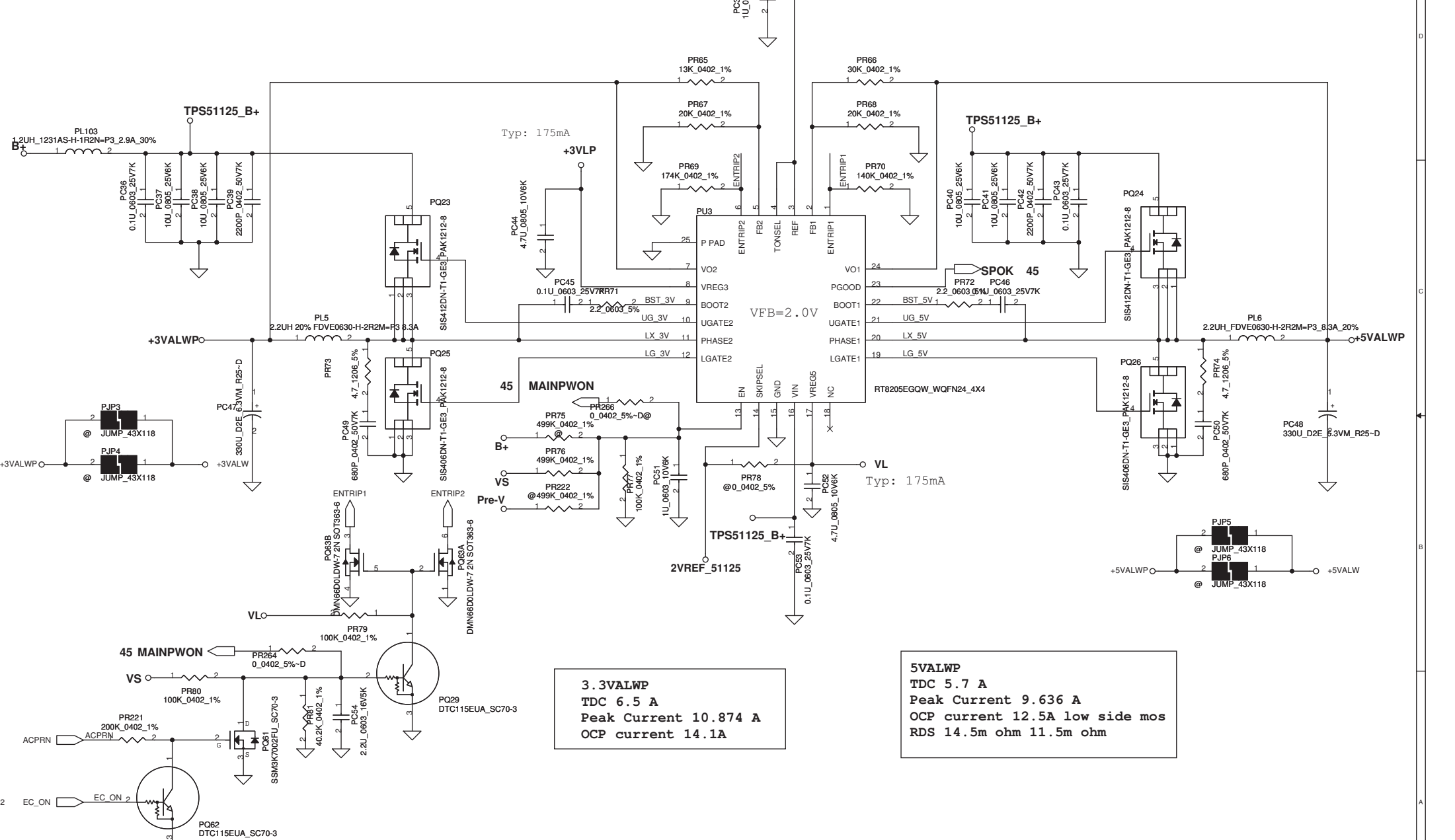
add 8/17 customer request



slave address : 0101101  
 please placemnet near R-sense

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Issued Date	2009/12/01	Deciphered Date	2010/05/28	PWR-CHARGER	
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Note:  
 Use TPS51125 IC can remove RTC refernece LDO  
 Use TPS51427 IC must keep RTC refernece LDO



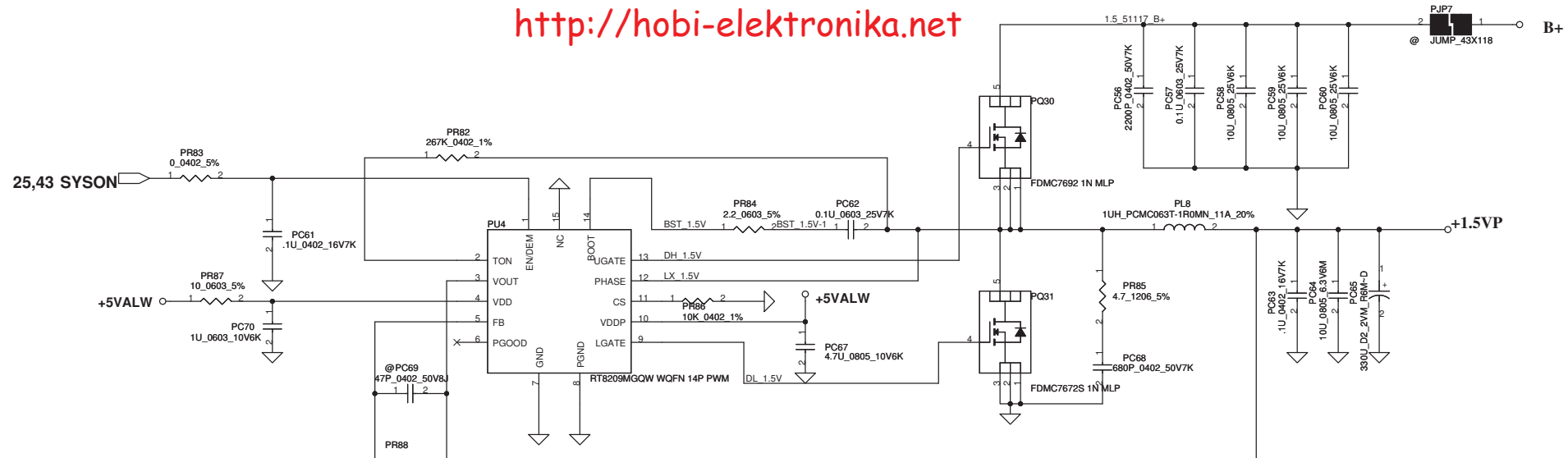
**3.3VALWP**  
 TDC 6.5 A  
 Peak Current 10.874 A  
 OCP current 14.1A

**5VALWP**  
 TDC 5.7 A  
 Peak Current 9.636 A  
 OCP current 12.5A low side mos  
 RDS 14.5m ohm 11.5m ohm

Security Classification	Compal Secret Data	
Issued Date	2009/12/01	Deciphered Date
		2010/05/28

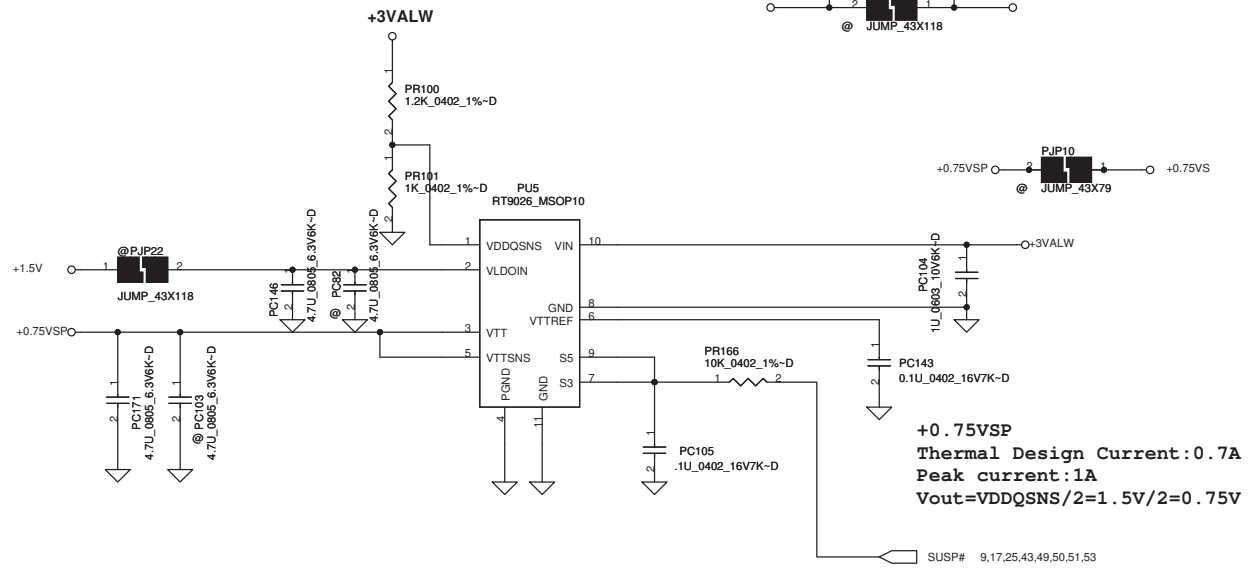
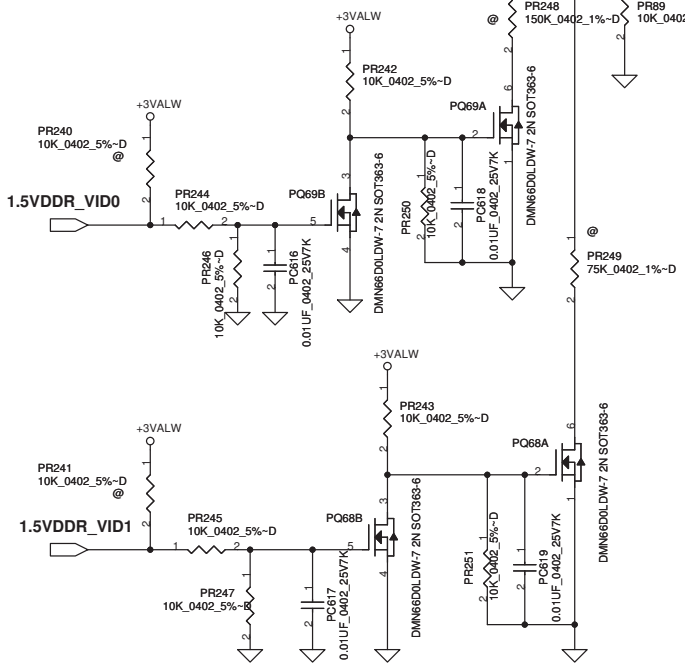
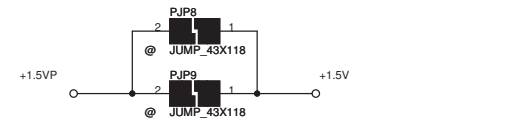
<b>Compal Electronics, Inc.</b>		
Title		
<b>3VALWP/5VALWP</b>		
Size	Document Number	Rev
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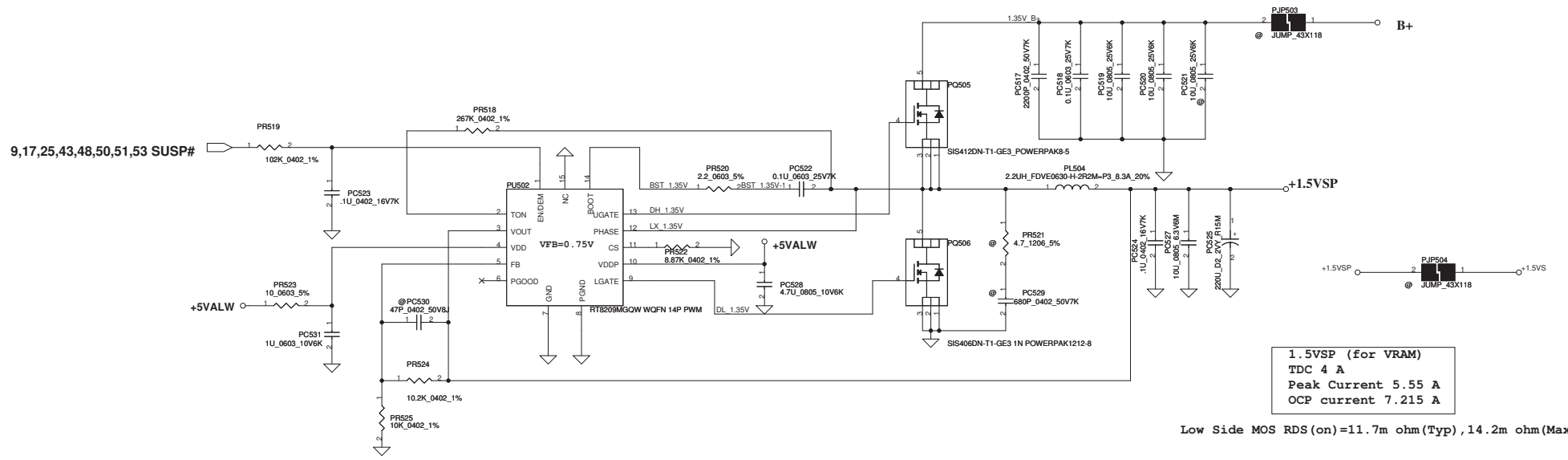


DDR GPIO Output Voltage Selection		
bit2 = 1.5DDR_VID0	bit1 = 1.5DDR_VID1	DDR Vout
0	0	1.65V
0	1	1.6V
1	0	1.55V
1	1	1.5V (Default)

**1.5VP**  
**TDC 8.9A**  
**Peak Current 12.72 A**  
**OCp current 16.5A**  
**low side mos RDS 4.5ohm 3.6ohm**



**+0.75VSP**  
**Thermal Design Current: 0.7A**  
**Peak current: 1A**  
**Vout=VDDQSNS/2=1.5V/2=0.75V**

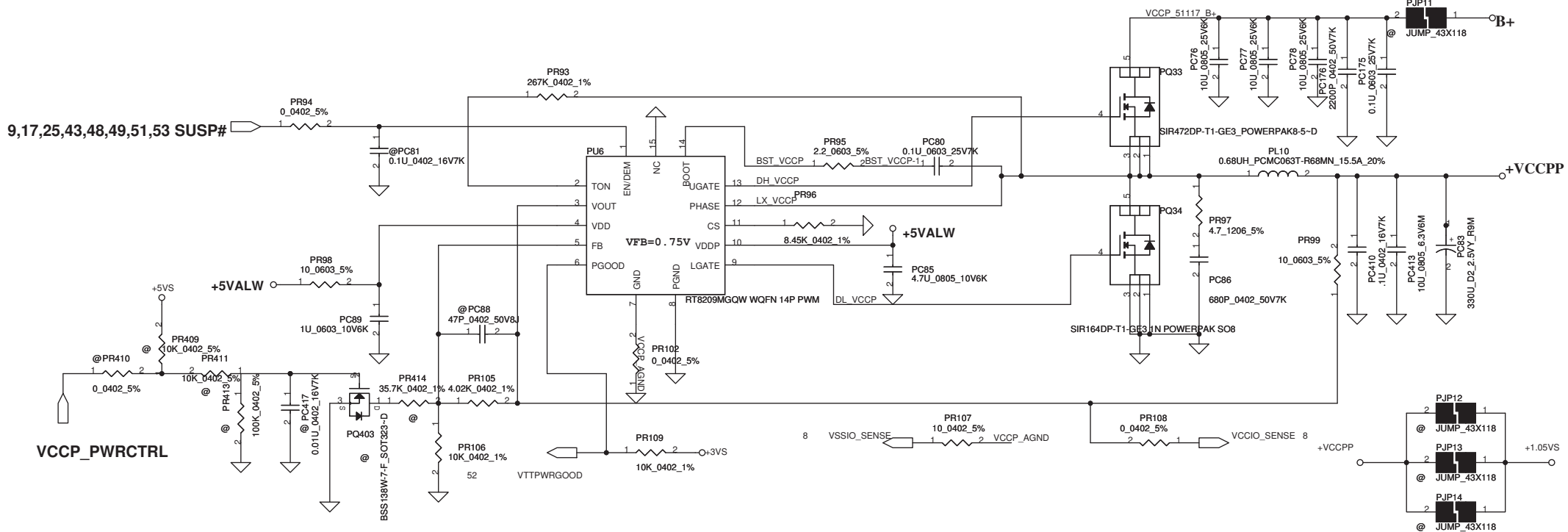


1.5VSP (for VRAM)  
 TDC 4 A  
 Peak Current 5.55 A  
 OCP current 7.215 A

Low Side MOS RDS(on)=11.7m ohm(Typ) , 14.2m ohm(Max)

9,17,25,43,48,50,51,53 SUSP#

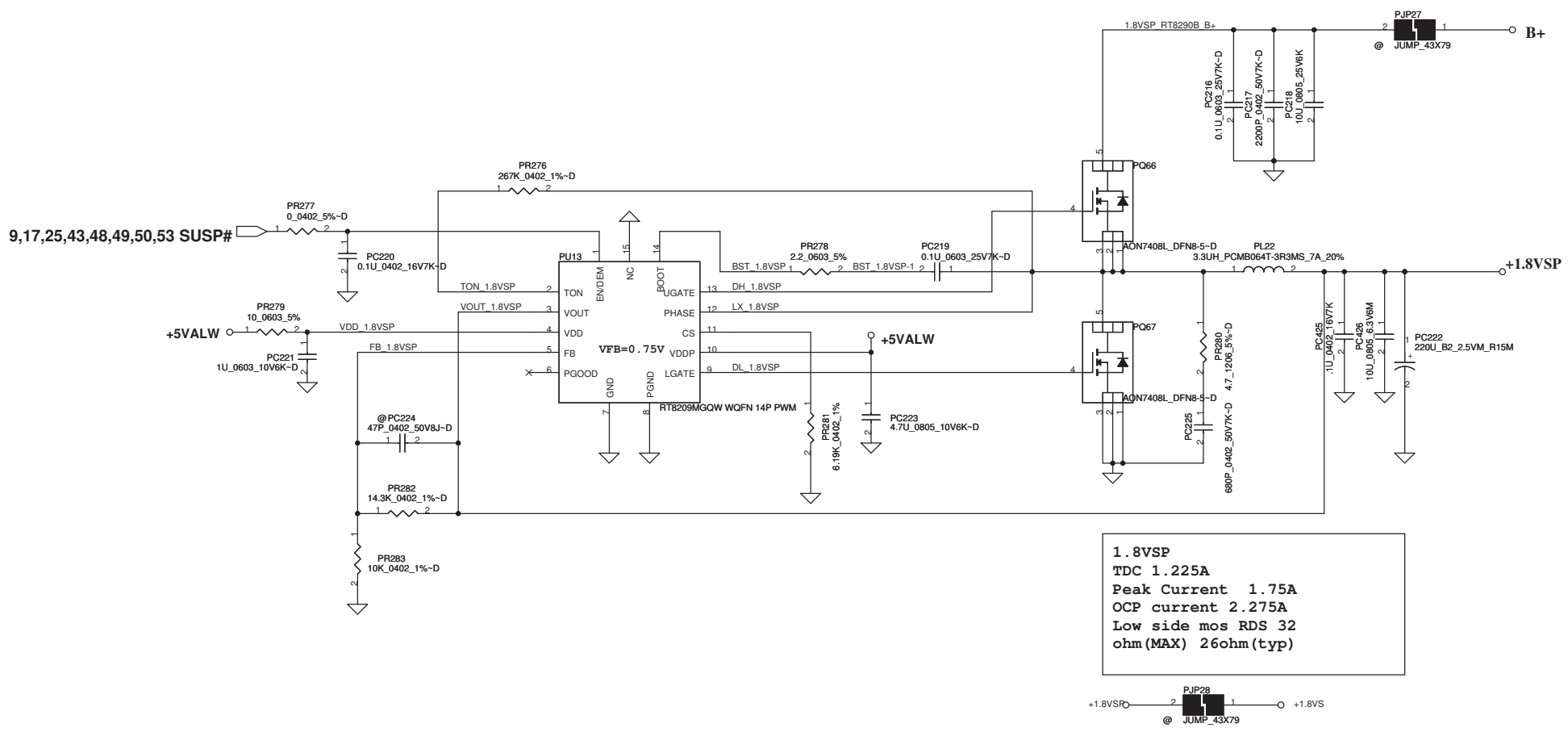
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Issued Date	2010/08/03	Deciphered Date	2011/08/03	Title
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VCCP  
 TDC 11.5 A  
 Peak Current 16.458 A  
 OCP 21.4 currentA  
 low side mos RDS 4.5 ohm(MAX)  
 3.6ohm(MAX)

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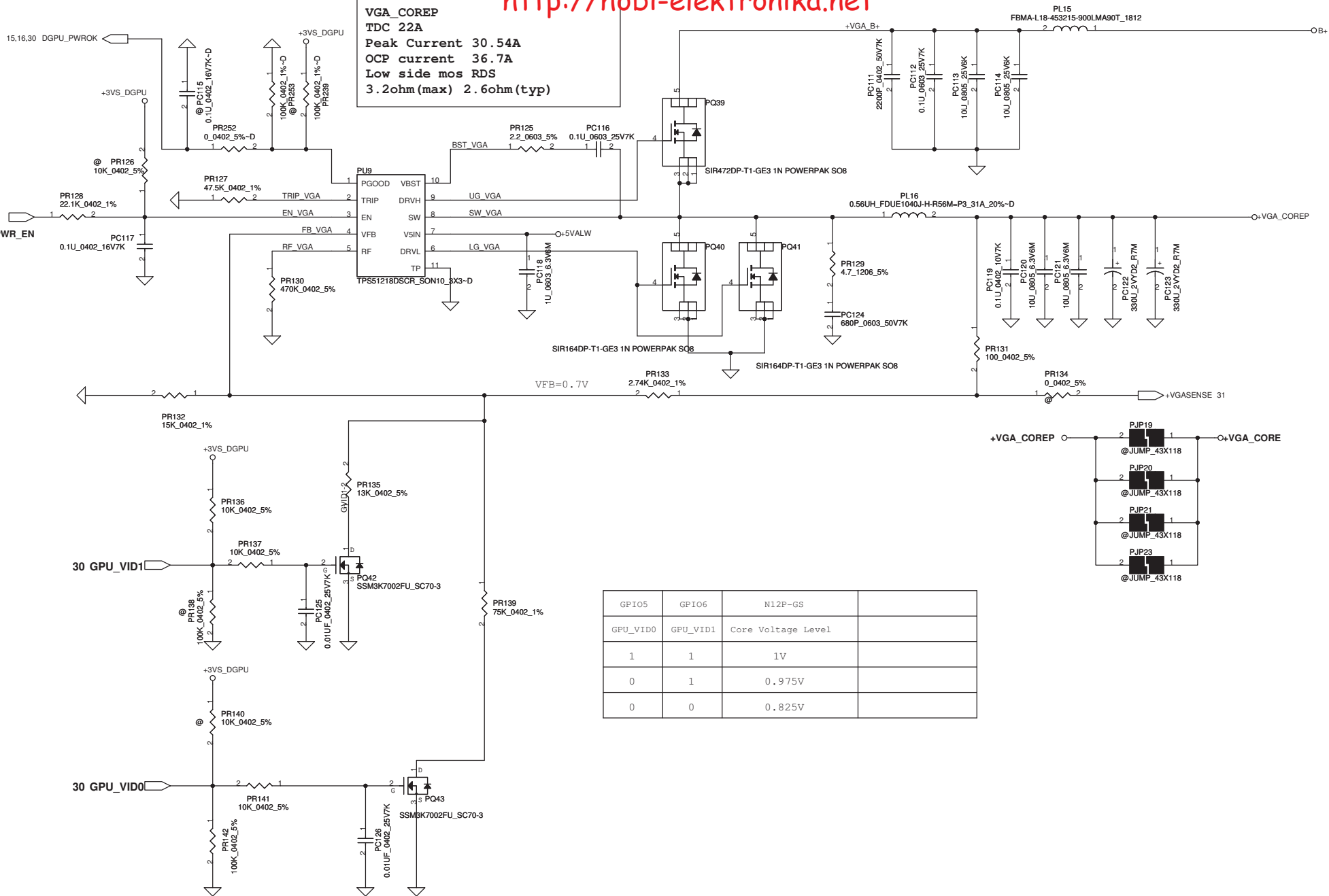




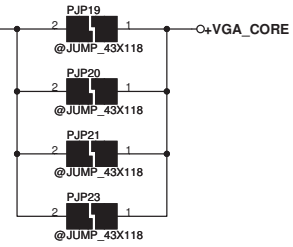
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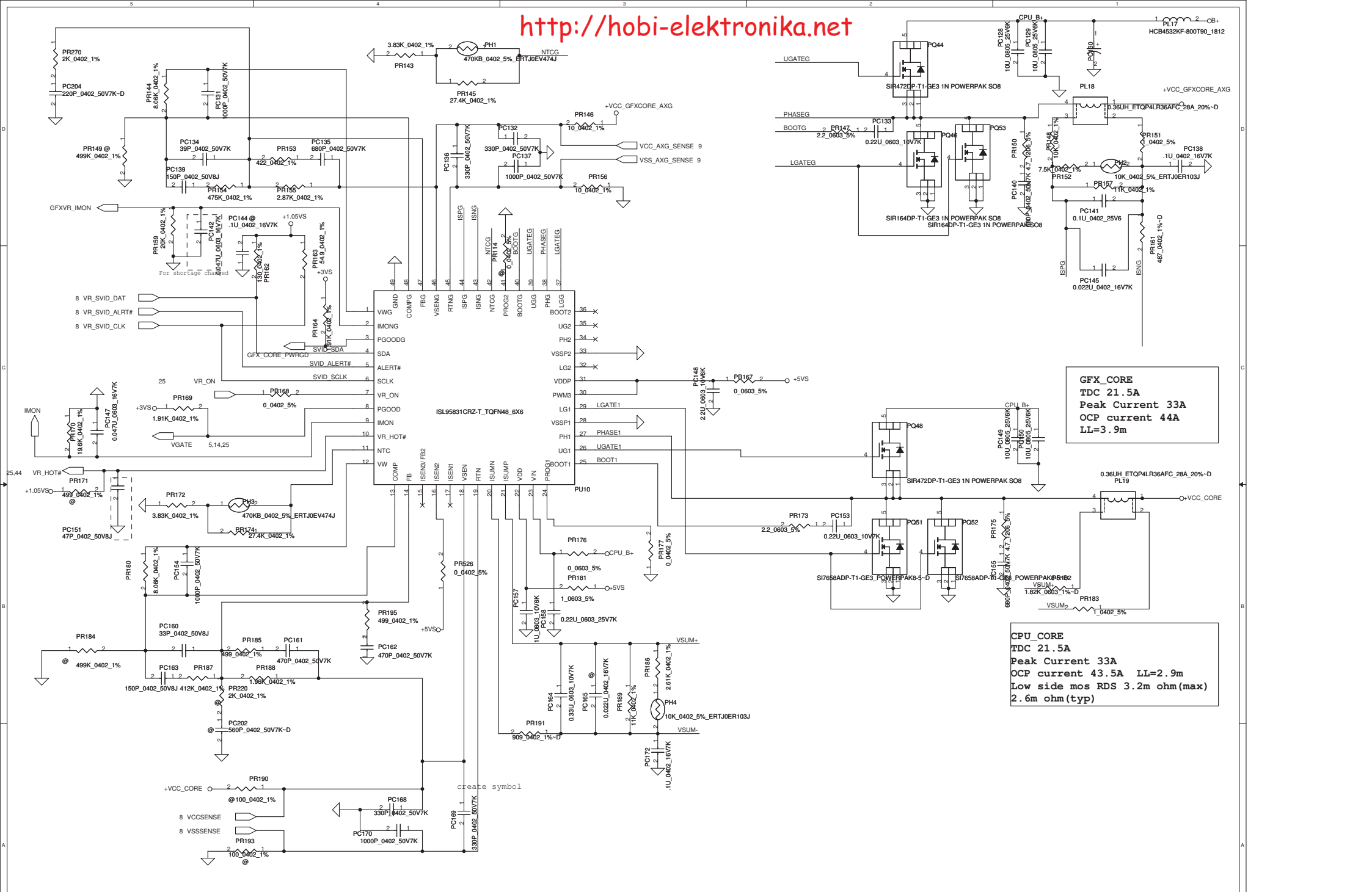


**VGA\_COREP**  
**TDC 22A**  
**Peak Current 30.54A**  
**OCP current 36.7A**  
**Low side mos RDS**  
**3.2ohm(max) 2.6ohm(typ)**



GPIO5	GPIO6	N12P-GS	
GPU_VID0	GPU_VID1	Core Voltage Level	
1	1	1V	
0	1	0.975V	
0	0	0.825V	





**GFX\_CORE**  
 TDC 21.5A  
 Peak Current 33A  
 OCP current 44A  
 LL=3.9m

**CPU\_CORE**  
 TDC 21.5A  
 Peak Current 33A  
 OCP current 43.5A  
 LL=2.9m  
 Low side mos RDS 3.2m ohm(max)  
 2.6m ohm(typ)

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				<b>PWR +CPU_CORE+VGFY CORE</b>
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Item	Reason for change	PG#	Modify List	Date	Phase
1	SYSON signal Pull low	43	Add R300	2010/10/15	PT
2	Q21 Reverse	25	Change Q21 DS pin	2010/10/15	PT
3	Fan voltage need to stable	26	Add C1923	2010/10/15	PT
4	Timing change	5	Add RC127,RC128,and Change BOM RC6 resrve	2010/10/15	PT
5	Leakge +3vs	13	Change BOM RH95 to resrve	2010/10/15	PT
6	EA crystal fail	25	Change BOM of C287,C288	2010/10/15	PT
7	EA crystal fail	13	Change BOM of CH23,CH24	2010/10/15	PT
8	EA crystal fail	21	Change BOM of CL18,CL19	2010/10/15	PT
9	High pot	21	Change CL39 to SB120102R1L	2010/10/15	PT
10	DFX request	42	Change JKB1 symbol	2010/10/15	PT
11	ME request	23	Change JBT1 symbol	2010/10/15	PT
12	PCH change version	12	Change BOM UH1 SA00004IV0L	2010/10/15	PT
13	Control LAN LED limiting light	21	Add series connection RL26,RL25,Change BOM RL20 to 0ohm	2010/10/17	PT
14	HuronRiver DC updated for HAD_SYNC pull-down 1M ohm	12	Add RH275 resistor connect to HDA_SYNC_R & GND	2010/10/17	PT
15	Control the LCD sequence for AUO requirement	20	Add R2005,R2006 to reserve EN_INVFWR & +LCDVDD solution	2010/10/17	PT
16	Control the LCD sequence for AUO requirement	20	Add R2013,R2014,Q305 to reserve INVFWR_B+ Discharg Circuit	2010/10/20	PT
17	USB3.0 controller change to UPD720200AF1DAPA	24	Add R1962,R1963 to UPD720200AF1DAPA solution	2010/10/20	PT
18	NV request	28	Change R463,R465 pin2 net to +3VS_DGPI	2010/10/22	PT
19	NV request	33	Change BOM of RV109,RV116 to 1Kohm	2010/10/22	PT
20	The double pull low	29	Change BOM R937 to resrve	2010/10/22	PT
21	Modify screw H18 for ME request	39	Change H18 symbol	2010/10/22	PT
22	The EC request	25	Change R1095 to EC_CRY2 net,	2010/10/22	PT
23	The EC request	25	Change BOM R253 to 0ohm,R1095 to 100Kohm,C287,C288, X1 resrve	2010/10/24	PT
24	The EC request	25	Change BOM R225 to 8.2kohm	2010/10/24	PT
25	The EC request	25	Change R222 to 5V1	2010/10/26	PT
26	Intel request	12-19	Change BOM UH1 SA00004IV1L	2010/12/1	ST
27	Changed from +3vs to +valw to fix issue can't wake from S3 by port of USB3.0	24	Change BOM Del R1963 ,Add R1962	2010/12/1	ST
28	NV request	41	Change BOM RV88 to 4.99K ohm	2010/12/1	ST
29	Maximum derateing changed from 12V to 20V	9	Change BOM QC4 to SB00000HK0L	2010/12/1	ST
30	Maximum derateing changed from 2V to 2.5V	9	Change BOM CC176 to SGA00005H0L	2010/12/1	ST
31	EMI request	20	Add L5 to SM01000DH0L	2010/12/6	ST
32	EMI request	20	Change BOM CU63 to 100PF	2010/12/6	ST
33	EMI request	20	Change BOM CI167 to 22PF	2010/12/6	ST
34	GLAN orange LED too dark	21	Change BOM RL26 to 200ohm	2010/12/6	ST
35	The EC request	25	Add C1947 to SB071200J6L	2010/12/8	ST
36	The safety request	12	Change DH4 pin1,2,3	2010/12/8	ST
37	The USB3_SMI# signal change to GPFI04	15	Change UH1 pin C23 and H15	2010/12/8	ST
38	The DP Power Dongle	29	Add C110	2010/12/8	ST
39	The ME request	8	Change BOM C110 to C112	2010/12/9	ST
40	For ENE EC protect	20	1712 add D13, R395		
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Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HW Changed-List History-1</b>		
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