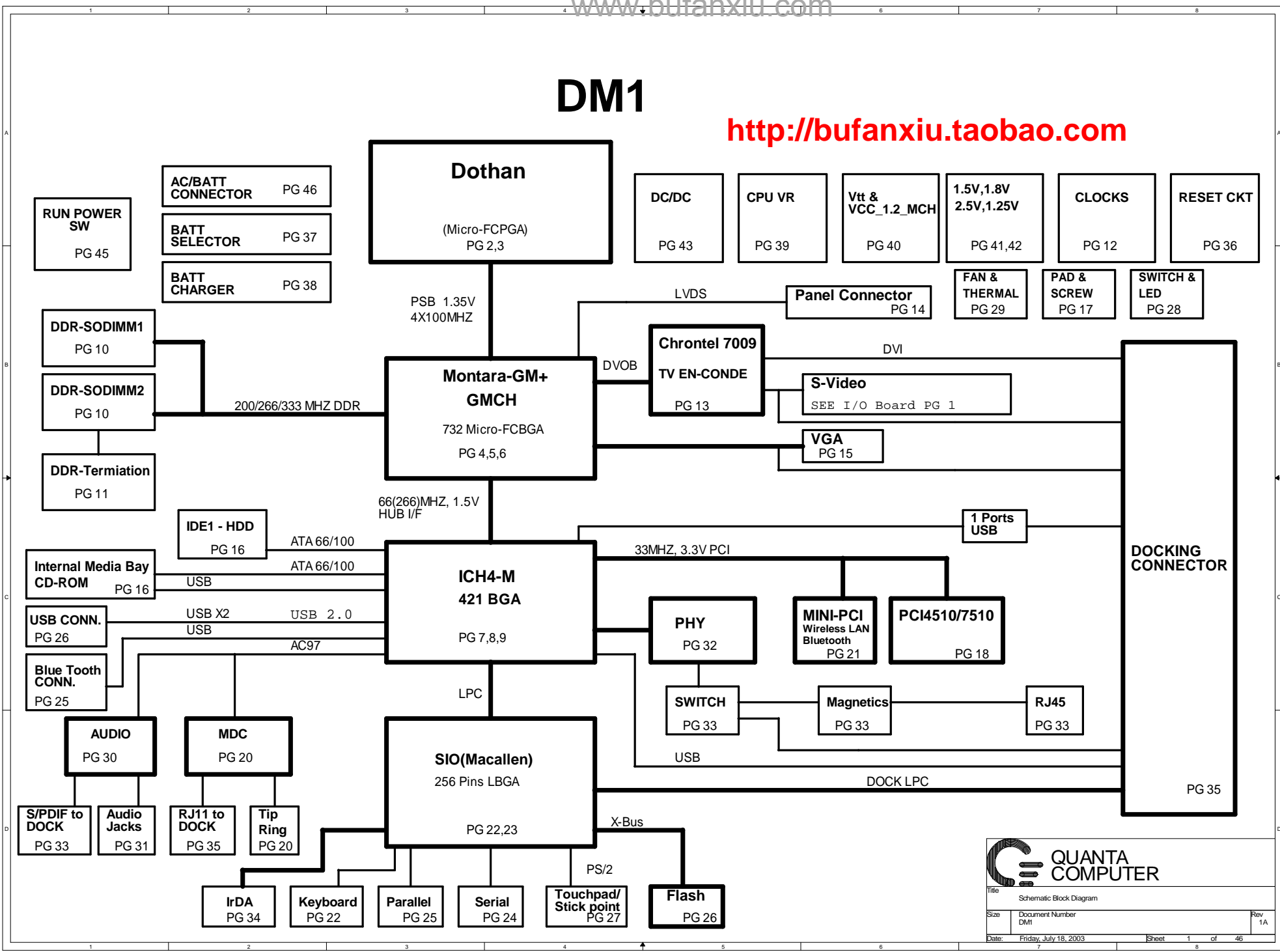
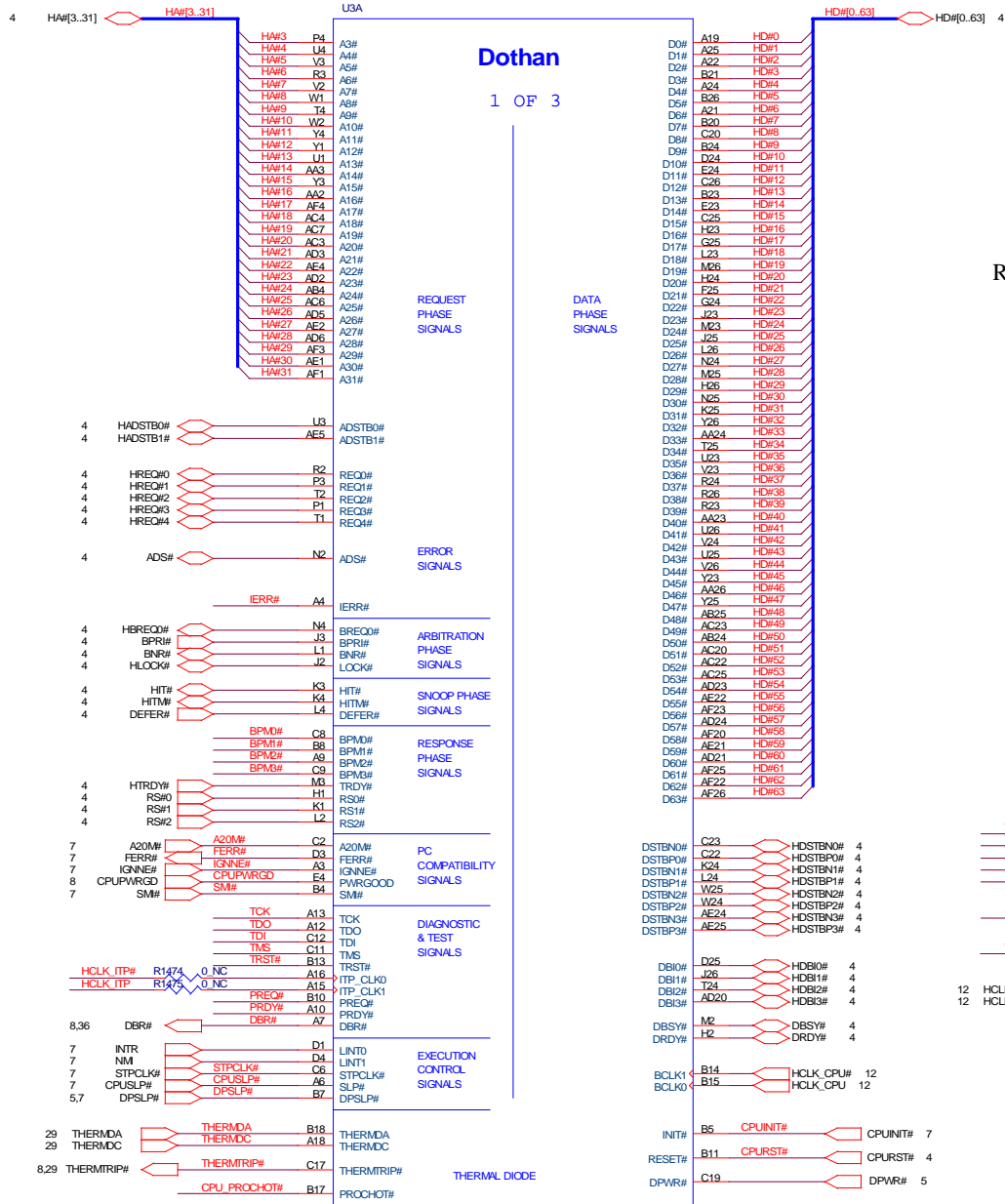


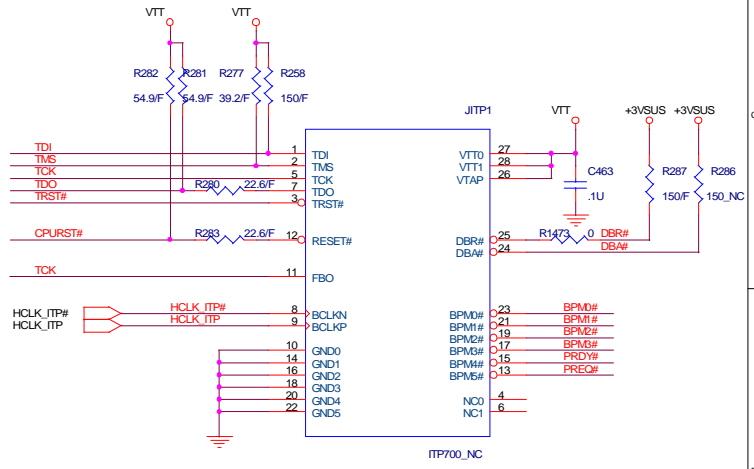
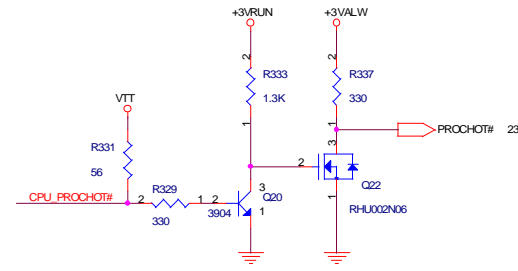
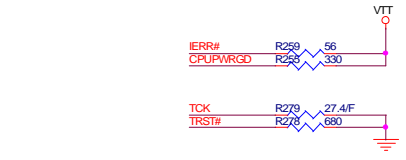
DM1

<http://bufanxiu.taobao.com>





R278 should be place within 2" of the processor ; others place near ITP



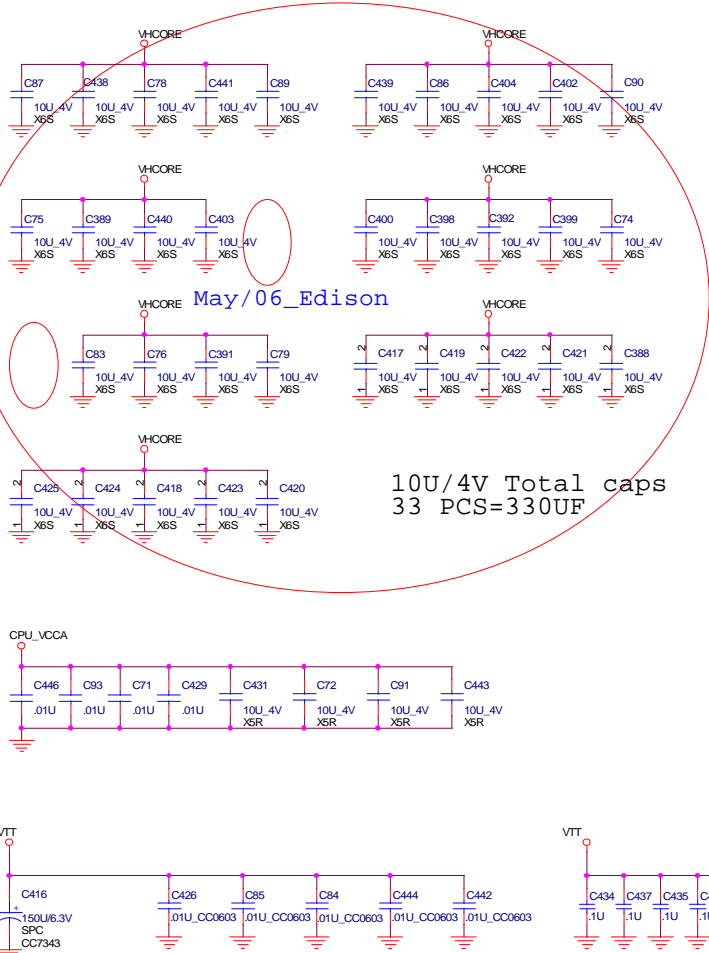
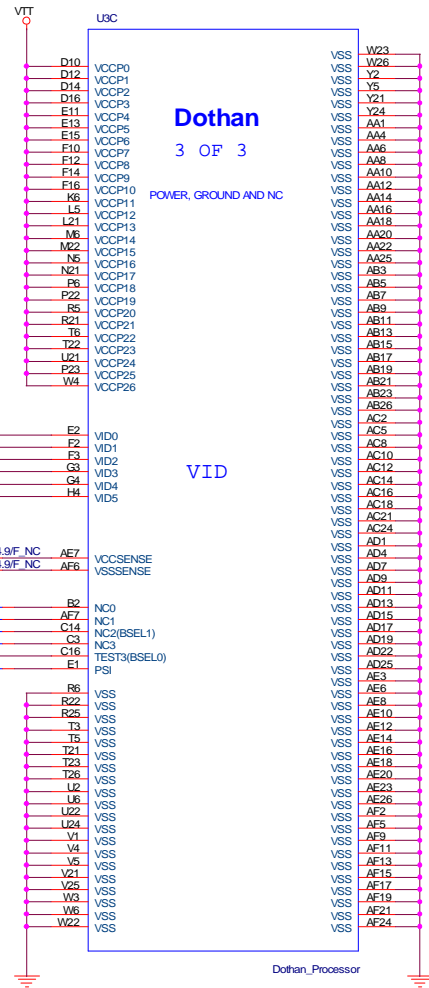
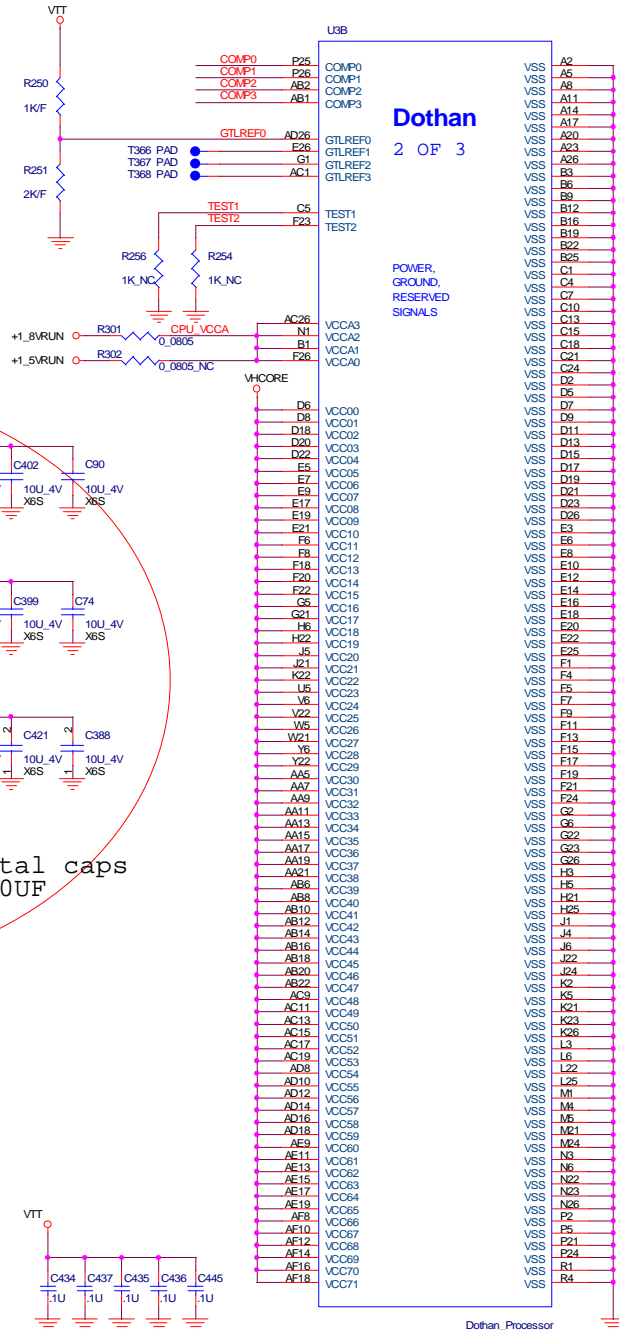
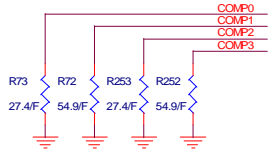
QUANTA COMPUTER

Title: Dothan Processor (HCST)

Size	Document Number DMI	Rev 1A
Date: Friday, July 18, 2003	Sheet 2 of 46	

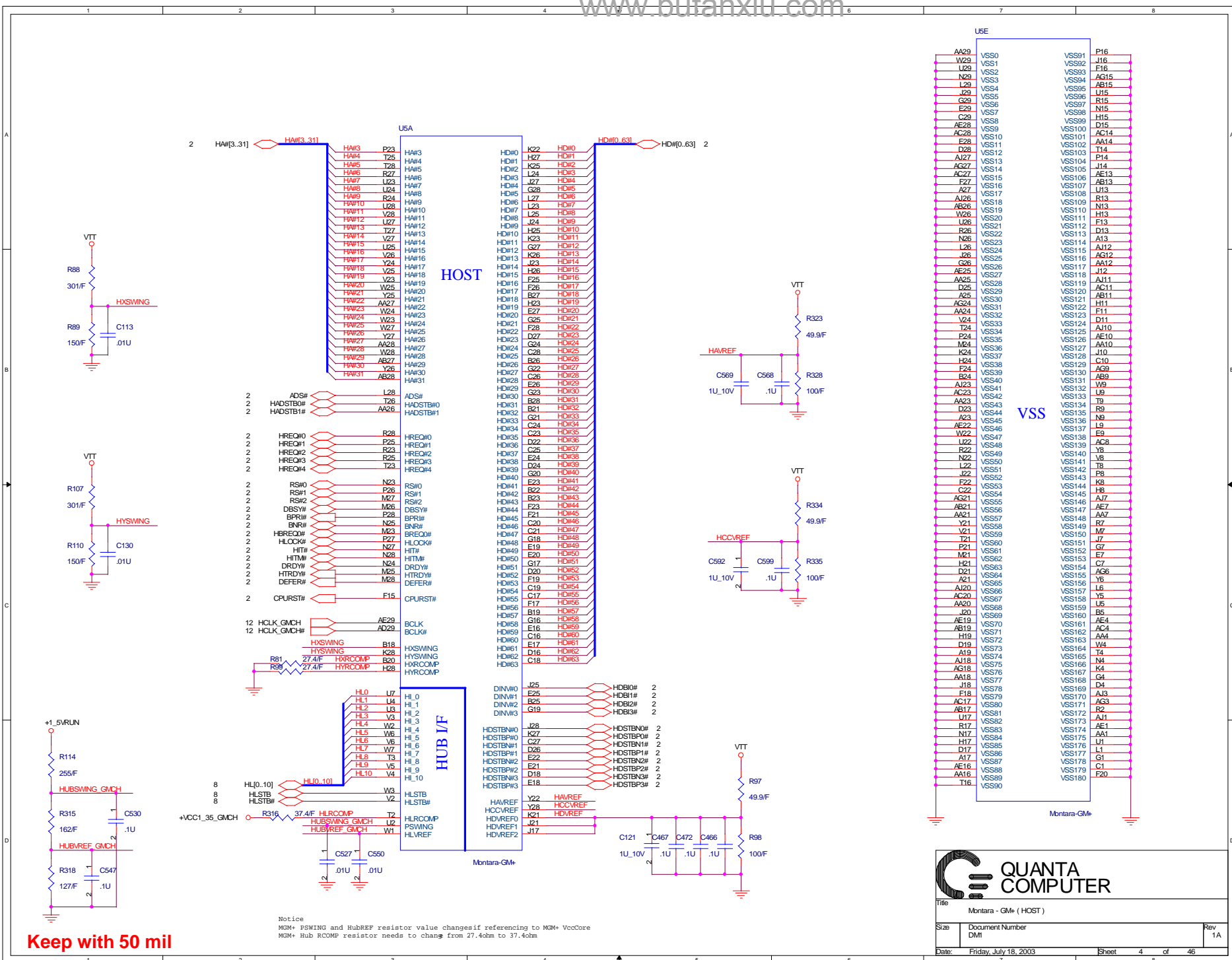
Dothan_Processor

These 4 Resistors need to place with 0.5" of CPU.
Comp0,2 trace need to be $z_0=27.4\ \text{ohm}$,
comp1,3 traces need to be $z_0=55\ \text{ohm}$.



QUANTA
COMPUTER

Title: Dothan Processor (POWER)		
Size: DM1	Document Number: DM1	Rev: 1A
Date: Friday, July 18, 2003	Sheet: 3	of 46



USE			
AA29	VSS0	VSS91	P16
W29	VSS1	VSS92	J16
L29	VSS2	VSS93	F16
N29	VSS3	VSS94	AG15
L29	VSS4	VSS95	AB15
G29	VSS5	VSS96	LH15
E29	VSS6	VSS97	R15
C29	VSS7	VSS98	N15
AE28	VSS8	VSS99	H15
AE28	VSS9	VSS100	D15
E28	VSS10	VSS101	AC14
D28	VSS11	VSS102	AA14
AJ27	VSS12	VSS103	T14
AC27	VSS13	VSS104	P14
F27	VSS14	VSS105	L14
A27	VSS15	VSS106	AE13
AJ26	VSS16	VSS107	U13
AE26	VSS17	VSS108	R13
W26	VSS18	VSS109	N13
R26	VSS19	VSS110	H13
N26	VSS20	VSS111	F13
L26	VSS21	VSS112	D13
G26	VSS22	VSS113	A13
E26	VSS23	VSS114	AJ12
C26	VSS24	VSS115	AG12
AE25	VSS25	VSS116	AA12
AE25	VSS26	VSS117	J12
D25	VSS27	VSS118	AJ11
A25	VSS28	VSS119	AC11
AC24	VSS29	VSS120	AB11
AC24	VSS30	VSS121	H11
V24	VSS31	VSS122	F11
P24	VSS32	VSS123	D11
M24	VSS33	VSS124	AJ10
K24	VSS34	VSS125	AE10
H24	VSS35	VSS126	AA10
F24	VSS36	VSS127	J10
B24	VSS37	VSS128	C10
AJ23	VSS38	VSS129	AG9
AC23	VSS39	VSS130	AB9
A23	VSS40	VSS131	W9
AE22	VSS41	VSS132	L9
AE22	VSS42	VSS133	T9
W22	VSS43	VSS134	R9
R22	VSS44	VSS135	N9
N22	VSS45	VSS136	H9
L22	VSS46	VSS137	E9
G22	VSS47	VSS138	AC8
E22	VSS48	VSS139	Y8
C22	VSS49	VSS140	V8
AE21	VSS50	VSS141	T8
AE21	VSS51	VSS142	P8
D21	VSS52	VSS143	L8
AJ20	VSS53	VSS144	K8
AC20	VSS54	VSS145	AJ7
A20	VSS55	VSS146	AE7
AJ19	VSS56	VSS147	AA7
AC19	VSS57	VSS148	R7
A19	VSS58	VSS149	M7
AA18	VSS59	VSS150	I7
	VSS60	VSS151	G7
	VSS61	VSS152	E7
	VSS62	VSS153	C7
	VSS63	VSS154	AC6
	VSS64	VSS155	Y6
	VSS65	VSS156	V6
	VSS66	VSS157	L6
	VSS67	VSS158	U5
	VSS68	VSS159	B5
	VSS69	VSS160	AE4
	VSS70	VSS161	AC4
	VSS71	VSS162	AA4
	VSS72	VSS163	W4
	VSS73	VSS164	T4
	VSS74	VSS165	N4
	VSS75	VSS166	H4
	VSS76	VSS167	K4
	VSS77	VSS168	D4
	VSS78	VSS169	AJ3
	VSS79	VSS170	AG3
	VSS80	VSS171	R2
	VSS81	VSS172	AJ1
	VSS82	VSS173	AE1
	VSS83	VSS174	AA1
	VSS84	VSS175	L1
	VSS85	VSS176	U1
	VSS86	VSS177	G1
	VSS87	VSS178	C1
	AE16	VSS88	H1
	AA16	VSS89	F20
	VSS90	VSS180	

QUANTA COMPUTER

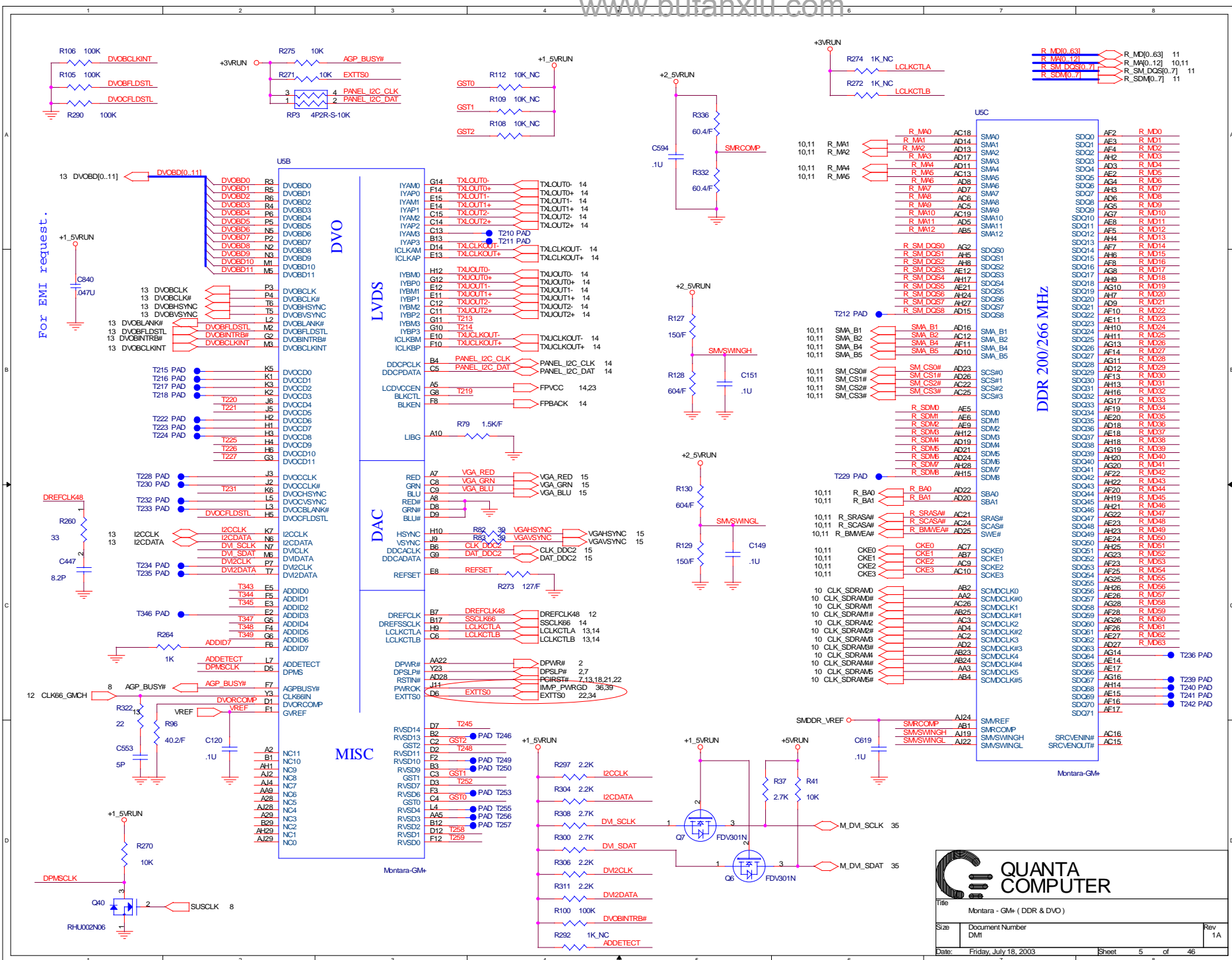
Title: Montara - GM+ (HOST)

Size: DMI	Document Number: DMI	Rev: 1A
-----------	----------------------	---------

Date: Friday, July 18, 2003 Sheet: 4 of 46

Keep with 50 mil

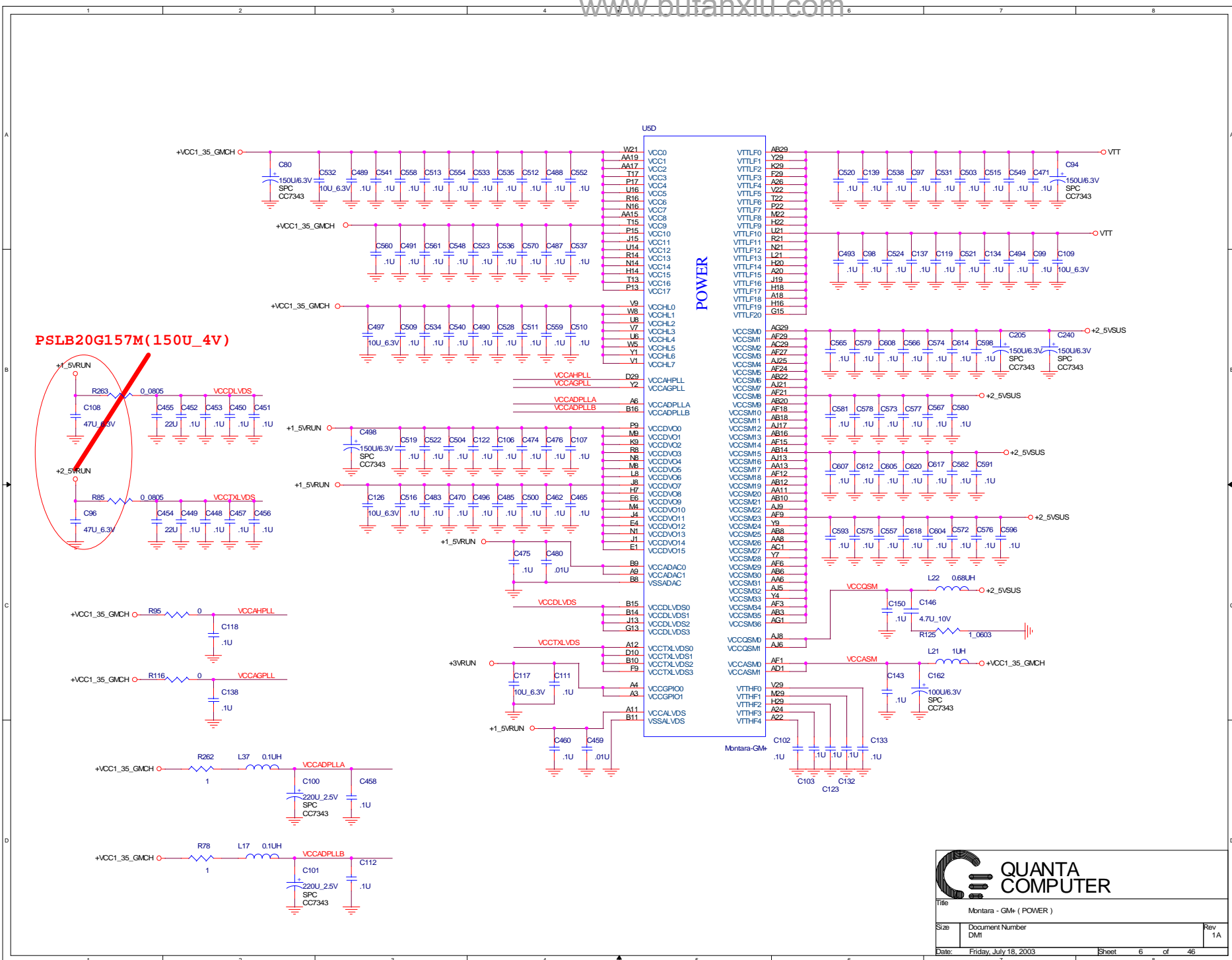
Notice
 GM+ PSWING and HubREF resistor value changes if referencing to GM+ VccCore
 GM+ Hub RCOMP resistor needs to change from 27.4ohm to 37.4ohm



Title		Montara - GM+ (DDR & DVO)	
Size	Document Number	Rev	
Dmt1		5	1A
Date:	Friday, July 18, 2003	Sheet	5 of 46

DDR 200/266 MHz

Montara-GM+



PSLB20G157M(150U_4V)

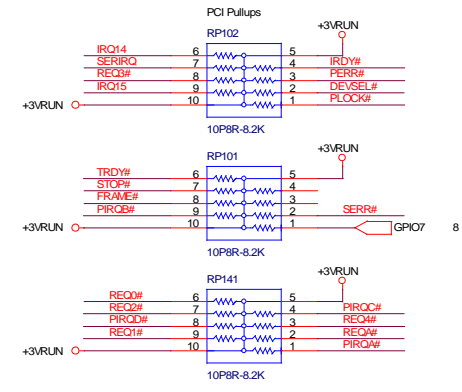
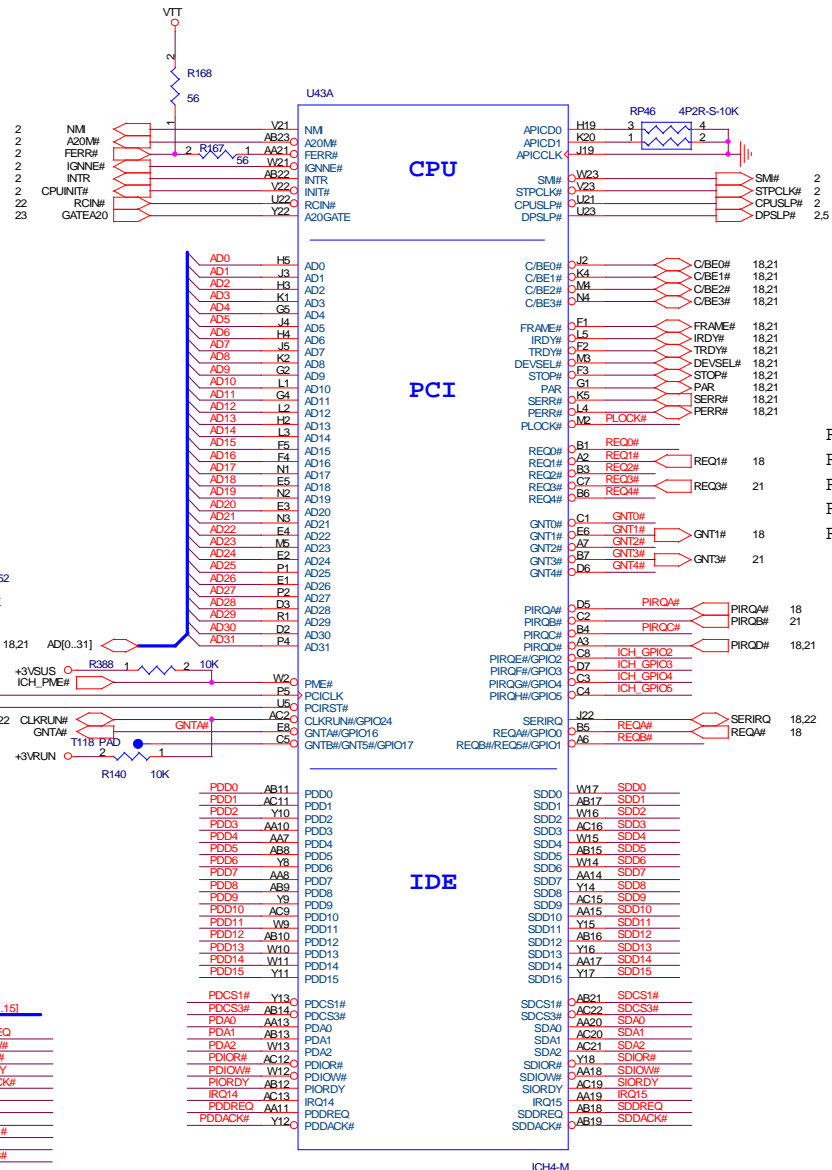
POWER

QUANTA COMPUTER

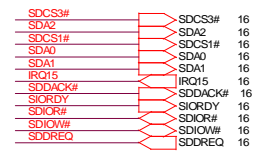
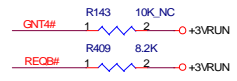
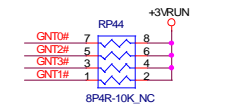
Title: Montara - GM+ (POWER)

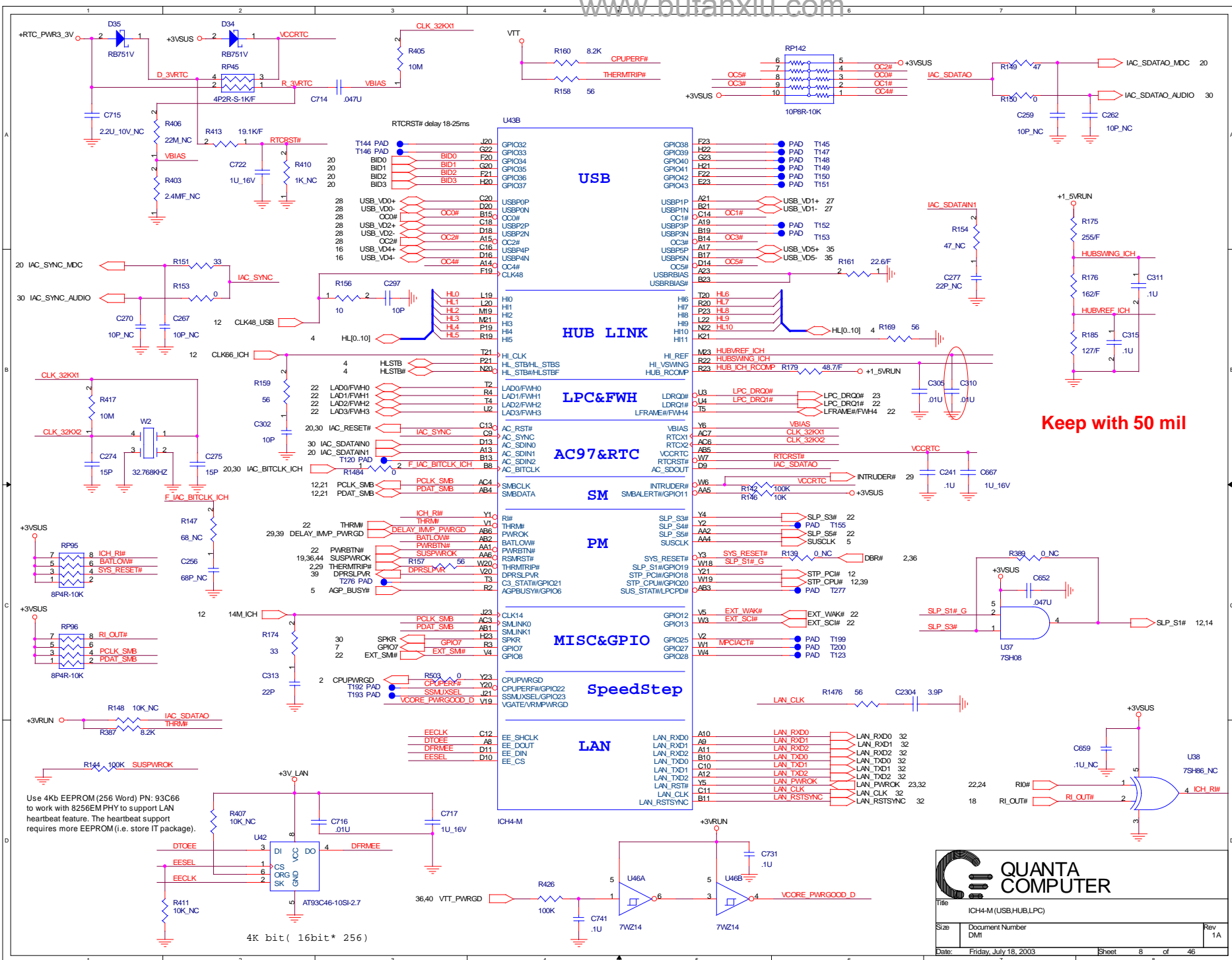
Size: Document Number: DM1 Rev: 1A

Date: Friday, July 18, 2003 Sheet: 6 of 46



REQ0 : RESERVED
 REQ1 : Card Bus
 REQ2 : RESERVED
 REQ3 : MINI PCI
 REQ4 : RESERVED

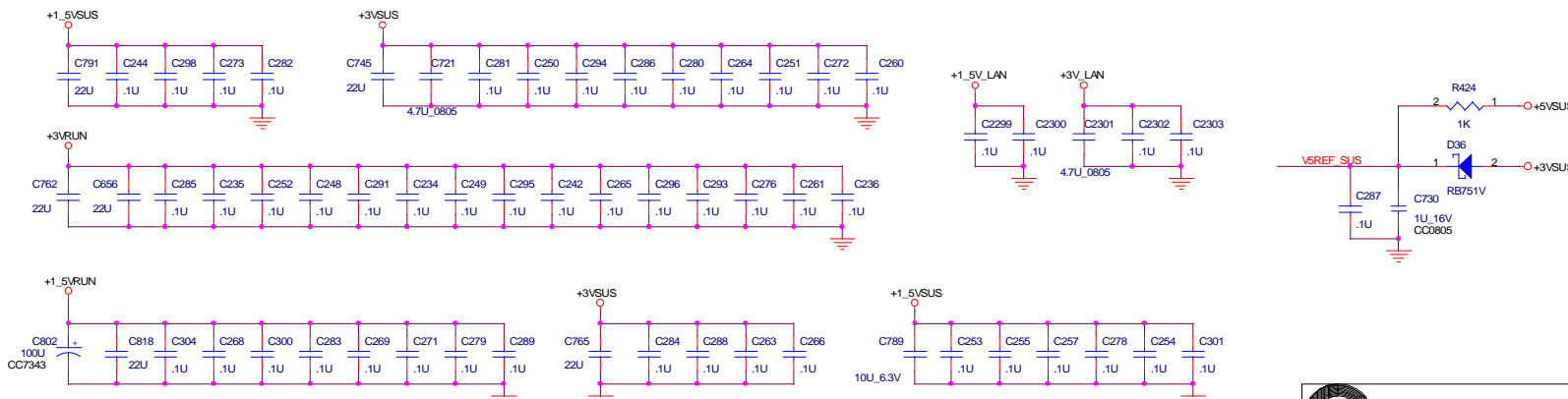
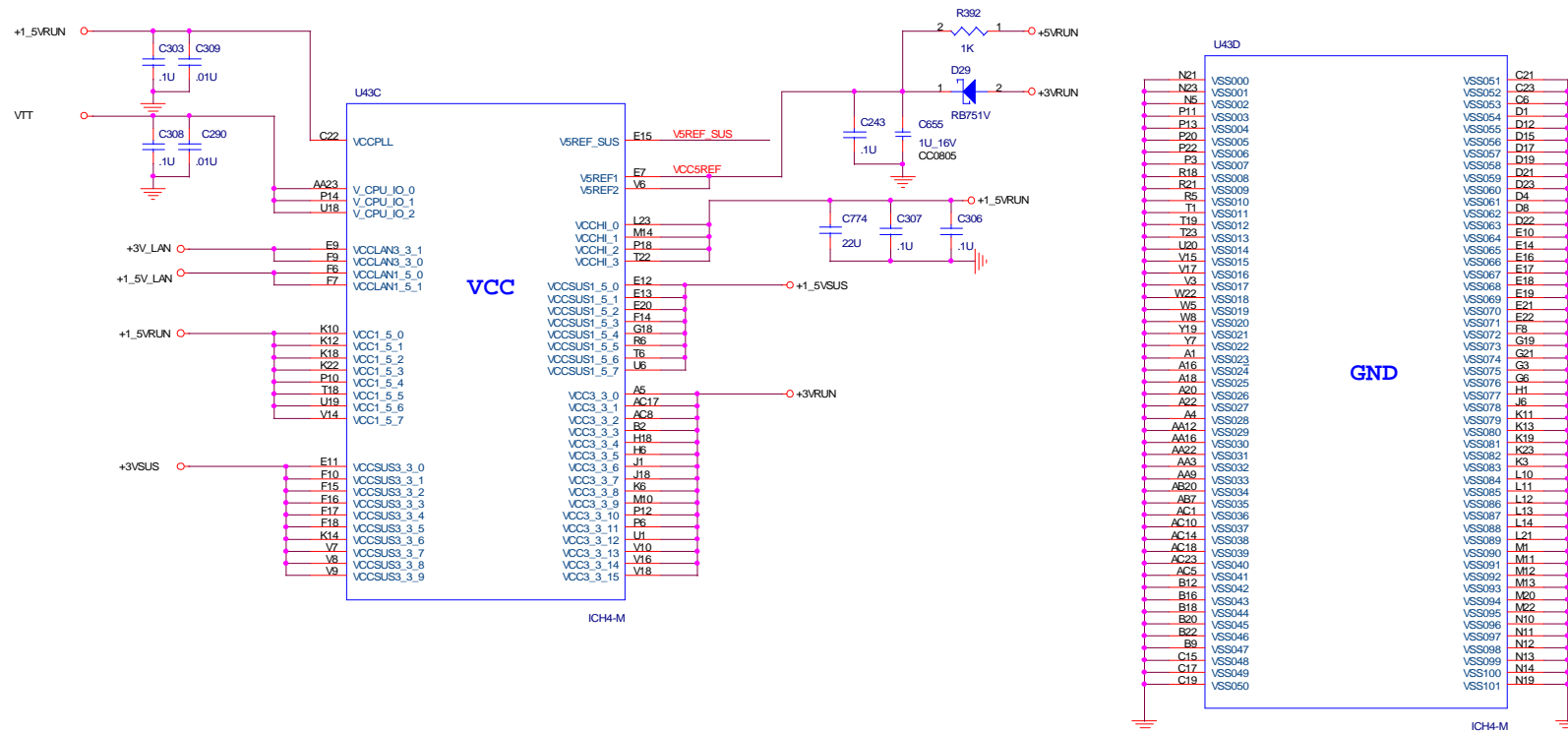




QUANTA COMPUTER

Title: ICH4-M (USB,HUB,LPC)

Size:	Document Number: DM1	Rev: 1A
Date:	Friday, July 18, 2003	Sheet: 8 of 46

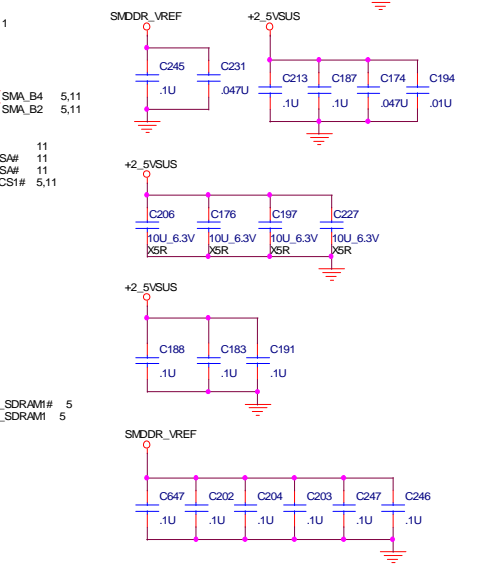
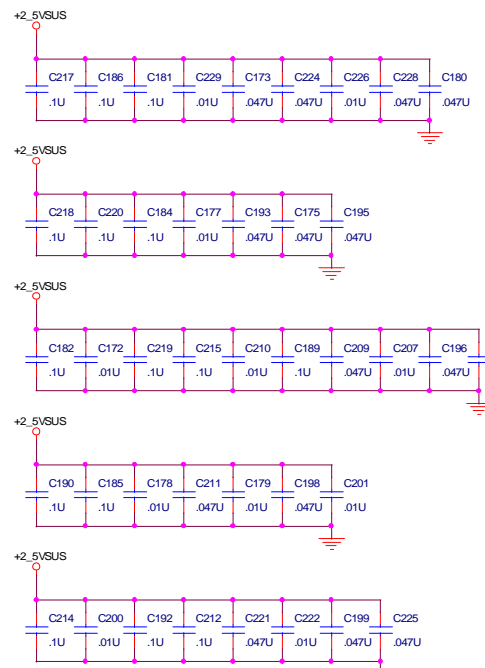
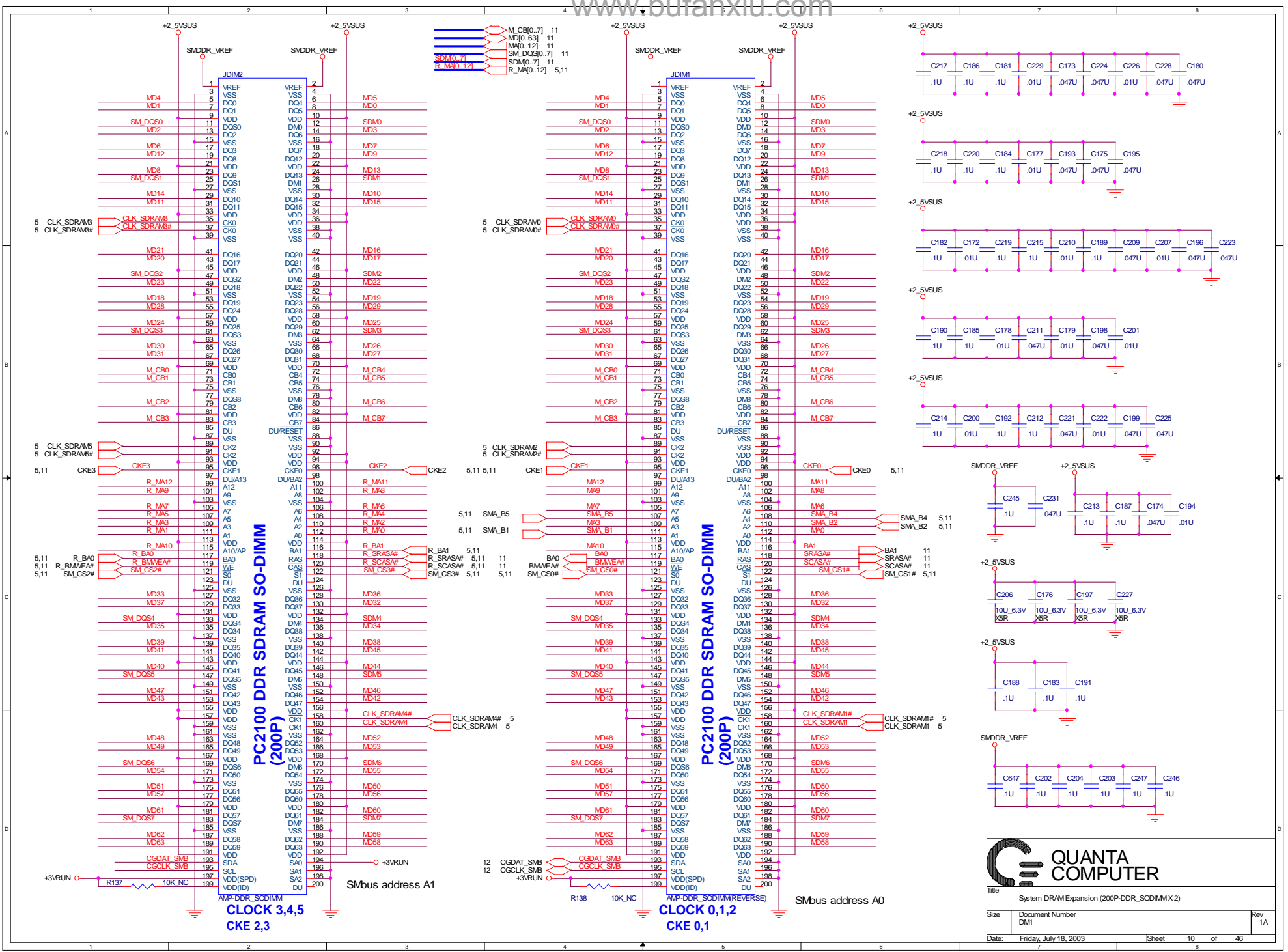


QUANTA COMPUTER

Title: ICH4-M (POWER&GND)

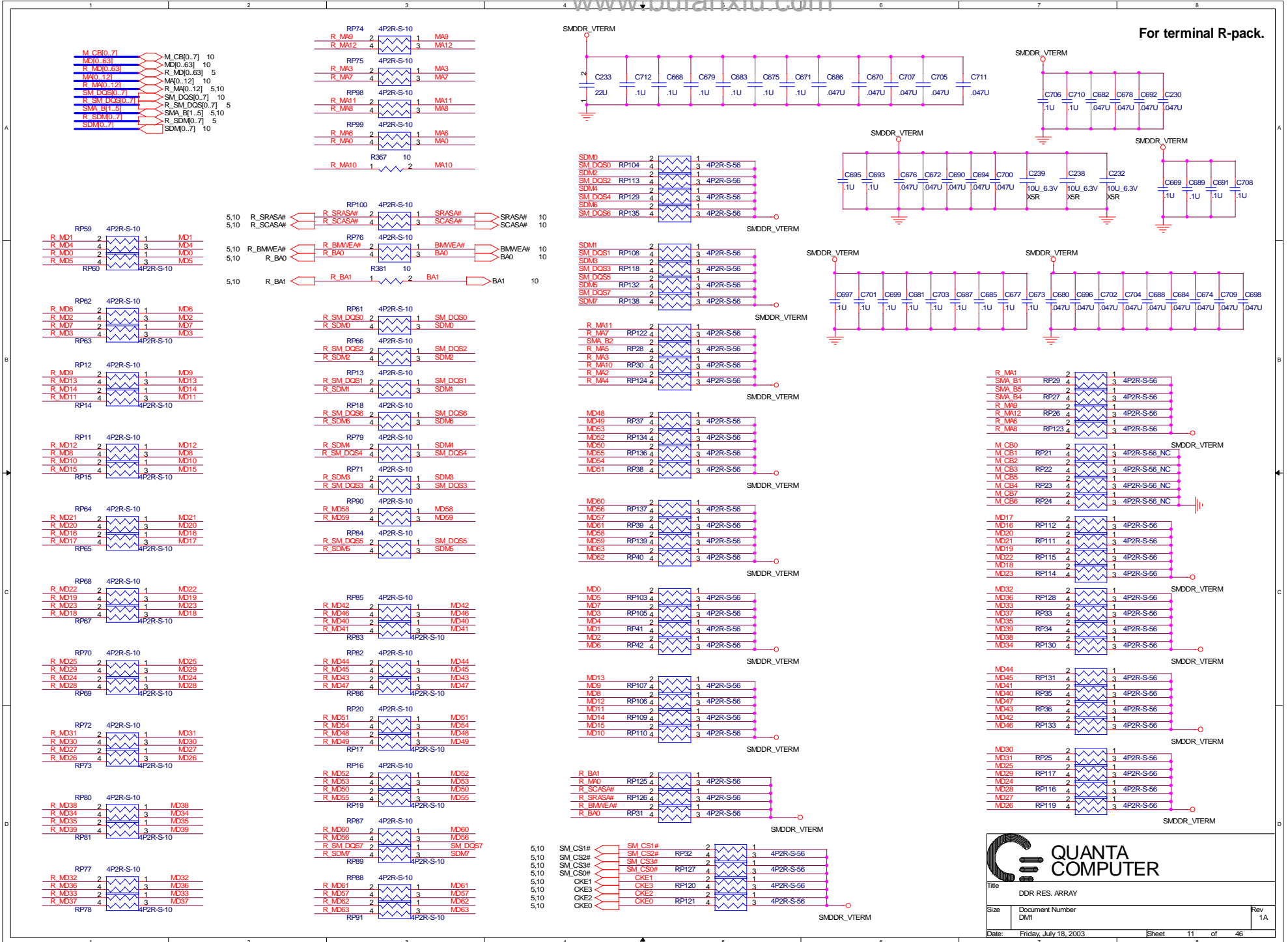
Size: DMT	Document Number: DMT	Rev: 1A
-----------	----------------------	---------

Date: Friday, July 18, 2003 Sheet: 9 of 46



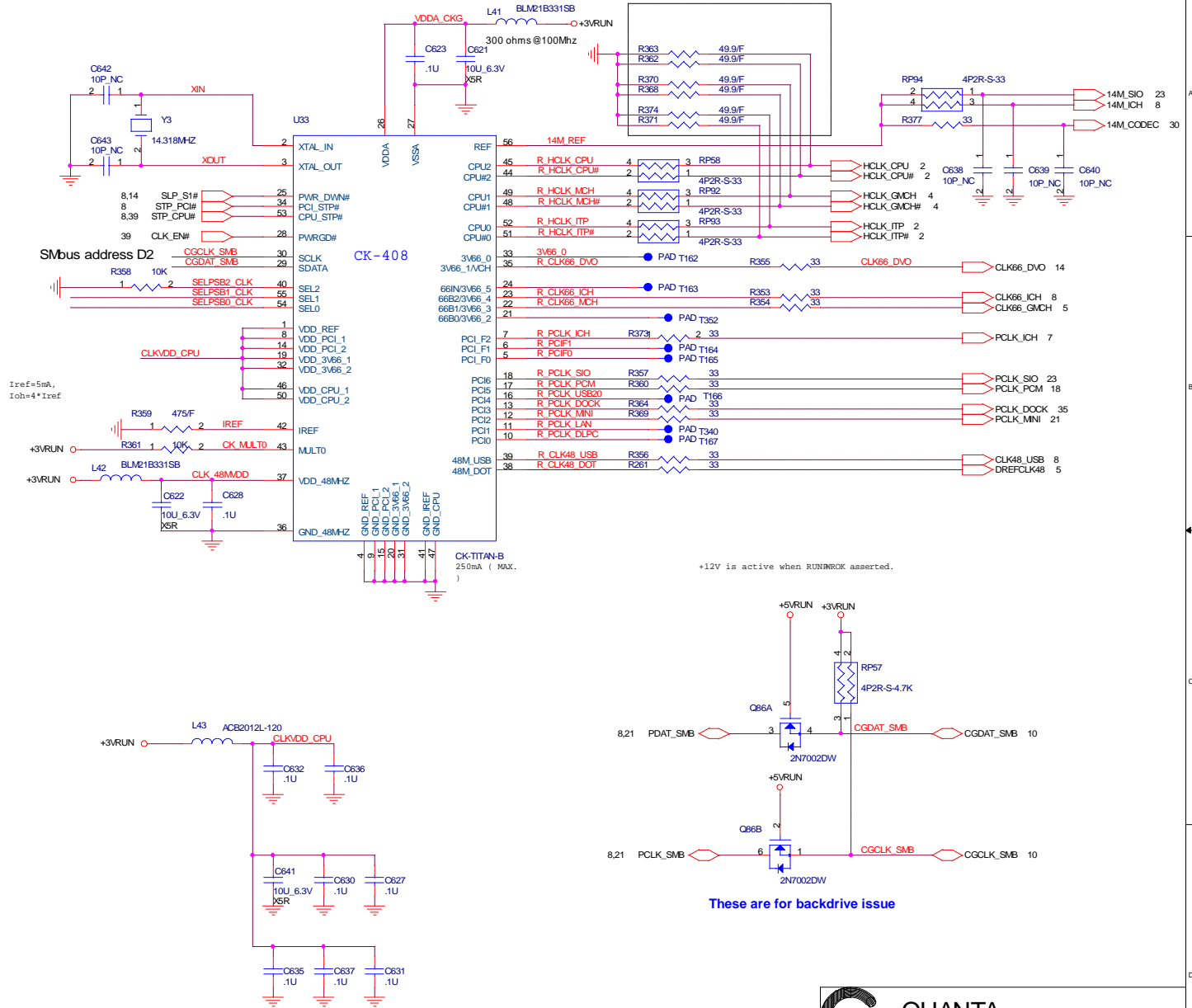
Title		
System DRAM Expansion (200P-DDR_SODIMM X2)		
Size	Document Number	Rev
	DM1	1A
Date:	Friday, July 18, 2003	Sheet 10 of 46

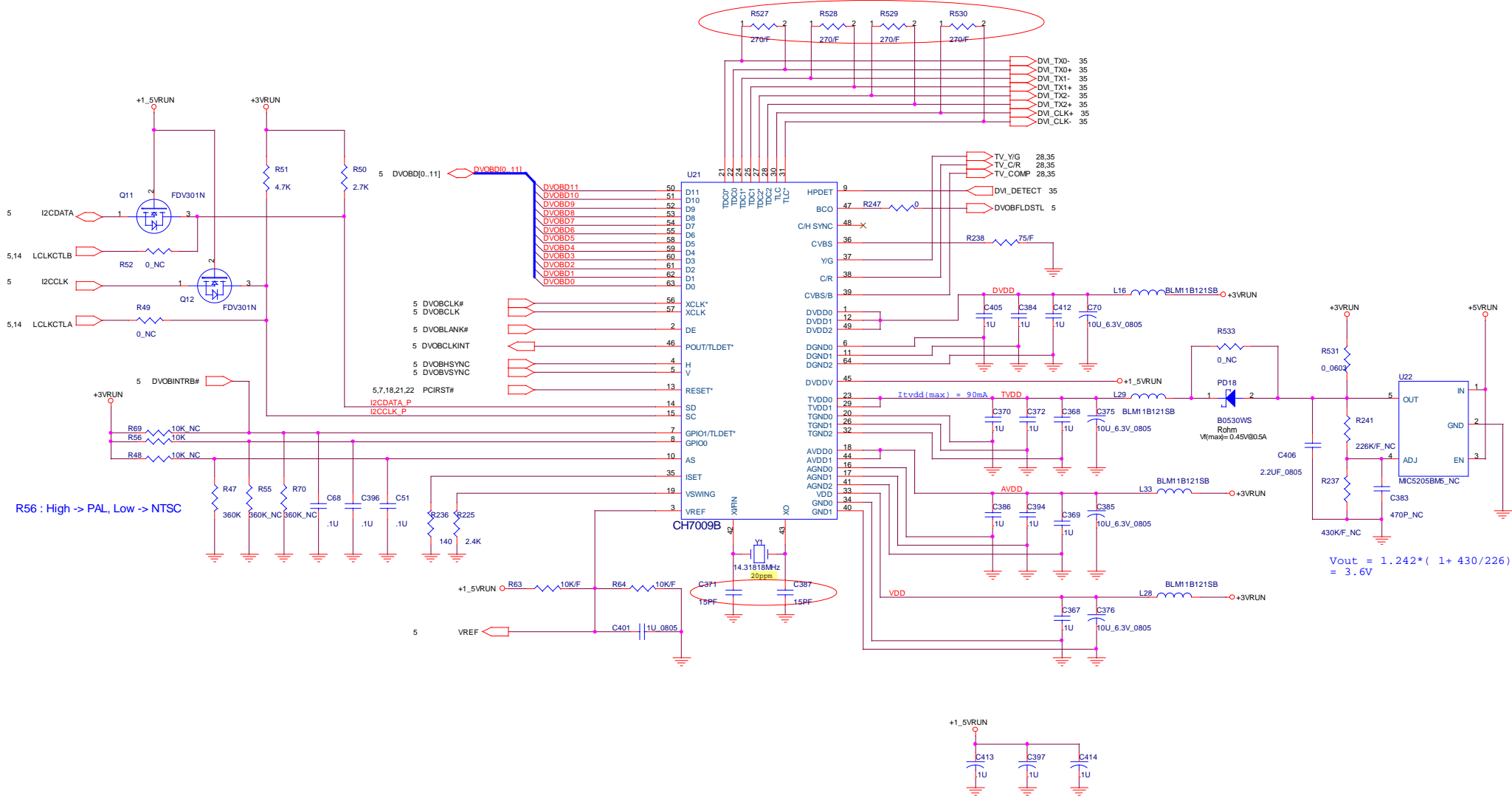
For terminal R-pack.

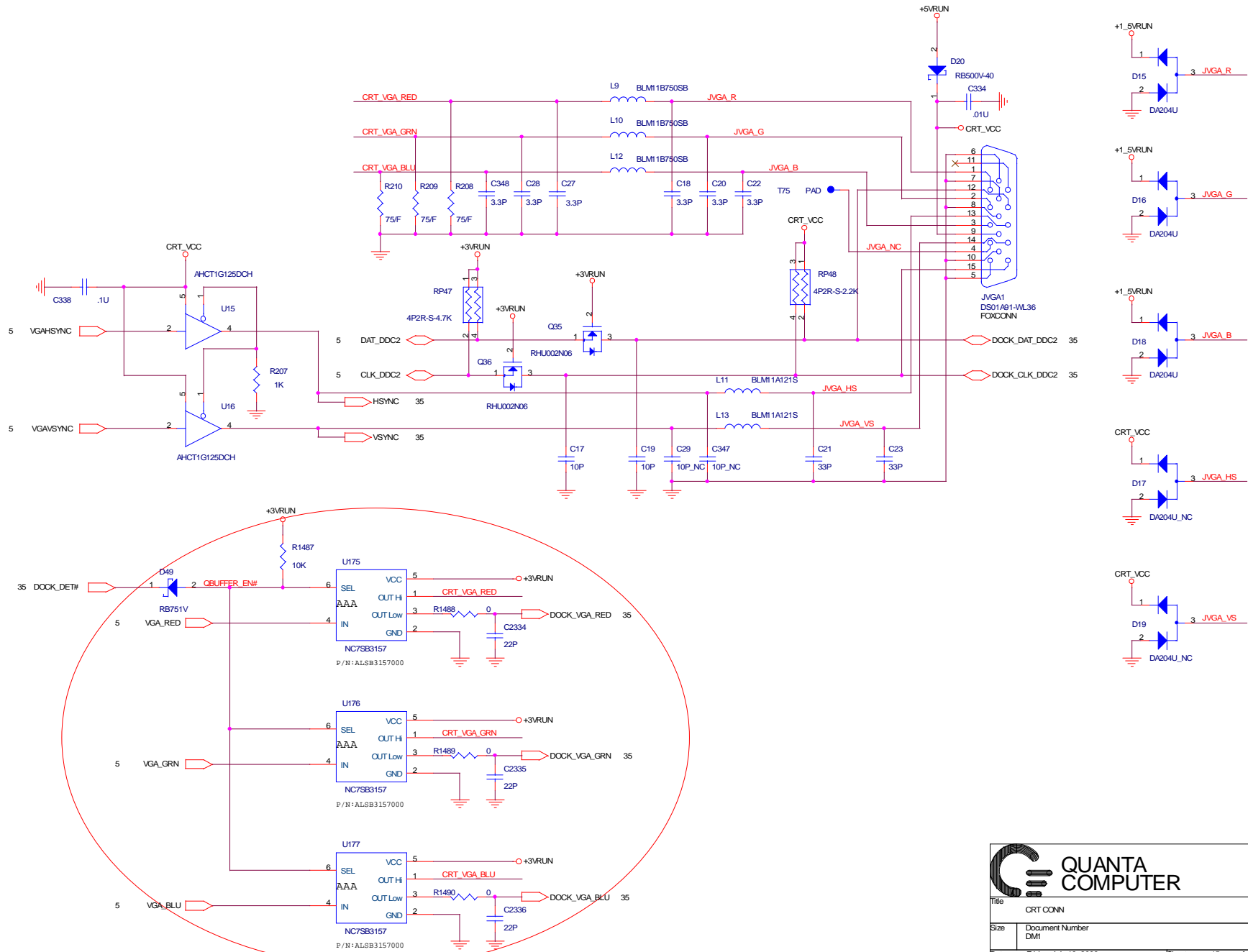


Place these termination to close CK408.

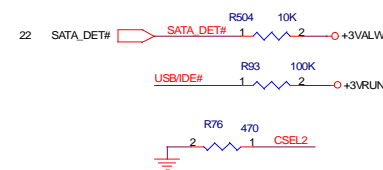
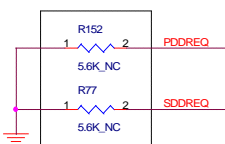
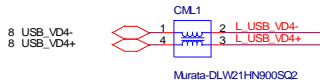
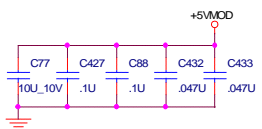
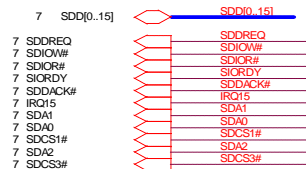
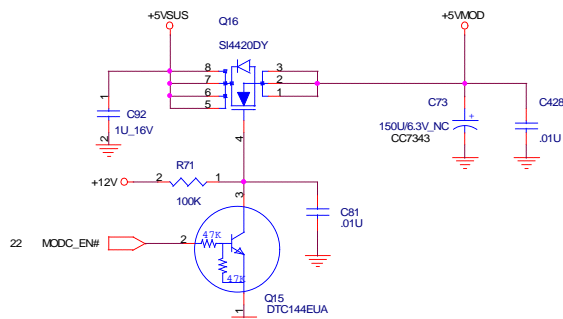
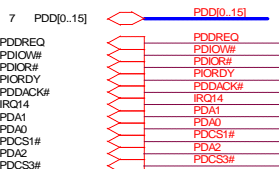
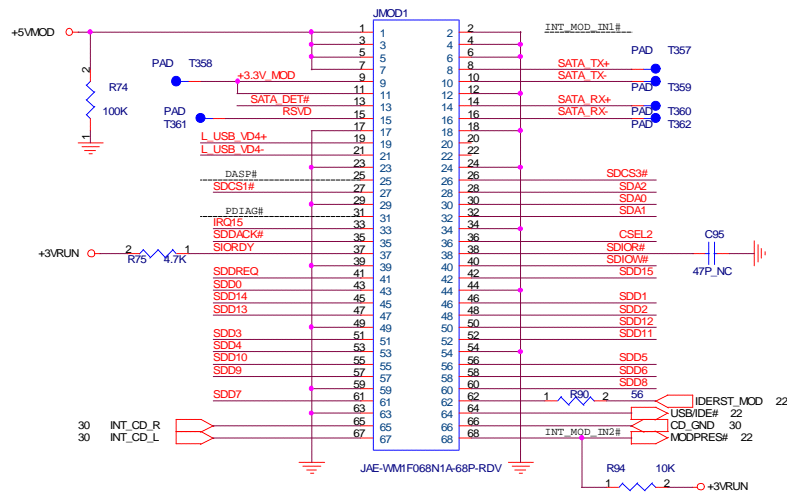
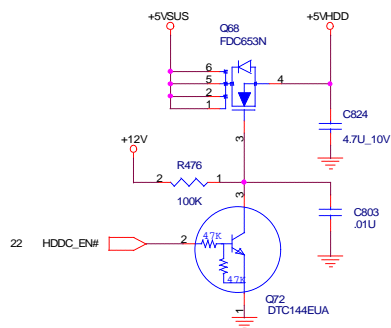
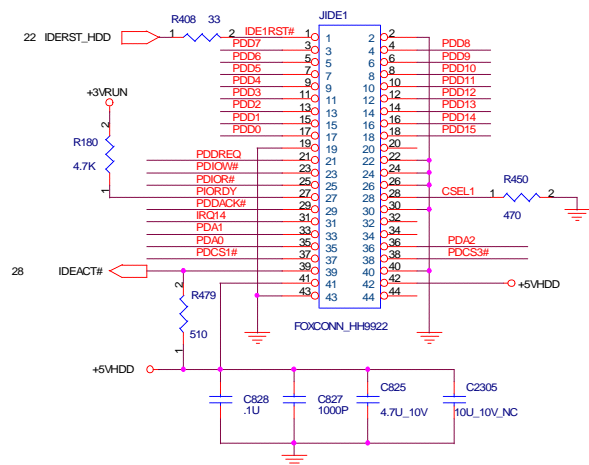
S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input

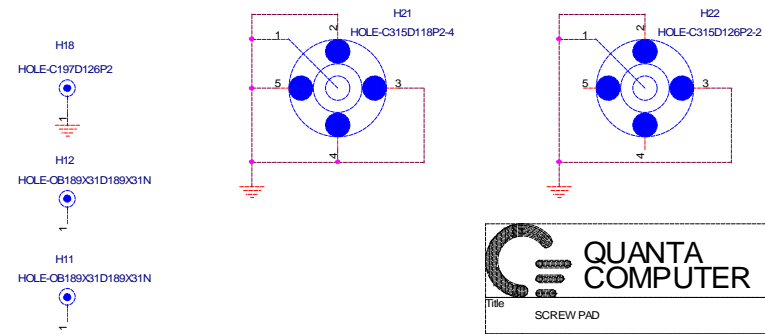
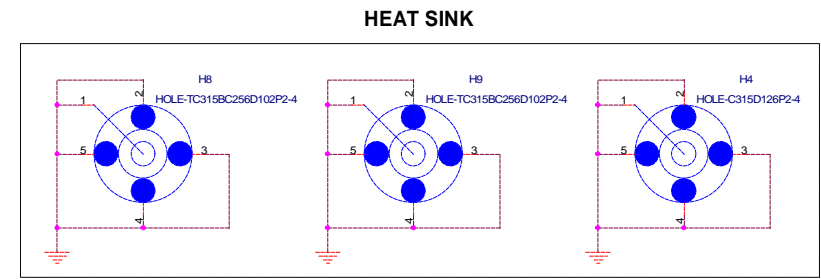
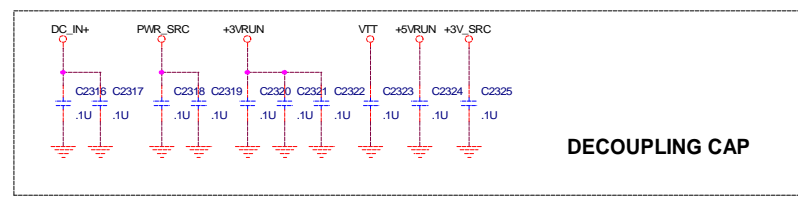
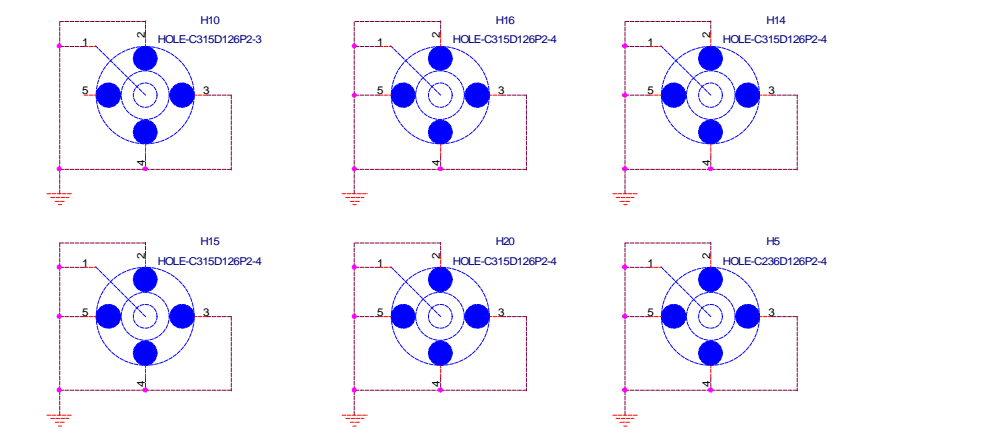
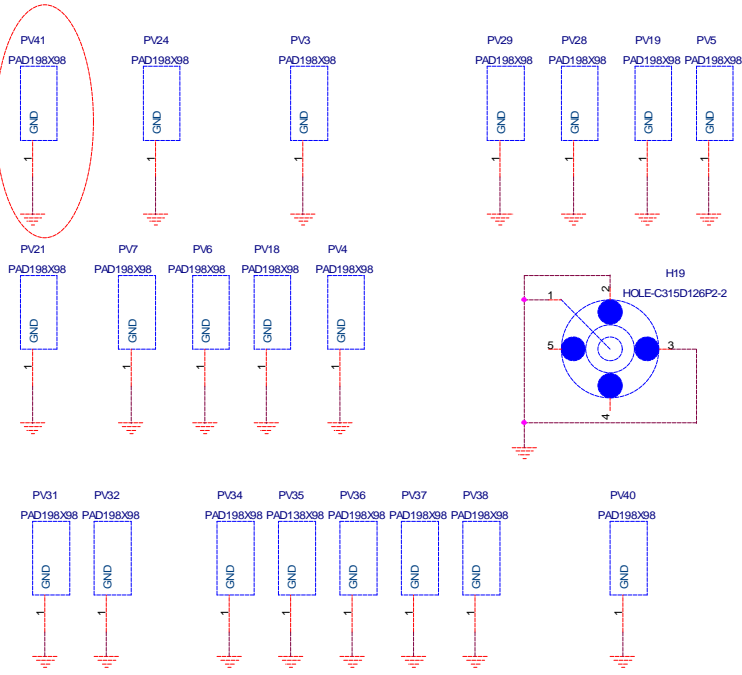
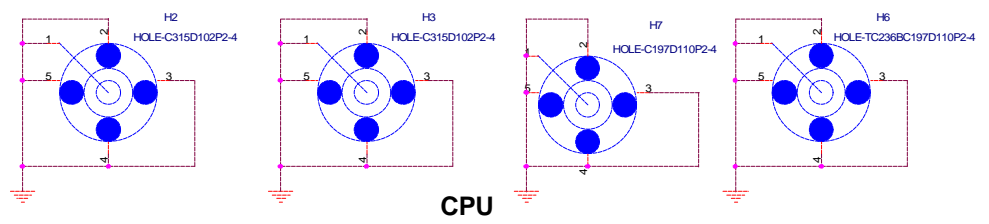
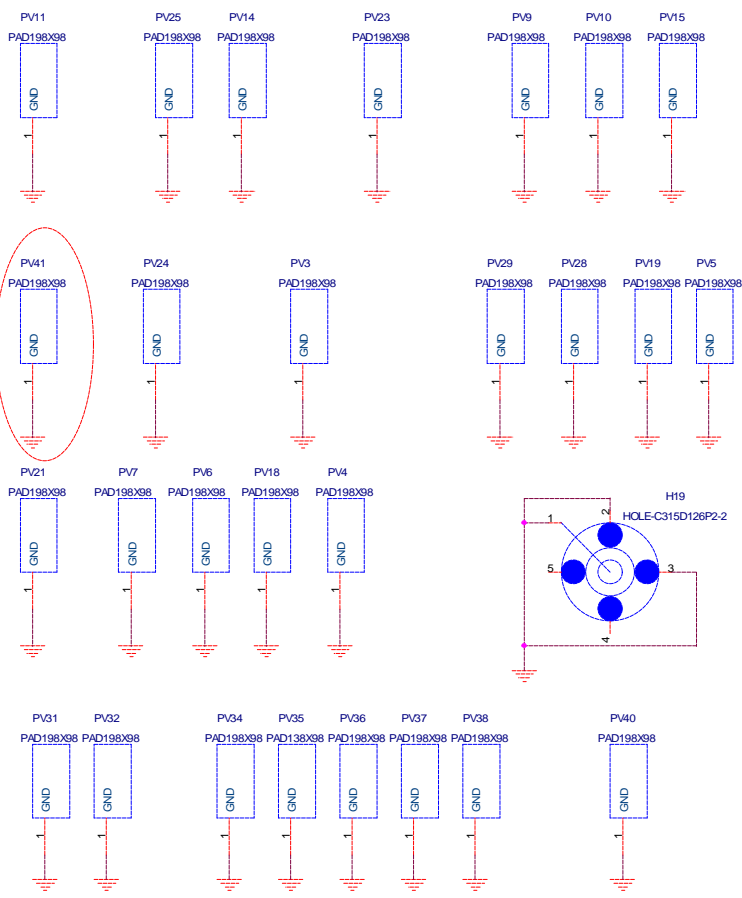






Title CRT CONN		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 15 of 46



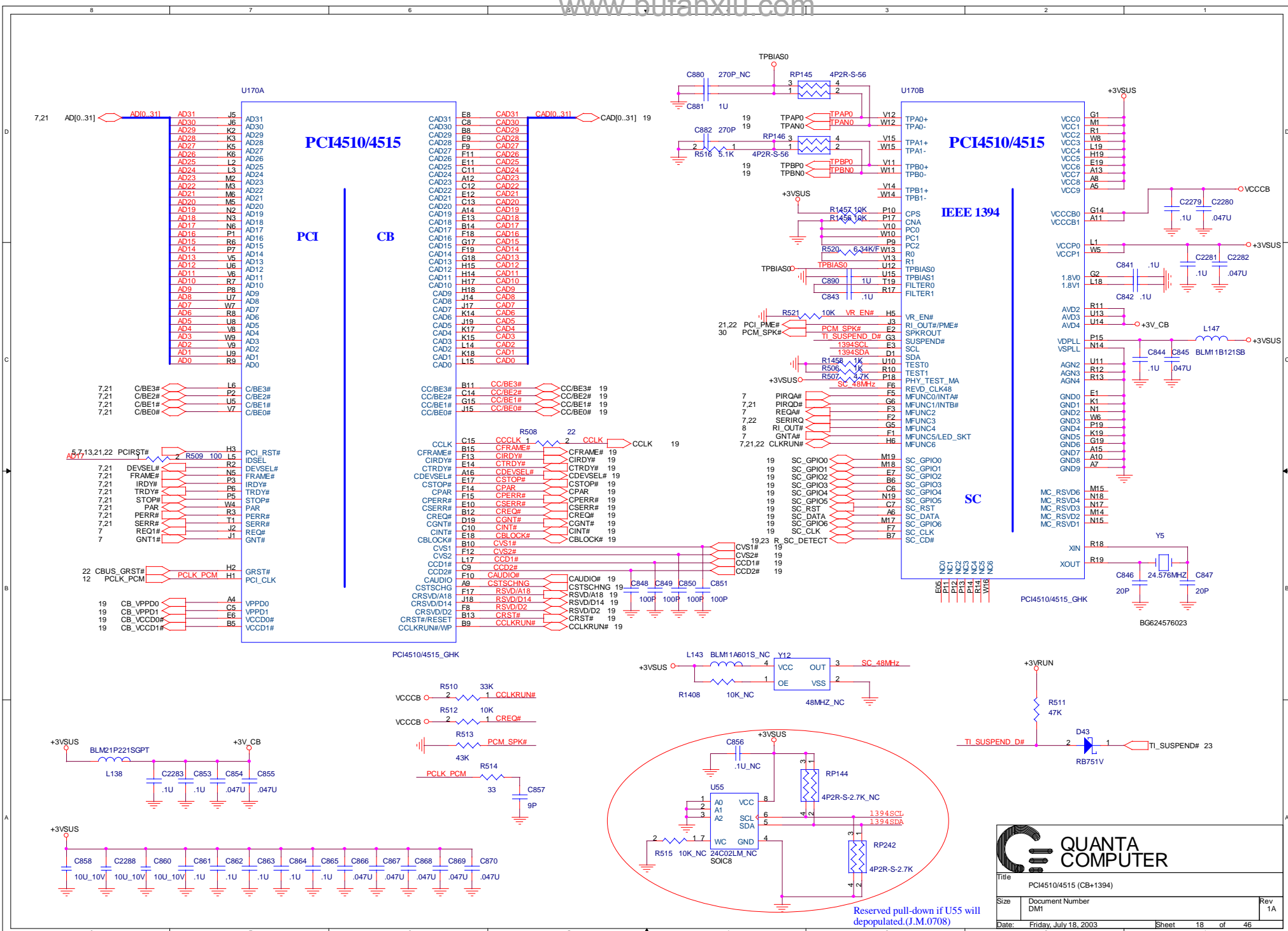


QUANTA COMPUTER

Title: SCREW PAD

Size: DM1	Document Number: DM1	Rev: 1A
-----------	----------------------	---------

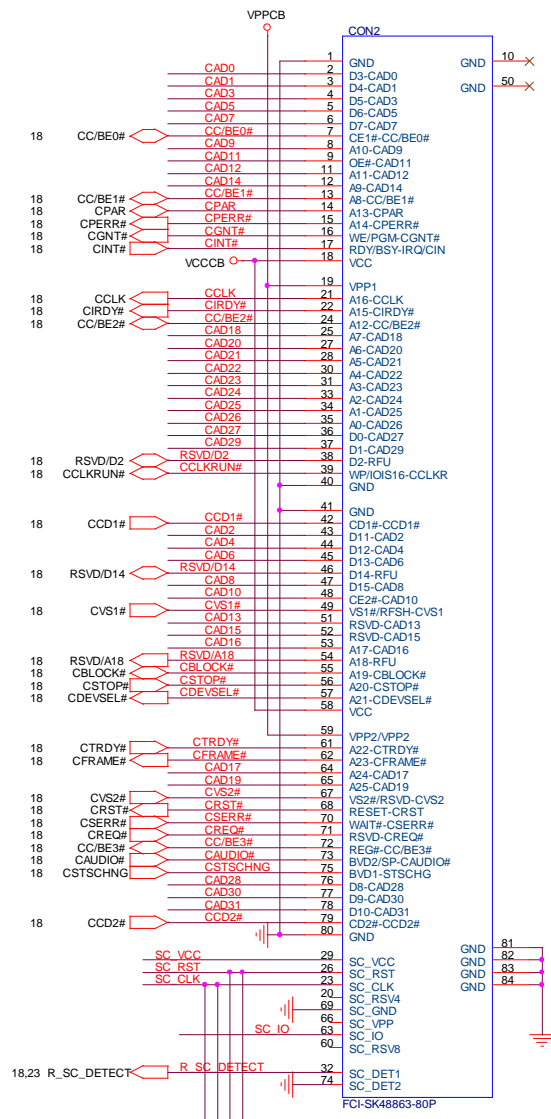
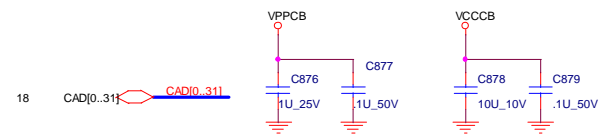
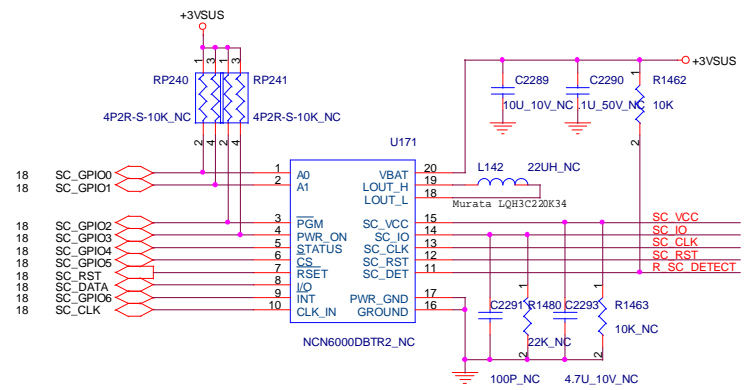
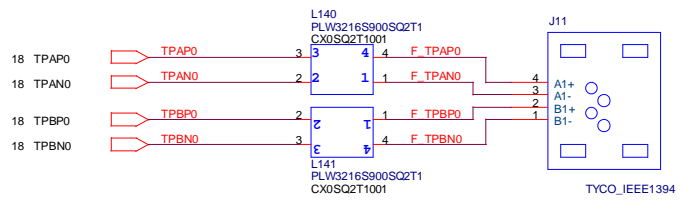
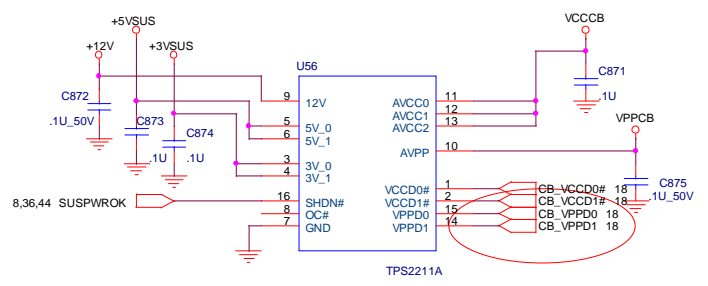
Date: Friday, July 18, 2003 Sheet 17 of 46



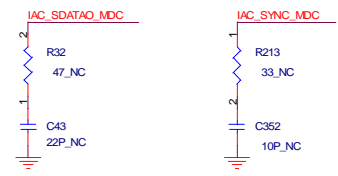
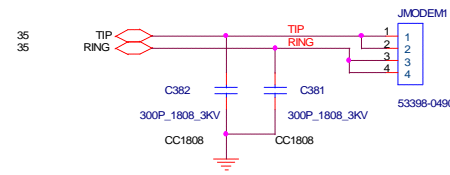
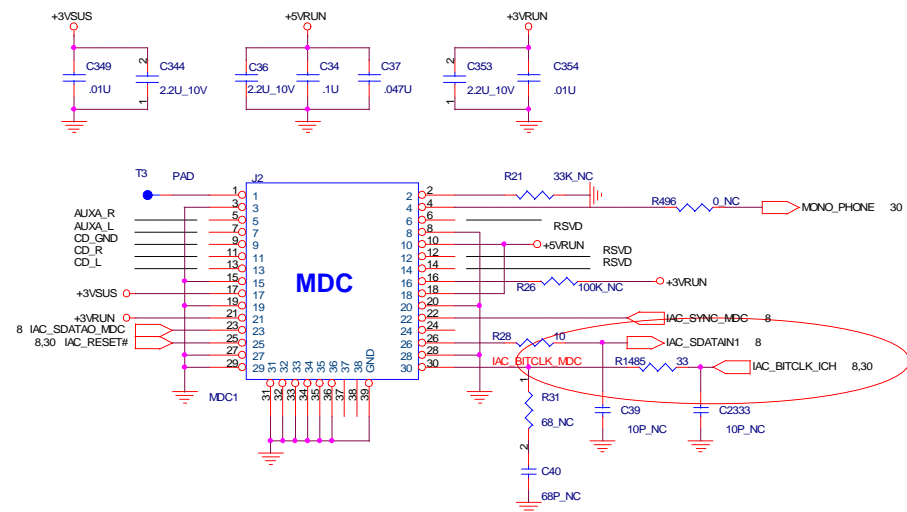
QUANTA COMPUTER

Title PCI4510/4515 (CB+1394)	
Size DM1	Document Number
Date Friday, July 18, 2003	Rev 1A
Sheet 18	of 46

Reserved pull-down if U55 will be depopulated.(J.M.0708)

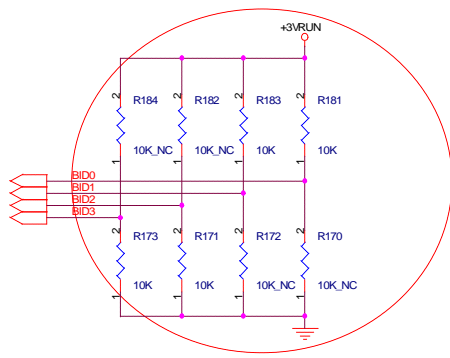


Title CB/1394 CONN		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 19 of 46

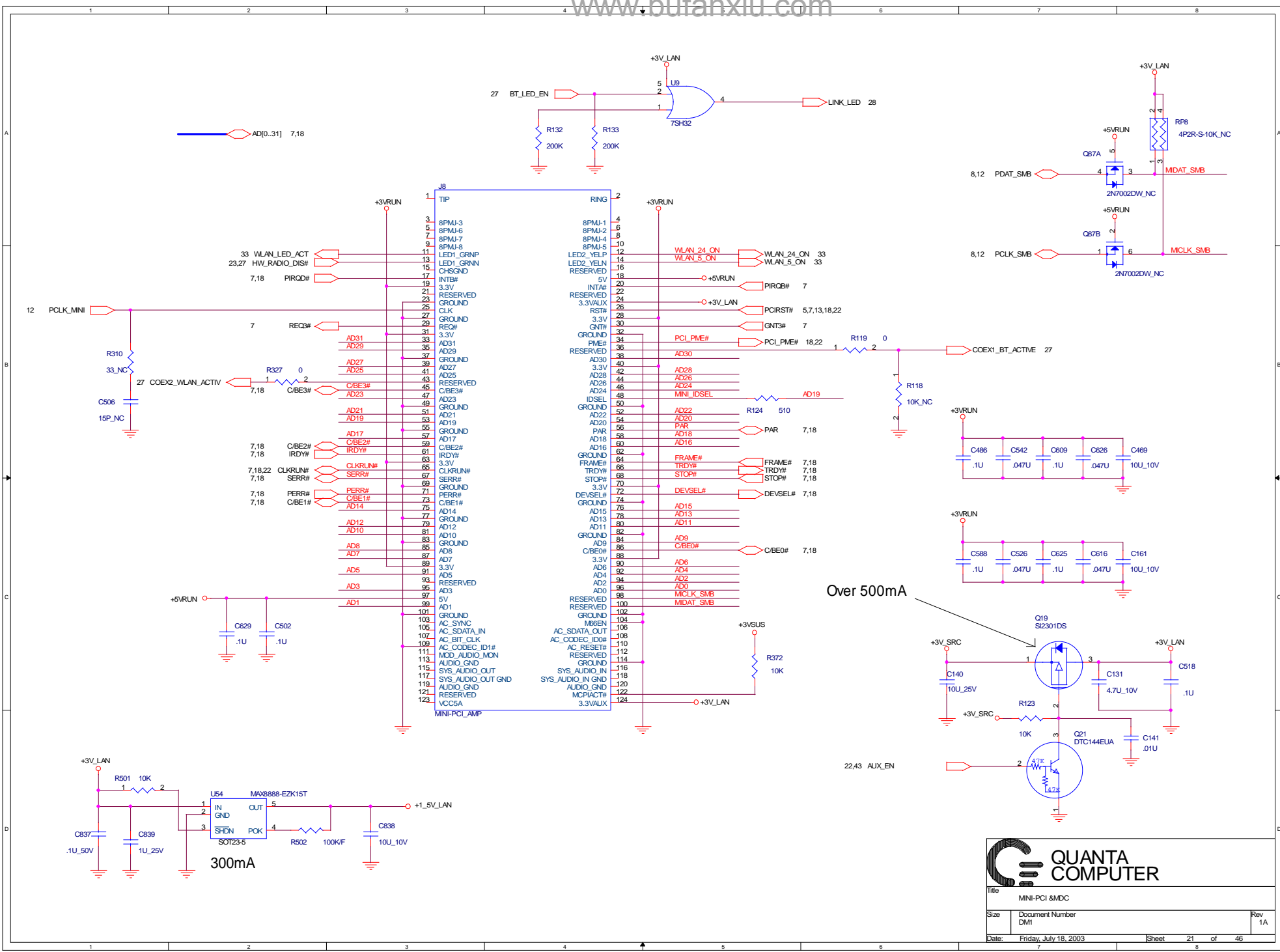


BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1
0	0	1	0	PROTO2
0	0	1	1	PROTO3
0	1	0	0	PROTO4
0	1	0	1	QT1
0	1	1	0	RAMP

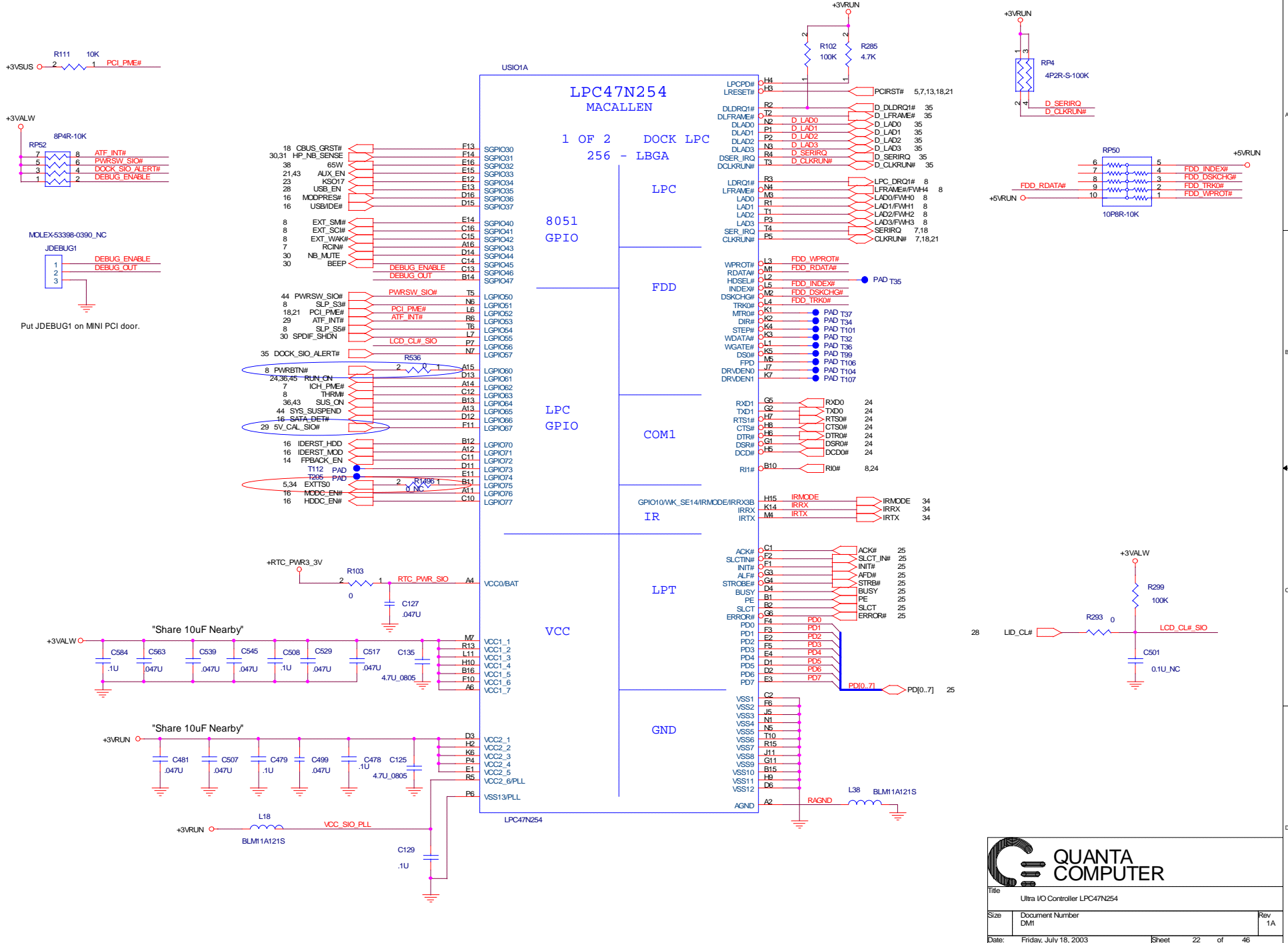
8 BID0
8 BID1
8 BID2
8 BID3

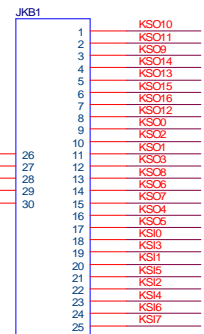
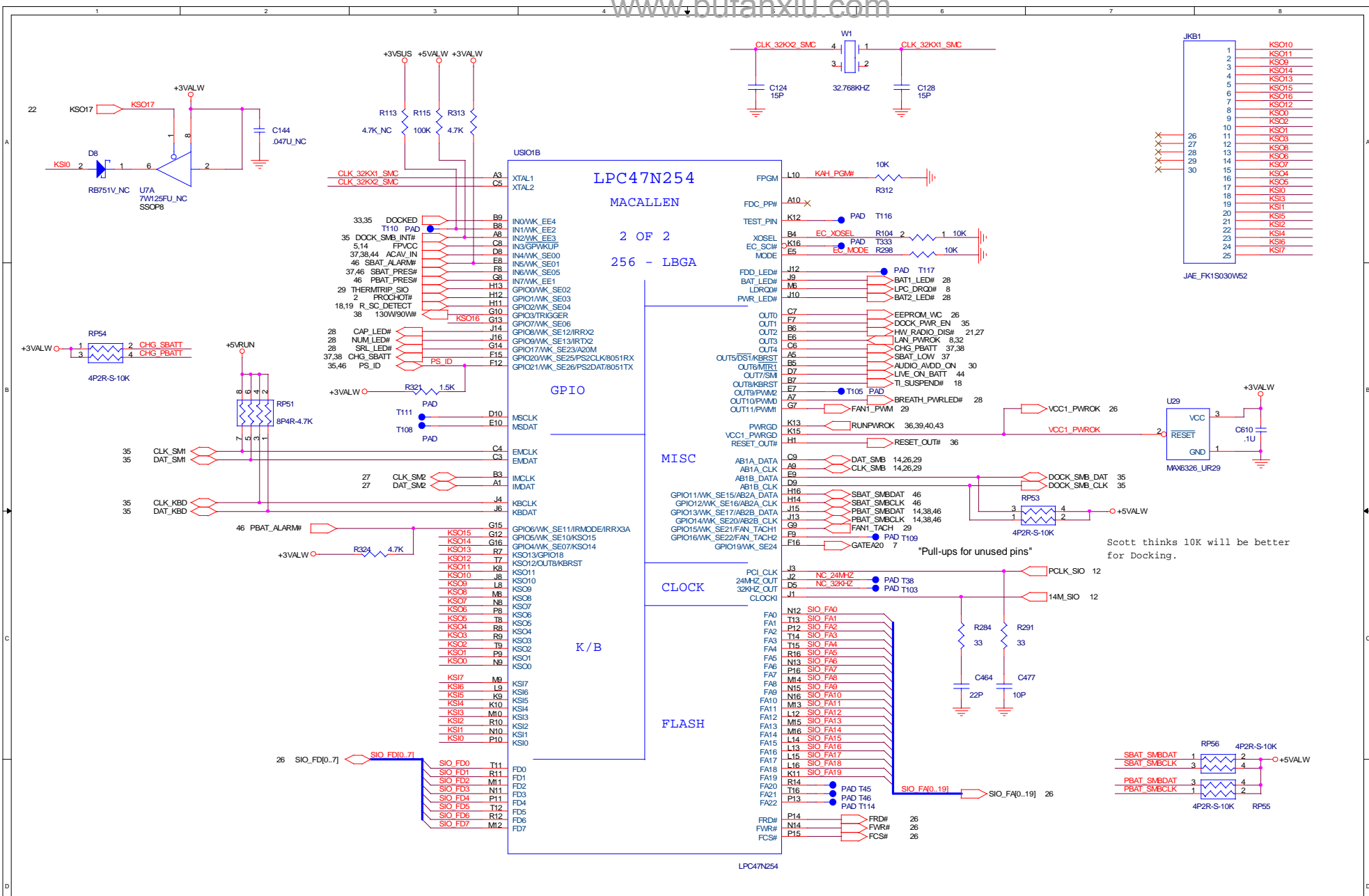


Title			MDC CONN.
Size	Document Number	Rev	
DM1		1A	
Date:	Friday, July 18, 2003	Sheet	20 of 46



Title		
MNI-PCI & MDC		
Size	Document Number	Rev
	DM1	1A
Date:	Friday, July 18, 2003	Sheet 21 of 46

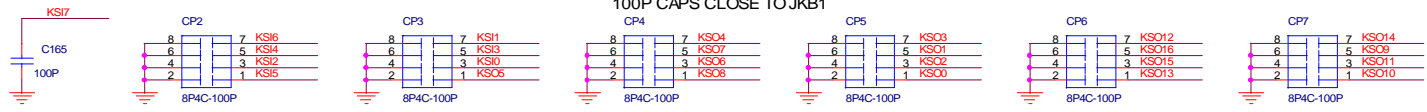




JAE_FK1S030W52

Scott thinks 10K will be better for Docking.

100P CAPS CLOSE TO JKB1

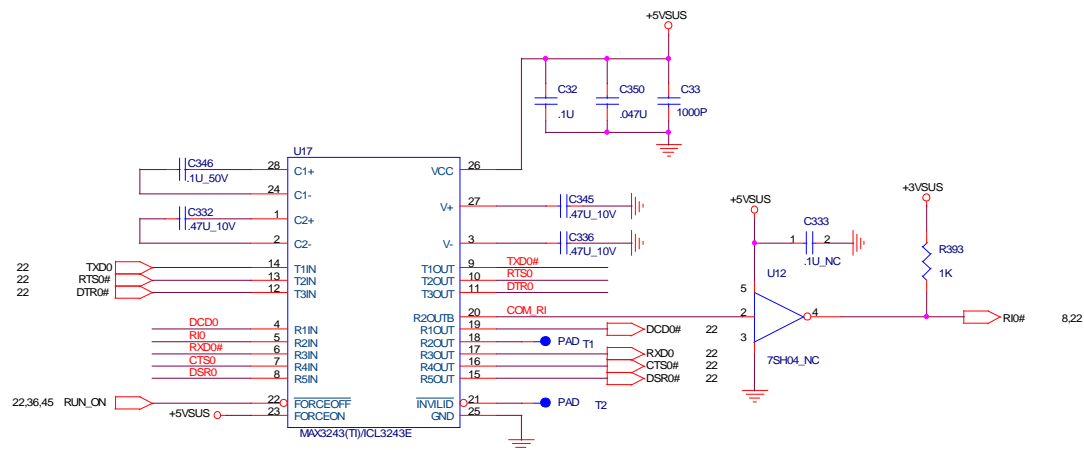


QUANTA COMPUTER

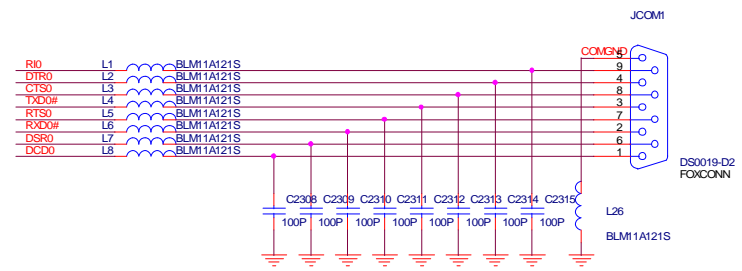
Title: Ultra I/O Controller LPC47N254(GPIO/KB/MSC/FLASH)

Size: Document Number DM1 Rev 1A

Date: Friday, July 18, 2003 Sheet 23 of 46



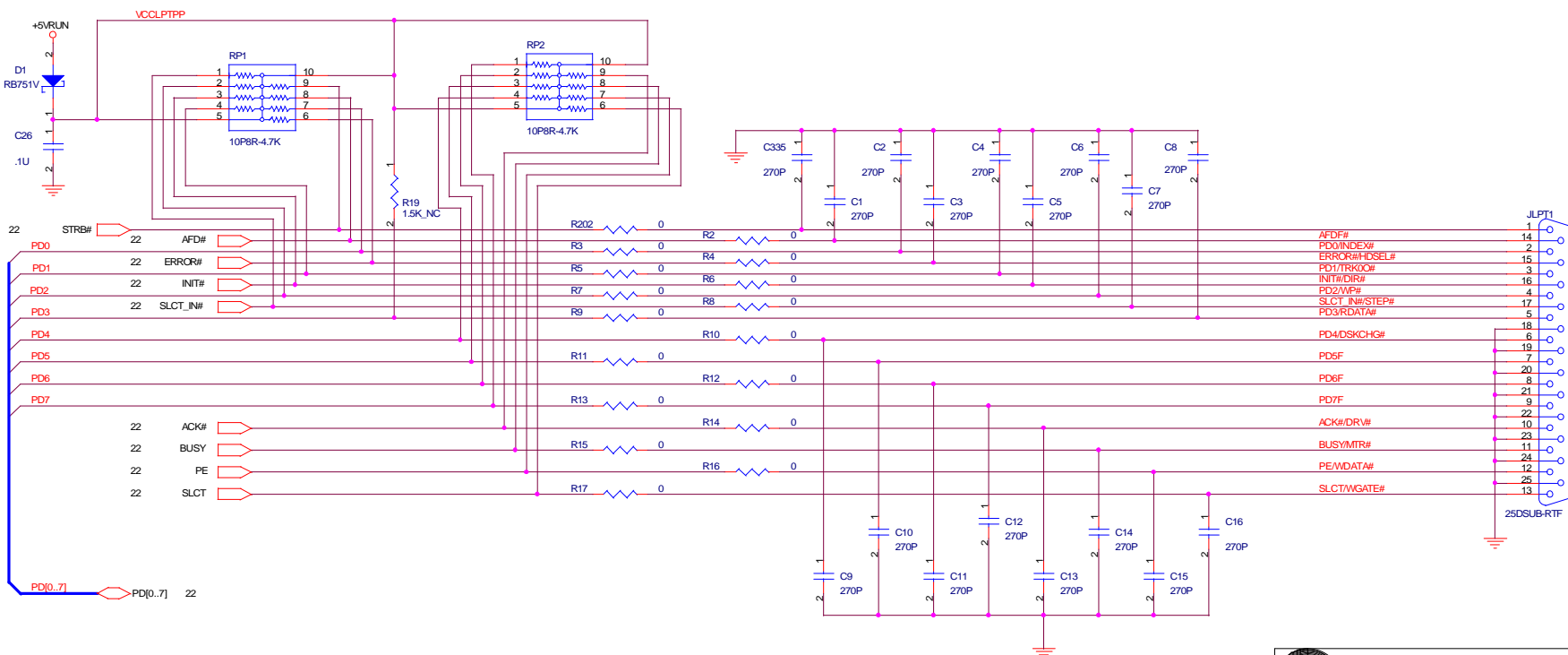
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out



Place these beads to JCOM1 as close as possible

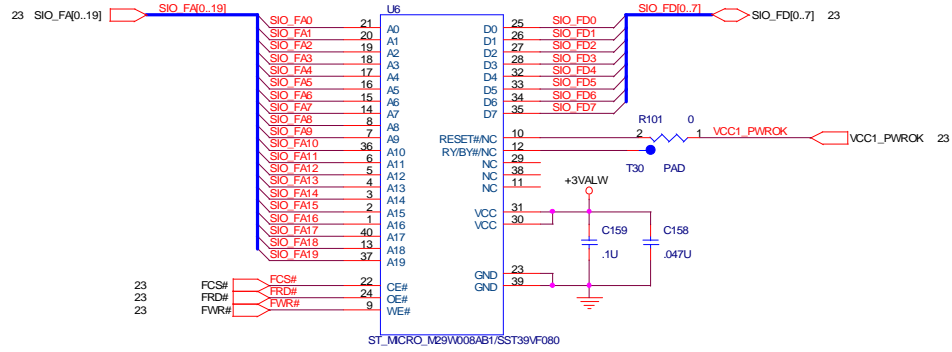


Title			Rev
SERIAL PORT			1A
Size	Document Number	DM1	
Date:	Friday, July 18, 2003	Sheet	24 of 46



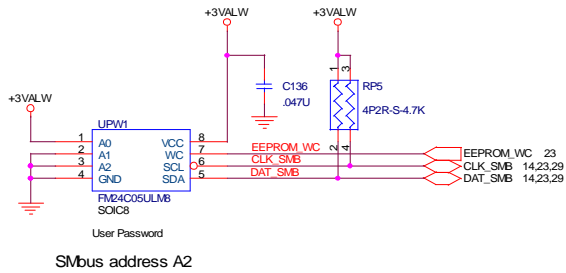
Title PARALLEL CONN.		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 25 of 46

8Mbit (1MByte),NO PLCC TYPE



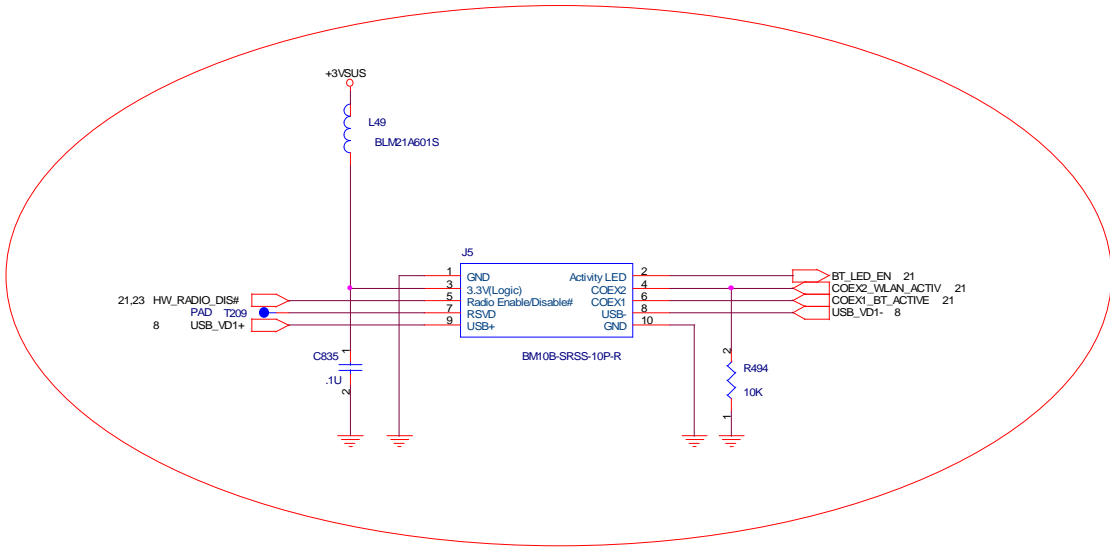
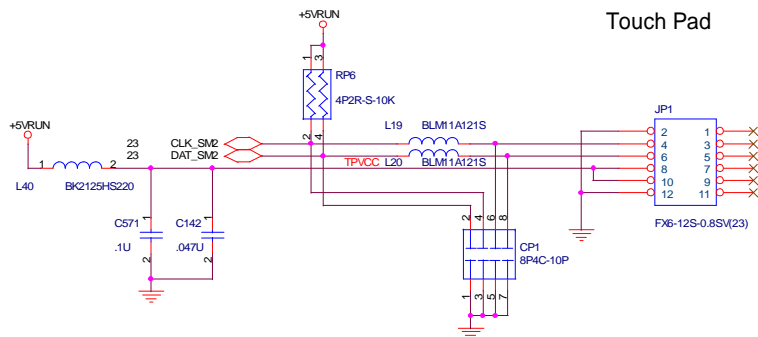
SST :Pin10,12 are NC

- 1.MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

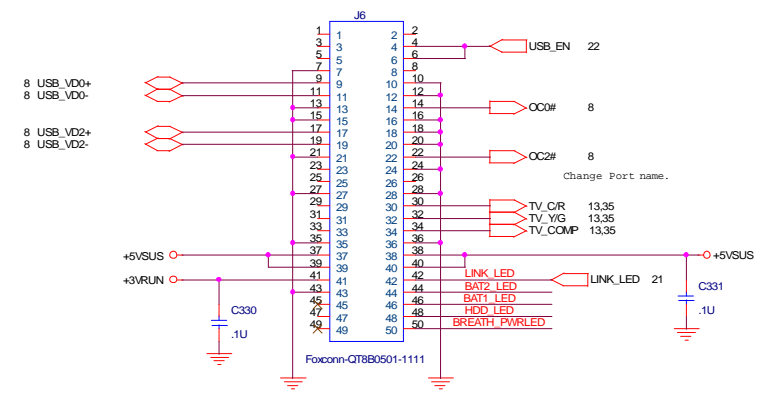
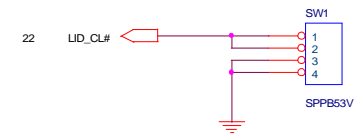
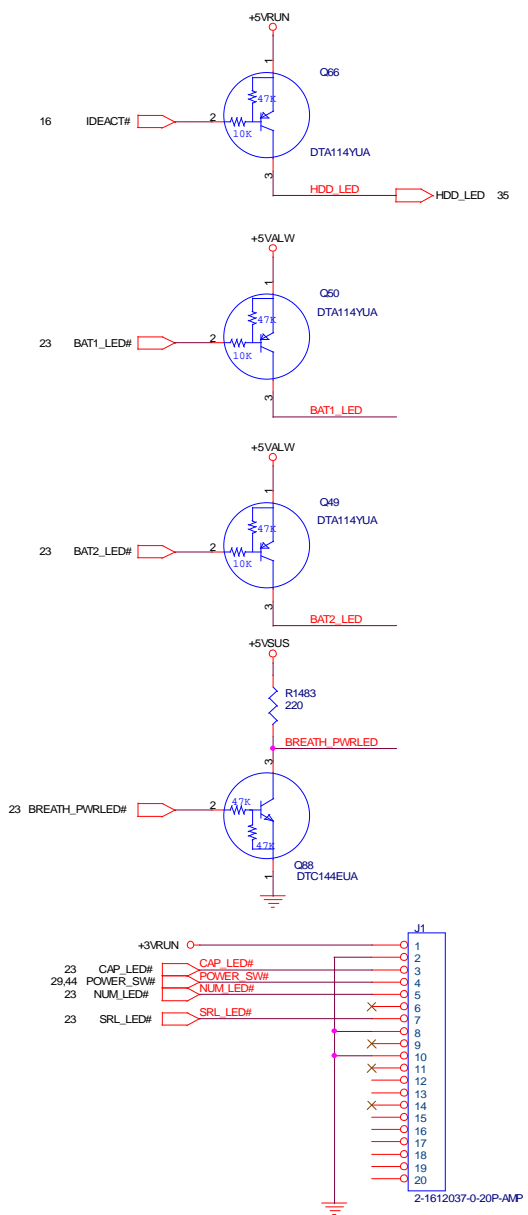


Title FLASH		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 26 of 46

Touch Pad



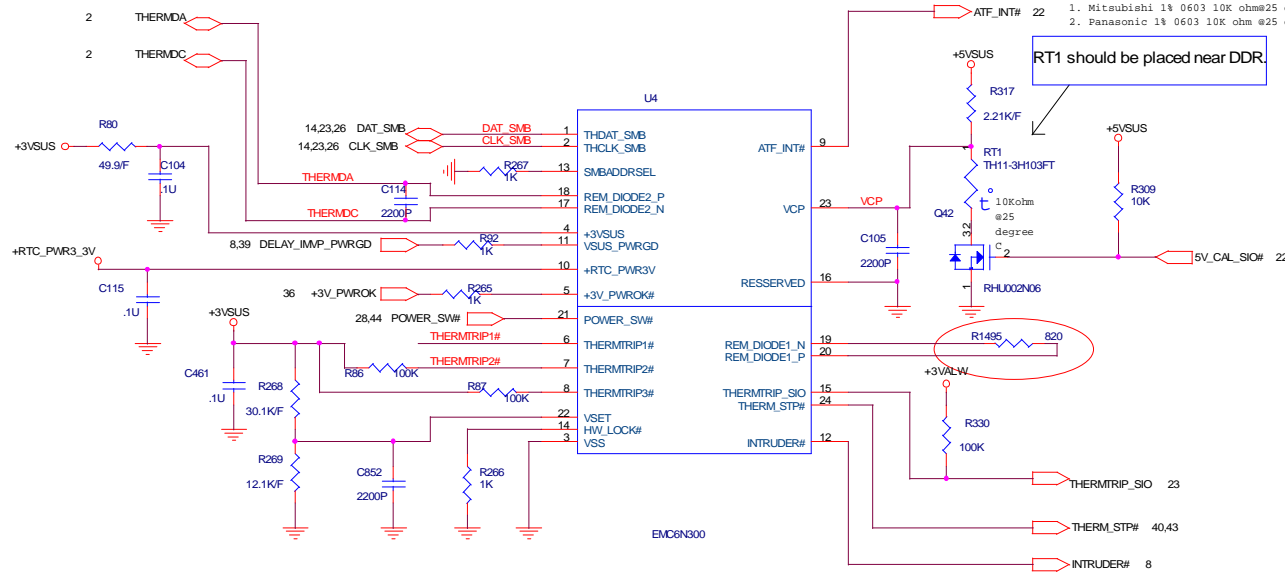
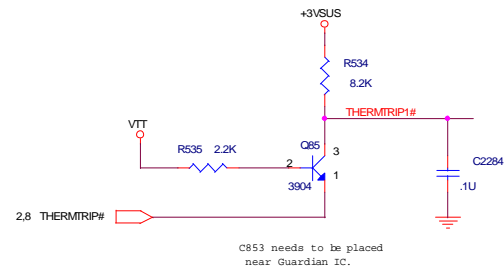
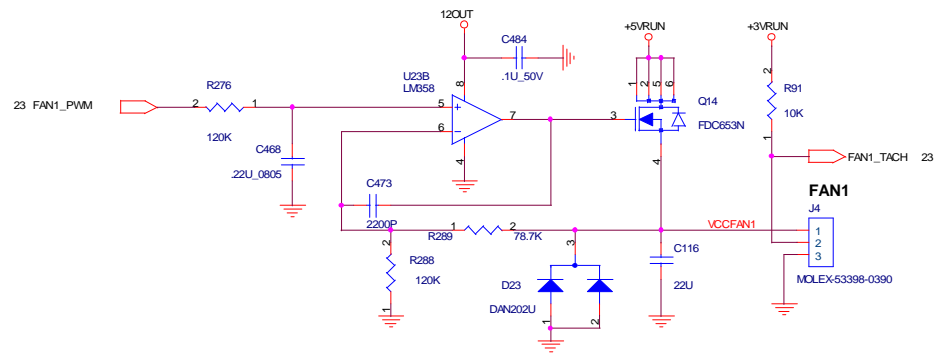
Title TOUCH PAD & BULE TOOTH		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 27 of 46



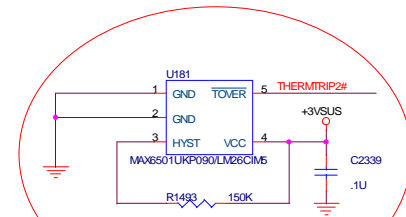
QUANTA COMPUTER

Title: SWITCH & LED

Size	Document Number	Rev
	DM1	1A
Date:	Friday, July 18, 2003	Sheet 28 of 46



- RT1:
 1. Mitsubishi 14 0603 10K ohm±25 degree C. P/N: TH11-3H103FT
 2. Panasonic 14 0603 10K ohm ±25 degree C. P/N: ERT31V0103FA



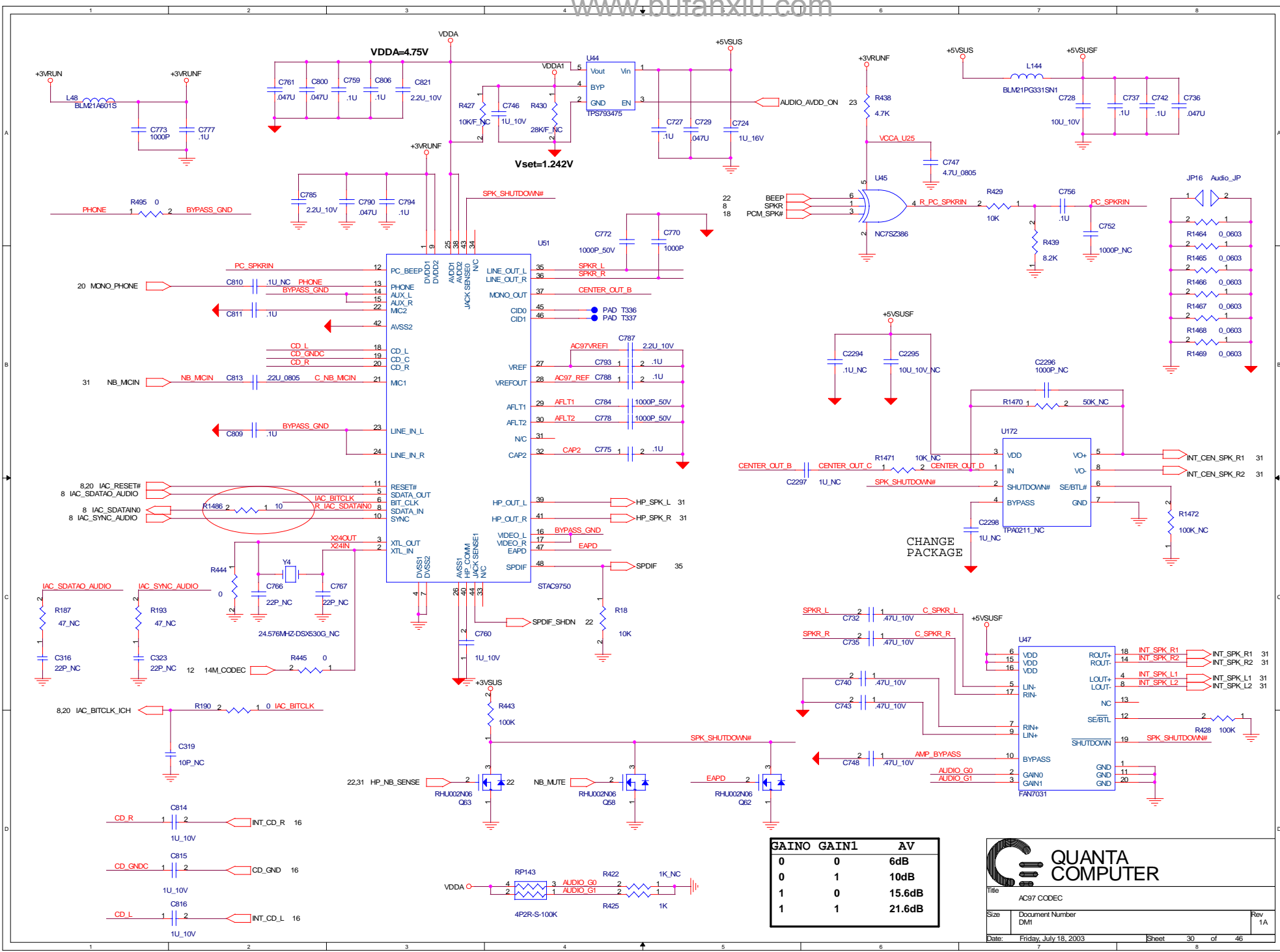
U136=LM26		
	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501		
	GND	VCC
HYST	2 degree	10 degree

Notes:
 $V_{set} = (T_p - 75) / 16$
 Where $T_p = 75$ to 106 degree C
 Set trip point = 90 degree C
 $V_{set} = (90 - 75) / 16 = 0.9375 V$
 Guardian temp-tolerance = ±3 degree C



Title: FAN & THERMAL		
Size: DM1	Document Number: DM1	Rev: 1A
Date: Friday, July 18, 2003	Sheet: 29	of 46



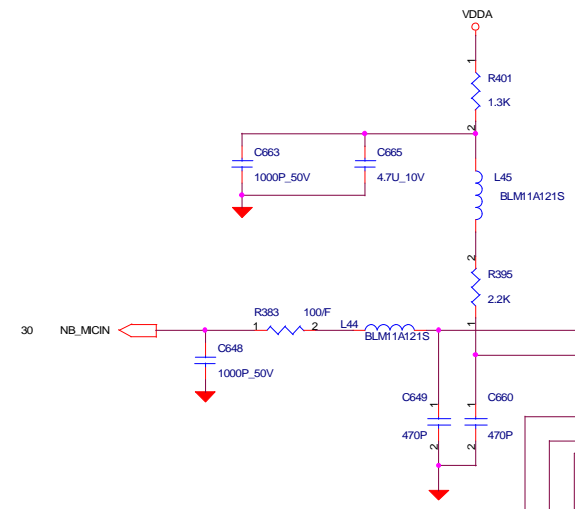
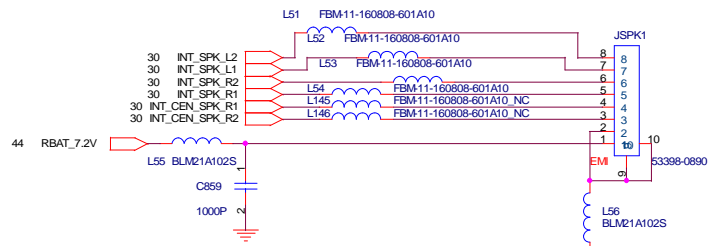
GAIN	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

QUANTA COMPUTER

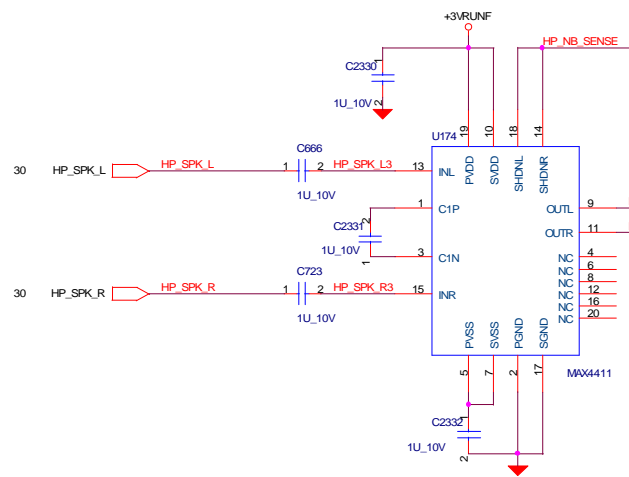
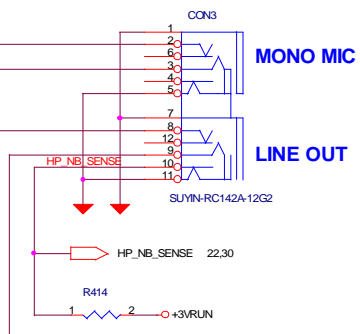
Title: AC97 CODEC

Size: Document Number DM1 Rev 1A

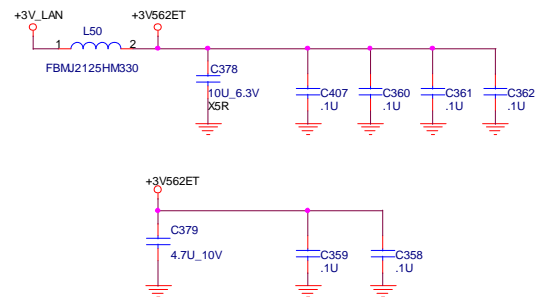
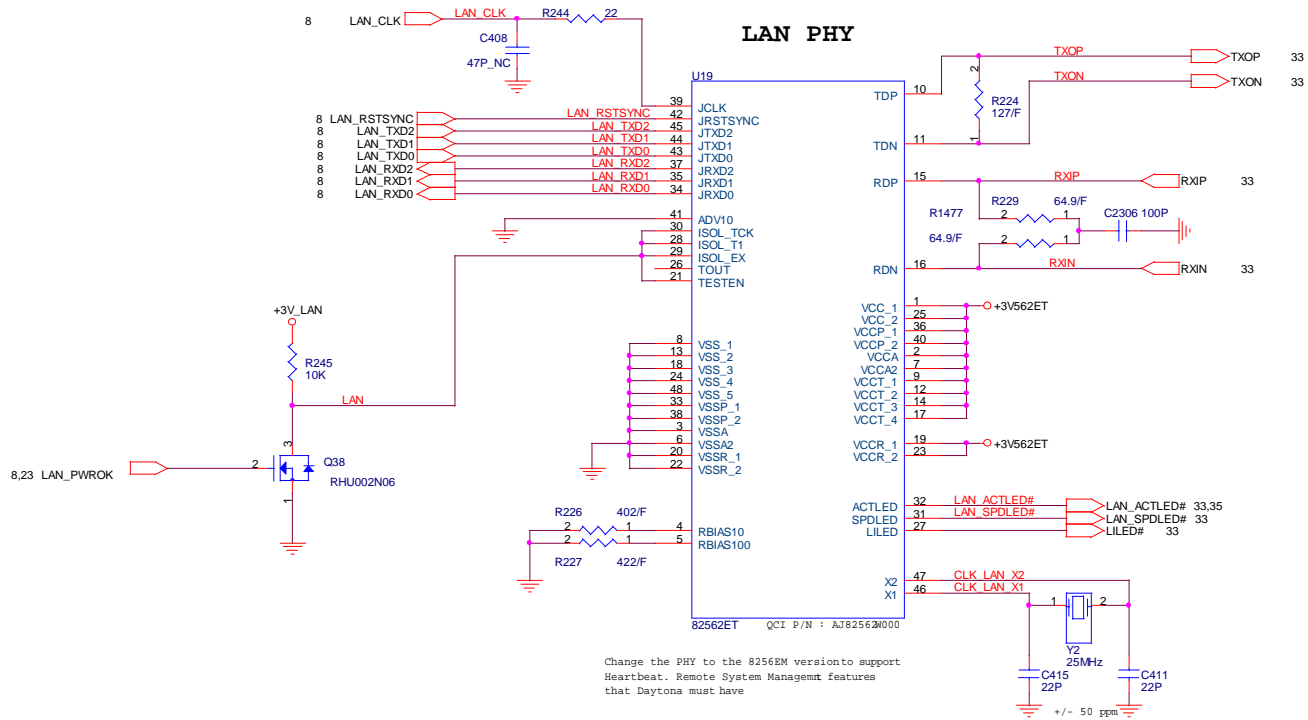
Date: Friday, July 18, 2003 Sheet 30 of 46



EXT MIC JACK



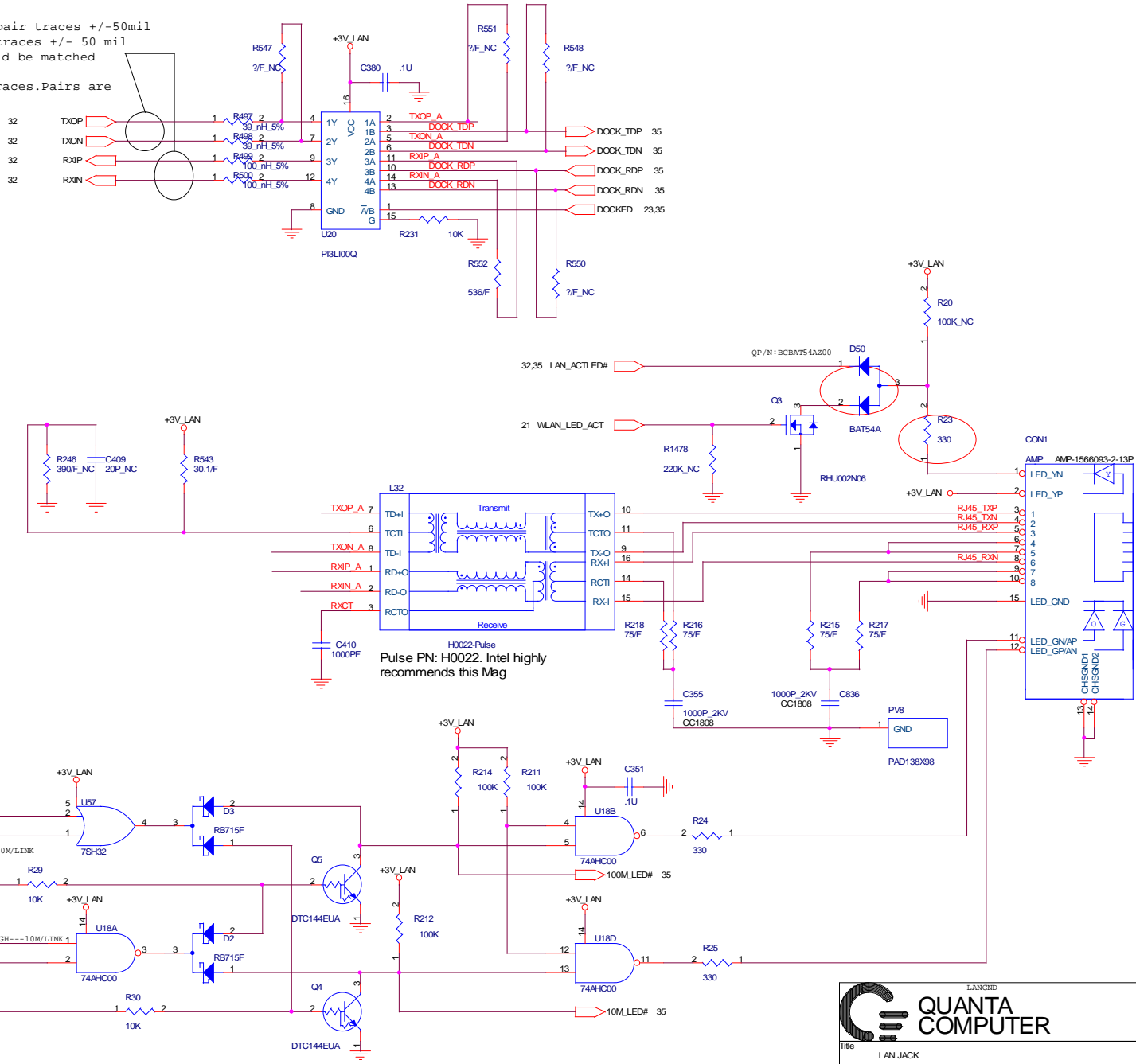
Title		
AUDIO CONN		
Size	Document Number	Rev
DM1		1A
Date:	Friday, July 18, 2003	Sheet 31 of 46



Match trace length

LAYOUT NOTES:

Match total length of chip side Rx and Tx pair traces +/-50mil
 Match length of cable side Rx and Tx pair traces +/- 50 mil
 Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
 Keep 50mil space between pairs and other traces. Pairs are 100ohm differential,

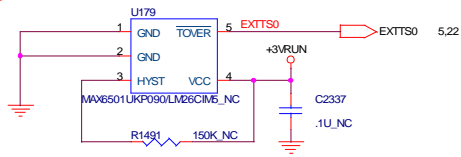
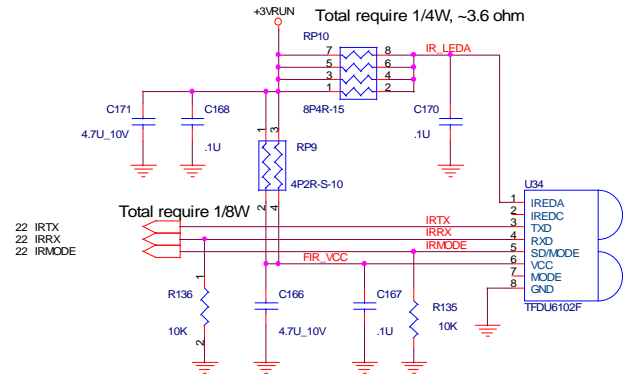


Pulse PN: H0022. Intel highly recommends this Mag

LAN_SPDLED#	SPEED
HI	10M
LO	100M



Title LAN JACK		
Size B	Document Number DM1	Rev 1A
Date: Friday, July 18, 2003	Sheet 33	of 46

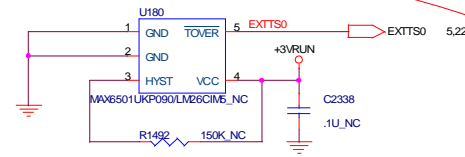


U136=LM26

	GND	VCC
HYST	10 degree	2 degree

U136=MAX6501

	GND	VCC
HYST	2 degree	10 degree



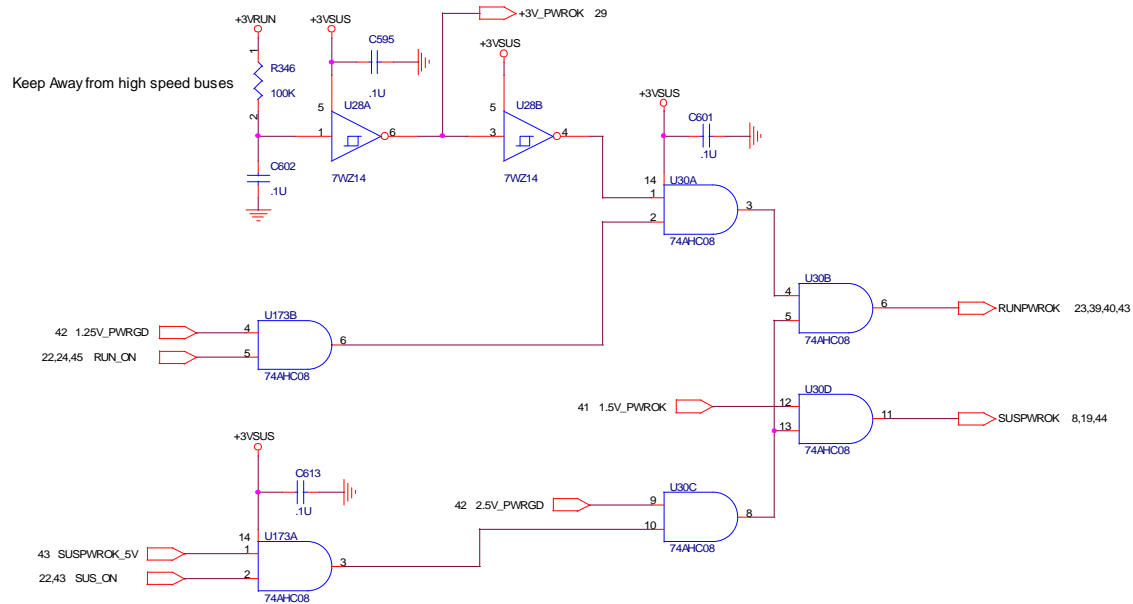
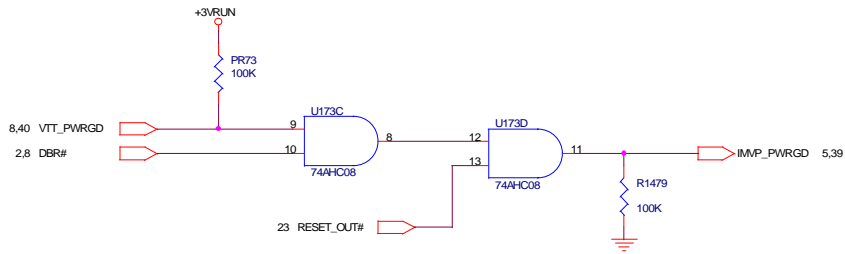
U136=LM26

	GND	VCC
HYST	10 degree	2 degree

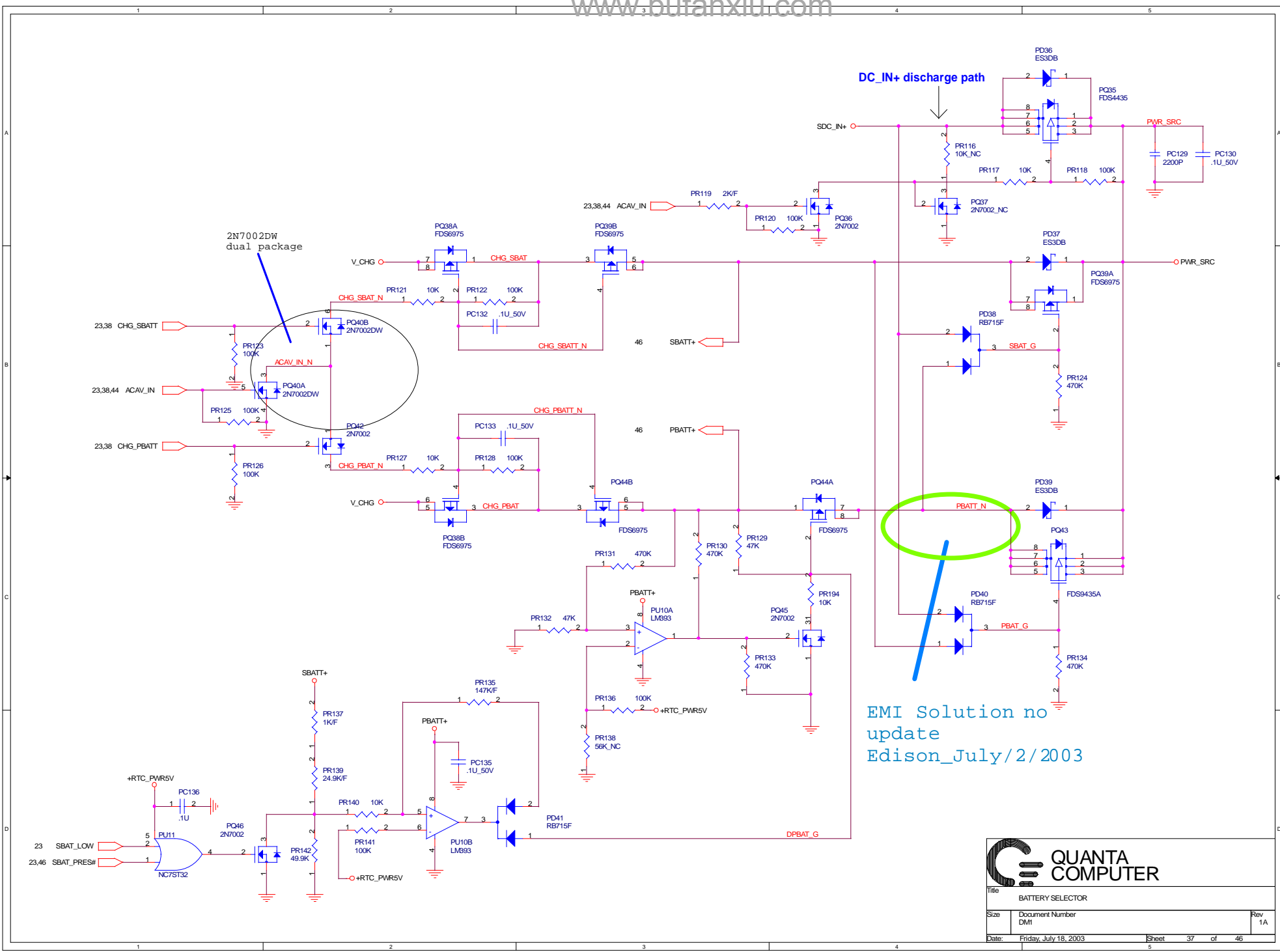
U136=MAX6501

	GND	VCC
HYST	2 degree	10 degree




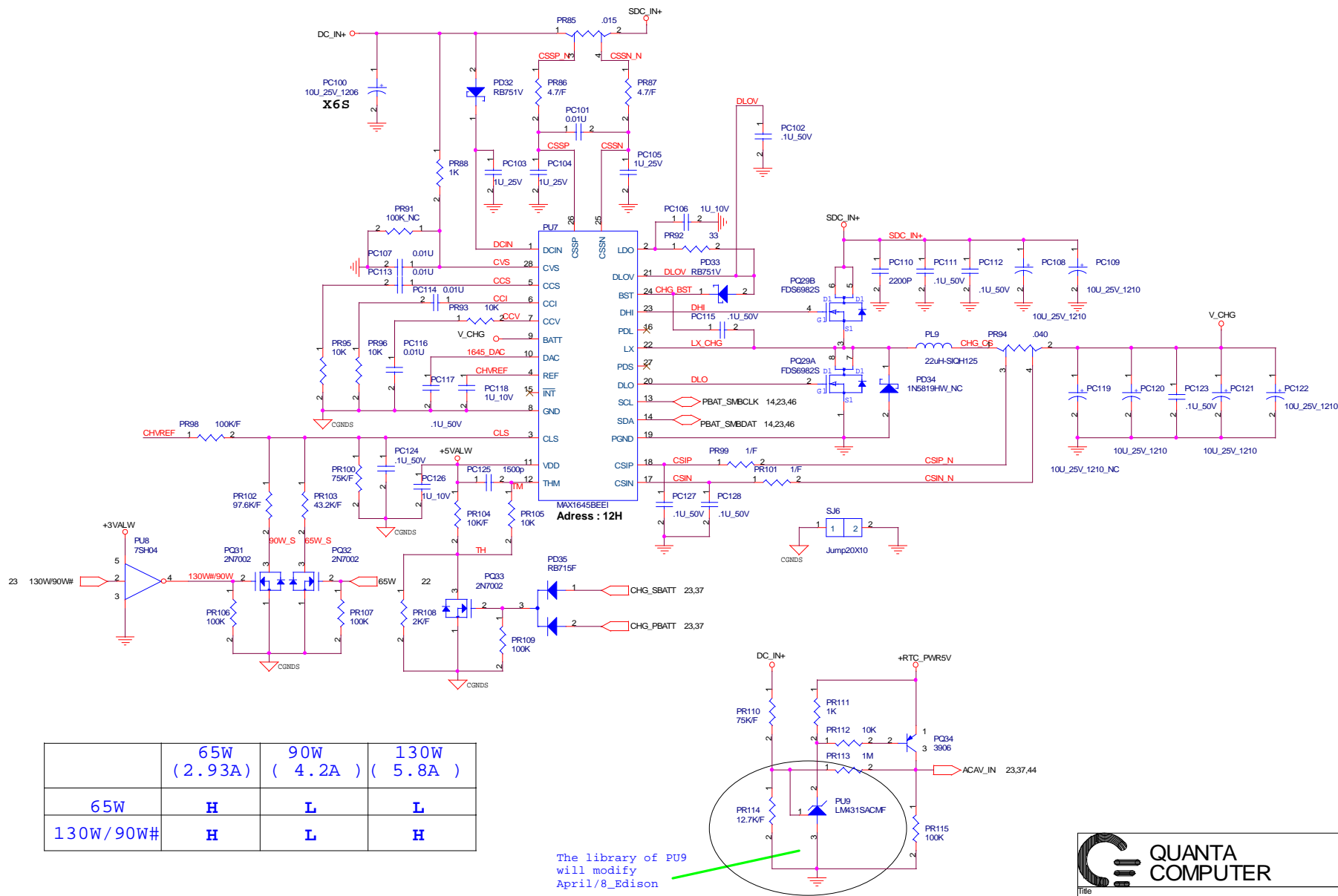


Title			POWER GOOD
Size	Document Number	Rev	
	DM1	1A	
Date:	Friday, July 18, 2003	Sheet	36 of 46



EMI Solution no update
Edison_July/2/2003

 QUANTA COMPUTER		
Title: BATTERY SELECTOR		
Size: DM1	Document Number: DM1	Rev: 1A
Date: Friday, July 18, 2003	Sheet: 37	of 46

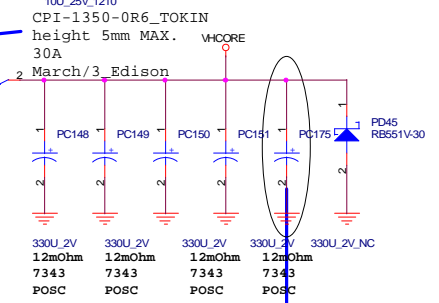
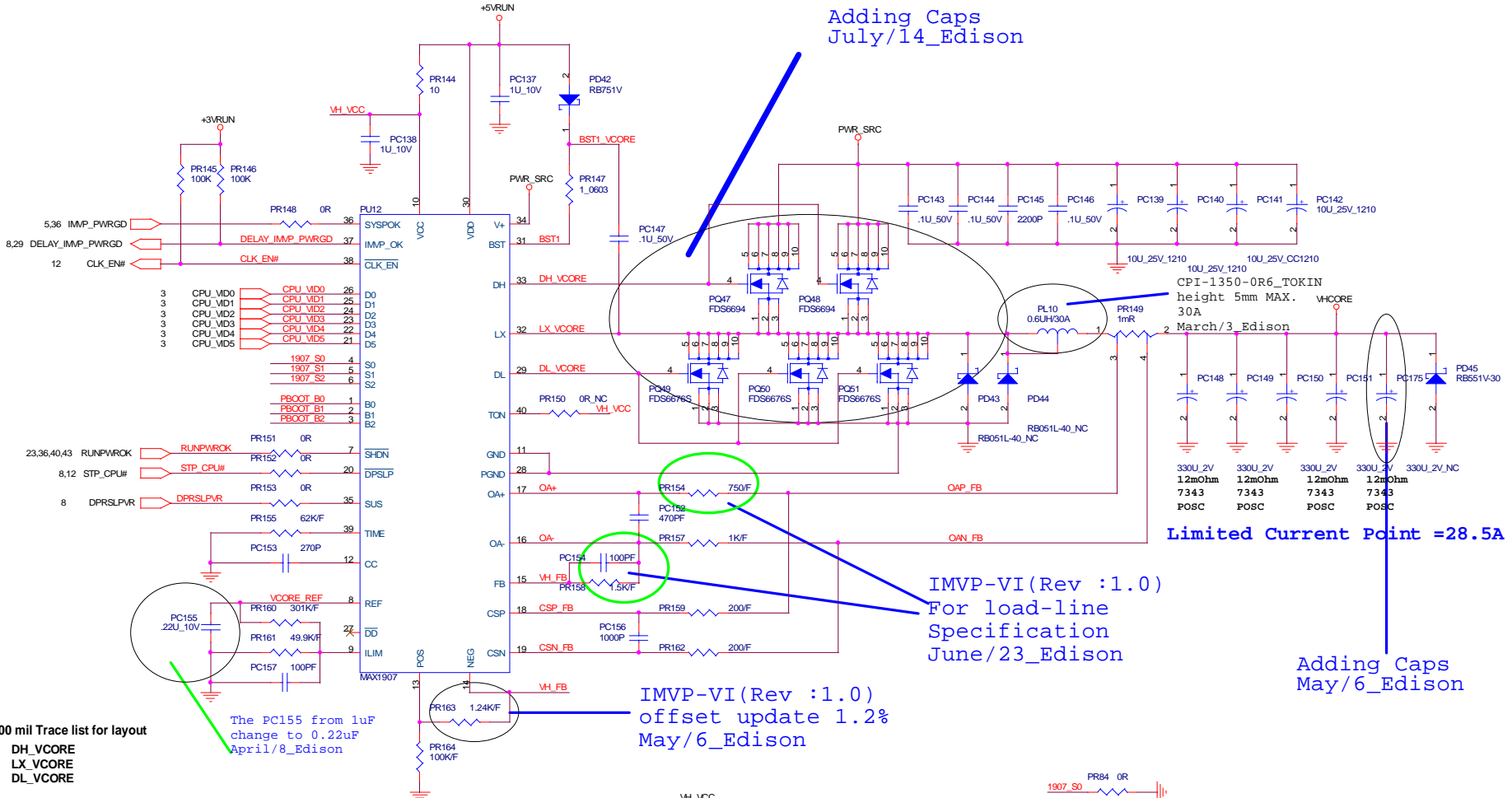


	65W (2.93A)	90W (4.2A)	130W (5.8A)
65W	H	L	L
130W/90W#	H	L	H

The library of PU9 will modify April/8_Edison



Adding Caps
July/14_Edison



Limited Current Point = 28.5A

IMVP-VI (Rev : 1.0)
For load-line
Specification
June/23_Edison

IMVP-VI (Rev : 1.0)
offset update 1.2%
May/6_Edison

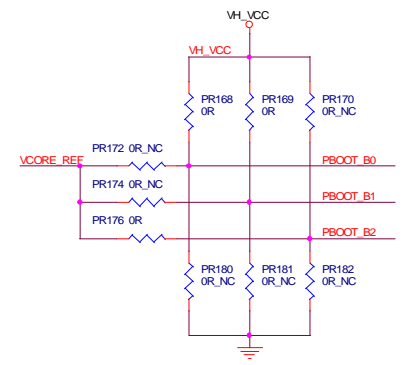
Adding Caps
May/6_Edison

100 mil Trace list for layout

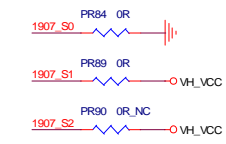
- DH_VCORE
- LX_VCORE
- DL_VCORE

The PC155 from 1uF
change to 0.22uF
April/8_Edison

V I D							Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	0	1	1	1	1	1.468	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	



PBOOT VOLTAGE
SETTING UP ON
1.212V



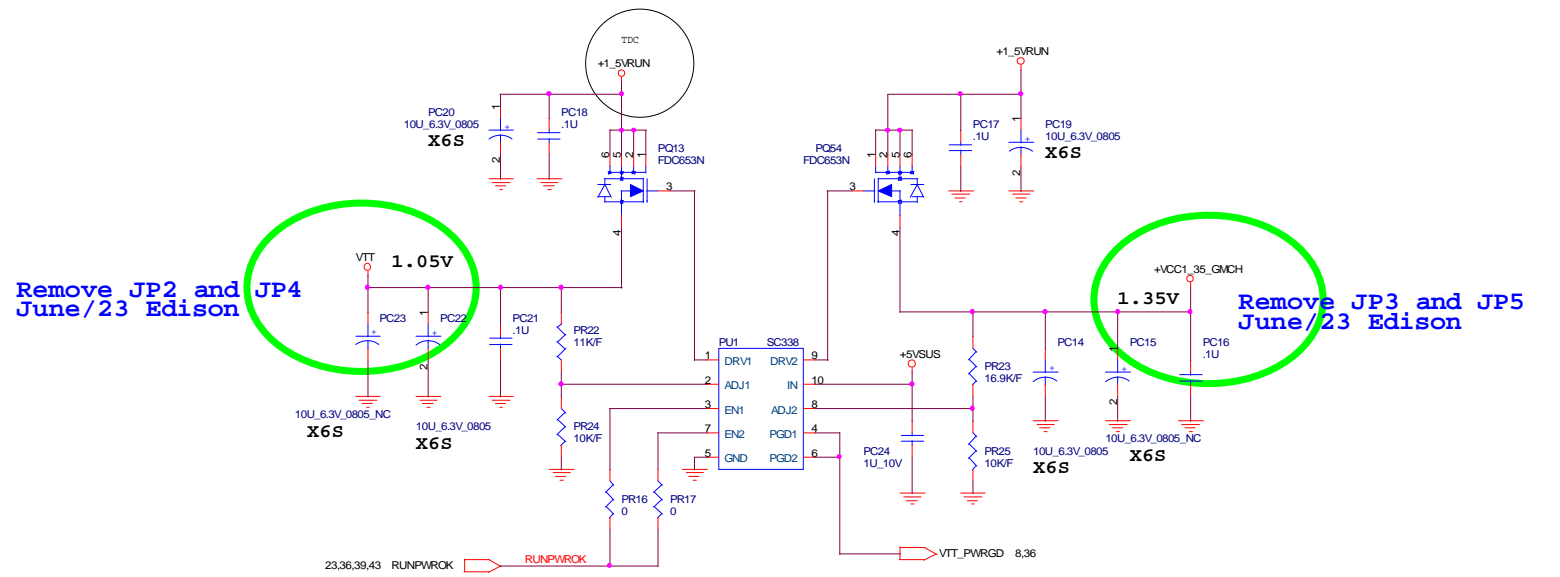
The C4 mode voltage is 0.748V

QUANTA COMPUTER

Title: CPU POWER

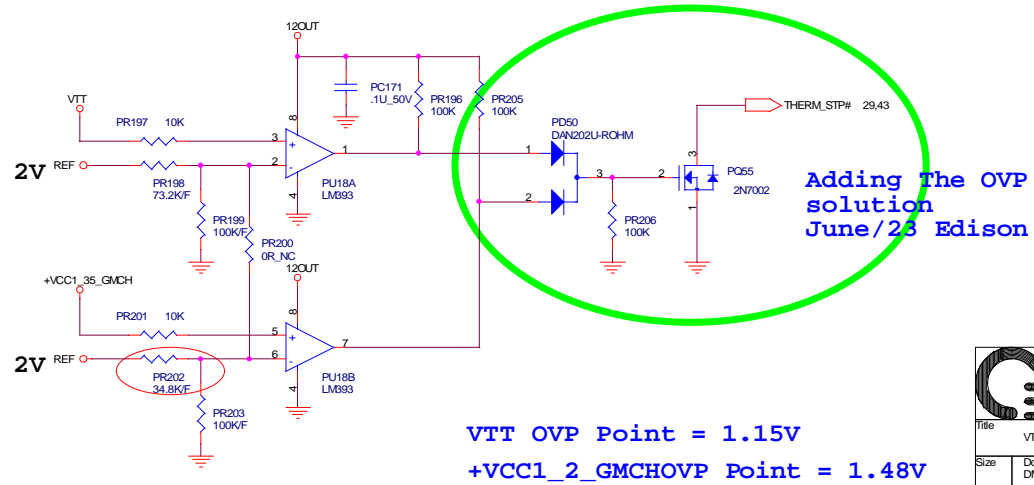
Size: Document Number DM1 Rev 1A

Date: Friday, July 18, 2003 Sheet 39 of 46



VTT Current Limite 3.2A

1.20V - GM, PR23=14.0K/F
 1.35V - GM+ PR23=16.9K/F
 +VCC1_2_GMCH Current Limite 3.2A



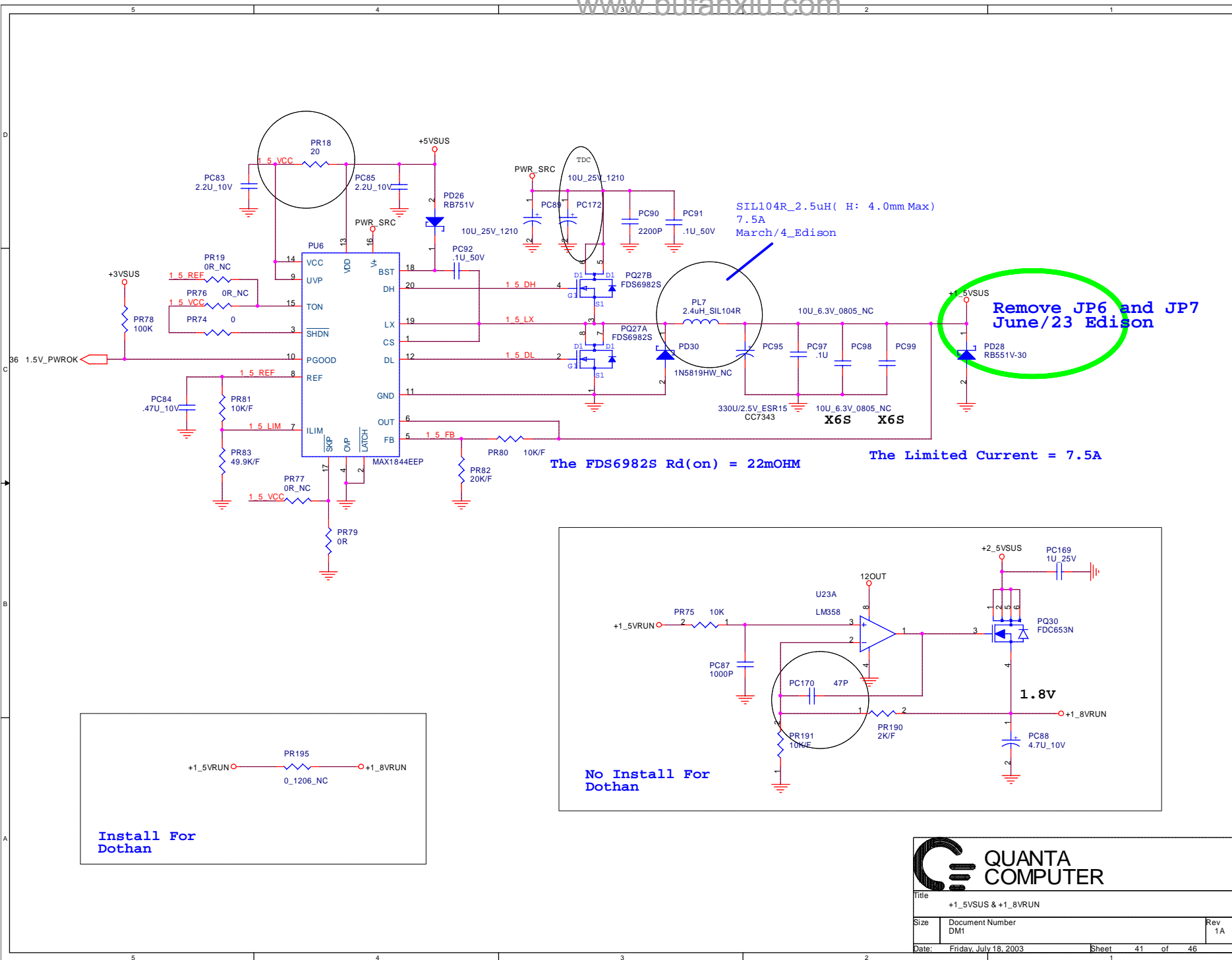
VTT OVP Point = 1.15V
 +VCC1_2_GMCHOVP Point = 1.48V

QUANTA COMPUTER

Title: VTT_VCC1_2_MCH

Size: Document Number DM1 Rev 1A

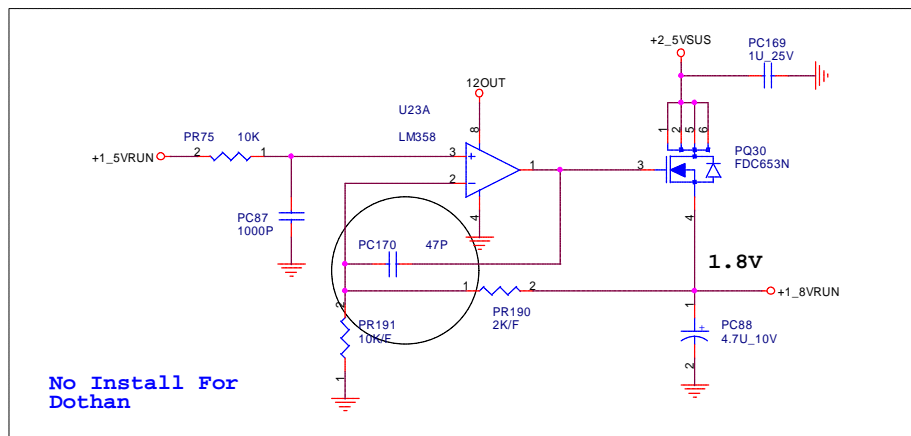
Date: Friday, July 18, 2003 Sheet 40 of 46



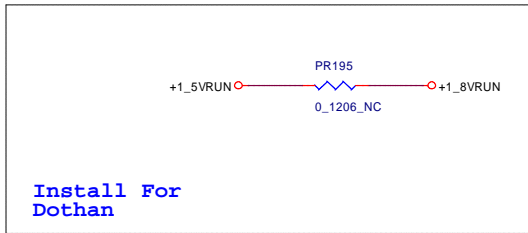
Remove JP6 and JP7
June/23 Edison

The FDS6982S Rd(on) = 22mOHM

The Limited Current = 7.5A



No Install For
Dothan

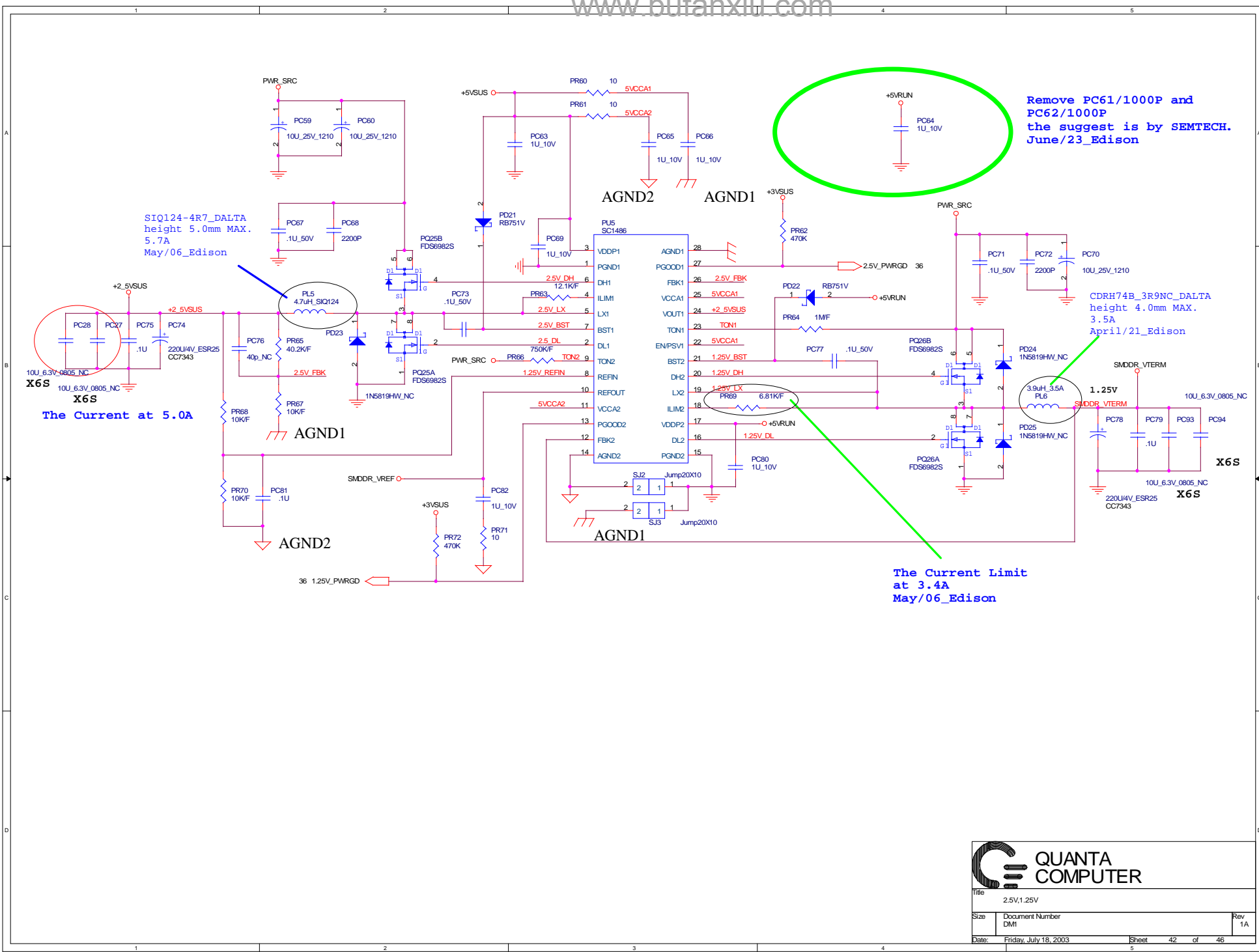


Install For
Dothan

QUANTA COMPUTER

Title: +1_5VSUS & +1_8VRUN

Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 41 of 46



Remove PC61/1000P and PC62/1000P
the suggest is by SEMTECH.
June/23_Edison

SIQ124-4R7_DALTA
height 5.0mm MAX.
5.7A
May/06_Edison

CDRH74B_3R9NC_DALTA
height 4.0mm MAX.
3.5A
April/21_Edison

10U_6.3V_0805_NC
X6S
10U_6.3V_0805_NC
X6S
The Current at 5.0A

1.25V
SMDDR_VTERM
10U_6.3V_0805_NC
X6S
220U/4V_ESR25
CC7343
X6S

The Current Limit
at 3.4A
May/06_Edison



Title		2.5V,1.25V
Size	Document Number	DM1
Date:	Friday, July 18, 2003	Sheet 42 of 46
		Rev 1A

Remove JP12 and JP14
June/23 Edison

Current limit at 4A for +3.3V

Place these CAPs close to FETs

SIL104R_100NC_DELTA
height 4.0mm MAX.
4.4A
April/8_Edison

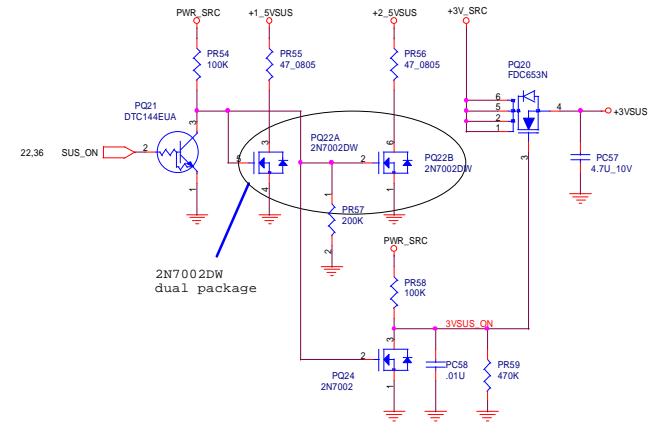
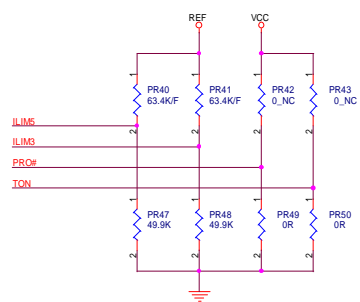
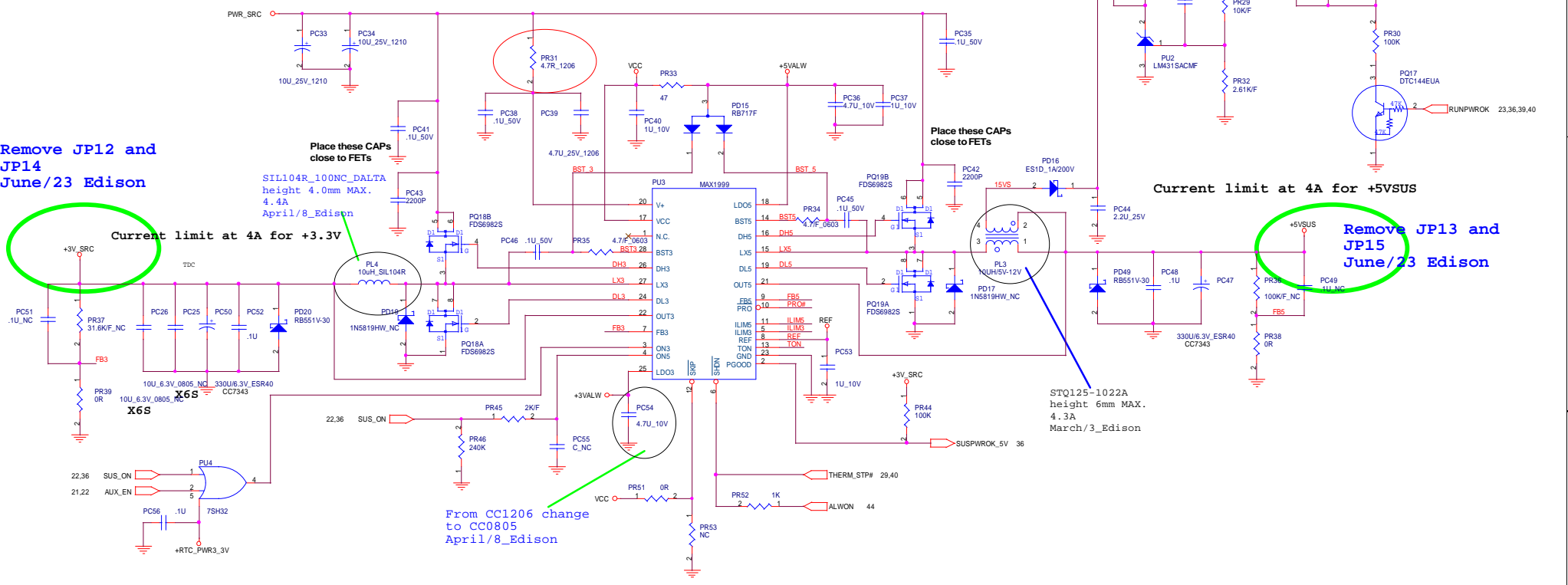
Place these CAPs close to FETs

Current limit at 4A for +5VSUS

Remove JP13 and JP15
June/23 Edison

From CC1206 change to CC0805
April/8_Edison

STQ125-1022A
height 6mm MAX.
4.3A
March/3_Edison

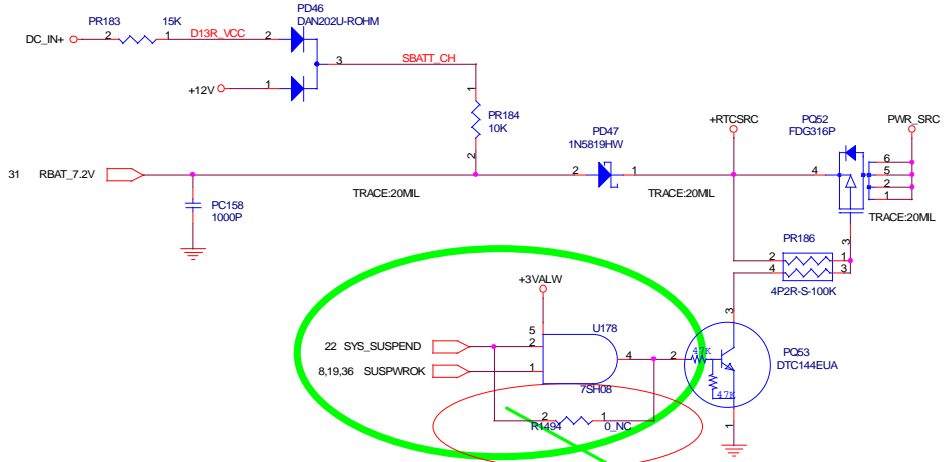


QUANTA COMPUTER

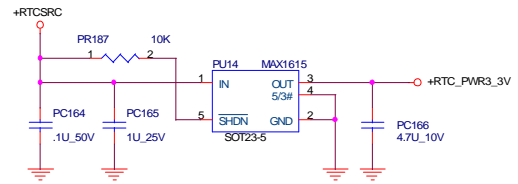
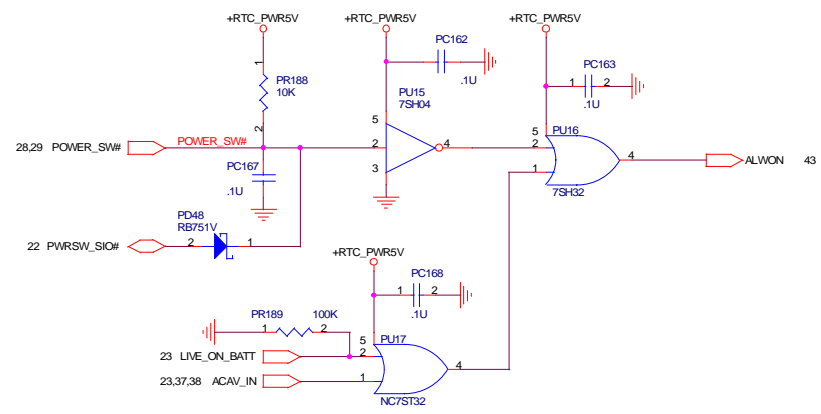
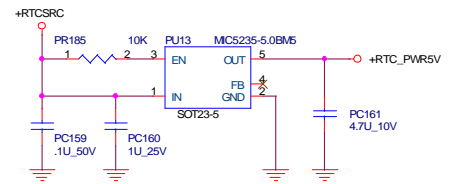
Title: +3VSRV & +3VSUS & +5VSUS

Size: Document Number DM1 Rev 1A

Date: Friday, July 18, 2003 Sheet 43 of 46



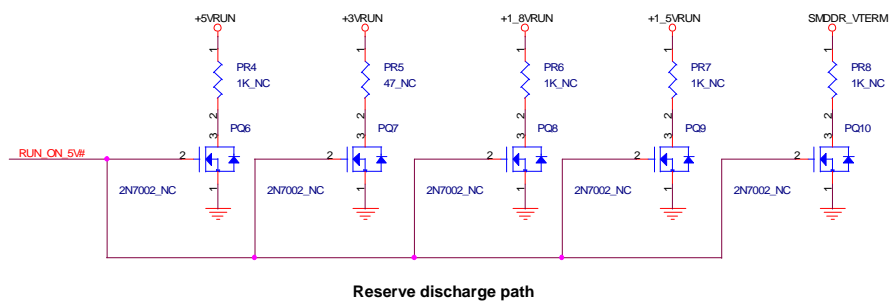
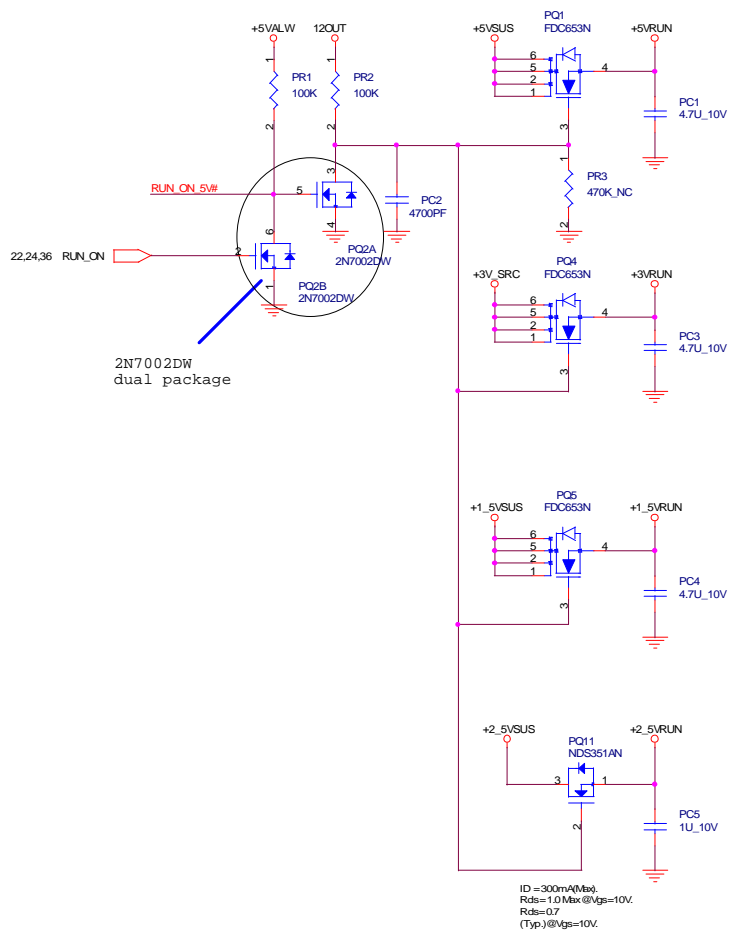
Adding RBATT protection
Edison_July/08/2003



QUANTA COMPUTER

Title: DCIN.BATT CONNECTOR

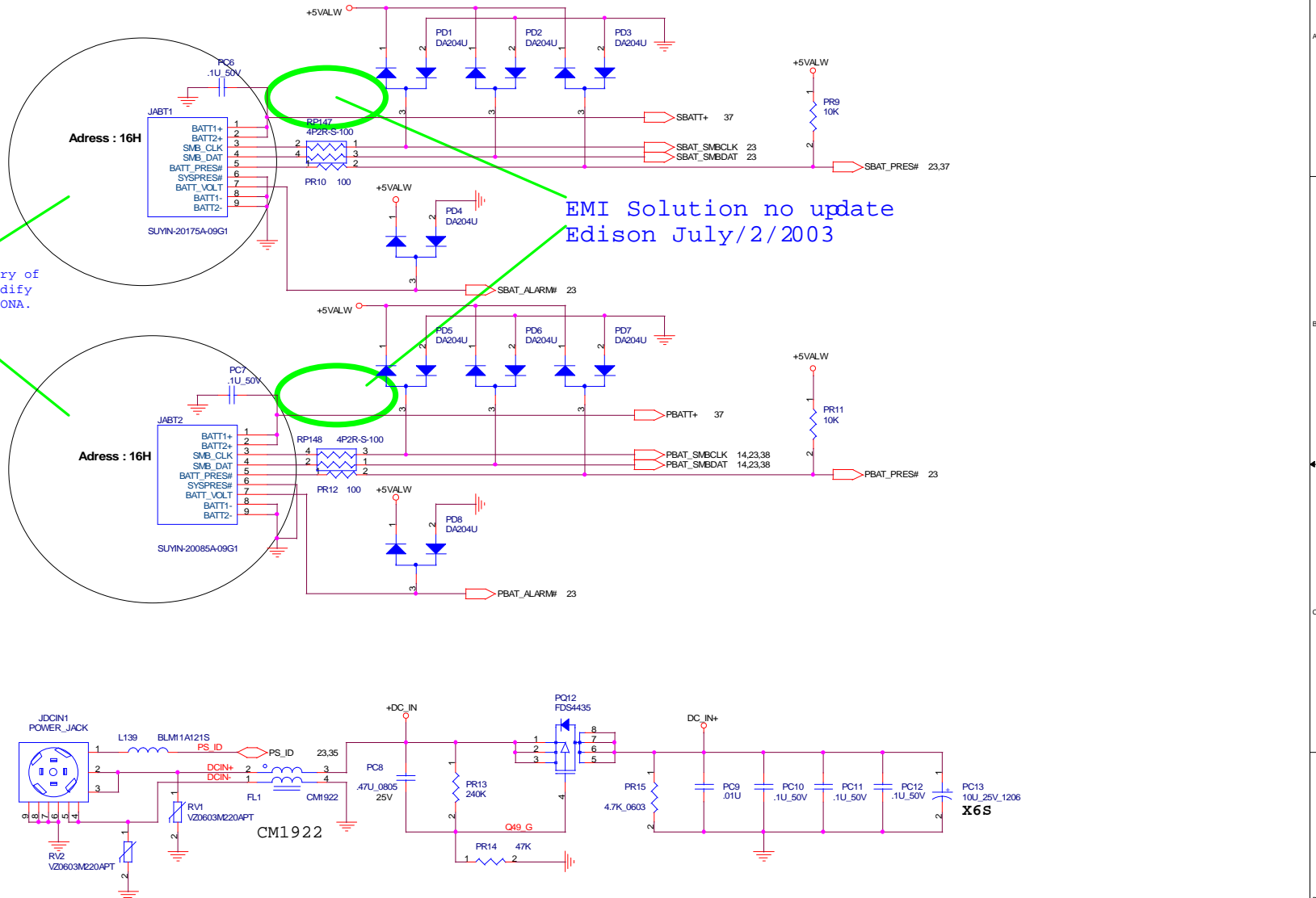
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 44 of 46



Title		
RUN POWER SW		
Size	Document Number	Rev
DM1		1A
Date:	Friday, July 18, 2003	Sheet 45 of 46

will the library of JABT1&JABT2 modify same with DAYTONA. April/8_Edison

EMI Solution no update Edison July/2/2003



Title DCIN.BATT CONNECTOR		
Size	Document Number DM1	Rev 1A
Date:	Friday, July 18, 2003	Sheet 46 of 46