

Model Name: KAT00 UMA
PCB NO: LA-5152P
BOM P/N: 43169631L01

Compal Confidential

Schematic Document

POITIER Montevina


2008 / 06 / 15 Rev:1.0

MB PCB

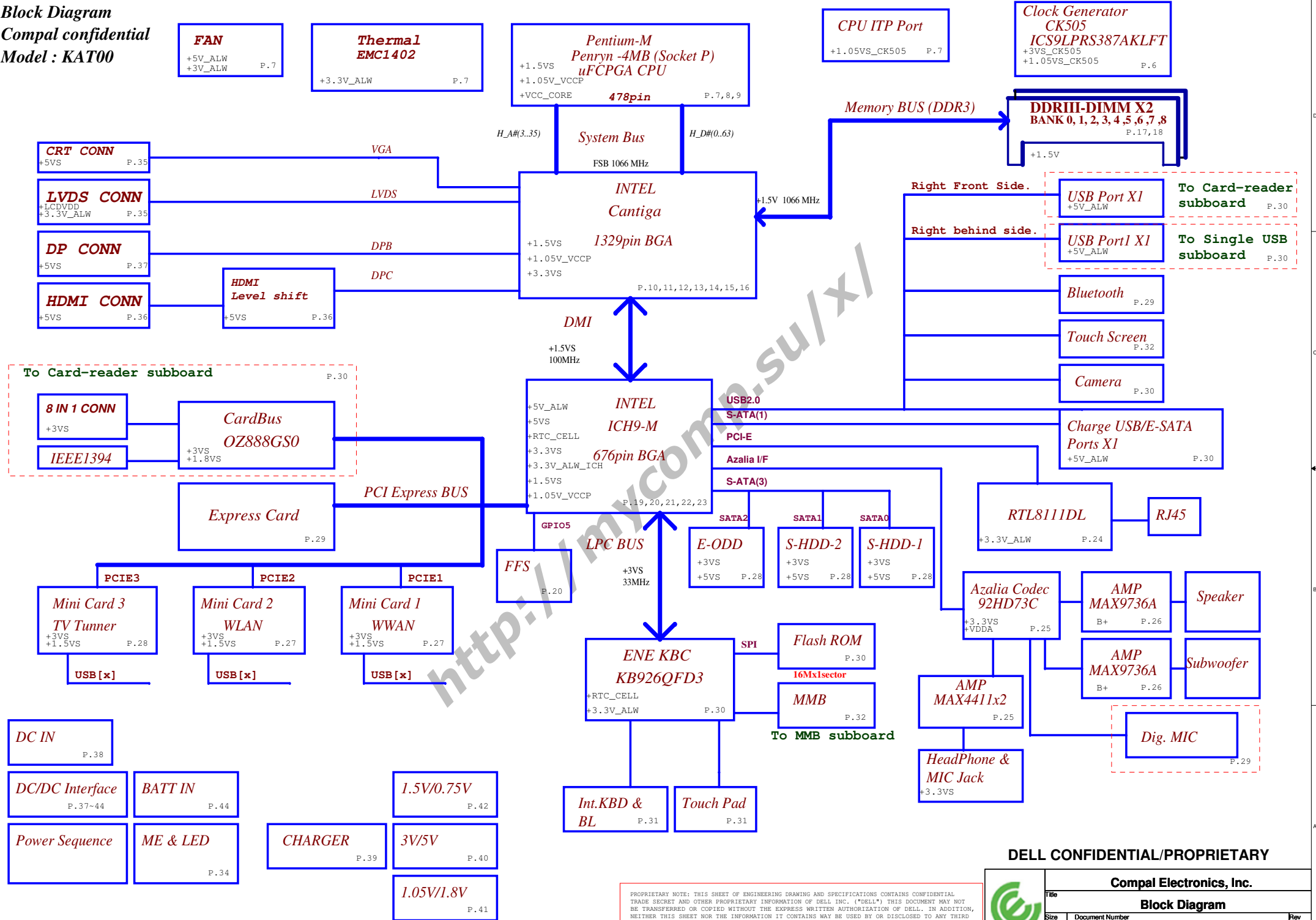
Part Number	Description
DAB0000E510	PCB 080 LA-5152P REV1 UMA M/B

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	Title Cover Sheet		
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Block Diagram
Compal confidential
Model : KAT00



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Voltage Rails **O MEANS ON** **X MEANS OFF**

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +VCCP +0.75VS +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

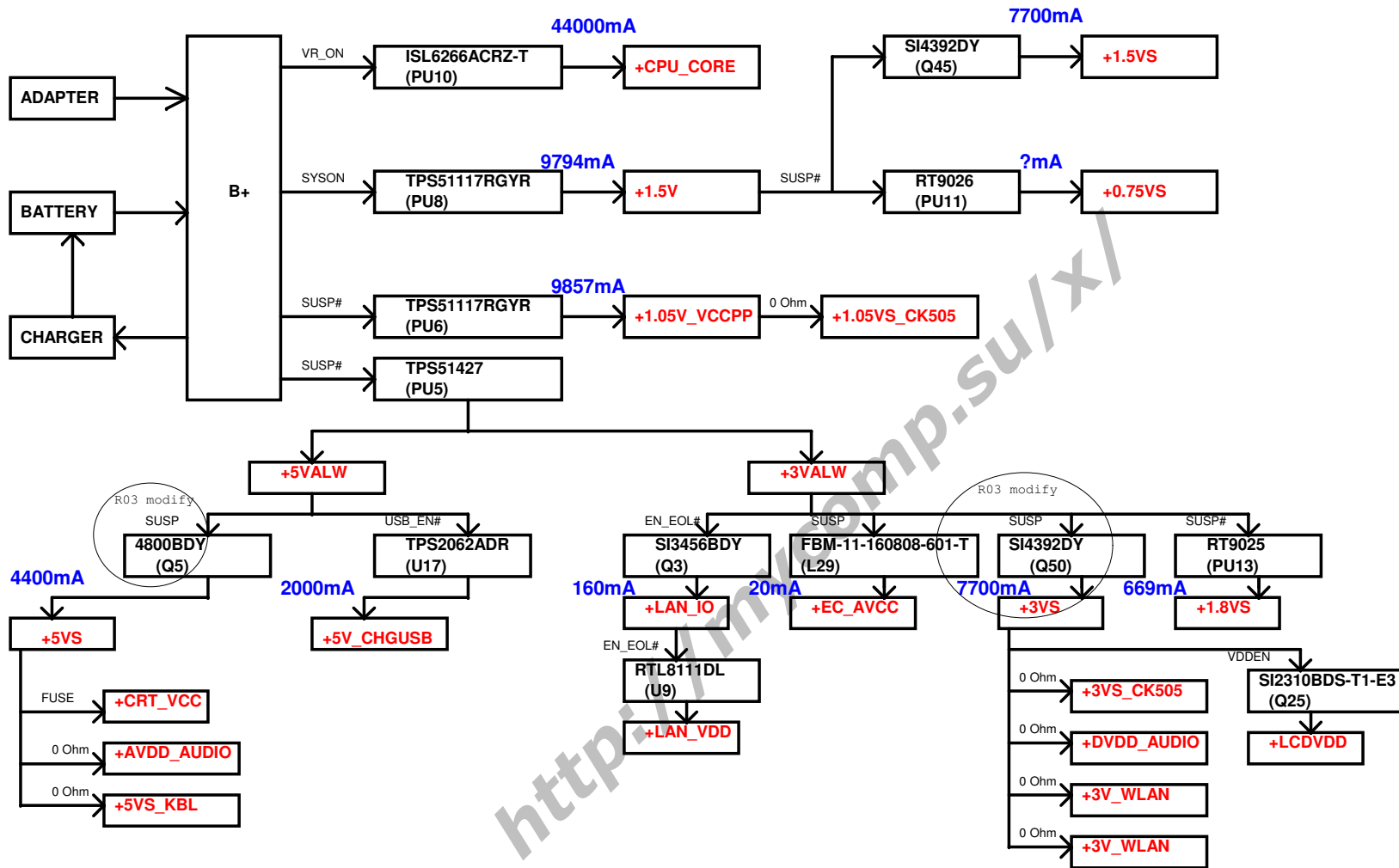
SATA Port	Device
0	JSATA2
1	JSATA1
2	JESA1
3	JODD

PCIe Port	Device
1	JWWAN1
2	JWLAN1
3	JWPAN1
4	Reader/BD (OZ888)
5	JEXP1
6	RTL8111DL

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Note List			
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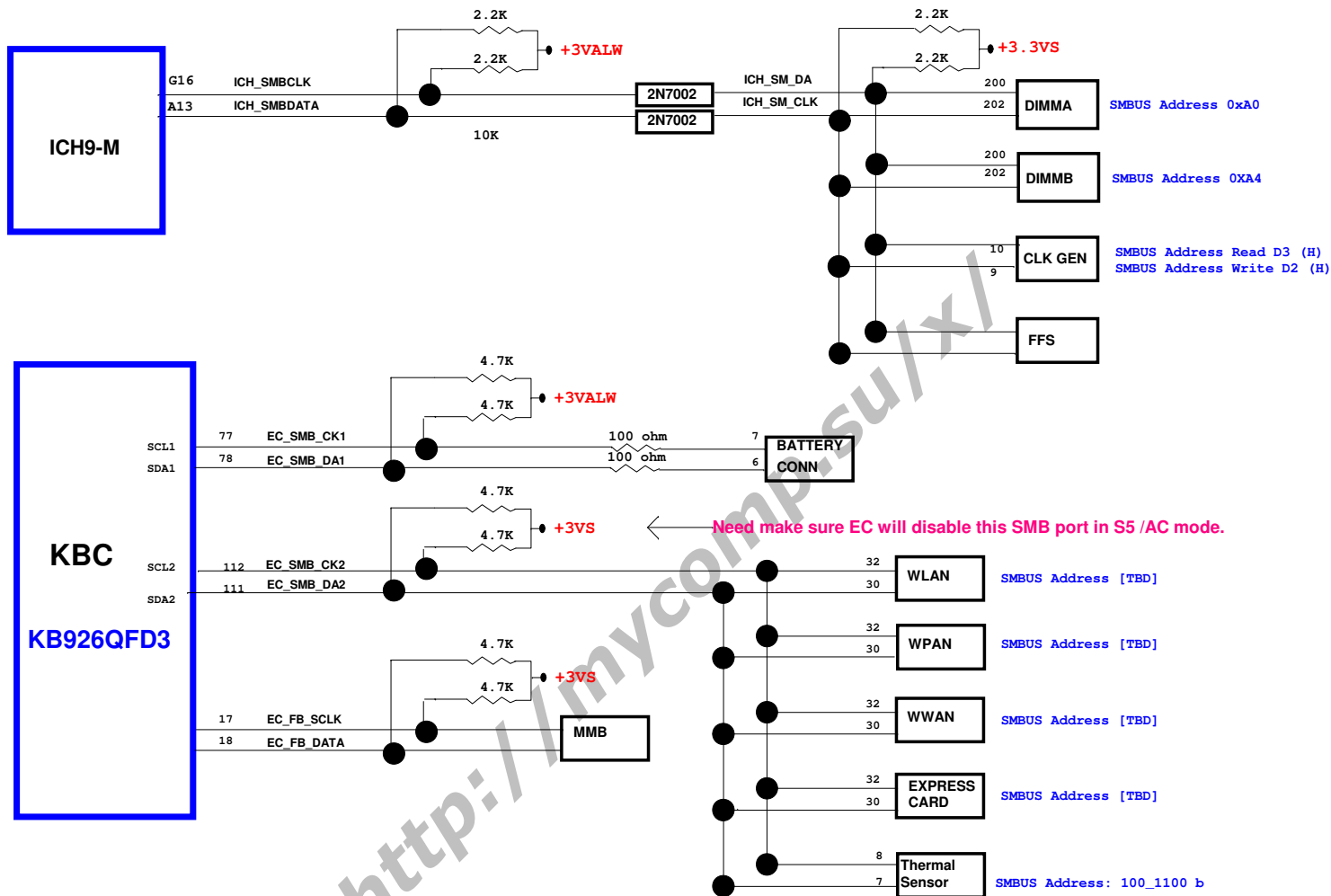


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Power Rail		
LA-5152P		
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Need make sure EC will disable this SMB port in S5 /AC mode.

I2C / SMBUS ADDRESSING

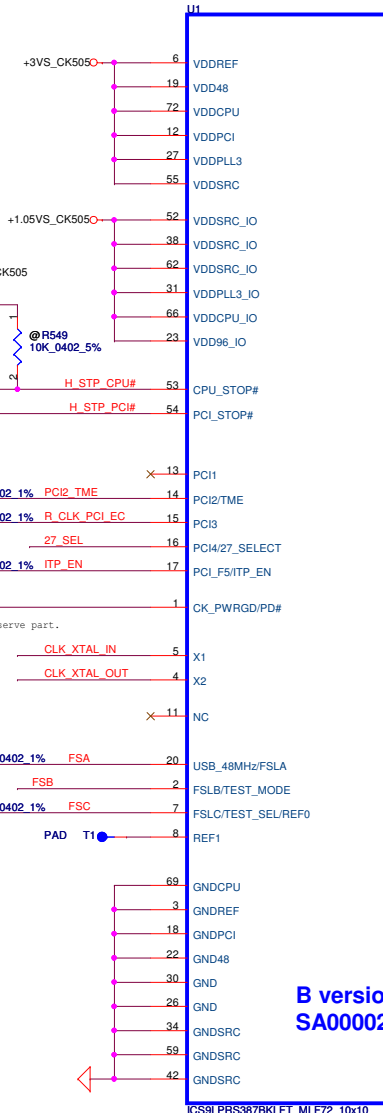
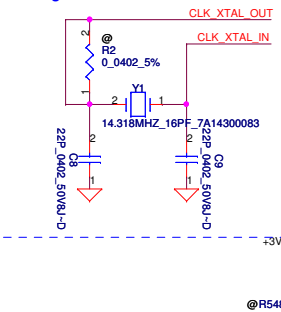
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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Compal Electronics, Inc.		
SMBUS TOPOLOGY		
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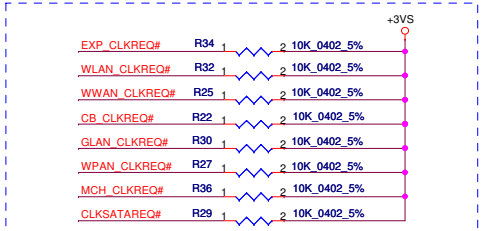
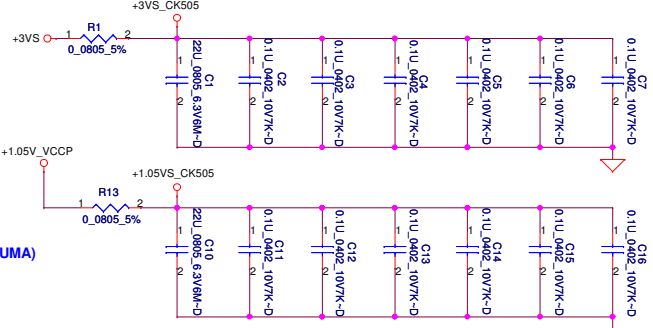
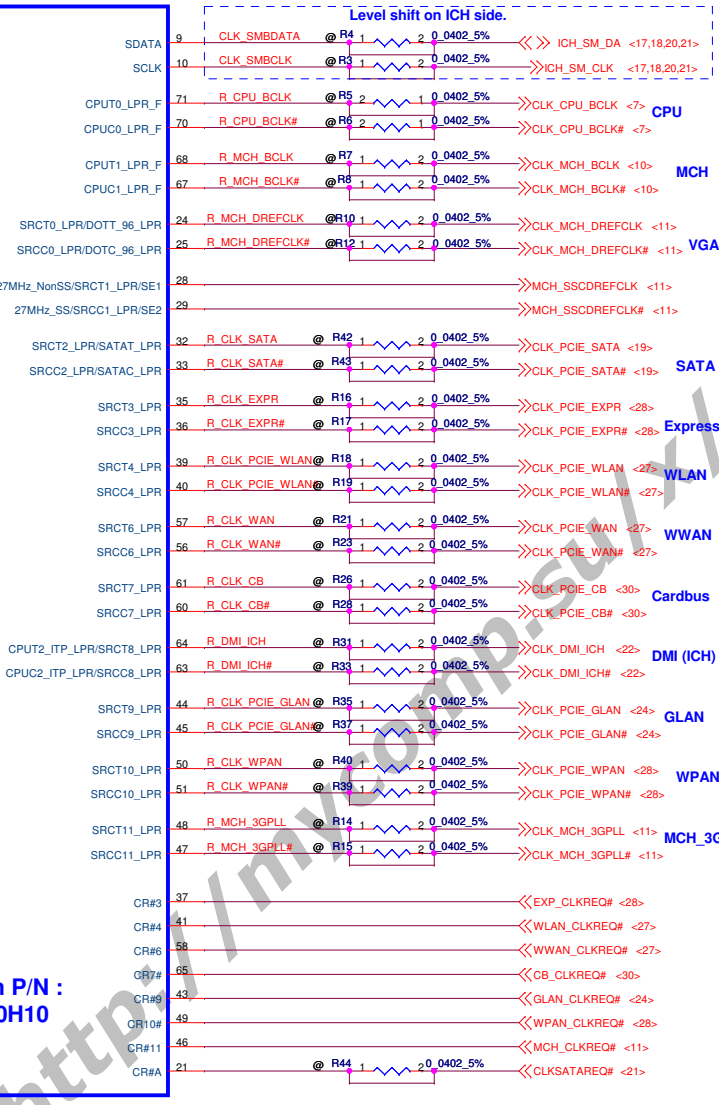
Routing the trace at least 10mil



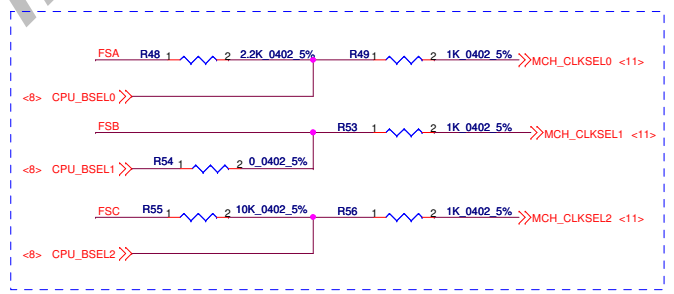
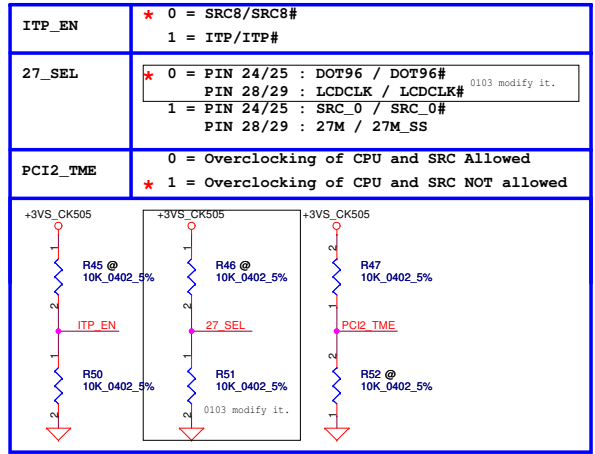
B version P/N : SA00020H10

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						

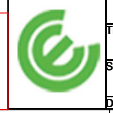
Reserved



Port	Device	REQ#	REQ# NAME
SRC0	PCIE_VGA		
SRC2	PCIE_SATA	REQ_A#	CLKSATAREQ#
SRC3	PCIE_EXPR	REQ#3	EXP_CLKREQ#
SRC4	PCIE_WLAN	REQ#4	WLAN_CLKREQ#
SRC6	PCIE_WWAN	REQ#6	WWAN_CLKREQ#
SRC7	PCIE_CB	REQ#7	CB_CLKREQ#
SRC8	DMI_ICH		
SRC9	PCIE_GLAN	REQ#9	GLAN_CLKREQ#
SRC10	PCIE_WPAN	REQ#10	WPAN_CLKREQ#
SRC11	MCH_3GPLL	REQ#11	MCH_CLKREQ#

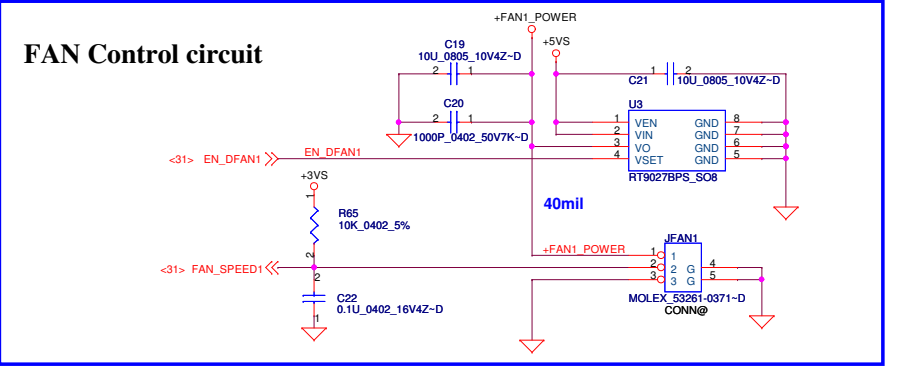
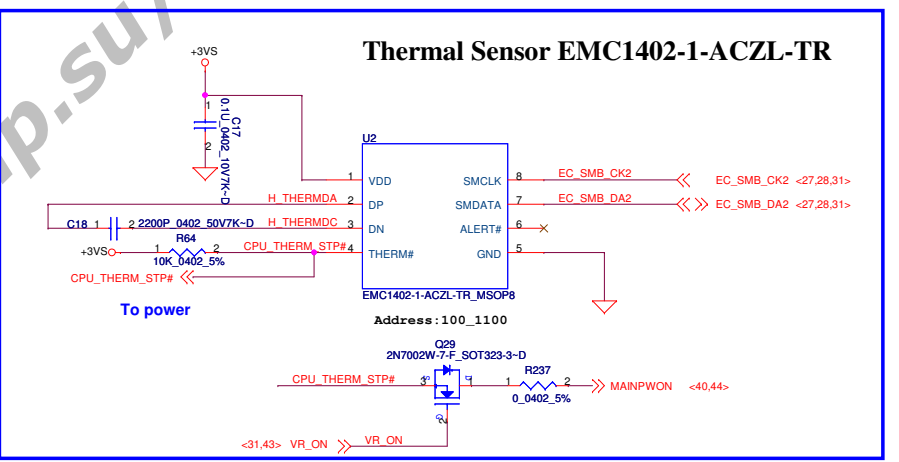
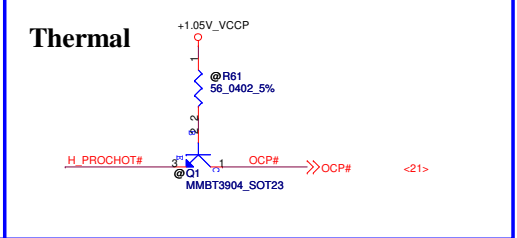
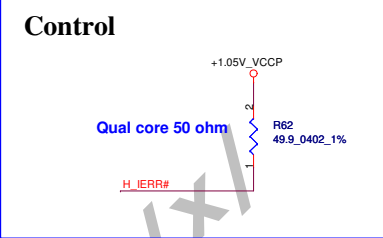
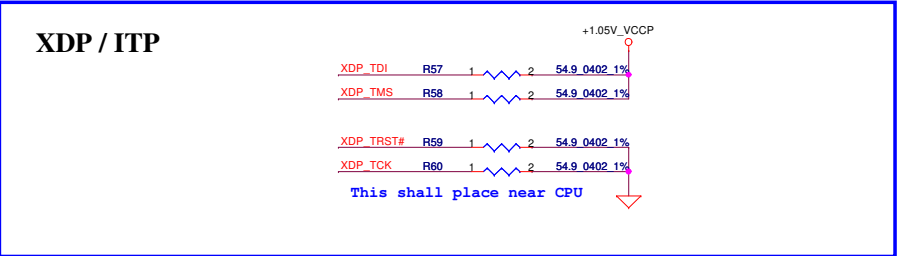
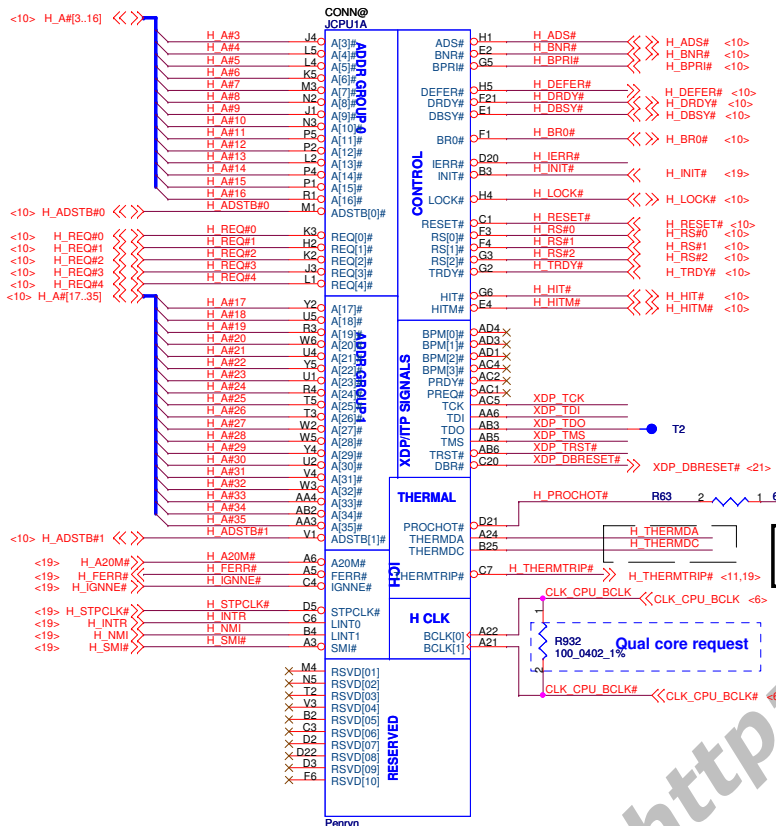


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Compal Electronics, Inc.		
Clock Generator CK505		
LA-5152P		
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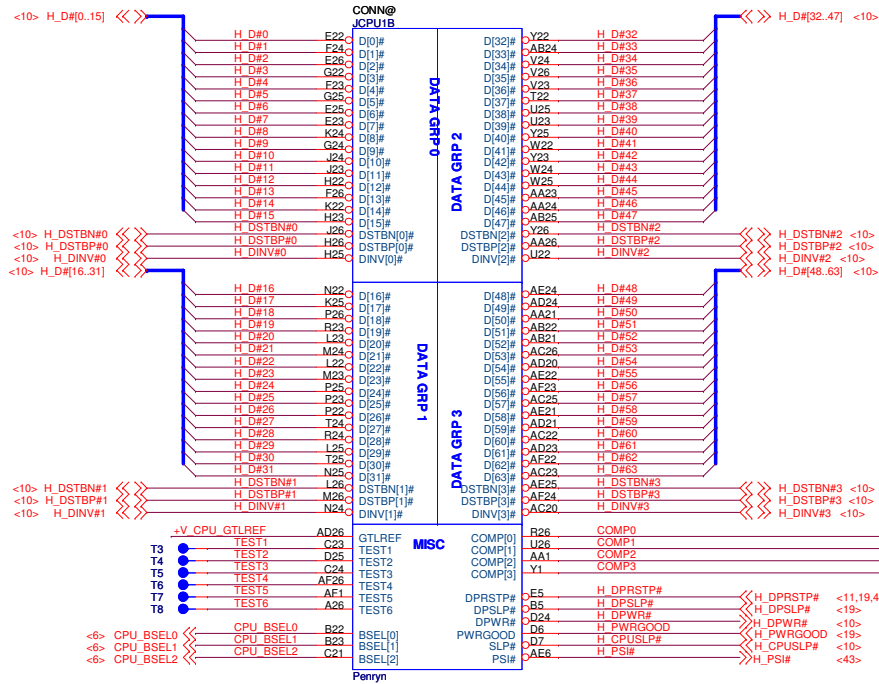
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

Qual core request

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Penryn(1/3)-AGTL+/ITP-XDP			
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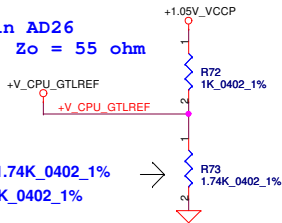
layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

Qual core value

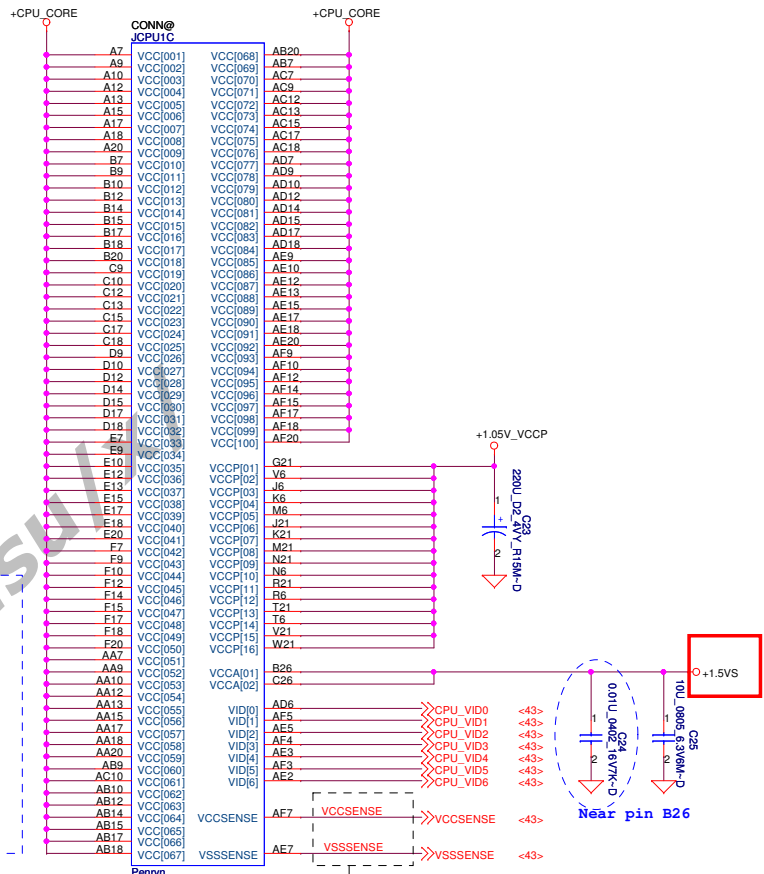
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Close to CPU pin AD26 within 500mils. $Z_o = 55 \text{ ohm}$

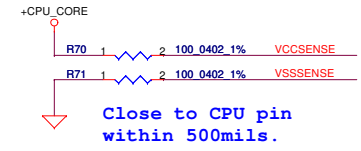


Cpu Quad Core, $R=1.74K_{0402_1\%}$

Cpu Dual Core, $R=2K_{0402_1\%}$



For 8 layer condition.
Length match within 25 mils.
The trace width/space/other is 20/7/25. $Z_o = 27.4 \text{ ohm}$.



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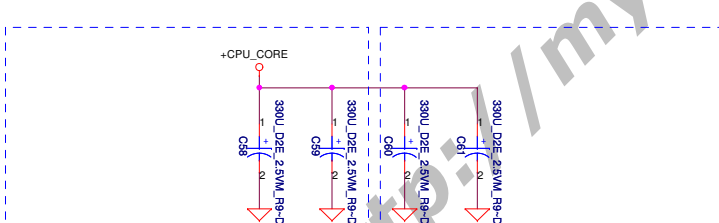
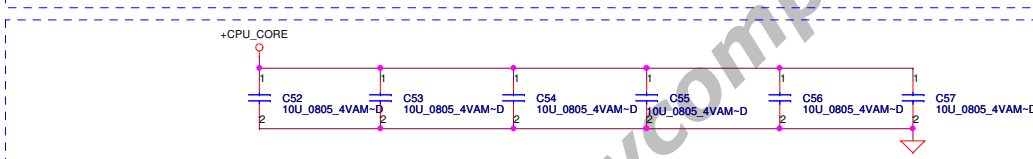
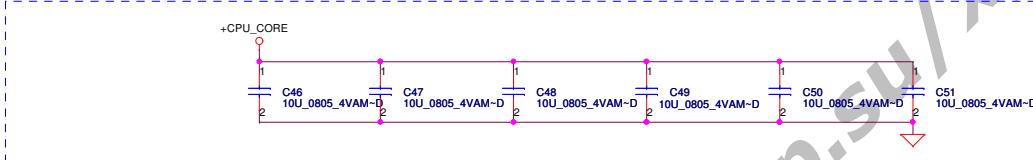
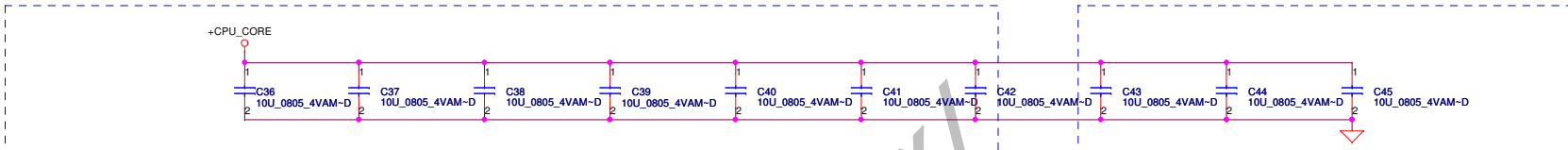
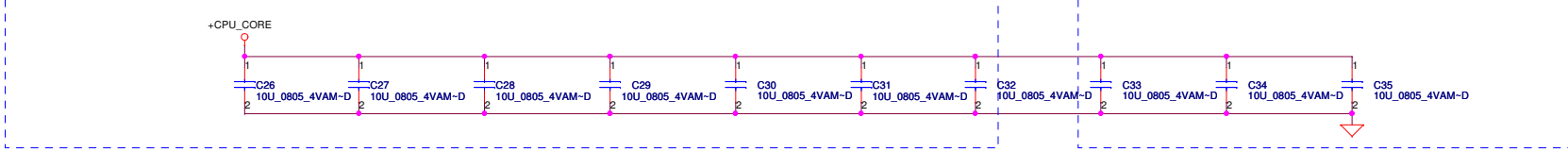


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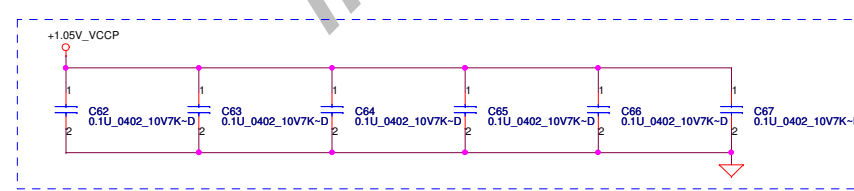
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High Frequency Decoupling
10uF 0805 X5R -> 85 degree.

CONN#	JCPU1D	VSS	P6
A4	VSS 001	VSS 082	P6
A8	VSS 002	VSS 083	P21
A11	VSS 003	VSS 084	P24
A14	VSS 004	VSS 085	R2
A16	VSS 005	VSS 086	R5
A19	VSS 006	VSS 087	R22
A23	VSS 007	VSS 088	R25
AF2	VSS 008	VSS 089	T1
BF	VSS 009	VSS 090	T4
B8	VSS 010	VSS 091	T23
B11	VSS 011	VSS 092	T26
B13	VSS 012	VSS 093	U3
B16	VSS 013	VSS 094	U6
B19	VSS 014	VSS 095	U21
B21	VSS 015	VSS 096	U24
B24	VSS 016	VSS 097	V2
C3	VSS 017	VSS 098	V5
C8	VSS 018	VSS 099	V22
C11	VSS 019	VSS 100	V25
C14	VSS 020	VSS 101	W1
C16	VSS 021	VSS 102	W4
C19	VSS 022	VSS 103	W23
C2	VSS 023	VSS 104	W26
C22	VSS 024	VSS 105	Y3
C25	VSS 025	VSS 106	Y6
D1	VSS 026	VSS 107	Y21
D4	VSS 027	VSS 108	Y24
D8	VSS 028	VSS 109	AA2
D11	VSS 029	VSS 110	AA5
D13	VSS 030	VSS 111	AA8
D16	VSS 031	VSS 112	AA11
D19	VSS 032	VSS 113	AA14
D23	VSS 033	VSS 114	AA16
D26	VSS 034	VSS 115	AA19
E3	VSS 035	VSS 116	AA22
E6	VSS 036	VSS 117	AA25
F8	VSS 037	VSS 118	AB1
F11	VSS 038	VSS 119	AB4
F14	VSS 039	VSS 120	AB8
F16	VSS 040	VSS 121	AB11
F19	VSS 041	VSS 122	AB13
E21	VSS 042	VSS 123	AB16
E24	VSS 043	VSS 124	AB19
F5	VSS 044	VSS 125	AB22
F8	VSS 045	VSS 126	AB26
F11	VSS 046	VSS 127	AC3
F13	VSS 047	VSS 128	AC6
F16	VSS 048	VSS 129	AC8
F19	VSS 049	VSS 130	AC11
F2	VSS 050	VSS 131	AC14
F22	VSS 051	VSS 132	AC16
F25	VSS 052	VSS 133	AC19
G4	VSS 053	VSS 134	AC21
G1	VSS 054	VSS 135	AC24
G26	VSS 055	VSS 136	AD2
H3	VSS 056	VSS 137	AD5
H6	VSS 057	VSS 138	AD8
H21	VSS 058	VSS 139	AD11
H24	VSS 059	VSS 140	AD13
J2	VSS 060	VSS 141	AD16
J5	VSS 061	VSS 142	AD19
J22	VSS 062	VSS 143	AD22
J25	VSS 063	VSS 144	AD25
K1	VSS 064	VSS 145	AE1
K4	VSS 065	VSS 146	AE4
K23	VSS 066	VSS 147	AE8
K26	VSS 067	VSS 148	AE11
L3	VSS 068	VSS 149	AE14
L6	VSS 069	VSS 150	AE16
L21	VSS 070	VSS 151	AE19
L24	VSS 071	VSS 152	AE23
L26	VSS 072	VSS 153	AE26
M2	VSS 073	VSS 154	A2
M5	VSS 074	VSS 155	AF6
M22	VSS 075	VSS 156	AF8
M25	VSS 076	VSS 157	AF11
N1	VSS 077	VSS 158	AF13
N4	VSS 078	VSS 159	AF16
N23	VSS 079	VSS 160	AF19
N26	VSS 080	VSS 161	AF21
P3	VSS 081	VSS 162	A25
		VSS 163	AF25



ESR <= 1.5m ohm
Capacitor > 880 uF

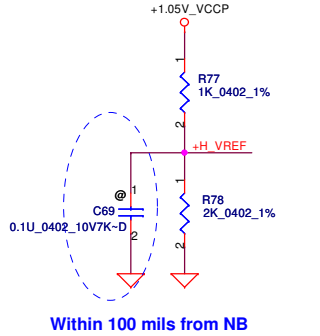
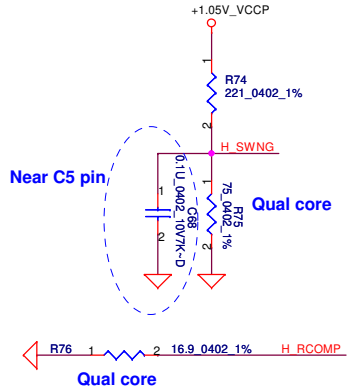


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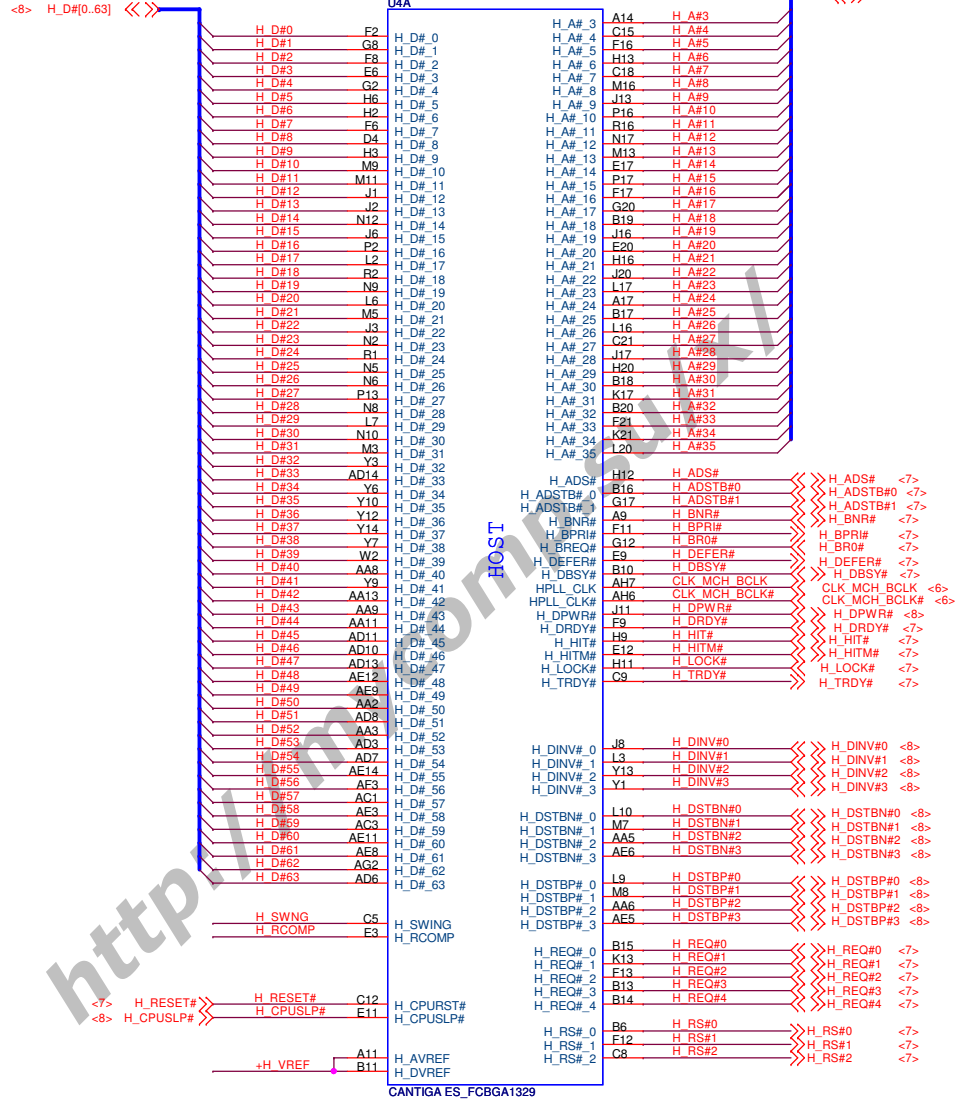
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Penryn(3/3)-AGTL+/ITP-XDP		
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Layout Note :
H_RCOMP / H_VREF / H_SWNG
 Trace width and spacing is 10 / 20



H_RCOMP Dual core 24.9 ohm_1% pull down
Qual core 16.9 ohm_1% pull down
H_SWNG Dual core 100 ohm_1% pull down
Qual core 75 ohm_1% pull down

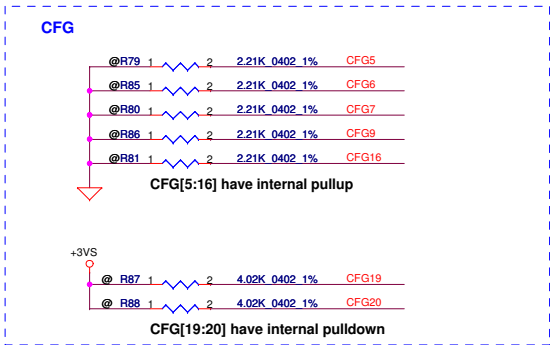


CANTIGA ES_FCBGA1329

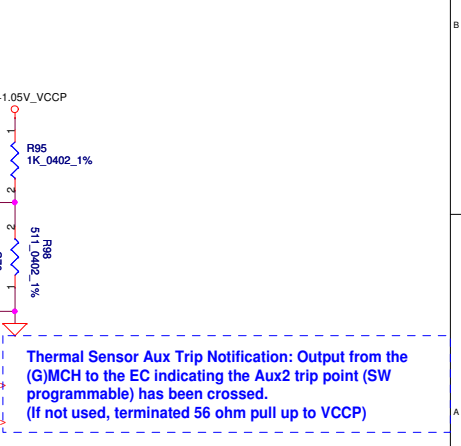
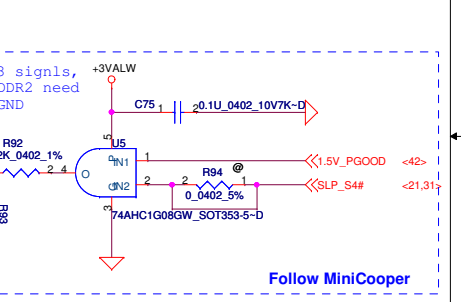
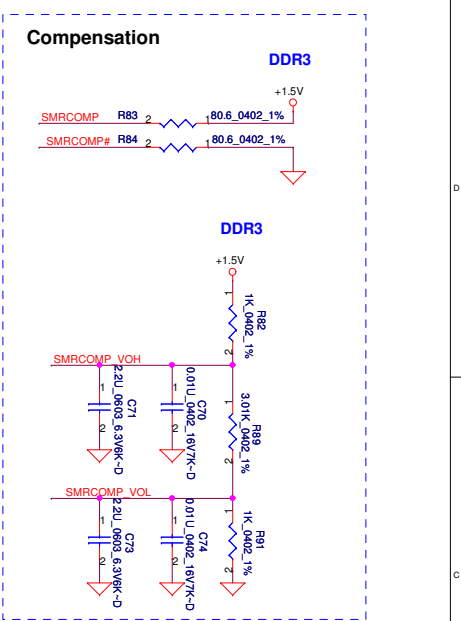
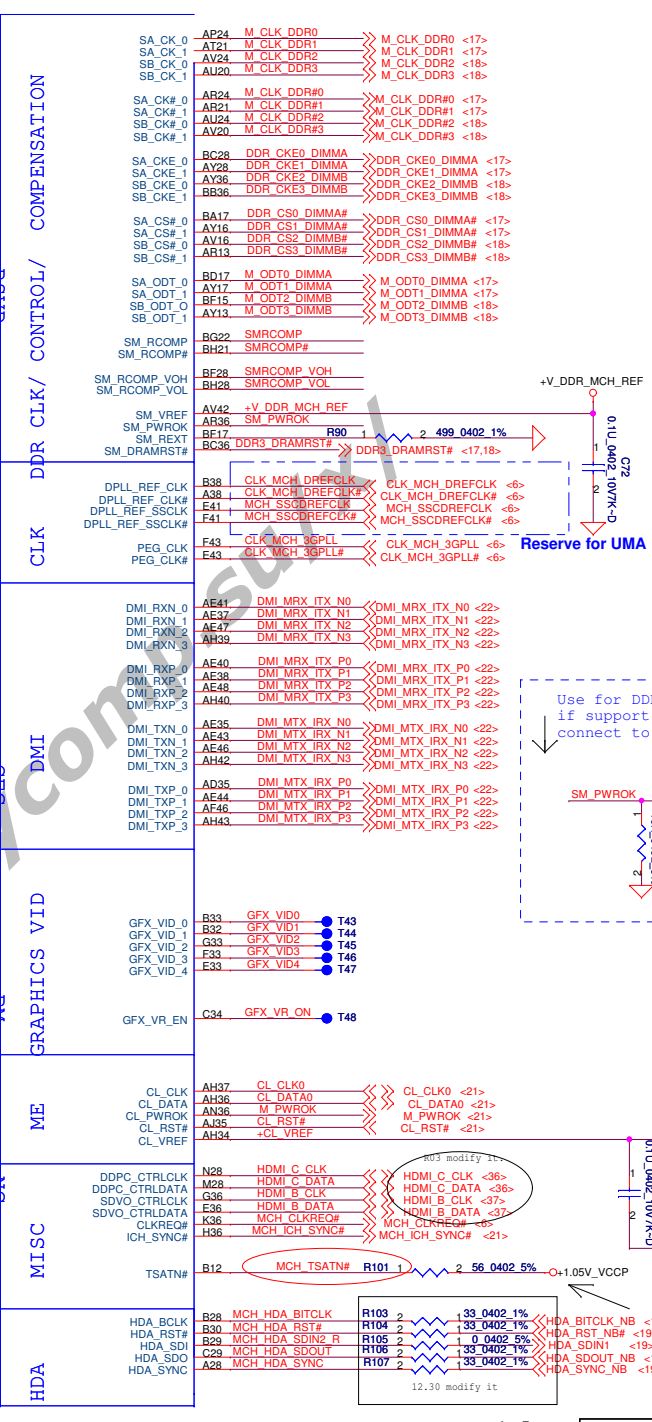
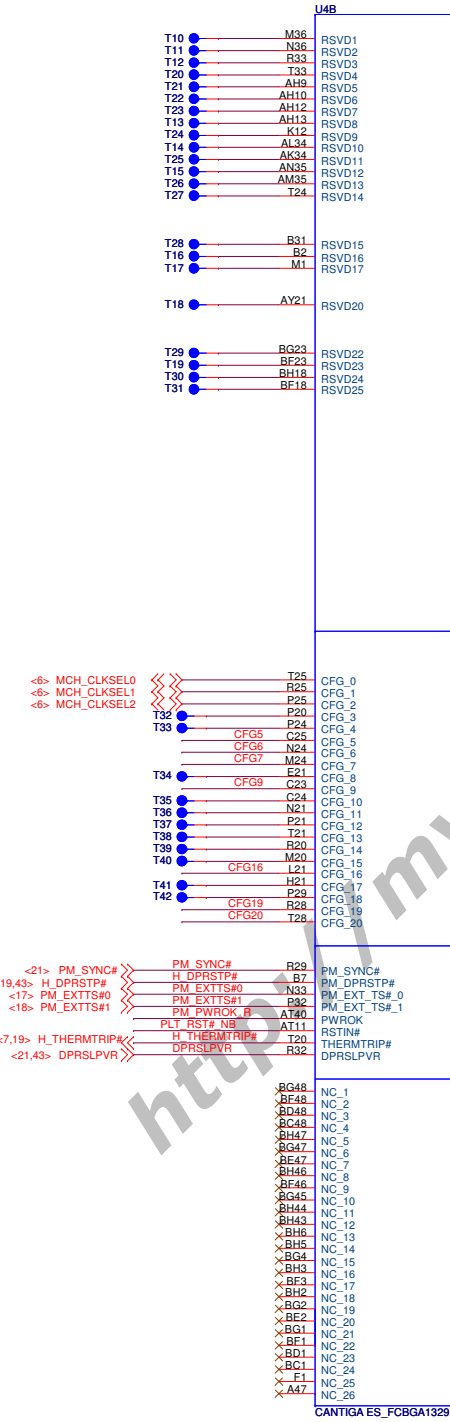
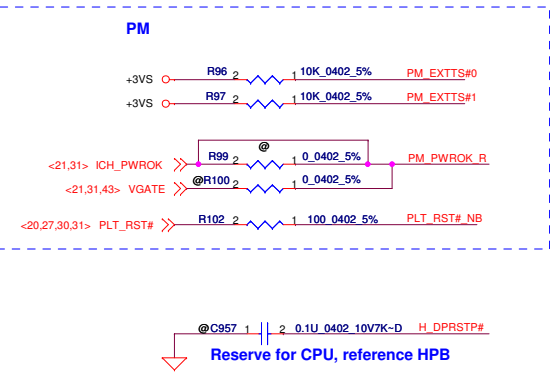
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Strap Pin Table		
CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	ITPM Host Interface	Low = ITPM enable High = ITPM disable(Default)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	Digital Display Port Concurrent Operation	Low=Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present



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Cantiga(2 of 7)

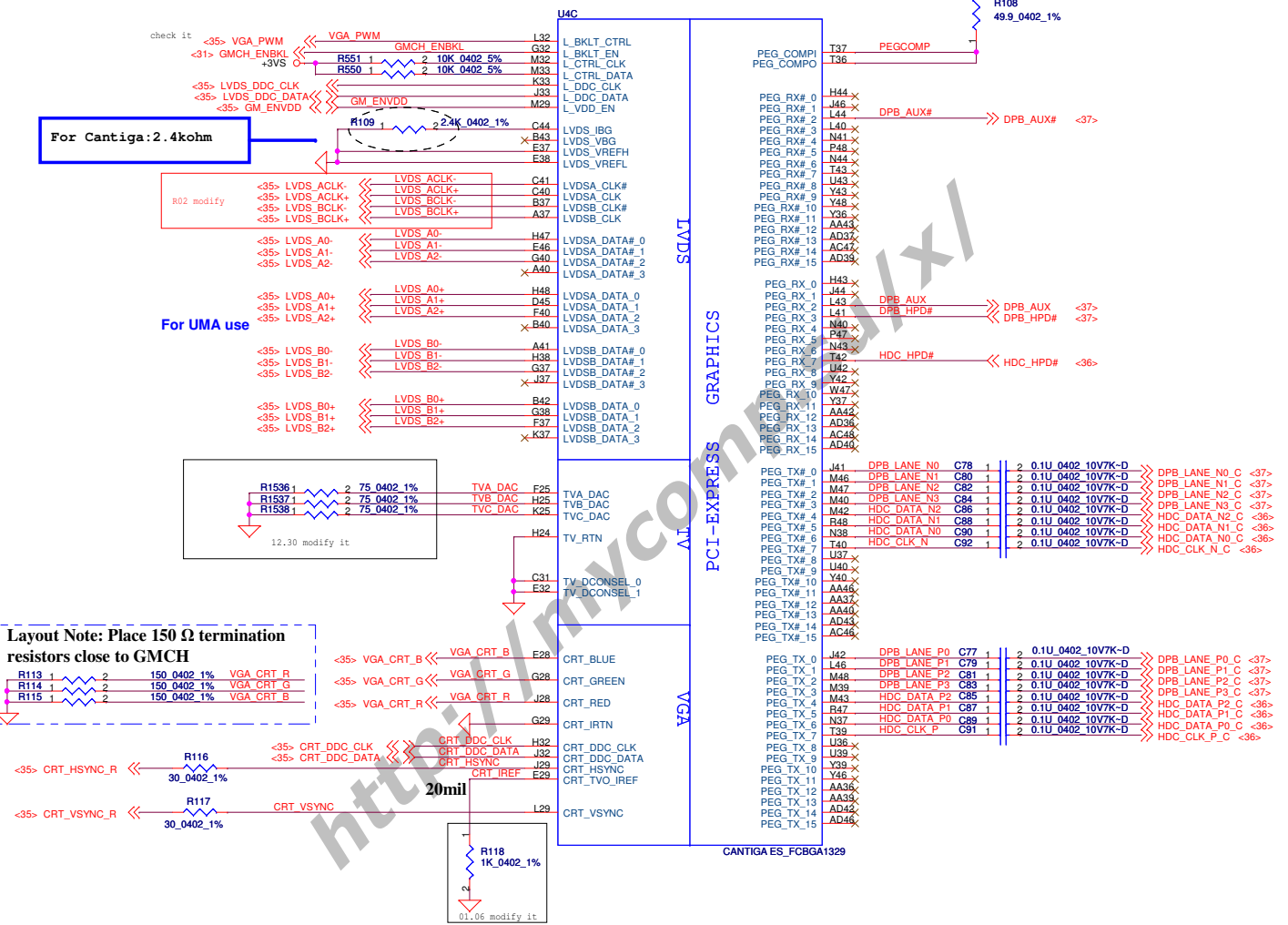
LA-5152P

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Note: All LVDS data signals/and it's compliments should be routed Differentially

Place the resistor within 500mils of the GMCH PEGCOMP trace width and spacing is 20/25 mils.



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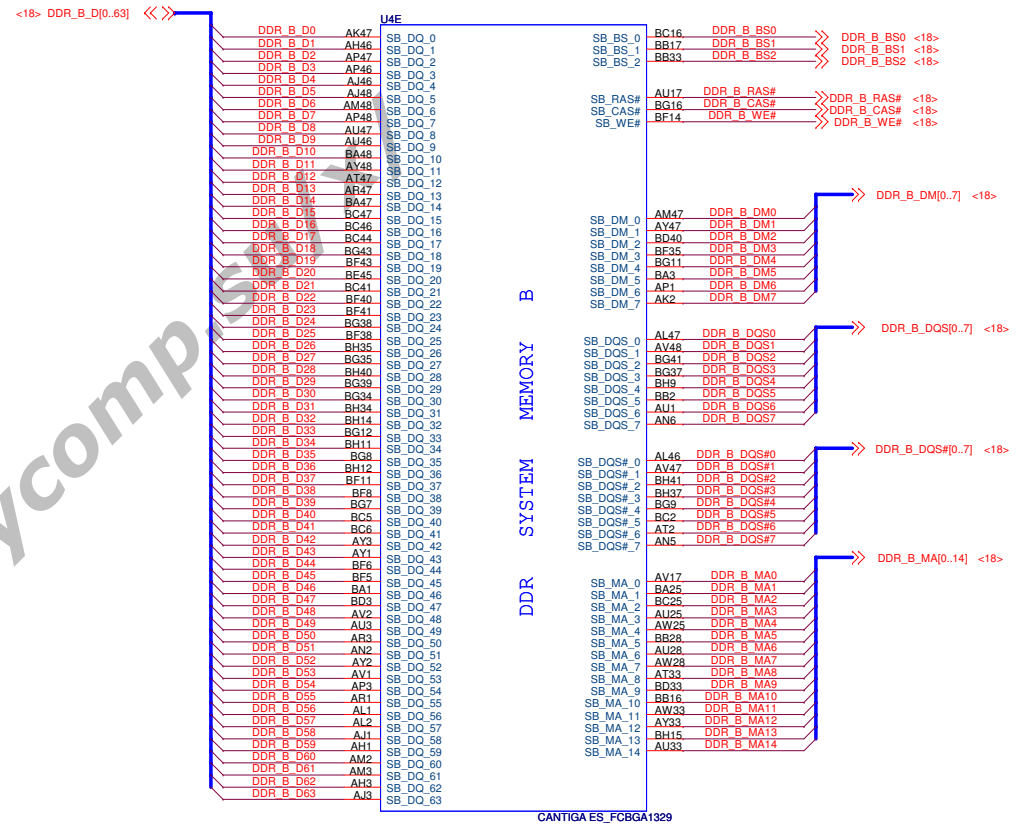
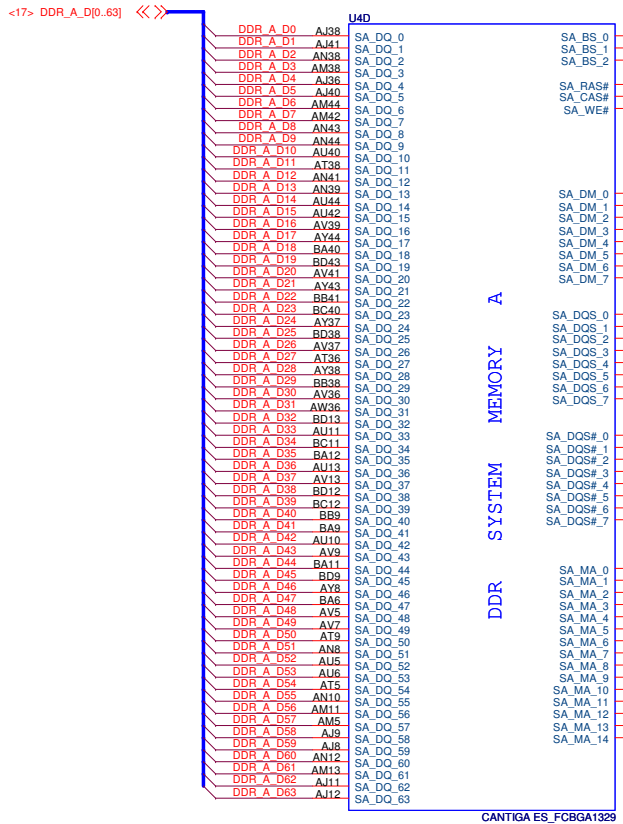
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Title Cantiga(3 of 7)

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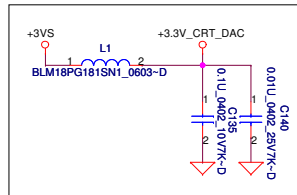
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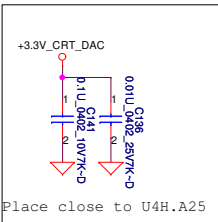
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Date	Monday, June 15, 2009	Sheet	13 of 51

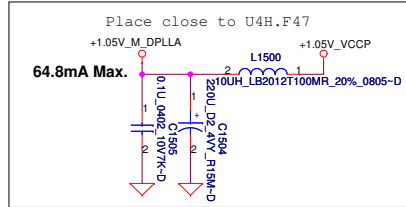
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Place close to U4H.B27 and A26

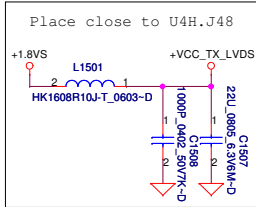


Place close to U4H.A25

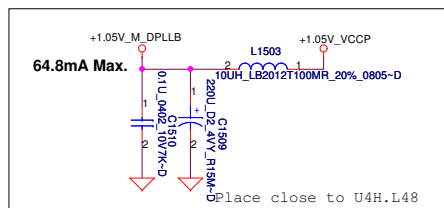


Place close to U4H.F47

64.8mA Max.

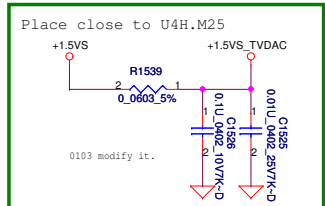


Place close to U4H.J48



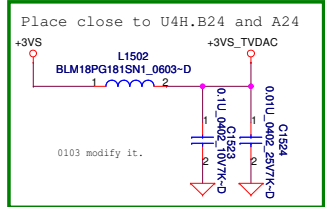
64.8mA Max.

Place close to U4H.L48



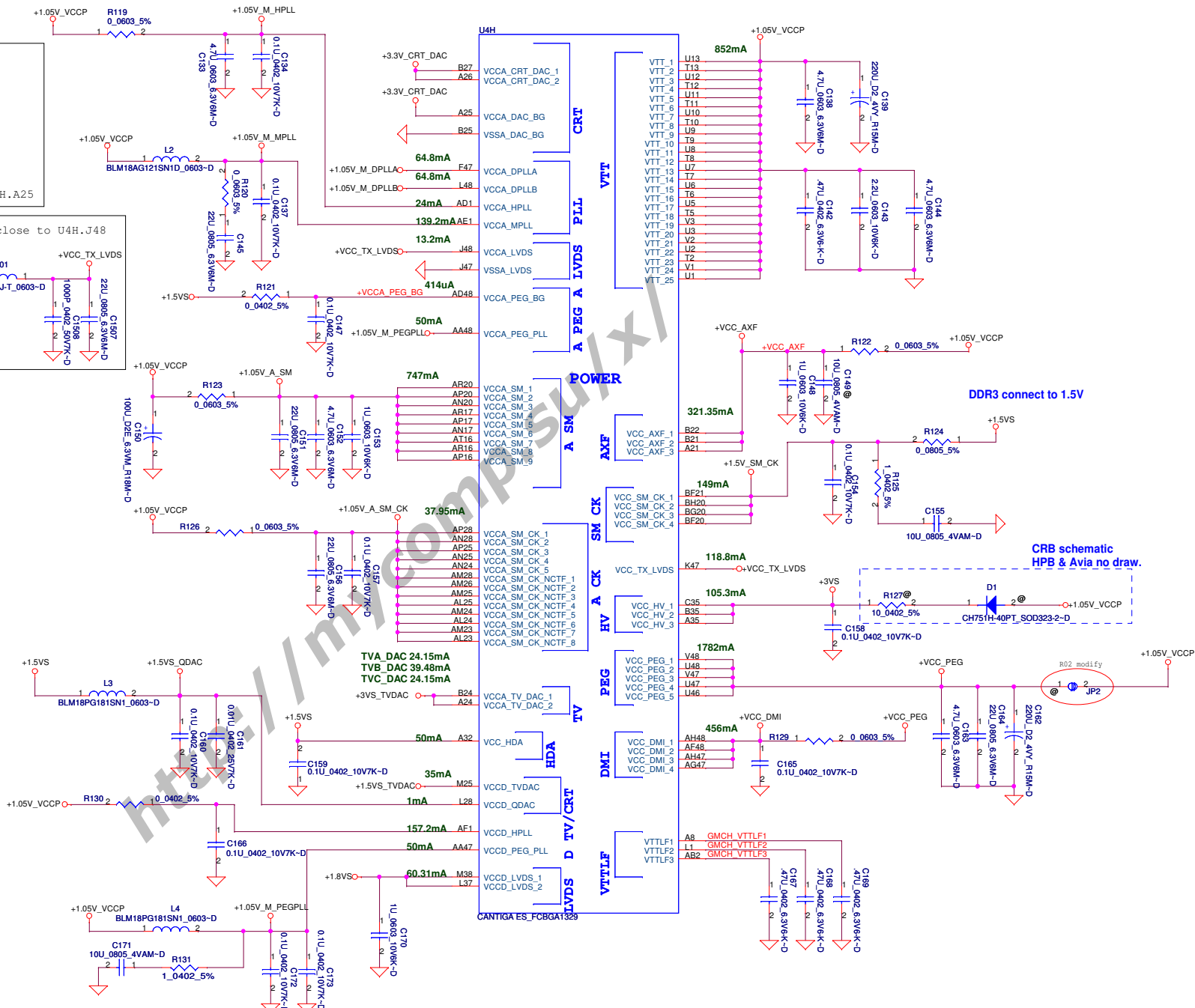
Place close to U4H.M25

0103 modify it.



Place close to U4H.B24 and A24

0103 modify it.



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		Compal Electronics, Inc.	
		Cantiga(6 of 7)	
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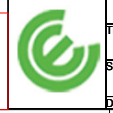
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ALJ48	VSS_1	VSS_100	AM36	AE36	
AR48	VSS_2	VSS_101	AE36	P36	
AL48	VSS_3	VSS_102	P36	L36	
BB47	VSS_4	VSS_103	L36	AP21	
AW47	VSS_5	VSS_104	AP21	F36	
AN47	VSS_6	VSS_105	F36	B36	
AJ47	VSS_7	VSS_106	B36	AH35	
AF47	VSS_8	VSS_107	AH35	AA35	
AD47	VSS_9	VSS_108	AA35	Y35	
AB47	VSS_10	VSS_109	Y35	U35	
Y47	VSS_11	VSS_110	U35	T35	
T47	VSS_12	VSS_111	T35	BF34	
N47	VSS_13	VSS_112	BF34	AM34	
L47	VSS_14	VSS_113	AM34	AJ34	
G47	VSS_15	VSS_114	AJ34	AF34	
BD46	VSS_16	VSS_115	AF34	AE34	
BA46	VSS_17	VSS_116	AE34	W34	
AV46	VSS_18	VSS_117	W34	B34	
AR46	VSS_19	VSS_118	B34	A34	
AM46	VSS_20	VSS_119	A34	BC33	
V46	VSS_21	VSS_120	BC33	BA33	
R46	VSS_22	VSS_121	BA33	AV33	
P46	VSS_24	VSS_122	AV33	AR33	
H46	VSS_25	VSS_124	AR33	AL33	
F46	VSS_26	VSS_125	AL33	AH33	
BF44	VSS_27	VSS_126	AH33	AB33	
AH44	VSS_28	VSS_127	AB33	P33	
AD44	VSS_29	VSS_128	P33	L33	
AA44	VSS_30	VSS_129	L33	H33	
Y44	VSS_31	VSS_130	H33	N32	
U44	VSS_32	VSS_131	N32	K32	
T44	VSS_33	VSS_132	K32	J32	
M44	VSS_34	VSS_133	J32	C32	
F44	VSS_35	VSS_134	C32	A31	
BC43	VSS_35	VSS_135	A31	AN29	
AV43	VSS_36	VSS_136	AN29	T29	
AU43	VSS_37	VSS_137	T29	N29	
AM43	VSS_38	VSS_138	N29	K29	
J43	VSS_39	VSS_139	K29	H29	
H43	VSS_40	VSS_140	H29	T29	
CG42	VSS_41	VSS_141	T29	A29	
AV42	VSS_42	VSS_142	A29	BG28	
AT42	VSS_43	VSS_143	BG28	BD28	
AN42	VSS_44	VSS_144	BD28	BA28	
AJ42	VSS_45	VSS_145	BA28	AV28	
AE42	VSS_46	VSS_146	AV28	AT28	
N42	VSS_47	VSS_147	AT28	AR28	
L42	VSS_48	VSS_148	AR28	AJ28	
BD41	VSS_49	VSS_149	AJ28	AG28	
AU41	VSS_50	VSS_150	AG28	AE28	
AM41	VSS_51	VSS_151	AE28	AB28	
AH41	VSS_52	VSS_152	AB28	Y28	
AD41	VSS_53	VSS_153	Y28	T28	
AA41	VSS_54	VSS_154	T28	K28	
Y41	VSS_55	VSS_155	K28	H28	
U41	VSS_56	VSS_156	H28	F28	
T41	VSS_57	VSS_157	F28	C28	
M41	VSS_58	VSS_158	C28	BF26	
G41	VSS_59	VSS_159	BF26	AH26	
B41	VSS_60	VSS_160	AH26	AF26	
BG40	VSS_61	VSS_161	AF26	AB26	
BB40	VSS_62	VSS_162	AB26	AA26	
AV40	VSS_63	VSS_163	AA26	C26	
AN40	VSS_64	VSS_164	C26	B26	
H40	VSS_65	VSS_165	B26	BH25	
F40	VSS_66	VSS_166	BH25	BD25	
AT39	VSS_67	VSS_167	BD25	AV25	
AM39	VSS_68	VSS_168	AV25	AR25	
AJ39	VSS_69	VSS_169	AR25	AJ25	
AE39	VSS_70	VSS_170	AJ25	AC25	
V39	VSS_71	VSS_171	AC25	Y25	
R39	VSS_72	VSS_172	Y25	N25	
B39	VSS_73	VSS_173	N25	J25	
BH38	VSS_74	VSS_174	J25	G25	
BC38	VSS_75	VSS_175	G25	E25	
BA38	VSS_76	VSS_176	E25	BF24	
AU38	VSS_77	VSS_177	BF24	AD24	
AH38	VSS_78	VSS_178	AD24	AY24	
AD38	VSS_79	VSS_179	AY24	AT24	
AA38	VSS_80	VSS_180	AT24	AJ24	
Y38	VSS_81	VSS_181	AJ24	AH24	
U38	VSS_82	VSS_182	AH24	AF24	
T38	VSS_83	VSS_183	AF24	AB24	
J38	VSS_84	VSS_184	AB24	B24	
F38	VSS_85	VSS_185	B24	L24	
C38	VSS_86	VSS_186	L24	K24	
C38	VSS_87	VSS_187	K24	J24	
BF37	VSS_88	VSS_188	J24	G24	
BS37	VSS_89	VSS_189	G24	Q24	
AW37	VSS_90	VSS_190	Q24	B9	
AT37	VSS_91	VSS_191	B9	BH8	
AJ37	VSS_92	VSS_192	BH8	BB8	
H37	VSS_93	VSS_193	BB8	AV8	
C37	VSS_94	VSS_194	AV8	B23	
BC36	VSS_95	VSS_195	B23	A23	
BD36	VSS_96	VSS_196	A23	A16	
AK15	VSS_97	VSS_197	A16		
AU36	VSS_98	VSS_198			
	VSS_99	VSS_199			

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U4J		VSS		AH8	
BG21	VSS_199	VSS_297	AH8	Y8	
L12	VSS_200	VSS_298	Y8	L8	
AW21	VSS_201	VSS_299	L8	E8	
AU21	VSS_202	VSS_300	E8	B8	
AP21	VSS_203	VSS_301	B8	AY7	
AN21	VSS_204	VSS_302	AY7	AU7	
AH21	VSS_205	VSS_303	AU7	AN7	
AF21	VSS_206	VSS_304	AN7	AJ7	
AB21	VSS_207	VSS_305	AJ7	AE7	
R21	VSS_208	VSS_306	AE7	AA7	
M21	VSS_209	VSS_307	AA7	N7	
J21	VSS_210	VSS_308	N7	J7	
C21	VSS_211	VSS_309	J7	BG6	
BC20	VSS_212	VSS_310	BG6	BD6	
BA20	VSS_213	VSS_311	BD6	AV6	
AW20	VSS_214	VSS_312	AV6	AT6	
AT20	VSS_215	VSS_313	AT6	AM6	
AU20	VSS_216	VSS_314	AM6	M6	
AG20	VSS_217	VSS_315	M6	C6	
Y20	VSS_218	VSS_316	C6	BA5	
M20	VSS_219	VSS_317	BA5	AH5	
K20	VSS_220	VSS_318	AH5	AD5	
F20	VSS_221	VSS_319	AD5	Y5	
C20	VSS_222	VSS_320	Y5	L5	
A20	VSS_223	VSS_321	L5	J5	
BG19	VSS_224	VSS_322	J5	H5	
A18	VSS_225	VSS_323	H5	F5	
BG17	VSS_226	VSS_324	F5	BE4	
BC17	VSS_227	VSS_325	BE4		
AW17	VSS_228				
AT17	VSS_229	VSS_327	BC3		
R17	VSS_230	VSS_328	AV3		
M17	VSS_231	VSS_329	AL3		
H17	VSS_232	VSS_330	R3		
C17	VSS_233	VSS_331	P3		
		VSS_332	F3		
BA16	VSS_235	VSS_333	BA2		
		VSS_334	AW2		
AU16	VSS_237	VSS_335	VSS_335		
AN16	VSS_238	VSS_336	AR2		
N16	VSS_239	VSS_337	AP2		
K16	VSS_240	VSS_338	AJ2		
E16	VSS_241	VSS_339	AH2		
BG15	VSS_242	VSS_340	AF2		
AC15	VSS_243	VSS_341	AE2		
A15	VSS_244	VSS_342	AD2		
BG14	VSS_245	VSS_343	AC2		
A14	VSS_246	VSS_344	Y2		
C14	VSS_247	VSS_345	M2		
AG14	VSS_248	VSS_346	K2		
C14	VSS_249	VSS_347	VSS_347		
BG13	VSS_250	VSS_348	AM1		
BC13	VSS_251	VSS_349	P1		
BA13	VSS_252	VSS_350	H1		
		VSS_351	U24		
AN13	VSS_255	VSS_352	U28		
AJ13	VSS_256	VSS_353	U25		
AE13	VSS_257	VSS_354	U29		
N13	VSS_258				
L13	VSS_259	VSS_NCTF_1	AF32		
G13	VSS_260	VSS_NCTF_2	AB32		
E13	VSS_261	VSS_NCTF_3	V32		
BF12	VSS_262	VSS_NCTF_4	AJ30		
AV12	VSS_263	VSS_NCTF_5	AM29		
AT12	VSS_264	VSS_NCTF_6	AF29		
AM12	VSS_265	VSS_NCTF_7	AB29		
AJ12	VSS_266	VSS_NCTF_8	U28		
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BD11	VSS_268	VSS_NCTF_10	AL20		
BB11	VSS_269	VSS_NCTF_11	V20		
AY11	VSS_270	VSS_NCTF_12	AC19		
AN11	VSS_271	VSS_NCTF_13	AL17		
AH11	VSS_272	VSS_NCTF_14	AJ17		
		VSS_NCTF_15	AA17		
		VSS_NCTF_16	U17		
Y11	VSS_275				
N11	VSS_276				
G11	VSS_277				
C11	VSS_278				
BG10	VSS_279	VSS_SCB_1	BH48		
AV10	VSS_280	VSS_SCB_2	BH1		
AT10	VSS_281	VSS_SCB_3	A48		
AJ10	VSS_282	VSS_SCB_4	C1		
AE10	VSS_283	VSS_SCB_5	A3		
AA10	VSS_284				
M10	VSS_285				
BF9	VSS_286	NC_26	E1		
BC9	VSS_287	NC_27	D2		
AN9	VSS_288	NC_28	C3		
AM9	VSS_289	NC_29	B4		
AD9	VSS_290	NC_30	A5		
Q9	VSS_291	NC_31	A6		
B9	VSS_292	NC_32	A43		
BH8	VSS_293	NC_33	A44		
BB8	VSS_294	NC_34	B45		
AV8	VSS_295	NC_35	C46		
AT8	VSS_296	NC_36	D47		
		NC_37	B47		
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		NC_41	C48		
		NC_42	B48		

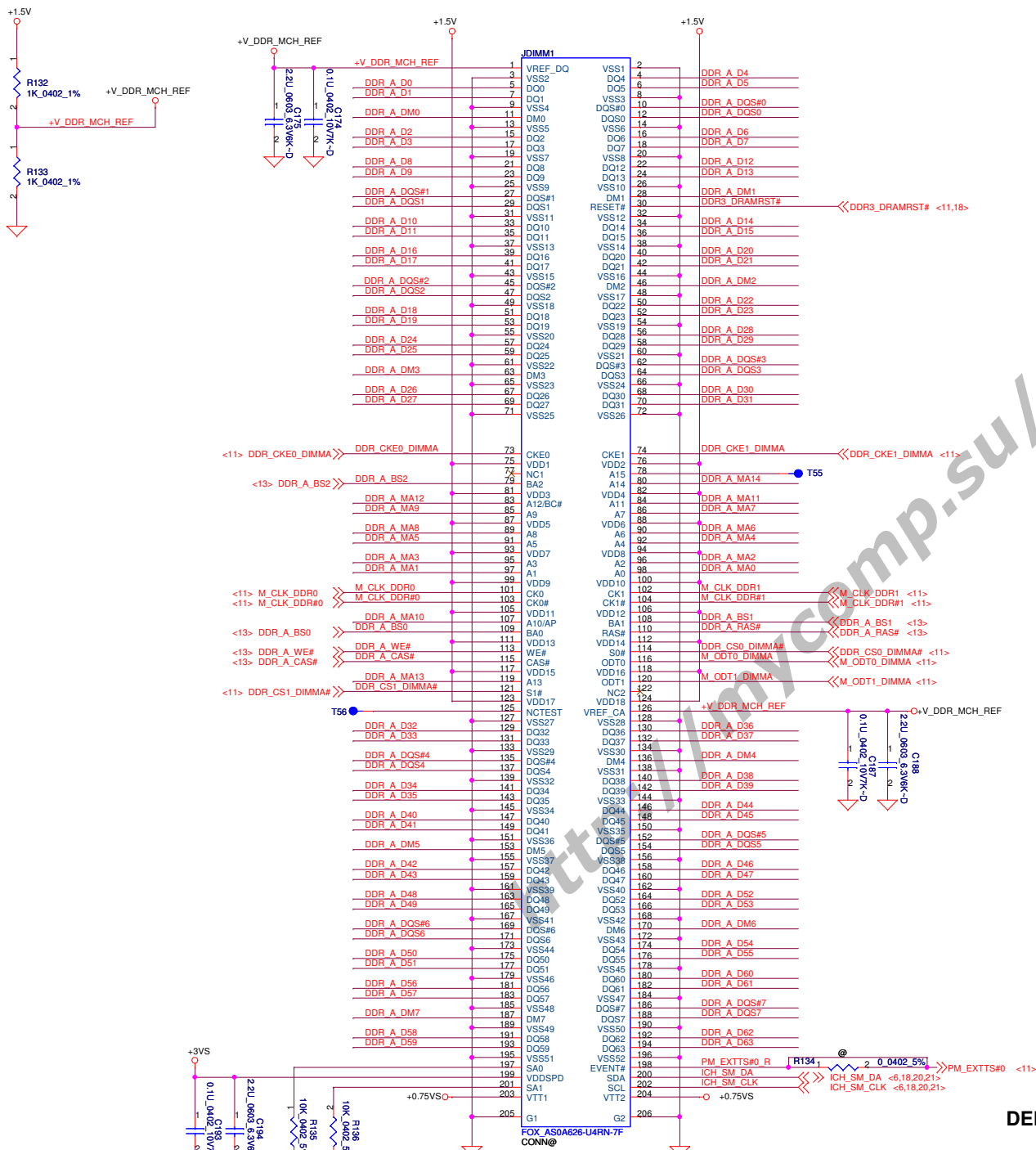
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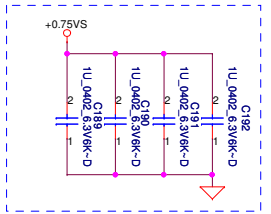
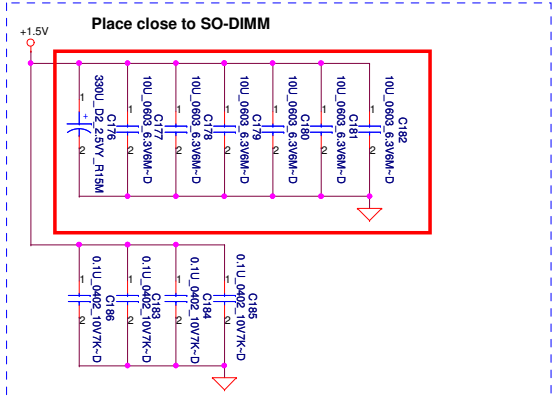
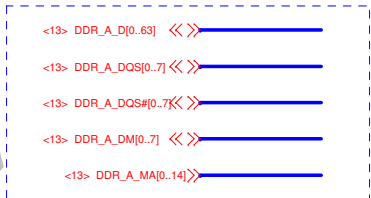


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Note :
 DDR3 command & control signals need no termination.
 DDR2 command & command signals 56 ohm pull up to VccSus0_9

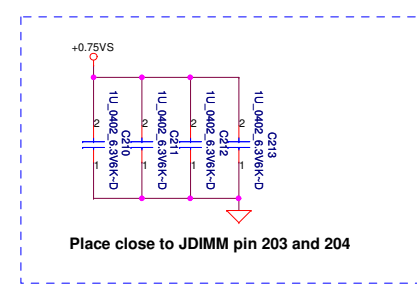
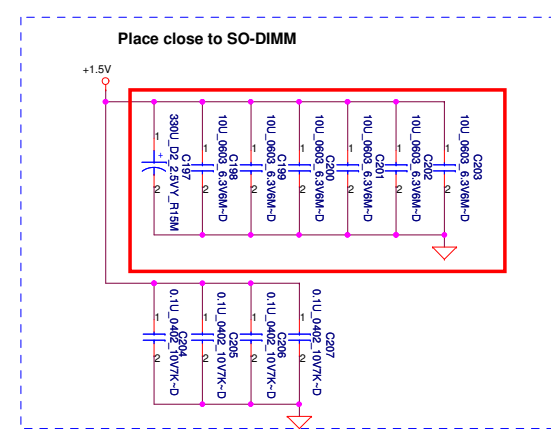
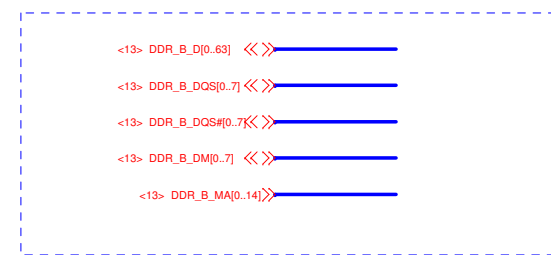
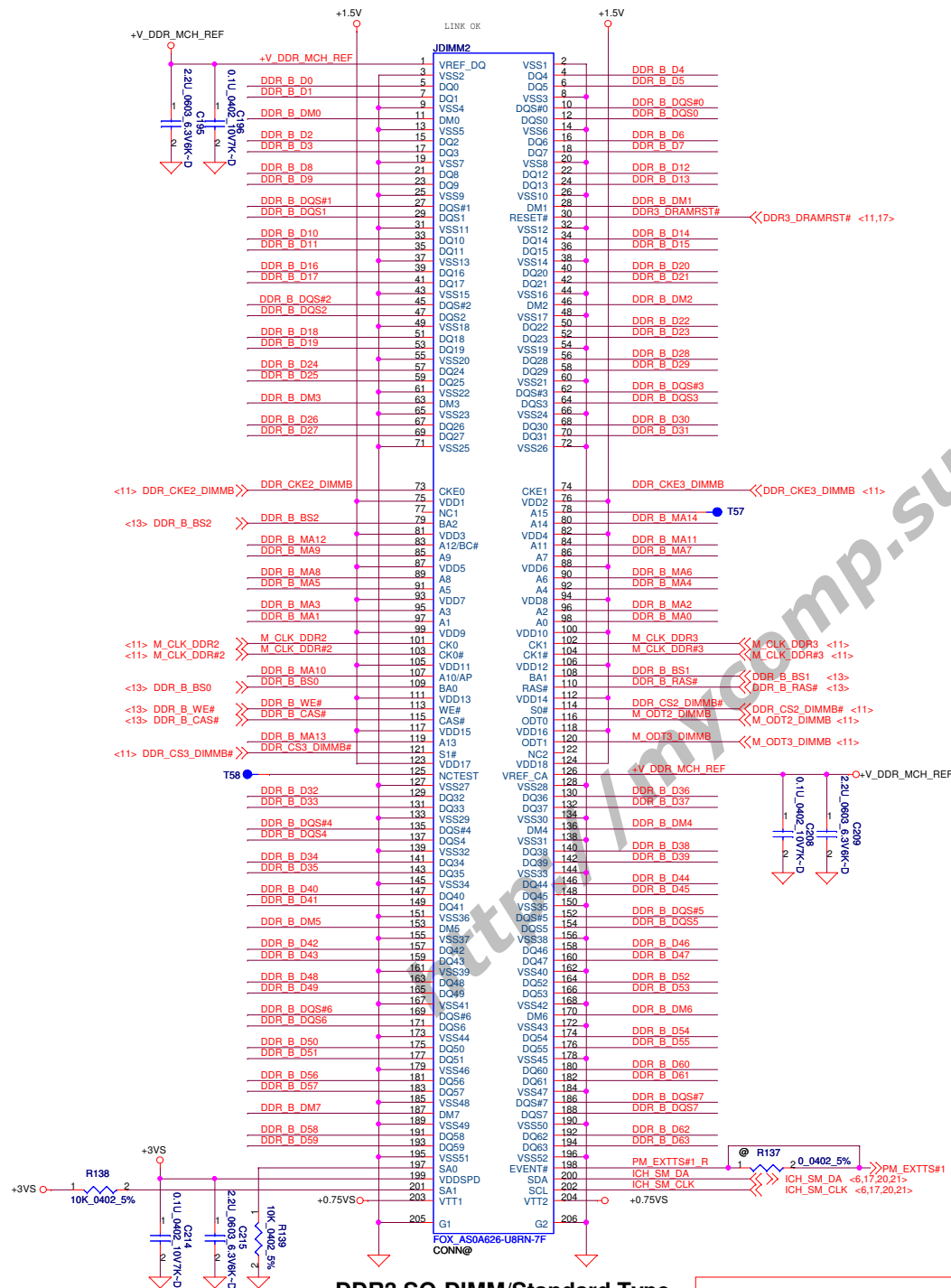


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DDR3 SO-DIMM/Standard Type

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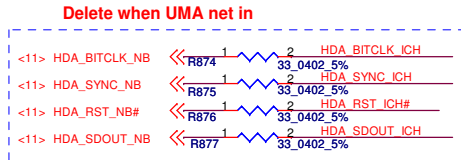
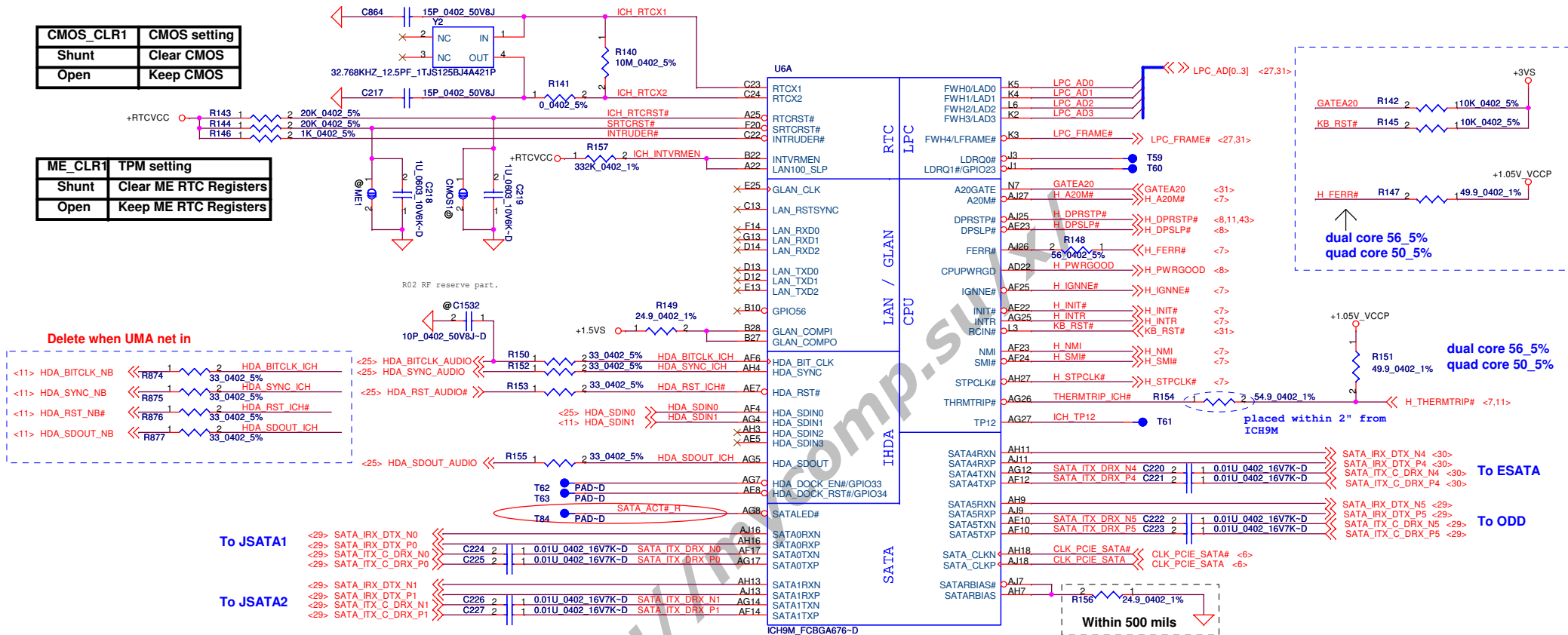
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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

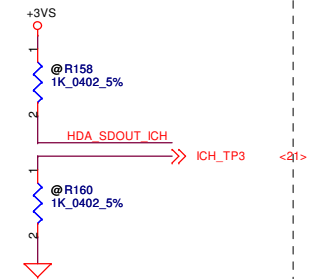


To JSATA1

To JSATA2

P/N : SA00002G12L (S IC AF82801IEM SLB8P A3 PBGA676P ICH9ME)

XOR Chain Entrance Strap		
ICH TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



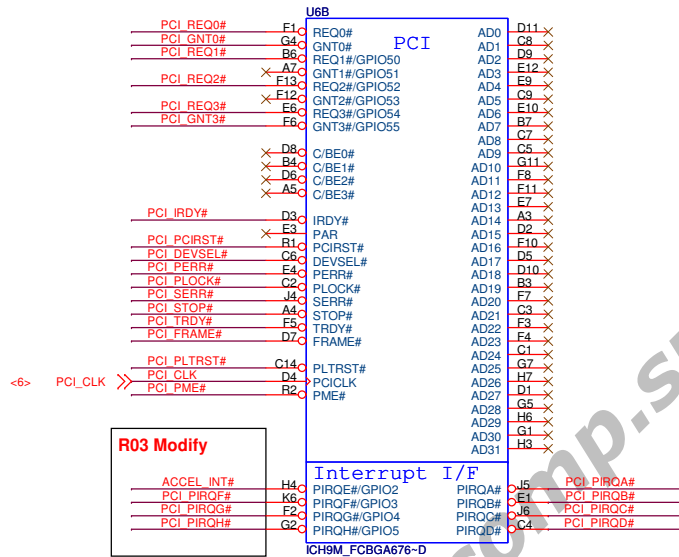
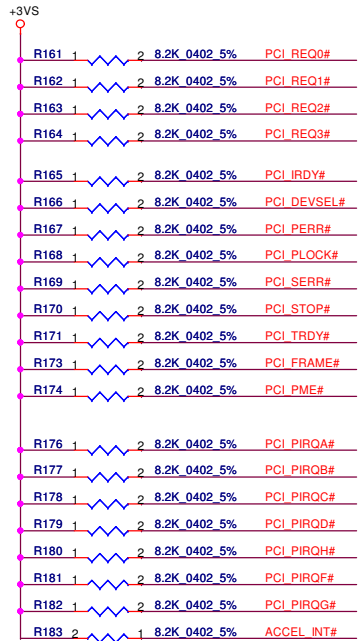
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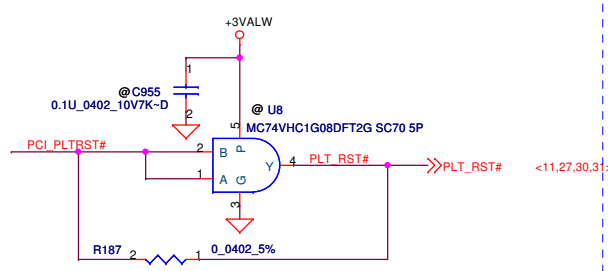
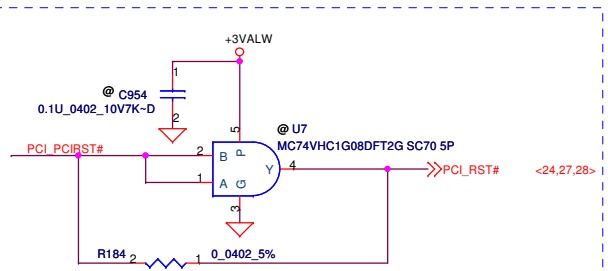
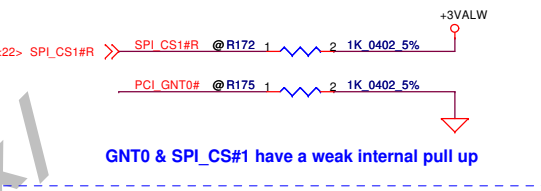
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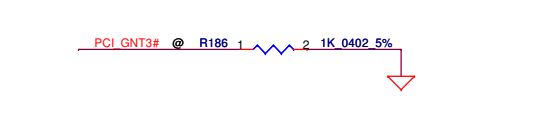




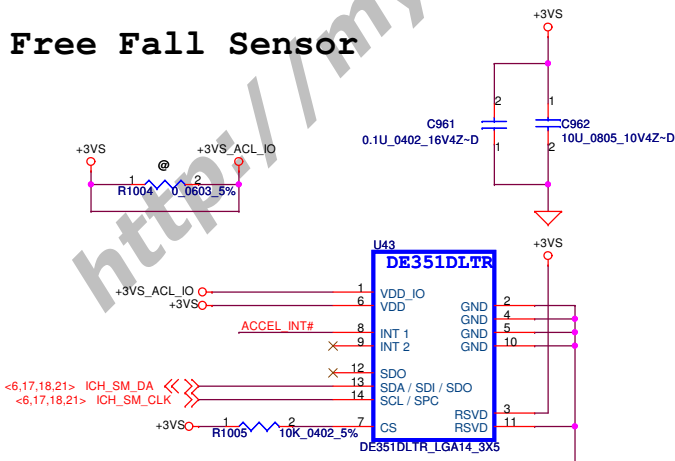
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *
1	1



Free Fall Sensor

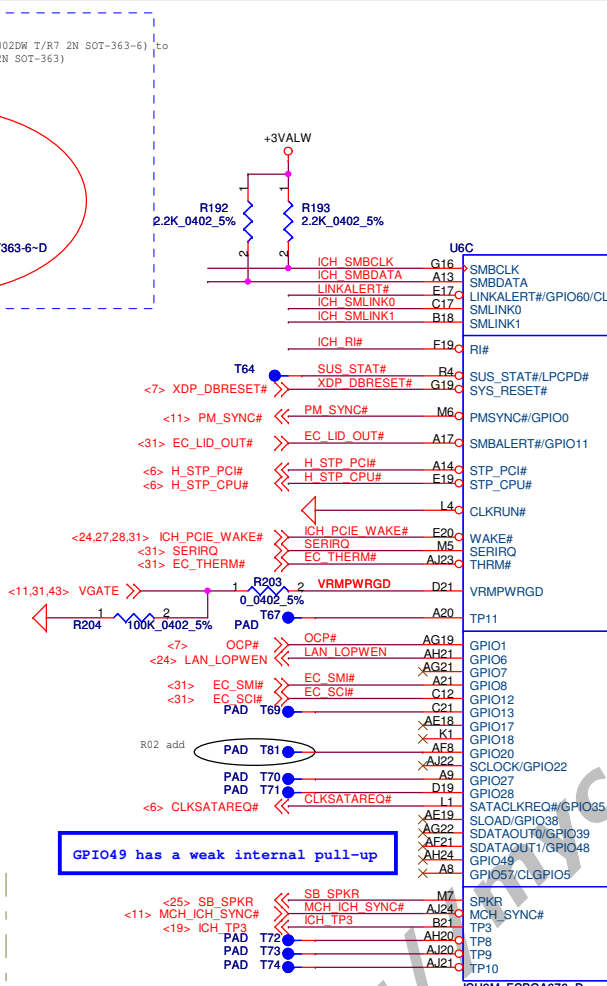
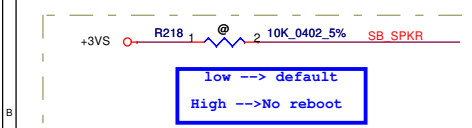
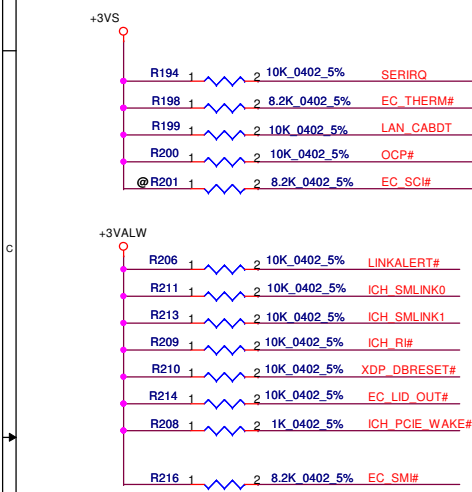
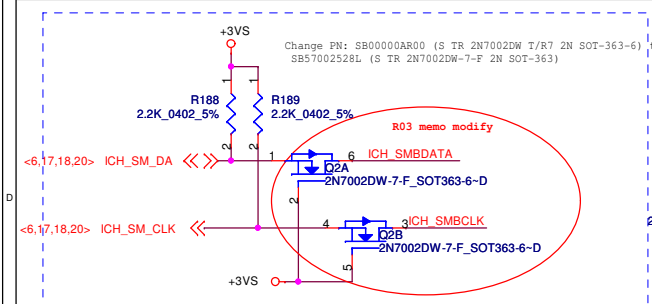


Must be placed in the center of the system.
 P/N : SA000039C00 (S IC DE351DLTR LGA 14P MOTION SENSOR)

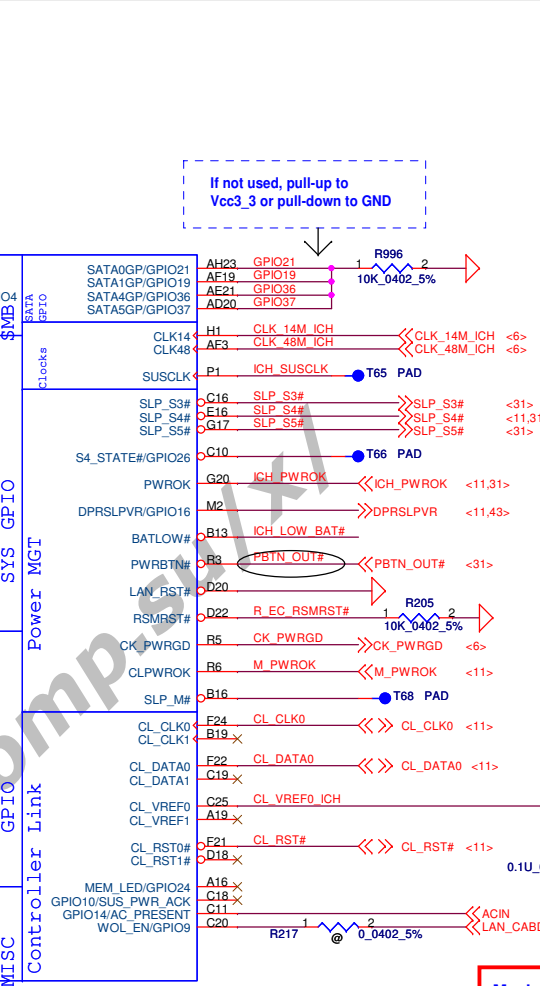
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		Compal Electronics, Inc.	
		ICH9-M(2/5)	
Title	Document Number LA-5152P	Date:	Monday, June 15, 2009
Size	Sheet 20 of 51	Rev	A00

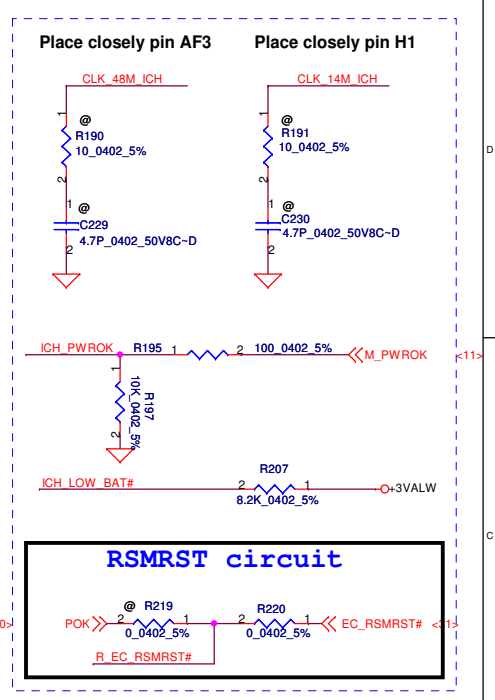
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GPIO49 has a weak internal pull-up



If not used, pull-up to Vcc3_3 or pull-down to GND



Maybach CL_CLK1/DATA1 connect to WLAN card to support iAMT

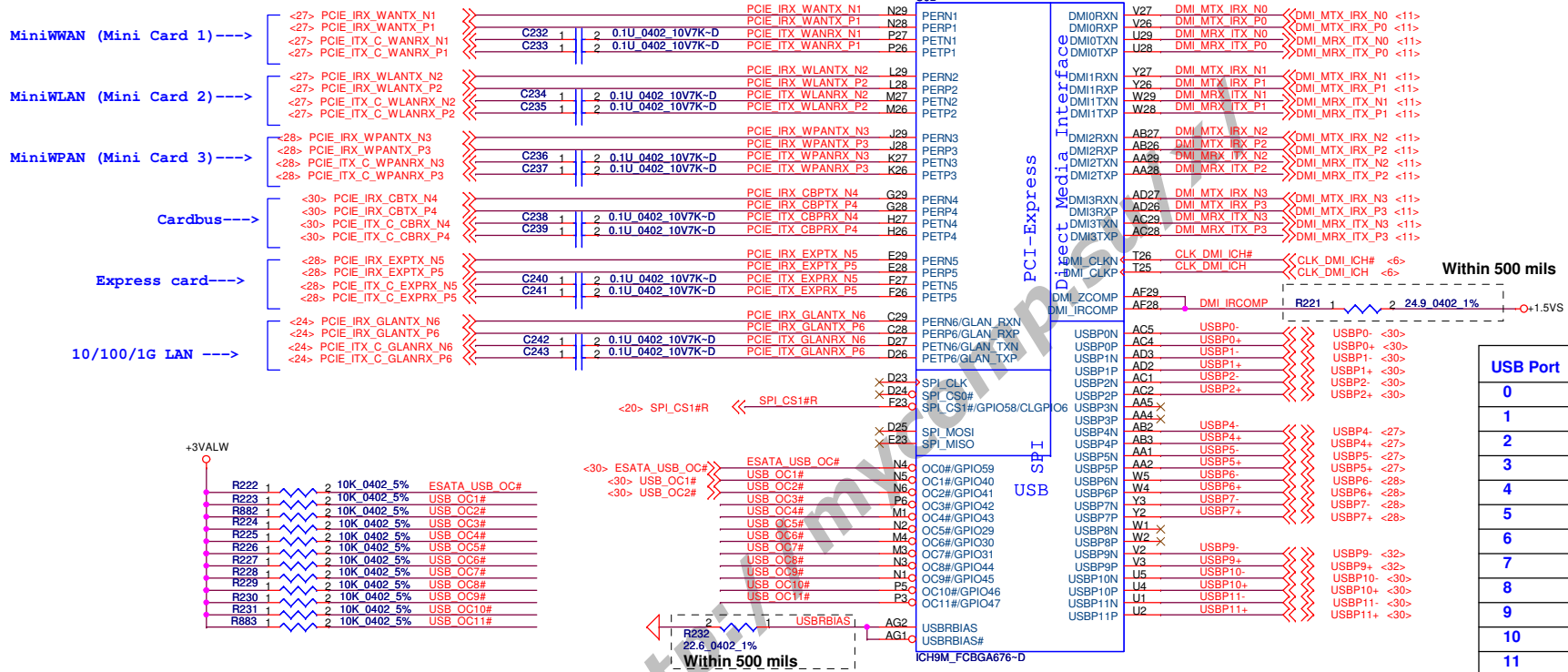
http://www.compart.com

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	LA-5152P	A00	
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Within 500 mils

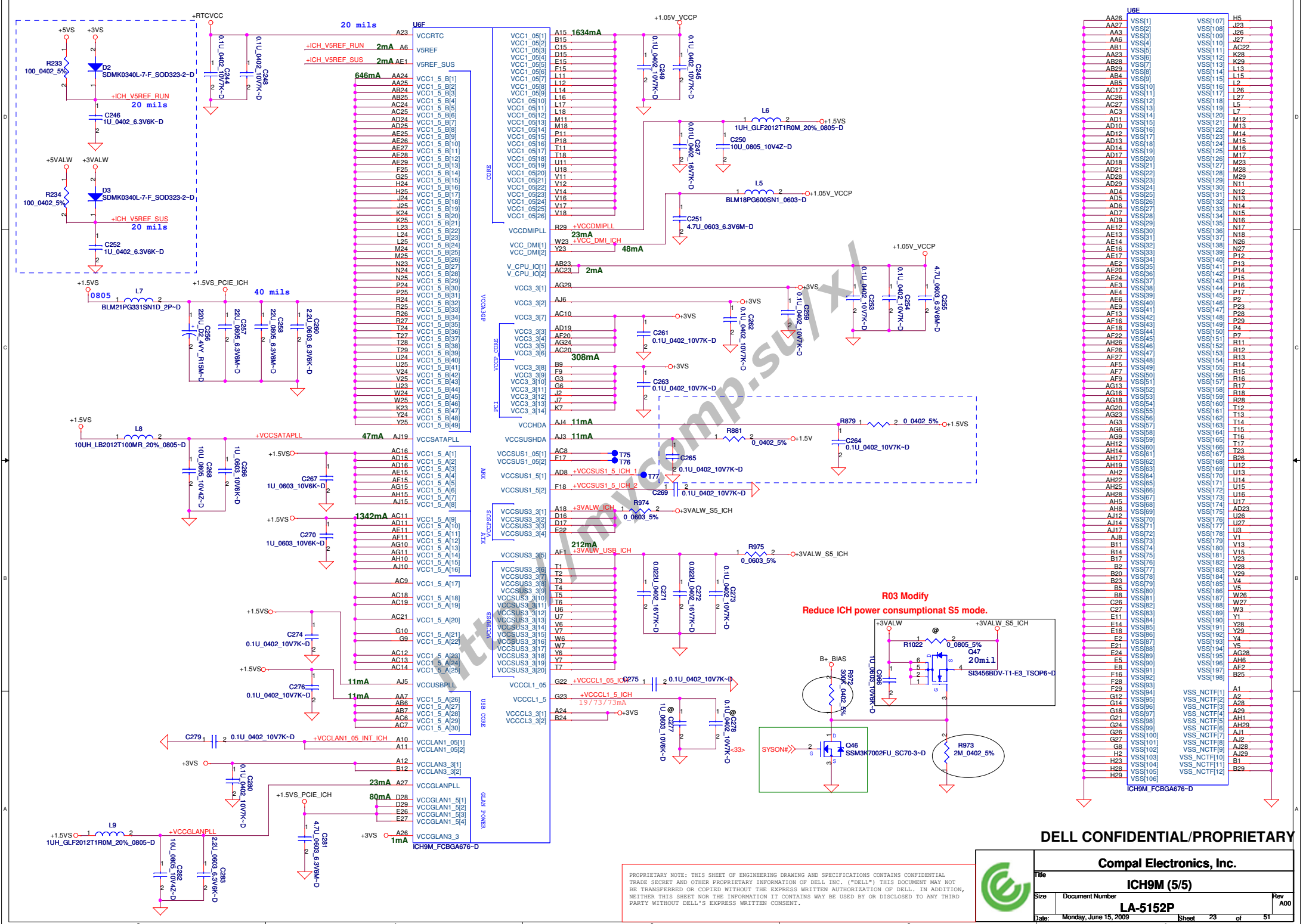
USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

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Title		ICH9-M(4/5)	
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Date: Monday, June 15, 2009		Sheet 22 of 51	

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U8E	AA26	VSS1[1]	VSS1[07]	H5
	AA27	VSS1[09]	VSS1[10]	J23
	AA3	VSS3[3]	VSS1[09]	J26
	AA6	VSS1[10]	VSS1[11]	J27
	AA23	VSS5[5]	VSS1[11]	AC22
	AA24	VSS5[6]	VSS1[12]	K28
	AB29	VSS8[7]	VSS1[13]	K29
	AB4	VSS9[8]	VSS1[14]	L13
	AB5	VSS1[15]	VSS1[15]	L5
	AC17	VSS1[11]	VSS1[17]	L26
	AC26	VSS1[12]	VSS1[17]	L27
	AD1	VSS1[15]	VSS1[20]	L7
	AD10	VSS1[16]	VSS1[20]	M12
	AD12	VSS1[17]	VSS1[21]	M13
	AD13	VSS1[18]	VSS1[22]	M14
	AD14	VSS1[19]	VSS1[24]	M15
	AD17	VSS1[20]	VSS1[24]	M16
	AD18	VSS1[21]	VSS1[25]	M17
	AD21	VSS1[22]	VSS1[27]	M23
	AD22	VSS1[23]	VSS1[28]	M29
	AD29	VSS1[24]	VSS1[30]	N11
	AD4	VSS1[25]	VSS1[32]	N12
	AD6	VSS1[26]	VSS1[32]	N14
	AD7	VSS1[27]	VSS1[34]	N15
	AD9	VSS1[29]	VSS1[35]	N16
	AE12	VSS3[0]	VSS1[36]	N17
	AE13	VSS3[1]	VSS1[37]	N18
	AE14	VSS3[2]	VSS1[38]	N26
	AE16	VSS3[3]	VSS1[39]	N27
	AE17	VSS3[4]	VSS1[40]	P12
	AE2	VSS3[5]	VSS1[40]	P13
	AE20	VSS3[6]	VSS1[41]	P14
	AE24	VSS3[7]	VSS1[43]	P15
	AE3	VSS3[8]	VSS1[44]	P17
	AE4	VSS3[9]	VSS1[45]	P18
	AE6	VSS3[10]	VSS1[45]	P2
	AE9	VSS3[11]	VSS1[47]	P23
	AF13	VSS3[12]	VSS1[48]	P28
	AF16	VSS3[13]	VSS1[48]	P29
	AF18	VSS3[14]	VSS1[49]	P4
	AF22	VSS3[15]	VSS1[51]	P7
	AH8	VSS3[16]	VSS1[52]	R11
	AH9	VSS3[17]	VSS1[53]	R12
	AF27	VSS3[18]	VSS1[53]	R13
	AF5	VSS3[19]	VSS1[55]	R14
	AF7	VSS3[20]	VSS1[56]	R15
	AG3	VSS3[21]	VSS1[57]	R17
	AG13	VSS3[22]	VSS1[58]	R16
	AG16	VSS3[23]	VSS1[59]	R18
	AG18	VSS3[24]	VSS1[60]	R28
	AG20	VSS3[25]	VSS1[61]	R29
	AG23	VSS3[26]	VSS1[62]	T2
	AG3	VSS3[27]	VSS1[62]	T3
	AH12	VSS3[28]	VSS1[63]	T4
	AH2	VSS3[29]	VSS1[63]	T13
	AH22	VSS3[30]	VSS1[64]	T14
	AH25	VSS3[31]	VSS1[64]	T15
	AH28	VSS3[32]	VSS1[65]	T16
	AH5	VSS3[33]	VSS1[66]	T17
	AH8	VSS3[34]	VSS1[68]	T23
	AH14	VSS3[35]	VSS1[68]	B26
	AH17	VSS3[36]	VSS1[69]	L12
	AH2	VSS3[37]	VSS1[69]	L13
	AH22	VSS3[38]	VSS1[70]	L14
	AH25	VSS3[39]	VSS1[72]	L15
	AH28	VSS3[40]	VSS1[72]	L16
	AH5	VSS3[41]	VSS1[73]	L17
	AH8	VSS3[42]	VSS1[74]	AD23
	AH12	VSS3[43]	VSS1[76]	U26
	AH14	VSS3[44]	VSS1[77]	U27
	AH17	VSS3[45]	VSS1[77]	U1
	AH2	VSS3[46]	VSS1[78]	V1
	AH22	VSS3[47]	VSS1[78]	V13
	AH25	VSS3[48]	VSS1[80]	V15
	AH28	VSS3[49]	VSS1[80]	V18
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	AH8	VSS3[51]	VSS1[82]	V28
	AH14	VSS3[52]	VSS1[83]	V29
	AH17	VSS3[53]	VSS1[84]	V3
	AH2	VSS3[54]	VSS1[85]	V4
	AH22	VSS3[55]	VSS1[86]	W26
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	AH28	VSS3[57]	VSS1[88]	W3
	AH5	VSS3[58]	VSS1[89]	Y1
	AH8	VSS3[59]	VSS1[90]	Y28
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	AH14	VSS3[61]	VSS1[92]	Y4
	AH17	VSS3[62]	VSS1[93]	Y5
	AH2	VSS3[63]	VSS1[94]	AG28
	AH22	VSS3[64]	VSS1[95]	AH6
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	AH28	VSS3[74]	VSS1[98]	
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	AH17	VSS3[78]	VSS1[98]	
	AH2	VSS3[79]	VSS1[98]	
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	AH28	VSS3[82]	VSS1[98]	
	AH5	VSS3[83]	VSS1[98]	
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	AH8	VSS3[100]	VSS1[98]	
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	AH22	VSS3[104]	VSS1[98]	
	AH25	VSS3[105]	VSS1[98]	
	AH28	VSS3[106]	VSS1[98]	
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		VSS_NCTF1[2]	VSS_NCTF[2]	A2
		VSS_NCTF1[3]	VSS_NCTF[3]	A28
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		VSS_NCTF1[5]	VSS_NCTF[5]	AH1
		VSS_NCTF1[6]	VSS_NCTF[6]	AH29
		VSS_NCTF1[7]	VSS_NCTF[7]	AJ1
		VSS_NCTF1[8]	VSS_NCTF[8]	AJ28
		VSS_NCTF1[9]	VSS_NCTF[9]	AJ29
		VSS_NCTF1[10]	VSS_NCTF[10]	B1
		VSS_NCTF1[11]	VSS_NCTF[11]	B29
		VSS_NCTF1[12]	VSS_NCTF[12]	

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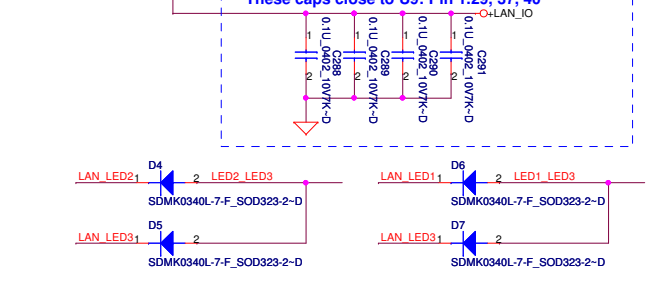
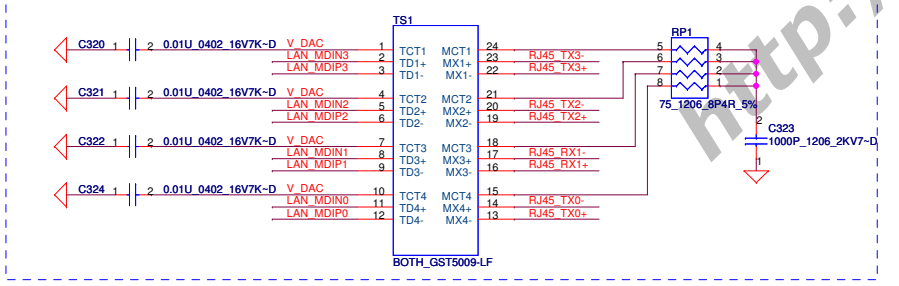
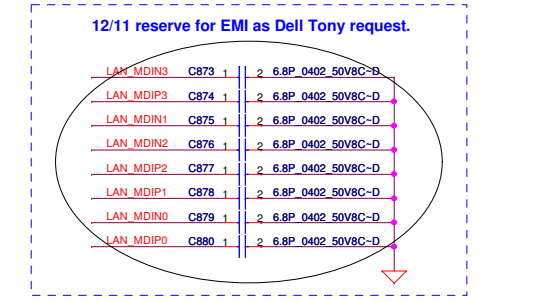
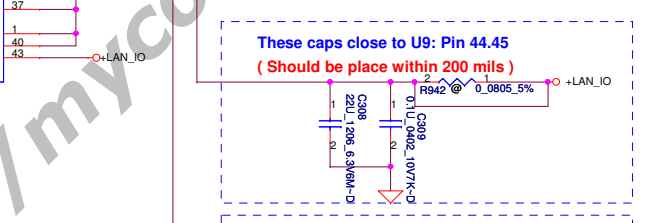
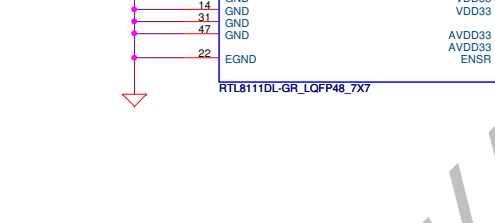
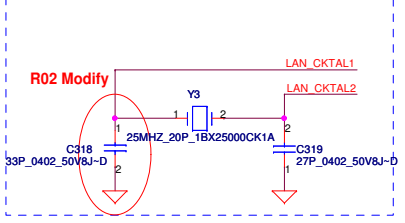
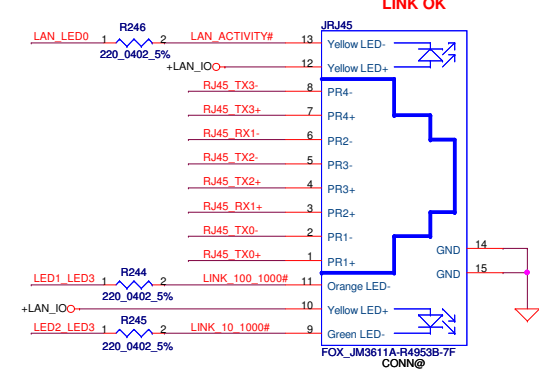
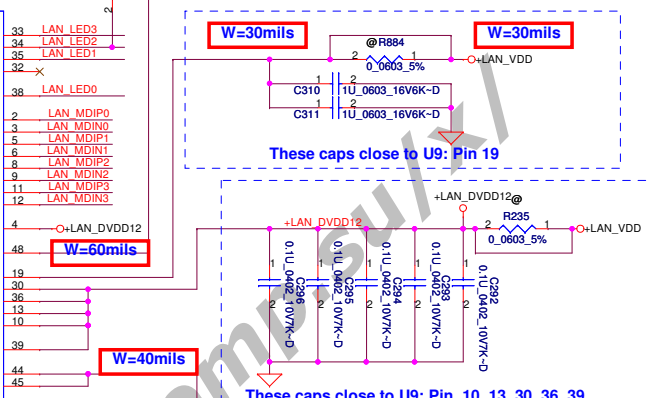
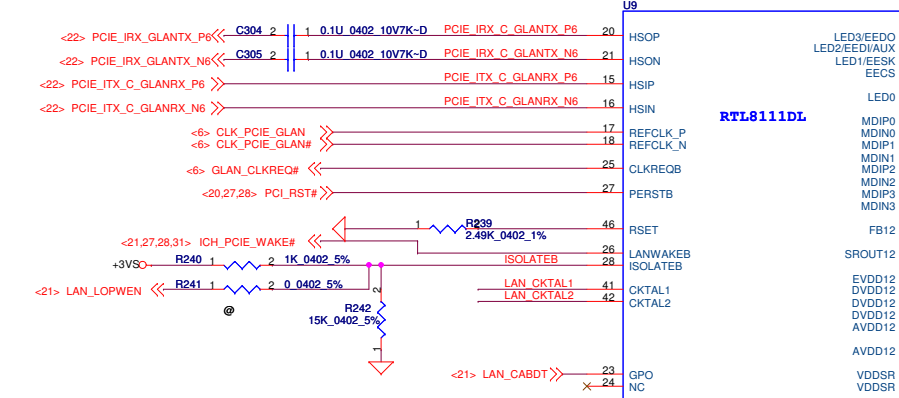
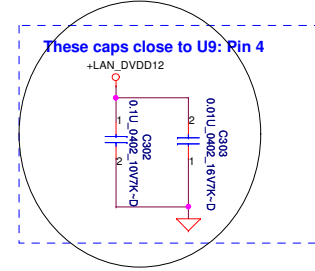
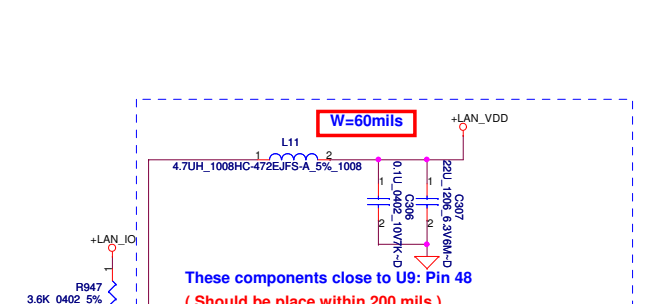
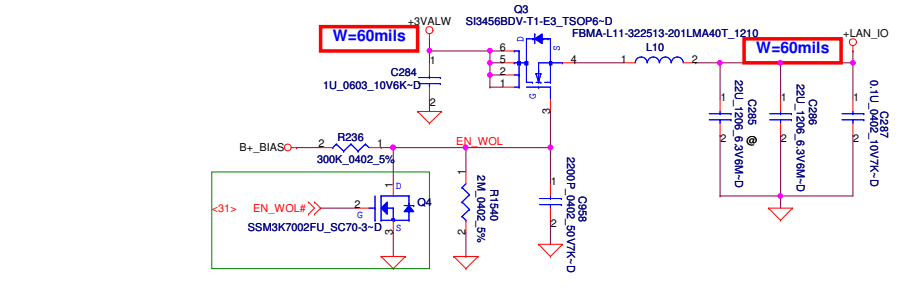
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ICH9M (5/5)

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LEDS1-0	00	01	10	11
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 / 100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT

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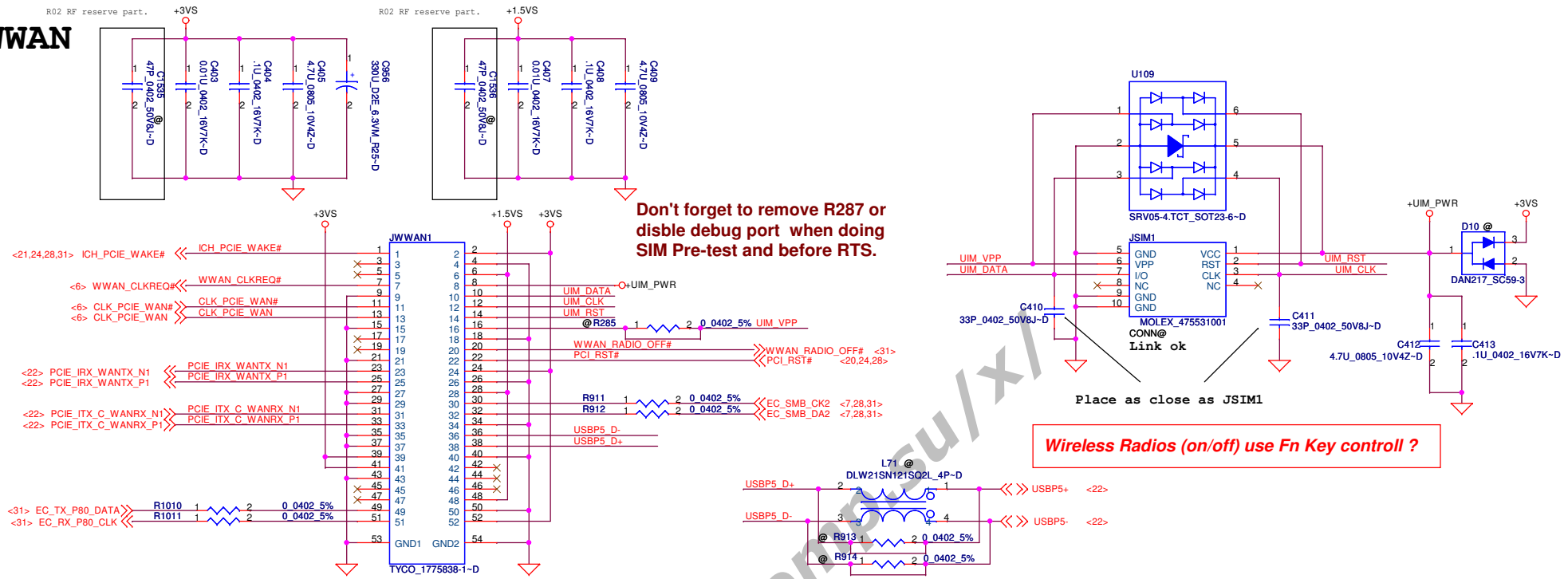
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Title
Gigabit LAN RTL8111DL

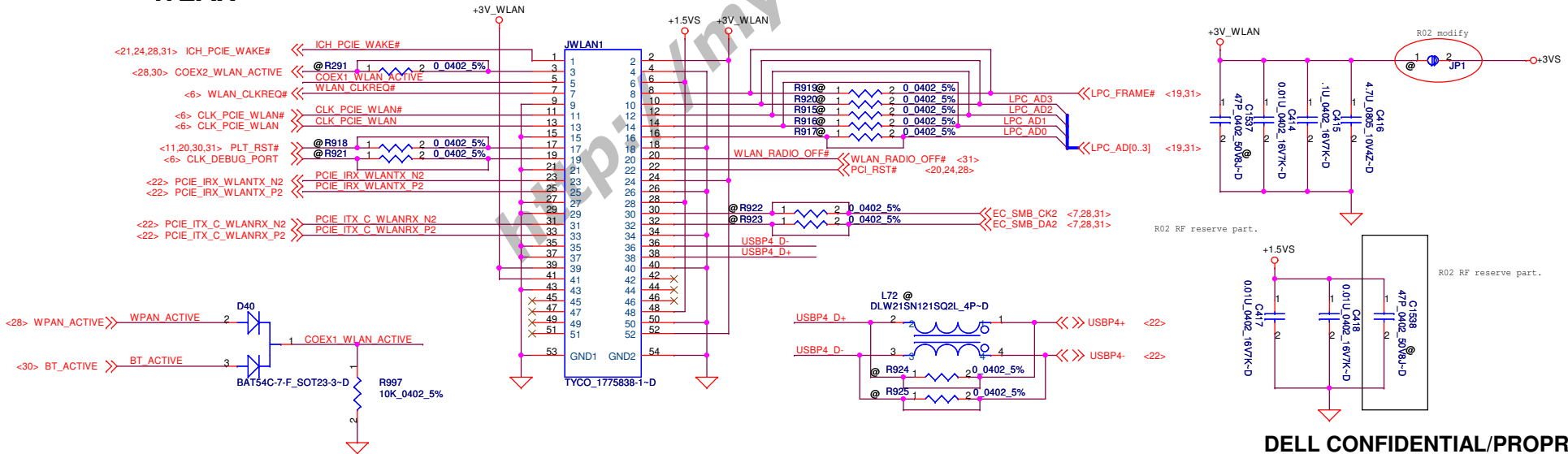
Size Document Number
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WWAN



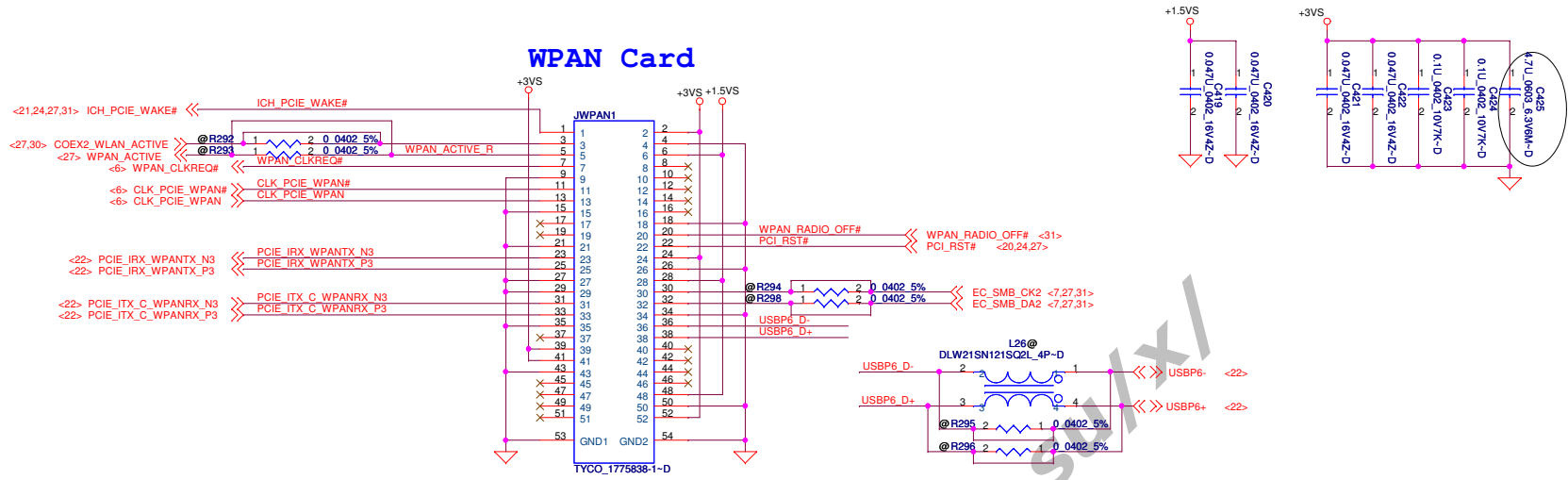
WLAN



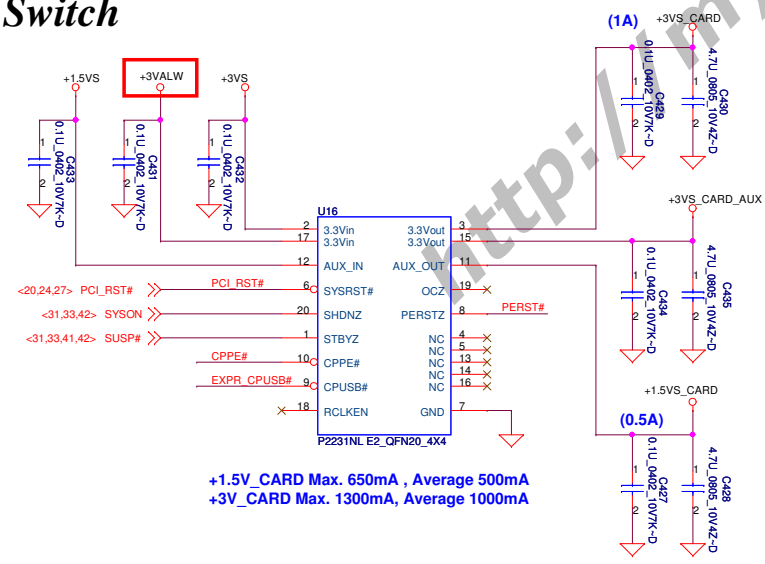
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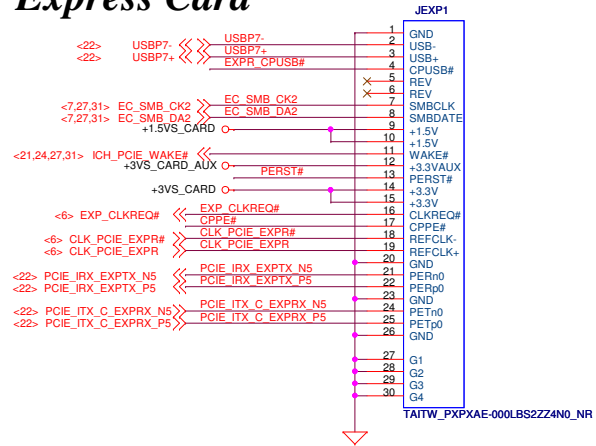
		Compal Electronics, Inc.	
		Mini Card WLAN/WWAN	
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Express Card Power Switch



Express Card

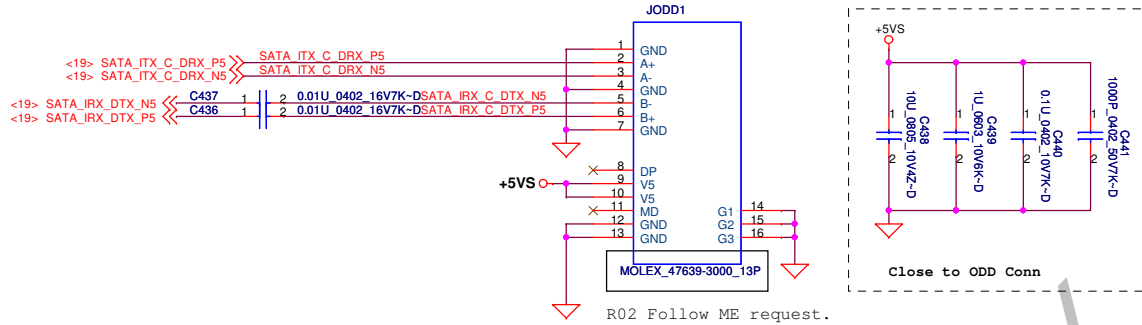


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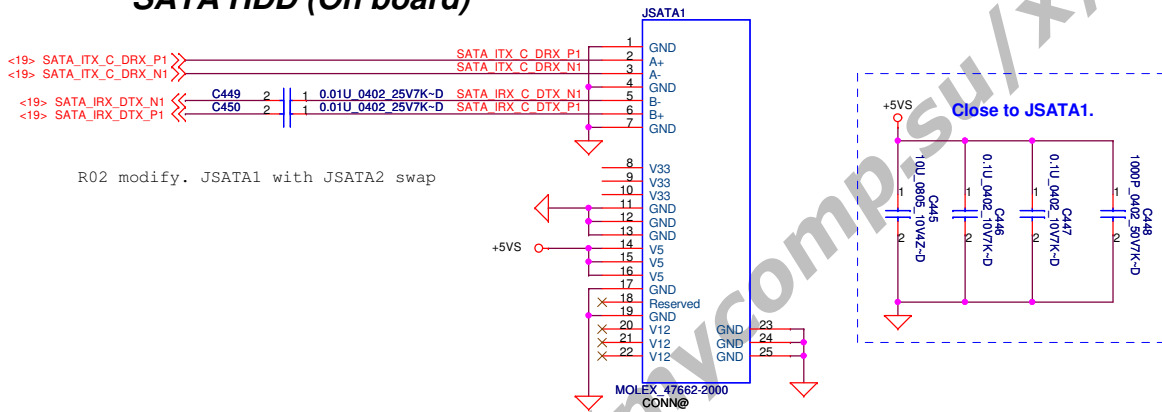
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	Compal Electronics, Inc.	
	WPAN / Express Card	
	Title Size Date	Document Number LA-5152P Monday, June 15, 2009

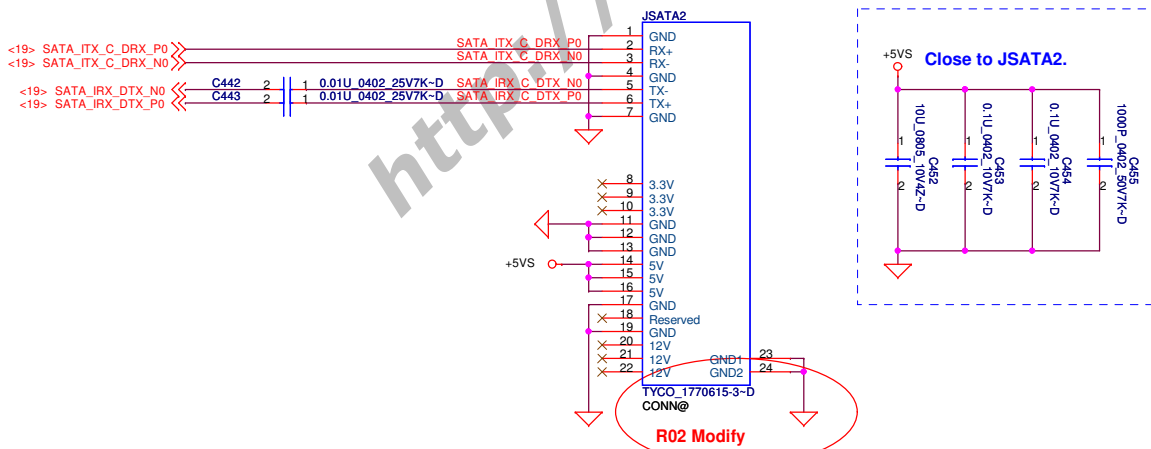
SATA ODD CONN



SATA HDD (On board)



SATA HDD



由於Kink pin尺寸大於kink hole，將導致零件干涉，也同時會使pin腳空焊 - 因此將 原HDD Conn.(REV.) -FOXCONN-SP01000LC0L layout 改成Tyco-SP01000E70L layout 即可解決造成pin腳空焊的問題

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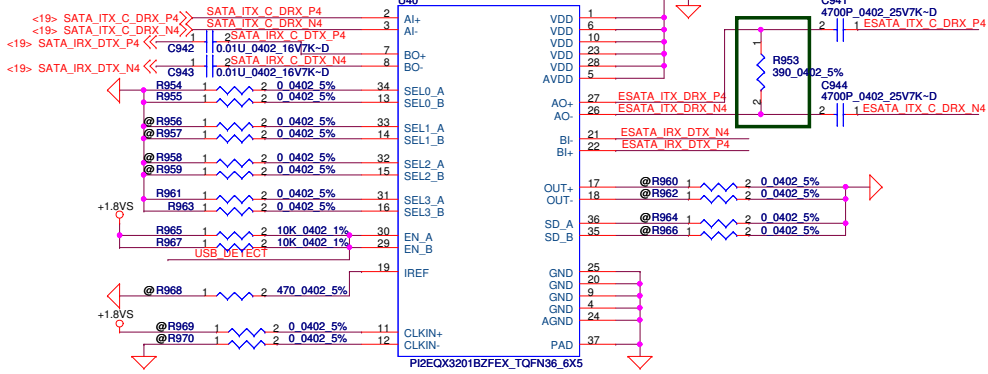
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ODD / SATA CONN		
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Output Swing Control

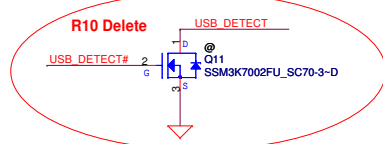
SEL2 [A:B]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL3 [A:B]	De-emphasis
0	0dB
1	-3.5dB

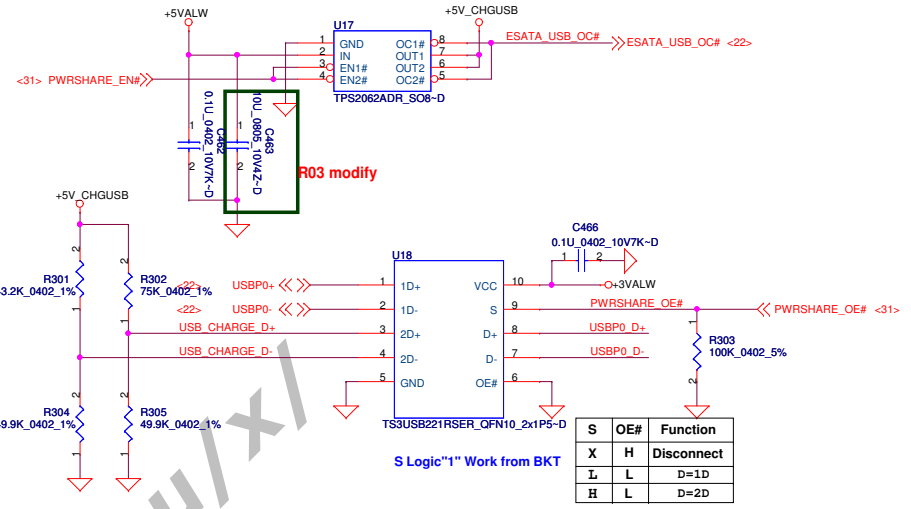
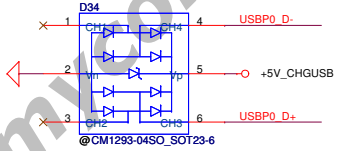


A00 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

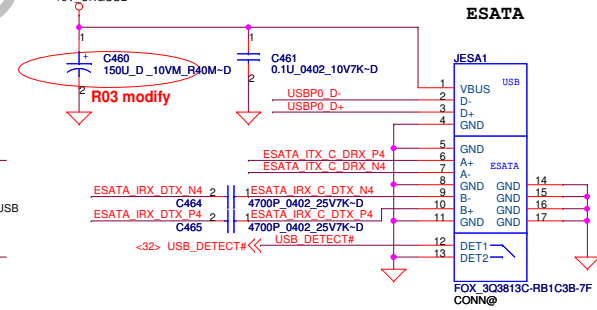


Equalizer Selection

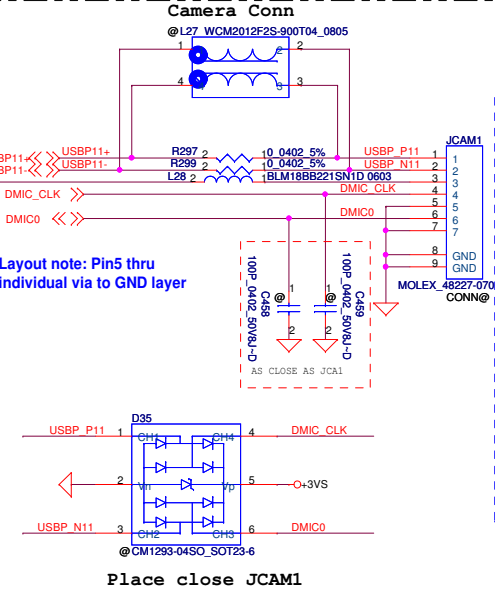
SEL0 [A:B]	SEL1 [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz



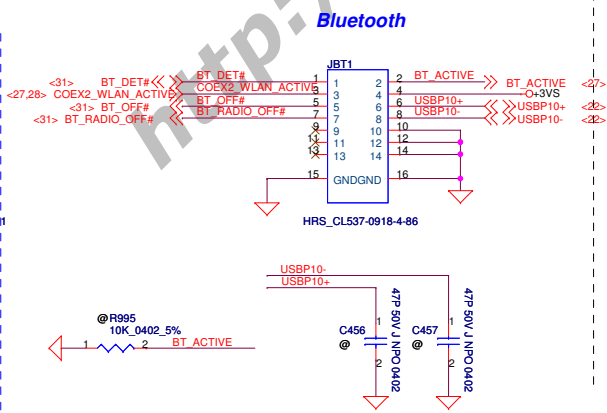
S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



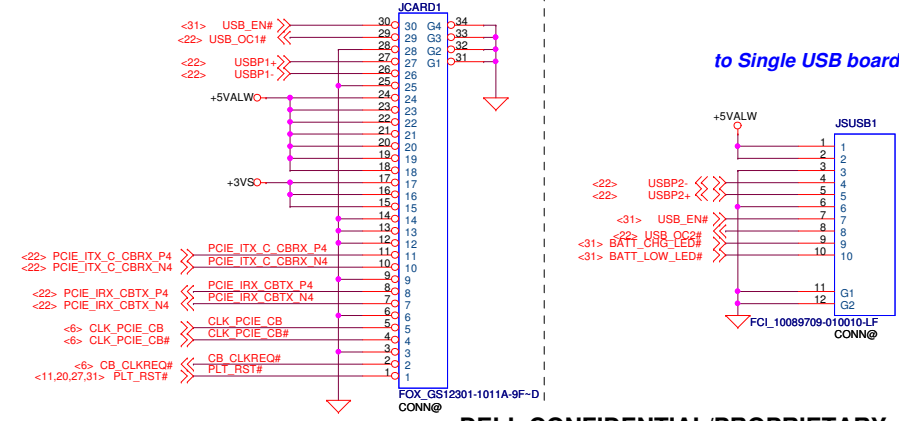
Place close JESA1



Place close JCAM1



Cardreader Connector



to Single USB board

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Compal Electronics, Inc.

USB / ESATA / BT / CAMARA

Document Number: **LA-5152P**

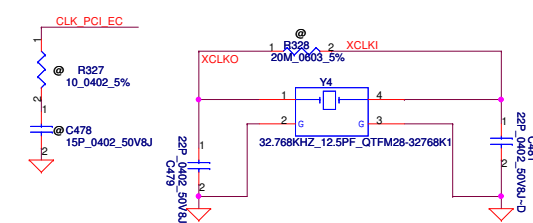
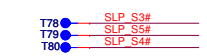
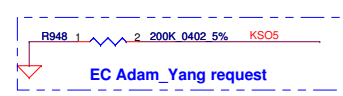
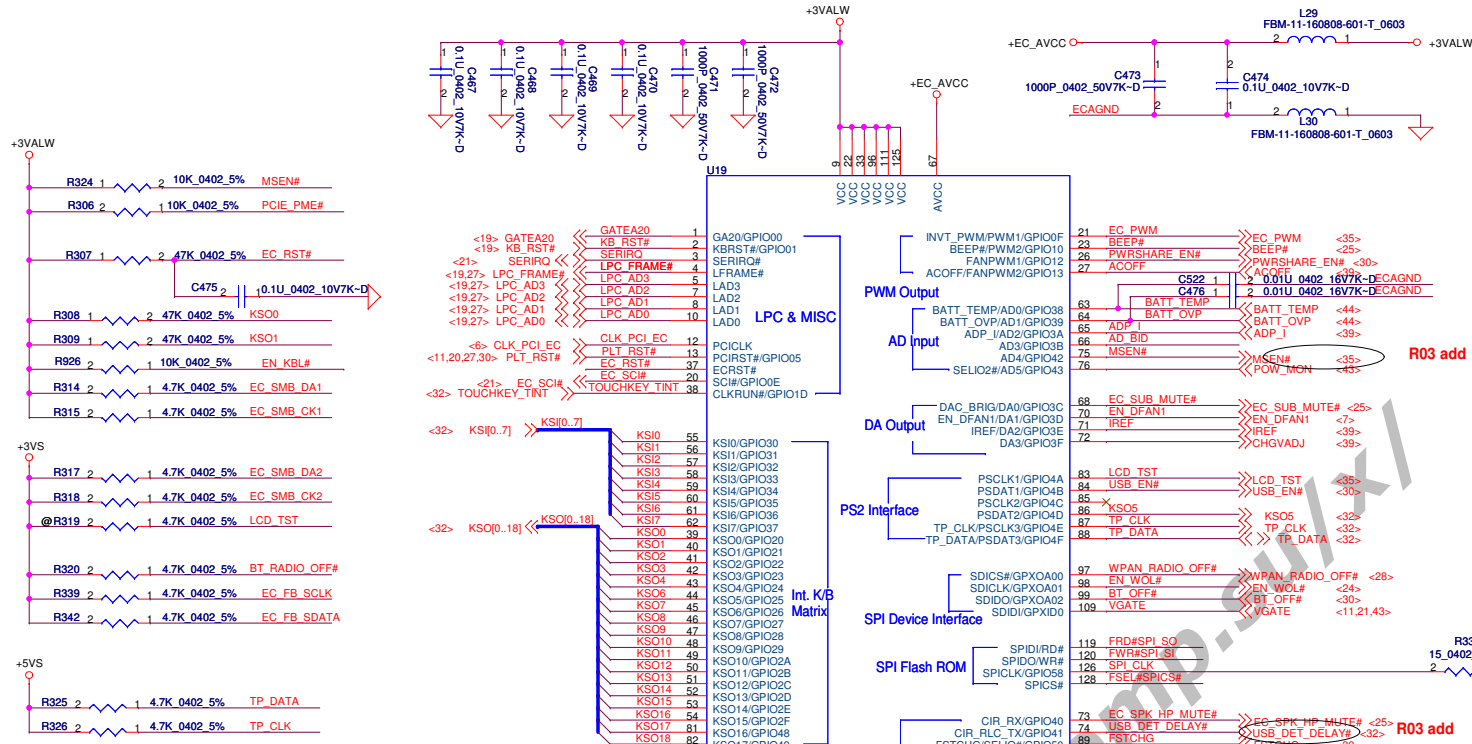
Date: Monday, June 15, 2009

Size: **LA-5152P**

Rev: **A00**

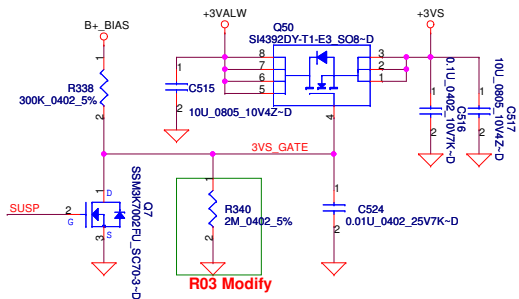
Date: Monday, June 15, 2009

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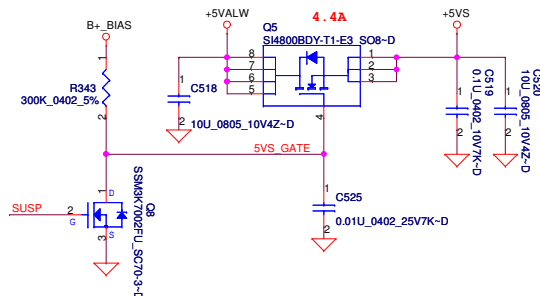


Pin	Signal	Component	Value
1	GATEA20		
2	KB_RST#		
3	SERIRQ		
4	LPC_FRAME#		
5	LPC_AD3		
6	LPC_AD2		
7	LPC_AD1		
8	LPC_AD0		
12	CLK_PCI_EC		
13	PLT_RST#		
14	EC_RST#		
15	EC_SCH#		
20	TOUCHKEY_TINT		
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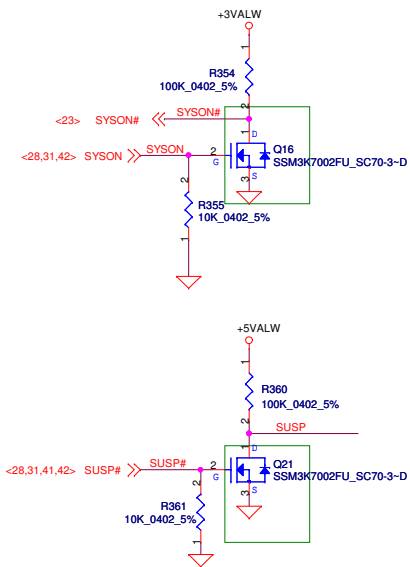
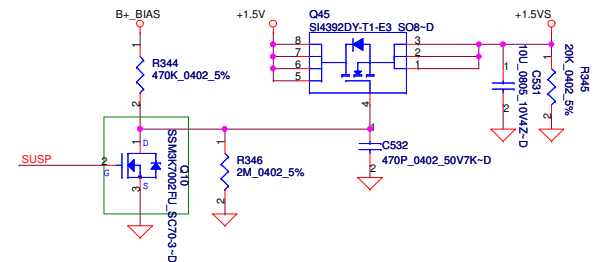
+3VALW to +3VS Transfer



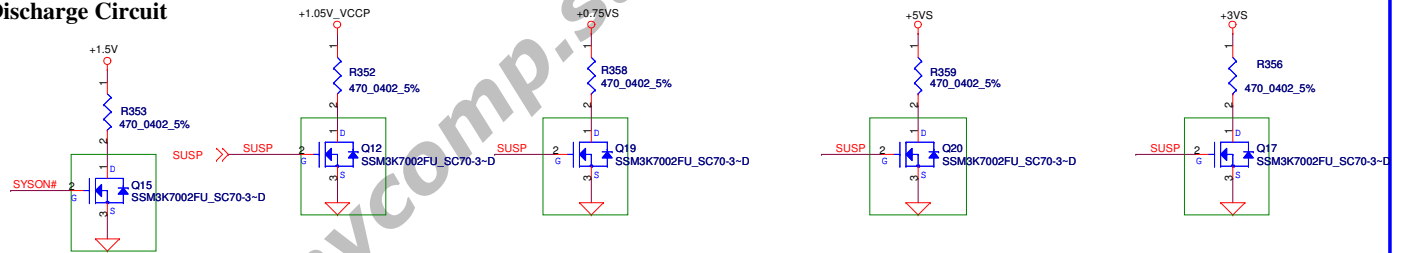
+5VALW to +5VS Transfer



+1.5V to +1.5VS Transfer



Discharge Circuit



R03 Delete +3V_WLAN discharge circuit.

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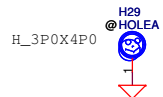
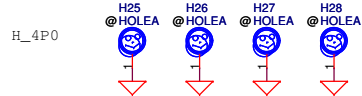
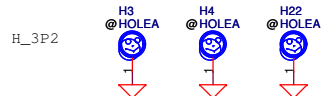
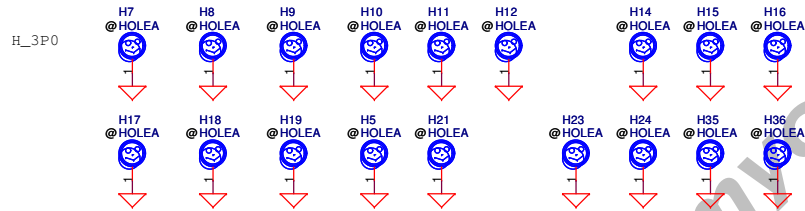
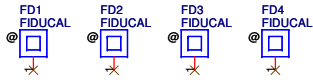
DC/DC Circuits

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<http://mycomp.su/xl>

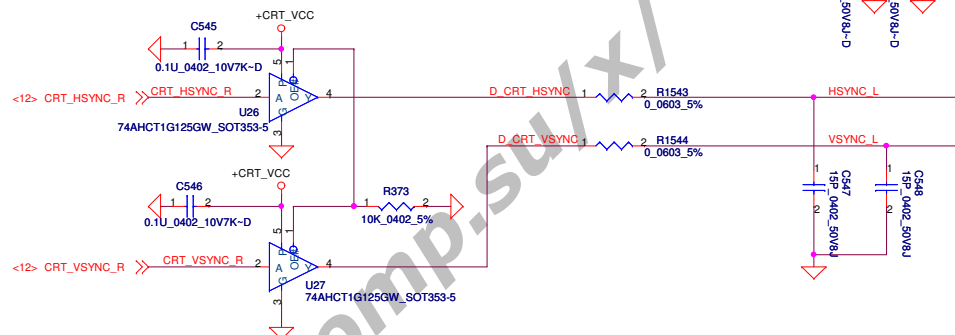
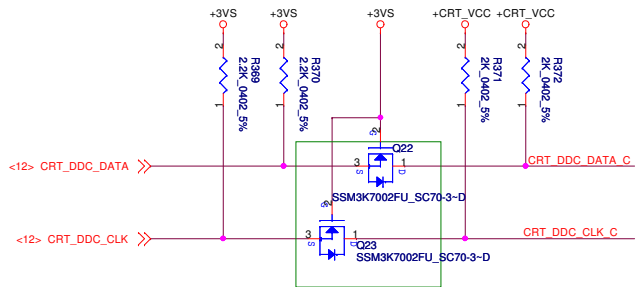
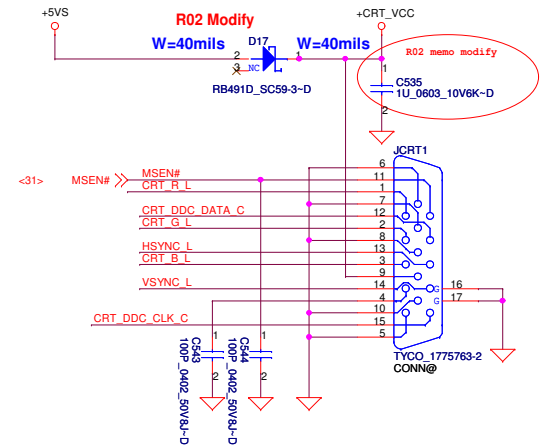
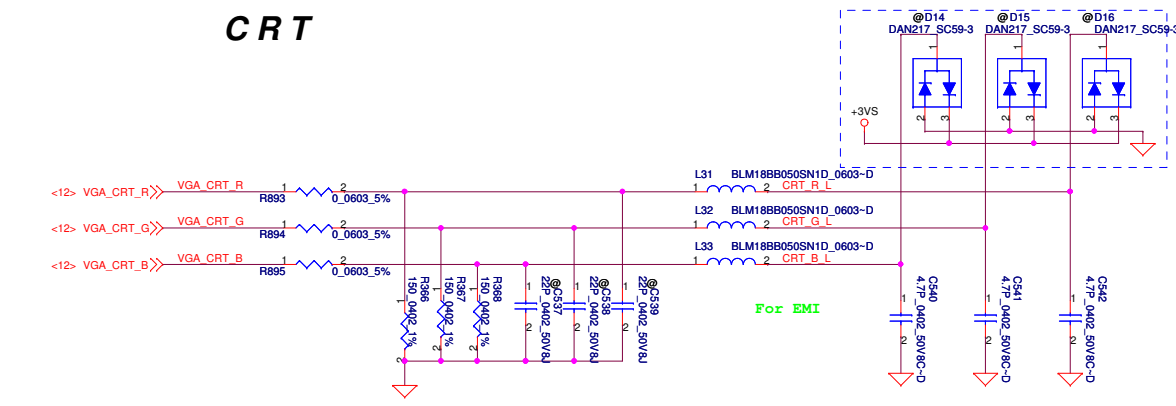
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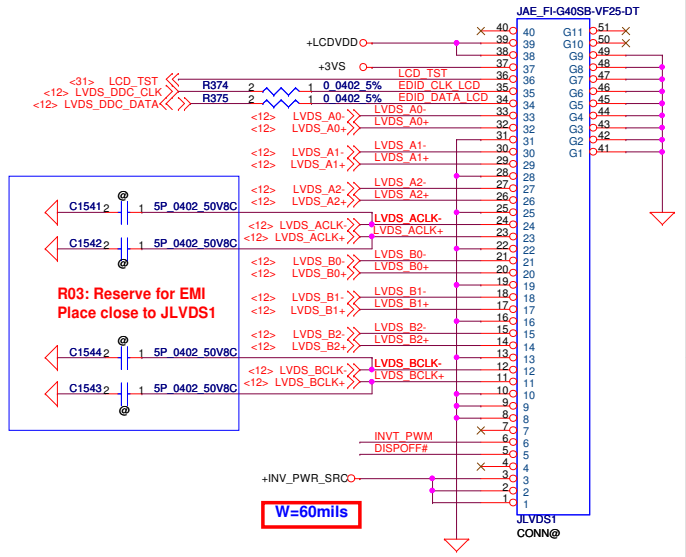
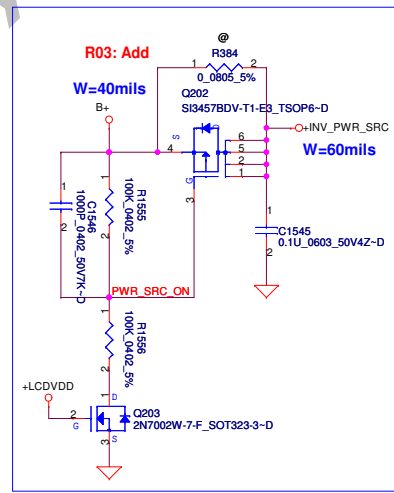
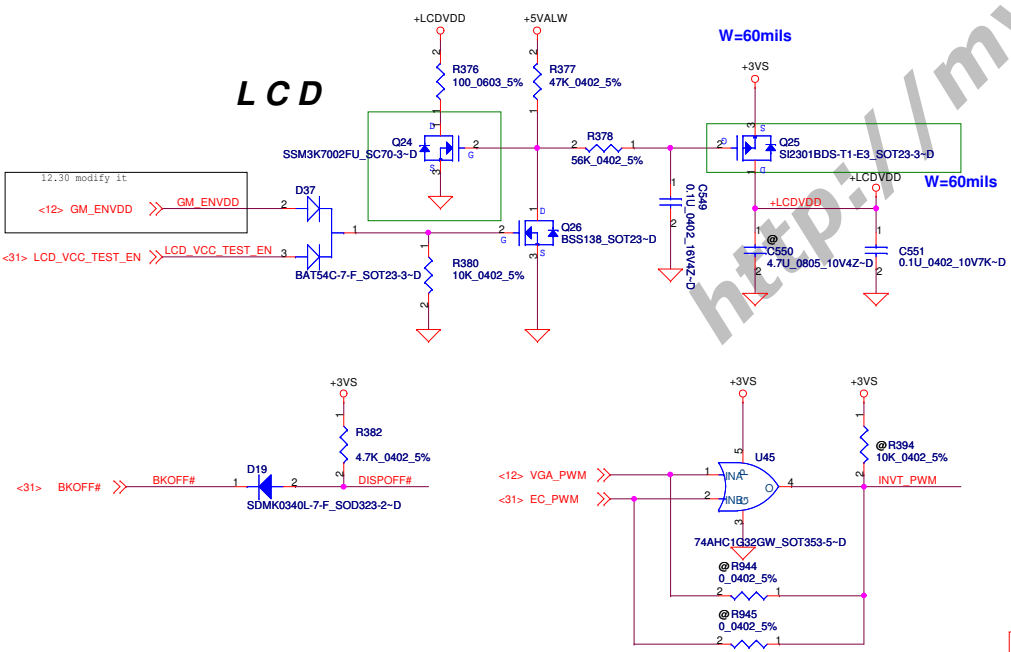


Compal Electronics, Inc.		
Title		
Screw		
Size	Document Number	Rev
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CRT



LCD

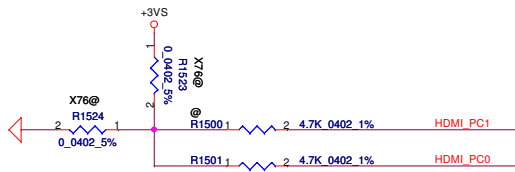


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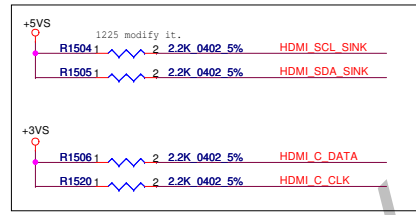
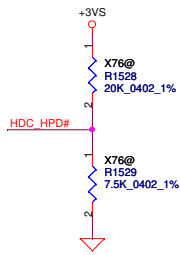
	Compal Electronics, Inc.	
	CRT / LVDS CONN	
	Size: LA-5152P Date: Monday, June 15, 2009	Document Number: LA-5152P Sheet: 35 of 51

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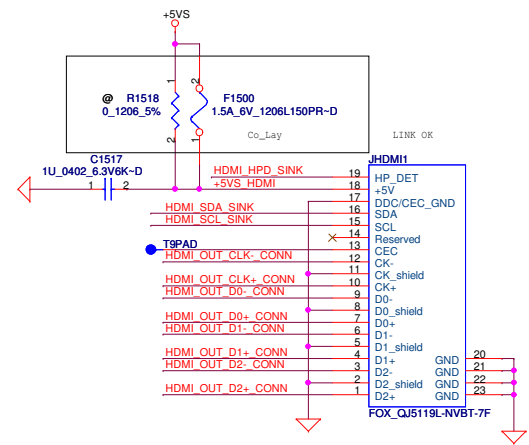
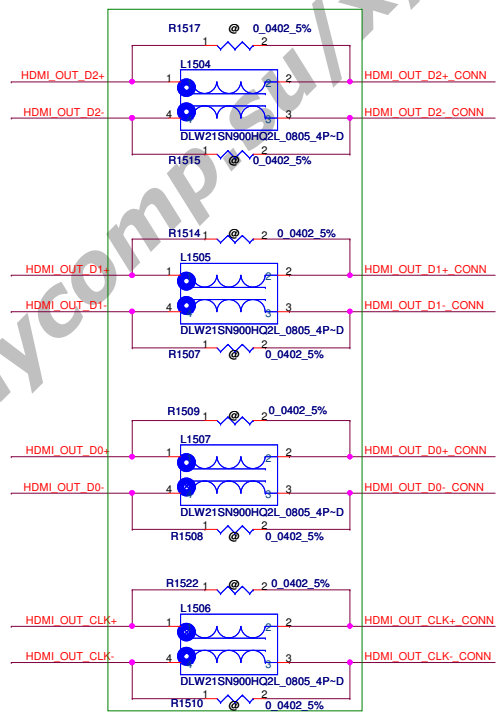
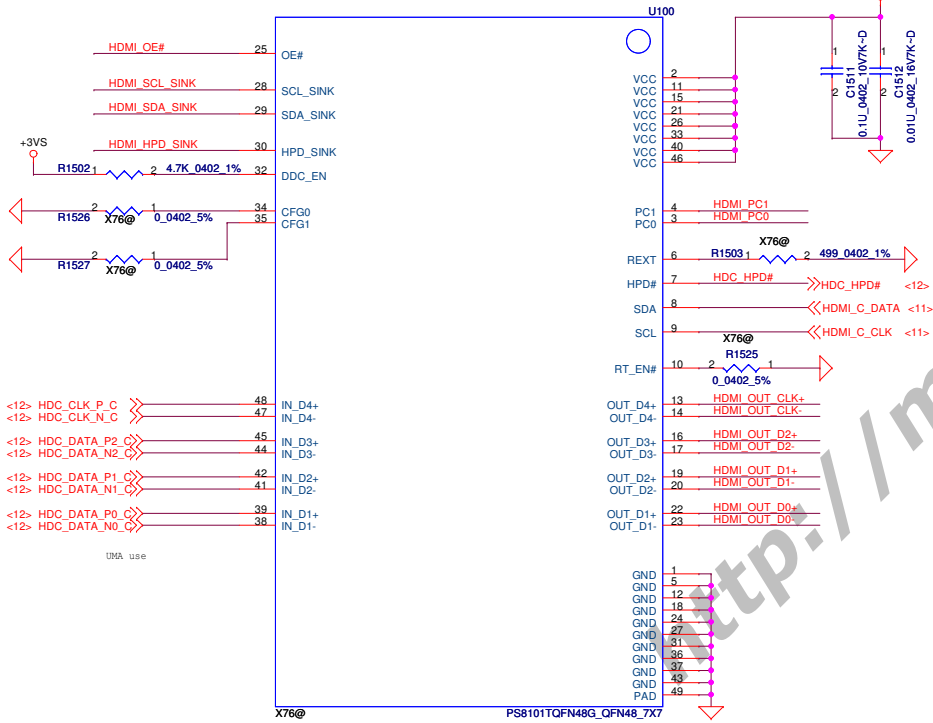
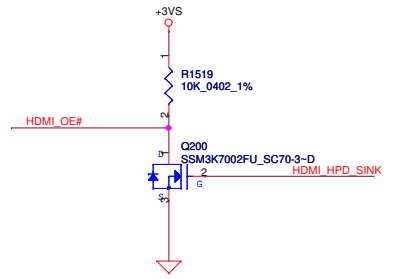
Recommended Equalization: [PC1,PC0]=01, 4dB



ST	Parade
R1523	X V
R1524	V V
R1503	4.3K 499
R1525	V X
R1526	V X
R1527	V X
R1528	V X
R1529	V X
U100	V V
R1500	V X
R1516	V X
R1511	V X
R1512	V X
R1513	V X
C1513	V X
C1514	V X
C1515	V X
C1516	V X



Vendor's suggestion for power saving.

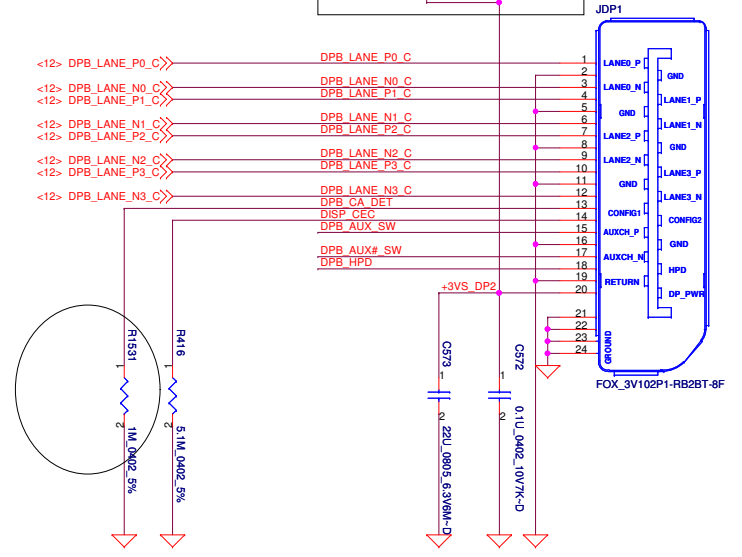
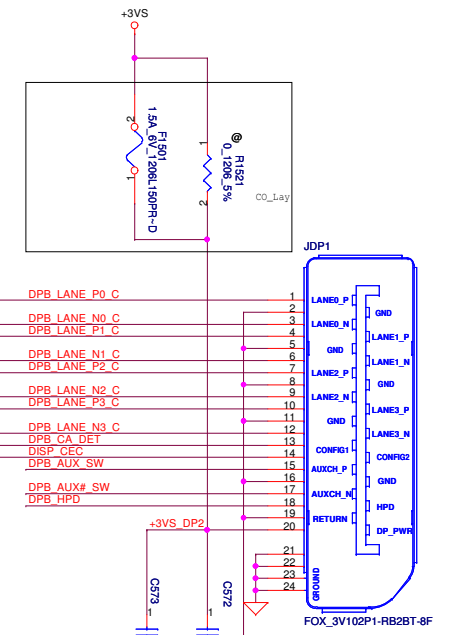
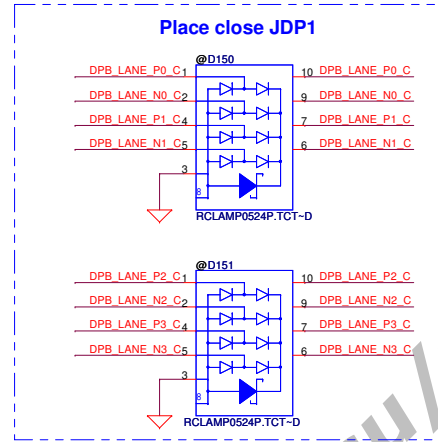
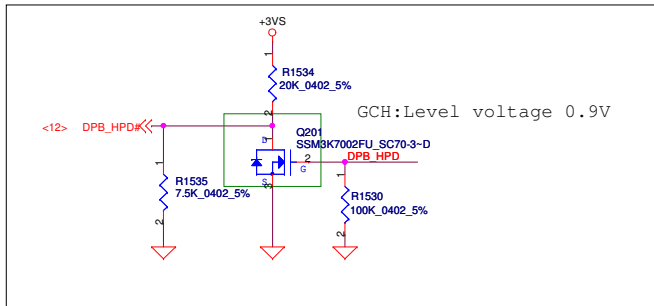


HDMI_OUT_D2+	@R1516	300_0402_1%	HDMI_OUT_D2+	@C1514	0.1U_0402_10V7K-D
HDMI_OUT_D1+	@R1511	300_0402_1%	HDMI_OUT_D1+	@C1513	0.1U_0402_10V7K-D
HDMI_OUT_D0+	@R1513	300_0402_1%	HDMI_OUT_D0+	@C1516	0.1U_0402_10V7K-D
HDMI_OUT_CLK+	@R1512	300_0402_1%	HDMI_OUT_CLK+	@C1515	0.1U_0402_10V7K-D

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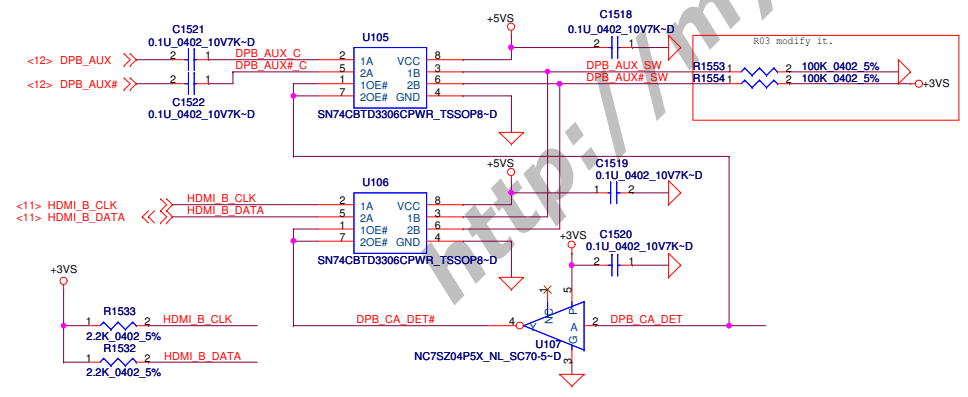
Compal Electronics, Inc.
HDMI CONN
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SW for MB side

DPB_CA_DET= 1 TMS Signaling
 DPB_CA_DET= 0 DP Signaling



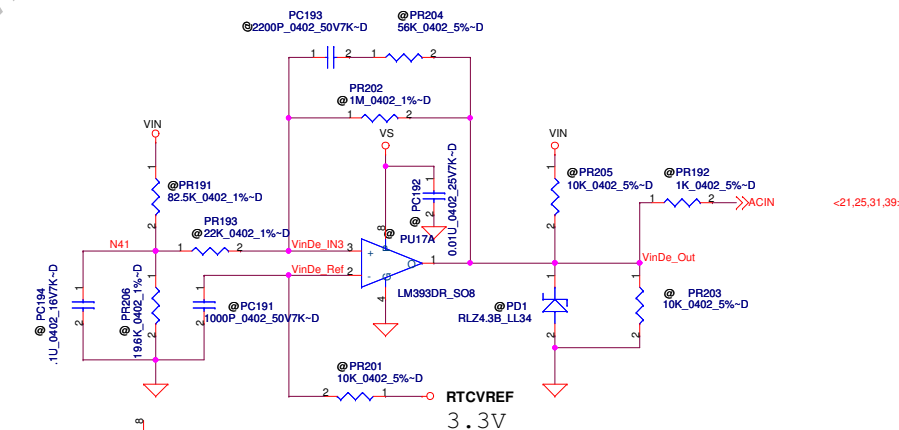
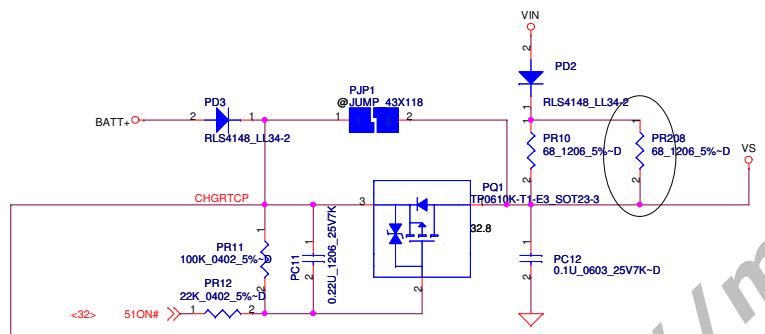
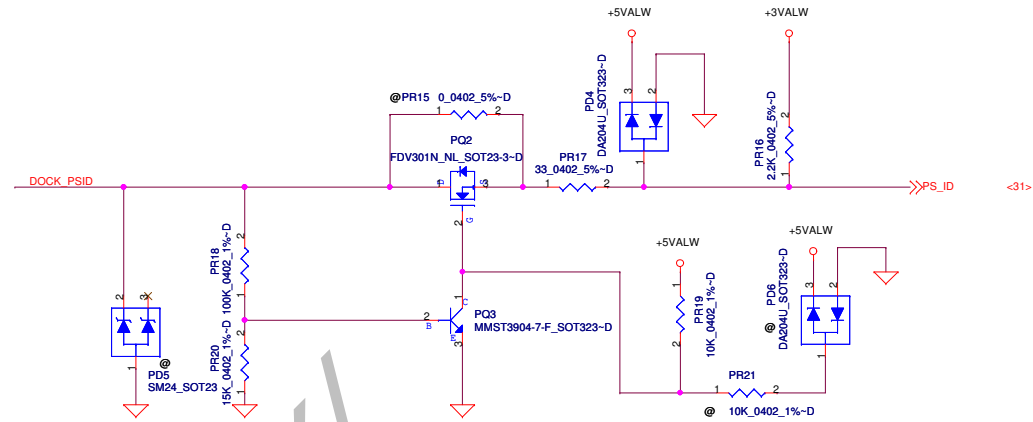
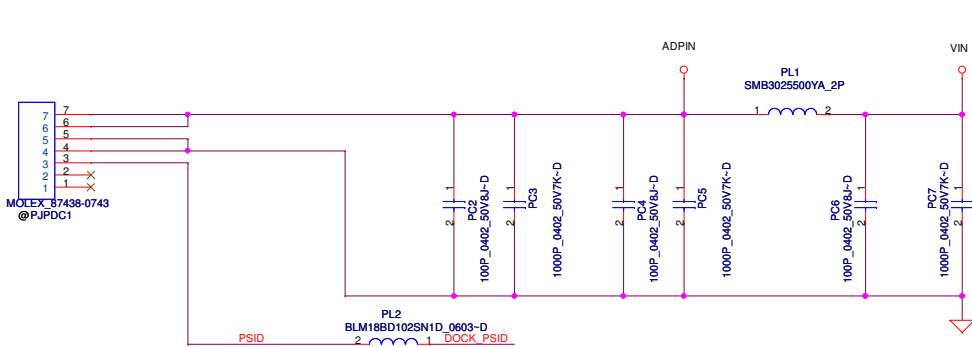
1225 modify it.

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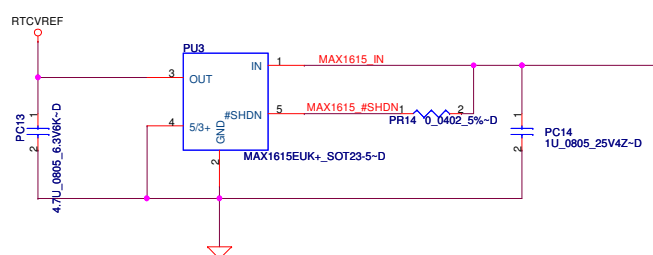
Compal Electronics, Inc.			
Display Port			
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Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

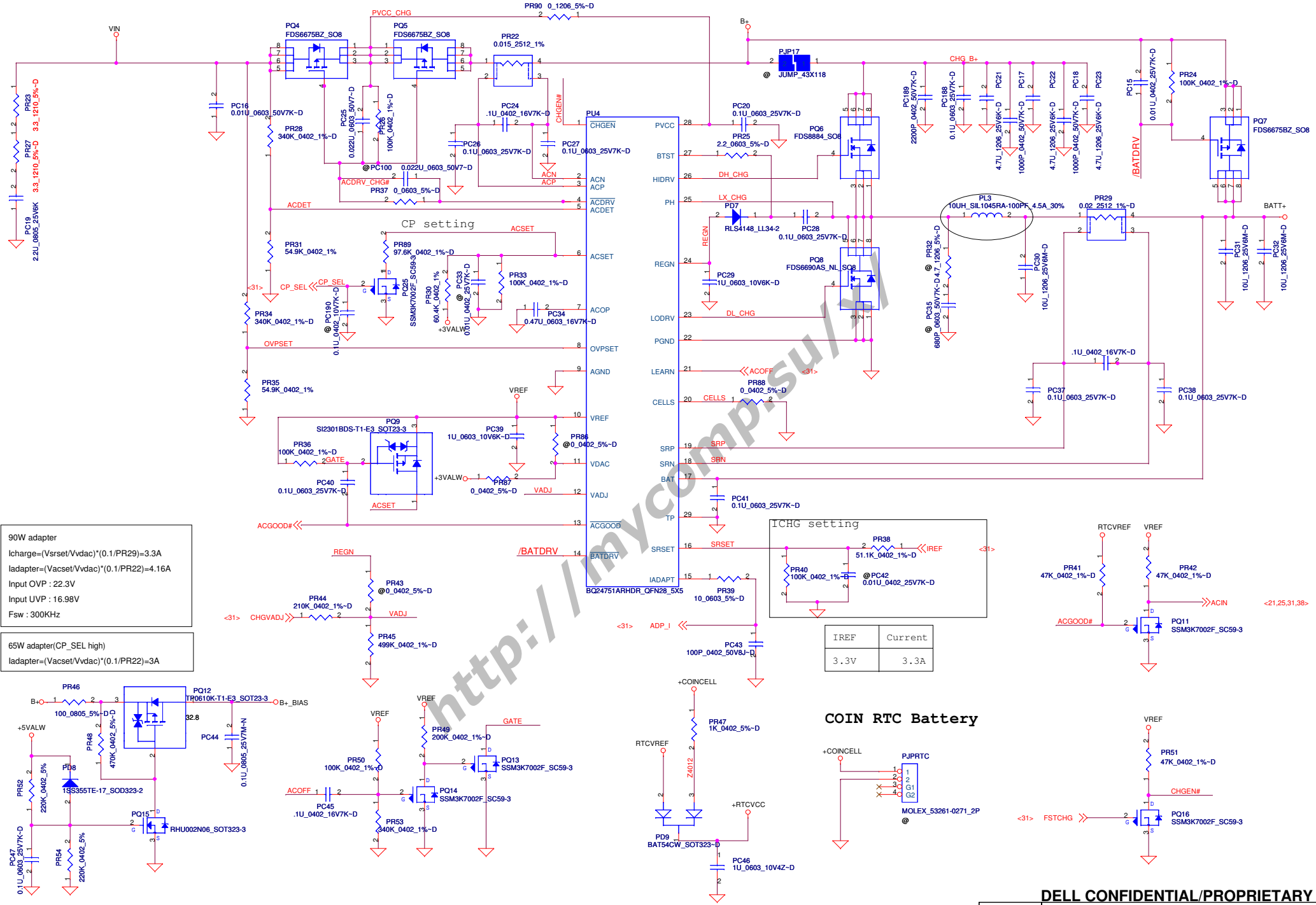


<http://mycomp.su/x/>

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Compal Electronics, Inc.
DCIN/Precharge
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90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR29) = 3.3A$
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR22) = 4.16A$
 Input OVP: 22.3V
 Input UVP: 16.98V
 Fsw : 300KHz

65W adapter(CP_SEL high)
 $I_{adapter} = (V_{acset}/V_{vdac}) * (0.1/PR22) = 3A$

IREF	Current
3.3V	3.3A

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Title: SCHEMATIC,MB A5152

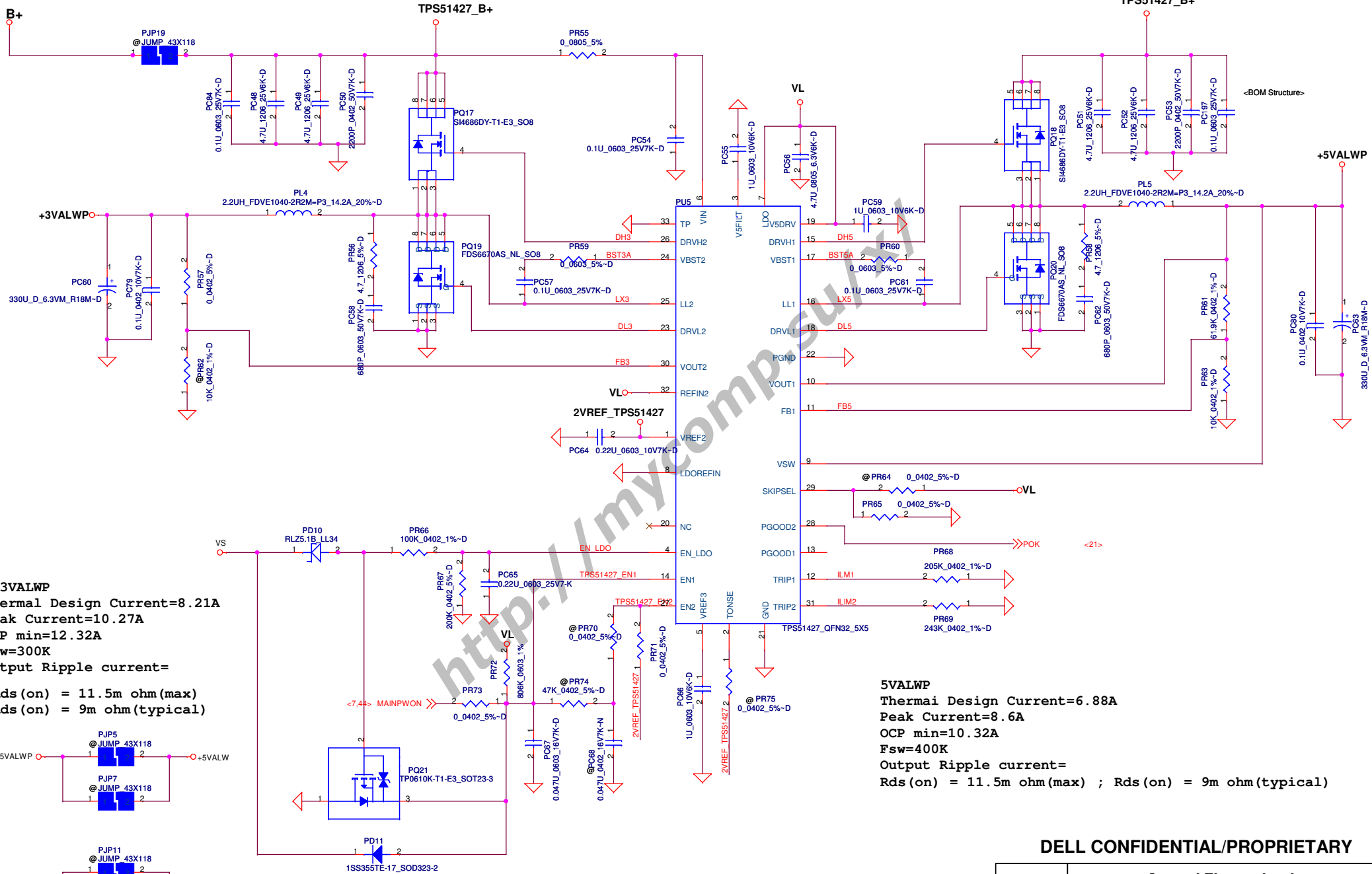
Size: LA-5152P

Date: Monday, June 15, 2009

Rev: A00

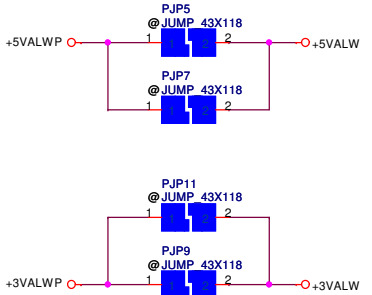
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3.3VALWP
 Thermal Design Current=8.21A
 Peak Current=10.27A
 OCP min=12.32A
 Fsw=300K
 Output Ripple current=
 Rds(on) = 11.5m ohm(max)
 Rds(on) = 9m ohm(typical)

5VALWP
 Thermal Design Current=6.88A
 Peak Current=8.6A
 OCP min=10.32A
 Fsw=400K
 Output Ripple current=
 Rds(on) = 11.5m ohm(max) ; Rds(on) = 9m ohm(typical)

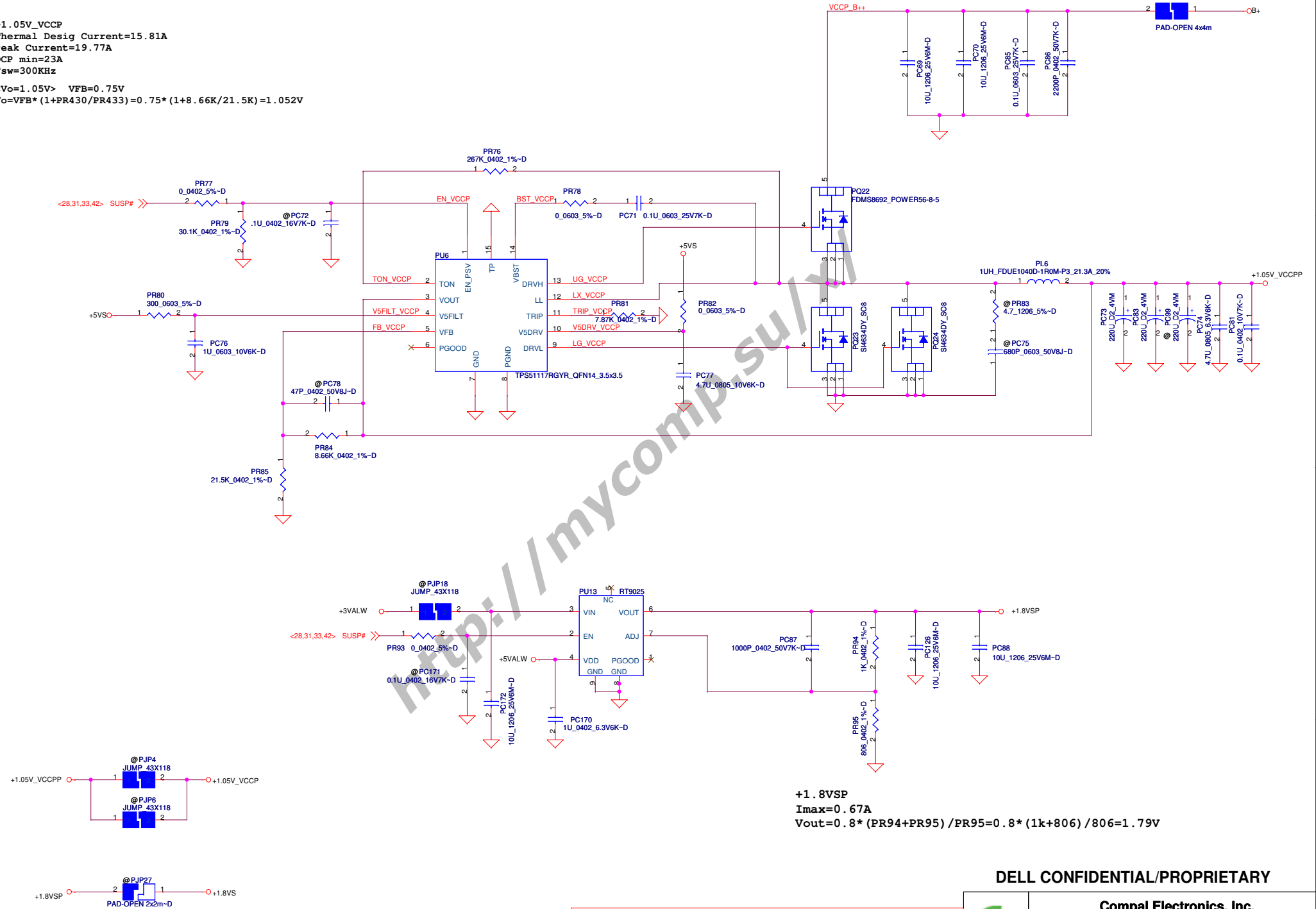


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Compal Electronics, Inc.		
+3VALWP/+5VALWP		
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+1.05V_VCCP
 Thermal Desig Current=15.81A
 Peak Current=19.77A
 OCP min=23A
 Fsw=300KHz
 $V_o=1.05V> \quad V_{FB}=0.75V$
 $V_o=V_{FB} * (1+PR430/PR433)=0.75 * (1+8.66K/21.5K)=1.052V$



+1.8VSP
 I_{max}=0.67A
 V_{out}=0.8 * (PR94+PR95) / PR95 = 0.8 * (1k+806) / 806 = 1.79V

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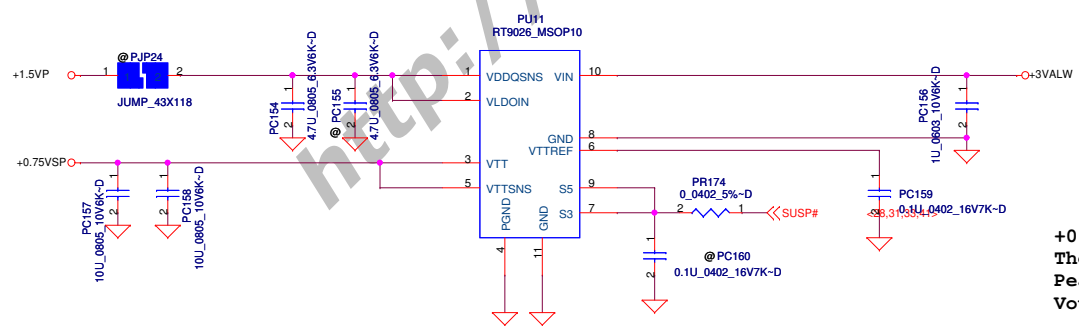
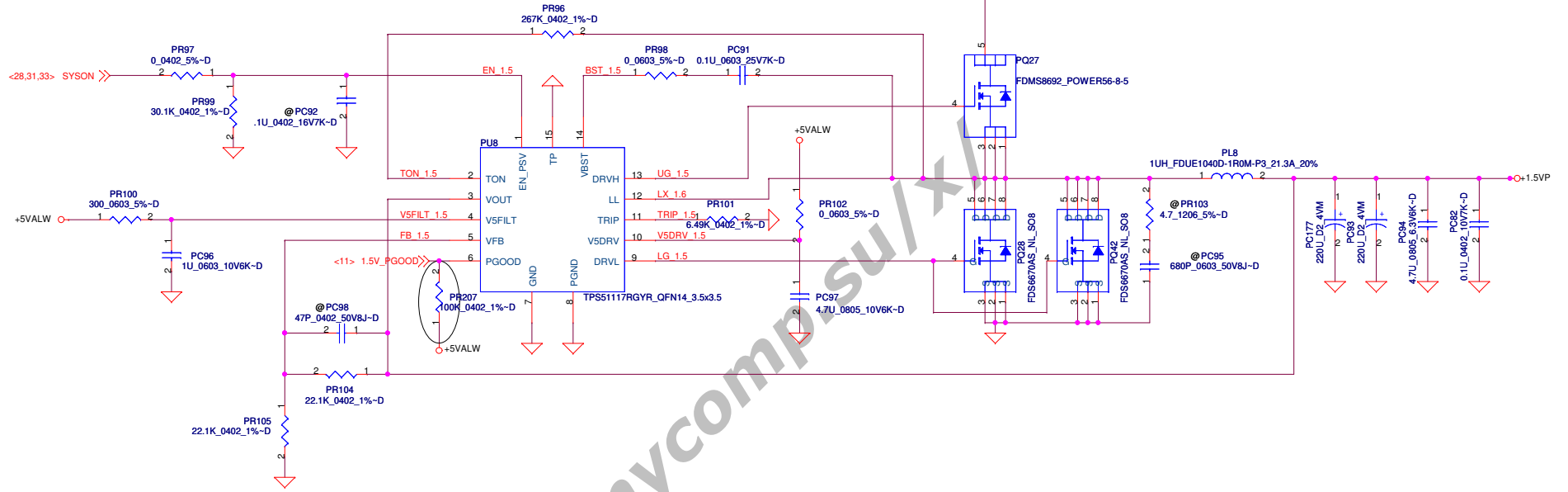


Compal Electronics, Inc.		
Title: +1.05V_VCCP/+1.8VSP		
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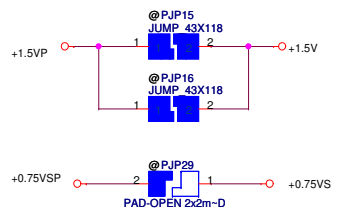
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1.5V
 Thermal Design Current=10.56A
 Peak Current=13.2A
 OCP_min=15.84A
 Fsw=298KHz

<Vo=1.5V> VFB=0.75V
 $V_o = V_{FB} * (1 + PR104/PR105) = 0.75 * (1 + 22.1K/22.1K) = 1.5V$



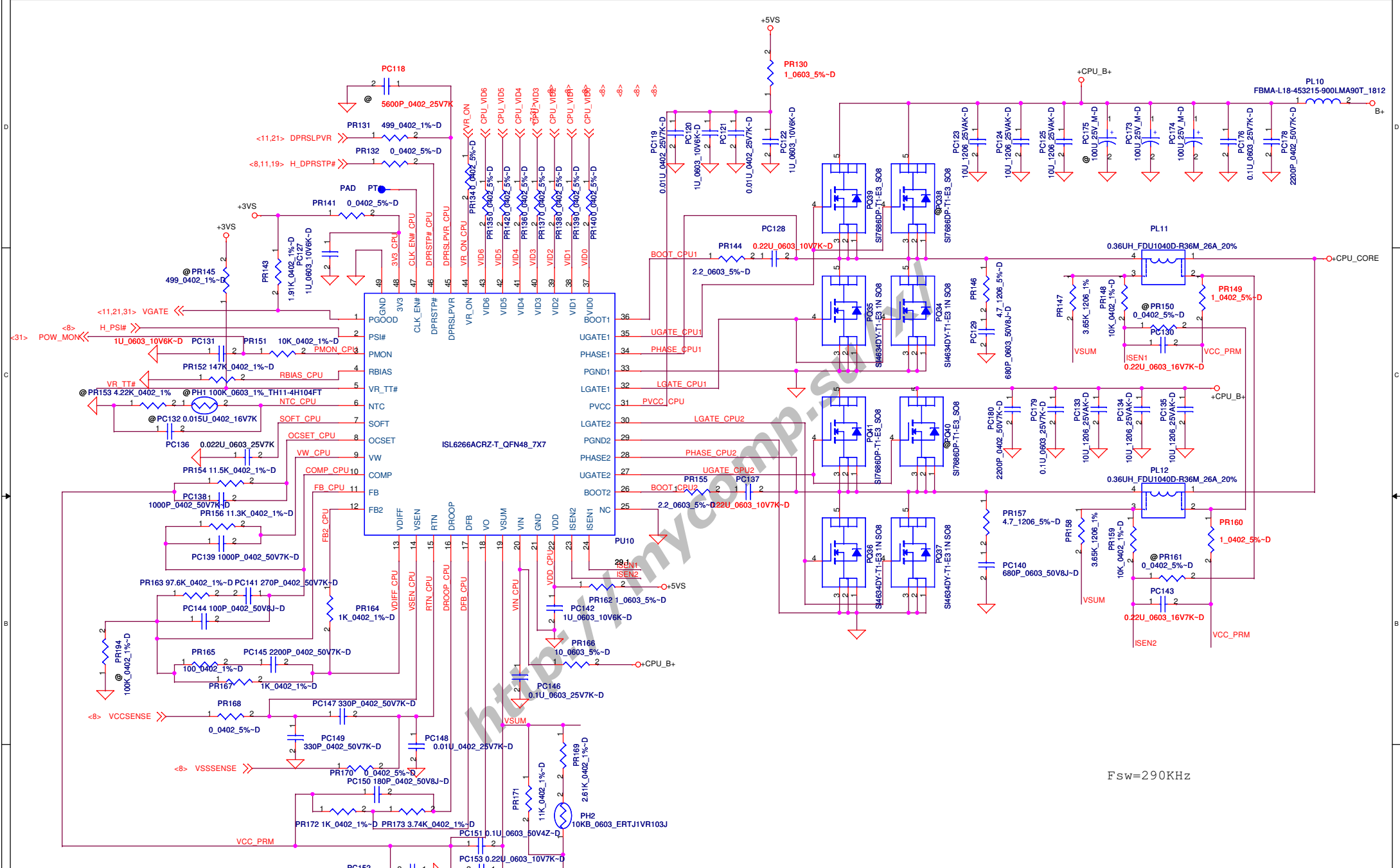
+0.75VSP
 Thermal Design Current:0.7A
 Peak current:1A
 $V_{out} = V_{DDQSNS} / 2 = 1.5V / 2 = 0.75V$



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		Compal Electronics, Inc.	
		Title +1.5VSP/+0.75VSP	
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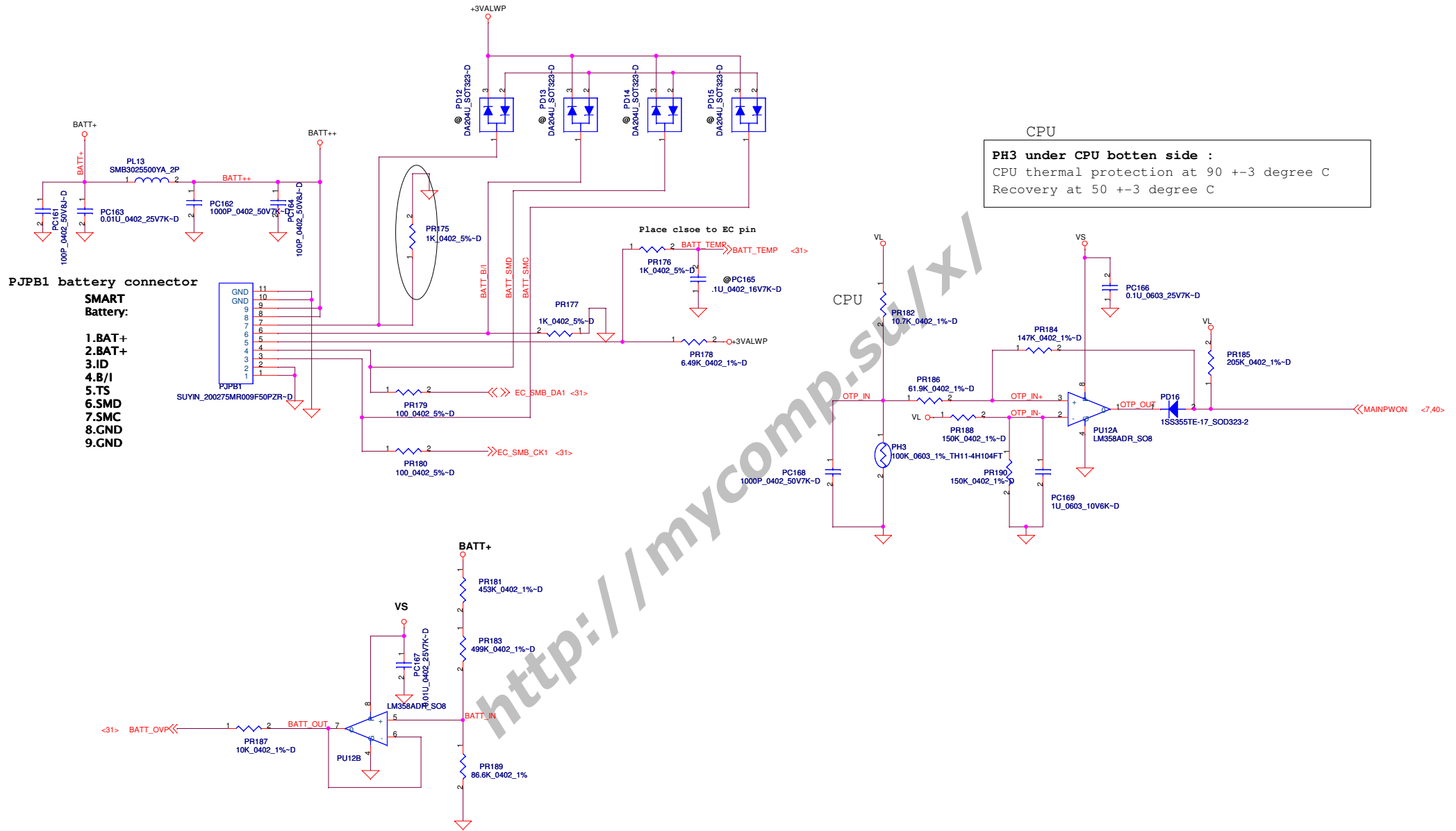


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	Compal Electronics, Inc.	
	Title CPU CORE	
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Battery Connect/OTP



CPU
PH3 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 50 +/-3 degree C

LI-3S :13.5V---BATT_OVP=1.126V
BATT_OVP=0.08338*BATT+

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Compal Electronics, Inc.		
BATTERY CONN		
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	06	Clock Generator	2009/03/03	Benson_Tung	Error connection of clock gne I2C.	Correct CLK_SMBDATA connect to U1.9 , CLK_SMBCLK connect to U1.10.	Rev02 (X01)
2	06	Clock Generator	2009/03/03	Benson_Tung	Error connection of CLK_PCIE_WPAN & CLK_PCIE_WPAN#	Correct WPAN CLK +/- signal of U1.	Rev02 (X01)
3	30	JCARD1	2009/03/03	COMPAL	1. Change JCARD1 pin 1 location to prevent cable twist. 2. Connect contact current rating is only 0.3 Ampere max.	1. Modify JCARD1 symbol 2. Add +5VALW pin count from 2 to 7 pins.	Rev02 (X01)
4	32	Keyboard	2009/03/03	Benson_Tung	Keyboard connector Pin 1 location is different with Keyboard module.	Correct keyboard pin 1 location to fit keyboard module.	Rev02 (X01)
5	32	Power share	2009/03/03	Benson_Tung	Power share didn't work.	Add power share schematic.	Rev02 (X01)
6	12	Cantiga (3 of 7)	2009/03/03	Benson_Tung	Error connection of LVDS CLK +/-.	1. Correct LVDS_ACLK+ connect to U4C.C40 2. Correct LVDS_ACLK- connect to U4C.C41 3. Correct LVDS_BCLK+ connect to U4C.A37 4. Correct LVDS_BCLK- connect to U4C.B37	Rev02 (X01)
7	33	DC/DC Interface	2009/03/03	Benson_Tung	Change DC to DC transfer of MOS parts	1. +3VALW to +3VS Ttransfer MOS change to U21 SI4800BDY-TI-E3 2. +5VALW to +5VS Ttransfer MOS change to U22 SI4800BDY-TI-E3 3. +1.5V to +1.5VS Ttransfer MOS change to Q45 SI4392DY-T1-E3	Rev02 (X01)
8	20	FFS	2009/03/03	Compal	Add FFS function	Add FFS circuit in page 20	Rev02 (X01)
9	4	Power Rail	2009/02/25	Bill_Huang	Correct error item.	Correct +3VS, +5VS Power consumption.	Rev02 (X01)
10	36	HDMI	2009/03/03	Benson_Tung	Error connection of Q200.3 and C1517.1 GND net name.	1. Change Q200.3 net form GND SIGNAL to GND. 2. Change C1517.1 net form GND SIGNAL to GND.	Rev02 (X01)
11	19-23	ICH9M	2009/03/04	Bill_Huang	Change ICH to consign P/N.	Change U6 P/N: form SA00002G11L to SA00002G12L.	Rev02 (X01)
12	35	CRT RGB EA	2009/03/10	Benson_Tung	CRT RGB signals EA failed on Rising / Falling time.	Change L31-L33 from SM01000AL00 (S SUPPRE_CHENG-HANN MBK1608301YZF 0603) to SM01000BP0L (BLM18BB050SN1D_0603-D)	Rev02 (X01)
13	35	CRT Diode	2009/03/03	Benson_Tung	CRT diode forward current is about 1Amp, need to change part to prevent damage.	Change D17 from SC1B411D010 (S DIO RB411DT146 SOT23) to SCSB491DA0L (S SCH DIO RB491D SC59-3 ROHM)	Rev02 (X01)
14	37 35 26	Display Port VGA / LVDS Sub woofer / Speaker AMP	2009/03/04	Jan_Chang	Change JDP1, JLVDS1 and JWOOFER1 symbol.	1. Update JDP1 symbol. 2. Change JLVDS1 symbol to JAE_FI-G40SB-VF25-DT 3. Change JWOOFER1 symbol to MOLEX_53398-0271-D	Rev02 (X01)
15	31 19 24	EC_KB926/BIOS/Reed SW ICH9M(1/5)_LAN,HD,SATA,LPC Gigabit LAN_RTL8111DL	2009/03/04	Benson_Tung	Meet Xtal EA spec.	1. Change C479,C481 from 15P_0402_50V8J to 22P_0402_50V8J 2. Change C217,C864 from 12P_0402_50V8J to 15P_0402_50V8J 3. Change C318 from 27P_0402_50V8J to 33P_0402_50V8J	Rev02 (X01)
16	25	HD Audio_IDT92HD73C	2009/03/04	Benson_Tung	1. SPK_MUTE# change to controlled by HP1_JD or HP2_JD. 2. Meet HP EA spec.	1. Add U108 OR gate. 2. Change C336, C337, C349, C350 , C354, C355 from 1U_0603 to 2.2U_0805.	Rev02 (X01)
17	27	Mini Card_WLAN/WWAN	2009/03/06	Compal	To supprot EC TX/RX debug card.	Change EC_TX_P80_DATA & EC_RX_P80_CLK connect to JWWAN1 pin 49 & 51	Rev02 (X01)
22	30	USB/Bluetooth/Camera	2009/03/06	Compal	To prevent antenna effect at E-SATA re-driver.	Add R1012 & R1013 place close U40 Pin2 & Pin3 Add R1014 & R1015 place close U40 Pin 21 & Pin22	Rev02 (X01)
23	32	PWROK/BTN/KB/Touch Pad	2009/03/06	Compal	Add powershare schematic.	Add powershare schematic.	Rev02 (X01)
24	33	DC/DC	2009/03/06	Compal	1. To fit power budget	1a. Change U21 & U22 from DMN3030LSS-13 to SI4800BDY 1b. Change U25 SI4800BDY to Q45 SI4329DY	Rev02 (X01)
25		Market / Capacitor	2009/03/06	Compal	Due to Janpan produce Y5V no more in the future.	change C133,C138,C144,C152,C163,C251,C255,C281,C425 from SE000009W0L to SE107475M0L	Rev02 (X01)
26	23	ICH9M(5/5)_POWER&GND	2009/03/06	Compal	ICH conect to ALW power rail have power wastage at S5 mode	Add MOSFET control circuit to reduce ICH power wastage at S5 mode.	Rev02 (X01)

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Compal Electronics, Inc.

EE PIR-1

Title: EE PIR-1

Size: Document Number
LA-5152P

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	24	Gigabit LAN_RTL8111DL	2009/03/06	Compal	1. Prevent B+_BIAS damage Q3 2. Correct +LAN_DVDD12 power name 3. Meet LAN EMI test.	1. Add R1006 (1.5M_0402) 2. Correct C302 & C303 power source from +LAN_VDD12 to +LAN_DVDD12 3. Pop C873 ~ C880 , SE07168AC0L(S CER CAP 6.8P 50V C NPO 0402)	Rev02 (X01)
28	35	VGA / LVDS	2009/03/06	Compal	1. LCD panel need to be turned backlight under this crisis recovery mode. 2. when FN+ D is pressed during POST, the LCD will perform the LCD BIST test and boot to PSA directly	add a gate to OR VGA_PWM and EC_PWM signals	Rev02 (X01)
28	21	ICH9M(3/5)_PM.GPIO	2009/03/06	Compal	Error net name PBTN_OUT#	Correct U6C.R3 net to PBTN_OUT#	Rev02 (X01)
29	4	Power Rail	2009/03/06	Compal	Correct +1.5V to +1.5VS.DC/DC Interface chip name	Form 4800BDY change to SI4392DY	Rev02 (X01)
30	25	HD Audio_IDT92HD73C	2009/03/11	Compal	Meet audio HP EA spec	1.C354,C355,C336,C337 change to 2.2uF 0805 size X7R 2.Add a series 2k ohm resistor between these caps and the maxim amp U10,U12., 3.At the pin of the maxim amp U10,U12 Pin 15 and U10,U12 Pin13 add a 220pF cap 0603 NPO to ground.	Rev02 (X01)
31	26	Speaker/Sub woofer AMP	2009/03/11	DELL	Gain setting to 20.6dB	1. C913,C914,C910,C909 form 6800P_0402_16V7K-D change to 2200P_0402_25V7K-D 2. R907,R902 100K_0402_1% to 280K 3. Delete C951,C952 0.015U_0402_16V7K part. 4.R900,R905 form 4.87K_0402 change to 43.2K_0402 5. U14 form MAX9736B change to MAX9736A 5.R901,R903,R906,R908 form 20K_0402 change to 25.5K_0402	Rev02 (X01)
32	34	Screws/LED/Switch	2009/03/11	ME	Modify MB drawing.	1. H2 change to NON-PTH 1.6mm. 2,. Delete H13 part	Rev02 (X01)
33	26 31 32	Speaker/Sub woofer AMP EC_KB926/BIOS/Reed SW PWROK/BTN/KB/Touch Pad	2009/03/11	EMC	Follow EMC request.	1. D20,D21 (PACDN042Y3R_SOT23-3) change to POP. 2. R330 (0_0402), C483 (0.1U_0402) change to POP. 3. Reserve ESD diode D1505 PJDLC05_SOT23-3 on touchpad 4. Change D1504 part to PJDLC05_SOT23-3.	Rev02 (X01)
34	29	ODD/SATA HDD	2009/03/11	ME	Follow ME request.	JODD1 form MOLEX_47639-4000_NR change to MOLEX_47639-3000_13P	Rev02 (X01)
35	26	Speaker/Sub woofer AMP	2009/03/11	COMPAL	Band-Pass Filtiter,fc=100 Hz, 500Hz, Av=1.45V/V	form MAX9737 change to MAX9736A. please see page 26	Rev02 (X01)
36	27	Display Port	2009/03/11	COMPAL	Meet HDMI test	1. R1518 0_1206 change to non-pop. 2. F1500 1.5A_6V_1206L150PR-D change to POP.	Rev02 (X01)
37	6 19 27 31	Clock Generator CK505 ICH9M(1/5)_LAN,HD,SATA,LPC Mini Card_WLAN/WWAN EC_KB926/BIOS/Reed SW	2009/03/13	Compal RF	Follow RF request.	RF reserve 1.C1531 part. CLK_14M_ICH need close U1 2.C1532 part. HDA_BITCLK_AUDIO need close U6 3.C1533 part.PCI_CLK need close U1 4.c1534 part. CLK_PCI_EC need close U1 5. C1535,C1536 part. Reserve 47 pF for +1.5V and +3V 6. C1537, C1538 part. Reserve 47 pF for +1.5V and +3V 7. Move R333 close to U19 and need reserve C1539 part.	Rev02 (X01)
38	27	USB/BlueTooth/Camera	2009/03/13	COMPAL	Delete E-SATA by-pass R.	Delete R1012,R1013,R949,R950,R951,R952,R1014,R1015 part .	Rev02 (X01)
39	25	HD Audio_IDT92HD73C	2009/03/13	COMPAL	Modify Audio control circuit.	please see page 25 about U46,U42,U108,U48,U47,U41,Q48 parts.	Rev02 (X01)
40	33	DC/DC Interface	2009/03/13	COMPAL	For reduce power consumption	1.R344 change to 470K. 2.R346 change to 2M.	Rev02 (X01)
41	31	EC_KB926/BIOS/Reed SW	2009/03/14	COMPAL	correct SPI_CLK_R non_pop parts.	R330,C483 change to non_pop.	Rev02 (X01)
42	36	HDMI	2009/03/16	COMPAL	Meet HDMI chip spec. X7616831L04 ALT. GROUP PARTS S-(SA00002C610) KAT00	R1500 change to pop part..	Rev02 (X01)
43	11	Cantiga (2 of 7)	2009/04/27	COMPAL	Correct HDMI CLK/DATA part B and C connect	DDPC_CTRLCOK should be connecting HDMI_C_CLK. =>Port C DDPC_CTRLDATA should be connecting HDMI_C_DATA. =>Port C SDVO_CTRLCLK should be connecting HDMI_B_CLK. =>Port B SDVO_CTRLDATA should be connecting HDMI_B_DATA. =>Port B	Rev03 (X02)

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44	36	HDMI Conn	2009/04/27	COMPAL	Follow EMI request of HDMI	L1504,L1505, L1506, L1507 parts change to DLW21SN900HQ2L	Rev03 (X02)
45	37	Display Port	2009/04/27	COMPAL	Follow INTEL Design Guide DP AUX circuit.	DPB_AUX_SW need connect R1553 (100kohm) to pull down. DPB_AUX#_SW need connect R1554 (100Kohm) to pull up +3VS.	Rev03 (X02)
46	33	DC/DC Interface	2009/04/28	COMPAL	Delete +3V_WLAN discharge circuit.	Delete +3V_WLAN discharge circuit.	Rev03 (X02)
47	28	Mini Card_WPAN / Express	2009/04/28	COMPAL	Chagne JEXP1 symbol.	JEXP1 change to TAITW_PXPXAE-000LBS2ZZ4N0_NR part.	Rev03 (X02)
48	34	Screws/LED/Switch	2009/04/29	COMPAL	Original H1 is fan alignment pin , but now cancel this function.	Delete H1 part.	Rev03 (X02)
49	25	HD Audio_IDT92HD73C	2009/04/29	COMPAL	Change EAPD# pull up to (+3VALW).	Change R1549.1, U46.5 and U47.5 to +3VALW power	Rev03 (X02)
50	23	ICH9M(5/5)_POWER&GND	2009/04/29	COMPAL	Change +ICH_V5REF_RUN and SUS resistance	R233,R234 form 10_0402_5% change to 100_0402_5%	Rev03 (X02)
51	32	PWROK/BTN/KB/Touch Pad	2009/04/30	COMPAL	follow EMC request.	1.Change L77 and L78 from 120 ohms to 600 ohms bead. 2. Implement ESD diode on cap sensor D1504 PJDLC05_SOT23-3 3. Implement ESD diode on TP_CLK and TP_DATA for touchpad D1505 PJDLC05_SOT23-3 4. Reserve PES24VS2UT_SOT23-3 ESD diode for speaker connector of D20, D21	Rev03 (X02)
52	23 24 35	ICH9M(5/5)_POWER&GND Gigabit LAN_RTL8111DL CRT / LVDS CONN	2009/04/30	COMPAL	Change to PSL parts	D2,D3,D4,D5,D6,D7,D19 form SC1H751H01L S DIO CH751H-40PT SOD-323 Change to SCS0340L01L SDMK0340L-7-F_SOD323-2-D	Rev03 (X02)
53	07 30	Penryn(1/3)-AGTL+/ITP-XDP USB/BlueTooth/Camera	2009/04/30	COMPAL	C19,C21,C463,C935 form S CER CAP 10U 16V Z F(Y5V) 1206 H1.15 change to SE053106Z8L S CER CAP 10U 10V Z Y5V0805 H1.25		Rev03 (X02)
53	07 30	Penryn(1/3)-AGTL+/ITP-XDP USB/BlueTooth/Camera	2009/04/30	COMPAL	Modify DC to DC circuit.	Modify +3VALW to +3VS and +5VALW to +5VS circuit.	Rev03 (X02)
54	23	ICH9M (5/5)	2009/05/01	COMPAL	Reduce ICH power consumption at S5 mode.	Populate Q47 and non-populate R1022	Rev03 (X02)
55	30	USB/BlueTooth/Camera	2009/05/01	COMPAL	Change E-SATA Output Swing Control TO 1.2x	1.Non-populate R958, R959 2. R953 change to 390 ohm.	Rev03 (X02)
56	30	USB/BlueTooth/Camera	2009/05/01	COMPAL	Solve USB Power Share fail issue.	Swap GPIO for USB_DET_DELAY# and EC_SPK_HP_MUTE#.	Rev03 (X02)
57	31	EC_KB926/BIOS/Reed SW	2009/05/04	COMPAL	Support S5 Power on when CRT insert	Pull-up MSEN# from +3VS to +3VALW	Rev03 (X02)
58	31	EC_KB926/BIOS/Reed SW	2009/05/04	COMPAL	FFS alert signal will change to other GPIO. Because original PIRQH is by USB controller used.	FFS change int to PIRQ setting from PIRQH to PIRQE	Rev03 (X02)
59	25	HD Audio_IDT92HD73C	2009/05/04	COMPAL	Change package form 0603 to 0402.	C1527, C1528, C1529, C1530 Change to 270P_0402_50V7K--D	Rev03 (X02)
60	35	VGA / LVDS	2009/05/05	COMPAL	Add MOSFET circuit for LVDS converter power		Rev03 (X02)
61	24	ICH9M(5/5)_POWER&GND	2009/05/06	COMPAL	Modify +3VALW_S5_ICH circuit.	R972 form 470Kohm change to 300Kohm. R973 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
62	35	VGA / LVDS	2009/05/06	COMPAL	Modify Keyboard back light circuit.	R928 form 470Kohm change to 300Kohm. R931 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
63	24	Gigabit LAN_RTL8111DL	2009/05/07	COMPAL	Modify LAN_IO power circuit.	R236 form 470Kohm change to 300Kohm. R1540 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
64	26	Speaker/Sub woofer AMP	2009/06/04	COMPAL	For Part source	C901, C902, C903, C916, C918, C977 form SE00000NZ0L (S CER CAP 22U 25V K X7R 1210 H2.5) change to SE00000GF8L (S CER CAP 22U 25V K X5R 1210 H2.5)	Rev10 (A00)
65	30	USB/BlueTooth/Camera	2009/06/04	COMPAL	due to E-SATA connector doesn't support E-SATA detect function.	De_pop SB00000960L (S TR SSM3K7002FU 1N SC70-3) Location: Q11	Rev10 (A00)

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66	32	PWROK/BTN/KB/Touch Pad	2009/06/04	Compal	Change to DELL AVL Part	Change PN: SCA00000A00 (S ZEN ROW PJDLCO5 3P C/A SOT23) to SCA00000J0L (S ZEN ROW PESD5V2S2UT 3P C/A SOT23 ESD) Location: D1504, D1505	Rev10 (A00)
67	25	HD Audio_IDT92HD73C	2009/06/04	Compal	Solve S0 to S3 pop noise of HP.	R1549 change to De_POP.	Rev10 (A00)
68	12	CANTIGA((3/7)-VGA/LVDS/TV	2009/06/04	Compal	CRT_HSYNC and CRT_VSYNC net name error	1. R116.1 net change to CRT_HSYNC_R 2. R117.1 net change to CRT_VSYNC_R	Rev10 (A00)
69	36	HDMI	2009/06/04	Compal	Cancel solder mask of by pass 0 ohm	1. Cancel solder mask R1517,R1515,R1514,R1507,R1509,R1508,R1522,R1510 parts. 2. Cancel solder mask R1521 part. 3. Cancel solder mask L26,L71,L72,L27 parts.	Rev10 (A00)
70	31	EC_KB926/BIOS/Reed SW	2009/06/04	Compal	Change Board ID	R312 change to 33Kohm	Rev10 (A00)
71			2009/06/04	Compal	Short by-pass 0 ohm	short parts of R2,R4,R3,R5,R6,R7,R8,R10,R12,R42,R43,R16,R17,R18,R19,R21,R23,R26,R28,R31,R33,R35,R37,R40,R39,R14,R15,R44,R99,R94,R134,R1004,R884,R235,R942,R248,R250,R285,R911,R912,R913,R914,R291,R918,R921,R919,R920,R915,R916,R917,R922,R923,R924,R925,R292,293,R292,R293,R294,R298,R295,R296	Rev10 (A00)
72	26	Speaker/Sub woofer AMP	2009/06/08	Compal	Main speaker AMP gain setting to 13dB	1. Change C908,C912 form 0.22uF to 0.1uF. 2. Change R903,R908 form 25.5Kohm to 16.5Kohm 3. Change R901,R906,R902,R907 form 280Kohm to 182Kohm 4. Change R904,R909 form 16.9ohm to 17.8Kohm 5. Change R900,R905 form 43.2K ohm to 11Kohm	Rev10 (A00)
73	26	Speaker/Sub woofer AMP	2009/06/08	Compal	Modify Main speaker AMP SHDN and mute # control circuit	1. Add D1507, R1558, C1547 diode and RC delay time of MUTE# pin.	Rev10 (A00)
74	30	USB/BlueTooth/Camera	2009/06/08	Compal	Solve E-SATA re-driver issue	Chagne U40 from SA00002D80L (S IC PI2EQX3201BZFEX TQFN 36P) to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)	Rev10 (A00)
75	25	HD Audio_IDT92HD73C	2009/06/08	Compal	Support unboot pc-beep sound function	Pop R1549	Rev10 (A00)
76	27	Mini Card_WLAN/WWAN	2009/06/15	Compal	delete short trace of jump	Delete R1010,R1011,R911,R912 pin1 and pin2 connect trace.	Rev10 (A00)

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01	40	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +5VALW OCP to 13.56A	Change PR68 from P/N:SD03429438L (294K +-1% 0402) to SD03433238L (332K +-1% 0402)	X01
02	40	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +3VALW OCP to 14.26A	Change PR69 from P/N: SD03424938L (249K +-1% 0402) to SD03434038L (340K +-1% 0402)	X01
03	41	+1.05V_VCCP/ +1.8VSP	01/22	Compal Mike	Setiing +1.05V_VCCP OCP to 23A	Change PR81 from P/N: SD03480618L (8.06K +-1% 0402) to SD03493118L (9.31K +-1% 0402)	X01
04	42	+1.5VSP/+0.75VSP	01/22	Compal Mike	Setiing +1.5VSP OCP to 15.84A	Change PR101 from P/N: SD03413728L (13.7K +-1% 0402) to SD03410528L (10.5K +-1% 0402)	X01
05	38	DCIN/Precharger	01/22	Compal Mike	Common circuit design modify	Change PR10 from P/N: SD00103308L (33 +-5% 1206) to SD011680A8L (68 +-5% 1206) Add PR208 SD011680A8L (68 +-5% 1206) parallel with PR10	X01
06	42	+1.5VSP/0.75VSP	01/22	Compal Mike	HW need to use +1.5VSP PGOOD signal,so need to add a pull high resister.	Add PR207 SD03410038L (100K +-1% 0402) between PU8 pin6 and PR97 pin 2.	X01
07	46	Charger	02/09	Compal Mike	Take off Cells selector function.	Populate PR88,take off PR37 and PQ10,change PR175 from 47K to SD02810018L(1K +-5% 0402)	X01
08	43	CPU_CORE	02/24	Compal Mike	Change CPU_CORE low-side MOSFET	Change PQ34,PQ35,PQ36,PQ37 from (SI4430BDY-T1-E3 1N SO-8) to SB00000DA00(SI4634DY-T1-E3 1N SO8)	X01
09	43	CPU_CORE	02/24	Compal Mike	HW don't need to use VR_TT# signal,so depopulate pull high resister.	Depopulate PR145 SD03449908L(499 +-1% 0402)	X01
10	43	CPU_CORE	02/24	Compal Mike	Change input cap from X7R(85°C) to X6S(105°C)	Change PC123,PC124,PC125,PC133,PC134,PC135 from (10U 25V M X5R1206 H1.6) to SE153106K8L(10U 25V K X6S 1206 H1.6)	X01
11	40	+3VALWP/+5VALWP	02/24	Compal Mike	Take off Manufacturer:COMPOSTAR from PC64	Change PC64 from P/N: SE080224K8L (.22U 10V K X7R 0603) to SE080224M8L (.22U 10V K X7R 0603)	X01
12	44	BATTERY CONN	02/24	Compal Mike	Take off non-PSL Manufacturer:Panjit	Change PQ45,PQ46 from P/N: SB000006800 (2N7002W T/R7 1N SOT-323) to SB00000B30L (PMF3800SN 1N SC70-3)	X01
13	39	Charger	02/24	Compal Mike	Take off non-Lead Free material.	Change PR29 from P/N: SD021200D0L (S RES 1W .02 +-1% 2512) to SD000001F0L (S RES 1W .02 +-1% 2512 50PPM/C)	X01
14	41	+1.05V_VCCP	02/24	Compal Mike	Change choke setting	Change PL6 from SH00000BQ0L (2.2UH +-20% MPLC1040L2R2 11A) to SH000009U00 (1UH +-20% FDUE1040D-1ROM=P3 21.3A)	X01
15	40	+3VALWP/+5VALWP	02/24	Compal Mike	Change choke reated current from 11A to 14.2A	Change PL4,PL5 from SH00000BQ0L (2.2UH +-20% MPLC1040L2R2 11A) to SH00000CG0L (2.2UH 20% FDVE1040-2R2M=P3 14.2A)	X01
16	38	DCIN / Precharge	03/03	Compal Antony	Prevent diode breakdown from battery inrush current	Change PD3 from SCS00002G00 to SC11N414880	X01

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17	38	DCIN / Precharge	03/03	Compal Antony	Change part number to L-end	Change PD4 part number from SC1A204U000 to SC1A204U00L	X01
18	40	+3VALWP/+5VALWP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR68 from 332K ohm to 205K ohm	X01
19	40	+3VALWP/+5VALWP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR69 from 340K ohm to 243K ohm	X01
20	41	+1.05V_VCCP/ +1.8VSP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR81 from 9.31K ohm to 7.87K ohm	X01
21	41	+1.05V_VCCP/ +1.8VSP	03/03	Compal Antony	Stabilize output voltage	Add PC83 220uF Capand Reserve PC99 Cap space to output	X01
22	42	+1.5VSP/+0.75VSP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR101 from 10.5K ohm to 6.49K ohm	X01
23	43	CPU_CORE	03/03	Compal Antony	To avoid noise	Add PC176、PC179 0.1uF Cap to +CPU_B+	X01
24	43	CPU_CORE	03/03	Compal Antony	To avoid noise	Add PC178、PC180 2200pF Cap to +CPU_B+	X01
25	43	CPU_CORE	03/03	Compal Antony	Reserve space for load line shift control	Reserve PR194 space	X01
26	43	CPU_CORE	03/16	Compal Antony	To improve transient response	Change PC151 from 0.068uF to 0.1uF	X01
27	43	CPU_CORE	03/16	Compal Antony	Let difference of CPU Load Line and Spec smaller than 2mV	Change PR173 from 3.57K ohm to 3.74K ohm	X01
28	44	BATTERY CONN	03/16	Compal Antony	Disable Hardware CPU OTP circuit	Reserve PQ45、PQ46、PR199、PR200 space	X01
29	39	Charger	03/20	Compal Antony	Change 65W CP setting	Changer PR89 from PR89 from 143K ohm to 97.6K ohm	X01
30	41	+1.05V_VCCP/ +1.8VSP	03/20	Compal Antony	For phash margin improved	Add PC87 1000pF capacitor between PU13 pin6 and pin7	X01
31	41	+1.05V_VCCP/ +1.8VSP	03/20	Compal Antony	For phash margin improved	Add PC126 10uF capacitor between PU13 pin6 and GND	X01
32	39	Charger	05/06	Compal Antony	TI FAE request	Reserve PQ26,PD19,PD20,PC203,PR115,PR133 space	X02

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33	39	Charger	05/06	Compal Antony	slove PQ5 design margin issue	Change PQ4,PQ5,PQ7 from FDS4435 to FDS6675 (SB966750080)	X02
34	43	CPU_CORE	05/06	Compal Antony	Montavina platform design	Change PC136 from 15nF to 22nF	X02
35	39	Charger	05/06	Compal Antony	TI FAE request	Reserve PQ26,PD19,PD20,PC203,PR115,PR133,PC25 space	X02
36	39	Charger	06/04	Compal Antony	TI FAE request	Delete PQ26,PD19,PD20,PC203,PR115,PR133	X03
37	39	Charger	06/04	Compal Antony	TI request to reserve protection circuit	Reserve PR90 0ohm , PR37 0ohm , PC100 space ,PC25 0.022uF ,PC20 change to 0603 size	X03
38	39	Charger	06/04	Compal Antony	Recover a correct component	recover correct component PR89 to 97.6K ohm	X03
39	38	DCIN/Precharge	06/04	Compal Antony	DELL command	Change PQ2 from SB502060000 (RHU002N06_SOT323-3) to SB50301008L (FDV301N 1N SOT23-3)	X03

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