Model Name: KAT00 UMA
PCB NO: LA-5152P
BOM P/N: 43169631L01

Compal Confidential

Schematic Document

POITIER Montevina

2008 / 06 / 15 Rev:1.0

MB PCB

Part Number	Description
DA80000E510	PCB 080 LA-5152P REV1 UMA M/B

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Title: Cover Sheet

Size: | Document Number: LA-5152P | Rev: A00

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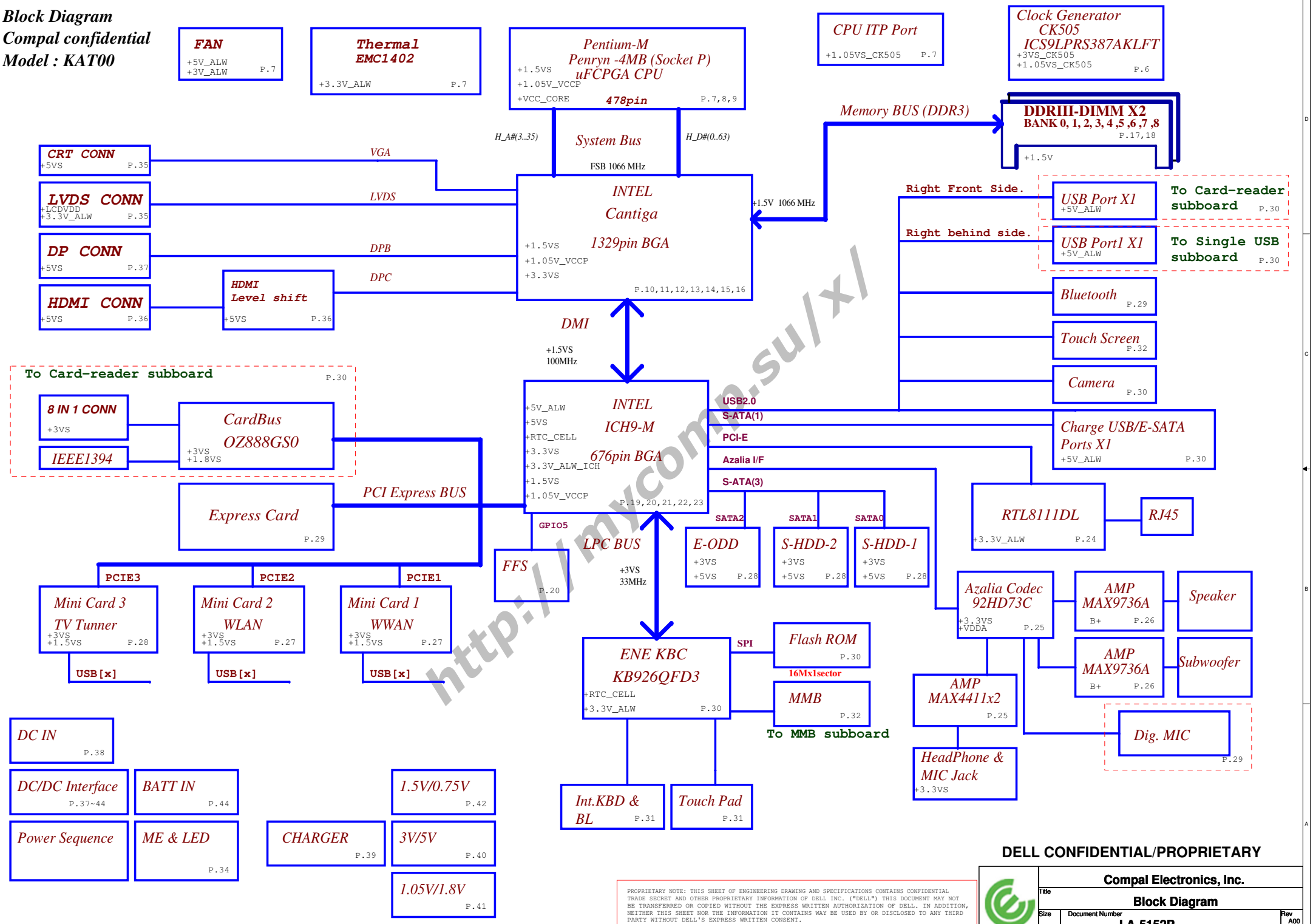
Block Diagram
Compal confidential
Model : KAT00



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Title	Block Diagram
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +VCCP +0.75VS +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

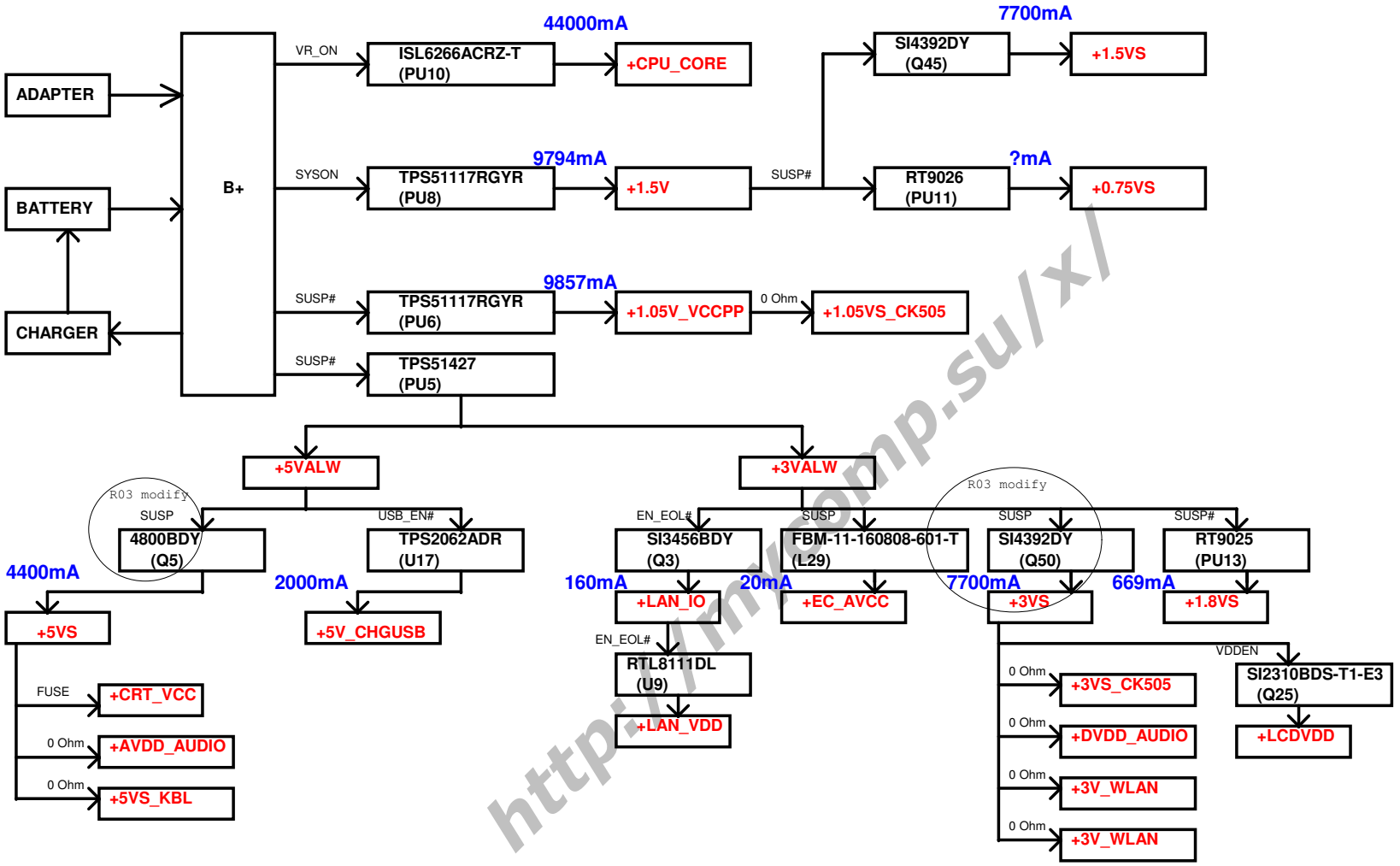
@ : means just reserve , no build

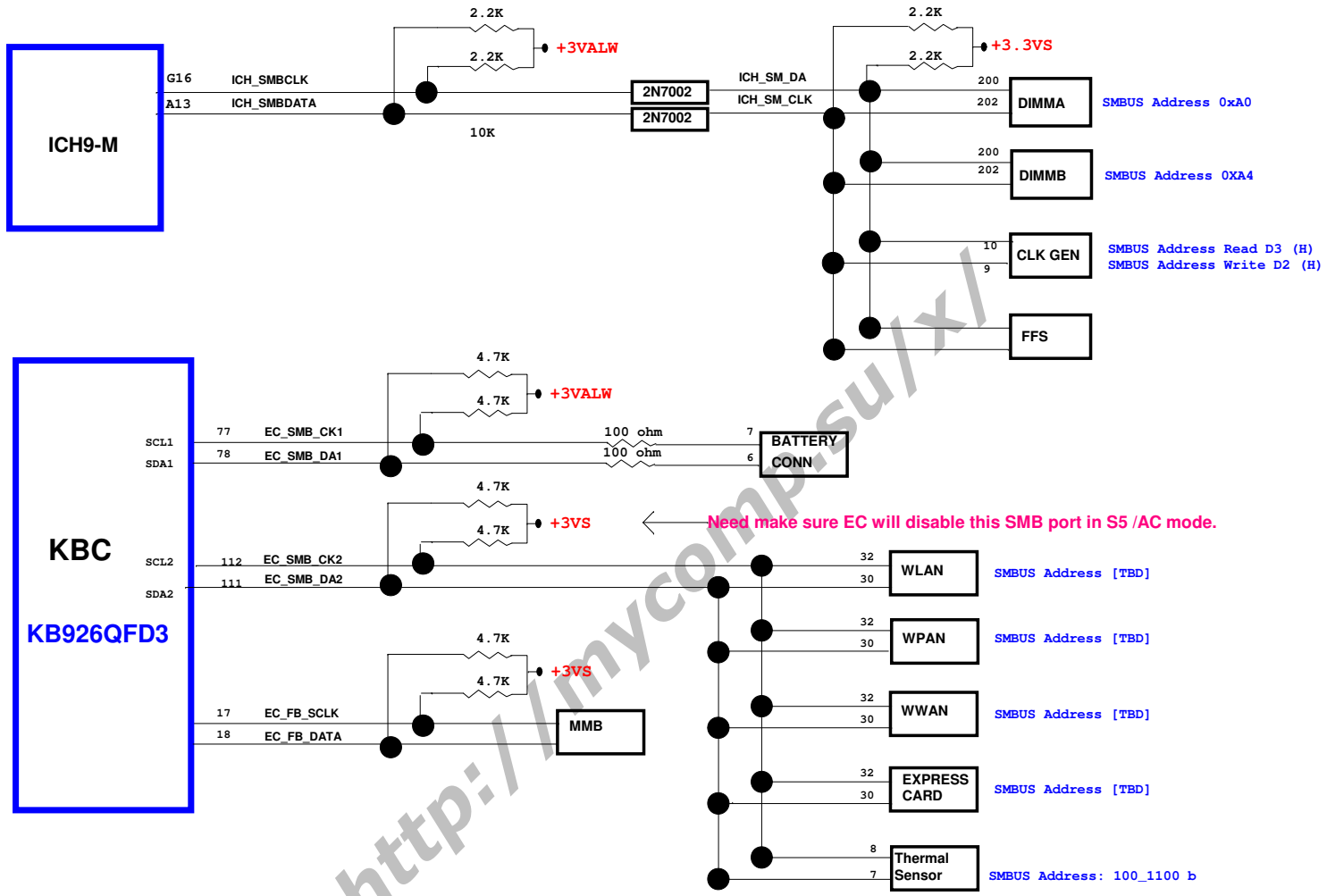
DEBUG@ : means just reserve for debug.

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

SATA Port	Device
0	JSATA2
1	JSATA1
2	JESA1
3	JODD

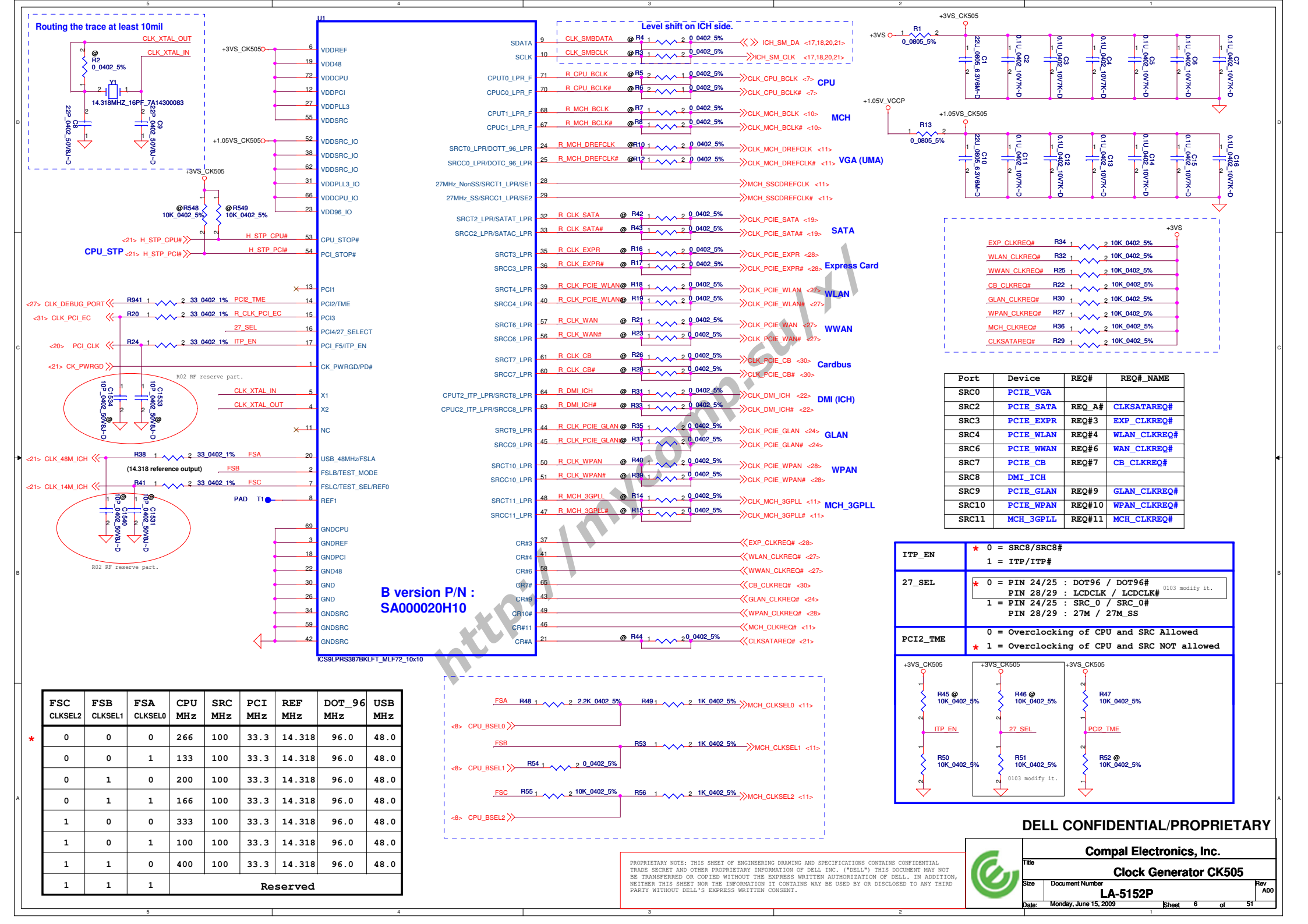
PCIE Port	Device
1	JWWAN1
2	JWLAN1
3	JWPAN1
4	Reader/BD (OZ888)
5	JEXP1
6	RTL8111DL





I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010



Port	Device	REQ#	REQ#_NAME
SRC0	PCIE_VGA		
SRC2	PCIE_SATA	REQ_A#	CLKSATAREQ#
SRC3	PCIE_EXPR	REQ#3	EXP_CLKREQ#
SRC4	PCIE_WLAN	REQ#4	WLAN_CLKREQ#
SRC6	PCIE_WWAN	REQ#6	WAN_CLKREQ#
SRC7	PCIE_CB	REQ#7	CB_CLKREQ#
SRC8	DMI_ICH		
SRC9	PCIE_GLAN	REQ#9	GLAN_CLKREQ#
SRC10	PCIE_WPAN	REQ#10	WPAN_CLKREQ#
SRC11	MCH_3GPLL	REQ#11	MCH_CLKREQ#

ITP_EN	* 0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	* 0 = PIN 24/25 : DOT96 / DOT96# PIN 28/29 : LCDCLK / LCDCLK# (0103 modify it.) 1 = PIN 24/25 : SRC_0 / SRC_0# PIN 28/29 : 27M / 27M_SS
PCI2_TME	0 = Overclocking of CPU and SRC Allowed * 1 = Overclocking of CPU and SRC NOT allowed

	FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
*	0	0	0	266	100	33.3	14.318	96.0	48.0
	0	0	1	133	100	33.3	14.318	96.0	48.0
	0	1	0	200	100	33.3	14.318	96.0	48.0
	0	1	1	166	100	33.3	14.318	96.0	48.0
	1	0	0	333	100	33.3	14.318	96.0	48.0
	1	0	1	100	100	33.3	14.318	96.0	48.0
	1	1	0	400	100	33.3	14.318	96.0	48.0
	1	1	1	Reserved					

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Title: Clock Generator CK505

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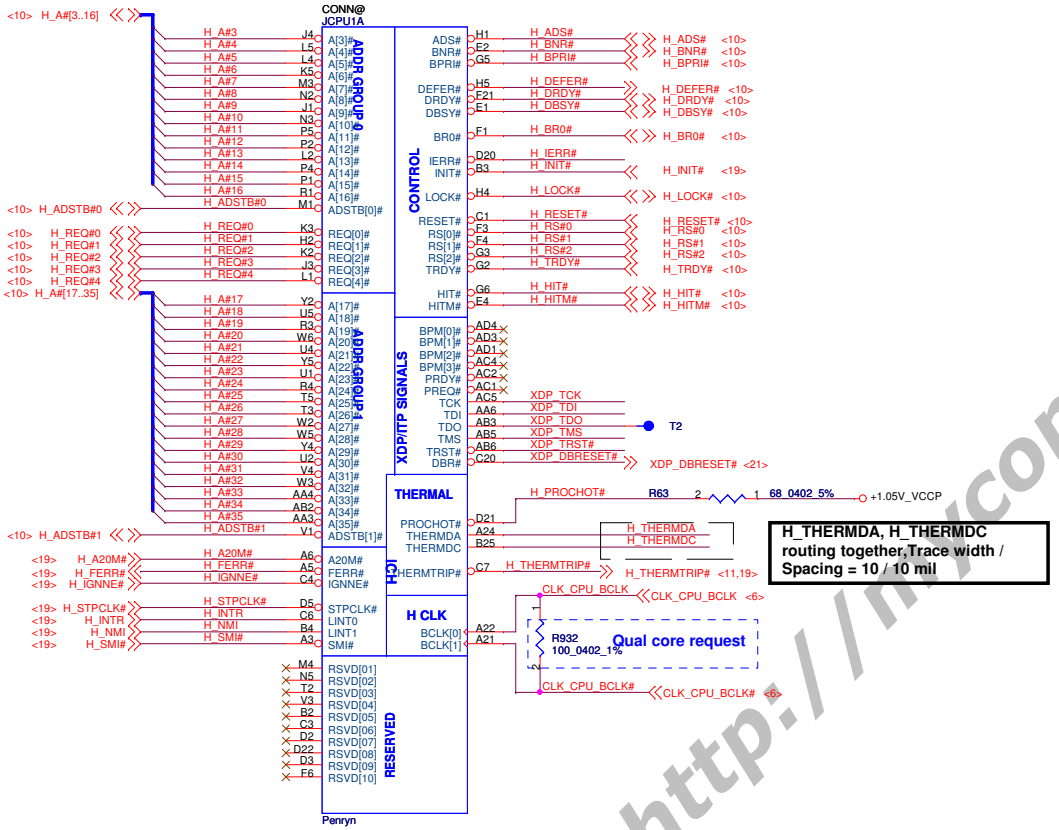
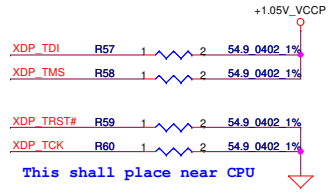
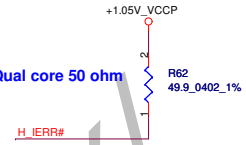


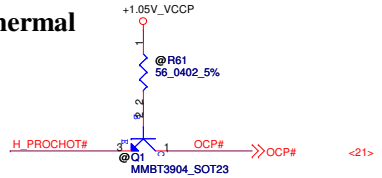
XDP / ITP



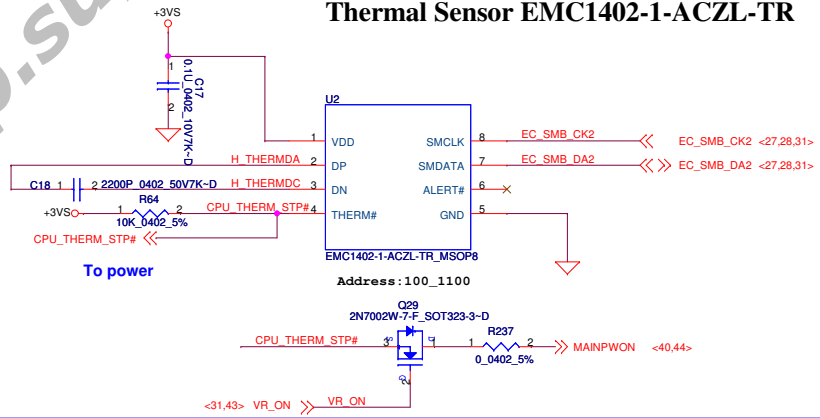
Control



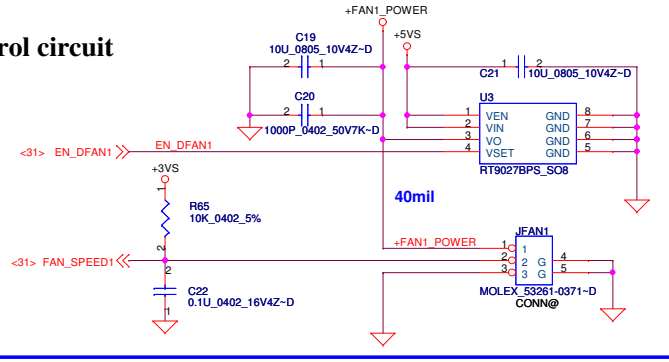
Thermal



Thermal Sensor EMC1402-1-ACZL-TR



FAN Control circuit



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Title	Penryn(1/3)-AGTL+/ITP-XDP
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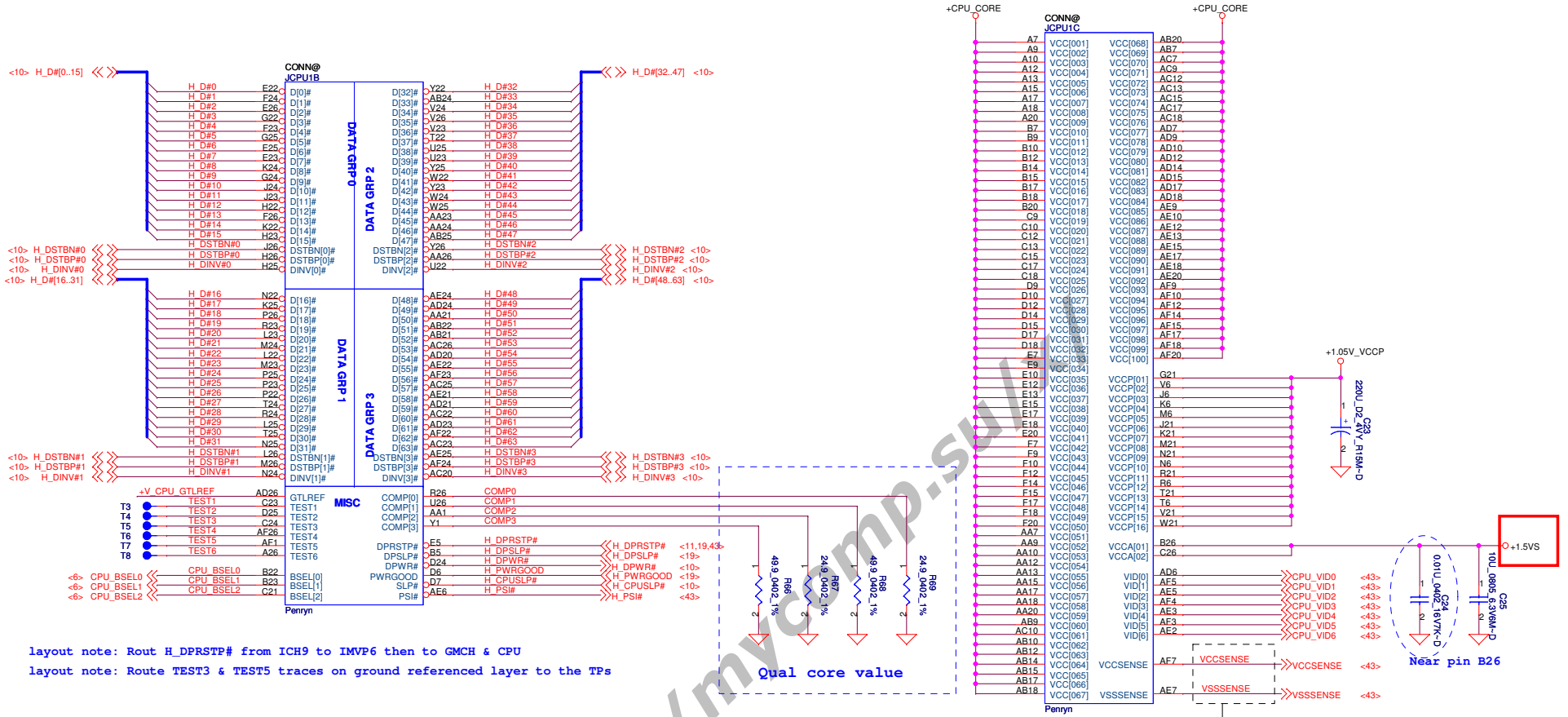

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

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Title: Penryn(2/3)-AGTL+/ITP-XDP

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High Frequence Decoupling

10uF 0805 X5R -> 85 degree.

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Title	Penryn(3/3)-AGTL+/ITP-XDP
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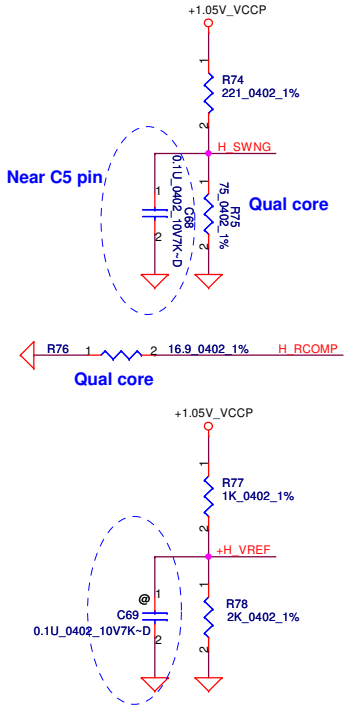
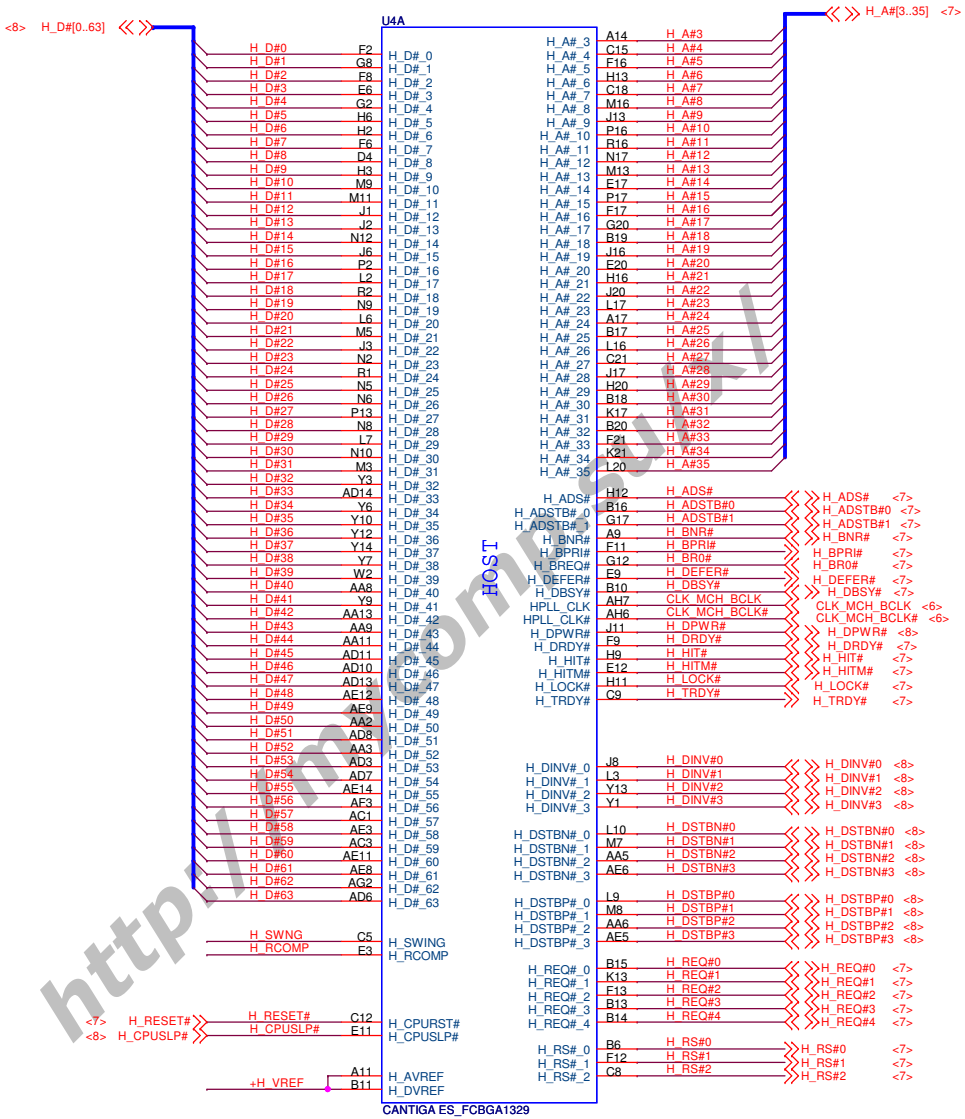
Layout Note :
H_RCOMP / H_VREF / H_SWNG
Trace width and spacing is 10 / 20



H_RCOMP Dual core 24.9 ohm_1% pull down
Qual core 16.9 ohm_1% pull down
H_SWNG Dual core 100 ohm_1% pull down
Qual core 75 ohm_1% pull down



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Title: Cantiga(1 of 7)

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CFG

@R79 2.21K 0402 1% CFG5
@R85 2.21K 0402 1% CFG6
@R80 2.21K 0402 1% CFG7
@R86 2.21K 0402 1% CFG9
@R81 2.21K 0402 1% CFG16

CFG[5:16] have internal pullup

+3VS
@ R87 4.02K 0402 1% CFG19
@ R88 4.02K 0402 1% CFG20

CFG[19:20] have internal pulldown

Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Defult)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	Digital Display Port Concurrent Operation	Low=Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present

PM

+3VS R96 10K_0402_5% PM_EXTTS#0
+3VS R97 10K_0402_5% PM_EXTTS#1
<21,31> ICH_PWROK R99 0_0402_5% PM_PWROK_R
<21,31,43> VGATE @R100 0_0402_5%
<20,27,30,31> PLT_RST# R102 100_0402_5% PLT_RST#_NB

@C957 0.1U_0402_10V7K~D H_DPRSTP#
Reserve for CPU, reference HPB

U4B

RSVD: T10 M36 RSVD1; T11 N36 RSVD2; T12 R33 RSVD3; T20 T33 RSVD4; T21 AH9 RSVD5; T22 AH10 RSVD6; T23 AH12 RSVD7; T13 AH13 RSVD8; T24 K12 RSVD9; T14 AL34 RSVD10; T25 AK34 RSVD11; T15 AN35 RSVD12; T26 AM35 RSVD13; T27 T24 RSVD14; T28 B31 RSVD15; T16 B2 RSVD16; T17 M1 RSVD17; T18 AY21 RSVD20; T29 BG23 RSVD22; T19 BF23 RSVD23; T30 BH18 RSVD24; T31 BF18 RSVD25

DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 AP24 M_CLK_DDR0 <17>; SA_CK_1 AT21 M_CLK_DDR1 <17>; SB_CK_0 AV24 M_CLK_DDR2 <18>; SB_CK_1 AU20 M_CLK_DDR3 <18>; SA_CK#_0 AR24 M_CLK_DDR#0 <17>; SA_CK#_1 AR21 M_CLK_DDR#1 <17>; SB_CK#_0 AU24 M_CLK_DDR#2 <18>; SB_CK#_1 AV20 M_CLK_DDR#3 <18>; SA_CKE_0 BC28 DDR_CKE0_DIMMA <17>; SA_CKE_1 AY28 DDR_CKE1_DIMMA <17>; SB_CKE_0 AY36 DDR_CKE2_DIMMB <18>; SB_CKE_1 BB36 DDR_CKE3_DIMMB <18>; SA_CS#_0 BA17 DDR_CS0_DIMMA# <17>; SA_CS#_1 AY16 DDR_CS1_DIMMA# <17>; SB_CS#_0 AV16 DDR_CS2_DIMMB# <18>; SB_CS#_1 AR13 DDR_CS3_DIMMB# <18>; SA_ODT_0 BD17 M_ODT0_DIMMA <17>; SA_ODT_1 AY17 M_ODT1_DIMMA <17>; SB_ODT_O BF15 M_ODT2_DIMMB <18>; SB_ODT_1 AY13 M_ODT3_DIMMB <18>; SM_RCOMP BG22 SMRCOMP; SM_RCOMP# BH21 SMRCOMP#; SM_RCOMP_VOH BF28 SMRCOMP_VOH; SM_RCOMP_VOL BH28 SMRCOMP_VOL; SM_VREF AV42 +V_DDR_MCH_REF; SM_PWROK AR36 SM_PWROK; SM_RCOMP BF17 R90 499_0402_1%; SM_DRAMRST# BC36 DDR3_DRAMRST# <17,18>

CLK DDR CLK/ CONTROL/ COMPENSATION: DPLL_REF_CLK B38 CLK_MCH_DREFCLK <6>; DPLL_REF_CLK# A38 CLK_MCH_DREFCLK# <6>; DPLL_REF_SSCLK E41 MCH_SSCDREFCLK <6>; DPLL_REF_SSCLK# F41 MCH_SSCDREFCLK# <6>; PEG_CLK F43 CLK_MCH_3GPLL <6>; PEG_CLK# E43 CLK_MCH_3GPLL# <6>

Reserve for UMA

DMI: DMI_RXN_0 AE41 DMI_MRX_ITX_N0 <22>; DMI_RXN_1 AE37 DMI_MRX_ITX_N1 <22>; DMI_RXN_2 AE47 DMI_MRX_ITX_N2 <22>; DMI_RXN_3 AH39 DMI_MRX_ITX_N3 <22>; DMI_RXP_0 AE40 DMI_MRX_ITX_P0 <22>; DMI_RXP_1 AE38 DMI_MRX_ITX_P1 <22>; DMI_RXP_2 AE48 DMI_MRX_ITX_P2 <22>; DMI_RXP_3 AH40 DMI_MRX_ITX_P3 <22>; DMI_TXN_0 AE35 DMI_MTX_IRX_N0 <22>; DMI_TXN_1 AE43 DMI_MTX_IRX_N1 <22>; DMI_TXN_2 AE46 DMI_MTX_IRX_N2 <22>; DMI_TXN_3 AH42 DMI_MTX_IRX_N3 <22>; DMI_TXP_0 AD35 DMI_MTX_IRX_P0 <22>; DMI_TXP_1 AE44 DMI_MTX_IRX_P1 <22>; DMI_TXP_2 AE46 DMI_MTX_IRX_P2 <22>; DMI_TXP_3 AH43 DMI_MTX_IRX_P3 <22>

CFG: <6> MCH_CLKSEL0 T25 CFG_0; <6> MCH_CLKSEL1 R25 CFG_1; <6> MCH_CLKSEL2 P25 CFG_2; T32 P20 CFG_3; T33 P24 CFG_4; CFG5 C25 CFG_5; CFG6 N24 CFG_6; CFG7 M24 CFG_7; T34 E21 CFG_8; CFG9 C23 CFG_9; C24 CFG_10; T35 N21 CFG_11; T36 P21 CFG_12; T37 T21 CFG_13; T38 R20 CFG_14; T39 M20 CFG_15; T40 CFG16 L21 CFG_16; H21 CFG_17; T41 P29 CFG_18; T42 CFG19 R28 CFG_19; CFG20 T28 CFG_20

PM: <21> PM_SYNC# R29 PM_SYNC#; <8,19,43> H_DPRSTP# B7 H_DPRSTP#; <17> PM_EXTTS#0 N33 PM_EXTTS#0; <18> PM_EXTTS#1 P32 PM_EXTTS#1; PM_PWROK_R AT40 PM_EXT_TS#_0; PLT_RST#_NB AT11 PM_EXT_TS#_1; <7,19> H_THERMTRIP# T20 H_THERMTRIP#; <21,43> DPRSLPVR R32 DPRSLPVR; PWROK; RSTIN#; THERMTRIP#

GRAPHICS VID: GFX_VID_0 B33 GFX_VID0 T43; GFX_VID_1 B32 GFX_VID1 T44; GFX_VID_2 G33 GFX_VID2 T45; GFX_VID_3 F33 GFX_VID3 T46; GFX_VID_4 E33 GFX_VID4 T47; GFX_VR_EN C34 GFX_VR_ON T48

ME: CL_CLK AH37 CL_CLK0 <21>; CL_DATA AH36 CL_DATA0 <21>; CL_PWROK AN36 M_PWROK <21>; CL_RST# AJ35 CL_RST# <21>; CL_VREF AH34 +CL_VREF

MISC: DDPC_CTRLCLK N28 HDMI_C_CLK; DDPC_CTRLDATA M28 HDMI_C_DATA; SDVO_CTRLCLK G36 HDMI_B_CLK; SDVO_CTRLDATA E36 HDMI_B_DATA; CLKREQ# K36 MCH_CLKREQ#; ICH_SYNC# H36 MCH_ICH_SYNC# <21>; TSATN# B12 MCH_TSATN# R101 56_0402_5% +1.05V_VCCP

R03 modify it.

HDA: HDA_BCLK B28 MCH_HDA_BITCLK; HDA_RST# B30 MCH_HDA_RST#; HDA_SDI B29 MCH_HDA_SDIN2_R; HDA_SDO C29 MCH_HDA_SDOUT; HDA_SYNC A28 MCH_HDA_SYNC

R103 33_0402_1% HDA_BITCLK_NB <19>
R104 33_0402_1% HDA_RST_NB# <19>
R105 0_0402_5% HDA_SDIN1 <19>
R106 33_0402_1% HDA_SDOUT_NB <19>
R107 33_0402_1% HDA_SYNC_NB <19>

12.30 modify it

NC: BG48 NC_1; BF48 NC_2; BD48 NC_3; BC48 NC_4; BH47 NC_5; BG47 NC_6; BE47 NC_7; BH46 NC_8; BF46 NC_9; BG45 NC_10; BH44 NC_11; BH43 NC_12; BH6 NC_13; BH5 NC_14; BG4 NC_15; BH3 NC_16; BE3 NC_17; BH2 NC_18; BG2 NC_19; BE2 NC_20; BG1 NC_21; BF1 NC_22; BD1 NC_23; BC1 NC_24; F1 NC_25; A47 NC_26

CANTIGA ES_FCBGA1329

Compensation

DDR3
+1.5V
SMRCOMP R83 80.6_0402_1%
SMRCOMP# R84 80.6_0402_1%

DDR3
+1.5V
R82 1K_0402_1%
SMRCOMP_VOH
C71 2.2U_0603_6.3V6K~D
C70 0.01U_0402_16V7K~D
R89 3.01K_0402_1%
SMRCOMP_VOL
C73 2.2U_0603_6.3V6K~D
C74 0.01U_0402_16V7K~D
R91 1K_0402_1%

+V_DDR_MCH_REF
C72 0.1U_0402_10V7K~D

Use for DDR3 signls, if support DDR2 need connect to GND
+3VALW
C75 0.1U_0402_10V7K~D
R92 12K_0402_1%
SM_PWROK
R93 10K_0402_5%
U5 74AHC1G08GW_SOT353-5~D
R94 @ 0_0402_5%
1.5V_PGOOD <42>
SLP_S4# <21,31>

Follow MiniCooper

+1.05V_VCCP
R95 1K_0402_1%
C76 0.1U_0402_10V7K~D
R98 511_0402_1%

Thermal Sensor Aux Trip Notification: Output from the (G)MCH to the EC indicating the Aux2 trip point (SW programmable) has been crossed.
(If not used, terminated 56 ohm pull up to VCCP)

For HDA UMA support 1.5V

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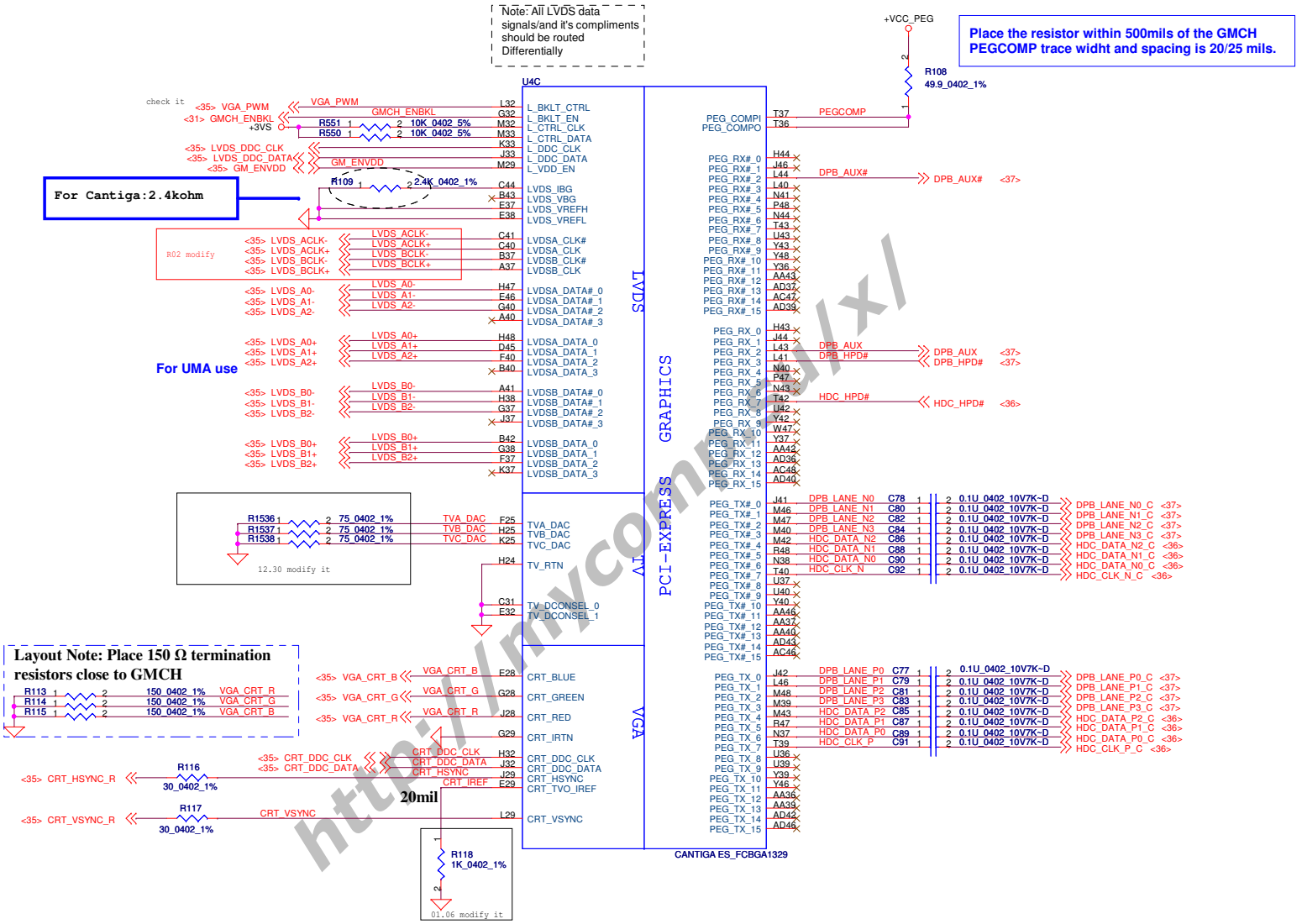

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Title: Cantiga(3 of 7)

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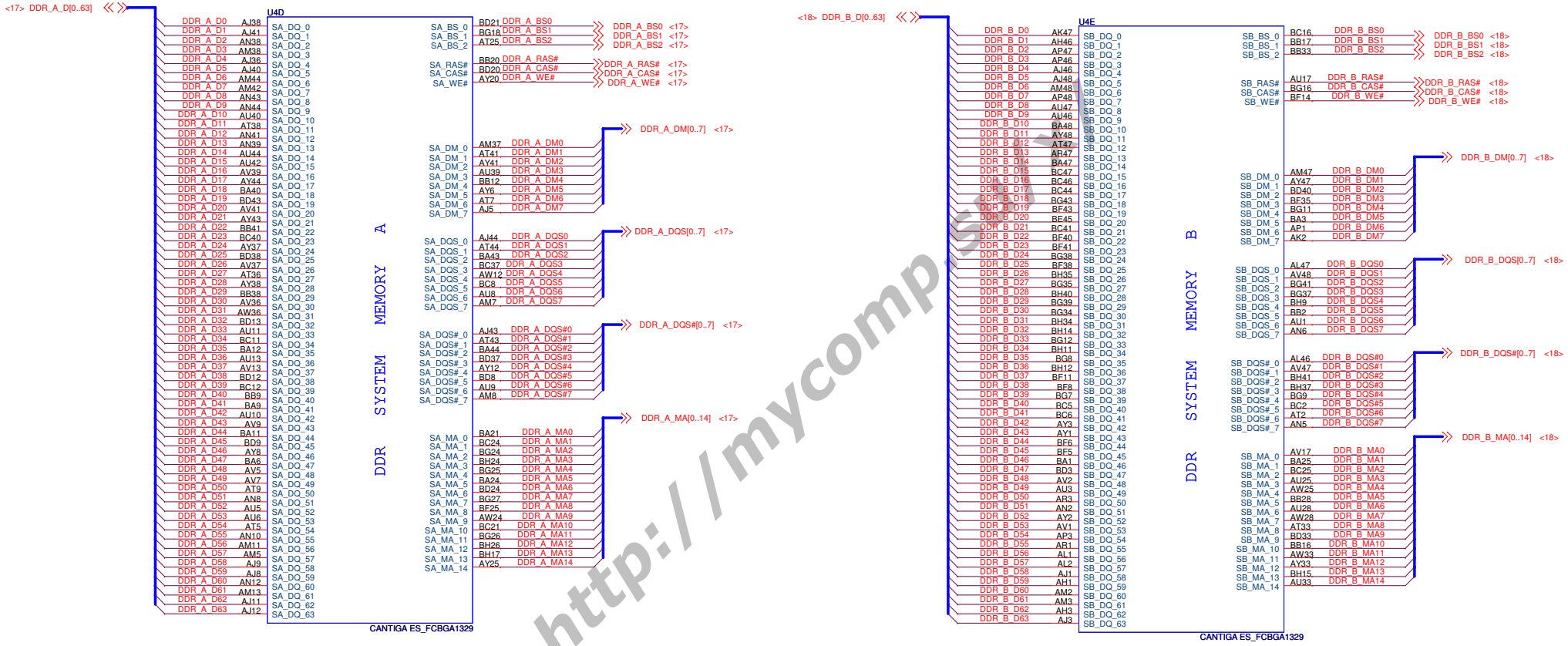

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Title: Cantiga(4 of 7)

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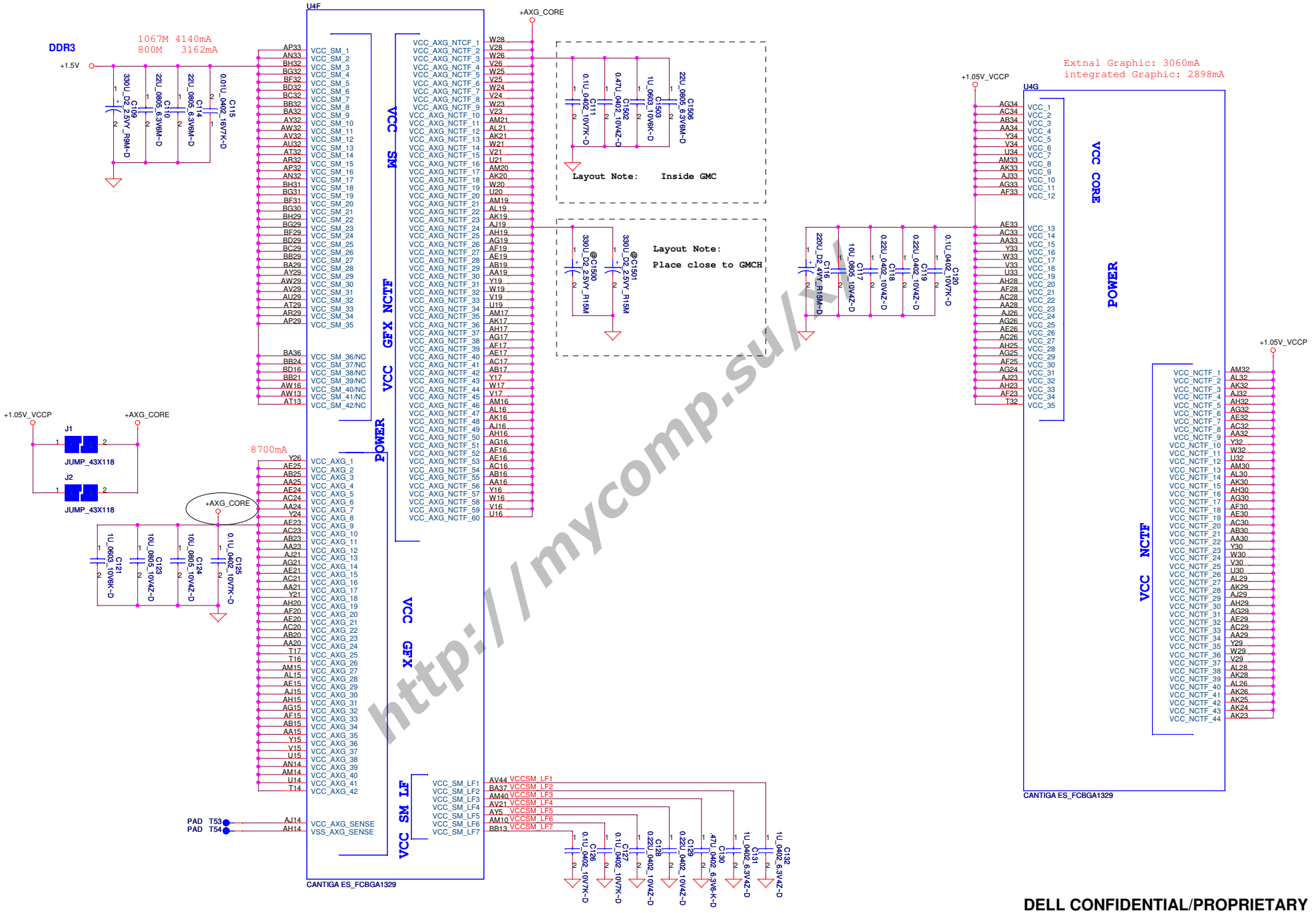

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Title	Cantiga(5 of 7)
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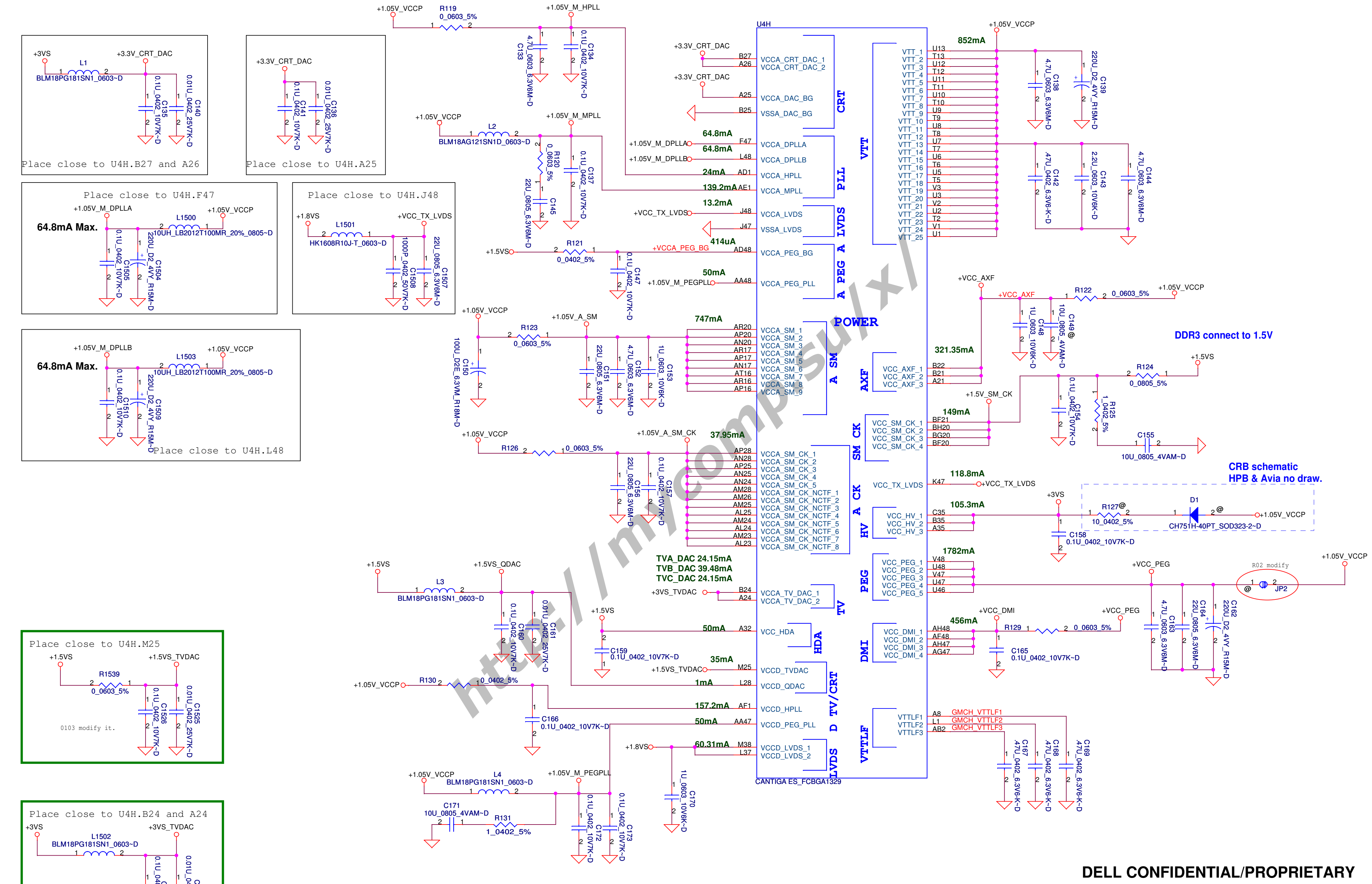
U4H
CANTIGA ES_FCBGA1329
CRT
PLL
LVDS
PEG
POWER
SM
AXF
SM CK
A CK
HV
TV
HDA
DMI
TV/CRT
VTTLF
VTT
Place close to U4H.B27 and A26
Place close to U4H.A25
Place close to U4H.F47
Place close to U4H.J48
Place close to U4H.L48
Place close to U4H.M25
Place close to U4H.B24 and A24
64.8mA Max.
DDR3 connect to 1.5V
CRB schematic
HPB & Avia no draw.
R02 modify
0103 modify it.
852mA
747mA
37.95mA
321.35mA
149mA
118.8mA
105.3mA
1782mA
456mA
TVA_DAC 24.15mA
TVB_DAC 39.48mA
TVC_DAC 24.15mA
+1.05V_VCCP
+3.3V_CRT_DAC
+1.05V_M_HPLL
+1.05V_M_MPLL
+1.05V_M_DPLLA
+1.05V_M_DPLLB
+VCC_TX_LVDS
+1.05V_A_SM
+1.05V_A_SM_CK
+1.5VS_TVDAC
+3VS_TVDAC
+1.5VS_QDAC
+1.05V_M_PEGPLL
+VCC_AXF
+VCC_PEG
+VCC_DMI
+1.5V_SM_CK
GMCH_VTTLF1
GMCH_VTTLF2
GMCH_VTTLF3

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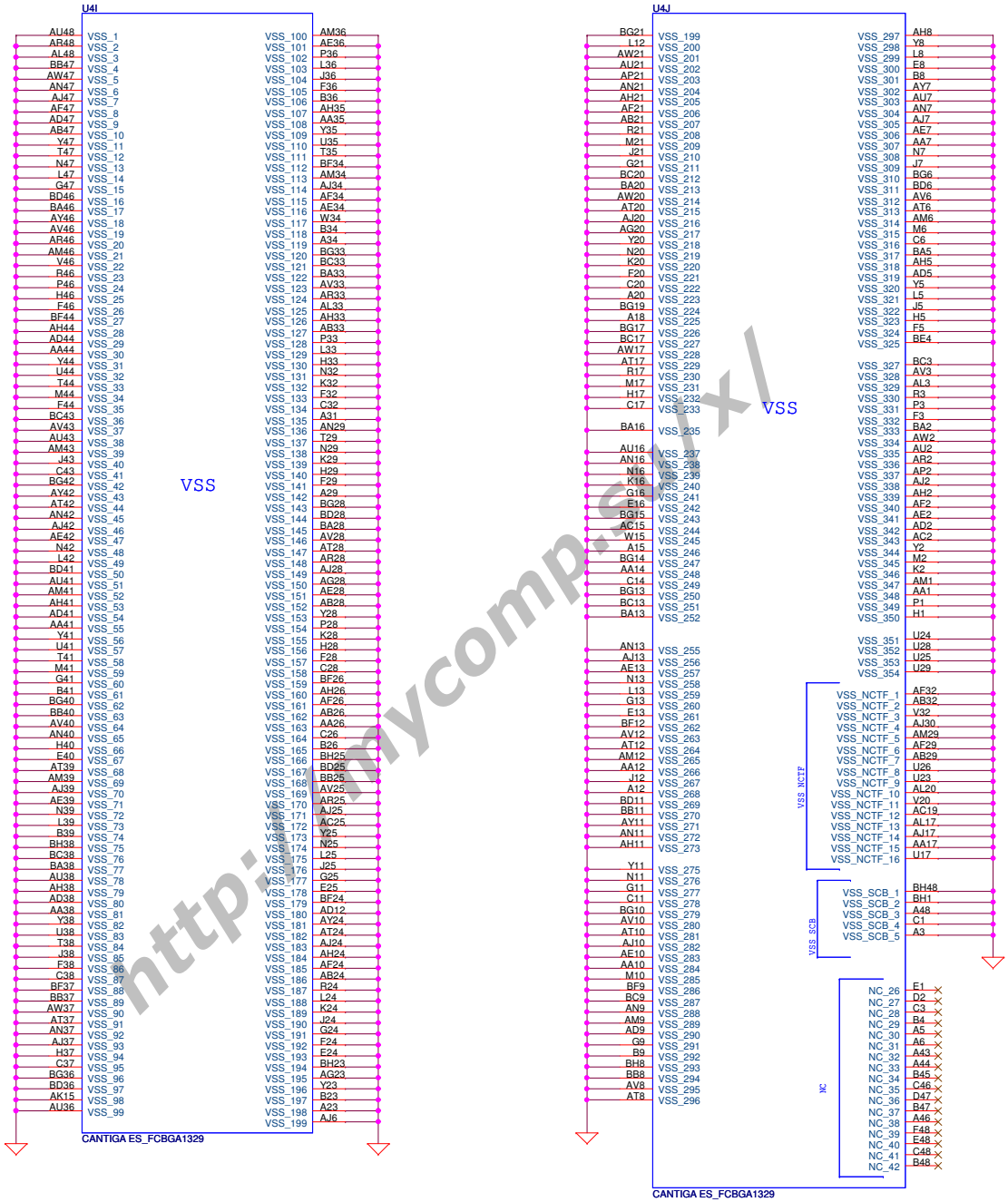

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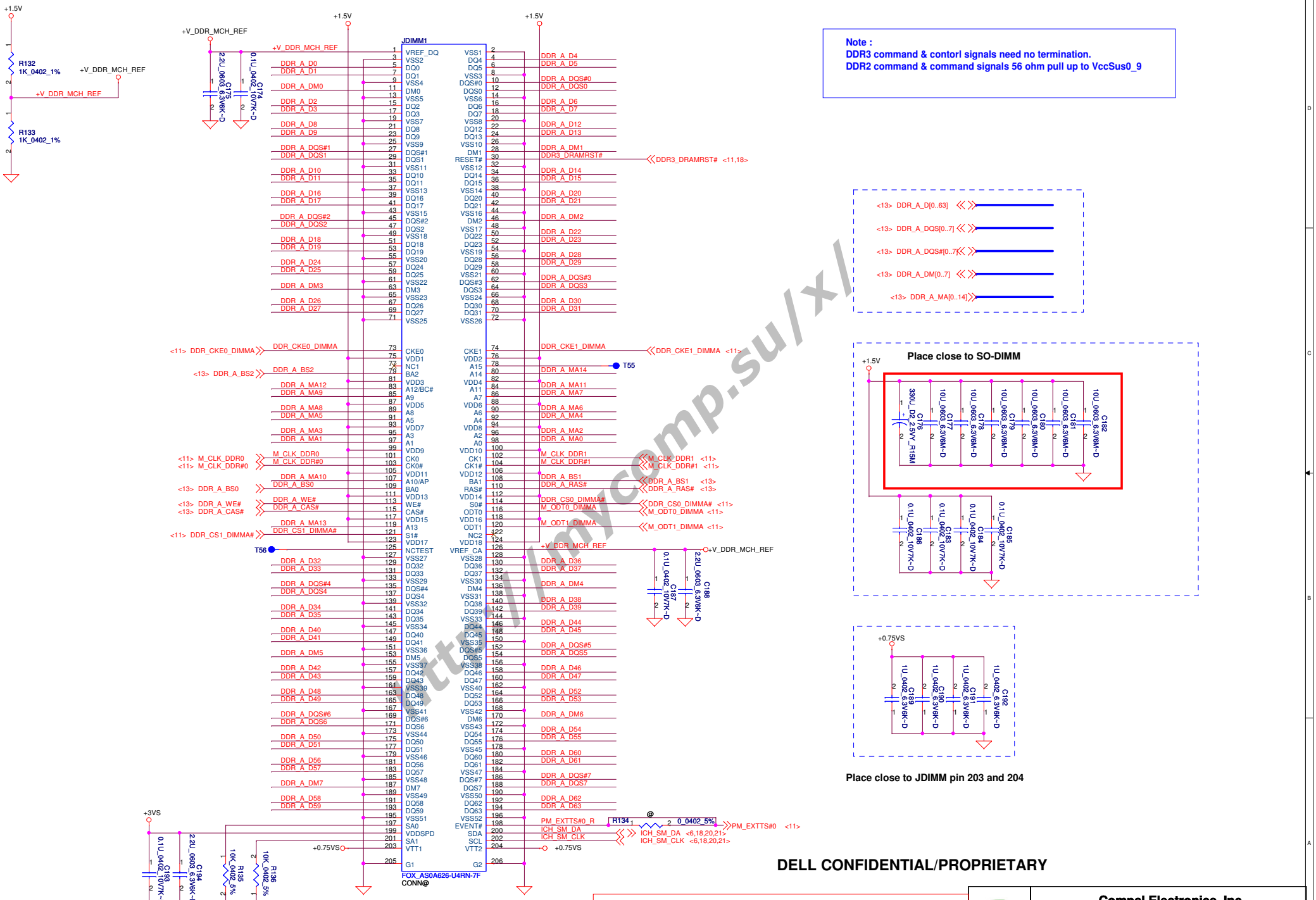
Title: Cantiga(7 of 7)

Size | Document Number: LA-5152P | Rev: A00

Date: Monday, June 15, 2009 | Sheet 16 of 51


JDIMM1
FOX_AS0A626-U4RN-7F
CONN@
DDR3 SO-DIMM/Standard Type
Note :
DDR3 command & contorl signals need no termination.
DDR2 command & command signals 56 ohm pull up to VccSus0_9
Place close to SO-DIMM
Place close to JDIMM pin 203 and 204
DELL CONFIDENTIAL/PROPRIETARY
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Compal Electronics, Inc.
DDRIII SO-DIMM A SLOT
LA-5152P
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Monday, June 15, 2009
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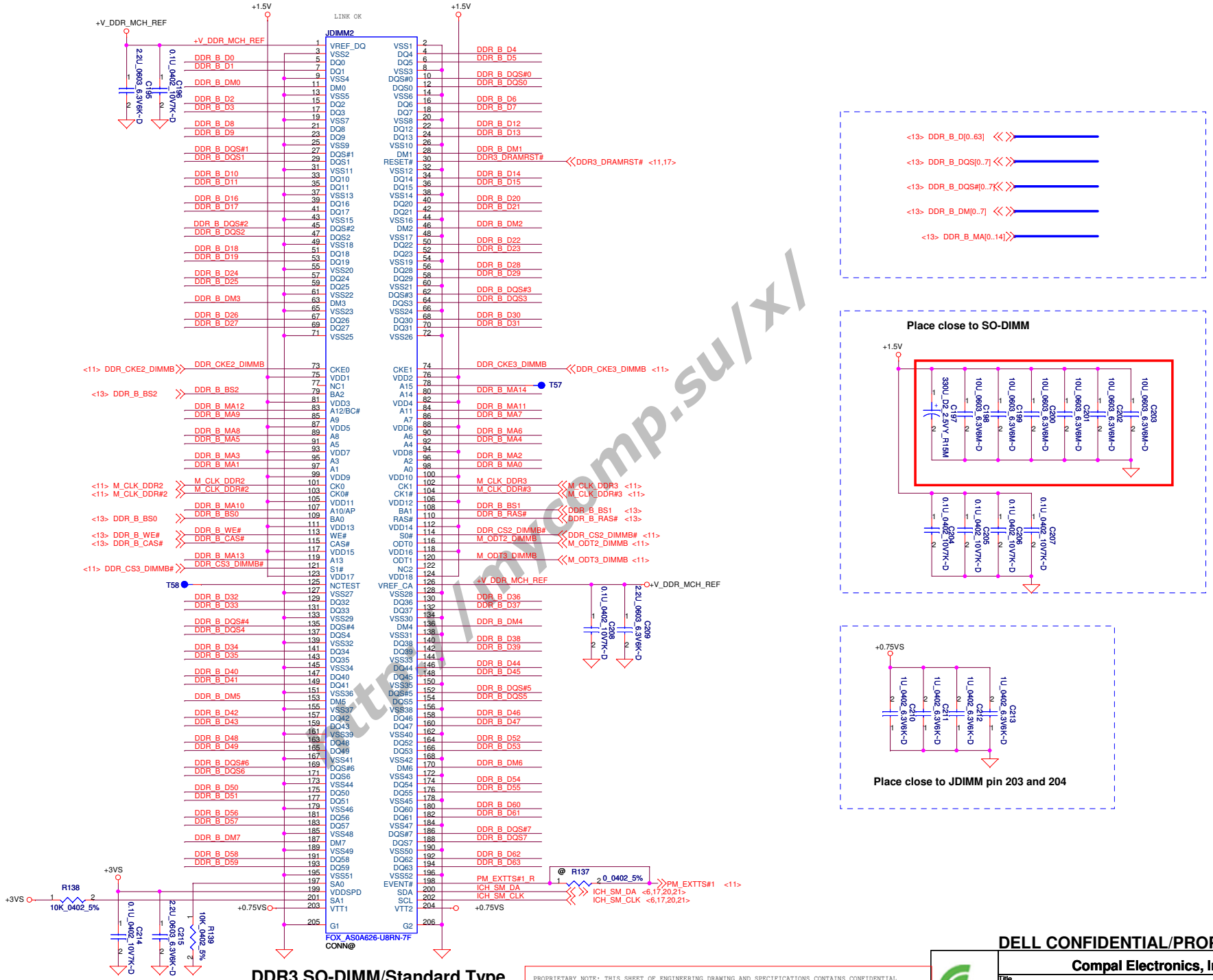
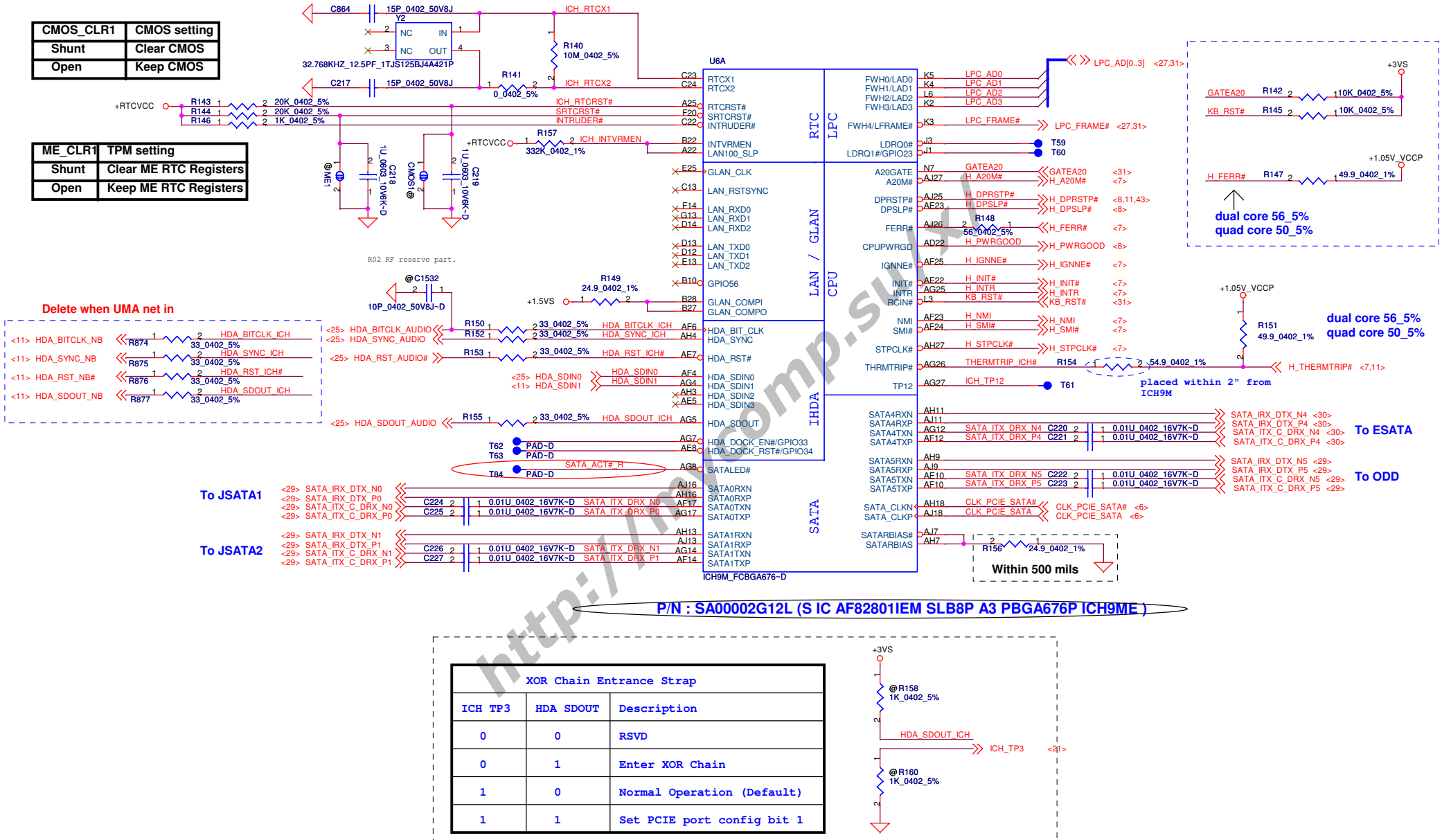

JDIMM2
LINK OK
FOX_AS0A626-U8RN-7F
CONN@
DDR3 SO-DIMM/Standard Type
Place close to SO-DIMM
Place close to JDIMM pin 203 and 204
DDR3_DRAMRST# <11,17>
T57
T58
PM_EXTTS#1 <11>
ICH_SM_DA <6,17,20,21>
ICH_SM_CLK <6,17,20,21>
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
DDRIII SO-DIMM B SLOT
LA-5152P
Monday, June 15, 2009
Sheet 18 of 51



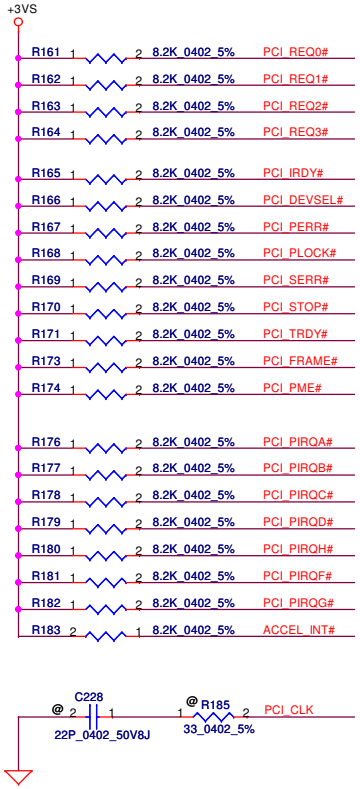
DELL CONFIDENTIAL/PROPRIETARY

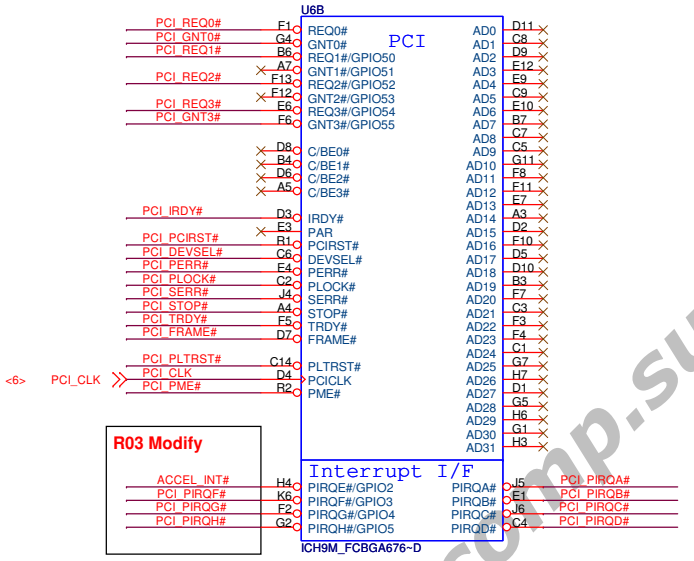
Compal Electronics, Inc.

Title: ICH9-M(1/5)

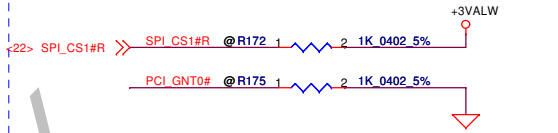
Size | Document Number: LA-5152P | Rev: A00

Date: Monday, June 15, 2009 | Sheet 19 of 51

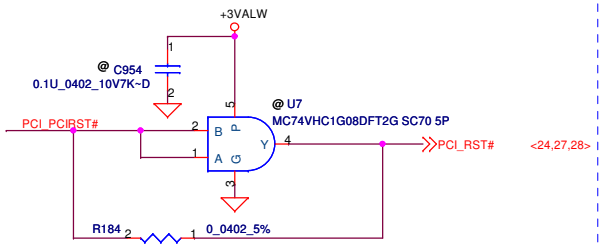




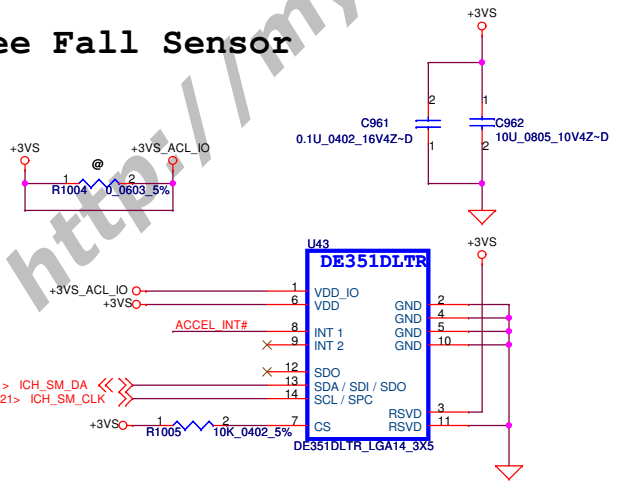
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



GNT0 & SPI_CS#1 have a weak internal pull up



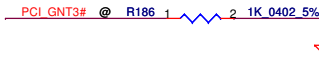
Free Fall Sensor



Must be placed in the center of the system.

P/N : SA000039C00 (S IC DE351DLTR LGA 14P MOTION SENSOR)

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *

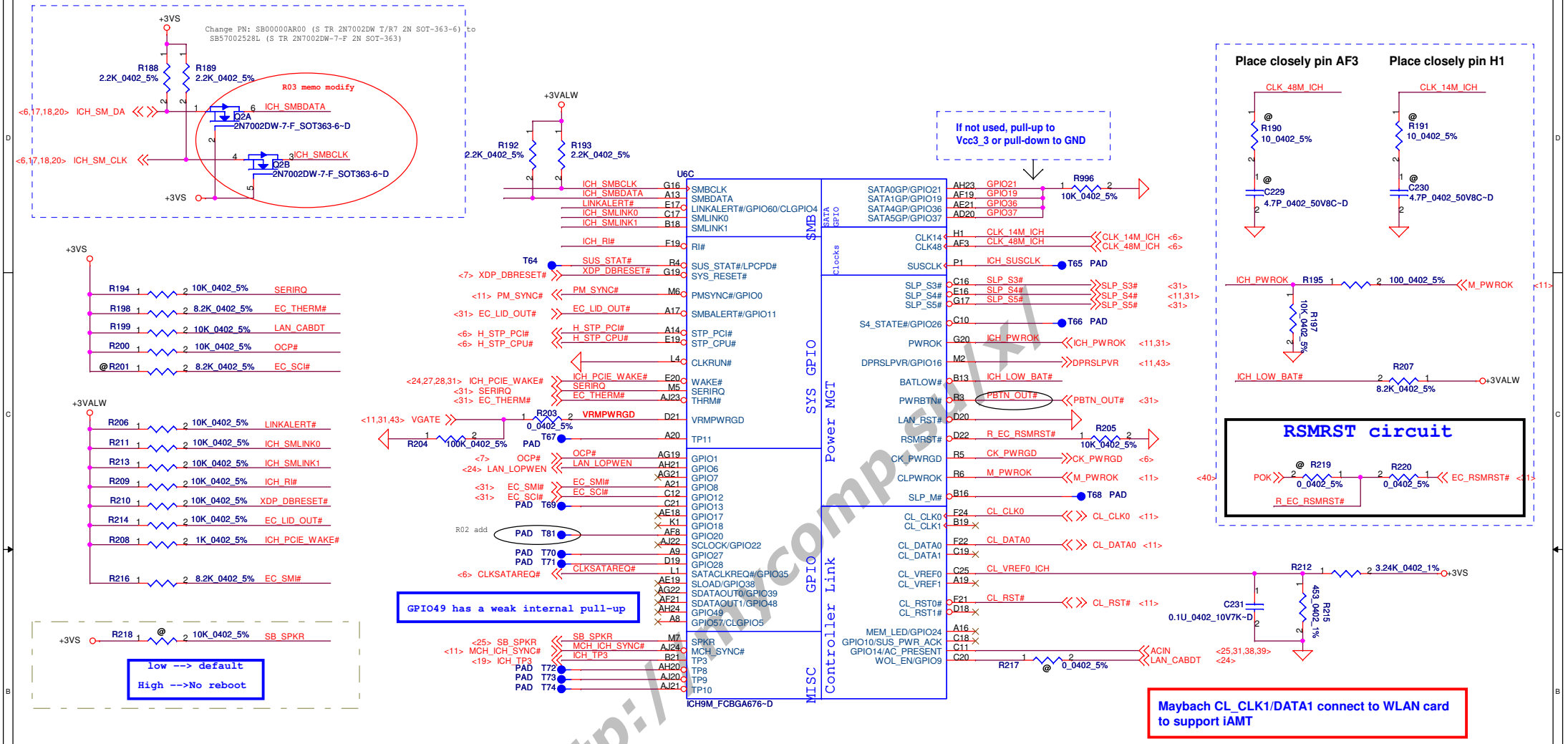


Compal Electronics, Inc.

Title: ICH9-M(2/5)

Size | Document Number: LA-5152P | Rev: A00

Date: Monday, June 15, 2009 | Sheet 20 of 51



Compal Electronics, Inc.	
Title	ICH9-M(3/5)
Size	Document Number: LA-5152P
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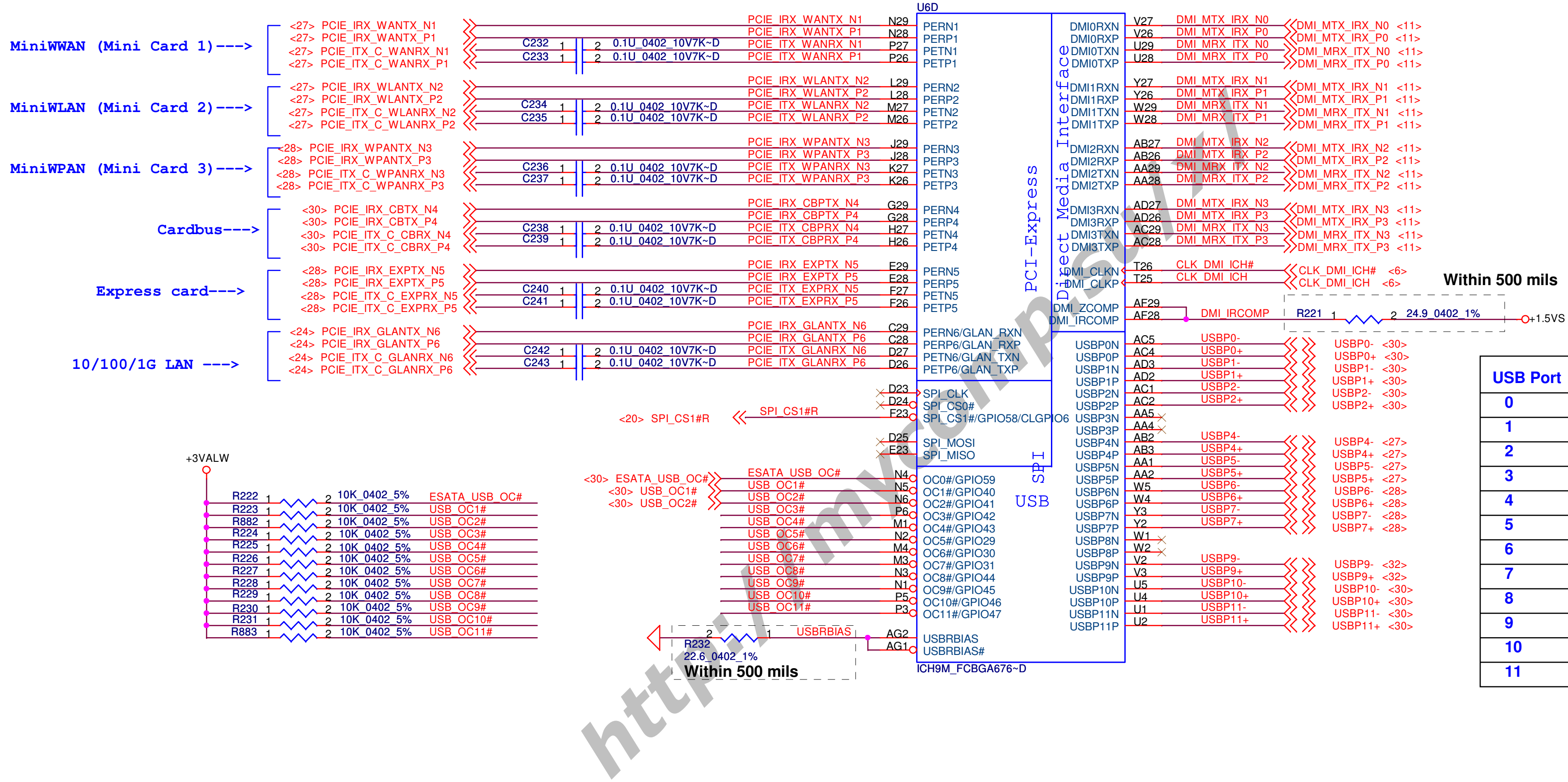
Date:	Monday, June 15, 2009
Sheet	21 of 51



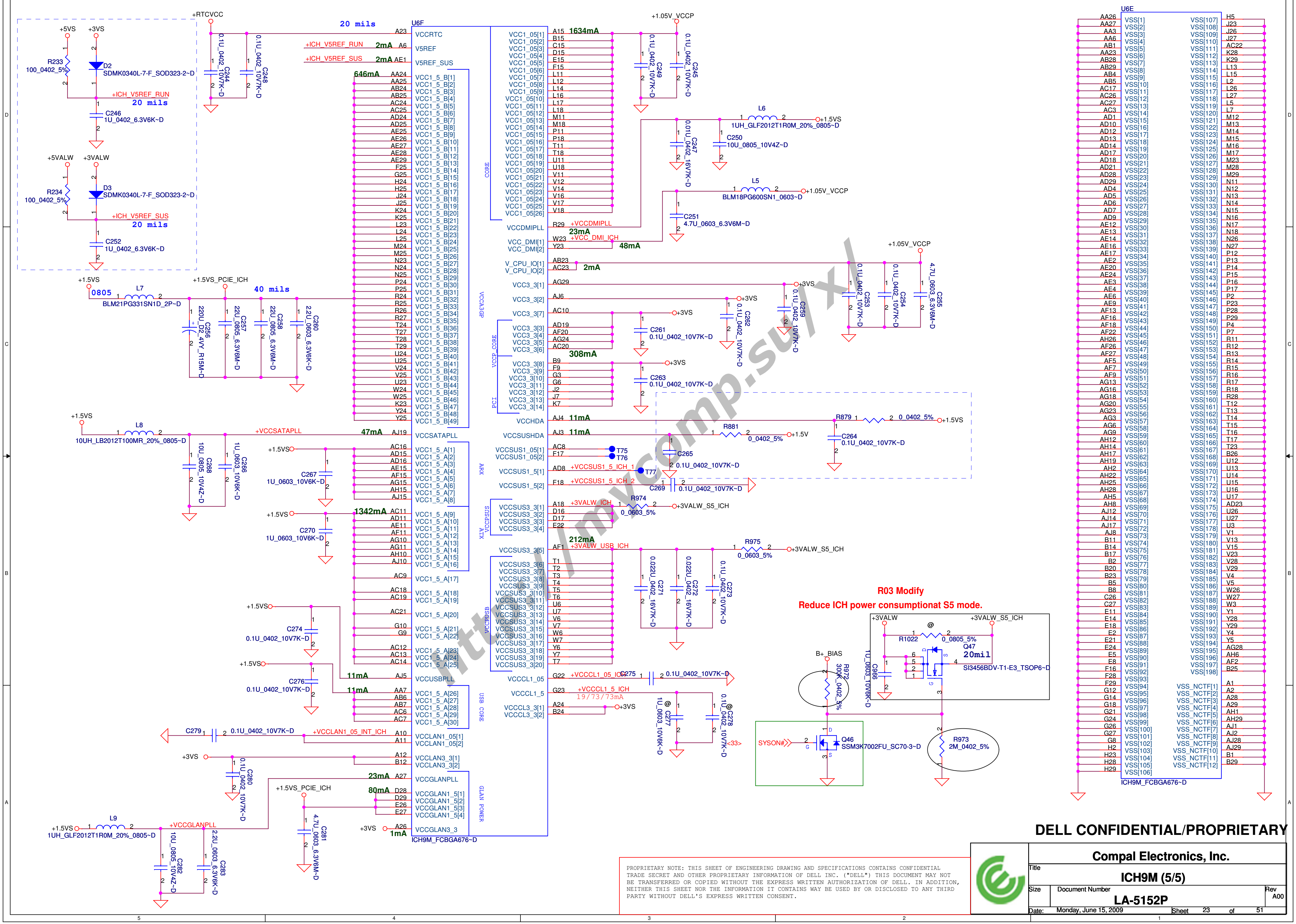
USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

Compal Electronics, Inc.

Title: ICH9-M(4/5)

Size | Document Number: LA-5152P | Rev: A00

Date: Monday, June 15, 2009 |



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Compal Electronics, Inc.

Title	ICH9M (5/5)	
Size	Document Number: LA-5152P	Rev: A00
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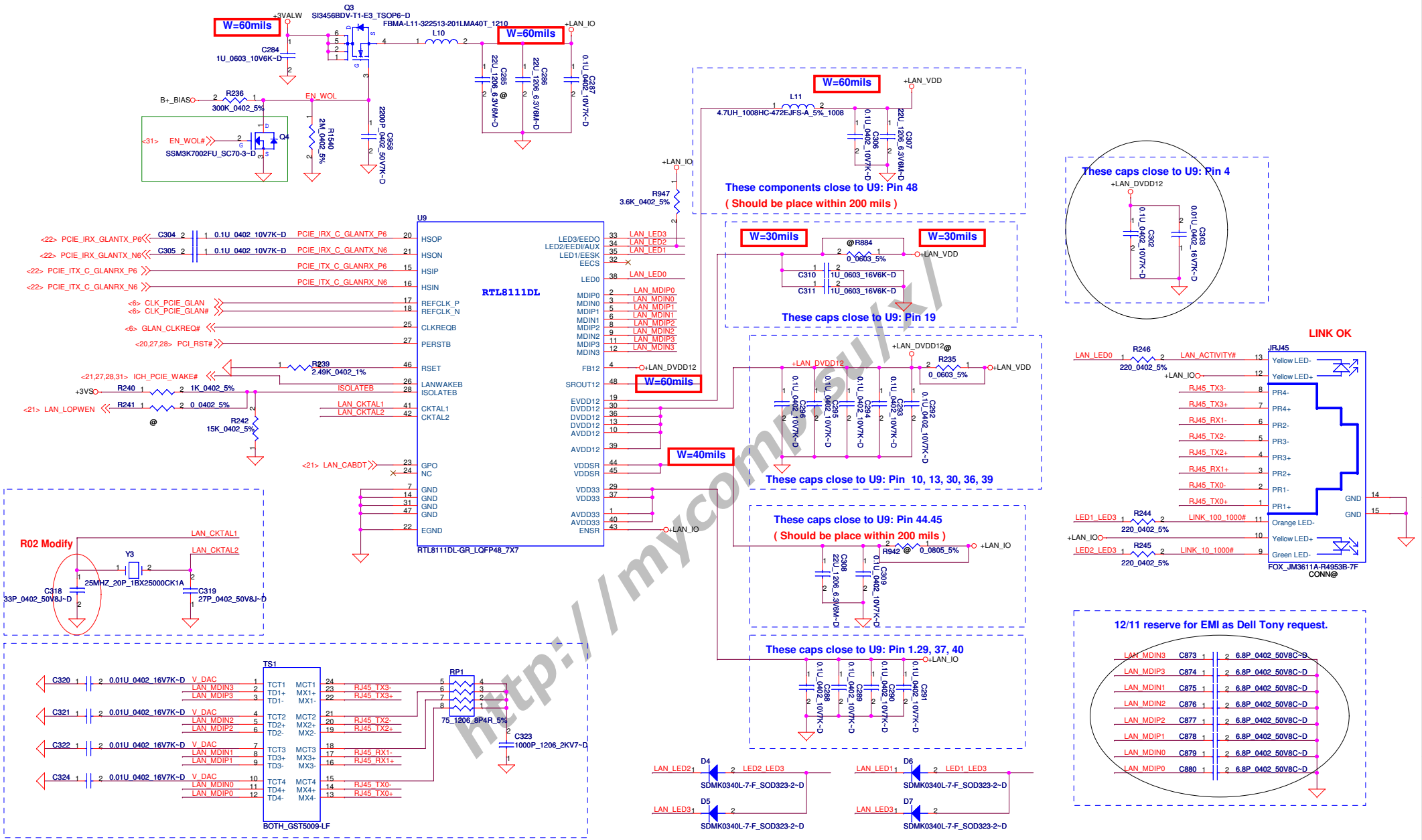

LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 /100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT

Compal Electronics, Inc.
Title: Gigabit LAN_RTL8111DL
Size: Document Number: LA-5152P
Rev: 1A
Date: Monday, June 15, 2009
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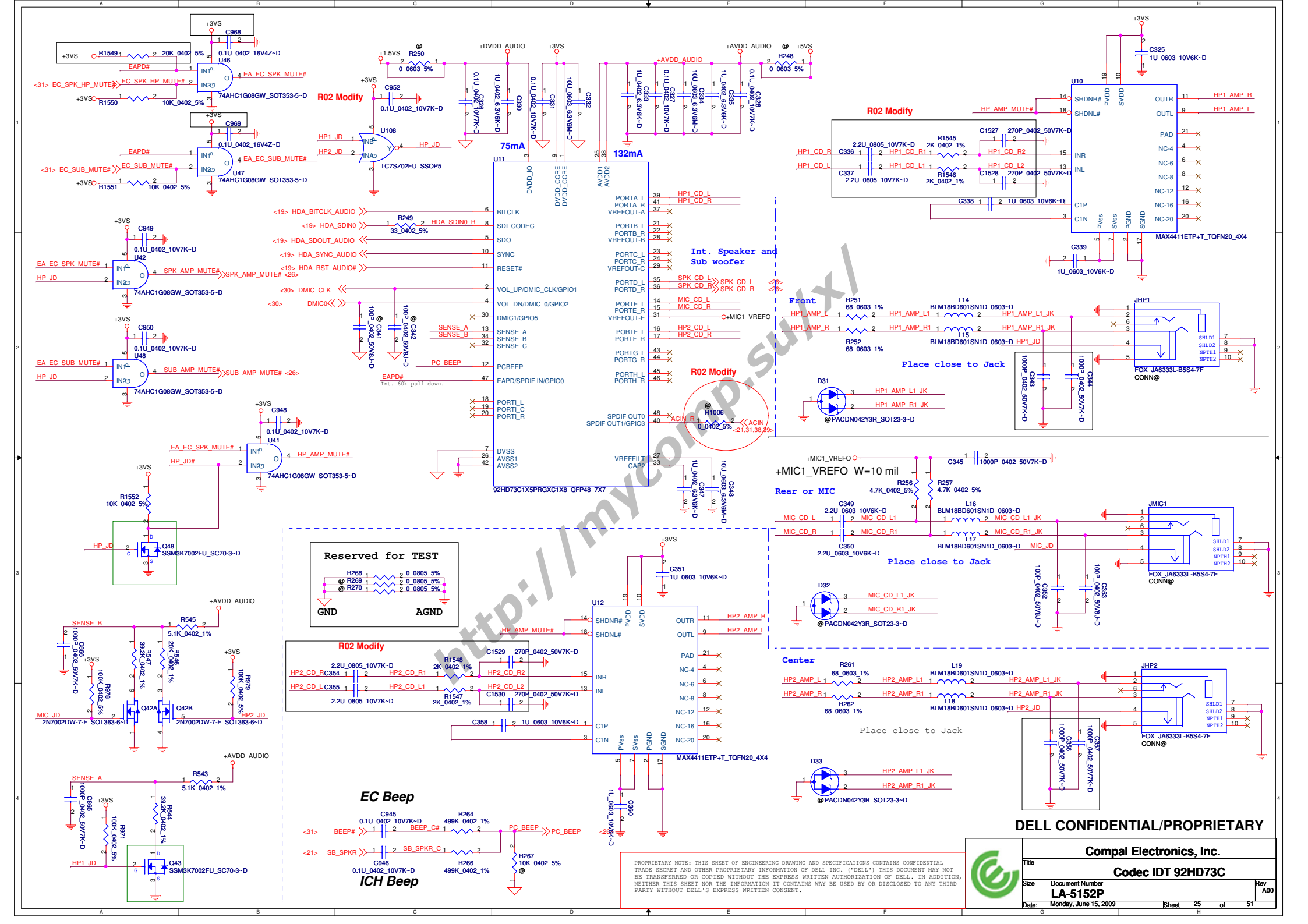

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Compal Electronics, Inc.	
Title	Codec IDT 92HD73C
Size	Document Number: LA-5152P
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Date:	Monday, June 15, 2009
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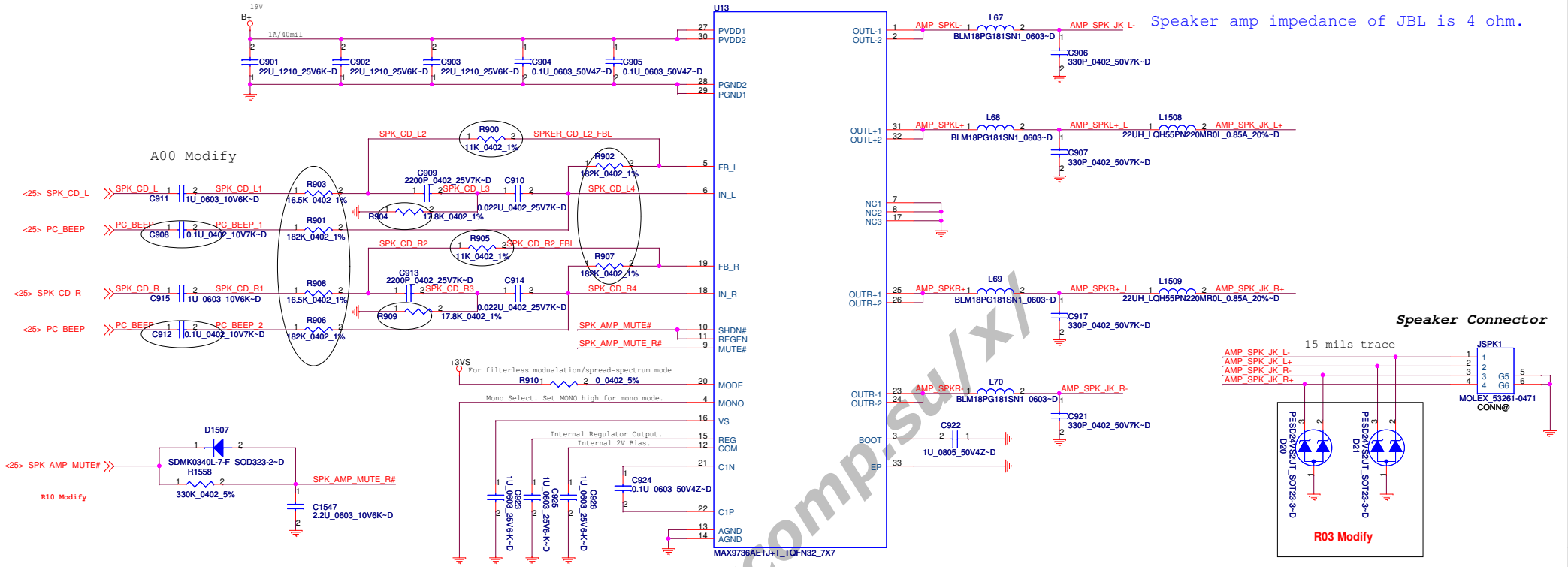
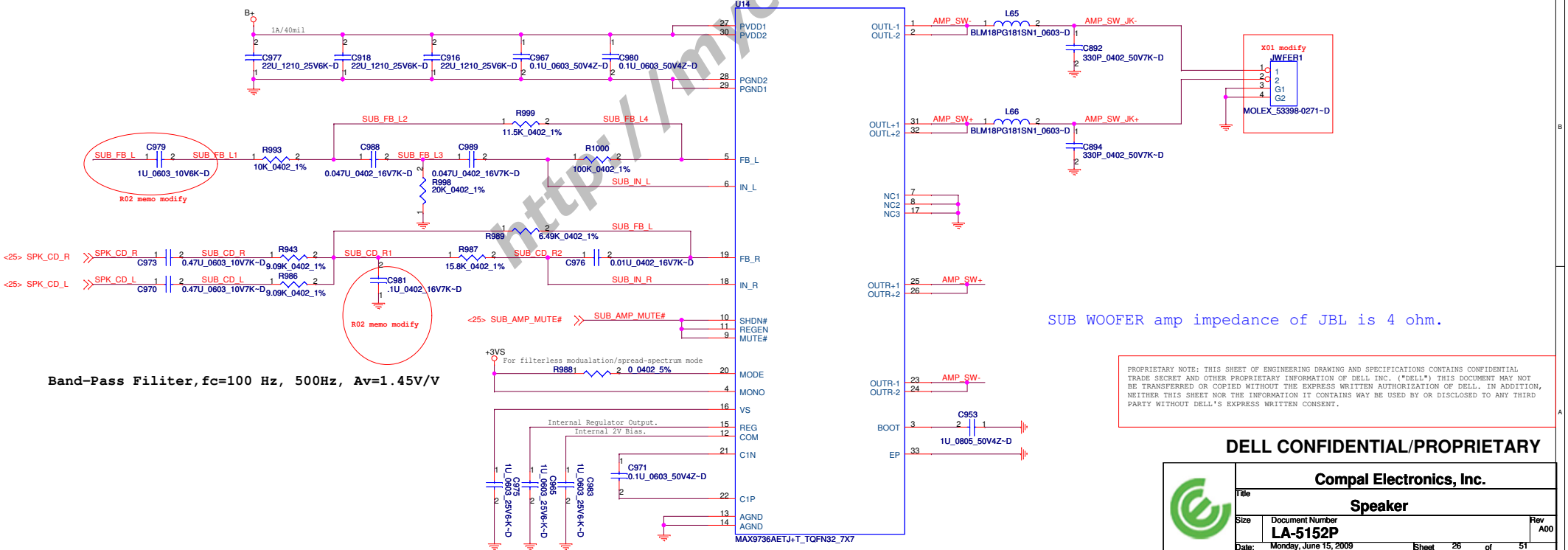
High-Pass Filiter,fc=500Hz, Av=1.45V/V



Band-Pass Filiter,fc=100 Hz, 500Hz, Av=1.45V/V



Compal Electronics, Inc.	
Title	Speaker
Size	Document Number: LA-5152P
Rev	A00
Date:	Monday, June 15, 2009
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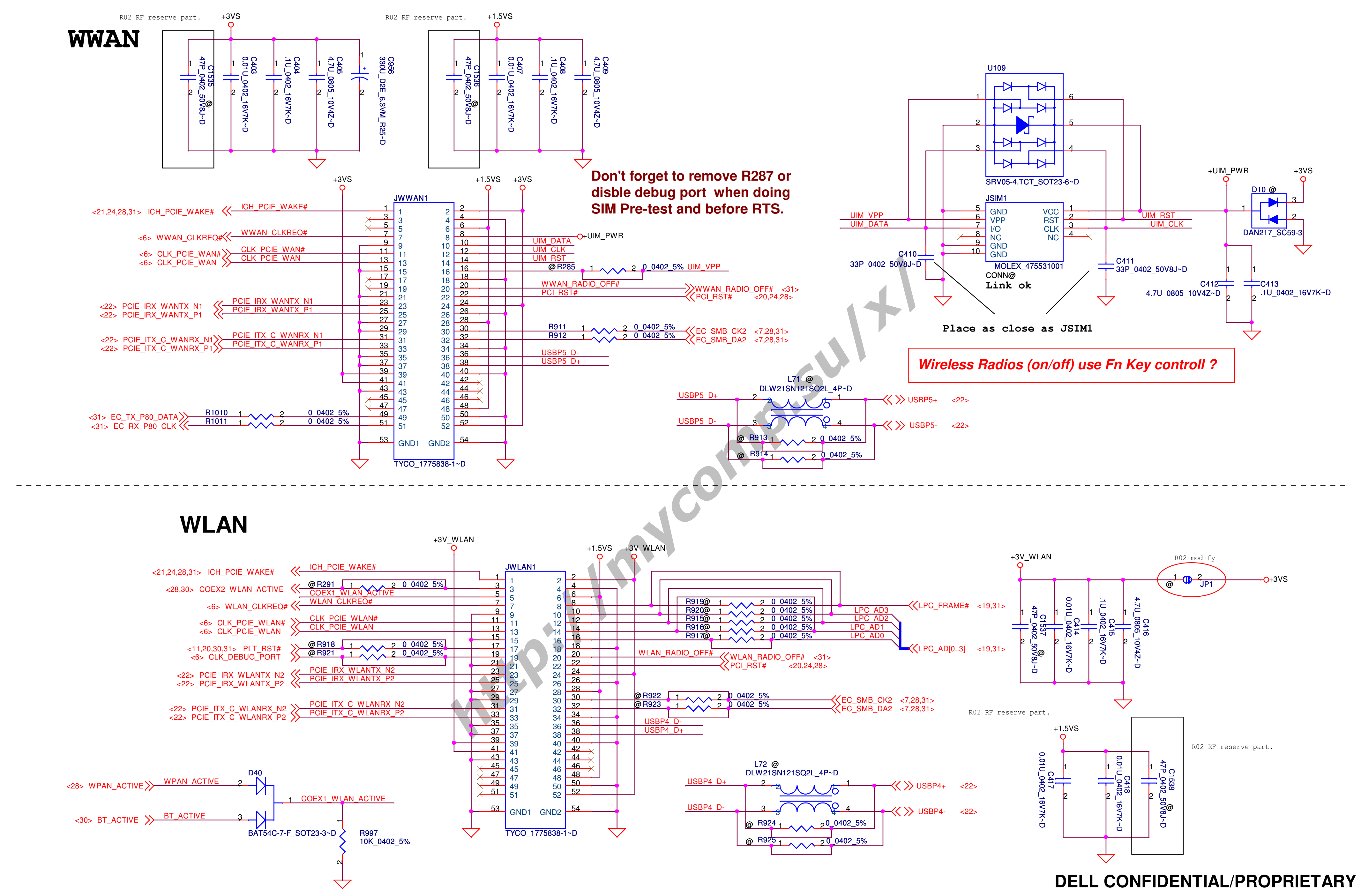

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	Mini Card_WLAN/WWAN
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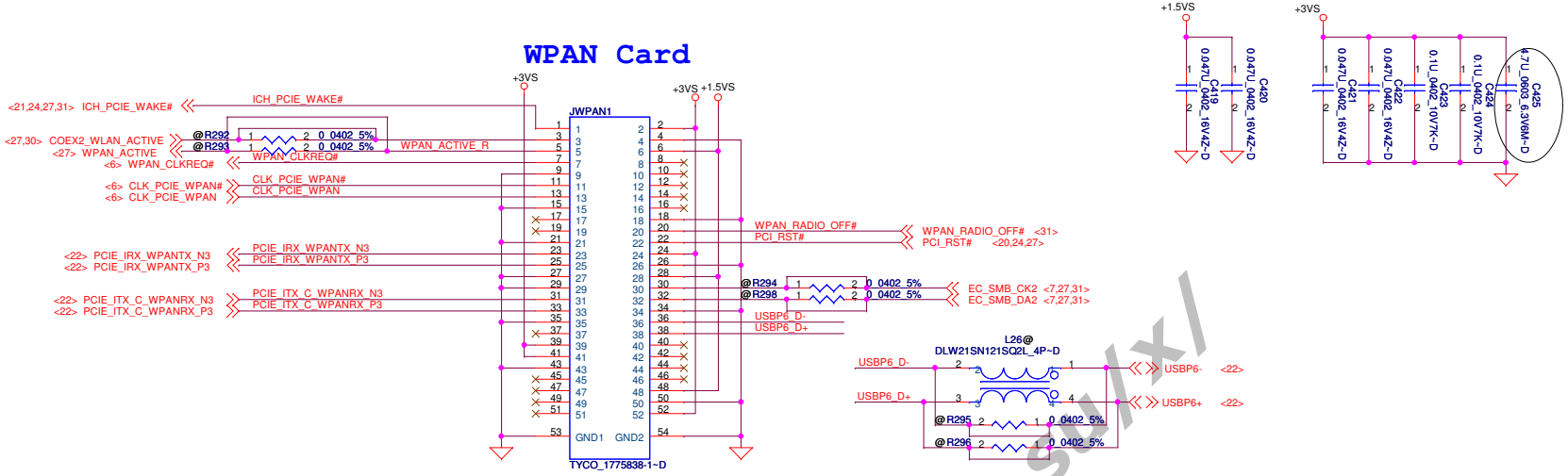
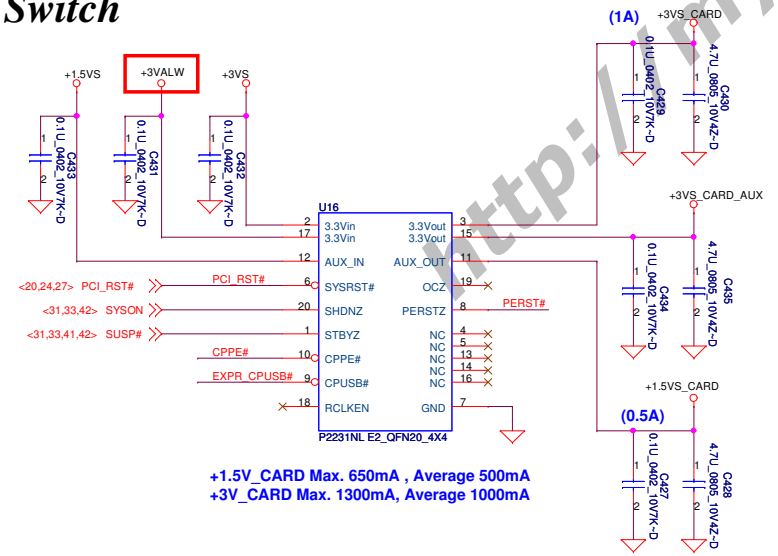
Date:	Monday, June 15, 2009 — Sheet 27 of 51

WPAN Card

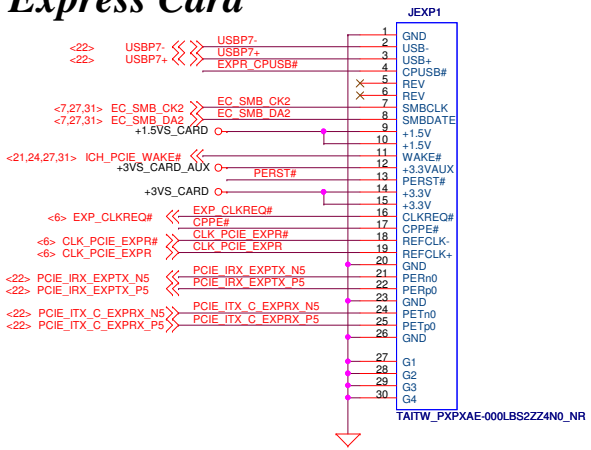


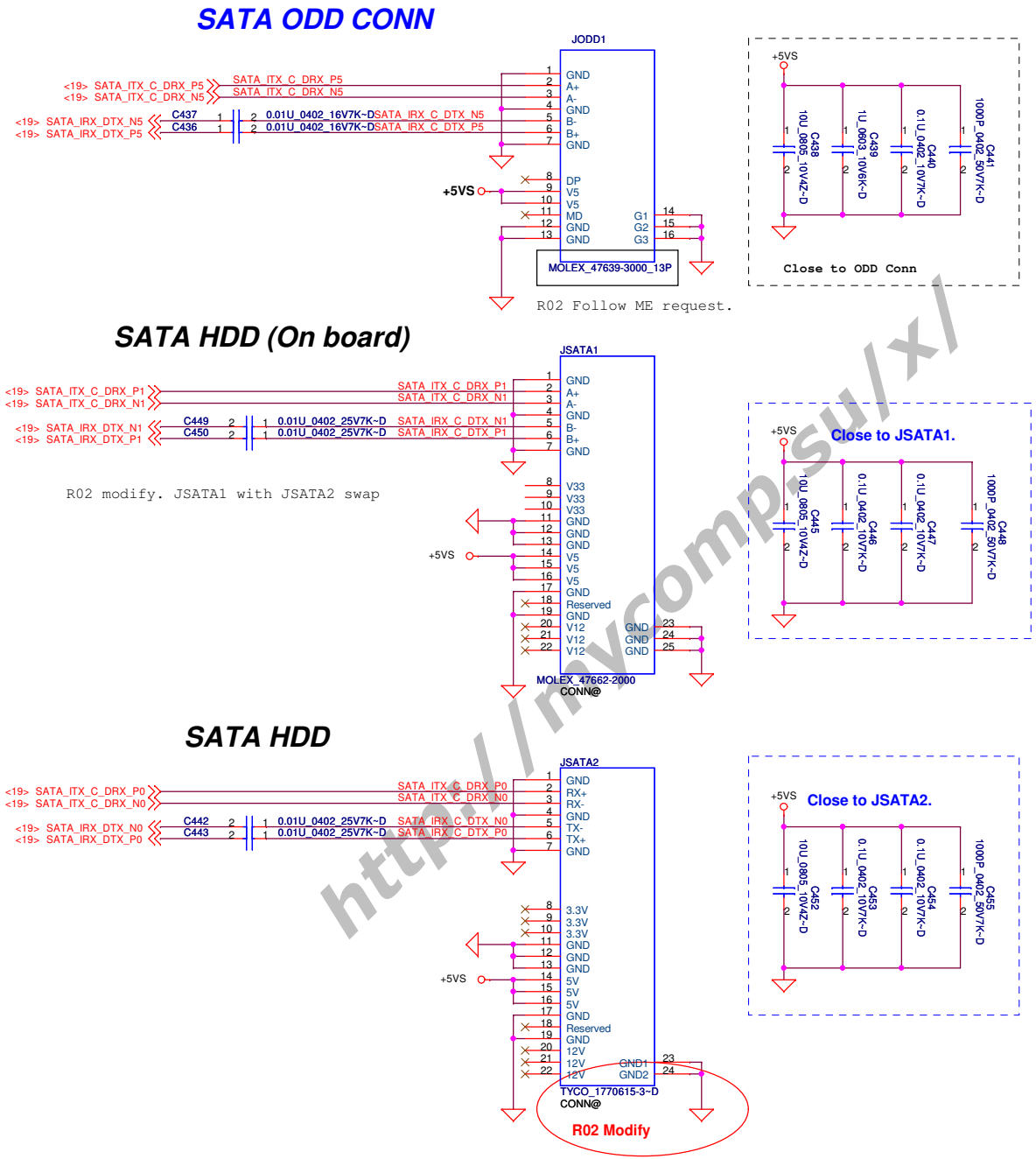
Express Card Power Switch



+1.5V_CARD Max. 650mA , Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

Express Card





由於Kink pin尺寸大於kink hole，將導致零件干涉，也同時會使pin腳空焊，
因此將 原HDD Conn.(REV.) –FOXCONN–SP01000LC0L layout 改成Tyco–SP01000E70L layout
即可解決造成pin腳空焊的問題

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	ODD / SATA CONN
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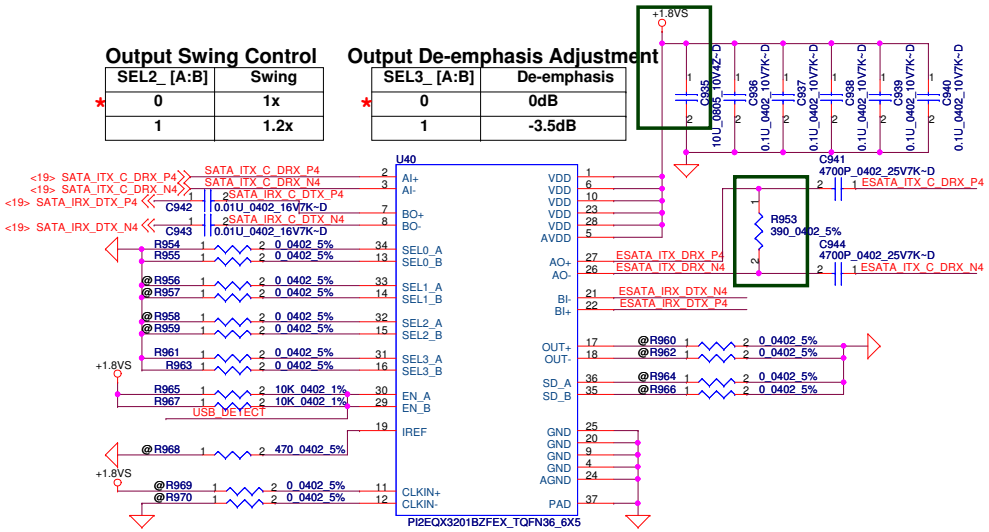
Output Swing Control

SEL2_ [A:B]	Swing
0	1x
1	1.2x

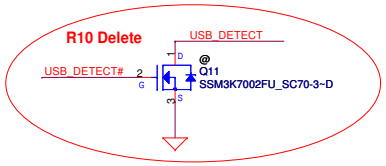
Output De-emphasis Adjustment

SEL3_ [A:B]	De-emphasis
0	0dB
1	-3.5dB



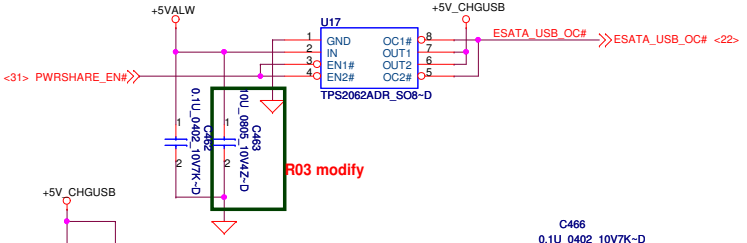
A00 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

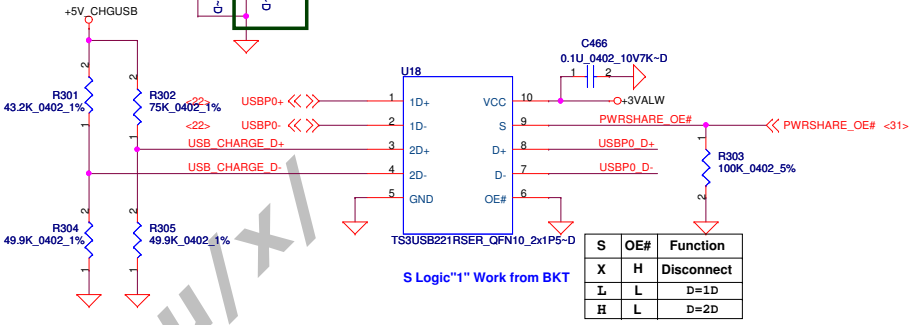
R10 Delete



Equalizer Selection

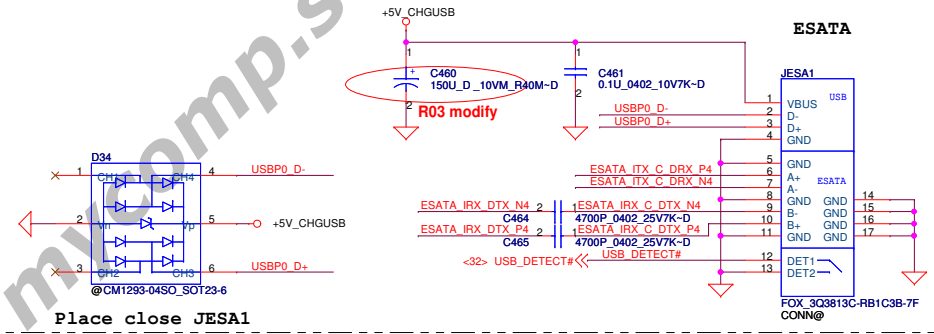
SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz



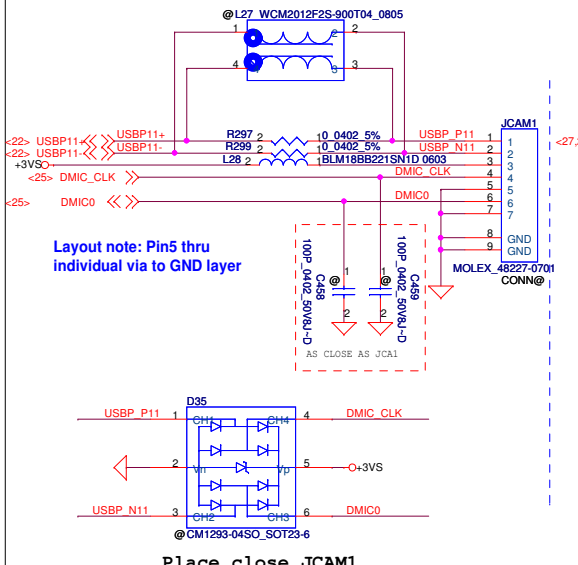


S Logic"1" Work from BKT

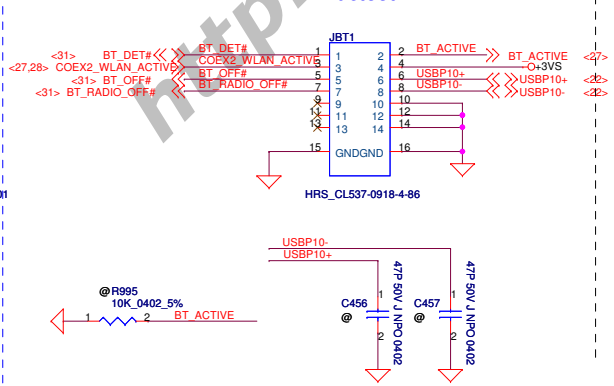
S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



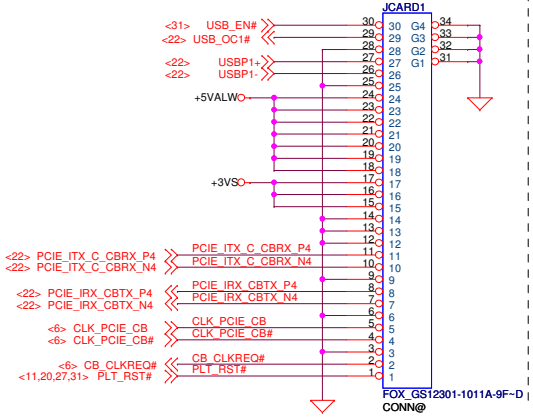
Camera Conn



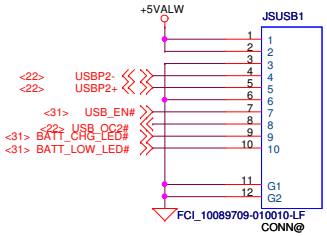
Bluetooth



Cardreader Connector



to Single USB board



Compal Electronics, Inc.

Title: USB / ESATA / BT / CAMARA

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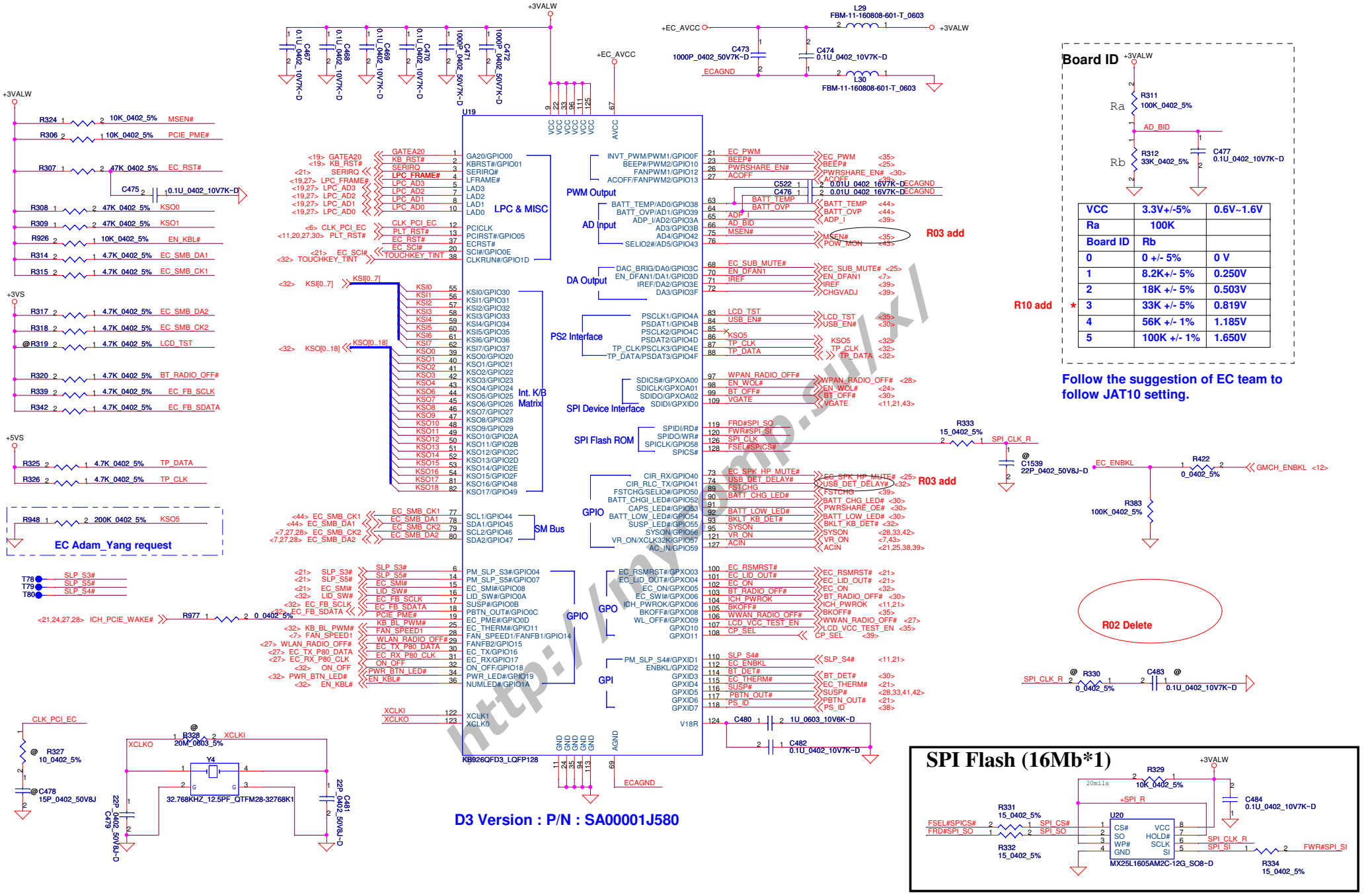
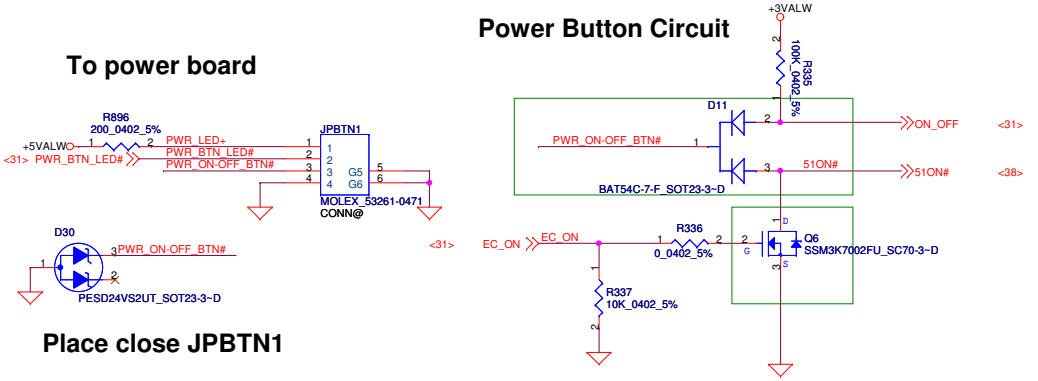


VCC	3.3V+/-5%	0.6V~1.6V
Ra	100K	
Board ID	Rb	
0	0 +/- 5%	0 V
1	8.2K+/- 5%	0.250V
2	18K +/- 5%	0.503V
3	33K +/- 5%	0.819V
4	56K +/- 1%	1.185V
5	100K +/- 1%	1.650V

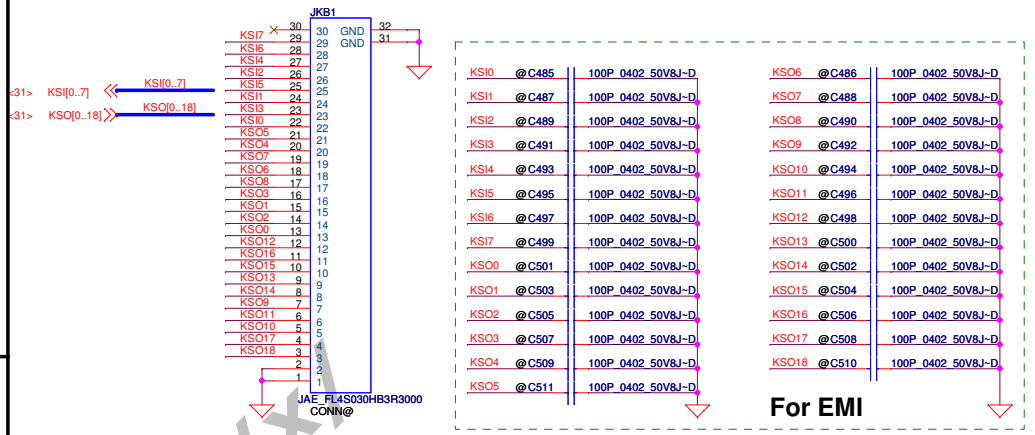
Power Button Circuit

To power board



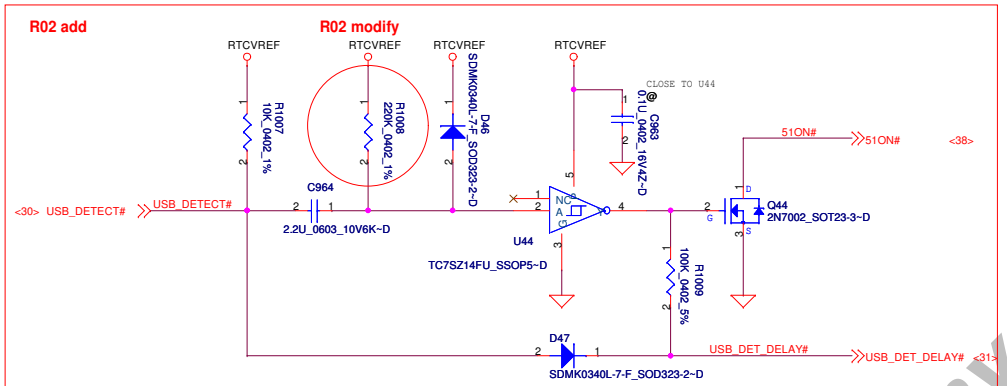
Place close JPBTN1

INT_KB_Conn.1



For EMI

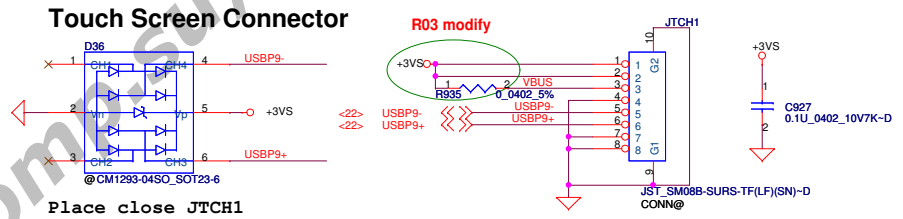
R02 add / R02 modify



Power share

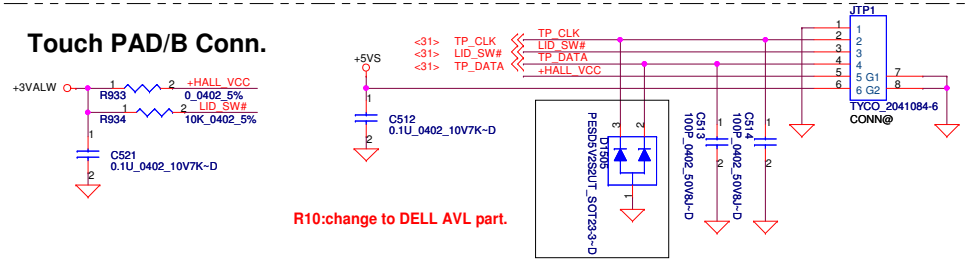
Touch Screen Connector

R03 modify



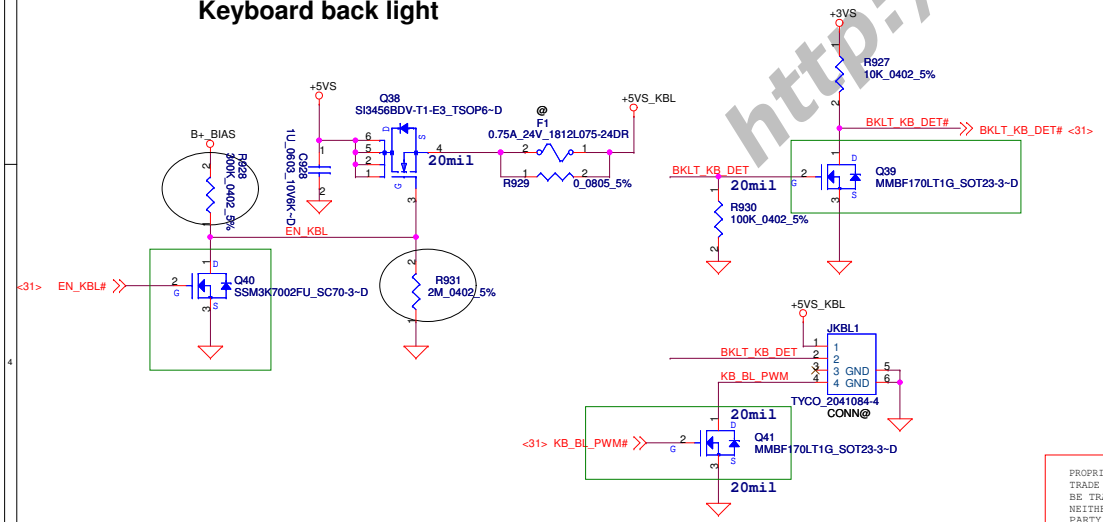
Place close JTCH1

Touch PAD/B Conn.



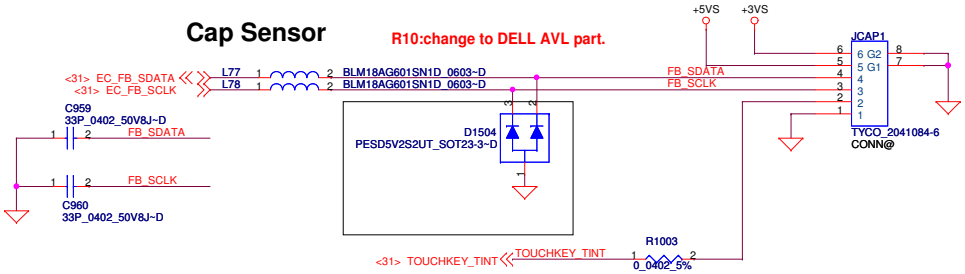
R10:change to DELL AVL part.

Keyboard back light



Cap Sensor

R10:change to DELL AVL part.



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	PWROK/BTN/KB/Touch Pad
Size	Document Number LA-5152P Rev A00
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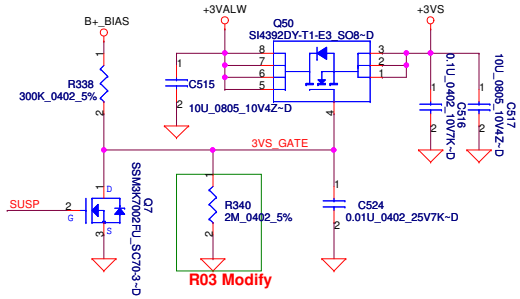
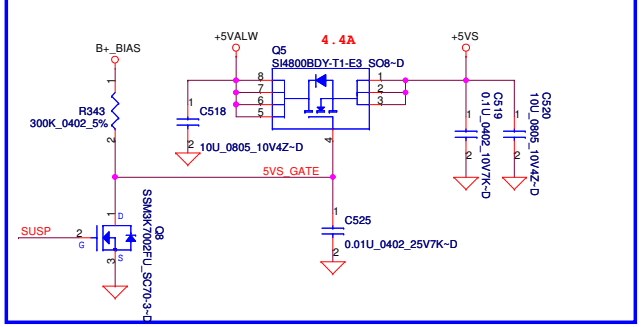
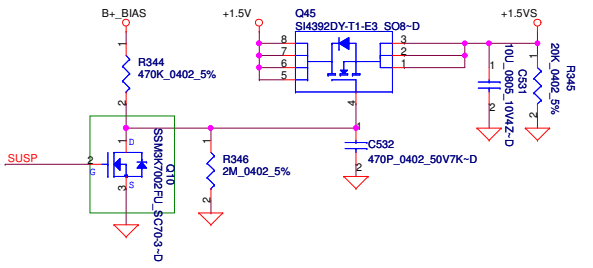
+3VALW to +3VS Transfer

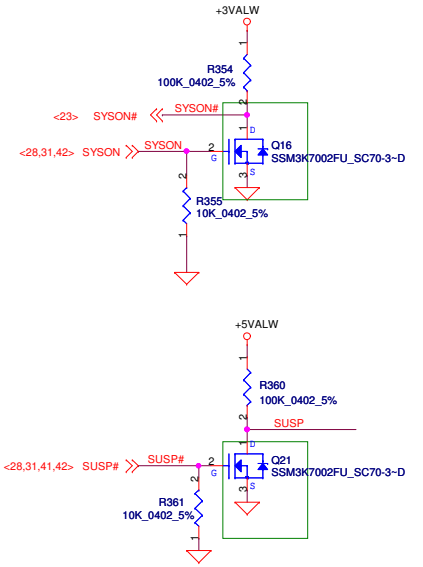


+5VALW to +5VS Transfer

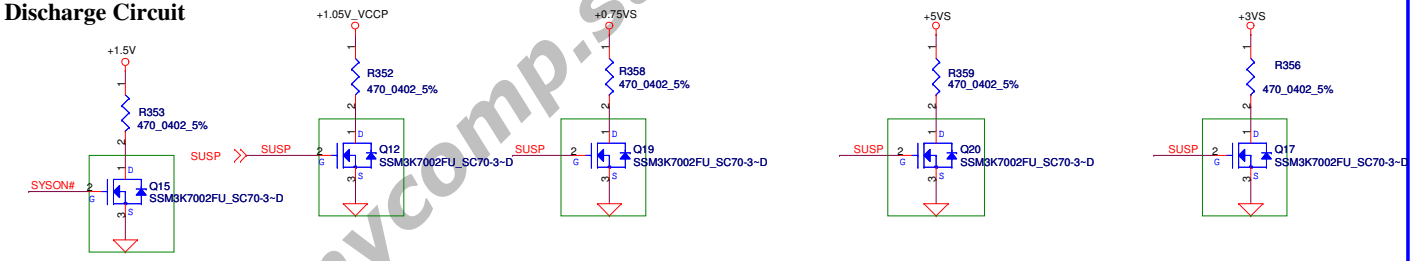


+1.5V to +1.5VS Transfer





Discharge Circuit



R03 Delete +3V_WLAN discharge circuit.

Compal Electronics, Inc.	
Title	DC/DC Circuits
Size	Document Number: LA-5152P
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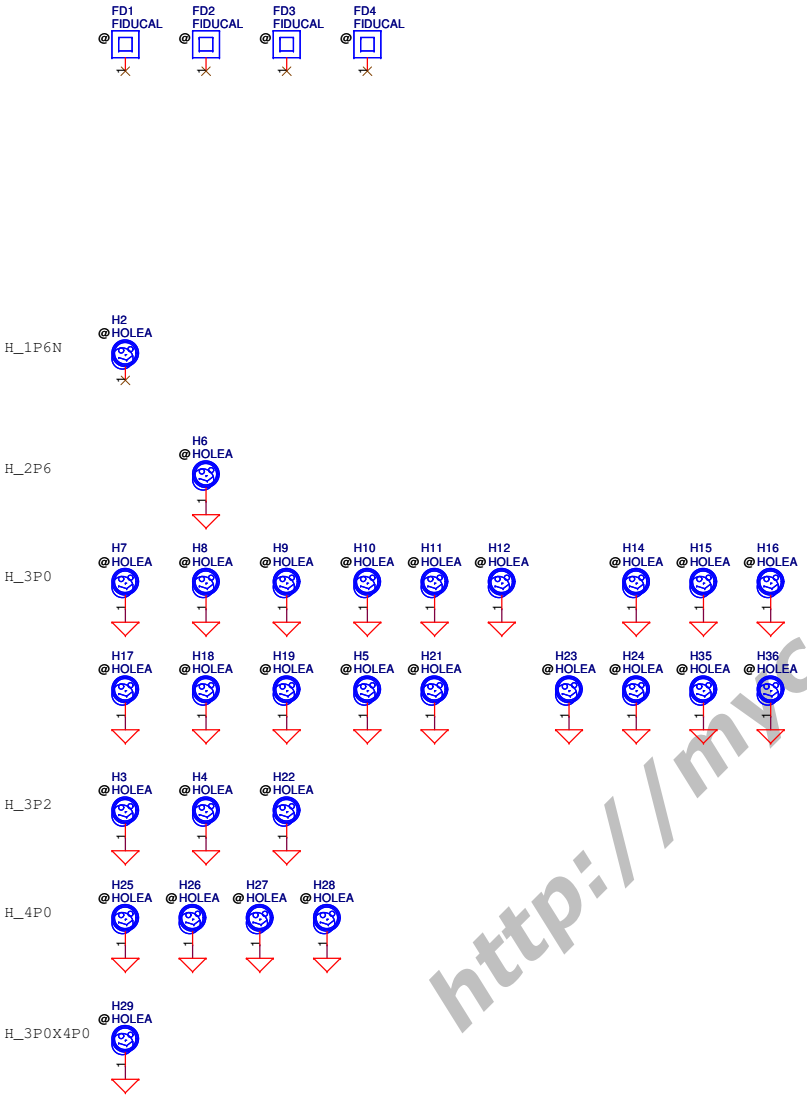

Compal Electronics, Inc.

Title: Screw

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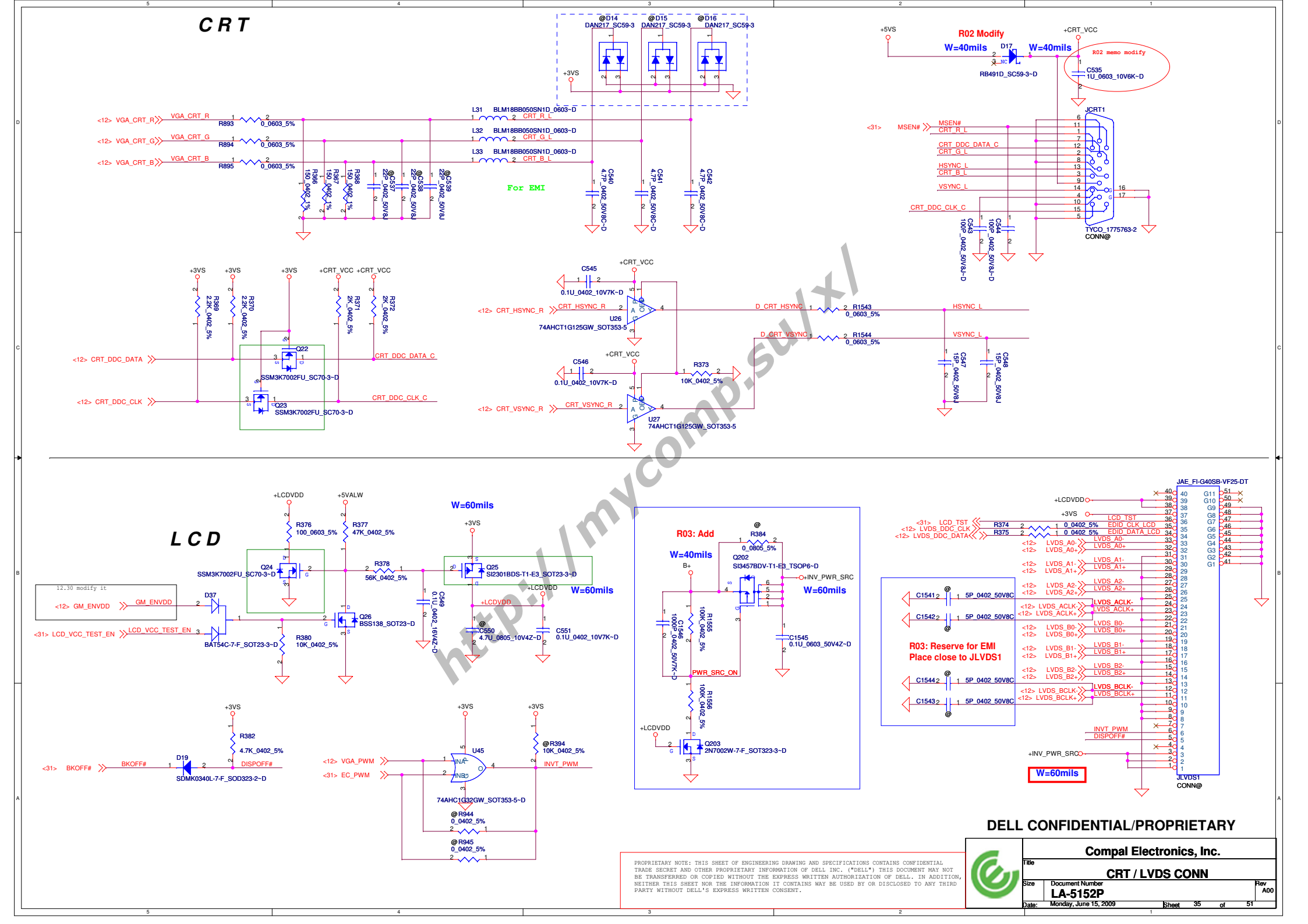

Recommended Equalization: [PC1,PC0]=01, 4dB

	ST	Parade
R1523	X	V
R1524	V	X
R1503	4.3K	499
R1525	V	X
R1526	V	X
R1527	V	X
R1528	V	X
R1529	V	X
U100	V	V
R1500	V	X
R1516	V	X
R1511	V	X
R1512	V	X
R1513	V	X
C1513	V	X
C1514	V	X
C1515	V	X
C1516	V	X

Vendor's suggestion for power saving.

Compal Electronics, Inc.

Title: HDMI CONN

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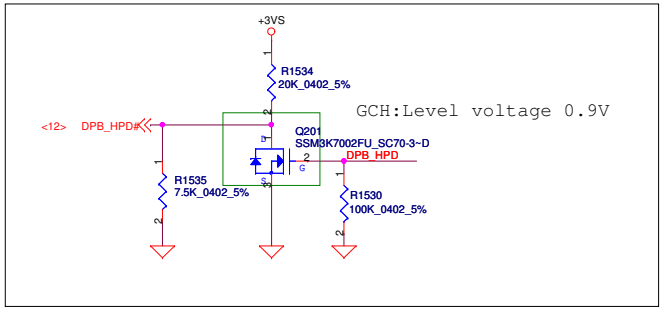
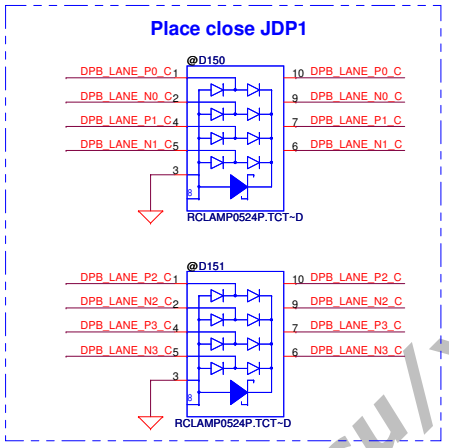
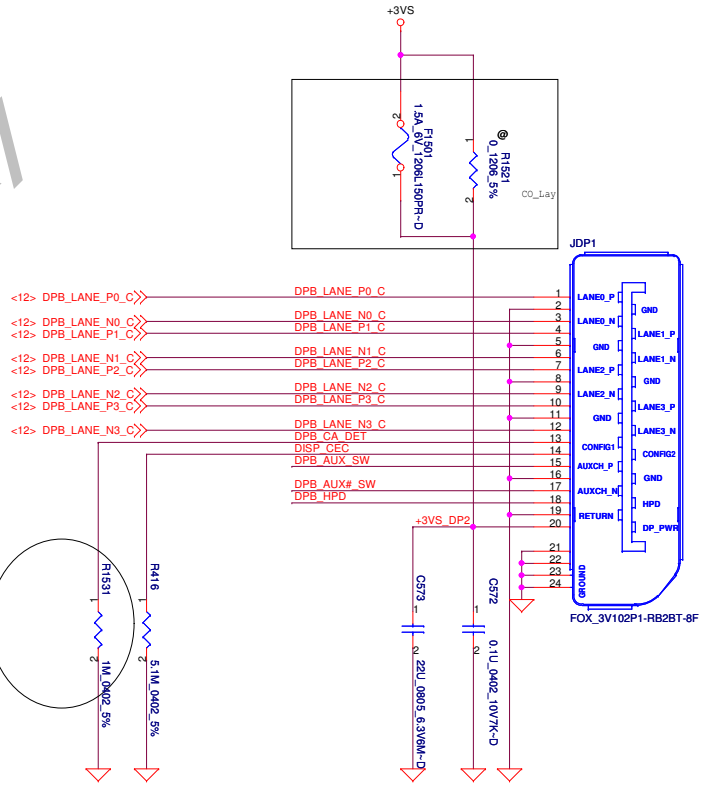
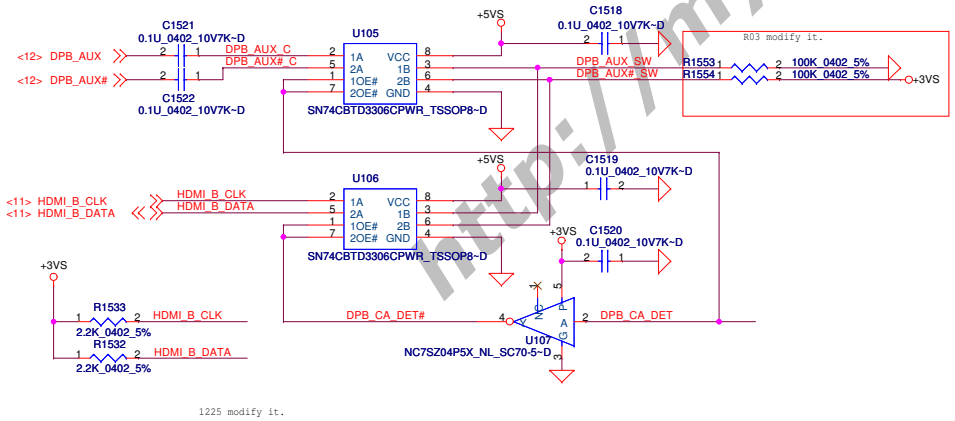






SW for MB side

DPB_CA_DET= 1 TMDS Signaling
DPB_CA_DET= 0 DP Signaling



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Display Port

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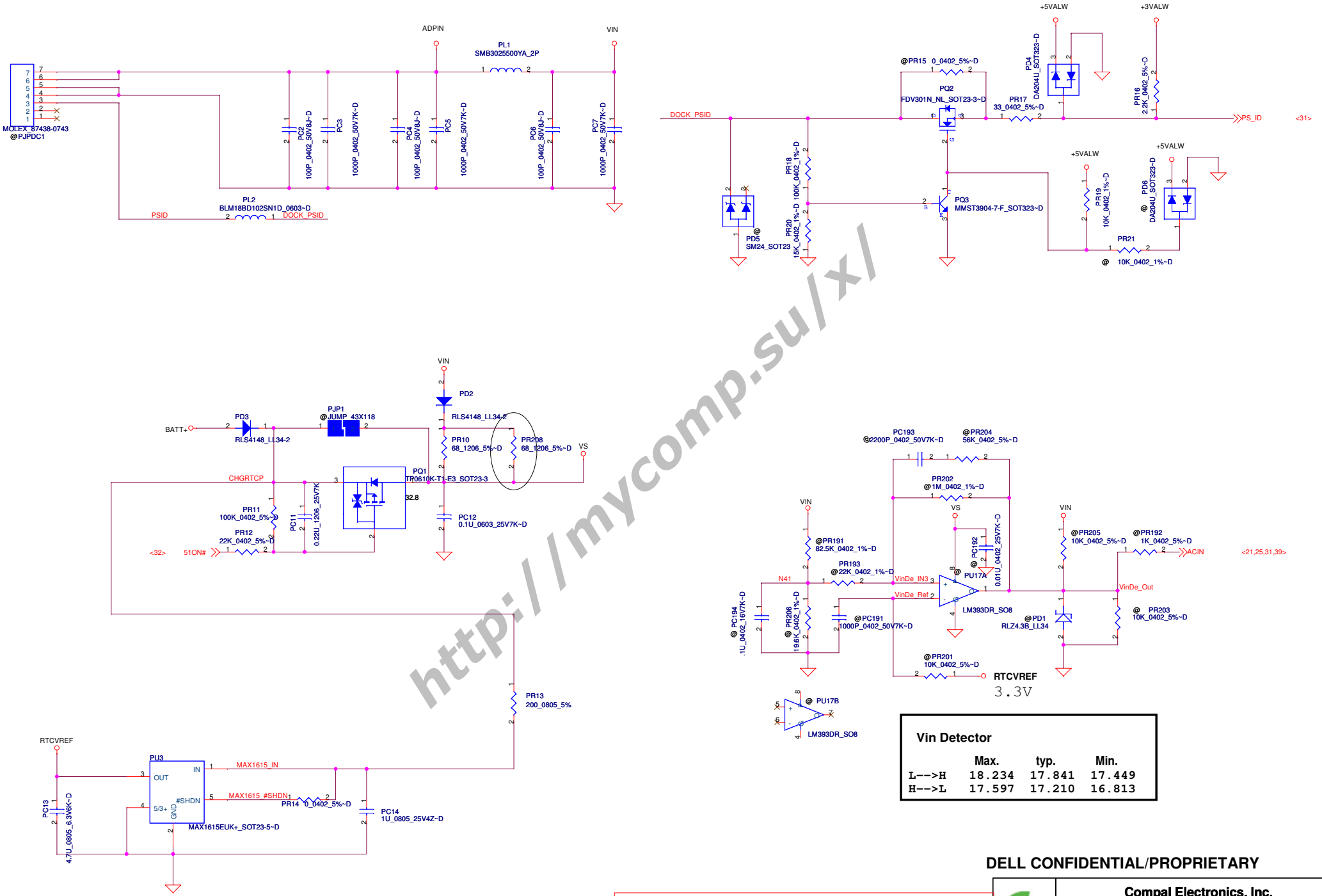
Date: Monday, June 15, 2009 | Sheet 37 of 51



Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	DCIN/Precharge
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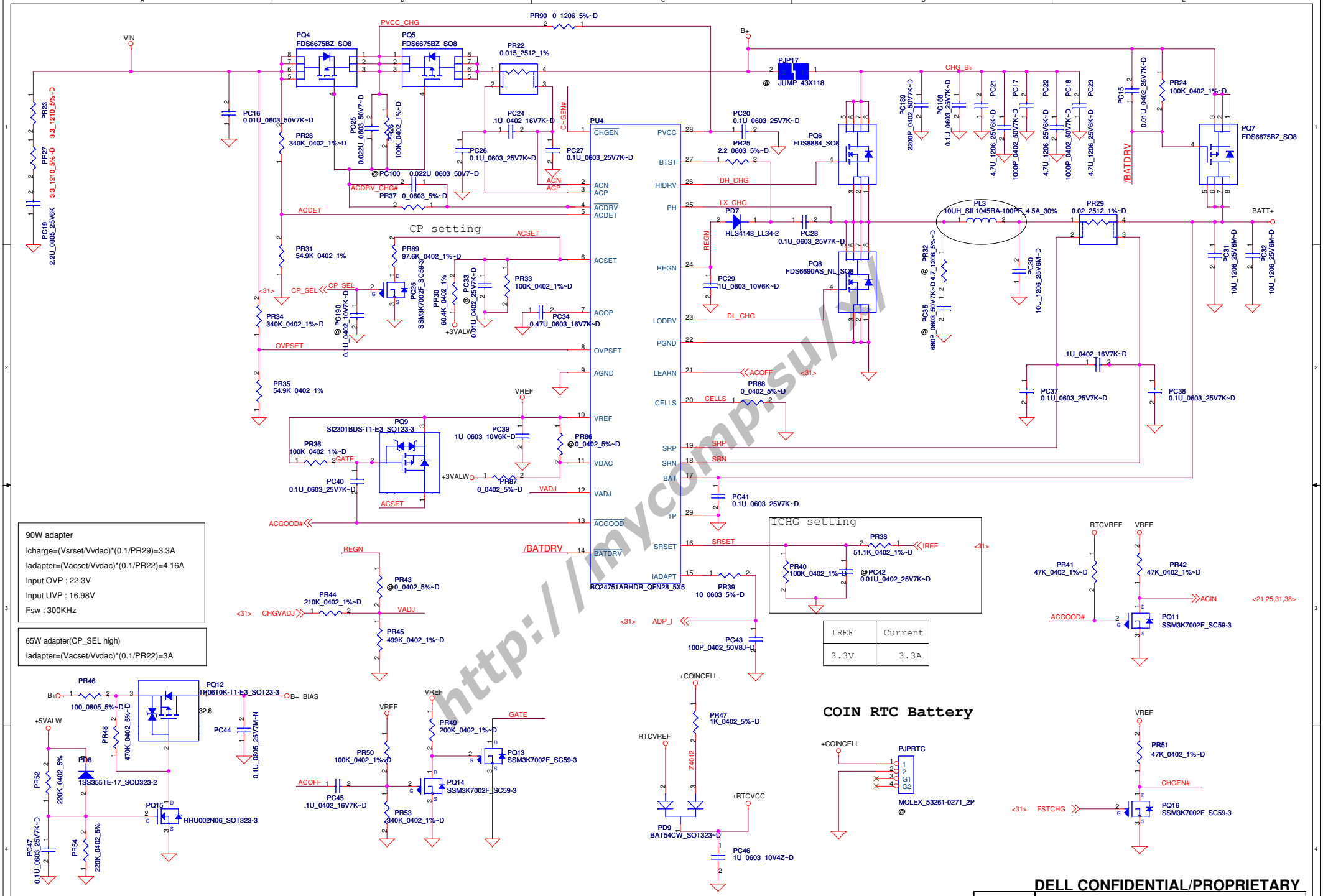

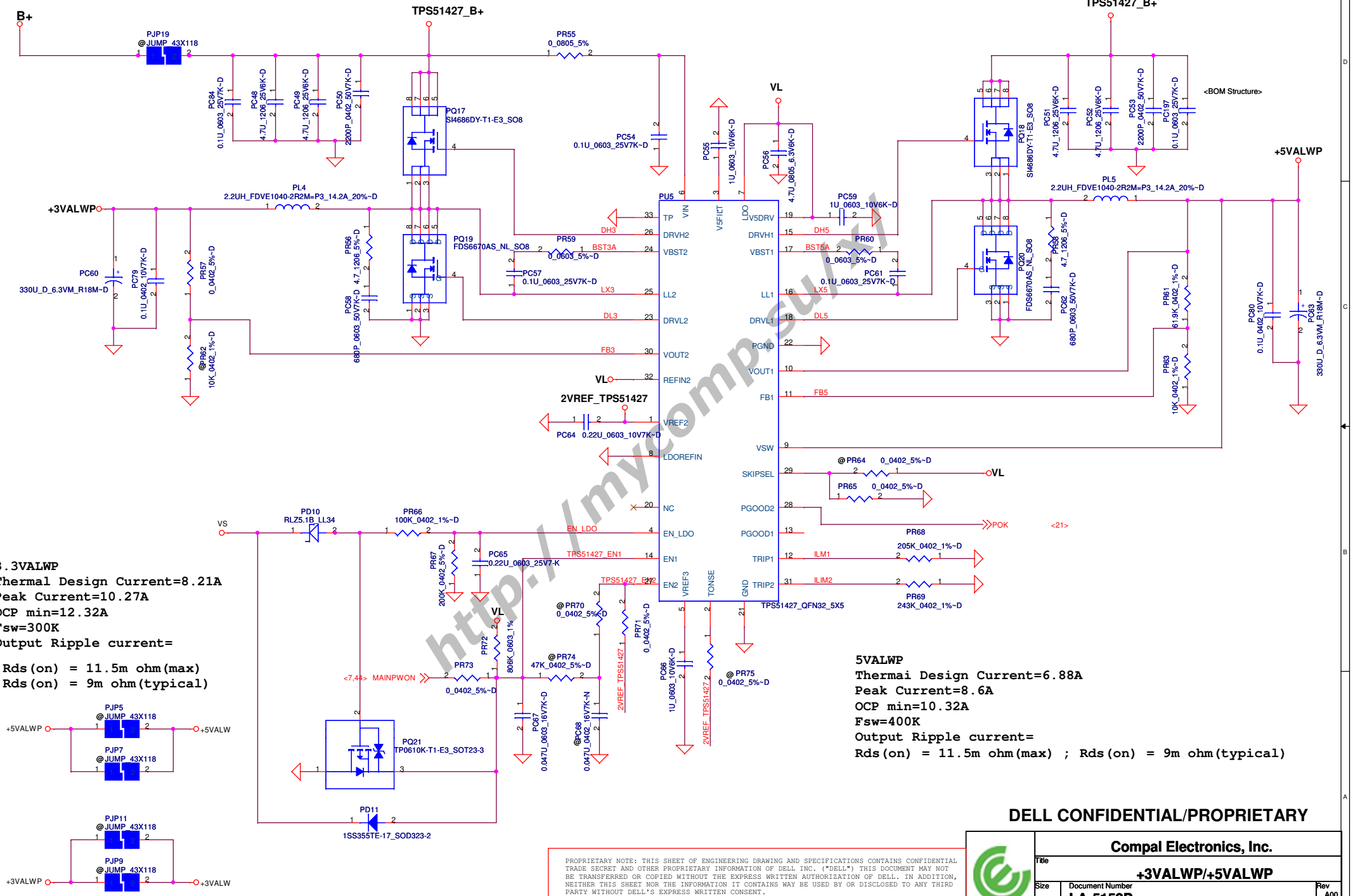

3.3VALWP
Thermal Design Current=8.21A
Peak Current=10.27A
OCP min=12.32A
Fsw=300K
Output Ripple current=

Rds(on) = 11.5m ohm(max)
Rds(on) = 9m ohm(typical)

5VALWP
Thermai Design Current=6.88A
Peak Current=8.6A
OCP min=10.32A
Fsw=400K
Output Ripple current=
Rds(on) = 11.5m ohm(max) ; Rds(on) = 9m ohm(typical)

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.	
Title	+3VALWP/+5VALWP
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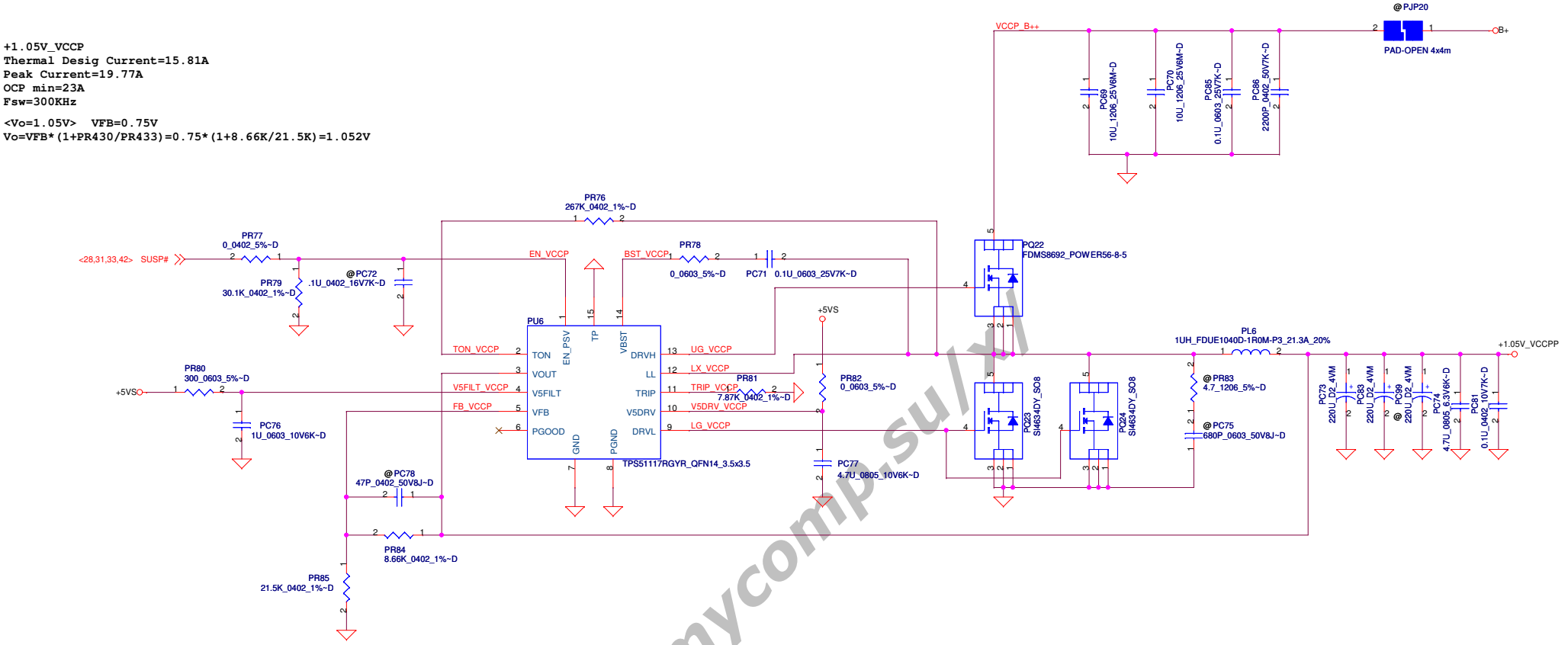
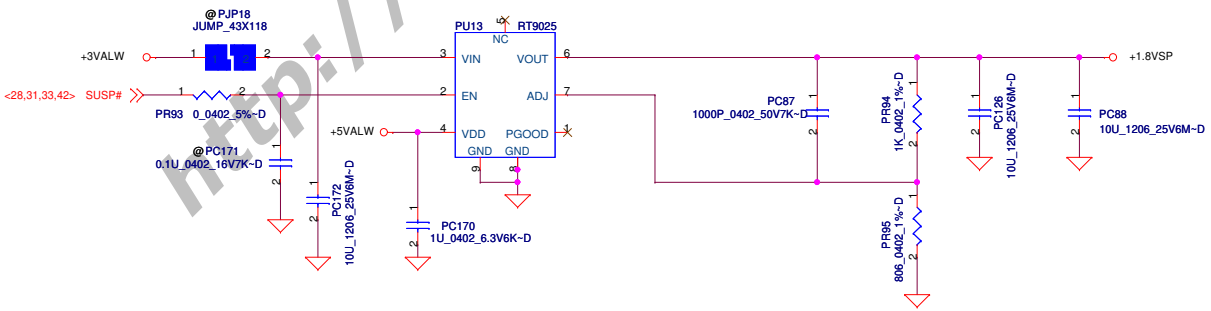
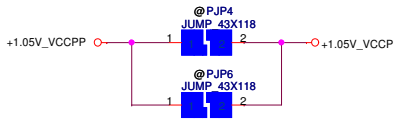
+1.05V_VCCP
Thermal Desig Current=15.81A
Peak Current=19.77A
OCP min=23A
Fsw=300KHz

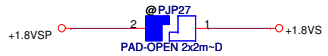
<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR430/PR433)=0.75*(1+8.66K/21.5K)=1.052V





+1.8VSP
Imax=0.67A
Vout=0.8*(PR94+PR95)/PR95=0.8*(1k+806)/806=1.79V





Compal Electronics, Inc.

Title: +1.05V_VCCP/+1.8VSP

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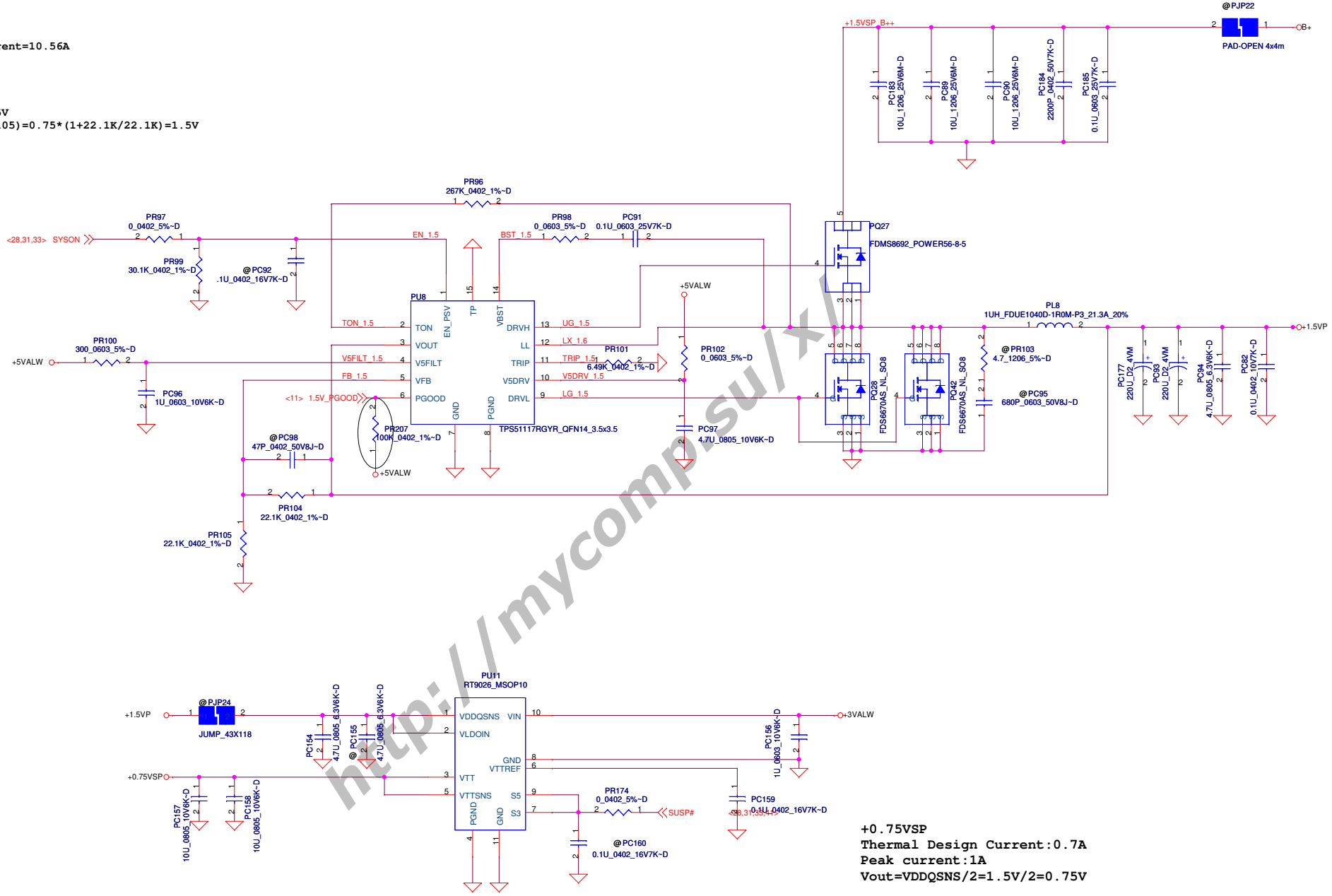
1.5V
Thermal Design Current=10.56A
Peak Current=13.2A
OCP min=15.84A
Fsw=298KHz

<Vo=1.5V> VFB=0.75V
Vo=VFB*(1+PR104/PR105)=0.75*(1+22.1K/22.1K)=1.5V



Compal Electronics, Inc.

Title: +1.5VSP/+0.75VSP

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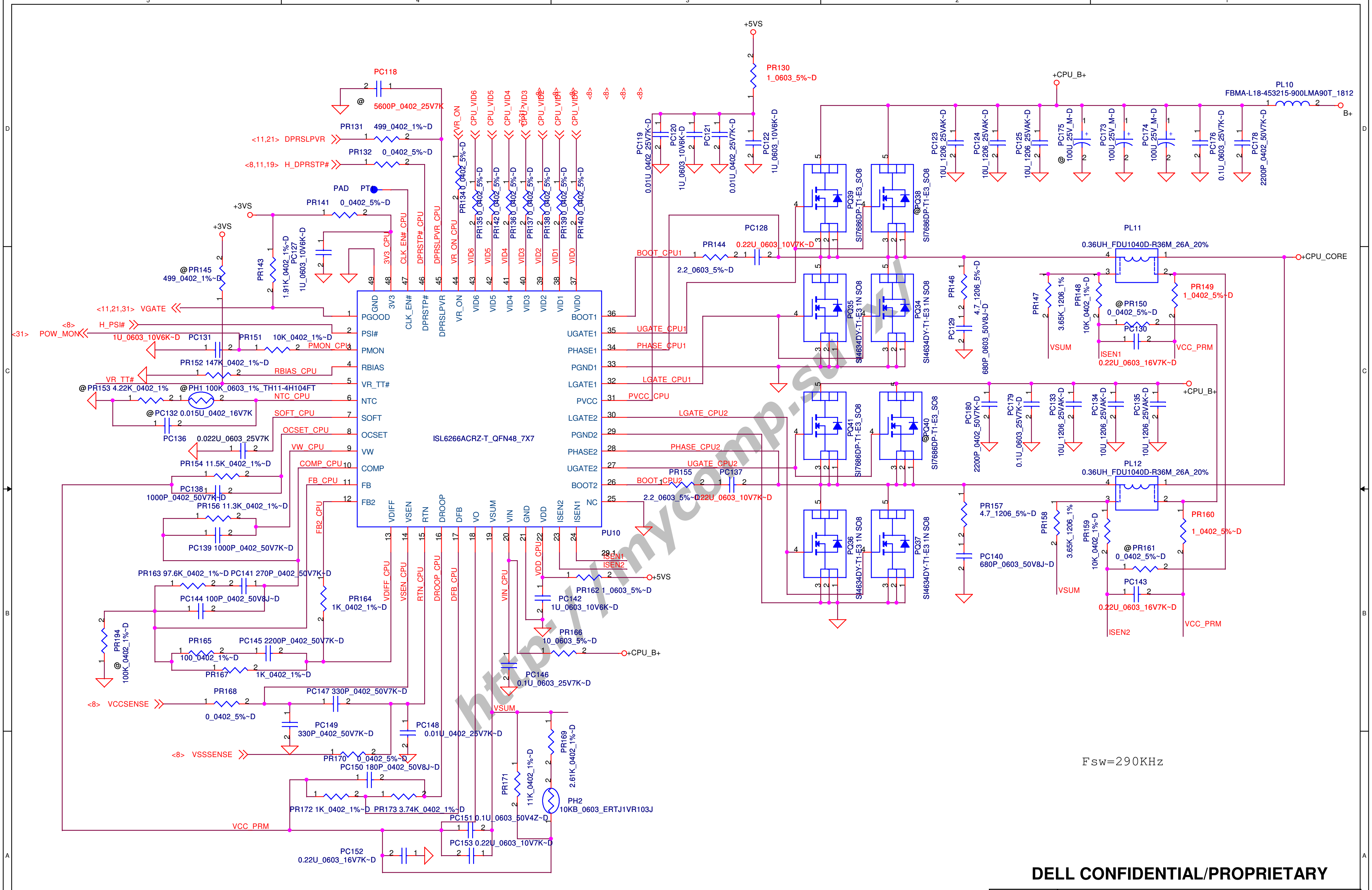

DELL CONFIDENTIAL/PROPRIETARY

	Compal Electronics, Inc.
Title	CPU_CORE
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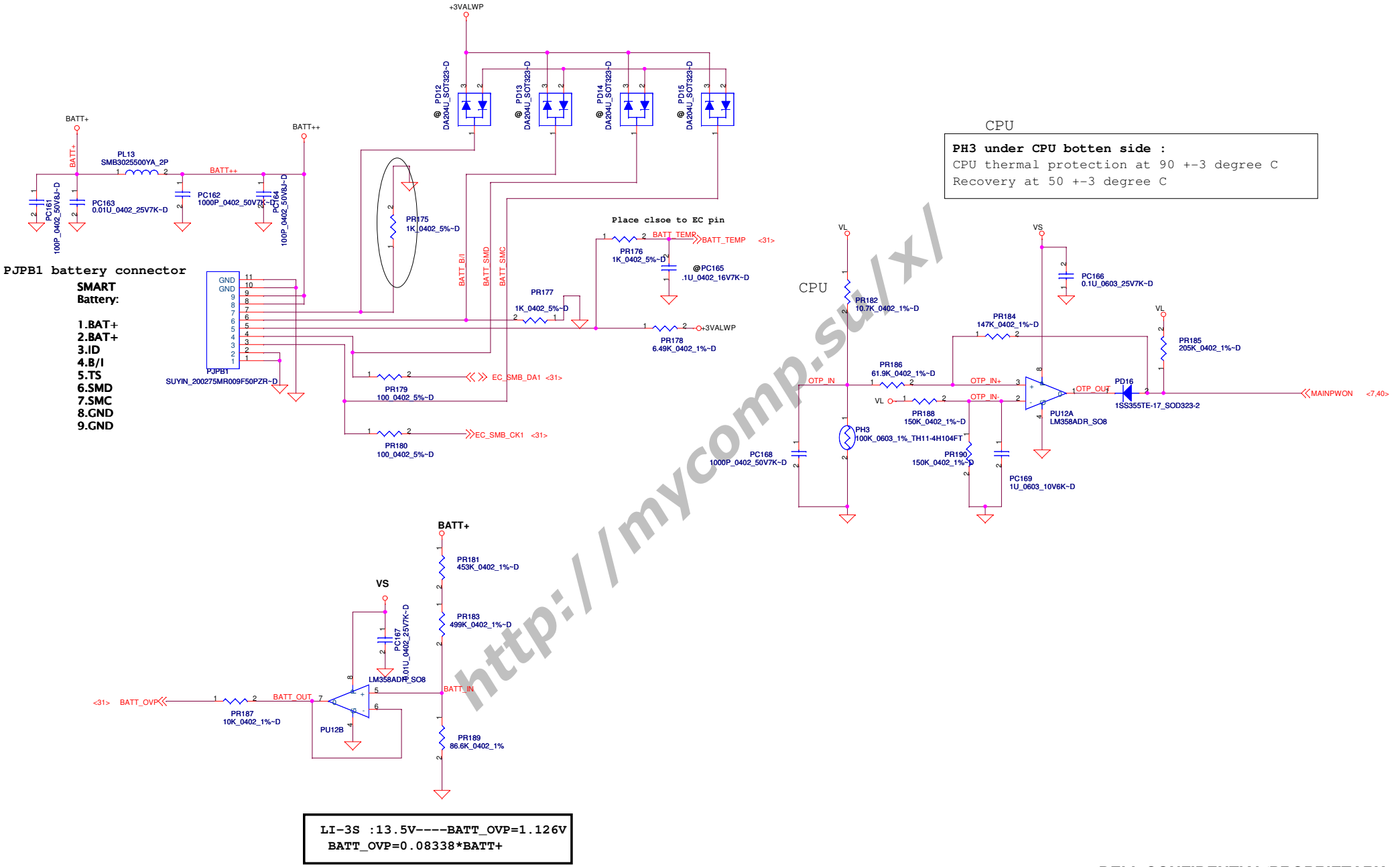
Battery Connect/OTP



CPU

PH3 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C

LI-3S :13.5V----BATT_OVP=1.126V
BATT_OVP=0.08338*BATT+

Compal Electronics, Inc.
Title: BATTERY CONN
Size: Document Number: LA-5152P
Rev: A00
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	06	Clock Generator	2009/03/03	Benson_Tung	Error connection of clock gne I2C.	Correct CLK_SMBDATA connect to U1.9 , CLK_SMBCLK connect to U1.10.	Rev02 (X01)
2	06	Clock Generator	2009/03/03	Benson_Tung	Error connection of CLK_PCIE_WPAN & CLK_PCIE_WPAN#	Correct WPAN CLK +/- signal of U1.	Rev02 (X01)
3	30	JCARD1	2009/03/03	COMPAL	1. Change JCARD1 pin 1 location to prevent cable twist. 2. Connect contact current rating is only 0.3 Ampere max.	1. Modify JCARD1 symbol 2. Add +5VALW pin count from 2 to 7 pins.	Rev02 (X01)
4	32	Keyboard	2009/03/03	Benson_Tung	Keyboard connector Pin 1 location is different with Keyboard module.	Correct keyboard pin 1 location to fit keyboard module.	Rev02 (X01)
5	32	Power share	2009/03/03	Benson_Tung	Power share didn't work.	Add power share schematic.	Rev02 (X01)
6	12	Cantiga (3 of 7)	2009/03/03	Benson_Tung	Error connection of LVDS CLK +/-.	1.Correct LVDS_ACLK+ connect to U4C.C40 2.Correct LVDS_ACLK- connect to U4C.C41 3.Correct LVDS_BCLK+ connect to U4C.A37 4.Correct LVDS_BCLK- connect to U4C.B37	Rev02 (X01)
7	33	DC/DC Interface	2009/03/03	Benson_Tung	Change DC to DC transfer of MOS parts	1. +3VALW to +3VS Ttransfer MOS change to U21 SI4800BDY-TI-E3 2. +5VALW to +5VS Ttransfer MOS change to U22 SI4800BDY-TI-E3 3. +1.5V to +1.5VS Ttransfer MOS change to Q45 SI4392DY-T1-E3	Rev02 (X01)
8	20	FFS	2009/03/03	Compal	Add FFS function	Add FFS circuit in page 20	Rev02 (X01)
9	4	Power Rail	2009/02/25	Bill_Huang	Correct error item.	Correct +3VS, +5VS Power consumption.	Rev02 (X01)
10	36	HDMI	2009/03/03	Benson_Tung	Error connection of Q200.3 and C1517.1 GND net name.	1.Change Q200.3 net form GND SIGNAL to GND. 2.Change C1517.1 net form GND SIGNAL to GND.	Rev02 (X01)
11	19-23	ICH9M	2009/03/04	Bill_Huang	Change ICH to consign P/N.	Change U6 P/N: form SA00002G11L to SA00002G12L.	Rev02 (X01)
12	35	CRT RGB EA	2009/03/10	Benson_Tung	CRT RGB signals EA failed on Rising / Falling time.	Change L31~L33 from SM01000AL00 (S SUPPRE_ CHENG-HANN MBK1608301YZF 0603) to SM01000BP0L (BLM18BB050SN1D_0603~D)	Rev02 (X01)
13	35	CRT Diode	2009/03/03	Benson_Tung	CRT diode forward current is about 1Amp, need to change part to prevent damage.	Change D17 from SC1B411D010 (S DIO RB411DT146 SOT23) to SCSB491DA0L (S SCH DIO RB491D SC59-3 ROHM)	Rev02 (X01)
14	37 35 26	Display Port VGA / LVDS Sub woofer / Speaker AMP	2009/03/04	Jan_Chang	Change JDP1,JLVDS1 and JWOOFER1 symbol.	1. Update JDP1 symbol. 2. Change JLVDS1 symbol to JAE_FI-G40SB-VF25-DT 3. Change JWOOFER1 symbol to MOLEX_53398-0271~D	Rev02 (X01)
15	31 19 24	EC_KB926/BIOS/Reed SW ICH9M(1/5)_LAN,HD,SATA,LPC Gigabit LAN_RTL8111DL	2009/03/04	Benson_Tung	Meet Xtal EA spec.	1.Change C479,C481 from 15P_0402_50V8J to 22P_0402_50V8J 2.Change C217,C864 from 12P_0402_50V8J to 15P_0402_50V8J 3.Change C318 from 27P_0402_50V8J to 33P_0402_50V8J	Rev02 (X01)
16	25	HD Audio_IDT92HD73C	2009/03/04	Benson_Tung	1. SPK_MUTE# change to controlled by HP1_JD or HP2_JD. 2. Meet HP EA spec.	1. Add U108 OR gate. 2. Change C336, C337, C349, C350 , C354, C355 from 1U_0603 to 2.2U_0805.	Rev02 (X01)
17	27	Mini Card_WLAN/WWAN	2009/03/06	Compal	To supprot EC TX/RX debug card.	Change EC_TX_P80_DATA & EC_RX_P80_CLK connect to JWWAN1 pin 49 & 51	Rev02 (X01)
22	30	USB/BlueTooth/Camera	2009/03/06	Compal	To prevent antenna effect at E-SATA re-driver.	Add R1012 & R1013 place close U40 Pin2 & Pin3 Add R1014 & R1015 place close U40 Pin 21 & Pin22	Rev02 (X01)
23	32	PWROK/BTN/KB/Touch Pad	2009/03/06	Compal	Add powershare schematic.	Add powershare schematic.	Rev02 (X01)
24	33	DC/DC	2009/03/06	Compal	1. To fit power budget	1a. Change U21 & U22 from DMN3030LSS-13 to SI4800BDY 1b. Change U25 SI4800BDY to Q45 SI4329DY	Rev02 (X01)
25		Market / Capacitor	2009/03/06	Compal	Due to Janpan produce Y5V no more in the fucture.	change C133,C138,C144,C152,C163,C251,C255,C281,C425 from SE000009W0L to SE107475M0L	Rev02 (X01)
26	23	ICH9M(5/5)_POWER&GND	2009/03/06	Compal	ICH coneect to ALW power rail have power wastage at S5 mode	Add MOSFET control circuit to reduce ICH power wastage at S5 mode.	Rev02 (X01)

Version Change List (P. I. R. List) Page 2

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
27	24	Gigabit LAN_RTL8111DL	2009/03/06	Compal	1. Prevent B+_BIAS damage Q3 2. Correct +LAN_DVDD12 power name 3. Meet LAN EMI test.	1. Add R1006 (1.5M_0402) 2. Correct C302 & C303 power source from +LAN_VDD12 to +LAN_DVDD12 3. Pop C873 ~ C880 , SE07168AC0L(S CER CAP 6.8P 50V C NPO 0402)	Rev02 (X01)
28	35	VGA / LVDS	2009/03/06	Compal	1. LCD panel need to be turned backlight under this crisis recovery mode. 2. when FN+ D is pressed during POST, the LCD will perform the LCD BIST test and boot to PSA directly	add a gate to OR VGA_PWM and EC_PWM signals	Rev02 (X01)
28	21	ICH9M(3/5)_PM,GPIO	2009/03/06	Compal	Error net name PBTN_OUT#	Correct U6C.R3 net to PBTN_OUT#	Rev02 (X01)
29	4	Power Rail	2009/03/06	Compal	Correct +1.5V to +1.5VS.DC/DC Interface chip name	Form 4800BDY change to SI4392DY	Rev02 (X01)
30	25	HD Audio_IDT92HD73C	2009/03/11	Compal	Meet audio HP EA spec	1.C354,C355,C336,C337 change to 2.2uF 0805 size X7R 2.Add a series 2k ohm resistor between these caps and the maxim amp U10,U12,. 3.At the pin of the maxim amp U10,U12 Pin 15 and U10,U12 Pin13 add a 220pF cap 0603 NPO to ground.	Rev02 (X01)
31	26	Speaker/Sub woofer AMP	2009/03/11	DELL	Gain setting to 20.6dB	1. C913,C914,C910,C909 form 6800P_0402_16V7K~D change to 2200P_0402_25V7K~D 2. R907,R902 100K_0402_1% to 280K 3. Delete C951,C952 0.015U_0402_16V7K part. 4.R900,R905 form 4.87K_0402 change to 43.2K_0402 5. U14 form MAX9736B change to MAX9736A 5.R901,R903,R906,R908 form 20K_0402 change to 25.5K_0402	Rev02 (X01)
32	34	Screws/LED/Switch	2009/03/11	ME	Modify MB drawing.	1. H2 change to NON-PTH 1.6mm. 2,. Delete H13 part	Rev02 (X01)
33	26 31 32	Speaker/Sub woofer AMP EC_KB926/BIOS/Reed SW PWROK/BTN/KB/Touch Pad	2009/03/11	EMC	Follow EMC request.	1. D20,D21 (PACDN042Y3R_SOT23-3) change to POP. 2. R330 (0_0402), C483 (0.1U_0402) change to POP. 3. Reserve ESD diode D1505 PJDLC05_SOT23-3 on touchpad 4. Change D1504 part to PJDLC05_SOT23-3.	Rev02 (X01)
34	29	ODD/SATA HDD	2009/03/11	ME	Follow ME request.	JODD1 form MOLEX_47639-4000_NR change to MOLEX_47639-3000_13P	Rev02 (X01)
35	26	Speaker/Sub woofer AMP	2009/03/11	COMPAL	Band-Pass Filiter,fc=100 Hz, 500Hz, Av=1.45V/V	form MAX9737 change to MAX9736A. please see page 26	Rev02 (X01)
36	27	Display Port	2009/03/11	COMPAL	Meet HDMI test	1. R1518 0_1206 change to non-pop. 2. F1500 1.5A_6V_1206L150PR~D change to POP.	Rev02 (X01)
37	6 19 27 31	Clock Generator CK505 ICH9M(1/5)_LAN,HD,SATA,LPC Mini Card_WLAN/WWAN EC_KB926/BIOS/Reed SW	2009/03/13	Compal RF	Follow RF request.	RF reserve 1.C1531 part. CLK_14M_ICH need close U1 2.C1532 part. HDA_BITCLK_AUDIO need close U6 3.C1533 part.PCI_CLK need close U1 4.c1534 part. CLK_PCI_EC need close U1 5. C1535,C1536 part. Reserve 47 pF for +1.5V and +3V 6. C1537, C1538 part. Reserve 47 pF for +1.5V and +3V 7. Move R333 close to U19 and need reserve C1539 part.	Rev02 (X01)
38	27	USB/BlueTooth/Camera	2009/03/13	COMPAL	Delete E-SATA by-pass R.	Delete R1012,R1013,R949,R950,R951,R952,R1014,R1015 part .	Rev02 (X01)
39	25	HD Audio_IDT92HD73C	2009/03/13	COMPAL	Modify Audio control circuit.	please see page 25 about U46,U42,U108,U48,U47,U41,Q48 parts.	Rev02 (X01)
40	33	DC/DC Interface	2009/03/13	COMPAL	For reduce power consumption	1.R344 change to 470K. 2.R346 change to 2M.	Rev02 (X01)
41	31	EC_KB926/BIOS/Reed SW	2009/03/14	COMPAL	correct SPI_CLK_R non_pop parts.	R330,C483 change to non_pop.	Rev02 (X01)
42	36	HDMI	2009/03/16	COMPAL	Meet HDMI chip spec. X7616831L04 ALT. GROUP PARTS S-(SA00002C610) KAT00	R1500 change to pop part..	Rev02 (X01)
43	11	Cantiga (2 of 7)	2009/04/27	COMPAL	Correct HDMI CLK/DATA part B and C connect	DDPC_CTRLCOK should be connecting HDMI_C_CLK. =>Port C DDPC_CTRLDATA should be connecting HDMI_C_DATA. =>Port C SDVO_CTRLCLK should be connecting HDMI_B_CLK. =>Port B SDVO_CTRLDATA should be connecting HDMI_B_DATA. =>Port B	Rev03 (X02)

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
44	36	HDMI Conn	2009/04/27	COMPAL	Follow EMI request of HDMI	L1504,L1505, L1506, L1507 parts change to DLW21SN900HQ2L	Rev03 (X02)
45	37	Display Port	2009/04/27	COMPAL	Follow INTEL Design Guide DP AUX circuit.	DPB_AUX_SW need connect R1553 (100kohm) to pull down. DPB_AUX#_SW need connect R1554 (100Kohm) to pull up +3VS.	Rev03 (X02)
46	33	DC/DC Interface	2009/04/28	COMPAL	Delete +3V_WLAN discharge circuit.	Delete +3V_WLAN discharge circuit.	Rev03 (X02)
47	28	Mini Card_WPAN / Express	2009/04/28	COMPAL	Chagne JEXP1 symbol.	JEXP1 change to TAITW_PXPXAE-000LBS2ZZ4N0_NR part.	Rev03 (X02)
48	34	Screws/LED/Switch	2009/04/29	COMPAL	Original H1 is fan alignment pin , but now cancel this function.	Delete H1 part.	Rev03 (X02)
49	25	HD Audio_IDT92HD73C	2009/04/29	COMPAL	Change EAPD# pull up to (+3VALW).	Change R1549.1, U46.5 and U47.5 to +3VALW power	Rev03 (X02)
50	23	ICH9M(5/5)_POWER&GND	2009/04/29	COMPAL	Change +ICH_V5REF_RUN and SUS resistance	R233,R234 form 10_0402_5% change to 100_0402_5%	Rev03 (X02)
51	32	PWROK/BTN/KB/Touch Pad	2009/04/30	COMPAL	follow EMC request.	1.Change L77 and L78 from 120 ohms to 600 ohms bead. 2. Implement ESD diode on cap sensor D1504 PJDLC05_SOT23-3 3. Implement ESD diode on TP_CLK and TP_DATA for touchpad D1505 PJDLC05_SOT23-3 4. Reserve PES24VS2UT_SOT23-3 ESD diode for speaker connector of D20, D21	Rev03 (X02)
52	23 24 35	ICH9M(5/5)_POWER&GND Gigabit LAN_RTL8111DL CRT / LVDS CONN	2009/04/30	COMPAL	Change to PSL parts	D2,D3,D4,D5,D6,D7,D19 form SC1H751H01L S DIO CH751H-40PT SOD-323 Change to SCS0340L01L SDMK0340L-7-F_SOD323-2~D	Rev03 (X02)
53	07 30	Penryn(1/3)-AGTL+/ITP-XDP USB/BlueTooth/Camera	2009/04/30	COMPAL	C19,C21,C463,C935 form S CER CAP 10U 16V Z F(Y5V) 1206 H1.15 change to SE053106Z8L S CER CAP 10U 10V Z Y5V0805 H1.25		Rev03 (X02)
53	07 30	Penryn(1/3)-AGTL+/ITP-XDP USB/BlueTooth/Camera	2009/04/30	COMPAL	Modify DC to DC circuit.	Modify +3VALW to +3VS and +5VALW to +5VS circuit.	Rev03 (X02)
54	23	ICH9M (5/5)	2009/05/01	COMPAL	Reduce ICH power consumption at S5 mode.	Populate Q47 and non-populate R1022	Rev03 (X02)
55	30	USB/BlueTooth/Camera	2009/05/01	COMPAL	Change E-SATA Output Swing Control TO 1.2x	1.Non-populate R958, R959 2. R953 change to 390 ohm.	Rev03 (X02)
56	30	USB/BlueTooth/Camera	2009/05/01	COMPAL	Solve USB Power Share fail issue.	Swap GPIO for USB_DET_DELAY# and EC_SPK_HP_MUTE#.	Rev03 (X02)
57	31	EC_KB926/BIOS/Reed SW	2009/05/04	COMPAL	Support S5 Power on when CRT insert	Pull-up MSEN# from +3VS to +3VALW	Rev03 (X02)
58	31	EC_KB926/BIOS/Reed SW	2009/05/04	COMPAL	FFS alert signal will change to other GPIO. Because original PIRQH is by USB controller used.	FFS change int to PIRQ setting from PIRQH to PIRQE	Rev03 (X02)
59	25	HD Audio_IDT92HD73C	2009/05/04	COMPAL	Change package fom 0603 to 0402.	C1527, C1528, C1529, C1530 Change to 270P_0402_50V7K~D	Rev03 (X02)
60	35	VGA / LVDS	2009/05/05	COMPAL	Add MOSFET circuit for LVDS converter power		Rev03 (X02)
61	24	ICH9M(5/5)_POWER&GND	2009/05/06	COMPAL	Modify +3VALW_S5_ICH circuit.	R972 form 470Kohm change to 300Kohm. R973 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
62	35	VGA / LVDS	2009/05/06	COMPAL	Modify Keyboard back light circuit.	R928 form 470Kohm change to 300Kohm. R931 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
63	24	Gigabit LAN_RTL8111DL	2009/05/07	COMPAL	Modify LAN_IO power circuit.	R236 form 470Kohm change to 300Kohm. R1540 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
64	26	Speaker/Sub woofer AMP	2009/06/04	COMPAL	For Part source	C901, C902, C903, C916, C918, C977 form SE00000NZ0L (S CER CAP 22U 25V K X7R 1210 H2.5) change to SE00000GF8L (S CER CAP 22U 25V K X5R 1210 H2.5)	Rev10 (A00)
65	30	USB/BlueTooth/Camera	2009/06/04	COMPAL	due to E-SATA connector doesn't sopport E-SATA detect function.	De_pop SB00000960L (S TR SSM3K7002FU 1N SC70-3) Location: Q11	Rev10 (A00)

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66	32	PWROK/BTN/KB/Touch Pad	2009/06/04	Compal	Change to DELL AVL Part	Change PN: SCA00000A00 (S ZEN ROW PJDLC05 3P C/A SOT23) to SCA00000J0L (S ZEN ROW PESD5V2S2UT 3P C/A SOT23 ESD) Location: D1504, D1505	Rev10 (A00)
67	25	HD Audio_IDT92HD73C	2009/06/04	Compal	Solve S0 to S3 pop noise of HP.	R1549 change to De_POP.	Rev10 (A00)
68	12	CANTIGA((3/7)-VGA/LVDS/TV	2009/06/04	Compal	CRT_HSYNC and CRT_VSYNC net name error	1. R116.1 net change to CRT_HSYNC_R 2. R117.1 net change to CRT_VSYNC_R	Rev10 (A00)
69	36	HDMI	2009/06/04	Compal	Cancel solder mask of by pass 0 ohm	1. Cancel solder mask R1517,R1515,R1514,R1507,R1509,R1508,R1522,R1510 parts. 2. Cancel solder mask R1521 part. 3. Cancel solder mask L26,L71,L72,L27 parts.	Rev10 (A00)
70	31	EC_KB926/BIOS/Reed SW	2009/06/04	Compal	Change Board ID	R312 change to 33Kohm	Rev10 (A00)
71			2009/06/04	Compal	Short by-pass 0 ohm	short parts of R2,R4,R3,R5,R6,R7,R8,R10,R12,R42,R43,R16,R17,R18,R19,R21,R23, R26,R28,R31,R33,R35,R37,R40,R39,R14,R15,R44,R99,R94,R134,R1004,R884,R235, R942,R248,R250,R285,R911,R912,R913,R914,R291,R918,R921,R919,R920,R915,R916, R917,R922,R923,R924,R925,R292,293,R292,R293,R294,R298,R295,R296	Rev10 (A00)
72	26	Speaker/Sub woofer AMP	2009/06/08	Compal	Main speaker AMP gain setting to 13dB	1. Change C908,C912 form 0.22uF to 0.1uF. 2. Change R903,R908 form 25.5Kohm to 16.5Kohm 3. Change R901,R906,R902,R907 form 280Kohm to 182Kohm 4. Change R904,R909 form 16.9ohm to 17.8Kohm 5. Change R900,R905 form 43.2K ohm to 11Kohm	Rev10 (A00)
73	26	Speaker/Sub woofer AMP	2009/06/08	Compal	Modify Main speaker AMP SHDN and mute # control circuit	1. Add D1507, R1558, C1547 diode and RC delay time of MUTE# pin.	Rev10 (A00)
74	30	USB/BlueTooth/Camera	2009/06/08	Compal	Solve E-SATA re-driver issue	Chagne U40 from SA00002D80L (S IC PI2EQX3201BZFEX TQFN 36P) to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)	Rev10 (A00)
75	25	HD Audio_IDT92HD73C	2009/06/08	Compal	Support unboot pc-beep sound function	Pop R1549	Rev10 (A00)
76	27	Mini Card_WLAN/WWAN	2009/06/15	Compal	delete short trace of jump	Delete R1010,R1011,R911,R912 pin1 and pin2 connect trace.	Rev10 (A00)

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01	40	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +5VALW OCP to 13.56A	Change PR68 from P/N:SD03429438L (294K +-1% 0402) to SD03433238L (332K +-1% 0402)	X01
02	40	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +3VALW OCP to 14.26A	Change PR69 from P/N: SD03424938L (249K +-1% 0402) to SD03434038L (340K +-1% 0402)	X01
03	41	+1.05V_VCCP/ +1.8VSP	01/22	Compal Mike	Setiing +1.05V_VCCP OCP to 23A	Change PR81 from P/N: SD03480618L (8.06K +-1% 0402) to SD03493118L (9.31K +-1% 0402)	X01
04	42	+1.5VSP/+0.75VSP	01/22	Compal Mike	Setiing +1.5VSP OCP to 15.84A	Change PR101 from P/N: SD03413728L (13.7K +-1% 0402) to SD03410528L (10.5K +-1% 0402)	X01
05	38	DCIN/Precharger	01/22	Compal Mike	Common circuit design modify	Change PR10 from P/N: SD00103308L (33 +-5% 1206) to SD011680A8L (68 +-5% 1206) Add PR208 SD011680A8L (68 +-5% 1206) parallel with PR10	X01
06	42	+1.5VSP/0.75VSP	01/22	Compal Mike	HW need to use +1.5VSP PGOOD signal,so need to add a pull high resister.	Add PR207 SD03410038L (100K +-1% 0402) between PU8 pin6 and PR97 pin 2.	X01
07	46	Charger	02/09	Compal Mike	Take off Cells selector function.	Populate PR88,take off PR37 and PQ10,change PR175 from 47K to SD02810018L(1K +-5% 0402)	X01
08	43	CPU_CORE	02/24	Compal Mike	Change CPU_CORE low-side MOSFET	Change PQ34,PQ35,PQ36,PQ37 from (SI4430BDY-T1-E3 1N SO-8) to SB00000DA00(SI4634DY-T1-E3 1N SO8)	X01
09	43	CPU_CORE	02/24	Compal Mike	HW don't need to use VR_TT# signal,so depopulate pull high resister.	Depopulate PR145 SD03449908L(499 +-1% 0402)	X01
10	43	CPU_CORE	02/24	Compal Mike	Change input cap from X7R(85℃) to X6S(105℃)	Change PC123,PC124,PC125,PC133,PC134,PC135 from (10U 25V M X5R1206 H1.6) to SE153106K8L(10U 25V K X6S 1206 H1.6)	X01
11	40	+3VALWP/+5VALWP	02/24	Compal Mike	Take off Manufacturer:COMPOSTAR from PC64	Change PC64 from P/N: SE080224K8L (.22U 10V K X7R 0603) to SE080224M8L (.22U 10V K X7R 0603)	X01
12	44	BATTERY CONN	02/24	Compal Mike	Take off non-PSL Manufacturer:Panjit	Change PQ45,PQ46 from P/N: SB000006800 (2N7002W T/R7 1N SOT-323) to SB00000B30L (PMF3800SN 1N SC70-3)	X01
13	39	Charger	02/24	Compal Mike	Take off non-Lead Free material.	Change PR29 from P/N: SD021200D0L (S RES 1W .02 +-1% 2512) to SD000001F0L (S RES 1W .02 +-1% 2512 50PPM/C)	X01
14	41	+1.05V_VCCP	02/24	Compal Mike	Change choke setting	Change PL6 from SH00000BQ0L (2.2UH +-20% MPLC1040L2R2 11A) to SH000009U00 (1UH +-20% FDUE1040D-1R0M=P3 21.3A)	X01
15	40	+3VALWP/+5VALWP	02/24	Compal Mike	Change choke reated current from 11A to 14.2A	Change PL4,PL5 from SH00000BQ0L (2.2UH +-20% MPLC1040L2R2 11A) to SH00000CG0L (2.2UH 20% FDVE1040-2R2M=P3 14.2A)	X01
16	38	DCIN / Precharge	03/03	Compal Antony	Prevent diode breakdown from battery inrush current	Change PD3 from SCS00002G00 to SC11N414880	X01

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17	38	DCIN / Precharge	03/03	Compal Antony	Change part number to L-end	Change PD4 part number from SC1A204U000 to SC1A204U00L	X01
18	40	+3VALWP/+5VALWP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR68 from 332K ohm to 205K ohm	X01
19	40	+3VALWP/+5VALWP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR69 from 340K ohm to 243K ohm	X01
20	41	+1.05V_VCCP/ +1.8VSP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR81 from 9.31K ohm to 7.87K ohm	X01
21	41	+1.05V_VCCP/ +1.8VSP	03/03	Compal Antony	Stabilize output voltage	Add PC83 220uF Capand Reserve PC99 Cap space to output	X01
22	42	+1.5VSP/+0.75VSP	03/03	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR101 from 10.5K ohm to 6.49K ohm	X01
23	43	CPU_CORE	03/03	Compal Antony	To avoid noise	Add PC176、PC179 0.1uF Cap to +CPU_B+	X01
24	43	CPU_CORE	03/03	Compal Antony	To avoid noise	Add PC178、PC180 2200pF Cap to +CPU_B+	X01
25	43	CPU_CORE	03/03	Compal Antony	Reserve space for load line shift control	Reserve PR194 space	X01
26	43	CPU_CORE	03/16	Compal Antony	To improve transient response	Change PC151 from 0.068uF to 0.1uF	X01
27	43	CPU_CORE	03/16	Compal Antony	Let difference of CPU Load Line and Spec smaller than 2mV	Change PR173 from 3.57K ohm to 3.74K ohm	X01
28	44	BATTERY CONN	03/16	Compal Antony	Disable Hardware CPU OTP circuit	Reserve PQ45、PQ46、PR199、PR200 space	X01
29	39	Charger	03/20	Compal Antony	Change 65W CP setting	Changer PR89 from PR89 from 143K ohm to 97.6K ohm	X01
30	41	+1.05V_VCCP/ +1.8VSP	03/20	Compal Antony	For phash margin improved	Add PC87 1000pF capacitor between PU13 pin6 and pin7	X01
31	41	+1.05V_VCCP/ +1.8VSP	03/20	Compal Antony	For phash margin improved	Add PC126 10uF capacitor between PU13 pin6 and GND	X01
32	39	Charger	05/06	Compal Antony	TI FAE request	Reserve PQ26,PD19,PD20,PC203,PR115,PR133 space	X02

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33	39	Charger	05/06	Compal Antony	slove PQ5 design margin issue	Change PQ4,PQ5,PQ7 from FDS4435 to FDS6675 (SB966750080)	X02
34	43	CPU_CORE	05/06	Compal Antony	Montavina platform design	Change PC136 from 15nF to 22nF	X02
35	39	Charger	05/06	Compal Antony	TI FAE request	Reserve PQ26,PD19,PD20,PC203,PR115,PR133,PC25 space	X02
36	39	Charger	06/04	Compal Antony	TI FAE request	Delete PQ26,PD19,PD20,PC203,PR115,PR133	X03
37	39	Charger	06/04	Compal Antony	TI request to reserve protection circuit	Reserve PR90 0ohm , PR37 0ohm , PC100 space ,PC25 0.022uF ,PC20 change to 0603 size	X03
38	39	Charger	06/04	Compal Antony	Recover a correct component	recover correct component PR89 to 97.6K ohm	X03
39	38	DCIN/Precharge	06/04	Compal Antony	DELL command	Change PQ2 from SB502060000 (RHU002N06_SOT323-3) to SB50301008L (FDV301N 1N SOT23-3)	X03