Tang/TangBTO Schematics Document

uFCBGA/uFCPGA Coppermine-T or Tualatin

2001-11-16

REV: 2.0

Compal Electronics, Inc.		
Title: Cover Sheet		
Size	Document Number: ADY11 LA-1181	Rev: 2
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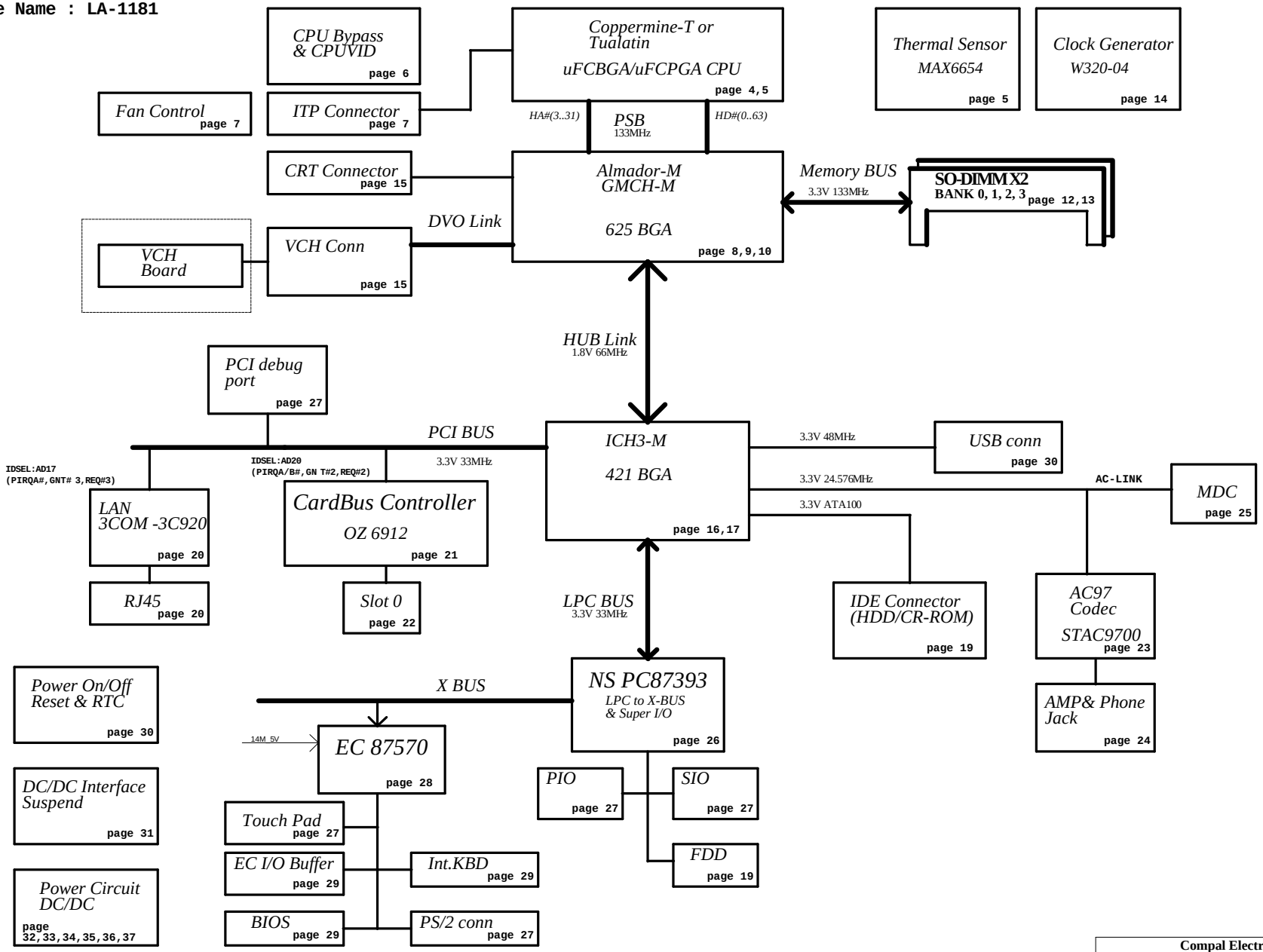
Compal confidential

Block Diagram

Model Name :ADY11(Tang)

File Name : LA-1181



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Title	Block Diagram	
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Note:"@" means all model depop
"#" means Tang depop

Function \ Model	M2P3	Tang
FDD	YES	NO
PS/2	YES	YES
Series port	NO	NO
Parallel port	YES	YES
RJ45	YES	NO
3Com Lan chipset(3C920)	YES	NO

	CHIPS Rev	CHIPS Rev	3C920-ST06
SST-Build	~~FW82830MG~~ QB88	~~FW82801CAM~~ QB63	Lot:M28010 DC:C0117
SST2-Build	QC34	QB62	Lot:M28010 DC:C0117
PT-Build	QC34	QB62	Lot:M28010 DC:C0117
ST-Build	QC34	QC42	Lot:M28010 DC:C0117

Note:"@" means all model depop
"&" means M2P3 depop
"#" means Tang depop

Compal Electronics, Inc.		
Title: Note & Revision		
Size	Document Number: ADY11 LA-1181	Rev: 2
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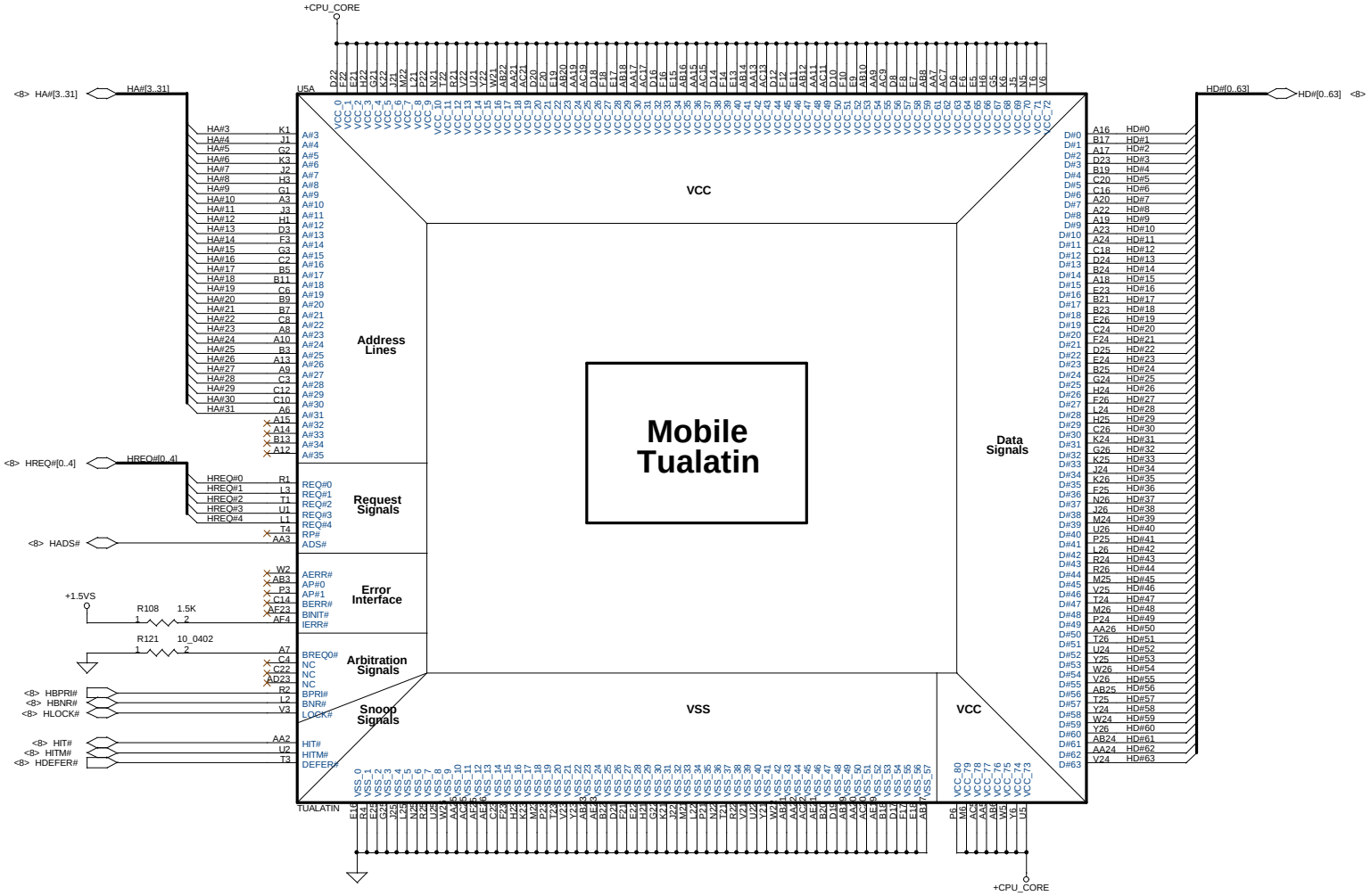

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Title	Mobile Tualatin uFCPGA	
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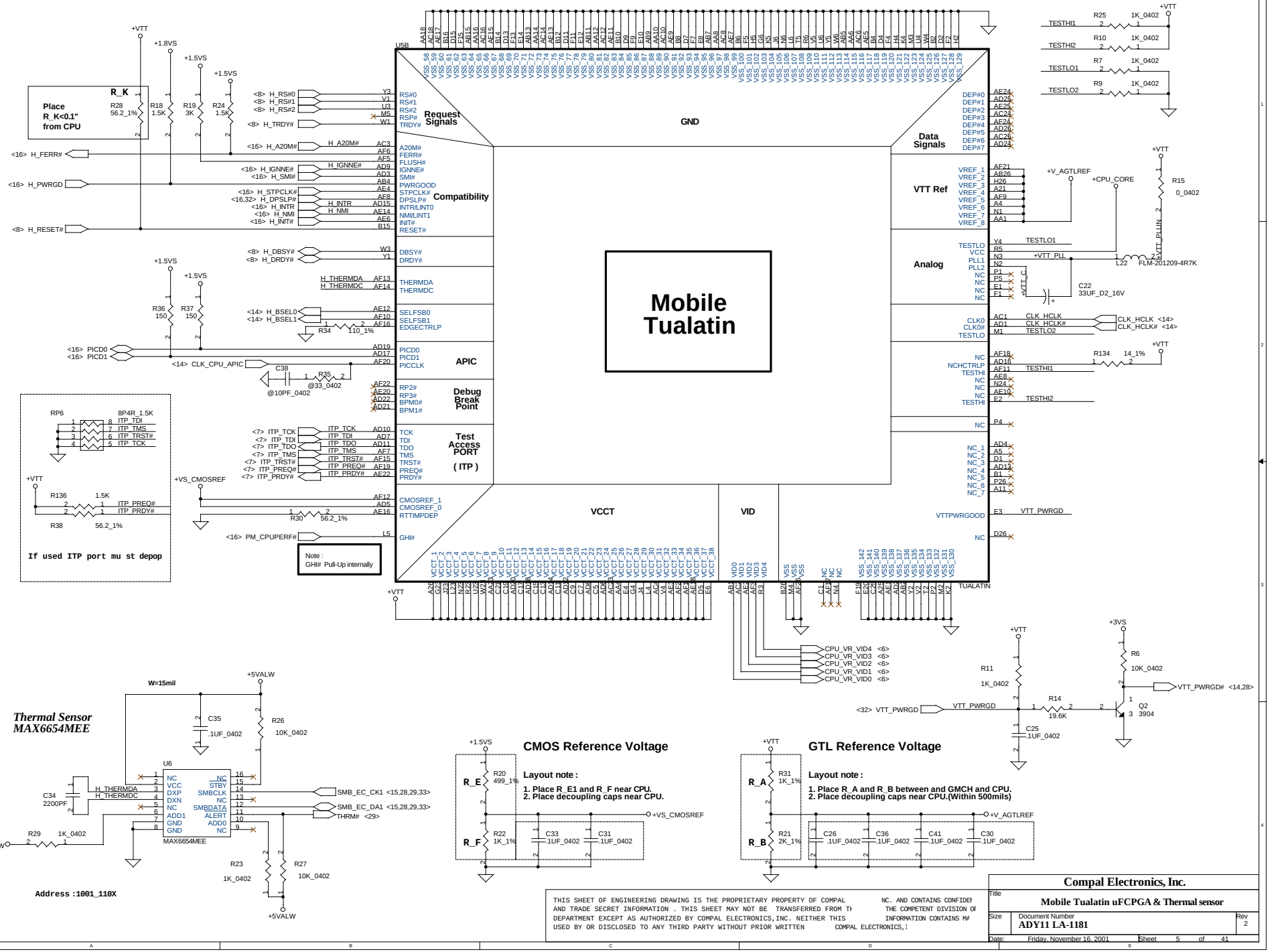

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Title: **Mobile Tualatin uFCPGA & Thermal sensor**

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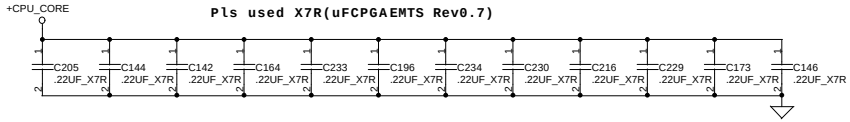
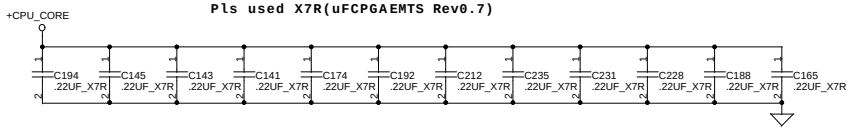
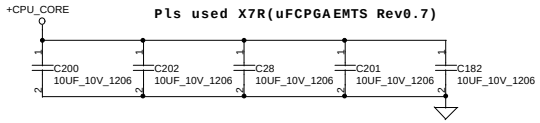
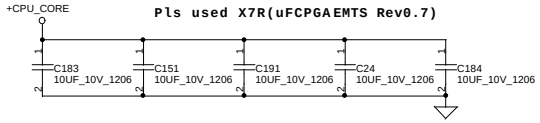
Layout note :

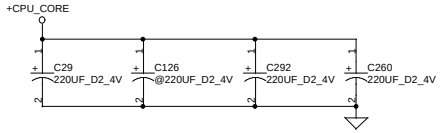
Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

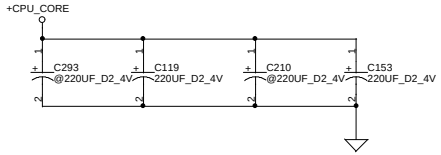


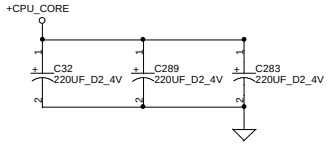






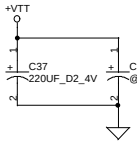


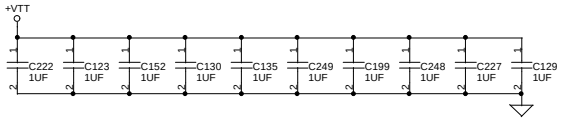




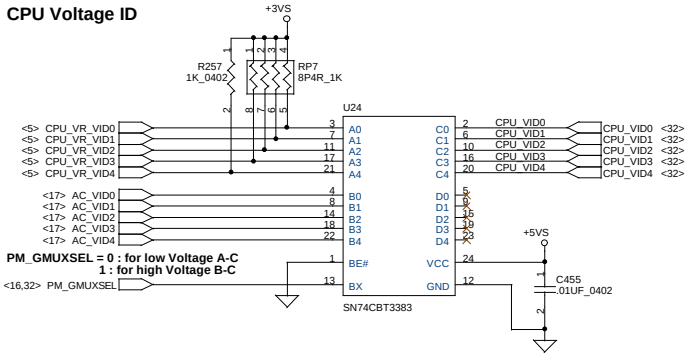
Layout note :

Place close to CPU,
Use 2 vias per PAD.





CPU Voltage ID



Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V	
0	1	1	0	0	1.15V	

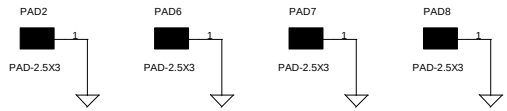
D4	D3	D2	D1	D0	CPU_Core(V)	QS (MP)
0	0	1	1	1	1.40V	
0	1	1	0	0	1.15V	

Coppermine-T

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	0	0	1	1.70V	
0	1	0	0	0	1.35V	

D4	D3	D2	D1	D0	CPU_Core(V)	QS (MP)
0	0	0	0	1	1.70V	
0	1	0	0	0	1.35V	

EMI Clip PAD for CPU



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Title: **CPU Bypass & CPU VID**

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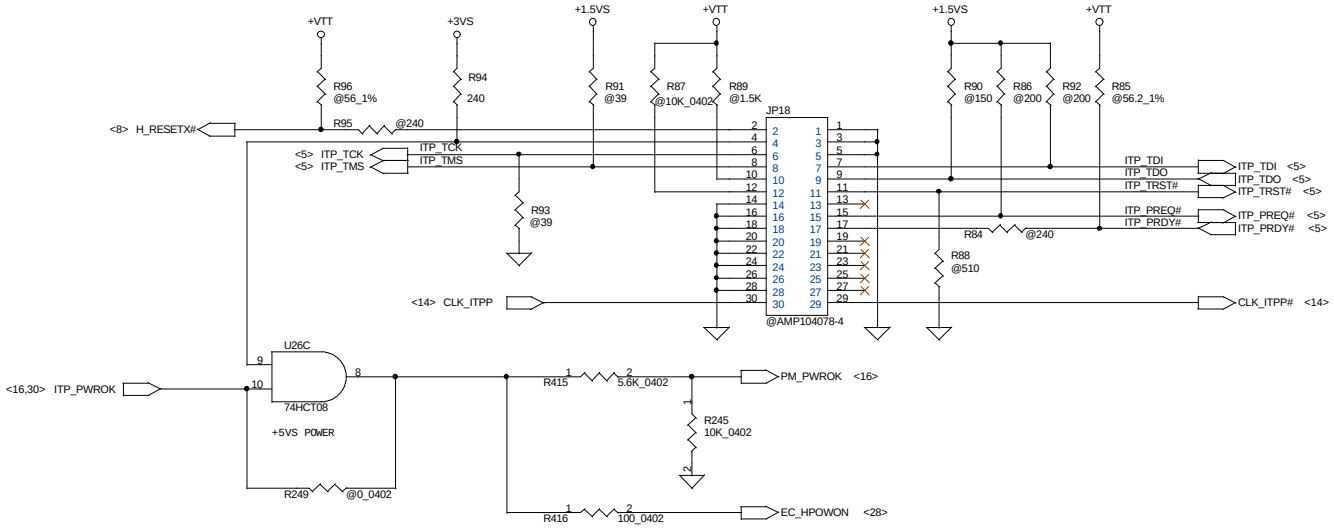
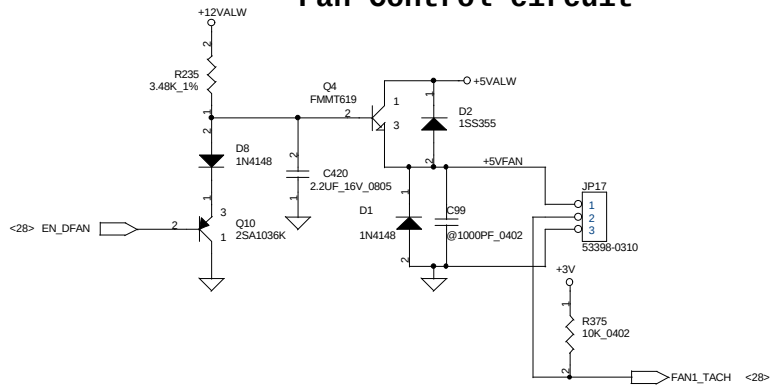
ITP PORT



Fan Control circuit



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Title	ITP PORT & Fan control	
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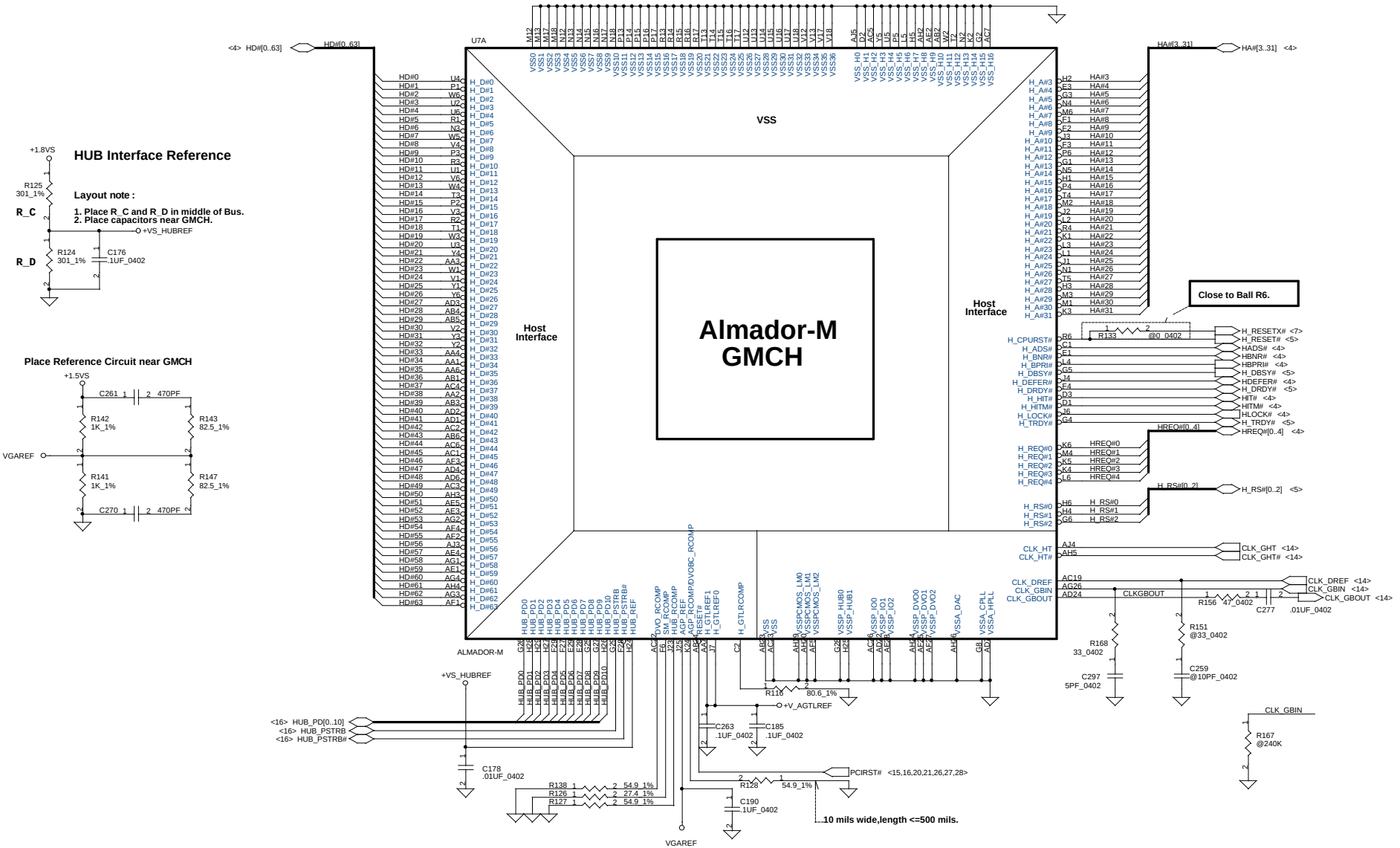

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Title	Almador-M GMCH(1/3)	
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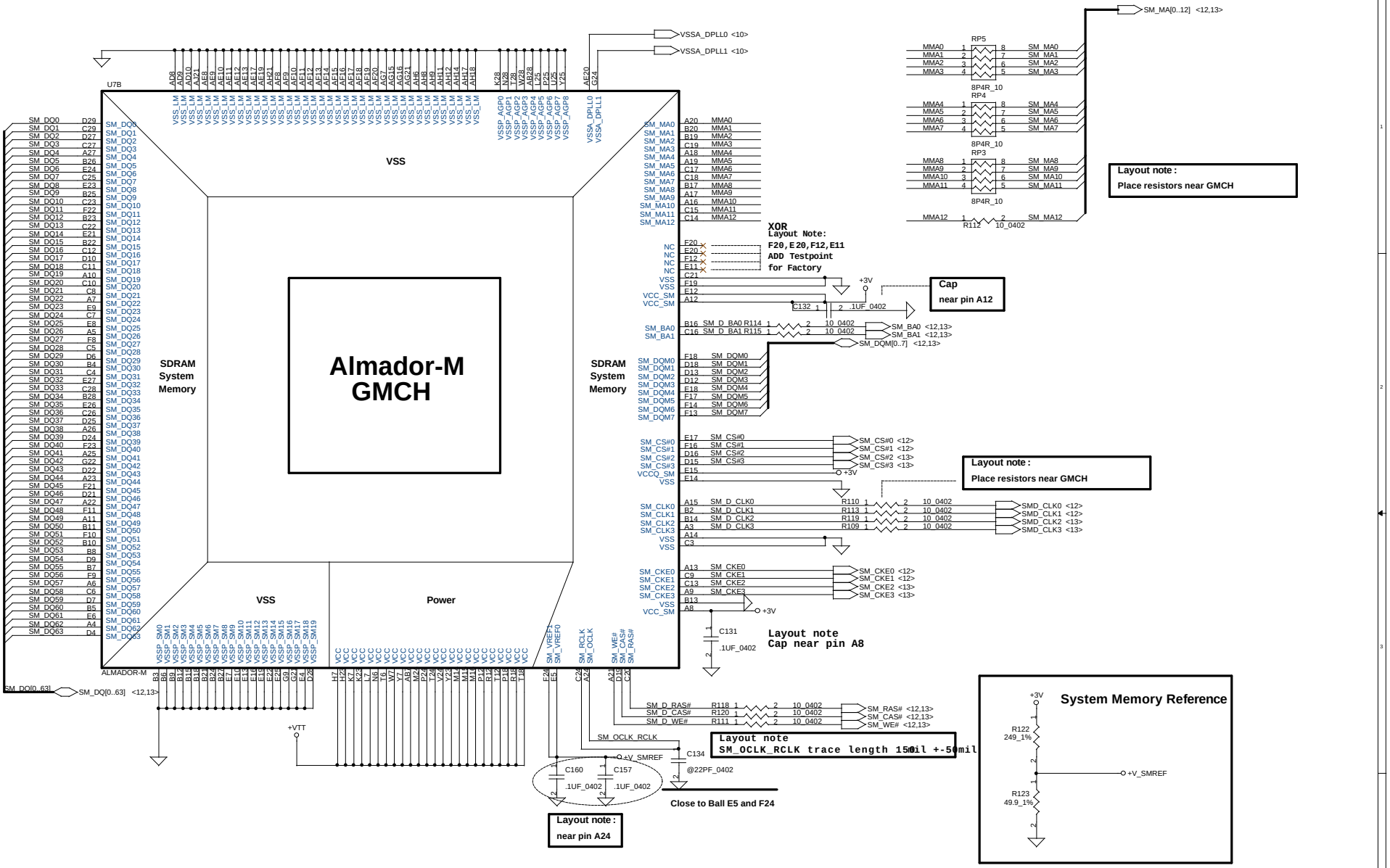

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Title: Almador-M GMCH(2/3)

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Strap Name	Low	High
DVOA_D1	IOQD=1	OQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term

Layout note :
Place close to AE16, AE15 of GMCH

Almador-M GMCH

Power Interface

AGP Interface
(DVOB/DVOC & ZV port)

Display Interface
(DVOA port)

Local Memory Interface

Local Memory Interface

XOR
Layout Note:
AE24,AJ25
ADD Testpoint for Factory

R_I

1. Place R_I and R_J near GMCH.

R_J

37.4_1% resistors and cap must be placed after RGB pi filter near CRT connector.

1.5V level clock

AGP_PAR : Strapping option for SW detection of AGP or DVO device.
0 -> DVO B/C device
1 -> AGP device

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Title	Almador-M GMCH(3/3)	
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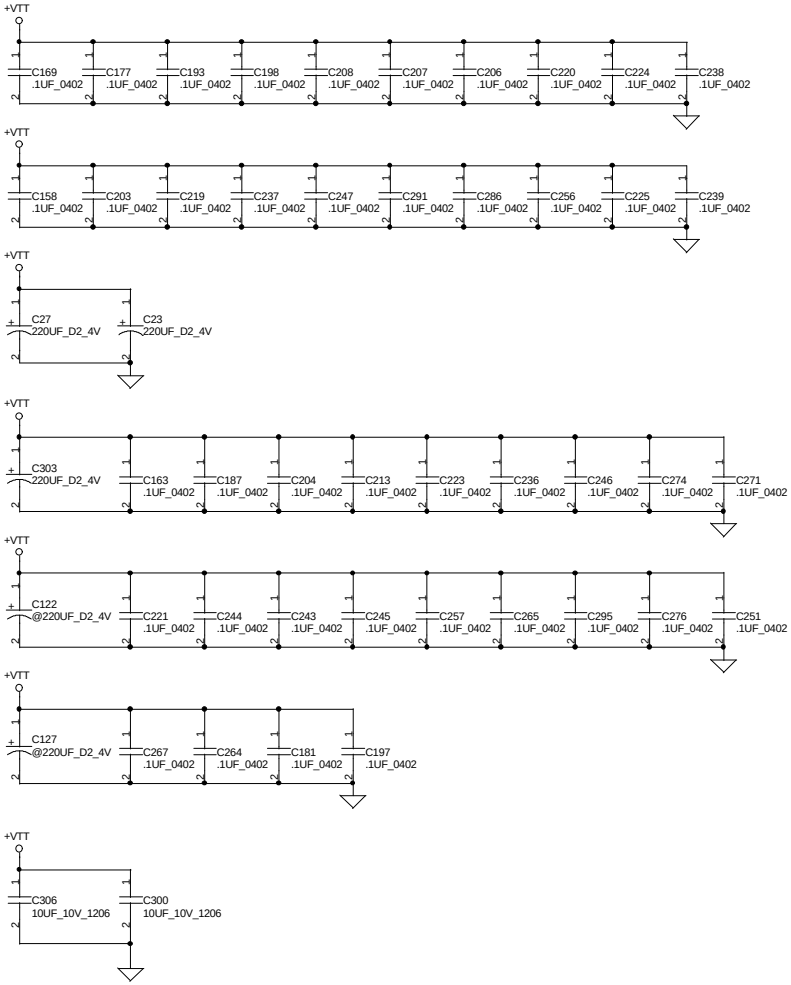
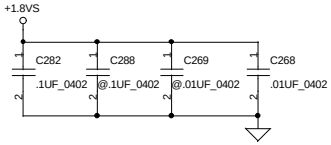
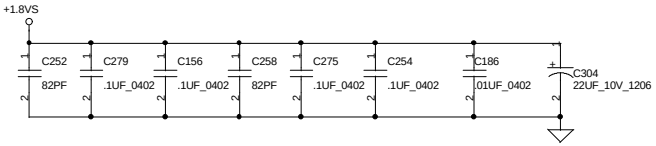
Layout note :
Distribute as close as possible to GMCH Processor Quadrant .



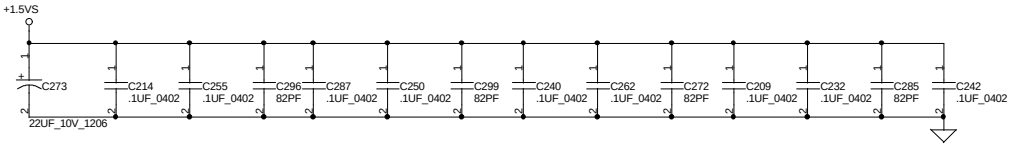
Layout note :
Distribute as close as possible to VCCPCMOS_LM. (GMCH pin AF6, AE7, AC9, AC8)



Layout note :
Distribute as close as possible to GMCH Local Memory Quadrant .

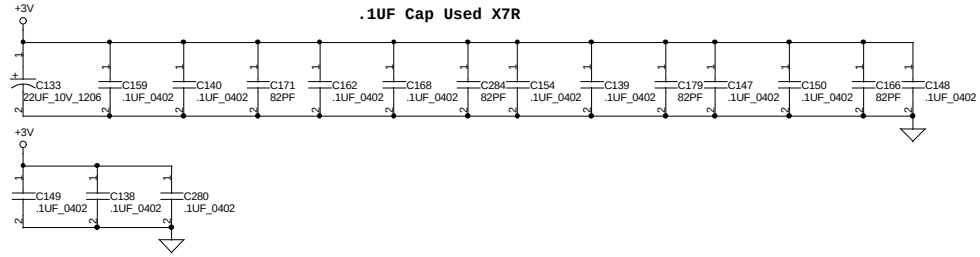


Layout note :
Distribute as close as possible to GMCH AGP/DVO Quadrant .

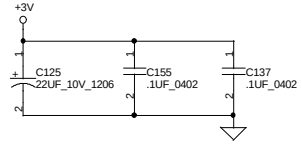


Layout note :
Distribute as close as possible to GMCH System Memory Quadrant .

.1UF Cap Used X7R



Layout note :
Distribute as close as possible to IO Quadrant .



Compal Electronics, Inc.		
Title: GMCH-M Decoupling		
Size	Document Number: ADY11 LA-1181	Rev: 2
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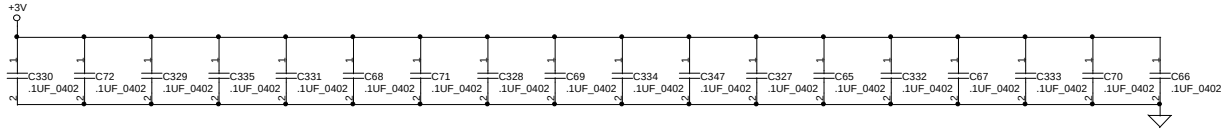
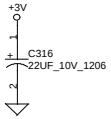
Layout note :

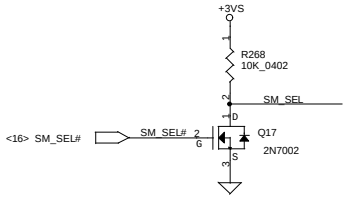
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 0) pin .

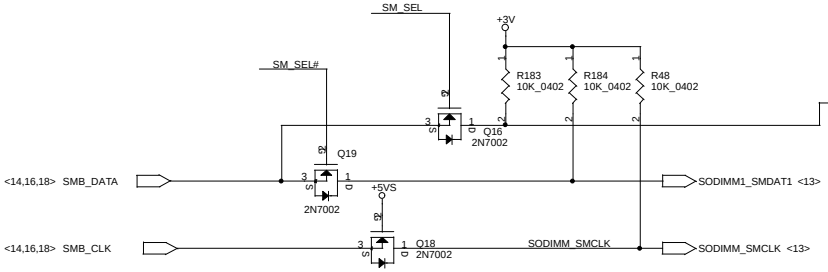


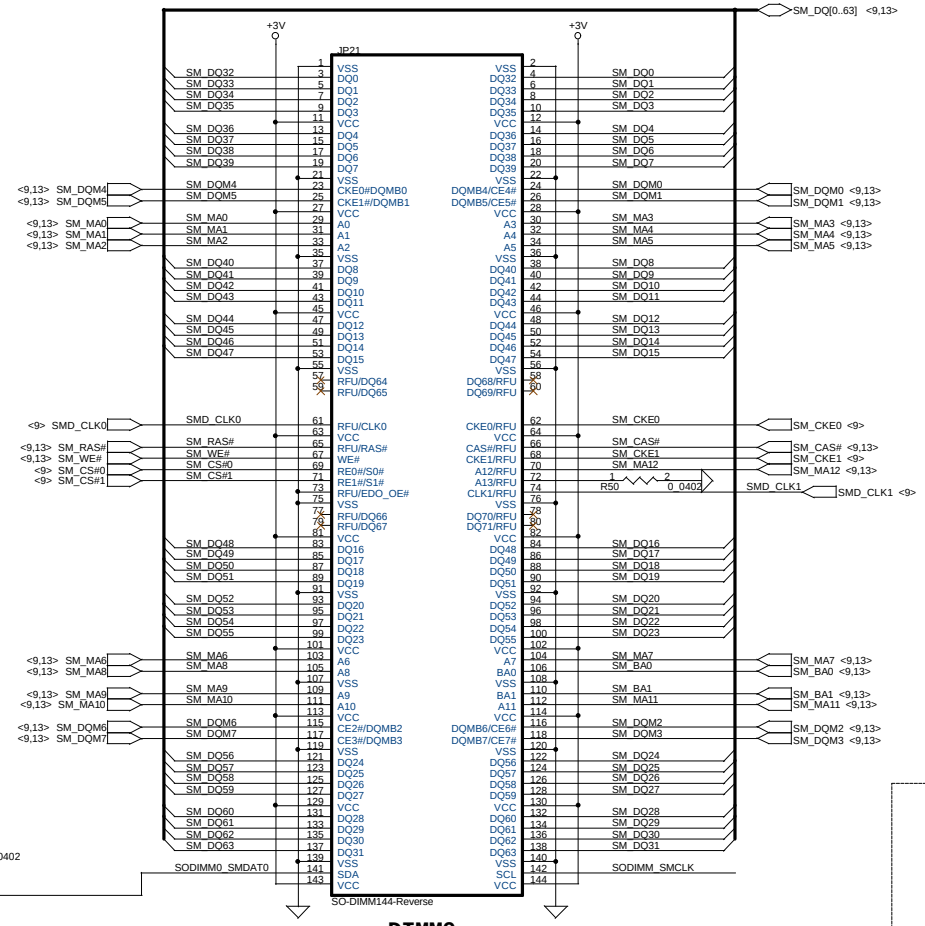


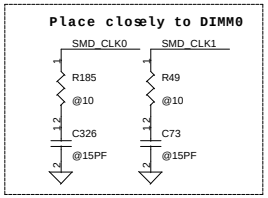
System S MBus Select

SM_SEL#
0=SODIMM0 ;
1=SODIMM1









Compal Electronics, Inc.

Title: **SO-DIMM SLOT0 /Decoupling & DIMM Select**

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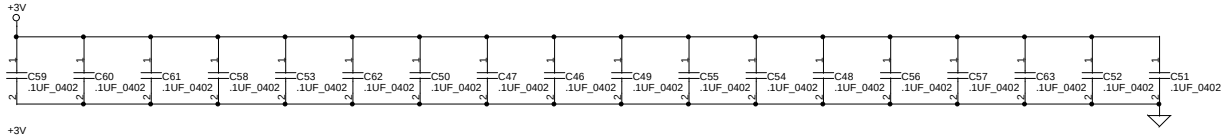
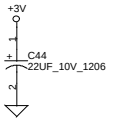
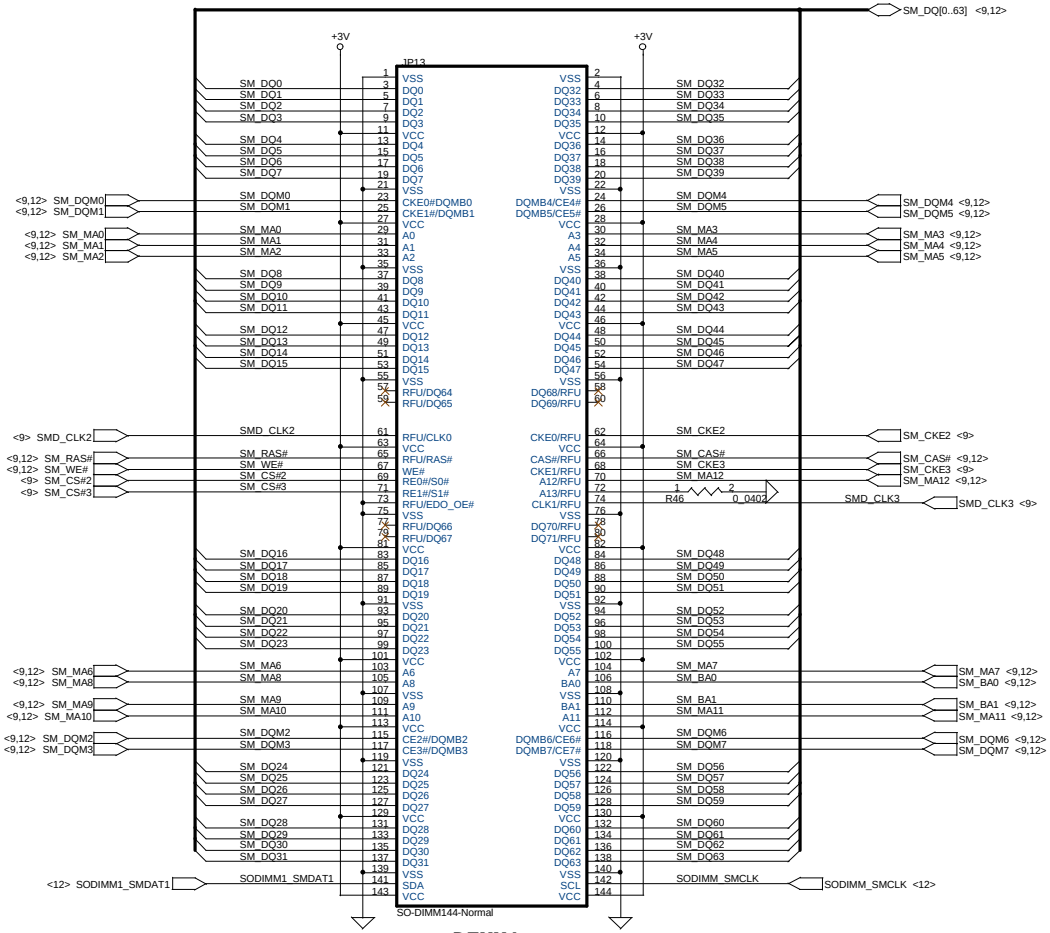
Layout note :

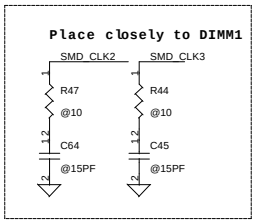
One .1uF cap per power pin .
Place each cap close to SODIMM(DIMM 1) pin .



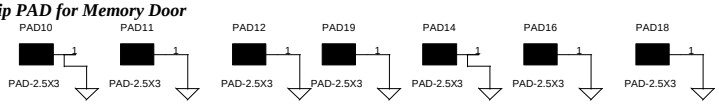




DIMM1



EMI Clip PAD for Memory Door



Compal Electronics, Inc.

Title	SO-DIMM SLOT1 & Decoupling	
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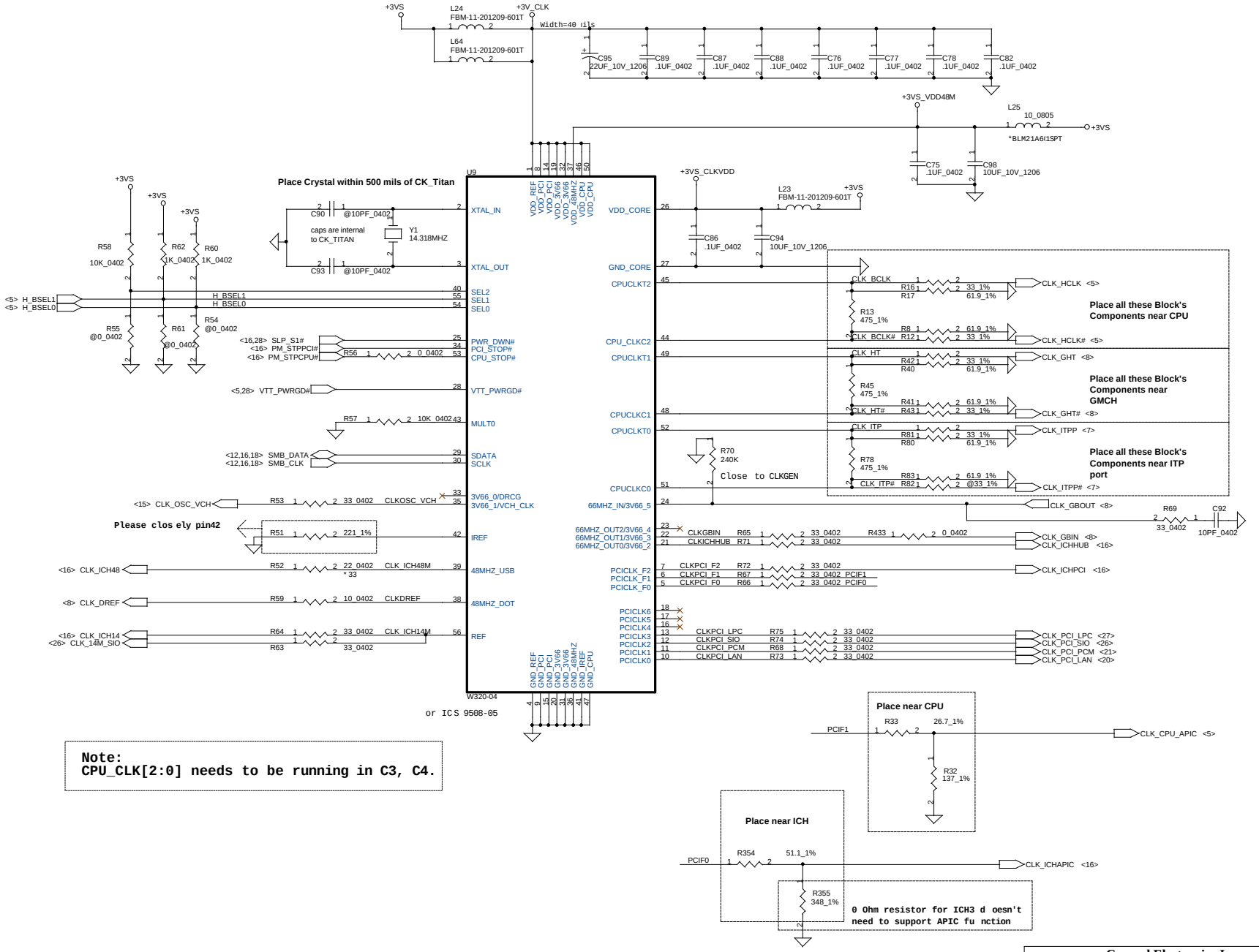

Compal Electronics, Inc.	
Title	Clock Generator
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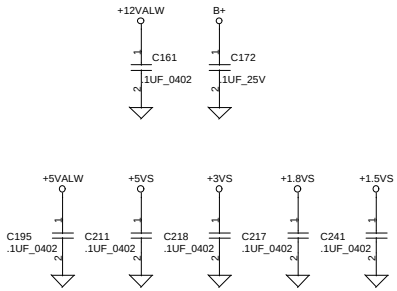
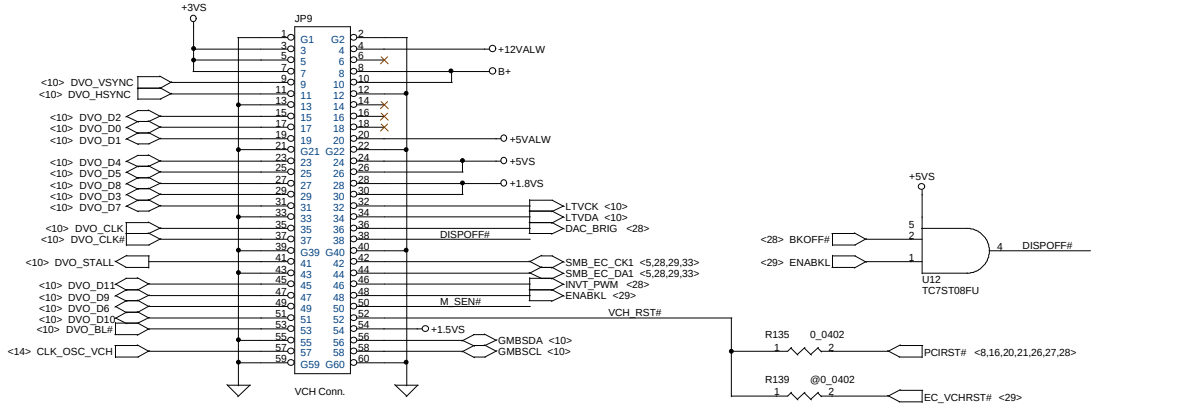
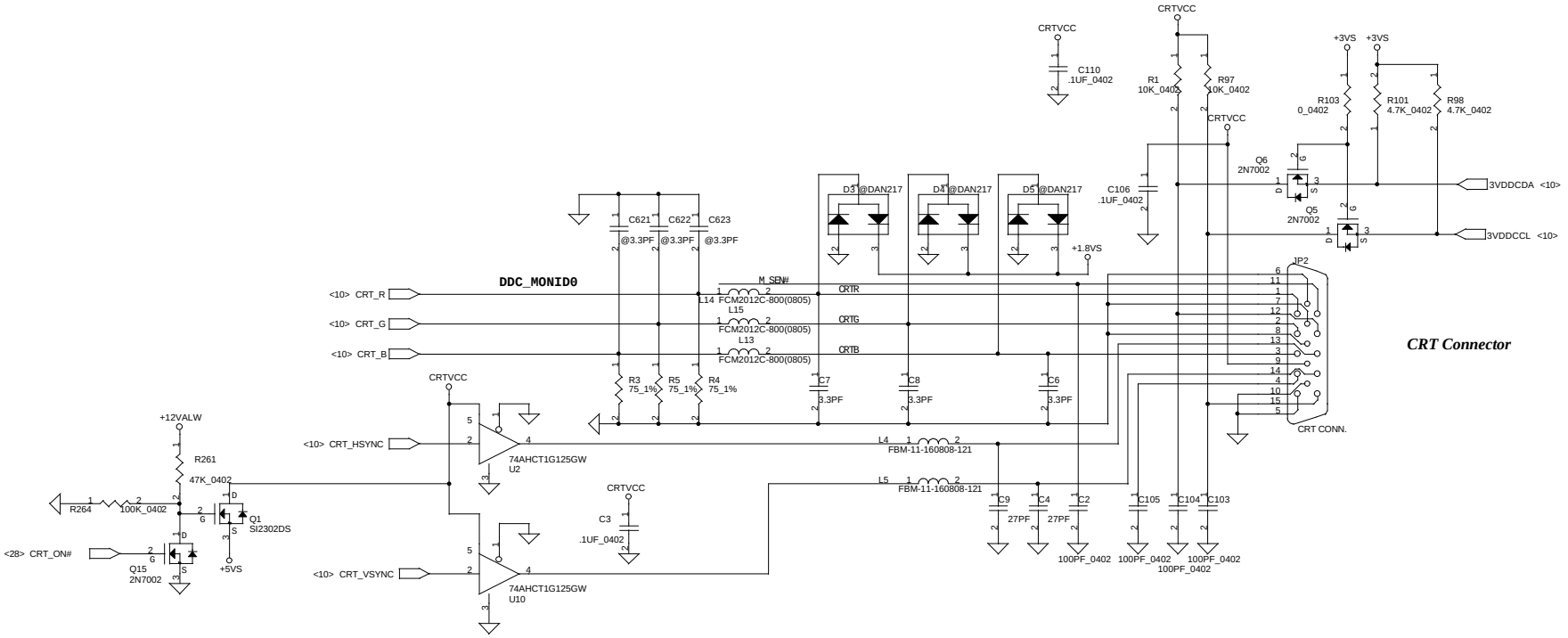
Please closely to VCH Conn. power pin







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Title	VCH Conn. & CRT	
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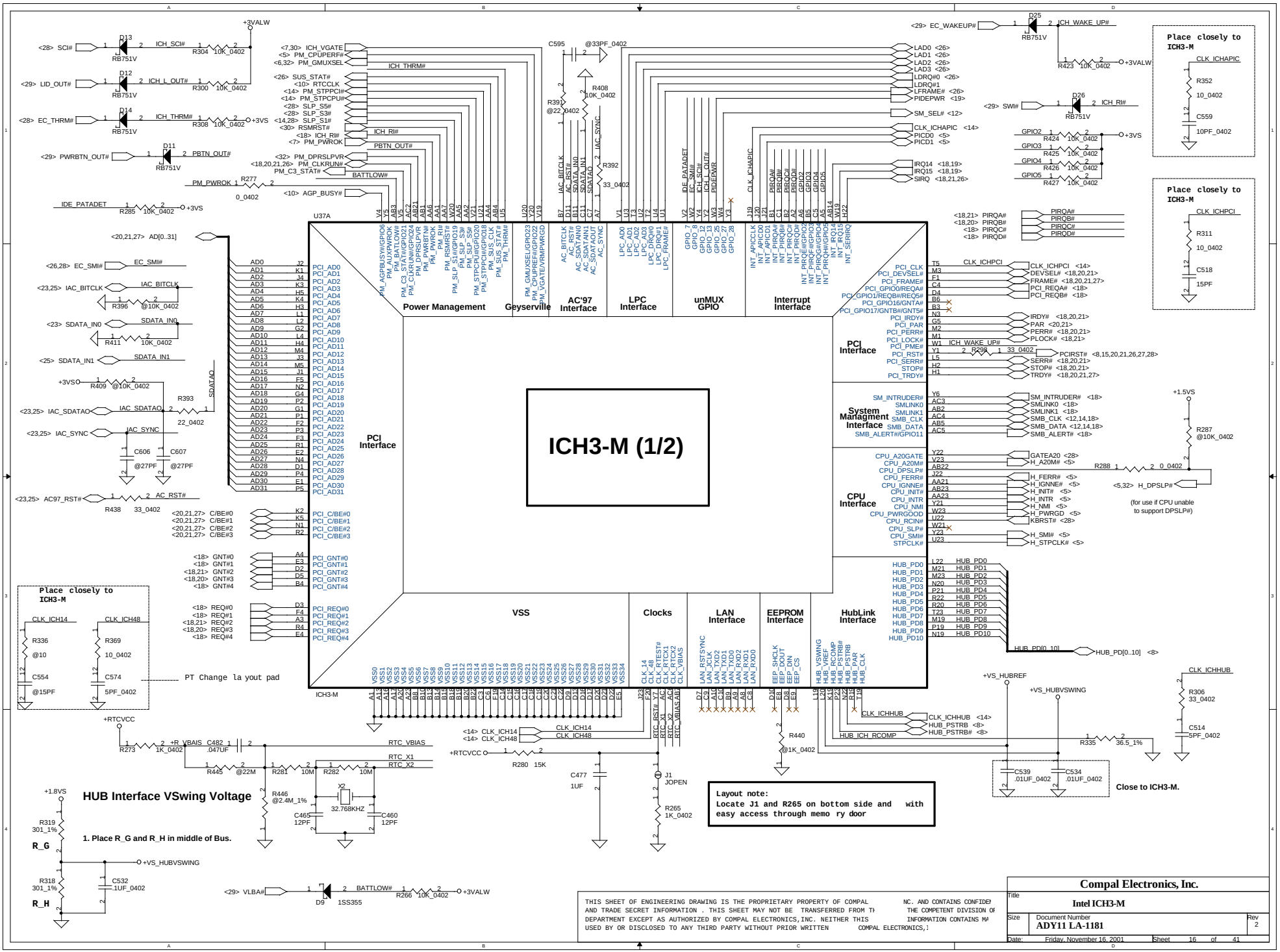

Compal Electronics, Inc.

Title: Intel ICH3-M

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ICH3-M (2/2)

Layout note The Cap c lose to ICH3-M(< 1 inch)

0=I2C CTRL CPUVID select
1=Bus switch CPUVID select

M/B ID

	MB_ID0	MB_ID1
SST	0	0
PT	1	0
ST	0	1
QT	1	1

Note:
R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LF pa rt)

Disable Timeo ut feature

Compal Electronics, Inc.

Title	Intel ICH3-M	
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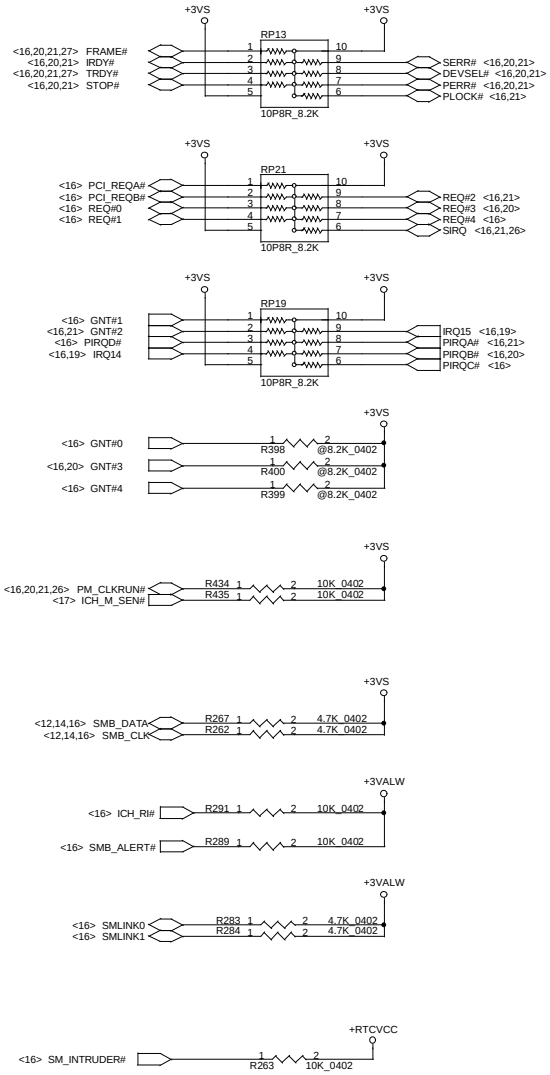

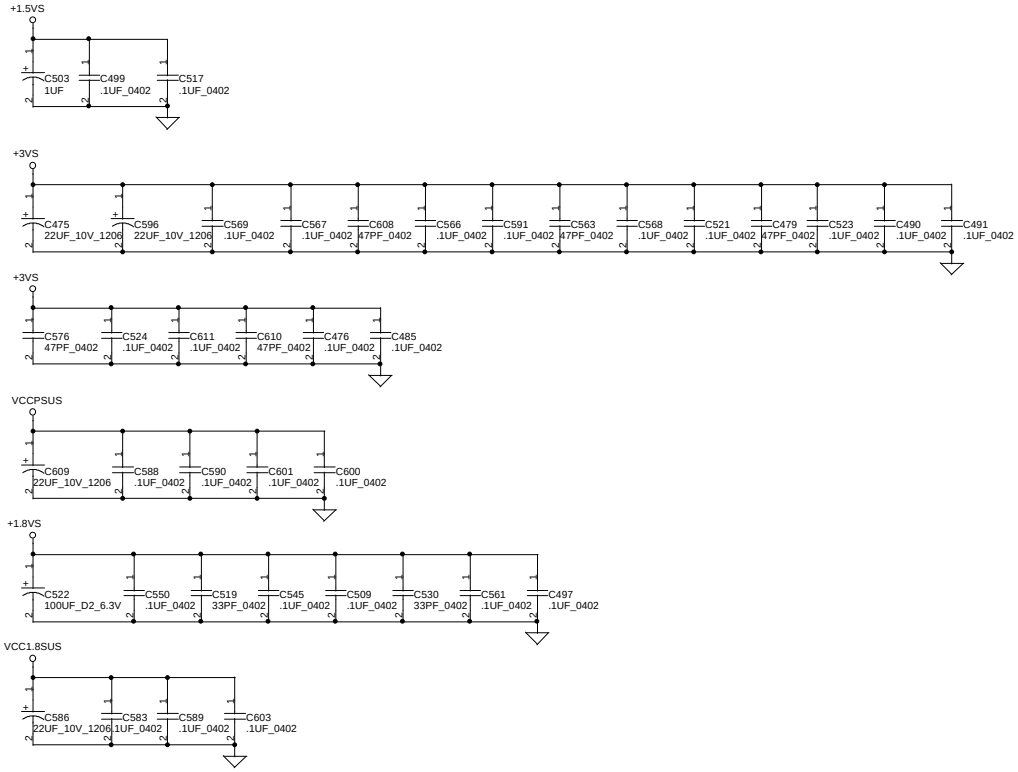

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Title: **ICH3-M Decoupling & Pull-Up**

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HDD Connector

<17> PDD[0..15] — PDD[0..15]

Correct HDD pin define ,pls update layout

JP20

<17> PIDERST#	1	2	
	PDD7	3	4	PDD8
	PDD6	5	6	PDD9
	PDD5	7	8	PDD10
	PDD4	9	10	PDD11
	PDD3	11	12	PDD12
	PDD2	13	14	PDD13
	PDD1	15	16	PDD14
	PDD0	17	18	PDD15
		19	20	
<17> PDDREQ	PDDREQ	21	22	
<17> PDIOW#		23	24	
<17> PDIOR#	PDIORDY	25	26	PCSEL 1 R239 2 470_0402
<17> PDIORDY	RPDDACK#	27	28	
	RIRQ14	29	30	
		31	32	
<17> PDA1		33	34	PDA2 <17>
<17> PDA0		35	36	PDCS3# <17>
<17> PDCS1#	PHDD_LED#	37	38	
+5VSHDD		39	40	
		41	42	+5VSHDD
		43	44	

R244 @10K_0402

HH99221-S6-HDDCON

+12VALW — R237 100K_0402 — +5VS — Q14 SI2301DS — +5VSHDD

<16> PIDEPWR — Q13 2N7002 — R428 150K — C438 .01UF_0402

SI2301DS: P CHANNEL
VGS: -4.5V, RDS: 130 mOHM
VGS: -2.5V, RDS: 190mOHM
Id(MAX): 2.3A
VGS(MAX): +-8V

S 3 2 G

D 1

 # means no-pop for Tang
Note: PT-test must pop these component s

FDD Connector

JP24

		1	+5V
<26> INDEX#	INDEX#	2	INDEX
		3	+5V
<26> DRV0#	DRV0#	4	DRIVE SELECT
		5	+5V
<26> DISKCHG#	DISKCHG#	6	DISK CHANGE
		7	NC
		8	READY
		9	DENSITY OUT
<26> MTR0#	MTR0#	10	MOTOR ON
	3MODE# 11	11	NC
<26> FDDIR#	FDDIR#	12	DIRECTION
	3MODE# 13	13	DENSITY 2
<26> STEP#	STEP#	14	STEP
		15	GND / NC
<26> WDATA#	WDATA#	16	WRITE DATA
		17	GND
<26> WGATE#	WGATE#	18	WRITE GATE
		19	GND
<26> TRK0#	TRK0#	20	TRACK 00
		21	NC / GND
<26> WRPRT#	WRPRT#	22	WRITE PROTECT
		23	GND
<26> RDATA#	RDATA#	24	READ DATA
<29> FDD_PRES#		25	GND
<26> HDSEL#	HDSEL#	26	SIDE 1 SELECT

#85201-2605-ACES-FDDCON

Placea caps. near HDD CONN.

+5VSHDD — **Layout Note: +5VSHD D trace width 60 mil**

C451 1000PF_0402 — C445 10UF_16V_1206 — C444 10UF_16V_1206 — C100 1UF_25V_0805 — C102 .1UF_0402

Placec caps. near FDD CONN.

+5VS — C599 #.1UF_0402 — C592 #10UF_16V_1206 — C587 #1UF_25V_0805 — C584 #.1UF_0402

R243 +3VS — PDIORDY — 4.7K_0402

<17> PDDACK# — R242 22_0402 — RPDDACK#

<16,18> IRQ14 — R241 22_0402 — RIRQ14

PDDREQ — R240 @5.6K_0402 — C443 33PF_0402

<26> 3MODE# — 3MODE# — R366 @0_0402 — R365 #0_0402

CD-ROM Connector

<17> SDD[0..15] — SDD[0..15]

C411 47PF_0402 — C413 47PF_0402 — CD_AGND <23> — C416 47PF_0402 — INT_CD_R <23>

<23> INT_CD_L

JP16

<17> SIDERST#	1	2	
	SDD7	3	4	SDD8
	SDD6	5	6	SDD9
	SDD5	7	8	SDD10
	SDD4	9	10	SDD11
	SDD3	11	12	SDD12
	SDD2	13	14	SDD13
	SDD1	15	16	SDD14
	SDD0	17	18	SDD15
		19	20	SDDREQ
<17> SDIOW#		21	22	SDDREQ <17>
<17> SDIORDY	SDIORDY	23	24	SDIOR# <17>
	RIRQ15	25	26	
		27	28	RSDDACK#
<17> SDA1		29	30	PDIAG# 1 R206 2 100K_0402 +5VS
<17> SDA0		31	32	SDA2 <17>
<17> SDCS1#	SHDD_LED#	33	34	SDCS3# <17>
		35	36	W=80mils
+5VS		37	38	
		39	40	
		41	42	+5VS
	SEC_CSEL	43	44	C83 .1UF_0402
		45	46	
		47	48	
		49	50	

R76 @10K_0402

R197 470_0402

CD-ROM CONN.

R212 +3VS — SDIORDY — 4.7K_0402

<17> SDDACK# — R213 22_0402 — RSDDACK#

<16,18> IRQ15 — R207 22_0402 — RIRQ15

SDDREQ — R217 @5.6K_0402 — C399 33PF_0402

Placea caps. near CDROM CONN.

+5VS — C365 1000PF_0402 — C364 .1UF_0402 — C366 1UF_25V_0805 — C81 10UF_16V_1206

+5VS — C376 1000PF_0402 — C377 .1UF_0402 — C378 1UF_25V_0805 — C85 10UF_16V_1206

RP20 (8P4R_1K)

DISKCHG#	1	8	+5VS
INDEX#	2	7	
WRPRT#	3	6	
TRK0#	4	5	

RP15 (10P8R_1K)

WDATA#	6	5	+5VS
WGATE#	7	4	STEP#
HDSEL#	8	3	MTR0#
FDDIR#	9	2	RDATA#
+5VS	10	1	DRV0#

+5VS — R79 100K_0402 — R238 100K_0402

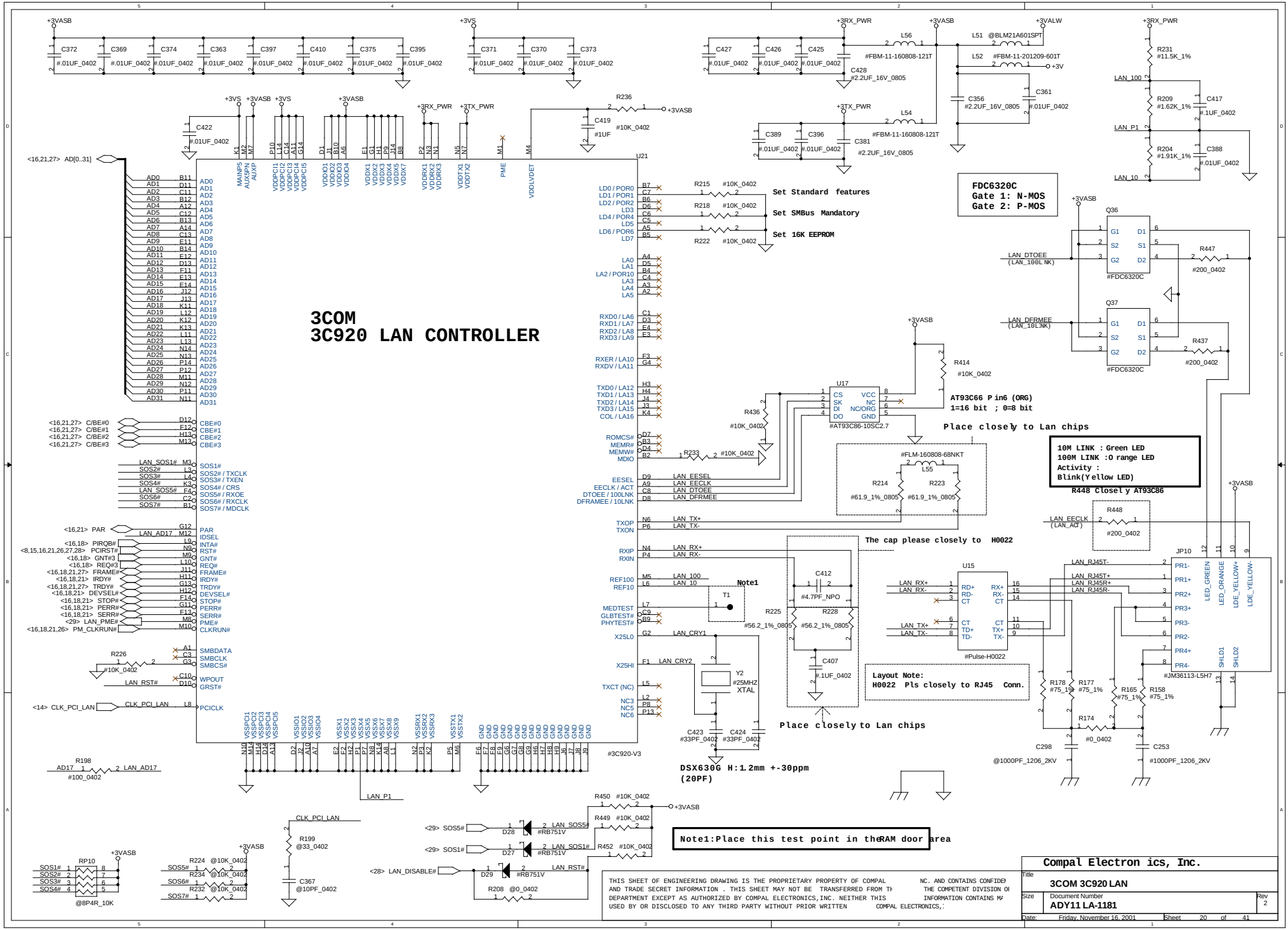
PHDD_LED# — U26D 74HCT08 — C101 .1UF_0402

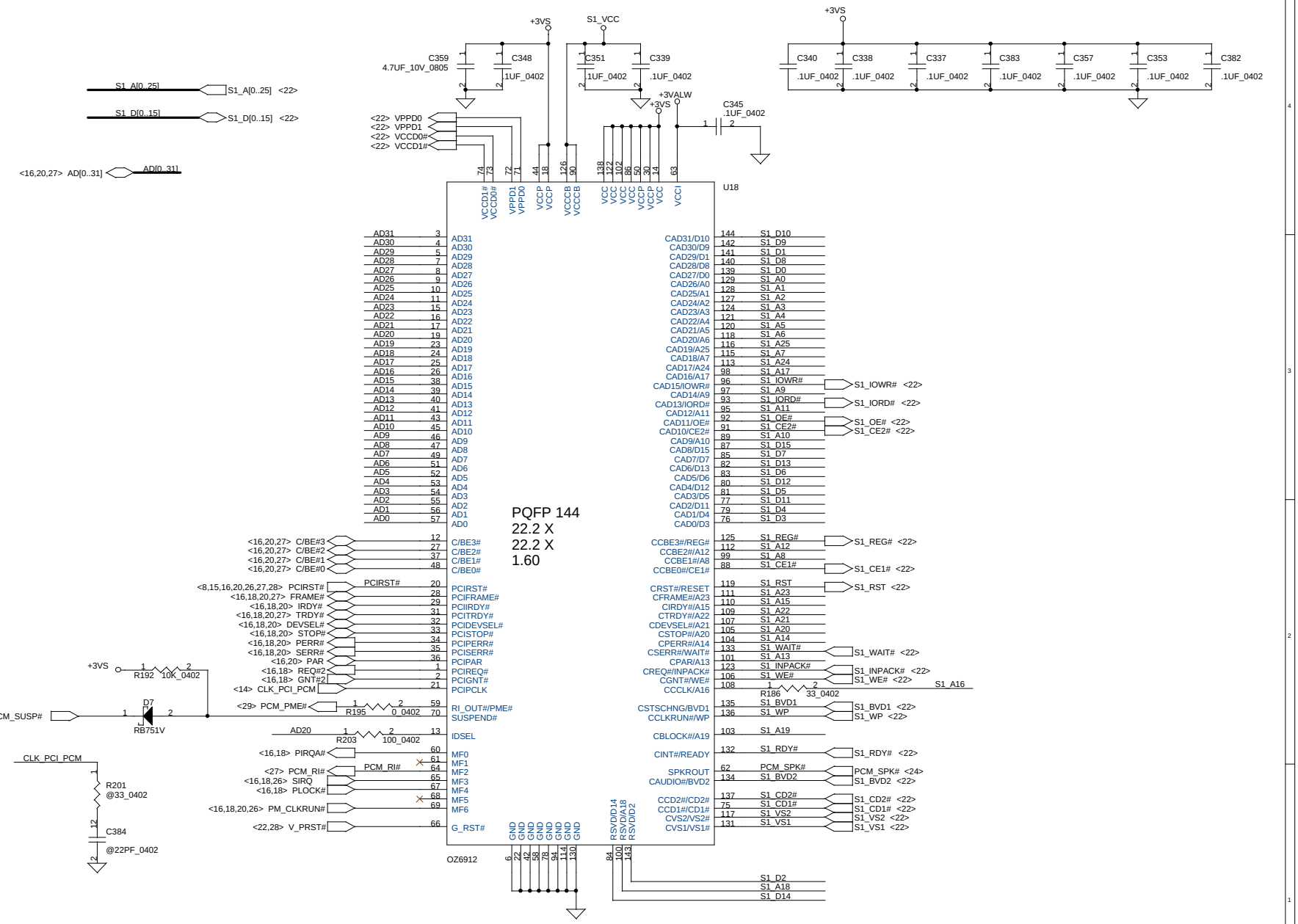
SHDD_LED# — U26A 74HCT08 — ACT_LED# — ACT_LED# <27>

DRV0#

Compal Electronics, Inc.

Title	IDE/FDD/CD-ROM Module	
Size	Document Number ADY11 LA-1181	Rev 2
Date: Friday, November 16, 2001	Sheet 19 of 41	


3COM
3C920 LAN CONTROLLER
U21
#3C920-V3
FDC6320C
Gate 1: N-MOS
Gate 2: P-MOS
Set Standard features
Set SMBus Mandatory
Set 16K EEPROM
AT93C66 Pin6 (ORG)
1=16 bit ; 0=8 bit
#AT93C86-10SC2.7
Place closely to Lan chips
10M LINK : Green LED
100M LINK :O range LED
Activity :
Blink(Yellow LED)
R448 Closely AT93C86
The cap please closely to H0022
Note1
DSX630G H:1.2mm +-30ppm
(20PF)
Layout Note:
H0022 Pls closely to RJ45 Conn.
#Pulse-H0022
#JM36113-L5H7
Note1:Place this test point in the RAM door area
@8P4R_10K
Compal Electronics, Inc.
3COM 3C920 LAN
ADY11 LA-1181
Rev 2
Friday, November 16, 2001
Sheet 20 of 41



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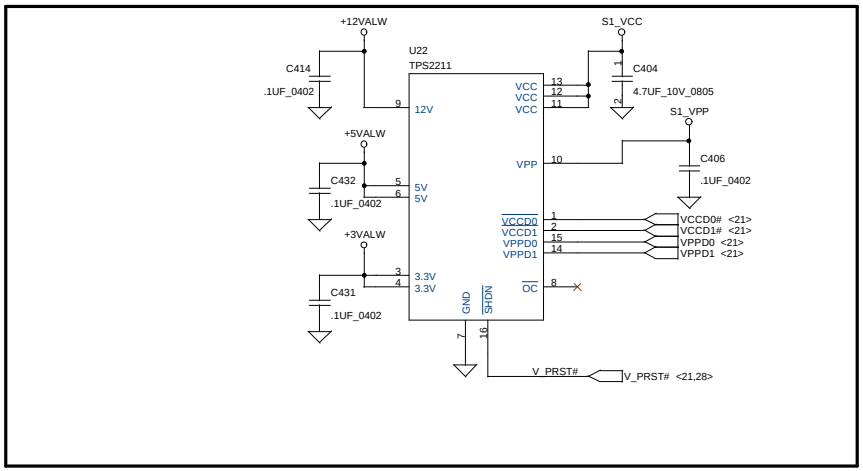
Compal Electronics, Ltd.

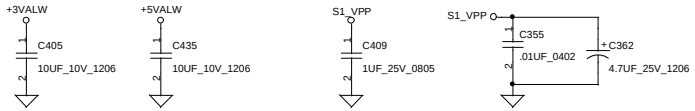
Title: **PCMCIA controller OZ6912**

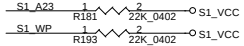
Size: Document Number: **ADY11 LA-1181** Rev: 2

Date: Friday, November 16, 2001 Sheet 21 of 41

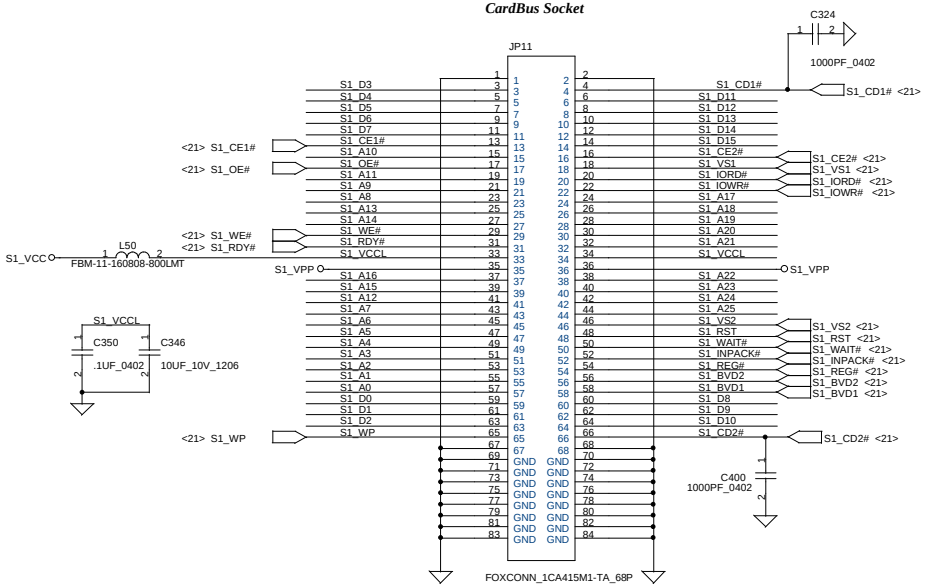
PCMCIA Power Controller





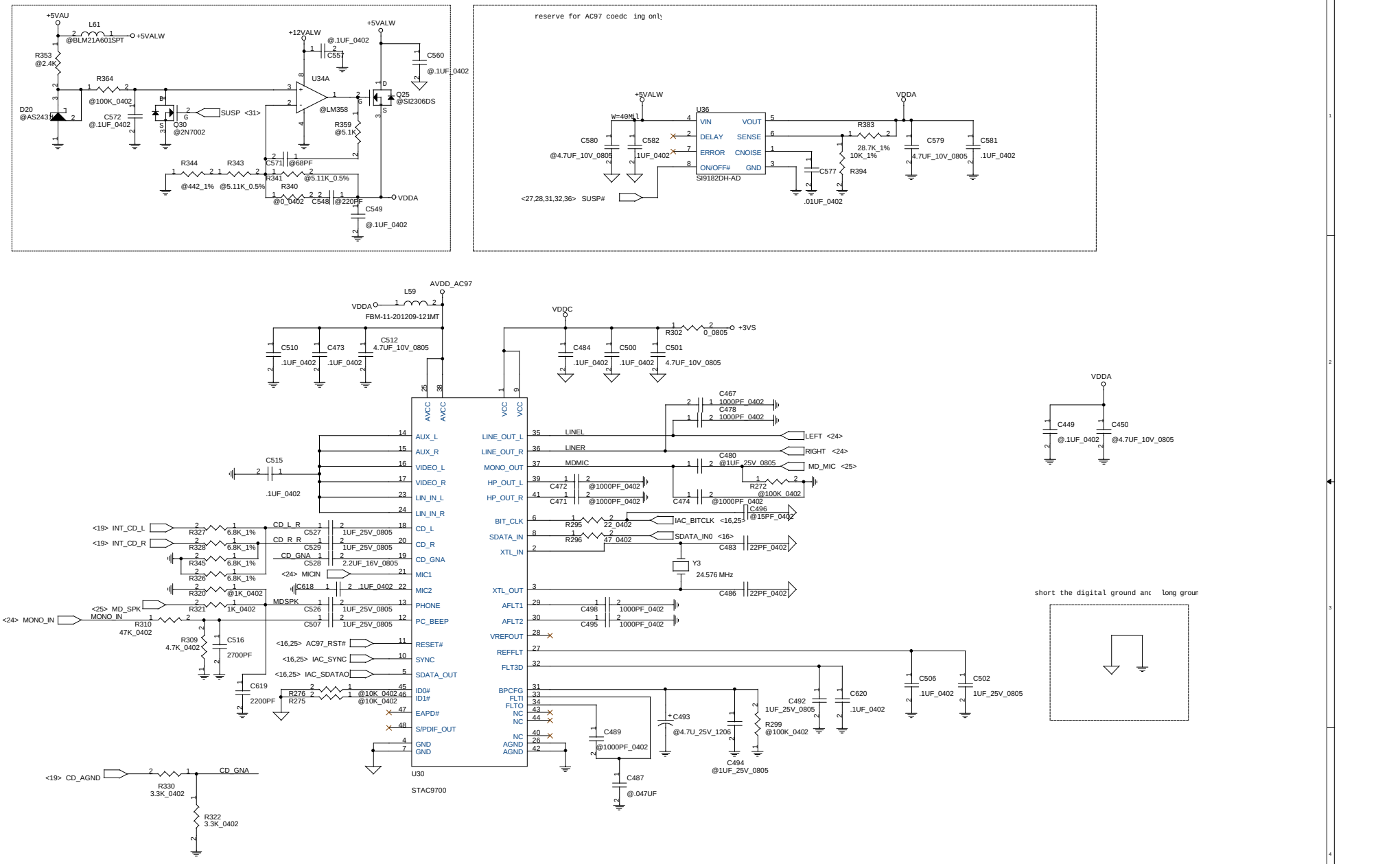


CardBus Socket



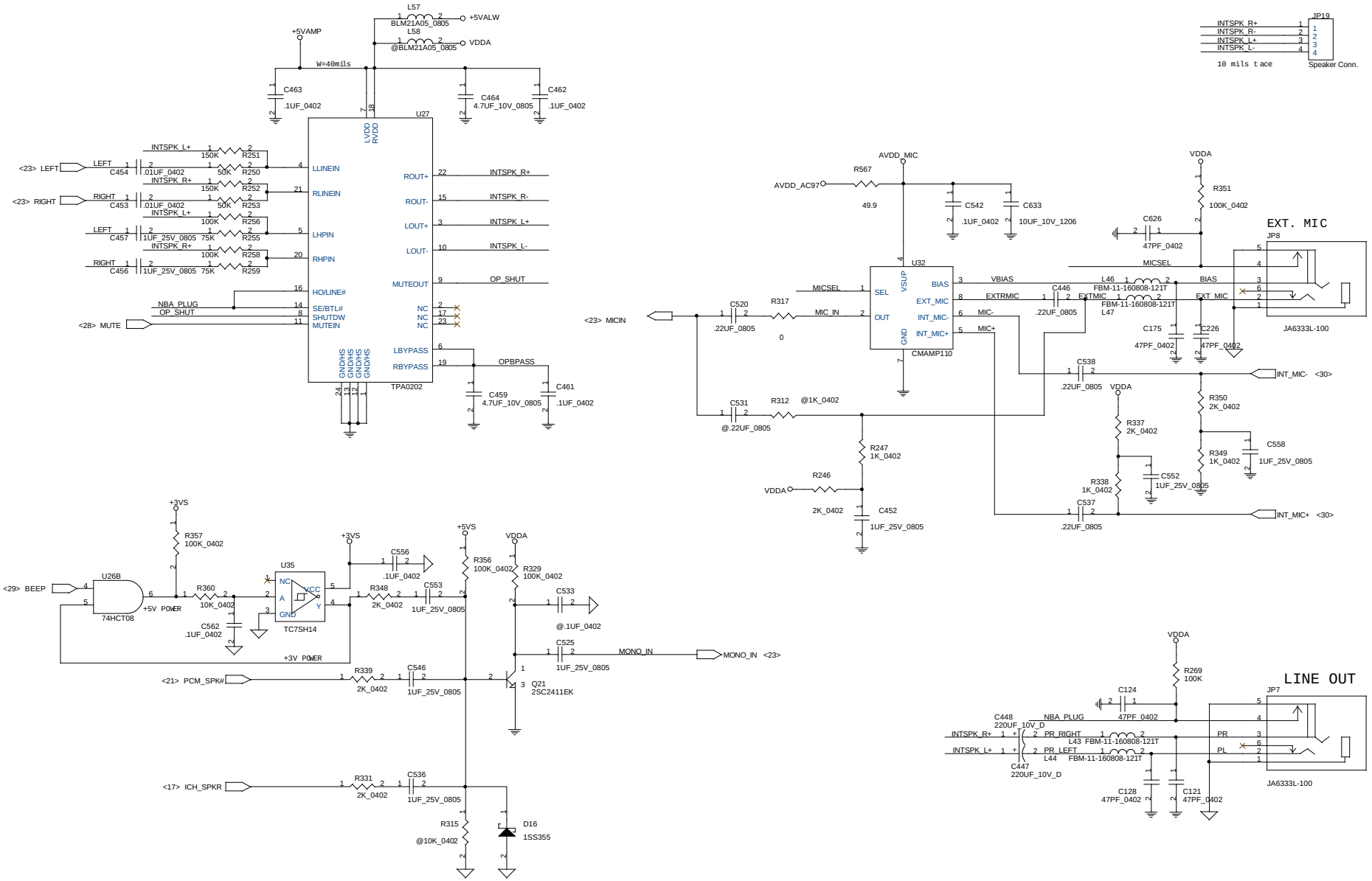
Compal Electronics, Inc.

Title	**CardBus Socket**	
Size	Document Number **ADY11 LA-1181**	Rev 2
Date: Friday, November 16, 2001	Sheet 22 of 41	



Compal Electronics, Inc.

Title	AC97 CODEC	
Size	Document Number: ADY11 LA-1181	Rev: 2
Date: Friday, November 16, 2001	Sheet 23 of 41	

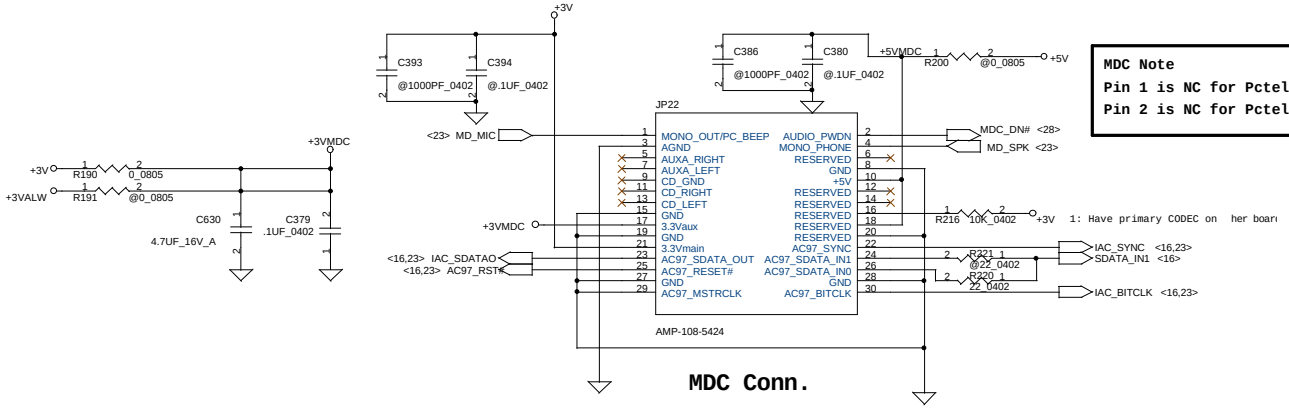


Compal Electronics, Inc.

Title: **AMP & Audio Jack**

Size: | Document Number: **ADY11 LA-1181** | Rev: 2

Date: Friday, November 16, 2001 | Sheet 24 of 41



MDC Note
Pin 1 is NC for Pctel and connexant MDC modem
Pin 2 is NC for Pctel and connexant MDC modem

MDC Conn.

Screw Hole

H6 C315D126 · H2 C315D126 · H1 C315D126 · H7 C315D126 · H22 C315D118 · H13 O193X134D193X134N · H12 S315D118

H4 C315D157 · H3 C315D157 · H10 C256D157 · H11 C256D157 · H8 C315D157 · H17 C134D134N

H23 C354D244 · H24 C354D244 · H15 O217X106D177X67 · H16 O217X106D177X67

H19 O106X217D67X177 · H25 O106X217D67X177 · H27 C315D110 · M9 S276D110 · M2 S394D138

H20 O75X213D40X177 · H21 O75X213D40X177 · H26 O75X213D40X177 · M3 S315D118

H18 S315D118 · H14 S315D118 · H9 R256X315D138 · H5 C315D118 · M1 C315D118 · M6 C315D118 · M10 S315D244 · M11 SMDC200M157

Fiduial Mark

FD1 FIDUCIAL MARK · FD3 FIDUCIAL MARK · FD2 FIDUCIAL MARK · FD4 FIDUCIAL MARK

FD6 FIDUCIAL MARK · FD5 FIDUCIAL MARK

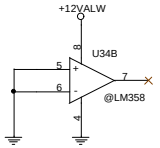
CF3 CF1 CF14 CF18 CF2 — SMDC40M80

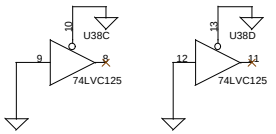
CF4 CF13 CF10 CF6 CF15 — SMDC40M80

CF12 CF7 CF11 CF17 CF16 — SMDC40M80

CF8 SMDC40M80

Spare Logic Gate



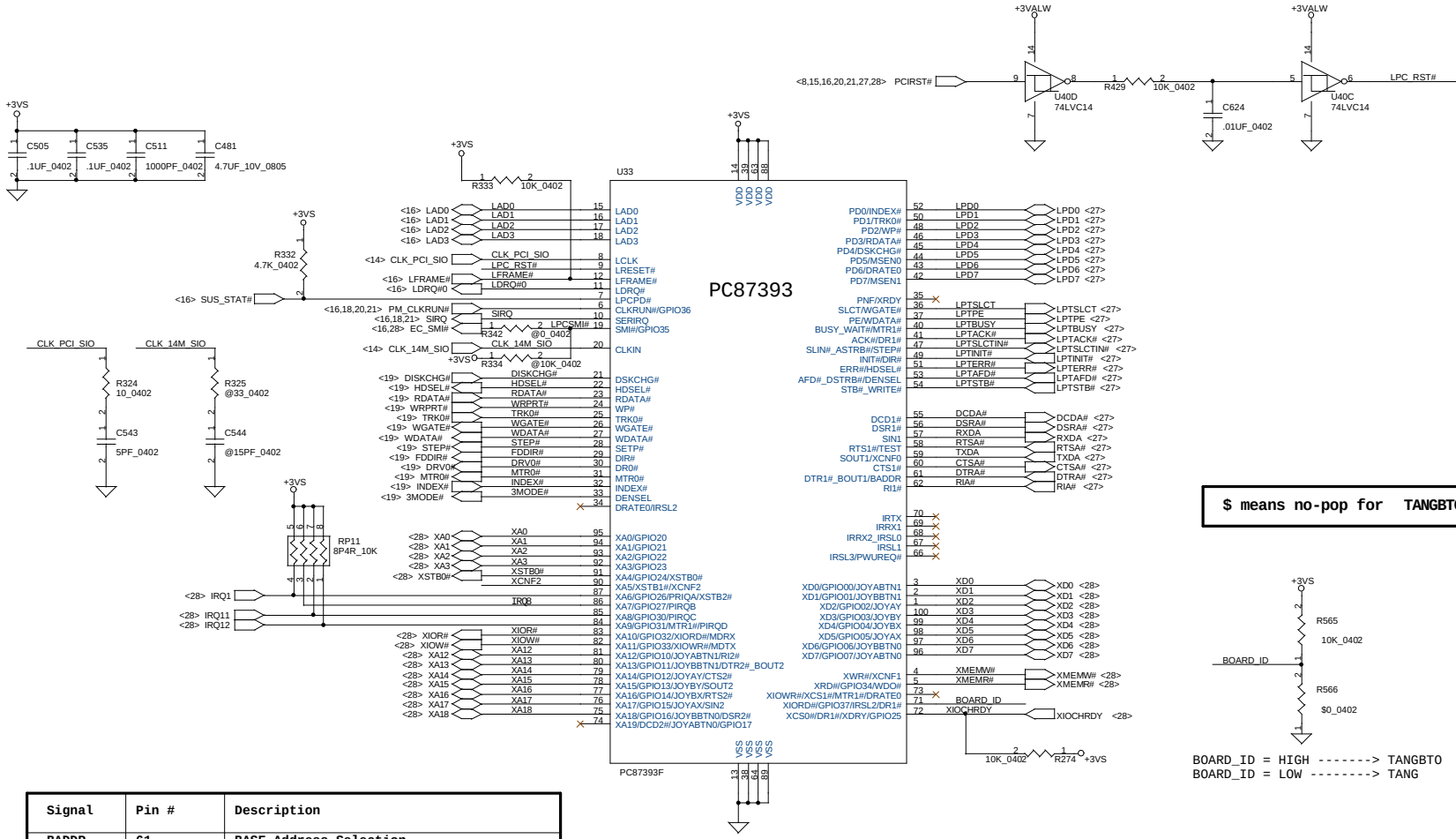


Compal Electronics, Inc.

Title: **MDC connector / Skew Hole**

Size: | Document Number: **ADY11 LA-1181** | Rev: 2

Date: Thursday, November 22, 2001 | Sheet 25 of 41



Signal	Pin #	Description		
BADDR	61	BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F		
TEST	58	"0": Normal (Default) "1": Test Mode		
XCNF[2:0]	90, 4, 59	2 1 0	Function	
		x 0 0	No BIOS	
		x 0 1	Normal Mode. XRDY dis abled	
	(default)	0 1 0	Latch Mode. XA12-19, XRDY enab led	
		1 1 0	Latch Mode. GPIO10~17,XRDY enab led	
		0 1 1	Latch Mode. XA12-19, XRDY disab led	
		1 1 1	Latch Mode. GPIO10~17,XRDY disab led	

* 1 ROM SOLUTION

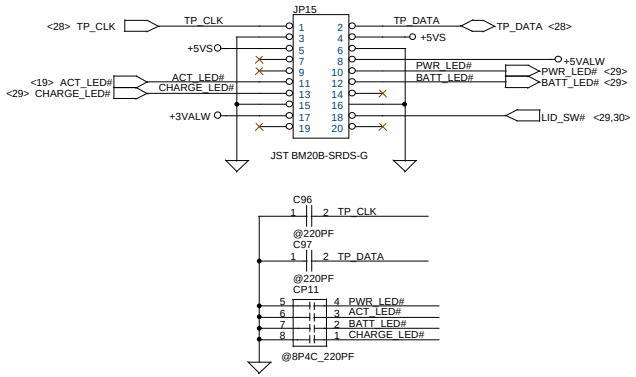
Compal Electronics, Inc.

Title: LPC Super I/O NS PC87393

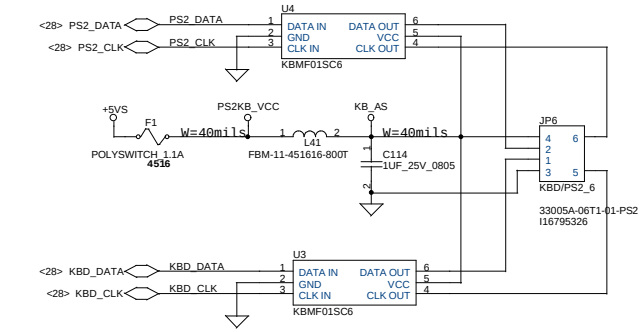
Size: | Document Number: ADY11 LA-1181 | Rev: 2

Date: Friday, November 16, 2001 | Sheet 26 of 41

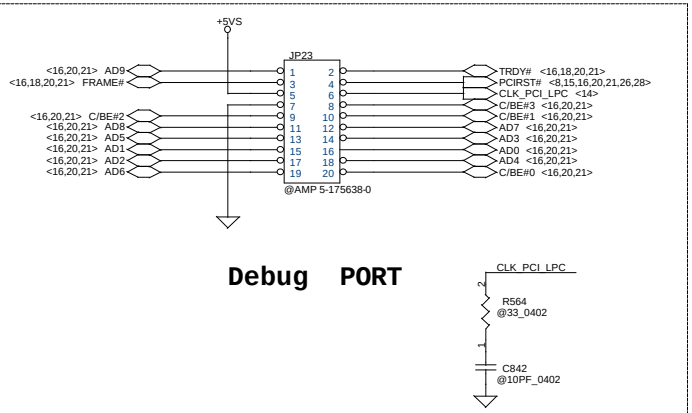
Touch Pad & Status LED Conn.



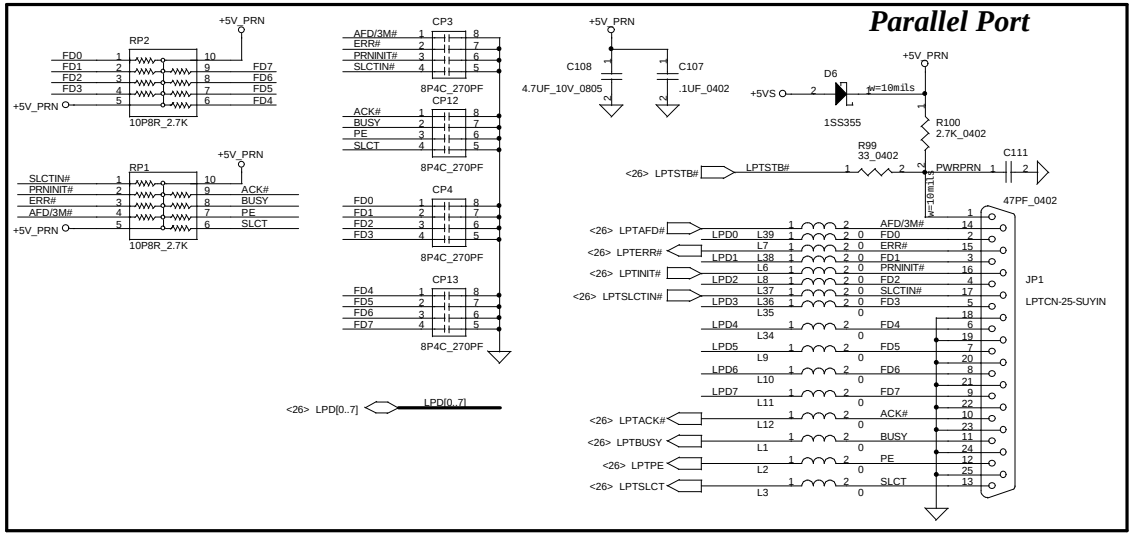
PS2 CONN.



Debug PORT

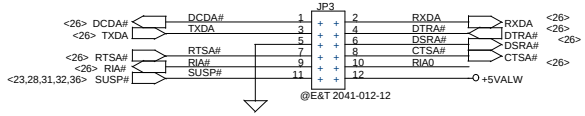


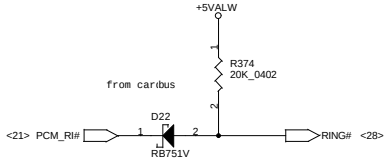
Parallel Port



S/W debug only

ACPI Debug port



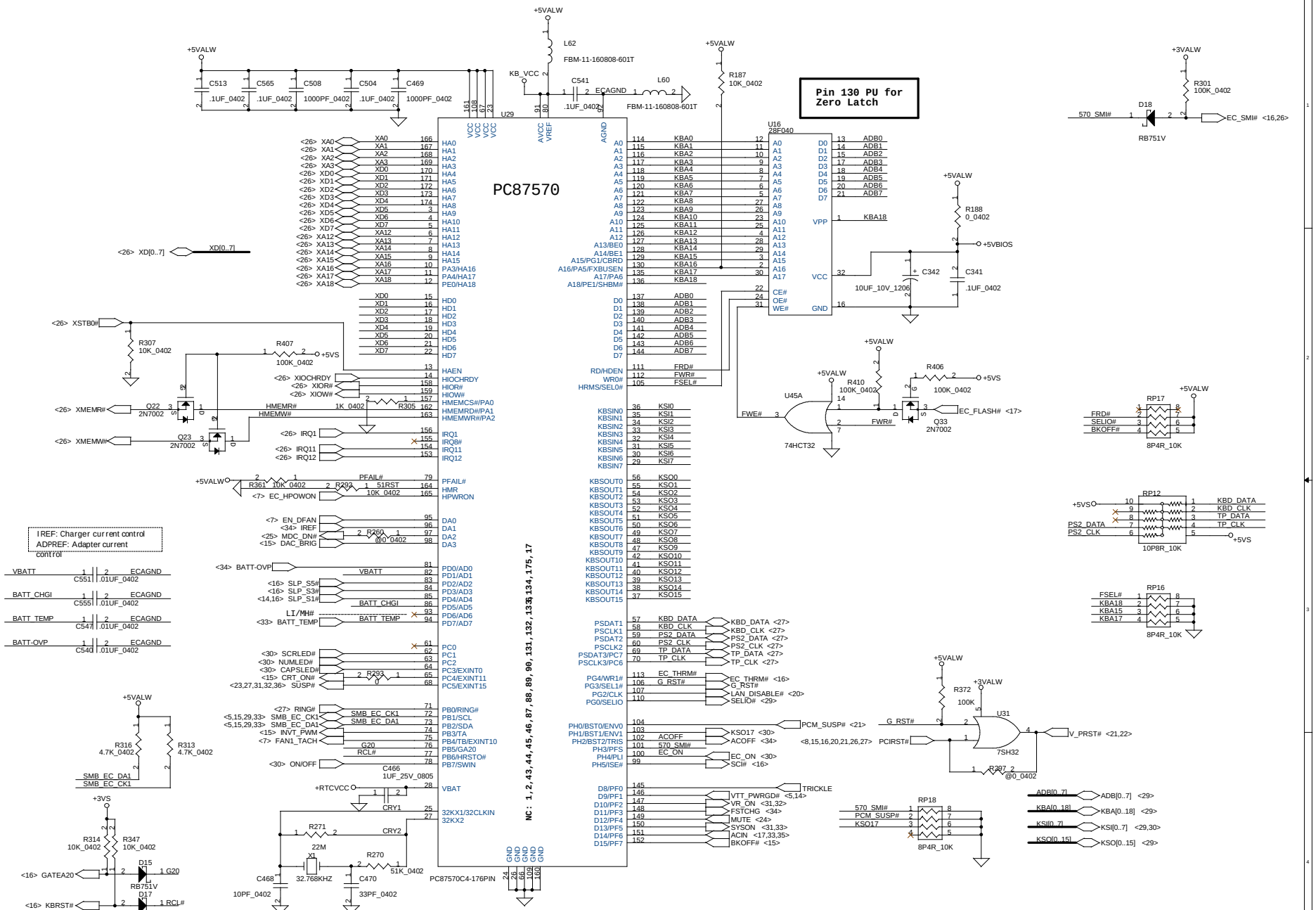


Compal Electronics, Inc.

Title: PIO/SIO/PS2 Port/T_P Conn. & LPC Debug Conn.

Size: | Document Number: ADY11 LA-1181 | Rev: 2

Date: Monday, November 19, 2001 | Sheet 27 of 41



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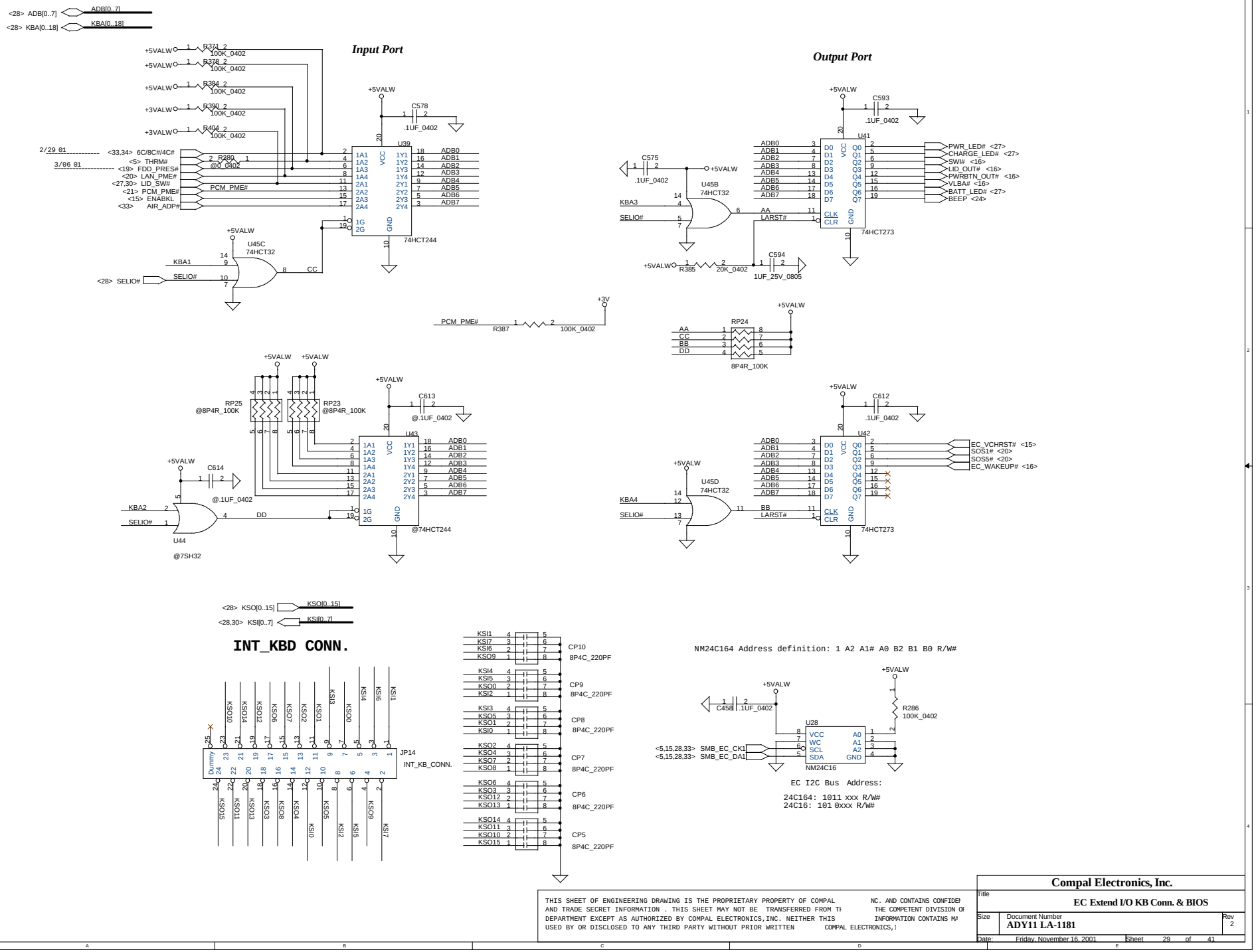
Compal Electronics, Inc.

Title	PC87570	
Size	Document Number: ADY11 LA-1181	Rev: 2
Date: Friday, November 16, 2001	Sheet 28 of 41	



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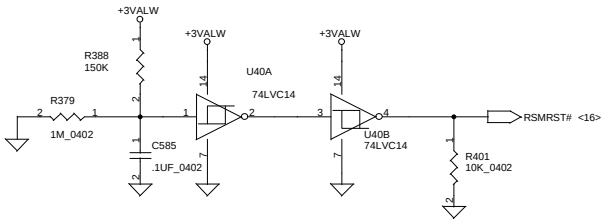
Compal Electronics, Inc.

Title: **EC Extend I/O KB Conn. & BIOS**

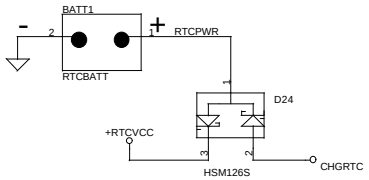
Size: | Document Number: **ADY11 LA-1181** | Rev: 2

Date: Friday, November 16, 2001 | Sheet 29 of 41

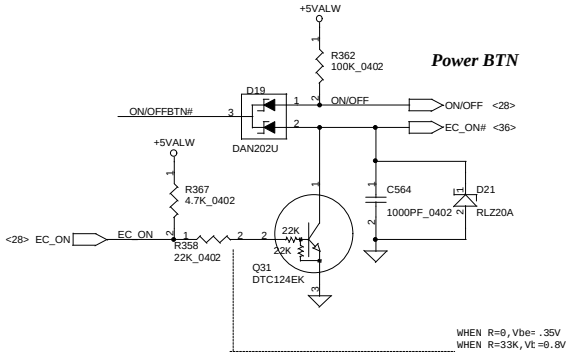
Power ON Circuit

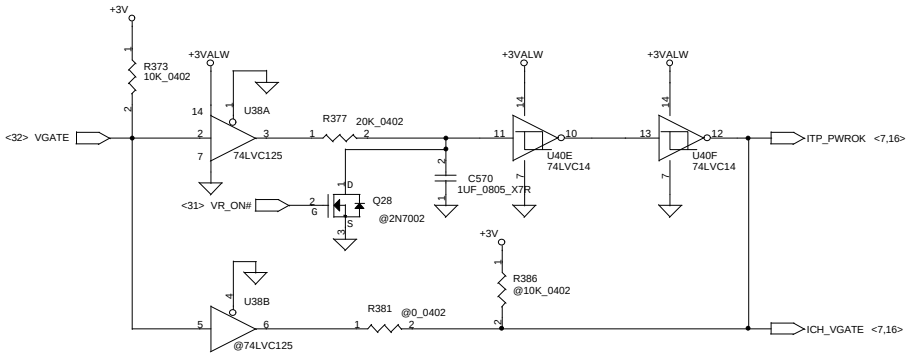


RTC Battery

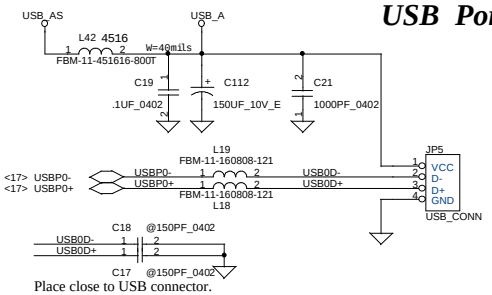


Power BTN



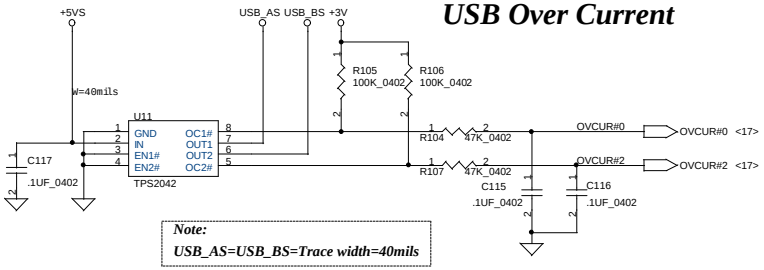


USB Port 0



Place close to USB connector.

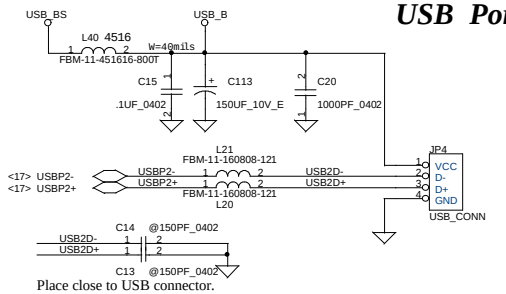
USB Over Current



Note:

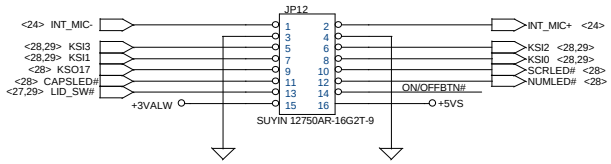
USB_AS=USB_BS=Trace width=40mils

USB Port 1



Place close to USB connector.

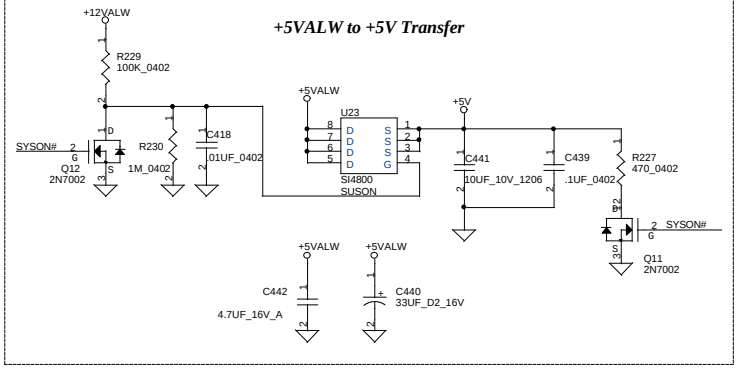
LID Switch & Function Button



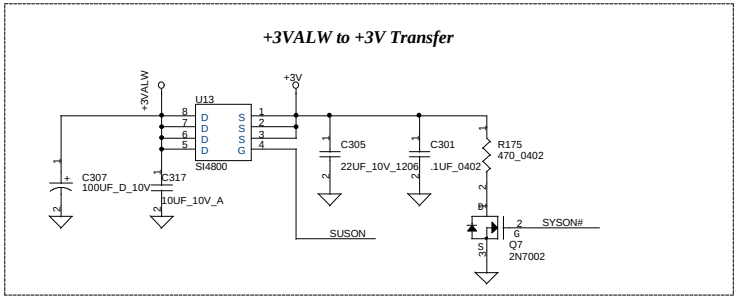
Compal Electronics, Inc.

Title	Power OK/Reset/RTC battery/USB Conn.& Lid Switch	
Size	Document Number ADY11 LA-1181	Rev 2
Date: Friday, November 16, 2001	Sheet 30 of 41	

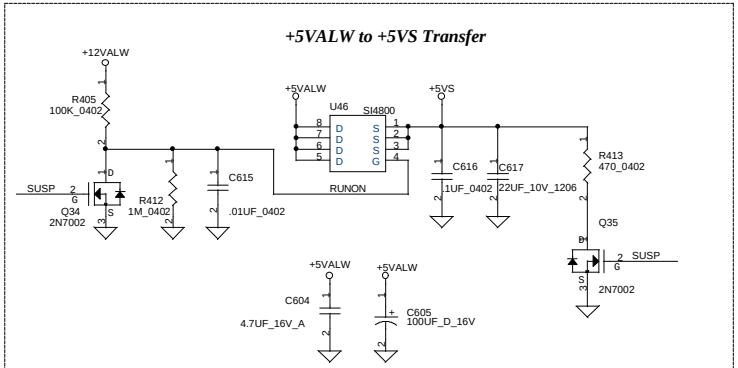
+5VALW to +5V Transfer



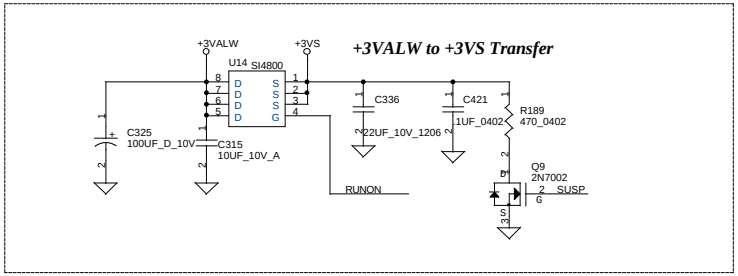
+3VALW to +3V Transfer

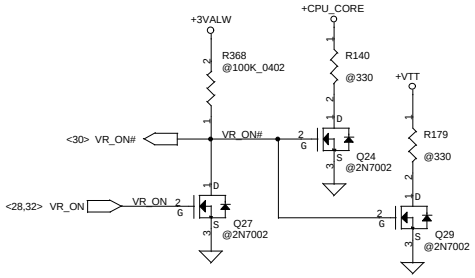


+5VALW to +5VS Transfer

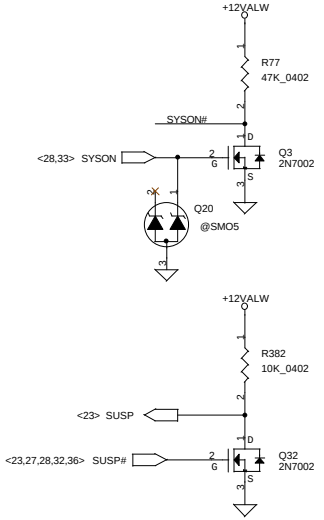


+3VALW to +3VS Transfer

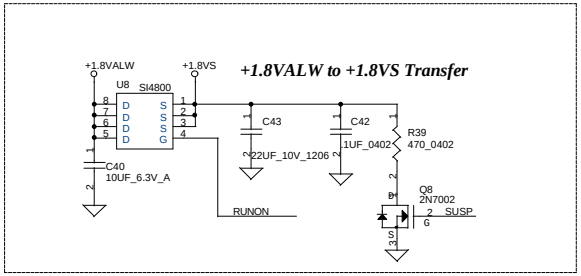




1.8VALW/+1.5VS Power direct prov ide



+1.8VALW to +1.8VS Transfer



Compal Electronics, Inc.

Title	DC/DC Circuit	
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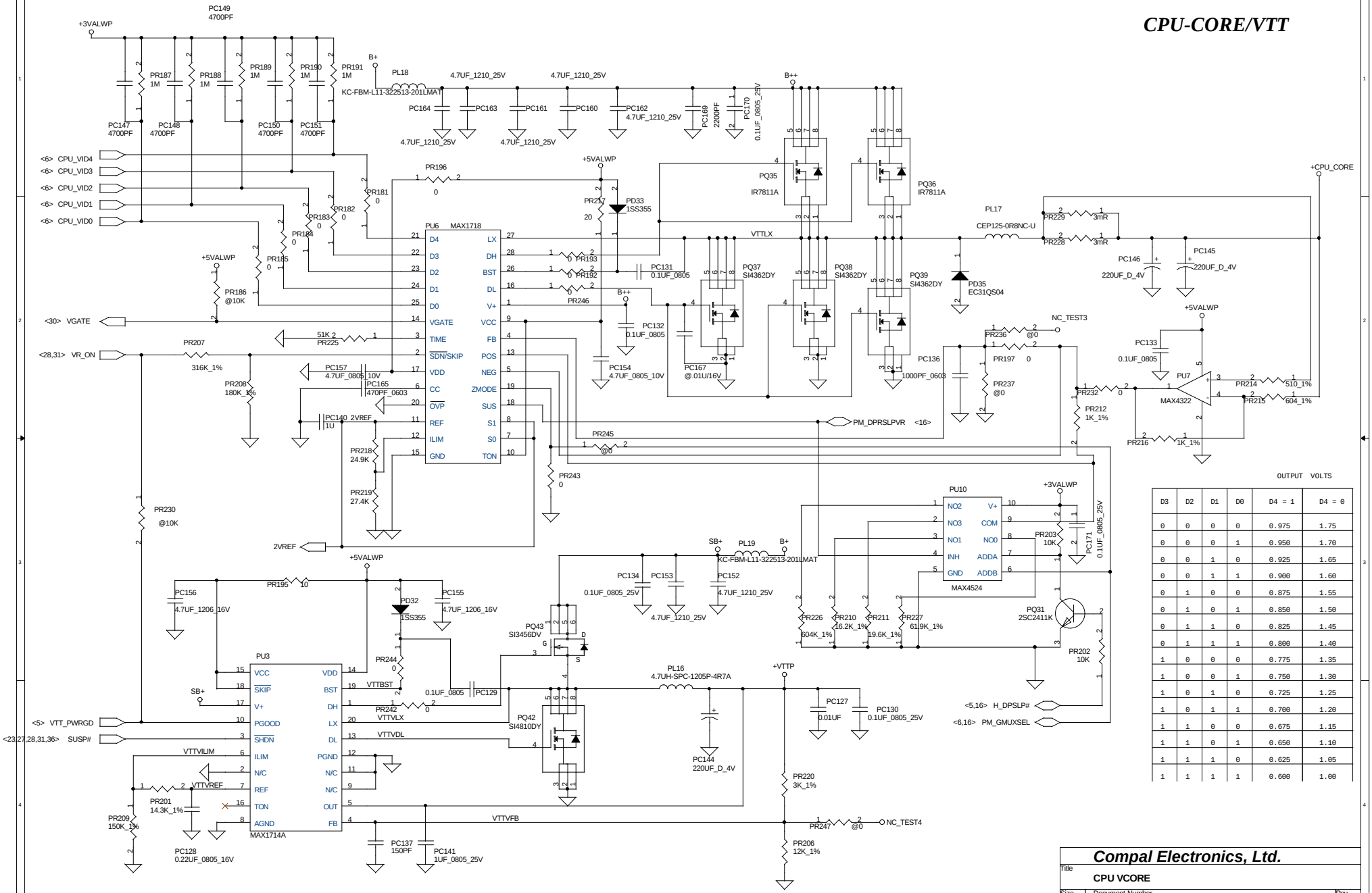
CPU-CORE/VTT



OUTPUT VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	0	0	1	0.950	1.70
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

Compal Electronics, Ltd.

Title	CPU VCORE	
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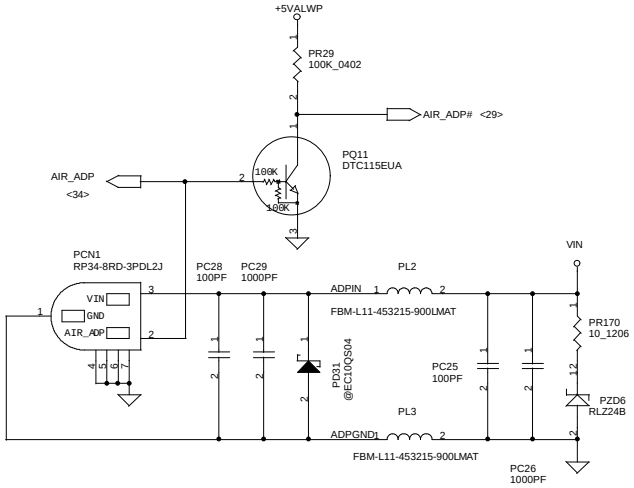
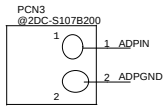
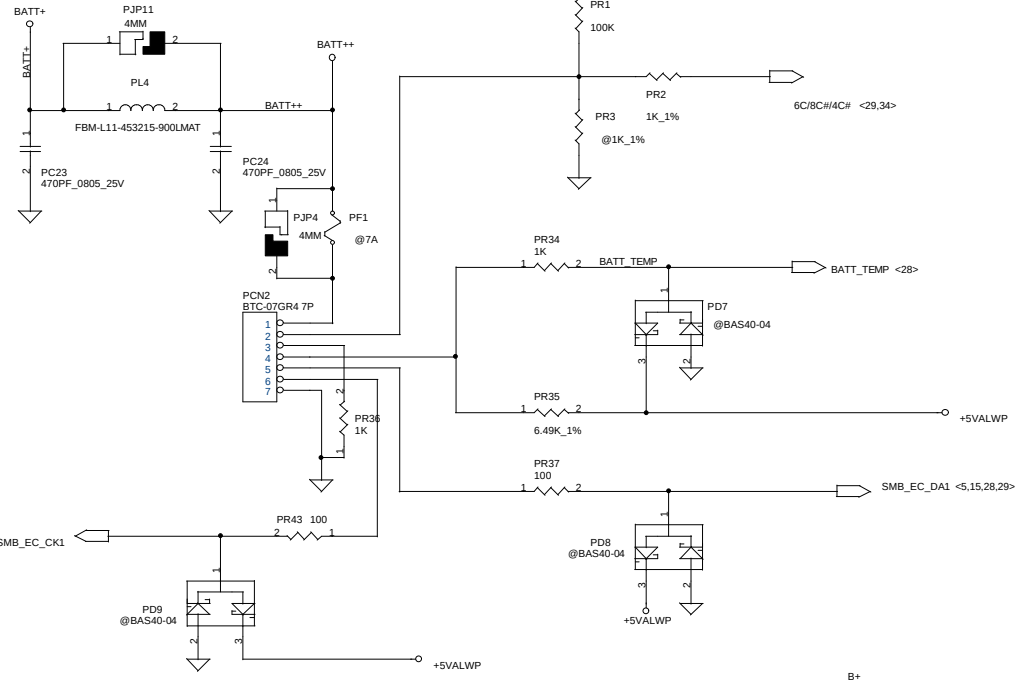
Detector



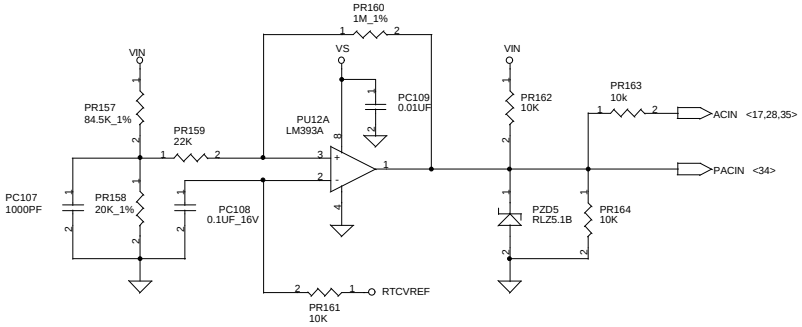


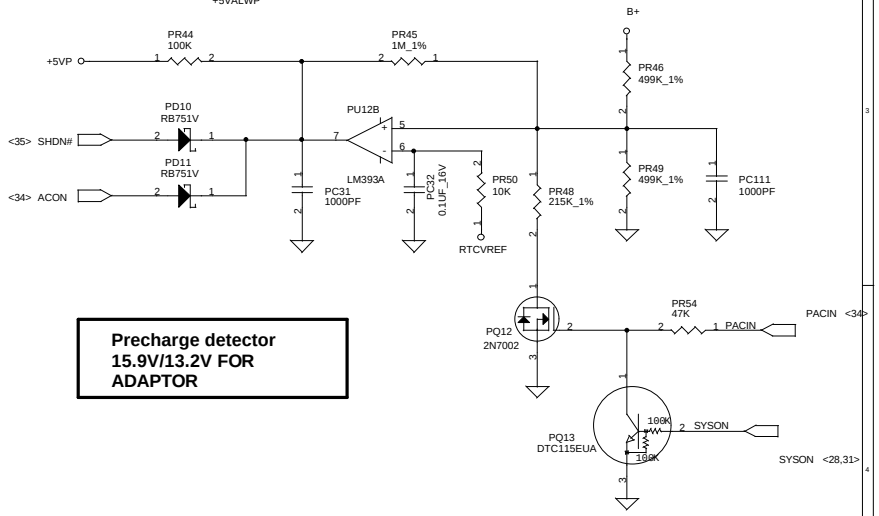


PCN2 battery connector pin assignm ent

SMART Battery:
1.BAT+
2.LI/MH#
3.B/I
4.TS
5.SMB_EC_DA1
6.SMB_EC_CK1
7.GND

Vin Detector 17.93V/17.2V





Precharge detector 15.9V/13.2V FOR ADAPTOR

Compal Electronics, Inc.

Title	Detector	
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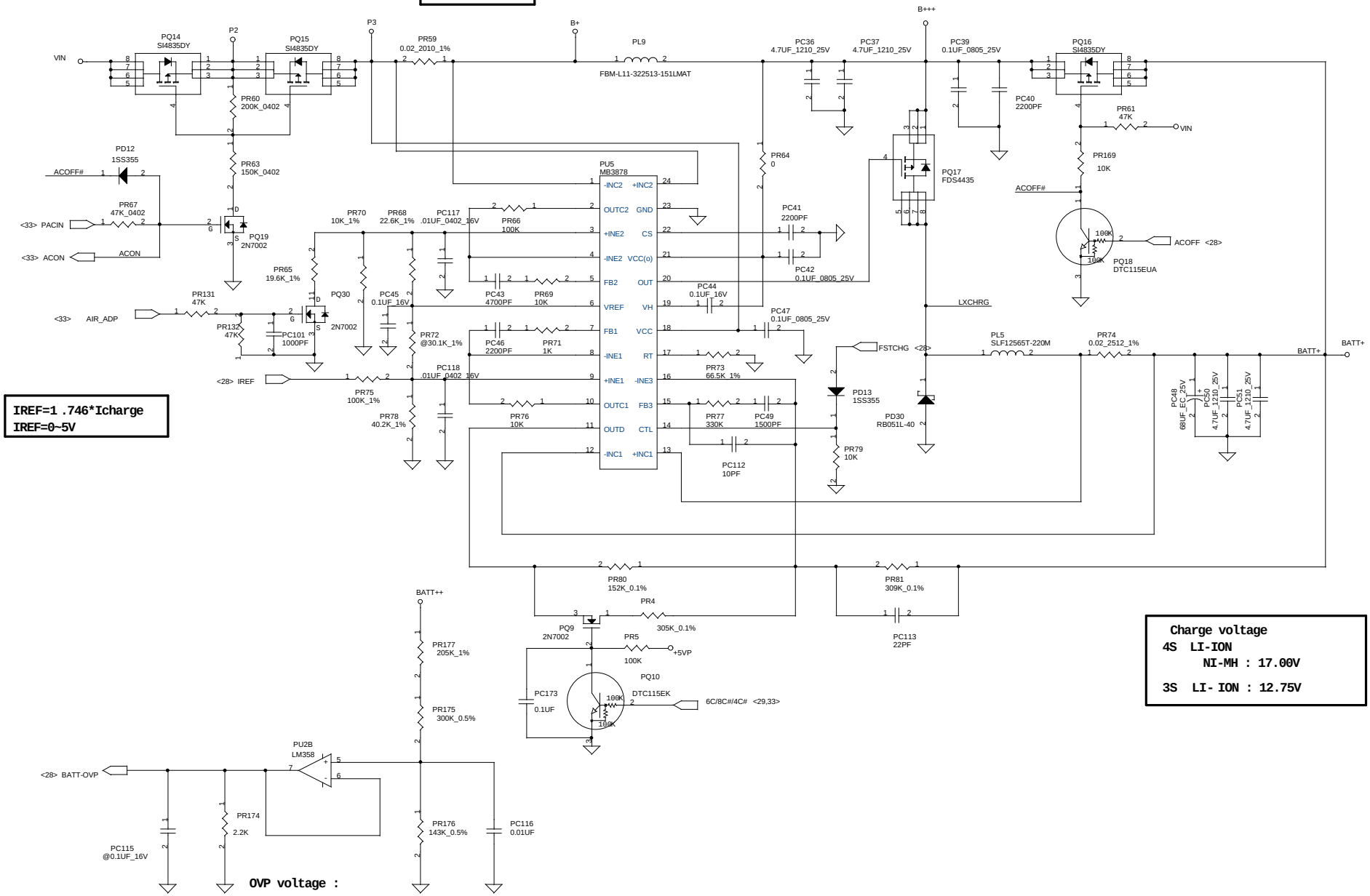
Charger

Iadp=0~3.07A
Iair=0~2.26A



IREF=1 .746*Icharge
IREF=0~5V

Charge voltage
4S LI-ION
NI-MH : 17.00V
3S LI- ION : 12.75V

OVP voltage :

LI-4S :18.0V----BATT-OVP =3.97V

LI-3S :13.5V----BATT-OVP =2.98V

BATT-OVP=0.2 206*BATT++

Compal Electronics, Inc.	
Title	Charger
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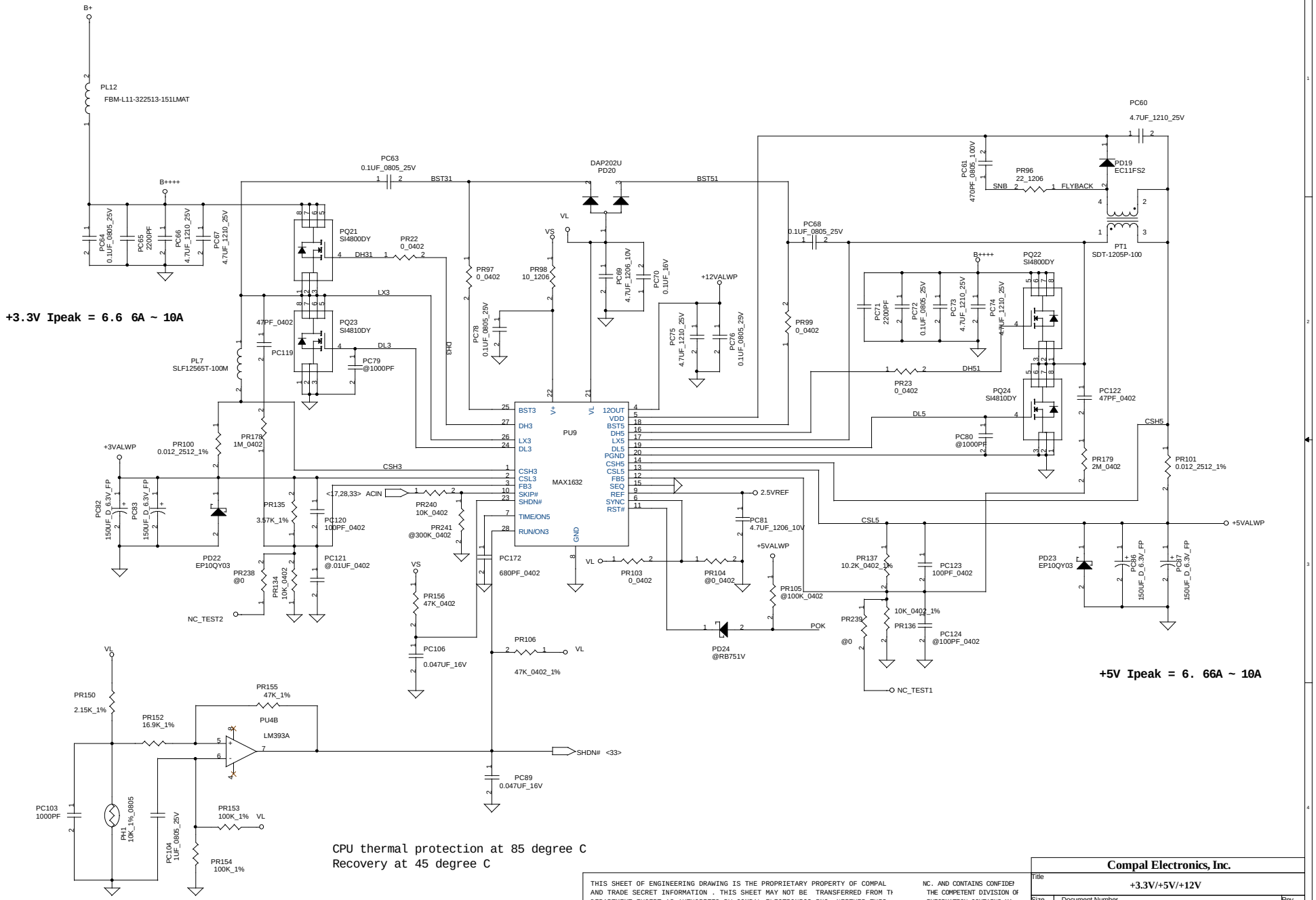
+3.3V/+5V/+12V



+3.3V Ipeak = 6.6 6A ~ 10A

+5V Ipeak = 6. 66A ~ 10A

CPU thermal protection at 85 degree C
Recovery at 45 degree C

Compal Electronics, Inc.

Title	+3.3V/+5V/+12V	
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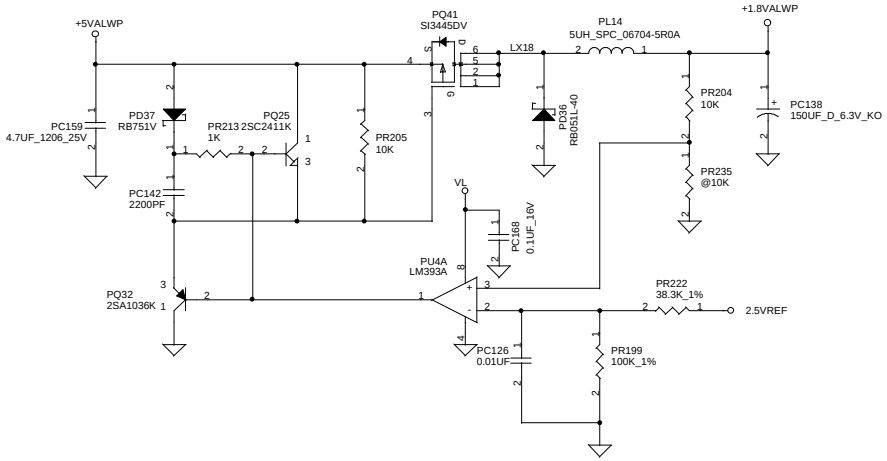
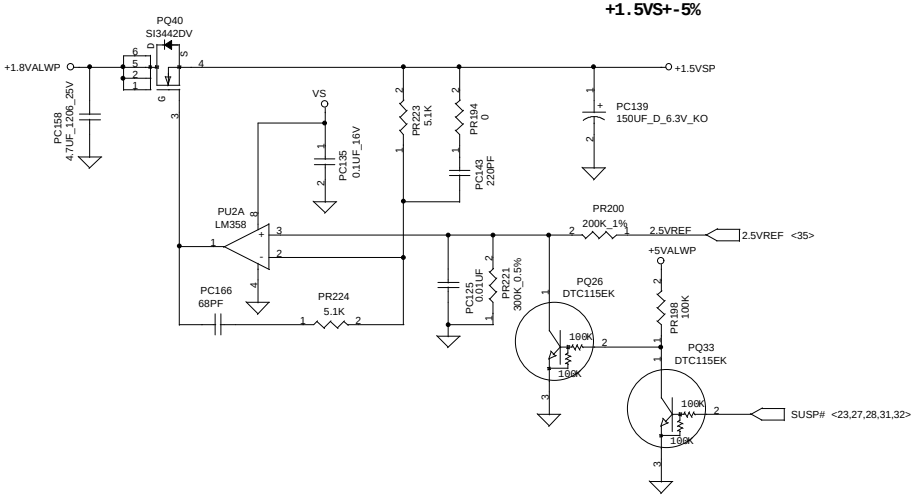
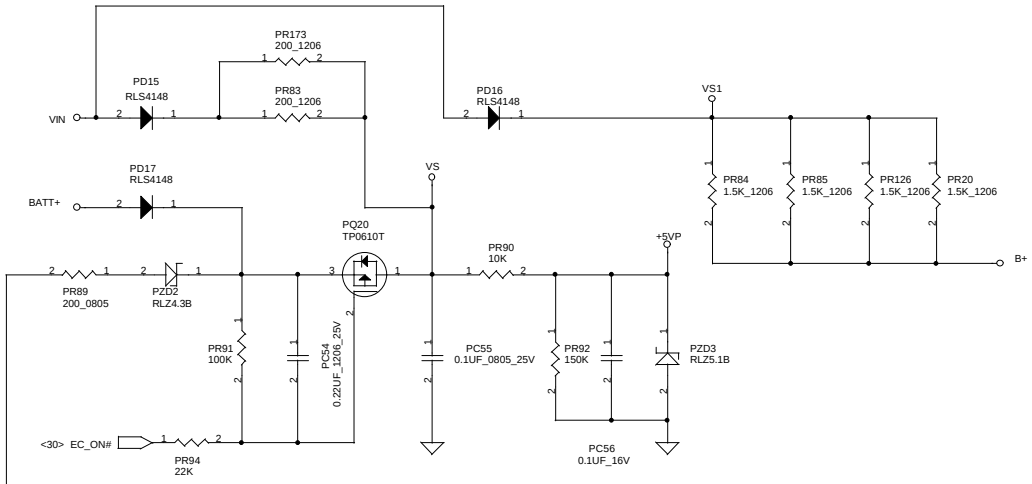
+1.8VALW/+1.5VS

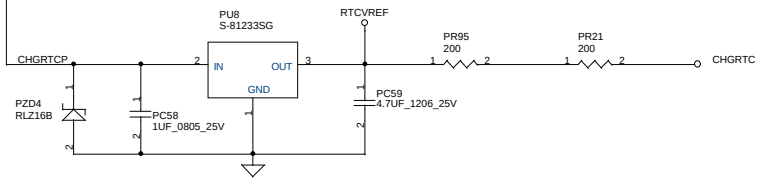
+1.8V+-5%

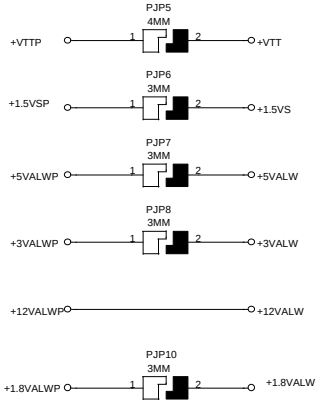


+1.5VS+-5%









Compal Electronics, Inc.		
Title: **+1.8VALW**		
Size	Document Number: **ADY11 LA-1181**	Rev: 2
Date: Tuesday, November 20, 2001	Sheet 36 of 41	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Core-logic Chipset r evision	Revision er ror	0.1B	3	FW82830M should be QB88 and FW8280 1CAM should be QB6 3	0.1	SST
2	Leakage is sue	+5VSHDD is on when plug AC-in and OS en ter S3,S4,S5. we used GPIO25 of ICH3-M to control IDE power,but this pin is resume plane, keep high af ter RSMRST#.	0.1B	19	Q14 pin3 change from +5VALW to +5V S power plan	0.2	SST-2
3	Leakage is sue	+5VS has about 500mv backdrive on S3;U2 6 is +5VS but pin9 pull up to +3V	0.1B	7	R94 pull up change t o +3VS	0.2	SST-2
4	Leakage is sue	+3VS has about 253mv backdrive on S3;Q 16 is on when S3	0.1B	12	R268 pull up change t o +3VS	0.2	SST-2
5	Leakage is sue	+3VS has about 253mv backdrive on S3;U37 pinU5 (ICH_THRM#)is +3VS plane	0.1B	16	ICH_THRM# pull up change to +3VS	0.2	SST-2
6	SM_CLK/DATA read and progr am failed	Signal connect e rror	0.1B	14	Correct net,U9 pin29 should be connec t to SMB_DATA U9 pin30 should be connect t o SMB_CLK	0.2	SST-2
7	Level shi ft	U26 is +5V output,but ICH3(U37)pinAA 6 is 3V level	0.1B	7	Change R415 from 100_0402 to 5.6K_04 02;BOM change	0.1	SST
8	Correct Part v aule	BOM and schematic vaule d ifferent	0.1B	19 20	Change JP20 vaule from"HH9927-S6" t o"HH9921-S6" Change JP10 vaule from"JM361 13-L1H" to "JM36113-L5 H7"	0.1	SST
9	None	Original design, EC_FLASH control by IC H3-M GPIO40 or 97338 pin 71. Follow compal common desi gn, use ICH3-M GPIO40 control EC_F LASH#.	0.1B	27	Change U33(97338) pin7 1 to NC	0.2	SST-2
10	VR_ON cont rol	For EC can control VR_ON after VT T_PWRGD# on	0.1B	29	VTT_PWRGD# connect to U2 9 pin146	0.2	SST-2
11	Debug ca rd	Design change,used PCI port 80 debug card solution	0.1B	28	Change JP23 connector type from "SUYI N 12793-10G2" to "AMP 5-175638-0";BOM change	0.2	SST-2
12	None	FAN power transistor change. Max. power of 2 SC2411 is 0.2W. Max. power of FMMT619 is 0.615W.	0.1B	7	Change Q4 from "2SC2411EK" to "FMMT619" BOM chan ge	0.2	SST-2
13	Component pad size	Component is 0402 size,but layout pad size is 0603	0.1C	17	Layout modified and correct vaule from"5PF" to "5PF_0402";BOM needn't change	0.2	SST-2
14	Mechanical limit issue	Mechanical limit H:2.2mm,used compone nt over limit	0.1C	32	Change C440 from "100UF_D_16V" to " 33UF_D2_16V" D2 size H=1.9mm; BOM change	0.2	SST-2
* 15	Delect item 11	PT implement PCI port 80 solution	0.1C	28	SST2 don't ch ange	0.2	SST-2
16	Clock wavef orm	Clock waveform ove r SPEC 1.CLK_HCLK/H CLK# 2.CLK_DR EF 3.CLK_ICHA PIC	0.1C	14 16	1.Change R16,R12 from"33_1%" to"10_1%" 2.Change R59 from"22_0402" to "10_0402" 3.Pop R352 (10_0402) and pop C559(10PF_04 02)	0.2	SST-2
17	None	LPC debug card on developer stage , depop it.	0.1C	28	Depop JP23 (S ST2)	0.2	SST-2
18	Correct Part v aule	BOM and schematic vaule d ifferent	0.1D	24	Change R383 vaule from "29K_1%" to "28.7K_1%"	0.1	SST
19	Fixed EE issue list item11(2001/6/5)	Intel recommend series resistor on IDERST	0.1D	17	Add R453(0_0402) series resistor on PIDERST #--- BOM modify	0.2	SST-2
20	Fixed EE issue list item10(2001/6/5)	VCCA_DAC should have a 0.1uf and 0 .01uf nearby	0.1D	10,11	We check layout file,C290 closely U7 pin AF26,so change C290 from pag11 to pag10, C156 and C 186 change to page 11(not change layout),and add C632 [0.01UF_0402] near AF 26	0.2	SST-2
21	Fixed EE issue list item26,27(2001/7/12)	1.Change CPU thermal skew hole s ize change. 2.CD-ROM skew hole size change.	0.1D	26	1.Change H1,H2,H6,H7 from 2.8m m to 3.2mm 2.Change H9 from 3.5mm long by 3.0mm wide	0.2	SST-2
* 22	CLK_HCLK/HCLK# resistor need n't change	Follow Dell's reco mmend	0.1E	14	R12,R16 resistor to restore,de l item16-1	0.1	SST
23	ICH3 revis ion	SST2 used QB62 or SL5LF revision	0.1E	17	Change R376 from"22.6_1%" to "18.2_1% ",BOM already change O K.	0.2	SST-2
24	CLK EMI is sue	Add AC termination on as belo w signals 1.CLK_GB IN 2.CLK_ICHH UB 3.CLK_ICH 48 4.CLK_PCI_S IO 5.CLK_GBO UT 6.CLK_ICHP CI	0.1F	8 16 27 14 16	1.Pop R168(33_0402) and C297(5PF_0402) 2.Pop R306(33_0402) and C514(5PF_0402) 3.Pop R369(10_0402) and C574(5PF_0402) 4.Pop R324(10_0402) and C543(5PF_0402) 5.Pop R69(33_0402) and C92(1 0PF_0402) 6.Pop R311(10_0402) and C518(15PF_0402)	0.2	SST-2
25	None	Gerber rele ase	0.2		Change Schematic revisio n to 0.2	0.2	SST-2

Compal Electronics, Inc.

Title: **P.I.R History**

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
26	None	Connector cha nge	0.2A	19	FDD Connector change to ACES 85201-2605	0.3	PT
27	None	Remove OZ6933 PCMCIA Co ntroller	0.2A	21 25	1. Del Page 21, and shift down page 2. Del CF5, CF9	0.3	PT
28	None	Remove Power Switch (2 slot) and change Ca rdBus Connector	0.2A	22	1. Schematic remove U20, C437, C403, C402 , C436, C434, C433, C415, C408, C429, R219, R211, C79, C 80, C430, C318, L53, C358, C343, C401 2. Change PCMCIA Socket vaule to FOXCO NN 1CA415M1-TA	0.3	PT
29	None	Add Board_ID for check Mosaic and Tang	0.2A	26	Add U33 Pin71 for BOARD_ID, and Add Resiste r R565 10K_0402 and R566 0_0 402	0.3	PT
30	None	Remove Serial Port	0.2A	27	De-pop C1, C5, C10, C11, C109, U1, JP3, CP1, CP2, L26, L27, L28, L29, L30, L31, L32, L33, Q26.	0.3	PT
31	None	Lid Switch function change to Touc h-pad Board	0.2A	27	Schematic change, JP15 Pin17 net to +3VS, JP15 Pin18 net to LID_S W#	0.3	PT
32	None	Debug Port change con nector	0.2A	27	Debug Port change connector from SUYIN 12793A-10G2 to AMP 5-17563 8-0	0.3	PT
33	None	Power on switch board change connector	0.2A	30	Power On switch board change from AM P 4-175638 to SUYIN 12750AR-16 G2T-9	0.3	PT
34	None	ICH_VGATE de lay	0.2A	30	1. Schematic change, connect R381 pin2 to U40 Pin12 2. De-pop R386, R381	0.3	PT
35	None	Schematic remove Serial PORT function	0.2A	27	Schematic remove U1, CP1, CP2, C1, C5, C 10, C11, C109, L26, L27, L28, L29, L30, L31, L32 , L33, Q26.	0.3	PT
36	CMOSREF not strong enough t o provide the target 2/3 ratio devider	Change divider to 0.5K/1K at the ne xt available opportunity to gain more CMOSR EF margin.	0.2A	5	BOM change R20 from 1K_1% to 499_1%, R22 from 2K_1% to 1K_1%	0.3	PT
37	None	M/B ID change t o PT	0.2A	17	BOM add R441 10K_0402, Depop R4 43 10K_0402	0.3	PT
38	None	Gerber rele ase	0.3		Gerber release, schematic cha nge to 0.3	0.3	PT
39	Cost do wn	Core_VCC and VTT capacitor reduce.	0.3	6 11	1. BOM depop C126, C120, C293, C210, C283, C118. 2. BOM change from 150UF_D2_6.3V (45mOhm) to 220U_D2_4V(25mOhm), Location C29, C39, C3 2, C292, C260, C119, C153, C289, C37. 3. BOM depop C122, C127. 4. BOM change from 150UF_D2_6.3V (45mOhm) to 220U_D2_4V(25mOhm), Location C27, C23, C303.	0.3	PT
40	None	Remove Capaci tor	0.3B	6	Schematic remove C120.	1.0	ST
41	None	Resister Package e rror.	0.3B	24	Change R351 100K_0603 to R351 100K_0402	1.0	ST
42	Suspend from lid switch, ca n't resume from open L CD.	Change Lid switch power plan from +3 VS to +3VALW.	0.3C	27 29 30	1. Schematic JP15 Pin.17 t o +3VALW 2. Schematic JP12 Pin.15 t o +3VALW 3. Schematic R404 Pin.1 t o +3VALW	1.0	ST
43	For thermal module difference Mosaic-P4	Add stand-off on mother board.	0.3C	6	Schematic remove C39, add M11 S MDC200M157, BOM add C283 220U_ 4V_D2.	1.0	ST
44	None	Change Capacitor spec.	0.3C	31	BOM change C307, C325, C605 from 10 0UF_D_16V to 100UF_D_10 V.	1.0	ST
45	CRT connector layout shift.	Shift CRT connector 1.33mm	0.3C			1.0	ST
46	Factory DXF fix.	Layout modi fy.	0.3C			1.0	ST
47	Test point rev iew.	Layout modi fy.	0.3C			1.0	ST
48	3COM 3C920 referance RJMA G version update .	VDDPCI[1:5] pins from +3VASB to +3VS.	0.3C	20	1. Schematic modify, U21 some pin change p ower plan from +3VASB to +3VS (VDDPCI [1:5]) 2. Schematic C370, C371, C373 change po wer plan from +3VASB to +3 VS.	1.0	ST
49	Poor quality w/static noise on recording func tion.	Change MIC-AMP power plan.	0.3C	24	1. Schematic modify, MIC-AMP change power plan from VDDA to AVDD_MIC with R567 49.9Ohm to AVDD_AC97 2. Schematic add C633 10UF_ 10V_1206	1.0	ST
50	None	M/B ID change t o ST	0.3D	17	BOM depop R441, R444, add R442, R4 43 10K_0402	1.0	ST
51	None	Change Back-light gate pow er plan.	1.0	15	1. U12 power plan from +3VS to +5VS. 2. U12 from SH08 t o ST08		

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	CPU_CORE voltage is unstable	Change PWM frequency from 300KHZ to 200KHz	0.1B	33	1.Change PR197 from 100 to 0 2.Connect pin10 of PU6 to pin9 of PU6	0.1	SST
2	+5VALWP is unstable	Change PWM frequency from 200KHz to 300KHz	0.1B	36	1.Delete PR104 and add PR103 0_0402 2.Connect pin15 of PU9 to ground	0.1	SST
3	Output capacitor of Charger interfere mechanical (switch board)	Change PC48 to small size,the height limited is 6mm in this area	0.1B	35	Change PC48 from 100UF to 68UF	0.2	SST2
4	The time sequency of +1.5VS is error	Change REF voltage from 2VREF of MAX1718 to 2.5VREF of MAX1632	0.1B	37	.Change PR200 from 100K_1% to 200K_1%	0.2	SST2
5	The time sequency between 1.8VALWP and 3.3VALWP is error	Delay 3.3VALWP start-up time	0.1B	36	Add PC172 680PF connected to pin7 of PU9	0.2	SST2
6	RTC battery that will be shortage.We changed RTC battery from Panasonic VL1220 to Maxell ML1220	Change LDO charger to 3.3V for Maxell ML1220 Modify Vin Detector and Precharger Detector circuit	0.1B	37 34	Change PU8 from S-81235SG to S-81233SG 1.Change PR157 from 78.7K_1% to 84.5K_1% 2.Change PR48 from 249K_1% to 215K_1%	0.2	SST2
7	Correct part vaule	BOM and schematic vaule different	0.1D	37	Change PL14 vaule from"5UH_SPC_06703" to "5UH_SPC_06704-5R0A"	0.1	SST
8	Correct curreent limited value	Modify current limited from 2.86A to 3.22A	0.1E	35	1. Change PR68 from 24.9K_1% to 21K_1% 2. Change PR65 from 14.3K_1% to 15.8K_1%	0.1	SST
9	Correct OCP of +VTT	Modify OCP current from 4.6A to 7A,because peak current of +VTT is 6A in spec.	0.1E	33	1. Change PR201 from 10K_1% to 14.3K_1% 2. Change PR209 from 15K_1% to 150K_1%	0.1	SST
10	Add ferrite bead for EMI	Based on EMI dept. test result, we must add bead and change capacity for EMI issue	0.1F	34	1. Add PL4 FBM-L11-453215-900LMAT 2. Change PC 24 from 0.1UF to 470PF and add PC23 470PF	0.3	PT
11	Add NI-MH battery	prevent NI-MH battery over charge/discharge	0.1F	34	Add PF1 7A fuse	0.3	PT
12	Plug in AC adapter and battery on time the system can't turn on.	Separate precharge path from VS net because leakage current is larger than p recharge current	0.1F	37	1. Connect pad2 of PD16 to VIN 2. Add PR20 1.5K and change PR84,PR85,and PR126 to 1.5K	0.3	PT
13	Safety protection for RTC battery	Add PR21 to prevent damging PR95 to damage RTC battery	0.1F	37	1.Add PR21 200 ohm	0.3	PT
14	Design margin is not enough	increase design margin for battery OVP prevent it misses	0.1F	35	Change battery OVP from 18.1V to 18.3V and BATT-OVP will be changed from 4V to 4.04V	0.3	PT

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
15	noise issue from DC-DC	Change choice heighter capacitor	0.1F	35	Change PC60 form 2.2F_1206_25V to 4.7UF_1210_25	0.3	PT
16	Implement 6cell li-on	Add identifird signal 6C/8C#/4C#	0.1F	33	1.Add PR1 100K and PR2 1K_1% 2.Add PR3 no-pop	0.3	PT
17	modify charge voltage	Change 4S charge voltage to 17V for 4 cell/8 cell and NI-MH,other 3S is 12.75V for 6cell	0.1F	34	1. Change PR80 from 100K_0.1% to 152_0.1% 2. Change PR81 from 316K_0.1% to 309_0.1% 3. Add PR4 305K_0.1% and PR5 100K 4. Add PQ9 2N7002 and PQ10 DTC115EK 5. Add PC173 0.1U	0.3	PT
18	AC adapter is changed to 60W	modify constant power limited to 49W and disable air adapter	0.1G	33 34	1. No-pop PCN1 and Populate PCN3 2. No-pop PR29 and PQ11 3. Change PR68 from 21K_1% to 28.7K_1% 4. No-pop PQ30, PR65,PR131,PC101	0.3	PT
19	Add compensation solution for +5VALWP	The solution will reduce quantity of output capacitor and increase stability	0.1G	35	1. Populate PC122 47PF_0402 2. Populate PR179 2M_0402 3. Populate PR137 10.2K_0402_1% 4. Populate PC123 100PF_0402 5. Change PR136 from 0_0402 to 10K_0402_1%	0.3	PT
20	AC adapter is changed to 70W	modify constant power limited to 64W and support air line adaptor identified	0.1H	33 34	1. No-pop PCN3 and Populate PCN1 2. Populate PR29 and PQ11 3. Change PR68 from 28.7K_1% to21K_1% 4. Populate PQ30, PR65,PR131,PC101	0.3	PT
21	Charger can't charge	Pin3 of PQ9 isn't connectted pad2 of PR80	0.3C	34	Pin3 of PQ9 isn't connectted pad2 of PR80	1.0	PT2
22	power limited for airline adapter is disabled	The control signal can't turn on PQ30	0.3C	34	1.Change control signal from AIR_ADP# to AIR_ADP 2.Change PQ30 from TP0610T to 2N7002	1.0	PT2
23	Delete on-pop component	Because the reverse component is not need	0.3C	35	Delete PC84,PC85,PC88	1.0	PT2
24	Add FUSE for safety of battery	Support NI-MH battery	0.3D	33	Reverse PF1 and add PJP4	1.0	ST
25	Fix Battery OVP protect point	Fix the table of Battery OVP and reserve PC115 about OP Amps oscillates	1.0	34	No-pop PC115	1.0	ST

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
26	enhance conductivity of connector	enhance conductivity of battery connector based on customer's requirement	1.0	33	Change PCN2 from BTC-07GR1 to BTC-07GR4	1.0	ST
27	modify constant power limit spec.	modify constant power limited from 3.22A to 3.07A	1.0	34	1. Change PR68 from 21K_1% to 22.6_1% 2. Change PR65 from 15.8K_1% to19.6K_1%	1.0	ST2
28	Fix DFX issue	The PL14 and PL15 is co-layout, but PL15 will not be used.	1.0	36	Delete PL15	1.0	ST2
29	Fix DFX issue	Delete PJP9 for SMT process.	1.0	36	Delete PJP9		