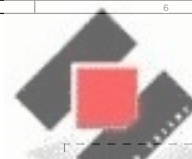
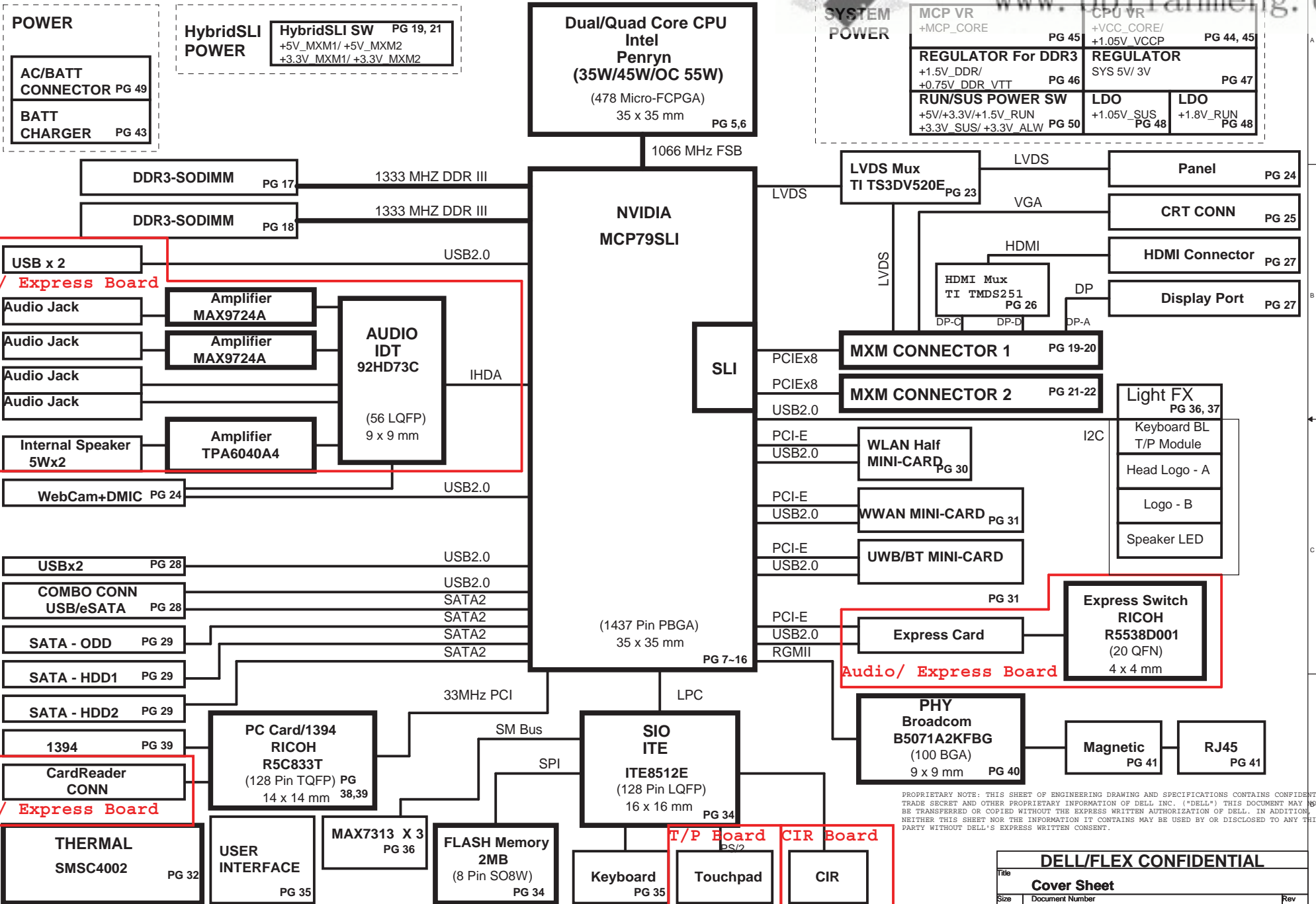


Quicksilver Design



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Power States

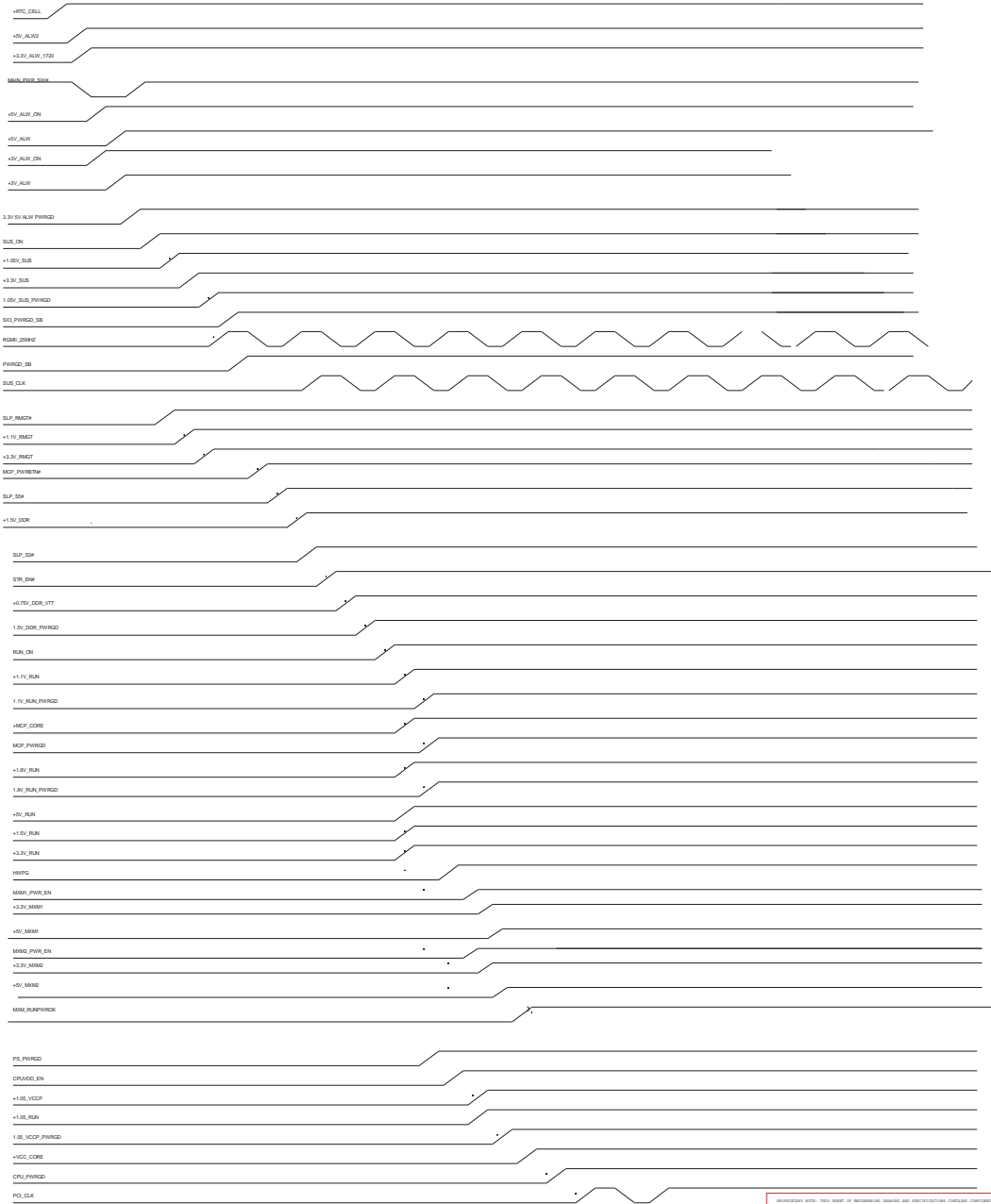
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off
+PWR_SRC	N/A	V	V	V	V	V		
+0.75V_DDR_VTT	RUN_ON	V						
+1.05V_VCCP	CPUVDD_EN	V						
+1.05V_RMGT	SLP_RMGT#	V						
+1.05V_SUS	SUS_ON	V	V					
+1.5V_RUN	RUN_ON	V						
+1.5V_DDR	SUS_ON	V	V					
+1.8V_RUN	RUN_ON	V						
+15V_ALW	N/A	V	V	V	V	V		
+3.3V_ALW	+3.3V_EN2	V	V	V	V	V		
+3.3V_RMGT	SLP_RMGT#	V						
+3.3V_RUN	RUN_ON	V						
+3.3V_SUS	SUS_ON	V	V					
+5V_ALW	+5V_EN1	V	V	V	V	V		
+5V_ALW2	N/A	V	V	V	V	V		
+5V_SUS	SUS_ON	V	V					
+5V_HDD	HDDC_EN	V	TBD					
+5V_MOD	MODC_EN	V	TBD					
+5V_RUN	RUN_ON	V						
+GFX_PWR_SRC	N/A	V	V	V	V	V		
+LCDVCC	ENVDD	V						
+MCP_CORE	RUN_ON	V						
+RTC_CELL	RTC	V	V	V	V	V		
+VCC_CORE	1.05V_VCCP_PWRGD	V						
+USB_RIGHT_PWR	USB_SIDE_EN#	V	TBD					
+USB_LEFT_PWR	USB_BACK_EN#	V	TBD					

By Anthony

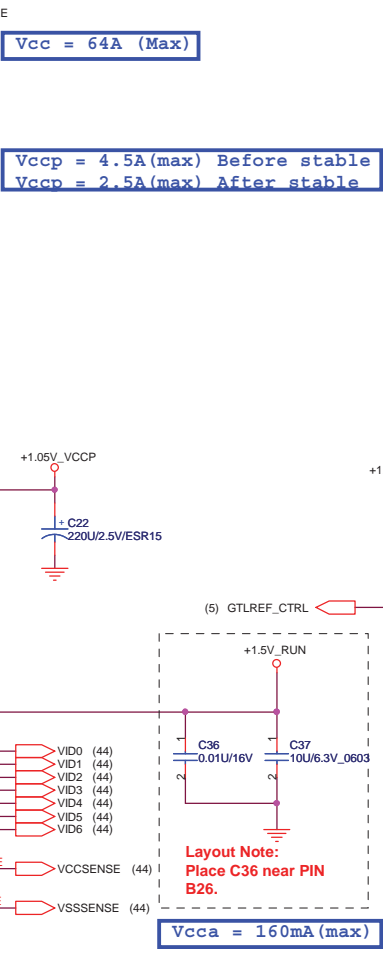
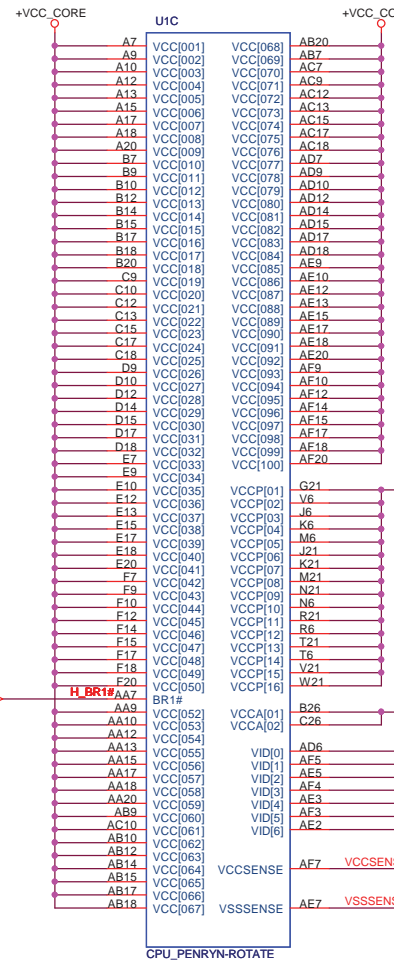
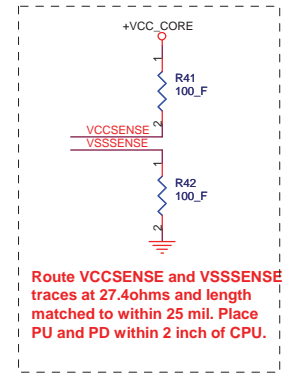
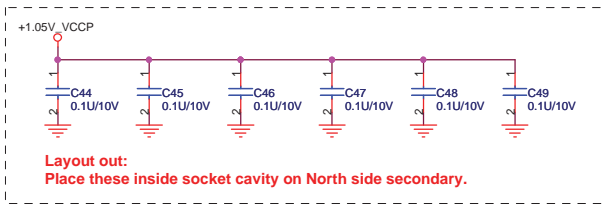
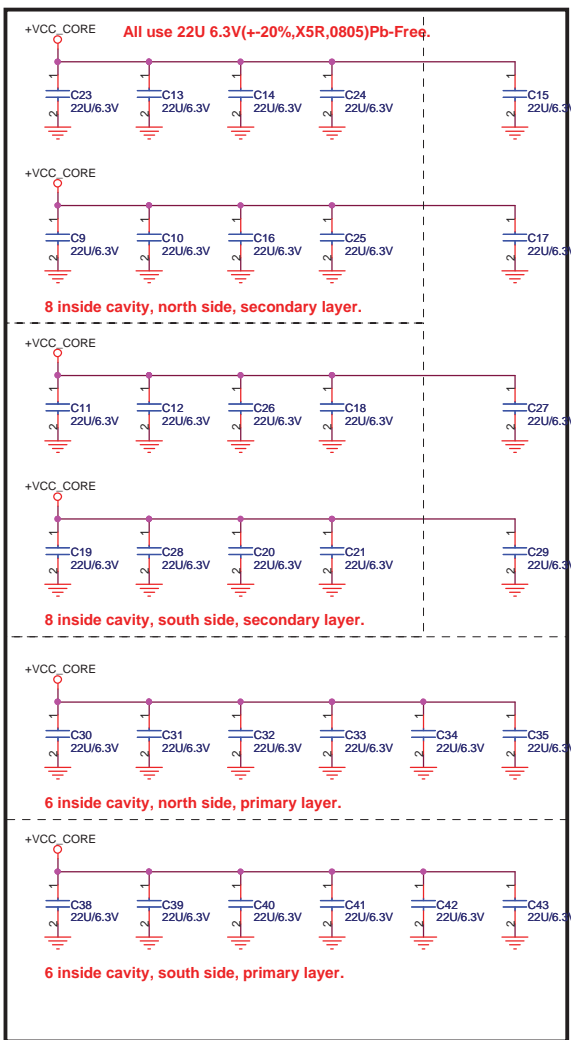
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Quicksilver Power Up Sequence.

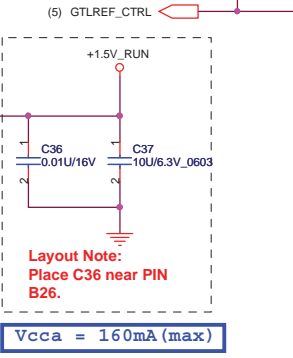


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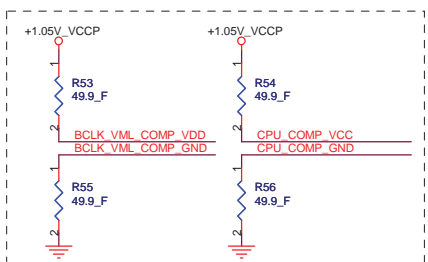
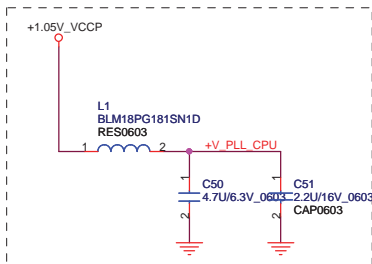
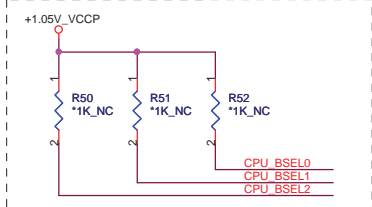
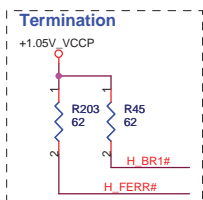
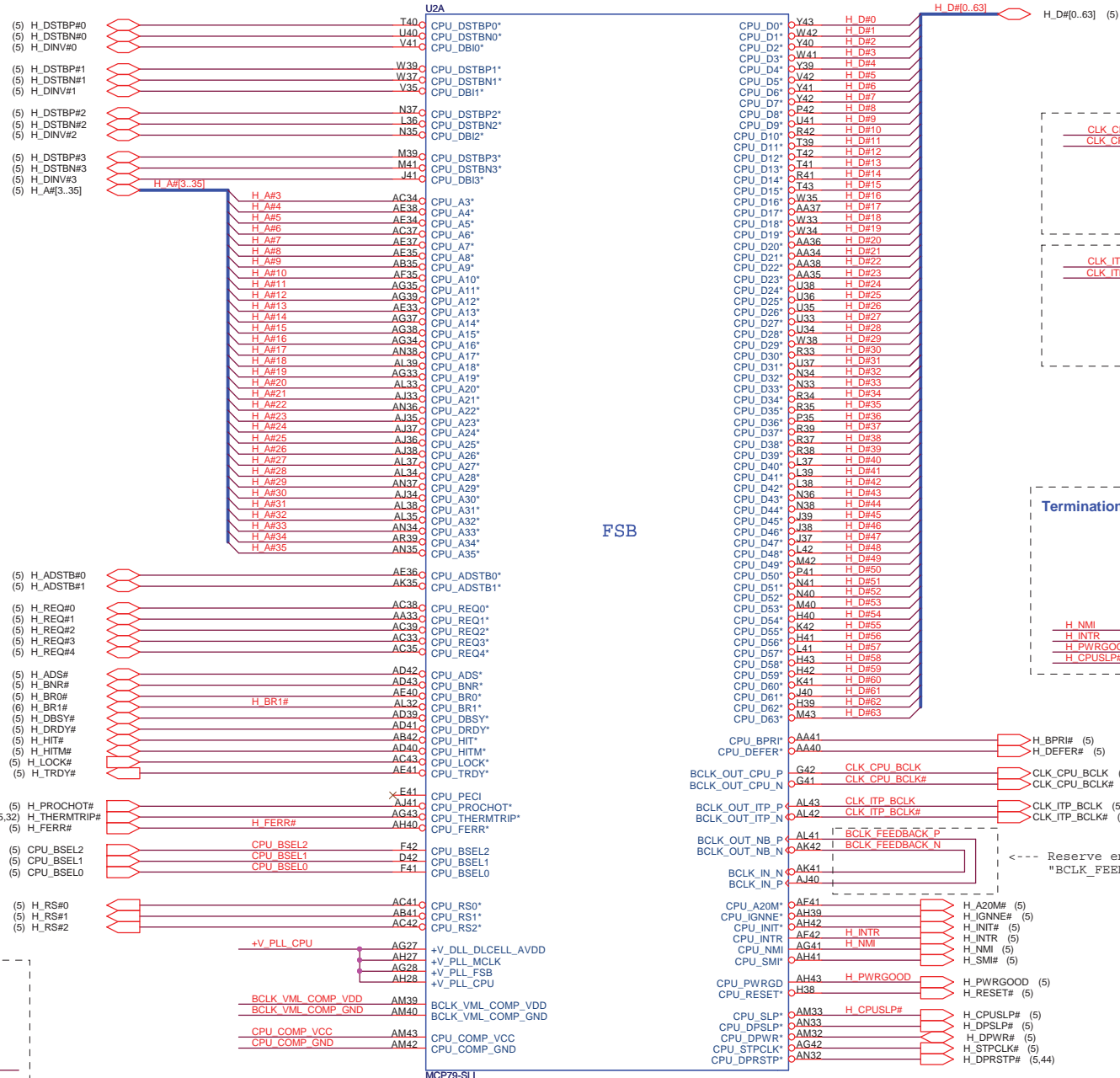


Vcc = 64A (Max)

**Vccp = 4.5A(max) Before stable
Vccp = 2.5A(max) After stable**

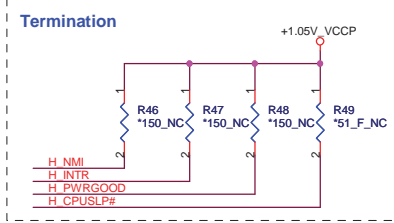
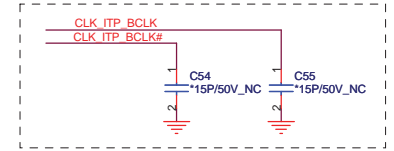
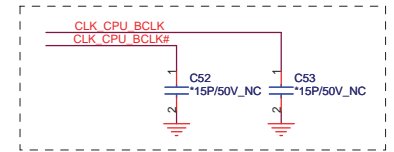


CPU Dual/ Quad Core Control Source		
	KBC	CPU
R21, R87, R689, R690, Q120, Q121, C798	Mounted	NC
R88	NC	Mounted

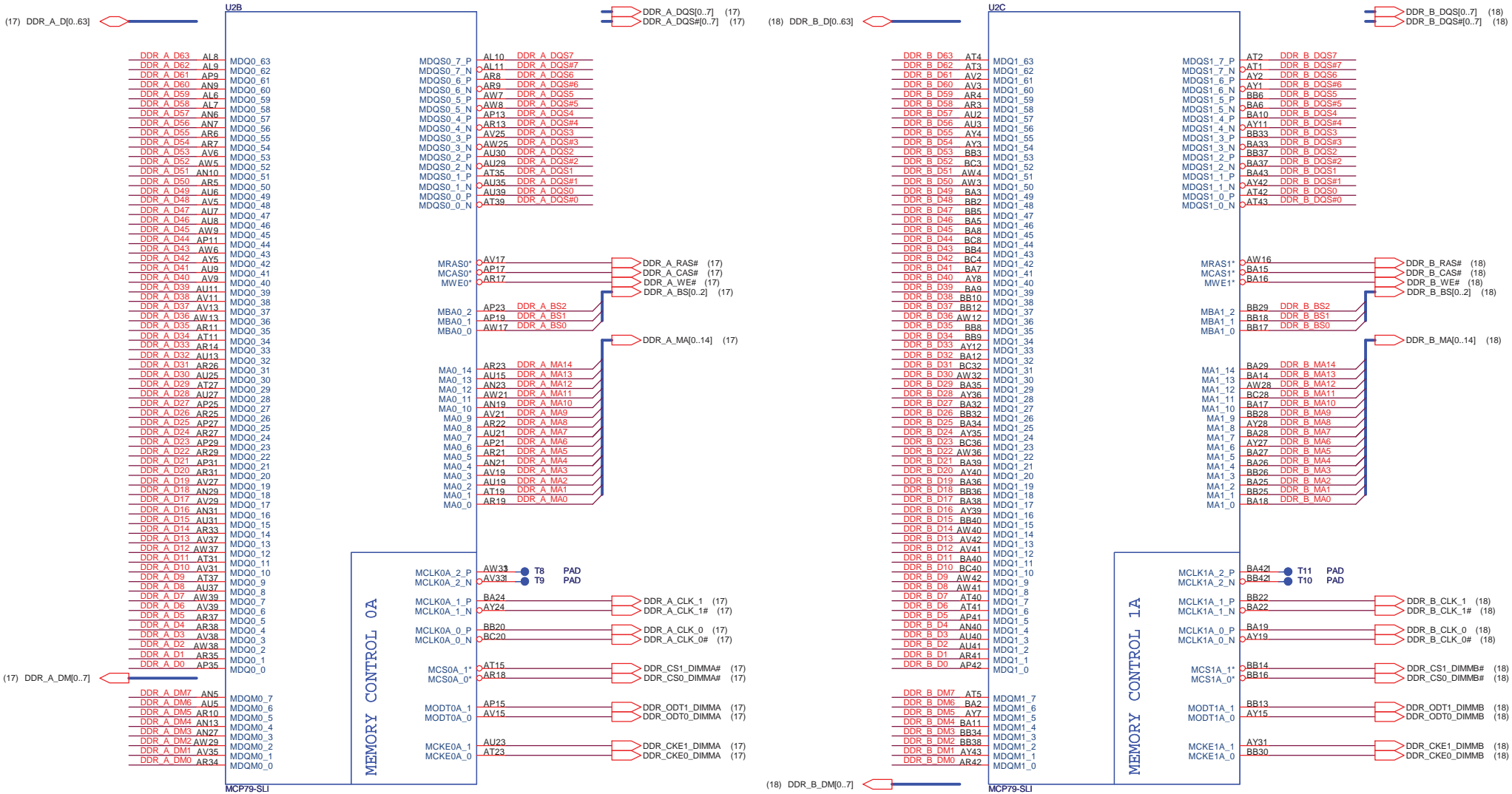


1. Route at normal impedance and 8 mils spacing to resistor.
 2. 49.9 ohm to GND or VTT_CPU less than 1 inch from MCP79.

+V_DLL_DLCELL_AVDD	+V_PLL_MCLK	+V_PLL_FSB	+V_PLL_CPU
150mA with RUN rail	20mA with RUN rail	29mA with RUN rail	15mA with RUN rail
1 x ferrite bead	1 x ferrite bead	1 x ferrite bead	1 x ferrite bead
1 x 4.7uF X5R ceramic	1 x 1uF X5R ceramic	1 x 4.7uF X5R ceramic	1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic	1 x 0.1uF X7R ceramic	1 x 0.1uF X7R ceramic	1 x 0.1uF X7R ceramic



<-- Reserve enough space "BCLK_FBBDACK_P/N" length routing.



Layout Notice:
Memory Data Signal Group
MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

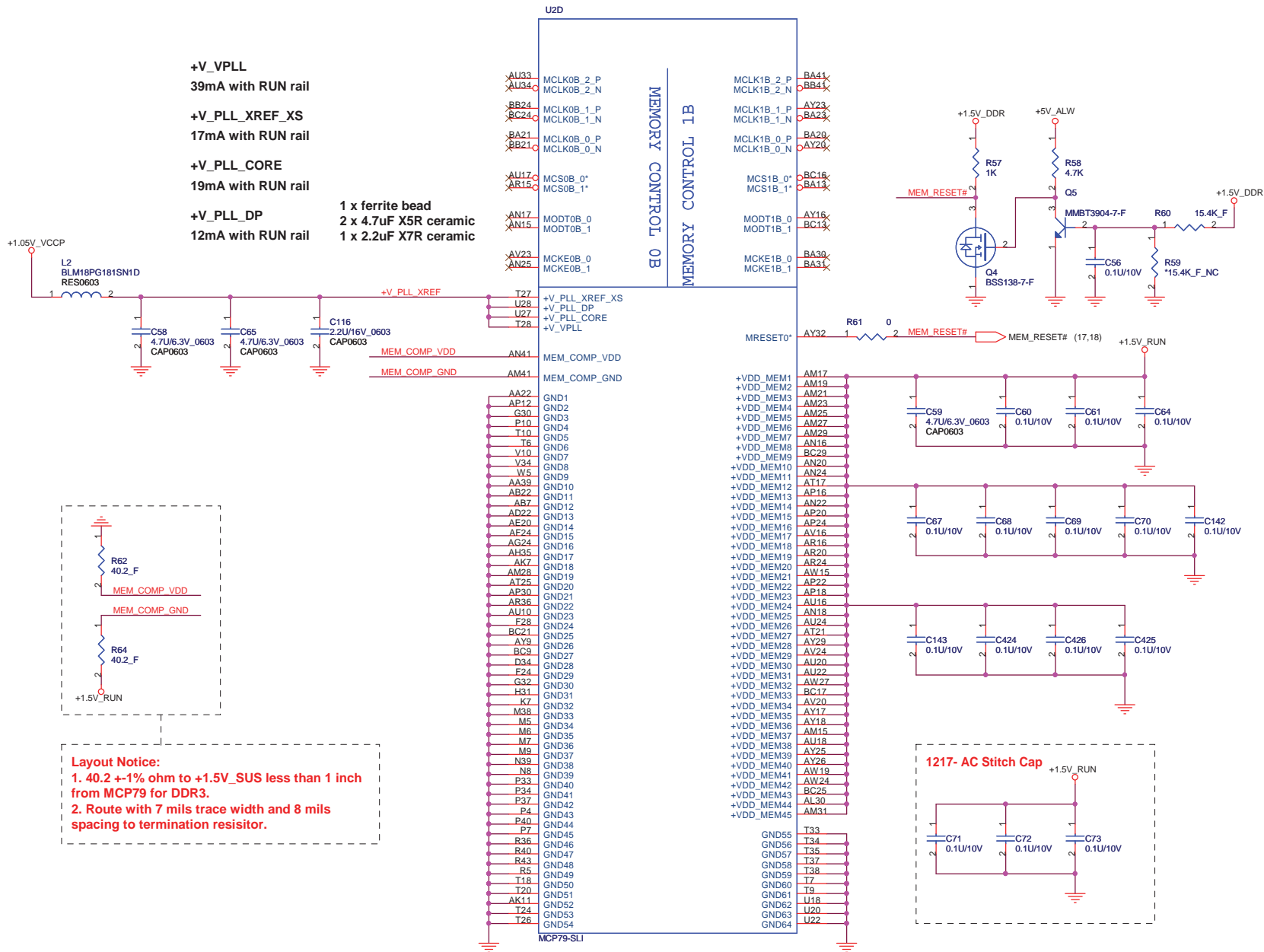
Memory Data Strobes
Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.
After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group
MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.
DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

<http://laptop-motherboard-schematic.blogspot.com/>

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- +V_VPLL**
39mA with RUN rail
- +V_PLL_XREF_XS**
17mA with RUN rail
- +V_PLL_CORE**
19mA with RUN rail
- +V_PLL_DP**
12mA with RUN rail

1 x ferrite bead
2 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic

4.3A with ALW rail for S0
318mA for S0 Idle
1 x 10uF ceramic
9 x 0.1uF X7R ceramic

Layout Notice:
1. 40.2 +/-1% ohm to +1.5V_SUS less than 1 inch from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils spacing to termination resistor.

1217- AC Stitch Cap

Title		
MCP79 C (MEM POWER)		
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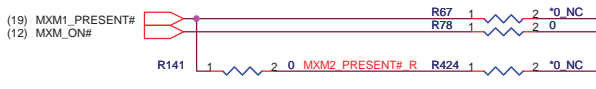
- (19) PCIE_MRX_GTX_P[0..7]
- (19) PCIE_MRX_GTX_N[0..7]
- (21) PCIE_MRX_GTX_P[8..15]
- (21) PCIE_MRX_GTX_N[8..15]

- PCIE_MTX_GRX_P[0..7] (19)
- PCIE_MTX_GRX_N[0..7] (19)
- PCIE_MTX_GRX_P[8..15] (21)
- PCIE_MTX_GRX_N[8..15] (21)

PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
 Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
 Route at 50 Signal end and 90 ohm differential.
 Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

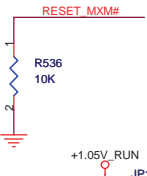
PCIE

- PCIE MRX GTX P0 E7
- PCIE MRX GTX N0 E7
- PCIE MRX GTX P1 D7
- PCIE MRX GTX N1 C7
- PCIE MRX GTX P2 E6
- PCIE MRX GTX N2 E6
- PCIE MRX GTX P3 E6
- PCIE MRX GTX N3 F5
- PCIE MRX GTX P4 E4
- PCIE MRX GTX N4 E3
- PCIE MRX GTX P5 D3
- PCIE MRX GTX N5 C3
- PCIE MRX GTX P6 G5
- PCIE MRX GTX N6 H5
- PCIE MRX GTX P7 J7
- PCIE MRX GTX N7 J6
- PCIE MRX GTX P8 J5
- PCIE MRX GTX N8 J5
- PCIE MRX GTX P9 L11
- PCIE MRX GTX N9 L10
- PCIE MRX GTX P10 L9
- PCIE MRX GTX N10 L8
- PCIE MRX GTX P11 L7
- PCIE MRX GTX N11 L6
- PCIE MRX GTX P12 N11
- PCIE MRX GTX N12 N10
- PCIE MRX GTX P13 N9
- PCIE MRX GTX N13 N9
- PCIE MRX GTX P14 N7
- PCIE MRX GTX N14 N6
- PCIE MRX GTX P15 N5
- PCIE MRX GTX N15 N4

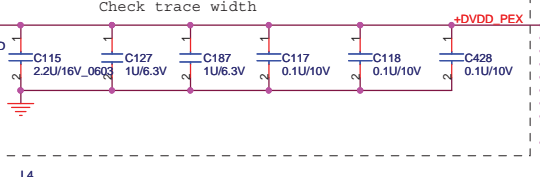


Express Card

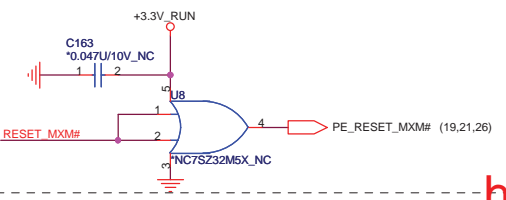
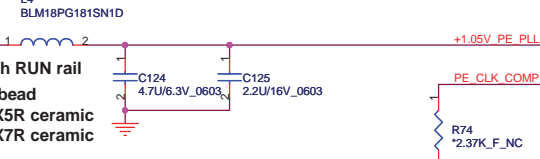
- (39) CARD_CLK_REQ#
- (33,39) EXPRGRD_PWREN#
- (30) MINI1CLK_REQ#
- (31) MINI2CLK_REQ#
- (31) MINI3CLK_REQ#
- (19,21,26) PE_RESET_MXM#
- (21,33) MXM2_PRESENT#
- (20,33) MXM1_PWR0K
- (20,33) MXM1_PWR0K
- (20,22,30,31,39) PCIE_WAKE#
- (39) PCIE_RX0_P
- (39) PCIE_RX0_N
- (30) PCIE_RX1_P
- (30) PCIE_RX1_N
- (31) PCIE_RX2_P
- (31) PCIE_RX2_N
- (31) PCIE_RX3_P
- (31) PCIE_RX3_N



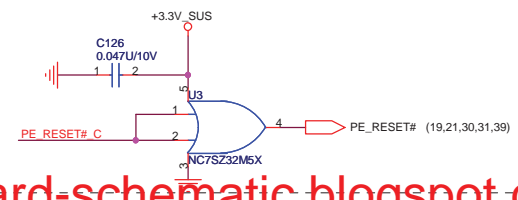
482mA with RUN rail
 1 x 2.2uF X5R ceramic
 2 x 1uF X5R ceramic
 2 x 0.1uF X7R ceramic



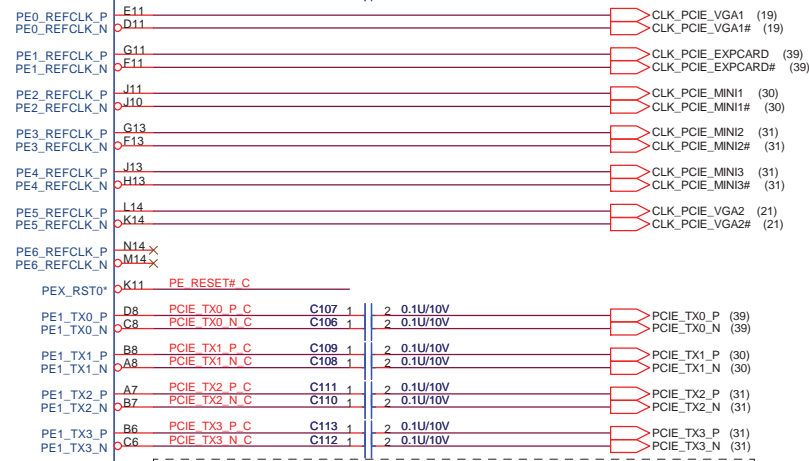
202mA with RUN rail
 1 x ferrite bead
 1 x 4.7uF X5R ceramic
 1 x 0.1uF X7R ceramic



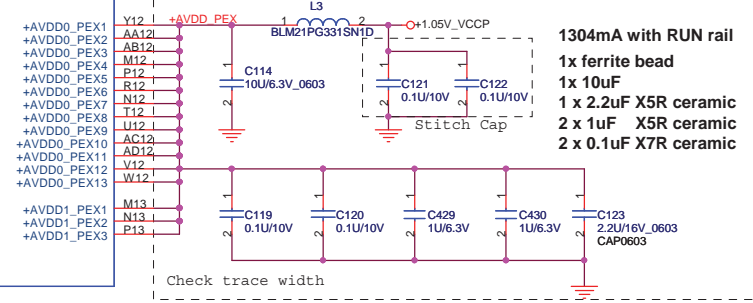
Layout Notice:
 1. 2.37K ohm to GND within 500 mil of MCP79
 2. Route an nominal impedance or wider trace and 8 mil spacing to resistor.



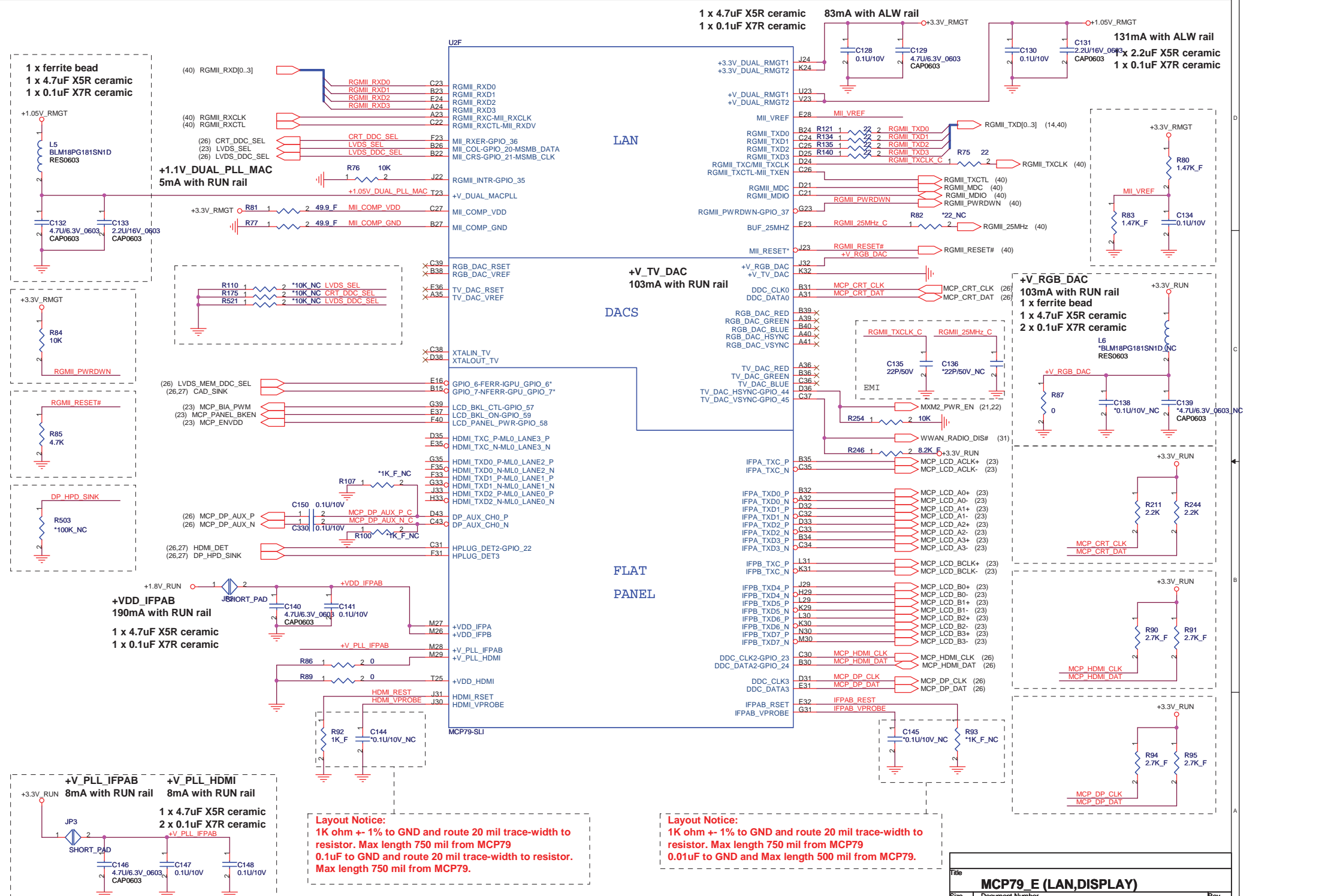
- PCIE MTX GRX C P0 C81
- PCIE MTX GRX C N0 C74
- PCIE MTX GRX C P1 C82
- PCIE MTX GRX C N1 C83
- PCIE MTX GRX C P2 C85
- PCIE MTX GRX C N2 C84
- PCIE MTX GRX C P3 C75
- PCIE MTX GRX C N3 C86
- PCIE MTX GRX C P4 C76
- PCIE MTX GRX C N4 C88
- PCIE MTX GRX C P5 C87
- PCIE MTX GRX C N5 C89
- PCIE MTX GRX C P6 C91
- PCIE MTX GRX C N6 C90
- PCIE MTX GRX C P7 C93
- PCIE MTX GRX C N7 C92
- PCIE MTX GRX C P8 C77
- PCIE MTX GRX C N8 C94
- PCIE MTX GRX C P9 C96
- PCIE MTX GRX C N9 C95
- PCIE MTX GRX C P10 C97
- PCIE MTX GRX C N10 C99
- PCIE MTX GRX C P11 C98
- PCIE MTX GRX C N11 C101
- PCIE MTX GRX C P12 C100
- PCIE MTX GRX C N12 C78
- PCIE MTX GRX C P13 C102
- PCIE MTX GRX C N13 C79
- PCIE MTX GRX C P14 C103
- PCIE MTX GRX C N14 C104
- PCIE MTX GRX C P15 C80
- PCIE MTX GRX C N15 C105



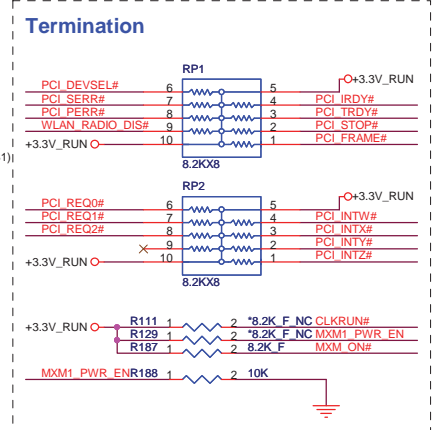
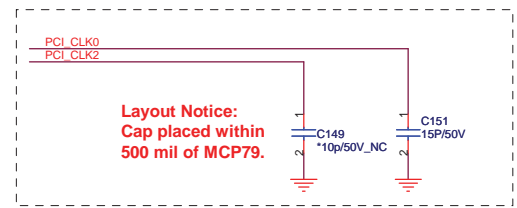
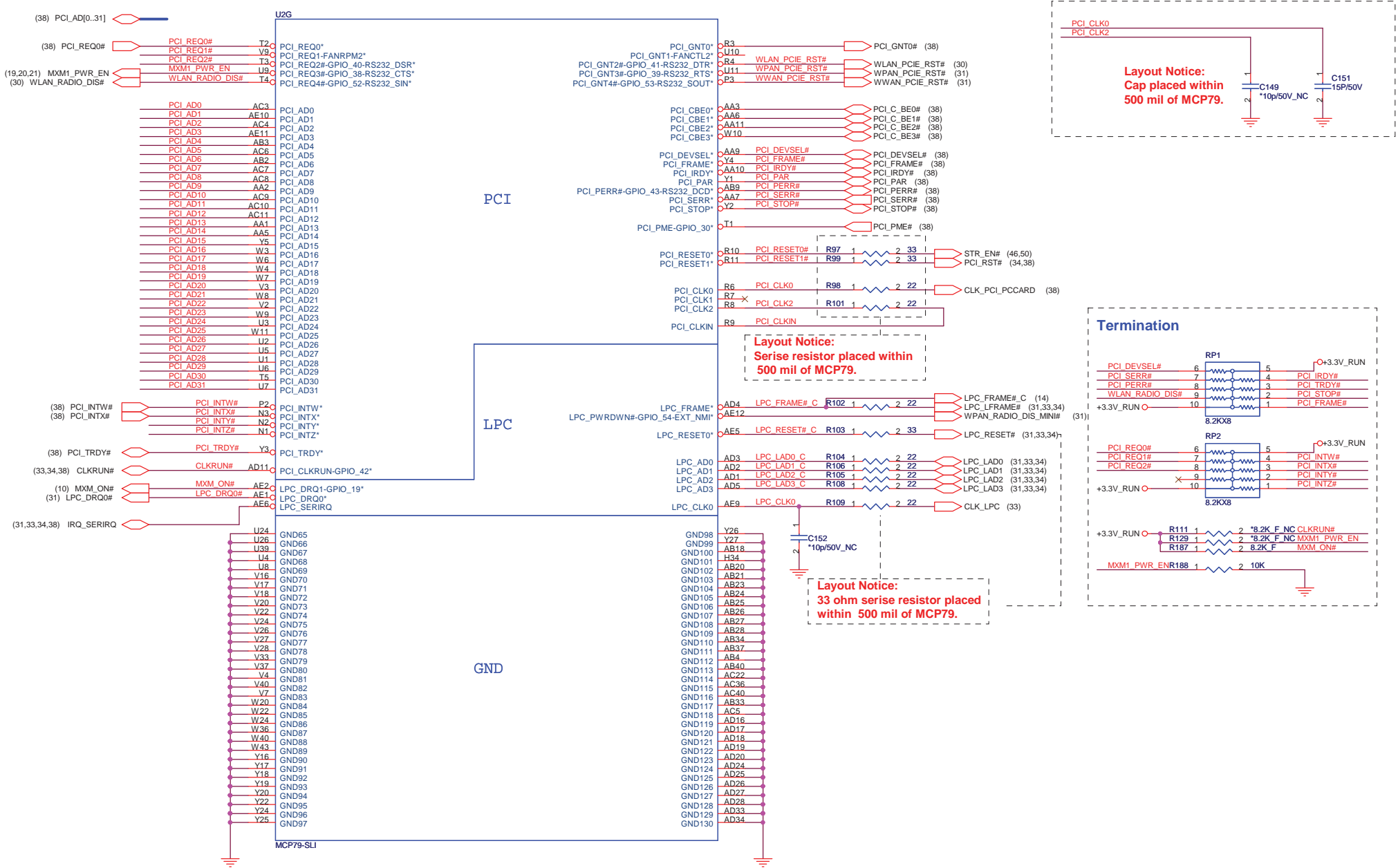
1304mA with RUN rail
 1x ferrite bead
 1x 10uF
 1 x 2.2uF X5R ceramic
 2 x 1uF X5R ceramic
 2 x 0.1uF X7R ceramic



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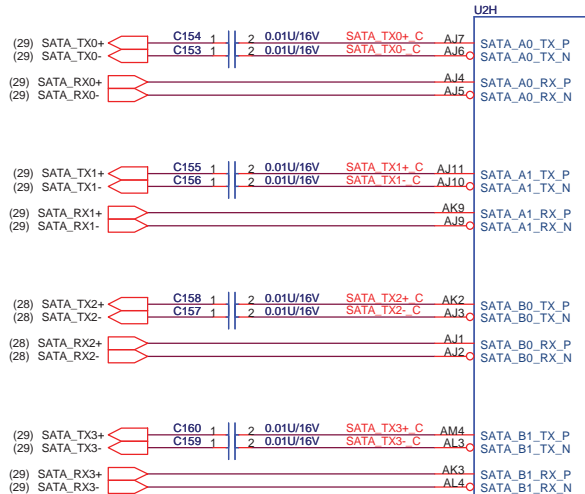


Title			
MCP79 E (LAN, DISPLAY)			
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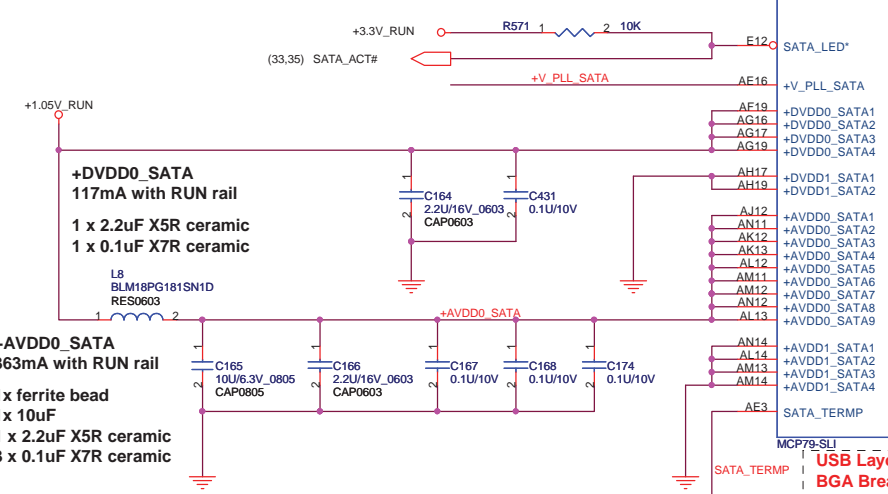


T41	1	PCI_REQ2#
T42	1	MXM1_PWR_EN
T43	1	WLAN_RADIO_DIS#
T44	1	WLAN_PCIE_RST#
T45	1	WPAN_PCIE_RST#
T54	1	WWAN_PCIE_RST#

Title		
MCP79_F (PCI,LPC)		
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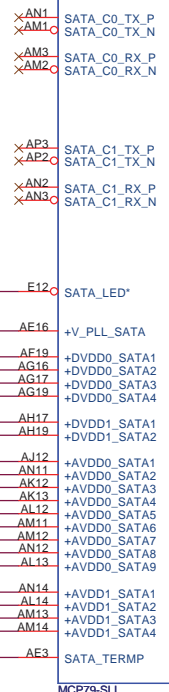


SATA Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum bracketout distance is 400 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA bracketout plus Fan-out distance is 500 mils.
After Bracketout:
 Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
 TX and RX intra-pair skew for a differential pair is 5 mils.

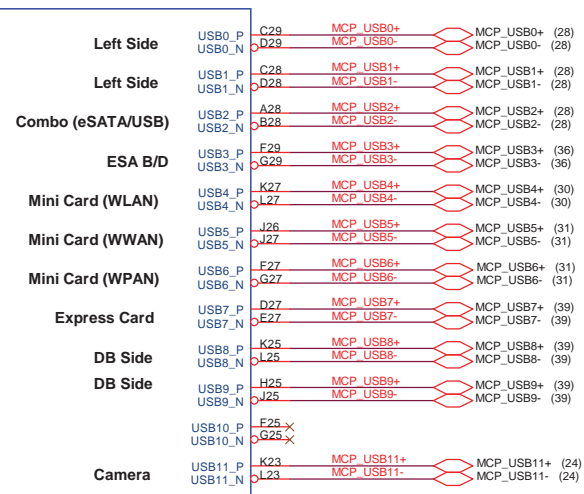


Layout Notice:
 2.49K ohm to GND within 500 mils of MCP79.
 Routing 8 mils spacing to resistor.

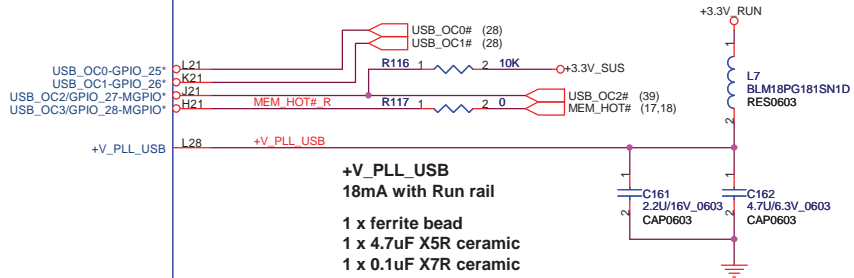
SATA



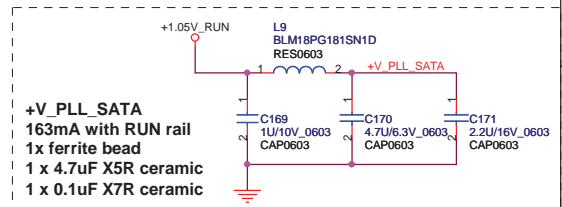
USB Layout Notice:
BGA Breakout:
 Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum bracketout distance is 300 mils of MCP79.
BGA Fan-out:
 Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA bracketout plus Fan-out distance is 400 mils.
After Bracketout:
 Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
 Each USB pair must be length matched to within 50 mil.



USB

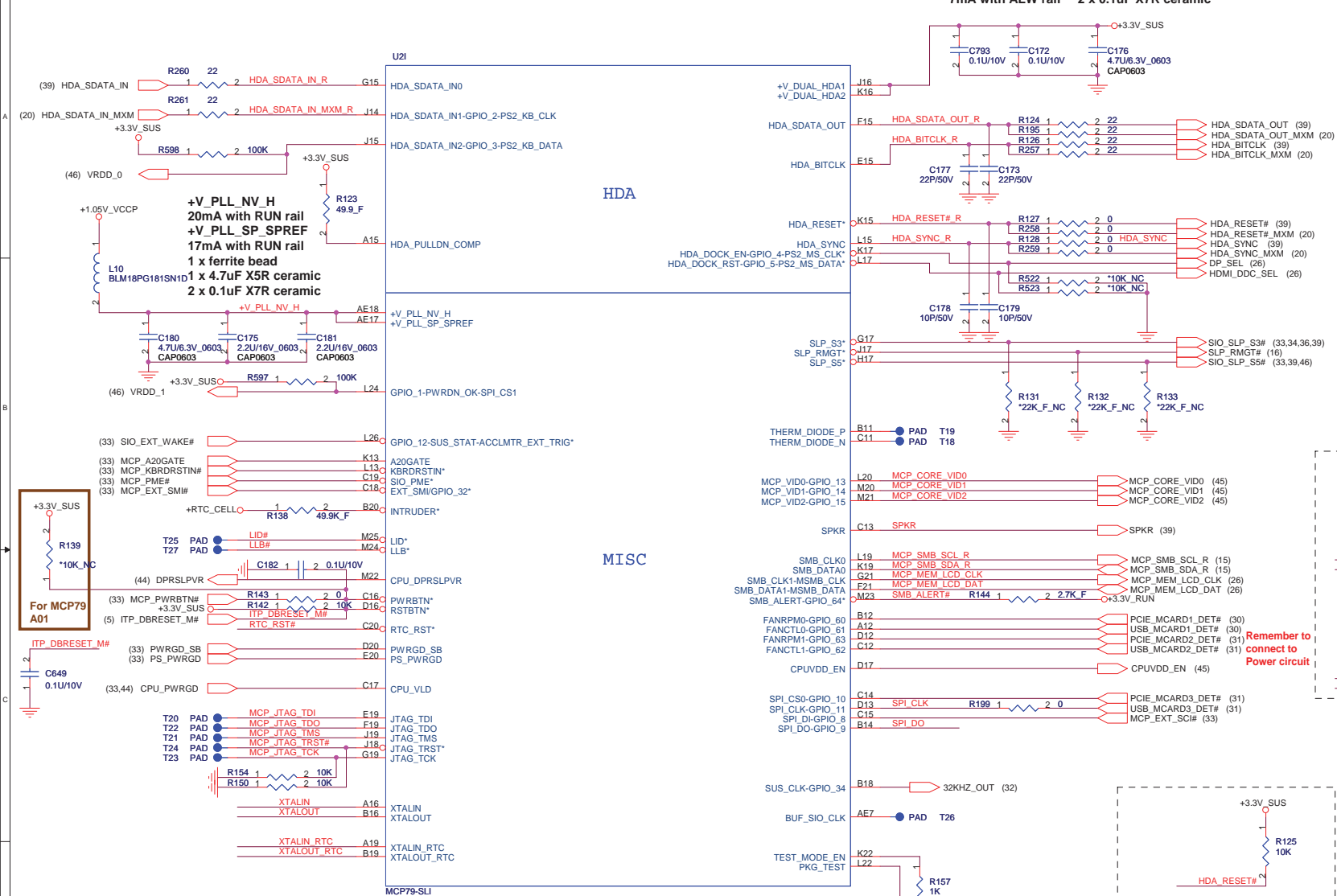


Layout Notice:
 806 ohm +/-1% to GND within 1000 mil of MCP79.
 Routing trace at least 8 mil wide to resistor.



Title			
MCP79 G (SATA,USB)			
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+V_DUAL_HDA 7mA with ALW rail **1 x 4.7uF X5R ceramic**
2 x 0.1uF X7R ceramic



MCP79 Strapping

Boot BIOS Strapping		
	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS(CS0)	1	0
SPI BIOS(CS1)	1	1

MCP79 Strapping

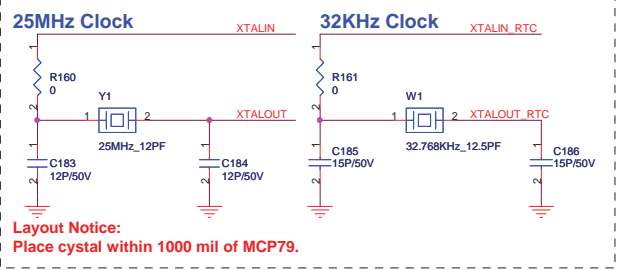
SIO Clock Select	
	HDA_SYNC
14.318MHz	0
24MHz	1

MCP79 Strapping

SPI CLK Frequency Select		
	SPI_DO	SPI_CLK
31MHz	0	0
41MHz	0	1
25MHz	1	0
1MHz	1	1

CLEAR CMOS ONLY

CLEAR	RTC_RST#
CLEAR	0
NORMAL	1



MCP79 Strapping

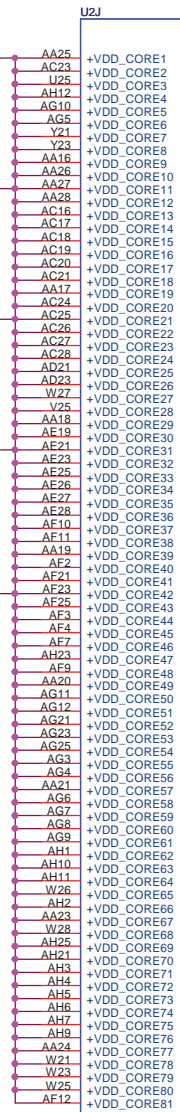
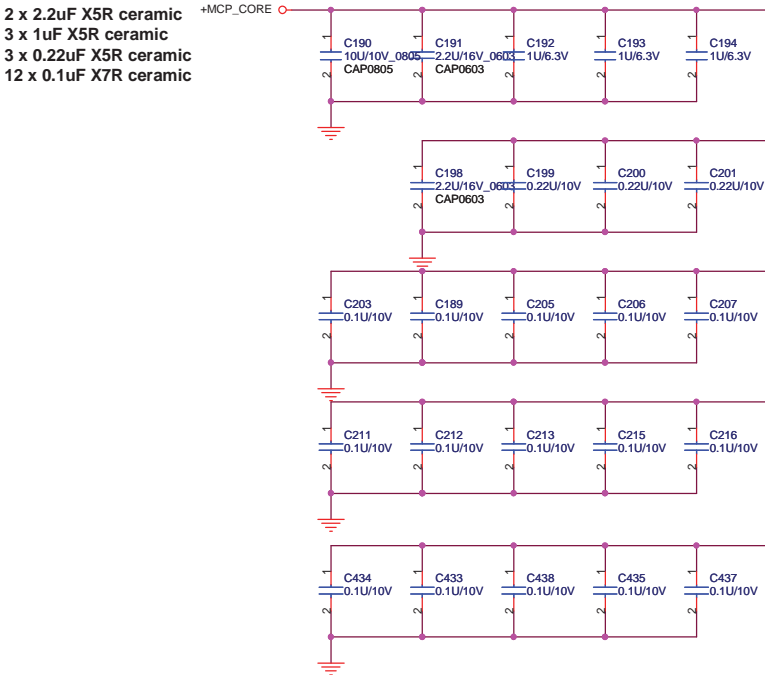
Boot Mode Select	
User Mode	Safe Mode
0	1

MCP79 Strapping

Networking Select	
MII	RGMI
0	1

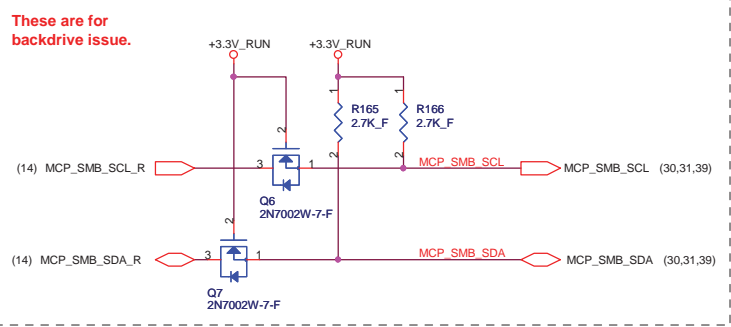
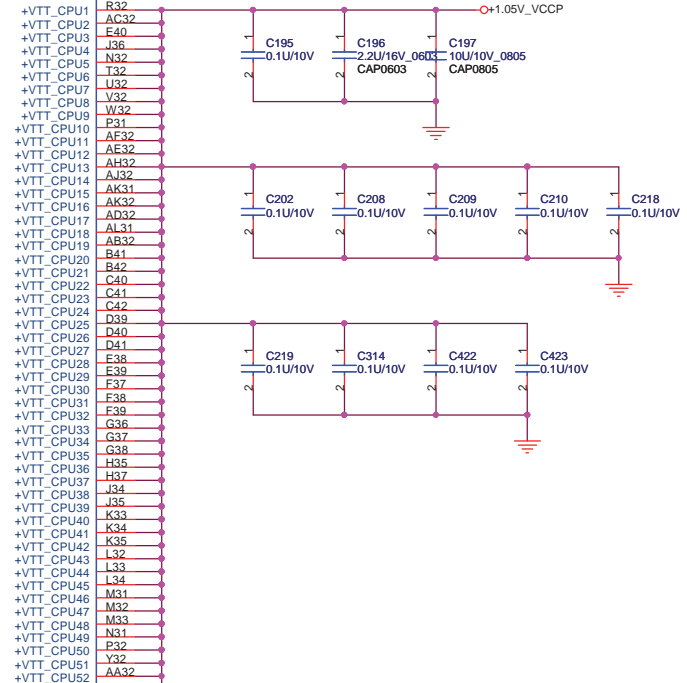
17.756A with RUN rail for S0
2850mA for S0 Idle

- 1 x 10uF ceramic
- 2 x 2.2uF X5R ceramic
- 3 x 1uF X5R ceramic
- 3 x 0.22uF X5R ceramic
- 12 x 0.1uF X7R ceramic



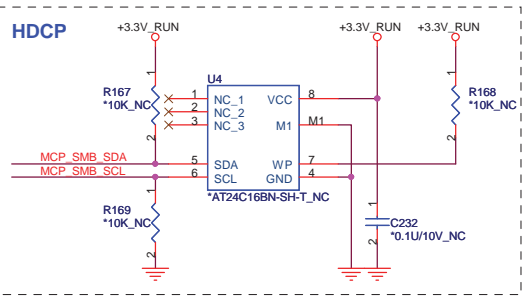
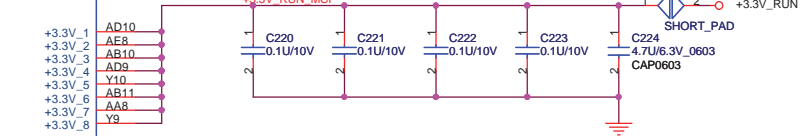
+VTT_CPU 1139mA for ALW rail
+VTT_CPUCLK 43mA for ALW rail

- 1 x 10uF ceramic
- 1 x 2.2uF X5R ceramic
- 3 x 0.1uF X7R ceramic

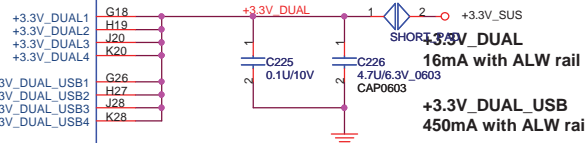


+3.3V_RUN_MCP 450mA with RUN rail

- 1 x 4.7uF X5R ceramic
- 4 x 0.1uF X7R ceramic

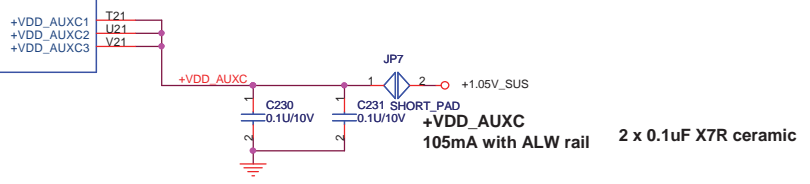


0.06mA with ALW rail for S0
2 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic



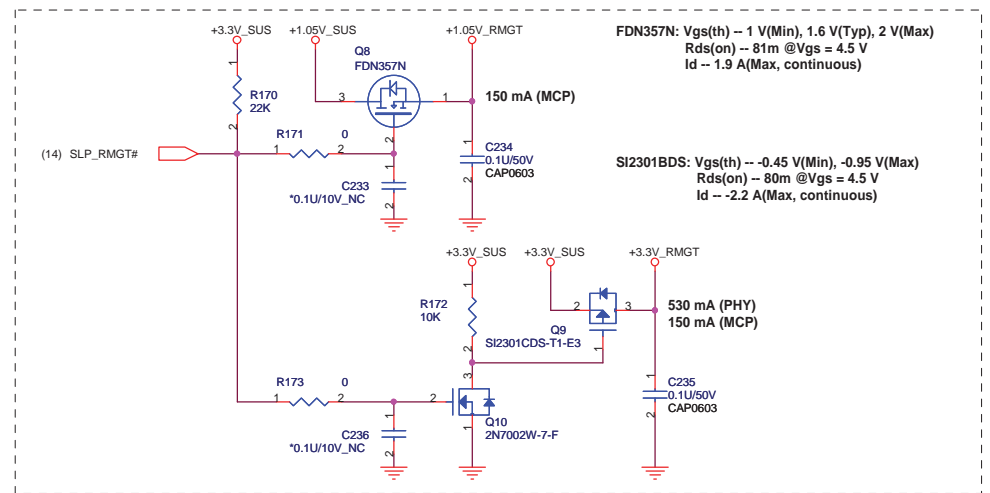
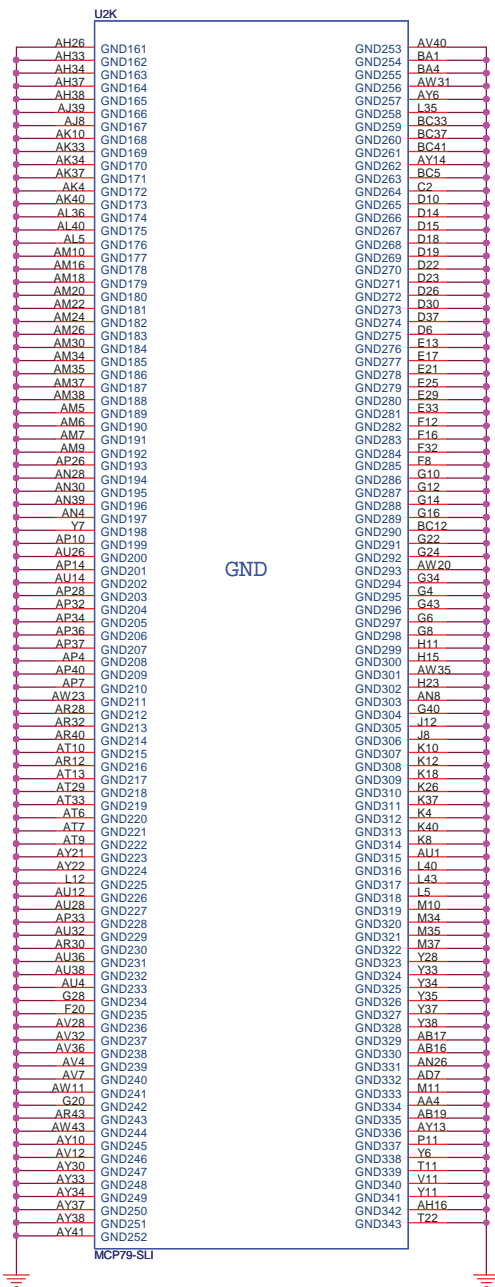
+3.3V_DUAL 16mA with ALW rail
+3.3V_DUAL_USB 450mA with ALW rail

- 1 x 4.7uF X5R ceramic
- 1 x 0.1uF X7R ceramic



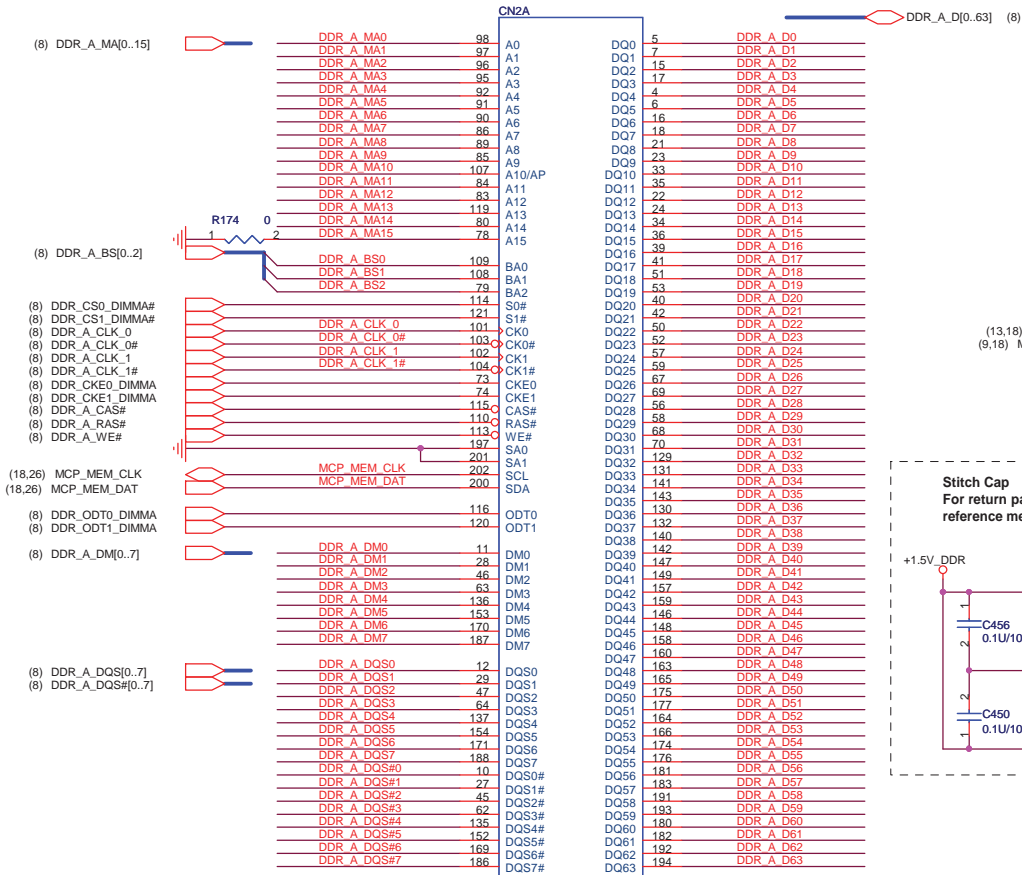
+VDD_AUXC 105mA with ALW rail
2 x 0.1uF X7R ceramic

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MCP79_1 (POWER)			
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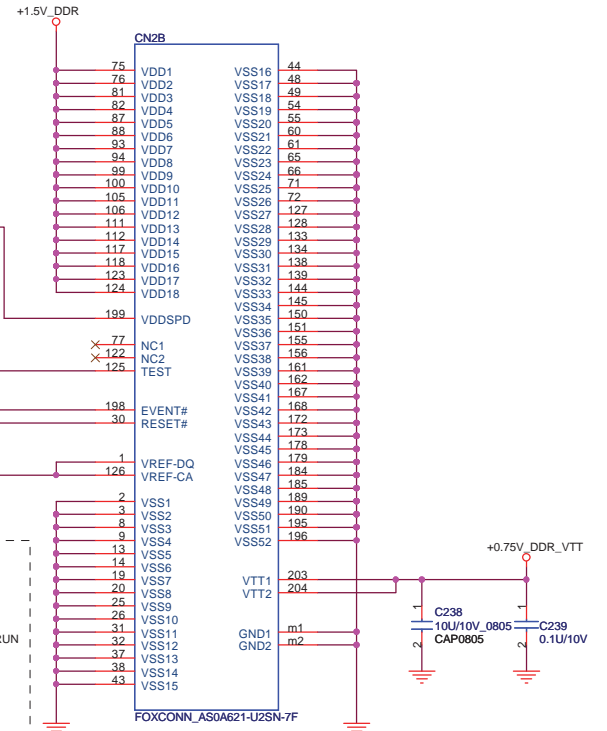
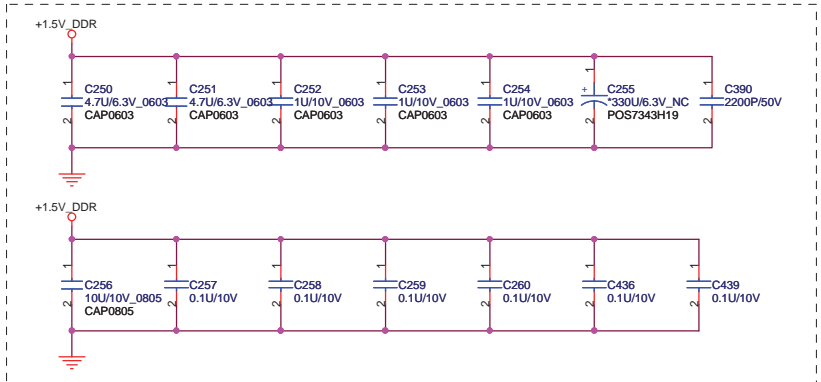
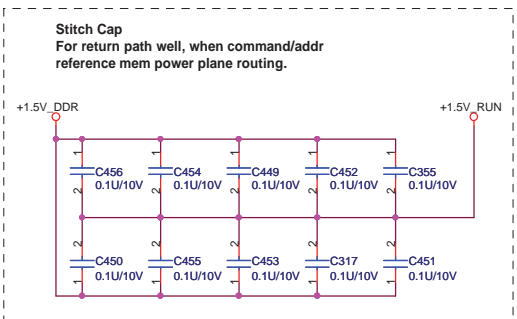
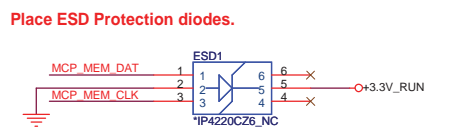
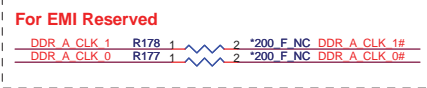
<http://laptop-motherboard-schematic.blogspot.com/>

Title		
MCP79_J (GND)		
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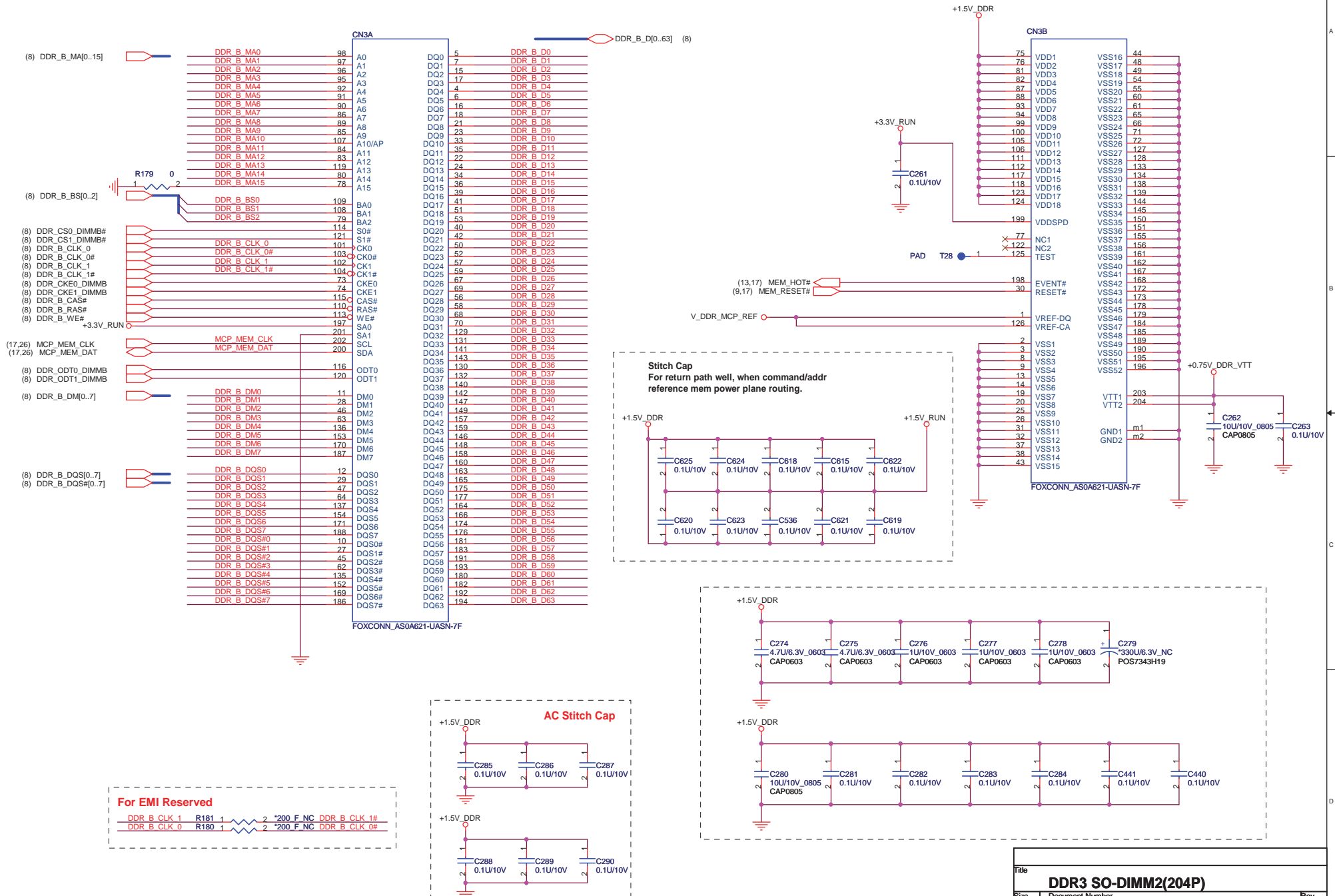


3/21 Neo: Update symbol.

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

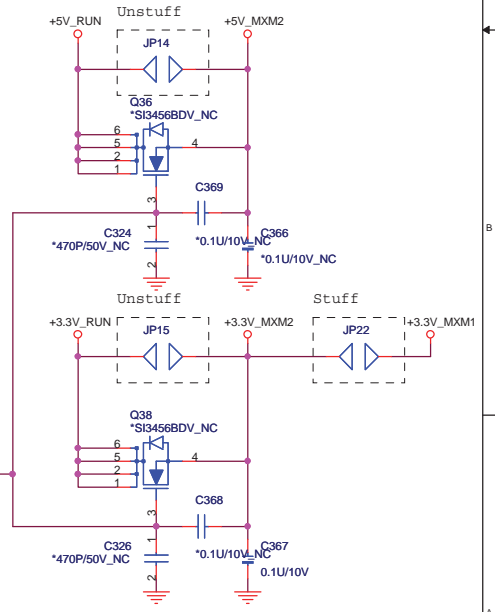
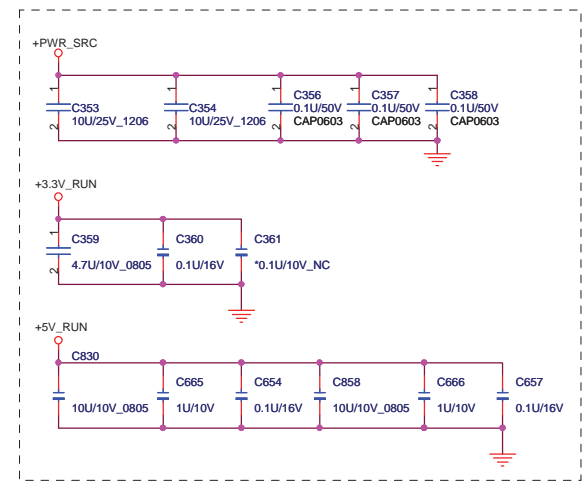
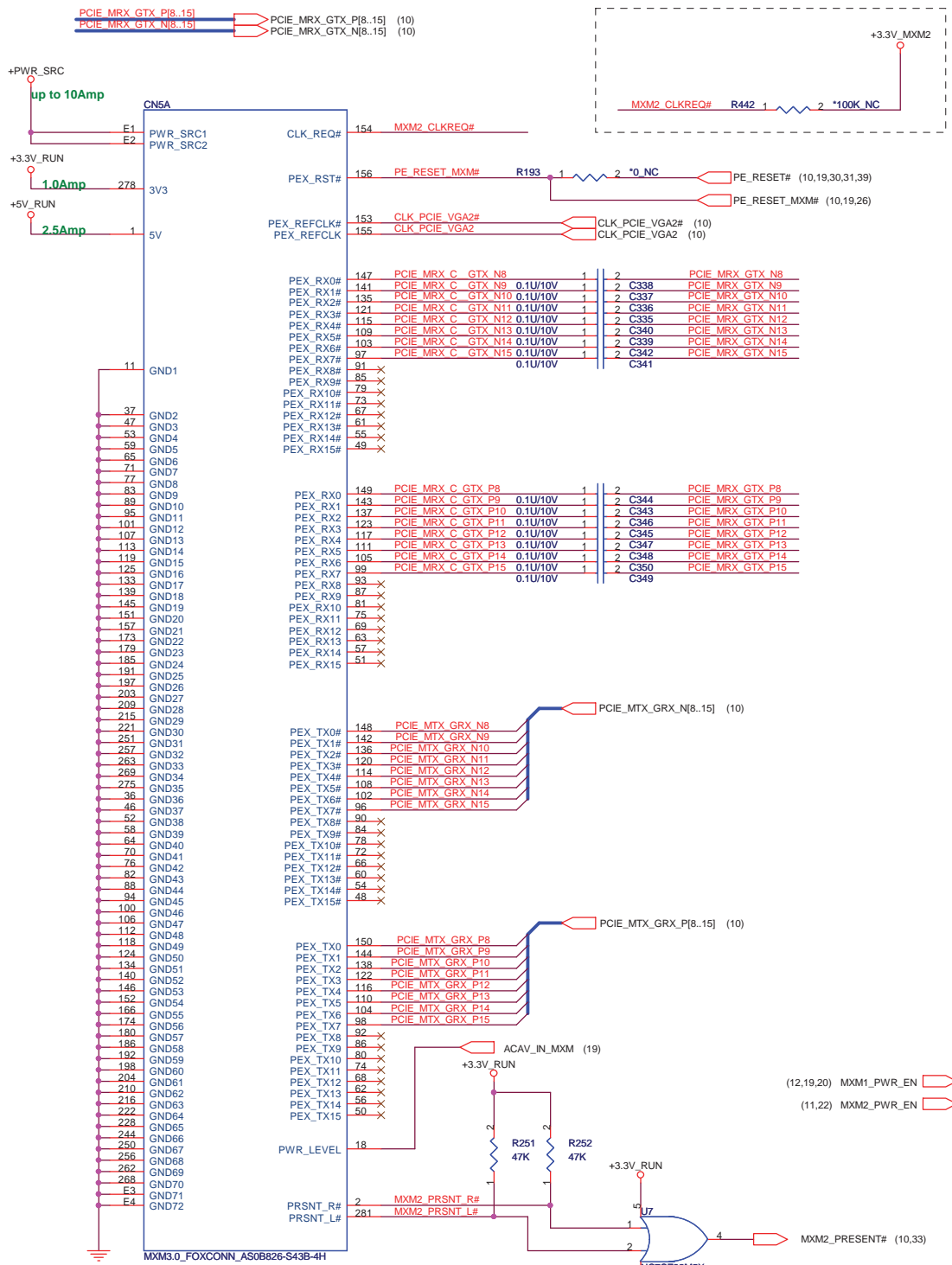


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Title		
DDR3 SO-DIMM2(204P)		
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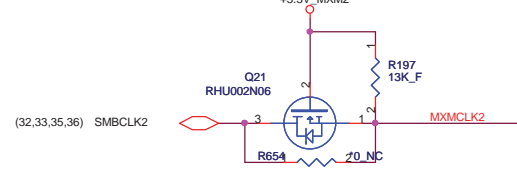
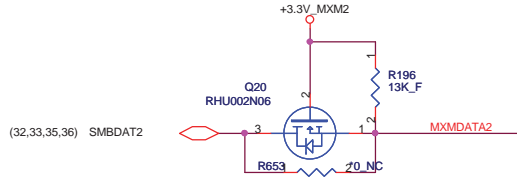
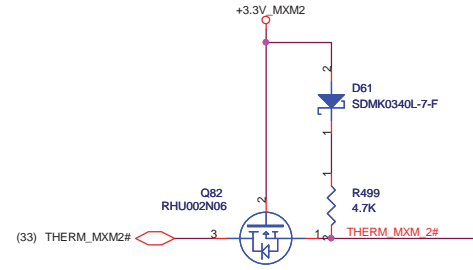
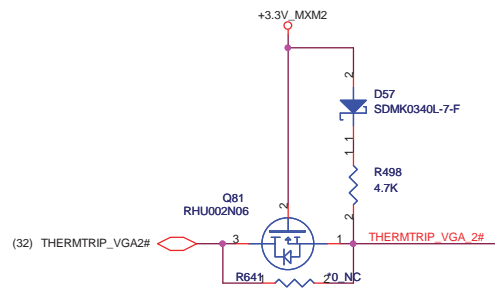




MXM Conn

<http://laptop-motherboard-schematic.blogspot.com/>

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CN5B	
X169	LVDS_UCLK#
X171	LVDS_UCLK
X193	LVDS_UTX0#
X187	LVDS_UTX1#
X181	LVDS_UTX2#
X175	LVDS_UTX3#
X195	LVDS_UTX0
X189	LVDS_UTX1
X183	LVDS_UTX2
X177	LVDS_UTX3
X176	LVDS_LCLK#
X178	LVDS_LCLK
X200	LVDS_LTX0#
X194	LVDS_LTX1#
X188	LVDS_LTX2#
X182	LVDS_LTX3#
X202	LVDS_LTX0
X196	LVDS_LTX1
X190	LVDS_LTX2
X184	LVDS_LTX3
X23	PNL_PWR_EN
X25	PNL_BL_EN
X27	PNL_BL_PWM
X33	LVDS_DDC_DAT
X35	LVDS_DDC_CLK
X164	VGA_HSYNC
X162	VGA_VSYNC
X168	VGA_RED
X170	VGA_GREEN
X172	VGA_BLUE
X158	VGA_DDC_DAT
X160	VGA_DDC_CLK
X45	OEM1
X44	OEM2
X43	OEM3
X42	OEM4
X41	OEM5
X40	OEM6
X39	OEM7
X38	OEM8
20	TH_OVERT#
22	TH_ALERT#
X24	TH_PWM
X26	GPIO0
X28	GPIO1
X30	GPIO2
32	SMB_DAT
34	SMB_CLK
X10	RSVD1
X12	RSVD2
X14	RSVD3
X16	RSVD4
X159	RSVD5
X161	RSVD6
X163	RSVD7
X165	RSVD8
X167	RSVD9
X227	RSVD10
X229	RSVD11
X231	RSVD12
X233	RSVD13
X235	RSVD14
X237	RSVD15
X238	RSVD16
X239	RSVD17
X240	RSVD18
M1	
M2	
H1	
H2	

DP-A

SC/VI

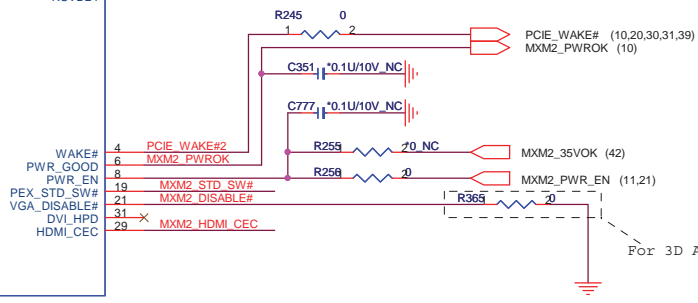
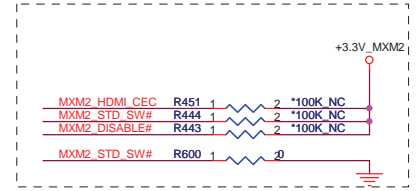
DP-B

IRP-C

DP-D/OEMO

THERMTRIP_VGA_2# 20
THERM_MXM2_# 22
MXM2DATA2 32
MXMCLK2 34

277	DP_A_AUX#
279	DP_A_AUX
253	DP_A_L0#
259	DP_A_L1#
265	DP_A_L2#
271	DP_A_L3#
255	DP_A_L0
261	DP_A_L1
267	DP_A_L2
273	DP_A_L3
276	DP_A_HPD
270	DP_B_AUX#
272	DP_B_AUX
246	DP_B_L0#
252	DP_B_L1#
258	DP_B_L2#
264	DP_B_L3#
248	DP_B_L0
254	DP_B_L1
260	DP_B_L2
266	DP_B_L3
274	DP_B_HPD
223	DP_C_AUX#
225	DP_C_AUX
199	DP_C_L0#
205	DP_C_L1#
211	DP_C_L2#
217	DP_C_L3#
201	DP_C_L0
207	DP_C_L1
213	DP_C_L2
219	DP_C_L3
234	DP_C_HPD
230	DP_D_AUX#
232	DP_D_AUX
206	DP_D_L0#
212	DP_D_L1#
218	DP_D_L2#
224	DP_D_L3#
208	DP_D_L0
214	DP_D_L1
220	DP_D_L2
226	DP_D_L3
236	DP_D_HPD
241	RSVD19
242	RSVD20
243	RSVD21
245	RSVD22
247	RSVD23
249	RSVD24
4	WAKE#
6	PWR_GOOD
8	PWR_EN
19	PEX_STD_SW#
21	VGA_DISABLE#
31	DVI_HPD
29	HDMI_CEC

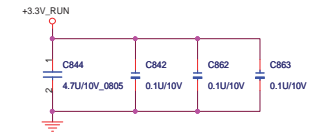
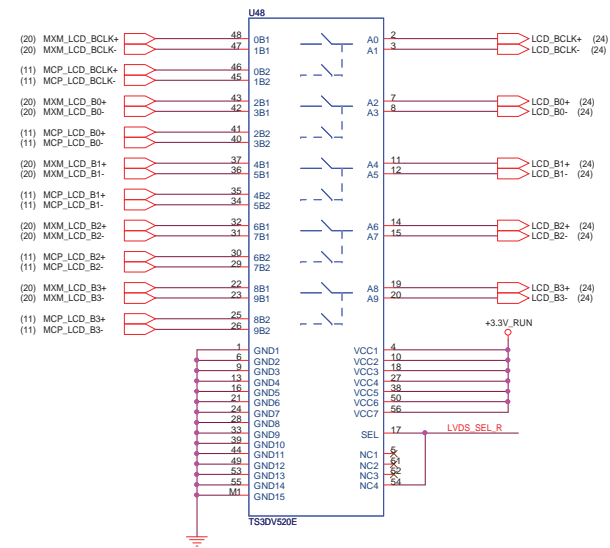
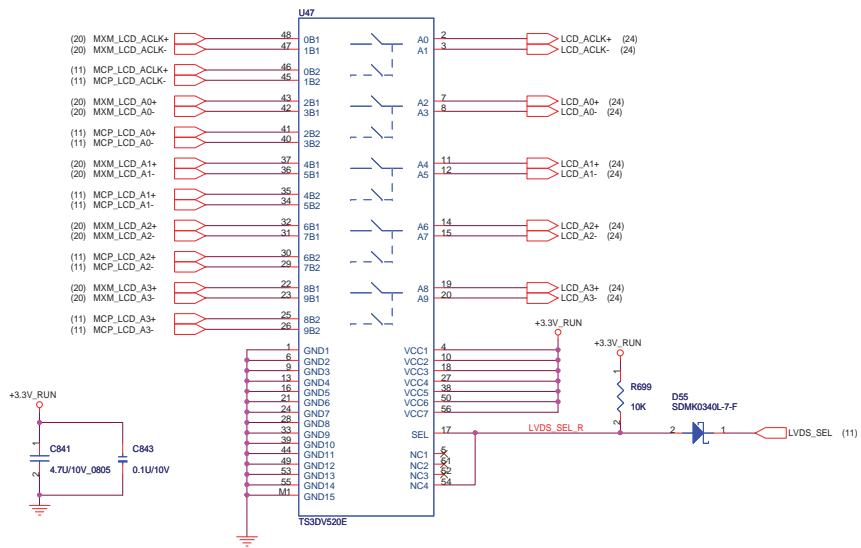


For 3D Accelerator Function.

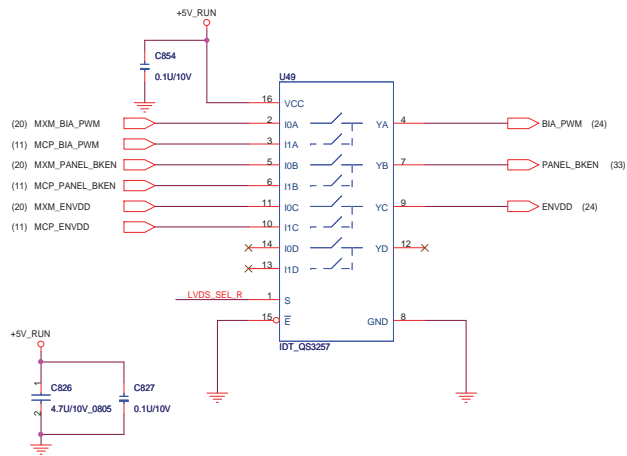
MXM Conn

MXM3.0_FOXCONN_AS0B826-S43B-4H

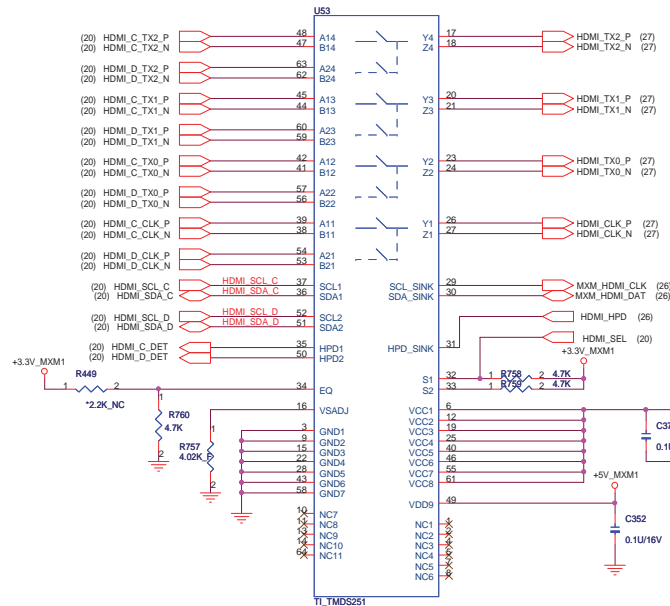
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MCP_LVDS_SEL	LVDS_SOURCE
L	MXM
H	MCP

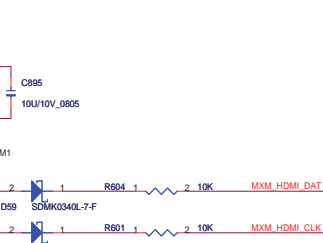
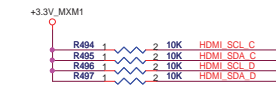


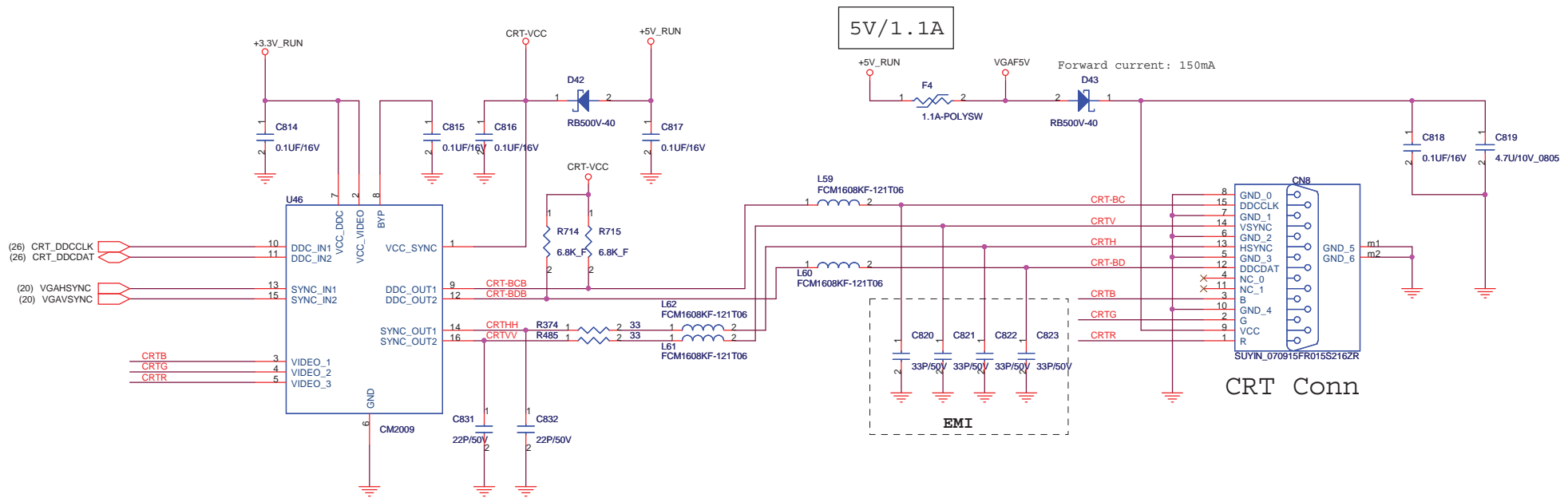
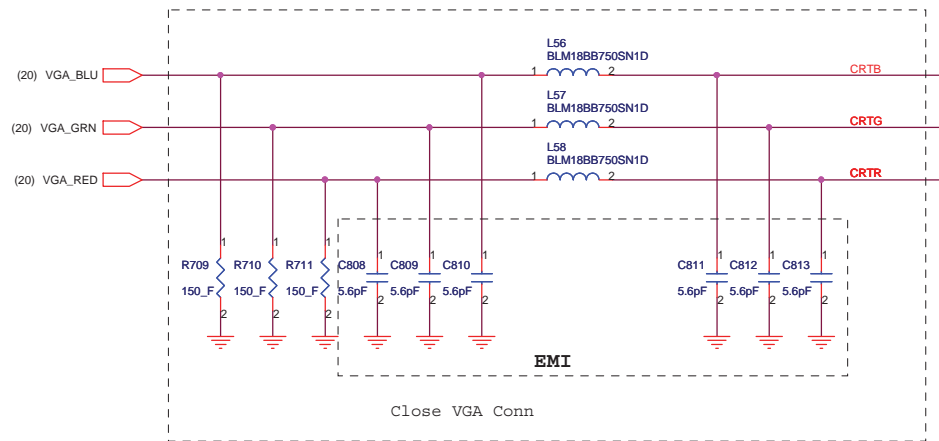
HDMI PORT C&D MUX



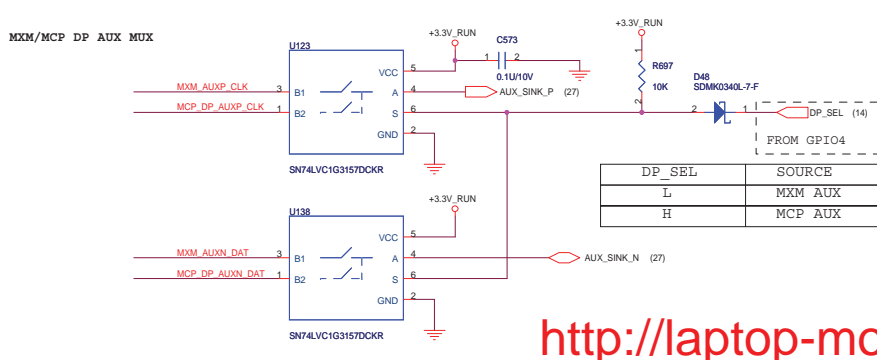
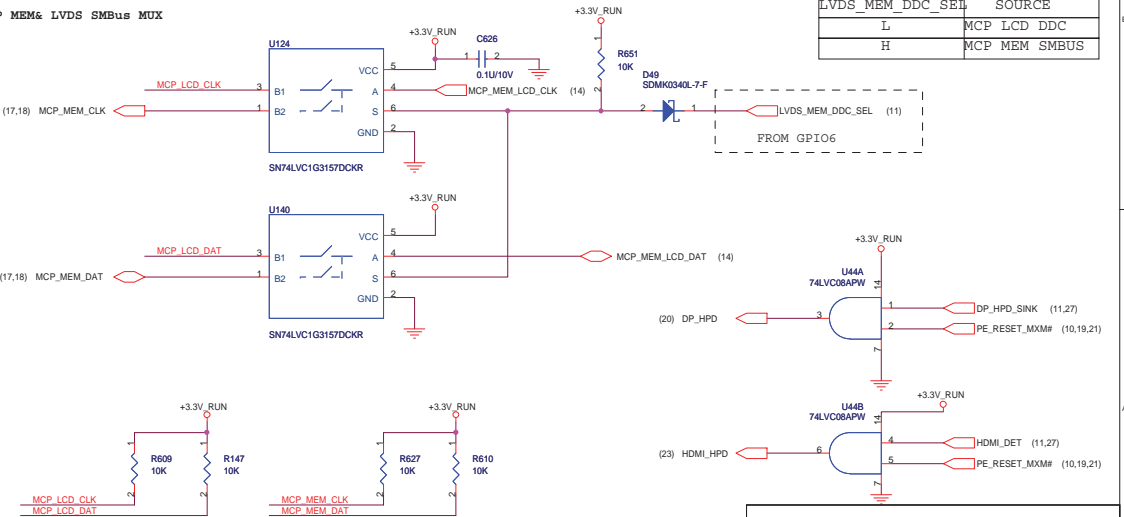
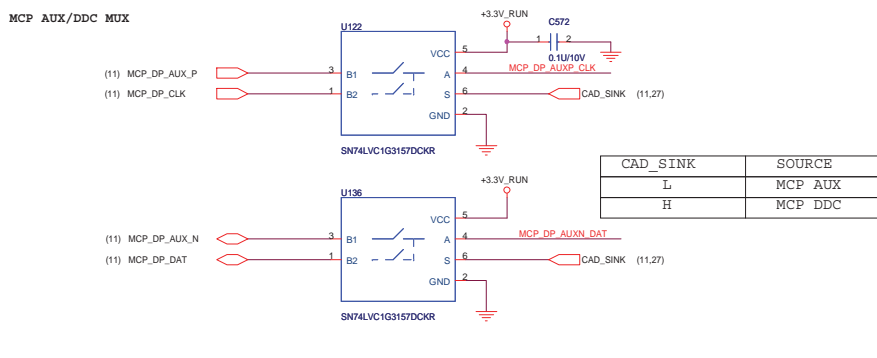
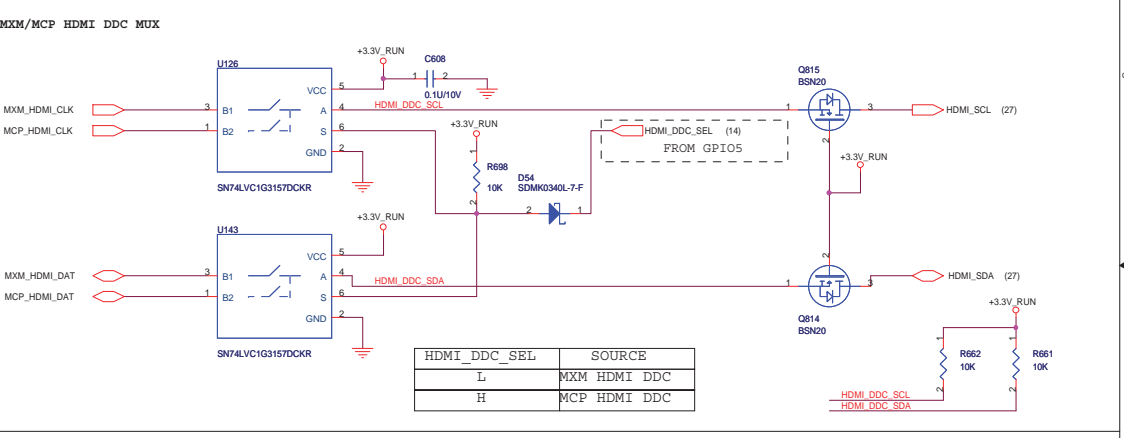
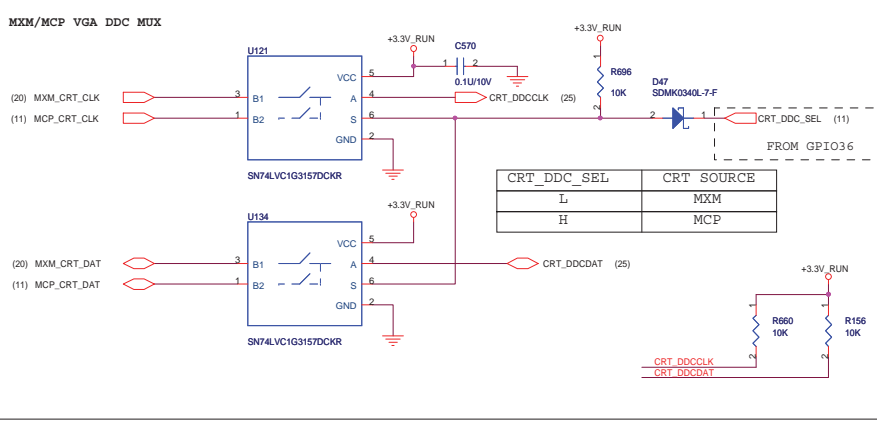
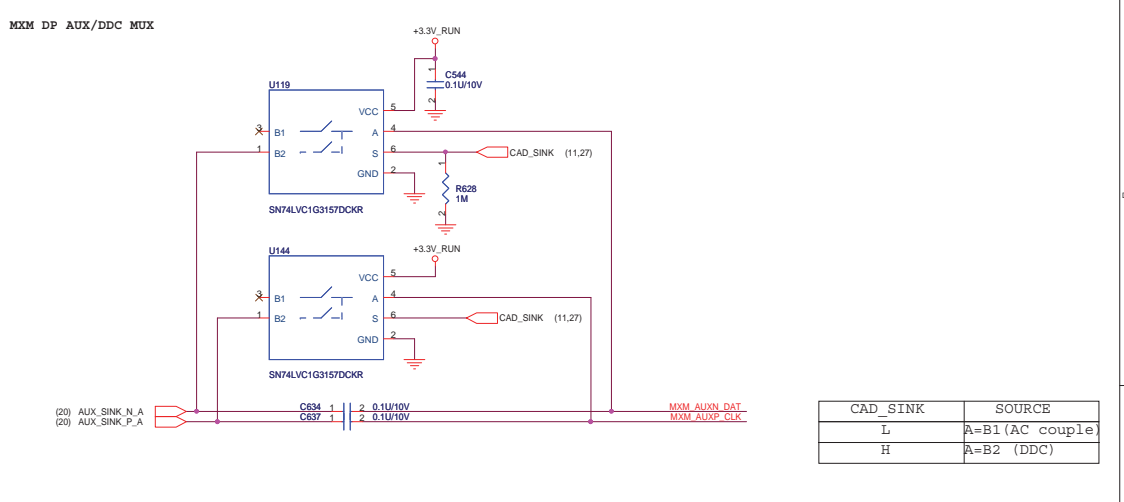
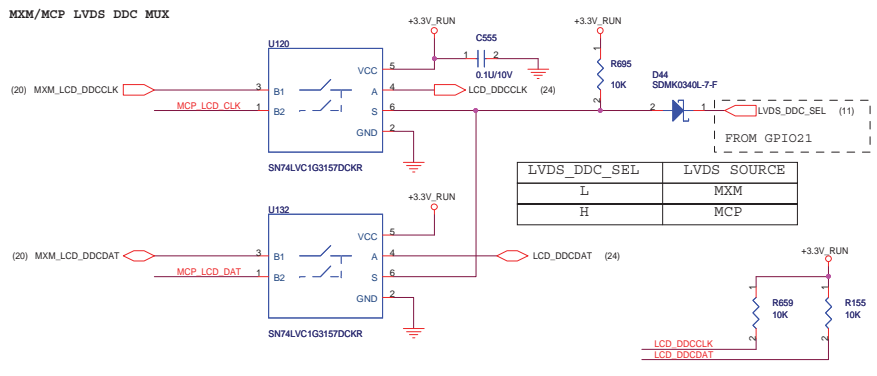
Close CN9

CONTROL BITS	I/O SELECTED	HOT PLUG DETECT STATUS
S2	S1 (OEM)	Y/Z SCL_SINK SDA_SINK
H	H	SCL1 A1/B1 SDA1 HPD_SINK L <small>For NB-980T</small>
H	L	A2/B2 SCL2 SDA2 L HPD_SINK <small>For NB-980TX</small>

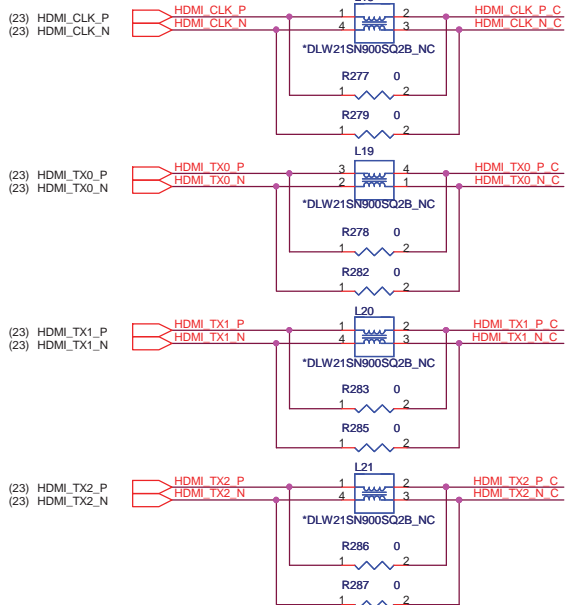




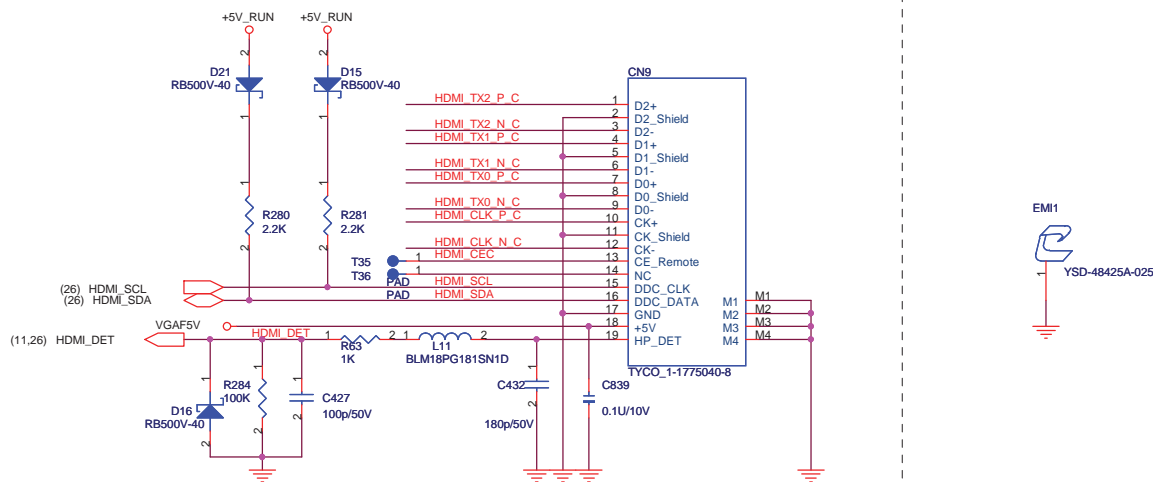
Title			
CRT CONN			
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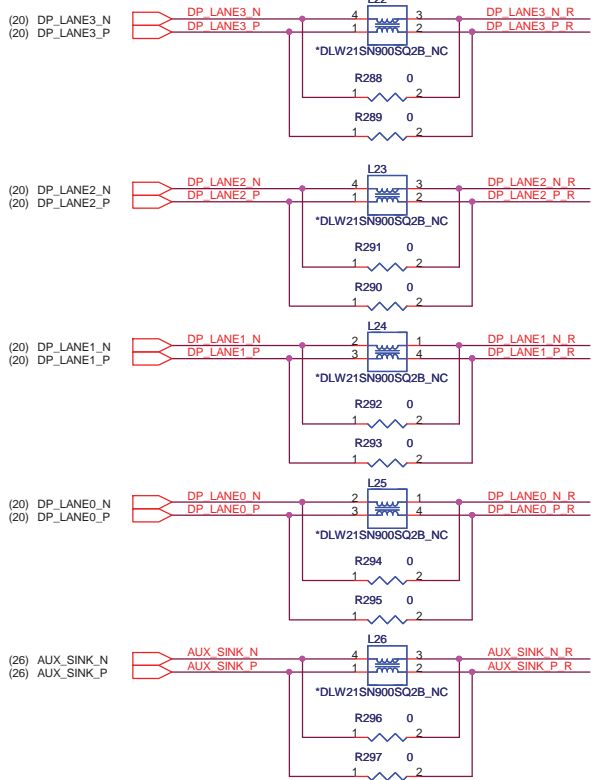
Reserve For EMI



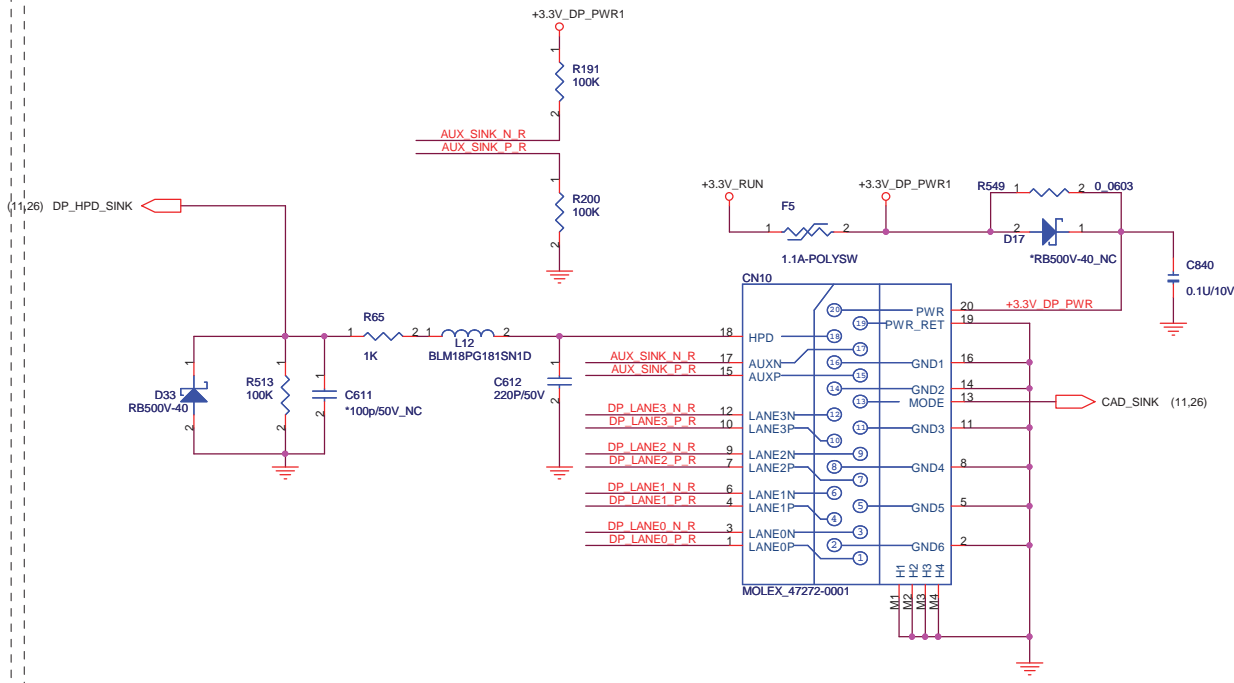
HDMI CONNECTOR



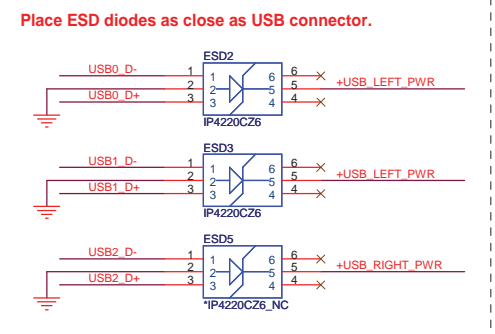
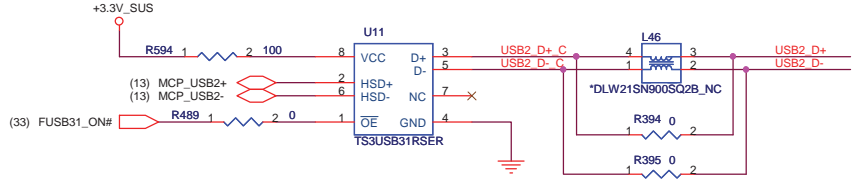
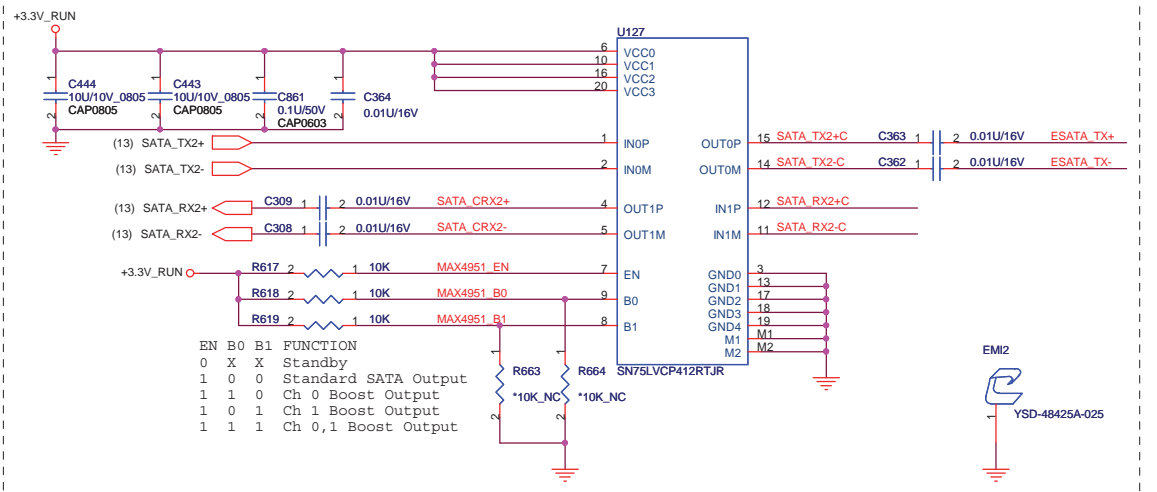
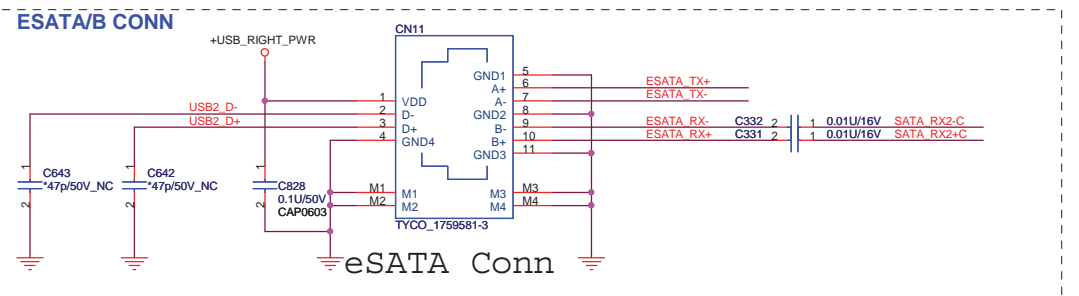
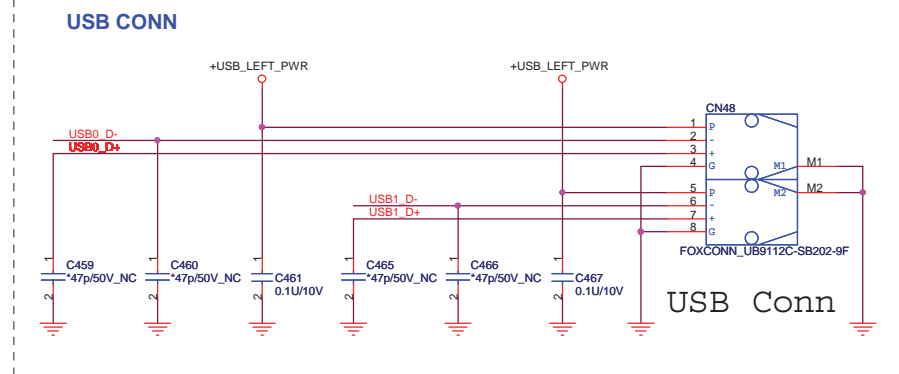
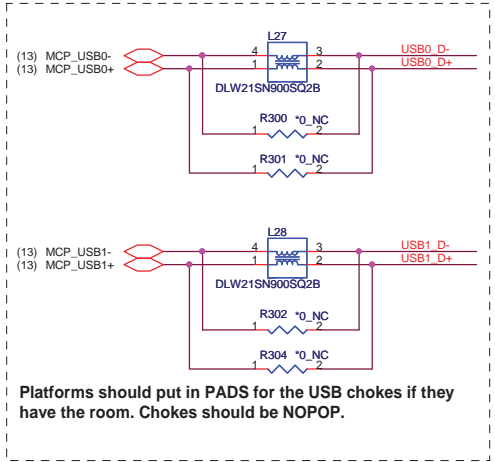
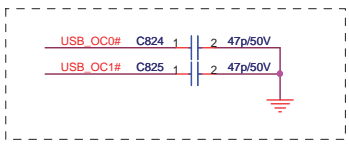
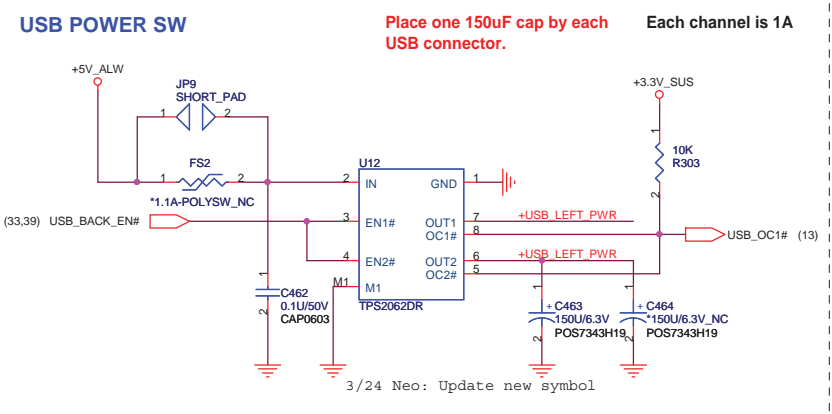
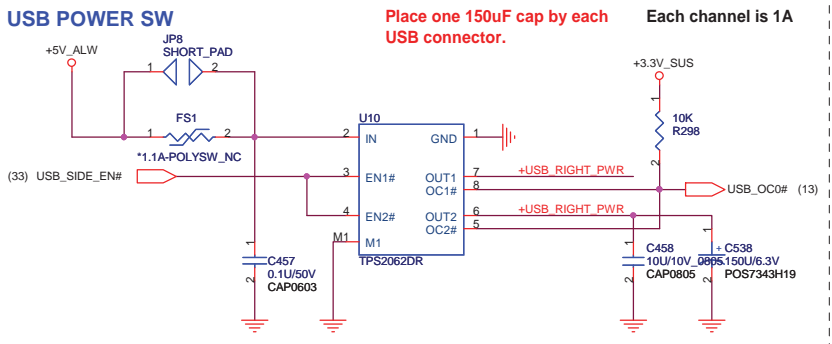
Reserve For EMI



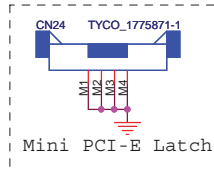
DISPLAY PORT CONNECTOR



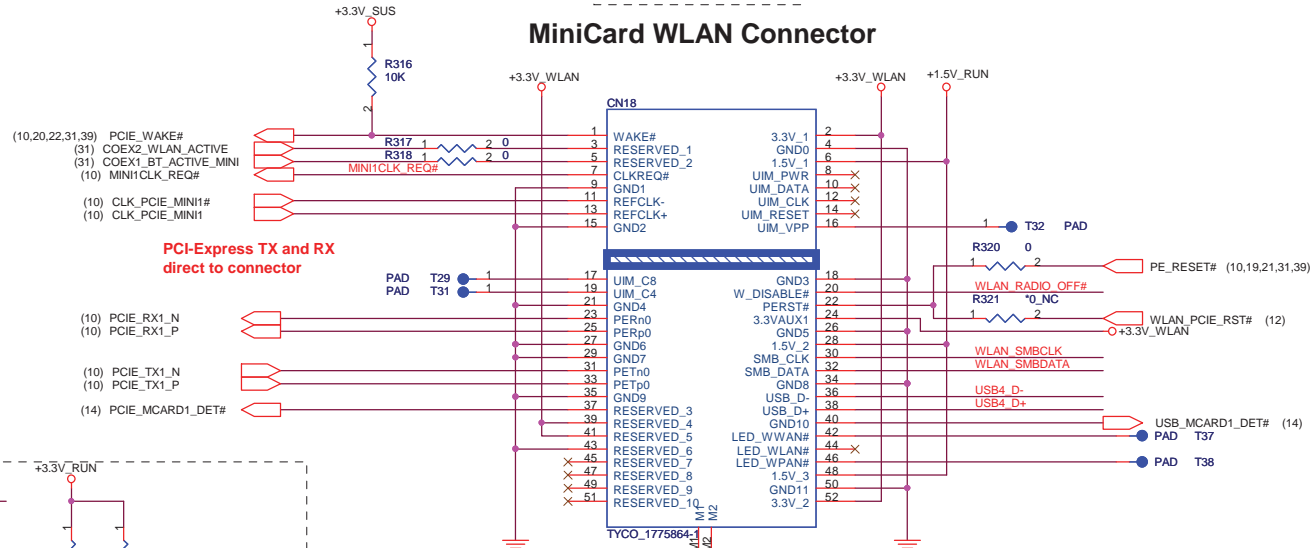
Title		
HDMI & DP CONN		
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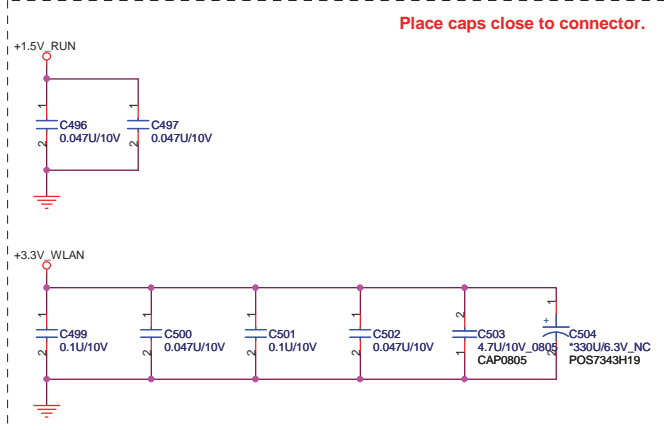
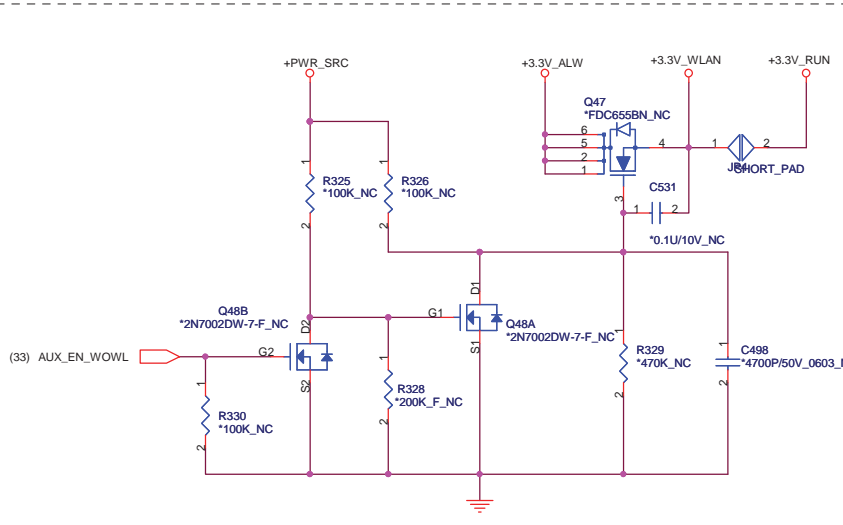
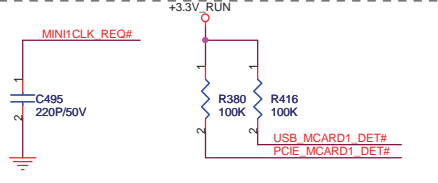
Title		
USBx2 & eSATA		
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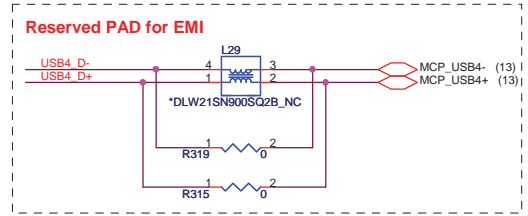
MiniCard WLAN Connector



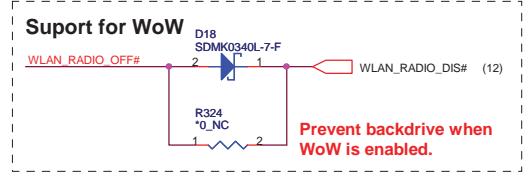
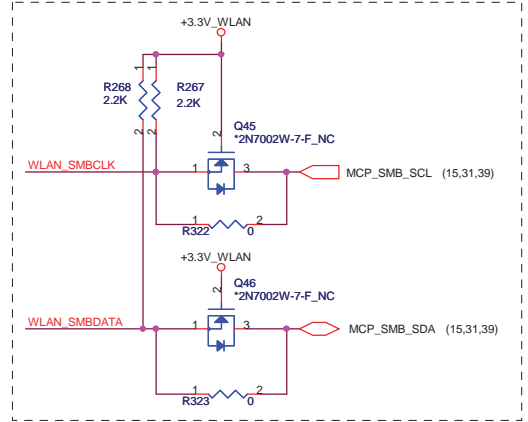
PCI-Express TX and RX direct to connector



Place caps close to connector.



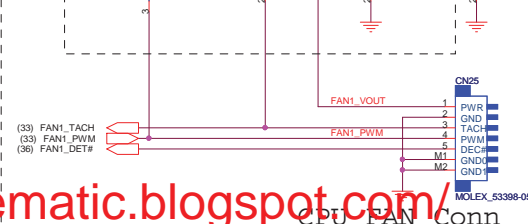
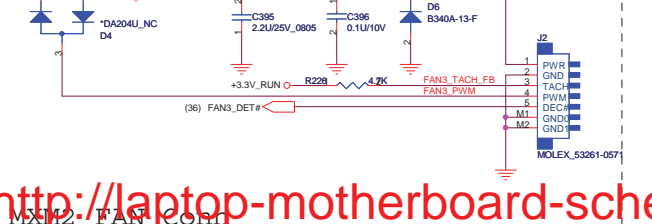
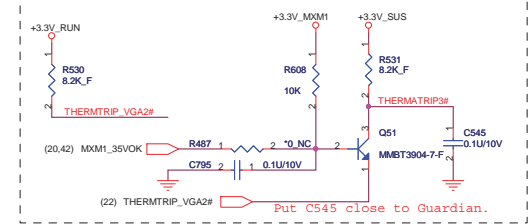
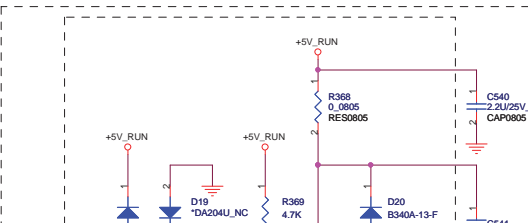
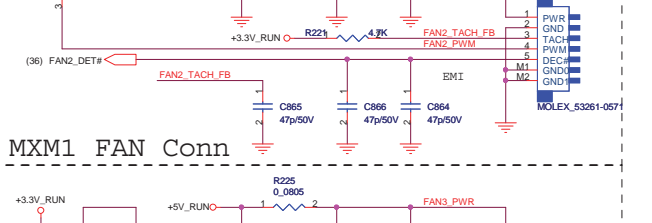
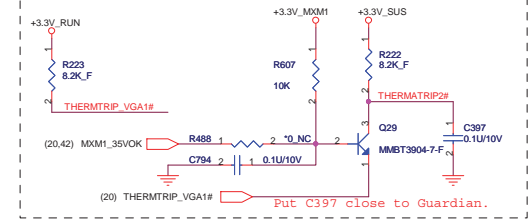
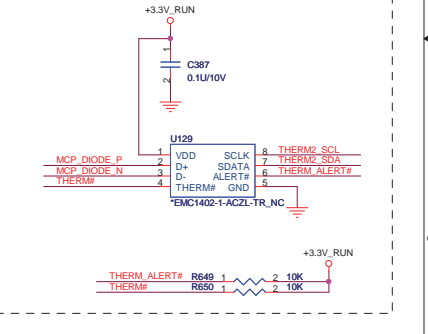
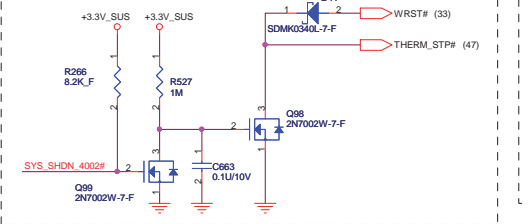
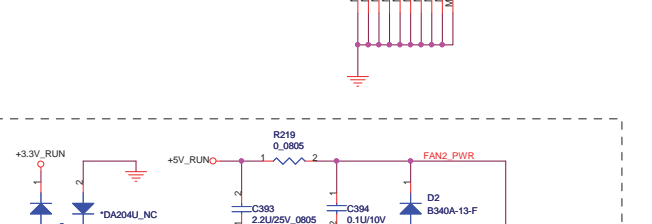
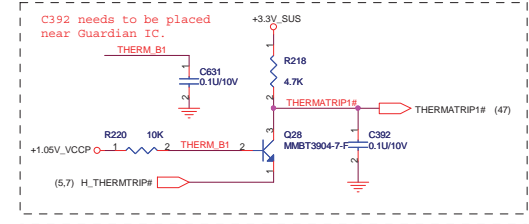
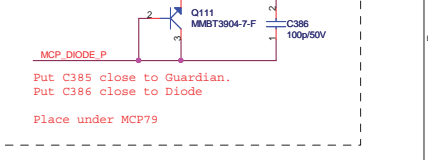
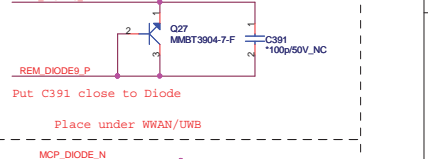
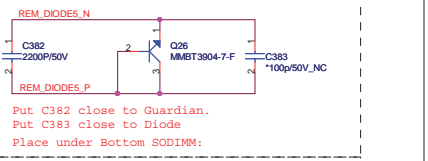
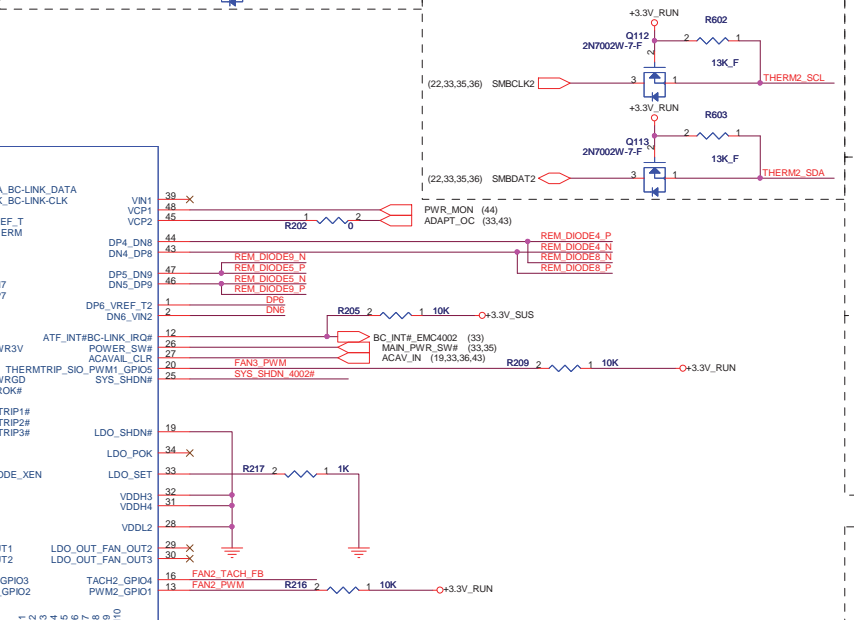
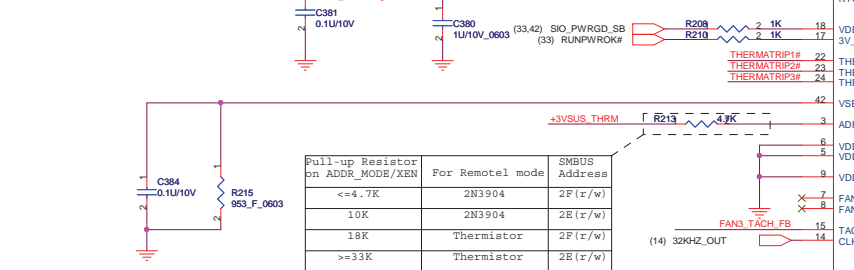
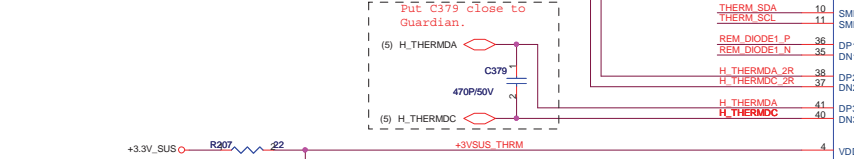
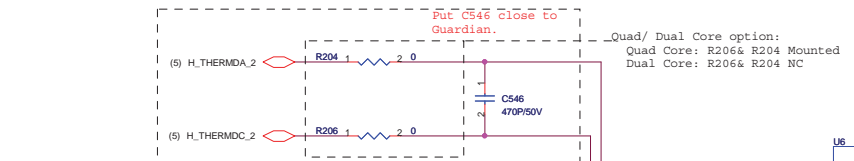
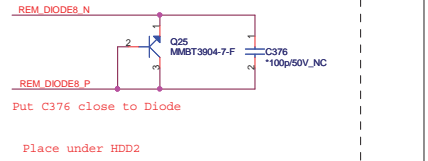
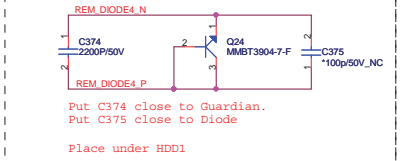
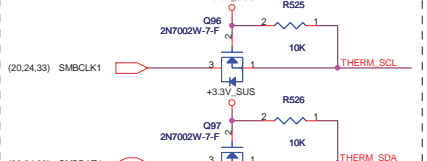
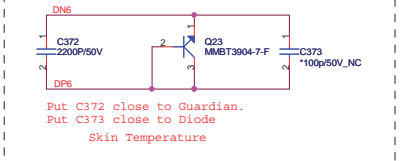
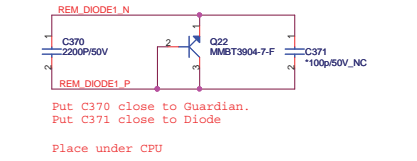
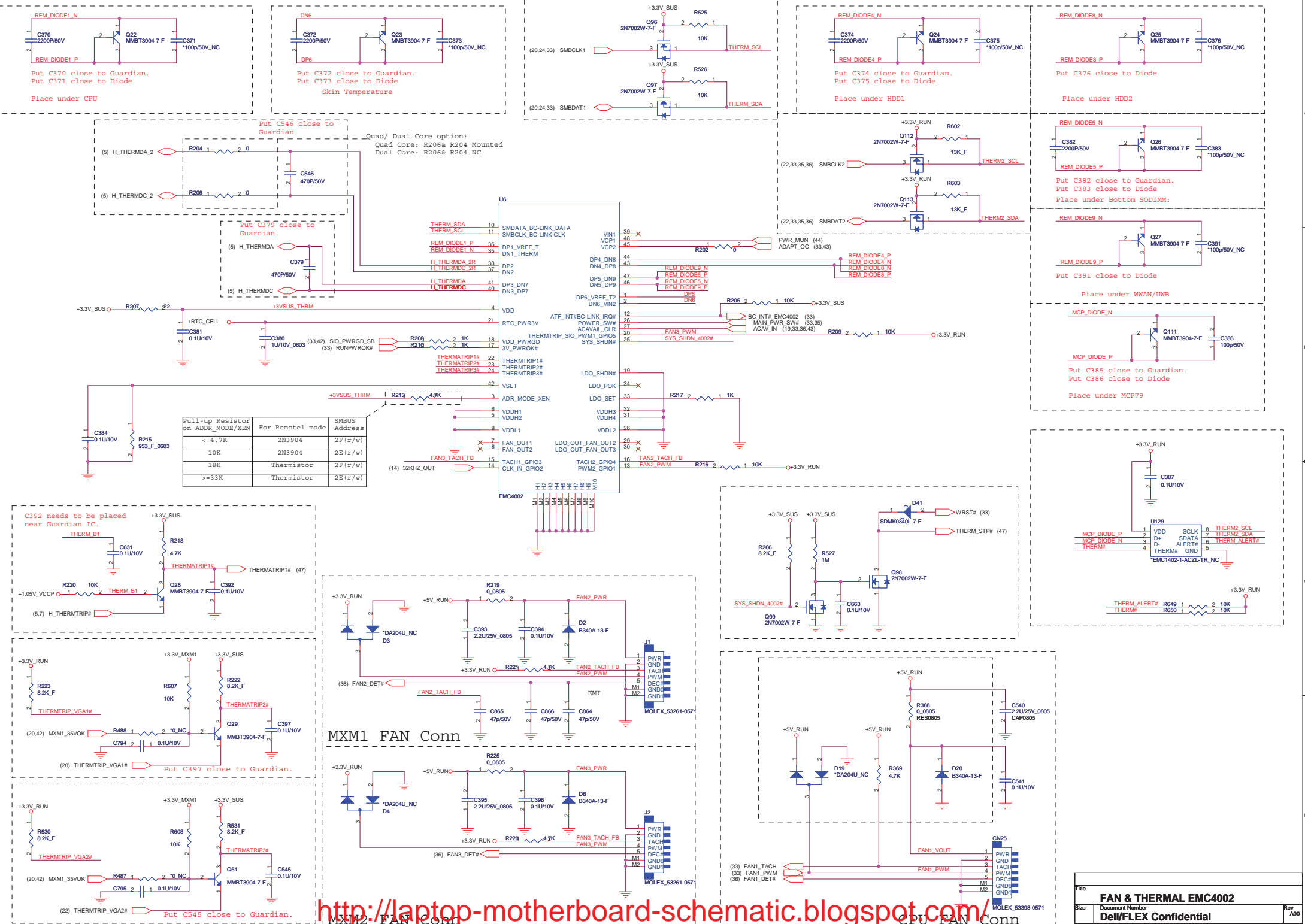
Reserved PAD for EMI



Support for WoW

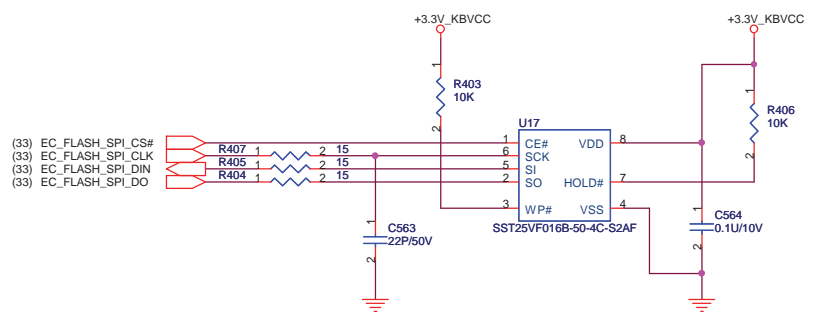
Prevent backdrive when WoW is enabled.

Title		
MINI-CARD (WLAN)		
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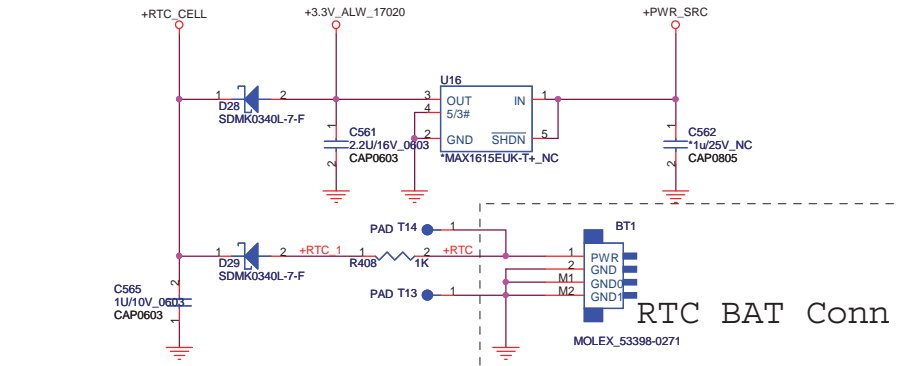


<http://laptop-motherboard-schematic.blogspot.com/>

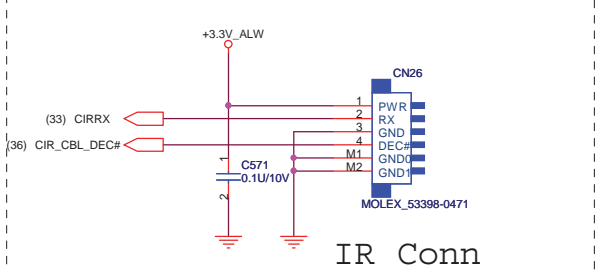
16Mbit (2M Byte), SPI



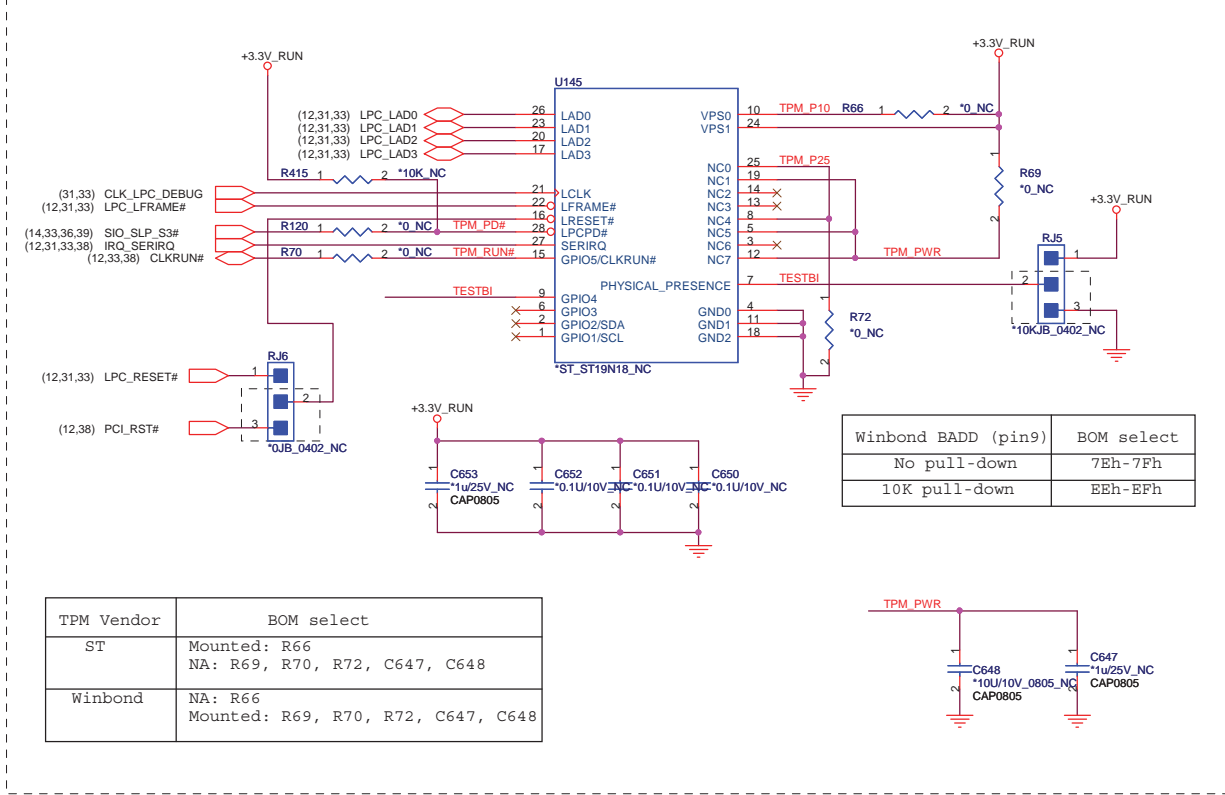
RTC BATTERY



to Consumer IR

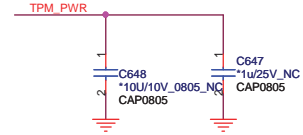


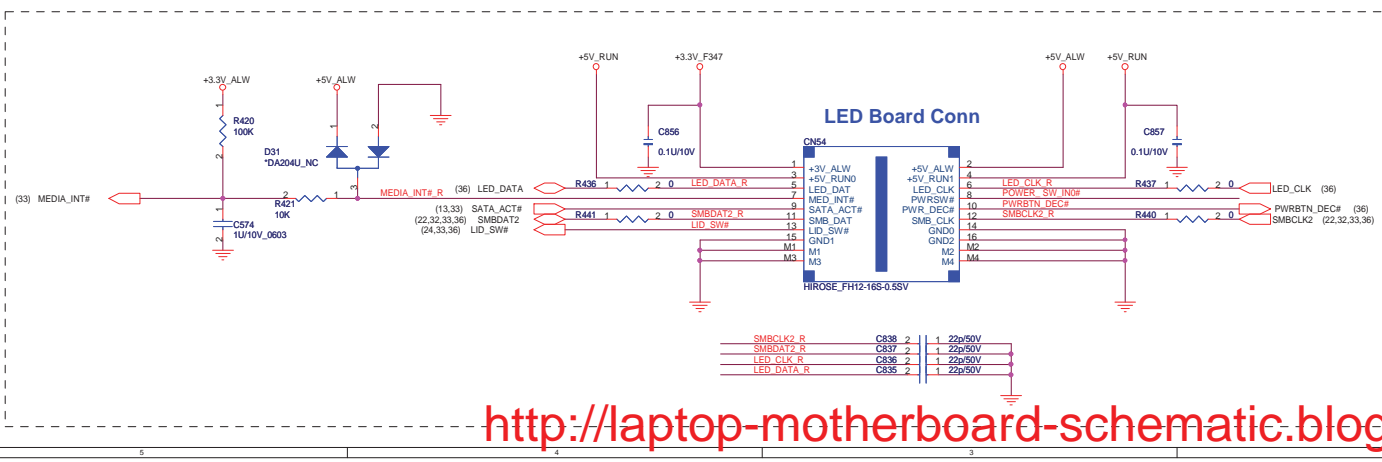
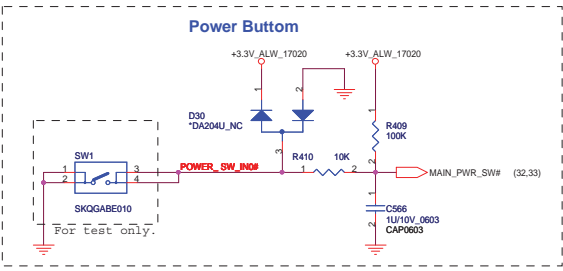
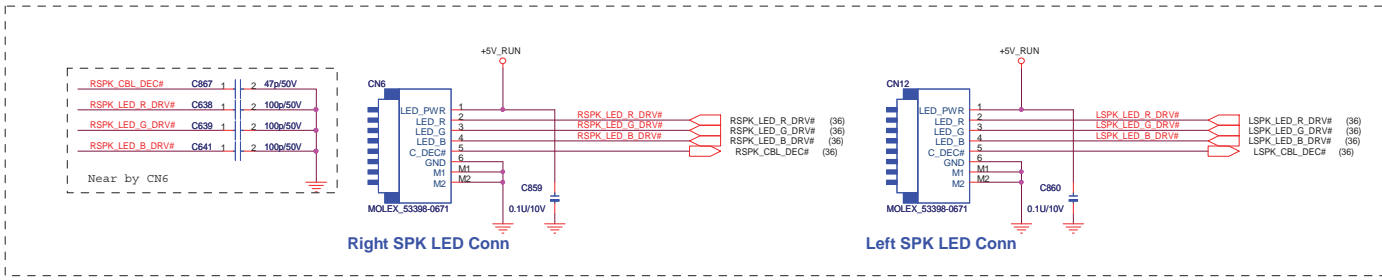
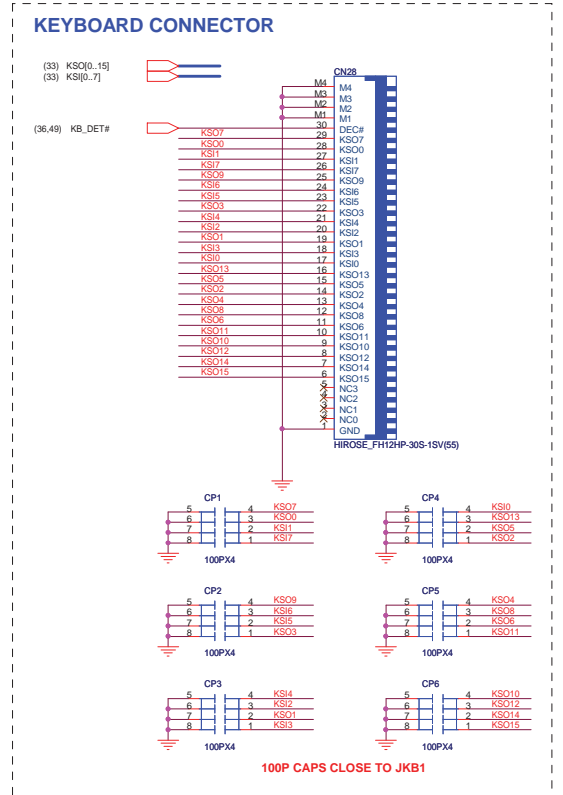
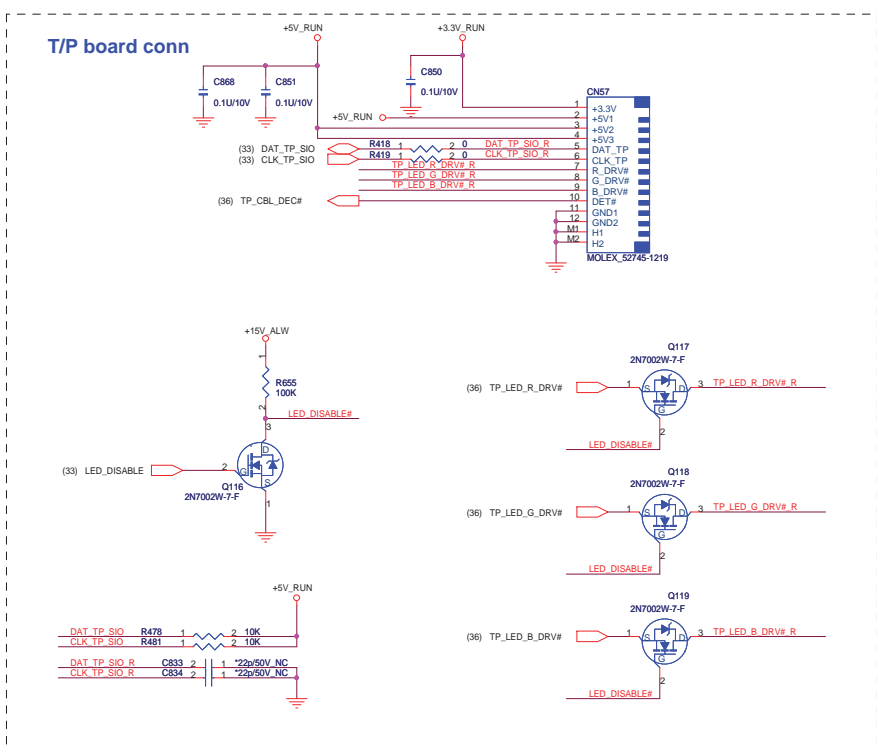
IR Conn



Winbond BADD (pin9)	BOM select
No pull-down	7Eh-7Fh
10K pull-down	EEh-EFh

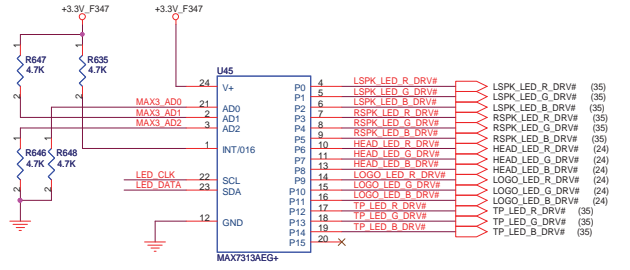
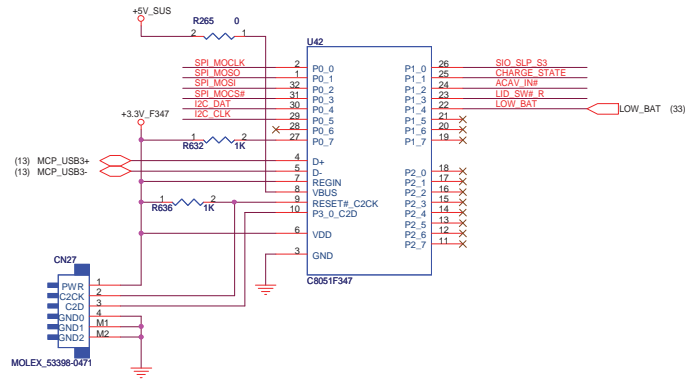
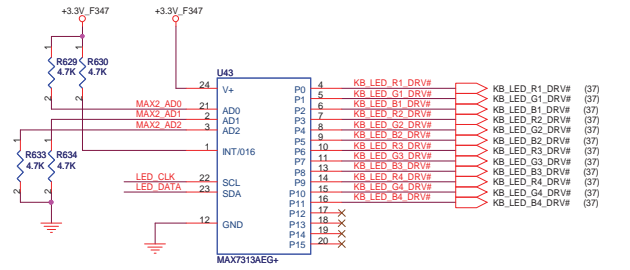
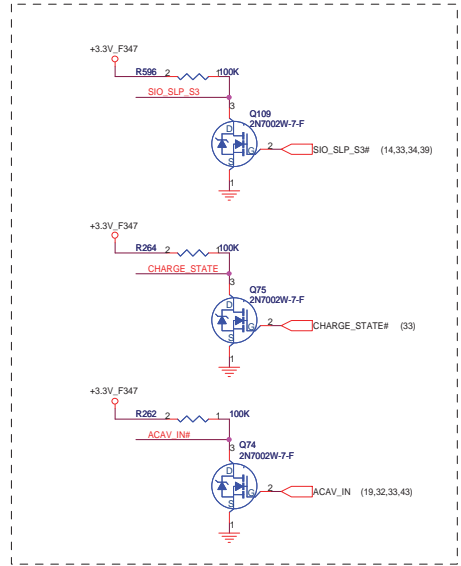
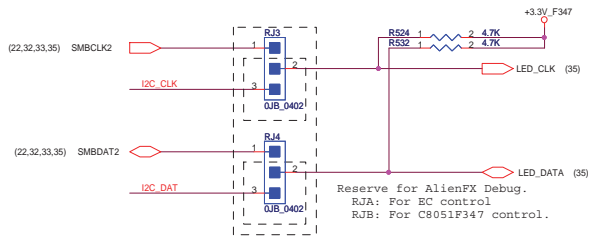
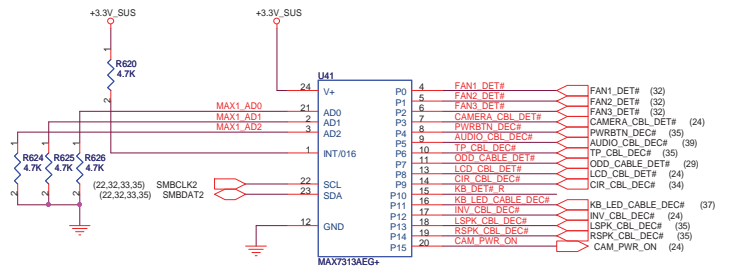
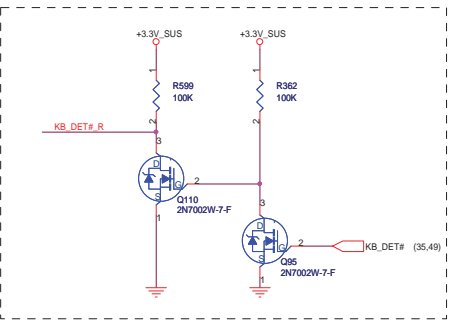
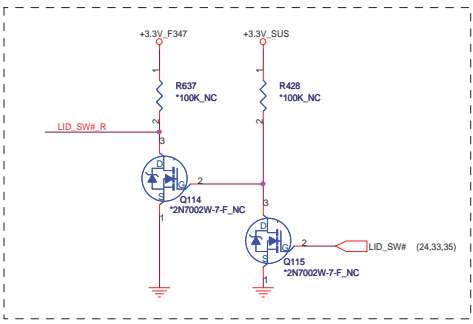
TPM Vendor	BOM select
ST	Mounted: R66 NA: R69, R70, R72, C647, C648
Winbond	NA: R66 Mounted: R69, R70, R72, C647, C648





<http://laptop-motherboard-schematic.blogspot.com/>

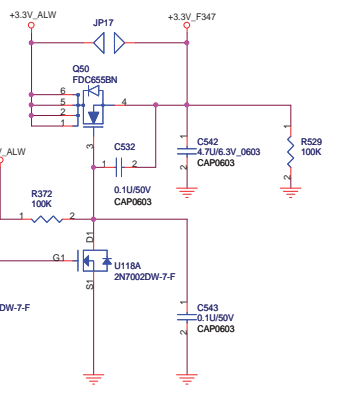
Title		KB/ DAUGHTER BOARD CONN	
Size	Document Number	Dell/FLEX Confidential	
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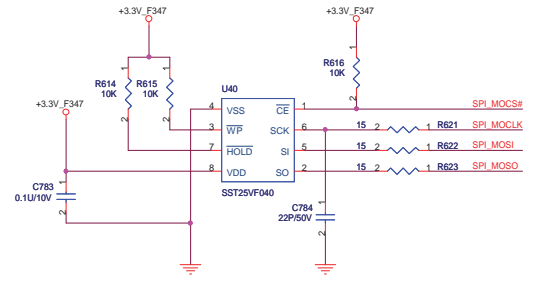
3.3V_F347 behavior

	State				
	S0	S3	S4	S5	
AC In	ON	ON	ON	ON	
BAT only	ON	ON	Off	Off	

AC mode Battery full in S5; turn off ELC controller.

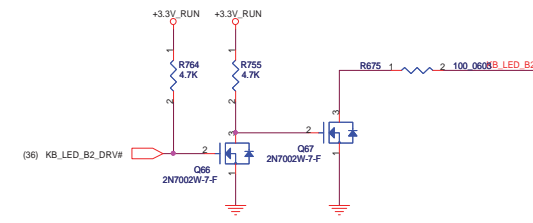
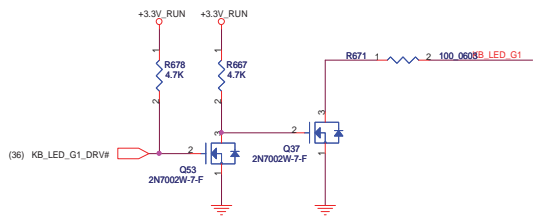
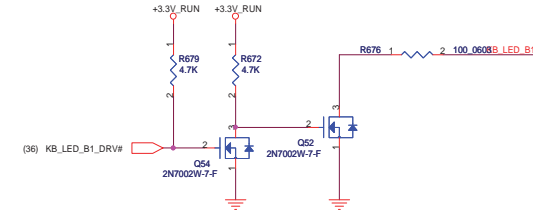
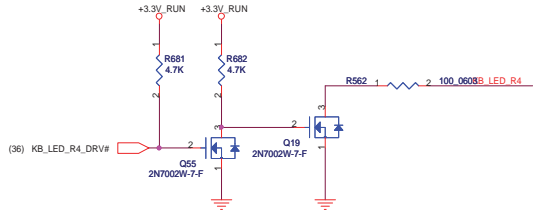
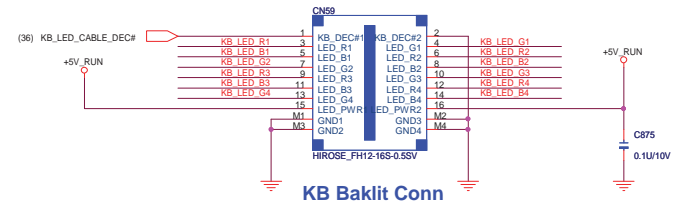
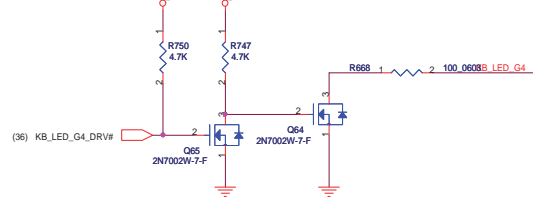
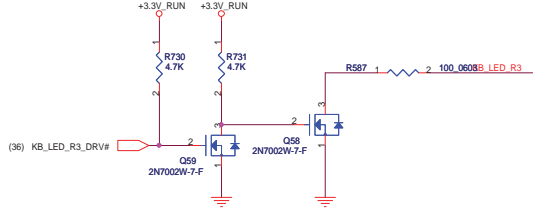
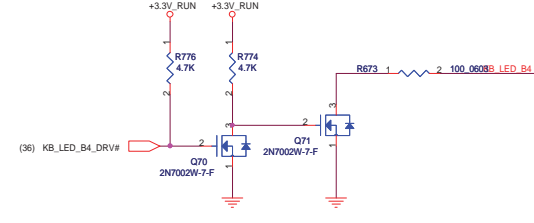
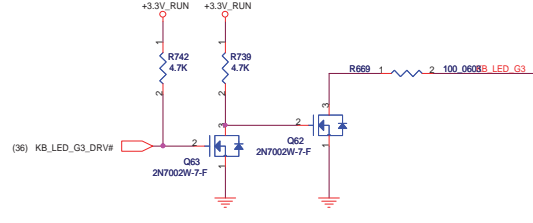
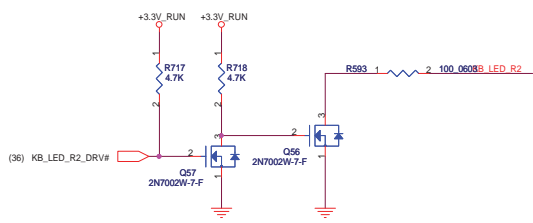
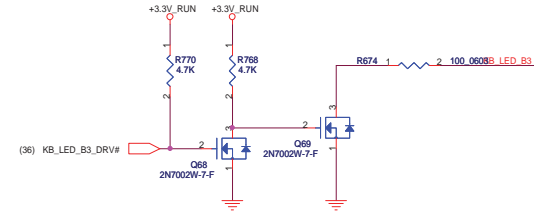
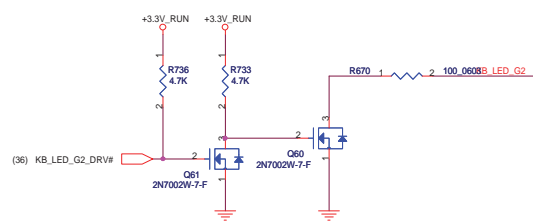
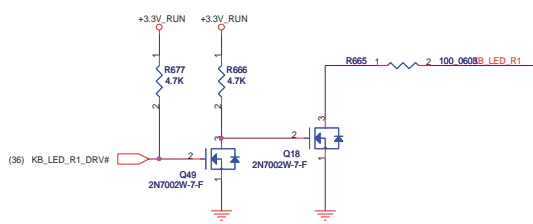


Reference	AD2	AD1	ADO	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPK& Head& Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

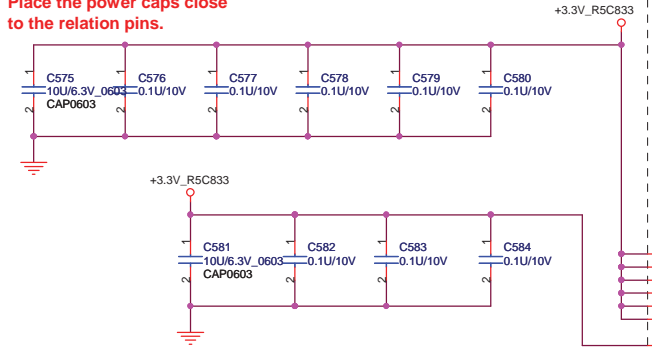


- CAMERA_CBL_DET# R427 1 2 100K
- AUDIO_CBL_DEC# R431 1 2 100K
- TP_CBL_DEC# R445 1 2 100K
- ODD_CABLE_DET# R446 1 2 100K
- LCD_CBL_DET# R447 1 2 100K
- CIR_CBL_DEC# R450 1 2 100K
- KB_LED_CABLE_DEC# R475 1 2 100K
- FAN1_DET# R462 1 2 100K
- FAN2_DET# R476 1 2 100K
- FAN3_DET# R477 1 2 100K
- INV_CBL_DEC# R480 1 2 100K
- LSPK_CBL_DEC# R483 1 2 100K
- RSPK_CBL_DEC# R484 1 2 100K
- PWRBTN_DEC# R680 1 2 100K
- CAM_PWR_ON R687 1 2 100K

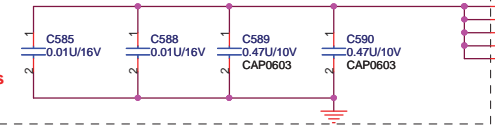
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM (U40)	1010 000b



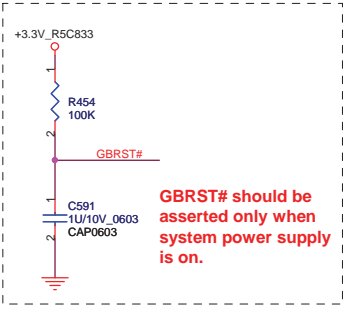
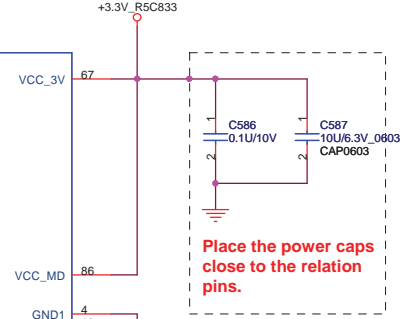
Place the power caps close to the relation pins.



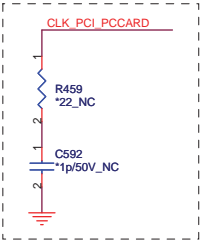
Please place capacitors for VCC_ROUTx as close to R5C833 as possible.



Place the power caps close to the relation pins.



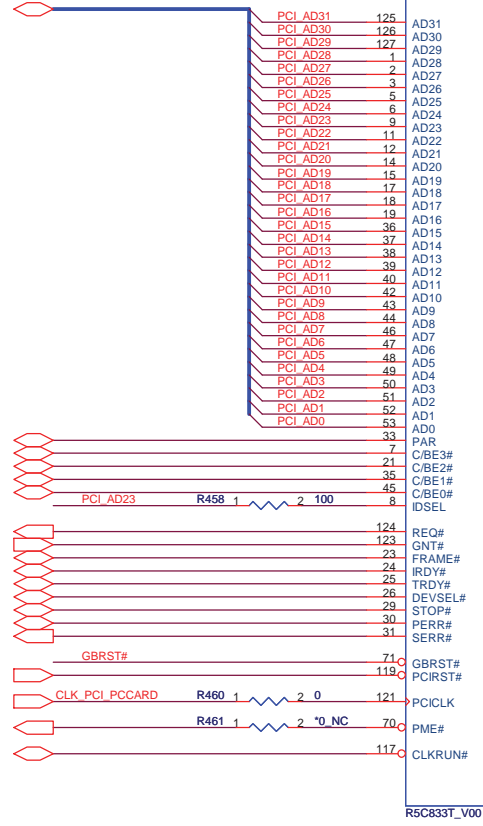
GBRST# should be asserted only when system power supply is on.



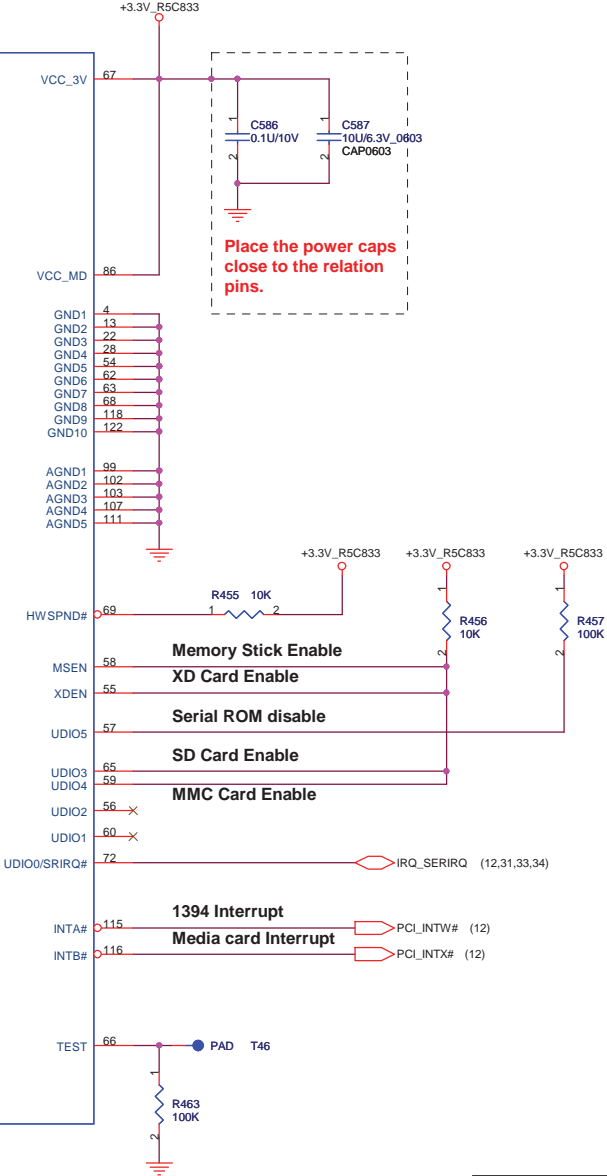
- (12) PCI_PAR
- (12) PCI_C_BE3#
- (12) PCI_C_BE2#
- (12) PCI_C_BE1#
- (12) PCI_C_BE0#

- (12) PCI_REQ0#
- (12) PCI_GNT0#
- (12) PCI_FRAME#
- (12) PCI_IRDY#
- (12) PCI_TRDY#
- (12) PCI_DEVSEL#
- (12) PCI_STOP#
- (12) PCI_PERR#
- (12) PCI_SERR#

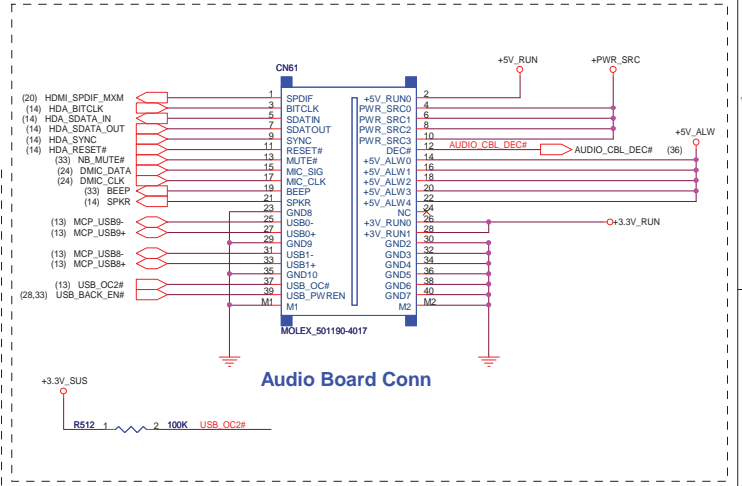
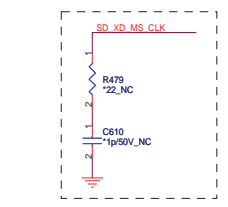
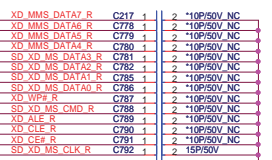
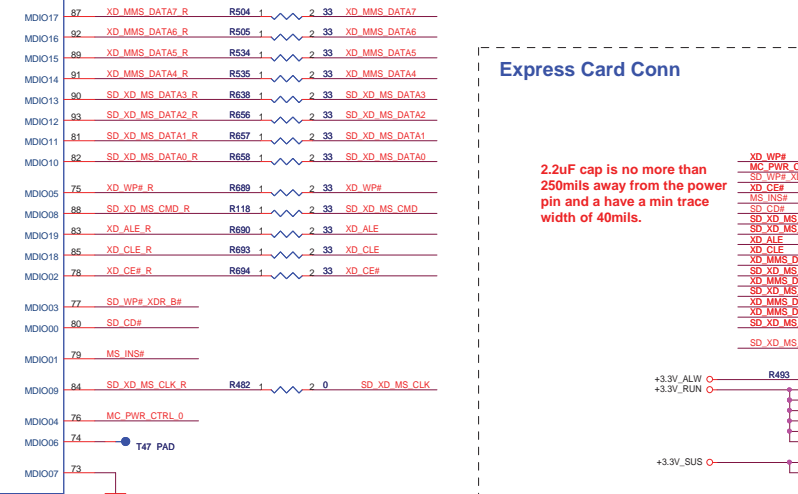
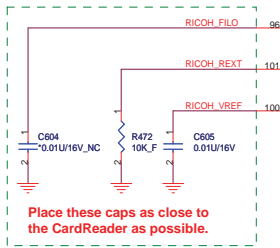
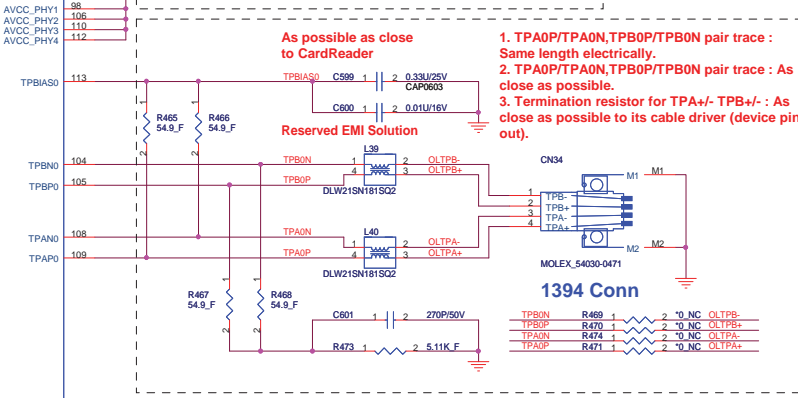
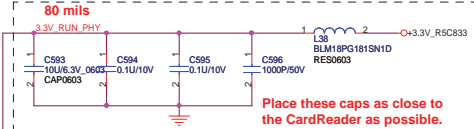
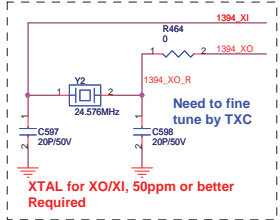
- (12,34) PCI_RST#
- (12) CLK_PCI_PCCARD
- (12) PCI_PME#
- (12,33,34) CLKRUN#



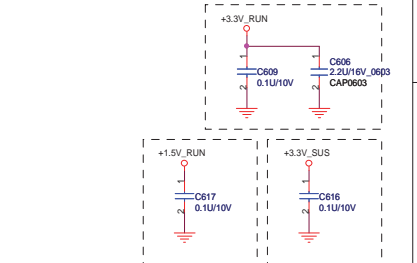
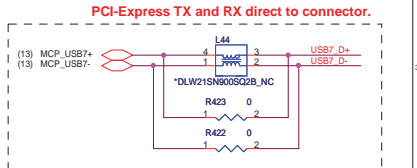
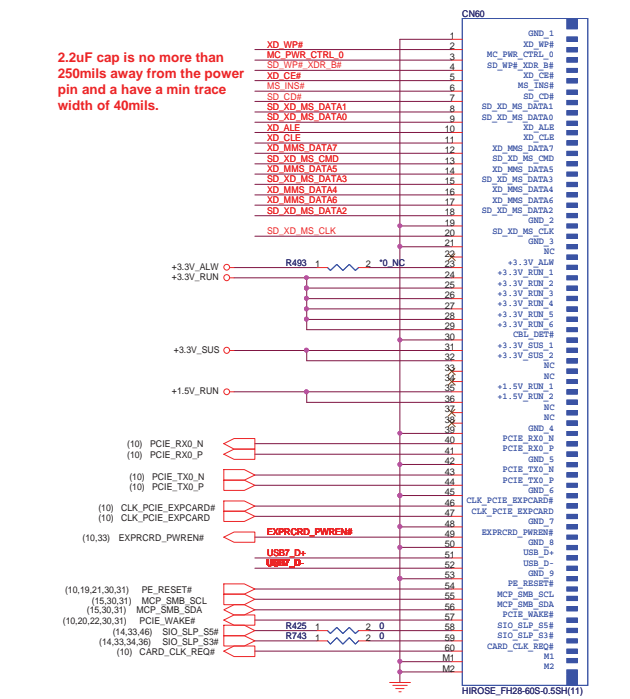
PCI / OTHER



Title CardReader (5C833)		
Size	Document Number	Rev A00
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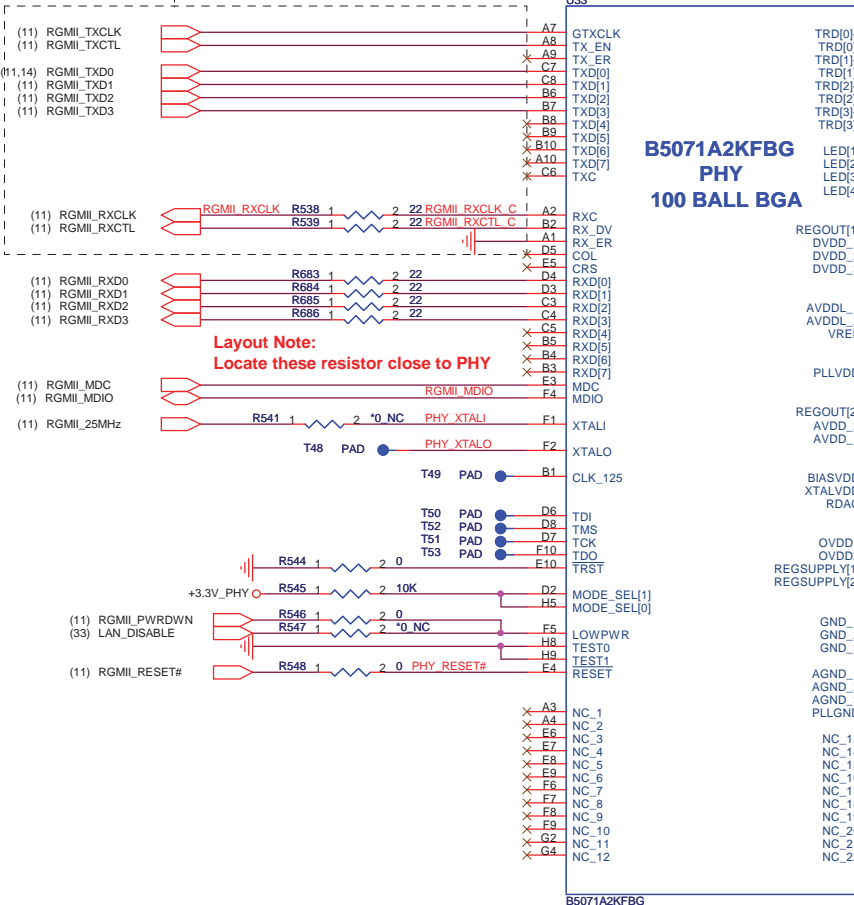
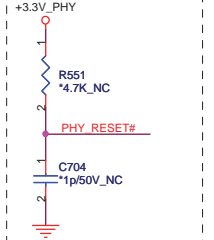
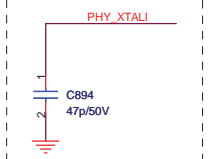
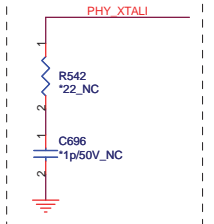
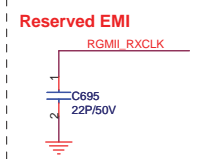
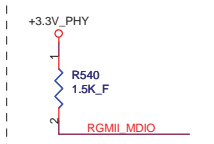
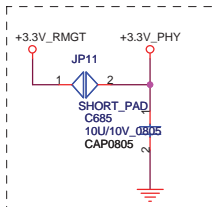


Express Card Conn

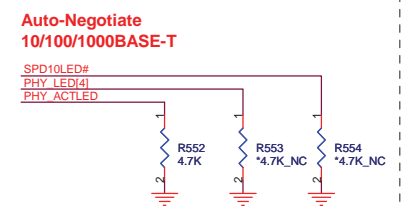
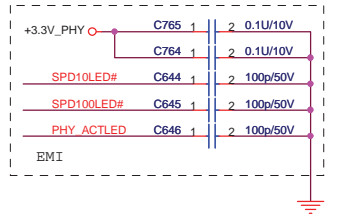
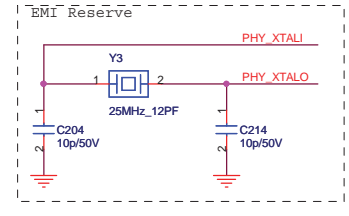


Layout Note:

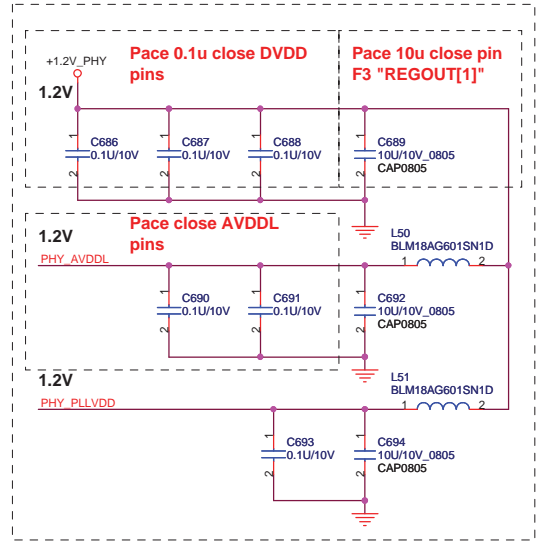
1. Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



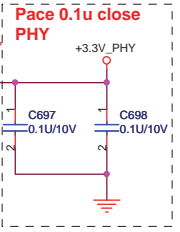
Layout Note:
Locate these resistor close to PHY



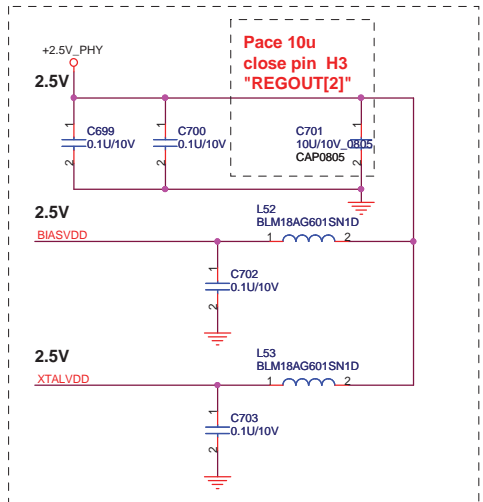
**B5071A2KFBG
PHY
100 BALL BGA**



Layout Note:
Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.



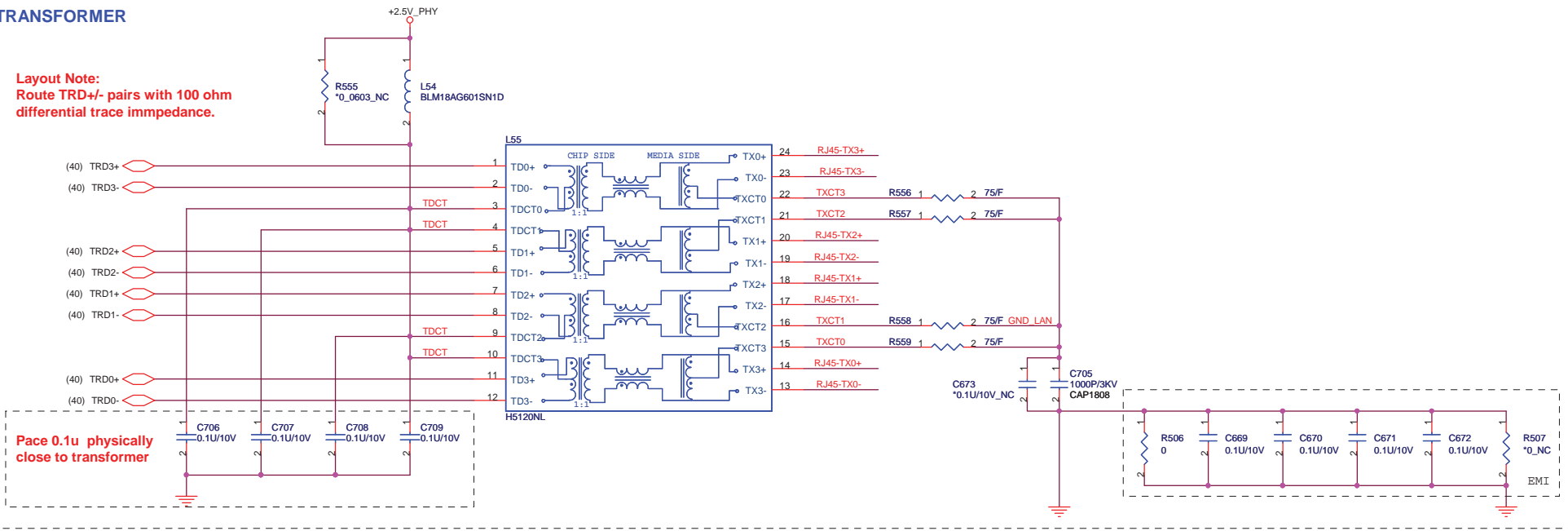
**Pull-High: Address 1
NC : Address 0**



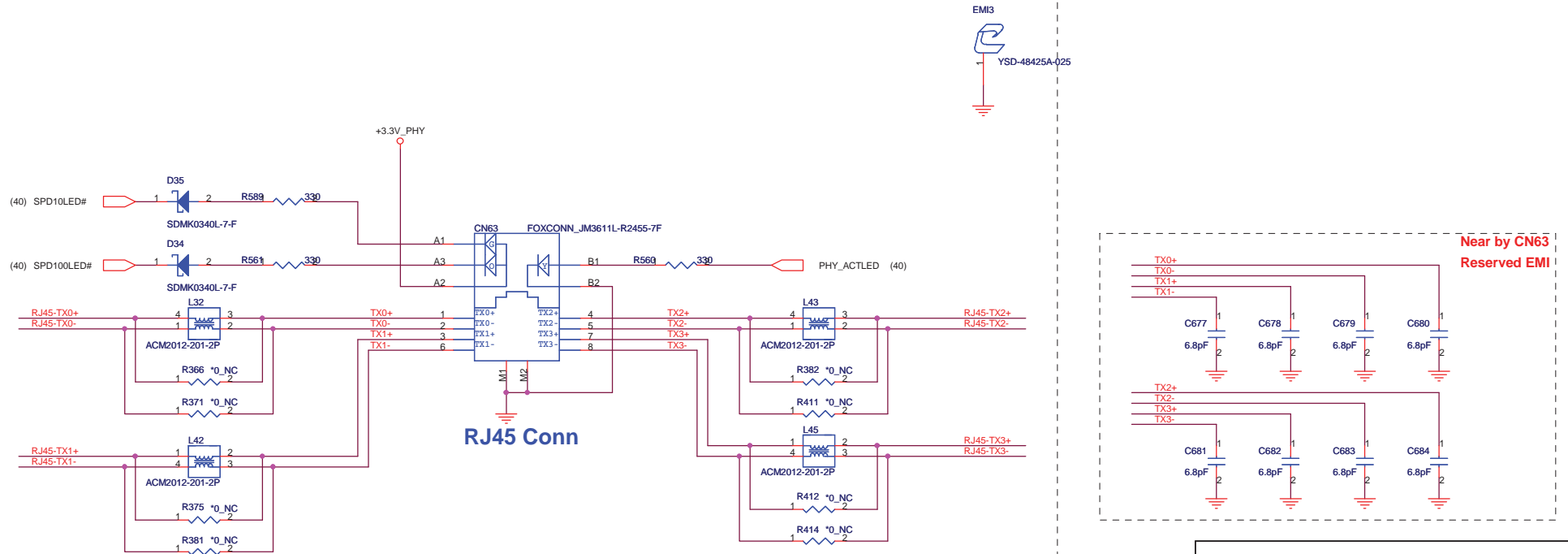
Title			PHY(B5071)		
Size	Document Number		Rev		A00
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TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.



RJ-45 Connector



Title			RJ-45/TRANSFORM		
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Date			Thursday, March 12, 2009		
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Note:
Component Values on Schematic are for MAX8731 only.
Please see table 1-3 for BQ24745 or ISL88731
component Values.

TABLE 3. PIN NAME DIFFERENCES

PIN	MAX8731A	ISL88731	bq24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDD5MB	VDD5MB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LAGIE	LAGIE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGATE
26	BST	BOOT	BOOT
25	VCC	VCC	ICOUT

*NC means no-connect

TABLE 2 BOM DIFFERENCES

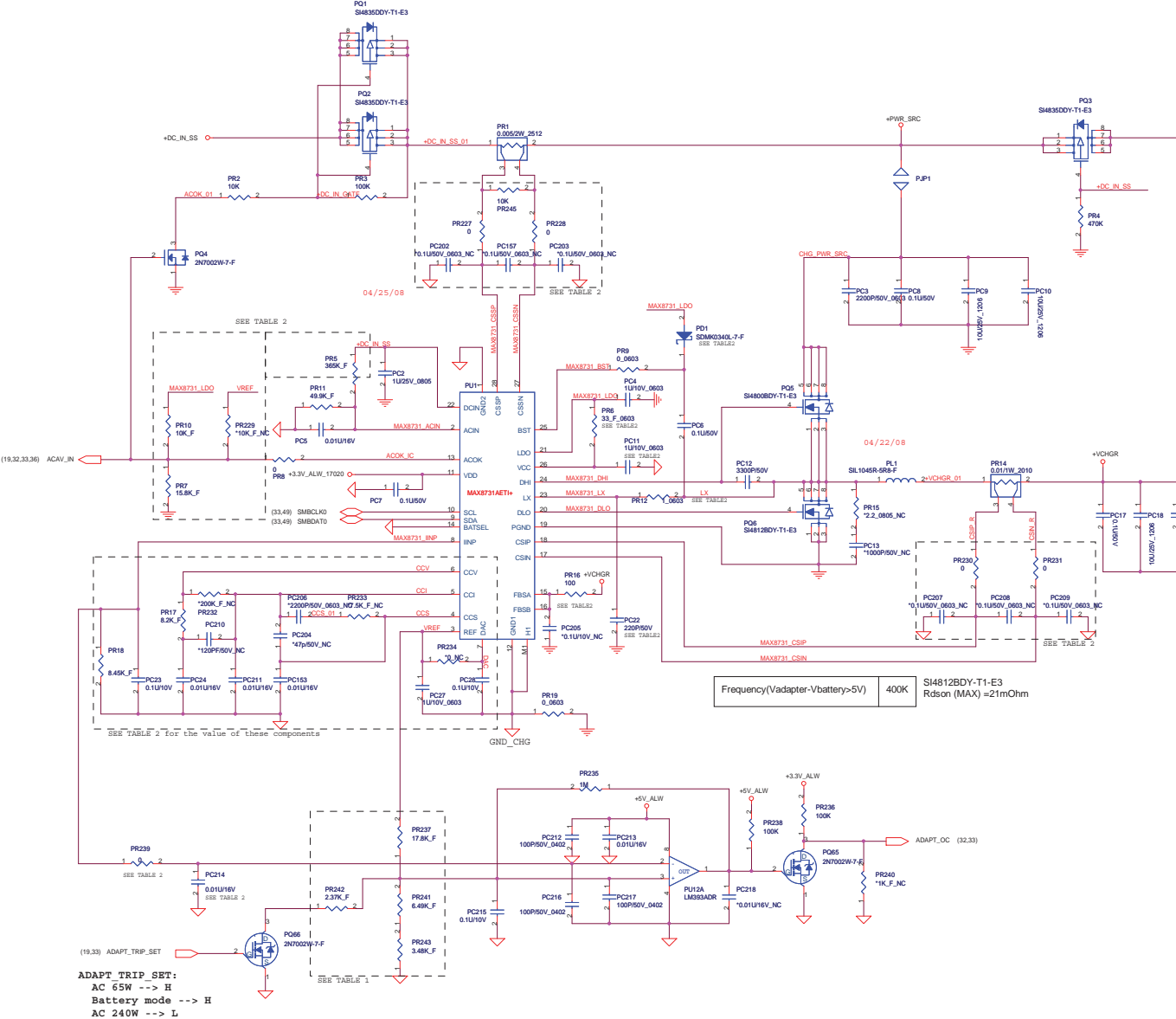
REF DES	MAXIM	INTERSIL	TI
PR245	NO STUFF	10K, 0.402, 5%	NO STUFF
PR227	0, 0.402, 5%	10, 0.402, 5%	0, 0.402, 5%
PR229	0, 0.402, 5%	10, 0.402, 5%	0, 0.402, 5%
PC157	NO STUFF	0, 1uF	0, 1uF
PC202	NO STUFF	NO STUFF	0, 1uF
PC203	NO STUFF	NO STUFF	NO STUFF
PR230	0, 0.402, 5%	10, 0.402, 5%	0, 0.402, 5%
PR231	0, 0.402, 5%	10, 0.402, 5%	0, 0.402, 5%
PC207	NO STUFF	NO STUFF	0, 1uF
PC208	NO STUFF	0, 1uF	0, 1uF
PC209	NO STUFF	NO STUFF	NO STUFF
PR17	8.2K, 0.402, 5%	2.2K, 0.402, 5%	4.7K, 0.402, 5%
PR18	8.45K, 0.402, 1%	NO STUFF	NO STUFF
PR232	NO STUFF	NO STUFF	200K, 0.402, 5%
PR233	NO STUFF	NO STUFF	7.5K, 0.402, 5%
PR234	NO STUFF	NO STUFF	0, 0.402, 5%
PC23	0.1uF, 0.402, 10V	NO STUFF	200uF, 0.402, 10V
PC24	0.01uF	0.01uF	NO STUFF
PC210	NO STUFF	NO STUFF	130uF, 0.402, 10V
PC211	0.01uF	NO STUFF	NO STUFF
PC153	0.01uF	0.01uF	NO STUFF
PC204	NO STUFF	NO STUFF	51uF, 0.402, 10V
PC27	1.0uF, 0.603, 10V	NO STUFF	3000uF, 0.402, 10V
PC29	0.1uF, 0.402, 10V	NO STUFF	NO STUFF
PR10	10K, 0.402, 1%	10K, 0.402, 1%	NO STUFF
PR7	15.8K, 0.402, 1%	15.8K, 0.402, 1%	NO STUFF
PR229	NO STUFF	NO STUFF	10K, 0.402, 5%
PR5	365K, 0.402, 1%	215K, 0.402, 1%	309K, 0.402, 5%
PD1	CH501H-40PT	NO STUFF	CH501H-40PT
PR6	33, 0.603, 1%	33, 0.603, 1%	NO STUFF
PC11	1.0uF, 0.603, 10V	1.0uF, 0.603, 10V	NO STUFF
PR12	1, 0.603, 1%	0, 0.603, 5%	0, 0.603, 5%
PR11	100, 0.402, 5%	100, 0.402, 5%	0, 0.402, 5%
PC22	220uF, 0.402, 50V	NO STUFF	NO STUFF
PR239	0, 0.402, 5%	8.45K, 0.402, 1%	8.45K, 0.402, 1%
PC24	0.1uF	0.1uF	0.1uF
PC12	3.3nF	NO STUFF	NO STUFF

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	MAX8731A/ISL88731				bq24745		
		R237	R241	R243	R242 (see Note 1)	R241	R243	R242 (see Note 1)
65	3.17	57.6K	13K	105	24.9K	12.4K	205	24.3K
150	7.43	30.9K	24.9K	499	10.7K	23.7K	499	10.5K
240	11.69 (see Note 2)	17.8K	6.49K	3.48K	2.37K	8.45K	1.18K	23.2K

Note 1 : R242 is populated if ADAPT_TRIP_SET is used to program for the next lower adapter
ADAPT_TRIP_SET is floating for the higher adapter , grounded for the lower adapter
Note 2 : RR1 must be 5mOhms instead of 10mOhms for the 240W adapter

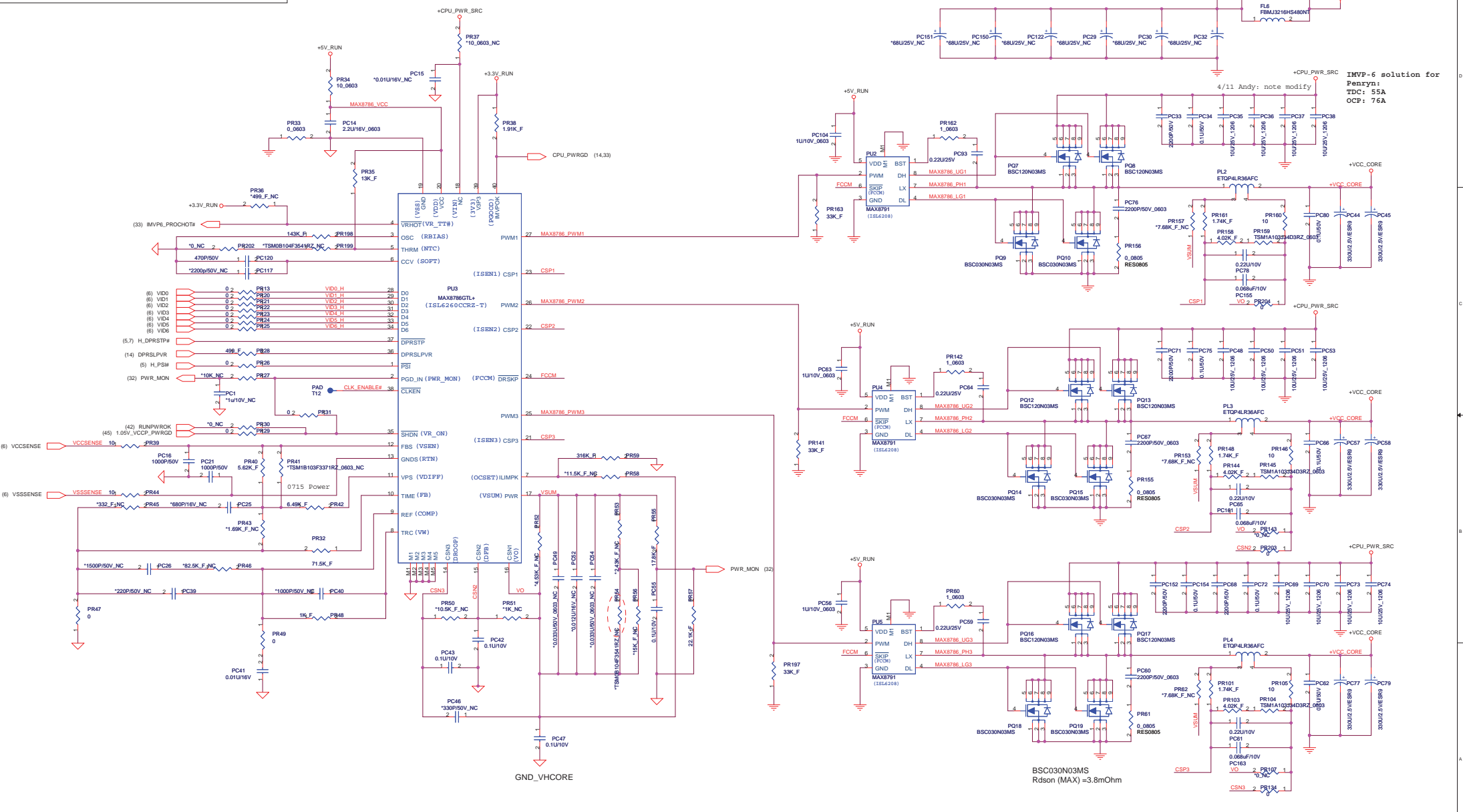
File	Charger (MAX8731)	
Size	Document Number	Rev
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Frequency(Vadapter-Vbattery>5V) 400K
SI4812BDY-T1-E3
Rds(on) (MAX) =21mOhm

ADAPT_TRIP_SET:
AC 65W --> H
Battery mode --> H
AC 240W --> L

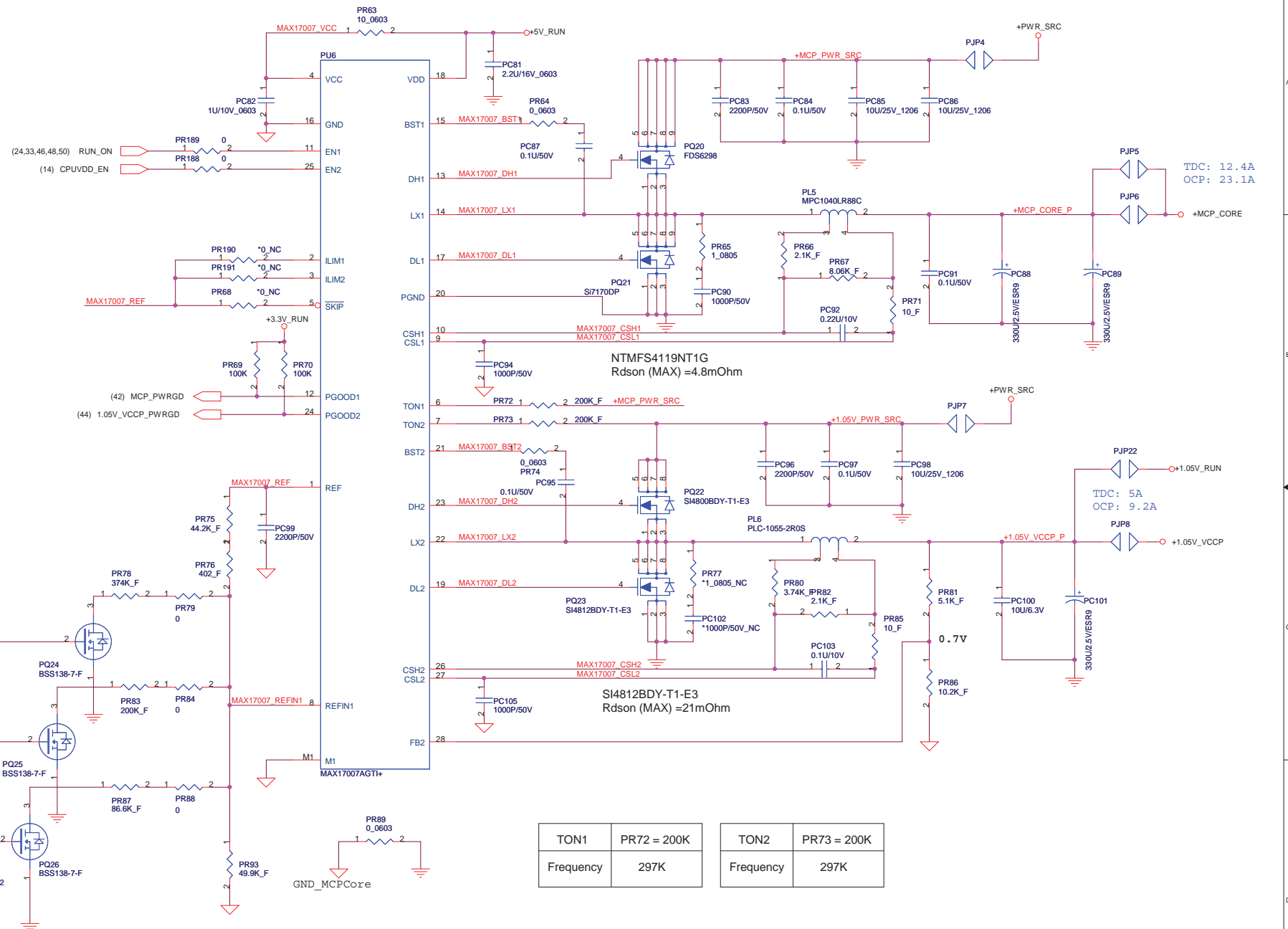
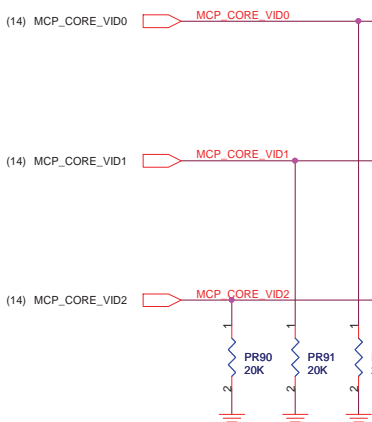
NOTE:
Component Values on Schematic are for MAXIM MAX8786 only.



File			CPU_CORE (MAX8786)	
Size	Document Number			Rev
	Dell/FLEX Confidential			Ado
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ILIM1/ILIM2	Current Limit
VCC	60mV
OPEN	45mV
REF	30mV
GND	15mV

VID2	VID1	VID0	+MCP_Core
L	L	L	NA
L	L	H	+1.000V
L	H	L	+0.950V
L	H	H	+0.900V
H	L	L	NA
H	L	H	NA
H	H	L	NA
H	H	H	NA



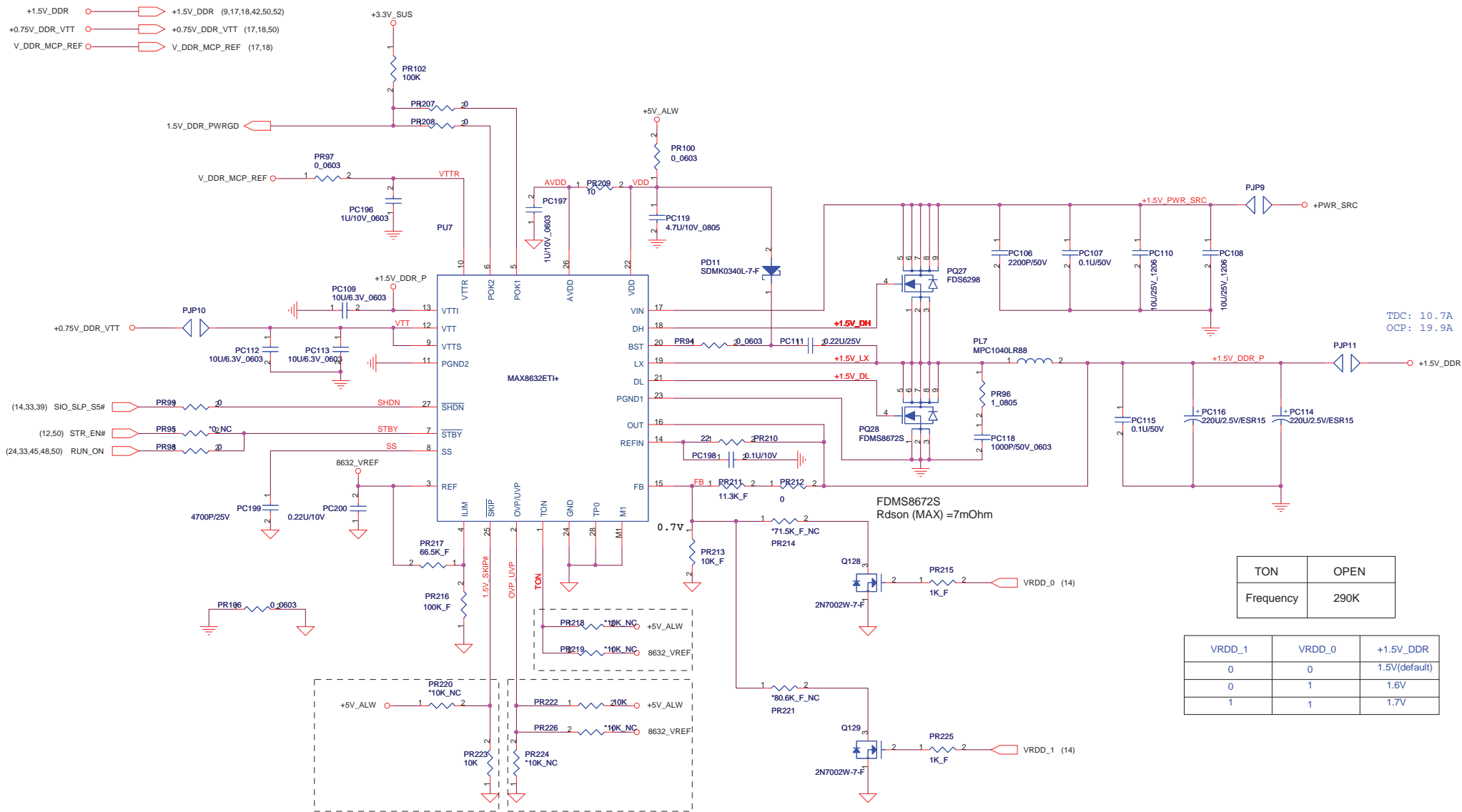
TON1	PR72 = 200K	TON2	PR73 = 200K
Frequency	297K	Frequency	297K

+MCP_CORE (15,52)
+1.05V_VCCP (5,6,7,9,10,14,15,32,52)

TDC: 12.4A
OCP: 23.1A

TDC: 5A
OCP: 9.2A

Title			MCP1.05VCC (MAX17007)		
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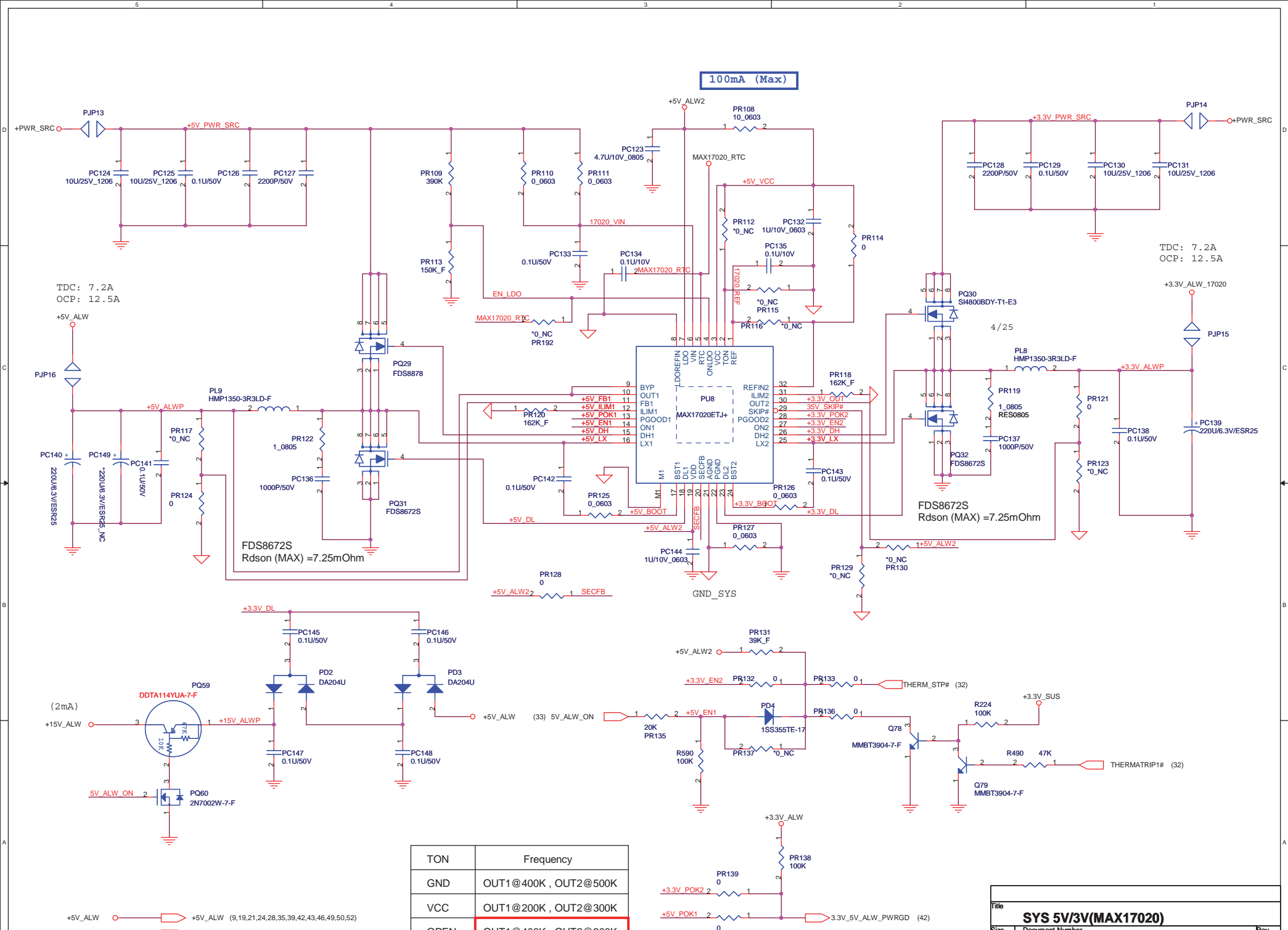


TDC: 10.7A
 OCP: 19.9A

TON	OPEN
Frequency	290K

VRDD_1	VRDD_0	+1.5V_DDR
0	0	1.5V(default)
0	1	1.6V
1	1	1.7V

Title		
DDR1.5/0.75(TPS51116)		
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100mA (Max)

TDC: 7.2A
OCP: 12.5A

TDC: 7.2A
OCP: 12.5A

FDS8672S
Rdson (MAX) = 7.25mOhm

FDS8672S
Rdson (MAX) = 7.25mOhm

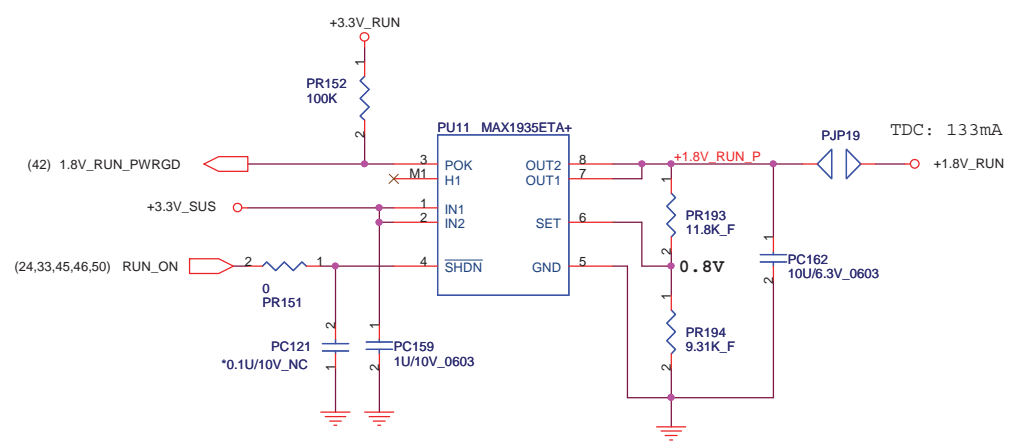
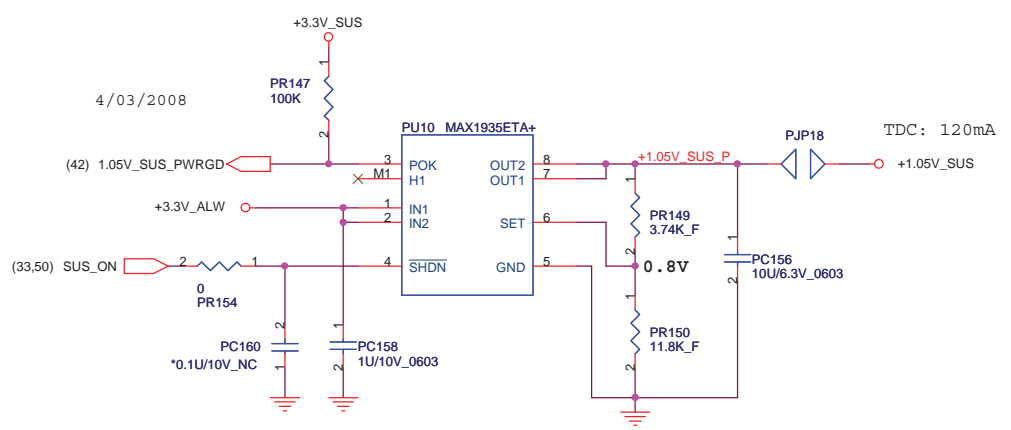
TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K

+5V_ALW ○ +5V_ALW (9,19,21,24,28,35,39,42,43,46,49,50,52)

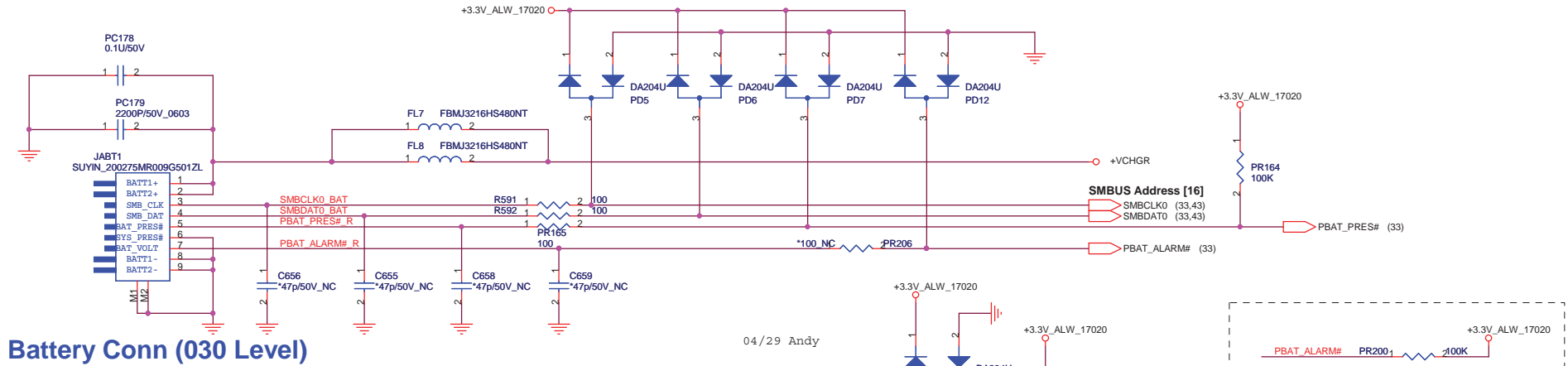
+3.3V_ALW_17020 ○ +3.3V_ALW_17020 (33,34,35,43,49,50)

Title		
SYS 5V/3V(MAX17020)		
Size	Document Number	Rev
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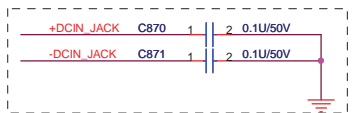
<http://laptop-motherboard-schematic.blogspot.com/>



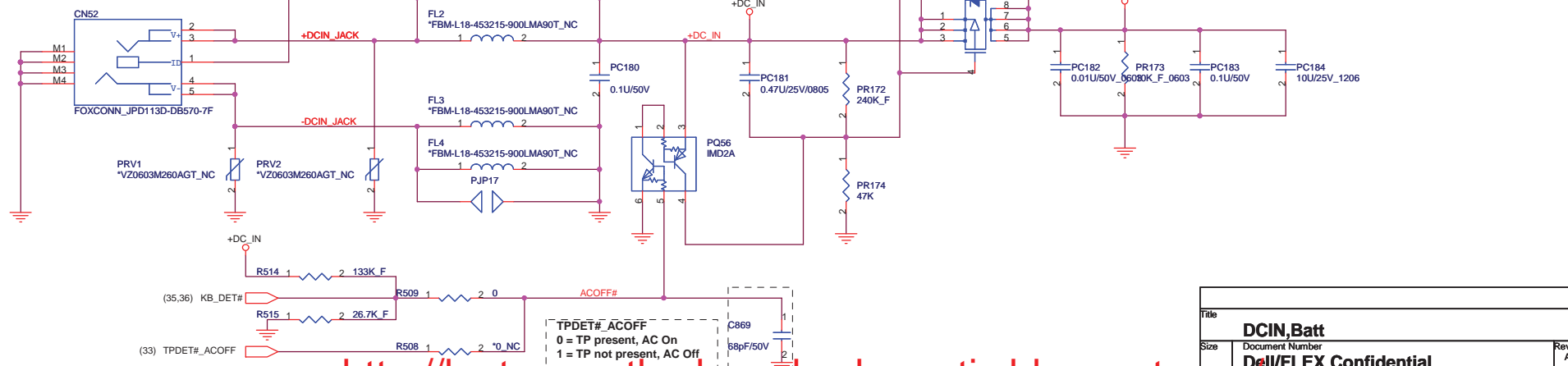
Title		
1.1V_SUS/1.8V_RUN		
Size	Document Number	Rev
	Dell Confidential	A00
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Battery Conn (030 Level)

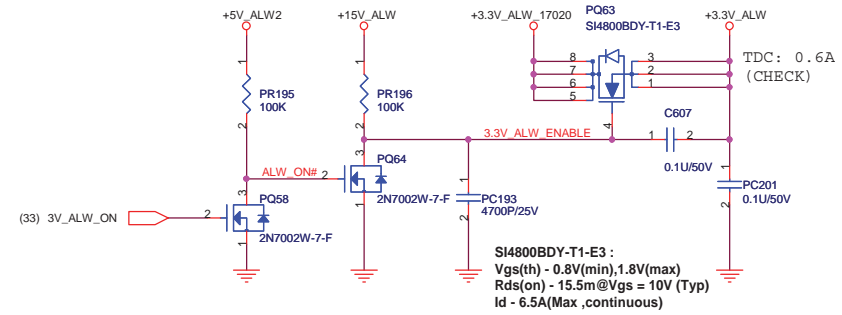
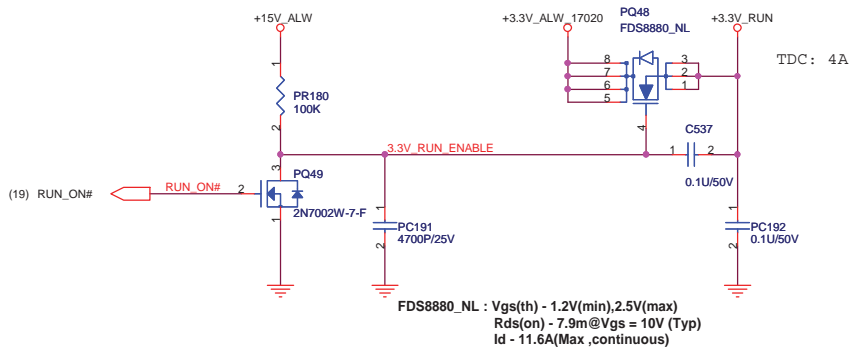
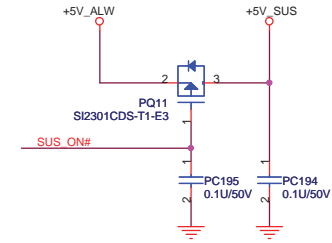
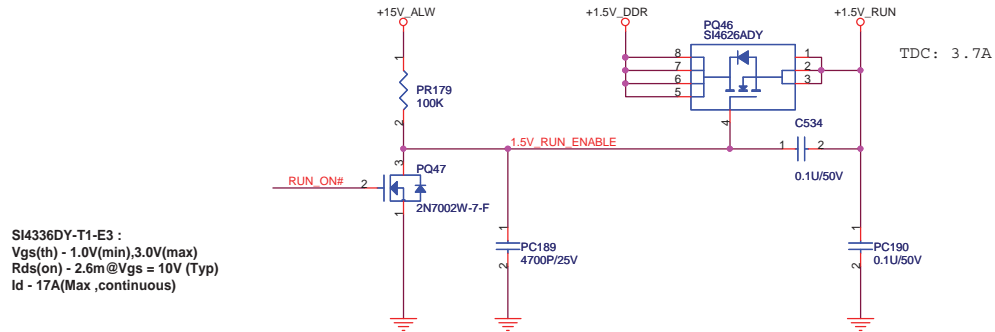
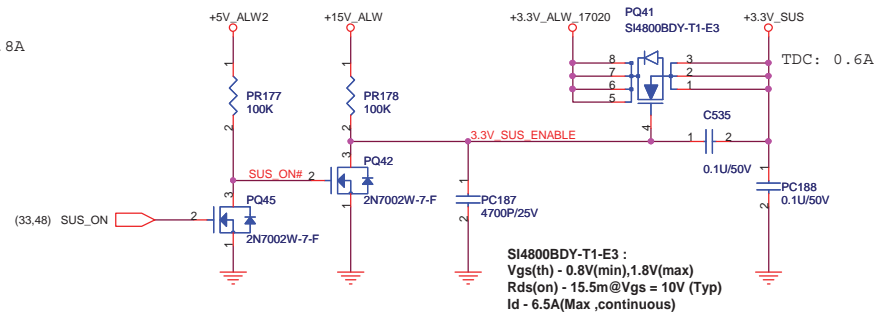
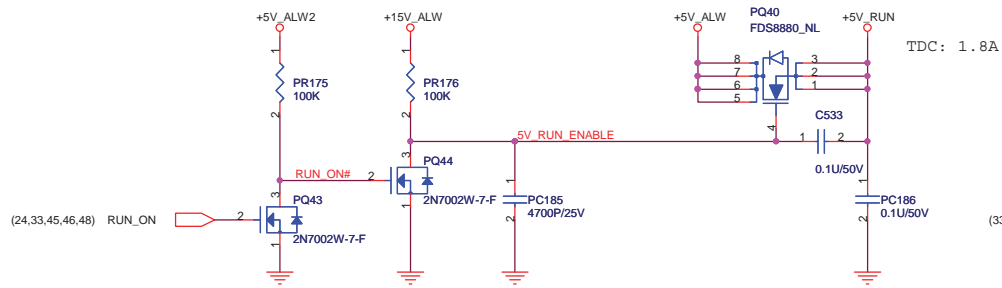


DC Jack (030 Level)

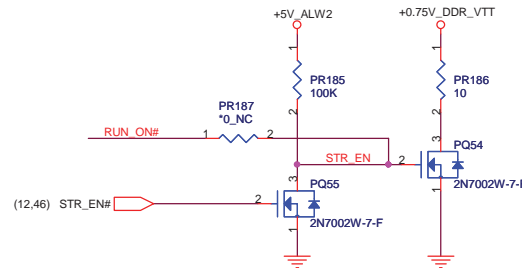
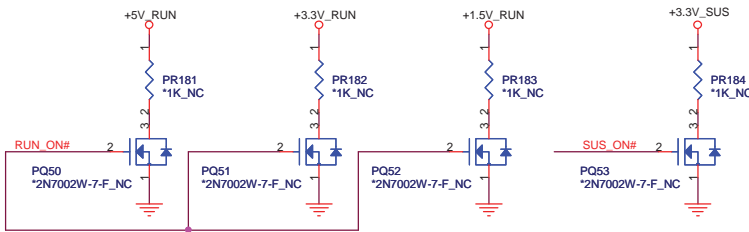


Title			DCIN_Batt
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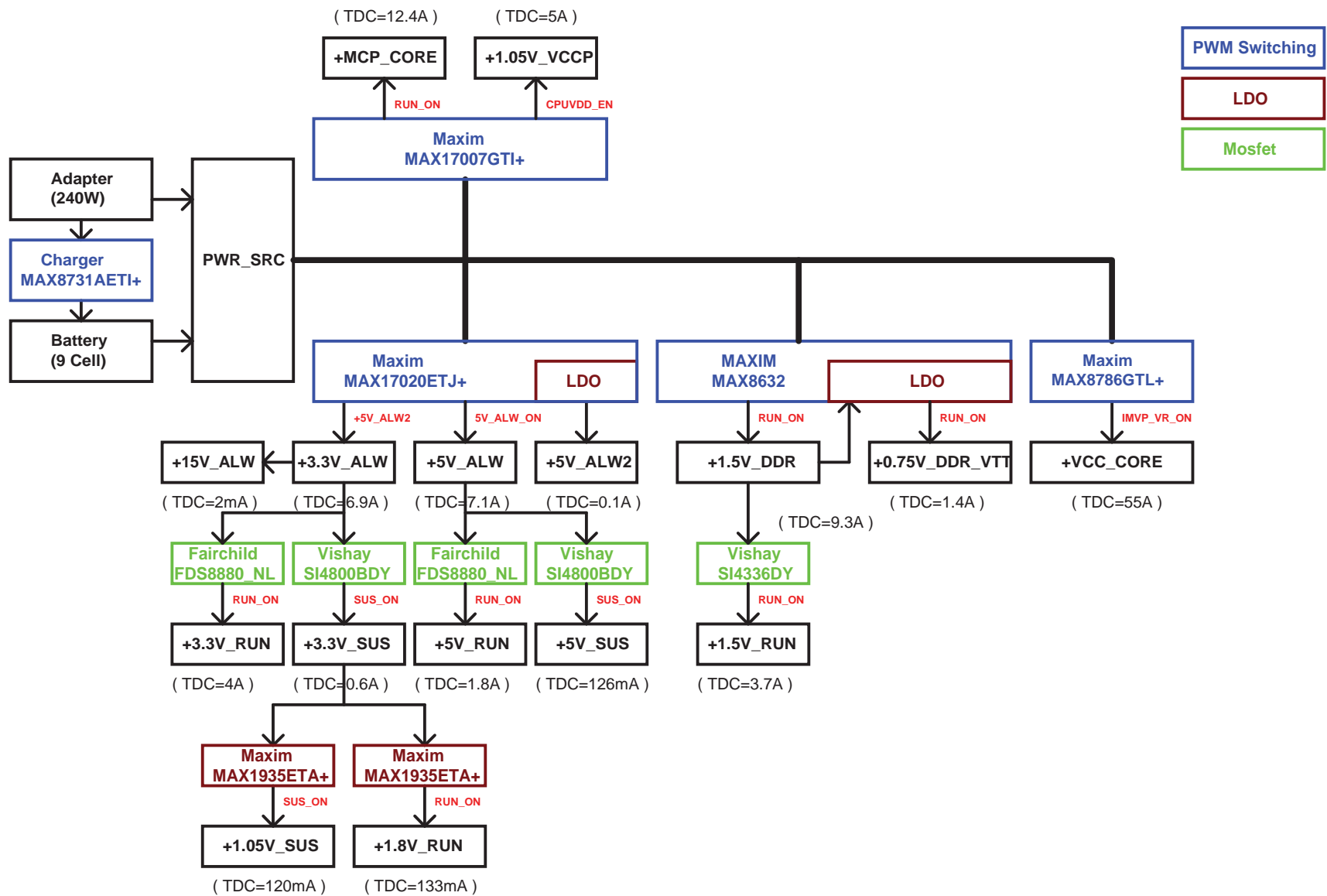
<http://laptop-motherboard-schematic.blogspot.com/>



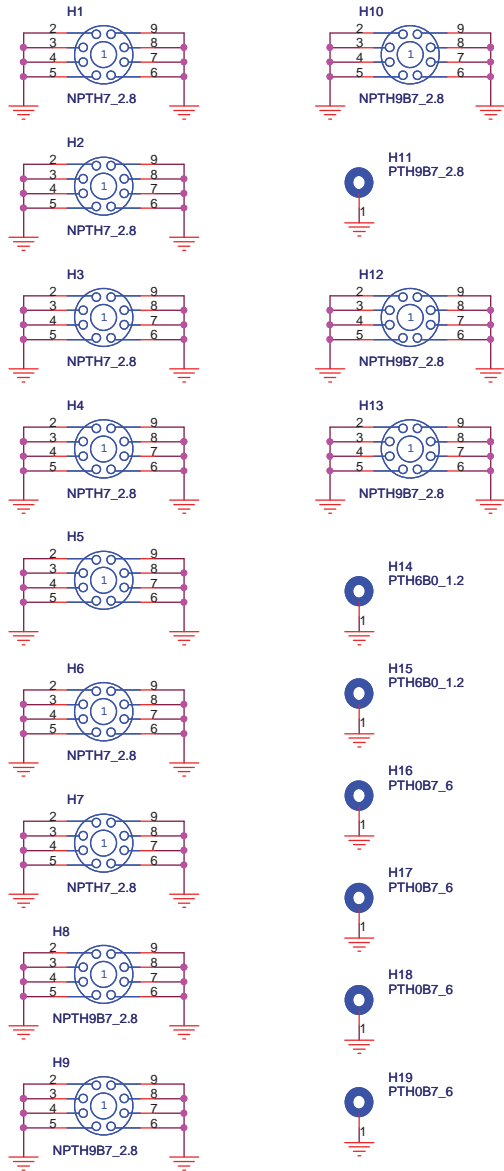
Reserve discharge path



Title		
RUN POWER SW		
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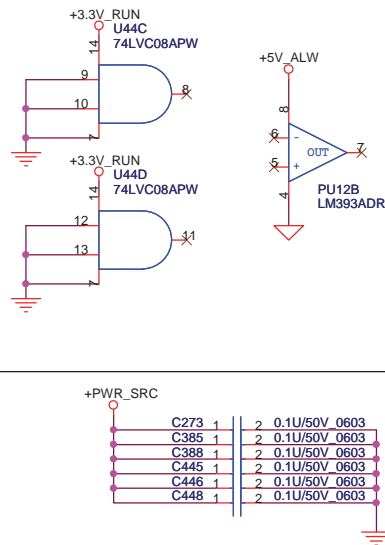
Screw Hole



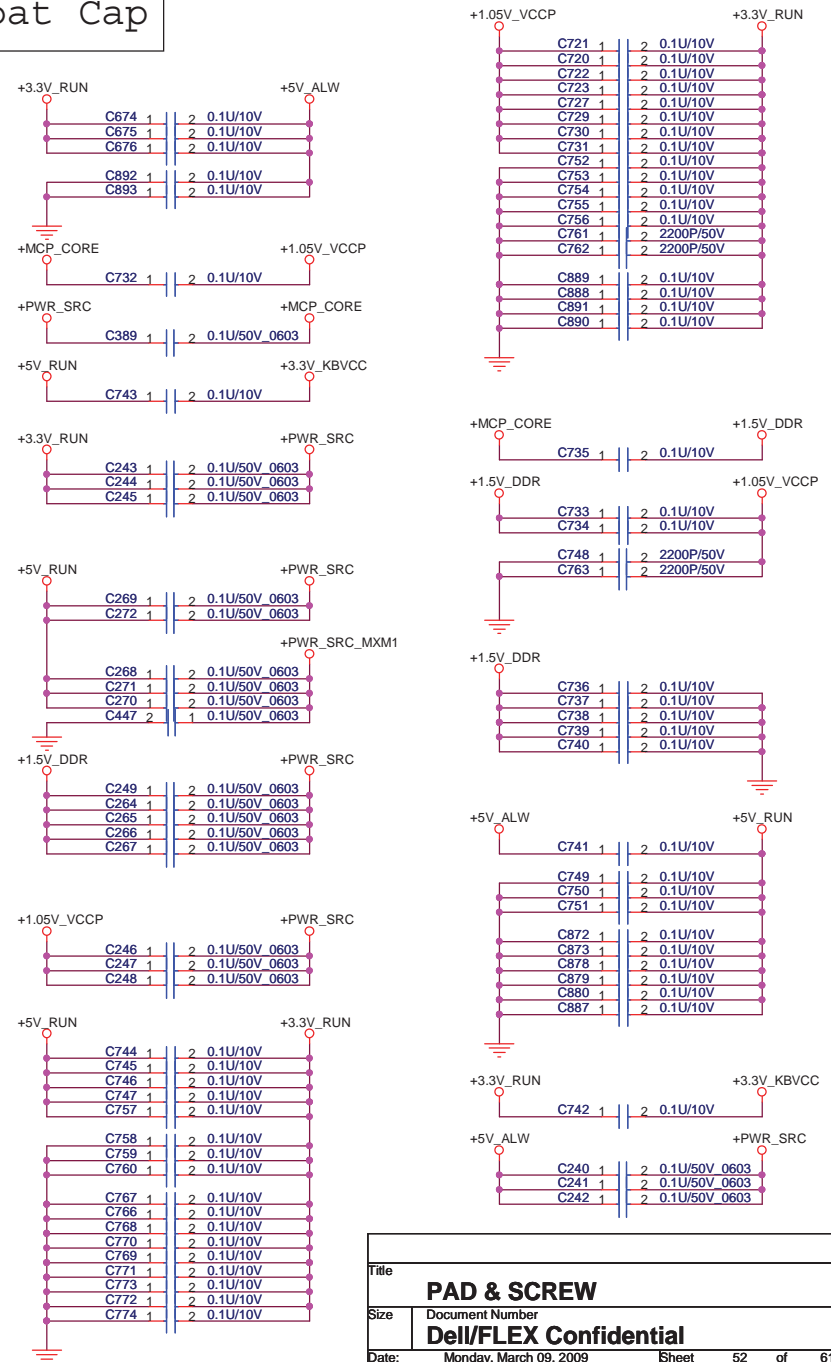
FID

- FID1 NC, NO CONNECT TO ANY.
- FID2 NC, NO CONNECT TO ANY.
- FID3 NC, NO CONNECT TO ANY.
- FID4 NC, NO CONNECT TO ANY.
- FID5 NC, NO CONNECT TO ANY.
- FID6 NC, NO CONNECT TO ANY.
- FID7 NC, NO CONNECT TO ANY.
- FID8 NC, NO CONNECT TO ANY.

Unused Gate

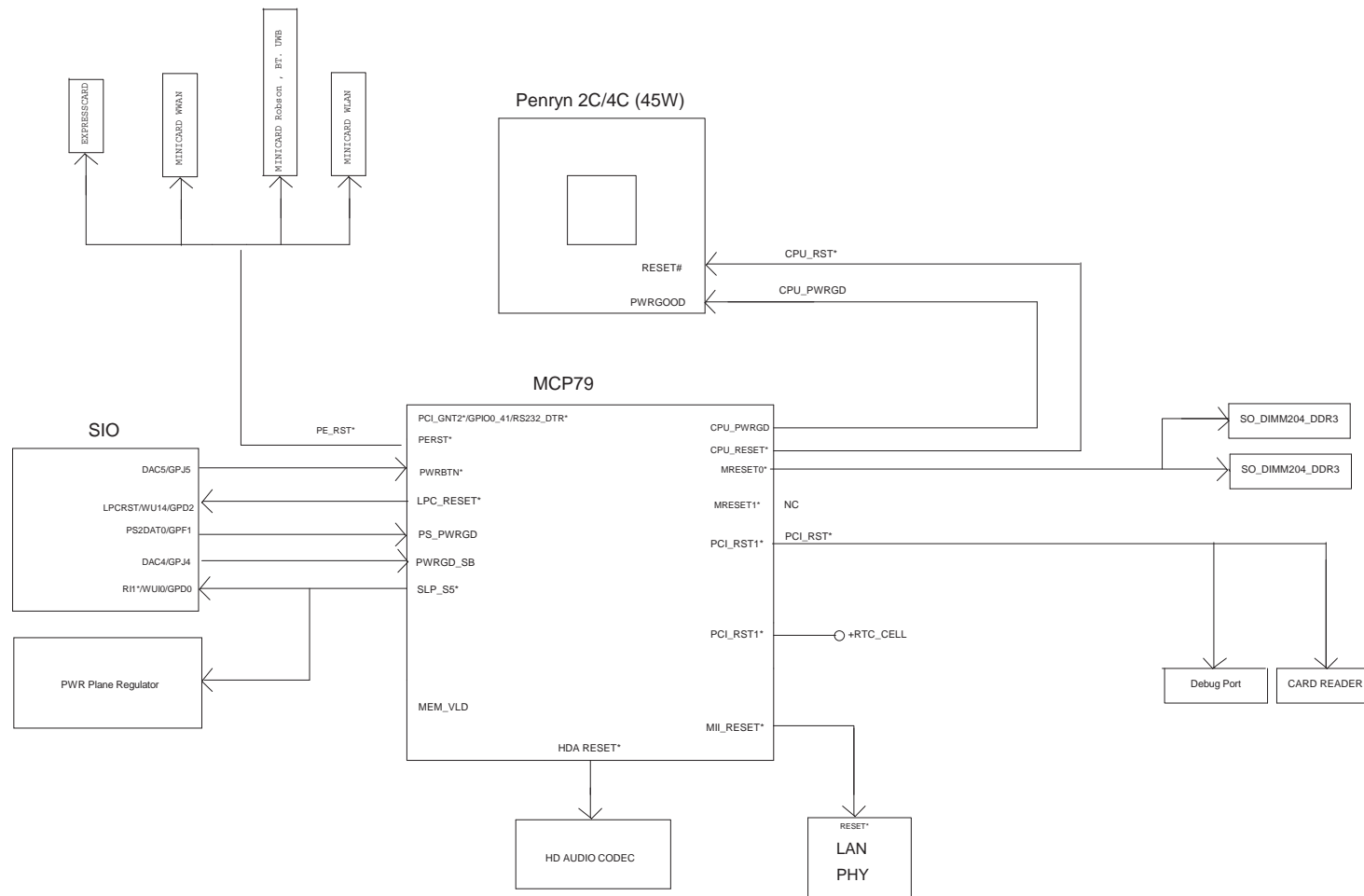


Moat Cap



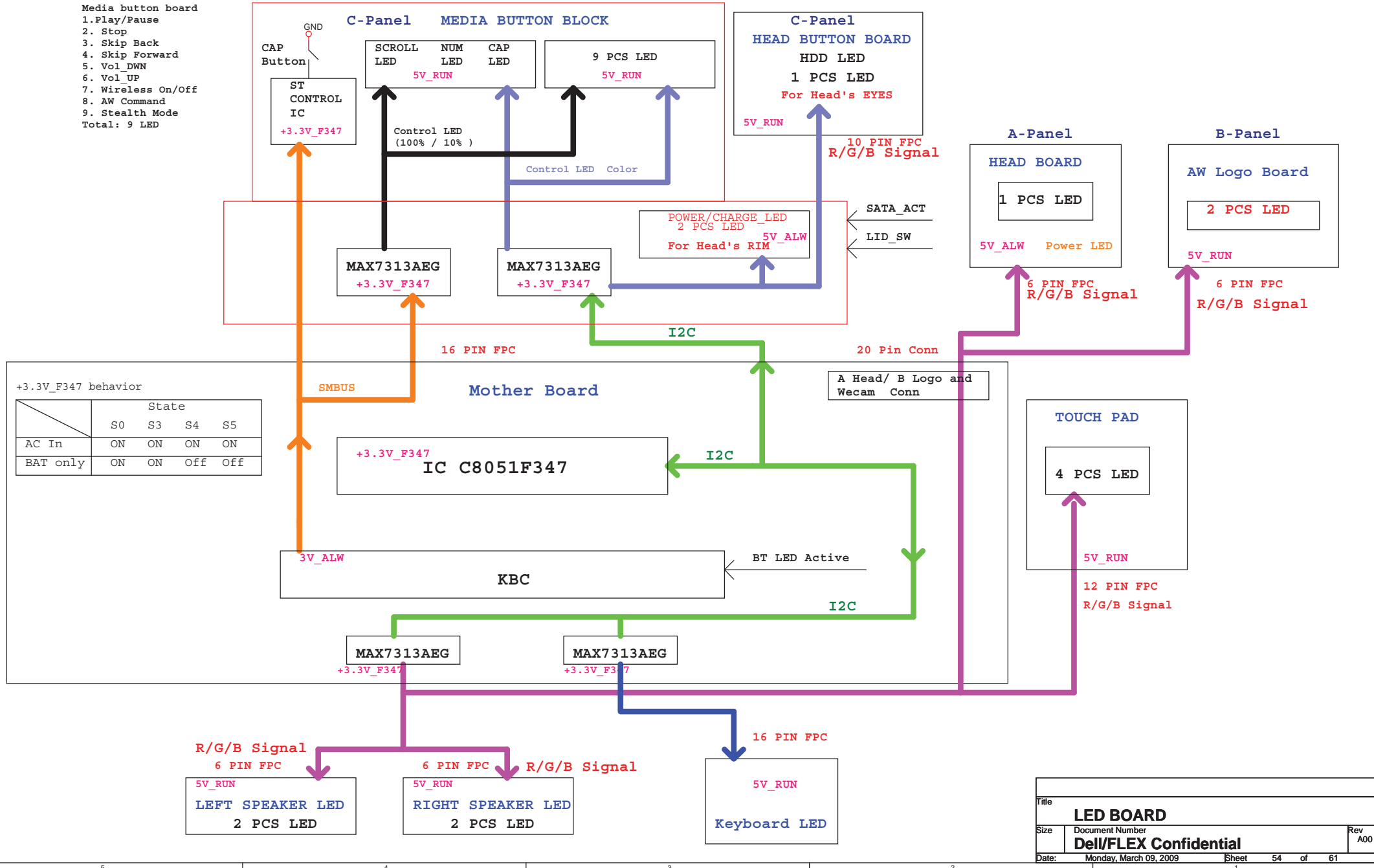
Title		
PAD & SCREW		
Size	Document Number	Rev
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RESET MAP



Title		PCI RESET MAP	
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- Media button board
1. Play/Pause
 2. Stop
 3. Skip Back
 4. Skip Forward
 5. Vol_DWN
 6. Vol_UP
 7. Wireless On/Off
 8. AW Command
 9. Stealth Mode
- Total: 9 LED



+3.3V_F347 behavior

	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

Title		
LED BOARD		
Size	Document Number	Rev
	Dell/FLEX Confidential	A00
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Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
1	EMI Modify Part of Bead		X00	44, 49	Modify Part of FL5, FL6, FL7, FL8 to BJ3216HS480NT.	X00	SSI
2	Modify Thermal sense Diode	To meet SMSC suggestion in Document AN1214.	X00	5, 6, 9, 32, 42, 49	Modify Q2, Q5, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q51, Q86, Q88, Q90, Q92, Q94, Q102, Q103, Q111, Q121, PQ37 to MMBT3904-7-F. (From MMST3904, also modify footprint)	X00	SSI
3	Modify ELC parts to NA.	To meet Dell circuit design requirement.	X00	36	1. Modify R637, R638, R639, R640, R641 to NA. 2. Modify Q50, R373, R372, R528, R529, C532, C542, C543, U118 to NA. 3. Modify U45 pin24, R635 pin2, R647 pin2 to +3.3V_ALW. 4. Modify U45 pin22 to LED_CLK, U45 pin23 to LED_DATA. 5. Add CN27 (4 pin debug header)	X00	SSI
4	Modify Footprint of Mini Card.	To separate Wini-lock& Connector	X00	30, 31	Del CN18(MiniCard WLAN Connector)& CN19(MiniCard WWAN, BT, UWB Connector)& CN20(Flash Cache Module Connector) Pin M3,M4,M5,M6.	X00	SSI
5	Move DP AUX pull-up& down resistor.	Modify by NV recommend.	X00	27	Move R191,R200 to CN10(DP conn) side.(NV recommend)	X00	SSI
6	Add LVDS DDC selection pull-up.	Add by NV recommend.	X00	26	Add R520 on U124 pin 1 and pull up to +3.3V_RUN	X00	SSI
7	Separate Head LED power	To meet Dell circuit design requirement.	X00	24	Modify CN62(CAM/ Head/ Logo Conn) pin11 to +5V_ALW& add C627 decoupling cap	X00	SSI
8	Fine tune MCP power trace.	To increase MCP power trace	X00	7, 9, 10, 13, 14, 15	1. Modify L1 pin1, L2 pin1, L3 pin2, L10 pin1 to +1.05V_VCCP. 2. DEL C427, C57, C62, C121, C122, C432, C174, C311, C217, C204, C214	X00	SSI
9	Modify ELC circuit design	To meet Dell circuit design requirement.	X00	36	1. Modify TP_LED_R_DRV#, TP_LED_G_DRV#, TP_LED_B_DRV# from U43 pin17, 18, 19 to U45 pin17, 18, 19. 2. Modify U51 pin 16 to +5V_ALW, U45 pin 1& 16 to +3.3V_ALW. 3. Modify U45 pin 22& 23 to LED_CLK& LED_DATA.	X00	SSI
10	Modify +1.5V_DDR power sequence	To meet NV power sequence recommend.	X00	46	1. Modify PR95& PR98 to connect "STBY". Also modify PR99 to "SHDN". 2. Modify PR100 to connect "+5V_ALW".	X00	SSI
11	Remove Hardware Total Power control	To solve CPU CLKSTP can't work issue.	X00	7	1. Remove R513 2. Add "H_CLKSTP" to connect MCP79& CPU directly.	X00	SSI
12	Modify Gating parts to NA.	Didn't use these Gating circuit but reserve all of these parts for MXM power gating.	X00	19, 21	Modify Q13, Q15, Q16, Q17, Q36, Q38, Q39, Q40, R189, R190, R248, R249, C310, C312, C313, C324, C326, C333, C334, C365, C366, C367, C368 and C369 to NA.	X00	SSI
13	Update all of connector lists	Update all of connector modification by M.E..	X00	24, 25, 29, 31, 35, 49	Modify footprint of CN7, CN8, CN14, CN16, CN17, CN23, CN52, CN57 and CN62.	X00	SSI
14	Add Moat capacity	Add Moat capacity by EMI request	X00	52	Add C761, C762& C763 Moat capacity by EMI request.	X00	SSI
15	Backlite final-tune.	Add reserve resistor for backlite final-tune.	X00	24	Add R520& R631 (0ohm_0603) for Backlite final-tune.	X00	SSI
16	WebCam DGND	WebCam DGND connect GND directly.	X00	24	Delete C673 to connect GND directly.	X00	SSI
17	Verify BIOS debug pin	Add test pad on Mini card pin 16, 17, 19.	X00	30	Add T29, T31, T32 on CN18 pin 16, 17, 19.	X00	SSI

Title			LED BOARD		
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Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
18	Add 100pF cap near by SIM con.	Verify SIM card DATA& Reset lines.	X00	31	Add C628& C629 to NA and near by CN23.	X00	SSI
19	Connect +V_TV_DAC to GND	Follow NV design guideline	X00	11	Delete R452 and connect it directly to GND.	X00	SSI
20	Modify ELC circuit	To meet Dell circuit design requirement.	X00	36	U42 changes: 1. Change VBUS(pin 8) power to +5V_SUS 2. Change REGIN(pin 7), R632 and R636 pullup to +3.3V_F347. You could use the Q50 circuit for this. 3. Generate +3.3V_F347 from +3V_ALW and control the power state by SUS_ON and ACIN. We need this power to be ON during S0/S3/S4/S5 when on AC. On Battery this power is available only in S3. 4. Connect U40 power to +3.3V_F347 power. 5. Remove all the RGB_OVERRIDE# circuit. 6. Connect LID_SW# to U42 (similar to KB_DET#_R FET circuit) 7. Connect a new GPIO LOW_BATTERY from EC to U42 GPIO. U51: Remove I2C/SMBDAT2 MUX switch. Not required as per new requirement from AlienFX. U43: Change the power to this part to +3.3V_F347 U45 Changes: 1. Change the power to this part to +3.3V_F347 2. Change SCL and SDA connection to I2C_CLK_R, I2C_DAT_R. Change R264, R262, R596 power to +3.3V_F347. Add LID_SW# circuit.	X00	SSI
21	Modify ELC circuit	To meet Dell circuit design requirement.	X00	35	Add R655, Q116, Q117, Q118, Q119 for TP_LED_DRV disable.	X00	SSI
22	Add HDD Power Bulk Capacity	To meet Dell circuit design requirement.	X00	35	Add C630 for HDD 3V power Bulk cap	X00	SSI
23	Improve thermal trip sequence	EMC4002 thermal trip sequence	X00	32	Add C631 for EMC4002 thermal trip sequence.	X00	SSI
24	Add Jumper near by DC Jack	Add Jumper for EMI parts reserve	X00	49	Add PJP12& PJP17 for EMI parts reserve.	X00	SSI
25	Delete S5, S3 pull-high resistor.	Delete EC S5, S3 PH resistor by NV recommend.	X00	33	Delete R380& R383 by NV recommend	X00	SSI
26	Add +5V_SUS gating circuit.	Add +5V_SUS gating circuit for ELC circuit	X00	50	Add PQ11, PC194, PC195 for ELC circuit.	X00	SSI
27	Remove power source cap	Remove it due to space issue.	X00	44	Remove PC31 due to space issue.	X00	SSI
28	Add EMI's modification.	Add EMI's modification.	X00	44	Page11: 1. R75 change from 0ohm to 22ohm. 2. Add 22ohm resistor*4pcs to Net RGMII_TXD0 ,RGMII_TXD1, RGMII_TXD2,RGMII_TXD3(close to MCP79SLI). Page 14: 1. C177,C173 change from 10pf to 22pf 2. R126,R257 change 0ohm to 22ohm Page24: 1. Mount C568,C569. 2. Modify R415,R416 to L63, L64. 3. Add 0.1uf caps between +5V_RUN and Gnd(close to CN7) for 1 EA (C633) 4. Add 0.1uf caps between +GFX_PWR_SRC and Gnd (close to CN7) for 2 EA (C635, C636) Page28: 1. Mount L27, L28, L46 and leave R300, R301, R302, R304, R394, R395 empty 2. Mount ESD2,ESD3,ESD5. Page 35: 1. Mount CP1,CP2,CP3,CP4,CP5,CP6.	X00	SSI
2. Add 100pf caps*3pcs to Net RSPK_LED_B_DRV# ,RSPK_LED_G_DRV#, RSPK_LED_R_DRV# to GND (close to CN6). (C638, C639, C641) Page 40: 1. Resved a Crystal 25MHz to Lan chip(close to U33) (Y3, C204, C214) 2. C136, C695 change from N/A to 22pf 3. R538, R541 change from 0ohm to 22ohm 4. Add 100pf caps* 3pcs to Net SPD10LDE, SPD100LED, PHY-ACTLED to GND. (C644, C645, C646) 5. Add 0.1uf caps between +3.3PHY and GND for 2 EA. (C764, C765) Page44: Mount PC67, PC76, PC60, R61,PR155,PR156 also change to 0 ohm. Page52: Add 0.1uf caps between 3.3V_RUN and GND for 9 EA. (C766, C767, C768, C769, C770, C771, C772 , C773, C774)							

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29	Modify 0603 resistor to JP	Mini-card power consumption more than R327 absorb.	X00	30	Delete R327 and Add JP4 to instead.	X00	SSI
30	Add 3 caps near by Vcore choke	To reduce AC droop	X00	44	Add PC155, PC161, PC163 parallel with PC78, PC65, PC61.	X00	SSI
31	Leave Power resisotr empty	Leave PR41 empty for line load modify	X00	44	Leave PR41 to empty.	X00	SSI
32	Add dampning resistor	Add dampning resistor by Ricoh recommend to final-tune media card signal.	X00	39	Add R504, R505, R534, R535, R638, R656, R657 ,R658 to final-tune Media card signal.	X00	SSI
33	Add PH resistor on display MUX	Add Pull-high resistor by TI recommend.	X00	39	Add R659, R155, R660, R56, R661, R662 pull-high resisotr by TI recommend.	X00	SSI
34	Add TPM circuit	Add TPM circuit by Dell requirement	X00	34	Add U145, R66, R69, R70, R72, R120, R415, RJ5, RJ6, C647, C648, C650, C650, C652, C653 for TPM circuit	X00	SSI
35	Change the MUX source for support Hybrid function	SN74LVC1G3157DCKR repair easier & lower cost than FUSB20.	X00	26	Change MUX source from FUSB20 (10pins) to SN74LVC1G3157DCKR(6pins). The SN74LVC1G3157DCKR amount need double. U120=> U120 & U132 (MXM/MCP LVDS DDC MUX) U121=> U121 & U134 (MXM/MCP VGA DDC MUX) U122=> U122 & U136 (MCP AUX/DDC MUX) U123=> U123 & U138 (MXM/MCP DP AUX MUX) U119=> U119 & U144 (MXM DP AUX/DDC MUX) U126=> U126 & U143 (MXM/MCP HDMI DDC MUX) U124=> U124 & U140 (MCP MEM& LVDS SMBus MUX)	X00	SSI
36	Add test-PAD	Add test-PAD for NV software debug.	X00	12	Add test-PAD on "PCI_REQ2, MXM1_PWR_EN, WLAN_RADIO_DIS#, WLAN_PCIE_RST#, WPAN_PCIE_RST#, WWAN_PCIE_RST#".	X00	SSI
37	Update EMI solution	Update EMI solution	X00	12	Page 29: Add 0.1uF cap between +5V_HDD& GND for 5 EA. (C660, C661, C662, C664, C667). Page 33: 1. R387 change from 0ohm to 22ohm 2. R396 change from N/A to 0ohm 3. C550 change from N/A to 10pf Page 41: Add 0.1uF between GND_LAN& GND and leave empty.	X00	SSI
38	Add Jumper& Modify power plante	Add Jumper& Modify power plante for MXM1 power measurement.	X00	19, 52	1. Add JP20& create +PWR_SRC_MXM1 power. 2. Modify power plante of C315, C316, C317, C318, C319, C320, C268, C270, C271, C447 to +PWR_SRC_MXM1.	X00	SSI
39	Add +5V_RUN_BLOGO power gating	Add +5V_RUN_BLOGO power gating by Dell ELC request.	X00	24	Add Q72, Q123, R96, R327 to gating +5V_RUN and create +5V_RUN_BLOGO power.	X00	SSI
40	Add stitch cap	Add stitch cap between +1.05V_VCCP& GND	X00	10	Add C121, C122 stitch cap fbetween +1.05V_VCCP and GND.	X00	SSI
41	Modify resistor value. (BOM)	Modify the value to meet PCI-E high swing function.	X01	20, 22	Modify R518& R600 to 0 ohm to meet PCI-E high swing function. (MXM card internal pull-high for 10Kohm)	X01	PT
42	eSATA re-drive IC setting	Add components for eSATA re-drive setting	X01	28	Add R663& R664 for eSATA future setting use	X01	PT
43	Revise EC control pin	Remove reserve circuit after double confirm with intel.	X01	5, 6	Page5: Remove R87, Page 6: Remove R689, R690, C798, Q120& Q121 to remove Quad core detect circuit. Page 33: Modify U15 pin 98 to "FUSB31_ON#"& pin 99 to "MXM2_PRESENT#".	X01	PT

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44	Fine tune 1394 signal (BOM)	Fine tune 1394 signal	X01	39	Modify R465, R466, R467& R468 to 54.9ohm.	X01	PT
45	Add Mini-Card card detect resistor	Add pull-high restor for Mini-Card detect	X01	30, 31	Add R380, R383, R402, R416& R452 for Mini-card detect level.	X01	PT
46	Add CAM power control circuit	Driver of CAM can't shut power down	X01	24, 36	Page 24: Add Q73, C668, C311. Page 30: Add R687 pull-high resistor& U41 pin20 for "CAM_PWR_ON"	X01	PT
47	Modify Media Card signal damping resistor. (BOM)	Modify Media Card signal damping resistor for EMI signal fine-tune	X01	39	Modify R504, R505, R534, R535, R638, R656, R657, R658& R482 to 27ohm for EMI signal fine-tune.	X01	PT
48	Imporve X'tal timing. (BOM)	To improve X'tal timing by Vendor suggestion.	X01	14, 33, 34	Modify C185, C186, C551& C552 to 15pF and modify C597& C598 to 20pF	X01	PT
49	Fine tune MXM sequence (BOM)	Fine tune MXM power sequence for reliability	X01	32, 42	P32: Delete R223, R224, R530& R374 and Add R607, R608, R487, R488, C794& C795 then connect to "MXM1_35VOK" P42: Modify R567 to 20Kohm and add C775 to GND.	X01	PT
50	Fine tune Media Card signal	Fine tune Media Card signal for EMI& reliability	X01	39	Add R689, R690, R693& R694 (27ohm) for Media Card signal fine tune.	X01	PT
51	For "PE0_PRNT16#" It need a SW control (MXM_ON#).	When "Hybrid" enabled and MXM_ON# assert to low, 2 of MXM cards PCIECLK will be active.(NV suggest)	X01	10	Stuff R78 and Unstuff R67& R424	X01	PT
52	For GPIO_47 it need to connect "MXM1_PRESENT#"	SBIOS used GPIO_47 to do a judgment whether MXM cards on board.(NV suggestion)	X01	10	Add R141	X01	PT
53	Unstuff DP HPD 100K pull low resistors.	MXM card has internal pull low.Follow MXM3.0 Design guideline.	X01	10, 27	Unstuff R503& R513	X01	PT
54	V_RGB_DAC can be shorted to GND if RGB interface is not used.	Follow MCP79 checklist v08	X01	11	Unstuff L6, C138& C139. Del C137 and Add R87	X01	PT
55	Follow MXM design guideline sequece	Follow MXM design guideline sequece.	X01	19, 21	Modify CN4& CN5 pin278, 280 to +3.3V_RUN. Change C327, C328, C329& C359 pin1 from +3.3V_MXM1(+3.3V_MXM2) to +3.3V_RUN. Modify CN4& CN5 pin1, 3, 5, 7, 9 to +5V_RUN. Change C829, C321, C322, C855, C325, C323, C830, C665, C654, C858, C666& C657 pin1 from +5V_MXM1(+5V_MXM2) to +5V_RUN. Add JP22 to connect +3.3V_MXM1& +3.3V_MXM2.	X01	PT
56	Fix MXM card leakage issue	Add gating circuit to fix leakage issue	X01	19, 20, 22	DEL +3.3V_RUN_HYBRID circuit. (R214,Q78,Q80,R402,C613,Q79,C614,C377) Change +3.3V_RUN_HYBRID power to +3.3V_MXM1(+3.3V_MXM2) . Stuff Q12, R185, Q14, R186, Q104, R500, Q105& R501 Unstuff R201, R582, R639& R640 Stuff Q81, R498, Q82, R499, Q20, R196, Q21& R197 Add D56& D57 Unstuff R641, R652, R653& R654	X01	PT
57	Reserve cap to fine tune sequence	Reserve cap to fine tune PWR_EN sequence	X01	20, 22	Reserve 0.1uf (Unstuff) C766& C777	X01	PT
58	Fix TMDS251 leakage issue	Plug external HDMI device will cause system leakage from TMDS251 vcc pin.	X01	19, 23	Add Q76,C377,C614,C613,C377 and Add net +3.3V_MXM1_HDMI.	X01	PT
59	Update EMI solution of X01 (BOM)	Update EMI solution of X01	X01	40	Modify R683, R684, R685, R686 to 22ohm.	X01	PT

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60	Let KBC can judge 2'nd MXM card plug in.	Connect MXM2_PRESENT2# to KBC.Let KBC can judge 2'nd MXM card plug in.	X01	33	MXM2_PRESENT2# connect to U15 pin 99.	X01	PT
61	Fix press 4 second shutdown leakage issue.	Crt_Ddc_Sel (GPIO36), Dp_Sel(GPIO4), Lvds_Sel(GPIO 20), Lvds_Ddc_Sel(GPIO 21), Lvds_Mem_Ddc_Sel (GPIO6), HDMI_DDC_Sel(GPIO5) active high after press 4 second shutdown then cause leakage to +3V_RUN.	X01	23, 26	Add pull high resistors & diodes. R695, R696, R697, R698, R699, D44, D47, D48, D54, D49& D55	X01	PT
62	Delay MXM1_35VOK sequence (BOM)	Delay MXM1_35VOK sequence to control MXM thermaltrip gating.	X01	42	Add C775 Change R567 to 20K	X01	PT
63	Delete HDMI pass resistor	Remove them to improve HDMI signal	X01	23	Remove R485, R486, R487, R488, R489, R490, R491, R492, R493, R607& R608.	X01	PT
64	Add cap near by Media card controller	Add cap to improve Media card signal	X01	39	Add C217, C778, C779, C780, C781, C782, C785, C786, C787, C788, C789, C790, C791& C792	X01	PT
65	Meet SMSC EMC4002 circuit design (BOM)	Add circuit to meet SMSC suggest, also keep Dell request.	X01	32, 47	Modify R218 to 4.7K ohm and pull-high power to +3.3V_SUS Add Q78, Q79, R224& R490.	X01	PT
66	Add Dampning resistor	Add 22 ohm resistor to improve CRT signal	X01	25	Add R374& R485	X01	PT
67	Fix Keyboard LED wrong color	In order to correct keyboard LED display	X01	37	Swap CN57 pin 3, 4 pin define from R to G & G to R.	X01	PT
68	Follow NV designguide (BOM)	Modify schematic to meet NV design guideline	X01	9, 10, 11, 13, 14, 15	Modify C115, C123, C131, C161, C164, C191, C196& C198 to 2.2uF. Unstuff R100 Modify R145, R146, R211& R244 to 2.2Kohm. Modify C116 to 2.2uF. Add C65, C174& C793	X01	PT
69	Update EMI solution of X01	Update EMI solution of X01	X01	11, 19, 24, 28, 32, 35, 39, 40, 47, 49, 52	Unstuff R82, R469, R470, R471, R474, R541& C136 Stuff C204, C214, C835, C836, C837, C838, L39, L40& Y3. Add C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C824, C825, C864, C865, C866, C867, C869, C870, C871, C872, C873, C874, C878, C879, C880, C887, C888, C889, C890, C891, C892, C893. Move C677, C678, C679, C680, C681, C682, C683& C684 to near by CN63. Delete R549 and Add C894.	X01	PT
71	Power VDS derating modify	To meet Power VDS derating specification	X01	45, 46, 47	Stuff PR65, PR96, PR119, PR122& PC90. Stuff PC118, PC136& PC137 and modify them to 1000pF	X01	PT
72	Improve AC-in Detect function	Due to MXM had internal pull-high at AC-in signal cause AC-in detection fail	X01	19	Add R491& Q120 and R502 to 100Kohm	X01	PT
73	Update eSATA re-drive& FSUSB31K8X IC setting (BOM)	Due to eSATA re-drive IC set to increase signal stress cause signal failure and FSUSB31K8X setting.	X01	28	Stuff R663& R664 and Unstuff R618& R619 for eSATA re-drive IC. Stuff R489 for FSUSB31K8X.	X01	PT
74	Reserve SIM card connector and stuff components to test FCM mini card connector (BOM)	In order to prepare reserve CN19 so stuff all of components for FCM and reserve SIM card connector	X01	31	Unstuff CN23, C523, C524, C525, C526, C527& ESD4. Stuff R333, R334, R335, R336, R337 R338, R339, R349, R351, R353& R355.	X01	PT

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75	Fine tune PCI clock (BOM)	Due to PCI clock fail of EA test report.	X01	12	Stuff C151 and modify to 15pF	X01	PT
76	Reserve unused MXM2 power sequence control circuit (BOM)	Reserve unused MXM2 power sequence control circuit	X01	42	Unstuff C724, C725, C726, C728, D45, D46, R611, R612, R613, R642, R643, R644, R645, Q100, Q101, Q102& Q103.	X01	PT
77	CRT signal improvement (BOM)	To improve CRT signal	X01	25	Modify L56, L57& L58 to BLM18BB750SN1D	X01	PT
78	Turn off SUS power in DC mode	Turn off SUS power in DC mode to prevent leakage current	X01	32, 33, 42	Modify R205 pin 1 to +3.3V_SUS. Add R492 and unstuff. Modify U15 pin 85 to "RUNPWROK#" and delete R590& Q77.	X01	PT
79	MCP79 Vcore table modify	To meet NV MCP79 designguide - DG-03328-001_v12	X01	45	Modify PR83 to 200Kohm_F. Also modify MCP79 Vcore table.	X01	PT
80	DP HPD floating (BOM)	R513 avoid DP HPD floating	X02	27	Mount R513	X02	ST
81	DP power drop too big (BOM also)	Avoid DP power drop cause by D17.	X02	27	Add R549 (0ohm_0603) and leave D17 NC.	X02	ST
82	DP leakage current issue (BOM)	Avoid DP leakage current	X02	27	Modify D33 from BAV99-7-F to RB500V-40.	X02	ST
83	HDMI TV leakage issue	Fix HDMI TV plug -in leakage from TMDS251 to system.	X02	19	Add Q77 (2N7002) for dis-charge.	X02	ST
84	Meet new inductor's droop voltage (BOM)	Meet new inductor's droop voltage	X02	44	Modify PL2, PL3, PL4 to ETQP4LR36WFC. Modify PR40& PR59 to 5.63Kohm & 316Kohm.	X02	ST
85	Media Board sometimes fail (BOM)	Improve SM bus fan-out ability for Media board	X02	22, 33	Modify R196, R197, R273, R274 to 13Kohm	X02	ST
86	EMI solution in ST phase - 1. (BOM)	Add EMI solution	X02	28, 41	Add EMI2& EMI3. Mounted L32, L42, L43& L45 and remove R366, R371, R375, R381, R382, R411, R412& R414 by BOM change.	X02	ST
87	AMD MXM leakage current issue	Avoid AMD MXM leakage current	X02	20, 22	Add D60& D61 and Delete R640& R652.	X02	ST
88	SM bus equivalent parallel resistance low (BOM)	SM bus equivalent parallel resistance too low so increase the value of resistor	X02	23, 26	Modify R494, R495, R496, R497, R601& R604 to 10Kohm in page 23. Modify R147, R155, R156, R609, R610, R627, R659, R660, R661& R662 to 10Kohm in page 26.	X02	ST
89	eSATA output driving strength (BOM)	Improve eSATA output driving strength	X02	28	R618, R619 Mount and R663, R664 NA.	X02	ST
90	Fine tune +3.3V MXM1 power sequence (BOM)	Fine tune +3.3V MXM1 power sequence to close 3V of MXM card's power sequence	X02	28	C310,C312,C614 change to NA	X02	ST
91	Fine tune MXM card power enable sequence (BOM)	Fine tune MXM card power enable sequence make sure +3.3V_MXM1 power sequence to close 3V of MXM card's power sequence	X02	20, 22	R192,R256 change to 10Kohm C776,C777 Mount.	X02	ST
92	Follow TI vendor suggestion	To make sure the TMDS 251 power stable	X02	23	Add 10UF on +3.3V_MXM1_HDMI	X02	ST
93	Reserve unused power (Audio board)	Reserve unused power for Media card of Audio board	X02	39	Add 0ohm and leave empty.	X02	ST

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94	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence (BOM)	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence .	X02	19	Stuff R176& Unstuff R486	X02	ST
95	USB waveform fail	Improve USB waveform	X02	28	Stuff R394, R395& Unstuff L46, ESD5	X02	ST
96	VGA ACAVIN control (BOM)	Add VGA ACAVIN	X02	19	Add Q80 and connect to ADAPT_TRIP_SET. Modify R502 to 4.7Kohm.	X02	ST
97	3.3V OCP keeping re-try (BOM)	Make sure signal won't floating and keep original request	X02	47	Modify PR135 to 20K Add R590	X02	ST
98	EMI solution in ST phase - 2. (BOM)	Add EMI solution	X02	39	C792 change from 10pf to 15pf R482 change from 27ohm to 0ohm	X02	ST
99	Media Card signal waveform improve	Media Card signal waveform improve	X02	39	R118, R504, R505, R534, R535, R638, R656, R657, R658, R689, R690, R693& R694 change from 27ohm to 33ohm Unmoute C217, C778, C779, C780, C781, C782, C785, C786, C787, C788, C789, C790, C791& C792.	X02	ST
100	1.5V power regulator level modify (BOM)	Modify 1.5V power regulator level	A00	46	Modify PR221 to 80.6Kohm	A00	MP
101	Fix 1.5V power non-modification (BOM)	Fix 1.5V power non-modification	A00	46	PR214& PR221 un-stuff	A00	MP
102	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence (BOM)	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence .	A00	19	Unstuff R176& stuff R486	A00	MP
103	Fine tune MXM card power enable sequence (BOM)	Fine tune MXM card power enable sequence make sure +3.3V_MXM1 power sequence to close 3V of MXM card's power sequence	A00	20, 22	R192,R256 change to 0ohm C776,C777 Unstuff.	A00	MP
104	Modify Display Port HPD vlotage sense.	Modify Display Port HPD vlotage sense to meet NV checklist	A00	27	Modify R65 to 1Kohm	A00	MP

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