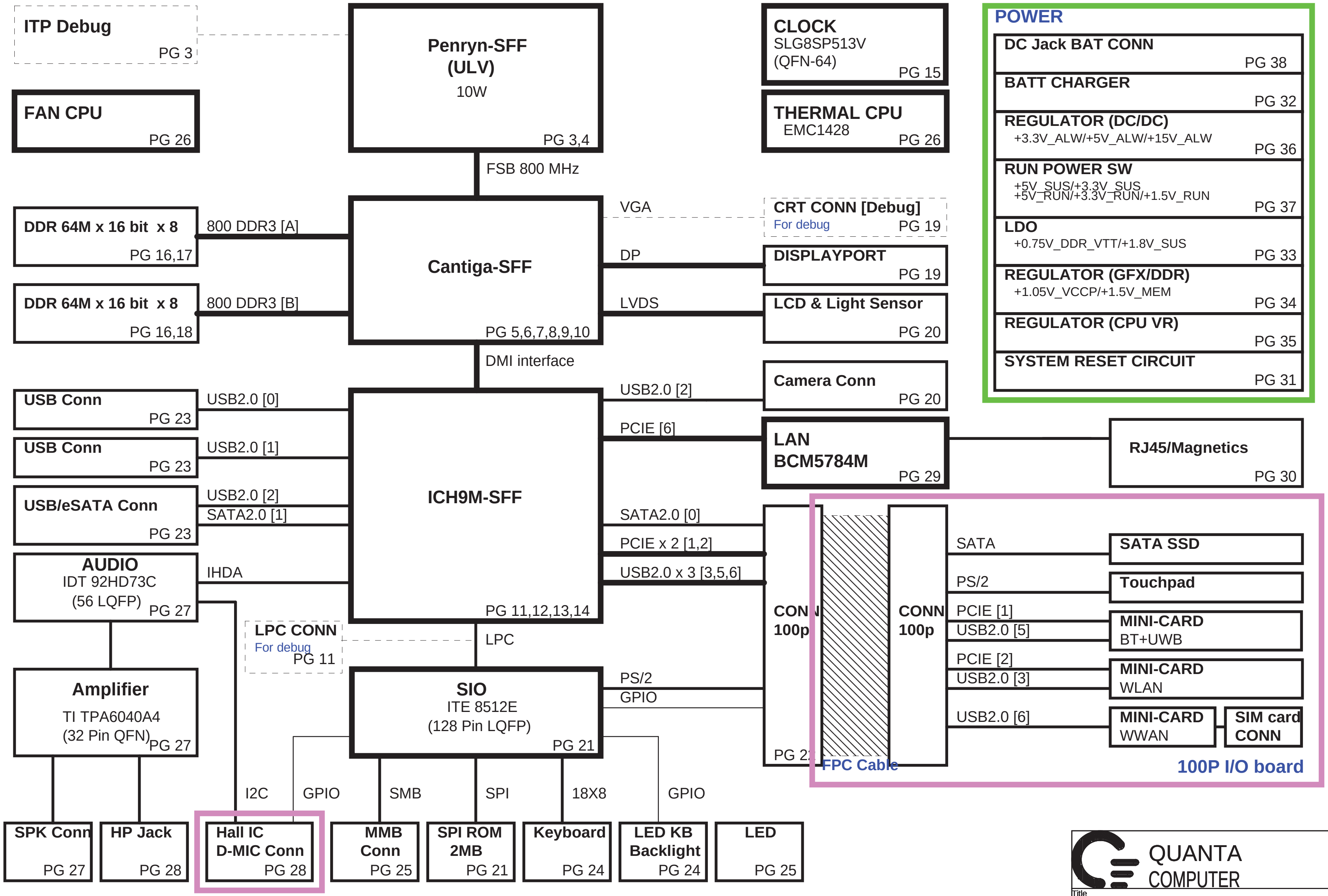
Adamo Montevina SFF Block Diagram

Rev: A00

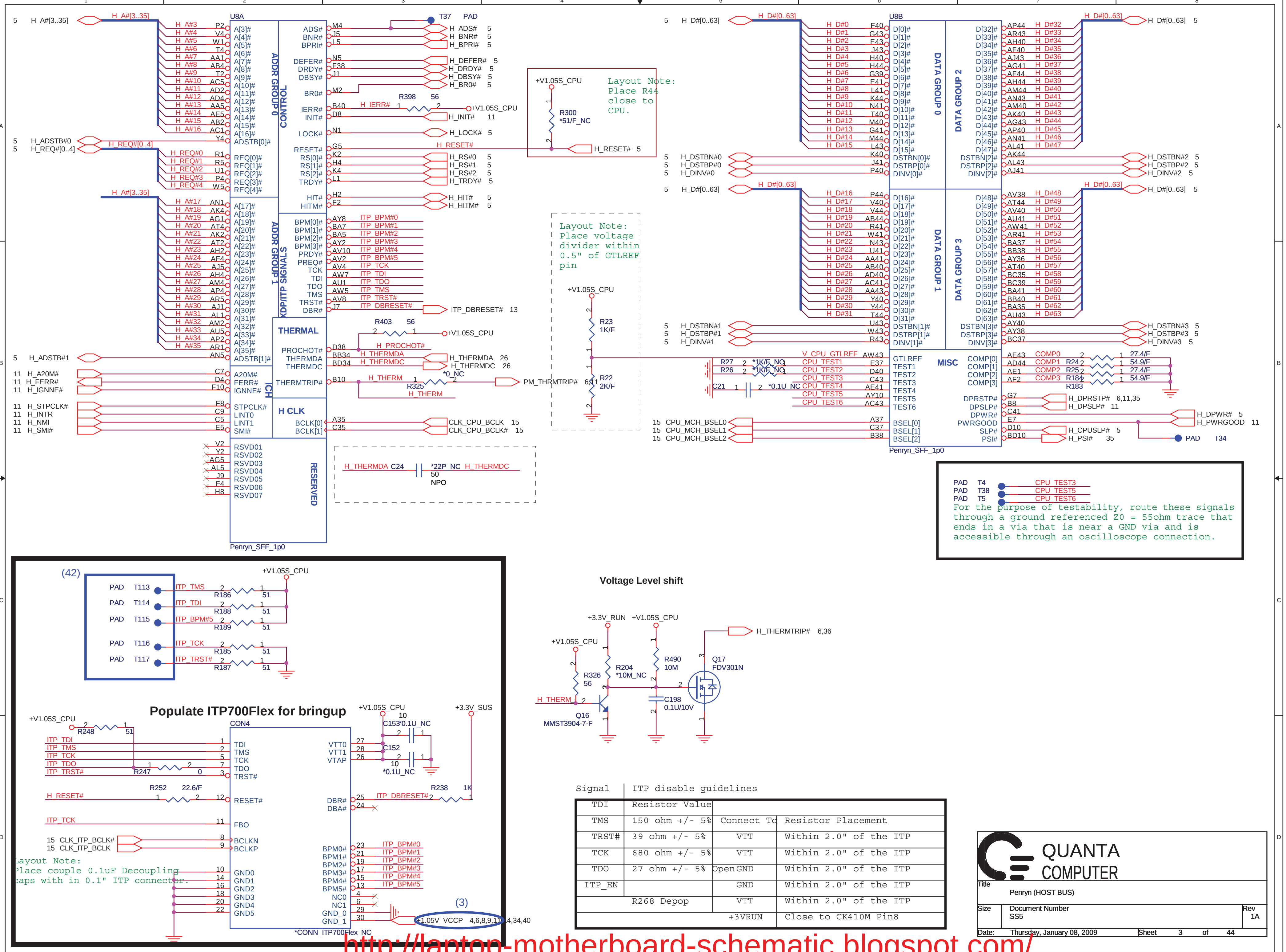


QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number SS5	Rev 1A
Date	Thursday, January 08, 2009	Sheet 1 of 44

QUANTA COMPUTER

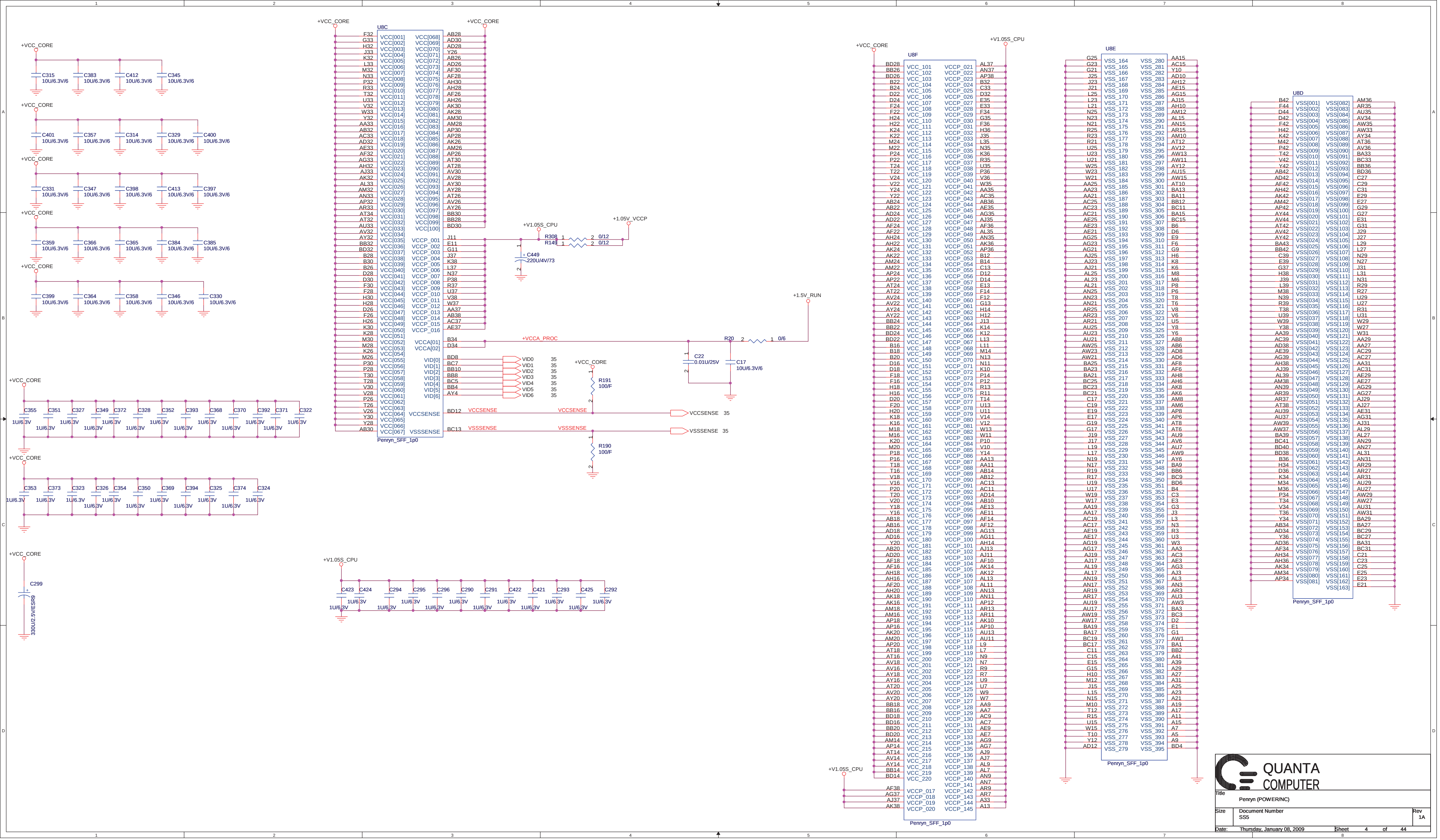
Title	Index & Power Status			
Size	Document Number SS5			Rev 1A
Date	Thursday, January 08, 2009	Sheet 2	of 44	

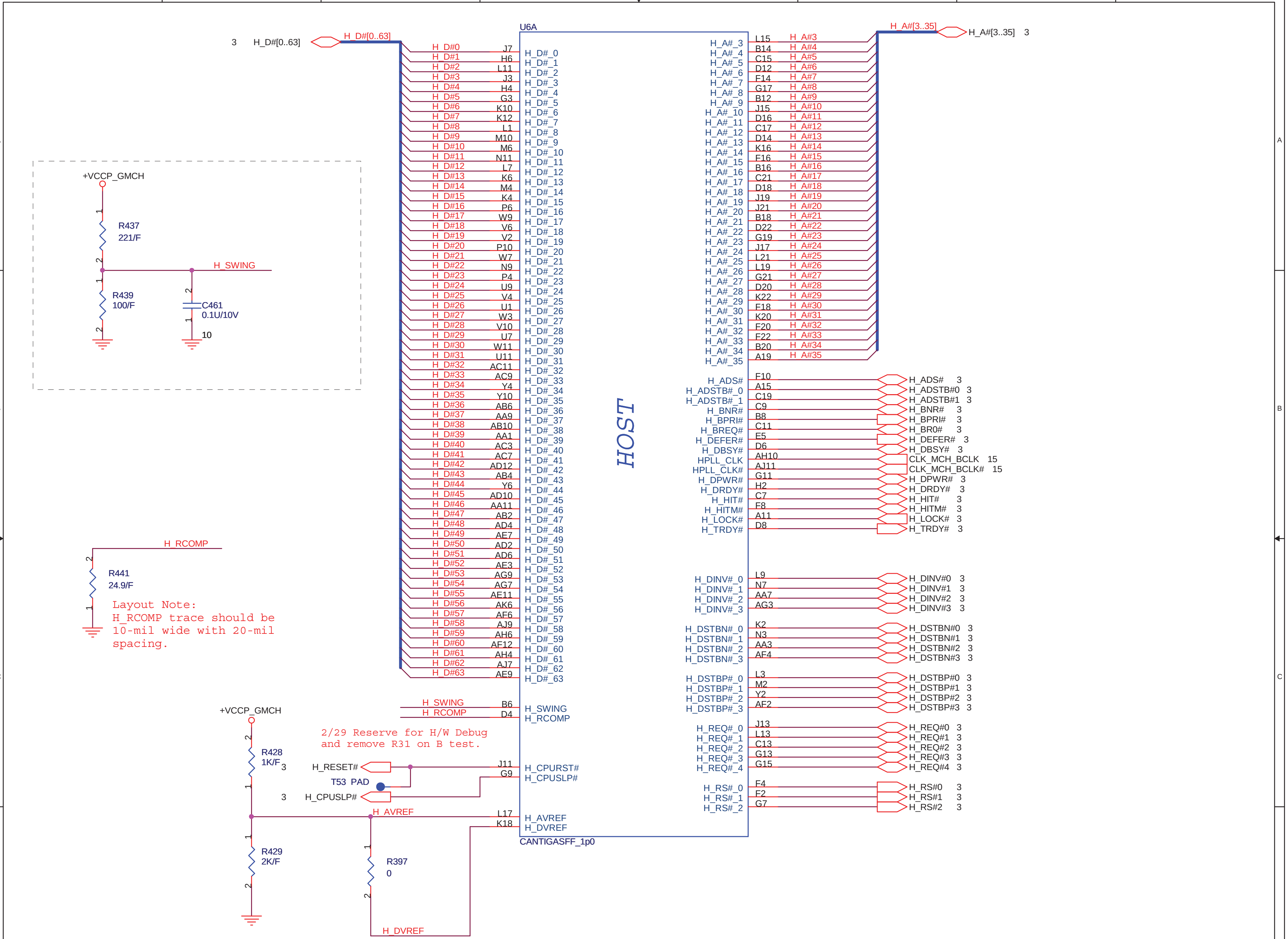


Signal	ITP disable guidelines		
TDI	Resistor Value		
TMS	150 ohm +/- 5%	Connect To	Resistor Placement
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TDO	27 ohm +/- 5%	Open GND	Within 2.0" of the ITP
ITP_EN		GND	Within 2.0" of the ITP
	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8

QUANTA COMPUTER

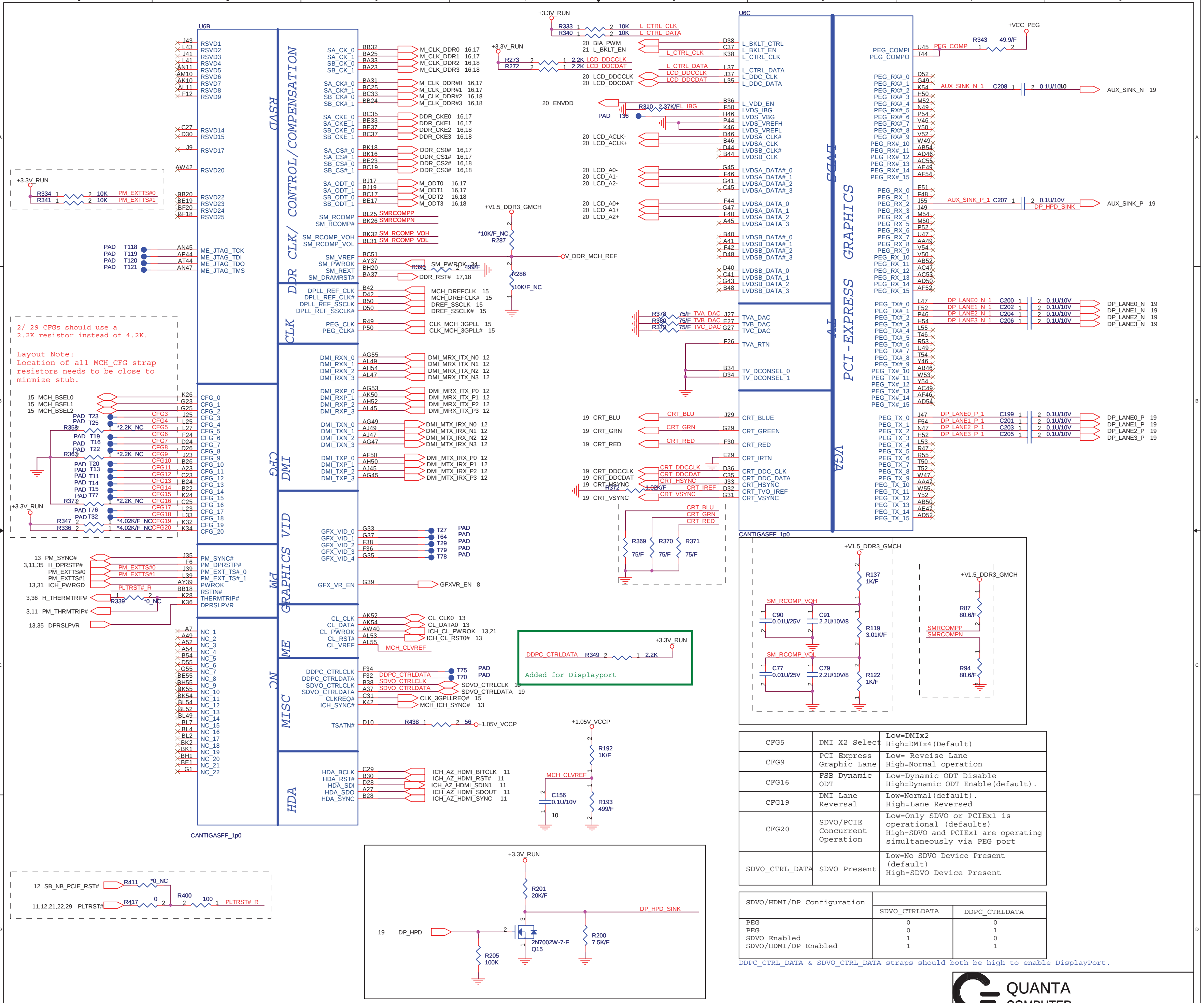
Title	Penryn (HOST BUS)	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 3 of 44	


U8C
U8F
U8E
U8D
+VCC_CORE
+V1.05S_CPU
+1.05V_VCCP
+1.5V_RUN
VCCSENSE
VSSSENSE
Penryn_SFF_1p0
QUANTA COMPUTER
Title
Penryn (POWER/NC)
Size
Document Number
SS5
Rev
1A
Date: Thursday, January 08, 2009
Sheet 4 of 44



QUANTA COMPUTER

Title	Cantiga_A (HOST)	
Size Custom	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 5 of 44	



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

SDVO/HDMI/DP Configuration	SDVO_CTRLDATA	DDPC_CTRLDATA
PEG	0	0
PEG	0	1
SDVO Enabled	1	0
SDVO/HDMI/DP Enabled	1	1

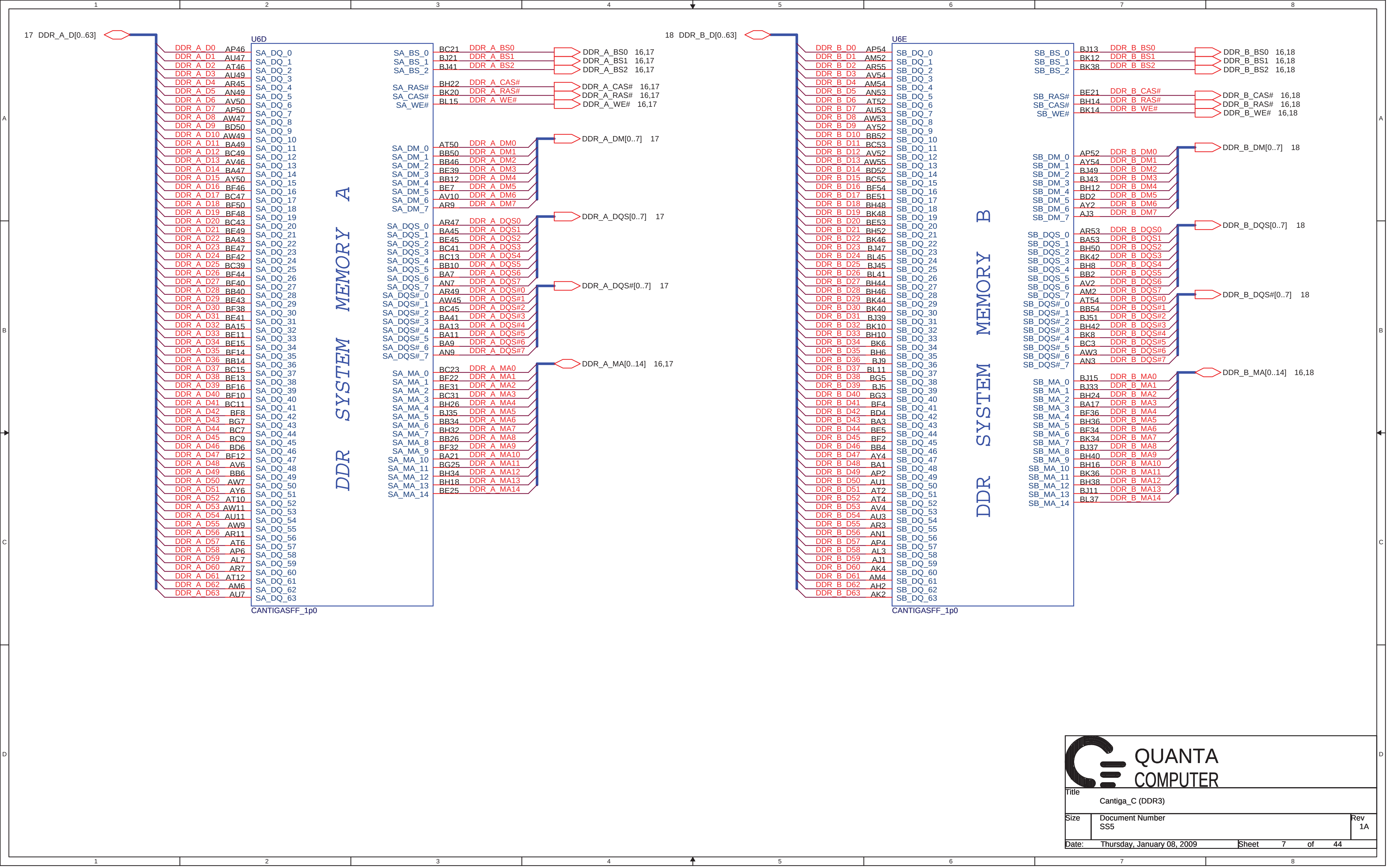
DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable DisplayPort.

QUANTA COMPUTER

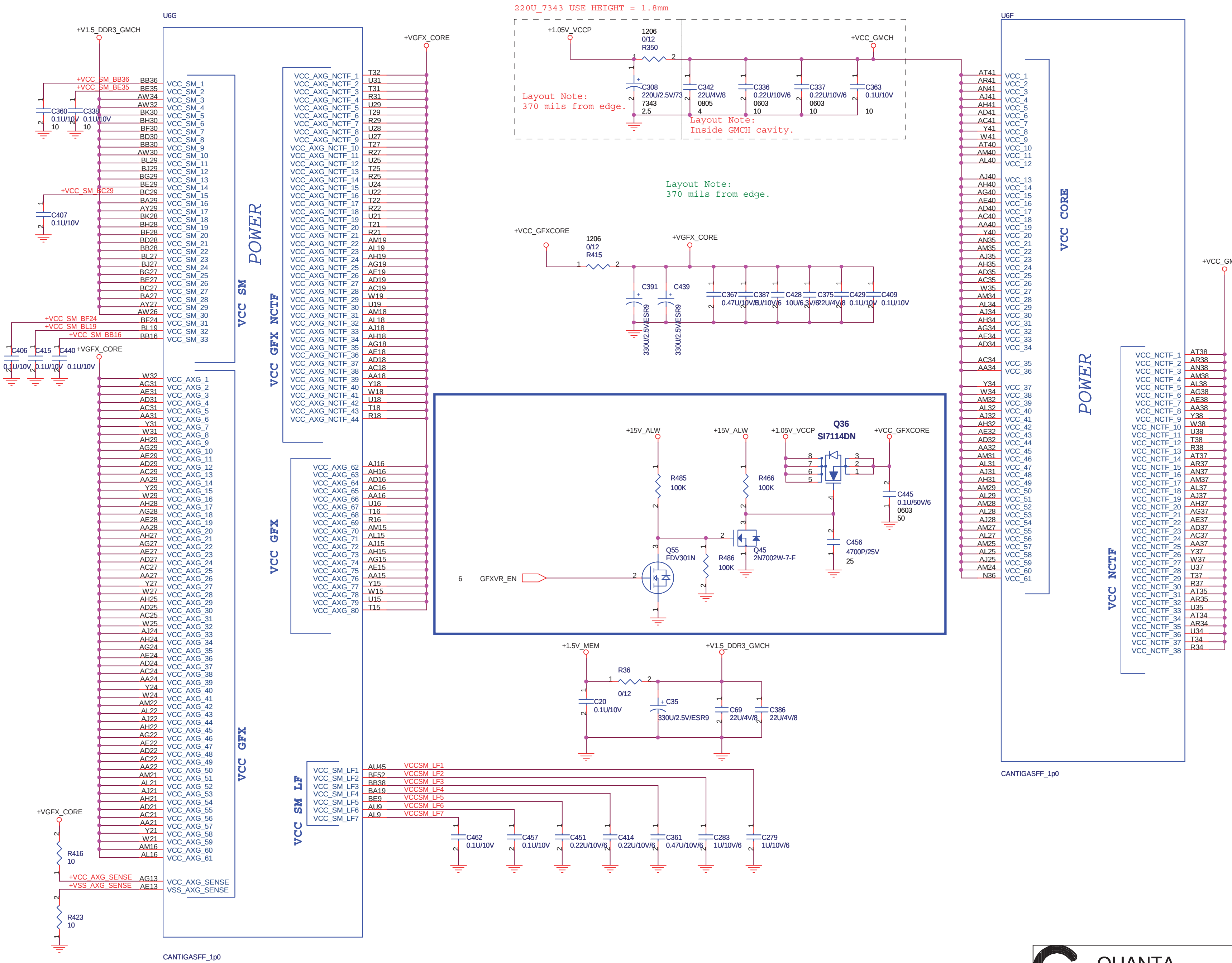
Title: Cantiga_B (VGA,DMI)

Size | Document Number | Rev 1A

Date: Thursday, February 01, 2009 | Sheet 6 of 44



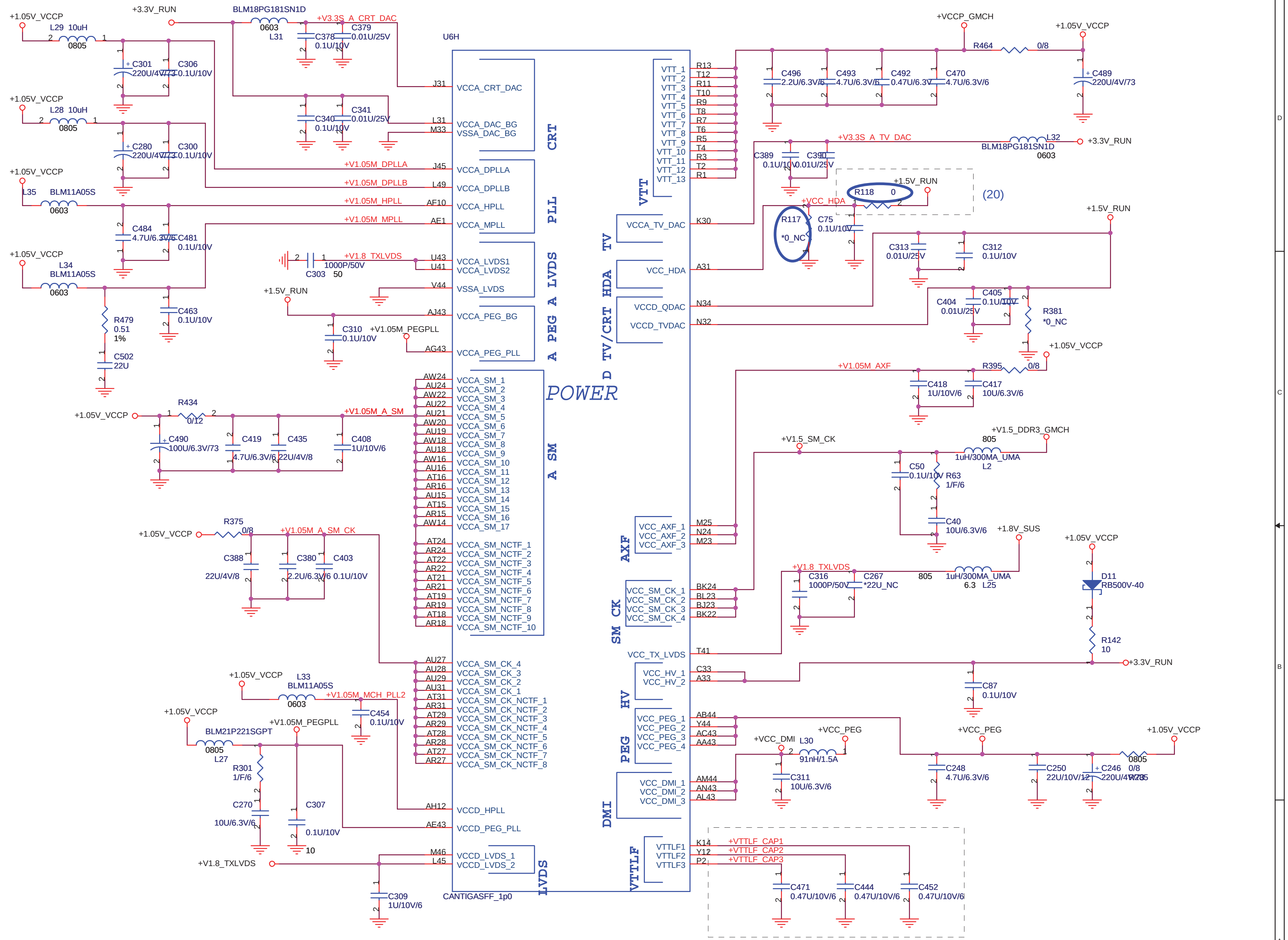
17 DDR_A_D[0..63]
U6D
DDR SYSTEM MEMORY A
DDR_A_D0 AP46 SA_DQ_0
DDR_A_D1 AU47 SA_DQ_1
DDR_A_D2 AT46 SA_DQ_2
DDR_A_D3 AU49 SA_DQ_3
DDR_A_D4 AR45 SA_DQ_4
DDR_A_D5 AN49 SA_DQ_5
DDR_A_D6 AV50 SA_DQ_6
DDR_A_D7 AP50 SA_DQ_7
DDR_A_D8 AW47 SA_DQ_8
DDR_A_D9 BD50 SA_DQ_9
DDR_A_D10 AW49 SA_DQ_10
DDR_A_D11 BA49 SA_DQ_11
DDR_A_D12 BC49 SA_DQ_12
DDR_A_D13 AV46 SA_DQ_13
DDR_A_D14 BA47 SA_DQ_14
DDR_A_D15 AY50 SA_DQ_15
DDR_A_D16 BF46 SA_DQ_16
DDR_A_D17 BC47 SA_DQ_17
DDR_A_D18 BF50 SA_DQ_18
DDR_A_D19 BF48 SA_DQ_19
DDR_A_D20 BC43 SA_DQ_20
DDR_A_D21 BE49 SA_DQ_21
DDR_A_D22 BA43 SA_DQ_22
DDR_A_D23 BE47 SA_DQ_23
DDR_A_D24 BF42 SA_DQ_24
DDR_A_D25 BC39 SA_DQ_25
DDR_A_D26 BF44 SA_DQ_26
DDR_A_D27 BF40 SA_DQ_27
DDR_A_D28 BB40 SA_DQ_28
DDR_A_D29 BE43 SA_DQ_29
DDR_A_D30 BF38 SA_DQ_30
DDR_A_D31 BE41 SA_DQ_31
DDR_A_D32 BA15 SA_DQ_32
DDR_A_D33 BE11 SA_DQ_33
DDR_A_D34 BE15 SA_DQ_34
DDR_A_D35 BF14 SA_DQ_35
DDR_A_D36 BB14 SA_DQ_36
DDR_A_D37 BC15 SA_DQ_37
DDR_A_D38 BE13 SA_DQ_38
DDR_A_D39 BF16 SA_DQ_39
DDR_A_D40 BF10 SA_DQ_40
DDR_A_D41 BC11 SA_DQ_41
DDR_A_D42 BF8 SA_DQ_42
DDR_A_D43 BG7 SA_DQ_43
DDR_A_D44 BC7 SA_DQ_44
DDR_A_D45 BC9 SA_DQ_45
DDR_A_D46 BD6 SA_DQ_46
DDR_A_D47 BF12 SA_DQ_47
DDR_A_D48 AV6 SA_DQ_48
DDR_A_D49 BB6 SA_DQ_49
DDR_A_D50 AW7 SA_DQ_50
DDR_A_D51 AY6 SA_DQ_51
DDR_A_D52 AT10 SA_DQ_52
DDR_A_D53 AW11 SA_DQ_53
DDR_A_D54 AU11 SA_DQ_54
DDR_A_D55 AW9 SA_DQ_55
DDR_A_D56 AR11 SA_DQ_56
DDR_A_D57 AT6 SA_DQ_57
DDR_A_D58 AP6 SA_DQ_58
DDR_A_D59 AL7 SA_DQ_59
DDR_A_D60 AR7 SA_DQ_60
DDR_A_D61 AT12 SA_DQ_61
DDR_A_D62 AM6 SA_DQ_62
DDR_A_D63 AU7 SA_DQ_63
SA_BS_0 BC21 DDR_A_BS0
SA_BS_1 BJ21 DDR_A_BS1
SA_BS_2 BJ41 DDR_A_BS2
DDR_A_BS0 16,17
DDR_A_BS1 16,17
DDR_A_BS2 16,17
SA_RAS# BH22 DDR_A_CAS#
SA_CAS# BK20 DDR_A_RAS#
SA_WE# BL15 DDR_A_WE#
DDR_A_CAS# 16,17
DDR_A_RAS# 16,17
DDR_A_WE# 16,17
SA_DM_0 AT50 DDR_A_DM0
SA_DM_1 BB50 DDR_A_DM1
SA_DM_2 BB46 DDR_A_DM2
SA_DM_3 BE39 DDR_A_DM3
SA_DM_4 BB12 DDR_A_DM4
SA_DM_5 BE7 DDR_A_DM5
SA_DM_6 AV10 DDR_A_DM6
SA_DM_7 AR9 DDR_A_DM7
DDR_A_DM[0..7] 17
SA_DQS_0 AR47 DDR_A_DQS0
SA_DQS_1 BA45 DDR_A_DQS1
SA_DQS_2 BE45 DDR_A_DQS2
SA_DQS_3 BC41 DDR_A_DQS3
SA_DQS_4 BC13 DDR_A_DQS4
SA_DQS_5 BB10 DDR_A_DQS5
SA_DQS_6 BA7 DDR_A_DQS6
SA_DQS_7 AN7 DDR_A_DQS7
DDR_A_DQS[0..7] 17
SA_DQS#_0 AR49 DDR_A_DQS#0
SA_DQS#_1 AW45 DDR_A_DQS#1
SA_DQS#_2 BC45 DDR_A_DQS#2
SA_DQS#_3 BA41 DDR_A_DQS#3
SA_DQS#_4 BA13 DDR_A_DQS#4
SA_DQS#_5 BA11 DDR_A_DQS#5
SA_DQS#_6 BA9 DDR_A_DQS#6
SA_DQS#_7 AN9 DDR_A_DQS#7
DDR_A_DQS#[0..7] 17
SA_MA_0 BC23 DDR_A_MA0
SA_MA_1 BF22 DDR_A_MA1
SA_MA_2 BE31 DDR_A_MA2
SA_MA_3 BC31 DDR_A_MA3
SA_MA_4 BH26 DDR_A_MA4
SA_MA_5 BJ35 DDR_A_MA5
SA_MA_6 BB34 DDR_A_MA6
SA_MA_7 BH32 DDR_A_MA7
SA_MA_8 BB26 DDR_A_MA8
SA_MA_9 BF32 DDR_A_MA9
SA_MA_10 BA21 DDR_A_MA10
SA_MA_11 BG25 DDR_A_MA11
SA_MA_12 BH34 DDR_A_MA12
SA_MA_13 BH18 DDR_A_MA13
SA_MA_14 BE25 DDR_A_MA14
DDR_A_MA[0..14] 16,17
CANTIGASFF_1p0
18 DDR_B_D[0..63]
U6E
DDR SYSTEM MEMORY B
DDR_B_D0 AP54 SB_DQ_0
DDR_B_D1 AM52 SB_DQ_1
DDR_B_D2 AR55 SB_DQ_2
DDR_B_D3 AV54 SB_DQ_3
DDR_B_D4 AM54 SB_DQ_4
DDR_B_D5 AN53 SB_DQ_5
DDR_B_D6 AT52 SB_DQ_6
DDR_B_D7 AU53 SB_DQ_7
DDR_B_D8 AW53 SB_DQ_8
DDR_B_D9 AY52 SB_DQ_9
DDR_B_D10 BB52 SB_DQ_10
DDR_B_D11 BC53 SB_DQ_11
DDR_B_D12 AV52 SB_DQ_12
DDR_B_D13 AW55 SB_DQ_13
DDR_B_D14 BD52 SB_DQ_14
DDR_B_D15 BC55 SB_DQ_15
DDR_B_D16 BF54 SB_DQ_16
DDR_B_D17 BE51 SB_DQ_17
DDR_B_D18 BH48 SB_DQ_18
DDR_B_D19 BK48 SB_DQ_19
DDR_B_D20 BE53 SB_DQ_20
DDR_B_D21 BH52 SB_DQ_21
DDR_B_D22 BK46 SB_DQ_22
DDR_B_D23 BJ47 SB_DQ_23
DDR_B_D24 BL45 SB_DQ_24
DDR_B_D25 BJ45 SB_DQ_25
DDR_B_D26 BL41 SB_DQ_26
DDR_B_D27 BH44 SB_DQ_27
DDR_B_D28 BH46 SB_DQ_28
DDR_B_D29 BK44 SB_DQ_29
DDR_B_D30 BK40 SB_DQ_30
DDR_B_D31 BJ39 SB_DQ_31
DDR_B_D32 BK10 SB_DQ_32
DDR_B_D33 BH10 SB_DQ_33
DDR_B_D34 BK6 SB_DQ_34
DDR_B_D35 BH6 SB_DQ_35
DDR_B_D36 BJ9 SB_DQ_36
DDR_B_D37 BL11 SB_DQ_37
DDR_B_D38 BG5 SB_DQ_38
DDR_B_D39 BJ5 SB_DQ_39
DDR_B_D40 BG3 SB_DQ_40
DDR_B_D41 BF4 SB_DQ_41
DDR_B_D42 BD4 SB_DQ_42
DDR_B_D43 BA3 SB_DQ_43
DDR_B_D44 BE5 SB_DQ_44
DDR_B_D45 BF2 SB_DQ_45
DDR_B_D46 BB4 SB_DQ_46
DDR_B_D47 AY4 SB_DQ_47
DDR_B_D48 BA1 SB_DQ_48
DDR_B_D49 AP2 SB_DQ_49
DDR_B_D50 AU1 SB_DQ_50
DDR_B_D51 AT2 SB_DQ_51
DDR_B_D52 AT4 SB_DQ_52
DDR_B_D53 AV4 SB_DQ_53
DDR_B_D54 AU3 SB_DQ_54
DDR_B_D55 AR3 SB_DQ_55
DDR_B_D56 AN1 SB_DQ_56
DDR_B_D57 AP4 SB_DQ_57
DDR_B_D58 AL3 SB_DQ_58
DDR_B_D59 AJ1 SB_DQ_59
DDR_B_D60 AK4 SB_DQ_60
DDR_B_D61 AM4 SB_DQ_61
DDR_B_D62 AH2 SB_DQ_62
DDR_B_D63 AK2 SB_DQ_63
SB_BS_0 BJ13 DDR_B_BS0
SB_BS_1 BK12 DDR_B_BS1
SB_BS_2 BK38 DDR_B_BS2
DDR_B_BS0 16,18
DDR_B_BS1 16,18
DDR_B_BS2 16,18
SB_RAS# BE21 DDR_B_CAS#
SB_CAS# BH14 DDR_B_RAS#
SB_WE# BK14 DDR_B_WE#
DDR_B_CAS# 16,18
DDR_B_RAS# 16,18
DDR_B_WE# 16,18
SB_DM_0 AP52 DDR_B_DM0
SB_DM_1 AY54 DDR_B_DM1
SB_DM_2 BJ49 DDR_B_DM2
SB_DM_3 BJ43 DDR_B_DM3
SB_DM_4 BH12 DDR_B_DM4
SB_DM_5 BD2 DDR_B_DM5
SB_DM_6 AY2 DDR_B_DM6
SB_DM_7 AJ3 DDR_B_DM7
DDR_B_DM[0..7] 18
SB_DQS_0 AR53 DDR_B_DQS0
SB_DQS_1 BA53 DDR_B_DQS1
SB_DQS_2 BH50 DDR_B_DQS2
SB_DQS_3 BK42 DDR_B_DQS3
SB_DQS_4 BH8 DDR_B_DQS4
SB_DQS_5 BB2 DDR_B_DQS5
SB_DQS_6 AV2 DDR_B_DQS6
SB_DQS_7 AM2 DDR_B_DQS7
DDR_B_DQS[0..7] 18
SB_DQS#_0 AT54 DDR_B_DQS#0
SB_DQS#_1 BB54 DDR_B_DQS#1
SB_DQS#_2 BJ51 DDR_B_DQS#2
SB_DQS#_3 BH42 DDR_B_DQS#3
SB_DQS#_4 BK8 DDR_B_DQS#4
SB_DQS#_5 BC3 DDR_B_DQS#5
SB_DQS#_6 AW3 DDR_B_DQS#6
SB_DQS#_7 AN3 DDR_B_DQS#7
DDR_B_DQS#[0..7] 18
SB_MA_0 BJ15 DDR_B_MA0
SB_MA_1 BJ33 DDR_B_MA1
SB_MA_2 BH24 DDR_B_MA2
SB_MA_3 BA17 DDR_B_MA3
SB_MA_4 BF36 DDR_B_MA4
SB_MA_5 BH36 DDR_B_MA5
SB_MA_6 BF34 DDR_B_MA6
SB_MA_7 BK34 DDR_B_MA7
SB_MA_8 BJ37 DDR_B_MA8
SB_MA_9 BH40 DDR_B_MA9
SB_MA_10 BH16 DDR_B_MA10
SB_MA_11 BK36 DDR_B_MA11
SB_MA_12 BH38 DDR_B_MA12
SB_MA_13 BJ11 DDR_B_MA13
SB_MA_14 BL37 DDR_B_MA14
DDR_B_MA[0..14] 16,18
CANTIGASFF_1p0
QUANTA COMPUTER
Title
Cantiga_C (DDR3)
Size
Document Number
SS5
Rev
1A
Date: Thursday, January 08, 2009
Sheet 7 of 44



UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.

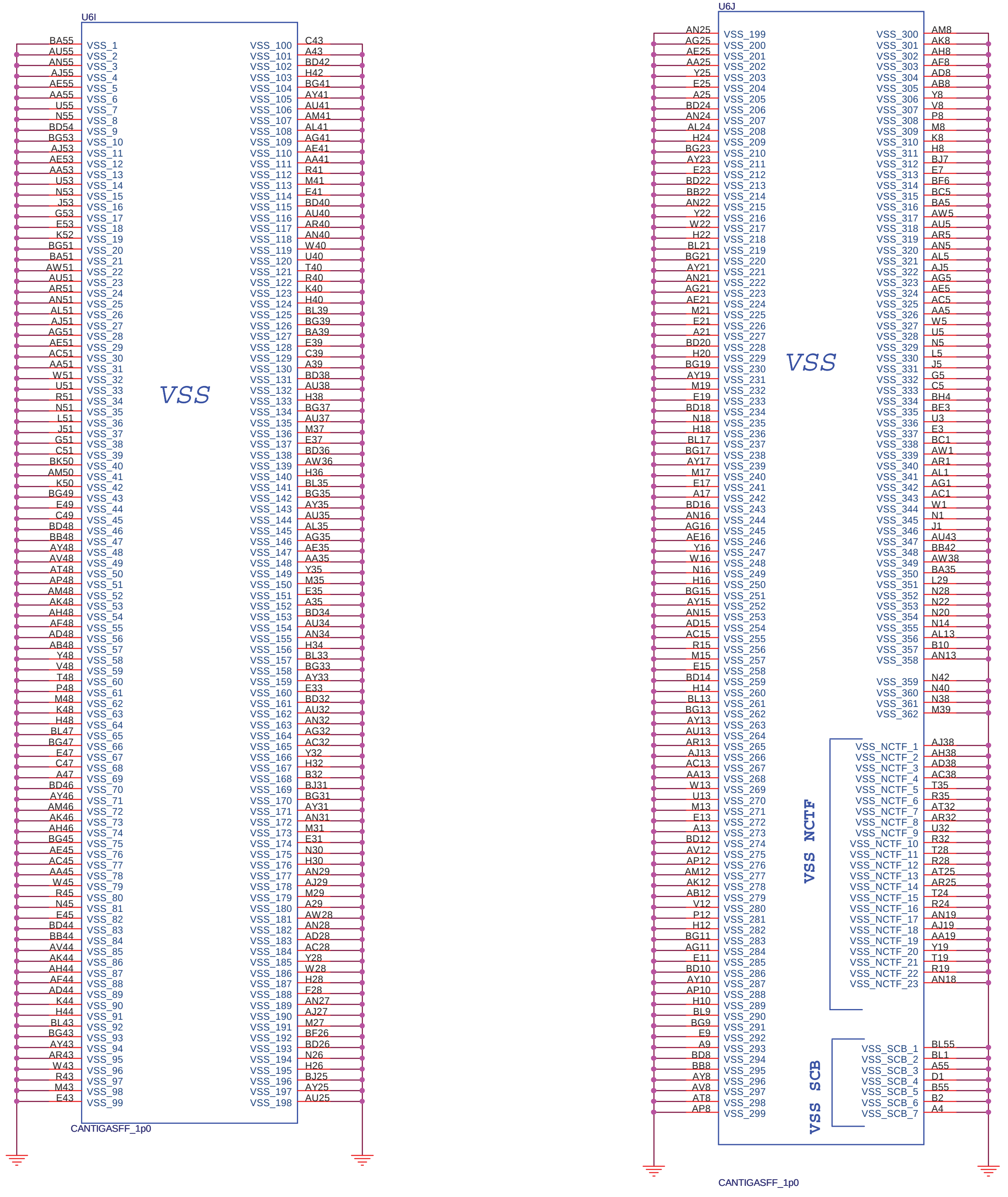
QUANTA COMPUTER

Title	Cantiga_D (VCC,NCTF)	
Size	Document Number SSI	Rev 1A
Date: Thursday, February 05, 2009	Sheet 8 of 44	



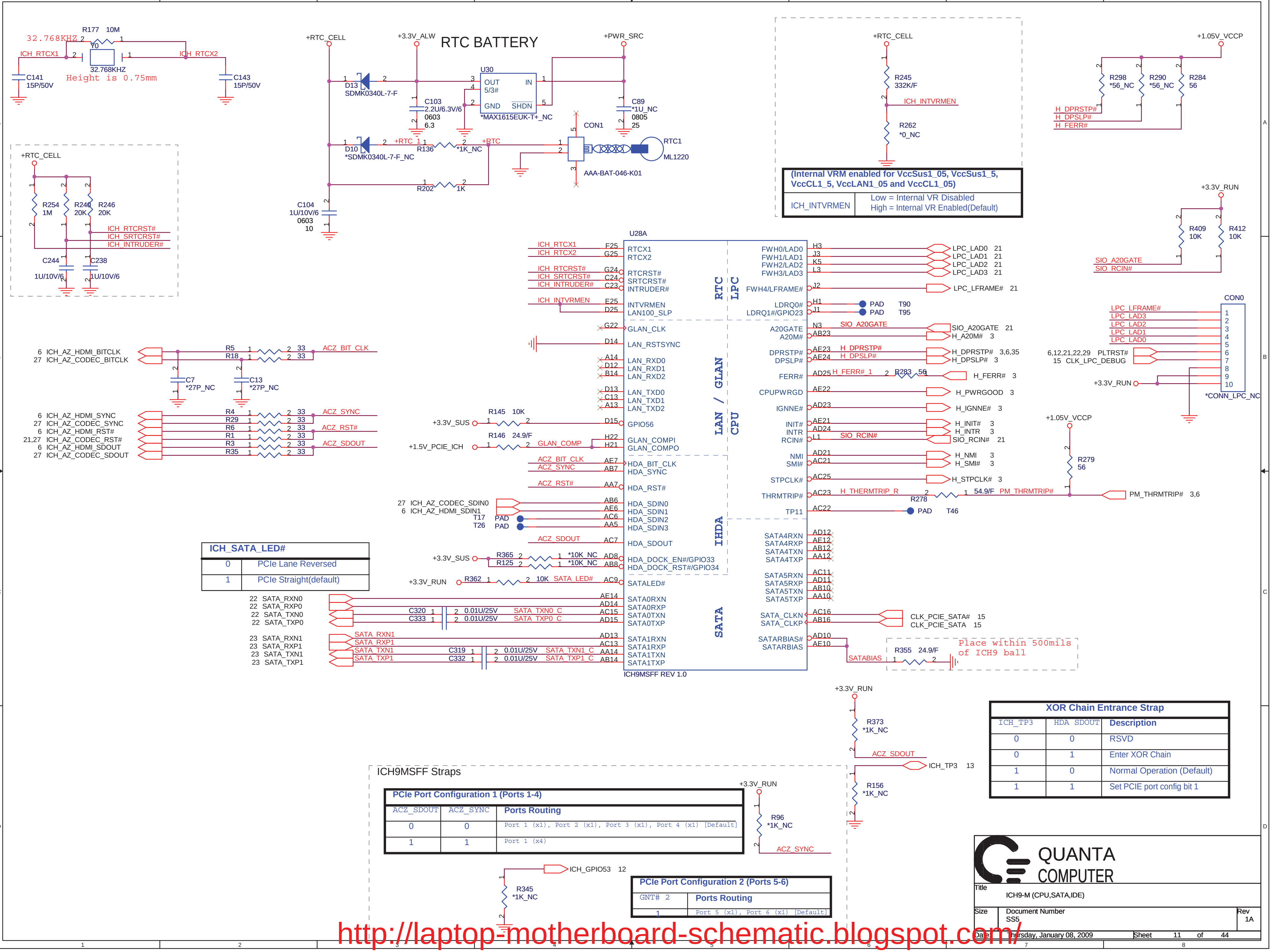
QUANTA COMPUTER

Title	Cantiga_E (POWER)	
Size	Document Number SS5	Rev 1A
Date: Monday, February 23, 2009	Sheet 9 of 44	



QUANTA COMPUTER

Title	Cantiga_F (VSS)	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 10 of 44	



ICH_SATA_LED#	
0	PCIe Lane Reversed
1	PCIe Straight(default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

ICH9MSFF Straps

PCIe Port Configuration 1 (Ports 1-4)

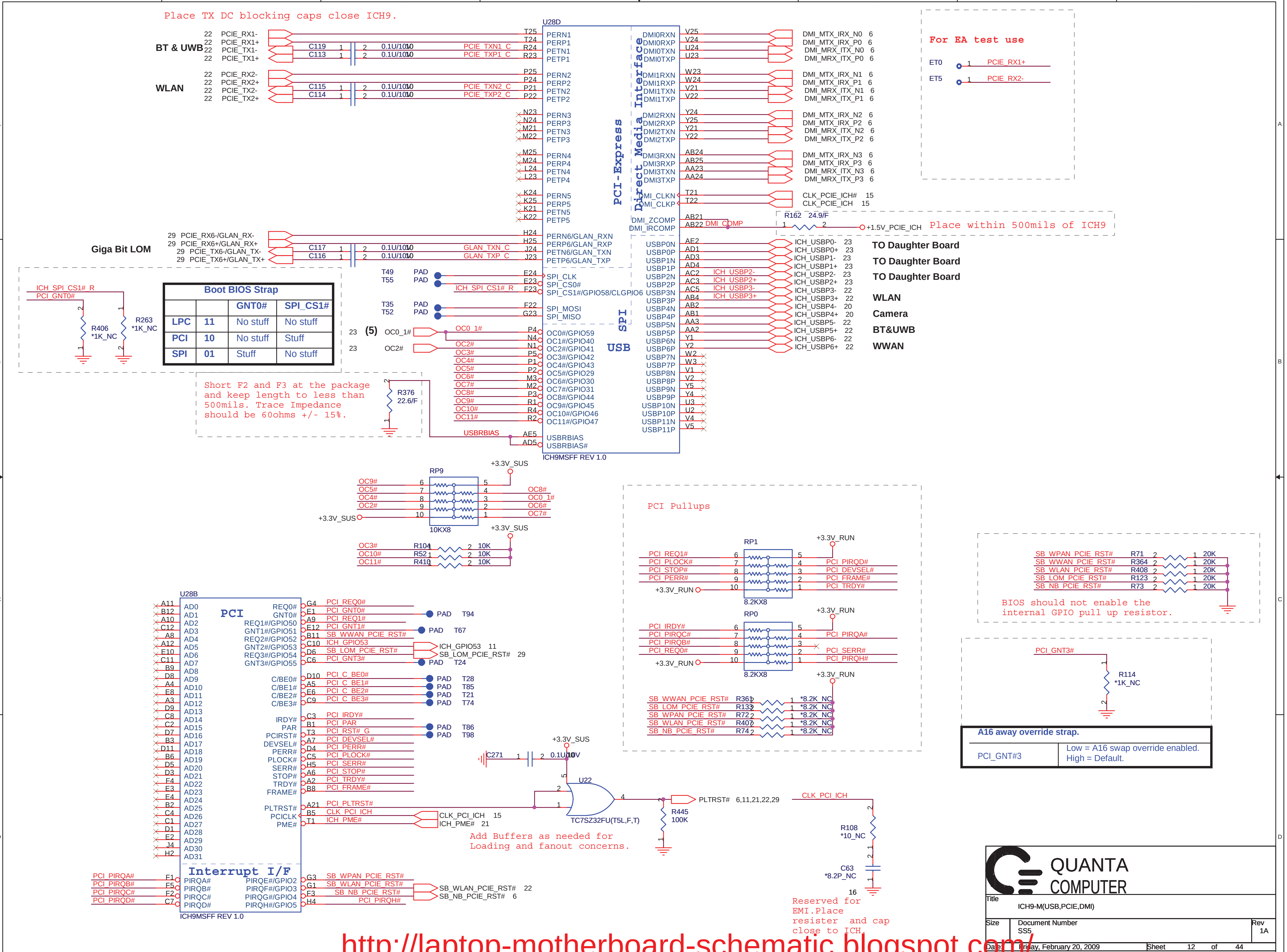
ACZ_SDOUT	ACZ_SYNC	Ports Routing
0	0	Port 1 (x1), Port 2 (x1), Port 3 (x1), Port 4 (x1) [Default]
1	1	Port 1 (x4)

PCIe Port Configuration 2 (Ports 5-6)

GNT# 2	Ports Routing
1	Port 5 (x1), Port 6 (x1) [Default]

QUANTA COMPUTER

Title	ICH9-M (CPU,SATA,IDE)
Size	Document Number SS5
Rev	1A
Date	Thursday, January 08, 2009
Sheet	11 of 44



Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

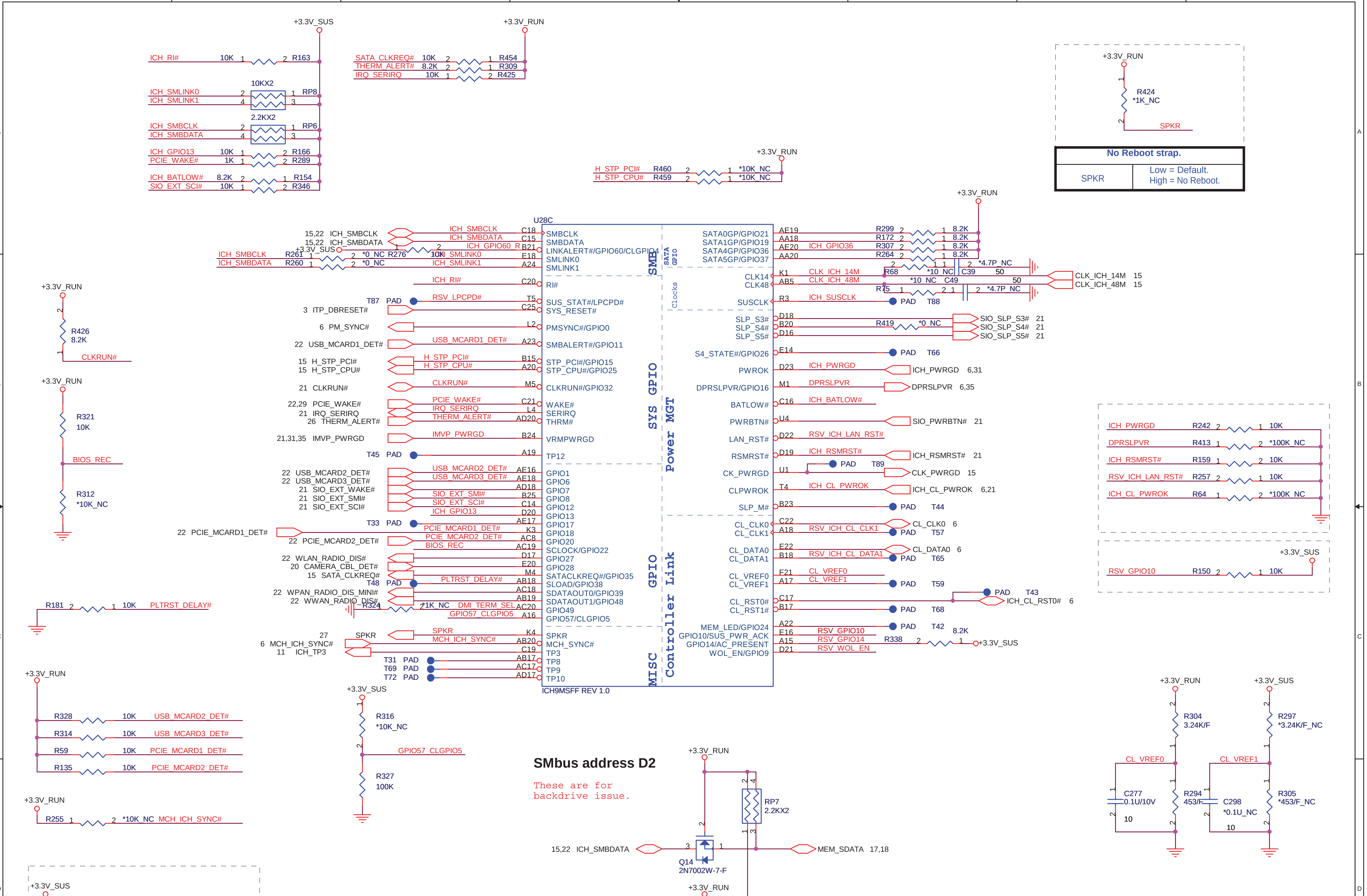
A16 away override strap.

PCI_GNT#3	Low = A16 swap override enabled. High = Default.

Title: ICH9-M(USB,PCIE,DMI)

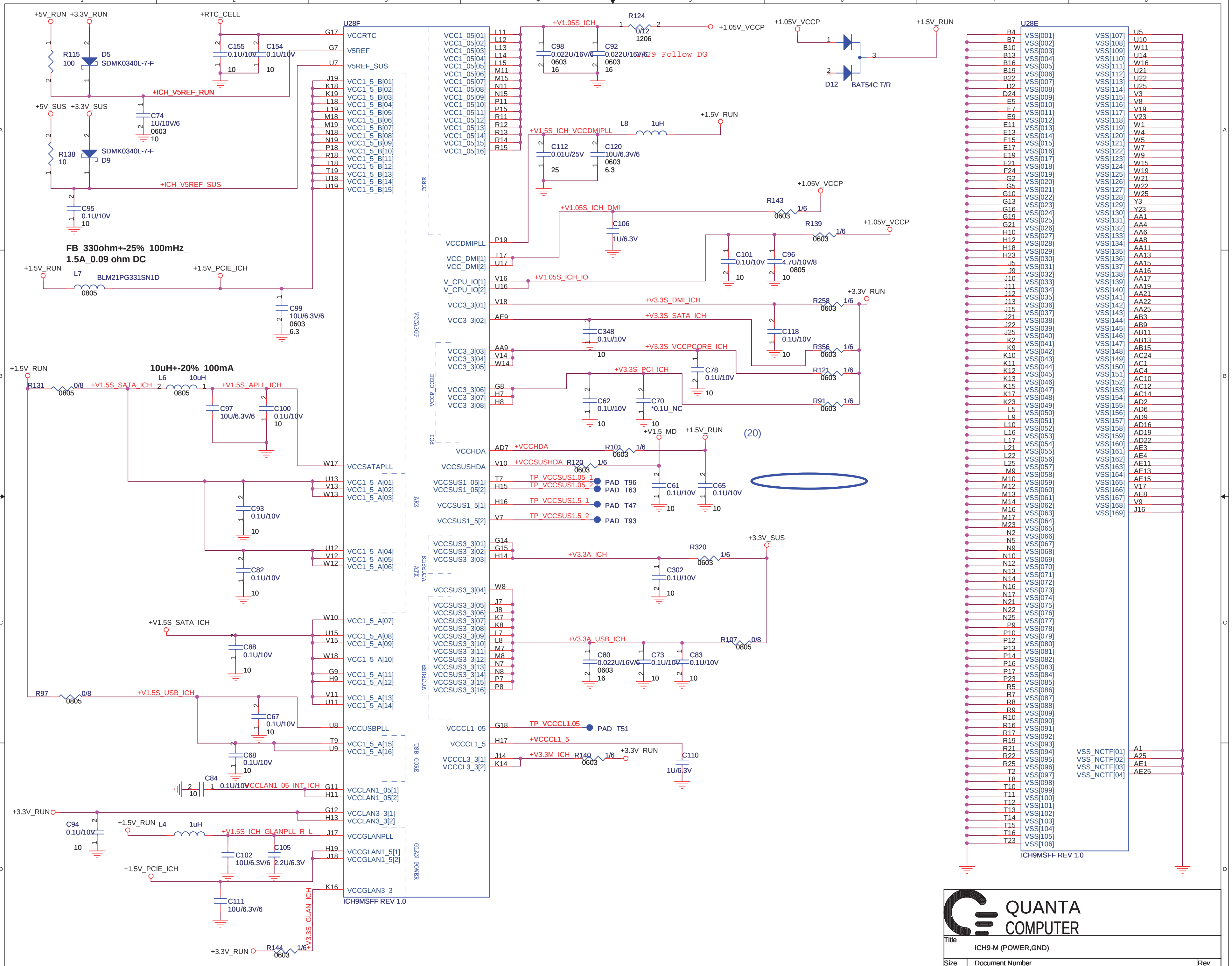
Size	Document Number	Rev
	SS5	1A

Date: Friday, February 20, 2009 Sheet 12 of 44



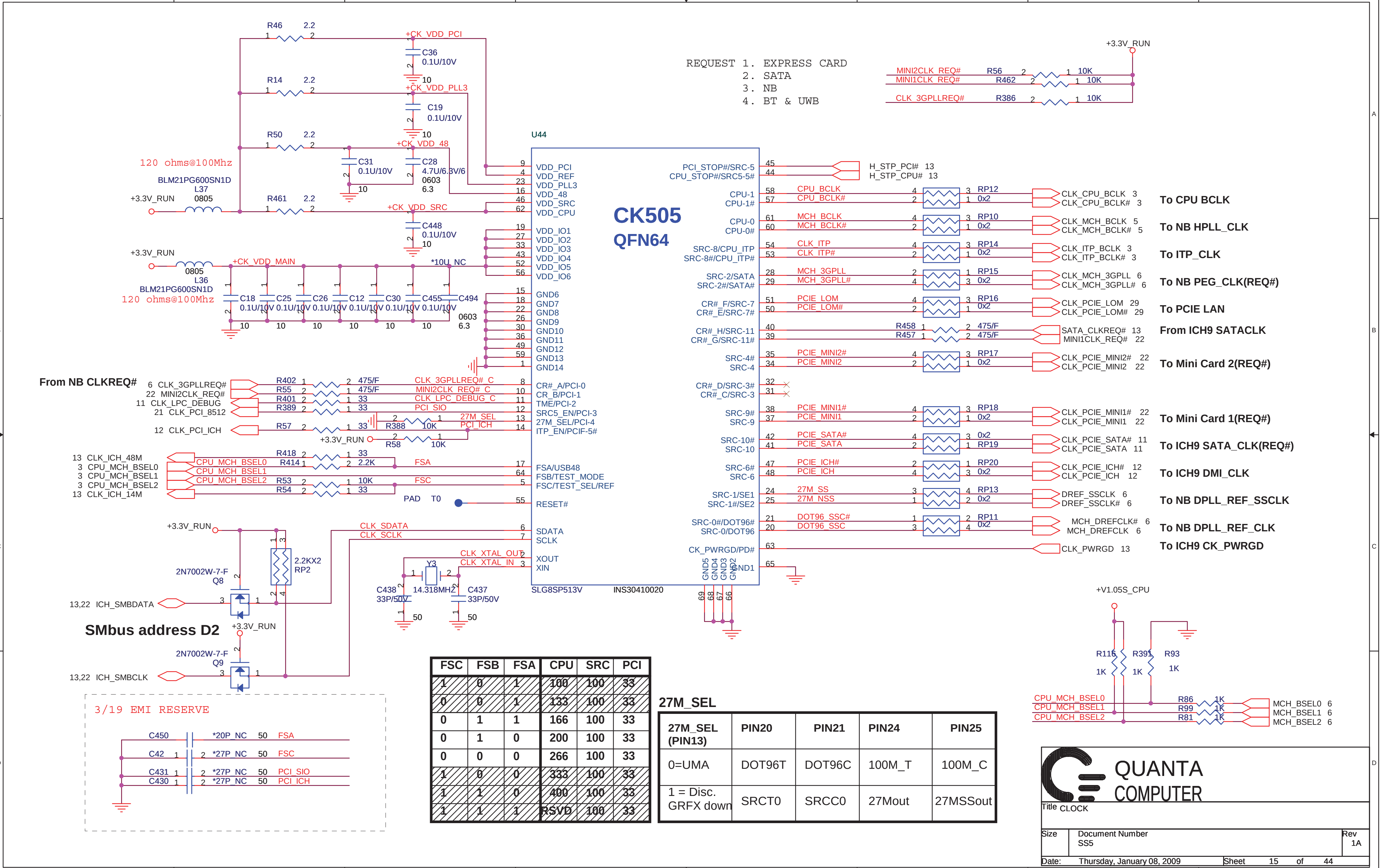
QUANTA COMPUTER

Title	ICH9-M (PM,GPIO,SMB)	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 13 of 44	



QUANTA COMPUTER

Title	ICH9-M (POWER,GND)	
Size	Document Number SS1	Rev 1A
Date: Thursday, January 08, 2009	Sheet 14 of 44	



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

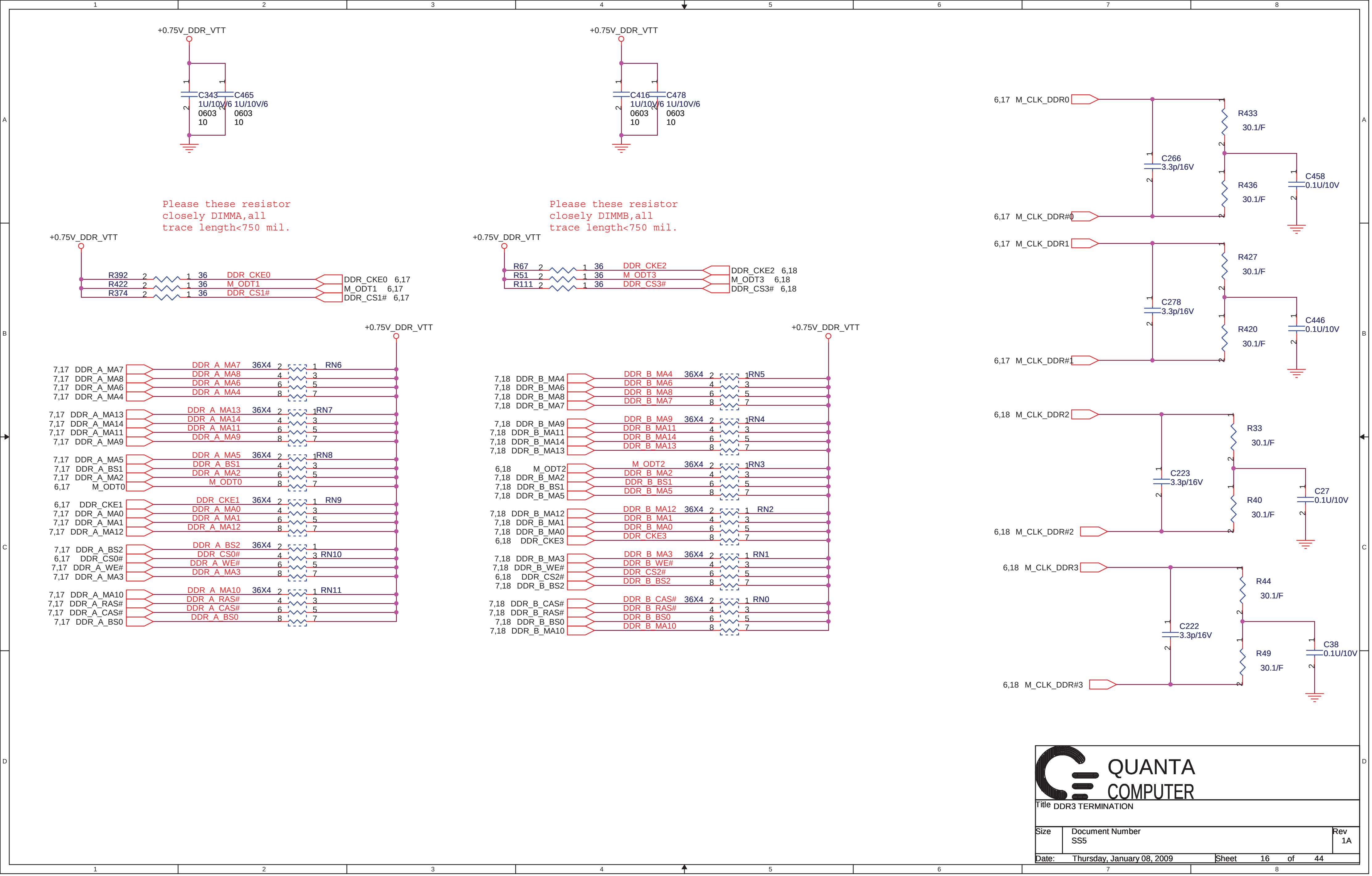
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	100M_T	100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

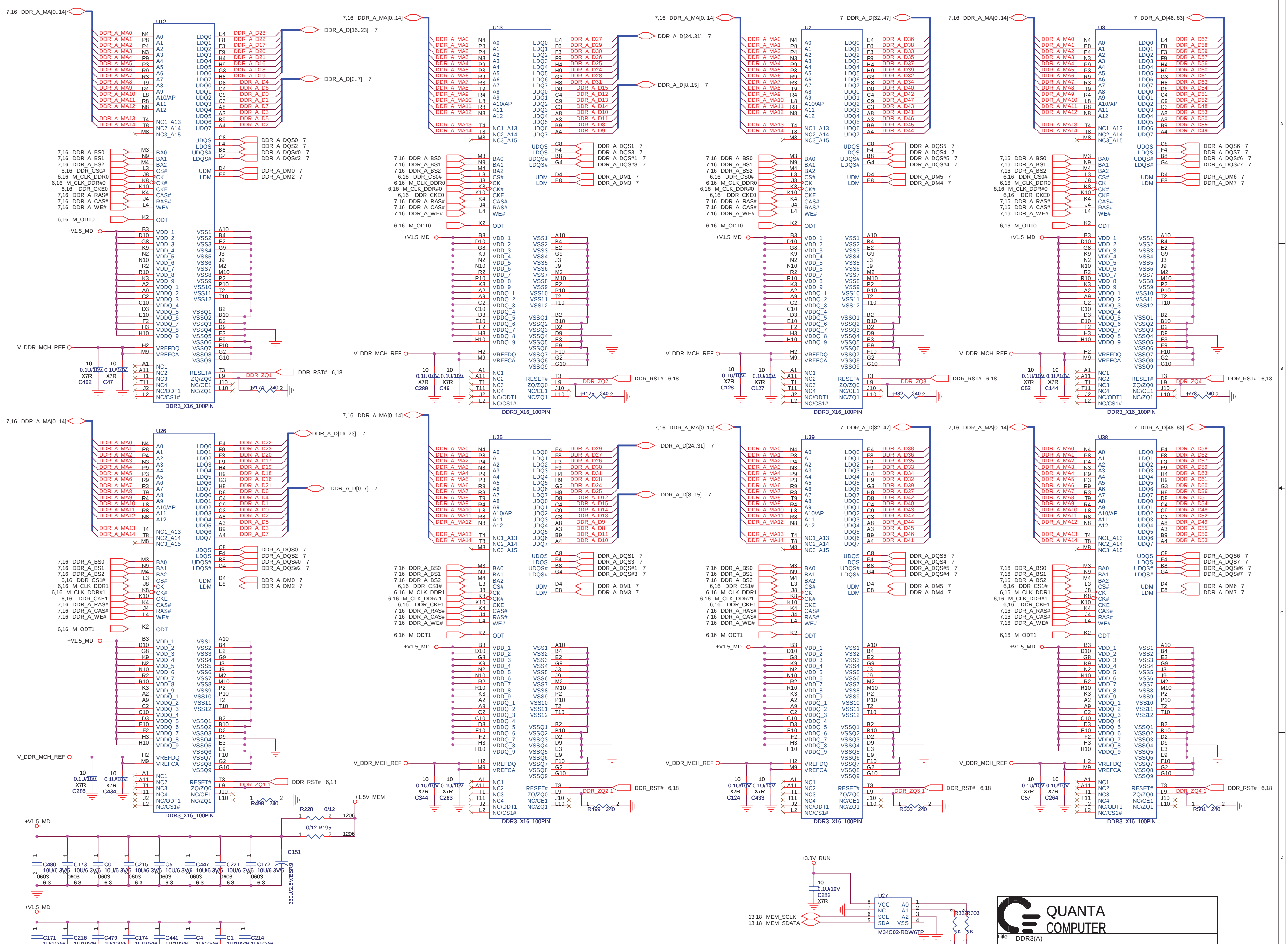
QUANTA COMPUTER

Title: CLOCK

Size	Document Number	Rev
	SS5	1A

Date: Thursday, January 08, 2009 Sheet 15 of 44


+0.75V_DDR_VTT
C343 1U/10V/6 0603 10
C465 1U/10V/6 0603 10
C416 1U/10V/6 0603 10
C478 1U/10V/6 0603 10
Please these resistor closely DIMMA,all trace length<750 mil.
Please these resistor closely DIMMB,all trace length<750 mil.
R392 R422 R374 36
DDR_CKE0 M_ODT1 DDR_CS1#
DDR_CKE0 6,17
M_ODT1 6,17
DDR_CS1# 6,17
R67 R51 R111 36
DDR_CKE2 M_ODT3 DDR_CS3#
DDR_CKE2 6,18
M_ODT3 6,18
DDR_CS3# 6,18
RN6 RN7 RN8 RN9 RN10 RN11 36X4
7,17 DDR_A_MA7
7,17 DDR_A_MA8
7,17 DDR_A_MA6
7,17 DDR_A_MA4
7,17 DDR_A_MA13
7,17 DDR_A_MA14
7,17 DDR_A_MA11
7,17 DDR_A_MA9
7,17 DDR_A_MA5
7,17 DDR_A_BS1
7,17 DDR_A_MA2
6,17 M_ODT0
6,17 DDR_CKE1
7,17 DDR_A_MA0
7,17 DDR_A_MA1
7,17 DDR_A_MA12
7,17 DDR_A_BS2
6,17 DDR_CS0#
7,17 DDR_A_WE#
7,17 DDR_A_MA3
7,17 DDR_A_MA10
7,17 DDR_A_RAS#
7,17 DDR_A_CAS#
7,17 DDR_A_BS0
RN5 RN4 RN3 RN2 RN1 RN0 36X4
7,18 DDR_B_MA4
7,18 DDR_B_MA6
7,18 DDR_B_MA8
7,18 DDR_B_MA7
7,18 DDR_B_MA9
7,18 DDR_B_MA11
7,18 DDR_B_MA14
7,18 DDR_B_MA13
6,18 M_ODT2
7,18 DDR_B_MA2
7,18 DDR_B_BS1
7,18 DDR_B_MA5
7,18 DDR_B_MA12
7,18 DDR_B_MA1
7,18 DDR_B_MA0
6,18 DDR_CKE3
7,18 DDR_B_MA3
7,18 DDR_B_WE#
6,18 DDR_CS2#
7,18 DDR_B_BS2
7,18 DDR_B_CAS#
7,18 DDR_B_RAS#
7,18 DDR_B_BS0
7,18 DDR_B_MA10
6,17 M_CLK_DDR0
6,17 M_CLK_DDR#0
R433 30.1/F
R436 30.1/F
C266 3.3p/16V
C458 0.1U/10V
6,17 M_CLK_DDR1
6,17 M_CLK_DDR#1
R427 30.1/F
R420 30.1/F
C278 3.3p/16V
C446 0.1U/10V
6,18 M_CLK_DDR2
6,18 M_CLK_DDR#2
R33 30.1/F
R40 30.1/F
C223 3.3p/16V
C27 0.1U/10V
6,18 M_CLK_DDR3
6,18 M_CLK_DDR#3
R44 30.1/F
R49 30.1/F
C222 3.3p/16V
C38 0.1U/10V
QUANTA COMPUTER
Title DDR3 TERMINATION
Size Document Number SS5 Rev 1A
Date: Thursday, January 08, 2009 Sheet 16 of 44

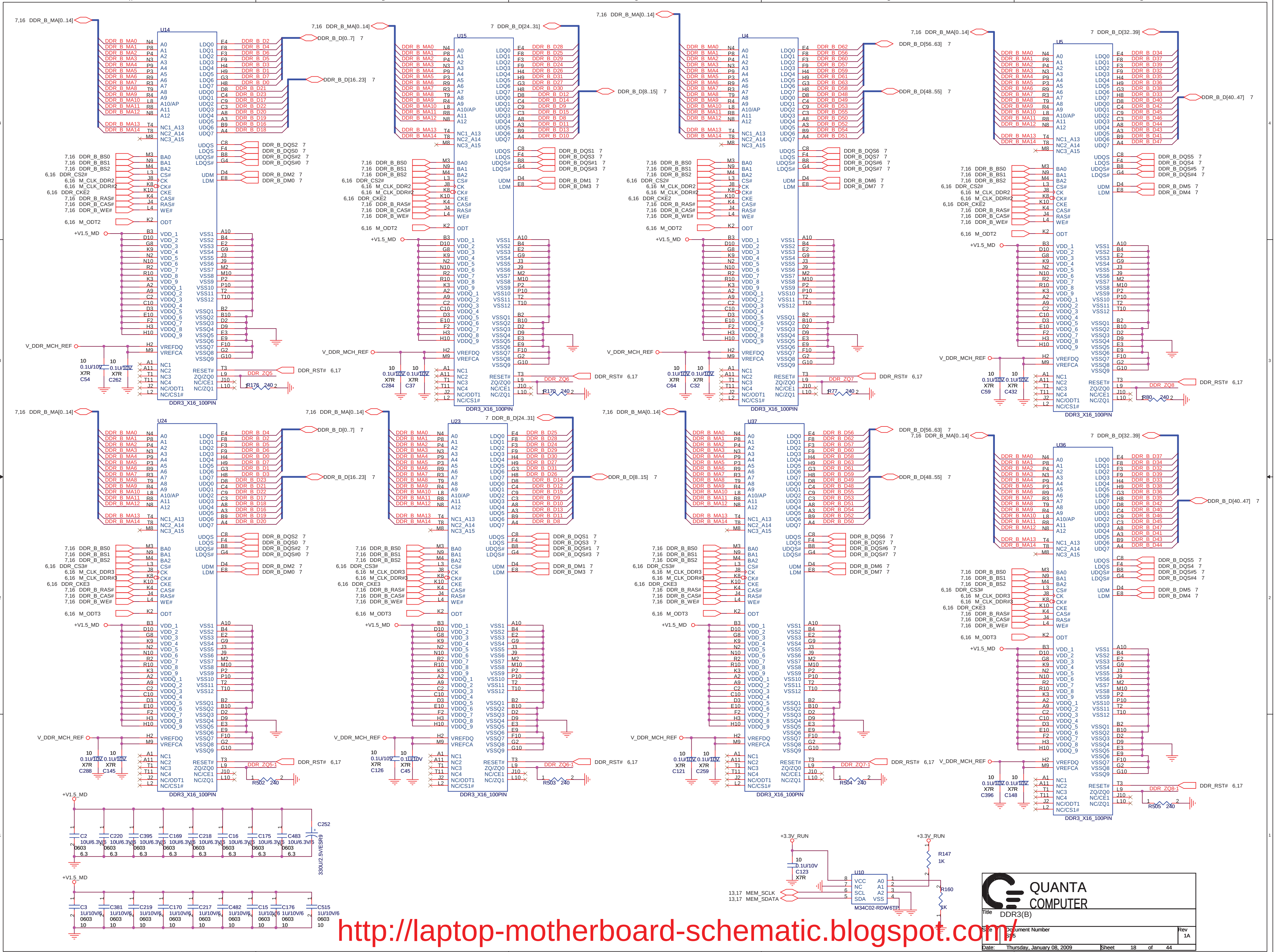


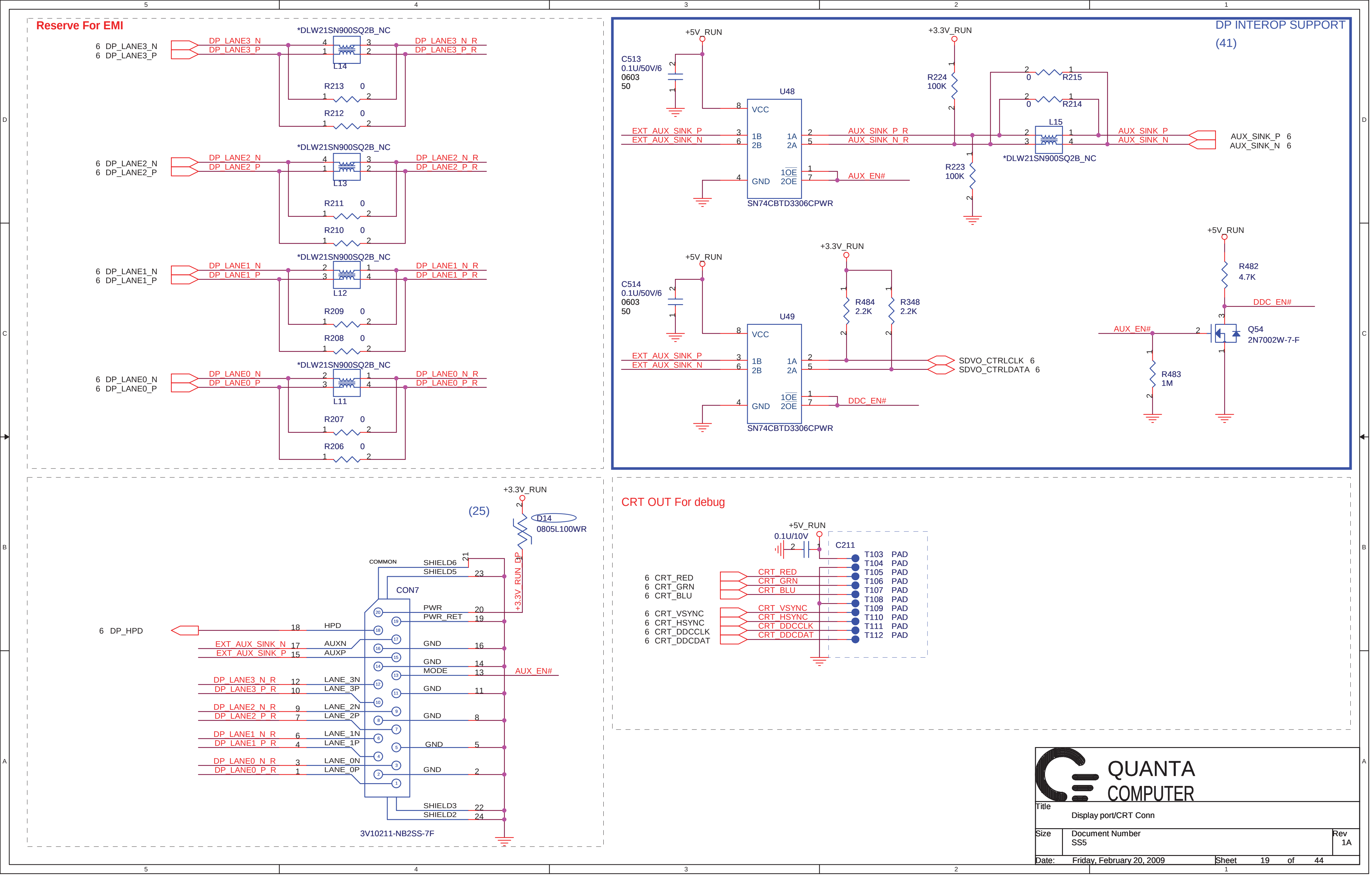
QUANTA COMPUTER

Title: DDR3(A)

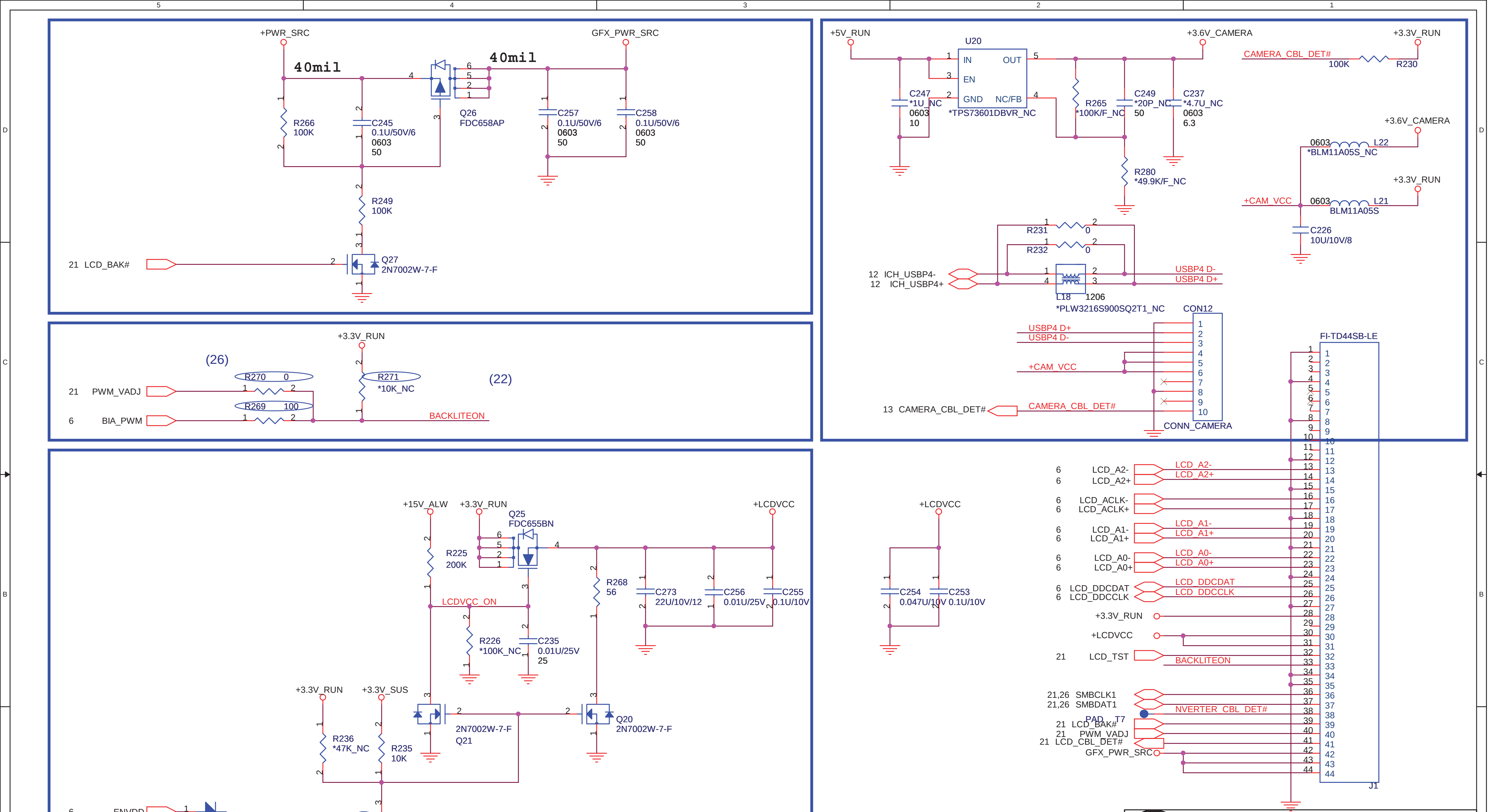
Size | Document Number | Rev 1A

Date: Thursday, January 08, 2009 | Sheet 17 of 44


U14
U15
U4
U5
U24
U23
U37
U36
DDR3_X16_100PIN
7,16 DDR_B_MA[0..14]
DDR_B_D[0..7] 7
DDR_B_D[16..23] 7
7 DDR_B_D[24..31]
DDR_B_D[8..15] 7
DDR_B_D[56..63] 7
DDR_B_D[48..55] 7
7 DDR_B_D[32..39]
DDR_B_D[40..47] 7
+V1.5_MD
V_DDR_MCH_REF
DDR_RST# 6,17
7,16 DDR_B_BS0
7,16 DDR_B_BS1
7,16 DDR_B_BS2
6,16 DDR_CS2#
6,16 M_CLK_DDR2
6,16 M_CLK_DDR#2
6,16 DDR_CKE2
7,16 DDR_B_RAS#
7,16 DDR_B_CAS#
7,16 DDR_B_WE#
6,16 M_ODT2
6,16 DDR_CS3#
6,16 M_CLK_DDR3
6,16 M_CLK_DDR#3
6,16 DDR_CKE3
6,16 M_ODT3
+3.3V_RUN
U10
M34C02-RDW6TP
13,17 MEM_SCLK
13,17 MEM_SDATA
R147 1K
R160 1K
C123 0.1U/10V X7R
C252 330U/2.5V/ESR9
QUANTA COMPUTER
Title
DDR3(B)
Size
Document Number
SJ5
Rev
1A
Date: Thursday, January 08, 2009
Sheet 18 of 44

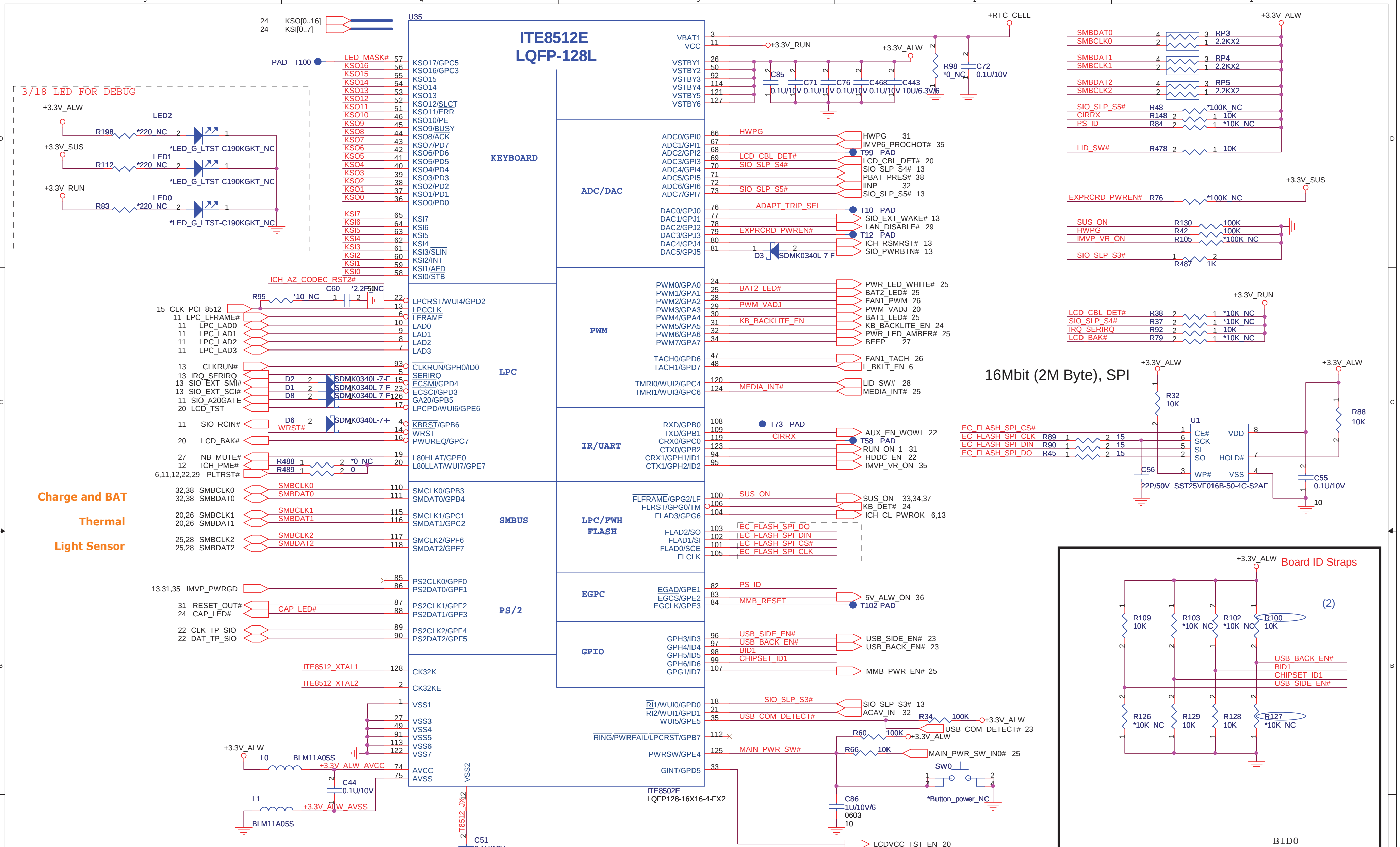


http://laptop-motherboard-schematic.blogspot.com/



QUANTA COMPUTER

Title	LCD CONN	
Size	Document Number SS5	Rev 1A
Date: Monday, February 23, 2009	Sheet 20 of 44	



BID0

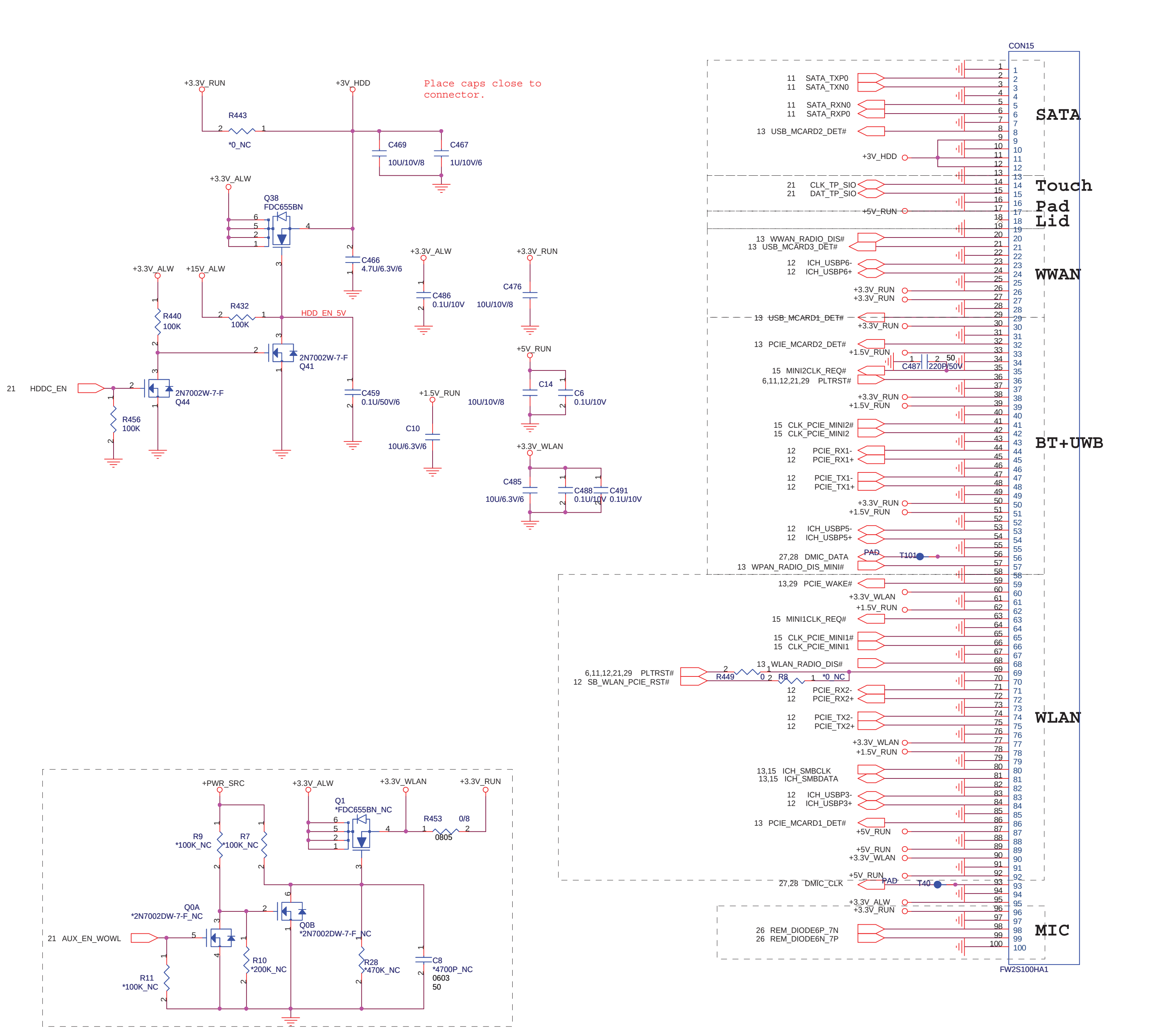
CHIPSET_ID1	USB_SIDE_EN#	BID1	USB_BACK_EN#	SS5
0	0	0	1	SSI(X00)
0	0	0	0	SSI(X00.1)
0	0	1	0	PT(X01)
0	0	1	1	ST(X02)
0	1	0	0	ST1(X02.1)
0	1	0	1	QT(A00)
0	1	1	0	A01

QUANTA COMPUTER

Title: SIO(ITE8512)

Size | Document Number: SS5 | Rev: 2A

Date: Friday, February 20, 2009 | Sheet 21 of 44

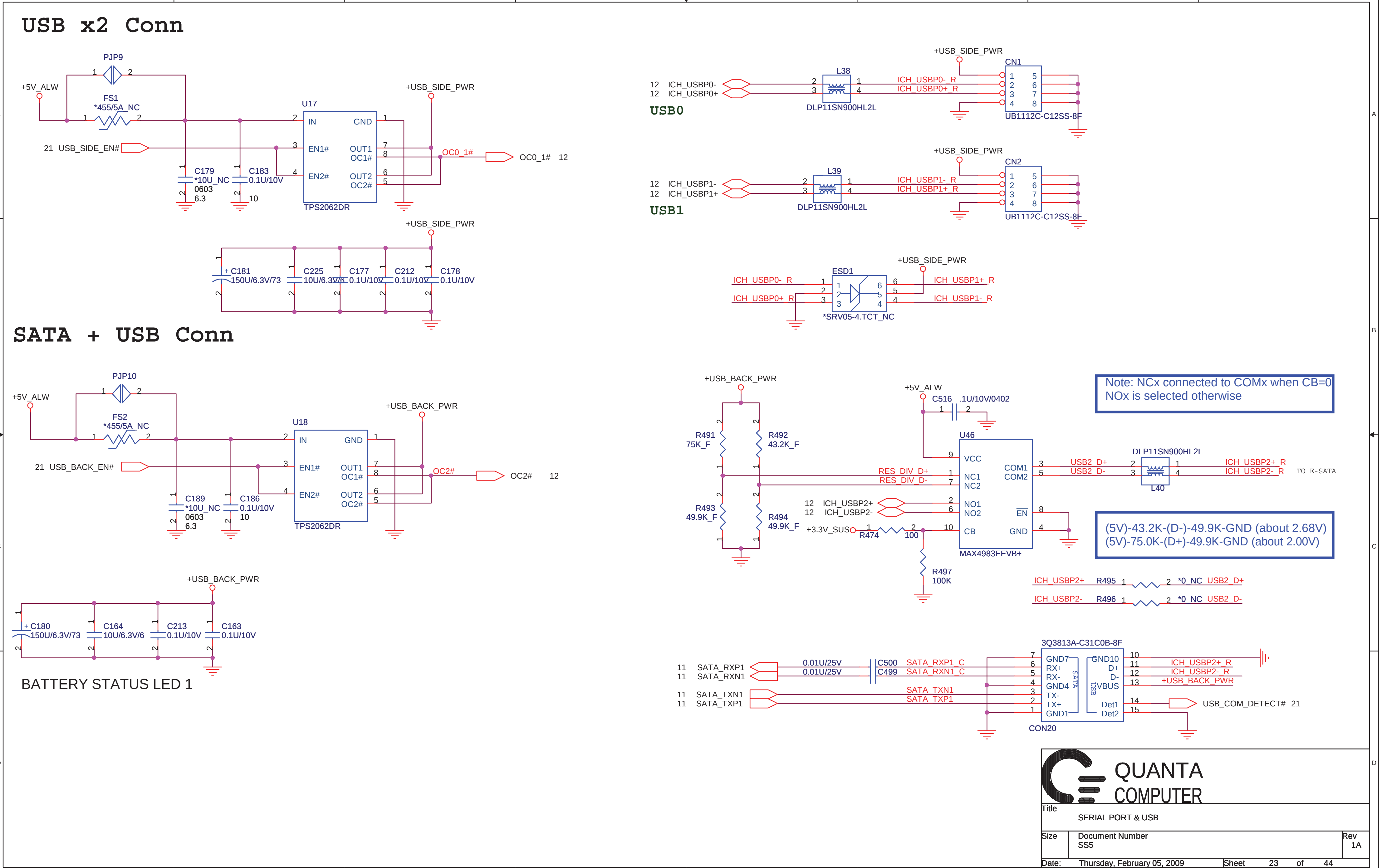


QUANTA COMPUTER

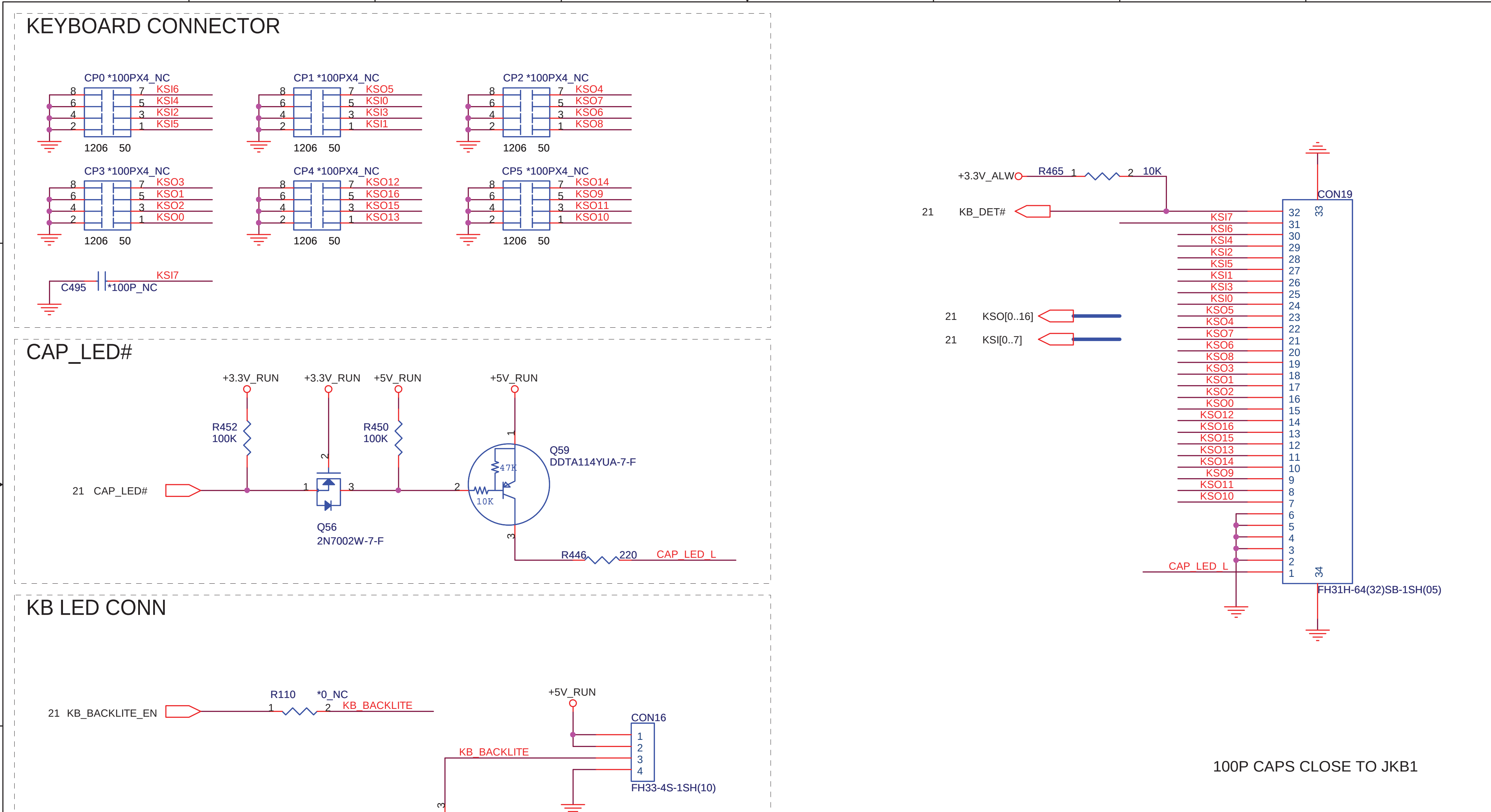
Title: All in one_100PIN

Size | Document Number: SS5 | Rev: 1A

Date: Thursday, January 08, 2009 | Sheet 22 of 44

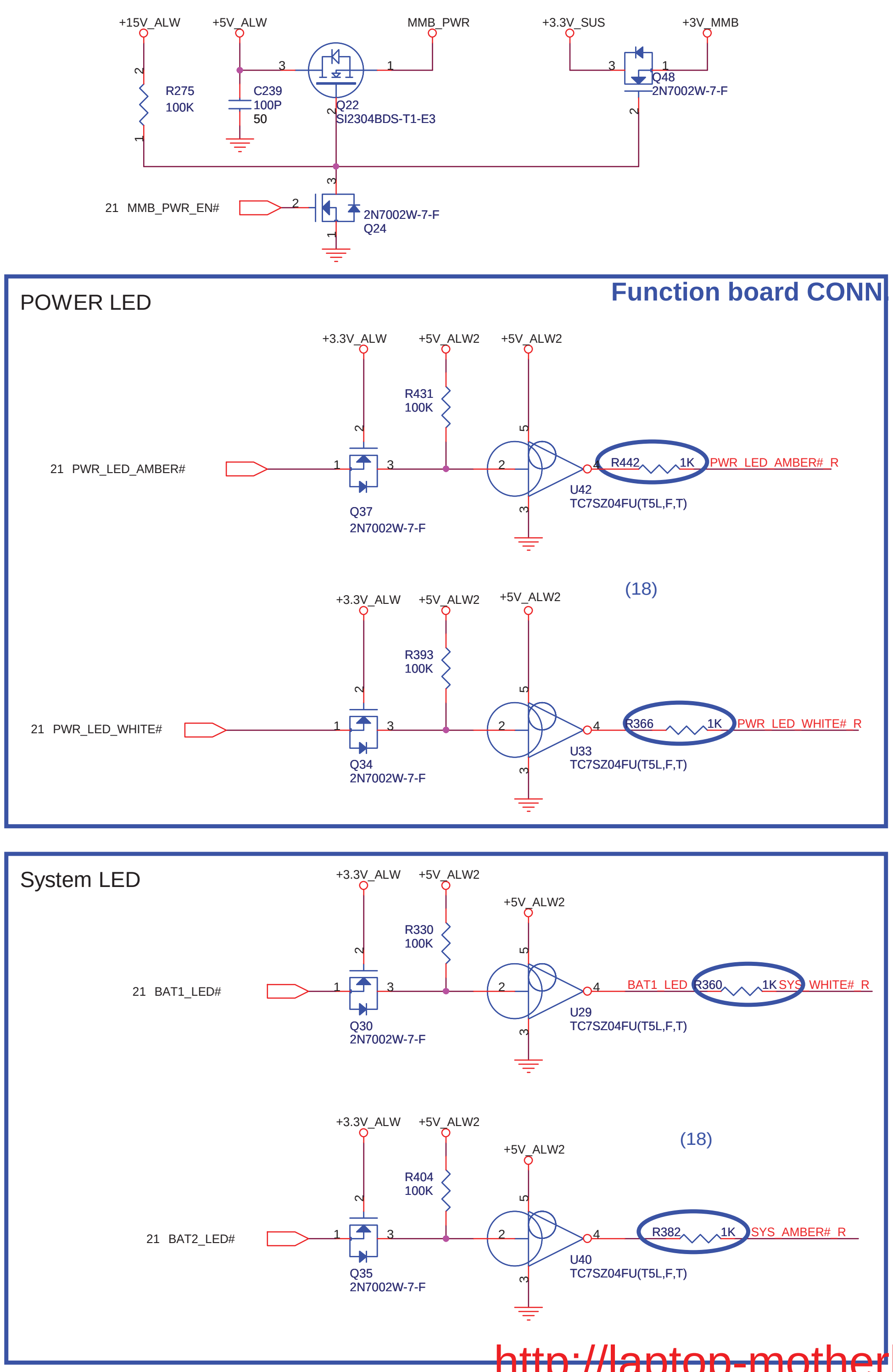


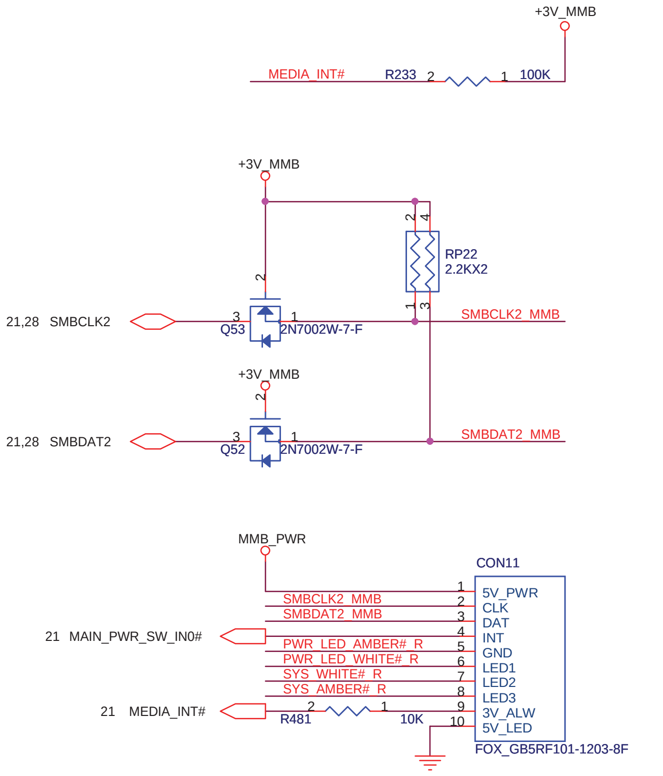
http://laptop-motherboard-schematic.blogspot.com/



QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number SS5	Rev 2A
Date:	Thursday, January 08, 2009	Sheet 24 of 44





System Power State	Power Source	Battery Charge State	LED Behavior
On (S0)	AC	0-100%	Off
On (S0)	DC	< 10%	Flash Amber
On (S0)	DC	> 10%	Off
Standby (S3)	AC	0-100%	"Breathe" White
Standby (S3)	DC	< 10%	Flash Amber
Standby (S3)	DC	> 10%	"Breathe" White
Off or Hibernate (S4/S5)	AC	< 90%	Solid Amber
Off or Hibernate (S4/S5)	AC	> 90%	Solid White
Off or Hibernate (S4/S5)	DC	0-100%	Off

QUANTA COMPUTER

Title: SWITCH, KEYBOARD & LED

Size | Document Number: SS5 | Rev: 1A

Date: Thursday, February 05, 2009 | Sheet 25 of 44

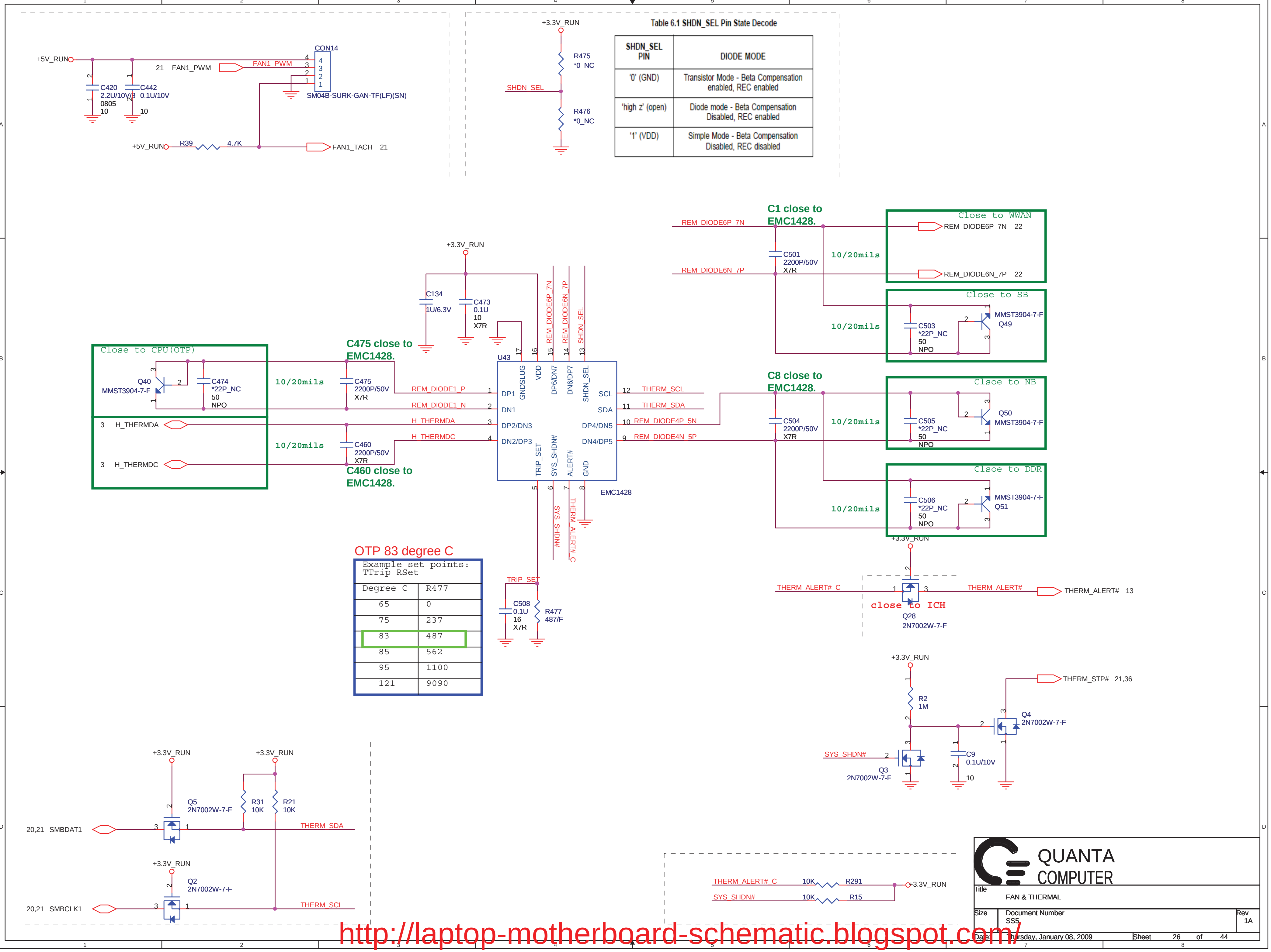


Table 6.1 SHDN_SEL Pin State Decode

SHDN_SEL PIN	DIODE MODE
'0' (GND)	Transistor Mode - Beta Compensation enabled, REC enabled
'high z' (open)	Diode mode - Beta Compensation Disabled, REC enabled
'1' (VDD)	Simple Mode - Beta Compensation Disabled, REC disabled

OTP 83 degree C

Example set points:
TTrip_RSet

Degree C	R477
65	0
75	237
83	487
85	562
95	1100
121	9090

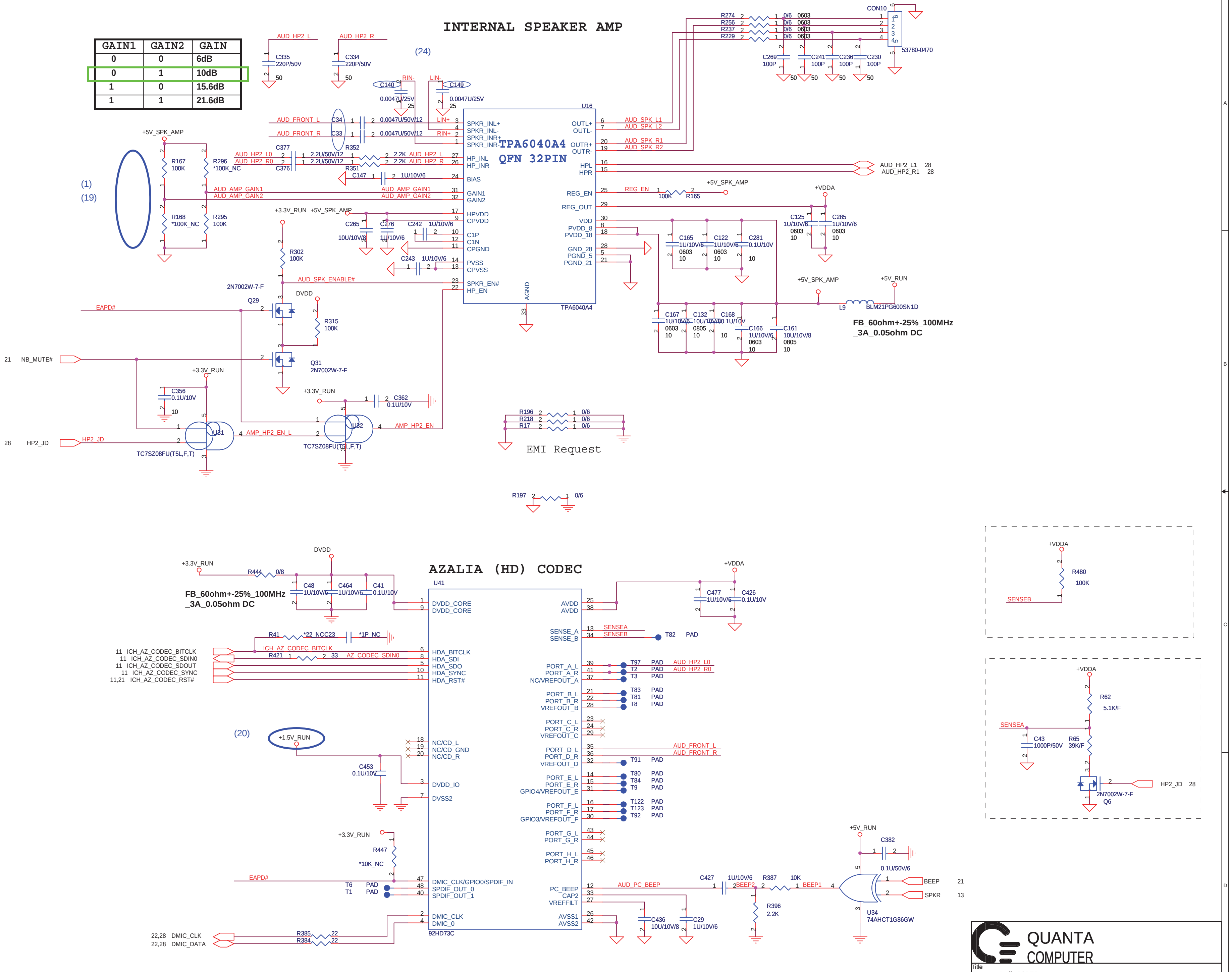
QUANTA COMPUTER

Title: FAN & THERMAL

Size | Document Number: SS5 | Rev 1A

Date: Thursday, January 08, 2009 | Sheet 26 of 44

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



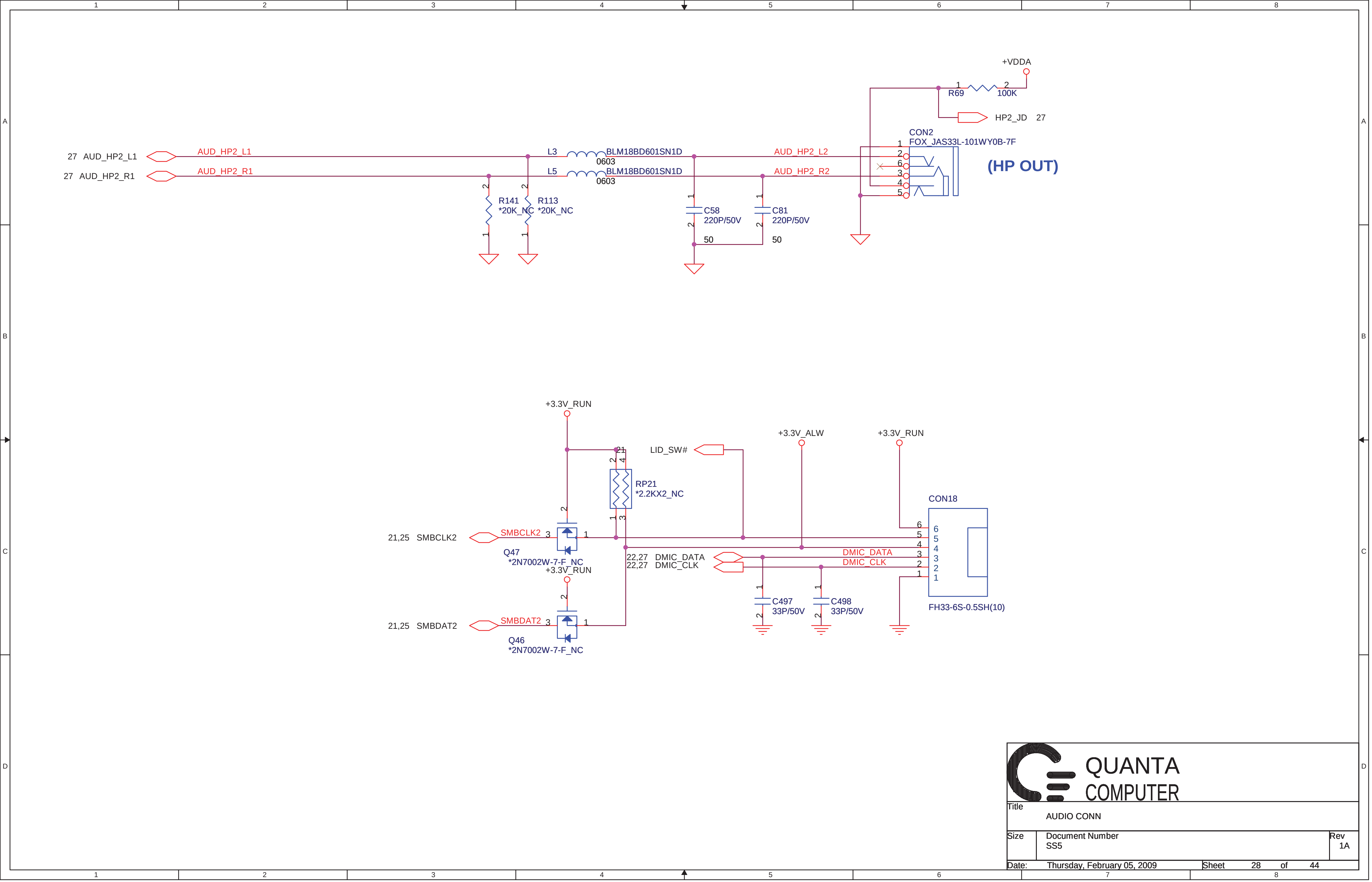
http://laptop-motherboard-schematic.blogspot.com/

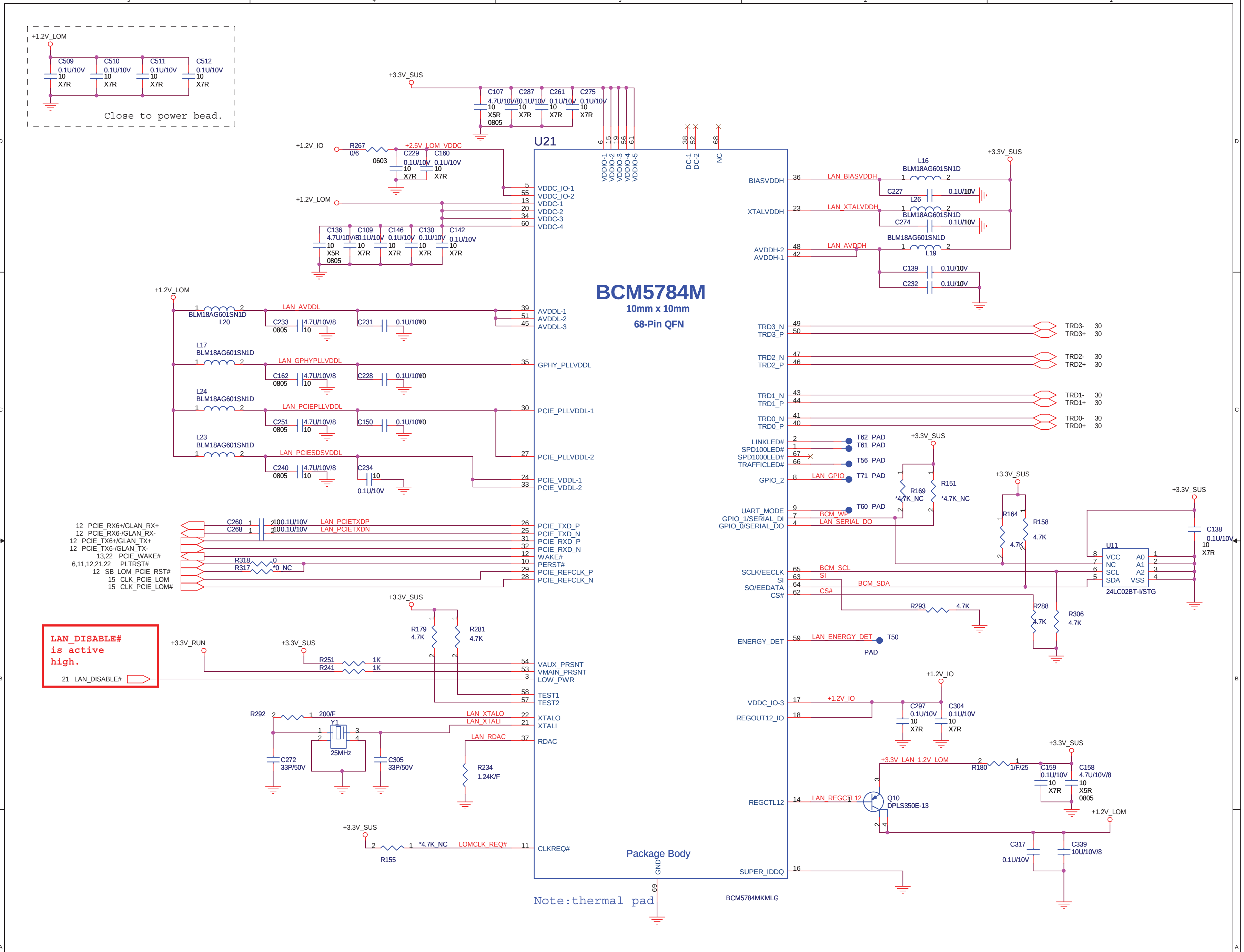
QUANTA COMPUTER

Title: Azalia CODEC

Size | Document Number: SS5 | Rev: 1A

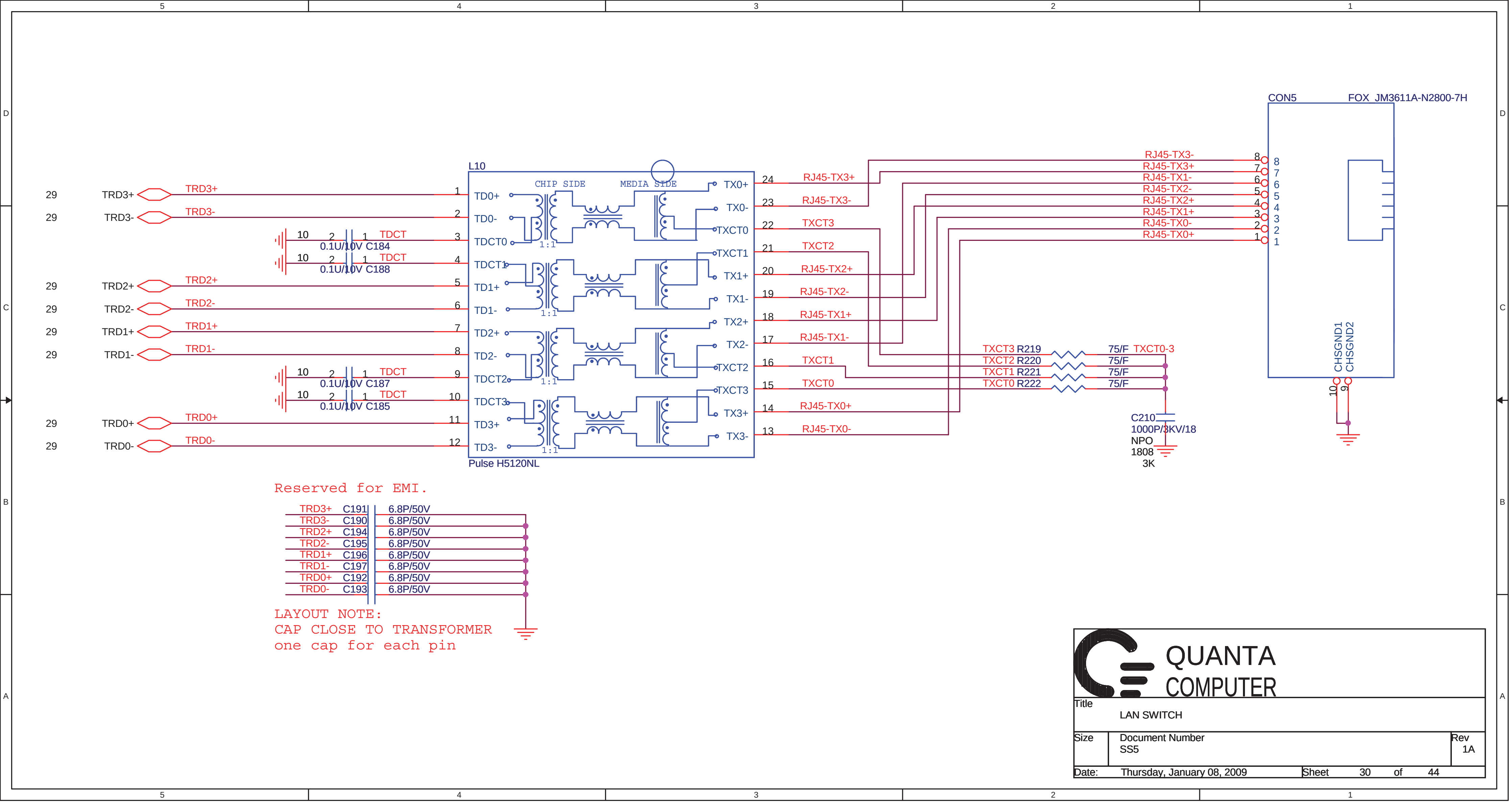
Date: Thursday, February 05, 2009 | Sheet 27 of 44


+VDDA
R69
100K
HP2_JD 27
CON2
FOX_JAS33L-101WY0B-7F
(HP OUT)
27 AUD_HP2_L1
27 AUD_HP2_R1
AUD_HP2_L1
AUD_HP2_R1
L3
L5
BLM18BD601SN1D
0603
BLM18BD601SN1D
0603
AUD_HP2_L2
AUD_HP2_R2
R141
*20K_NC
R113
*20K_NC
C58
220P/50V
50
C81
220P/50V
50
+3.3V_RUN
RP21
*2.2KX2_NC
LID_SW#
+3.3V_ALW
+3.3V_RUN
CON18
21,25 SMBCLK2
SMBCLK2
Q47
*2N7002W-7-F_NC
+3.3V_RUN
22,27 DMIC_DATA
22,27 DMIC_CLK
DMIC_DATA
DMIC_CLK
FH33-6S-0.5SH(10)
C497
33P/50V
C498
33P/50V
21,25 SMBDAT2
SMBDAT2
Q46
*2N7002W-7-F_NC
QUANTA
COMPUTER
Title
AUDIO CONN
Size
Document Number
SS5
Rev
1A
Date: Thursday, February 05, 2009
Sheet 28 of 44

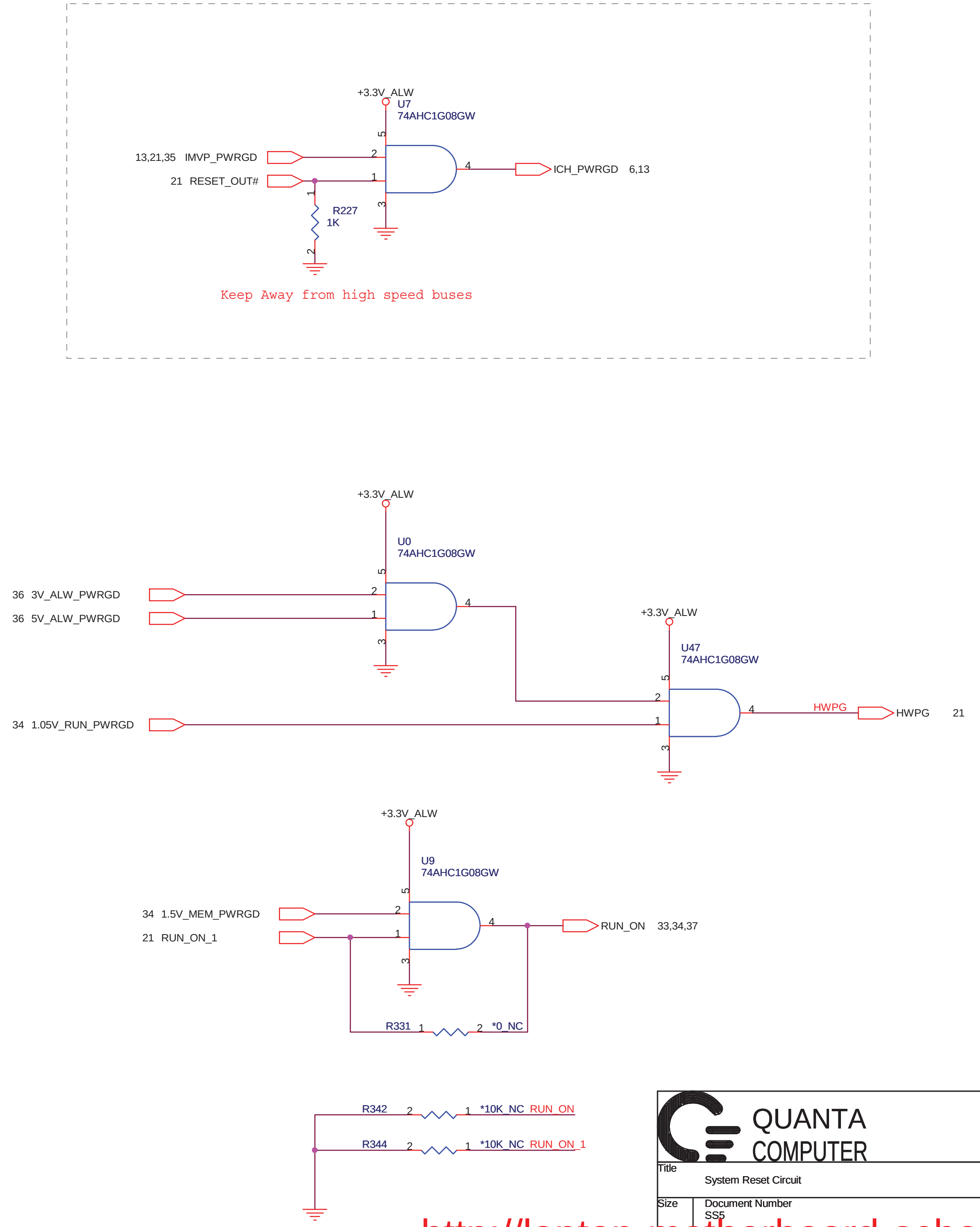


QUANTA COMPUTER

Title: LAN		
Size	Document Number: SS5	Rev: 1A
Date: Thursday, January 08, 2009	Sheet 29 of 44	



CON5
FOX JM3611A-N2800-7H
L10
CHIP SIDE
MEDIA SIDE
Pulse H5120NL
TD0+
TD0-
TDCT0
TDCT1
TD1+
TD1-
TD2+
TD2-
TDCT2
TDCT3
TD3+
TD3-
TX0+
TX0-
TXCT0
TXCT1
TX1+
TX1-
TX2+
TX2-
TXCT2
TXCT3
TX3+
TX3-
1:1
29 TRD3+
29 TRD3-
29 TRD2+
29 TRD2-
29 TRD1+
29 TRD1-
29 TRD0+
29 TRD0-
TDCT
0.1U/10V C184
0.1U/10V C188
0.1U/10V C187
0.1U/10V C185
RJ45-TX3+
RJ45-TX3-
TXCT3
TXCT2
RJ45-TX2+
RJ45-TX2-
RJ45-TX1+
RJ45-TX1-
TXCT1
TXCT0
RJ45-TX0+
RJ45-TX0-
RJ45-TX3-
RJ45-TX3+
RJ45-TX1-
RJ45-TX2-
RJ45-TX2+
RJ45-TX1+
RJ45-TX0-
RJ45-TX0+
CHSGND1
CHSGND2
TXCT3 R219 75/F TXCT0-3
TXCT2 R220 75/F
TXCT1 R221 75/F
TXCT0 R222 75/F
C210
1000P/3KV/18
NPO
1808
3K
Reserved for EMI.
TRD3+ C191 6.8P/50V
TRD3- C190 6.8P/50V
TRD2+ C194 6.8P/50V
TRD2- C195 6.8P/50V
TRD1+ C196 6.8P/50V
TRD1- C197 6.8P/50V
TRD0+ C192 6.8P/50V
TRD0- C193 6.8P/50V
LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin
QUANTA
COMPUTER
Title
LAN SWITCH
Size
Document Number
SS5
Rev
1A
Date: Thursday, January 08, 2009
Sheet 30 of 44

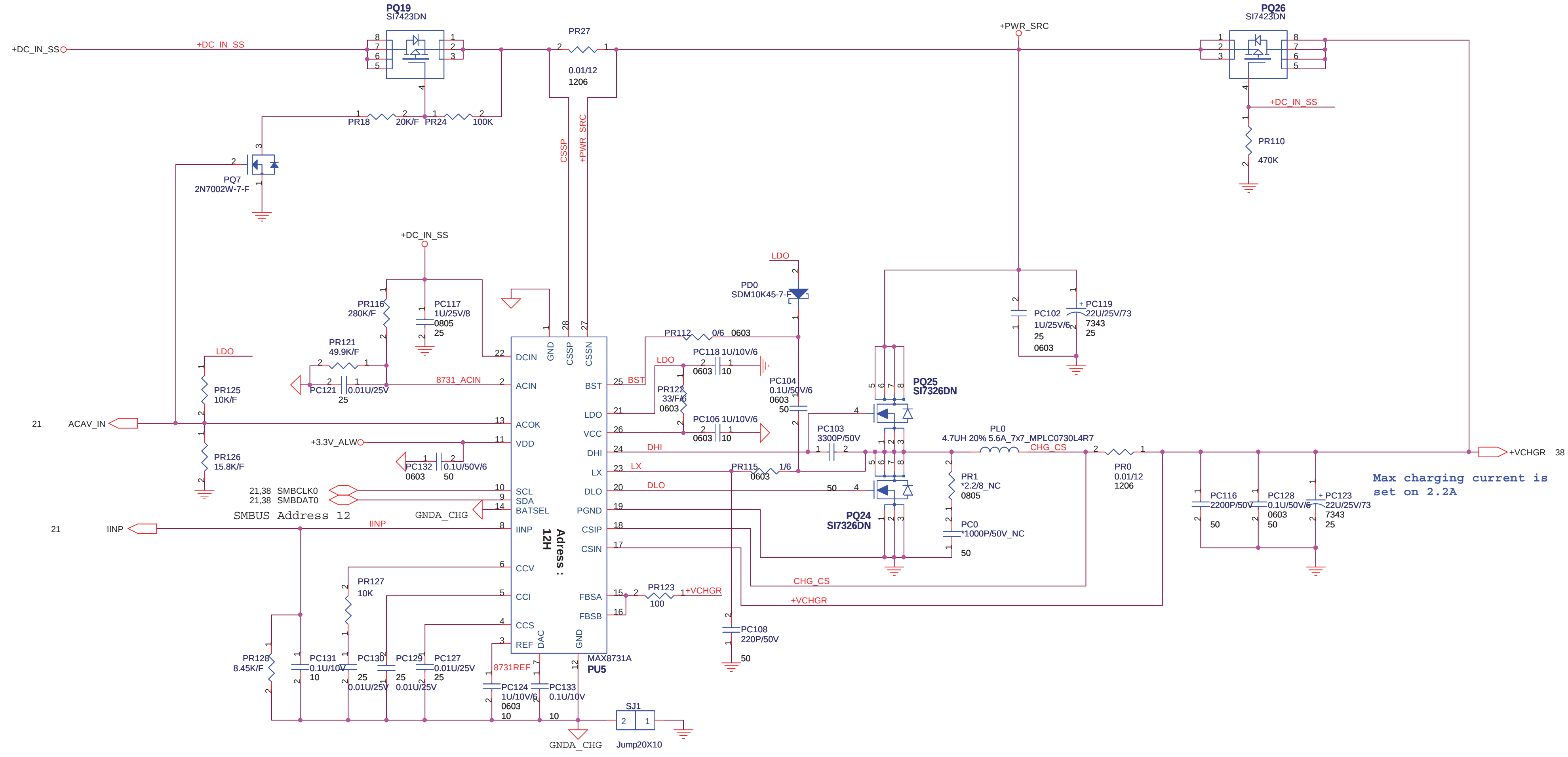


QUANTA COMPUTER

Title: System Reset Circuit

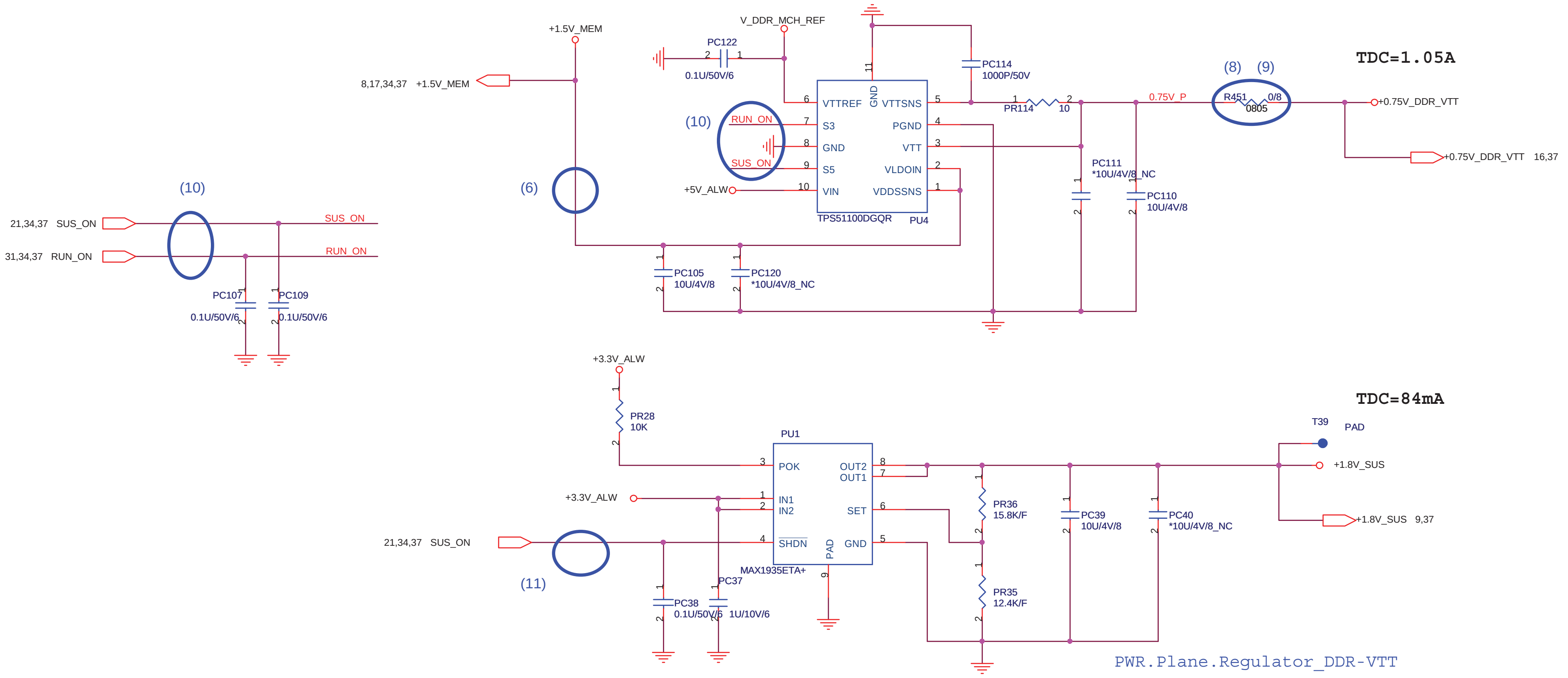
Size | Document Number: SS5 | Rev: 1A

Date: Thursday, January 08, 2009 | Sheet 31 of 44



QUANTA COMPUTER

Title	Charger (MAX8731)	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 32 of 44	



QUANTA COMPUTER

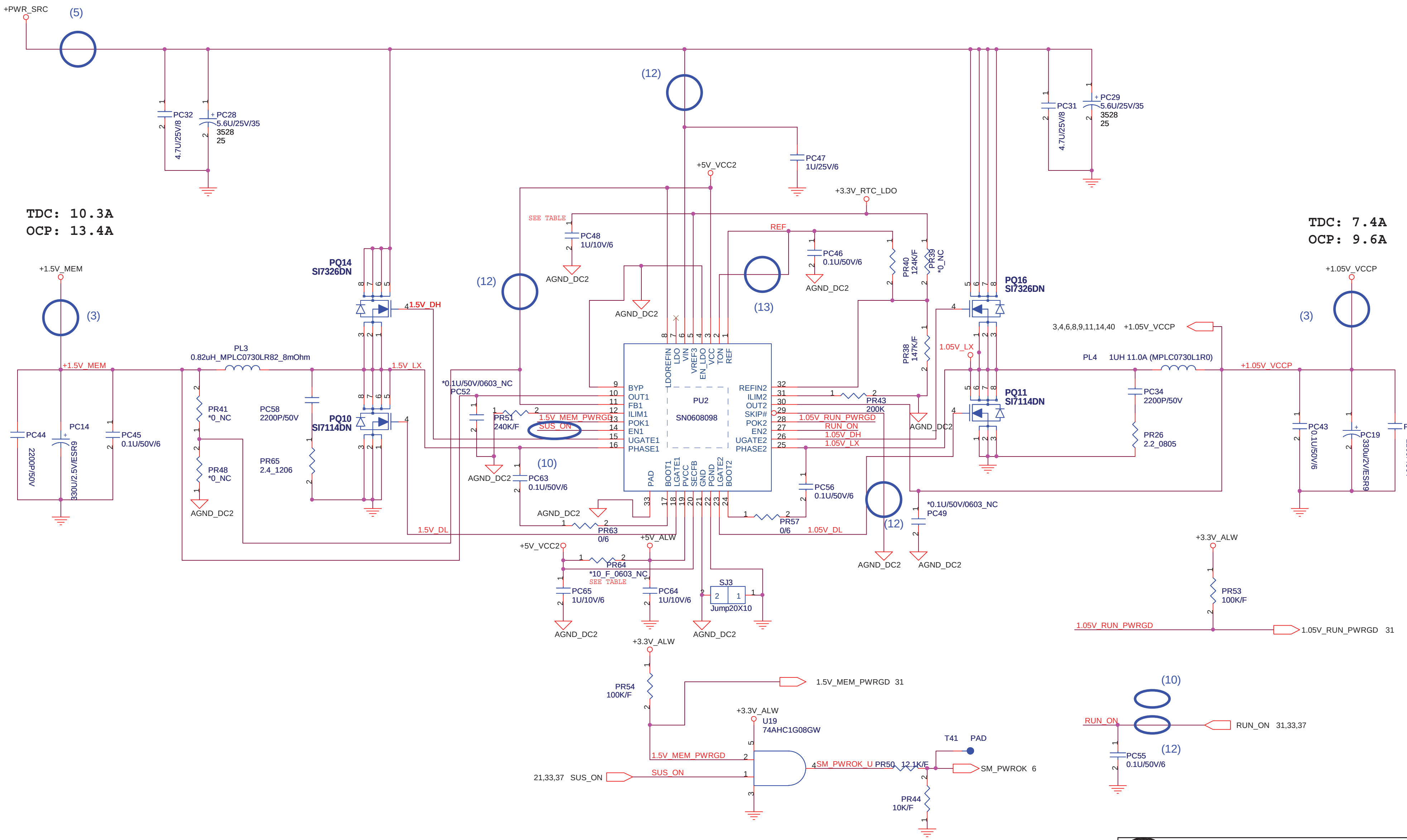
Title: 0.75V_DDR_VTT, 1.8V_RUN

Size	Document Number	Rev
	SS5	1A

Date: Thursday, January 08, 2009 Sheet 33 of 44

M'09

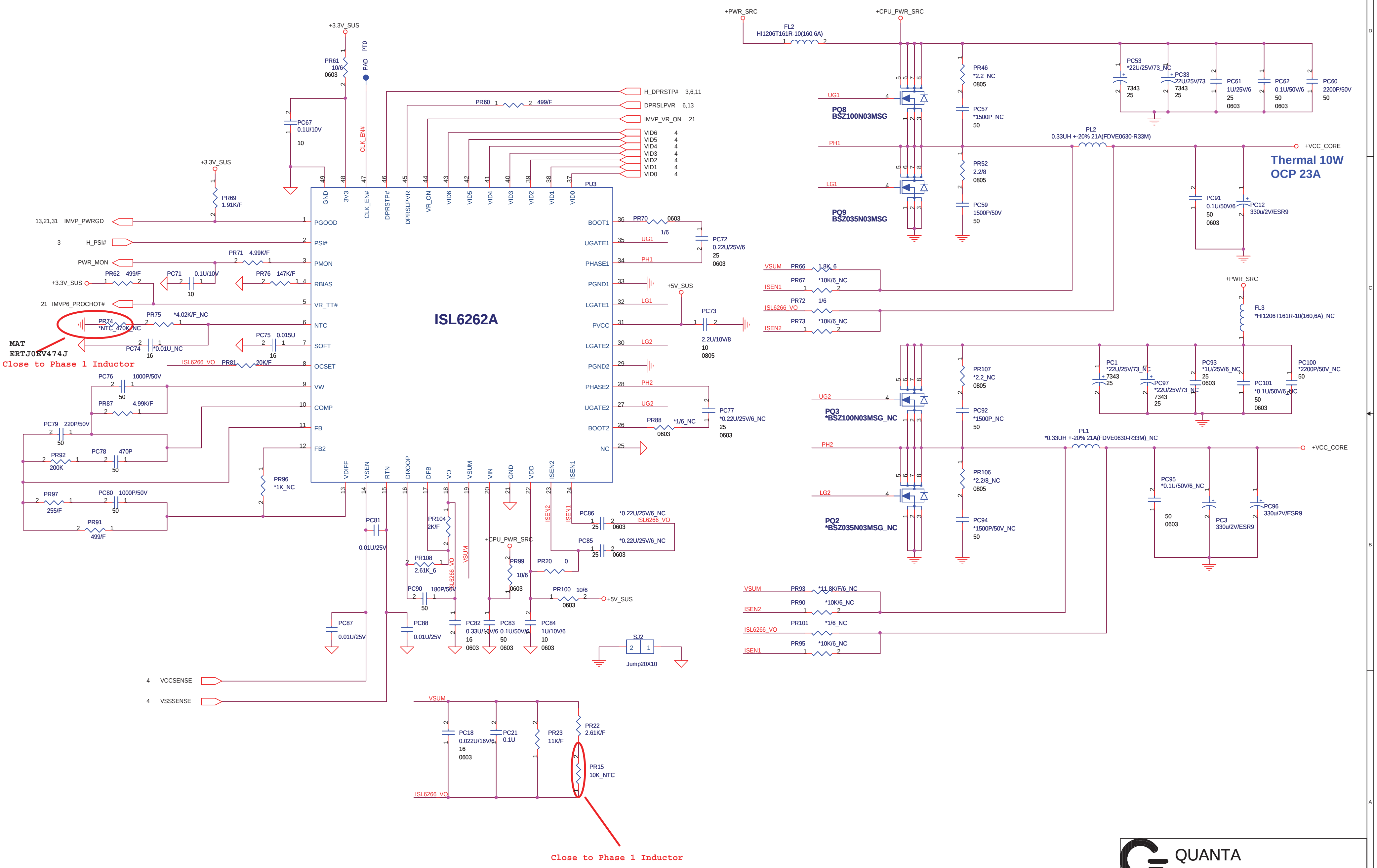
+1.5V_MEM /+1.05V_VCCP /+3.3_RTC_LDO



REF DESIGNATOR	MAXIM	INTERSIL	TI
PR64	10, 0603	NO STUFF	NO STUFF
PC48	1uF	0.1uF	1uF

QUANTA COMPUTER

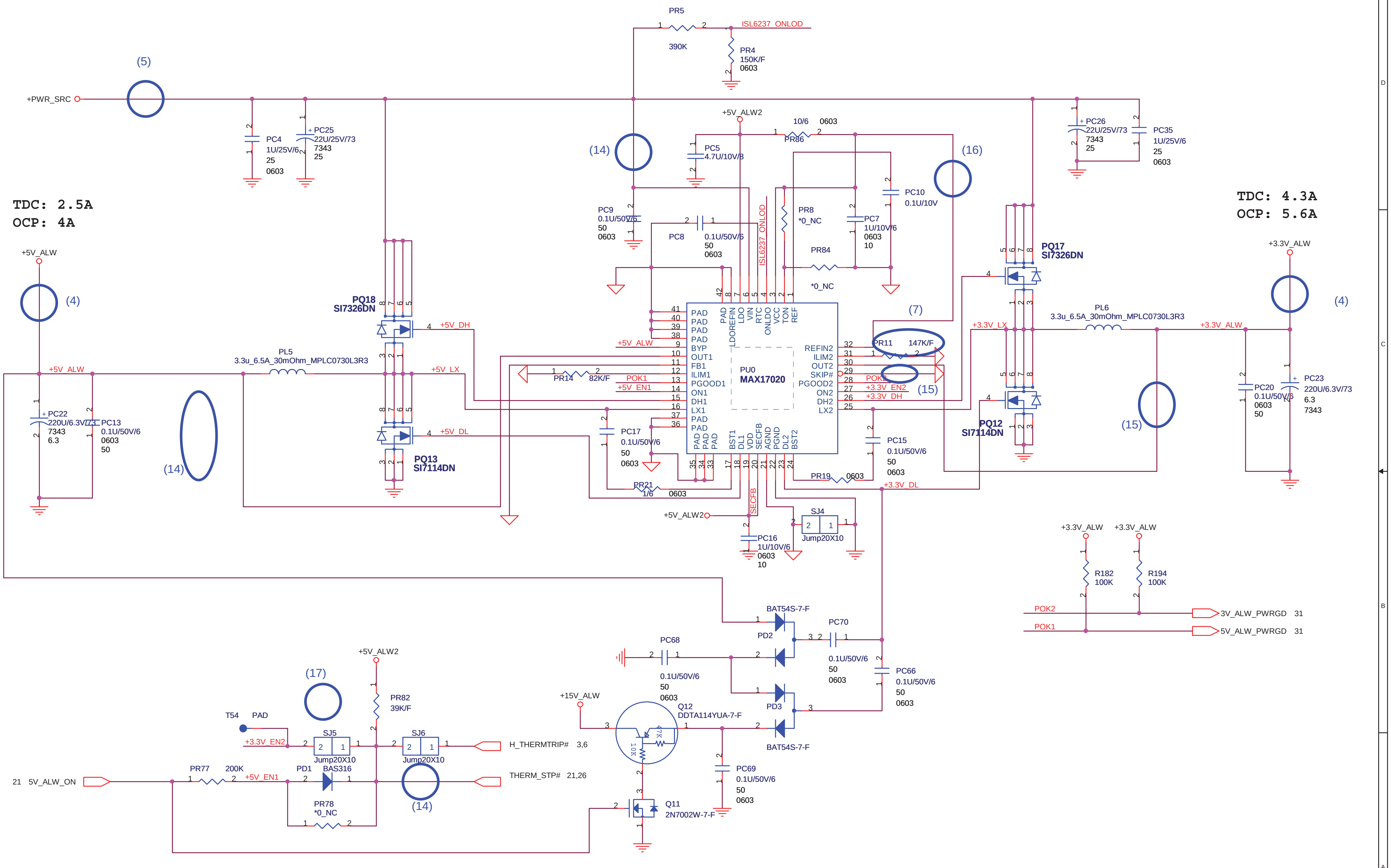
Title	1.05V_VCCP & 1.5V_MEM	
Size	Document Number SS5	Rev 1A
Date: Friday, February 20, 2009	Sheet 34 of 44	



QUANTA COMPUTER

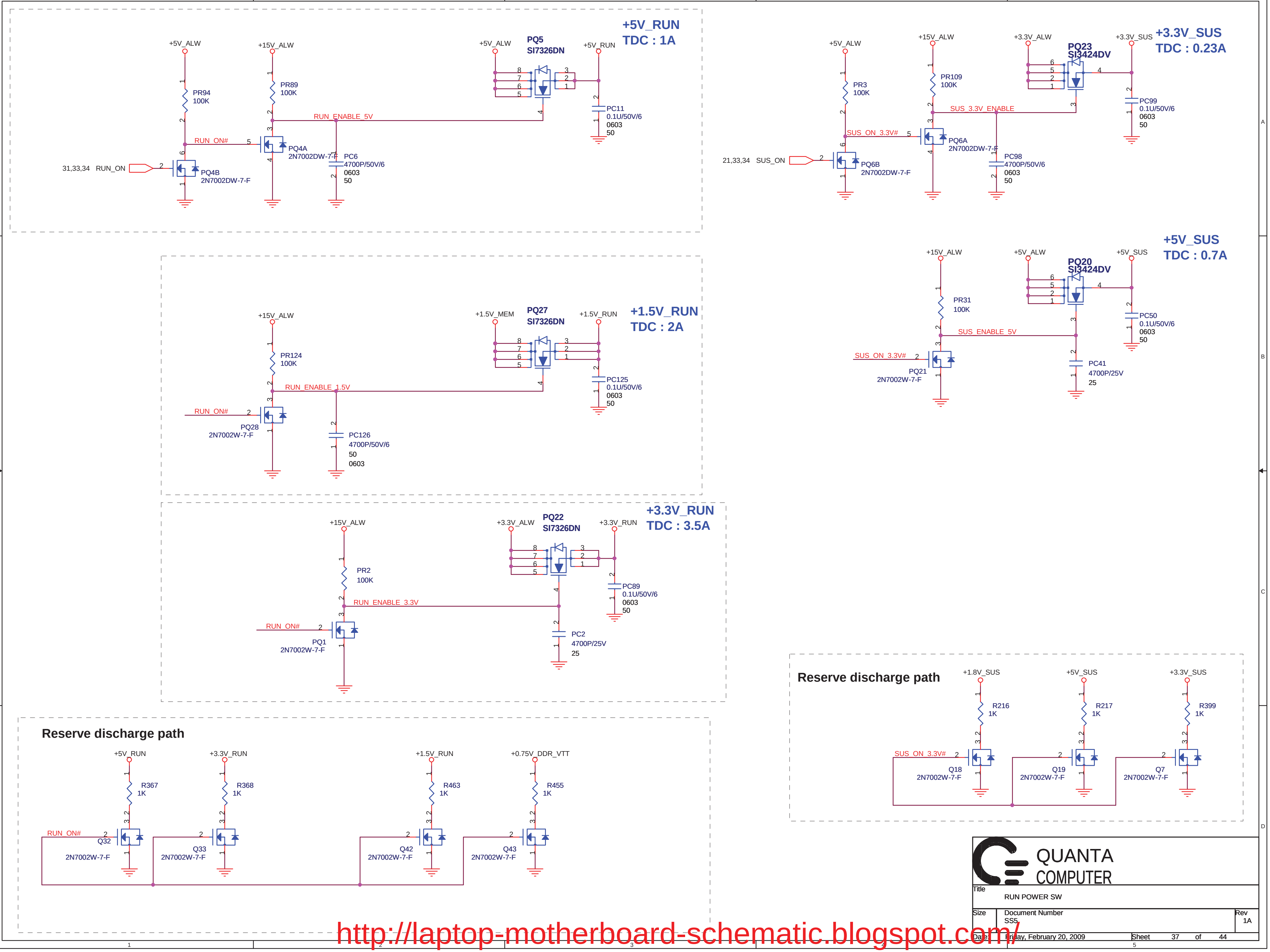
Title	CPU_Core_2Phase (ISL6266)	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 35 of 44	

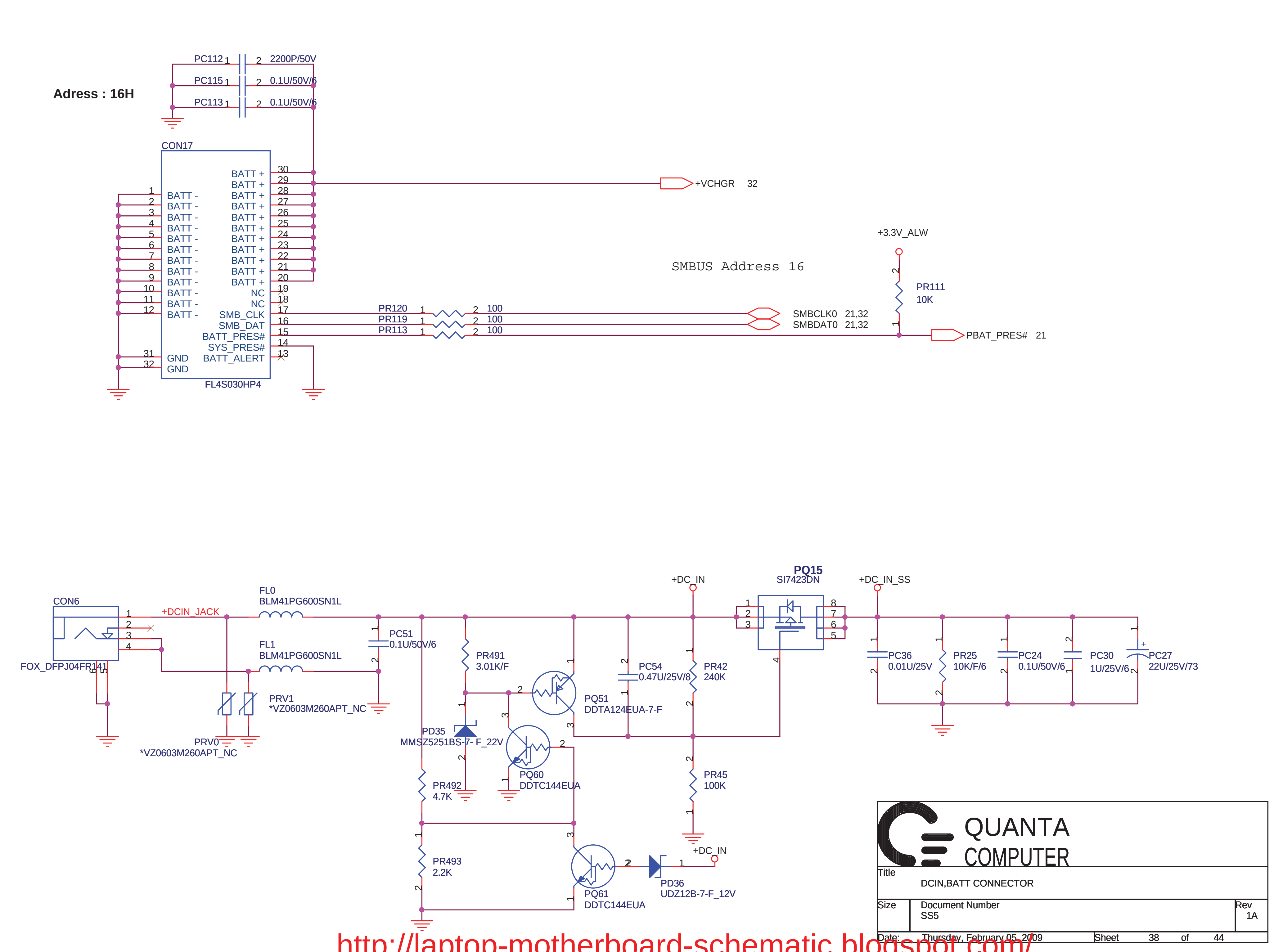
DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



QUANTA COMPUTER

Title	3VALW,5V,3V, Power On	
Size	Document Number SS5	Rev 1A
Date	Thursday, January 08, 2009	Sheet 36 of 44


+5V_RUN
TDC : 1A
+5V_ALW
+15V_ALW
PR94
100K
PR89
100K
RUN_ENABLE_5V
RUN_ON#
PQ4A
2N7002DW-7-F
PC6
4700P/50V/6
0603
50
31,33,34
RUN_ON
PQ4B
2N7002DW-7-F
PQ5
SI7326DN
+5V_RUN
PC11
0.1U/50V/6
0603
50
+3.3V_SUS
TDC : 0.23A
+3.3V_ALW
PQ23
SI3424DV
PR3
100K
PR109
100K
SUS_3.3V_ENABLE
SUS_ON_3.3V#
PQ6A
2N7002DW-7-F
21,33,34
SUS_ON
PQ6B
2N7002DW-7-F
PC98
4700P/50V/6
0603
50
PC99
0.1U/50V/6
0603
50
+5V_SUS
TDC : 0.7A
PQ20
SI3424DV
PR31
100K
SUS_ENABLE_5V
PQ21
2N7002W-7-F
PC50
0.1U/50V/6
0603
50
PC41
4700P/25V
25
+1.5V_RUN
TDC : 2A
+1.5V_MEM
PQ27
SI7326DN
PR124
100K
RUN_ENABLE_1.5V
PQ28
2N7002W-7-F
PC126
4700P/50V/6
50
0603
PC125
0.1U/50V/6
0603
50
+3.3V_RUN
TDC : 3.5A
PQ22
SI7326DN
PR2
100K
RUN_ENABLE_3.3V
PQ1
2N7002W-7-F
PC89
0.1U/50V/6
0603
50
PC2
4700P/25V
25
Reserve discharge path
+1.8V_SUS
R216
1K
R217
1K
R399
1K
Q18
2N7002W-7-F
Q19
2N7002W-7-F
Q7
2N7002W-7-F
Reserve discharge path
+0.75V_DDR_VTT
R367
1K
R368
1K
R463
1K
R455
1K
Q32
2N7002W-7-F
Q33
2N7002W-7-F
Q42
2N7002W-7-F
Q43
2N7002W-7-F
QUANTA
COMPUTER
Title
RUN POWER SW
Size
Document Number
SS5
Rev
1A
Date
Friday, February 20, 2009
Sheet 37 of 44



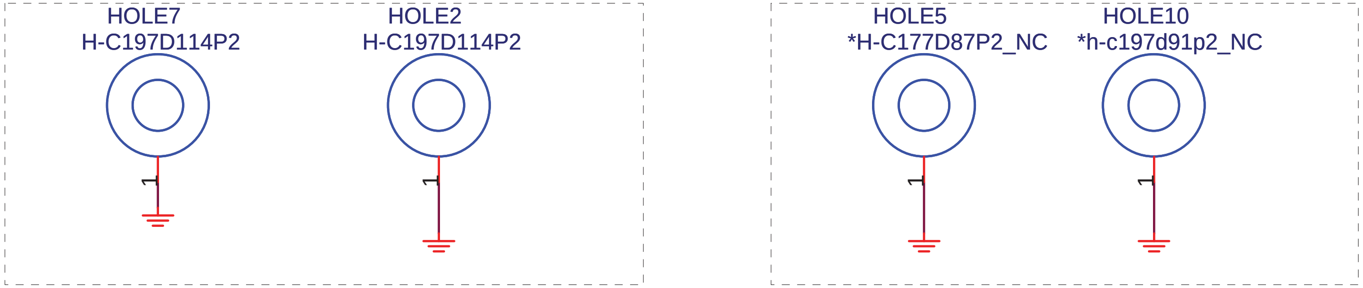
QUANTA COMPUTER

Title: DCIN,BATT CONNECTOR

Size | Document Number: SS5 | Rev: 1A

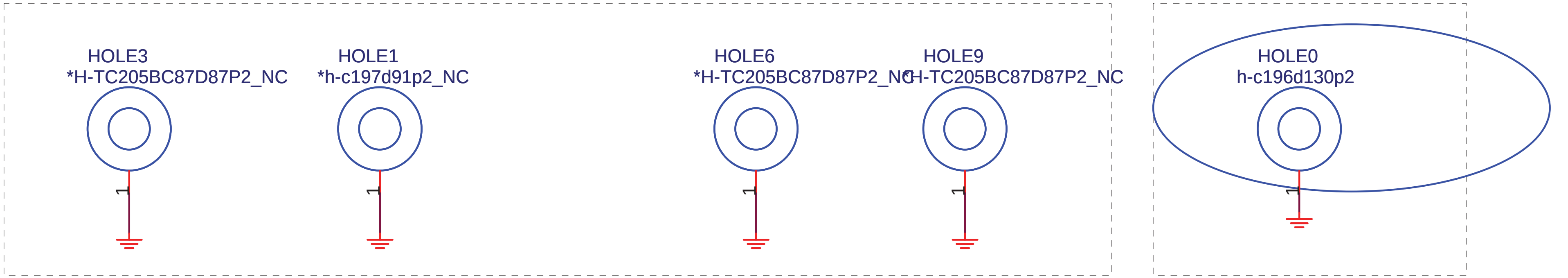
Date: Thursday, February 05, 2009 | Sheet 38 of 44

Thermal Screw



Housing Screw

Outer diameter = 4.5mm

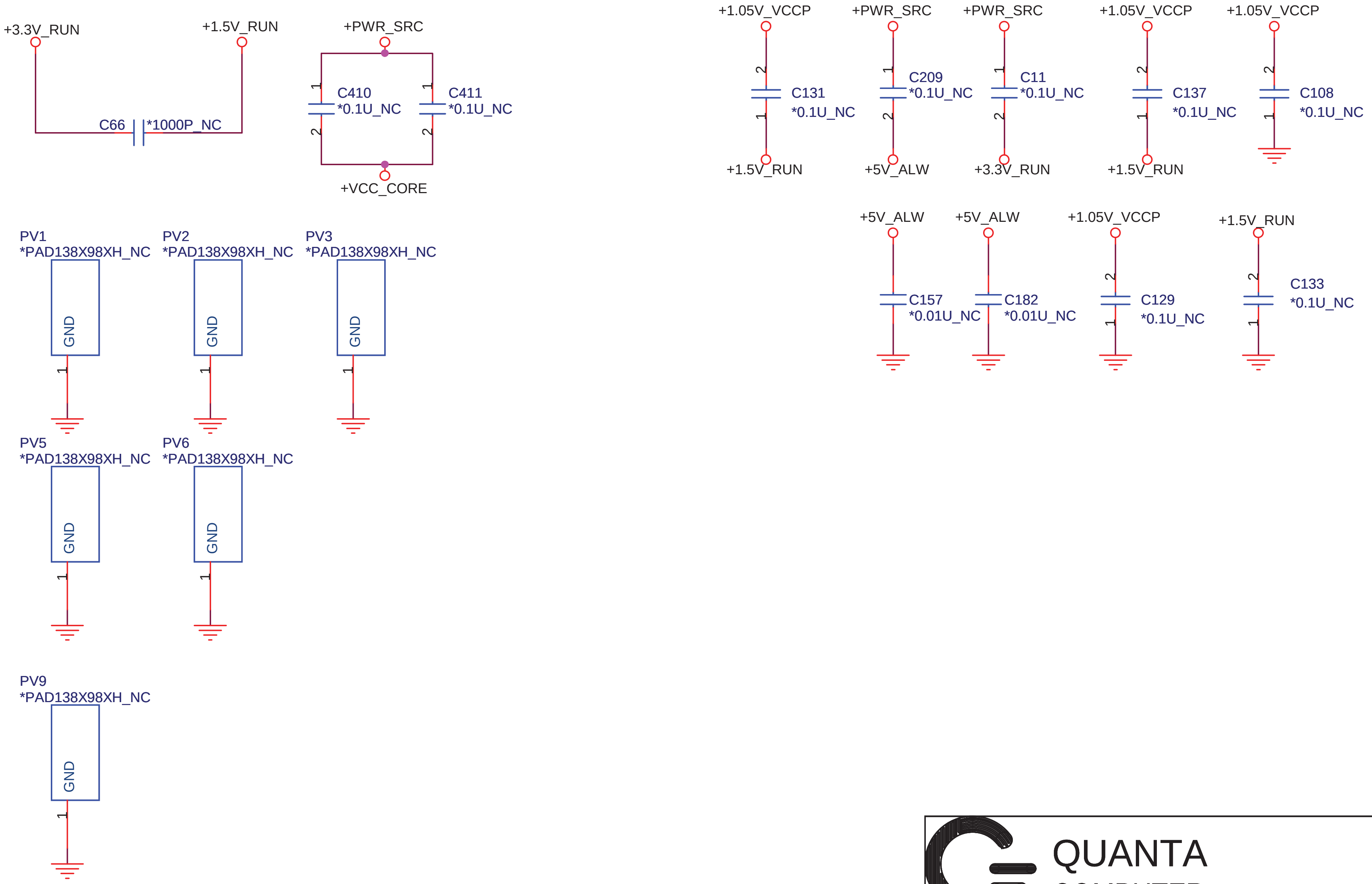


P/N is ok.
Also need change FP 12/29.

QUANTA COMPUTER

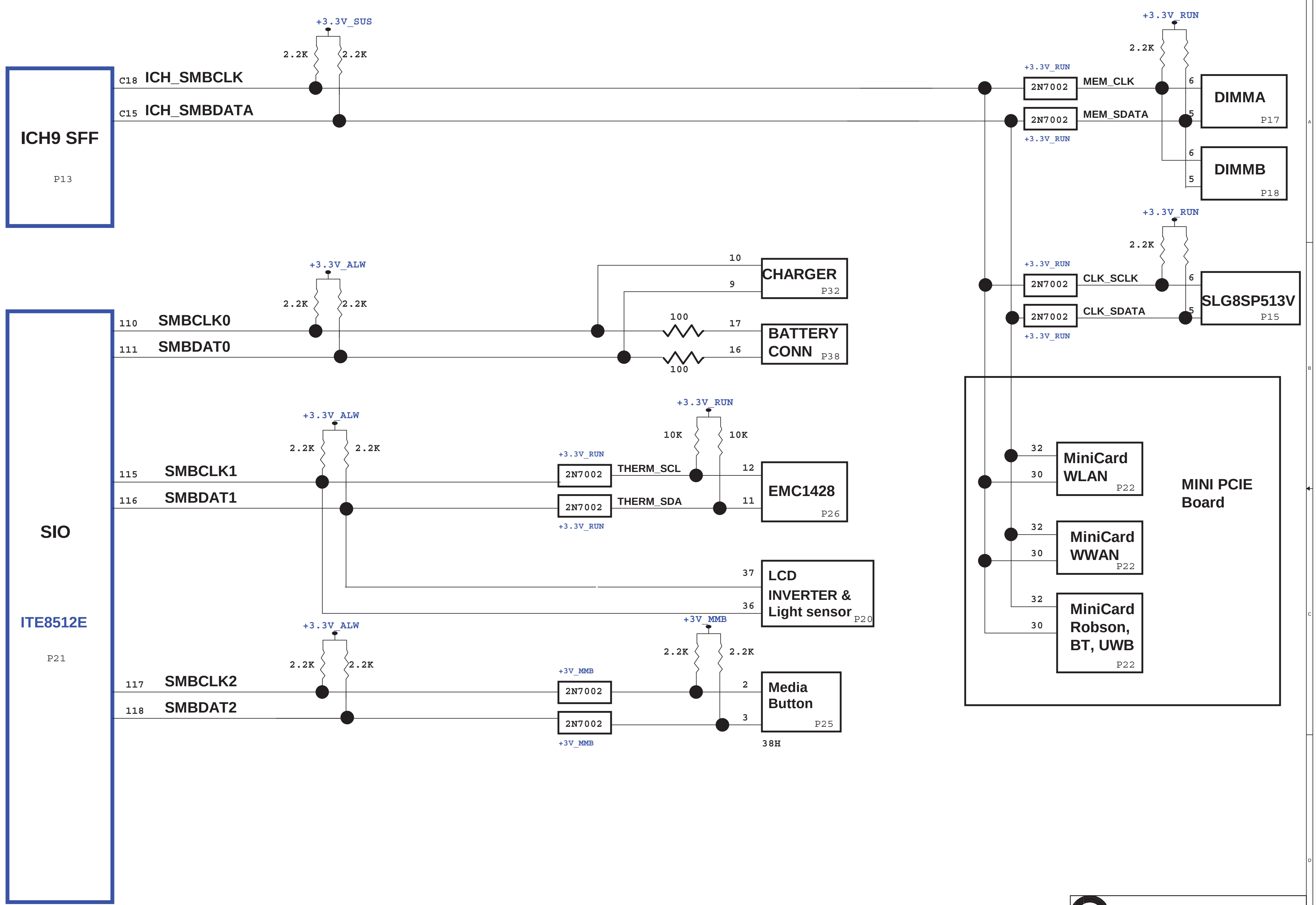
Title	SCREW PAD	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 39 of 44	

Reserved for EMI.   Stitching caps.



QUANTA COMPUTER

Title	EMI CAP	
Size	Document Number SS5	Rev 1A
Date: Thursday, January 08, 2009	Sheet 40 of 44	



QUANTA COMPUTER

Title	SMBUS BLOCK
Size	Document Number: FX6 — Rev: 3A
Date:	Thursday, January 08, 2009 — Sheet 41 of 44

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00 change to X00.1		
1	12	5/20/2008	EE	Schematic have pull up resistor and pull down resistor. Remove all pull up resistor for those signal. SB_WWAN_PCIE_RST#, SB_LOM_PCIE_RST#, SB_WPAN_PCIE_RST#, SB_WLAN_PCIE_RST# and SB_NB_PCIE_RST#.	Depop R361, R133, R72, R407, R74.	X00.1
2	20, 28	5/20/2008	EE	LCD and CCD connect need combin as one connect. Del Camera connect (P28) and change (P20)J1 from 30pin to 44pin. Move 2 USB and 1 Combo connect to MB.	Del CON12(P28) and move rest of Camera componets to P20. Change J1 from 30pin to 44pin.	X00.1
3	23	5/20/2008	EE	Move IO Board connect (2 USB and 1 E-Sata) to Mother Board side.	Add L38, R468, R469, CN1 For USB0 Add L39, R470, R471, CN2 and ESD1 for USB1. Add L40, R472, R473, CON20 for USB2 & E-SATA	X00.1
4	23	5/20/2008	EE	To support USB charger function, Added USB Switch to solve leakage issue.	Added U46 and R474 USB Switch circuit.	X00.1
5	23	5/20/2008	EE	Follow safety design, added Fuse on USB power avoide TPS2062DR no function.	Added PJP9 and FS1_NC for USB0 and USB1. Added PJP10 and FS2_NC for USB3.	X00.1
6	3, 26	5/20/2008	EE	Follow Thermal requirement to measured OTP, CPU, NB, DDR, SB and WWAN temperature.	Added C501, C502, Q48, C503, Q49 for DDR and NB. Added C504, C505, Q50, C506, Q51 for SB and WWAN Added rest of EMC1428 components C508, R477, R475, R476	X00.1
7	12, 23	5/20/2008	EE	For USB P0/P1 use same power rail. Change over current design. Change net OC0# and OC1# to OC0_1#.	Change U17.5 and U17.8 to net OC0_1#. Remove R132.	X00.1
8	25	5/21/2008	EE	Change MMB connect from 15pin to 10pin. Remove Media Buttom function. Added System LED signal on MMB connect.	Change CON11 from 15pin to 10pin. Added SYS_WHITE#_R and SYS_AMBER#_R signal MMB connect.	X00.1
9	28	5/21/2008	EE	Follow ME/ID requirement. Change Audio connect type.	Udate CON2 symbol and footprint.	X00.1
10	38	5/21/2008	EE	Follow ME/ID requirement. Change DC_IN Jack connect type.	Udate CON6 symbol and footprint.	X00.1
11	11	5/23/2008	EE	ME Z-Hing limite, need change RTC type to small size. It need support charge function.	Chnge CON1 footprint and Added R202 1kohm support charge.	X00.1
12	13, 22	5/23/2008	EE	Added USB_MCARD3 detect pin for WWAN card.	Added input port on USSB_MCARD3 and connect to CON15.21	X00.1
13	18	5/23/2008	EE	Memory A and B chanel have same SMBUS address. Change SMBUS address to A4.	Change R147 from pull low to pull up +3.3V_RUN.	X00.1
14	19	5/23/2008	EE	Display Port need chnge to TOP mount type. Change new Connect Footprint.	Change CON7 symbol and Footprint.	X00.1
15	20, 21	5/23/2009	EE	Added SMBUS signal and connection to LCD Connect(J1).	Added SMB_CLK1 form U35.115 to J1.6. SMB_DAT1 from U35.116 to J1.5.	X00.1
16	21, 31	5/23/2009	EE	Remove GPIO diode on GPD0, GPF1 and GPF2.	GPF0 -> SIO_SLP_S3# solve S5 can enter issue. (Remove D0) GPF1 -> IMVP_PWRGD input pin, can't havd diode. (Remove D17) GPF2 -> RESET_OUT# out put pin, don't have leakage concerm. (Remove D7 and R110)	X00.1
17	22, 27	5/23/2009	EE	ME define MIC connect on MB side.Remove MIC signal to 100 pin connect. Change those 2 pin for Thermal Diode signal(WWAN).	REM_DIODE6P_7N -> CON15.98 connection to U43.15 REM_DIODE6N_7P -> CON15.99 connection to U43.14	X00.1
18	22	5/23/2009	EE	ID don't support WLAN/WWAN/WPAN LED. Remove LED signal from CON15. Added 1 pin +5VRUN.	Remove out LED_WWAN#/ LED_BT_UWB# / LED_WLAN_OUT#. CON15-21,56 and 87pin	X00.1
19	23	5/23/2009	EE	Change USB connect layout footprint.	Change CN1 schematic symbol and layout footprint. Change CN2 schematic symbol and layout footprint.	X00.1
20	23	5/23/2009	EE	Change E-Sata/USB connect layout footprint. Added detect# signal for detect USB plug in.	Change CON20 E-Sata/USB connect layout footprint. Connection CON20.14 (USB_COM_DETECT#) to EC.	X00.1
21	24	5/23/2009	EE	Sync with ME and EE keyboard Matrix. Update Footprint.	Update CON19 layout footprint and reserve keyboard pin to match M09 keyboard.	X00.1
22	25	5/23/2009	EE	Power LED and System LED need light during S5. Due to S5 state, +5V-ALW will turn off.	Change R431, U42.5, R393, U33.5, R330, U29.5, R404, U40.5 from +5V_ALW to +5V_ALW2.	X00.1
23	21	5/23/2009	EE	Move Back R233 to MB. Reserved GPIO pull up for EC WUI pin.	Move R233 pull up (+3.3V_ALW) to U35.124 Media_INT#.	X00.1
24	9	5/23/2009	EE	Follow Intel Reference Design. Added AC terminal RC.	Added R479 (0.51ohm) and C502 (22uF) on +1.05M_MPLL	X00.1
25	27	5/23/2009	EE	Add R480 100k on 92HD73C pin 13 SENSEA.	Add R480 100k on 92HD73C pin 13 SENSEA.	X00.1
26	32	5/23/2009	P	Change ACIN threshole to 11.9V from 17V	Change PR116 from 365K/F ohm to 240K/F ohm.	X00.1
27	38	5/23/2009	P	Change to +5V_ALW from +5V_ALW2.	Chanage PR3 pin1 to +5V_ALW from +5V_ALW2.	X00.1
28	38	5/26/2009	P	Change CON17 to FLS030HP1 and update footprint.	Change CON17 footprint to fl4sxxxhp1-30p-r	X00.1
29	38	5/26/2009	EE	Follow layout request to exchange signals.	Exchange CP0, CP2, CP3, CP4, CP5, L18 signals for layout request.	X00.1
30	29	5/28/2009	EE	Follow BCM recommand. Change Pin 27 to correct power rail and add 0.1uF*4 for π type filter.	Change U21.27 to U21.30 and Add C509~C512 at +1.2V_LOM.	X00.1
31	9	5/29/2009	EE	Depop R118 to let VCC_HDA connect to GND.	Depop R118 0 ohm.	X00.1
32	25	5/29/2009		The different power rail between MMB and SIO. Need added level circuit.	Added Q48, Q53, Q52, RP22level shift circuit.	

QUANTA COMPUTER

PROJECT : SS5	DOC. NO. : 204	REV: X00		Title: Change List1 — QUANTA
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tsing	DATE : May. 19, 2008 SHEET : OF : 11	Size / Document Number: SS5 — COMPUTER — Rev: 1A
				Date: Thursday, January 08, 2009 — Sheet 42 of 44

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
				X00.1 change to X01		
33	32	6/10/2008	EE	Change AC_IN volt threshold on 13.5V with a 280K resister of PR116	Change PR116 from 240K to 280K	X01
34	32	6/11/2008	EE	Change to SI7326 for 2.2A charging	Change PQ24 from SI7114DN to SI7326DN	X01
35	32	6/11/2008	EE	No need to populate them	unpop PR1 and PC0	X01
36	35	6/11/2008	EE	Adjust the slew rate of load line	Chagne PR93 and PR66 from 3.83K to 11.8K Chagne PR104 from 1K to 4.99K, PR108 from 3.83K to 6.49K Chagne PC18 from 0.22u to 0.033u, PC21 from 0.022u to 3300P	X01
37	32-36	6/11/2008	EE	Replace 0R/0603 resister by power jumper	Chagne 0R/0603 to power jumper as the SJ1, SJ2, , SJ3, SJ4	X01
38	32-36	6/11/2008	EE	Replace 0R/0606 resister by short	Replace 0R/0606 resister by short as the PR102, PR103, PR59 , PR68	X01
39	34	6/11/2008	EE	Adjust controller Freq on 400K/300K from 200K/300K	PR32 NC and pop PR33	X01
40	20	6/11/2008	EE	Follow ME define Camera routing. Added Camera connect.	Added CON12 camera connect.	X01
41	19	6/11/2008	EE	DVI monitor can not detected by DVI dongle.	Follow Intel reference Board, added MUX to select I2C or AUX signal.	X01
42	3	6/16/2008	EE	Move CPU ITP Debug test pad to bottom side for ICT engineer requirement.	Added T113, T114, T115, T116 and T117 put on Bottom side.	X01
43	6	6/16/2008	EE	Added NB JTAG Debug test pad on bottom side for ICT engineer requirement.	Added T118, T119, T120 and T121 put on Bottom side.	X01
44	8	6/16/2008	EE	Modify +VDD_GFXCORE power enable pin follow intel CRB design.	Added R485, Q55 and R486.	X01
45	21	6/16/2008	EE	Follow Quanta M09 lesson learn. Connect HD_RST# signal to EC for Mute timing control.	Added ICH_AZ_CODEC_RST# connect to SIO(U35.22)	X01
46	21,24	6/22/2008	EE	Follow MRD design added CAP LED circuit.	ITE8512 (U35.88) GPIO for Cap_LED#. Added R453, R450, Q56, Q59 and R446.	X01
47	24	6/22/2008	EE	Change LED_KB circuit. Change to PWM control.	Modify Q39.	X01
48	31	6/22/2008	EE	Solve Bits issue DF225364, CMOS load defalut when disconnect AC.	Added Pull down on RESET_OUT# to avoid ICH_PWRGD glitch in inital state.	X01
49	3	6/22/2008	EE	H_RESET leakage from pull up resisrtor. Follow Intel remove out it.	Depop R300.	X01
50	3	6/24/2008	EE	+3.3V_RUN faster then H_THERM. H_THERMTRIP will cause +3.3V_ALW shut down.	Change R204 to form 1M to 10M. It will delay Q17 turn on timing.	X01
51	21	6/24/2008	EE	SIO_SLP_S3# have glitch from EC when system power up. Add PD resistor to solve it.	Pull down R487 1k ohm at SIO_SLP_S3#.	X01
52	8	6/24/2008	EE	GFX_VR_EN(0.9V) can't meet 2N7002W-7-F(Vgs=1V~2V). Need change to FDV301N(Vgs=0.85V).	Chagne Q55 from 2N7002W-7-F to FDV301N.	X01
53	29	6/25/2008	EE	Follow Crystal test report. Chagne LAN Crystal caps from 22pF to 33pF.	Chagne C272, C305 from 22pF to 33pF.	X01
54	21	6/25/2008	EE	Reserve PLTRST# option at for U35 pin 20 to detect SIO_A20.	Add R488, R489 to option ICH_PME#, PLTRST#.	X01
55	28	6/25/2008	EE	Follow IDT feedback. Change L3, L5 to BLM18BD601SN1D for AP test.	Change L3, L5 to BLM18BD601SN1D.	X01
56	40	6/25/2008	EE	Follow EMI team feedback. Reserve spring for EMI.	Add PV1~PV10.	X01
57	23	6/25/2008	EE	Follow EMI team feedback. Connect USB connecot dip pin to GND.	Connect CN1, CN2 pin 7, 8 to GND.	X01
58	3	6/26/2008	EE	Reserve R490 1M ohm for Q17 compatiable FDV301V.	Add R490 1M ohm and pull up +V1.05S_CPU.	
				X01 change to X02		
1	27	7/22/2008	EE	Change port F to port A for Microsoft default drive support port A only.	Change port F to port A also swap SENSEA, SENSEB circuit.	X02
2	3,5,6,8,11,13 20,21,28,29,31	8/13/2008	EE	Remove 0 ohm.	Remove R173, R430, R354, R239, R282, R405, R178, R243, R244, R277, R47, R488, R132, R203, R152, R153, R311, R16, R19, R30	X02
3	6,9,13,17,18,21 27,29,34,35	8/14/2008	EE	Remove 0 ohm.	R134, R435, R448, R70, R199, R394, PR58, R161, R319, R260, R261, R353, R357, R313, R329, PR56, R61, R322, R323, R335, R337, R383, R106, R43, PR98	X02
4	23	8/15/2008	EE	Change USB choke to DLP11SN900HL2L for Z-high form 1.6mm to 0.6mm.	Change L38, L39, L40 fp and remove R468, R469, R470, R471, R472, R473.	X02
5	26	8/28/2008	EE	System can't shut down during OTP sest to 85 degree C.Follow SDA to modify OTP to 83 degree C.	Change R477 from 562 ohm to 487 ohm.	X02
6	11	8/29/2008	EE	Confirm Safty team to depop D10 and R136 for RTC charge function.	Depop D10 and R136 10k ohm.	X02
7	35	9/3/2008	EE	Changes for cost down (CPU regulator from two to one phase)	Depop PC53, PR67, PR73, FL3, PC100, PC101, PC93, PC97, PC1, PR107, PC92, PQ3, PQ2, PR106, PC94, PL1, PC95, PC3, PR93, PR90, PR101, PR95, PC77, PR88, PC86, PC85, and PR96 Change PR66 from 11.8K to 1.8K, PR104 from 4.99K to 4.02K, PR108 from 6.49K to 1.8K, PC21 from 3300P to 0.01u, PC18 from 0.033 to 0.068, PR81 from 12.7K to 20K, PR87 from 6.81K to 4.99K, PR91 from 1K to 2K Add a resister of PR20(0R)	X02
8	33, 36, 37	9/3/2008	EE	Changes for cost down	Depop PC25, PC105, PC110, PC39 and PC40 Change PQ23 from SI7326DN to SI3424DV, PQ20 from SI7326DN to SI3424DV, PQ22 from SI7114DN to SI7326DN,	X02

QUANTA COMPUTER

PROJECT : SS5	DOC. NO. : 204	REV: X00	
APPROVED BY : Cory Lin	CHECKED BY: Cory Lin	DRAWN BY : Leo Tsung	DATE : May. 19, 2008 · SHEET · OF 11

Title: Change List1 — QUANTA COMPUTER
Size · Document Number: SS5 · Rev: 1A
Date: Thursday, January 08, 2009 · Sheet 43 of 44

Change List

Item	Page#	Date	T	Issue Description	Solution Description	Rev
9	38	9/3/2008	PR	Reserve a protection circuit to avoid votage variation of input (13<Vin<20)	Add some parts of PR492, Pr493, PR491, PD35, PD36, PQ51, PQ61 and PQ62	X02
10	21	9/4/2008	EE	H/W workaround for DOS re-boot commend.	Depop R489 and Pop R488 0 ohm resistor.	X02
11	6, 8, 20, 21	9/4/2008	EE	Remove R250, R467, R157 0 ohm.	Remove R250, R467, R157 0 ohm.	X02
12	22	9/8/2008	EE	Reserve DMIC DATA/CLK to Minipcie board.	Reserve DMIC DATA/CLK to CON15 pin 56, 93	X02
13	33	9/8/2008	EE	Short PJP6 for thermal module have latch in Power jump.	Remove PJP6 and change +1.8V_RUN_P to +1.8V_SUS.	X02
14	18	9/8/2008	EE	Add C515 for memory +1.5V_MD.	Add C515 for memory +1.5V_MD.	X02
15	23	9/8/2008	EE	To fix USB charge on Blackberry and Ipod in S5 issue.	Change U46 to MAX4983E. Add R491, R492, R493, R494, C516, R495, R496, R497. Remove ESD2.	X02
16	20	9/15/2008	EE	Supply DPST function	Depop R270 and Pop R271 resistor.	X02
17	21	9/15/2008	EE	For cost down ,remove debug LED	Depop R83,R112,R198,LED0,LED1,LED2	X02
				X02 change to X02.1		
18	38	9/18/2008	EE	For Safty to add fuse at battery connector.	Add FS3 at CON17	X02.1
19	6, 21	9/26/2008	EE	Add L_BKLT_EN connect NB's L_BKLT_EN and EC pin 48 to slove LCD can't dispaly issue.	Add L_BKLT_EN connect U6 pin C37 to EC pin 48.	X02.1
20	17, 18	10/02/2008	EE	Follow Intel feedback. Each DRAM device needs to have its own ZQ cal resistor.	Add R498~R505 240 ohm to DRAM U23, U24, U25, U26, U36, U37, U38, U39.	X02.1
21	21	10/07/2008	EE	Change BID from X02 to X02.1	Depop R102, R100, R126 and pop R109, R126, R127 100k ohm.	X02.1
22	13	10/07/2008	EE	Re-add ICH_SMLINK0/1 PU resistor and reserve R260, R261.	Reserve and depop R260, R261 0 ohm and Add RP8 PU resistor for ICH_SMLINK0/1.	X02.1
23	38	10/08/2008	EE	Confimr Power team to remvoe fuse. fuse move on battery.	Rmove FS3 and short by shape.	X02.1
24	33	10/16/2008	PR	rise center voltage from 1.79V to 1.82V	change PR36 from 12.4KF to 15.8KF, and PR35 from 10KF to 12.4K, and pop PC39	X02.1
25	35	10/16/2008	PR	PL2 is not in PSL, so channg it to Toko which is in PSL. And adjust some values for PL2's change.	change PR92 from 97.6K to 200K, PR91 from 2K to 499R, PR104 from 4.02K to 2K, PR108 from 1.8K to 2.61K, PC21 from 0.01uF to 0.1uF, PC18 from 0.068uF to 0.022uF, pop PC3	X02.1
				X02.1 change to A00		
1	27	11/10/2008	EE	Change TPA6040A4 GAIN from 15.6dB to 6dB for speaker midified.	Depop R296 and pop R295 100k ohm.	A00
2	21	11/10/2008	EE	Change Board ID to A00.	Depop R217 and pop R100 10k ohm.	A00
3	3, 34	11/10/2008	EE	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	Remove PJP0, PJP2 and short by trace for 1.05V, 1.5V.	A00
4	36	11/10/2008	EE	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	Remove PJP1, PJP3 and short by trace for 3.3V, 5V.	A00
5	34, 36	11/10/2008	EE	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	Remove PJP4, PJP5 and short by trace for +PWR_SRC.	A00
6	33	11/10/2008	EE	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	Remove PJP8 and short by trace. Change PU4.1, PU4.2 to +1.5V_MEM.	A00
7	36	12/22/2008	EE	Rising up OCP point to cover second source controller IC of PU0	Change PR11 from 110k ohm to 147k ohm.	A00
8	33	12/22/2008	EE	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	Remove R451 0 ohm and short by trace. Change 0.75V_P to for +0.75V_DDR_VTT.	A00
9	33	12/29/2008	EE	Remove R451 will effect DDR reference voltage trace.	Restore the R451 0 ohm.	A00
10	33, 34	12/29/2008	P	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	Remove PR118, PR117 0 ohm and short by trace. Change S5_1.8V to SUS_ON, S3_1.8V to RUN_ON.	A00
11	33	12/29/2008	P	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	Remove PR29 0 ohm and short by trace. Remove PR30 *0_NC and NC.	A00
12	34	12/29/2008	P	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	Remove PR34, PR47, PR49, PR55 0 ohm and short by trace. Change EN_2 to RUN_ON.	A00
13	34	12/29/2008	P	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	Remove PR33 0 ohm and short by trace. Remove PR32, PR37 *0_NC and NC.	A00
14	36	12/29/2008	P	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	Remove PR85, PR83, PR12 0 ohm and short by trace. Remove PR10 *0_NC and NC.	A00
15	36	12/29/2008	P	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	Remove PR13, PR17 0 ohm and short by trace. Remove PR16 *0_NC and NC.	A00
16	36	12/29/2008	P	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	Remove PR9 0 ohm and short by trace. Remove PR6, PR7 *0_NC and NC.	A00
17	36	12/29/2008	P	Change PR79, PR80 to short jump SJ5, SJ6.	Change PR79, PR80 to short jump SJ5, SJ6.	A00
18	25	12/29/2008	EE	Change Power/System LED resistor from 220 to 1k ohm to reduce LED brightness.	Change R360 , R382, R366, R442 from 220 to 1k ohm.	A00
19	27	12/29/2008	EE	Follow Dell request. Change TPA6040A4 GAIN from 6dB to 10dB for speaker midified.	Depop R168 and pop R167 100k ohm.	A00
20	9, 14, 27	01/05/2009	EE	Change GMH, ICH, IDT HDA power to 1.5V for slove HDMI no sound issue.	Depop R117 and pop R118 0 ohm. Change U41.3, R101.1 to +1.5V_RUN and R120.1 to +V1.5_MD.	A00
21	21	01/06/2009	EE	HDA bus are +1.5V power rail. The ICH_AZ_CODEC_RST# also need add level shift to connect EC.	Add R506 100k ohm , R507 390k ohm, C135 0.1uF, Q60 3904, Q61 2N7002.	A00
22	20	02/05/2009	EE	Add DPST funtion in ST build.	Depop R271 10k ohm and pop R269 0 ohm.	A00
23	21	02/05/2009	EE	Remove C135 to reduce Q60 pin 2 rise time. It will effect ICH_AZ_CODEC_RST2# asserted.	Depop C135 0.1uF.	A00
24	27	02/05/2009	EE	Follow Speaker Vendor NXP to moidfy AMP caps.	Change C33, C34 from 0.033U to 0.0047U and C140, C149 from 0.033U to 0.0047U.	A00
25	19	02/05/2009	EE	Diode causing voltage drop. The VGA controller on the dongle goes into reset and stops functioning	Change D14 Diode to Fuse 0805L100WR and there is no voltage drop on VGA controller.	A00
26	20	02/23/2009	EE	LCD self test function lose (D + Power Button) when enable DPST function.	Pop R270 0 ohm and change R260 to 100 ohm.	

QUANTA COMPUTER

PROJECT : SS5 DOC. NO. : 204 REV: A00

APPROVED BY : Cory Lin CHECKED BY: Cory Lin DRAWN BY : Leo Tsung DATE: May. 19, 2008 SHEET: OF: 11

Title	Change List1	QUANTA
Size	Document Number SS5	COMPUTER
Rev	1A	
Date:	Monday, February 23, 2009	Sheet 44 of 44