

# UM3/UM6 SYSTEM BLOCK DIAGRAM

## POWER

**AC/BATT CONNECTOR**  
PG 53

**SYSTEM RESET CIRCUIT** PG 42

**BATT CHARGER** PG 45

**RUN POWER SW**  
+3.3V\_SUS/+5V\_SUS  
+5V/+3.3V/+1.8V PG 52

**CPU VR** PG 51

**DC/DC**  
+3.3V\_ALW/+5V\_ALW/  
+15V\_ALW PG 46

**REGULATOR**  
+1.5V\_SUS/+0.75V\_DDR\_VTT PG 47

+1.05V\_PCH PG 48

+1.05V\_VTT PG 49

**THERMAL**  
SMSC1422 PG 38

**CLOCK**  
SLG8SP585VTR  
(QFN-32) PG 15

**DDR3-SODIMM1**  
RVS Type PG 13

Dual Channel DDR3  
800/1066 1.5V

**DDR3-SODIMM2**  
RVS Type PG 14

**Arrandale**  
  
( rPGA 989 )  
PG 3,4,5,6

**ATI M92-LP S2**  
**PCI EXPRESS GFX**  
631 uFCBGA 23mm\*23mm  
PG 16,17,18,19,20,21,22

**DDR3 x 4**  
(512M 64bits)  
PG 22

**Panel Connector**  
PG 24

**HDMI CONN.** PG 24

**CRT CONN.** PG 25

**PCH**  
(HM55)  
PG 7,8,9,10,11,12

**SATA-ODD** PG 35

**SATA-HDD** PG 35

**USB conn x 1** PG 33

**Bluetooth BTB Conn**  
BT365 PG 32

**Camera** PG 24  
To LCD Conn

**AUDIO/AMP**  
ALC269Q-GR PG 39

**A- MIC conn**  
PG 39

**Audio SPK conn**  
PG 39

**Audio Jacks x2**  
PG 26

**USER INTERFACE**  
PG 37

**KBC**  
ITE8502 PG 29

**FLASH 1Mbytes**  
PG 30

**Touchpad**  
PG 36

**FLASH 4Mbytes**  
PG 30

**Keyboard**  
PG 36

**LOM**  
RTL8103E PG 41

**MINI-CARD**  
WLAN PG 32

**MINI-CARD**  
WWAN PG 31

**USB conn x 2**

**CARD READER**  
RTS5159

**IO Board** PG 26

**VER :C3B**  
**PWA:**  
**PWB:**




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25	CRT CONN
26	DB CONN / R5U230
27	BLANK PAGE
28	BLANK PAGE
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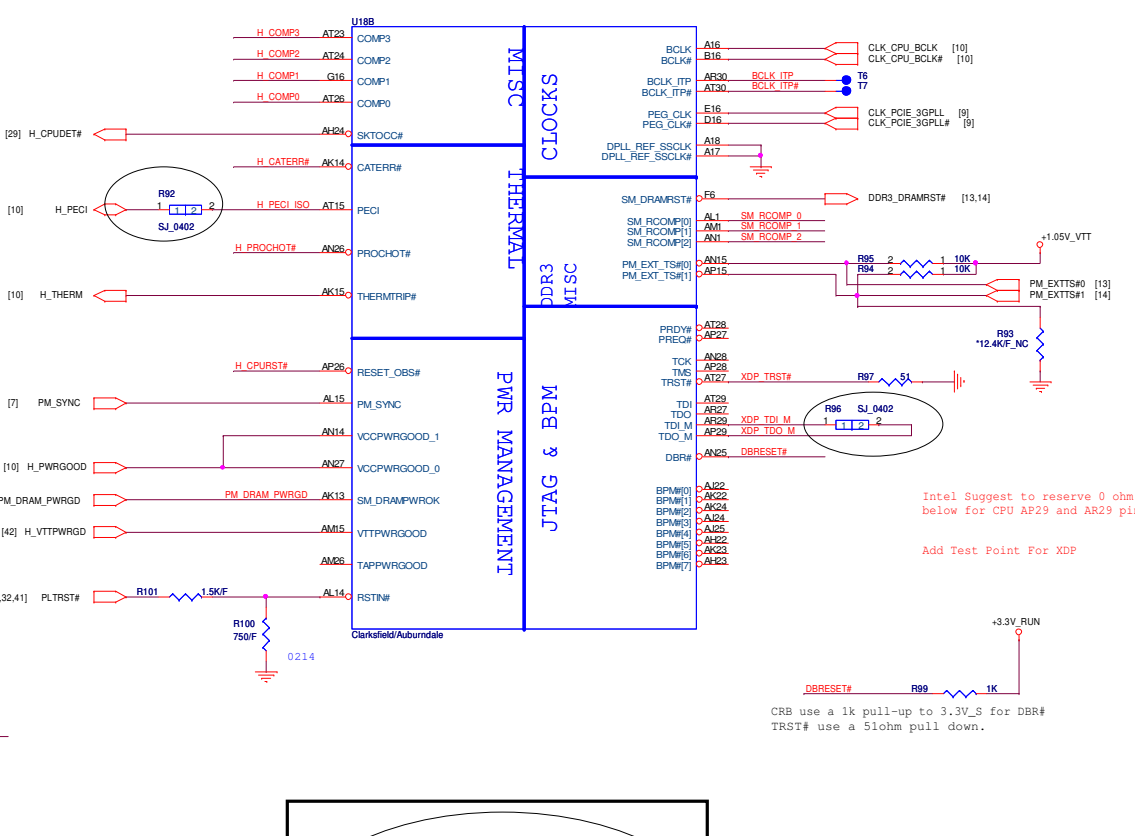
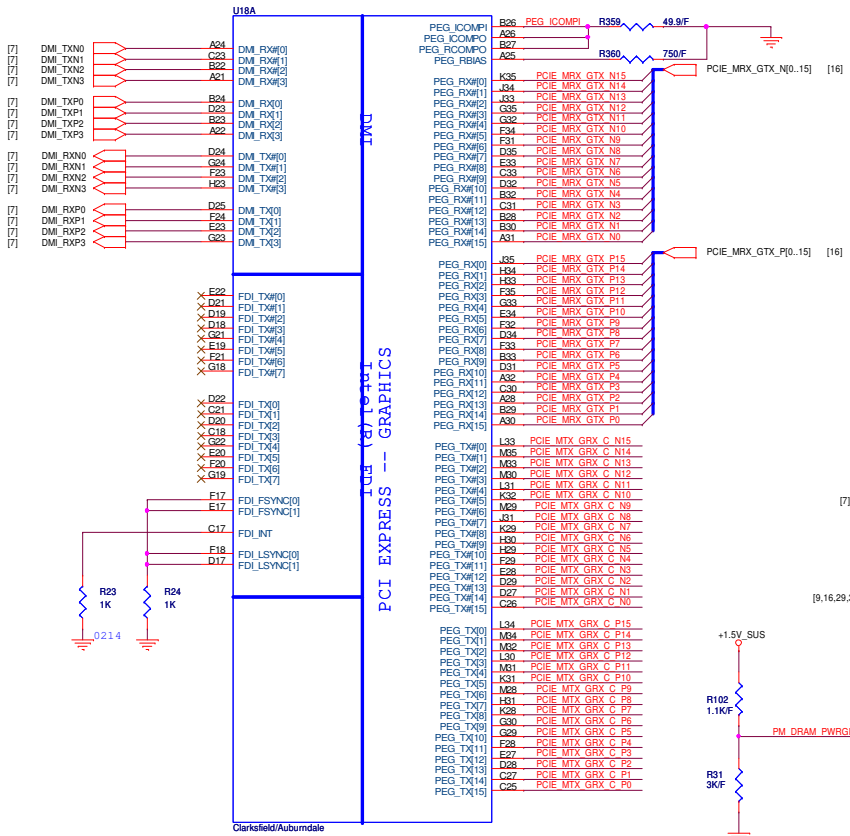
**Power States**

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW	+5V	37,44,46,47,49,50,53	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,37,44,45,46,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,26,33,37,46,48,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,24,36,37,41,42,44,47,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,37,38,39,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,19,24,25,26,29,30,31,32,35,38,39,41,42,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	GFX_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_+1.1_EN	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44	VGA POWER	GFX_+1.8_EN	
+1.05V_PCH	+1.05V	07,08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+1.05V_VTT	+1.1V	03,05,10,11,49	CPU POWER	RUN_ON	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

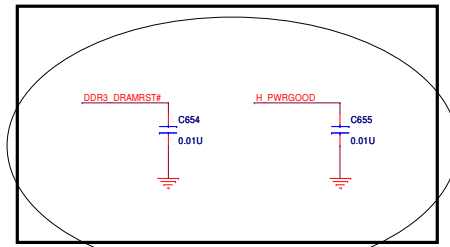
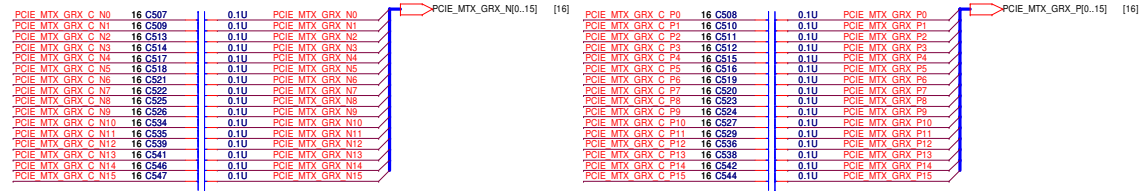
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI, PEG, FDI)

AUBURNDALE/CLARKSFIELD PROCESSOR (CLK, MISC, JTAG)

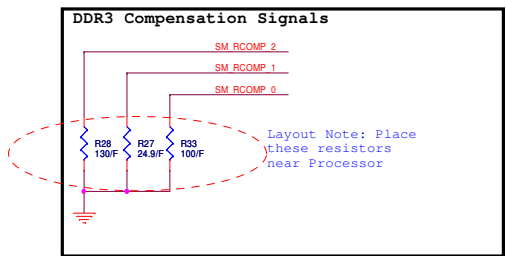
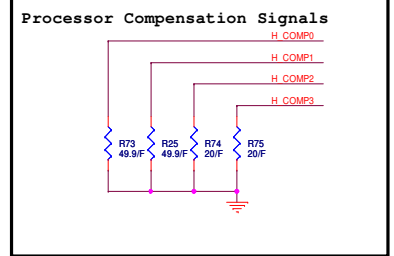
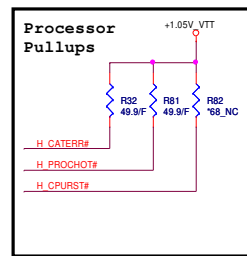


Intel suggest to reserve 0 ohm below for CPU AP29 and AR29 pins.  
Add Test Point For XDP

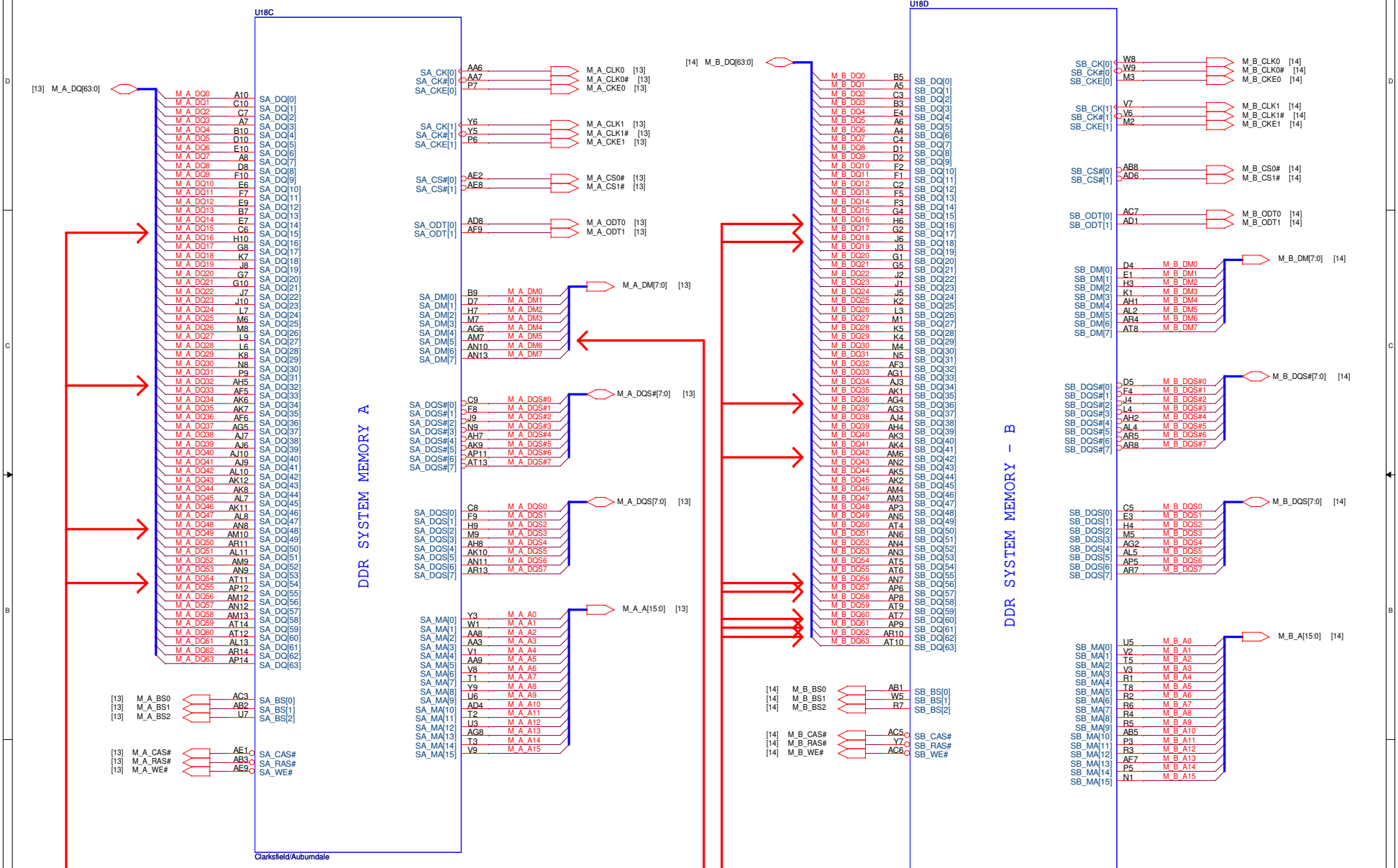
DBRESET# R99 1K  
TRST# use a 51ohm pull down.



Remove XDP Function



# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

**QUANTA COMPUTER**

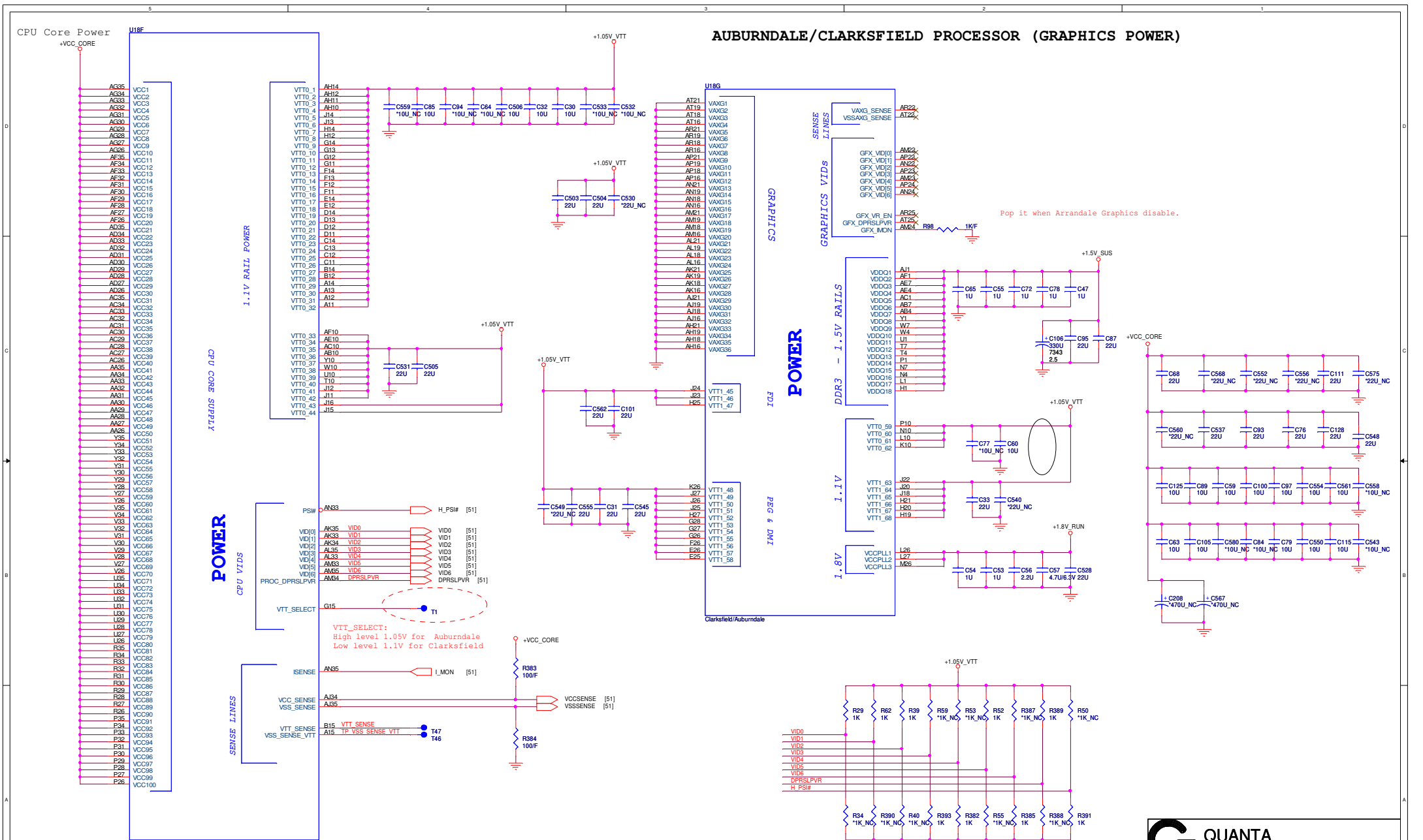
Title: AUBURNDALE 2/4

Size	Document Number	Rev
	UM3	1A

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CPU Core Power

# AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



## AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

**QUANTA COMPUTER**

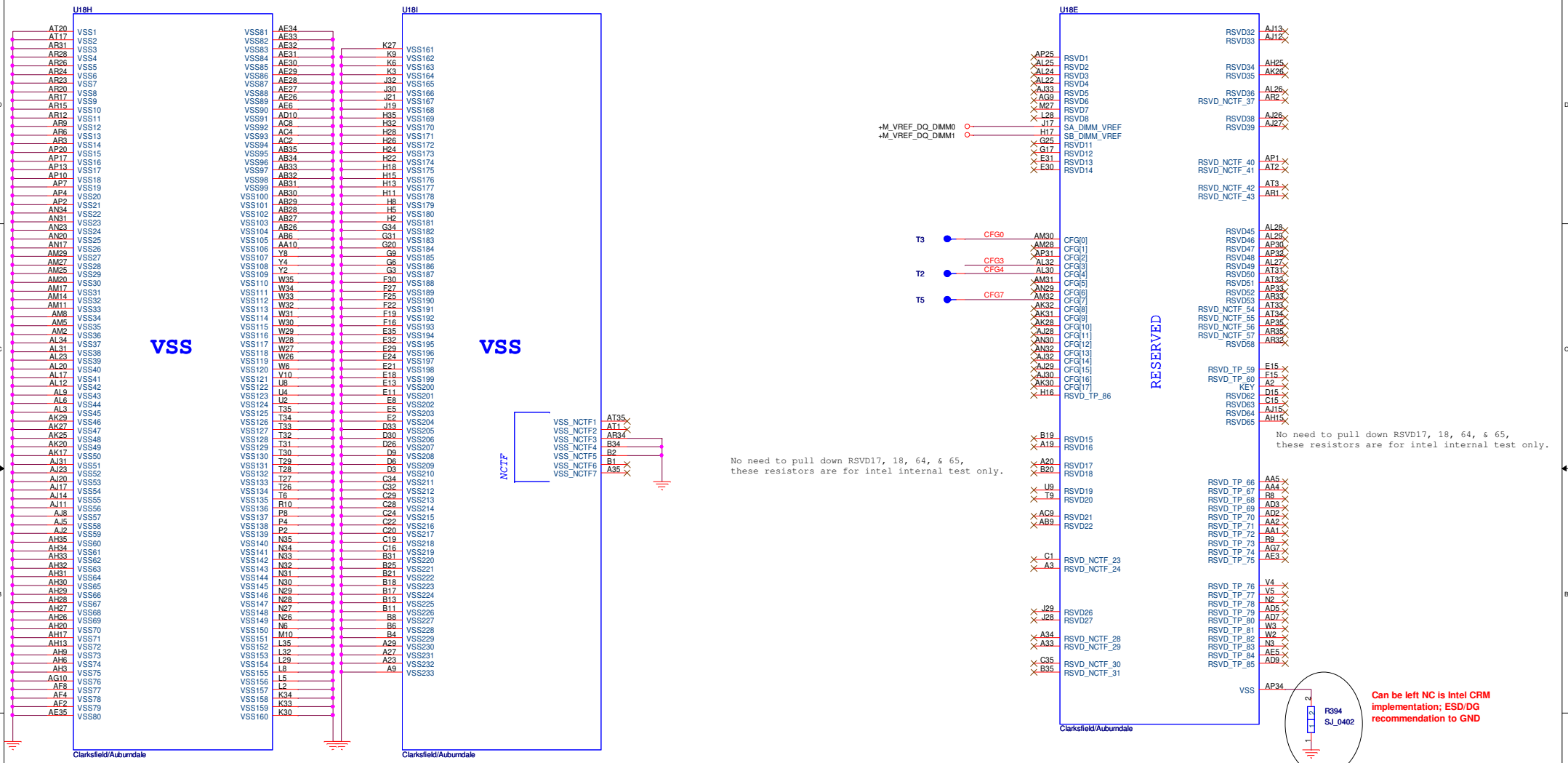
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Size: Document Number UMS Rev 1A

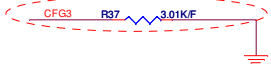
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# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

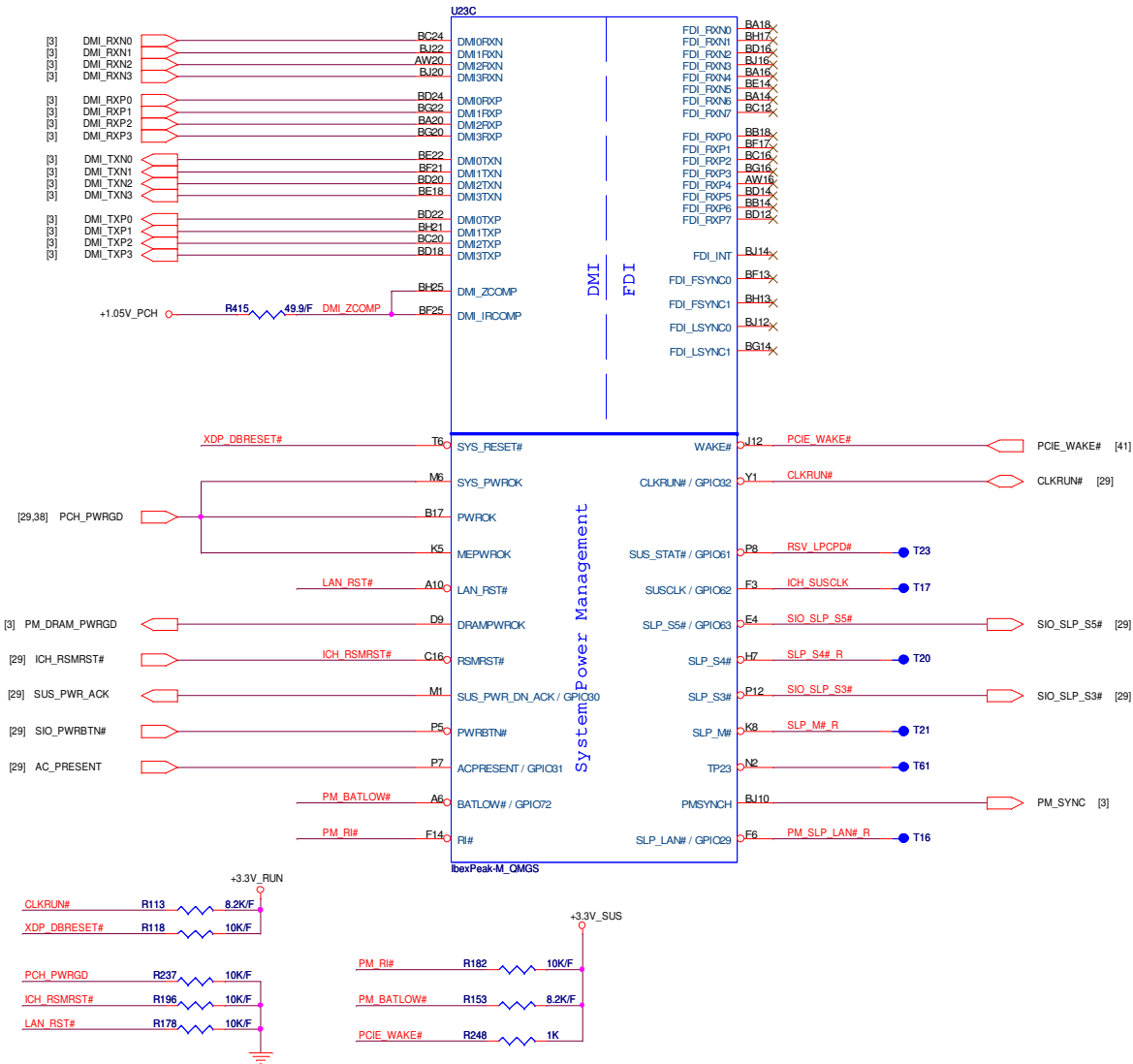
**QUANTA COMPUTER**

1100 AUBURNDALE 4/4

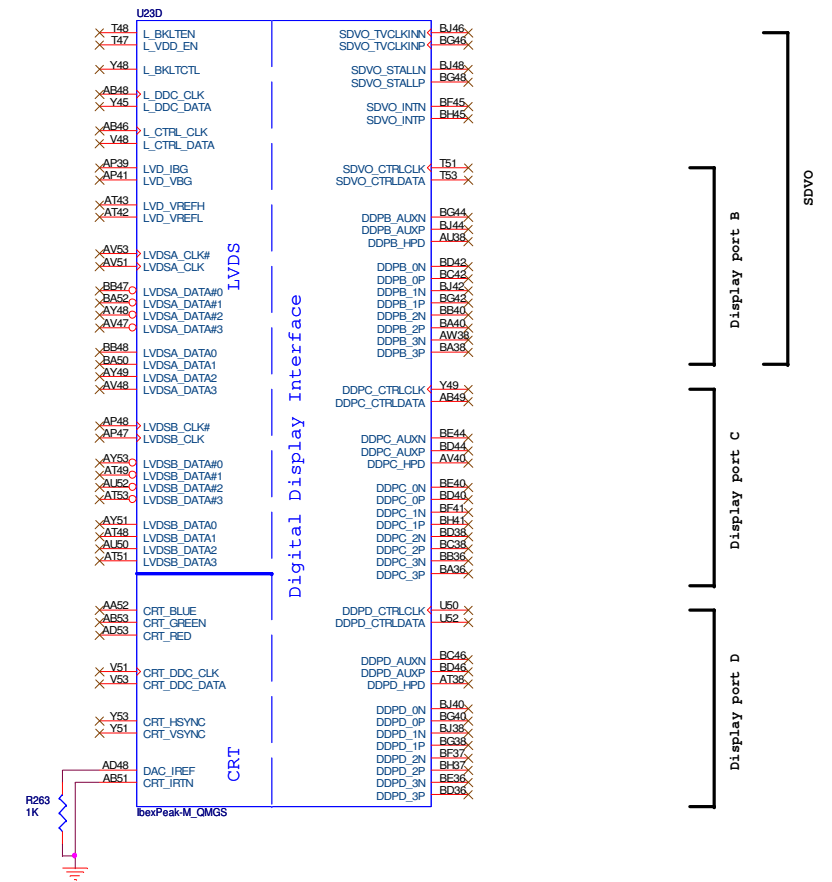
Size Document Number LMS Rev 1A

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# IBEX PEAK-M (DMI, FDI, GPIO)



# IBEX PEAK-M (LVDS, DDI)



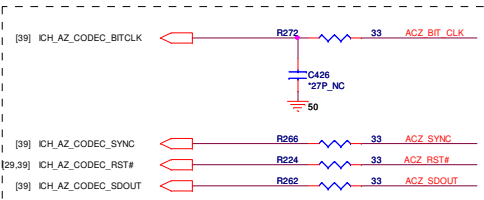
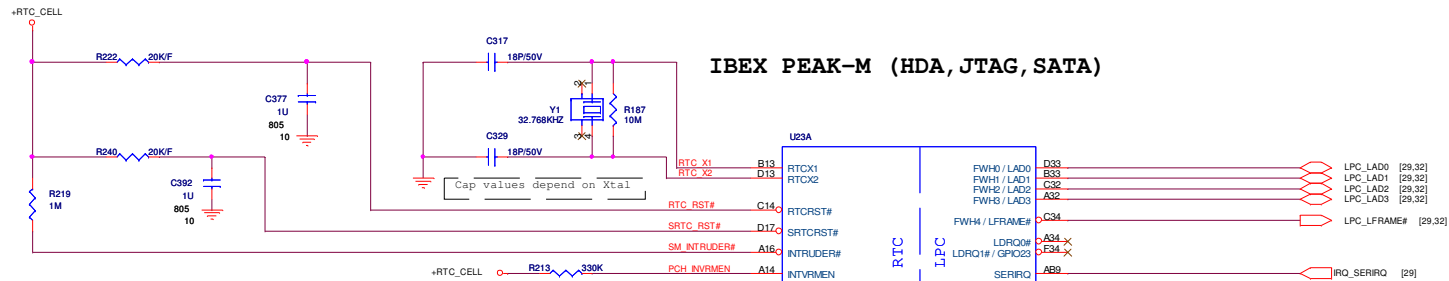
**QUANTA COMPUTER**

Title: IBEX PEAK-M 1/6

Size	Document Number	Rev
	UM3	1A

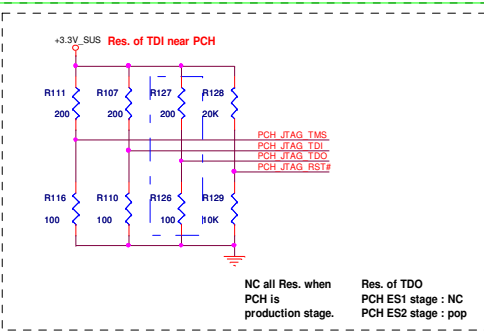
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# IBEX PEAK-M (HDA, JTAG, SATA)

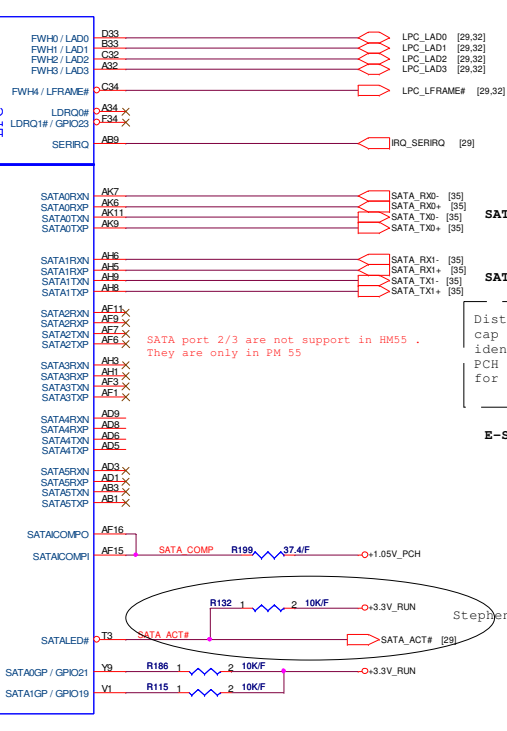
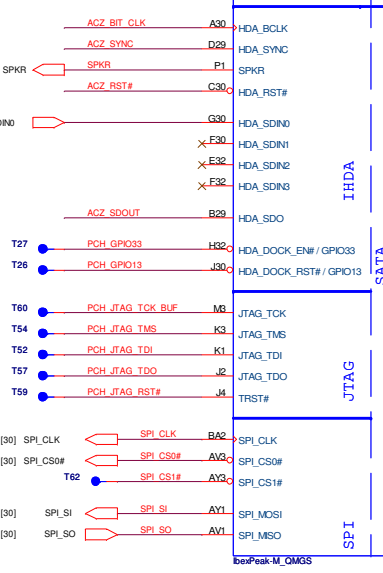


**INTVRMEN (Internal Voltage Regulator Enable) :**  
This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.

Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

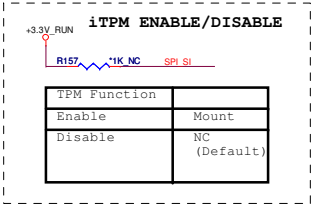


[39] ICH\_AZ\_CODECSDIN0



Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for the same pair.

**JTAG**  
Test Pads are need to put on the same side of mother board.



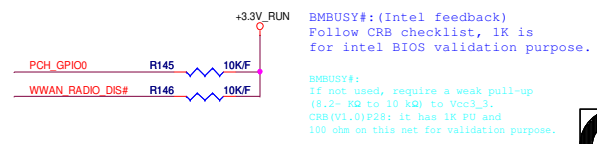
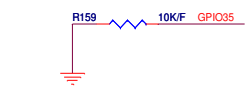
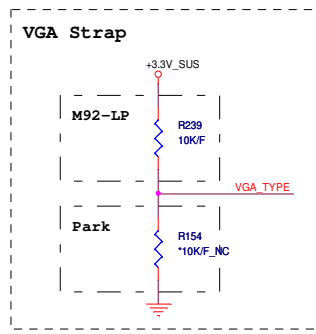
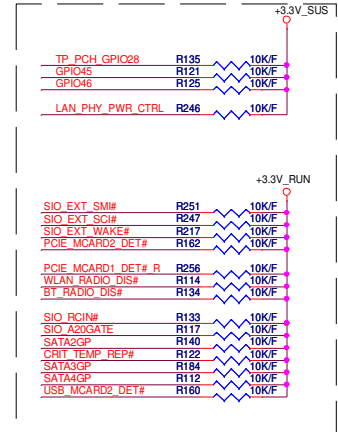
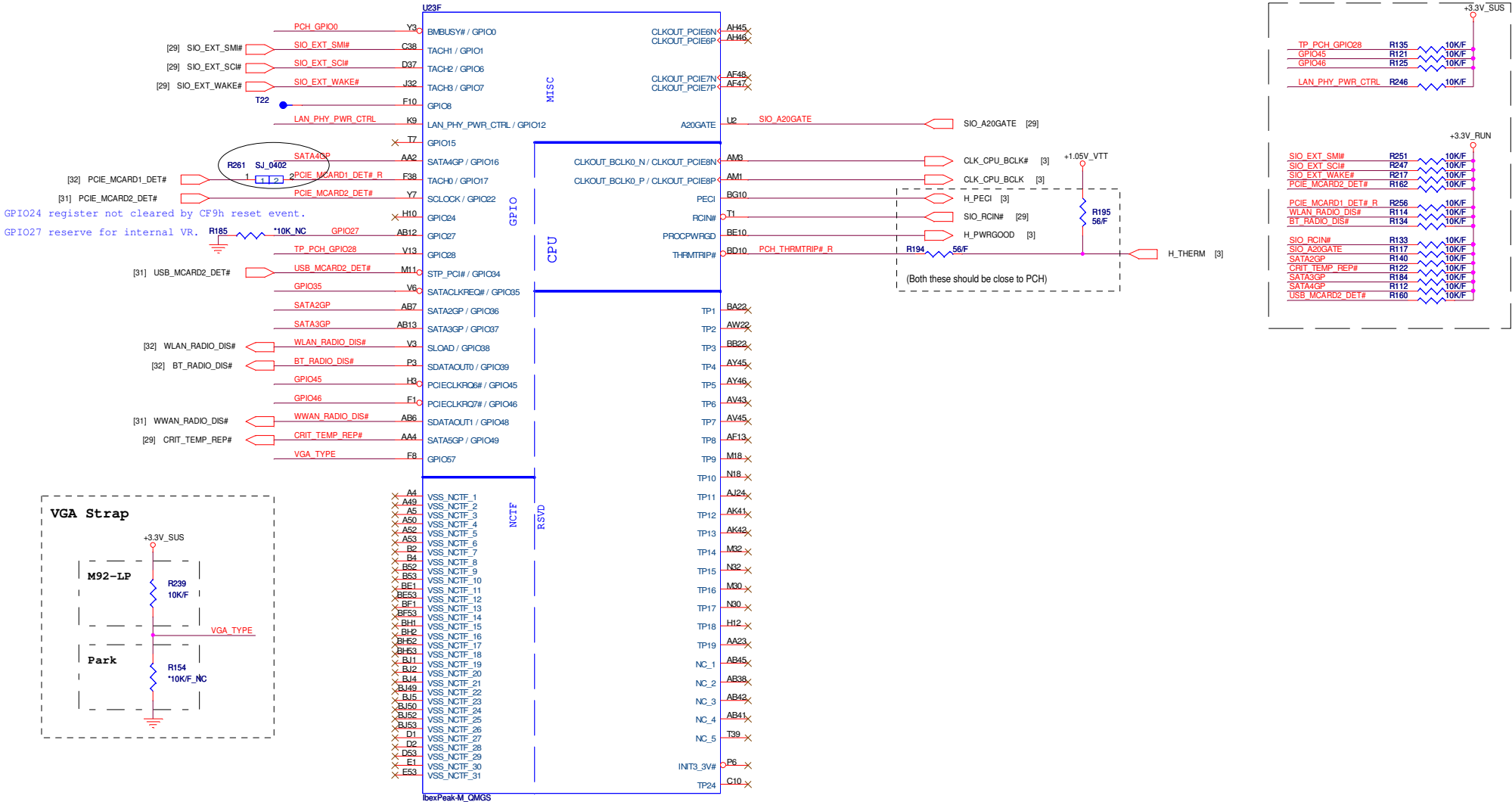
**QUANTA COMPUTER**

File: IBEX PEAK-M 2/6  
 Size: UMS Document Number  
 Date: Thursday, October 15, 2009 Sheet 8 of 63 Rev 1A





# IBEX PEAK-M (GPIO, VSS\_NCTF, RSVD)



WWAN\_RADIO\_DIS# 1-X High = Strong (Default)

BMBUSY#:(Intel feedback)  
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:  
If not used, require a weak pull-up (8.2- 1K to 10 kΩ) to Vcc3.3.  
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

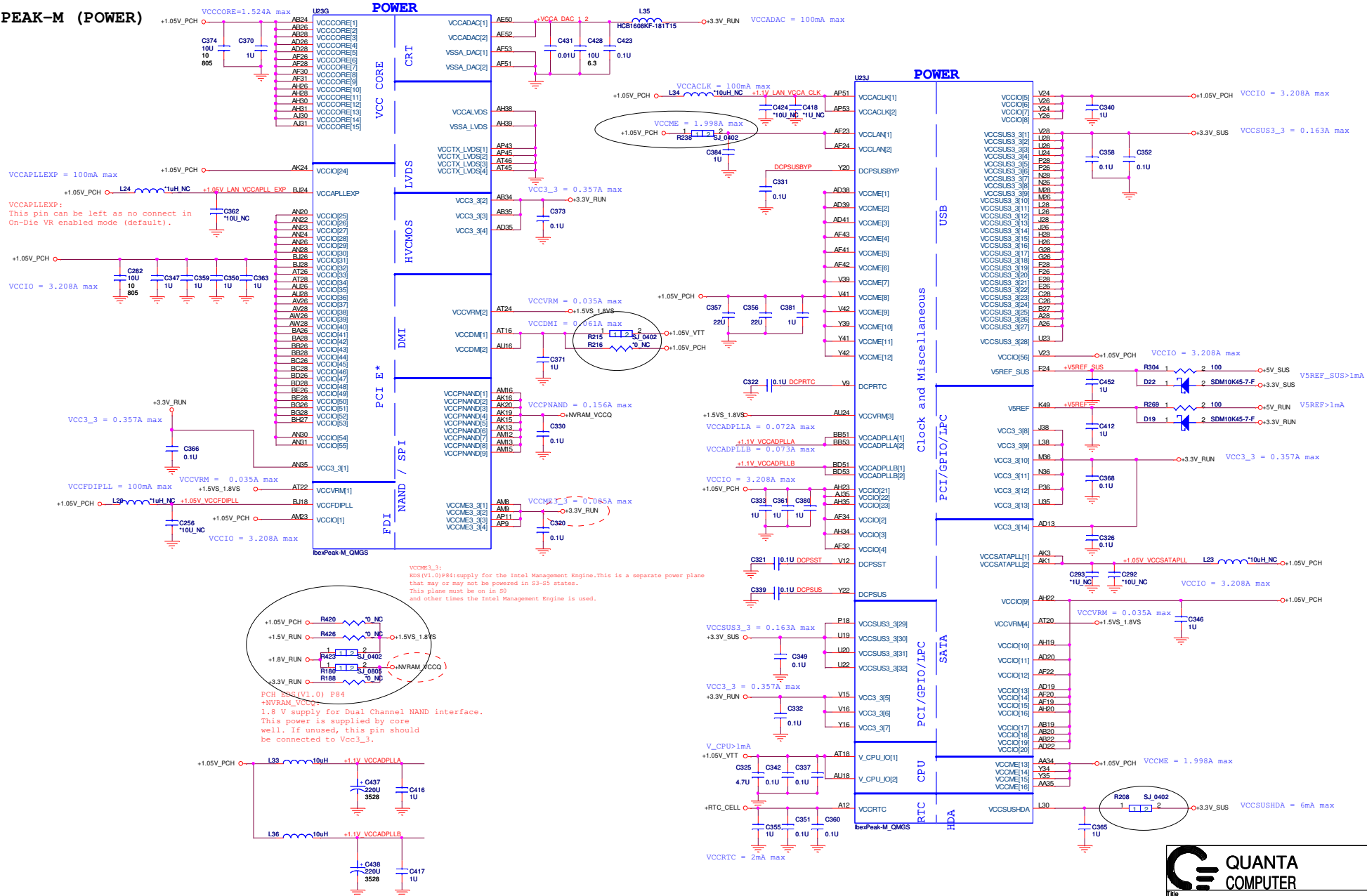
QUANTA COMPUTER

Title: IBEX PEAK-M 46

Size	Document Number	Rev
	UMS	1A

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# IBEX PEAK-M (POWER)



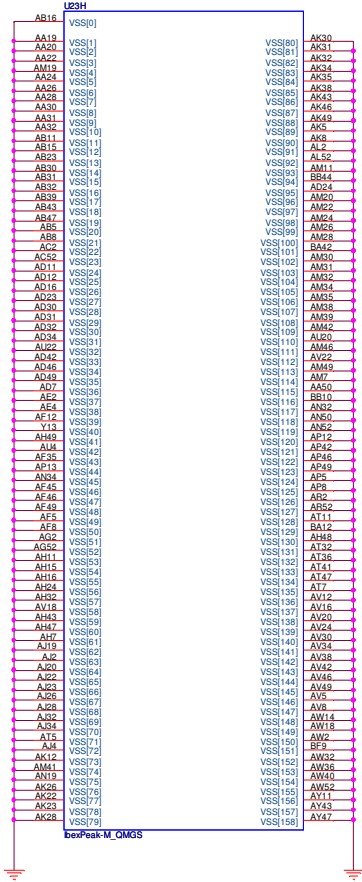
**VCCME\_1:**  
EDS(V1.0)P84:supply for the Intel Management Engine.This is a separate power plane that may or may not be powered in S3-S5 states. This plane must be on in S0 and other times the Intel Management Engine is used.

**VCC3\_3:**  
PCH PMS(V1.0) P84 +NVRAM\_VCC3. 1.8 V supply for Dual Channel NAND interface. This power is supplied by core well. If unused, this pin should be connected to Vcc3\_3.

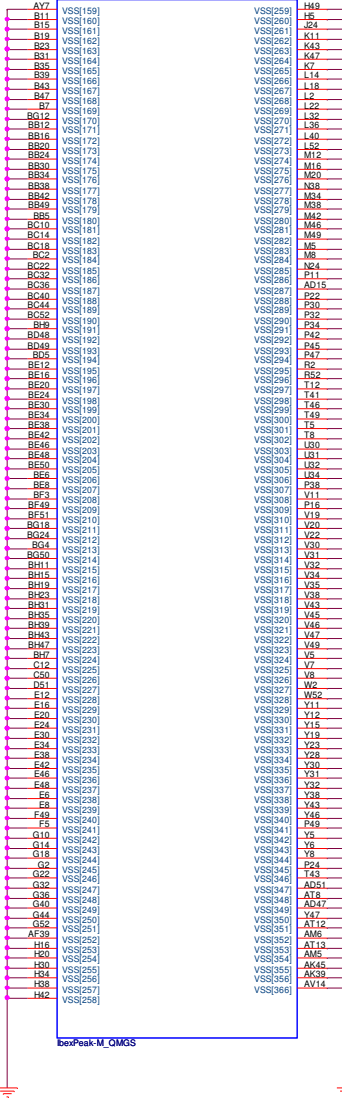


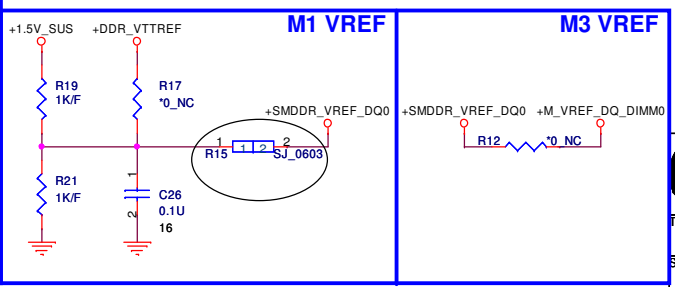
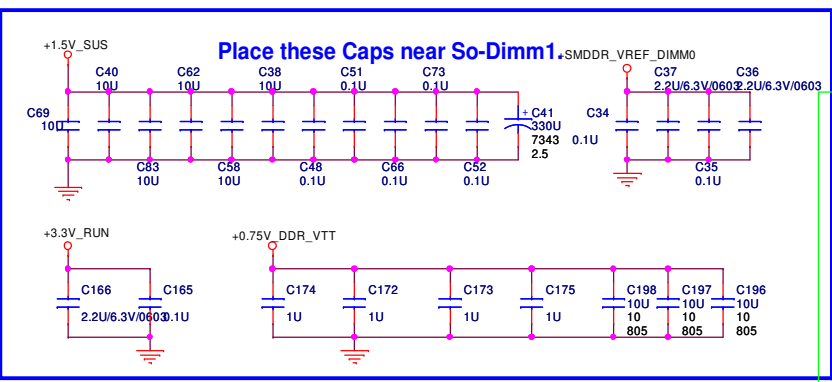
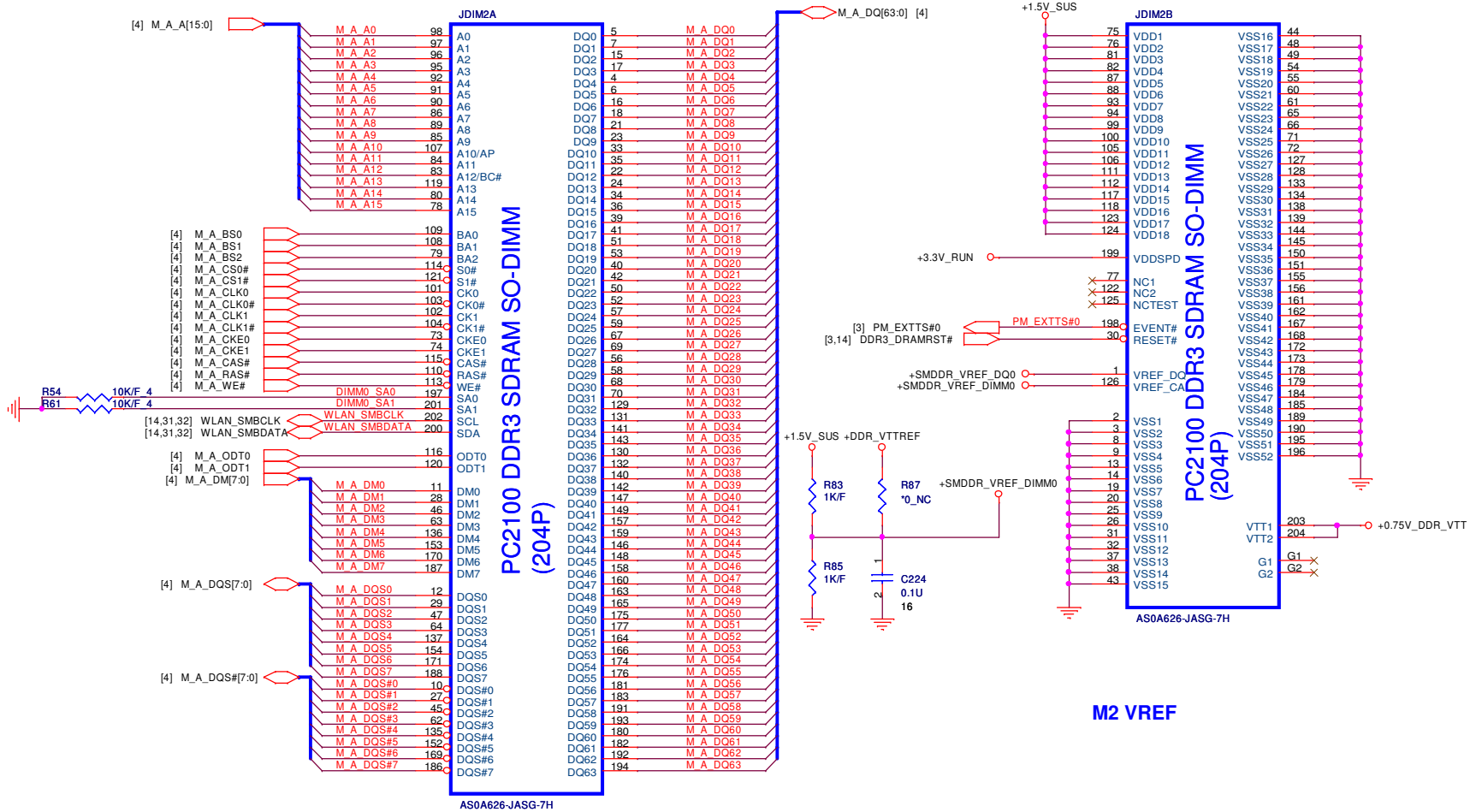
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Size	Document Number	Rev	
UM3		1A	
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**IBEX PEAK-M (GND)**

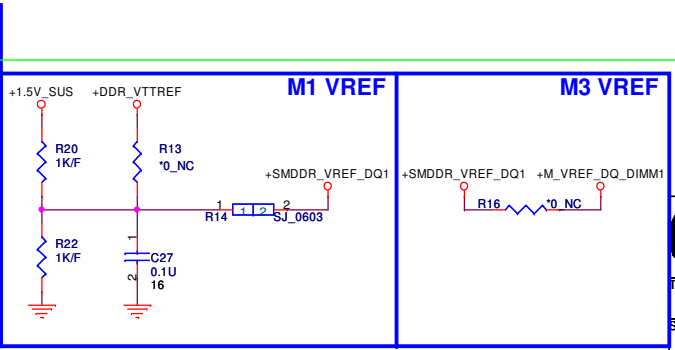
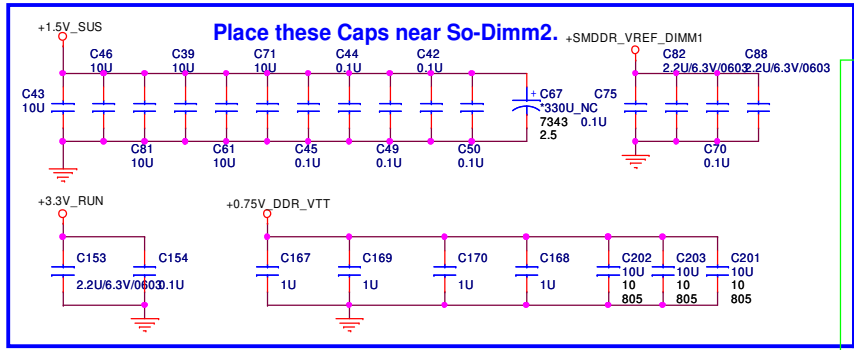
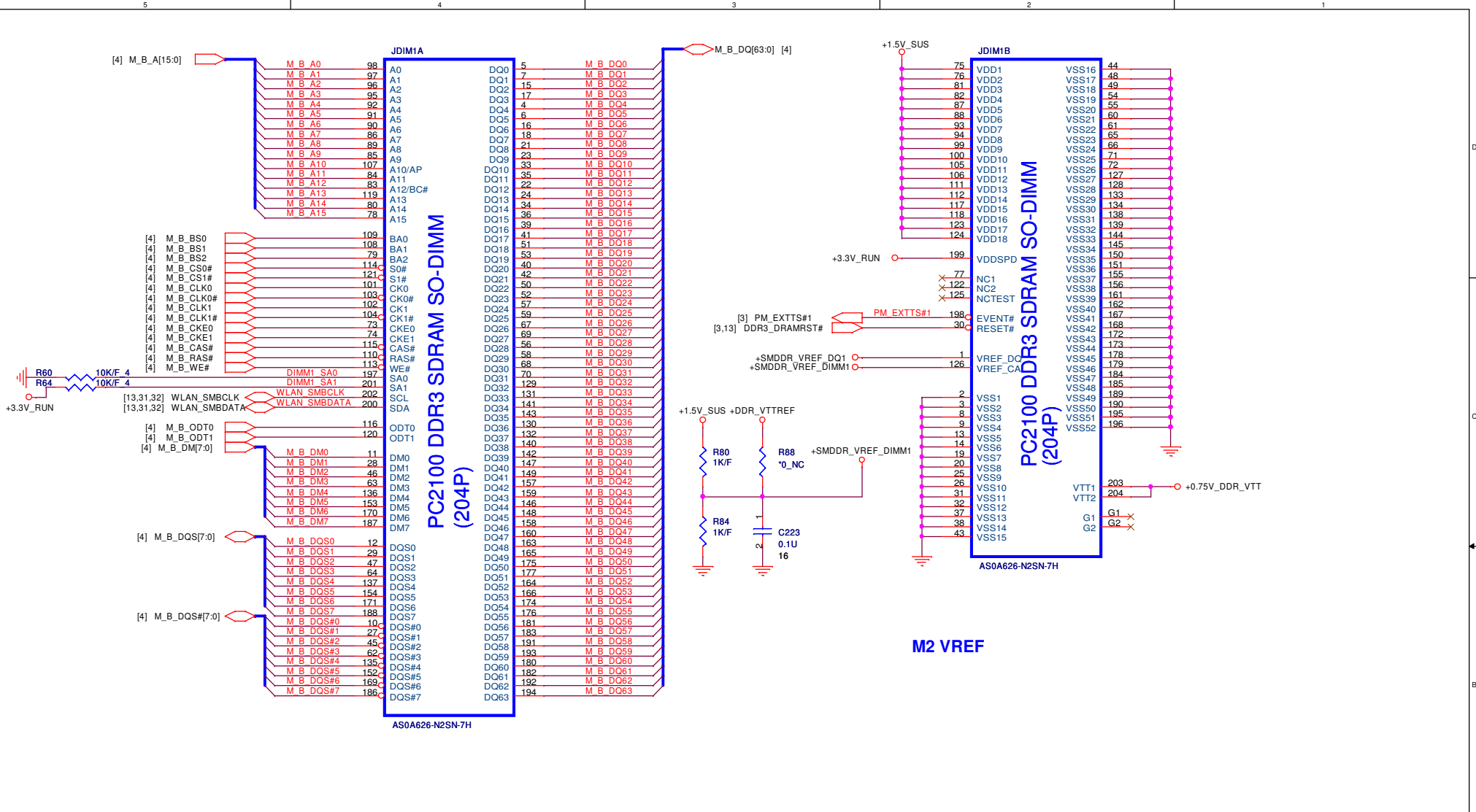


**U23I**

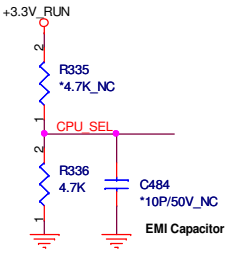
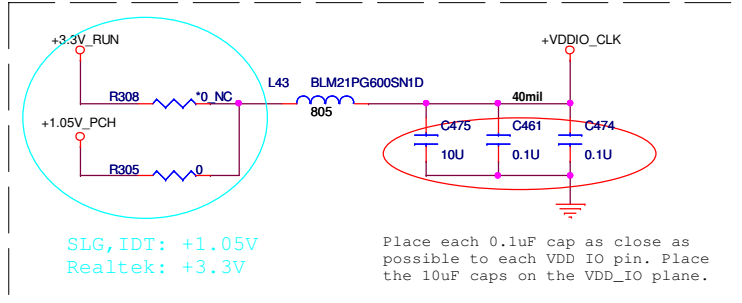
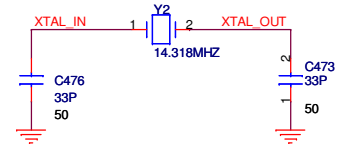
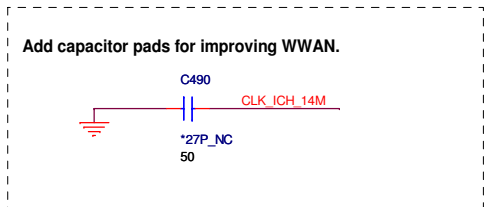
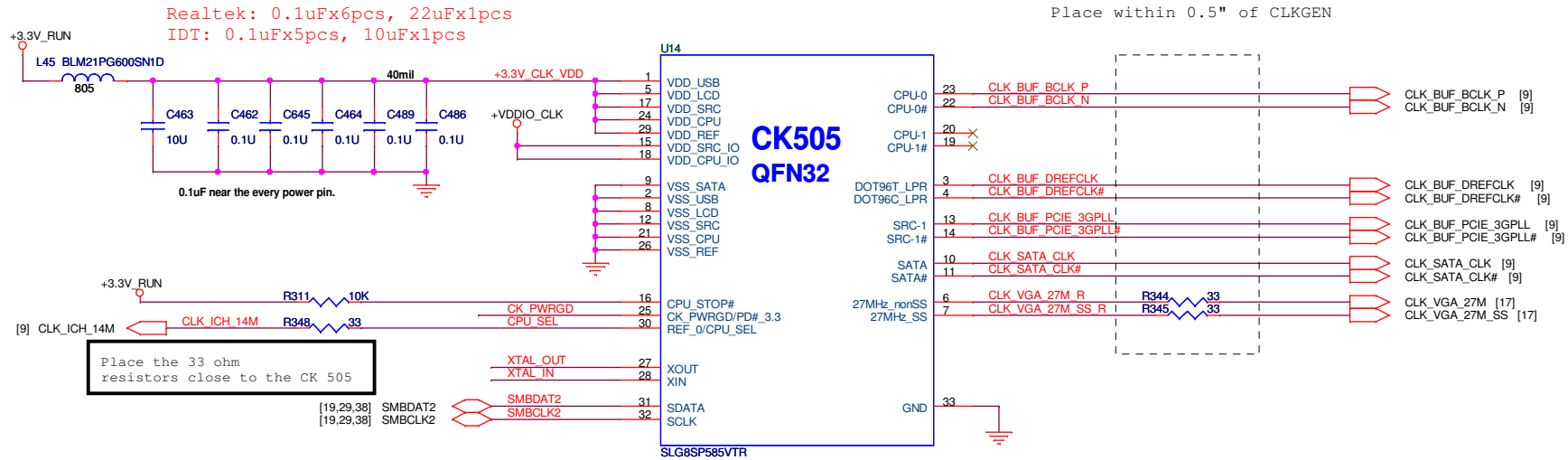




Title: DDR3 DIMM-0		
Size: UMS	Document Number: UMS	Rev: 1A
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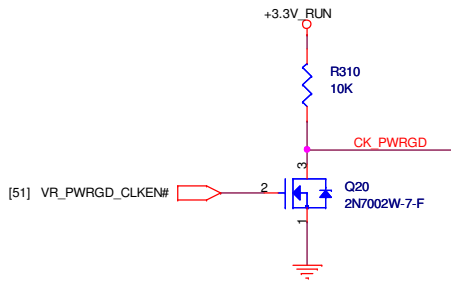


File: DDR3 DIMM-1  
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 Rev: 1A



PIN 30	CPU_0	CPU_1
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU\_SEL:  
 SLG date sheet (V0.2) P15:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 Realtek date sheet(V1.2) P11:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.  
 IDT date sheet(V0.7) P10:  
 High Voltage: Min 0.7V, Max 1.5V.  
 Low Voltage: Min Vss-0.3V, Max 0.35V.



+VDDIO\_CLK:  
 SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.  
 Realtek date sheet(V1.2) P11: Min 1.05V, Max 3.3V.  
 IDT date sheet(V0.7) P10: Min 0.9975V, Max 3.465V.

**QUANTA COMPUTER**

Title: Clock Generator

Size: Document Number UM3 Rev 1A

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[3] PCIe\_MTX\_GRX\_P[0..15]  
 [3] PCIe\_MTX\_GRX\_N[0..15]

[3] PCIe\_MRX\_GTX\_P[0..15]  
 [3] PCIe\_MRX\_GTX\_N[0..15]

U19A  
 PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_MTX_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_MRX_GTX_C_P0
PCIE_MTX_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_MRX_GTX_C_N0
PCIE_MTX_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AC29	PCIE_MRX_GTX_C_P1
PCIE_MTX_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_MRX_GTX_C_N1
PCIE_MTX_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_MRX_GTX_C_P2
PCIE_MTX_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_MRX_GTX_C_N2
PCIE_MTX_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_MRX_GTX_C_P3
PCIE_MTX_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_MRX_GTX_C_N3
PCIE_MTX_GRX_P4	AB30	PCIE_RX4P	PCIE_TX4P	AC25	PCIE_MRX_GTX_C_P4
PCIE_MTX_GRX_N4	AA31	PCIE_RX4N	PCIE_TX4N	AB25	PCIE_MRX_GTX_C_N4
PCIE_MTX_GRX_P5	AA29	PCIE_RX5P	PCIE_TX5P	Y23	PCIE_MRX_GTX_C_P5
PCIE_MTX_GRX_N5	Y28	PCIE_RX5N	PCIE_TX5N	Y24	PCIE_MRX_GTX_C_N5
PCIE_MTX_GRX_P6	Y30	PCIE_RX6P	PCIE_TX6P	AD27	PCIE_MRX_GTX_C_P6
PCIE_MTX_GRX_N6	W31	PCIE_RX6N	PCIE_TX6N	AB26	PCIE_MRX_GTX_C_N6
PCIE_MTX_GRX_P7	W29	PCIE_RX7P	PCIE_TX7P	Y27	PCIE_MRX_GTX_C_P7
PCIE_MTX_GRX_N7	V28	PCIE_RX7N	PCIE_TX7N	Y26	PCIE_MRX_GTX_C_N7
PCIE_MTX_GRX_P8	V30	PCIE_RX8P	PCIE_TX8P	W24	PCIE_MRX_GTX_C_P8
PCIE_MTX_GRX_N8	U31	PCIE_RX8N	PCIE_TX8N	W23	PCIE_MRX_GTX_C_N8
PCIE_MTX_GRX_P9	U29	PCIE_RX9P	PCIE_TX9P	V27	PCIE_MRX_GTX_C_P9
PCIE_MTX_GRX_N9	T28	PCIE_RX9N	PCIE_TX9N	U26	PCIE_MRX_GTX_C_N9
PCIE_MTX_GRX_P10	T30	PCIE_RX10P	PCIE_TX10P	U24	PCIE_MRX_GTX_C_P10
PCIE_MTX_GRX_N10	R31	PCIE_RX10N	PCIE_TX10N	U23	PCIE_MRX_GTX_C_N10
PCIE_MTX_GRX_P11	R29	PCIE_RX11P	PCIE_TX11P	T26	PCIE_MRX_GTX_C_P11
PCIE_MTX_GRX_N11	P28	PCIE_RX11N	PCIE_TX11N	T27	PCIE_MRX_GTX_C_N11
PCIE_MTX_GRX_P12	P30	PCIE_RX12P	PCIE_TX12P	T24	PCIE_MRX_GTX_C_P12
PCIE_MTX_GRX_N12	N31	PCIE_RX12N	PCIE_TX12N	T23	PCIE_MRX_GTX_C_N12
PCIE_MTX_GRX_P13	N29	PCIE_RX13P	PCIE_TX13P	P27	PCIE_MRX_GTX_C_P13
PCIE_MTX_GRX_N13	M28	PCIE_RX13N	PCIE_TX13N	P26	PCIE_MRX_GTX_C_N13
PCIE_MTX_GRX_P14	M30	PCIE_RX14P	PCIE_TX14P	P24	PCIE_MRX_GTX_C_P14
PCIE_MTX_GRX_N14	L31	PCIE_RX14N	PCIE_TX14N	P23	PCIE_MRX_GTX_C_N14
PCIE_MTX_GRX_P15	L29	PCIE_RX15P	PCIE_TX15P	M27	PCIE_MRX_GTX_C_P15
PCIE_MTX_GRX_N15	K30	PCIE_RX15N	PCIE_TX15N	M26	PCIE_MRX_GTX_C_N15

PCIE_MRX_GTX_P0	0.1U	2	1	C142	16	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	0.1U	2	1	C133	16	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	0.1U	2	1	C180	16	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	0.1U	2	1	C148	16	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	0.1U	2	1	C195	16	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	0.1U	2	1	C181	16	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	0.1U	2	1	C217	16	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	0.1U	2	1	C204	16	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	0.1U	2	1	C236	16	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	0.1U	2	1	C225	16	PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10	0.1U	2	1	C245	16	PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11	0.1U	2	1	C240	16	PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12	0.1U	2	1	C268	16	PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13	0.1U	2	1	C271	16	PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14	0.1U	2	1	C284	16	PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15	0.1U	2	1	C278	16	PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0	0.1U	2	1	C143	16	PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1	0.1U	2	1	C134	16	PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2	0.1U	2	1	C184	16	PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3	0.1U	2	1	C149	16	PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4	0.1U	2	1	C205	16	PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5	0.1U	2	1	C186	16	PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6	0.1U	2	1	C222	16	PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7	0.1U	2	1	C215	16	PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8	0.1U	2	1	C227	16	PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9	0.1U	2	1	C228	16	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	0.1U	2	1	C254	16	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	0.1U	2	1	C250	16	PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12	0.1U	2	1	C276	16	PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13	0.1U	2	1	C259	16	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	0.1U	2	1	C285	16	PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15	0.1U	2	1	C280	16	PCIE_MRX_GTX_C_N15


100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.  
 clock must be provided less than 400ns  
 after CLKREQ# is asserted

[9] CLK\_PCIE\_VGA  
 [9] CLK\_PCIE\_VGA#

[3,9,29,31,32,41] PLTRST#

(1.1V)  
 +PCIE\_VDDC

M92-S2 XT AJ072800T04 100-CG1675 (216-0728004)  
 M92-S2 AJ072800T03 100-CG1643 (216-0728003)



**QUANTA  
COMPUTER**

Title: VGA-M92-XT PCIe

Size	Document Number	Rev
	UM3	1A

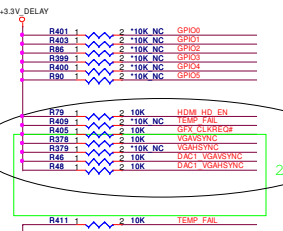
Date: Thursday, October 15, 2009 Sheet 16 of 63



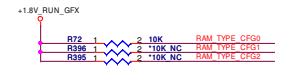
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0	0
256MB	0	0	1	1
64MB	0	1	1	0
512MB	1	0	0	0



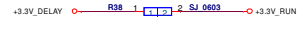
GPIO Straps Table	DESCRIPTION OF DEFAULT SETTINGS	FW setting
GPIO0	GPIO0: TX_PWRD_EN (Transceiver Power Savings Enable) 0: 50% Tx output swing for enable mode 1: Full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1: TX_DEEMPH_EN (Transceiver De-emphasis Enable) 0: Tx de-emphasis disabled for enable mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2: BIF_GBK2_EN (5.0 GT/s Enable) 0: Step-Attenuation-Controlled Gen2 1: Step-Attenuation-Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO5: AC_BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 3.3 V	0
GPIO6	ATI reserved only	0
HSYNC (A426)	00: No Audio function 01: Audio for Displayport only 10: Audio for Displayport only and HDMI if dongle is detected 11: Audio for both Displayport and HDMI. HDMI must only be enabled on systems that are legally certified, it is the responsibility of the system designer to ensure that the system is certified to support this feature.	11
VSYNC (A27)		



DACTL_VGA_VSYNC	HD Audio straps
0/0	No audio function
0/1	Audio for Displayport only
1/0	Audio for Displayport and HDMI if dongle is detected
1/1	Audio for both Displayport and HDMI

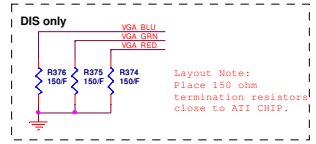
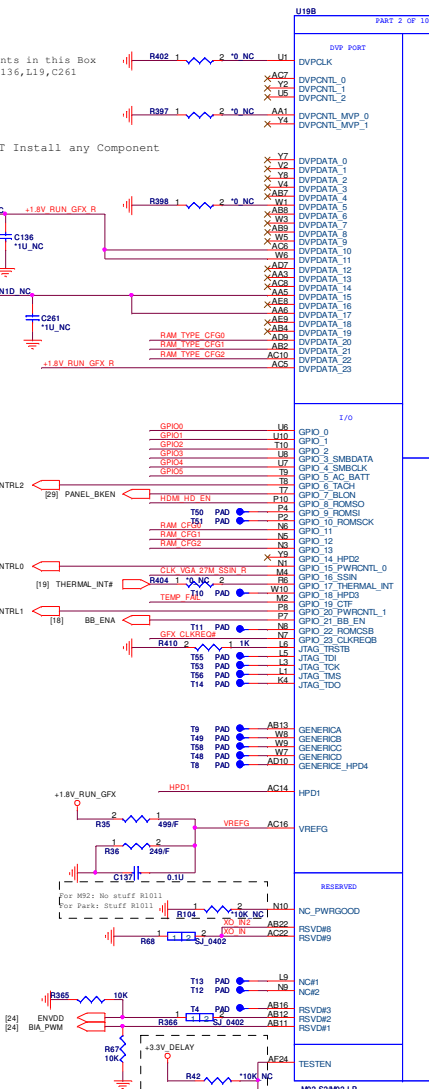
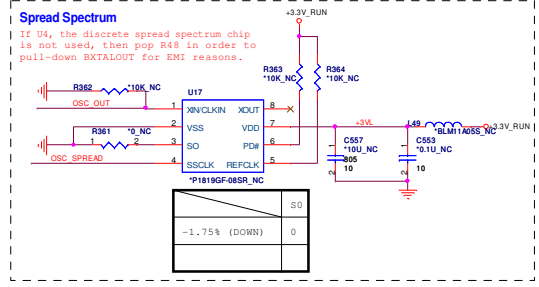
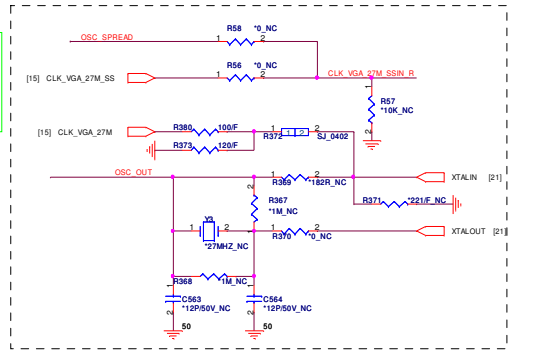
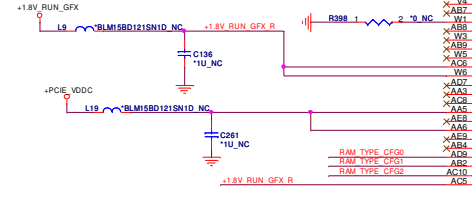


Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	31 level PN
800MHZ	0	0	1	AKD5LGGT502		K4W1G1646E-HC12	
512MB(64M*16) Samsung	0	0	1				
800MHZ	0	1	0	AKD5LGTW00		H5TQ1663BFR-12C	
512MB(64M*16) Hynix	0	1	0				

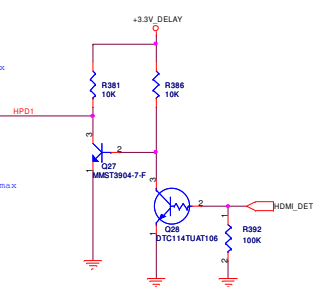


For Park S3:  
Install All components in this Box  
R402, R397, R398, L9, C136, L19, C261

For M92-S2: DO NOT Install any Component in this Box.



Layout Note:  
Place 150 ohm termination resistors close to ATI CHIP.

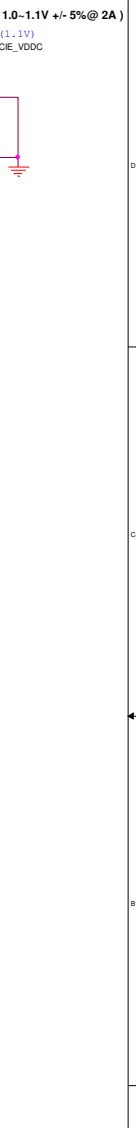
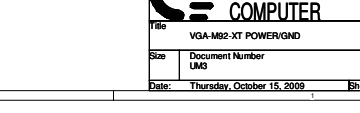
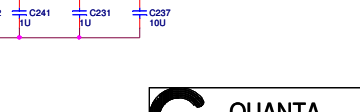
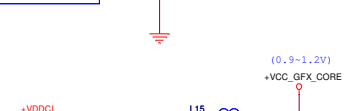
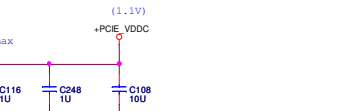
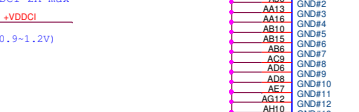
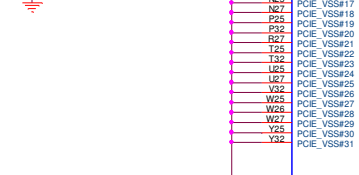
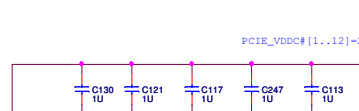
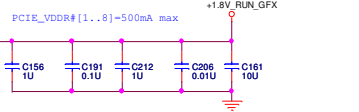
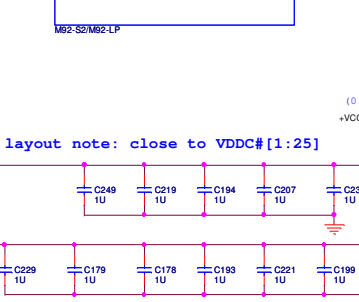
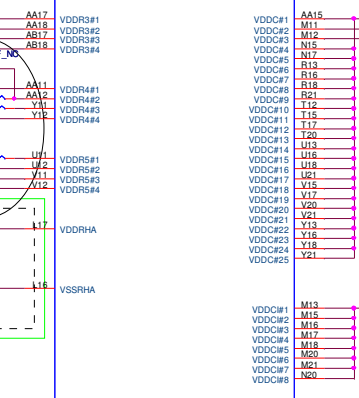
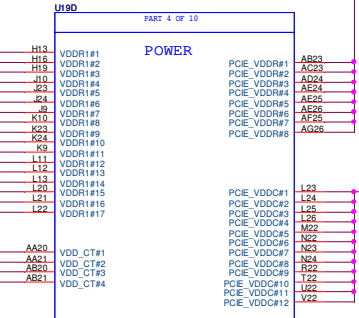
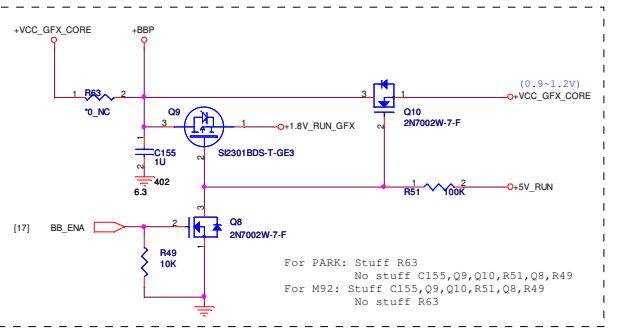
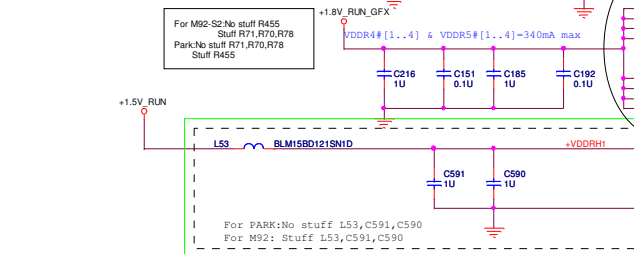
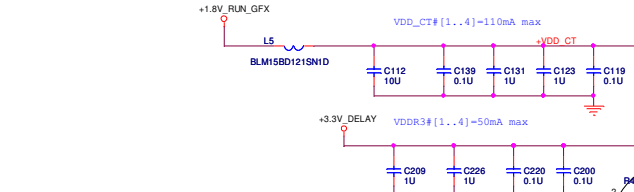
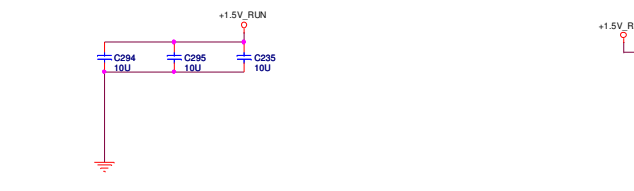
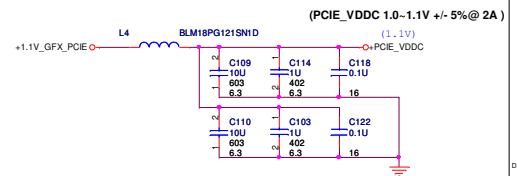
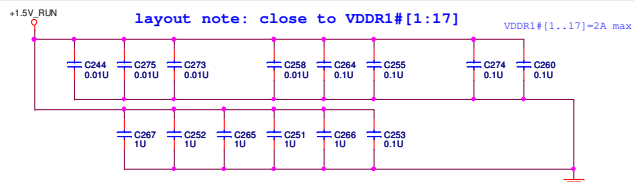


**QUANTA COMPUTER**

Part: VGA-M92-KT10

Rev: 1A

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**QUANTA COMPUTER**

File: VGA-M92-XT POWER/GND

Size: Document Number UMS

Date: Thursday, October 15, 2009

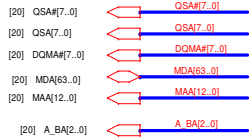
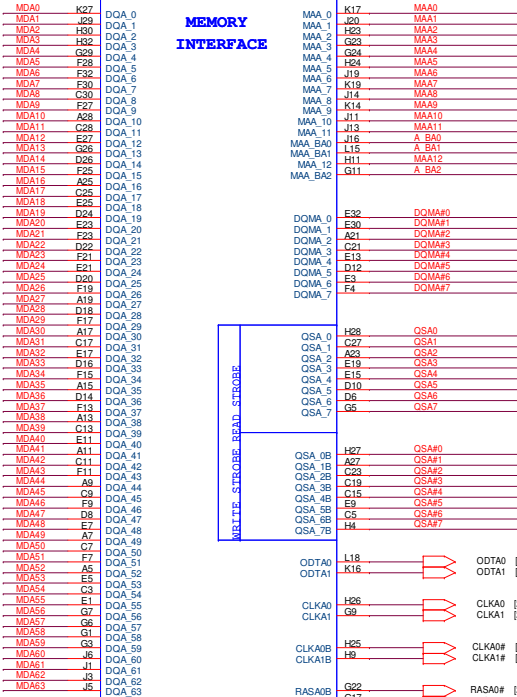
Sheet: 18 of 63

Rev: 1A

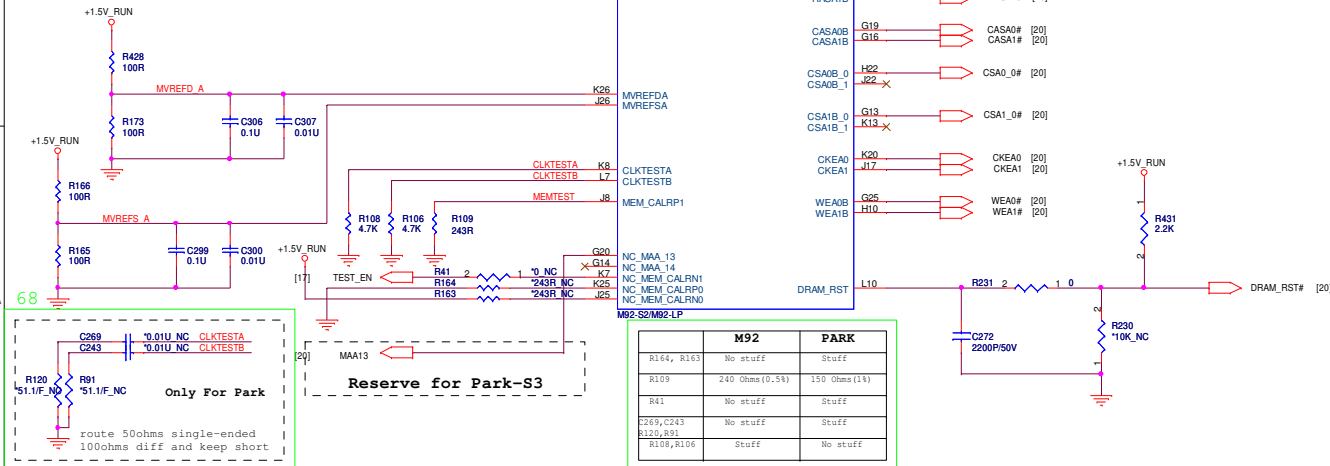
# MEMORY INTERFACE

U18C

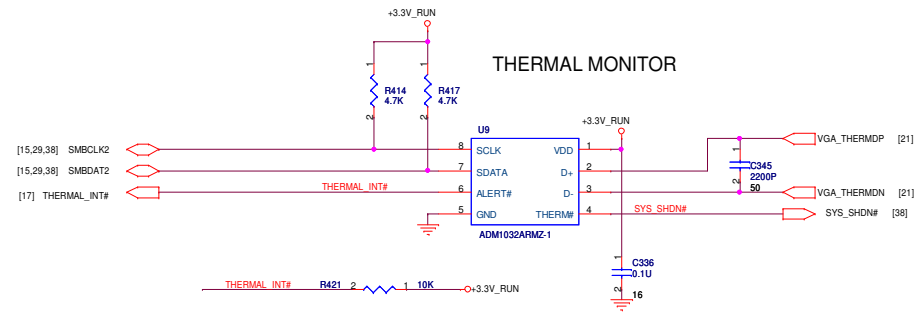
PART 3 OF 10  
**MEMORY INTERFACE**



DIVIDER RESISTORS	DDR3
MVREF TO 1.5V	100R
MVREF TO GND	100R



	M92	PARK
R164, R163	No stuff	Stuff
R109	240 Ohms(0.5%)	150 Ohms(1%)
R41	No stuff	Stuff
C269, C243	No stuff	Stuff
R120, R91	Stuff	No stuff



Change BOM  
Change U7003 from AL001032001 to AL001032002

	M92	Park
R230	No stuff	Stuff
R231	0 ohm	680 ohm
R431	Stuff	No stuff
C272	2200pF PN: CH2226K9B00	68pF PN: CH06806JB01

**QUANTA COMPUTER**

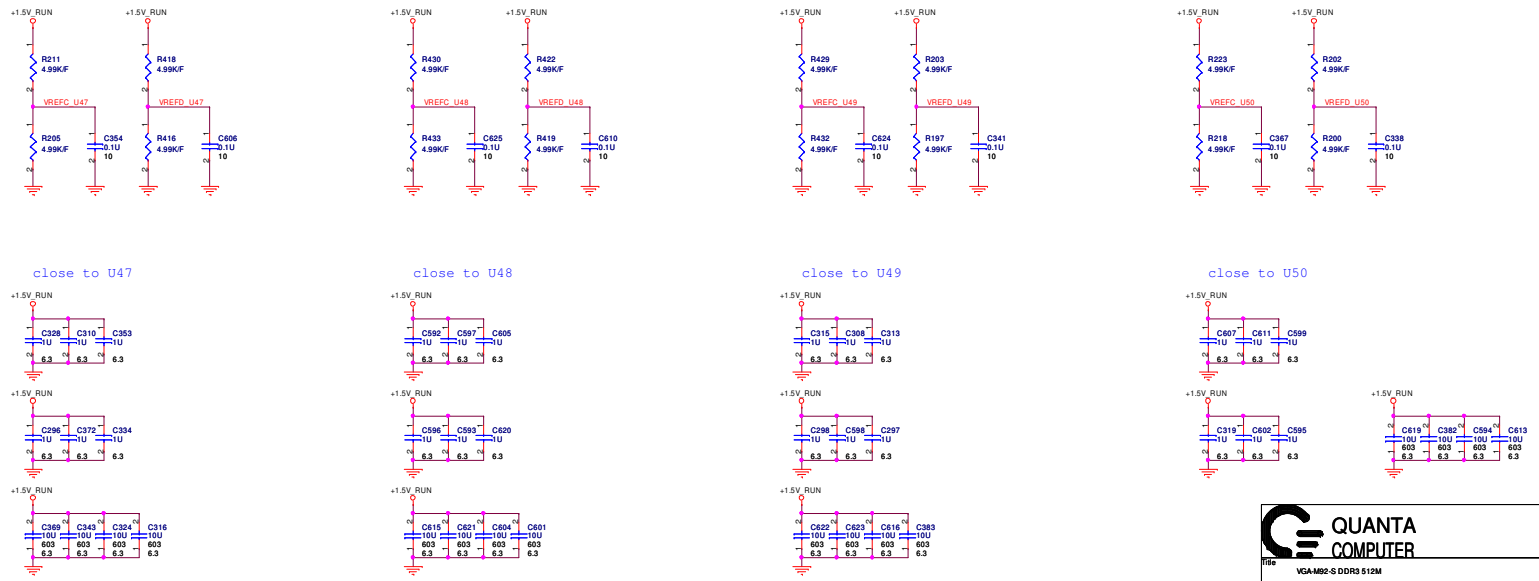
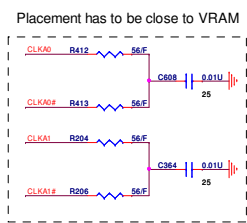
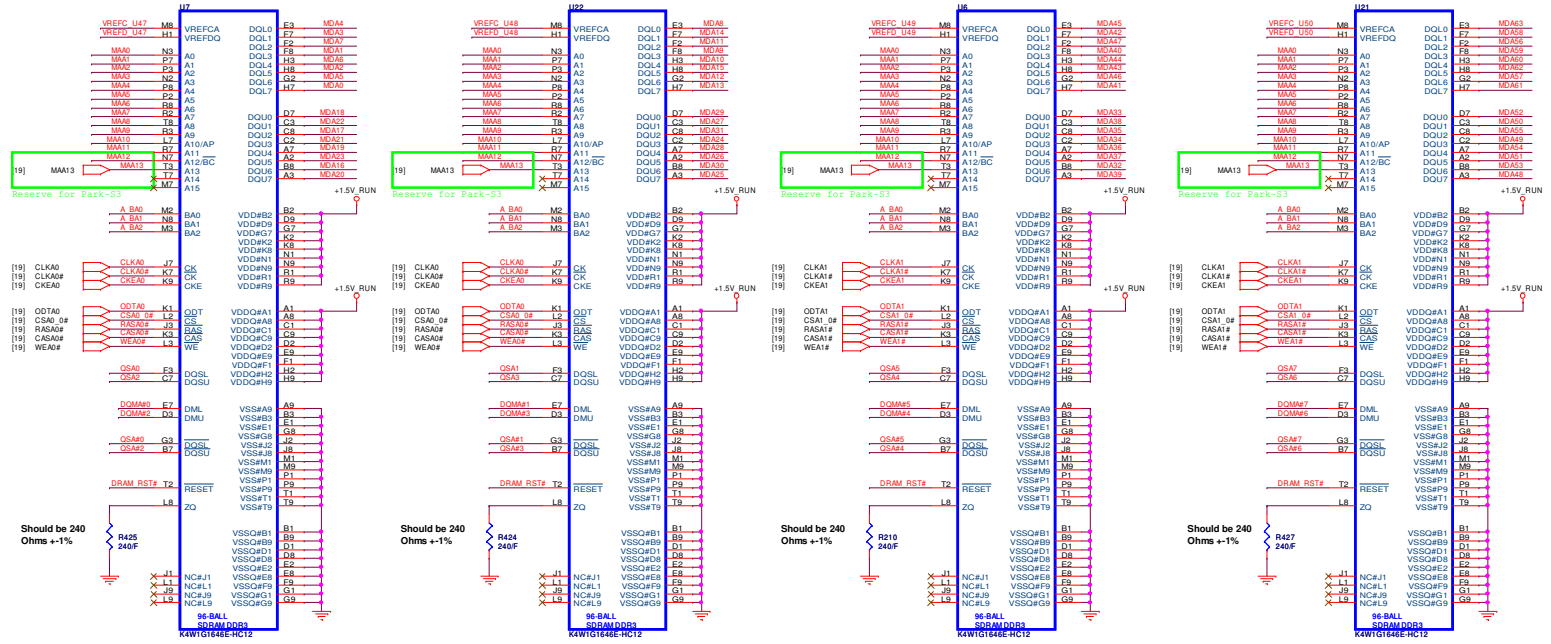
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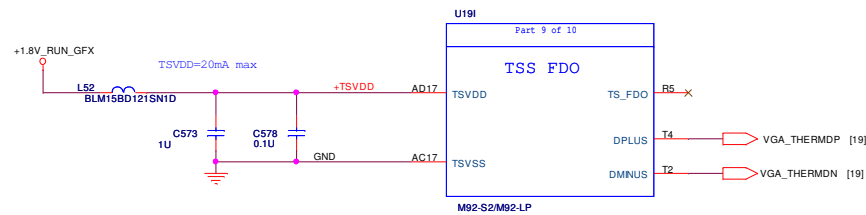
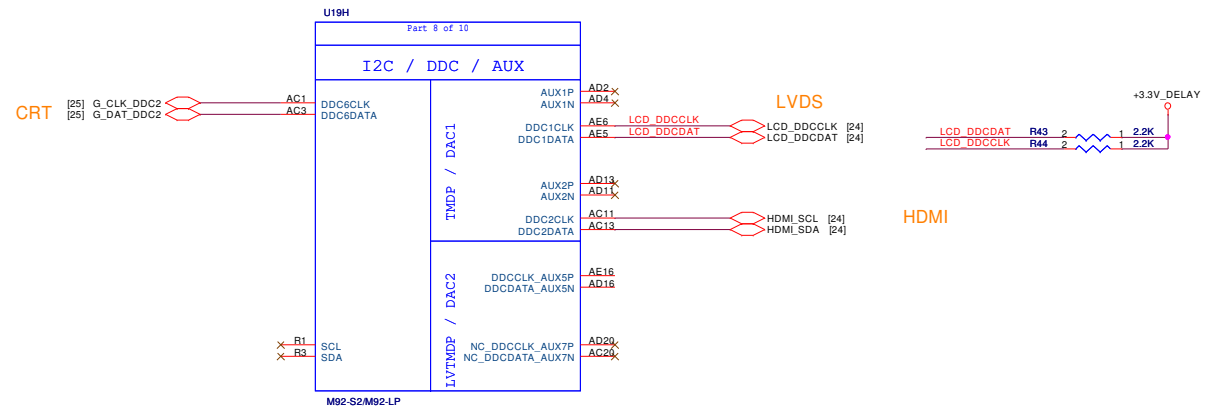
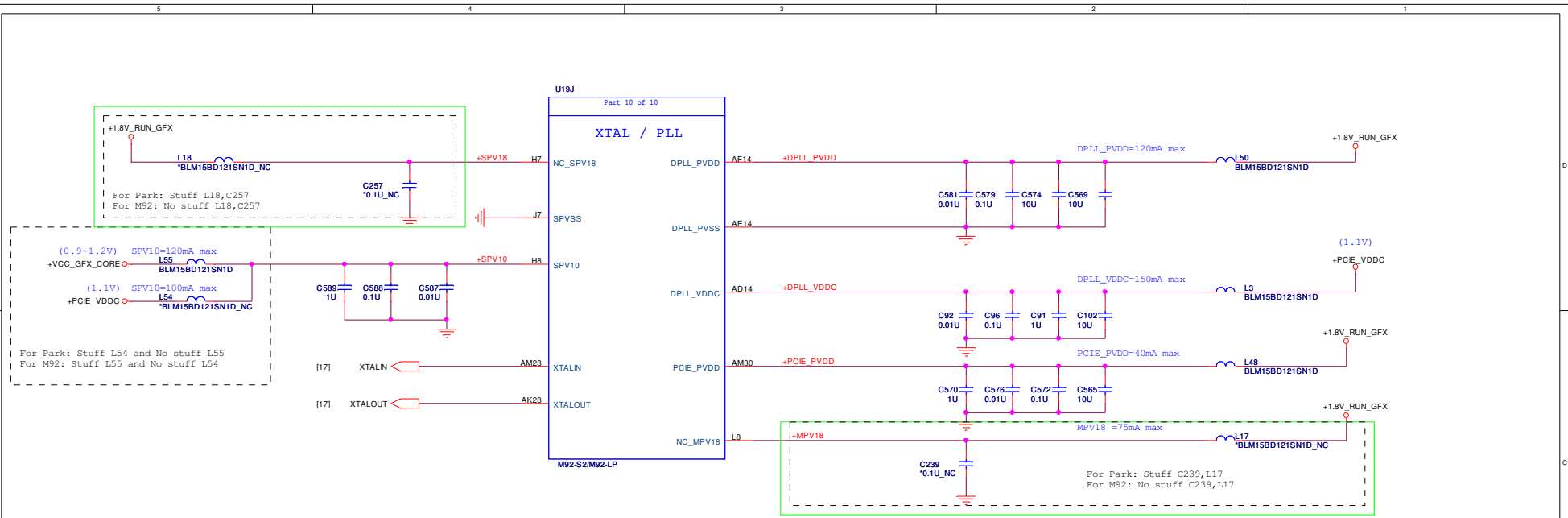
Size: Document Number UMS Rev 1A

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- [19] MD463.0
- [19] MA12.0
- [19] OS47.0
- [19] OS47.0
- [19] DQMM47.0
- [19] DRAM\_RST#
- [19] A\_BA2.0

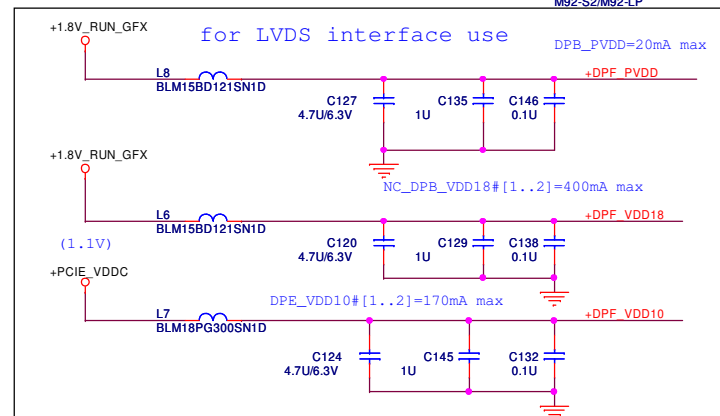
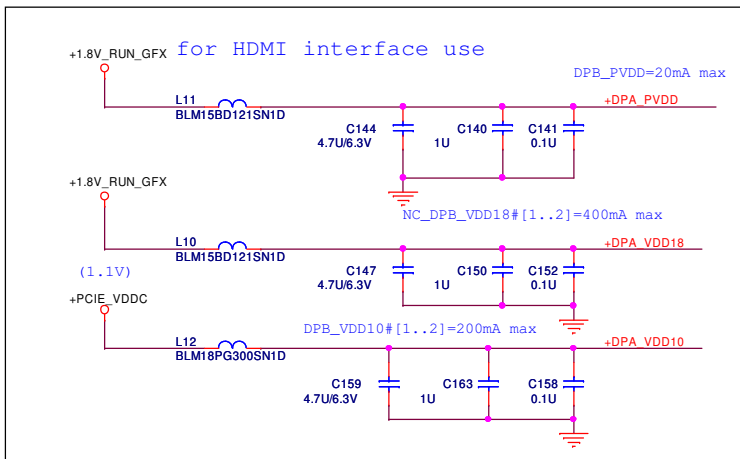
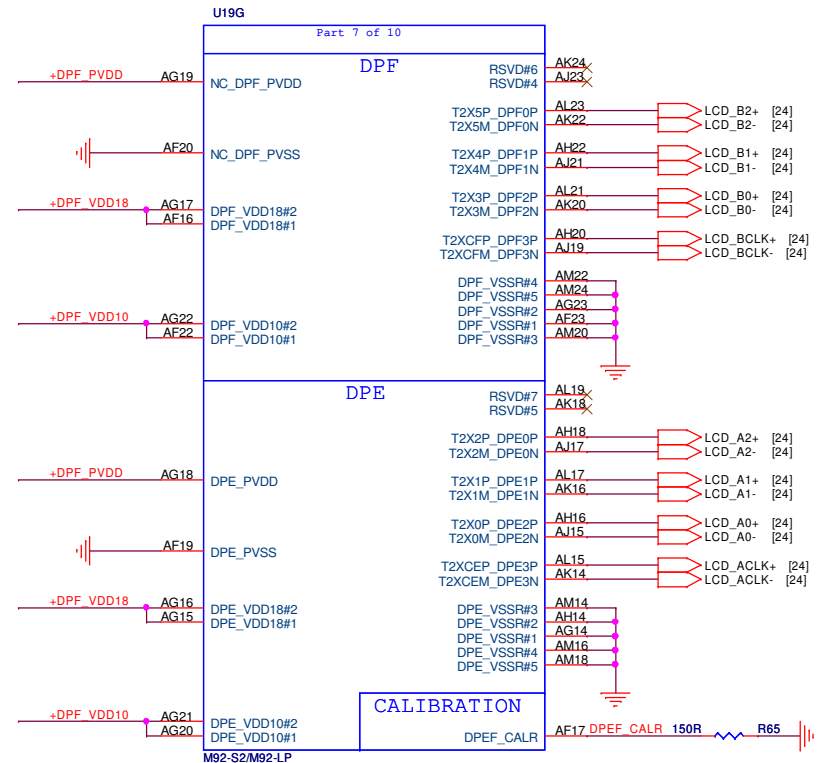
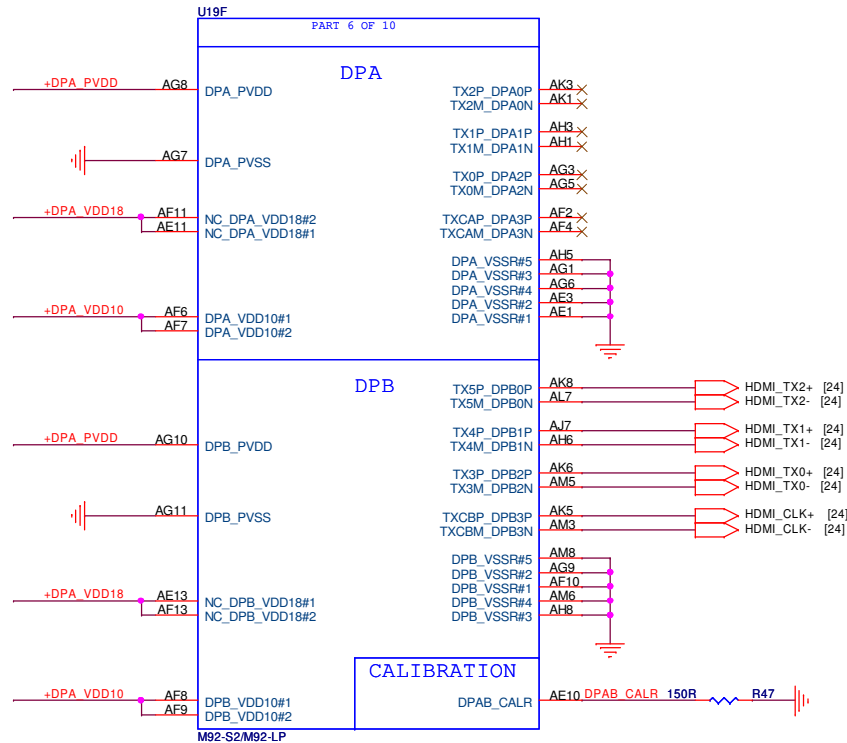
### DDR3





# TMDP(HDMI) INTERFACE

# LVDS INTERFACE



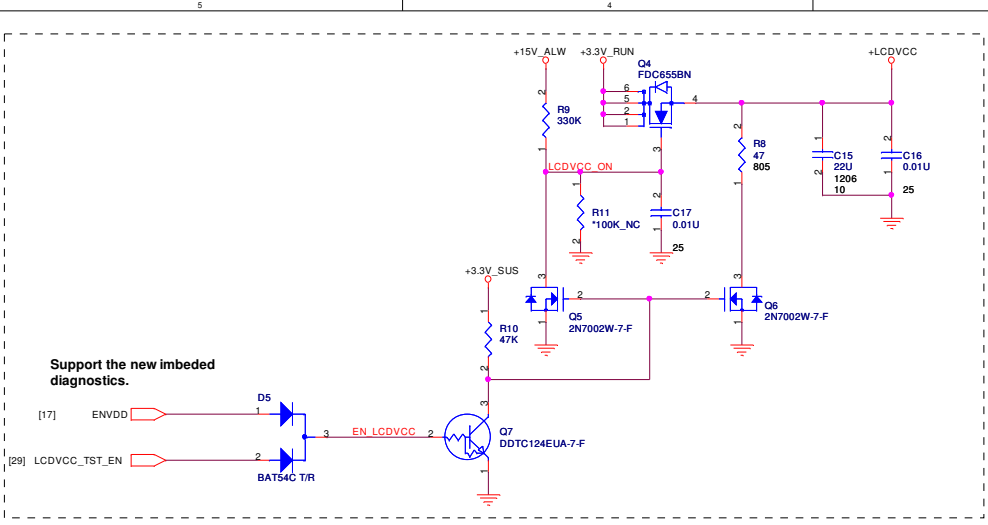
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VGA-M92-XT TMDP I/F		
Size	Document Number	Rev
	UMS	1A
Date:	Thursday, October 15, 2009	Sheet 22 of 63

	5	4	3	2	1
D					
C					
B					
A					

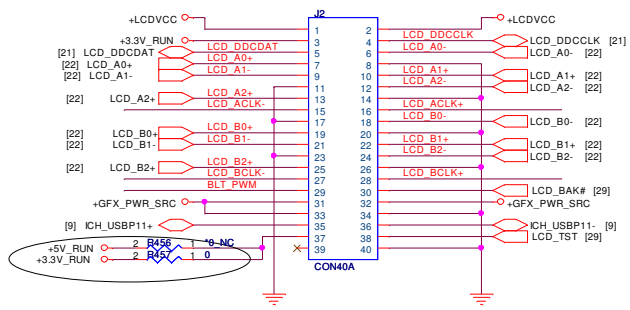
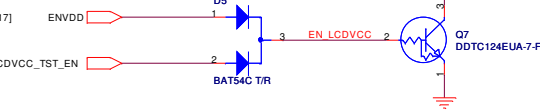


**QUANTA  
COMPUTER**

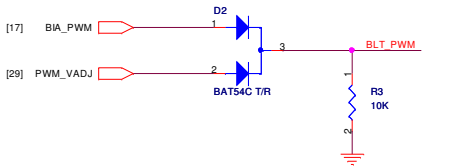
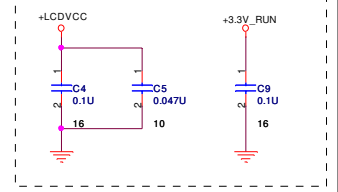
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Size	Document Number		Rev		
	UM3		1A		
Date:	Thursday, October 15, 2009		Sheet	23	of 63



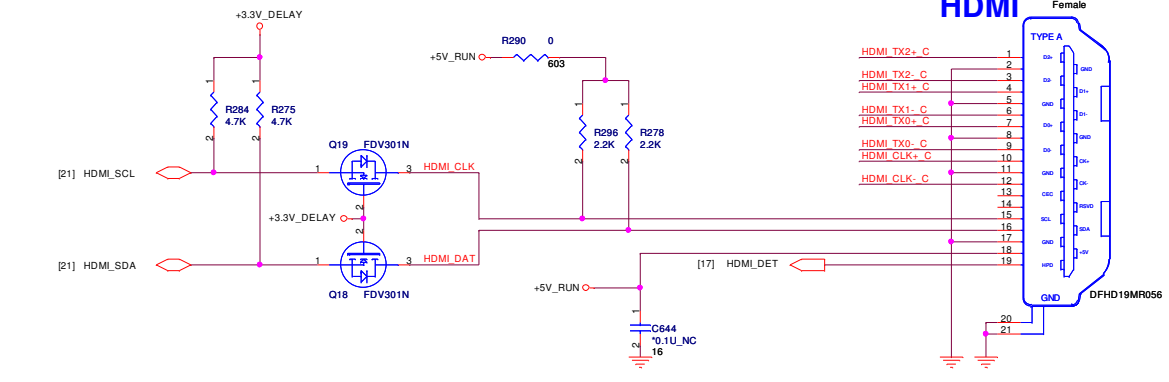
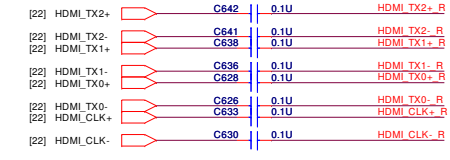
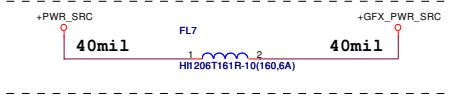
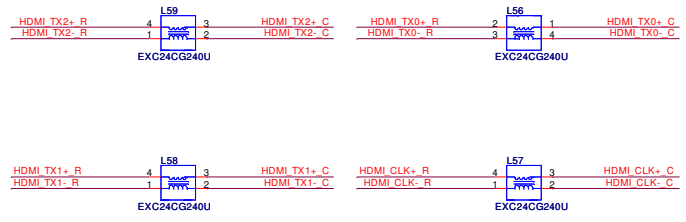
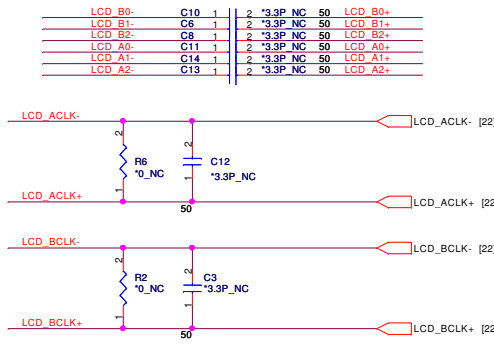
Support the new imbedded diagnostics.



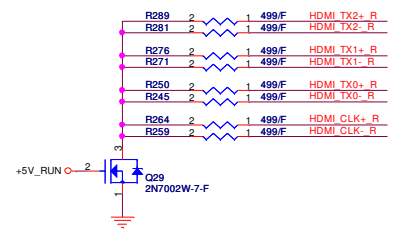
Need to check DF'WF40MR000



Shunt capacitors on LVDS for improving WWAN.



DFHD19MR056



**QUANTA COMPUTER**

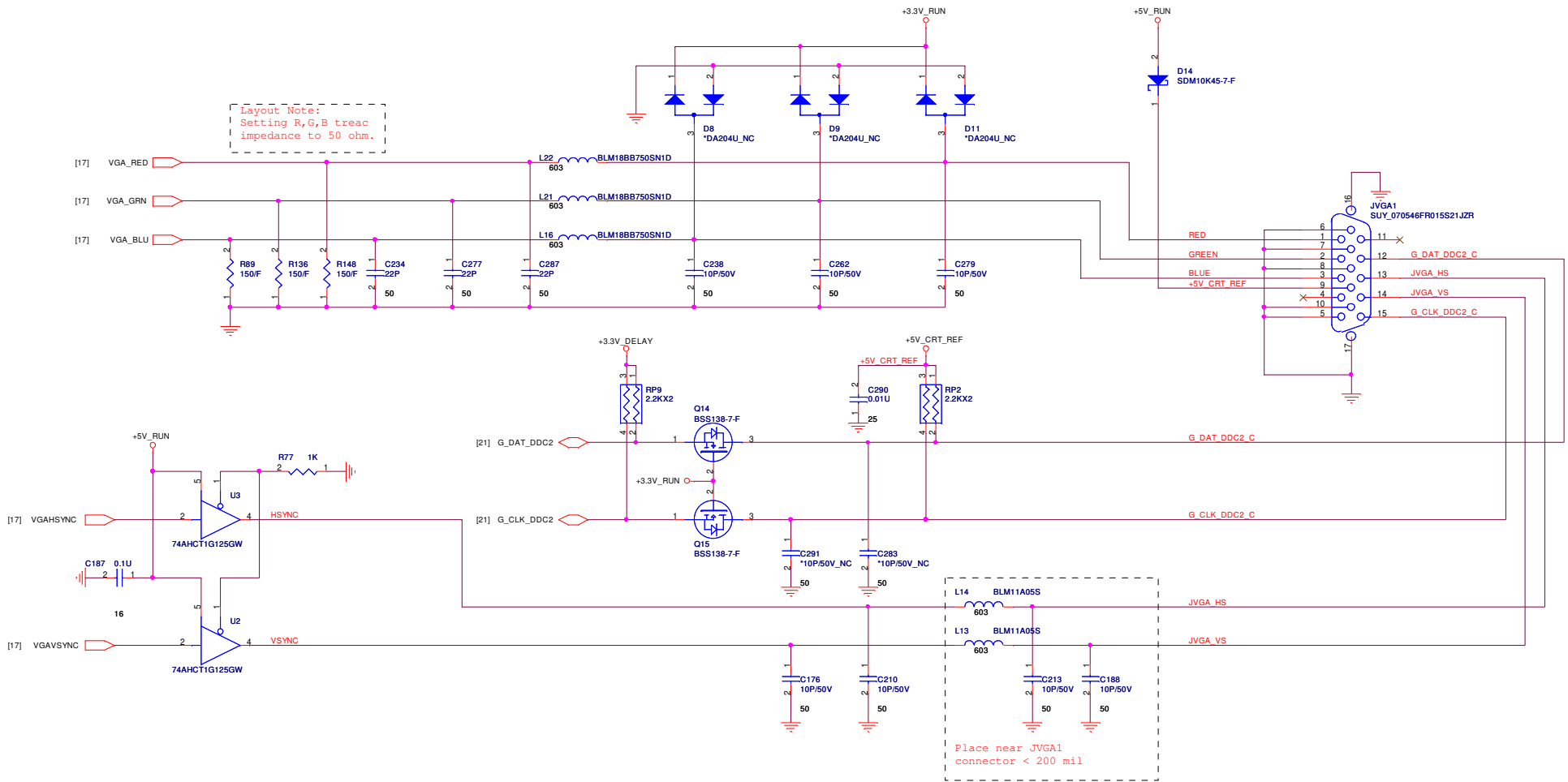
Title: LCD CONN / HDMI CONN

Size: Document Number UMS Rev 1A


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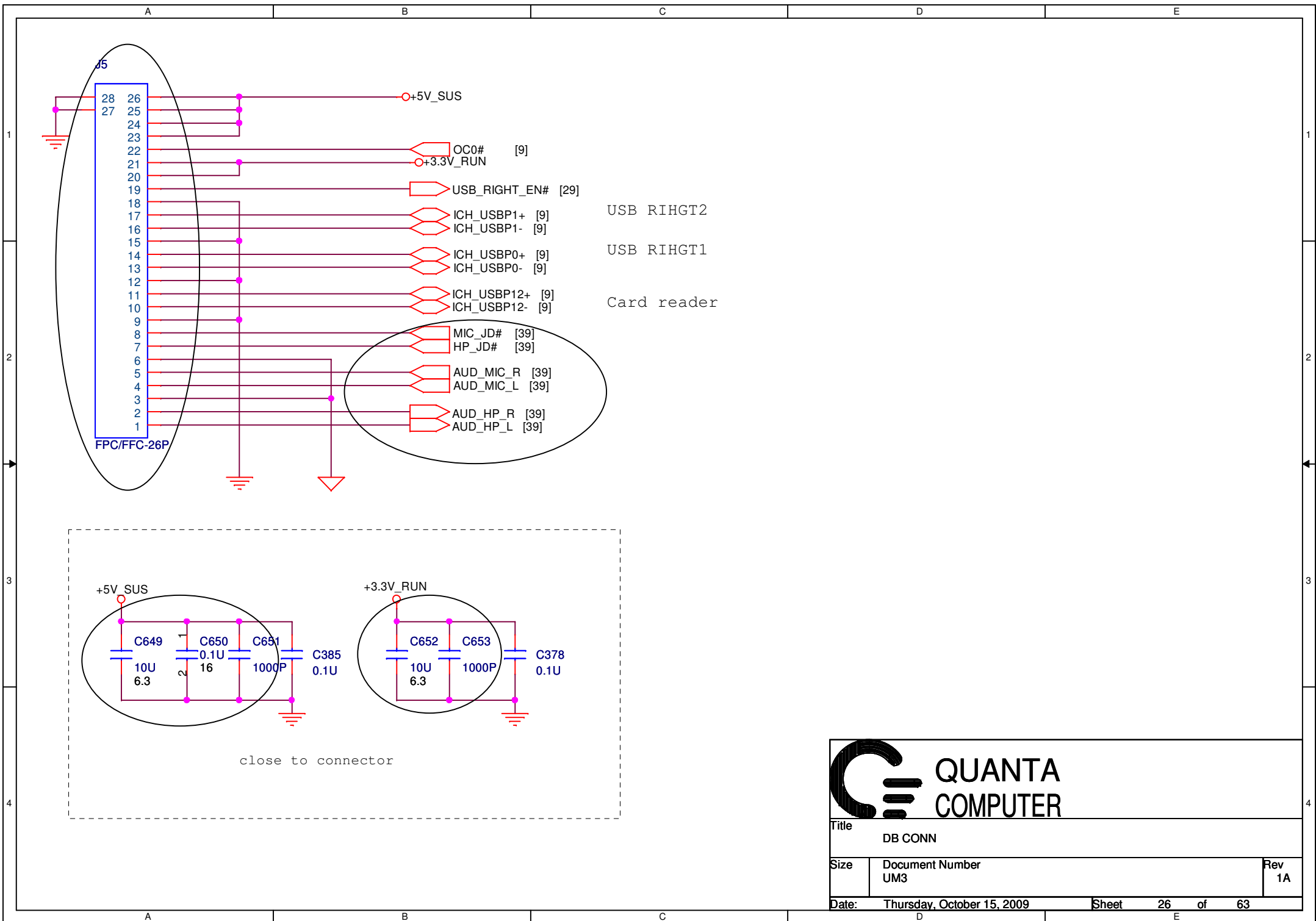


Layout Note:  
Setting R,G,B treac  
impedance to 50 ohm.



Place near JVG1  
connector < 200 mil

 <b>QUANTA COMPUTER</b>		
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Title		
DB CONN		
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		<b>QUANTA COMPUTER</b>
Title Blank Page		
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A


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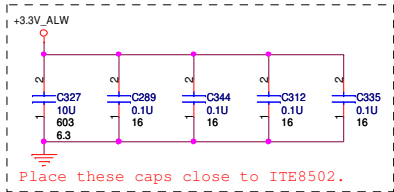
C

D

E

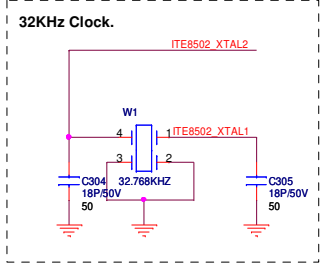
	1	2	3	4	5	6	7	8
A								
B								
C								
D								

 <b>QUANTA COMPUTER</b>		
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oc(v1.0)P38:  
8.2-k pull-up to +V3.3S  
CRB uses a 10-k pull-up to +V3.3S.

**Charge and BAT**  
**CLK, LCD and Thermal**  
**M92**



[36]	KSO[0..17]	U8
[36]	KS[0..7]	
	KSO17	57
	KSO16	56
	KSO15	55
	KSO14	54
	KSO13	53
	KSO12	52
	KSO11	51
	KSO10	46
	KSO9	45
	KSO8	44
	KSO7	43
	KSO6	42
	KSO5	41
	KSO4	40
	KSO3	39
	KSO2	38
	KSO1	37
	KSO0	36
	KS17	65
	KS16	64
	KS15	63
	KS14	62
	KS13	61
	KS12	60
	KS11	59
	KS10	58
	KS17	65
	KS16	64
	KS15	63
	KS14	62
	KS13	61
	KS12	60
	KS11	59
	KS10	58

### ITE8502E LQFP-128L

#### KEYBOARD

#### ADC/DAC

#### PWM

#### LPC

#### IR/UART

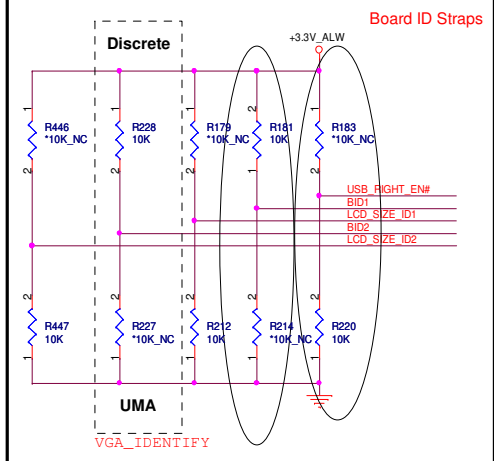
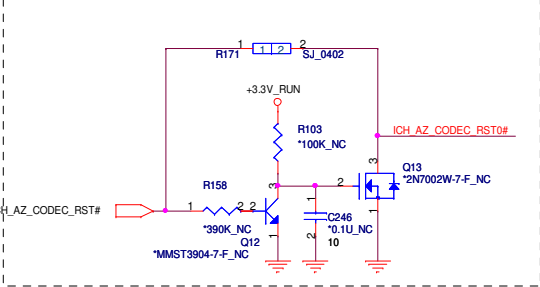
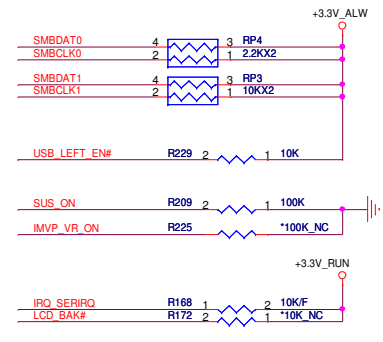
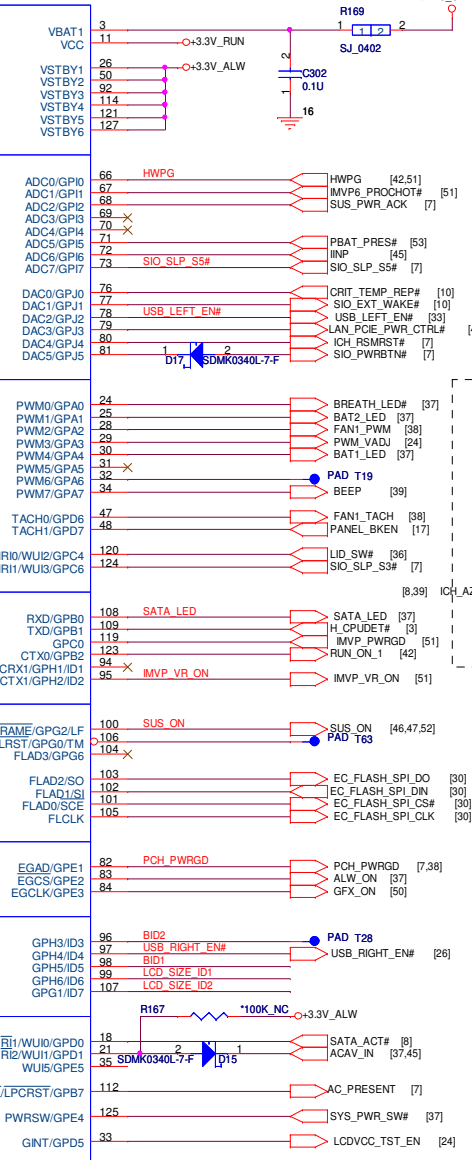
#### SMBUS

#### LPC/FWH FLASH

#### EGPC

#### PS/2

#### GPIO



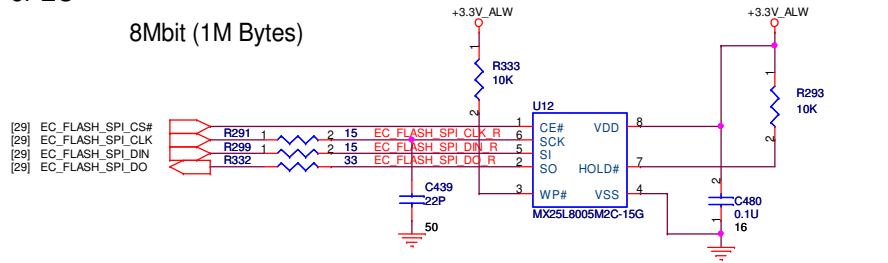
	LCD_SIZE_ID1 (99)	LCD_SIZE_ID2 (107)
14"	0	0
15.6"	1	0
17"	0	1

BID1	BID0	UM3B(UMA)	UM3(Dis)
0	0	SSI (X00)	SSI (X00)
0	1	PT (X01)	PT (X01)
1	0	ST (X02)	ST (X02)
1	1	OT (A00)	OT (A00)
0	0	(A01)	(A01)

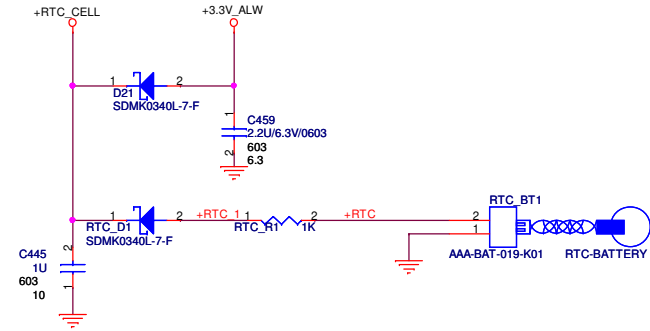


For EC

8Mbit (1M Bytes)

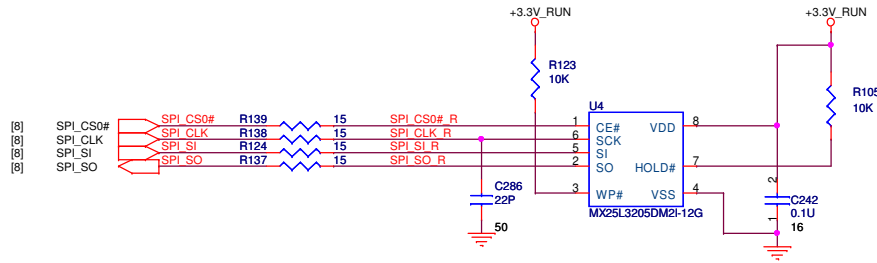


RTC BATTERY



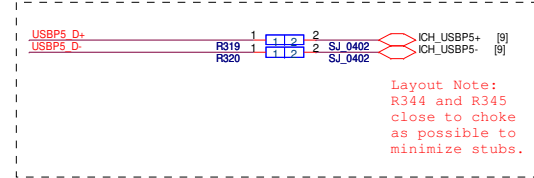
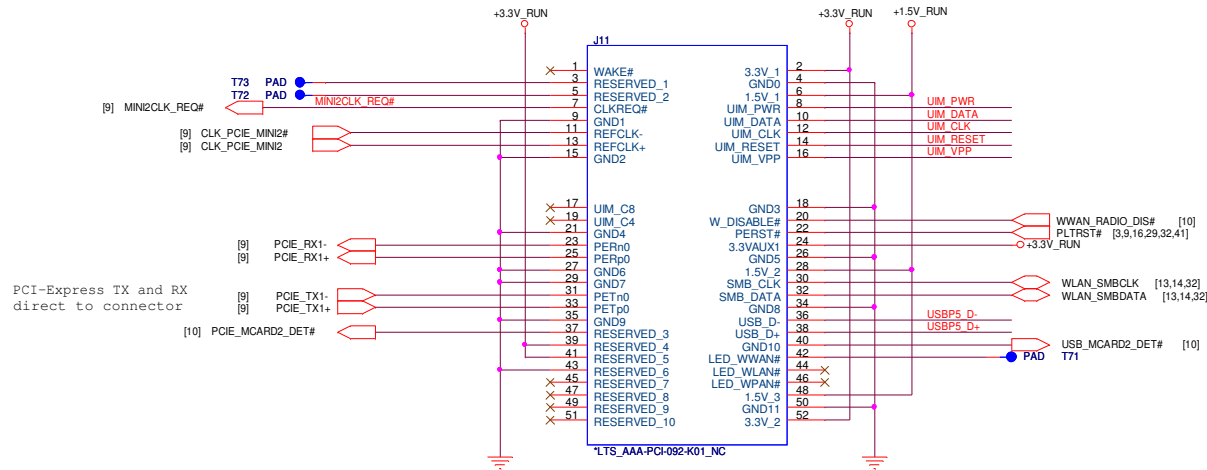
For PCH

32Mbit (4M Bytes)

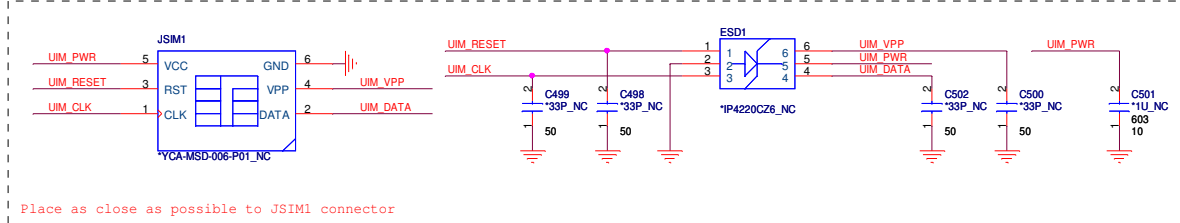


Title FLASH/RTC		
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### MiniCard WWAN connector

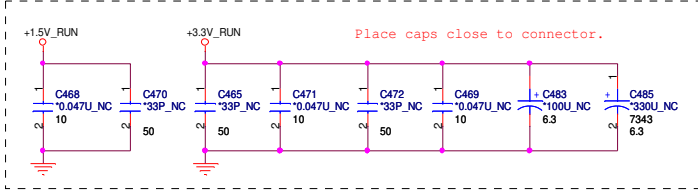


Layout Note:  
R344 and R345  
close to choke  
as possible to  
minimize stubs.



Place as close as possible to JSM1 connector

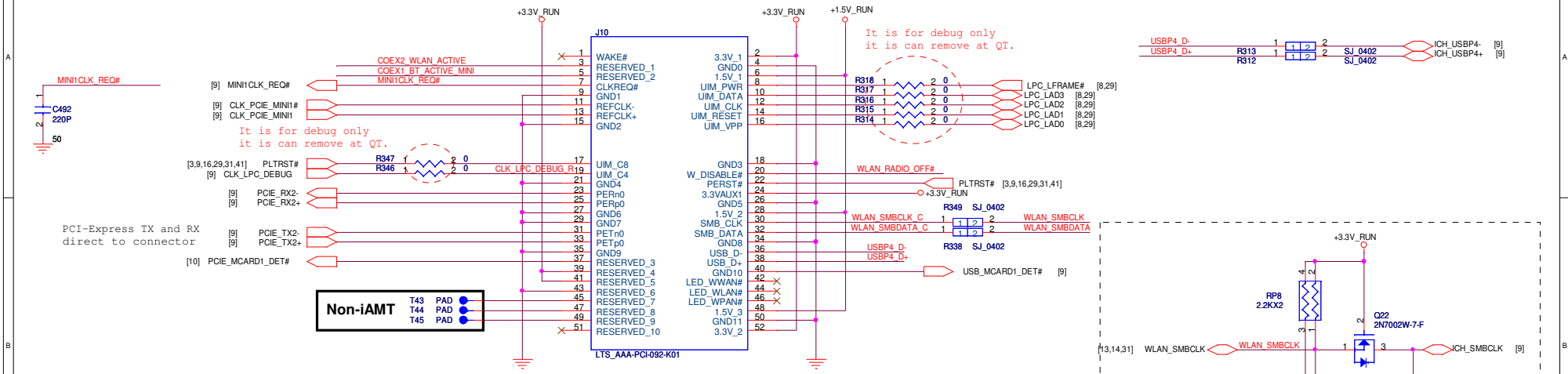
DFHS06FR043



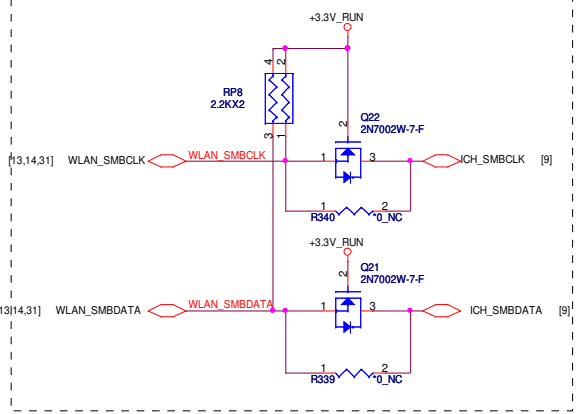
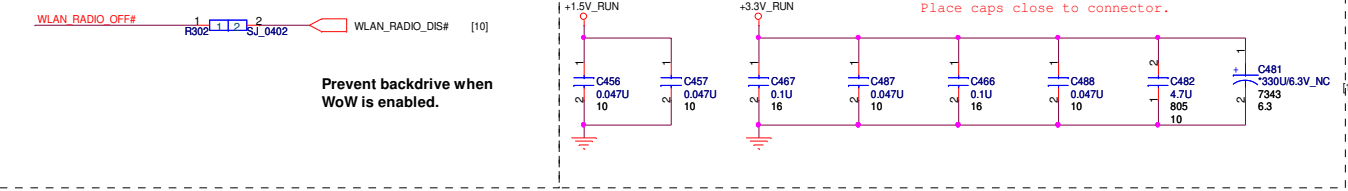
Place caps close to connector.



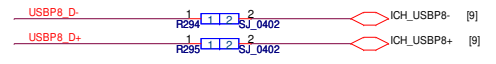
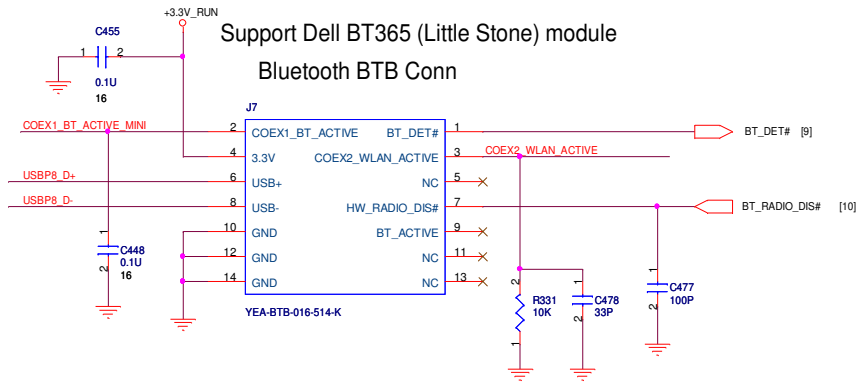
# MiniCard WLAN connector



## Support for WoW

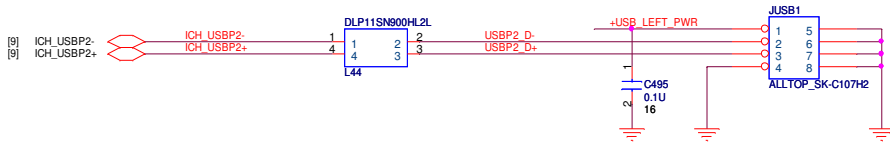


## Support Dell BT365 (Little Stone) module Bluetooth BTB Conn



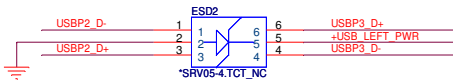


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

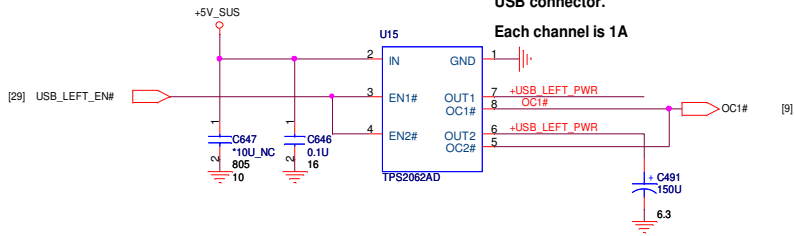


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

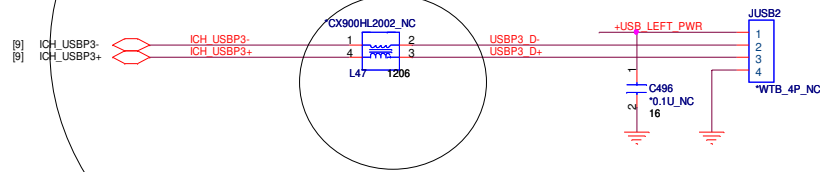


Place one 150uF cap by each USB connector.  
Each channel is 1A



REV FOR 17"

Add L47 ,C496 , JUSB2 for UM5



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QUANTA  
COMPUTER

Title		
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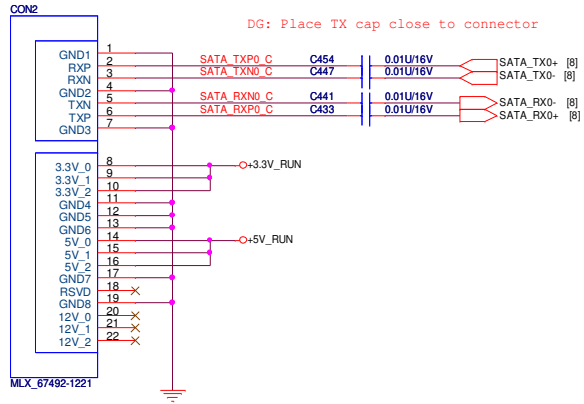
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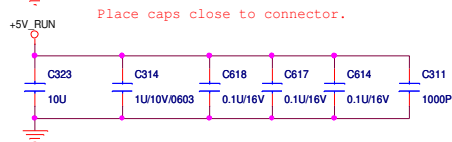
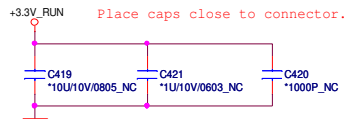
**SATA Connector.**



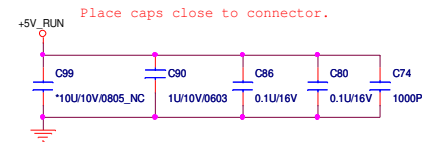
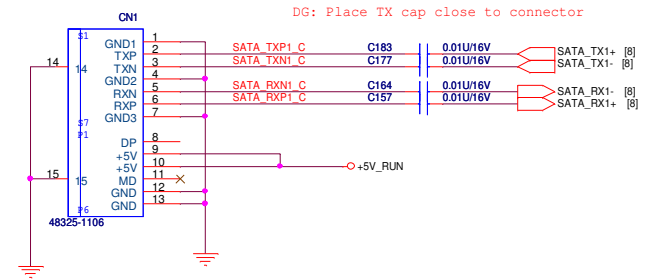
UM5與UM3/6不同，只差在高度，footprint沒變

UM5/UM5B  
 PN:DFHS22FR137  
 Mfr:67492-1224

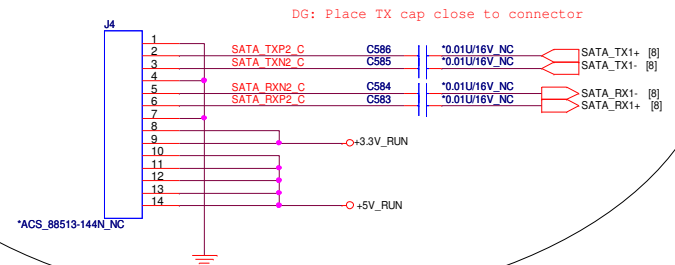
UM3/UM3B/UM6/UM6B  
 PN:DFHS22FR0B2  
 Mfr:67492-1921



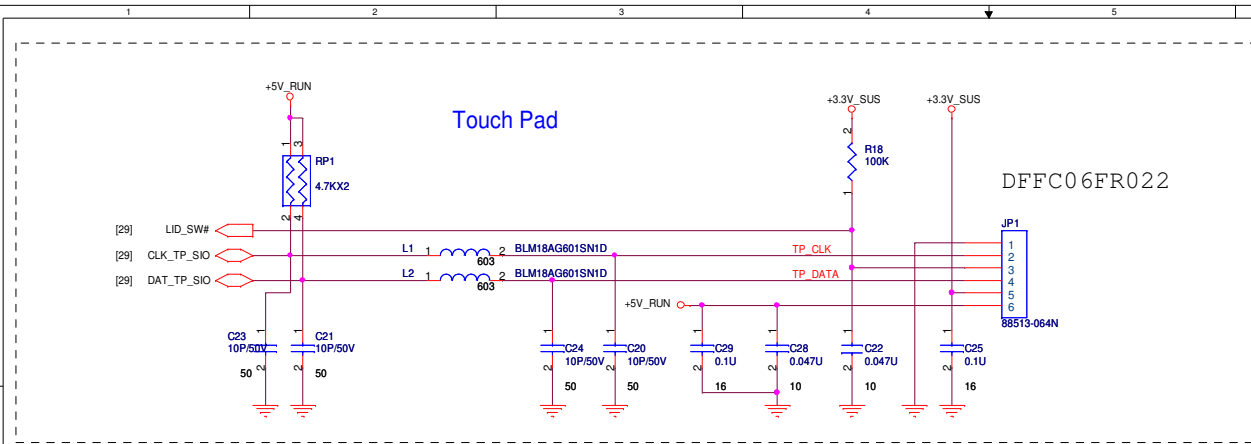
**ODD Connector**



REV FOR 15.6"

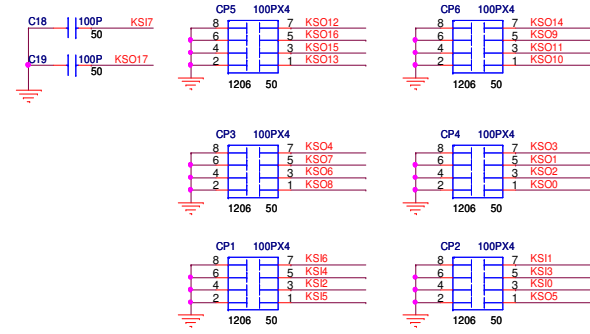
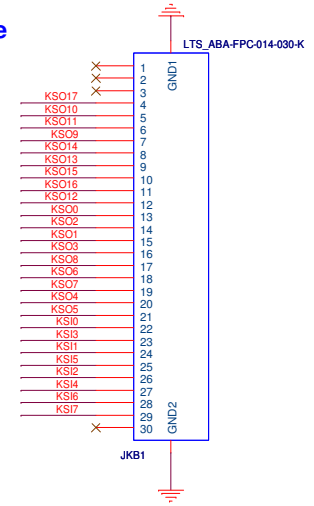


Title		
SATA (HDD&CD_ROM)		
Size	Document Number	Rev
	UM5	1A
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KEYBOARD CONNECTOR

Top side

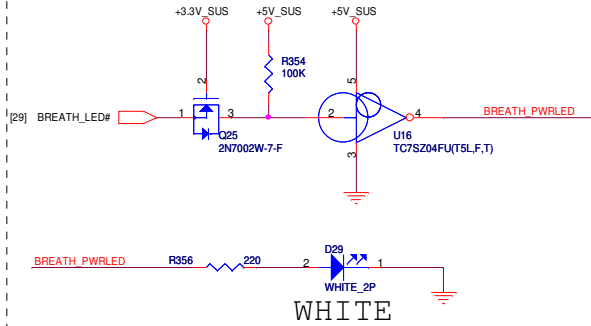


100P CAPS CLOSE TO JKB1

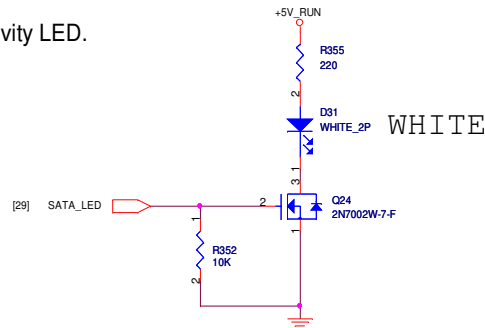


Title		
TOUCH PAD, KB		
Size	Document Number	Rev
	UM3	1A
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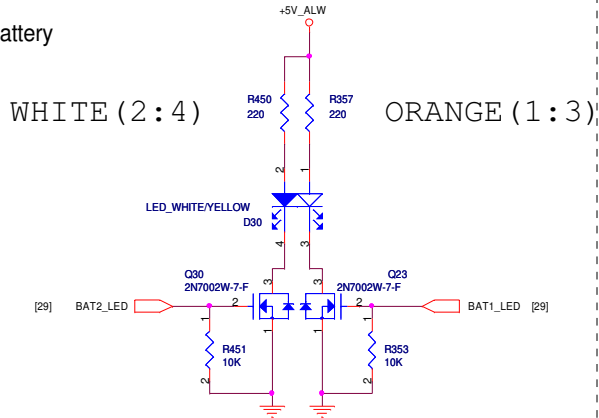
Power



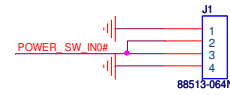
HDD activity LED.



Battery



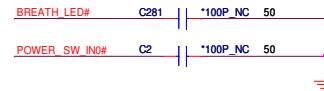
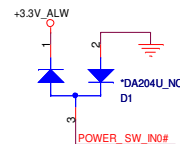
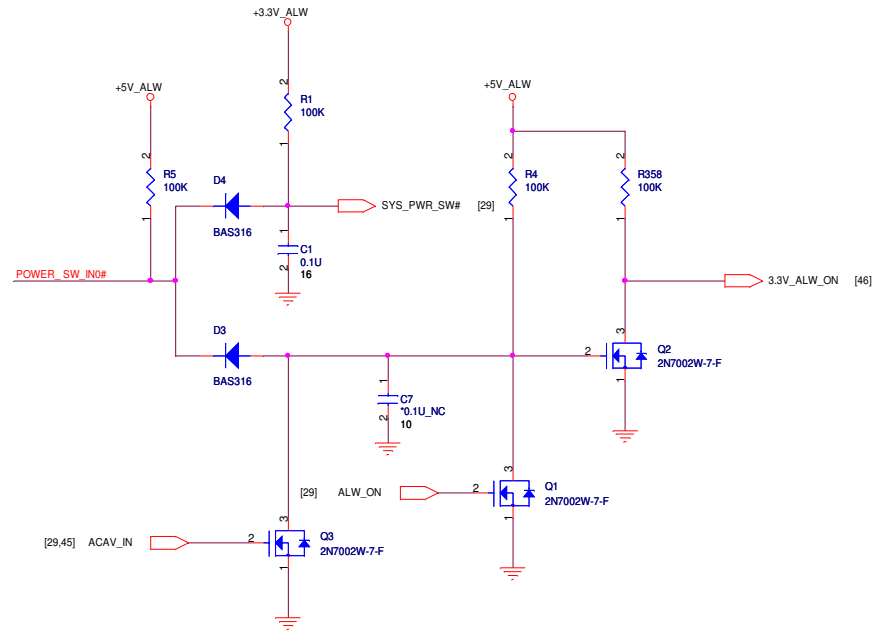
Power button Cable



Stephen 7/31

DFFC04FR014

3VALW ON POWER LOGIC



**QUANTA COMPUTER**

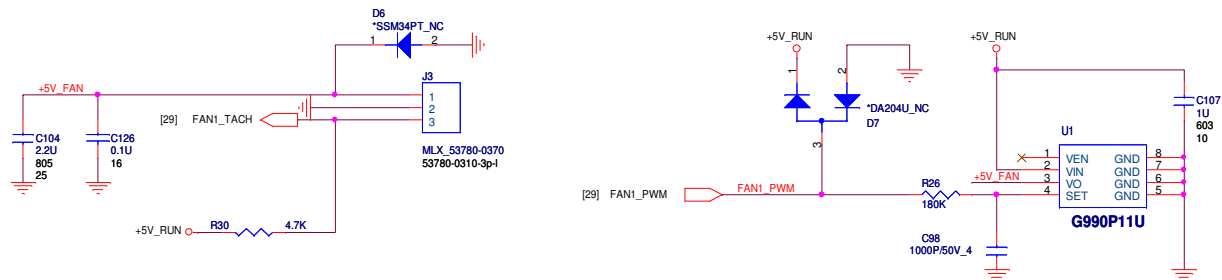
Title: SWITCH, LED

Size	Document Number	Rev
	UM3	1A

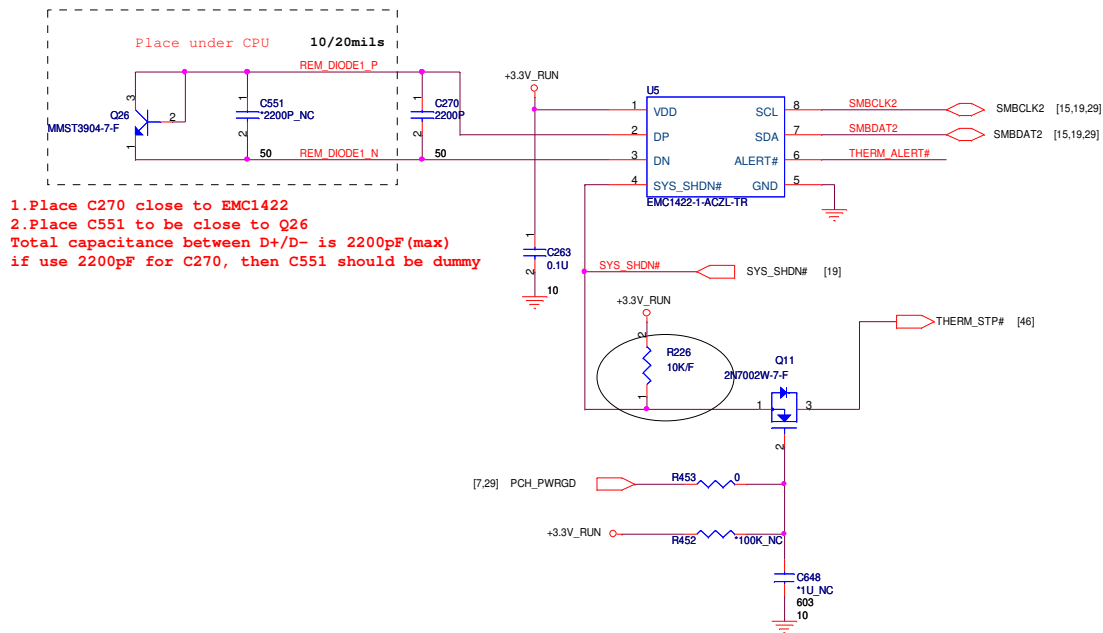
Date: Thursday, October 15, 2009 Sheet 37 of 63

FAN CONTROL

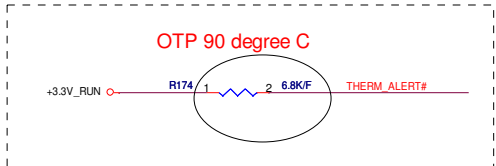
6/23 COPY FROM RM6



Thermal sensor



- 1. Place C270 close to EMC1422
- 2. Place C551 to be close to Q26
- Total capacitance between D+/D- is 2200pF(max)
- if use 2200pF for C270, then C551 should be dummy

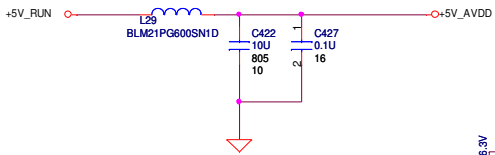


**QUANTA COMPUTER**

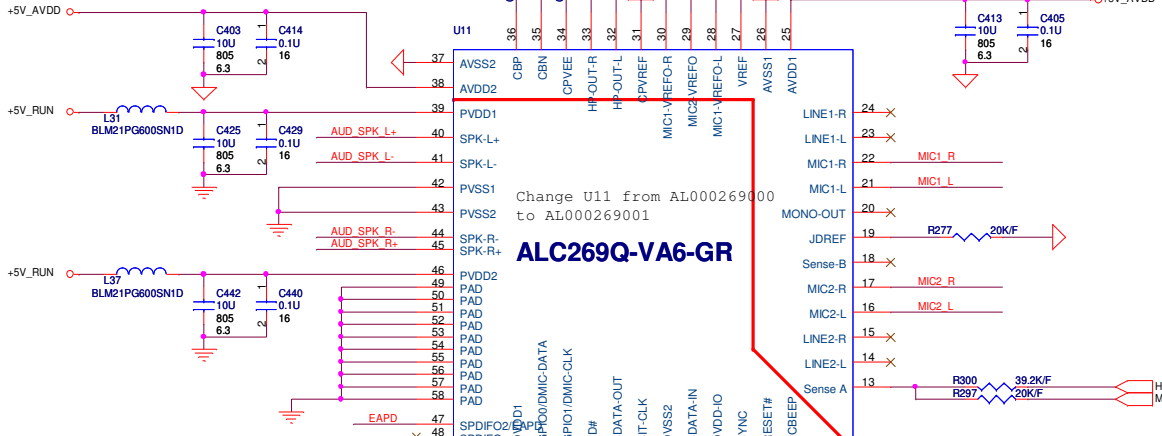
Title: FAN & THERMAL

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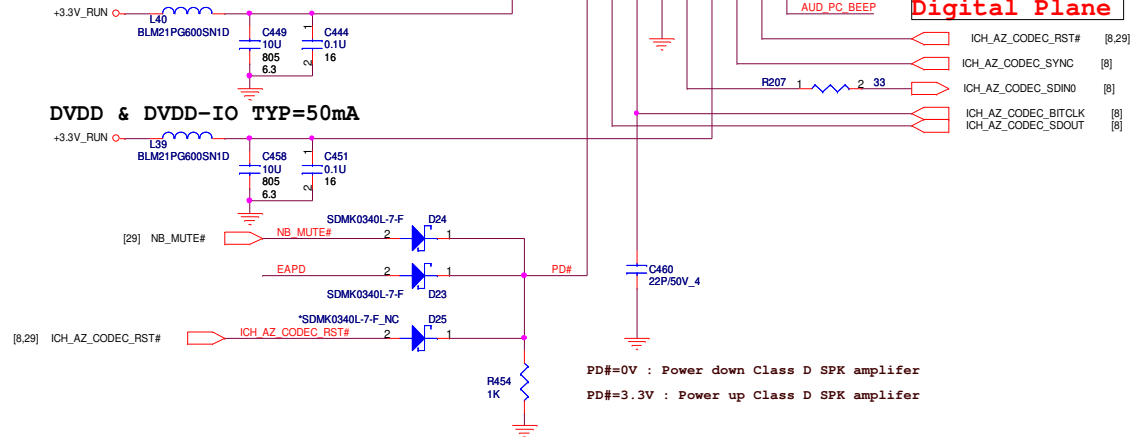
AVDD1, AVDD2 TYP=48mA



**ALC269Q-VA6-GR**

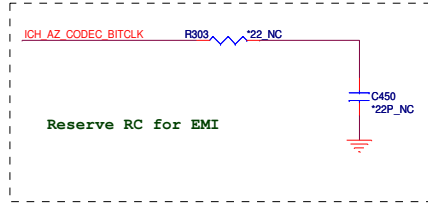
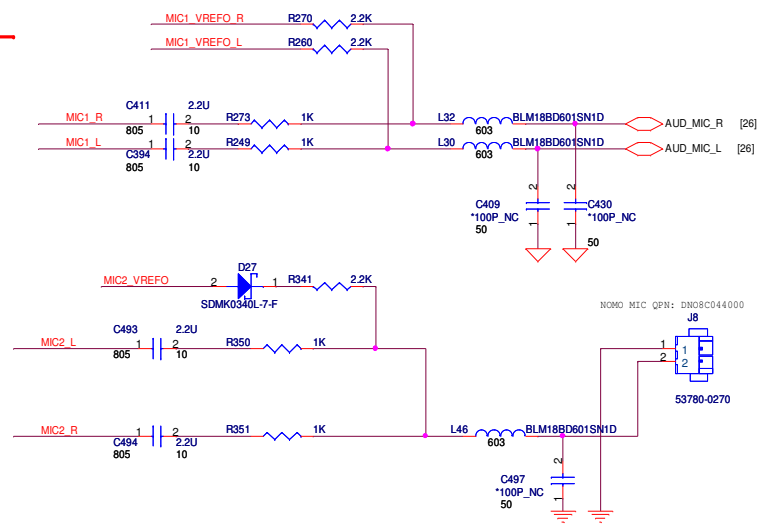
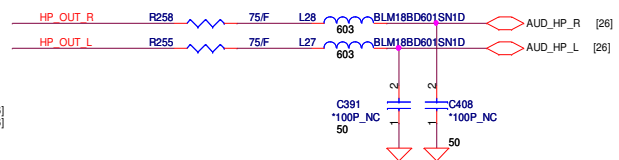
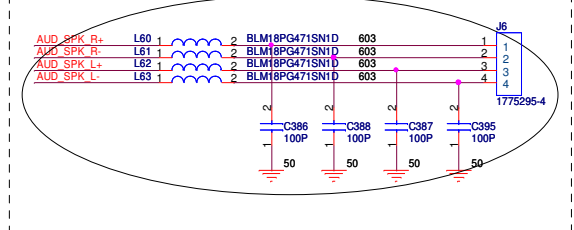
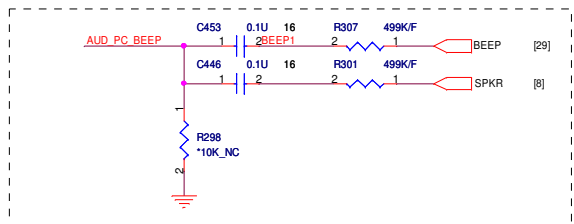
AVDD1, AVDD2 TYP=48mA

DVDD & DVDD-IO TYP=50mA

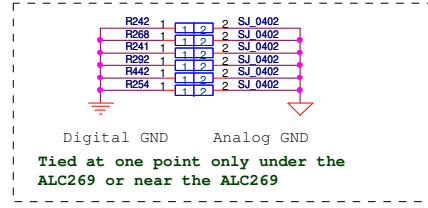


PD#=0V : Power down Class D SPK amplifier  
 PD#=3.3V : Power up Class D SPK amplifier

Analog Plane  
 Digital Plane



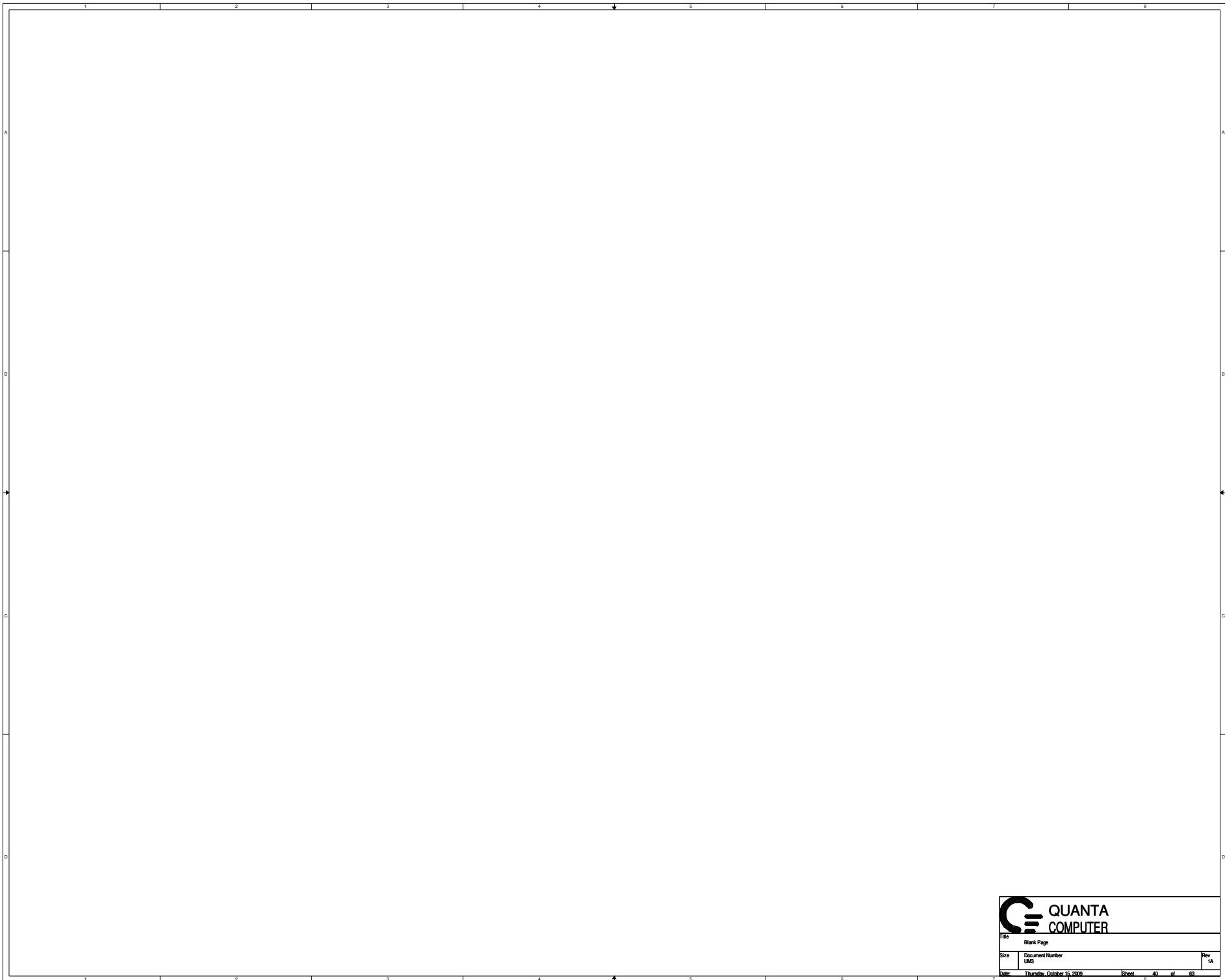
Reserve RC for EMI




Digital GND Analog GND  
 Tied at one point only under the  
 ALC269 or near the ALC269

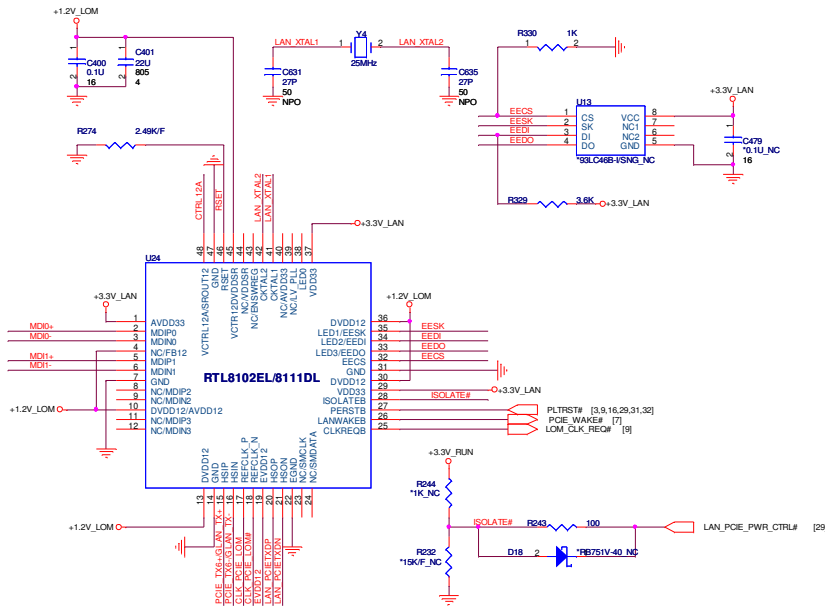


Title Azelia CODEC		
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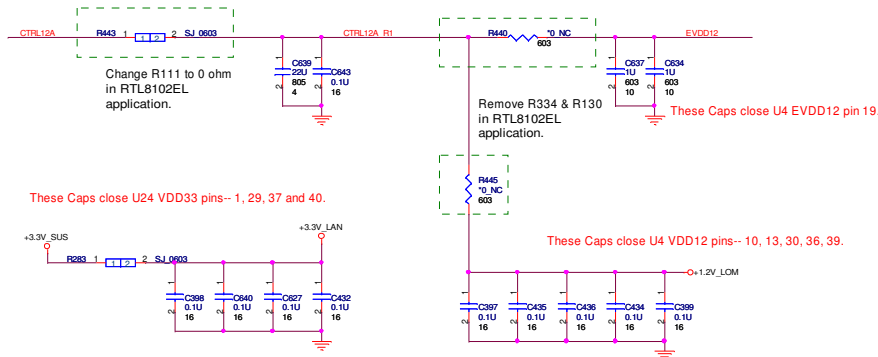
		<b>QUANTA</b> <b>COMPUTER</b>
File		Blank Page
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Note 1: The Trace length between R111 and 8111DL's Pin 1 must be within 0.5 cm. C199 and C171 to R111 must be within 0.5cm. Refer to Layout guide for more detail.

- [9] CLK\_PCIE\_LOM
- [9] CLK\_PCIE\_LOM#
- [9] PCIE\_RX6+GLAN\_RX#
- [9] PCIE\_RX6-GLAN\_RX#
- [9] PCIE\_TX6+GLAN\_TX#
- [9] PCIE\_TX6-GLAN\_TX#

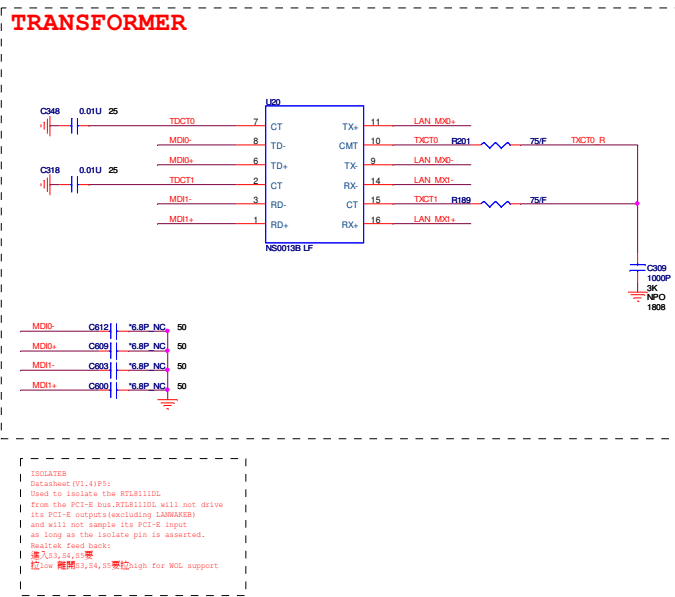


These Caps close U24 VDD33 pins-- 1, 29, 37 and 40.

These Caps close U4 VDD12 pins-- 10, 13, 30, 36, 39.

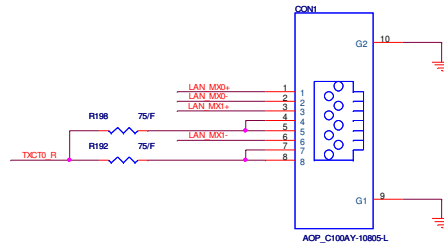
Change R111 to 0 ohm in RTL8102EL application.

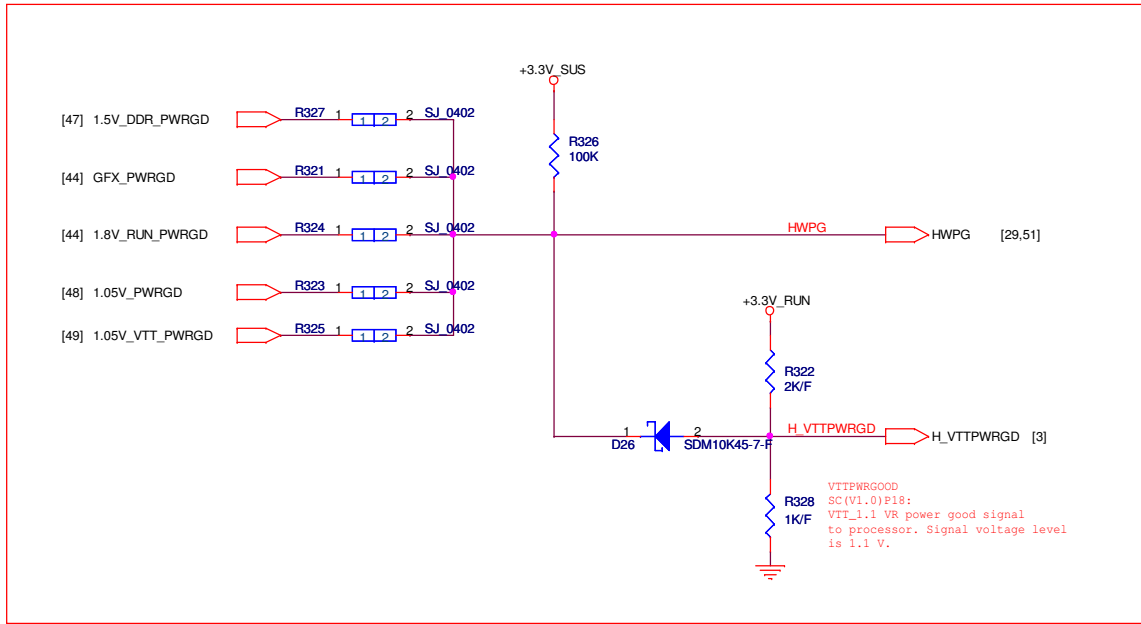
Remove R334 & R130 in RTL8102EL application.



ISOLATE#  
 Database(V1.4)P1  
 Used to isolate the RTL8111DL  
 from the PCIe Bus. RTL8111DL will not drive  
 its PCIe outputs(excluding LANWAKEB)  
 and will not sample its PCIe input  
 as long as the isolate pin is asserted.  
 Backtalk feed back:  
 1. 3.3V\_50mA 1.0A  
 2. 3.3V\_50mA 1.0A  
 3. 3.3V\_50mA 1.0A  
 4. 3.3V\_50mA 1.0A

### RJ-45 Connector COPY FROM UM2





Title			Rev
System Reset Circuit			1A
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	UM3		
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QUANTA  
COMPUTER

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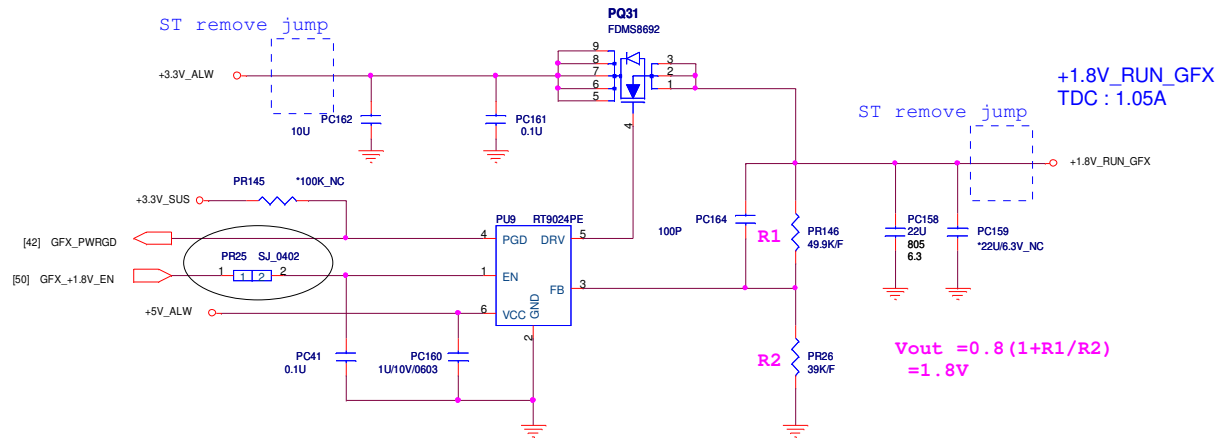
1

2

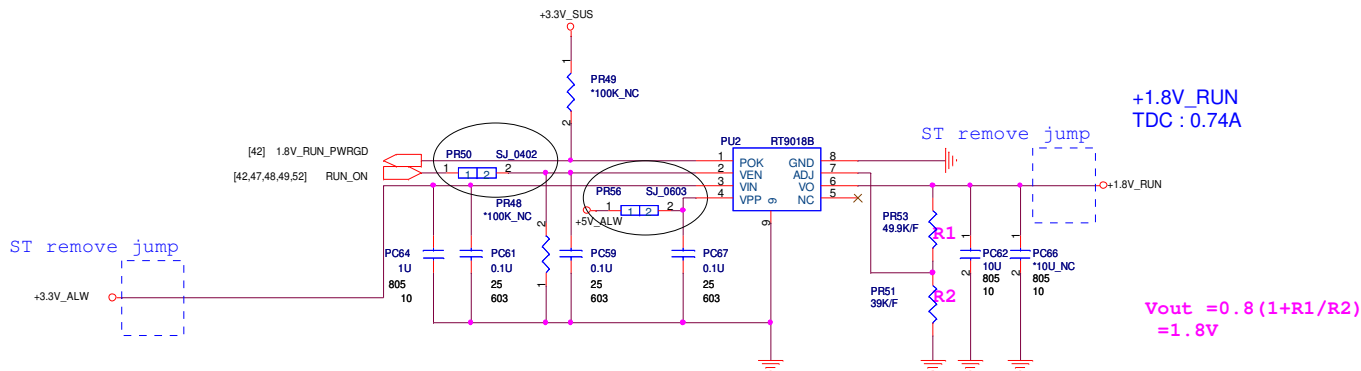
3

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5

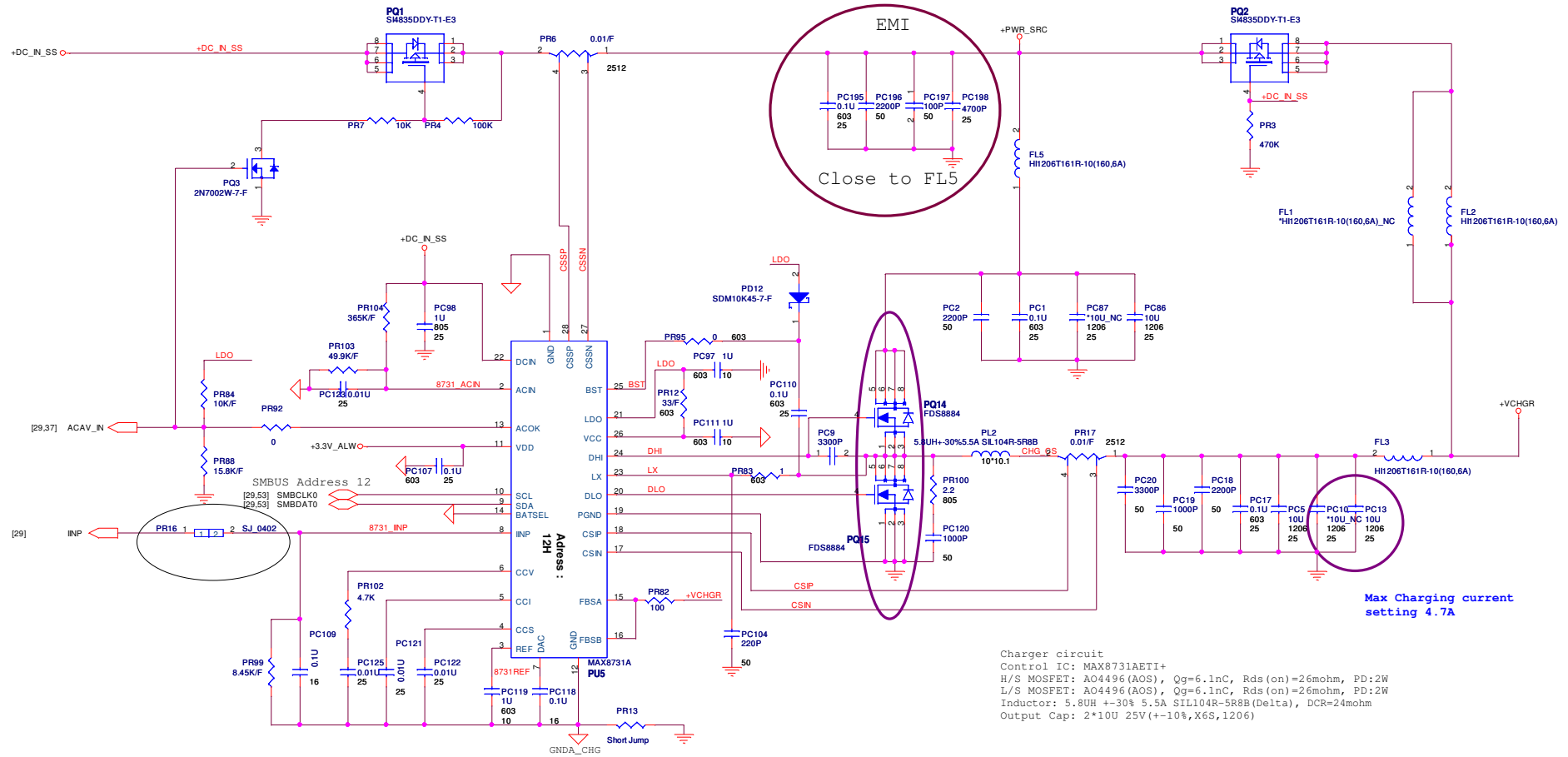


+1.8V\_RUN\_GFX for VGA 1.8V  
 +1.8V\_RUN for CPU and PCH 1.8V



Continuous current : 13A  
Rds (on) : 18mohm

Continuous current : 13A  
Rds (on) : 18mohm



Charger circuit  
Control IC: MAX8731AETI+  
H/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:2W  
L/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:2W  
Inductor: 5.8uH +30% 5.5A SLL104R-5R8B(Delta), DCR=24mohm  
Output Cap: 2\*10u 25V(+10%,X6S,1206)

ST remove jump

ST remove jump

+5V\_SUS  
Fs=400K  
TDC : 5.83A  
Peak current : 8.33A  
OCP:10A

ST remove jump

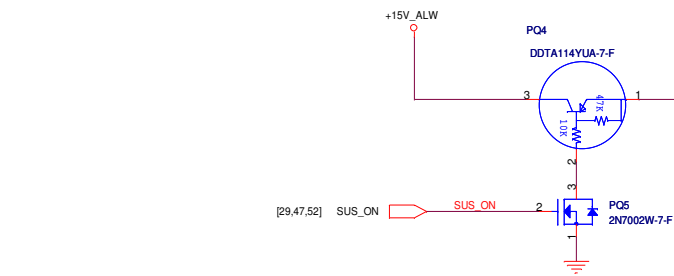
Place these CAPs close to MOSFETs

Place these CAPs close to MOSFETs

+3.3V\_ALW  
Fs=300K  
TDC : 8.23A  
Peak : 11.77A  
OCP:14A

+5V\_ALW  
Control IC: TPS51427A  
H/S MOSFET: FDS8884 (Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W  
L/S MOSFET: FDS6690AS (Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W  
Inductor: 3.3u20x13.5A (EPI0603H-3R3M-K01) (TTA), DCR=25mohm  
Output Cap: 1\*150U 6.3V (20%, ESR25, 3528, H=1.9)

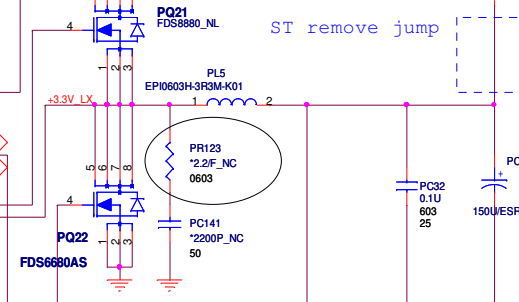
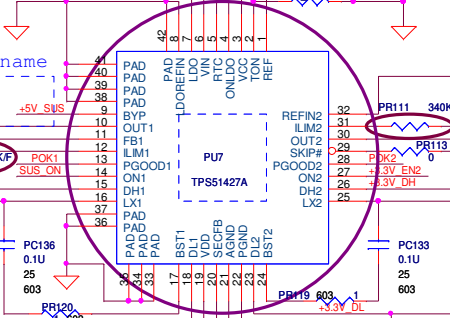
+3.3V\_ALW  
Control IC: TPS51427A  
H/S MOSFET: FDS6298 (Fairchild), Qg=14nC, Rds(on)=12mohm, PD:3W  
L/S MOSFET: FDS6676AS (Fairchild), Qg=35nC, Rds(on)=7.25mohm, PD:2.5W  
Inductor: 3.3u20x13.5A (EPI0603H-3R3M-K01) (TTA), DCR=25mohm  
Output Cap: 1\*150U 6.3V (20%, ESR25, 3528, H=1.9)



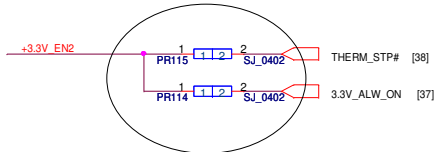
ST change net-name

ST remove jump

ST change net-name



Ton	GND	VREF2 or Float	5V
Channel1 Fs	400 kHz	400 kHz	200 kHz
Channel2 Fs	500 kHz	300 kHz	300 kHz

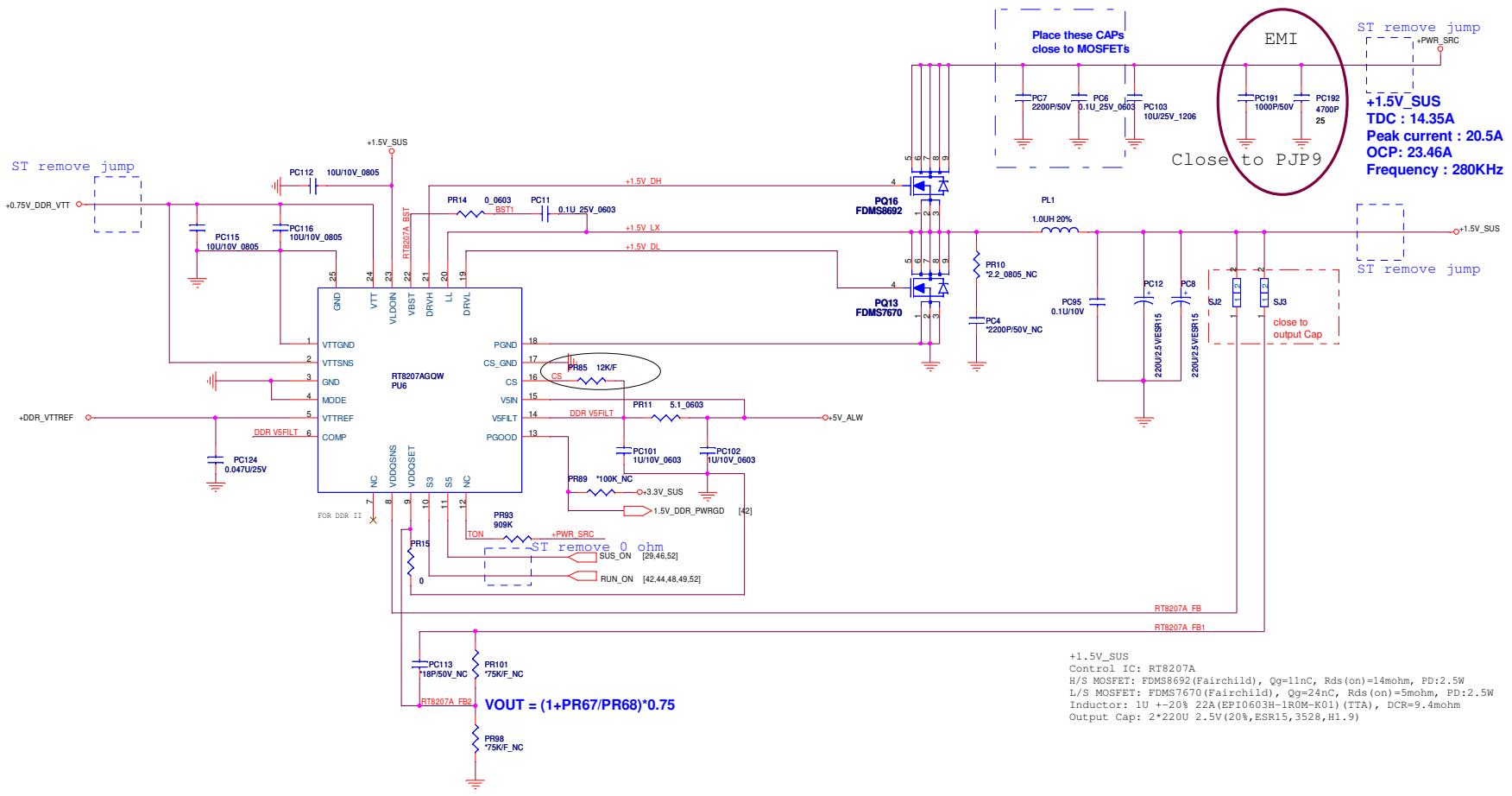


Title: 3.3V\_ALW/5V\_ALW (TPS51427A)

Size: Document Number: UMS

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Rev 1A



**+1.5V\_SUS**  
**TDC : 14.35A**  
**Peak current : 20.5A**  
**OCF: 23.46A**  
**Frequency : 280KHz**

+1.5V\_SUS  
 Control IC: RT8207A  
 H/S MOSFET: FDM58692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W  
 L/S MOSFET: FDM57670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W  
 Inductor: 1U +20% 22A (EPTI0603H-1R0M-K01) (TTA), DCR=9.4mohm  
 Output Cap: 2\*220U 2.5V(20%,ESR15,3528,H1.9)

**VDDQ and VTT discharge control**

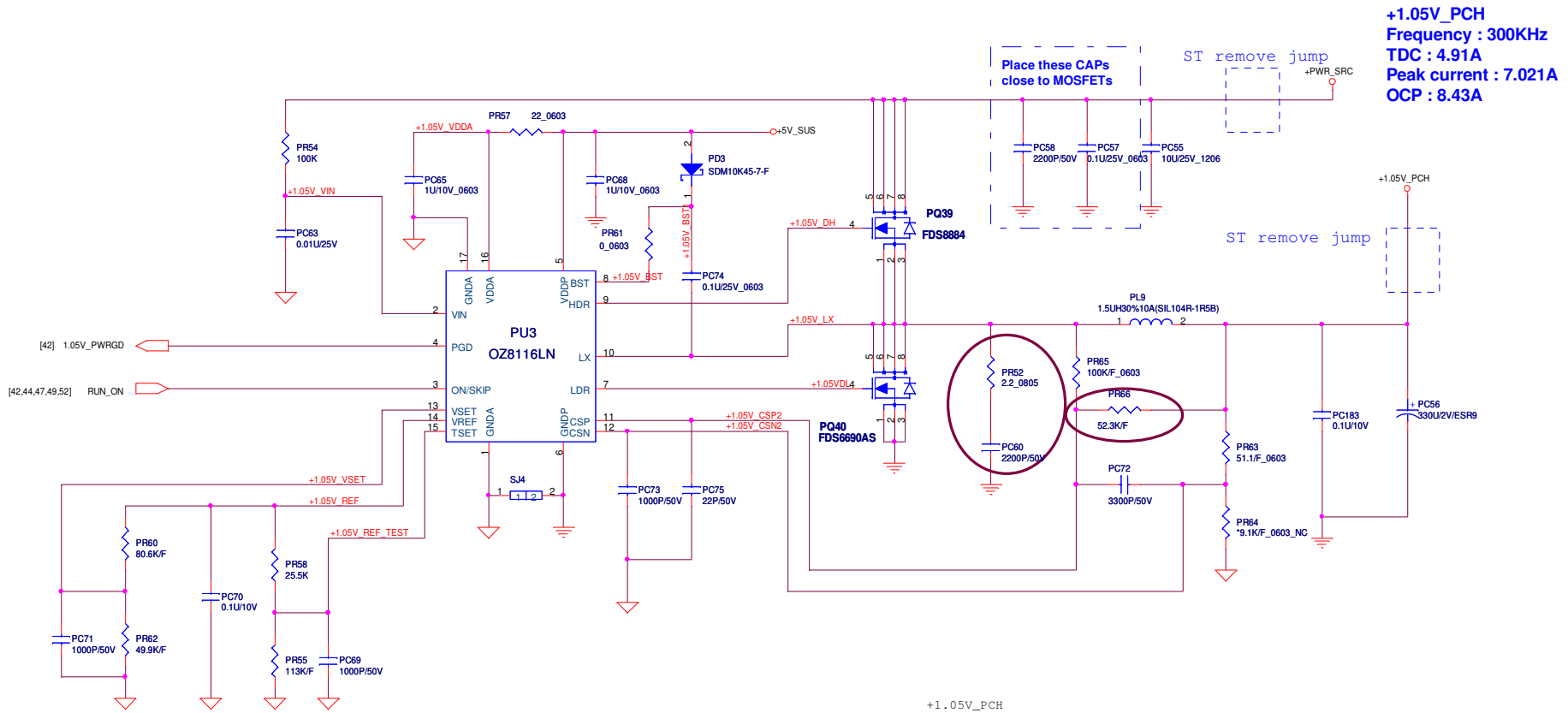
MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

**VDDQ output voltage selection**

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

**Outputs Management by S3, S5 control**

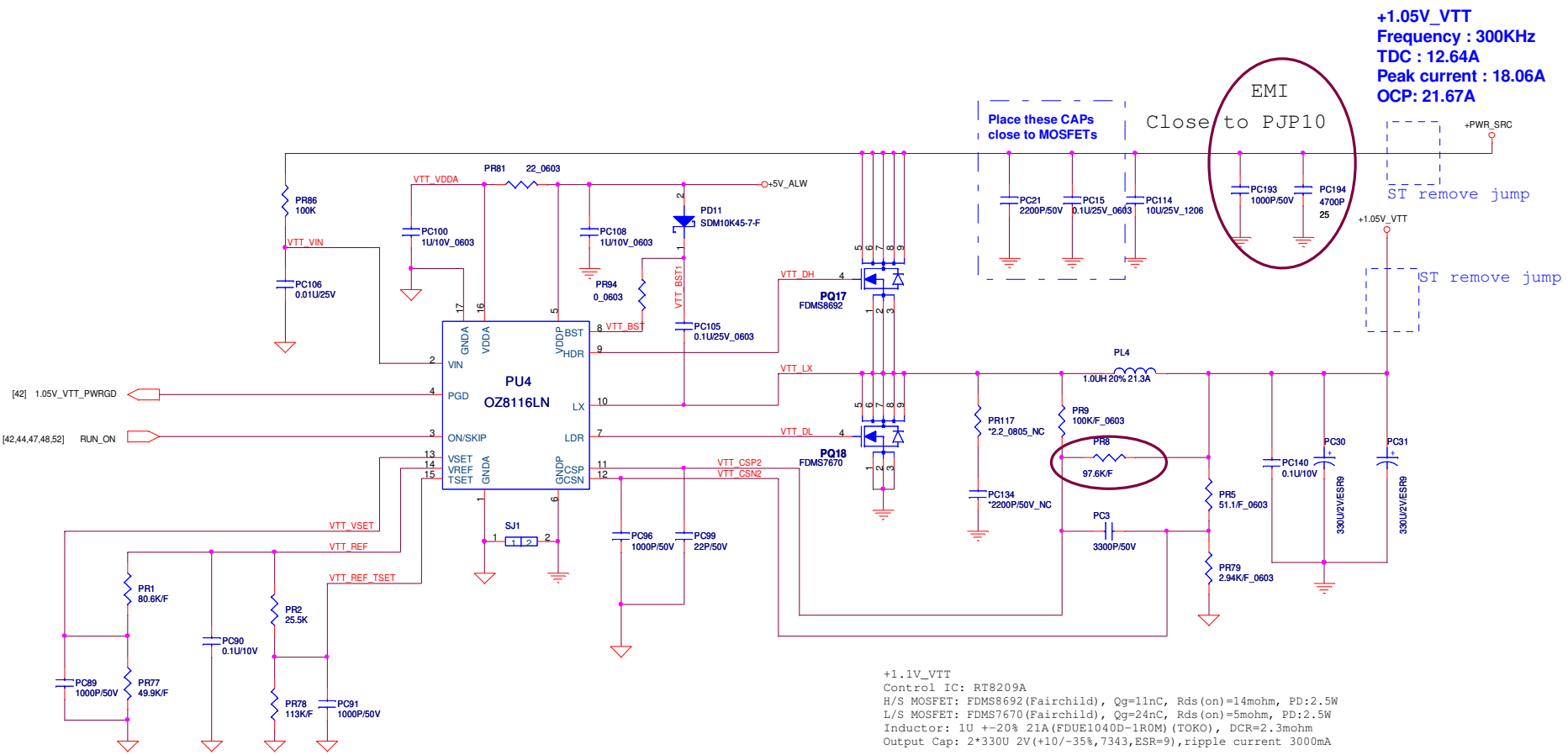
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)



**+1.05V\_PCH**  
**Frequency : 300KHz**  
**TDC : 4.91A**  
**Peak current : 7.021A**  
**OCF : 8.43A**

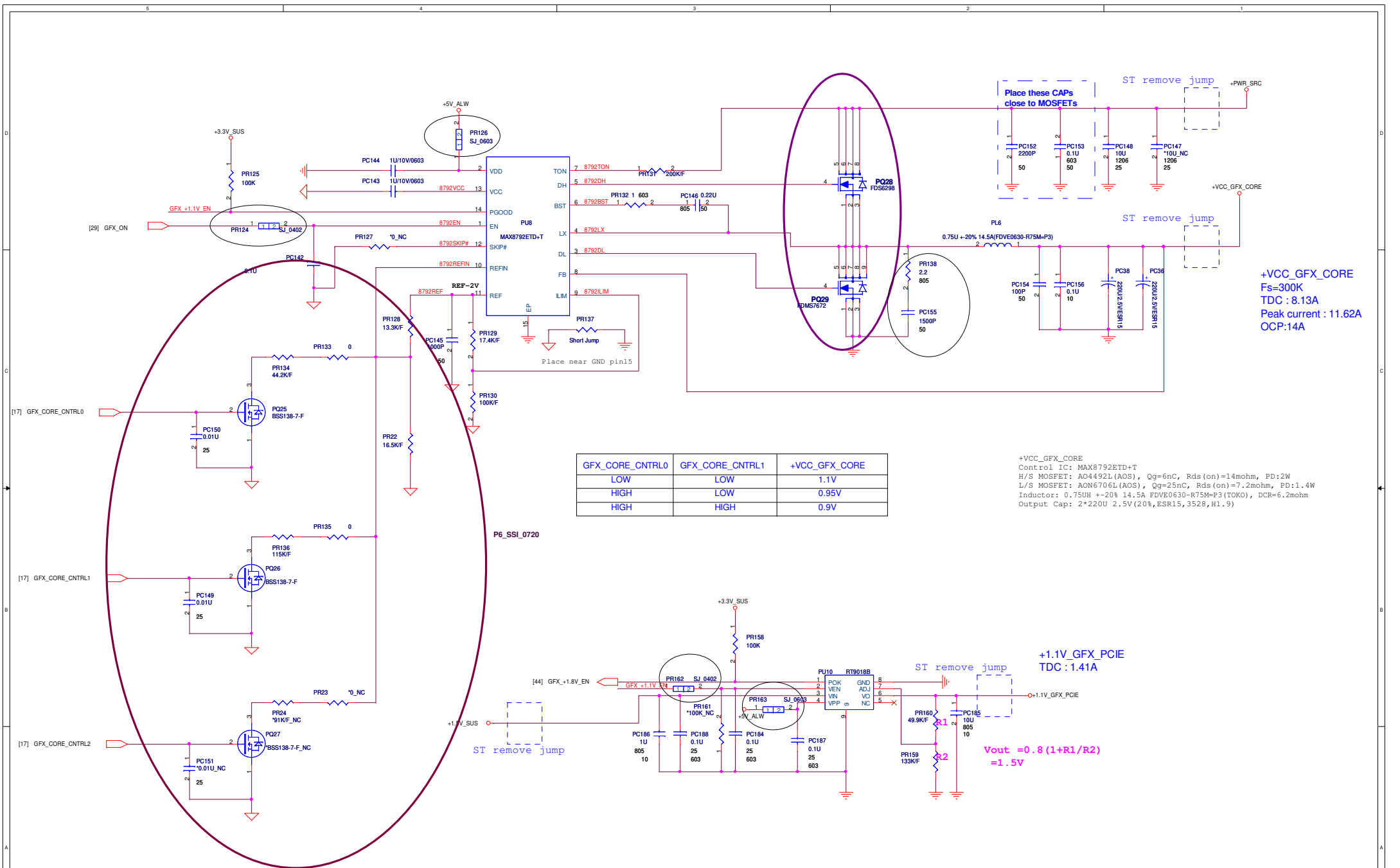
+1.05V\_PCH  
 Control IC: RT8209A  
 H/S MOSFET: FDS8884 (Fairchild), Qg=7nC, Rds(on)=30mohm, PD=2.5W  
 L/S MOSFET: FDS6690AS (Fairchild), Qg=13nC, Rds(on)=15mohm, PD=2.5W  
 Inductor: 1.5UH +-30% 10A SIL104R-1R5B (Delta), DCR=8.1mohm  
 Output Cap: 1\*330U 2V (20%, ESR9, 7343, H1.9)

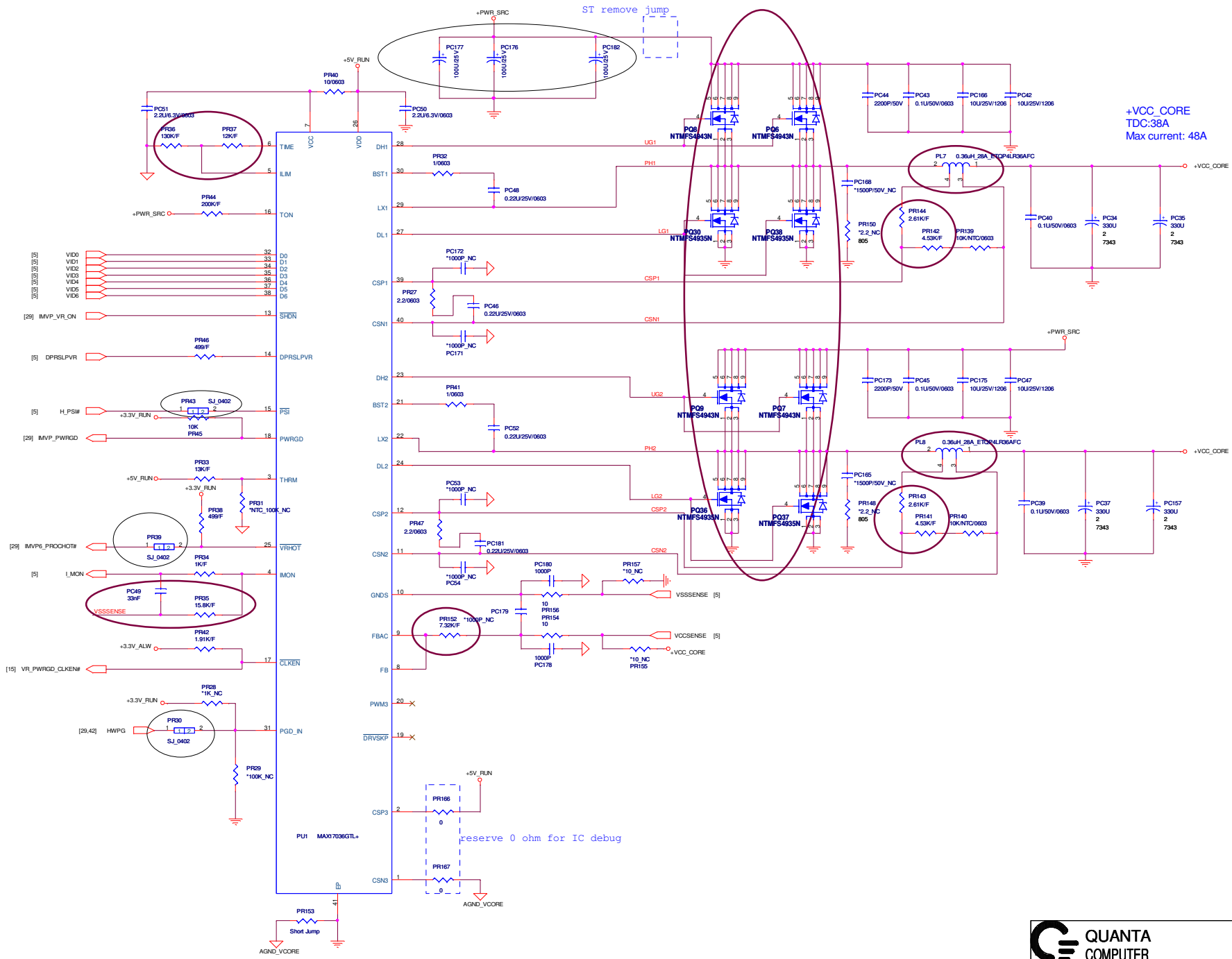


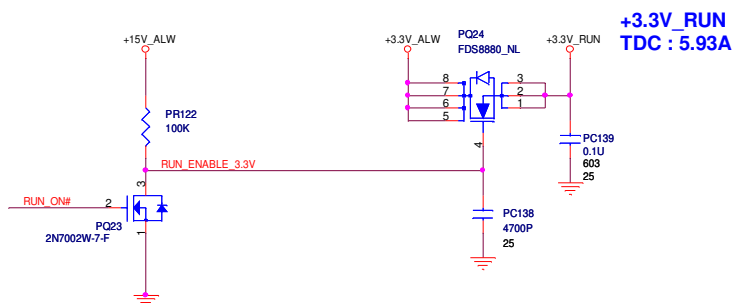
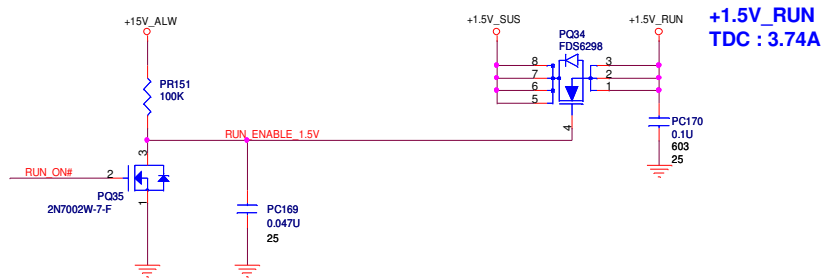
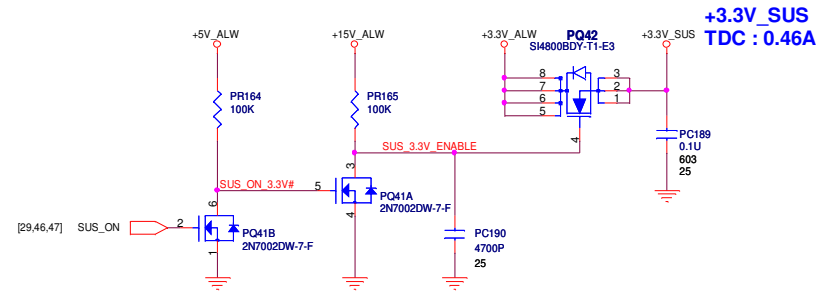
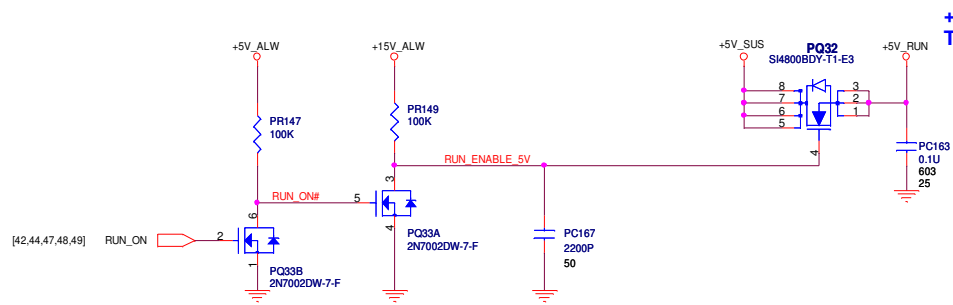


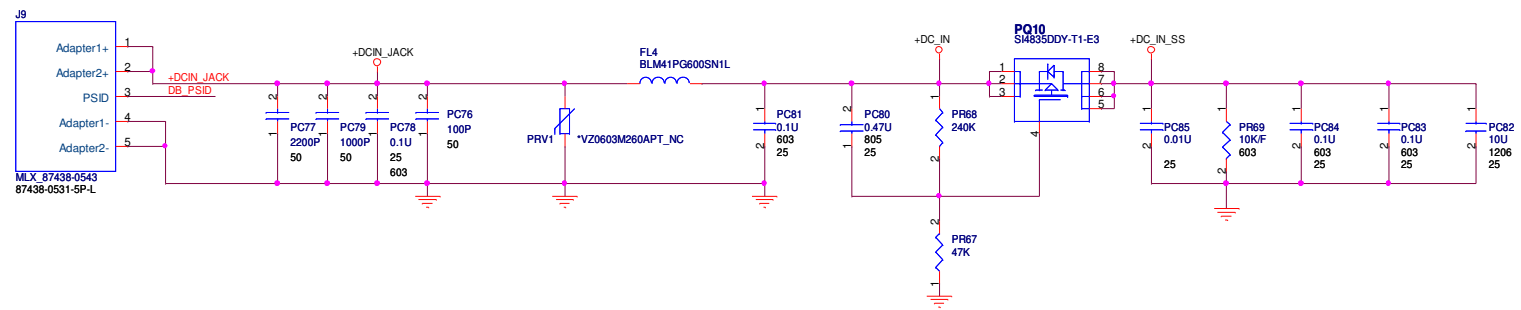
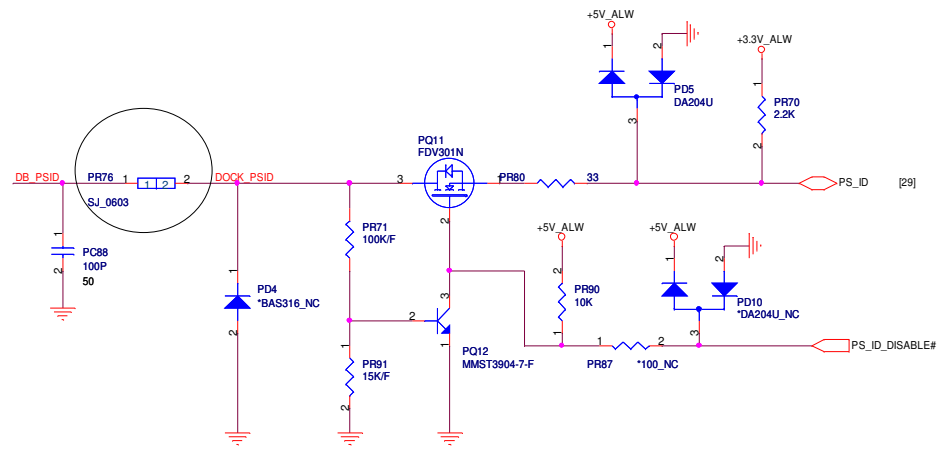
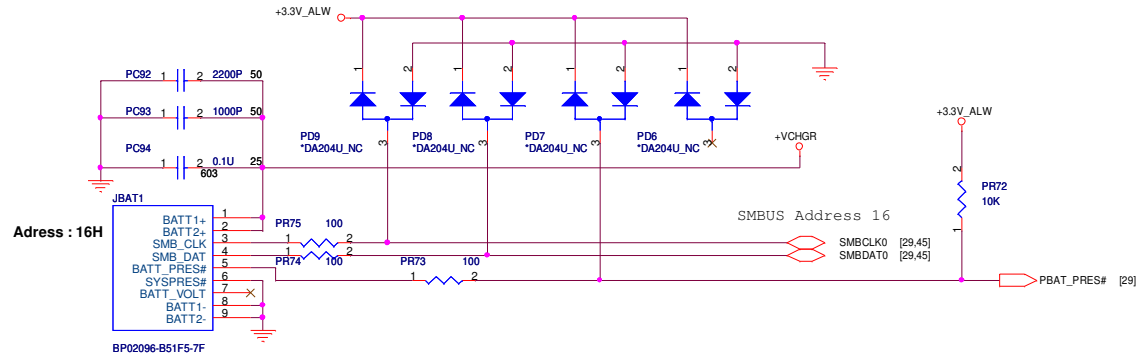
**+1.05V\_VTT**  
**Frequency : 300KHz**  
**TDC : 12.64A**  
**Peak current : 18.06A**  
**OCP: 21.67A**

**+1.1V\_VTT**  
 Control IC: RT8209A  
 H/S MOSFET: FDMS8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W  
 L/S MOSFET: FDMS7670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W  
 Inductor: 1U +-20% 21A (FDUE1040D-1R0M) (TOKO), DCR=2.3mohm  
 Output Cap: 2\*330U 2V(+10/-35%, 7343, ESR=9), ripple current 3000mA







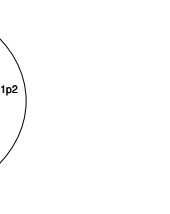
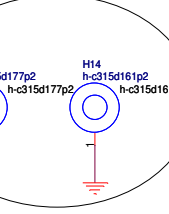
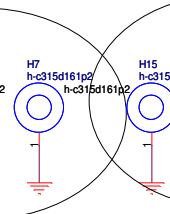
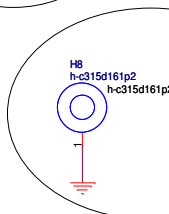
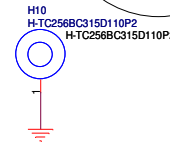
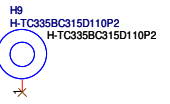
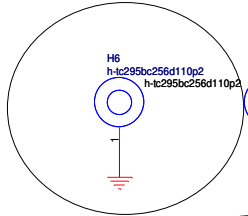
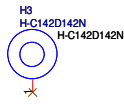
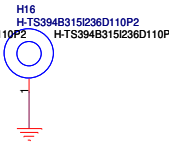
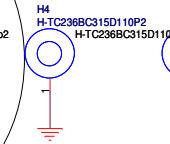
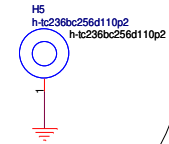
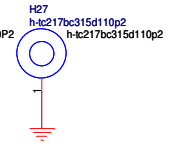
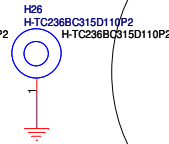
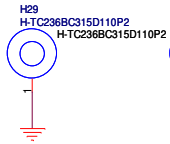
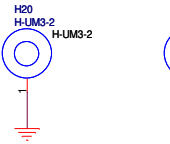
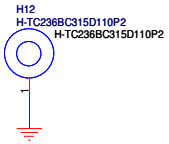
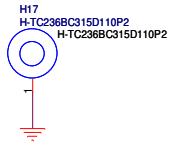
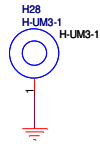
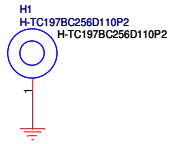


**QUANTA COMPUTER**

File: DCINBATT CONNECTOR

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**WWAN**

H21  
H-TC118BC197D61P2  
H-TC118BC197D61P2

BOT  
QPN: FBFM8001010

**WLAN**

H19  
H-TC118BC197D61P2\_NC  
H-TC118BC197D61P2

H11  
h-c175d175n  
h-c175d175n

**GPU**

H18  
h-c295d161p2  
h-c295d161p2

H13  
h-c295d161p2  
h-c295d161p2

H25  
H-O142X236D142X236N  
H-O142X236D142X236N

**BT**

TOP  
QPN: FBCW4003010

H23  
H-TC217BC197D118P2  
H-TC217BC197D118P2

H24  
H-TC217BC315D110P2  
H-TC217BC315D110P2

H22  
h-tc256bc315d110p2  
h-tc256bc315d110p2

H30  
O-UM3B-1  
O-UM3B-1


**QUANTA COMPUTER**

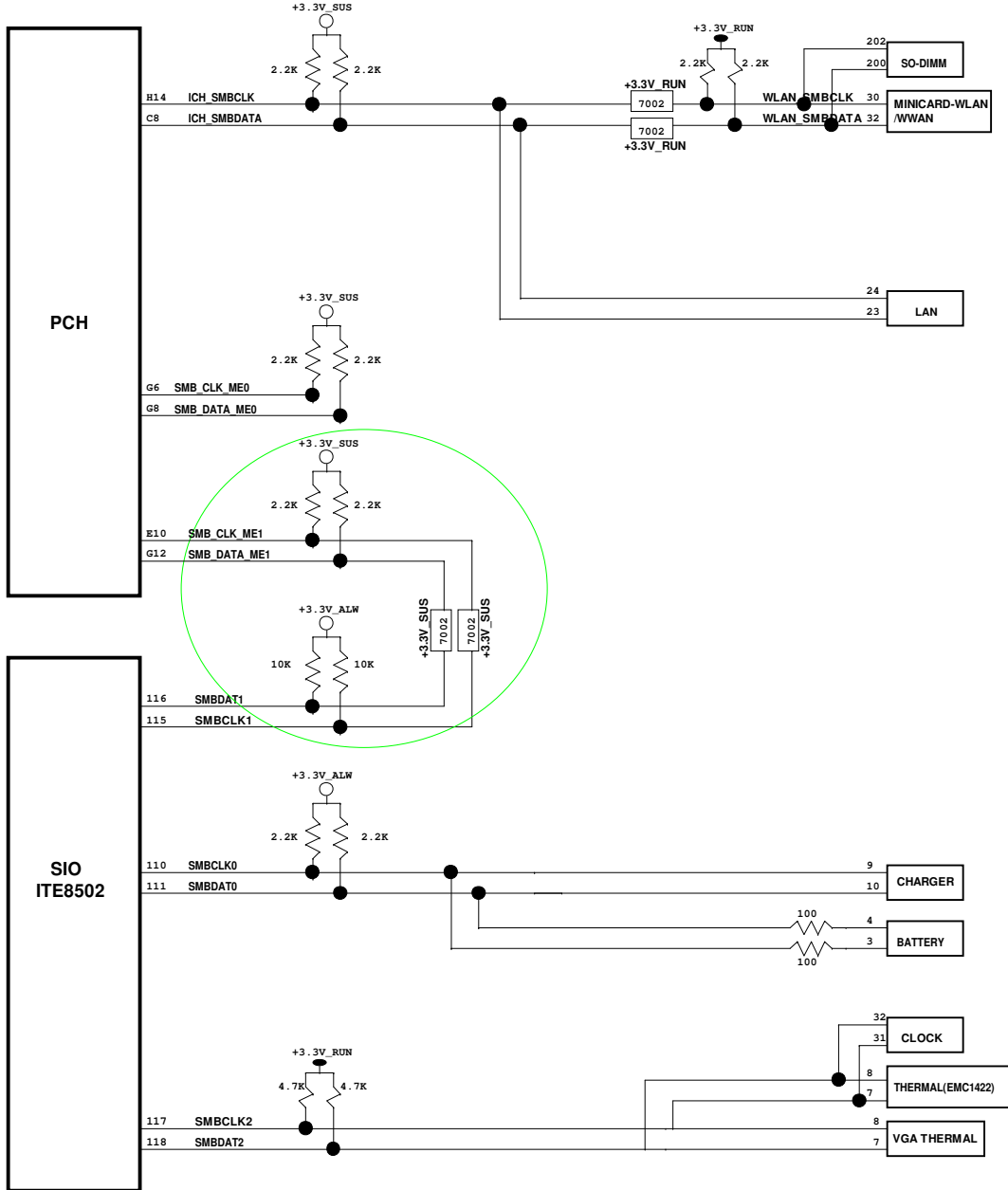
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Size	Document Number	Rev
	UM3	1A

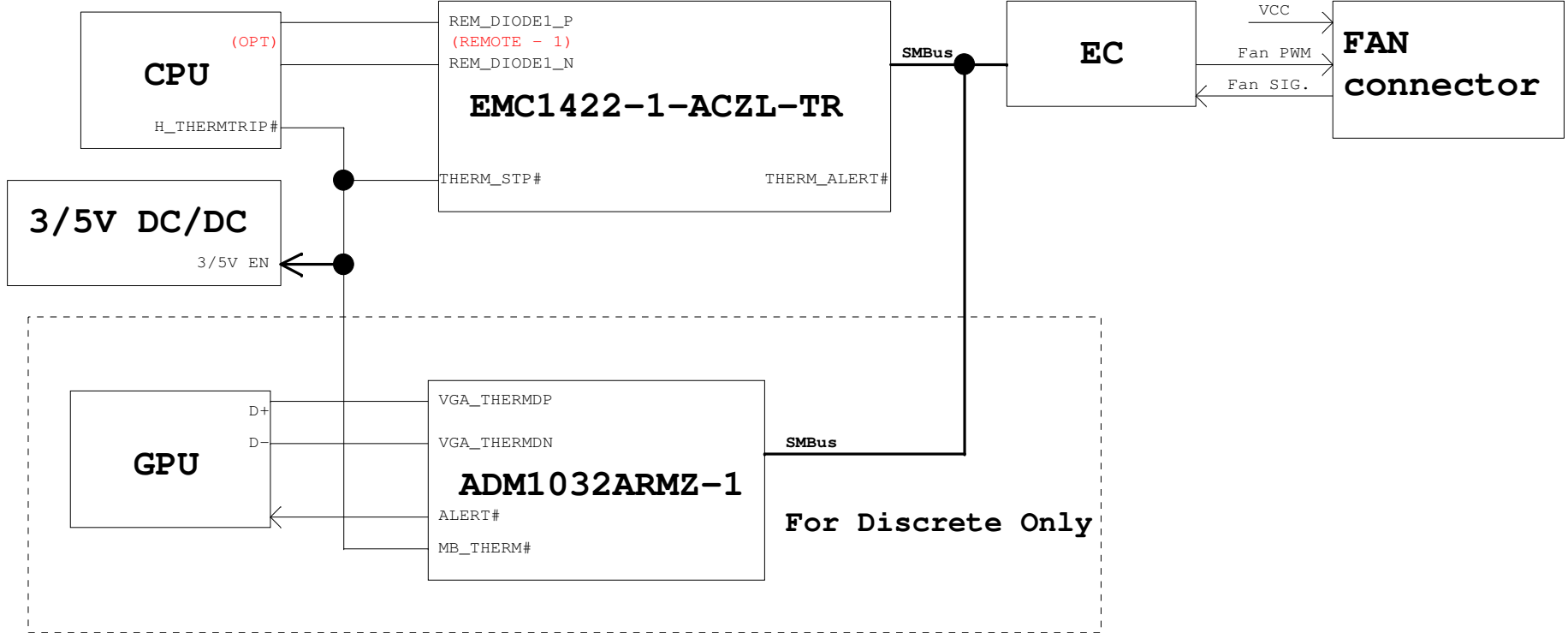
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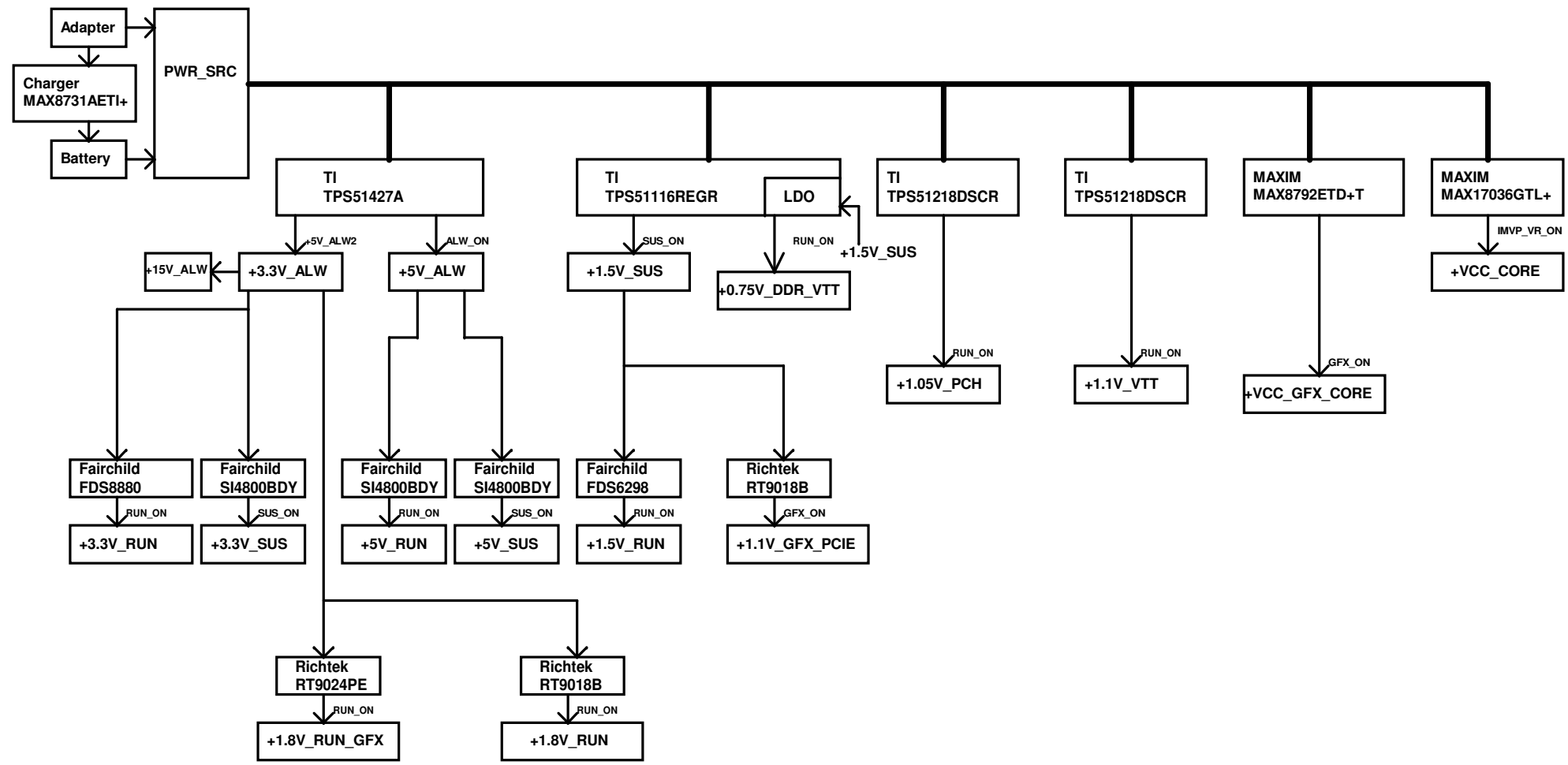
Reserved for EMI.

 <b>QUANTA COMPUTER</b>		
Title: EMI CAP		
Size: UMS	Document Number:	Rev: 1A
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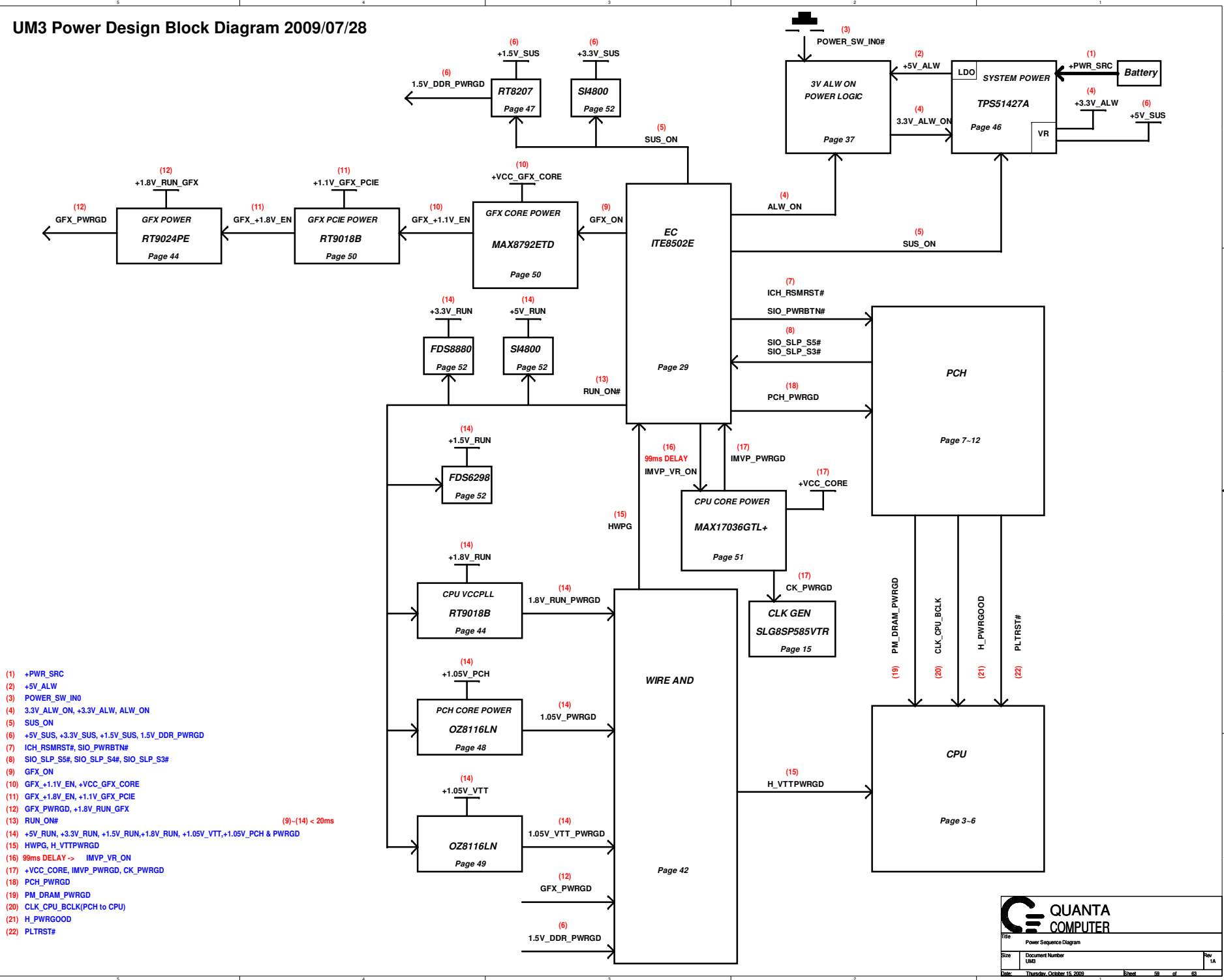








# UM3 Power Design Block Diagram 2009/07/28



- (1) +PWR\_SRC
- (2) +5V\_ALW
- (3) POWER\_SW\_IN#
- (4) 3.3V\_ALW\_ON, +3.3V\_ALW, ALW\_ON
- (5) SUS\_ON
- (6) +5V\_SUS, +3.3V\_SUS, +1.5V\_SUS, 1.5V\_DDR\_PWRGD
- (7) ICH\_RSMRST#, SIO\_PWRBTN#
- (8) SIO\_SLP\_S5#, SIO\_SLP\_S4#, SIO\_SLP\_S3#
- (9) GFX\_ON
- (10) GFX\_+1.1V\_EN, +VCC\_GFX\_CORE
- (11) GFX\_+1.8V\_EN, +1.1V\_GFX\_PCIE
- (12) GFX\_PWRGD, +1.8V\_RUN\_GFX
- (13) RUN\_ON#
- (14) +5V\_RUN, +3.3V\_RUN, +1.5V\_RUN, +1.8V\_RUN, +1.05V\_VTT, +1.05V\_PCH & PWRGD
- (15) HWPG, H\_VTTPWRGD
- (16) 99ms DELAY -> IMVP\_VR\_ON
- (17) +VCC\_CORE, IMVP\_PWRGD, CK\_PWRGD
- (18) PCH\_PWRGD
- (19) PM\_DRAM\_PWRGD
- (20) CLK\_CPU\_BCLK(PCH to CPU)
- (21) H\_PWRGOOD
- (22) PLTRST#

**QUANTA  
COMPUTER**

Title: Power Sequence Diagram

Size: Document Number: UM3 Row: 1A

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1

2

3

4

5

A

A

B

B

C

C

D

D



QUANTA  
COMPUTER

Title		XDP	
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1

2

3

4

5