Wistron CONFIDENTIAL

MODEL NAME : ***Diaz UMA***

Project Code: ***91.4AR01.001***

PCB NO : ***08217-1***

Diaz Intergrate Intel GM Schematics Document

uFCPGA Mobile Merom

Intel Crestline-GM + ICH8M

REV : A00

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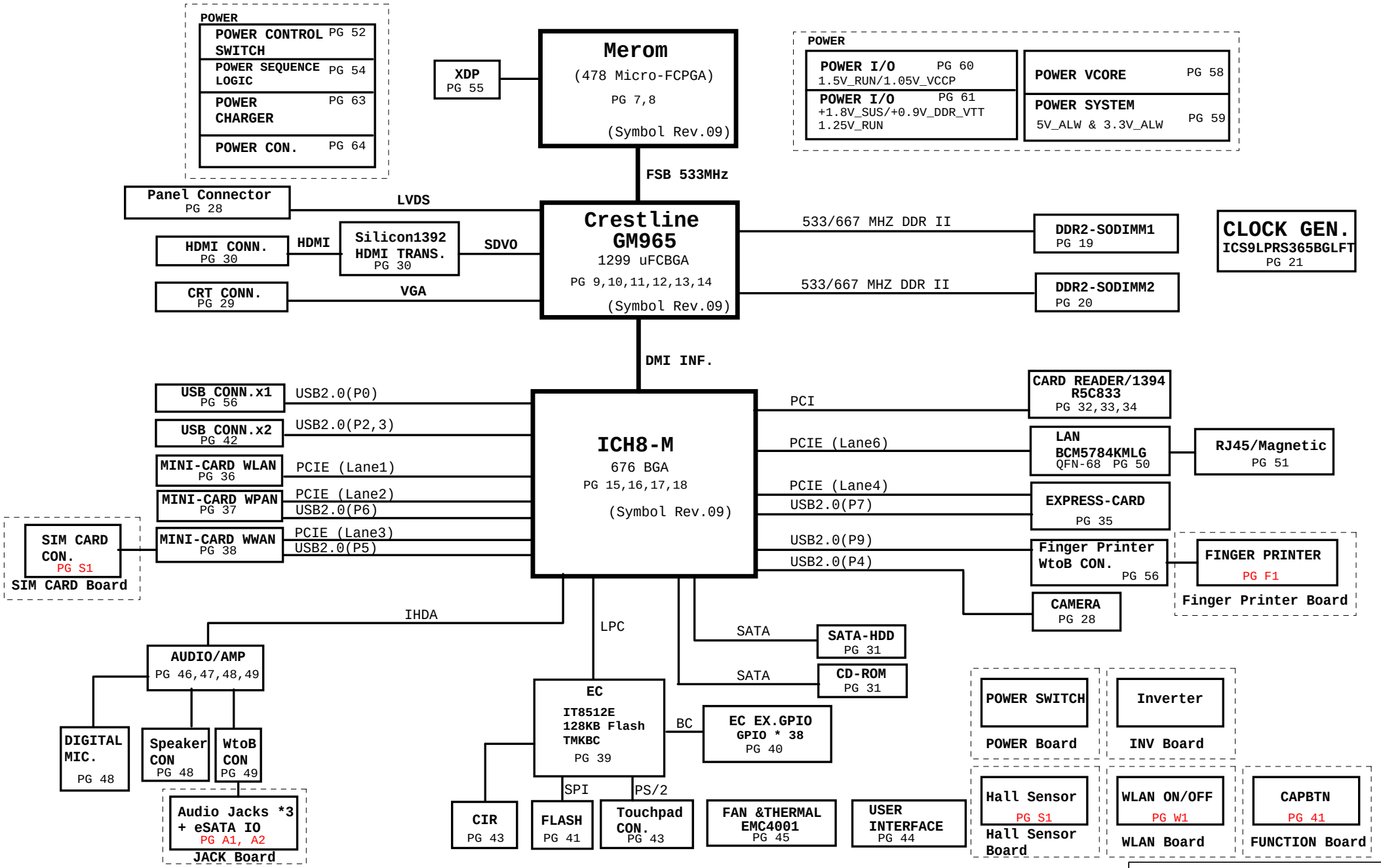
Diaz Block Diagram of Intel GM



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Title	BLOCK DIAGRAM	
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Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

PCI Express TABLE

Lane 1	WLAN / Mini Card
Lane 2	WPAN / Mini Card
Lane 3	WWAN / Mini Card
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5784KMLG

USB TABLE

ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	
ICH8-2 (EHCI#1)	User2 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User3 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	Camera
ICH8-5 (EHCI#1)	WWAN / Mini Card
ICH8-6 (EHCI#2)	WPAN / Mini Card
ICH8-7 (EHCI#2)	ExpressCard
ICH8-8 (EHCI#2)	Note : No USB for WLAN
ICH8-9 (EHCI#2)	Finger Printer

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Title: Bus Connection

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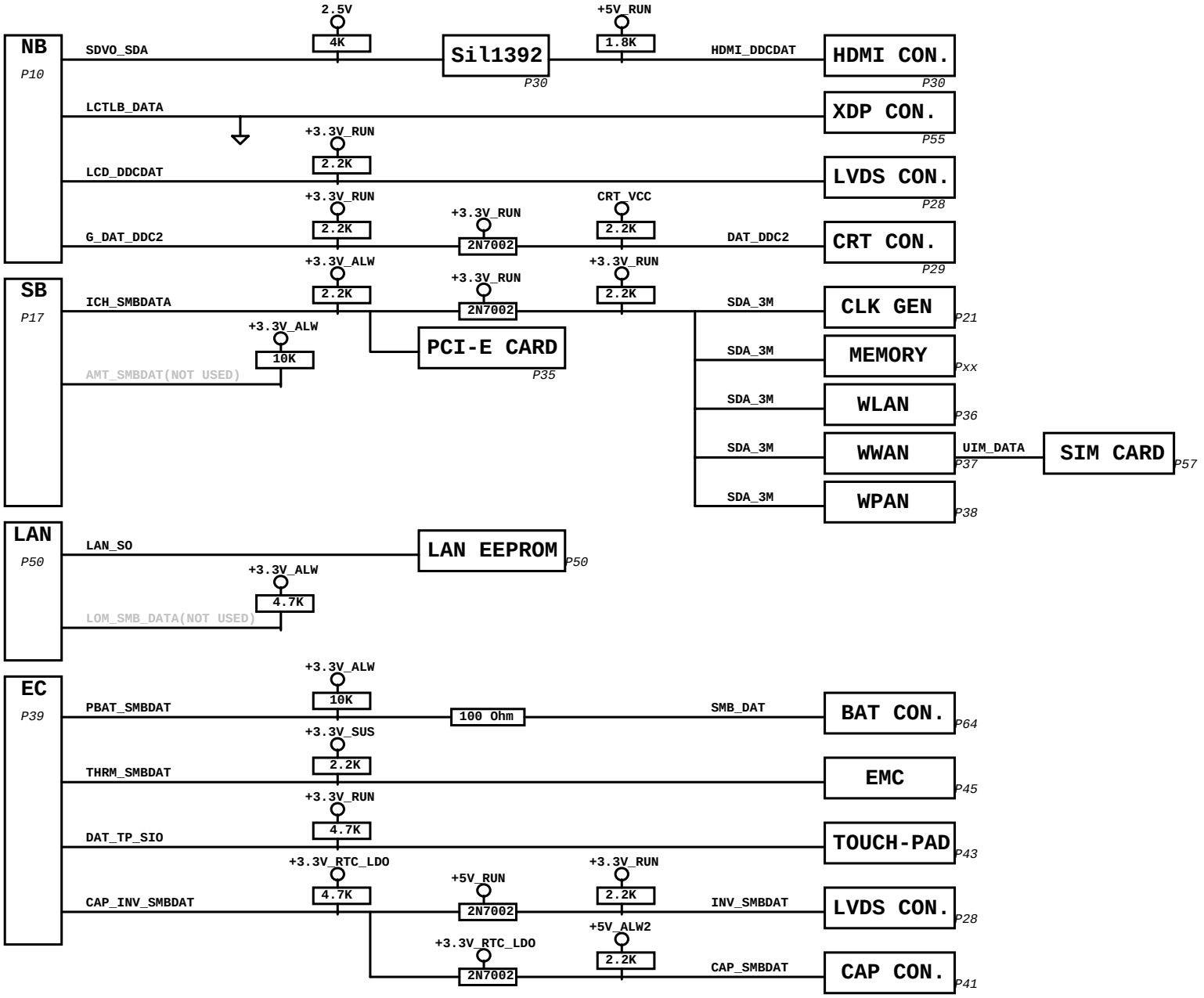

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Title: SM BUS

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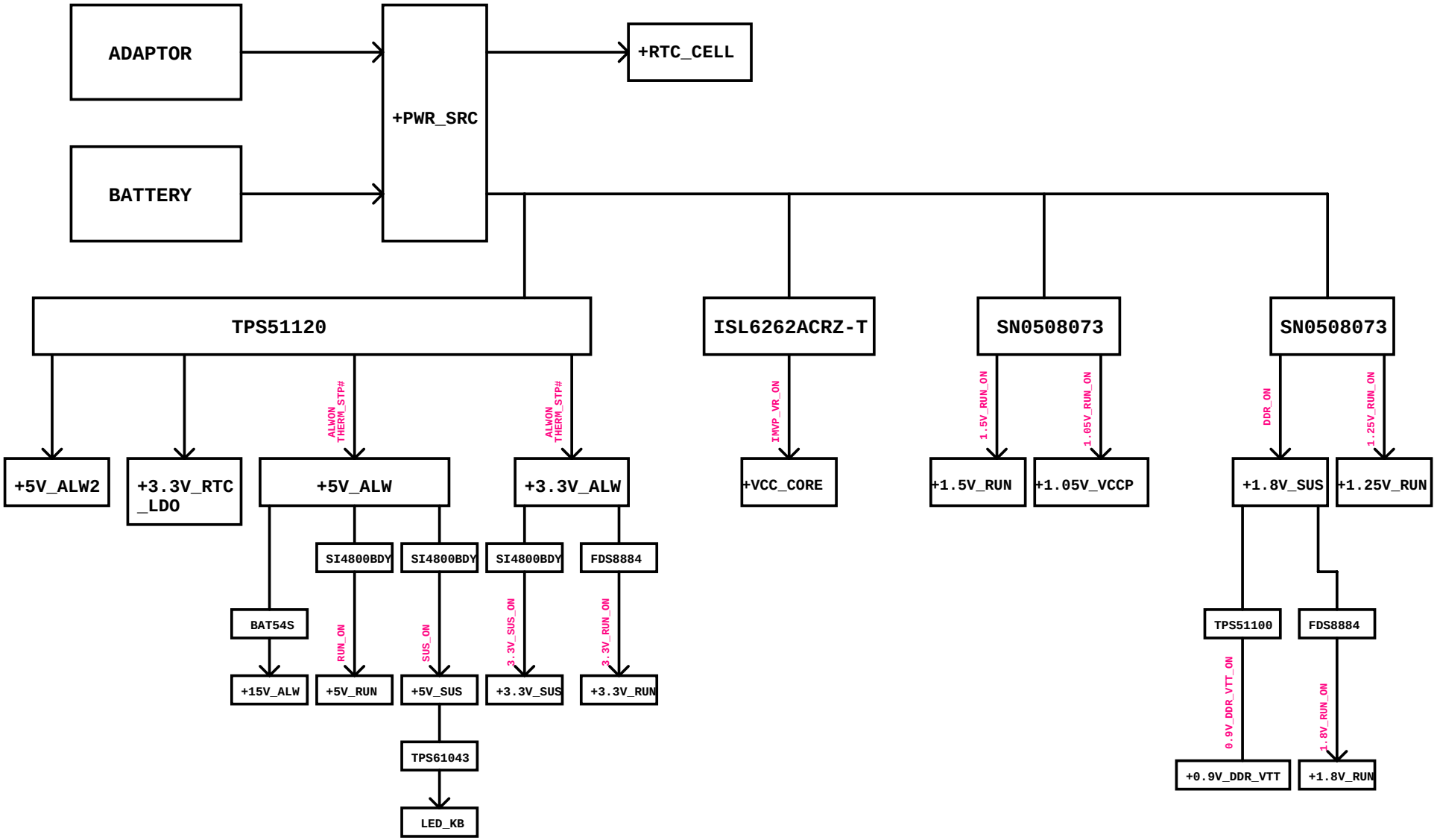

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Title: Intel UMA POWER RAIL

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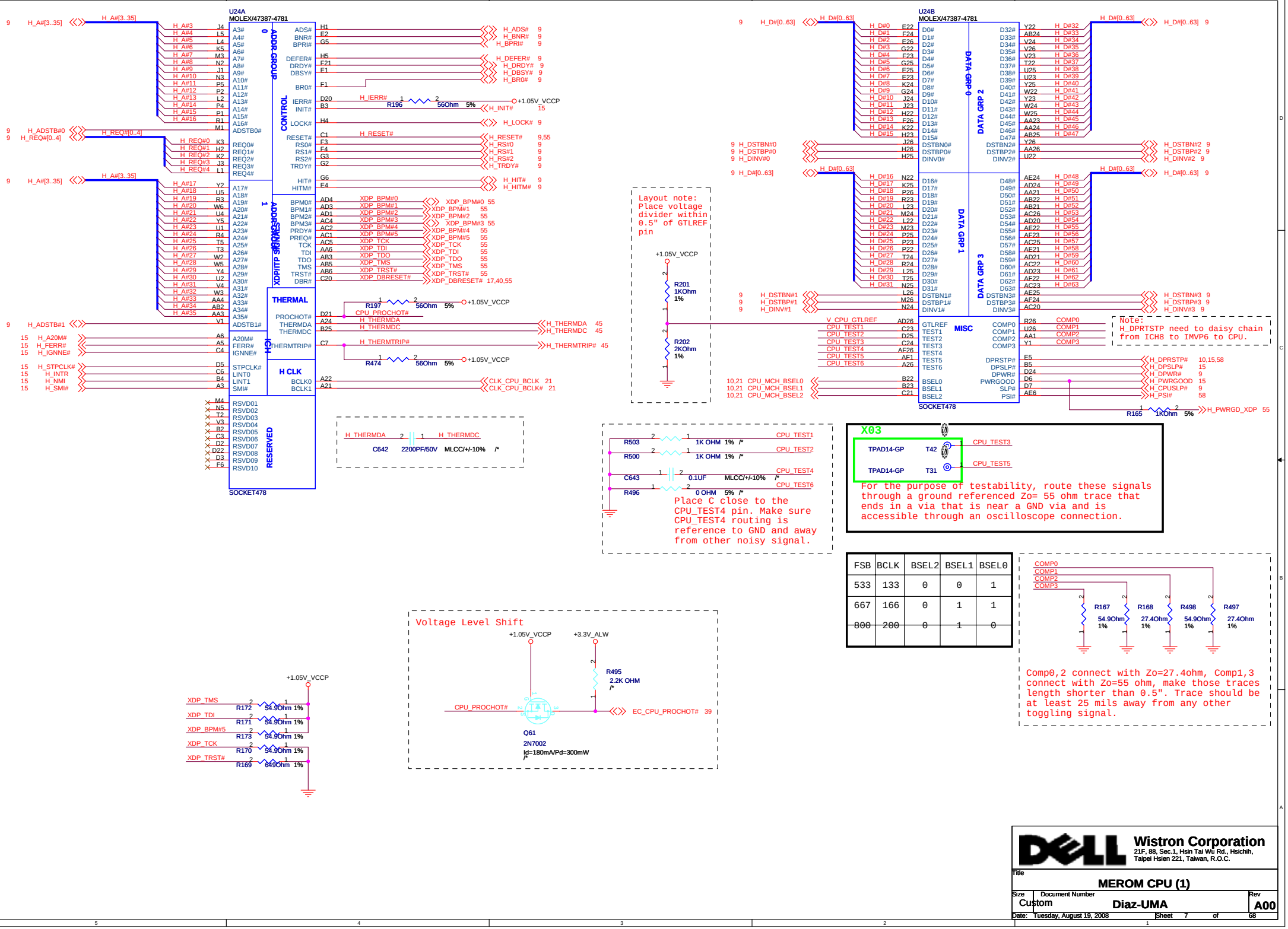

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

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Title: MEROM CPU (1)

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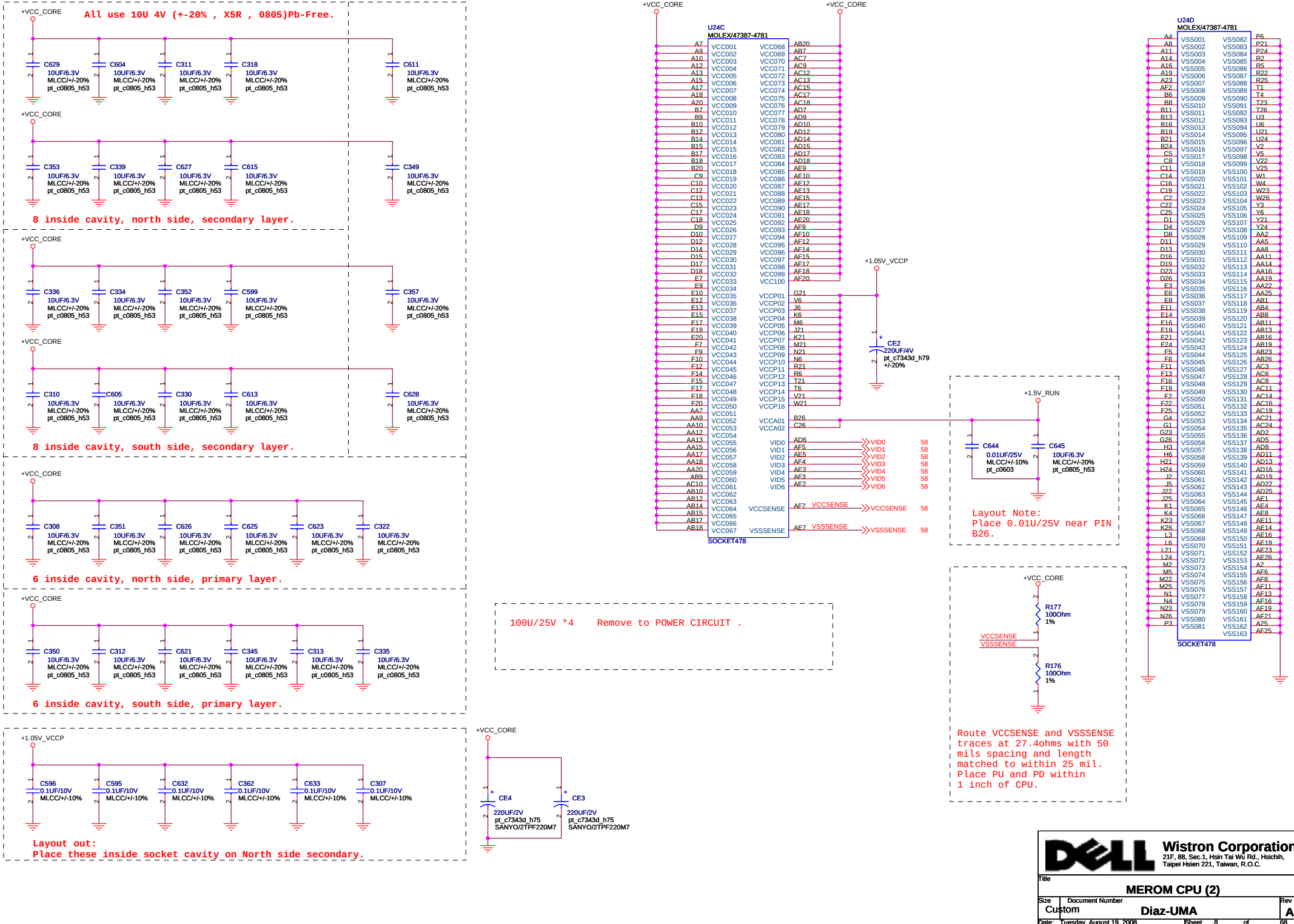

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Title: MEROM CPU (2)

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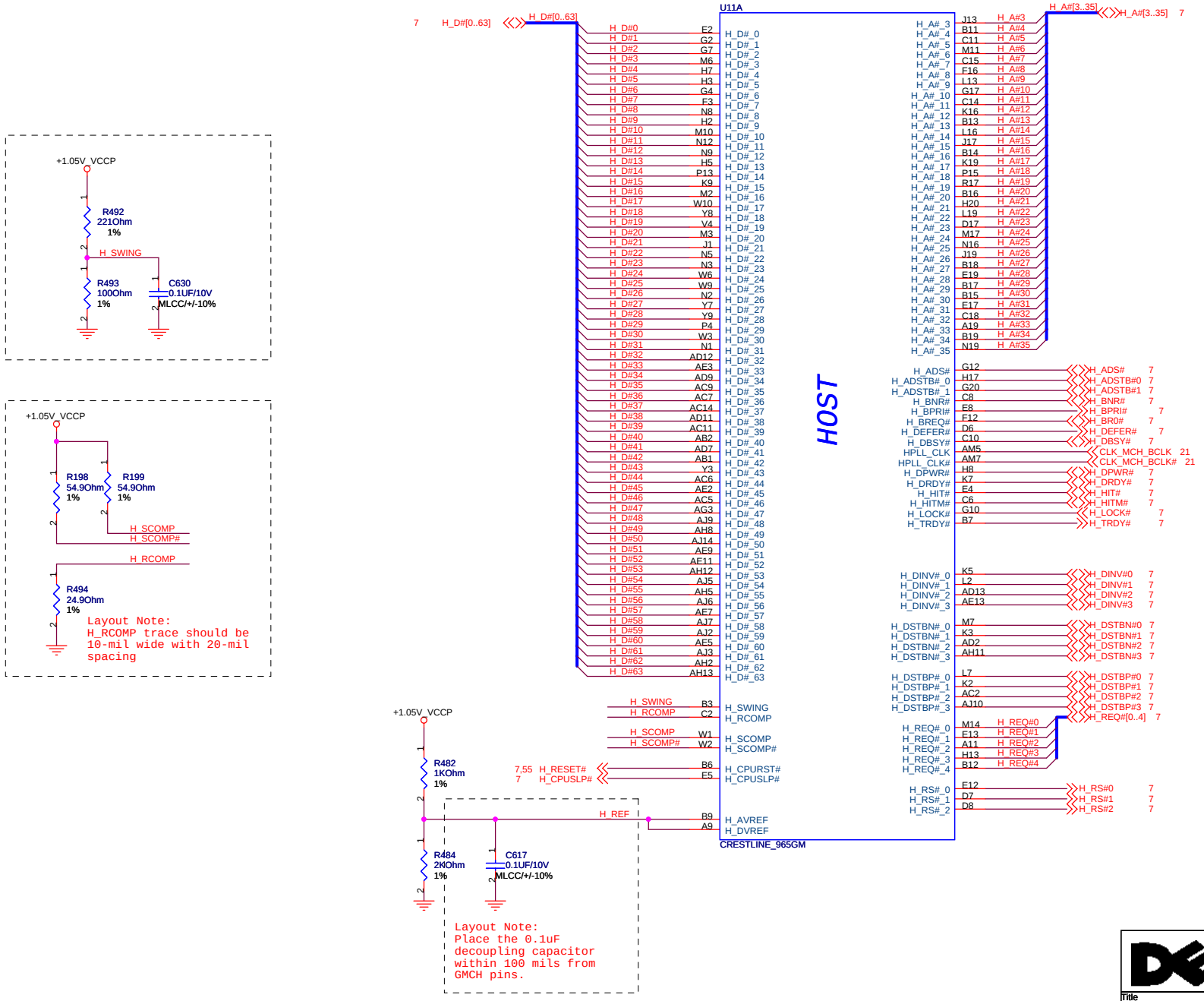

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Title: Crestline(HOST)					
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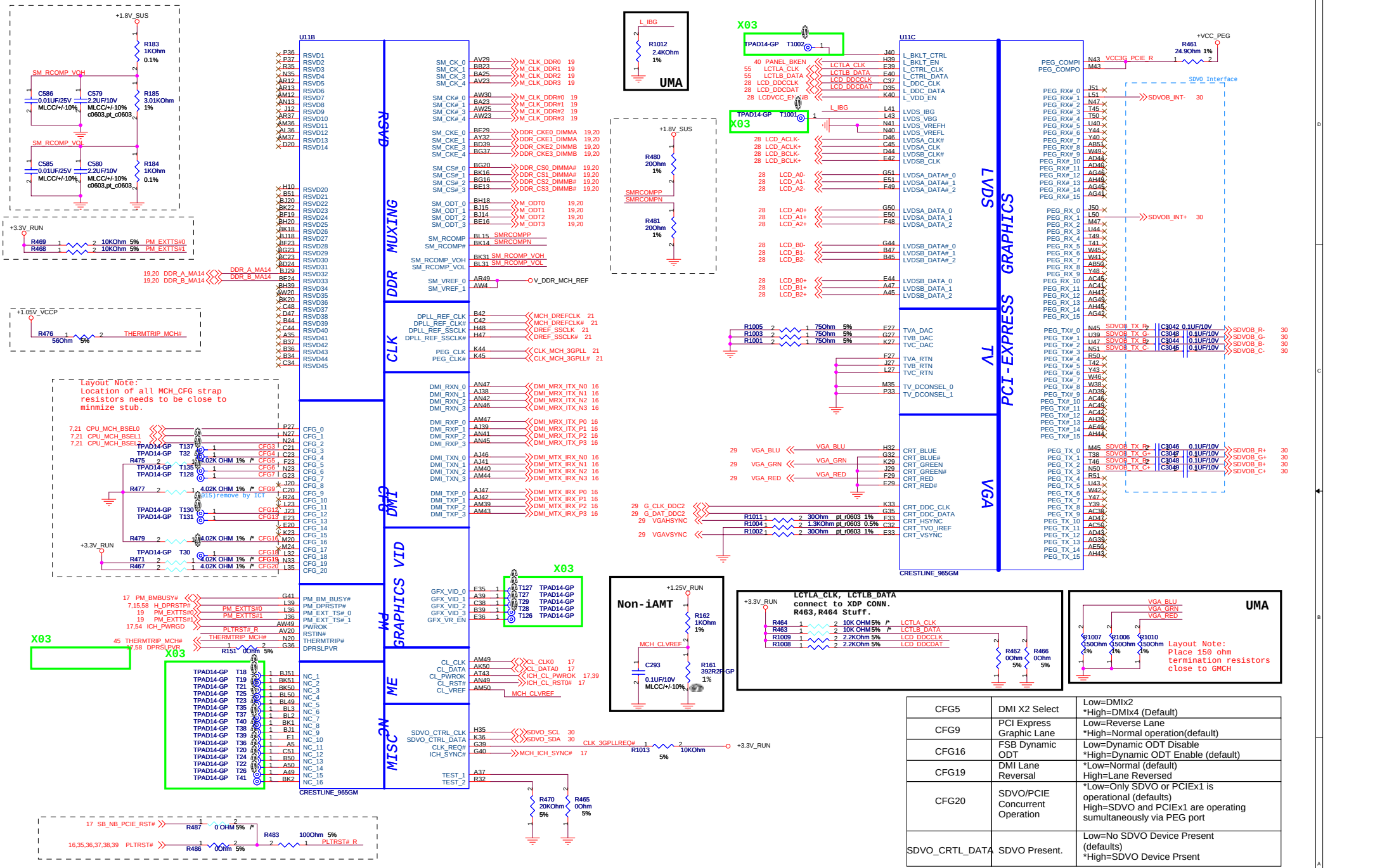
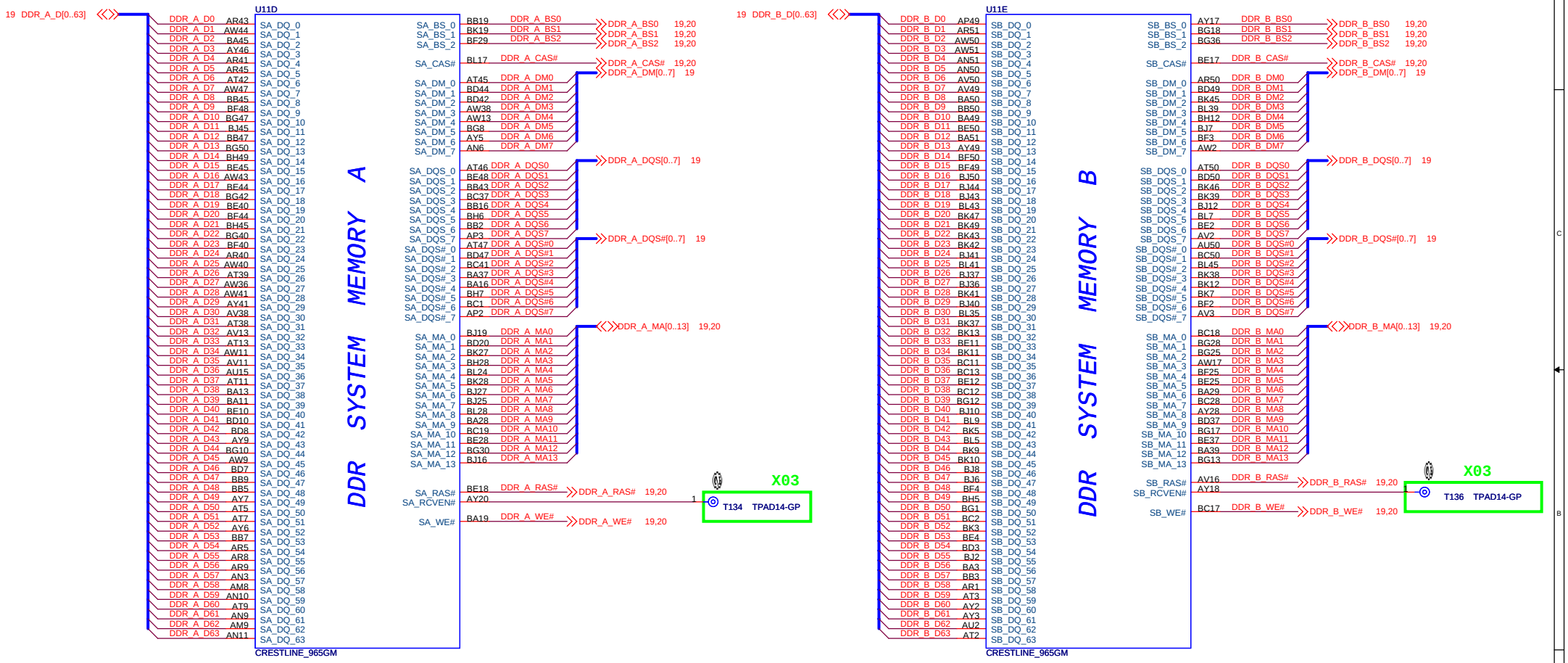


CFG5	DMI X2 Select	Low=DMIx2 *High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane *High=Normal operation(default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable *High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	*Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	*Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) *High=SDVO Device Prsent



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Title	Crestline(DDR2)	
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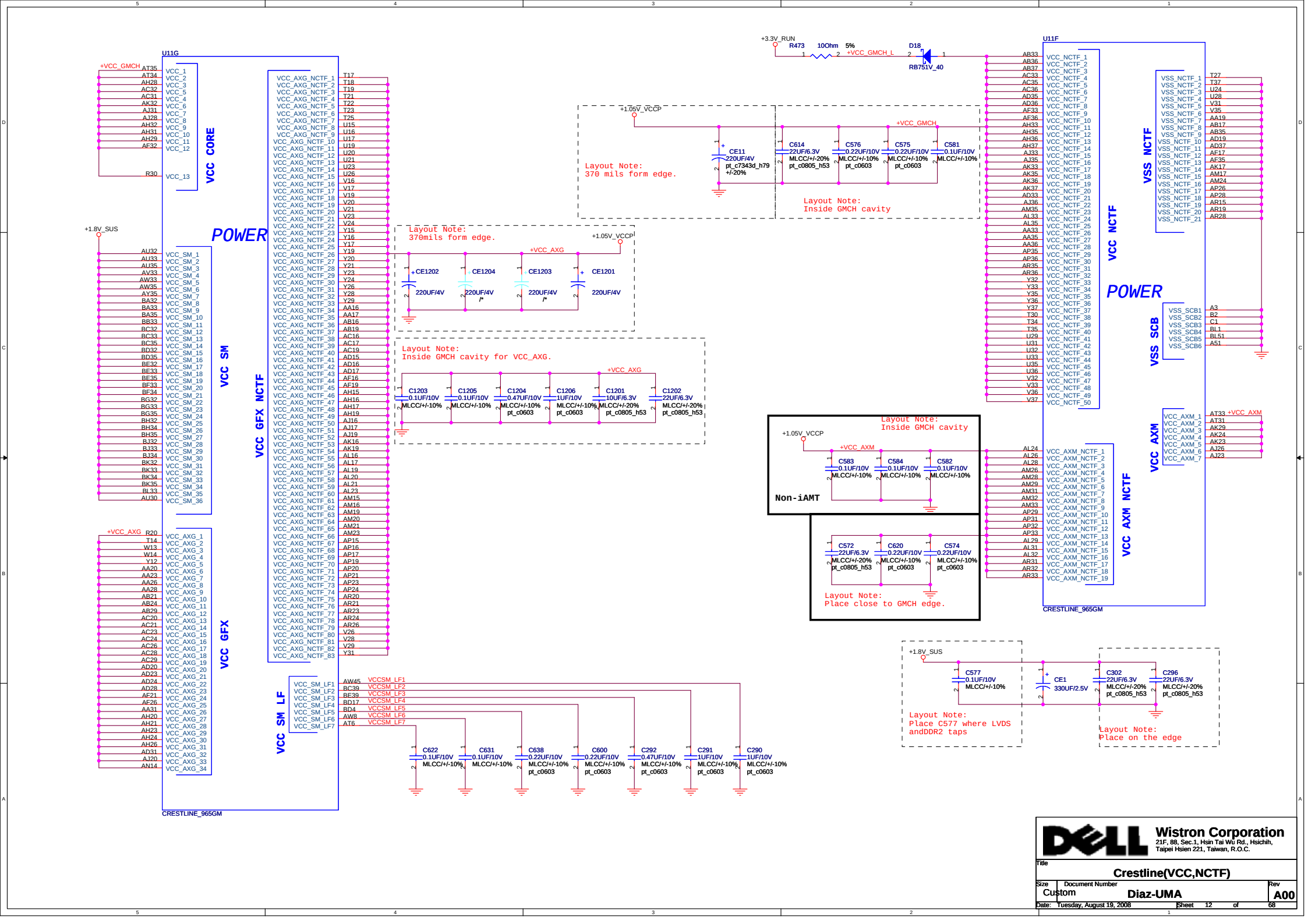

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Title	Crestline(VCC,NCTF)
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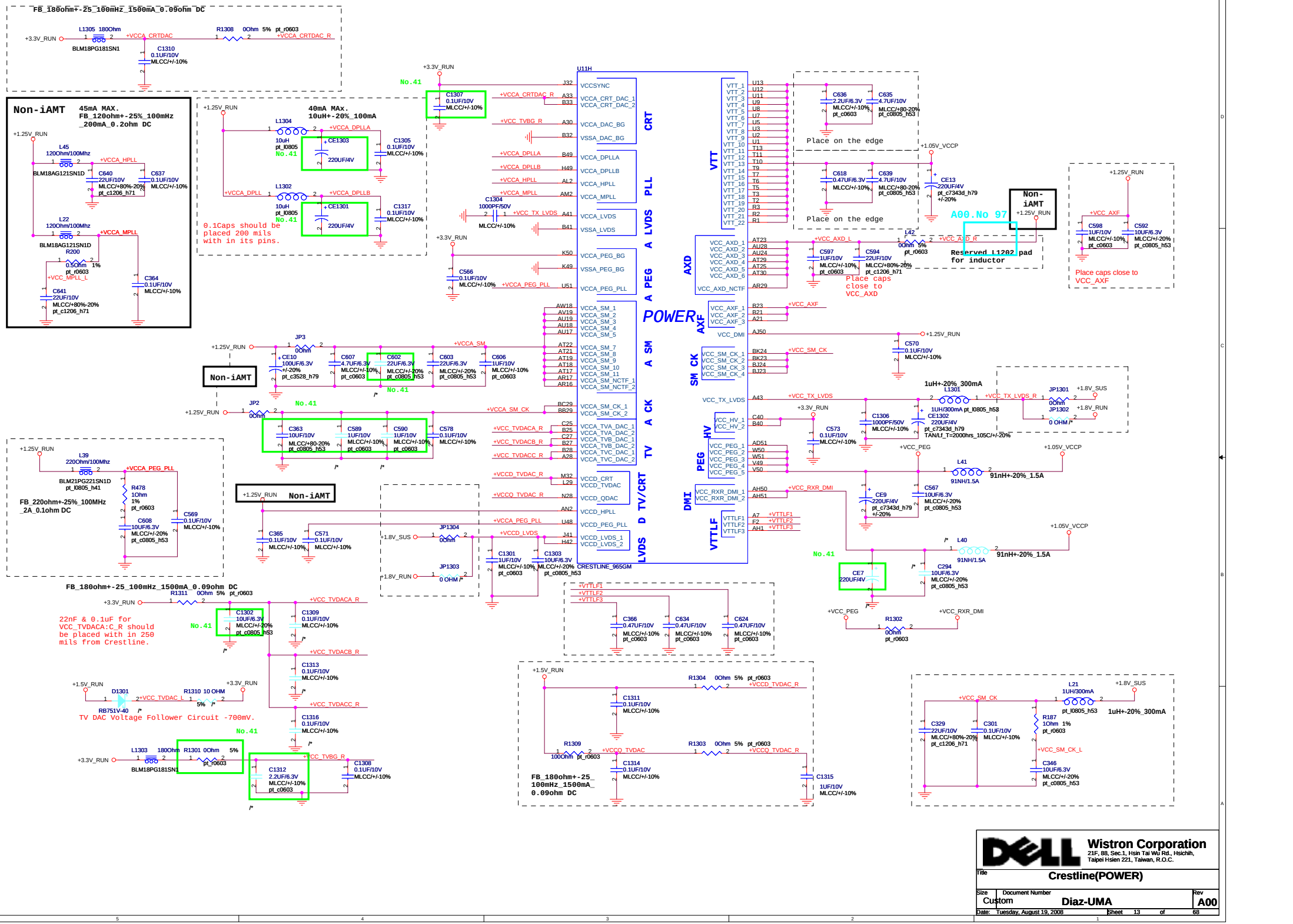

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Title	Crestline(POWER)
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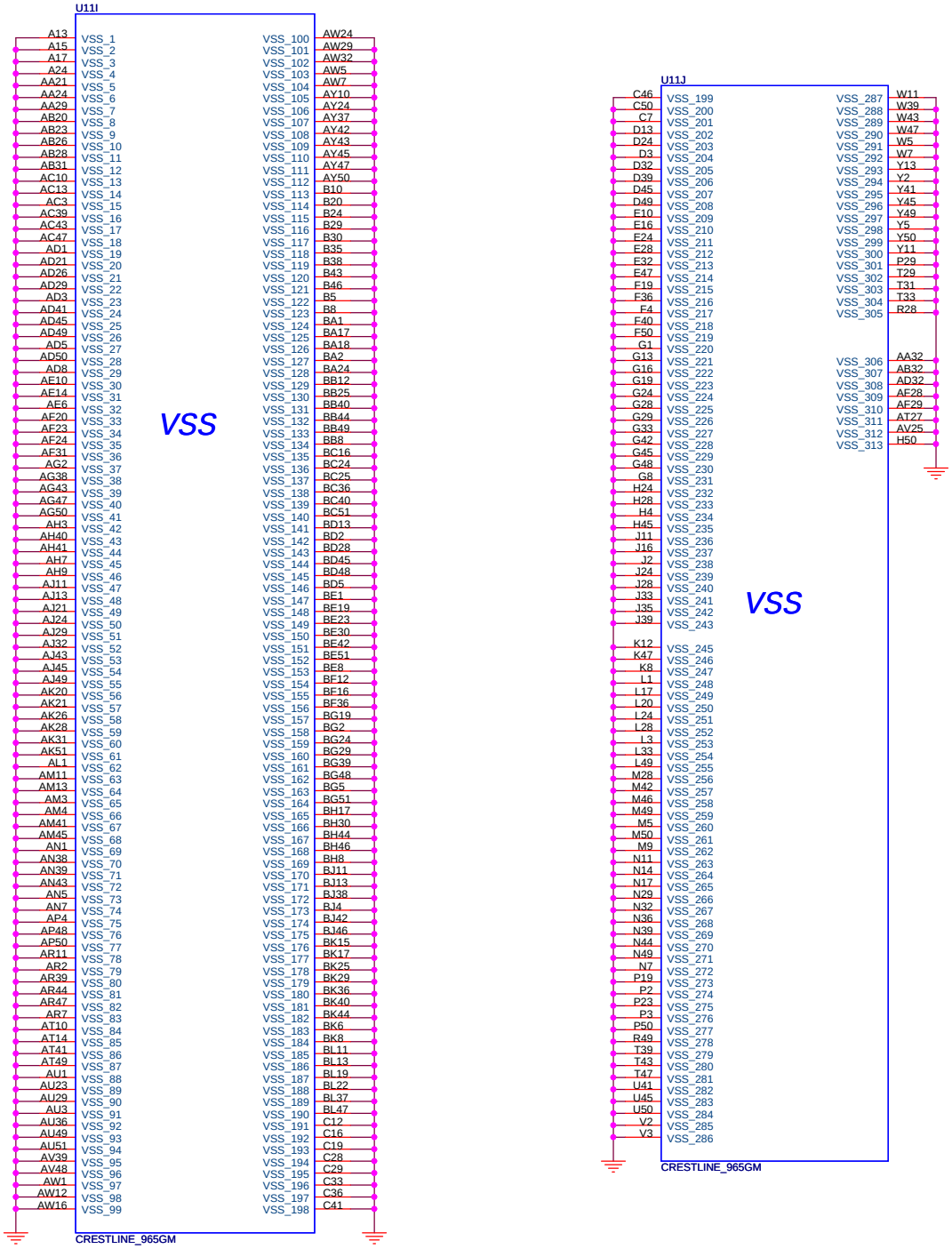

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Title: Crestline(VSS)		
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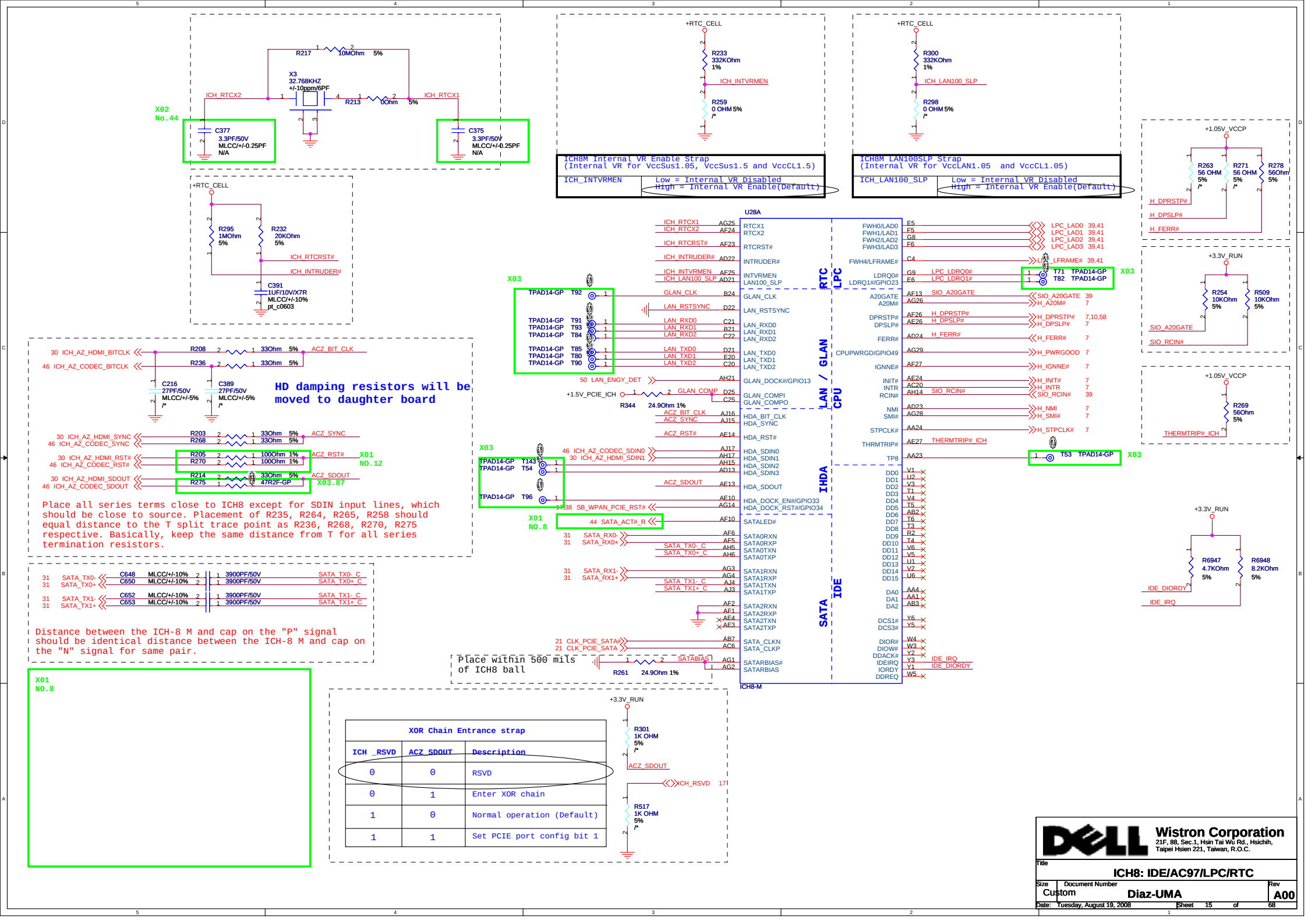

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Title: ICH8: IDE/AC97/LPC/RTC

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Place TX DC blocking caps close ICH8.

A00

C434 0.1UF/10V MLCC/+/-10% PCIE_TXN1_C
C436 0.1UF/10V MLCC/+/-10% PCIE_TXP1_C
C443 /* 0.1UF/10V MLCC/+/-10% PCIE_TXN2_C
C439 /* 0.1UF/10V MLCC/+/-10% PCIE_TXP2_C
C762 0.1UF/10V MLCC/+/-10% PCIE_TXN3_C
C761 0.1UF/10V MLCC/+/-10% PCIE_TXP3_C
C458 0.1UF/10V MLCC/+/-10% PCIE_TXN4_C
C461 0.1UF/10V MLCC/+/-10% PCIE_TXP4_C
C714 0.1UF/10V MLCC/+/-10% GLAN_TXN_C
C713 0.1UF/10V MLCC/+/-10% GLAN_TXP_C

U28D

PCI-Express Direct Media Interface

MiniWLAN
MiniWPAN
MiniWWAN
ExpressCard

SPI

USB

ICH8-M

BIOS should not enable the internal GPIO pull up resistor

R354 20KOhm 5%
R356 20KOhm 5%
A00

Place within 500 mils of ICH8

R286 24.9Ohm 1%

Layout Note:
Place 15 ohm within
500 mils from ICH.

X03 T214 TPAD14-GP

USER1 Left side pair top/left
USER2 Left side pair bottom/right
USER3 Right side pair top/left
USER3 Right side pair bottom/right
CCD
WWAN
WPAN
Express Card
FINGER PRINTER

PCI Pullups

R350 8.2KOhm 5%

RP4E RP4F RP4G RP4H RP4D RP4C RP4B RP4A
RP3E RP3F RP3G RP3H RP3D RP3C RP3B RP3A
8.2KOhm 5%

A00

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

R561 22.6Ohm 1% pt_r0603

Non-iAMT

RP1E RP1F RP1G RP1H RP1D RP1C RP1B RP1A
10KOhm 5%

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

R347 1K OHM 5%
R337 1K OHM 5%

PCI Device

R5C833	IDSEL: AD17	REQ1# GNT1#	PIRQC# PIRQD#

U28B

PCI

Interrupt I/F

X03 T95 TPAD14-GP
T77 TPAD14-GP
T89 TPAD14-GP

A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled. High = Default.

R346 1K OHM 5%

Non-iAMT

X02 NO.45

Add Buffers as needed for Loading and fanout concerns.

C689 0.047UF/10V MLCC/+/-10%
U30 SN74AHC1G32DBVR
R1601 100Ohm 1%
X01 NO.12
C6663 10PF/50V MLCC/+/-0.5PF
C382 0.047UF/10V MLCC/+/-10%
U14 SN74AHC1G32DBVR
R1602 0Ohm 5%
C747 0.047UF/10V MLCC/+/-10%
U37 SN74AHC1G32DBVR
R1603 0Ohm 5%
C758 47PF/50V MLCC/+/-5%

RP2D RP2C RP2B RP2A
100KOhm 5%

R355 10 OHM 5%
C475 8.2PF/50V MLCC/+/-0.25PF

Reserved for EMI.
Place resister and cap close to ICH.

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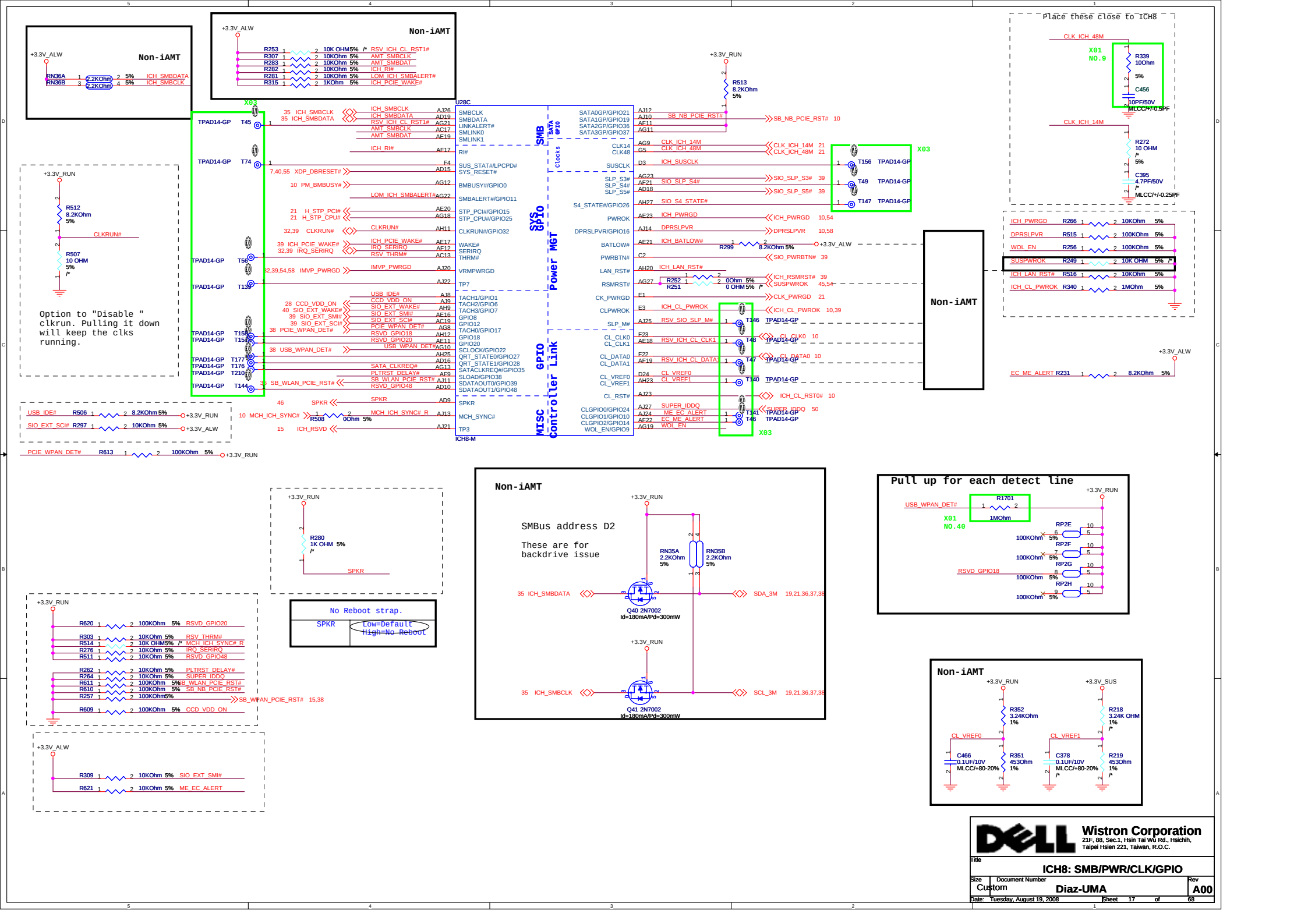
Non-iAMT
+3.3V_ALW
RN36A 2.2KOhm
RN36B 2.2KOhm
ICH_SMBDATA
ICH_SMBCLK
R253 10K OHM 5% RSV_ICH_CL_RST1#
R307 10KOhm 5% AMT_SMBCLK
R283 10KOhm 5% AMT_SMBDAT
R282 10KOhm 5% ICH_RI#
R281 10KOhm 5% LOM_ICH_SMBALERT#
R315 1KOhm 5% ICH_PCIE_WAKE#
X03
TPAD14-GP T45
TPAD14-GP T74
TPAD14-GP T56
TPAD14-GP T139
TPAD14-GP T158
TPAD14-GP T159
TPAD14-GP T177
TPAD14-GP T176
TPAD14-GP T210
TPAD14-GP T144
U28C
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
ICH8-M
SMB
SATA GPIO
Clocks
SYS PWR MGT
GPIO
GPIO Controller Link
MISC
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
+3.3V_RUN
R513 8.2KOhm 5%
SB_NB_PCIE_RST#
CLK_ICH_14M
CLK_ICH_48M
ICH_SUSCLK
SIO_SLP_S3#
SIO_SLP_S4#
SIO_SLP_S5#
SIO_S4_STATE#
ICH_PWRGD
DPRSLPVR
ICH_BATLOW#
R299 8.2KOhm 5%
ICH_LAN_RST#
R252 0Ohm 5%
R251 0 OHM 5%
ICH_RSMRST#
SUSPWROK
CLK_PWRGD
ICH_CL_PWROK
RSV_SIO_SLP_M#
RSV_ICH_CL_CLK1
CL_CLK0
CL_DATA0
CL_VREF0
CL_VREF1
ICH_CL_RST0#
SUPER_IDDQ
ME_EC_ALERT
EC_ME_ALERT
WOL_EN
T156 TPAD14-GP
T49 TPAD14-GP
T147 TPAD14-GP
T146 TPAD14-GP
T48 TPAD14-GP
T47 TPAD14-GP
T140 TPAD14-GP
T141 TPAD14-GP
T46 TPAD14-GP
Non-iAMT
Place these close to ICH8
CLK_ICH_48M
X01 NO.9
R339 10Ohm 5%
C456 10PF/50V MLCC/+/-0.5PF
CLK_ICH_14M
R272 10 OHM /* 5%
C395 4.7PF/50V /* MLCC/+/-0.25PF
ICH_PWRGD R266 10KOhm 5%
DPRSLPVR R515 100KOhm 5%
WOL_EN R256 100KOhm 5%
SUSPWROK R249 10K OHM 5% /*
ICH_LAN_RST# R516 10KOhm 5%
ICH_CL_PWROK R340 1MOhm 5%
EC_ME_ALERT R231 8.2KOhm 5%
+3.3V_ALW
+3.3V_RUN
R512 8.2KOhm 5%
CLKRUN#
R507 10 OHM 5% /*
Option to "Disable " clkrun. Pulling it down will keep the clks running.
USB_IDE# R506 8.2KOhm 5%
SIO_EXT_SCI# R297 10KOhm 5%
PCIE_WPAN_DET# R613 100KOhm 5%
R508 0Ohm 5%
MCH_ICH_SYNC# MCH_ICH_SYNC# R
ICH_RSVD
SPKR
R280 1K OHM 5% /*
No Reboot strap.
SPKR Low=Default High=No Reboot
Non-iAMT
SMBus address D2
These are for backdrive issue
RN35A 2.2KOhm 5%
RN35B 2.2KOhm 5%
35 ICH_SMBDATA
SDA_3M 19,21,36,37,38
Q40 2N7002 Id=180mA/Pd=300mW
35 ICH_SMBCLK
SCL_3M 19,21,36,37,38
Q41 2N7002 Id=180mA/Pd=300mW
Pull up for each detect line
USB_WPAN_DET#
R1701 1MOhm
X01 NO.40
RP2E 100KOhm 5%
RP2F 100KOhm 5%
RP2G 100KOhm 5%
RP2H 100KOhm 5%
RSVD_GPIO18
+3.3V_SUS
R620 100KOhm 5% RSVD_GPIO20
R303 10KOhm 5% RSV_THRM#
R514 10K OHM5% /* MCH_ICH_SYNC# R
R276 10KOhm 5% IRQ_SERIRQ
R511 10KOhm 5% RSVD_GPIO48
R262 10KOhm 5% PLTRST_DELAY#
R264 10KOhm 5% SUPER_IDDQ
R611 100KOhm 5% SB_WLAN_PCIE_RST#
R610 100KOhm 5% SB_NB_PCIE_RST#
R257 100KOhm 5%
SB_WPAN_PCIE_RST# 15,38
R609 100KOhm 5% CCD_VDD_ON
R309 10KOhm 5% SIO_EXT_SMI#
R621 10KOhm 5% ME_EC_ALERT
R352 3.24KOhm 1%
R218 3.24K OHM 1% /*
CL_VREF0
CL_VREF1
C466 0.1UF/10V MLCC/+80-20%
R351 453Ohm 1%
C378 0.1UF/10V MLCC/+80-20% /*
R219 453Ohm 1% /*
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Title
ICH8: SMB/PWR/CLK/GPIO
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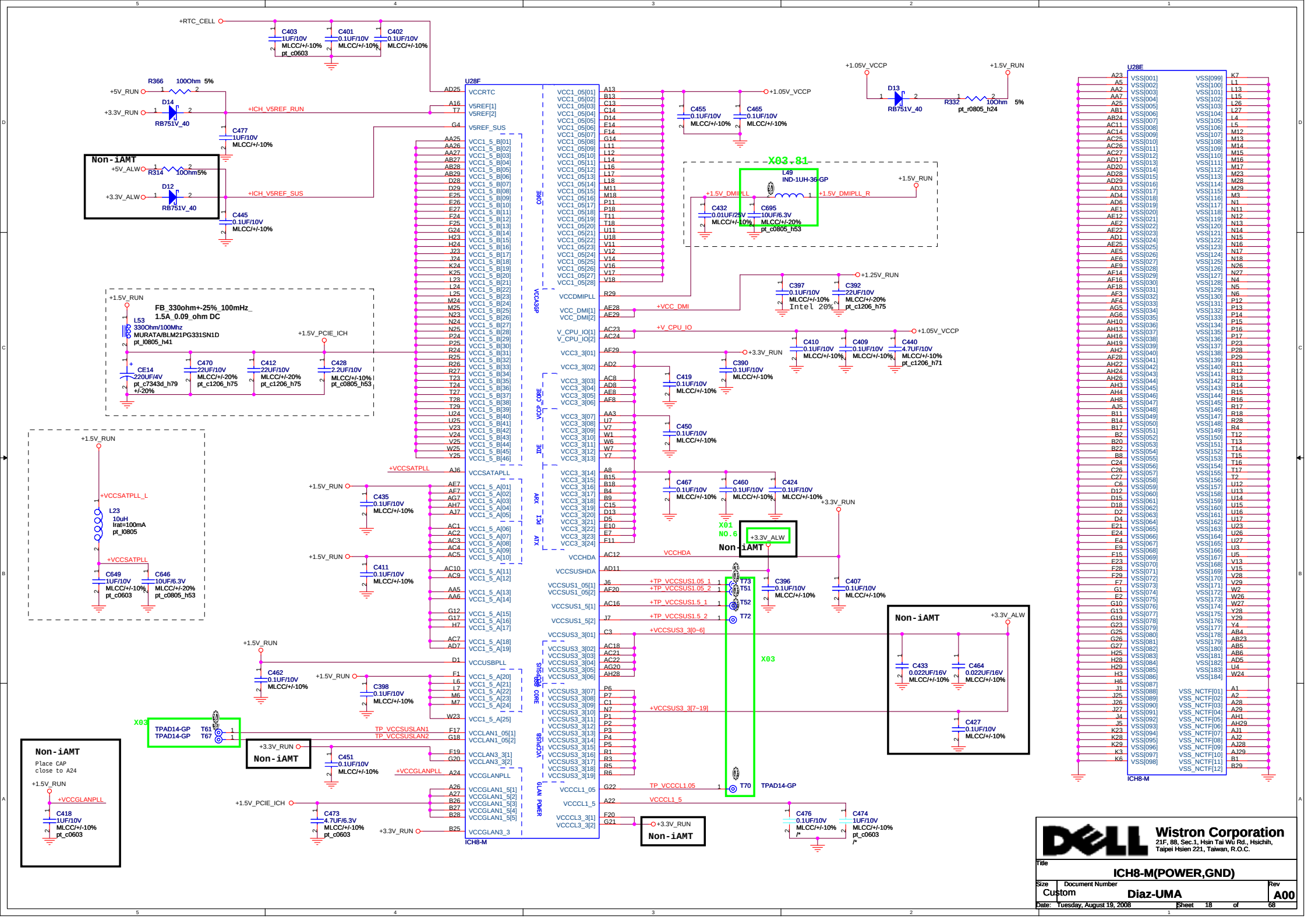

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A is required to route to Top SODIMM for AMT to function
Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

+1.8V_SUS
V_DDR_MCH_REF

CON14

1	VREF	VSS46	2		DDR_A_D6	DDR_A_D0	
3	VSS47	DQ4	4		DDR_A_D1	DDR_A_D5	
5	DQ0	DQ5	6				
7	DQ1	VSS15	8			DDR_A_DM0	
9	VSS37	DM0	10		DDR_A_DQS#0		
11	DQS#0	VSS5	12		DDR_A_DQS0	DDR_A_D7	
13	DQS0	DQ6	14			DDR_A_D4	
15	VSS48	DQ7	16				
17	DQ2	VSS16	18		DDR_A_D3	DDR_A_D15	
19	DQ3	DQ12	20		DDR_A_D2	DDR_A_D13	
21	VSS38	DQ13	22				
23	DQ8	VSS17	24		DDR_A_D8	DDR_A_DM1	
25	DQ9	DM1	26		DDR_A_D12		
27	VSS49	VSS53	28				
29	DQS#1	CK0	30		DDR_A_DQS#1	M_CLK_DDR0	10
31	DQS1	CK0#	32		DDR_A_DQS1	M_CLK_DDR#0	10
33	VSS39	VSS41	34				
35	DQ10	DQ14	36		DDR_A_D9	DDR_A_D14	
37	DQ11	DQ15	38		DDR_A_D11	DDR_A_D10	
39	VSS50	VSS54	40				
41			42				
43	VSS18	VSS20	44		DDR_A_D17	DDR_A_D21	
45	DQ16	DQ20	46		DDR_A_D20	DDR_A_D18	
47	DQ17	DQ21	48				
49	VSS1	VSS6	50		DDR_A_DQS#2	PM_EXTTS#0	PM_EXTTS#0 10
51	DQS#2	NC3	52		DDR_A_DQS2	DDR_A_DM2	
53	DQS2	DM2	54				
55	VSS19	VSS21	56		DDR_A_D16	DDR_A_D22	
57	DQ18	DQ22	58		DDR_A_D19	DDR_A_D23	
59	DQ19	DQ23	60				
61	VSS22	VSS24	62		DDR_A_D24	DDR_A_D28	
63	DQ24	DQ28	64		DDR_A_D25	DDR_A_D29	
65	DQ25	DQ29	66				
67	VSS23	VSS25	68		DDR_A_DM3	DDR_A_DQS#3	
69	DM3	DQS#3	70			DDR_A_DQS3	
71	NC4	DQS3	72				
73	VSS9	VSS10	74		DDR_A_D31	DDR_A_D26	
75	DQ26	DQ30	76		DDR_A_D30	DDR_A_D27	
77	DQ27	DQ31	78				
79	VSS4	VSS8	80		10,20 DDR_CKE0_DIMMA	DDR_CKE1_DIMMA	10,20
81	CKE0	CKE1	82				
83	VDD7	VDD8	84				
85	NC1	A15	86		DDR_A_BS2	DDR_A_MA14	DDR_A_MA14 10,20
87	A16_BA2	A14	88		11,20 DDR_A_BS2		
89	VDD9	VDD11	90		DDR_A_MA12	DDR_A_MA11	
91	A12	A11	92		DDR_A_MA9	DDR_A_MA7	
93	A9	A7	94		DDR_A_MA8	DDR_A_MA6	
95	A8	A6	96				
97	VDD5	VDD4	98		DDR_A_MA5	DDR_A_MA4	
99	A5	A4	100		DDR_A_MA3	DDR_A_MA2	
101	A3	A2	102		DDR_A_MA1	DDR_A_MA0	
103	A1	A0	104				
105	VDD10	VDD12	106		DDR_A_MA10	DDR_A_BS1	11,20
107	A10/AP	BA1	108		11,20 DDR_A_BS0	DDR_A_RAS#	11,20
109	BA0	RAS#	110		DDR_A_WE#	DDR_CS0_DIMMA#	10,20
111	WE#	S0#	112				
113	VDD2	VDD1	114		11,20 DDR_A_CAS#	M_ODT0	M_ODT0 10,20
115	CAS#	ODT0	116		10,20 DDR_CS1_DIMMA#	DDR_A_MA13	
117	S1#	A13	118				
119	VDD3	VDD6	120		10,20 M_ODT1		
121	ODT1	NC2	122				
123	VSS11	VSS12	124		DDR_A_D33	DDR_A_D36	
125	DQ32	DQ36	126		DDR_A_D32	DDR_A_D38	
127	DQ33	DQ37	128				
129	VSS26	VSS28	130		DDR_A_DQS#4	DDR_A_DM4	
131	DQS#4	DM4	132		DDR_A_DQS4		
133	DQS4	VSS42	134			DDR_A_D37	
135	VSS2	DQ38	136		DDR_A_D34	DDR_A_D39	
137	DQ34	DQ39	138		DDR_A_D35		
139	DQ35	VSS55	140			DDR_A_D41	
141	VSS27	DQ44	142		DDR_A_D44	DDR_A_D43	
143	DQ40	DQ45	144		DDR_A_D40		
145	DQ41	VSS43	146			DDR_A_DQS#5	
147	VSS29	DQS#5	148		DDR_A_DM5	DDR_A_DQS5	
149	DM5	DQS5	150				
151	VSS51	VSS56	152		DDR_A_D42	DDR_A_D45	
153	DQ42	DQ46	154		DDR_A_D46	DDR_A_D47	
155	DQ43	DQ47	156				
157	VSS40	VSS44	158		DDR_A_D49	DDR_A_D52	
159	DQ48	DQ52	160		DDR_A_D48	DDR_A_D53	
161	DQ49	DQ53	162				
163	VSS52	VSS57	164			M_CLK_DDR1	10
165	NCTEST	CK1	166			M_CLK_DDR#1	10
167	VSS30	CK1#	168		DDR_A_DQS#6		
169	DQS#6	VSS45	170		DDR_A_DQS6	DDR_A_DM6	
171	DQS6	DM6	172				
173	VSS31	VSS32	174		DDR_A_D55	DDR_A_D54	
175	DQ50	DQ54	176		DDR_A_D50	DDR_A_D51	
177	DQ51	DQ55	178				
179	VSS33	VSS35	180		DDR_A_D60	DDR_A_D63	
181	DQ56	DQ60	182		DDR_A_D59	DDR_A_D61	
183	DQ57	DQ61	184				
185	VSS3	VSS7	186		DDR_A_DM7	DDR_A_DQS#7	
187	DM7	DQS#7	188			DDR_A_DQS7	
189	VSS34	DQS7	190				
191	DQ58	VSS36	192		DDR_A_D57	DDR_A_D58	
193	DQ59	DQ62	194		DDR_A_D56	DDR_A_D62	
195	VSS14	DQ63	196				
197	SDA	VSS13	198		17,21,36,37,38 SDA_3M		
199	SCL	SA0	200		17,21,36,37,38 SCL_3M		
201	VDDSPD	SA1	202				
203	GND0	GND1	204				
	NP_NC1	NP_NC2					

REV
FOXCONN/AS0A426-N2RN-7F

CLOCK 0 , 1
CKE 0 , 1

DDR_A_DM[0..7] 11
DDR_A_D[0..63] 11
DDR_A_DQS[0..7] 11
DDR_A_DQS#[0..7] 11
DDR_A_MA[0..13] 11,20

V_DDR_MCH_REF
C280 MLCC/+/-80-20% 0.1UF/10V
C278 MLCC/+/-10% 2.2UF/6.3V
pt_c0805_h53

R505 10KOhm 5%
R501 10KOhm 5%

+3.3V_RUN
Non-iAMT
C373 MLCC/+/-10% 2.2UF/6.3V
C374 MLCC/+80-20% 0.1UF/10V
pt_c0805_h53

SDA_3M
SCL_3M
+3.3V_RUN
Non-iAMT
SMbus address A0

BOT

+1.8V_SUS
V_DDR_MCH_REF

CON15

1	VREF	VSS46	2		DDR_B_D1	DDR_B_D0	
3	VSS47	DQ4	4		DDR_B_D5	DDR_B_D4	
5	DQ0	DQ5	6				
7	DQ1	VSS15	8			DDR_B_DM0	
9	VSS37	DM0	10		DDR_B_DQS#0		
11	DQS#0	VSS5	12		DDR_B_DQS0	DDR_B_D6	
13	DQS0	DQ6	14			DDR_B_D7	
15	VSS48	DQ7	16				
17	DQ2	VSS16	18		DDR_B_D2	DDR_B_D12	
19	DQ3	DQ12	20		DDR_B_D3	DDR_B_D11	
21	VSS38	DQ13	22				
23	DQ8	VSS17	24		DDR_B_D14	DDR_B_DM1	
25	DQ9	DM1	26		DDR_B_D15		
27	VSS49	VSS53	28				
29	DQS#1	CK0	30		DDR_B_DQS#1	M_CLK_DDR2	10
31	DQS1	CK0#	32		DDR_B_DQS1	M_CLK_DDR#2	10
33	VSS39	VSS41	34				
35	DQ10	DQ14	36		DDR_B_D13	DDR_B_D8	
37	DQ11	DQ15	38		DDR_B_D10	DDR_B_D9	
39	VSS50	VSS54	40				
41			42				
43	VSS18	VSS20	44		DDR_B_D17	DDR_B_D16	
45	DQ16	DQ20	46		DDR_B_D20	DDR_B_D21	
47	DQ17	DQ21	48				
49	VSS1	VSS6	50		DDR_B_DQS#2	PM_EXTTS#1	PM_EXTTS#1 10
51	DQS#2	NC3	52		DDR_B_DQS2	DDR_B_DM2	
53	DQS2	DM2	54				
55	VSS19	VSS21	56		DDR_B_D19	DDR_B_D22	
57	DQ18	DQ22	58		DDR_B_D18	DDR_B_D23	
59	DQ19	DQ23	60				
61	VSS22	VSS24	62		DDR_B_D29	DDR_B_D28	
63	DQ24	DQ28	64		DDR_B_D24	DDR_B_D25	
65	DQ25	DQ29	66				
67	VSS23	VSS25	68		DDR_B_DM3	DDR_B_DQS#3	
69	DM3	DQS#3	70			DDR_B_DQS3	
71	NC4	DQS3	72				
73	VSS9	VSS10	74		DDR_B_D27	DDR_B_D31	
75	DQ26	DQ30	76		DDR_B_D30	DDR_B_D26	
77	DQ27	DQ31	78				
79	VSS4	VSS8	80		10,20 DDR_CKE2_DIMMB	DDR_CKE3_DIMMB	10,20
81	CKE0	CKE1	82				
83	VDD7	VDD8	84				
85	NC1	A15	86		DDR_B_BS2	DDR_B_MA14	DDR_B_MA14 10,20
87	A16_BA2	A14	88		11,20 DDR_B_BS2		
89	VDD9	VDD11	90		DDR_B_MA12	DDR_B_MA11	
91	A12	A11	92		DDR_B_MA9	DDR_B_MA7	
93	A9	A7	94		DDR_B_MA8	DDR_B_MA6	
95	A8	A6	96				
97	VDD5	VDD4	98		DDR_B_MA5	DDR_B_MA4	
99	A5	A4	100		DDR_B_MA3	DDR_B_MA2	
101	A3	A2	102		DDR_B_MA1	DDR_B_MA0	
103	A1	A0	104				
105	VDD10	VDD12	106		DDR_B_MA10	DDR_B_BS1	11,20
107	A10/AP	BA1	108		11,20 DDR_B_BS0	DDR_B_RAS#	11,20
109	BA0	RAS#	110		DDR_B_WE#	DDR_CS2_DIMMB#	10,20
111	WE#	S0#	112				
113	VDD2	VDD1	114		11,20 DDR_B_CAS#	M_ODT2	M_ODT2 10,20
115	CAS#	ODT0	116		10,20 DDR_CS3_DIMMB#	DDR_B_MA13	
117	S1#	A13	118				
119	VDD3	VDD6	120		10,20 M_ODT3		
121	ODT1	NC2	122				
123	VSS11	VSS12	124		DDR_B_D34	DDR_B_D37	
125	DQ32	DQ36	126		DDR_B_D32	DDR_B_D36	
127	DQ33	DQ37	128				
129	VSS26	VSS28	130		DDR_B_DQS#4	DDR_B_DM4	
131	DQS#4	DM4	132		DDR_B_DQS4		
133	DQS4	VSS42	134			DDR_B_D38	
135	VSS2	DQ38	136		DDR_B_D33	DDR_B_D39	
137	DQ34	DQ39	138		DDR_B_D35		
139	DQ35	VSS55	140			DDR_B_D40	
141	VSS27	DQ44	142		DDR_B_D41	DDR_B_D45	
143	DQ40	DQ45	144		DDR_B_D46		
145	DQ41	VSS43	146			DDR_B_DQS#5	
147	VSS29	DQS#5	148		DDR_B_DM5	DDR_B_DQS5	
149	DM5	DQS5	150				
151	VSS51	VSS56	152		DDR_B_D47	DDR_B_D44	
153	DQ42	DQ46	154		DDR_B_D43	DDR_B_D42	
155	DQ43	DQ47	156				
157	VSS40	VSS44	158		DDR_B_D52	DDR_B_D48	
159	DQ48	DQ52	160		DDR_B_D49	DDR_B_D53	
161	DQ49	DQ53	162				
163	VSS52	VSS57	164			M_CLK_DDR3	10
165	NCTEST	CK1	166			M_CLK_DDR#3	10
167	VSS30	CK1#	168		DDR_B_DQS#6		
169	DQS#6	VSS45	170		DDR_B_DQS6	DDR_B_DM6	
171	DQS6	DM6	172				
173	VSS31	VSS32	174		DDR_B_D55	DDR_B_D50	
175	DQ50	DQ54	176		DDR_B_D51	DDR_B_D54	
177	DQ51	DQ55	178				
179	VSS33	VSS35	180		DDR_B_D57	DDR_B_D60	
181	DQ56	DQ60	182		DDR_B_D56	DDR_B_D61	
183	DQ57	DQ61	184				
185	VSS3	VSS7	186		DDR_B_DM7	DDR_B_DQS#7	
187	DM7	DQS#7	188			DDR_B_DQS7	
189	VSS34	DQS7	190				
191	DQ58	VSS36	192		DDR_B_D63	DDR_B_D59	
193	DQ59	DQ62	194		DDR_B_D62	DDR_B_D58	
195	VSS14	DQ63	196				
197	SDA	VSS13	198		SDA_3M		
199	SCL	SA0	200		SCL_3M		
201	VDDSPD	SA1	202				
203	GND0	GND1	204				
	NP_NC1	NP_NC2					

REV
FOXCONN/AS0A426-NARN-7F

CLOCK 2 , 3
CKE 2 , 3

DDR_B_DM[0..7] 11
DDR_B_D[0..63] 11
DDR_B_DQS[0..7] 11
DDR_B_DQS#[0..7] 11
DDR_B_MA[0..13] 11,20

V_DDR_MCH_REF
C281 MLCC/+/-80-20% 0.1UF/10V
C275 MLCC/+/-10% 2.2UF/6.3V
pt_c0805_h53

+3.3V_RUN
Non-iAMT
C651 MLCC/+/-10% 2.2UF/6.3V
C647 MLCC/+80-20% 0.1UF/10V
pt_c0805_h53

Non-iAMT
+3.3V_RUN
R211
R212 10KOhm 5%

SMbus address A4

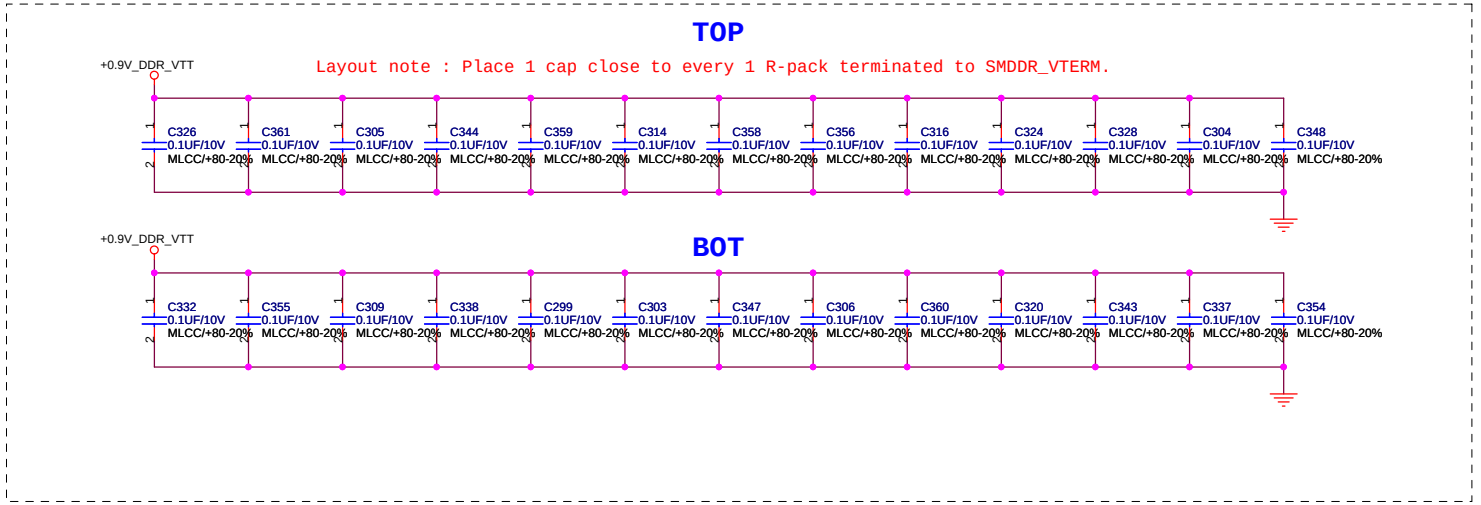
+1.8V_SUS
Please these Caps near So-Dimm1
C327 C300 C333 C341 C342
2.2UF/6.3V MLCC/+/-10% pt_c0603

+1.8V_SUS
Please these Caps near So-Dimm2
C321 C619 C591 C331 C317
2.2UF/6.3V MLCC/+/-10% pt_c0603

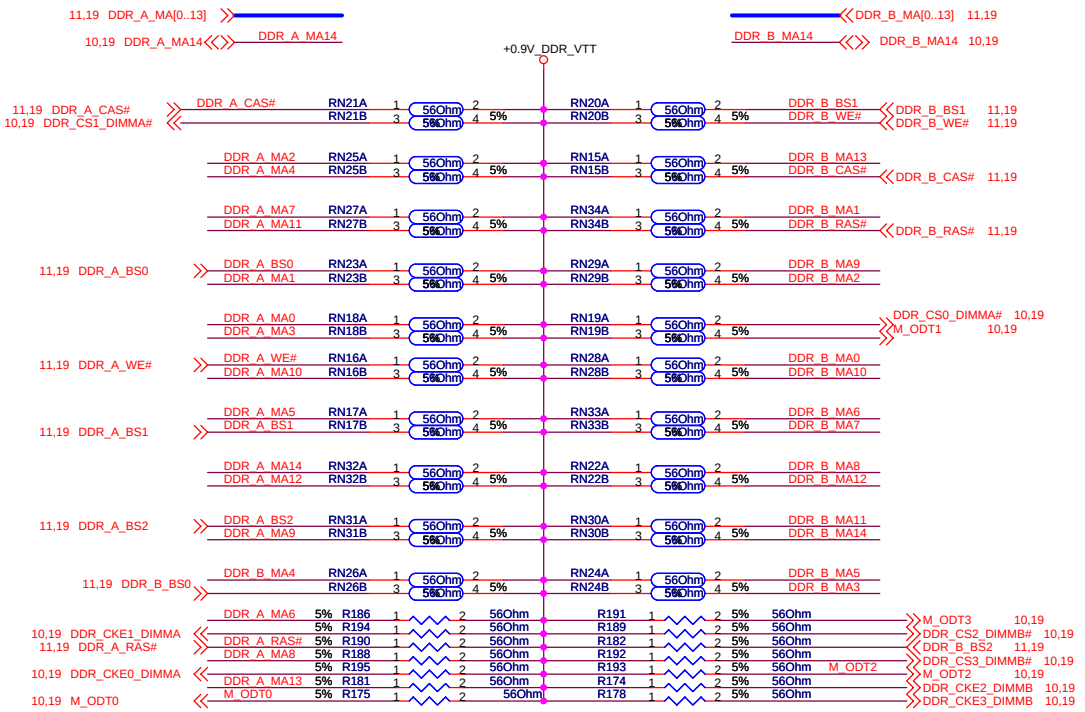
+1.8V_SUS
Please these Caps near So-Dimm1
C315 C325 C319 C323
0.1UF/10V MLCC/+80-20%

+1.8V_SUS
Please these Caps near So-Dimm2
C340 C601 C609 C616
0.1UF/10V MLCC/+80-20%

Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR2 SO-DIMM (0)			
Size: Custom	Document Number: Diaz-UMA	Rev: A00	
Date: Tuesday, August 19, 2008	Sheet 19 of 68		



Please these resistor closely DIMMA, all trace length<750 mil.



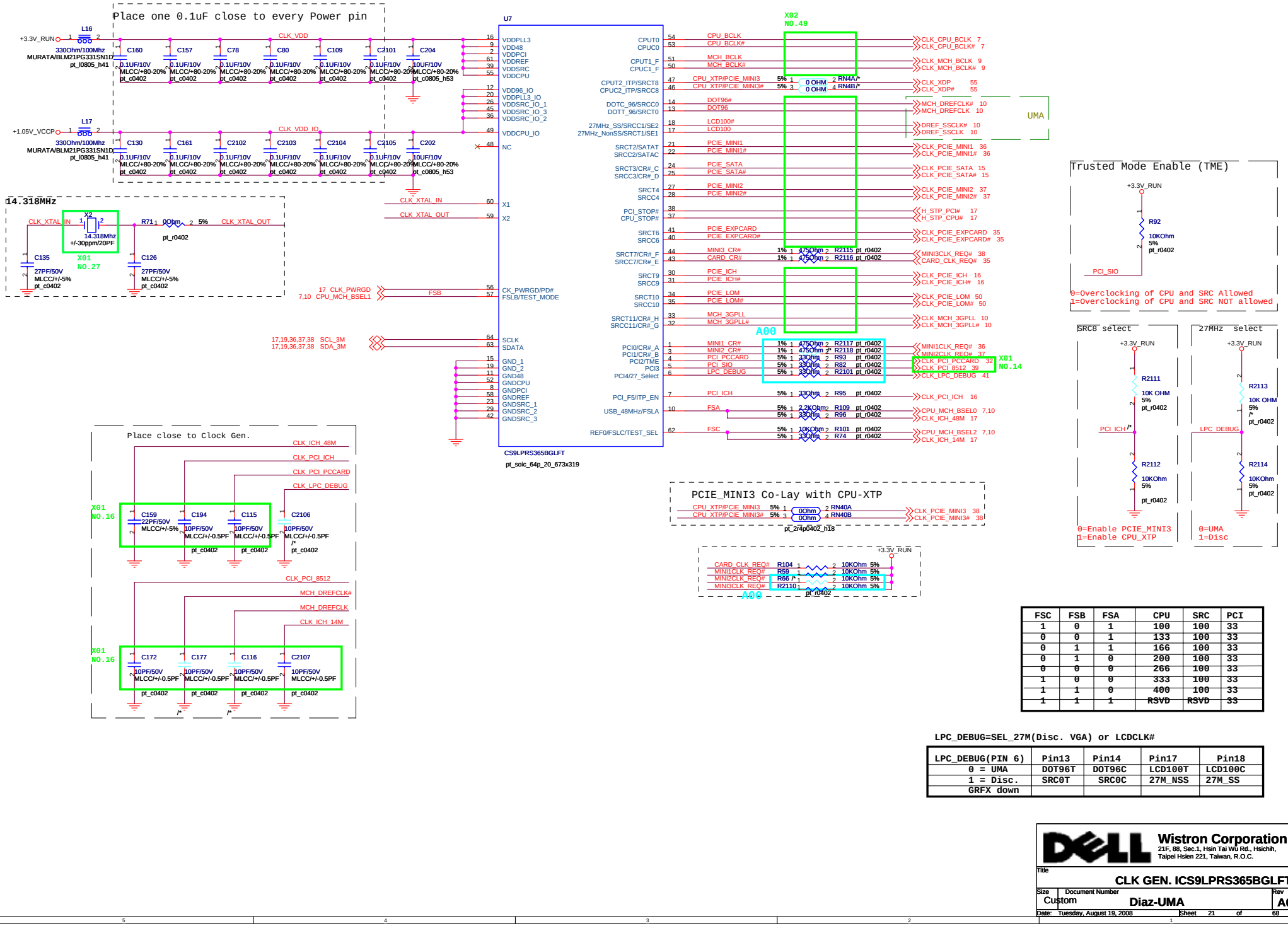
Please these resistor closely DIMMB, all trace length<750 mil.

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2 SO-DIMM (1)**

Size	Document Number	Rev
A3	Diaz-UMA	A00

Date: Tuesday, August 19, 2008 Sheet 20 of 68



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	RSVD	33

LPC_DEBUG=SEL_27M(Disc. VGA) or LCDCLK#

LPC_DEBUG(PIN 6)	Pin13	Pin14	Pin17	Pin18
0 = UMA	DOT96T	DOT96C	LCD100T	LCD100C
1 = Disc.	SRC0T	SRC0C	27M_NSS	27M_SS
GRFX down				

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CLK GEN. ICS9LPRS365BGLFT

Size: Custom | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 21 of 68

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Title: BLANK PAGE

Size: A3 | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 22 of 68

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Date: Tuesday, August 19, 2008 | Sheet 23 of 68

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Title: BLANK PAGE		
Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 24 of 68	

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Title		
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Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 25 of 68	

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Title: BLANK PAGE

Size: A3 | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 26 of 68

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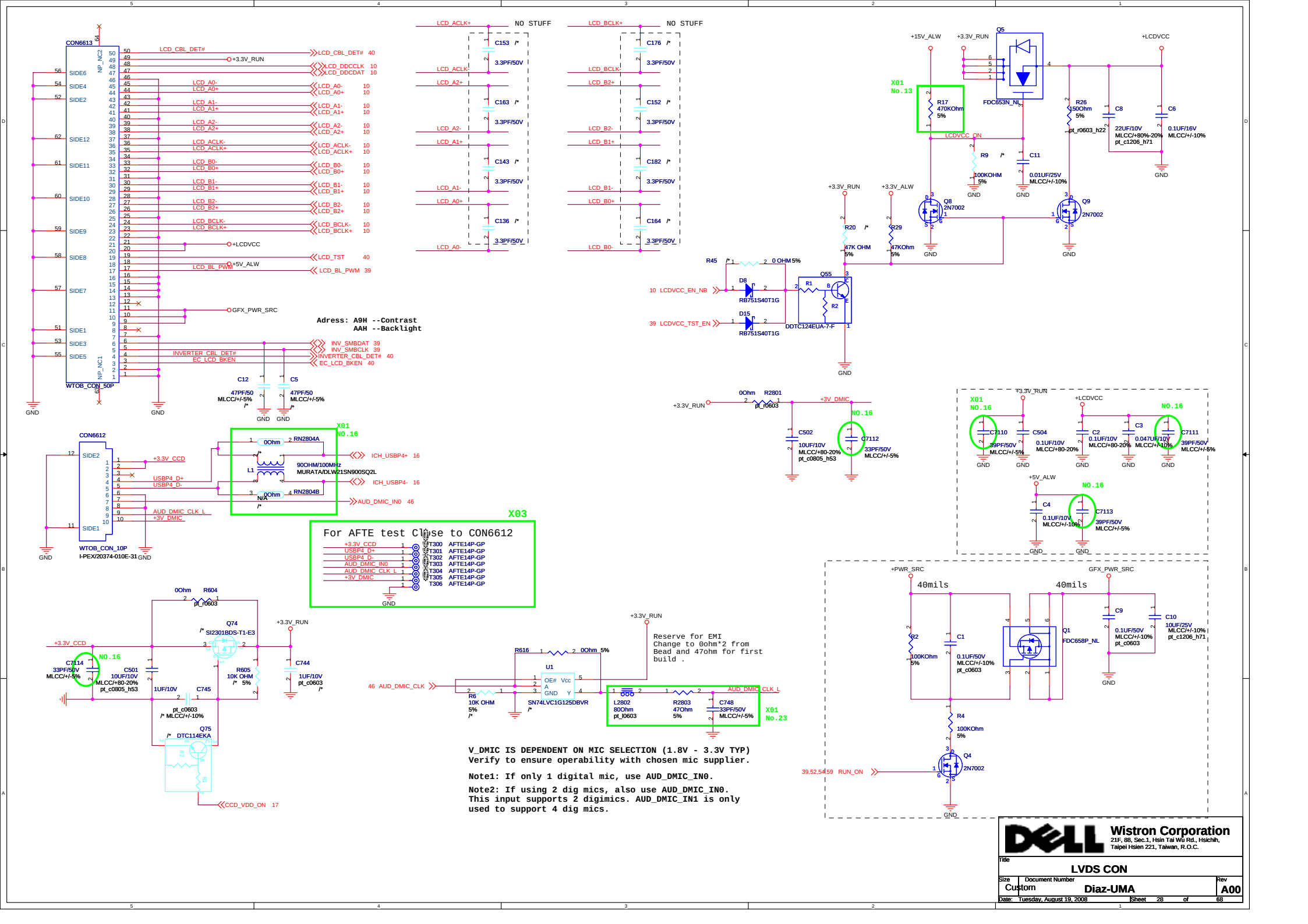
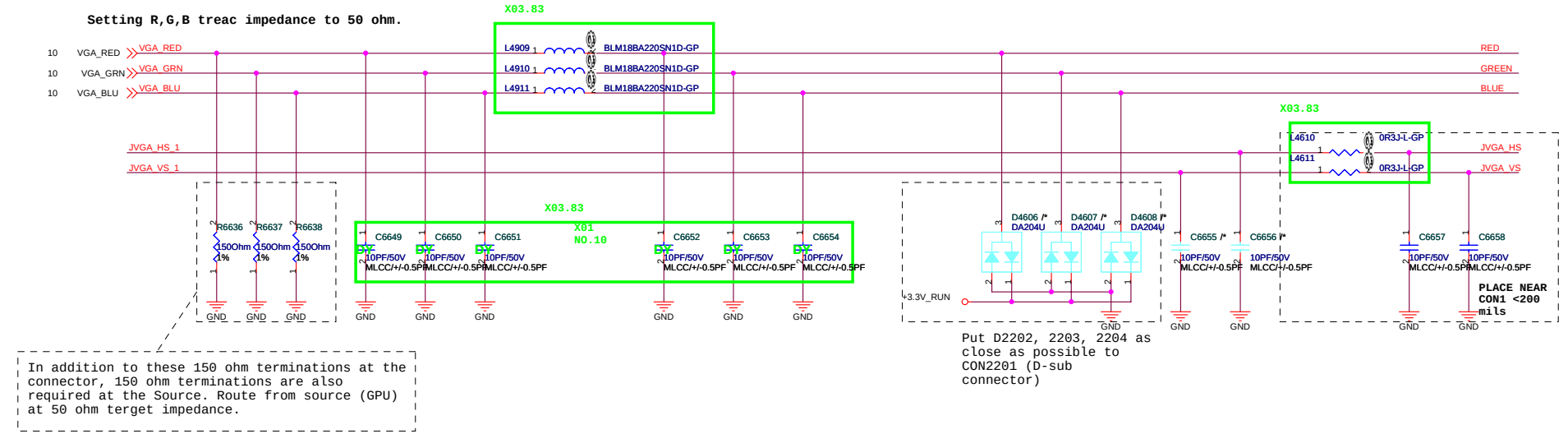
Title: BLANK PAGE		
Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 27 of 68	

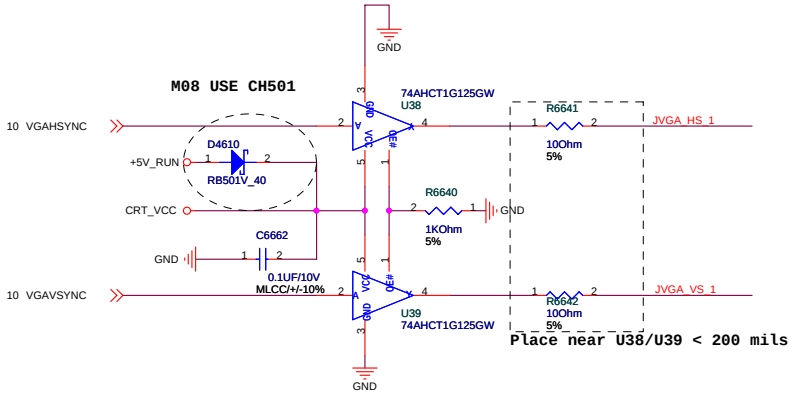

CON6613
WTOB_CON_50P
LCD_CBL_DET#
+3.3V_RUN
LCD_DDCCLK
LCD_DDCDAT
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
LCD_ACLK-
LCD_ACLK+
LCD_B0-
LCD_B0+
LCD_B1-
LCD_B1+
LCD_B2-
LCD_B2+
LCD_BCLK-
LCD_BCLK+
+LCDVCC
LCD_TST
+5V_ALW
LCD_BL_PWM
GFX_PWR_SRC
INV_SMBDAT
INV_SMBCLK
INVERTER_CBL_DET#
EC_LCD_BKEN
Adress: A9H --Contrast
AAH --Backlight
C12
C5
47PF/50
MLCC/+/-5%
CON6612
WTOB_CON_10P
I-PEX/20374-010E-31
+3.3V_CCD
USBP4_D+
USBP4_D-
AUD_DMIC_CLK_L
+3V_DMIC
RN2804A
RN2804B
L1
90OHM/100MHz
MURATA/DLW21SN900SQ2L
ICH_USBP4+
ICH_USBP4-
AUD_DMIC_IN0
X01
NO.16
X03
For AFTE test Close to CON6612
AFTE14P-GP
C153
C163
C143
C136
C176
C152
C182
C164
3.3PF/50V
NO STUFF
R45
0 OHM 5%
D8
D15
RB751S40T1G
Q55
DDTC124EUA-7-F
LCDVCC_EN_NB
LCDVCC_TST_EN
Q5
FDC653N_NL
R17
470KOhm
5%
R26
150Ohm
C8
22UF/10V
MLCC/+80%-20%
pt_c1206_h71
C6
0.1UF/16V
MLCC/+/-10%
LCDVCC_ON
R9
100KOHM
C11
0.01UF/25V
MLCC/+/-10%
Q8
2N7002
Q9
R20
47K OHM
R29
47KOhm
R2801
0Ohm
pt_r0603
C502
10UF/10V
MLCC/+80-20%
pt_c0805_h53
C7112
33PF/50V
C7110
C504
0.1UF/10V
C2
C3
0.047UF/10V
C7111
C4
C7113
Q74
SI2301BDS-T1-E3
R604
R605
10K OHM
C501
C744
C745
1UF/10V
Q75
DTC114EKA
CCD_VDD_ON
R616
U1
SN74LVC1G125DBVR
R6
10K OHM
L2802
80Ohm
pt_l0603
R2803
47Ohm
C748
33PF/50V
AUD_DMIC_CLK
Reserve for EMI
Change to 0ohm*2 from
Bead and 47ohm for first
build .
V_DMIC IS DEPENDENT ON MIC SELECTION (1.8V - 3.3V TYP)
Verify to ensure operability with chosen mic supplier.
Note1: If only 1 digital mic, use AUD_DMIC_IN0.
Note2: If using 2 dig mics, also use AUD_DMIC_IN0.
This input supports 2 digimics. AUD_DMIC_IN1 is only
used to support 4 dig mics.
+PWR_SRC
GFX_PWR_SRC
40mils
R2
100KOhm
C1
0.1UF/50V
Q1
FDC658P_NL
C9
C10
10UF/25V
R4
Q4
2N7002
RUN_ON
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LVDS CON
Size
Custom
Document Number
Diaz-UMA
Rev
A00
Date: Tuesday, August 19, 2008
Sheet 28 of 68

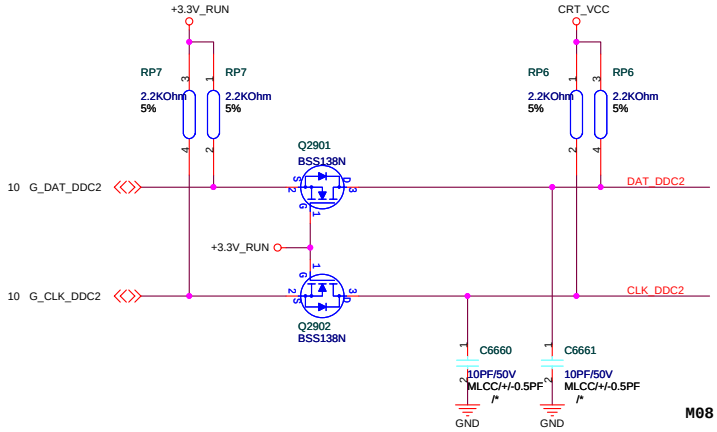
Setting R,G,B treac impedance to 50 ohm.

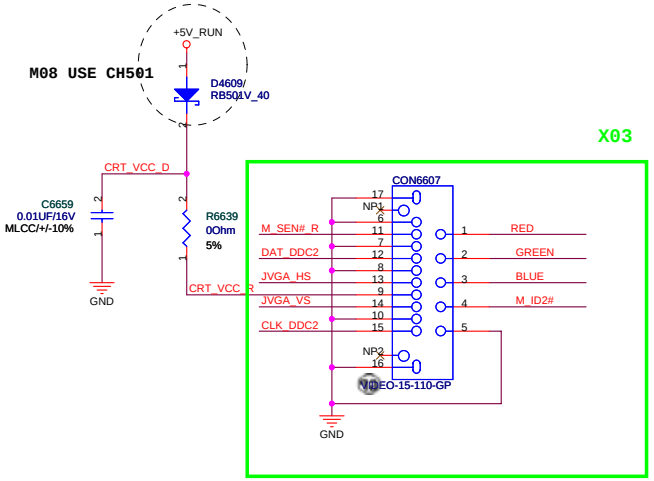


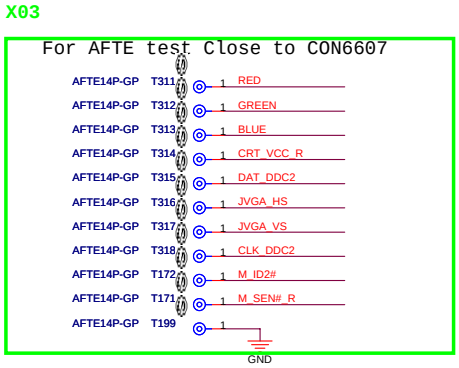
In addition to these 150 ohm terminations at the connector, 150 ohm terminations are also required at the Source. Route from source (GPU) at 50 ohm terget impedance.

Put D2202, 2203, 2204 as close as possible to CON2201 (D-sub connector)









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Title: VGA CRT CON

Size: Custom | Document Number: Diaz-UMA | Rev: A00

Date: Tuesday, August 19, 2008 | Sheet 29 of 68

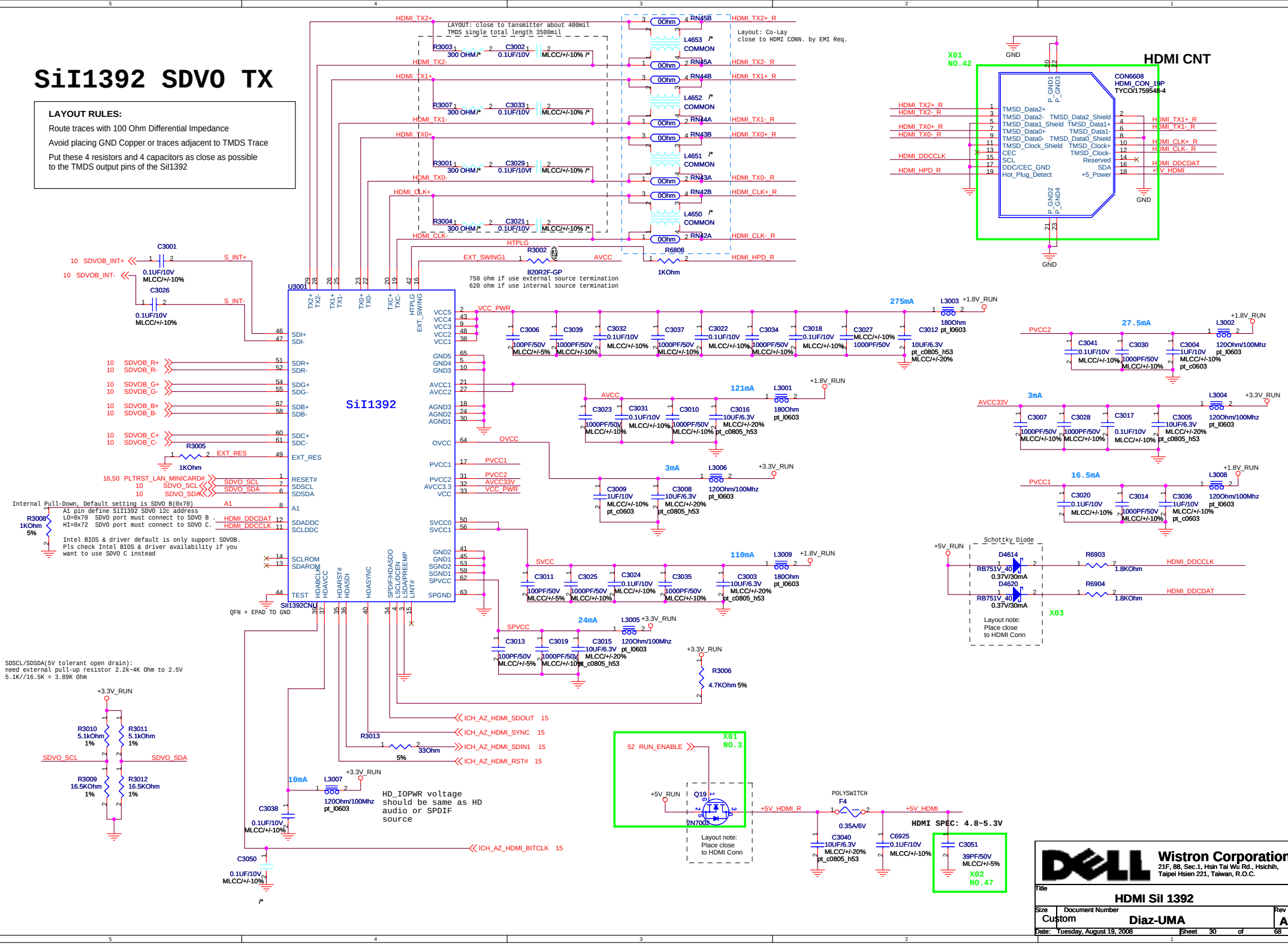
SiI1392 SDVO TX

LAYOUT RULES:

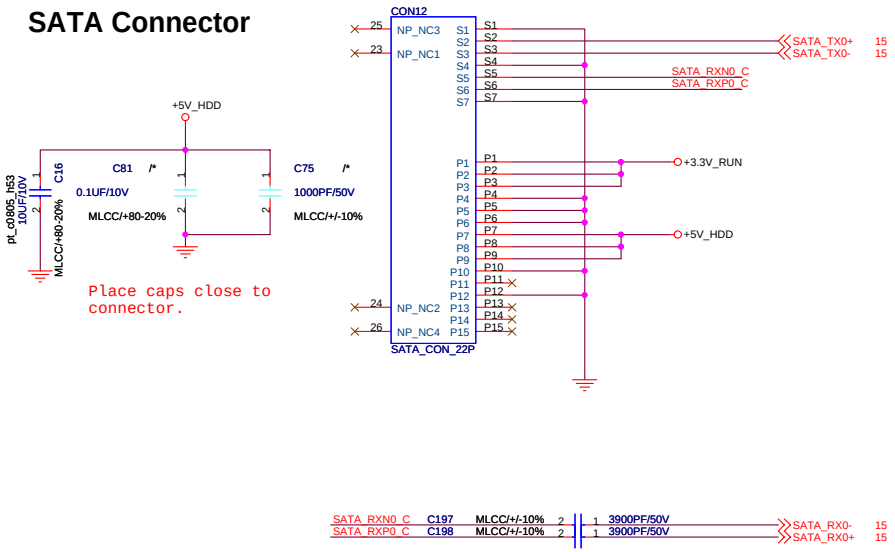
Route traces with 100 Ohm Differential Impedance

Avoid placing GND Copper or traces adjacent to TMDS Trace

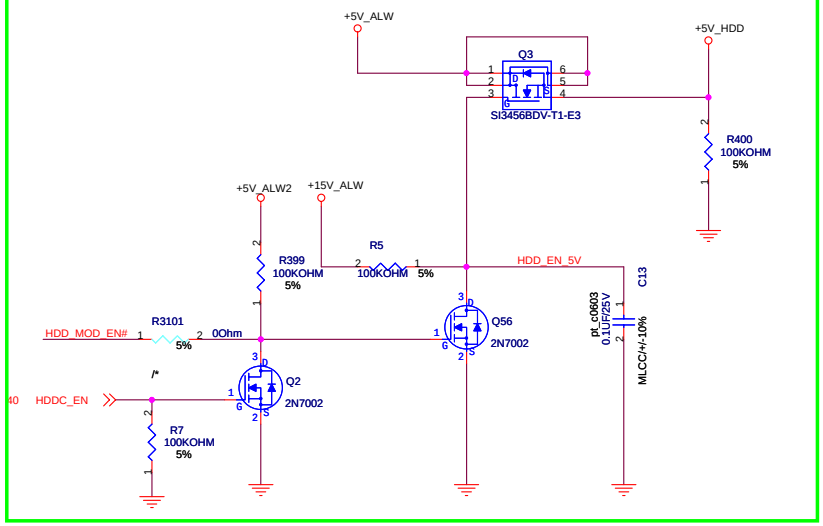
Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the Sil1392



SATA Connector

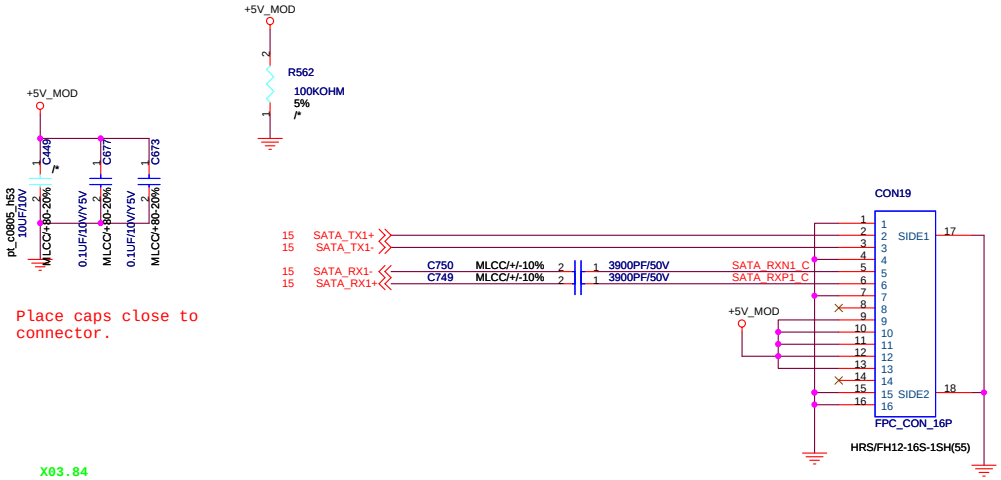


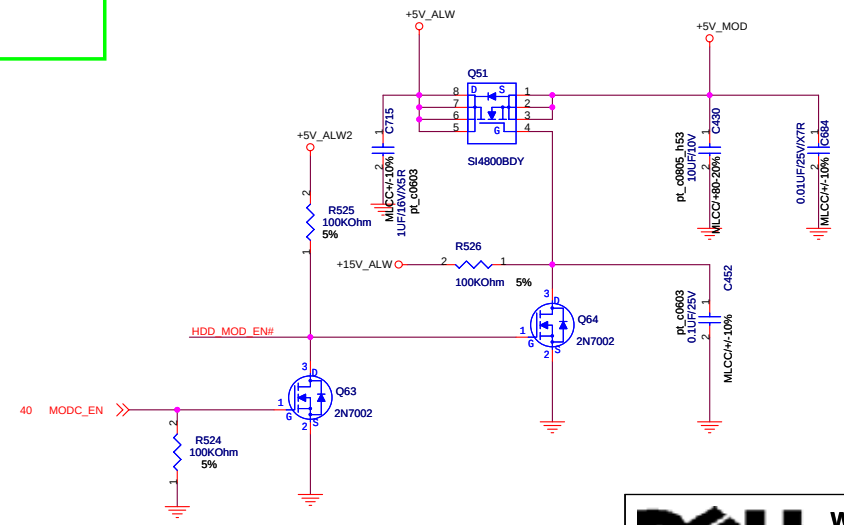
NO.32



X03.84

ODD Connector





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Title: SATA(HDD & CD_ROM)			
Size: Custom	Document Number: Diaz-UMA		Rev: A00
Date: Tuesday, August 19, 2008	Sheet 31 of 68		

Place these caps as close as possible to the device pins.

+3.3V_R5C832
C669 10UF/10V MLCC/+80-20% pt_c0805_h53
C437 0.01UF/16V MLCC/+/-10%
C415 0.01UF/16V MLCC/+/-10%
C446 0.01UF/16V MLCC/+/-10%
C694 0.01UF/16V MLCC/+/-10%
C472 0.01UF/16V MLCC/+/-10%

+3.3V_R5C832
C670 10UF/10V MLCC/+80-20% pt_c0805_h53
C414 0.1UF/10V MLCC/+80-20%
C431 0.01UF/16V MLCC/+/-10%
C420 0.01UF/16V MLCC/+/-10%
C413 0.47UF/10V MLCC/+/-10% pt_c0603
C680 0.01UF/16V MLCC/+/-10%
C707 0.47UF/10V MLCC/+/-10% pt_c0603
C416 0.01UF/16V MLCC/+/-10%

+3.3V_RUN
R363 0Ohm 5% pt_r0603
+3.3V_R5C832

U16B
R5C833_TQFP128
C.S R5C833 TQFP128

VCC_PCI3V_1 10
VCC_PCI3V_2 20
VCC_PCI3V_3 27
VCC_PCI3V_4 32
VCC_PCI3V_5 41
VCC_PCI3V_6 128
VCC_RIN 61
VCC_ROUT1 16
VCC_ROUT2 34
VCC_ROUT3 64
VCC_ROUT4 114
VCC_ROUT5 120

VCC_3V 67
VCC_MD 86
+3.3V_R5C832
C425 0.01UF/16V MLCC/+/-10%
C468 10UF/10V MLCC/+80-20% pt_c0805_h53

GND1 4
GND2 13
GND3 22
GND4 28
GND5 54
GND6 62
GND7 63
GND8 68
GND9 118
GND10 122
AGND1 99
AGND3 102
AGND2 103
AGND4 107
AGND5 111
+3.3V_R5C832
R287 10KOhm 5%

HWSPND# 69
MSEN 58
XDEN 55
UDIO5 57
UDIO3 65
UDIO4 59
UDIO2 56
UDIO1 60
UDIO0/SRIRQ# 72
INTA# 115
INTB# 116
TEST 66

R288 10KOhm 5% +3.3V_R5C832
R289 100KOhm 5% +3.3V_R5C832

Memory Stick Enable
XD Card Enable
Serial ROM disable
SD Card Enable
MMC Card Enable

IRQ_SERIRQ 17,39
PCI_PIRQD# 16 1394 : INTA#
PCI_PIRQC# 16 4in1 : INTB#
Pull-up resistors to +3.3V_RUN are required on the ICH schematics.

X03
T55 TPAD14-GP
R292 100KOhm 5%

PCI / OTHER

PCI_AD31 125 AD31
PCI_AD30 126 AD30
PCI_AD29 127 AD29
PCI_AD28 1 AD28
PCI_AD27 2 AD27
PCI_AD26 3 AD26
PCI_AD25 5 AD25
PCI_AD24 6 AD24
PCI_AD23 9 AD23
PCI_AD22 11 AD22
PCI_AD21 12 AD21
PCI_AD20 14 AD20
PCI_AD19 15 AD19
PCI_AD18 17 AD18
PCI_AD17 18 AD17
PCI_AD16 19 AD16
PCI_AD15 36 AD15
PCI_AD14 37 AD14
PCI_AD13 38 AD13
PCI_AD12 39 AD12
PCI_AD11 40 AD11
PCI_AD10 42 AD10
PCI_AD9 43 AD9
PCI_AD8 44 AD8
PCI_AD7 46 AD7
PCI_AD6 47 AD6
PCI_AD5 48 AD5
PCI_AD4 49 AD4
PCI_AD3 50 AD3
PCI_AD2 51 AD2
PCI_AD1 52 AD1
PCI_AD0 53 AD0

16 PCI_AD[0..31]

16 PCI_PAR PAR 33
16 PCI_C_BE3# C/BE3# 7
16 PCI_C_BE2# C/BE2# 21
16 PCI_C_BE1# C/BE1# 35
16 PCI_C_BE0# C/BE0# 45
16 PCI_AD17 PCI_AD17 IDSEL 8
R580 1 2 100Ohm 5% R5C832_IDSEL

16 PCI_REQ1# REQ# 124
16 PCI_GNT1# GNT# 123
16 PCI_FRAME# FRAME# 23
16 PCI_IRDY# IRDY# 24
16 PCI_TRDY# TRDY# 25
16 PCI_DEVSEL# DEVSEL# 26
16 PCI_STOP# STOP# 29
16 PCI_PERR# PERR# 30
16 PCI_SERR# SERR# 31

Pull-up resistors to +3.3V_RUN are required on the ICH schematics.

GBRST# 71
16 PCI_RST# PCIRST# 119
PCICLK 121
21 CLK_PCI_PCCARD
Route to CLK GEN .

40 SYS_PME# R308 1 2 0 OHM 5% /* PME# 70
Pull-up to +3.3V_ALW is required on SYS_PME# on EC schematics. (From EC). 0 ohm of PME# is no-stuff to prevent backdrive from this signal since the controller is powered of the RUN rail

17,39 CLKRUN# R566 1 2 0Ohm 5% CLKRUN# 117
The ICH schematics need to include a pull-up resistor to implement CLKRUN#, and the ICH schematics must have a pull-down, or constantly drive the signal low, in order to disable CLKRUN#.
R571 10K OHM 5% /*

It may need to be fine tuned value of RC.
+3.3V_R5C832
R294 100KOhm 5%
17,39,54,58 IMVP_PWRGD R6944 1 2 0 OHM 5% /*
C423 1UF/10V/X7R MLCC/+/-10% pt_c0603

Reserve for EMI
R361 10 OHM 5% /*
C471 10PF/50V MLCC/+/-0.5PF /*

Ricoh R5C832 Package Type : TQFP-128-P1 (1414)

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Title: R5C833 - PCI INTERFACE
Size: Custom | Document Number: Diaz-UMA | Rev: A00
Date: Tuesday, August 19, 2008 | Sheet 32 of 68

Recommended Crystal Specs from Data Sheet:

Normal Frequency : 24.576 MHz
Frequency Tolerance : +/- 50ppm @ 25C
Driver Level : .1 mW
Load capacitance : 10pF
Equ. Resistance : 50 Ohm Max
Shunt Capacitance : 7.0pF Max

X01
NO.27

C454 22PF/50V MLCC/+/-5%
X4 24.576Mhz +/-30ppm/16PF
C453 22PF/50V MLCC/+/-5%
R342 0Ohm 5%
1394_XI
1394_XO

C463 0.01UF/16V MLCC/+/-10%
R576 10KOhm 1%
C469 0.01UF/16V MLCC/+/-10%
RICHO_FILO
RICHO_REXT
RICHO_VREF

Place as close to R5C832 as possible.

U16A
IEEE1394/SD
R5C833_TQFP128
C.S R5C833 TQFP128

+3.3V_RUN_PHY
AVCC_PHY3V_1 98
AVCC_PHY3V_2 106
AVCC_PHY3V_3 110
AVCC_PHY3V_4 112

+3.3V_RUN_CARD
C662 0.01UF/16V MLCC/+/-10%
C661 0.01UF/16V MLCC/+/-10%
C663 0.01UF/16V MLCC/+/-10%
R530 150KOhm 5%
Place these components close to the flash memory card connector

TPBIAS0 113 TPBIAS0 34
TPBN0 104 TPB0N 34
TPBP0 105 TPB0P 34
TPAN0 108 TPA0N 34
TPAP0 109 TPA0P 34

XI 94
XO 95
FIL0 96
REXT 101
VREF 100
RSV 97

MDIO17 87 XD_DATA7
MDIO16 92 XD_DATA6
MDIO15 89 XD_DATA5
MDIO14 91 XD_DATA4
MDIO13 90 SD/XD/MS_DATA3
MDIO12 93 SD/XD/MS_DATA2
MDIO11 81 SD/XD/MS_DATA1
MDIO10 82 SD/XD/MS_DATA0
MDIO05 75 XD_WP#
MDIO08 88 SD/XD/MS_CMD
MDIO19 83 XD_ALE
MDIO18 85 XD_CLE
MDIO02 78 XD_CE#
MDIO03 77 SD_WP#(XDR/B#)
MDIO00 80
MDIO01 79
MDIO09 84
MDIO04 76 MC_PWR_CTRL_0
MDIO06 74 MS_LED#
MDIO07 73

SD_CD#
D20 1N4148W-7-F
D19 1N4148W-7-F
XD_CDSW#
MS_INS#
A00.No 97
R545 33R2F-3-GP SD/XD/MS_CLK
X03
T153 TPAD14-GP
C757 /* 10PF/50V MLCC/+/-0.5PF

For SD/MS Card Power

+3.3V_R5C832
+3.3V_RUN_CARD
U26 TPS2051BDBVR (GND, OC#, EN, IN, OUT)
MC_PWR_CTRL_0
C660 0.1UF/10V MLCC/+80-20%
C659 1UF/10V MLCC/+80%-20% pt_c0603

+3.3V_RUN_CARD
C668 2.2UF/16V MLCC/+/-10% pt_c0603
SD/XD/MS_CMD

CON20
TAISOL/144-2400000900
CARD_READER_41P

XD_0(GND) 41
XD_1(CD) 40 XD_CDSW#
XD_2(R/-B) 39 SD_WP#(XDR/B#)
XD_3(-RE) 38 SD/XD/MS_CLK
XD_4(-CE) 37 XD_CE#
XD_5(CLE) 36 XD_CLE
XD_6(ALE) 34 XD_ALE
XD_7(-WE) 31 SD/XD/MS_CMD
XD_8(-WP) 27 XD_WP#
XD_9(GND) 23
XD_10(D0) 19 SD/XD/MS_DATA0
XD_11(D1) 15 SD/XD/MS_DATA1
XD_12(D2) 12 SD/XD/MS_DATA2
XD_13(D3) 11 SD/XD/MS_DATA3
XD_14(D4) 9 XD_DATA4
XD_15(D5) 7 XD_DATA5
XD_16(D6) 6 XD_DATA6
XD_17(D7) 5 XD_DATA7
XD_18(VCC) 4
MS_1(VSS) 14
MS_2(BS) 16
NP_NC1 42
NP_NC2 43
P_GND1 44
P_GND2 45

MS_3(DATA1) 18 SD/XD/MS_DATA1
MS_4(DATA0) 20 SD/XD/MS_DATA0
MS_5(DATA2) 22 SD/XD/MS_DATA2
MS_6(INS) 24 MS_INS#
MS_7(DATA3) 26 SD/XD/MS_DATA3
MS_8(SCLK) 28 SD/XD/MS_CLK
MS_9(VCC) 30
MS_10(VSS) 32
SD_1(DAT3) 33 SD/XD/MS_DATA3
SD_2(CMD) 29 SD/XD/MS_CMD
SD_3(VSS) 25
SD_4(VDD) 21
SD_5(CLK) 17 SD/XD/MS_CLK
SD_6(VSS) 13
SD_7(DAT0) 10 SD/XD/MS_DATA0
SD_8(DAT1) 8 SD/XD/MS_DATA1
SD_9(DAT2) 35 SD/XD/MS_DATA2
SD(CD2/WP2/GND) 1
SD(CD1) 2 SD_CD#
SD(WP1) 3 SD_WP#

Q76 2N7002 /*
SD_WP#(XDR/B#)
XD_CDSW#
SD_WP# R3301 0Ohm 5% SD_WP#(XDR/B#)

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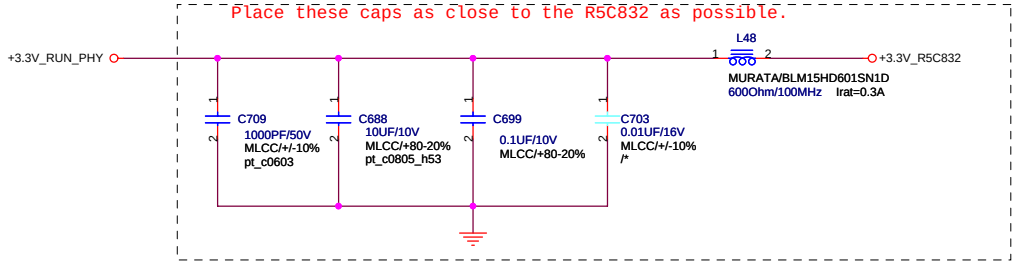
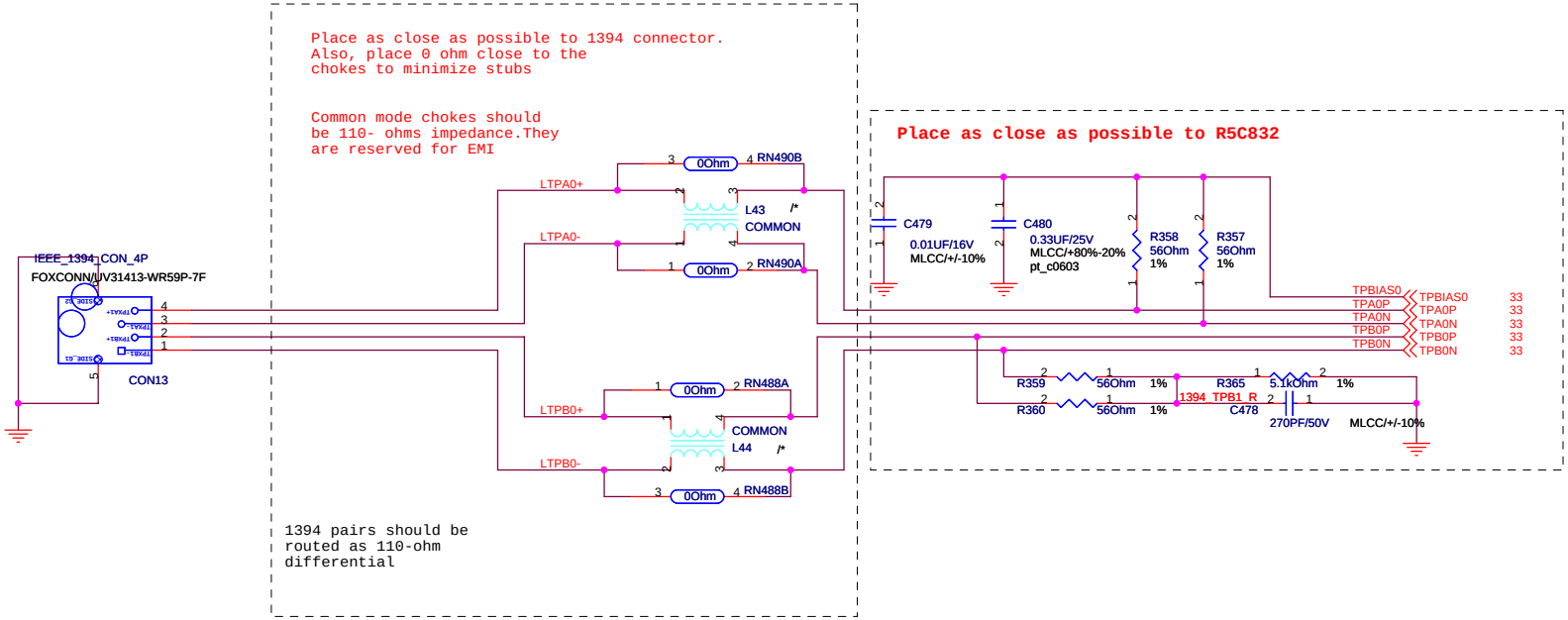
Title: R5C833 - FLASH MEMORY PART			
Size: Custom	Document Number: Diaz-UMA	Rev: A00	
Date: Tuesday, August 19, 2008	Sheet 33 of 68		





(20071005)for choke & 0ohm colayout

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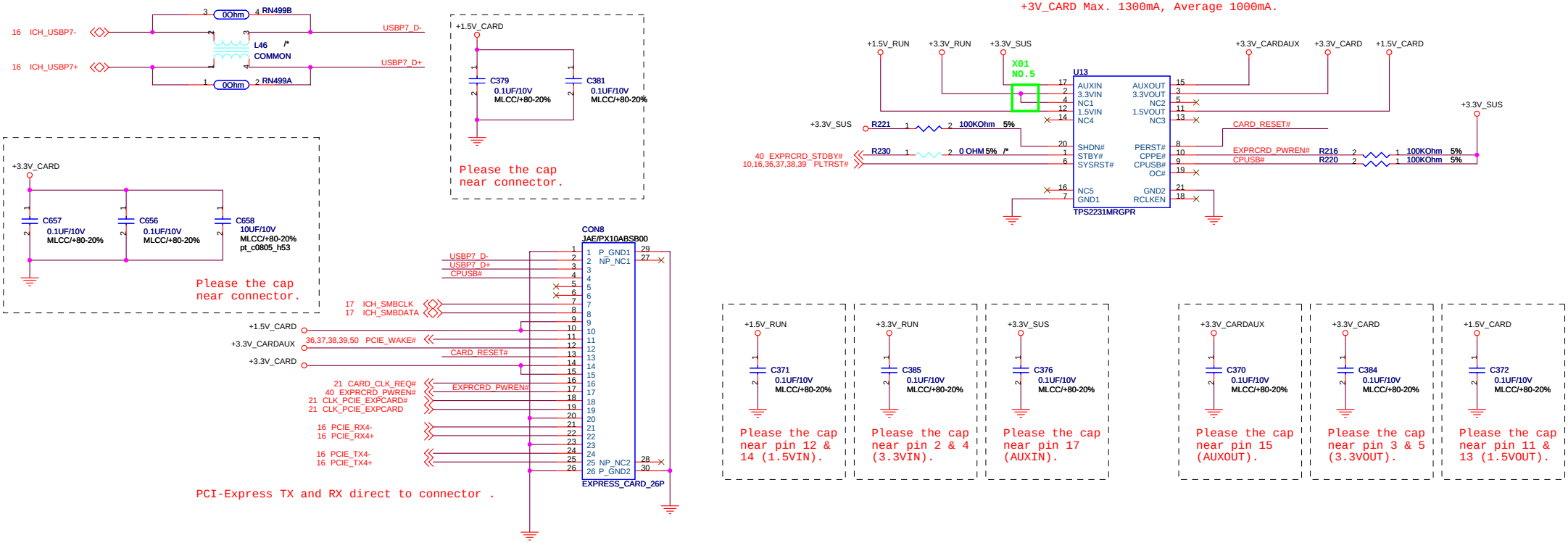
Title: R5C833 - IEEE1394 PART		
Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 34 of 68	

Express Card



+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

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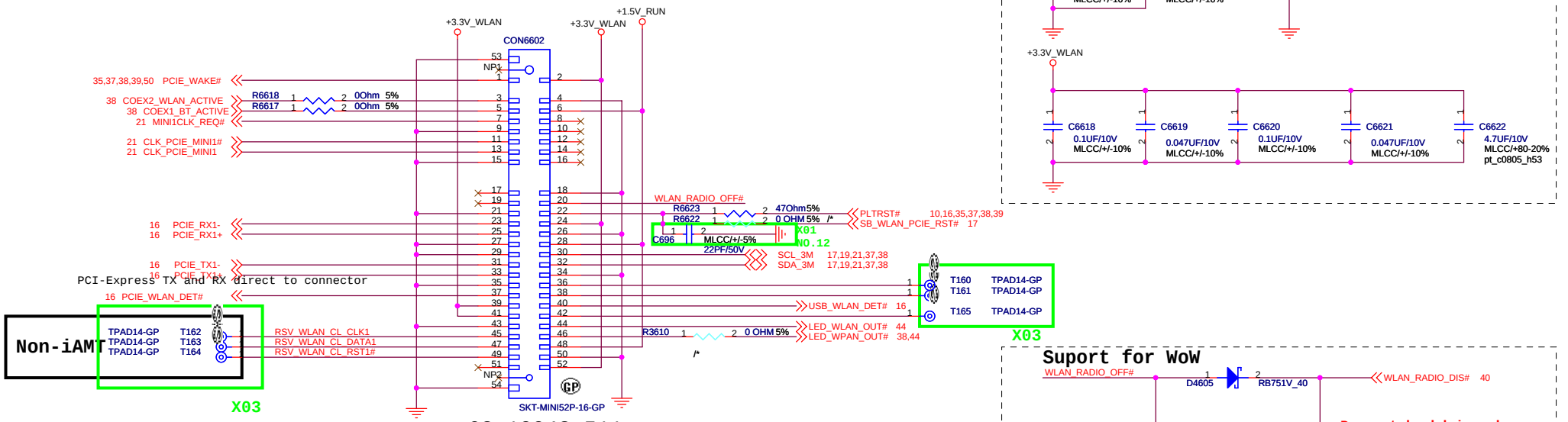
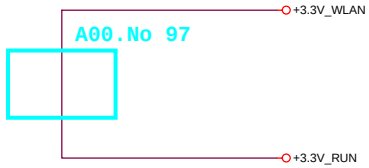
Title: PCI-Express Card		
Size: Custom	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 35 of 68	



DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



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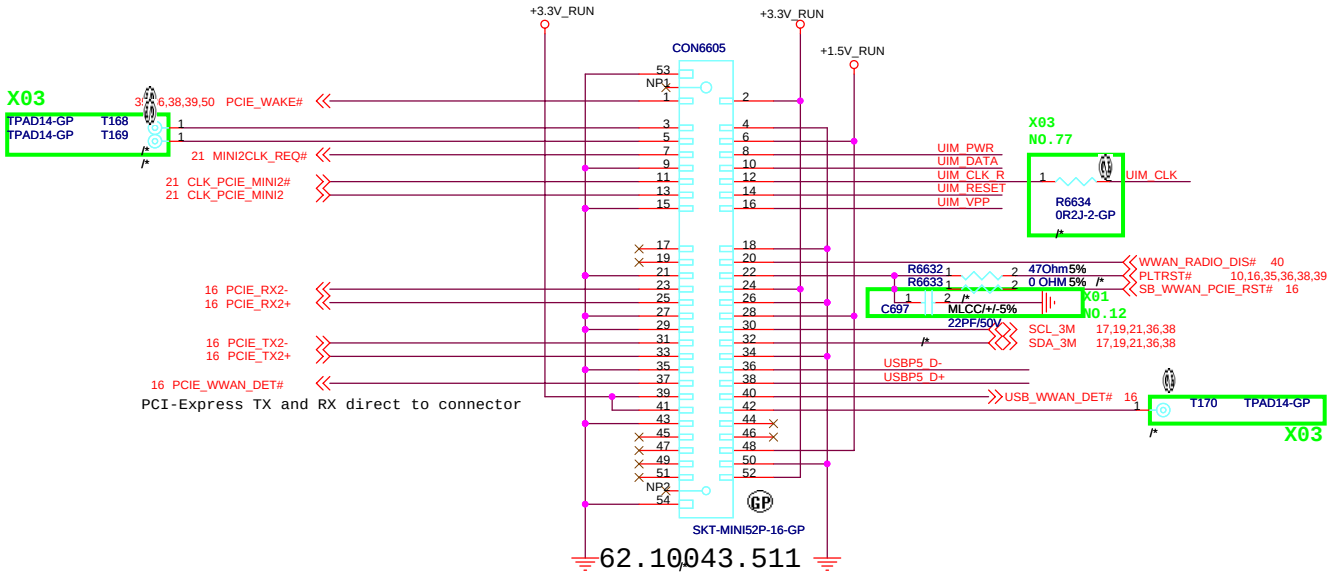
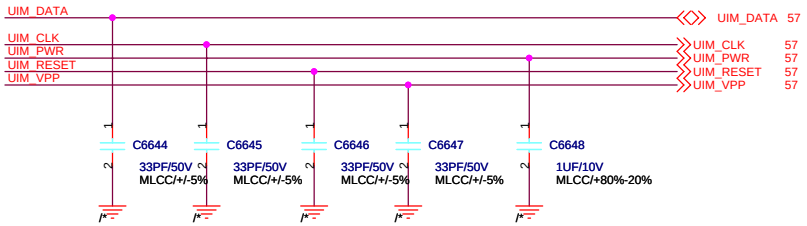
Title: MINI CARD - Kedron

Size: A3 | Document Number: Diaz-UMA | Rev: A00

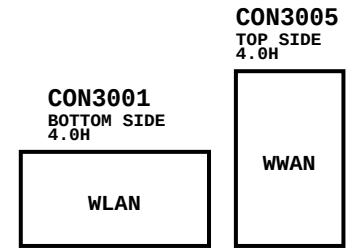
Date: Tuesday, August 19, 2008 | Sheet 36 of 68

MiniCard WWAN connector

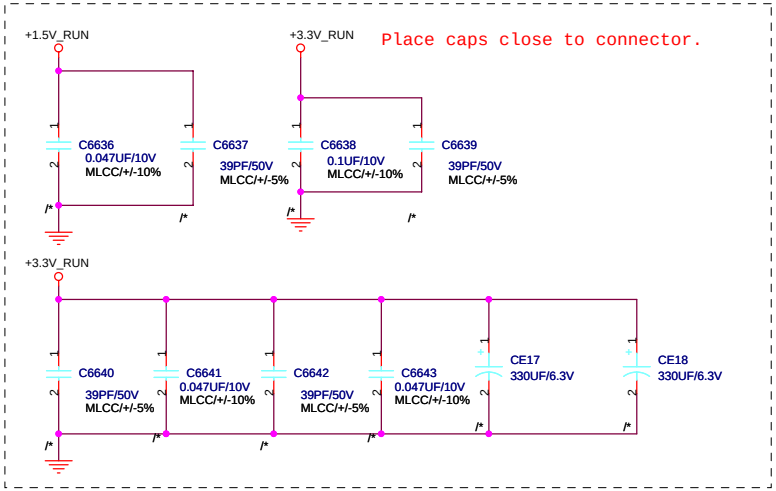


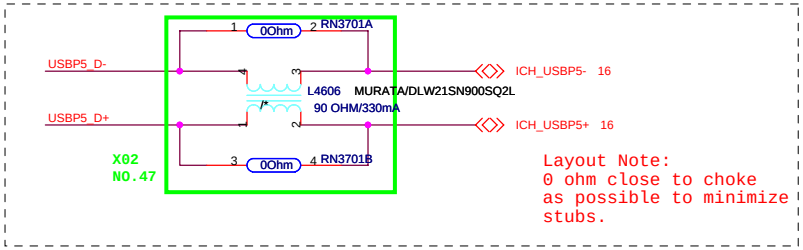


MiniCard Relative Location (TOP VIEW):



MiniCard * 2 Absolutely Location (TOP VIEW):
Upper / Right side on MB





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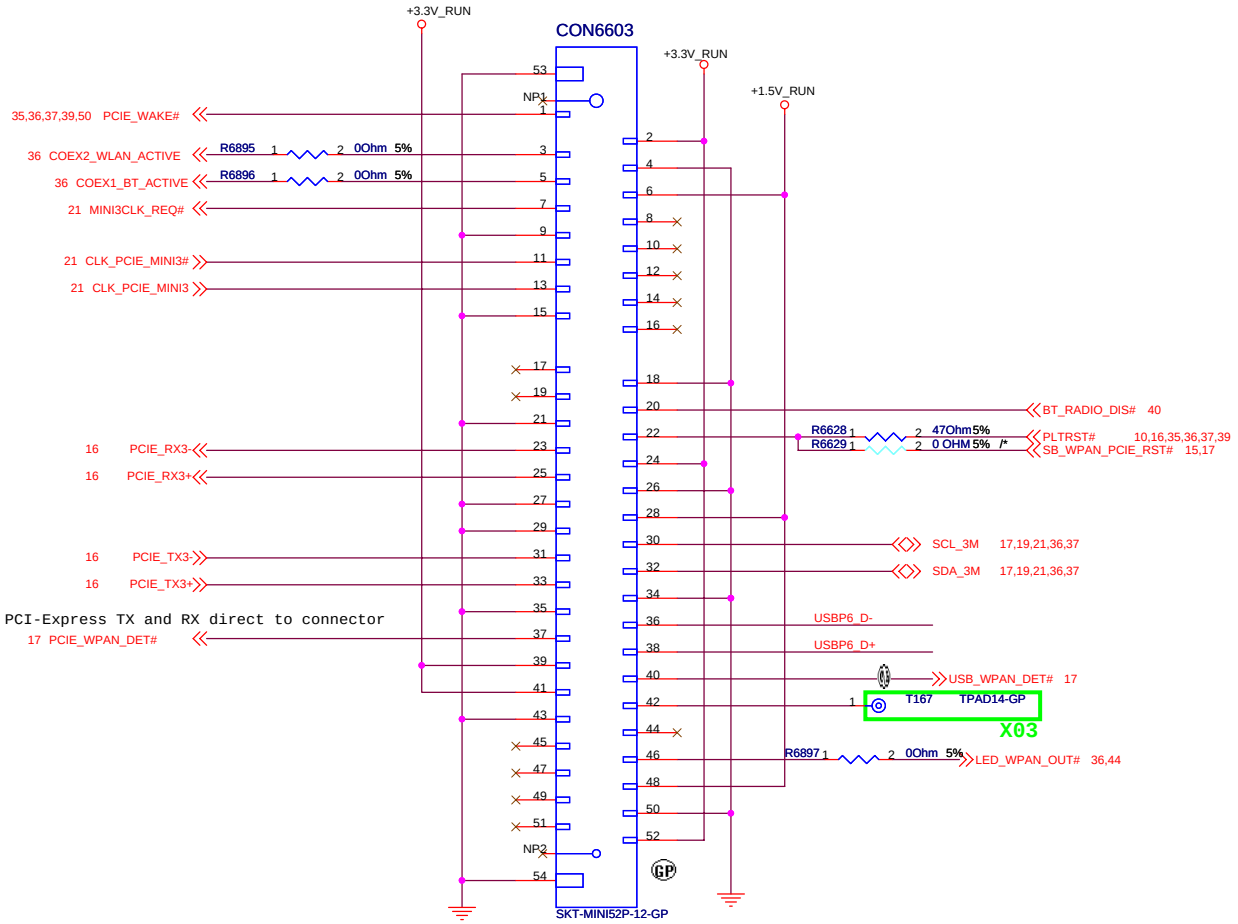
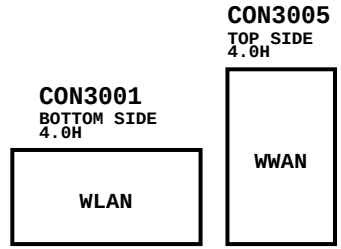
Title	MINI CARD - Robson	
Size A3	Document Number Diaz-UMA	Rev A00
Date: Tuesday, August 19, 2008	Sheet 37 of 68	

MiniCard WPAN connector

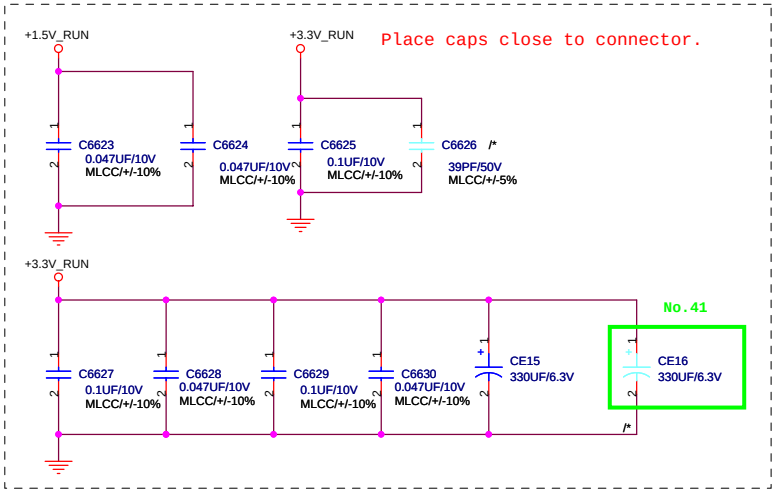


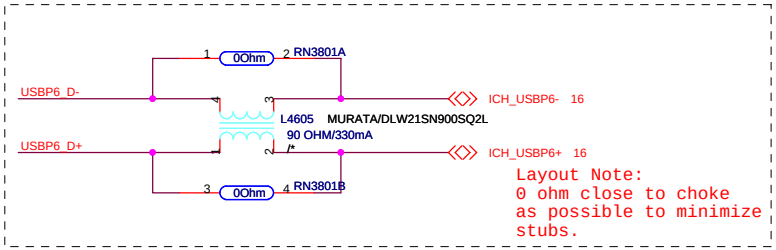
62.10043.441

MiniCard Relative Location (TOP VIEW):



MiniCard * 2 Absolutely Location (TOP VIEW):
Upper / Right side on MB





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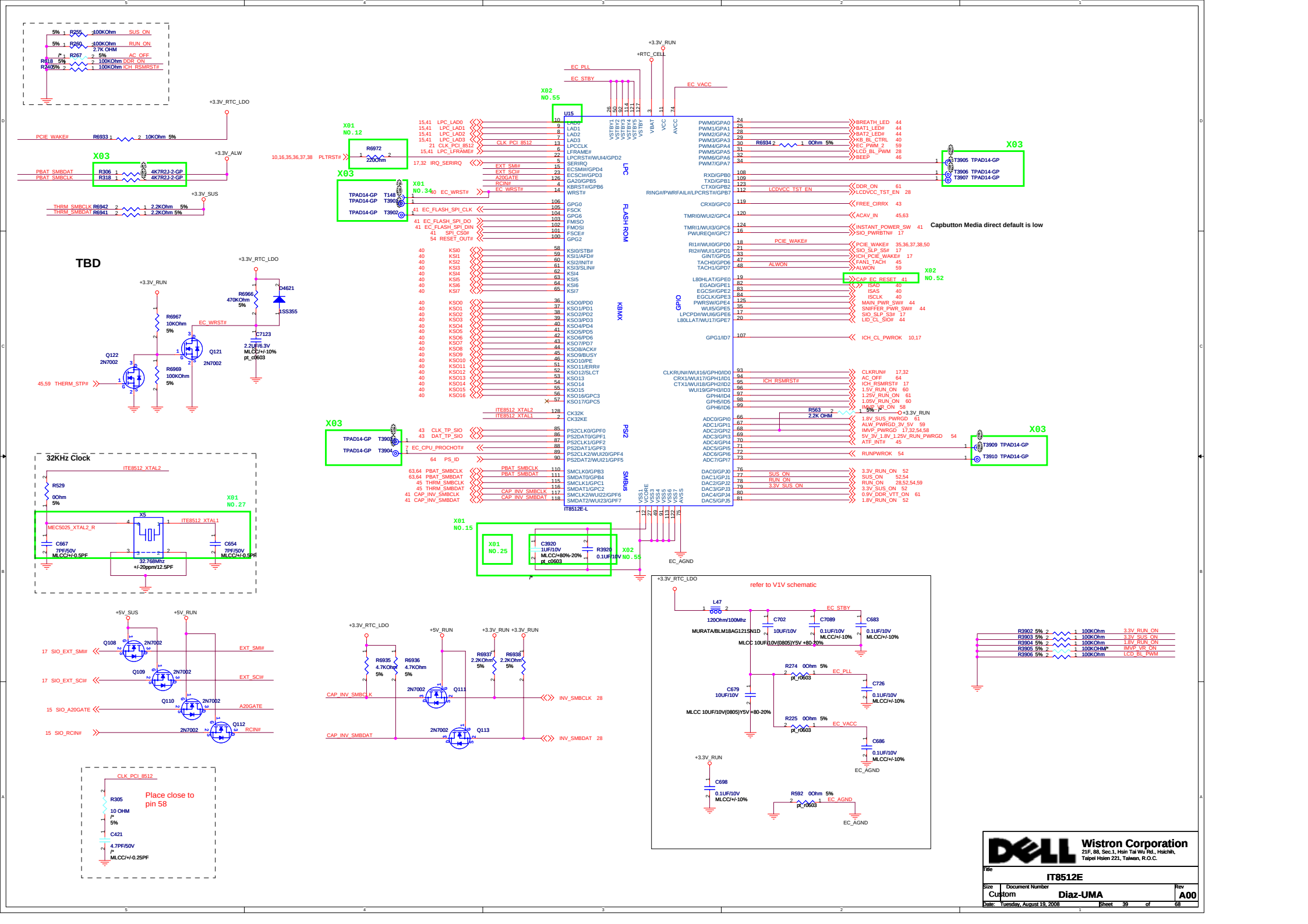
Title: MINI CARD - Robson		
Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 38 of 68	


IT8512E
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Size: Custom
Document Number: Diaz-UMA
Rev: A00
Date: Tuesday, August 19, 2008
Sheet 39 of 68
TBD
32KHz Clock
Capbutton Media direct default is low
refer to V1V schematic
Place close to pin 58
U15
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS2
SMBus

VGA_IDENTIFY
1 = Discrete Gfx.
0 = UMA

Board ID Straps

Discrete

X03.85

+3.3V_RTC_LDO

X03
No.43

R541 10K OHM 5%

R537 DY /* 10K OHM 5%

R535 DY /* 10KOhm 5%

BID0

BID1

VGA_IDENTIFY

R542 10KOhm 5%

R536 10KOhm 5%

R534 10K OHM 5%

UMA

BID1	BID0	M/B VER
0	0	A00
0	1	A01
1	0	A02
1	1	A03

R568 100KOhm 5% LCD_TST
R328 100KOhm 5% PANEL_BKEN
R4020 1M OHM 5% /* EC_LCD_BKEN

+3.3V_RTC_LDO

C7105 0.1UF/10V MLCC/+/-10%

U29

ISAD
ISCLK
R229 100KOhm 5%
R226 100KOhm 5%
EC_WRST#
SYS_PME#
USB_RSIDE_EN#
USB_LSIDE_EN#
NB_MUTE#
ADAPT_OC
ADAPT_TRIP_SEL
XDP_DBRESET#
PS_ID_DISABLE#
PANEL_BKEN
SNIFFER_WHITE
BID0
HDDC_EN
HDDC_EN
MODC_EN
BID1
LOM_LOW_PWR
LOM_LOW_PWR

VSS1 GPIO_DATA CYCLE_START GPIO_CLK CHIP_SEL1 CHIP_SEL0 RESET# GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 VSS2

VSTBY1 GPIO16 GPIO17 GPIO18 GPIO19 GPIO20 GPIO21 GPIO22 GPIO23 GPIO24 GPIO25 GPIO26 GPIO27 GPIO28 GPIO29 GPIO30 GPIO31 GPIO32 GPIO33 GPIO34 GPIO35 GPIO36 GPIO37 VSTBY2

IT8301E

LED_MASK# 44
R241 0Ohm 5%
SIO_EXT_WAKE# 17
ICH_PME# 16
WLAN_RADIO_DIS# 36
WIRELESS_ON/OFF# 44
BT_RADIO_DIS# 38
WWAN_RADIO_DIS# 37
EXPRCRD_PWREN# 35
EXPRCRD_STDBY# 35
EC_LCD_BKEN 28
LCD_TST 28

X03
T4001 TPAD14-GP

PLATFORM_ID0
PLATFORM_ID1
X01 NO.17
NUM_LED#
CAP_LED#
INT_KB_DET#
BID2
X03.85
T4002 TPAD14-GP

INVERTER_CBL_DET# 28
LCD_CBL_DET# 28
VGA_IDENTIFY

+3.3V_RTC_LDO

C7106 0.1UF/10V MLCC/+/-10%

R106 LED_BL_DET — LED_BL_DET_CON DY 10KR2F-2-GP

R158 /* 20KR2F-L-GP DY

LED Connector

+5V_RUN

C4001 22UF/10V

F4001 0.5A

L4001 180Ohm

+5V_KB_BL

C4002 0.1UF/16V

X01 NO.19

LED_BL_DET_CON

FPC_CON_4P SIDE1 SIDE2 CON4010

KB_BL_CTRL#

+3.3V_RUN

R4018 /* 100KOHM

39 KB_BL_CTRL

R4019 100KOhm

U4001 FDC653N_NL

X03

+5V_KB_BL

KB_BL_CTRL#

T528 AFTE14P-GP
T529 AFTE14P-GP

For AFTE test Close to CON4010

+3.3V_RUN

R6943 10KOhm
R324 200KOhm 5%
R304 200KOhm 5%
R4011 200KOhm 5%

INT_KB_DET#
INVERTER_CBL_DET#
LCD_CBL_DET#
SYS_PME#

+5V_RUN +5V_RUN

R4012 100KOhm 5%
R4013 10KOhm 5%

Q4010 2N7002
Q4011 PMBS3906

+3.3V_RUN

R4014 330Ohm

NUM_LED#
NUM_LED_R

X01
NO.17
NO.26

PLATFORM_ID0
PLATFORM_ID1

R4026 10KOhm 5%
R4028 10KOhm 5%

ID1	ID0	PLATFORM
0	0	INTEL SR
0	1	INTEL MV
1	0	AMD

+5V_RUN +5V_RUN

R4016 100KOhm 5%
R4017 10KOhm 5%

Q4012 2N7002
Q4013 PMBS3906

+3.3V_RUN

R4015 330Ohm

CAP_LED#
CAP_LED_R

Keyboard Connector

CON5 FPC_CON_30P SIDE1 SIDE2

INT_KB_DET#
KSI7 KSI6 KSI4 KSI2 KSI5 KSI1 KSI3 KSI0 KSO5 KSO4 KSO7 KSO6 KSO8 KSO3 KSO1 KSO2 KSO0 KSO12 KSO16 KSO15 KSO13 KSO14 KSO9 KSO11 KSO10
CAP_LED_R
NUM_LED_R

X01 NO.16

33PF/50V

X03

T500 T501 T502 T503 T504 T505 T506 T507 T508 T509 T510 T511 T512 T513 T514 T515 T516 T517 T518 T519 T520 T521 T522 T523 T524 T525 T526 T527 AFTE14P-GP

For AFTE test Close to CON5

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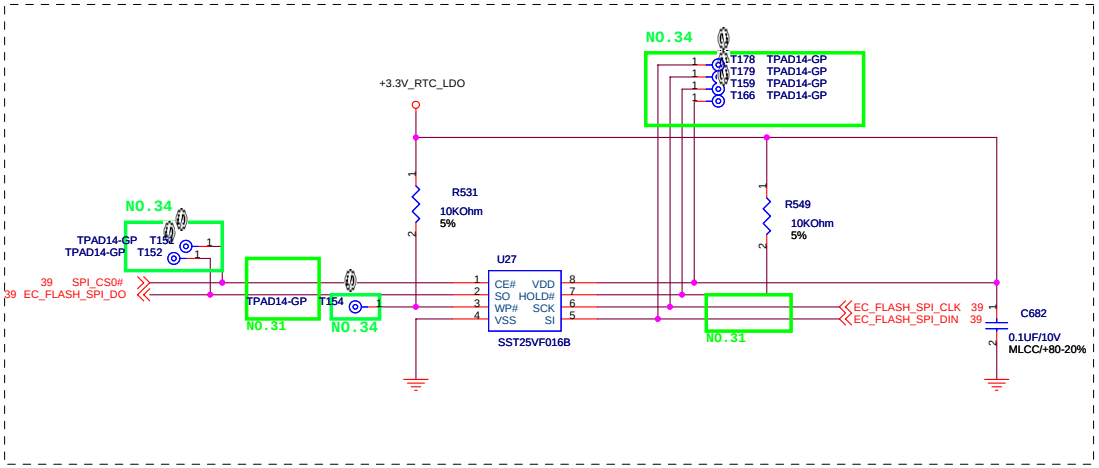
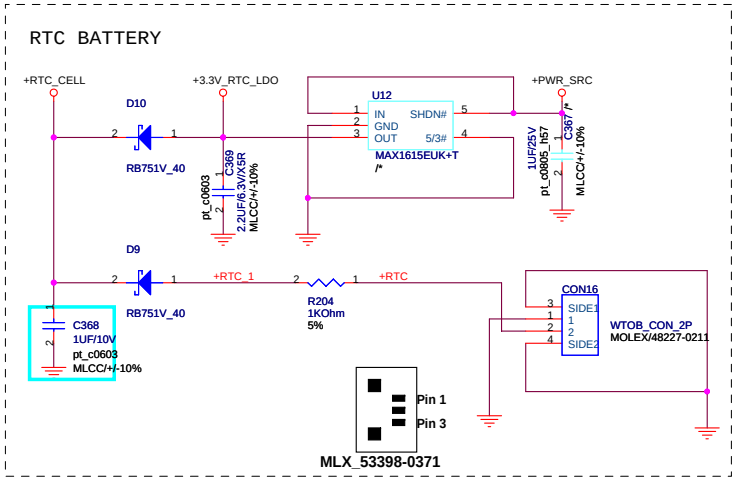
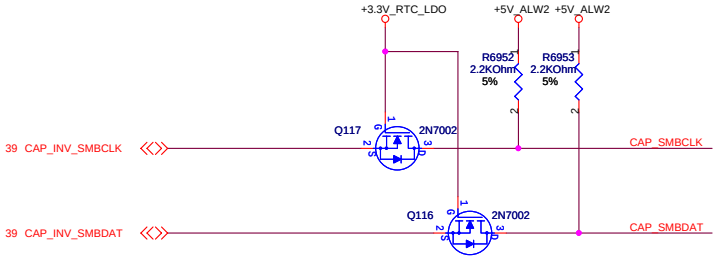
Title: IT8301E

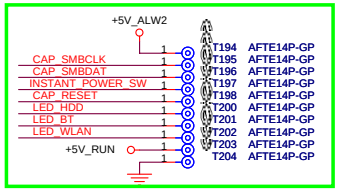
Size: Custom | Document Number: Diaz-UMA | Rev: A00

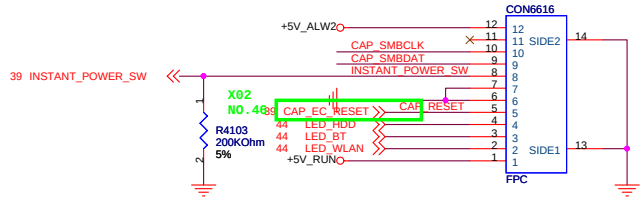
Date: Tuesday, August 19, 2008 | Sheet 40 of 68



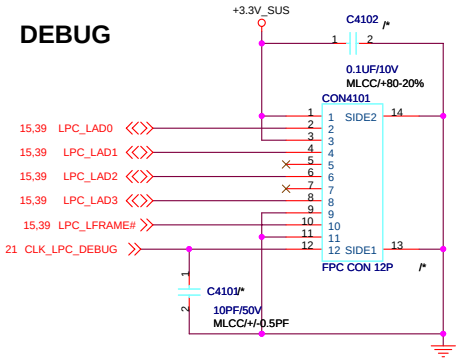








CAPBTN CON.



Note:
+5V_ALW2 => for Capbutton PSOC and Media direct LED only.
+5V_RUN => for Capbutton LED and Photo sensor.

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Title: FLASH & RTC

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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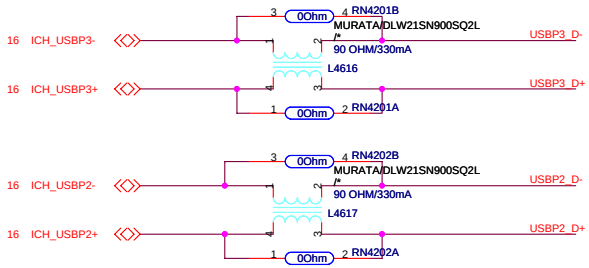
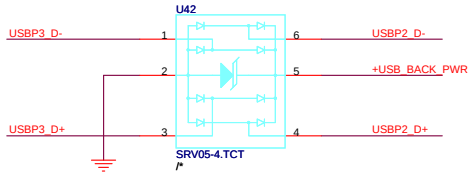
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

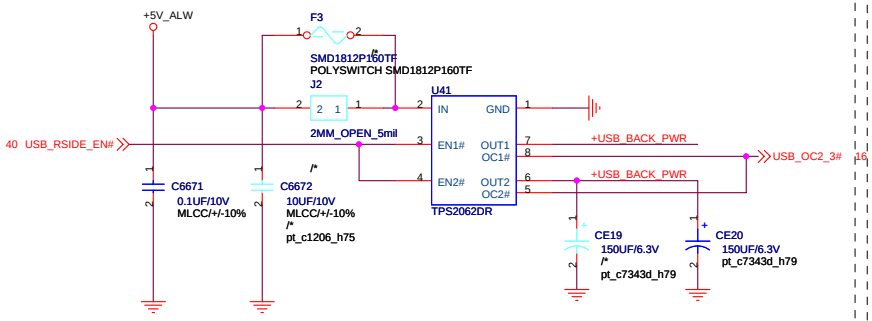


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

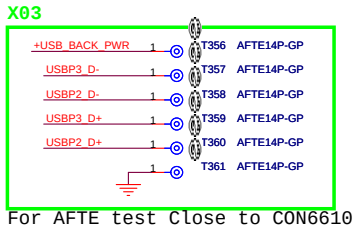
Place one 150uF cap by each USB connector



Each channel is 1A

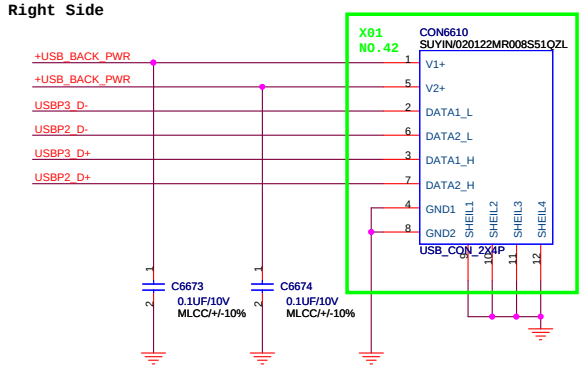
Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines. Add PADS ONLY until proven diodes are really needed.

X03



For AFTE test Close to CON6610

Right Side



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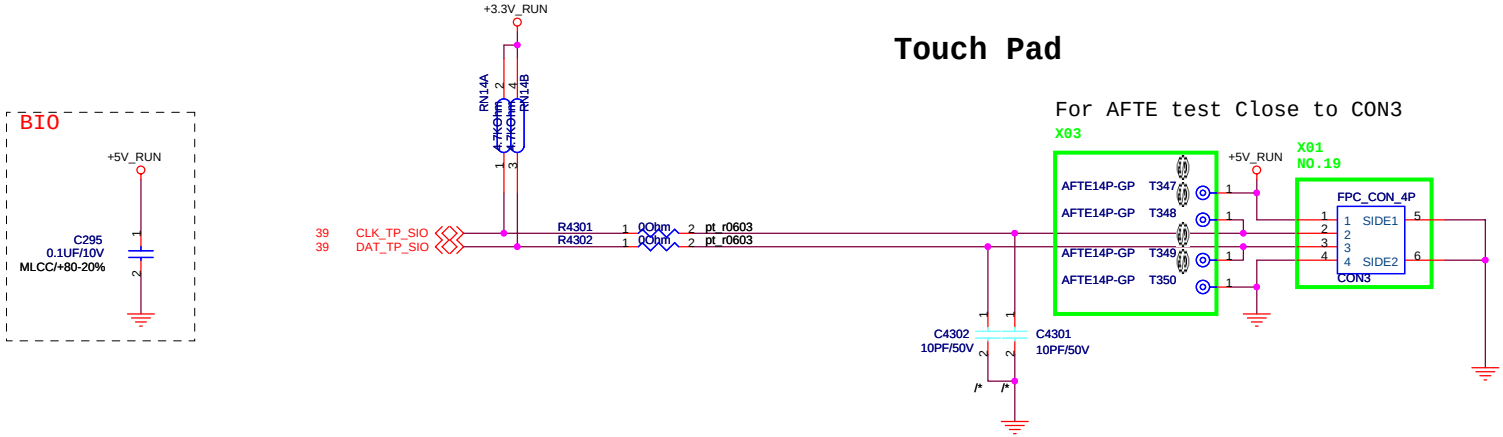
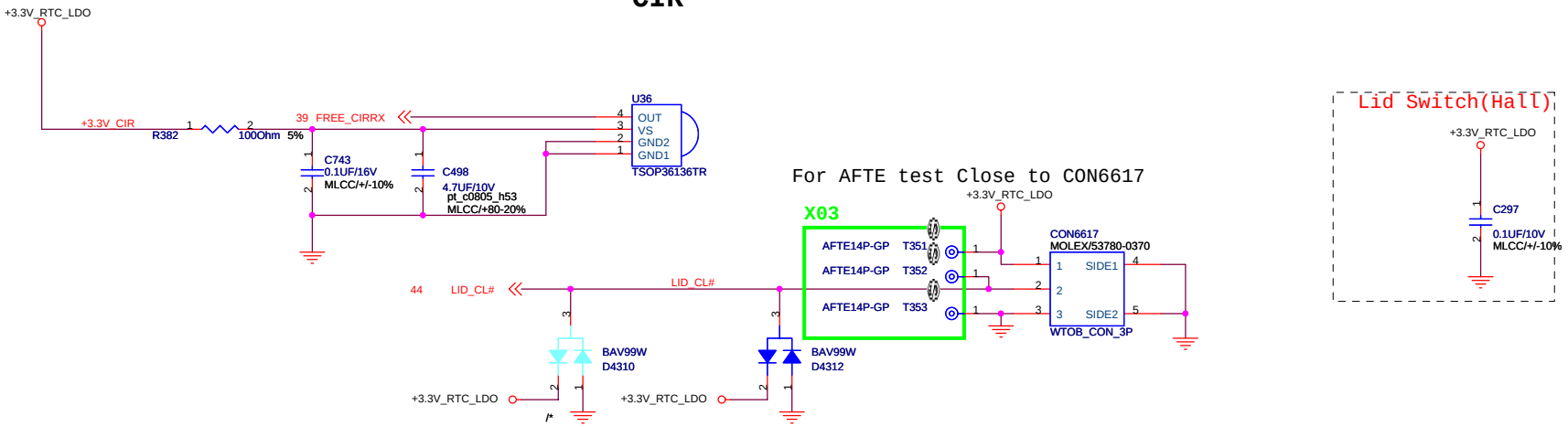
Title: USB PORT x 2			
Size: Custom	Document Number: Diaz-UMA		Rev: A00
Date: Tuesday, August 19, 2008	Sheet 42 of 68		

Touch Pad



CIR



HALL SENSOR

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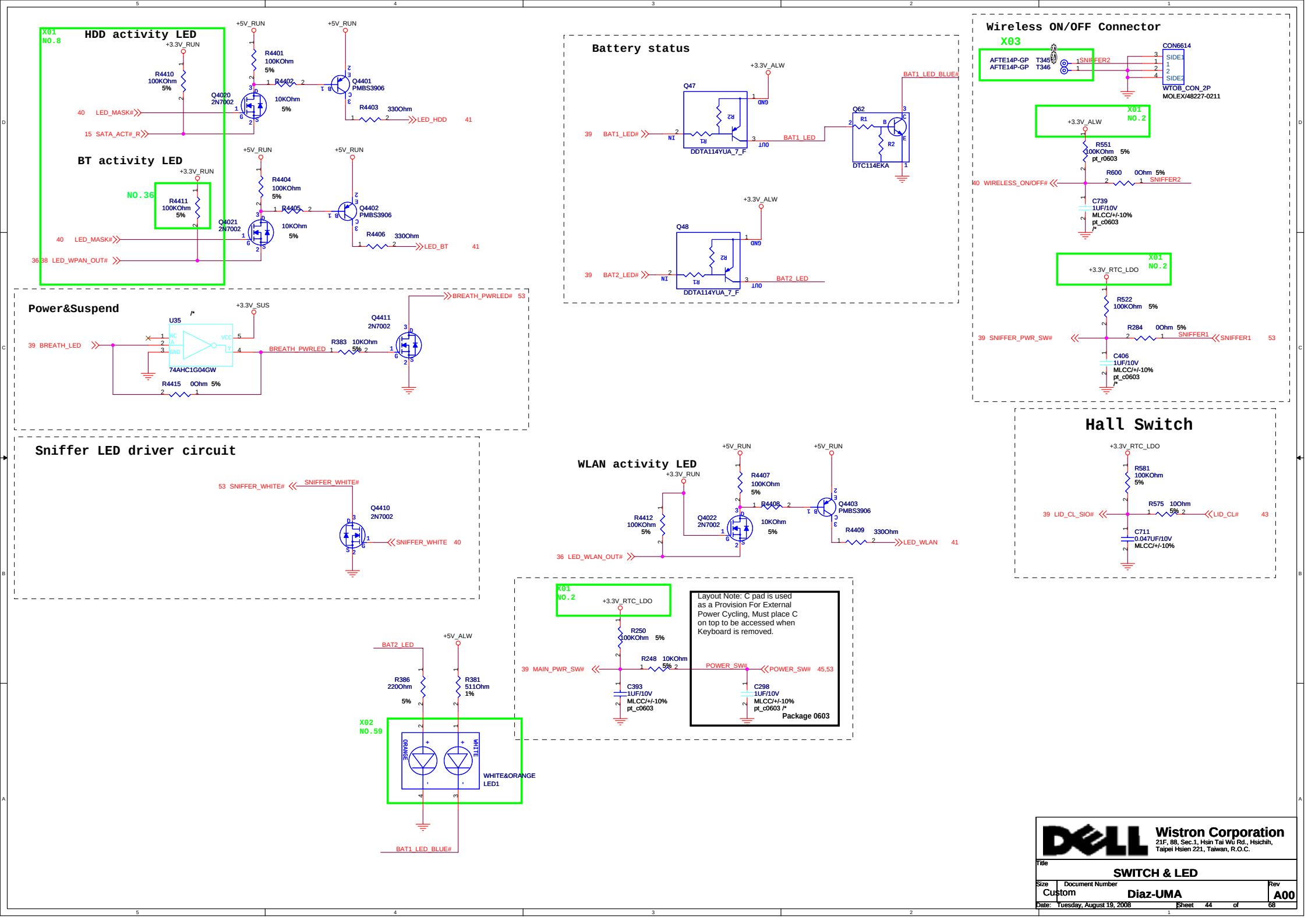
Title: TOUCH PAD & BT & CIR & LID		
Size: A3	Document Number: Diaz-UMA	Rev: A00
Date: Tuesday, August 19, 2008	Sheet 43 of 68	



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Title: SWITCH & LED

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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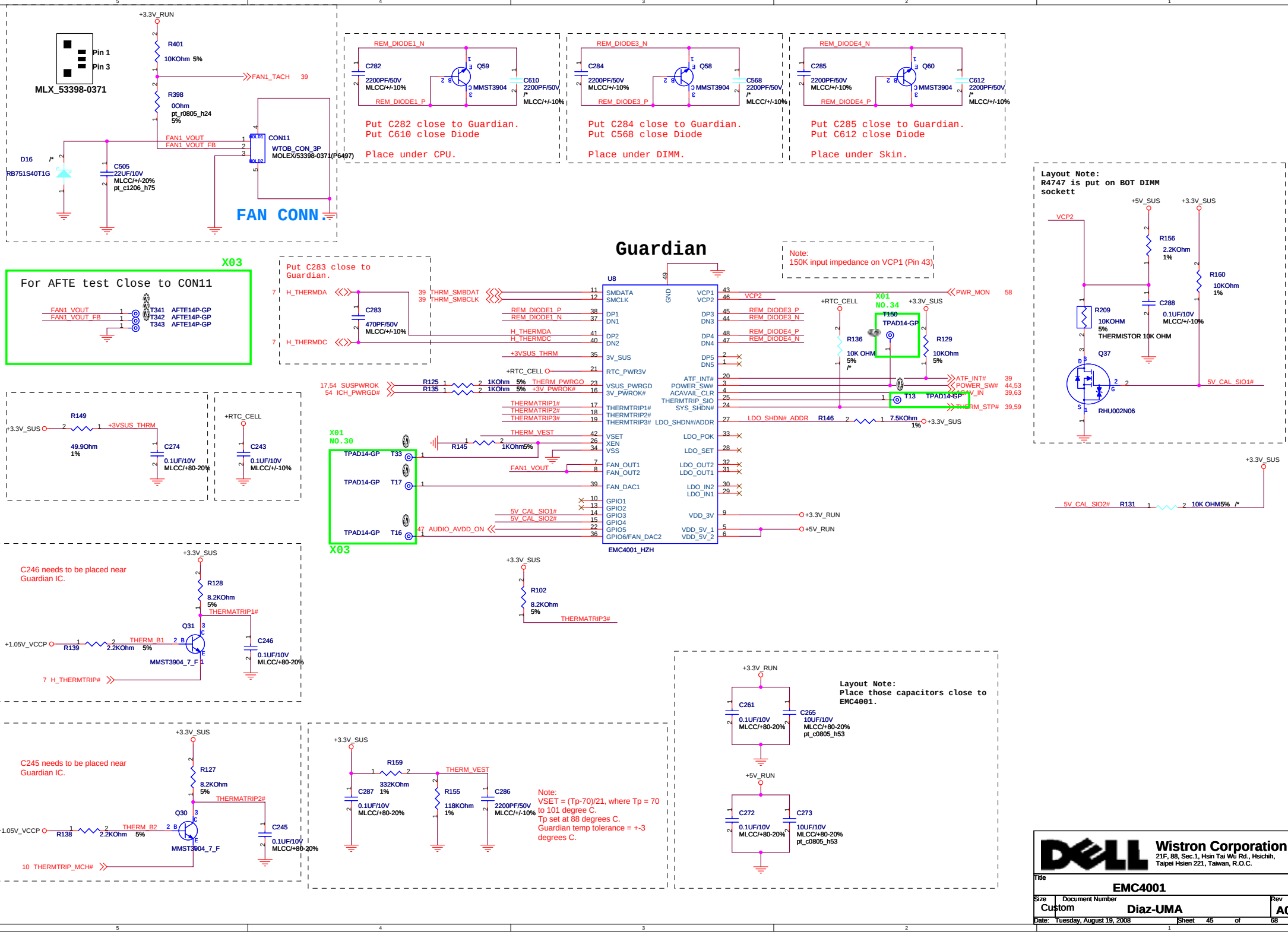

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Title: EMC4001

Size	Document Number	Rev
Custom	Diaz-UMA	A00

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Port A---> HP2
Port E---> HP1
Port B---> INT MIC
Port F---> ext Mic
Port D---> Speaker

FROM ICH
17 SPKR
39 BEEP
FROM EC
U17
SN74AHCT1G86DCKR
VDDA
MLCC/+/-10%
C457 0.1UF/16V/X7R
R335 47KOhm
MLCC/+/-10%
C448 0.1UF/16V/X7R
AUD_PC_BEEP
R336 4.7KOhm

MURATA/BLM18EG601SN1D
Irat=500mA
L4601 600Ohm/100Mhz
+3.3V_RUN
C693 0.1UF/10V
C687 0.1UF/10V
C444 10UF/10V pt_c0805_h53
DVDD_CORE

U18
ALC888-GR
DVDD
DVDD_IO
JDREF
BCLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
GPIO0/DMIC_CLK
GPIO1/DMIC_DATA
SPDIF/EAPD
SPDIFO
DVSS1
DVSS2
AVDD1
AVDD2
SenseA
SenseB
PCBEEP
NC
VREF
AVSS1
AVSS2

R6957 20KOhm 1%
15 ICH_AZ_CODEC_BITCLK
R557 33Ohm 5% HDA_SDI
15 ICH_AZ_CODEC_SDIN0
15 ICH_AZ_CODEC_SDOUT
15 ICH_AZ_CODEC_SYNC
15 ICH_AZ_CODEC_RST#

VDDA
AVDD_CODEC
C724 10UF/10V pt_c0805_h53
C7115 10UF/10V pt_c0805_h53
C722 0.1UF/10V
C723 0.1UF/10V

AUD_SENSE_A
AUD_SENSE_B

R345 39.2KOhm 1%
Q50 2N7002
48,49 AUD_HP2_NB_SENSE

X02
NO.58
R559 20KOhm 1%
R553 39.2KOhm 1%
49 AUD_MIC_SWITCH#
Q67 2N7002
47,49 AUD_HP1_NB_SENSE

NO.28
+3.3V_RUN
+1.5V_RUN
R4601 100KOhm
R6958 10KOhm
Q123 PMBS3904
R4602 0Ohm /*
47,48 AUD_EAPD#

28 AUD_DMIC_CLK
28 AUD_DMIC_IN0

FRONT_L(Port_D)
FRONT_R(Port_D)
LINE2_L(Port_E_L)
LINE2_R(Port_E_R)
LINE2_VREFO
MIC2_L(Port_F_L)
MIC2_R(Port_F_R)
MIC2_VREFO
CENTER(Port_G_L)
LFE(Port_G_R)
SIDE_L(Port_H_L)
SIDE_R(Port_H_R)
CD_L
CD_GND
CD_R
PIN37_VREFO
MIC1_L(Port_B_L)
MIC1_R(Port_B_R)
MIC1_VREFO_L
MIC1_VREFO_R
LINE1_L(Port_C_L)
LINE1_R(Port_C_R)
LINE1_VREFO
SURR_L(Port_A_L)
SURR_R(Port_A_R)

AUD_HP2_OUT_L 48
AUD_HP2_OUT_R 48
AUD_LINE_OUT_L 47
AUD_LINE_OUT_R 47
AUD_HP1_OUT_L 47
AUD_HP1_OUT_R 47
AUD_INT_MIC_OP 48
AUD_VREFOUT_B 48
AUD_EXT_MIC_L 49
AUD_EXT_MIC_R 49
AUD_VREFOUT_F_L 49
AUD_VREFOUT_F_R 49

X02
NO.58
AUD_INT_MIC_L 1UF/10V/X7R MLCC/+/-10% pt_c0603 C7116
AUD_INT_MIC_R 1UF/10V/X7R MLCC/+/-10% pt_c0603 C7117
AUD_EXT_MIC_L3 1UF/10V/X7R MLCC/+/-10% pt_c0603 C7118
AUD_EXT_MIC_R3 1UF/10V/X7R MLCC/+/-10% pt_c0603 C7119
D4601 1N4148WS-7-F
D4602 1N4148WS-7-F
AUD_VREFOUT_F

C729 10UF/10V pt_c0805_h53
R348 0Ohm /*
R603 0Ohm /*
R333 0Ohm /*

PLACE CLOSE TO U18 PIN6
ICH_AZ_CODEC_BITCLK
C692 22PF/50V MLCC/+/-5% /*

X02
NO.58
AUD_VREFOUT_B
AUD_VREFOUT_F
C4601 10UF/10V pt_c0805_h53
C7121 10UF/10V pt_c0805_h53

PLACE BETWEEN U18 and U19
JP5 SHORTPIN /*

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Title: ALC888
Size: Custom
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Date: Tuesday, August 19, 2008
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Signal Inveter for Speaker Shutdown

Allow speakers to work while class driver is installed

+5V_SPK_AMP
R367 100KOhm
AUD_SPK_ENABLE#
Q69 2N7002
R593 100KOhm
46,48 AUD_EAPD#
Q68 2N7002
40,48 NB_MUTE#

PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT

+5V_RUN — L52 60Ohm — +5V_SPK_AMP
pt_l0805_h41
MURATA/BLM21PG600SN1(Y8220)<G>
Irat=3A
C725 10UF/10V MLCC/+80-20% pt_c0805_h53

VDDA Range = 1.21V ~ 4.85V (SET =1.23V).
If SET=0 V, VDDA = 4.75V

VDDA
C741 1UF/10V/X7R MLCC/+/-10% pt_c0603
C742 1UF/10V/X7R MLCC/+/-10% pt_c0603

Place C490 close to Pin 30

+5V_SPK_AMP
C490 0.1UF/10V
C495 1UF/10V/X7R MLCC/+/-10% pt_c0603
C491 1UF/10V/X7R MLCC/+/-10% pt_c0603

NOTE:For TPA6040A, pop C487 and C486(0402 X5R) and no pop R601 and R376. C487 andC486 value should match C494 and C493

AUD_AMP_GAIN1
AUD_AMP_GAIN2

NO.28
HP1_INL_AMP1
HP1_INR_AMP1
X02 NO.48
C496 pt_c1206_h75 2.2UF/16V MLCC/+/-10% — AUD_HP1_OUT_L 46
C492 pt_c1206_h75 2.2UF/16V MLCC/+/-10% — AUD_HP1_OUT_R 46
C489 47PF/50V MLCC/+/-5% /*
C488 47PF/50V MLCC/+/-5% /*

+5V_SPK_AMP
R378 100KOhm /*
Note: For TPA6040A, pop R378 and no pop R375
R375 0Ohm — AUDIO_AVDD_ON 45

NO.30
T34 TPAD14-GP
C732 0.1UF/16V MLCC/+/-10%
+3.3V_CPVDD_HPVDD
If AUD_EAPD# not be used, pop R6929 and depop R6930.
R6929 /* 0Ohm
R6930 0Ohm — AUD_EAPD# 46,48

NO.28
46 AUD_LINE_OUT_R
C4701 1UF/10V/X7R MLCC/+/-10% pt_c0603
R4701 24.3KOhm
R4702 100KOhm
X02 NO.56
46 AUD_LINE_OUT_L
C4702 1UF/10V/X7R MLCC/+/-10% pt_c0603
R4703 24.3KOhm
R4704 100KOhm

TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.

C740 47PF/50V MLCC/+/-5% /*
C738 47PF/50V MLCC/+/-5% /*
C487 0.033UF/16V/X7R MLCC/+/-10%
R601 0Ohm
NO.28

0.033UF/100V pt_c1206_h59 — C494 MLCC/+/-10%
0.033UF/100V pt_c1206_h59 — C493 MLCC/+/-10%
45 AUDIO_AVDD_ON — R376 /* 0Ohm — FROM EC
C486 0.033UF/16V/X7R MLCC/+/-10%

NOTE:For TPA6040A, pop C486 and no pop R376

U19 TPA6040A4RHBR

	SPKR_RIN-	SPKR_RIN+	SPKR_LIN+	SPKR_LIN-	SPGND1	LOUT+	LOUT-	SPVDD1	CPVDD1	C1P	CPGND2	C1N	CPVSS	HPVSS	HP_OUTR	HP_OUTL	GND1	HPVDD	SPVDD2	ROUT-	ROUT+	SPGND2	HP_EN	SPKR_EN#	BYPASS
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	33	17	18	19	20	21	22	23	24

GAIN1 32, GAIN0 31, VDD 30, REG_OUT 29, SGND 28, HP_INL 27, HP_INR 26, REG_EN 25, GND2 34, GND3 35, GND4 36, GND5 37

SPKR_INR_AMP1
SPKR_INL_AMP1
48 AUD_SPK_L1
48 AUD_SPK_L2
C484 pt_c0603 1UF/10V/X7R MLCC/+/-10% — AUD_SPK_ENABLE#
AUD_SPK_R1 48
AUD_SPK_R2 48

U32D 74AHC08PW (VCC 12, GND 11)
U32C 74AHC08PW (VCC 9, GND 14) — NB_MUTE# 40,48; AUD_HP1_NB_SENSE 46,49

+5V_SPK_AMP
C483 1UF/10V/X7R MLCC/+/-10% pt_c0603
C481 10UF/10V pt_c0805_h53
C735 10UF/10V pt_c0805_h53
C485 1UF/10V/X7R MLCC/+/-10% pt_c0603

ROUTE VIA TRACE BACK TO TIE POINT.

AUD_HP1_JACK_L 49
AUD_HP1_JACK_R 49

ROUTE VIA TRACE BACK TO TIE POINT.

+3.3V_RUN Irat=200mA
L54 600Ohm
MURATA/BLM18AG601SN1(J5535)<G>
+3.3V_CPVDD_HPVDD

C736 1UF/10V/X7R MLCC/+/-10% pt_c0603
C734 1UF/10V/X7R MLCC/+/-10% pt_c0603
C733 10UF/10V pt_c0805_h53
C482 1UF/10V/X7R MLCC/+/-10% pt_c0603

ROUTE VIA TRACE BACK TO TIE POINT.

GAIN SETTING RESISTORS

+5V_SPK_AMP +5V_SPK_AMP X02 NO.56
R379 100KOhm
R374 100KOhm
AUD_AMP_GAIN1
AUD_AMP_GAIN2
/*
R377 100KOhm
R368 100KOhm

Gain1	Gain2	Gain
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

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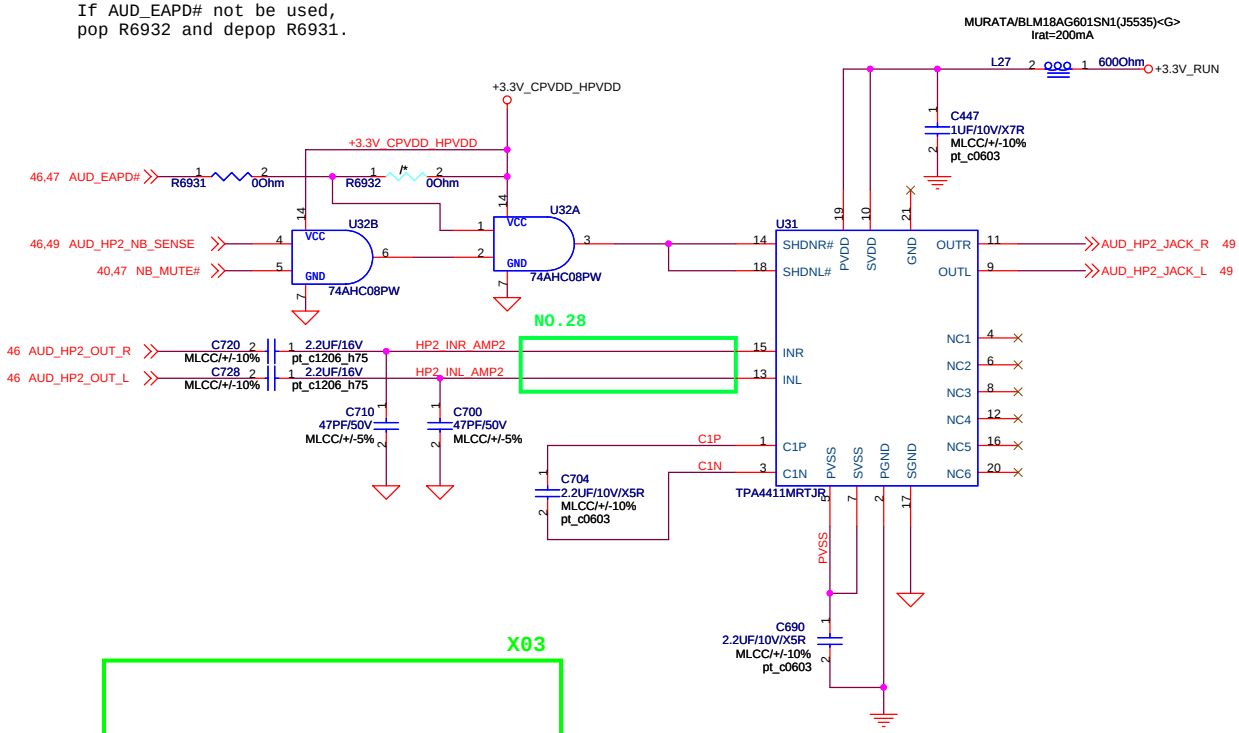
Title: AMP TPA6040
Size: Custom | Document Number: Diaz-UMA | Rev: A00
Date: Tuesday, August 19, 2008 | Sheet 47 of 68

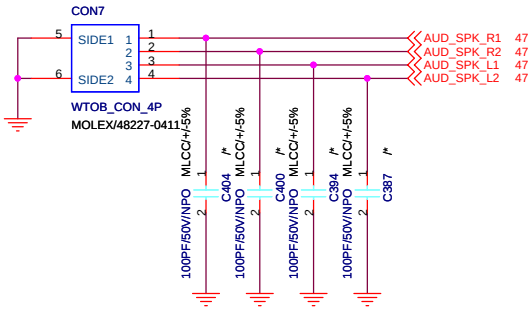
Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

If AUD_EAPD# not be used,
pop R6932 and depop R6931.

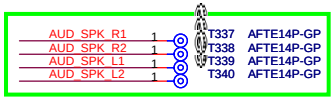


Speaker CON



Need to adjust EMI cap values as necessary.

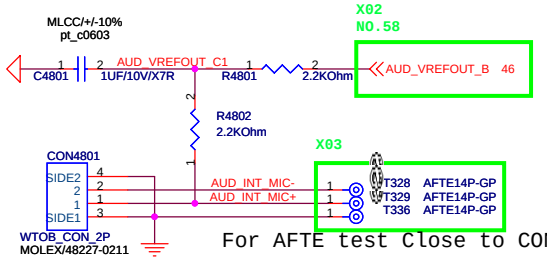
X03



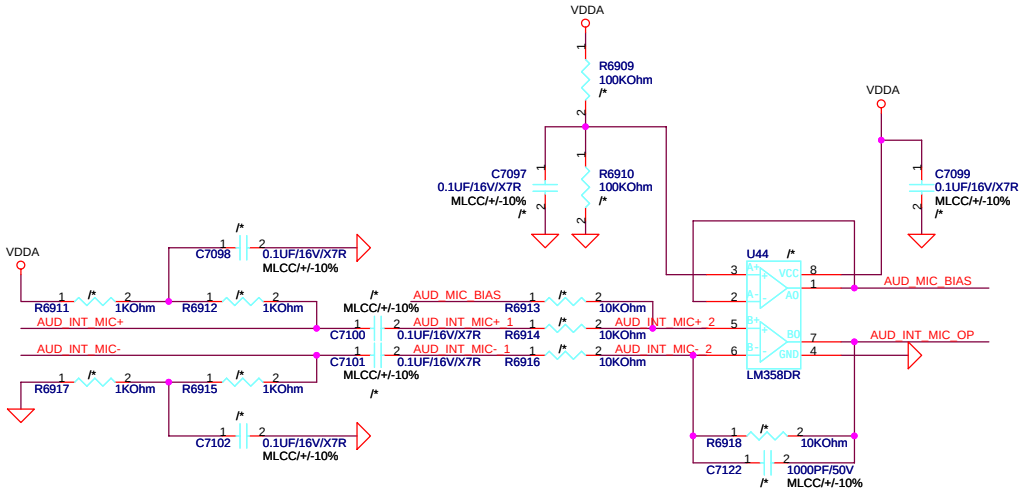
For AFTE test Close to CON07

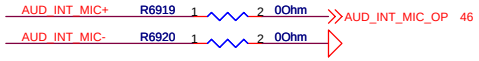
X03

X02
NO.58



For AFTE test Close to CON4801





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Title: AMP MAX4411 & MIC_AMP

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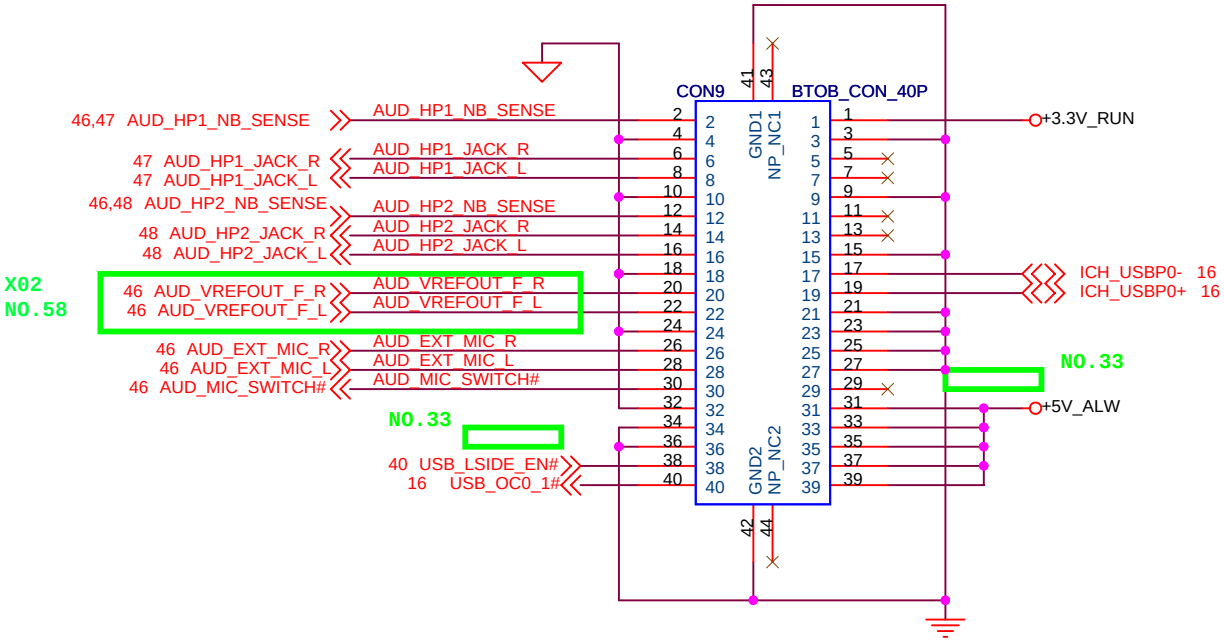

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Title: **AUDIO BtoB CON**

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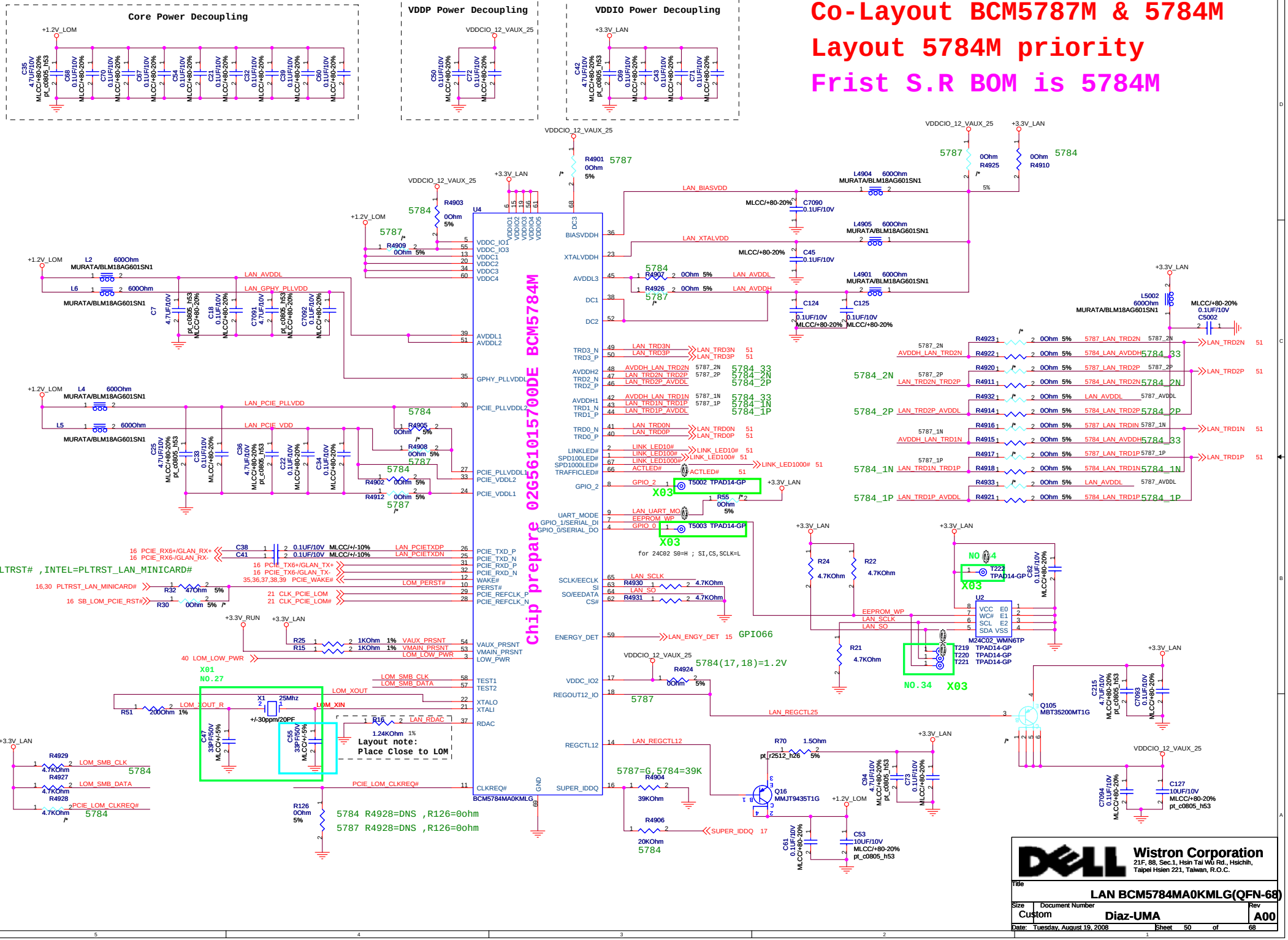
Co-Layout BCM5787M & 5784M
Layout 5784M priority
Frist S.R BOM is 5784M

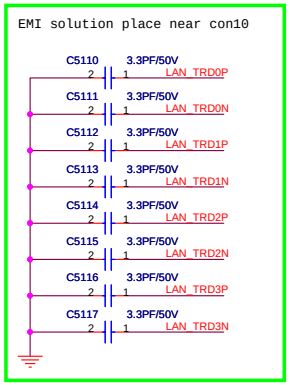


This BOM is 5784M

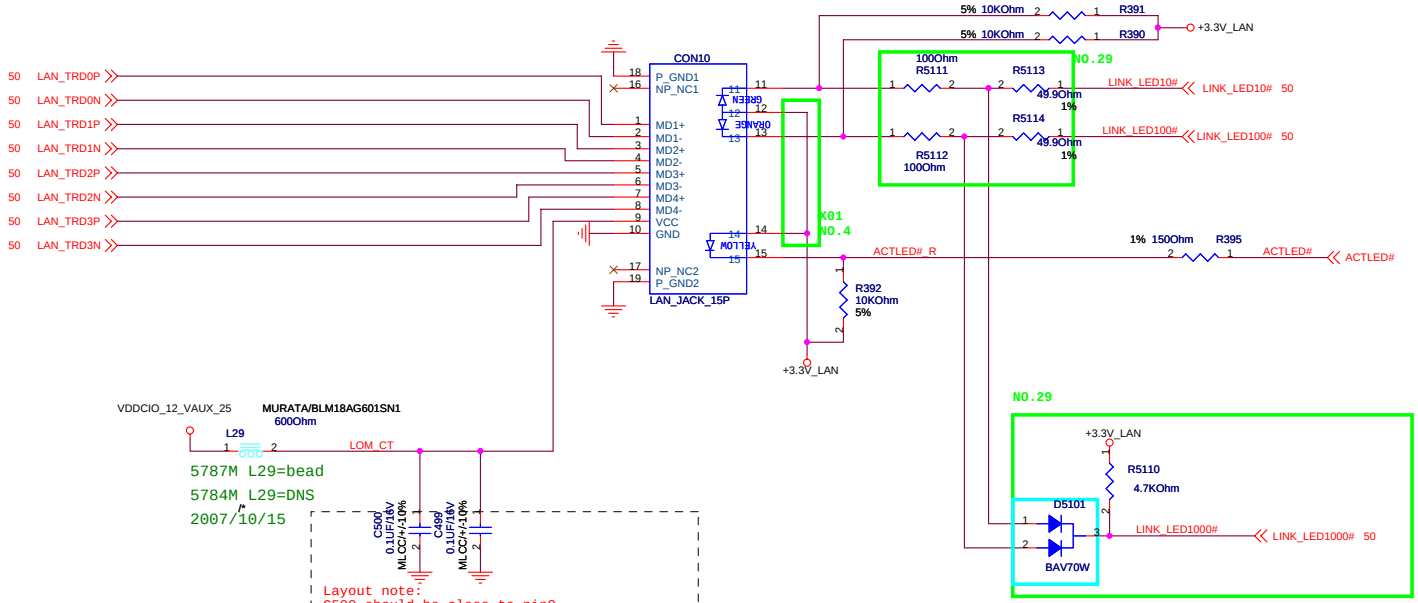
require S3 support wake on LAN 2007/10/05

NO.29

EMI solution place near con10

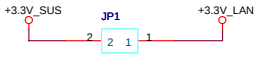


RJ45 should be 12G14801110KDE



+3.3V_LAN Source Guideline:

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on_LAN is required out of S4, S5



2007/10/08

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Title: Magnetics and RJ-45

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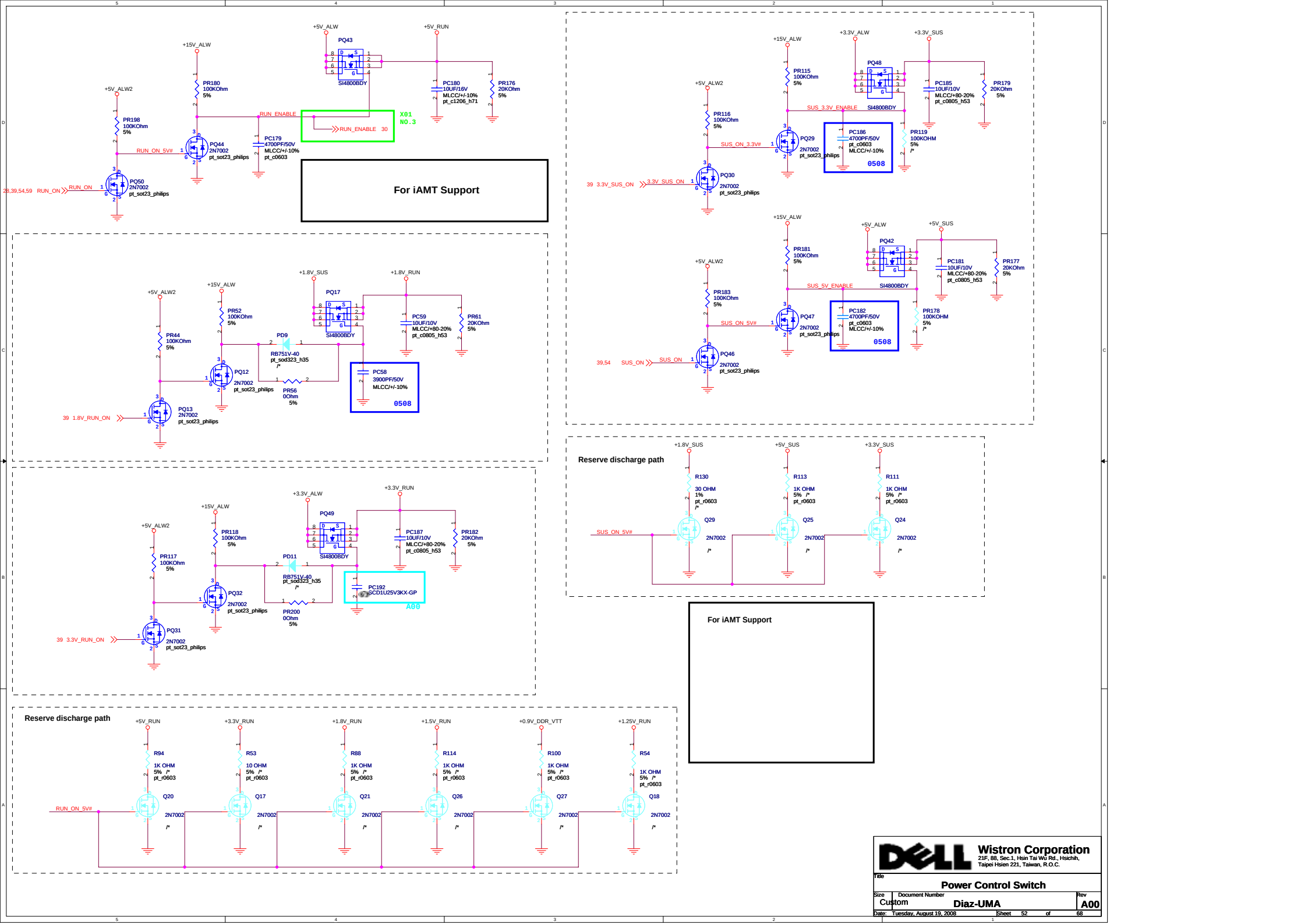

DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Power Control Switch	
Size: Custom	Document Number: Diaz-UMA	Rev: A00
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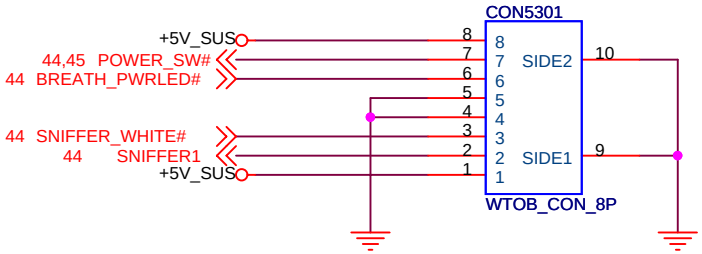

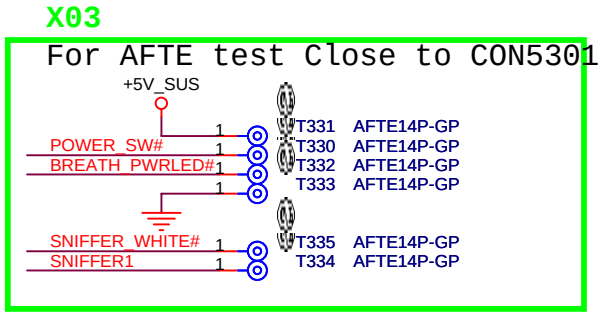

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Title: **Power Buttom Board**

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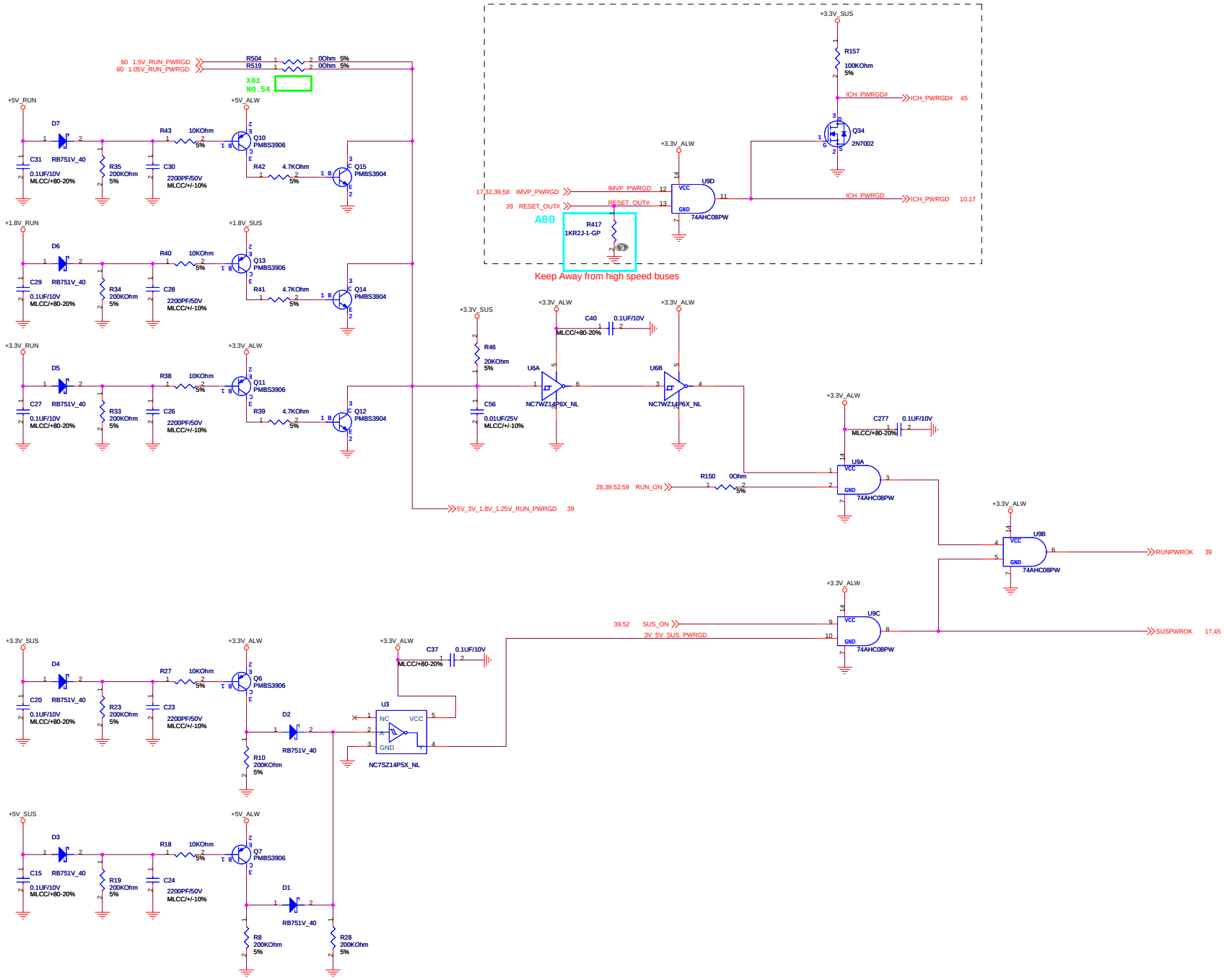

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Title: Power Sequence Logic		
Size: Custom	Document Number: Diaz-UMA	Rev: A00
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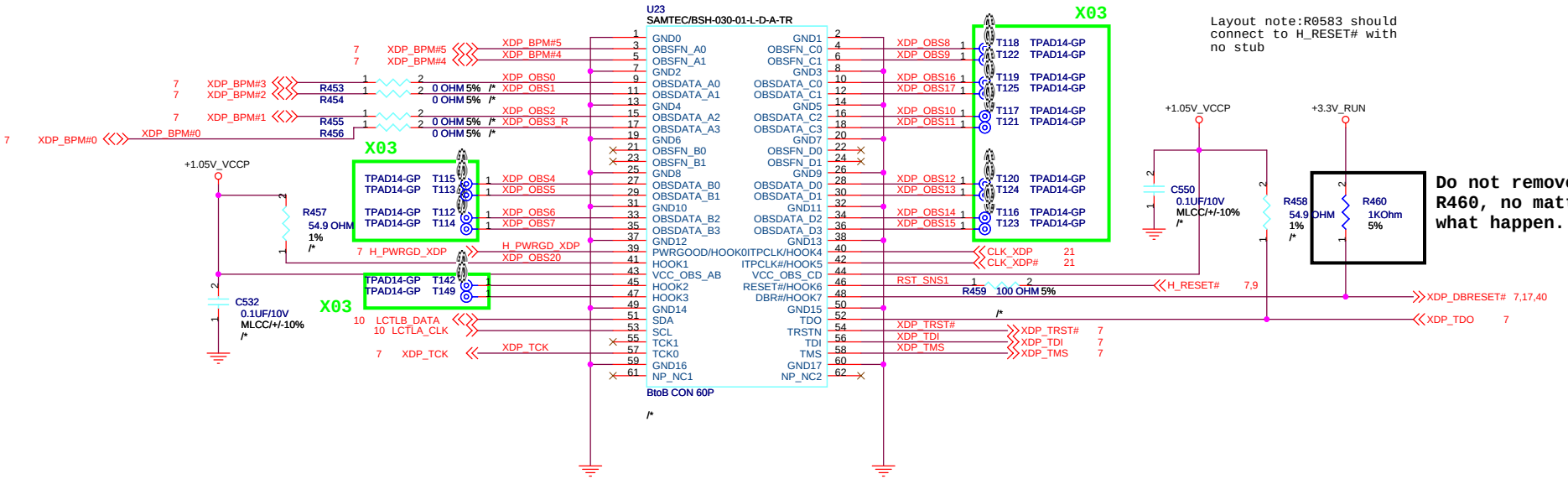
XDP



CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

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Title: XDP		
Size: A3	Document Number: Diaz-UMA	Rev: A00
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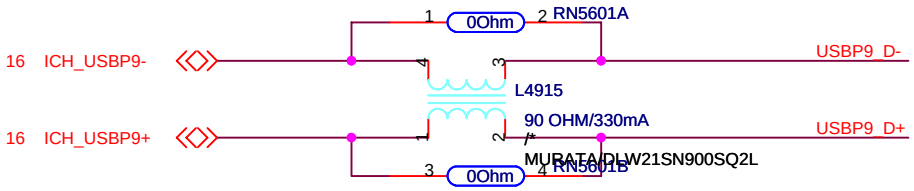
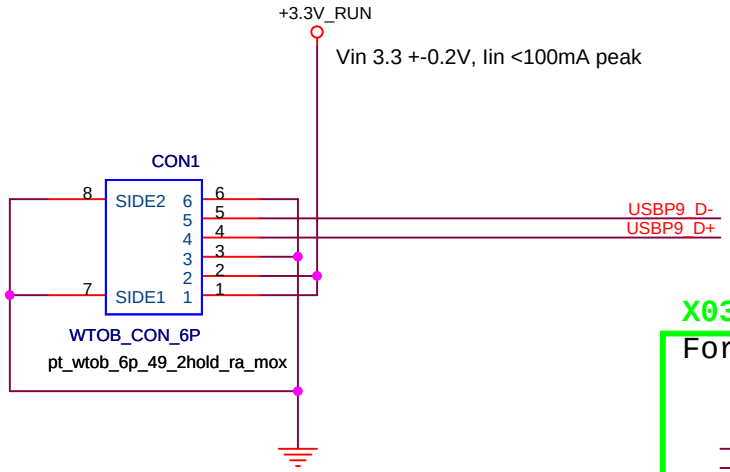
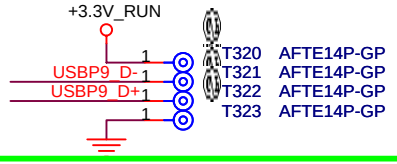
FINGER PRINTER





X03

For AFTE test Close to CON1



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Title: **FINGER PRINTER Port**

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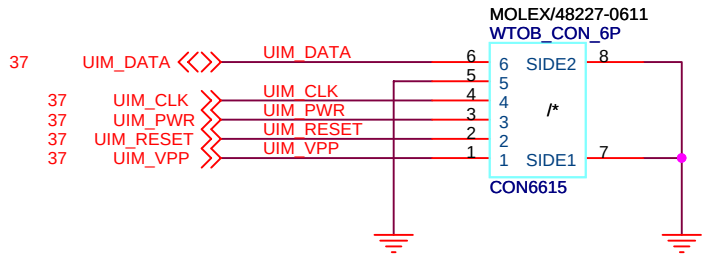
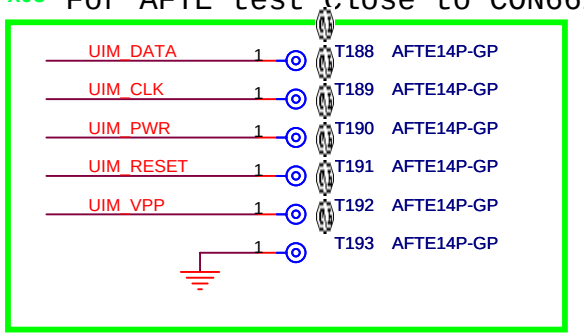


X03 For AFTE test Close to CON6615



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Title: SIM CARD		
Size: A4	Document Number: Diaz-UMA	Rev: A00
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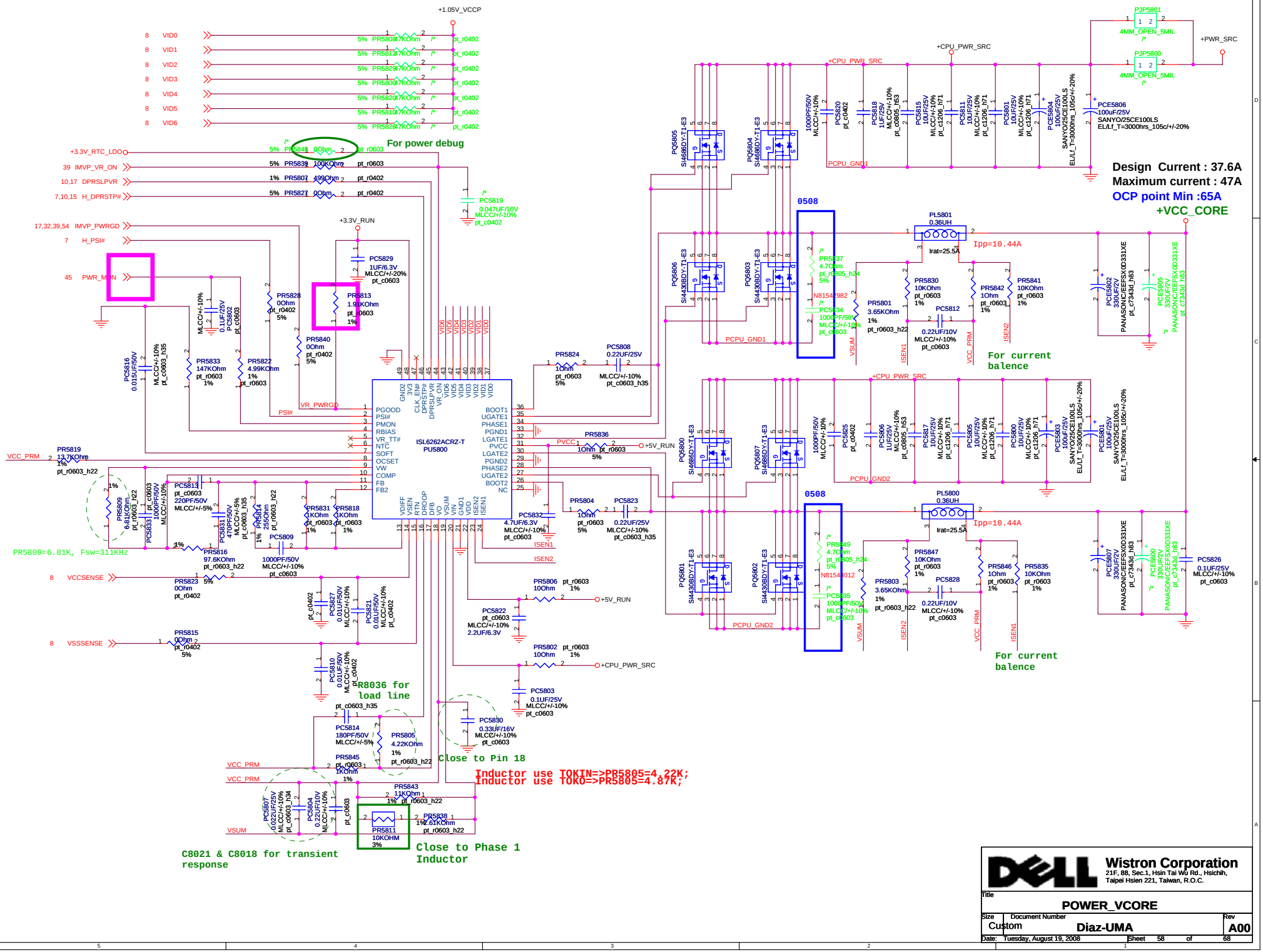

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Title	POWER_VCORE		
Size	Document Number		Rev
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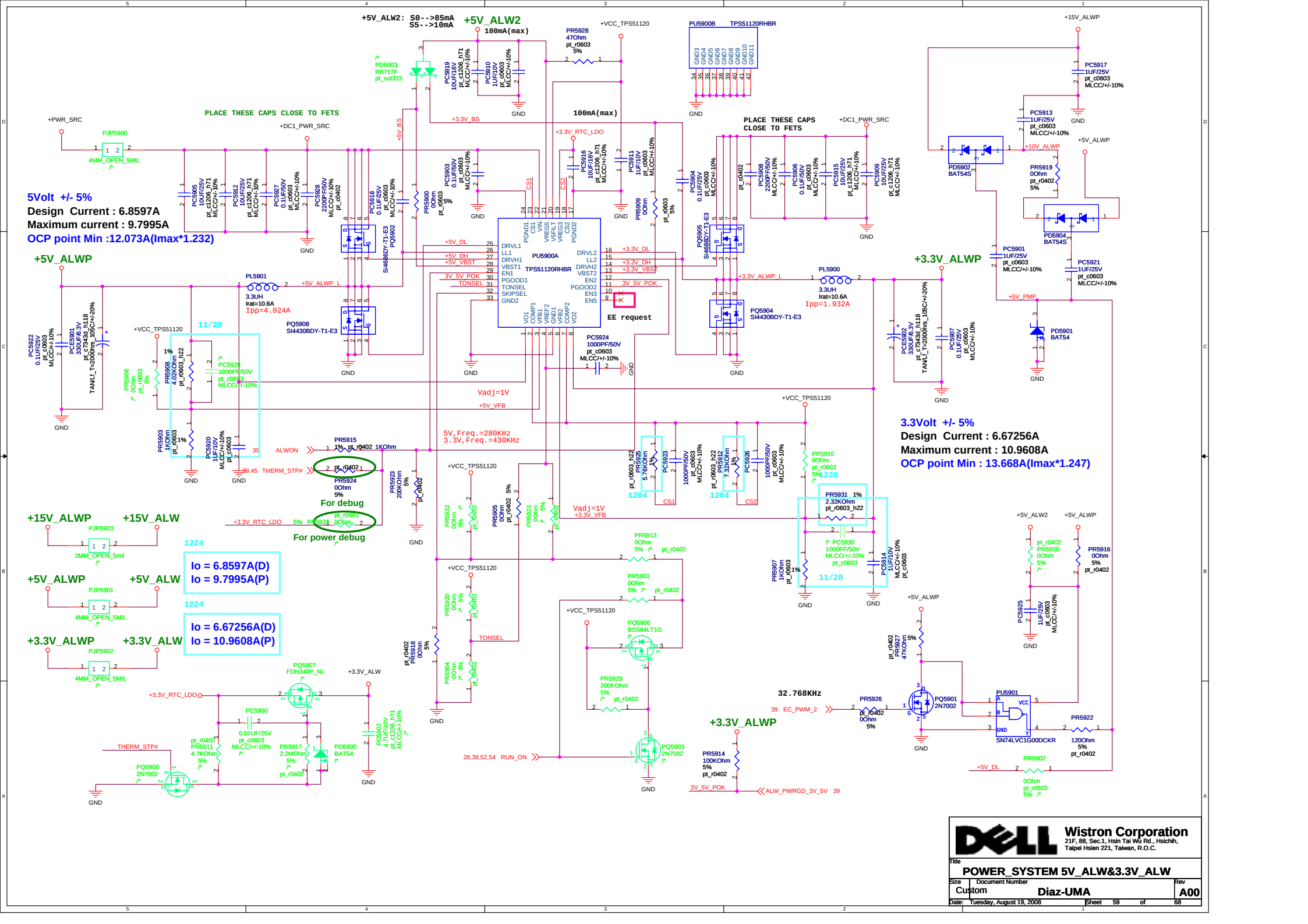
+5V_ALW2: S0-->85mA S5-->10mA
+5V_ALW2
100mA(max)
PR5928 47Ohm pt_r0603 5%
+VCC_TPS51120
PU5900B TPS51120RHBR
PLACE THESE CAPS CLOSE TO FETS
+PWR_SRC
PJP5900
4MM_OPEN_5MIL
+DC1_PWR_SRC
+3.3V_BS
+5V_BS
+3.3V_RTC_LDO
100mA(max)
PLACE THESE CAPS CLOSE TO FETS
+DC1_PWR_SRC
5Volt +/- 5%
Design Current : 6.8597A
Maximum current : 9.7995A
OCP point Min :12.073A(Imax*1.232)
+5V_ALWP
PL5901
3.3UH
Irat=10.6A
Ipp=4.024A
PU5900A TPS51120RHBR
PL5900
3.3UH
Irat=10.6A
Ipp=1.932A
+3.3V_ALWP
EE request
11/28
Vadj=1V
+5V_VFB
5V,Freq.=280KHz
3.3V,Freq.=430KHz
3.3Volt +/- 5%
Design Current : 6.67256A
Maximum current : 10.9608A
OCP point Min : 13.668A(Imax*1.247)
ALWON
THERM_STP#
For debug
For power debug
+15V_ALWP
+15V_ALW
PJP5903
2MM_OPEN_5mil
1224
Io = 6.8597A(D)
Io = 9.7995A(P)
+5V_ALWP
+5V_ALW
PJP5901
4MM_OPEN_5MIL
1224
Io = 6.67256A(D)
Io = 10.9608A(P)
+3.3V_ALWP
+3.3V_ALW
PJP5902
4MM_OPEN_5MIL
32.768KHz
+3.3V_ALWP
+10V_ALWP
+5V_PMP
+5V_DL
+3.3V_DL
+5V_DH
+3.3V_DH
+5V_VBST
+3.3V_VBST
3V_5V_POK
TONSEL
RUN_ON
ALW_PWRGD_3V_5V
EC_PWM_2
SN74LVC1G00DCKR
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Title
POWER_SYSTEM 5V_ALW&3.3V_ALW
Size Custom
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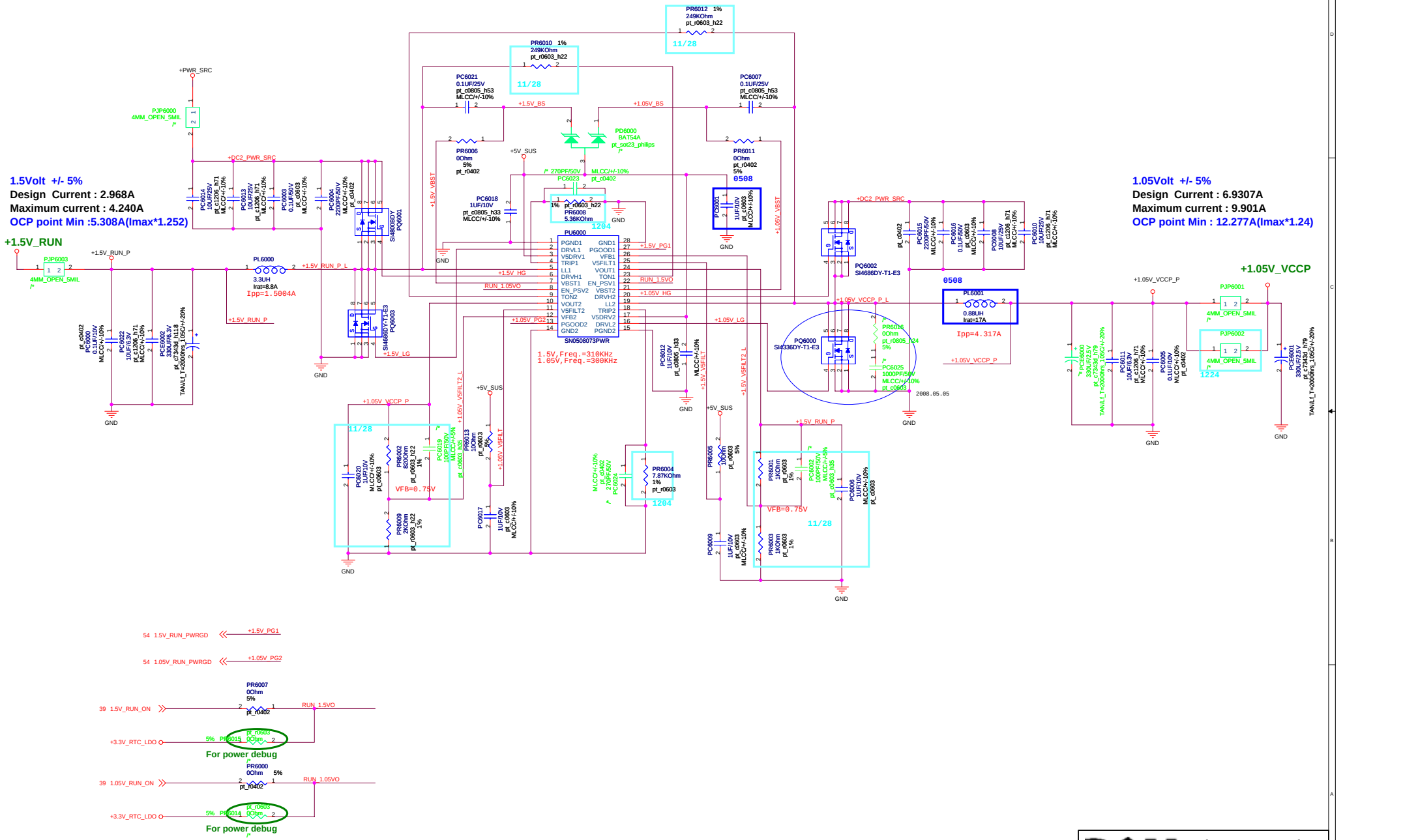
1.5Volt +/- 5%
Design Current : 2.968A
Maximum current : 4.240A
OCP point Min :5.308A(Imax*1.252)
+1.5V_RUN
1.05Volt +/- 5%
Design Current : 6.9307A
Maximum current : 9.901A
OCP point Min : 12.277A(Imax*1.24)
+1.05V_VCCP
PU6000
SN0508073PWR
1.5V,Freq.=310KHz
1.05V,Freq.=300KHz
PL6000
3.3UH
Ipp=1.5004A
PL6001
0.88UH
Ipp=4.317A
PQ6000
SI4336DY-T1-E3
PQ6002
SI4686DY-T1-E3
PD6000
BAT54A
VFB=0.75V
For power debug
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POWER_I/O_1.5VS & 1.05VS
Custom
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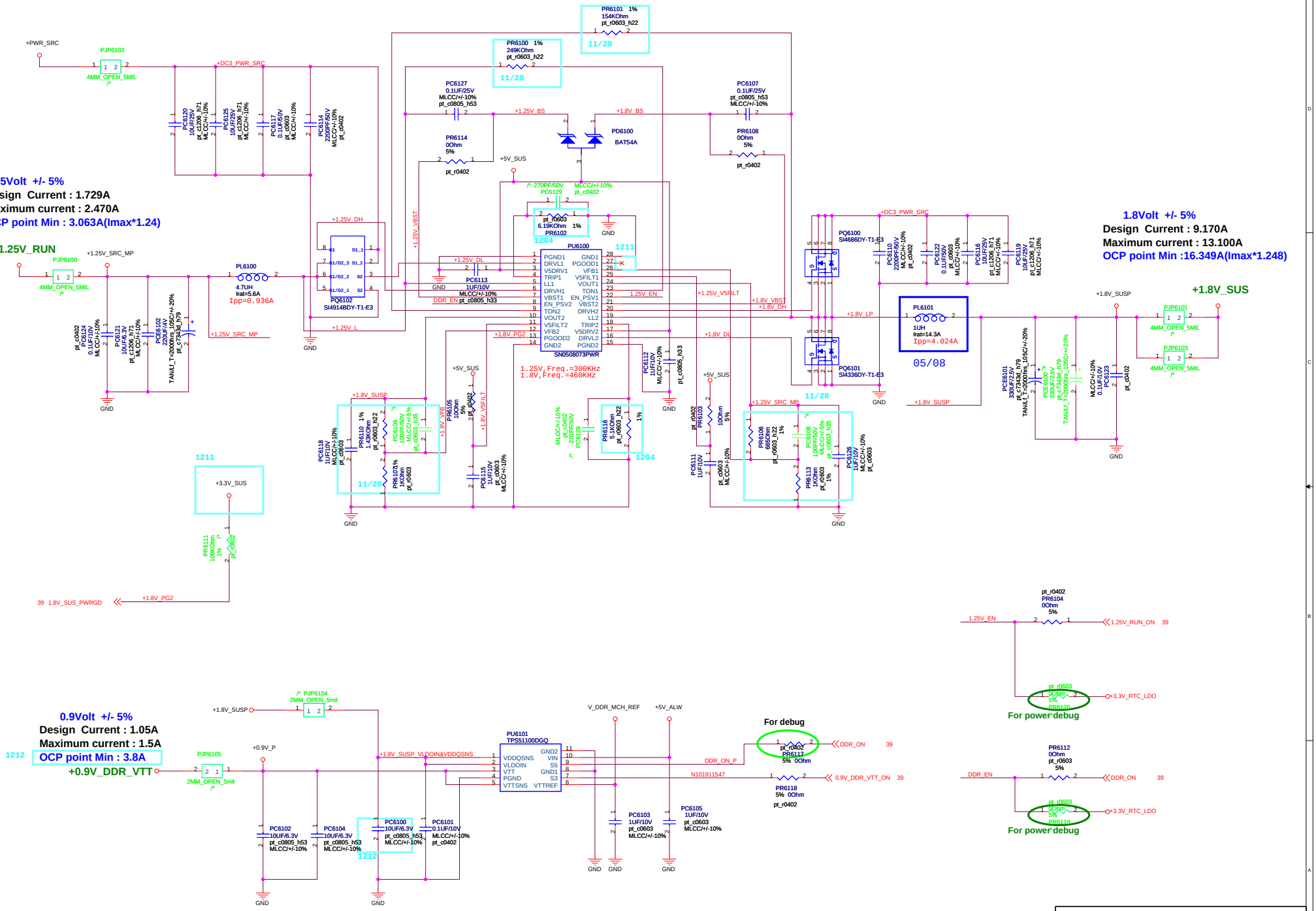
1.25Volt +/- 5%
Design Current : 1.729A
Maximum current : 2.470A
OCP point Min : 3.063A(Imax*1.24)
+1.25V_RUN
1.8Volt +/- 5%
Design Current : 9.170A
Maximum current : 13.100A
OCP point Min :16.349A(Imax*1.248)
+1.8V_SUS
0.9Volt +/- 5%
Design Current : 1.05A
Maximum current : 1.5A
OCP point Min : 3.8A
+0.9V_DDR_VTT
1.25V,Freq.=300KHz
1.8V,Freq.=460KHz
For debug
For power debug
For power debug
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
POWER_I/O_DDR & VTT & 1.25V
Custom
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Title: BLANK PAGE		
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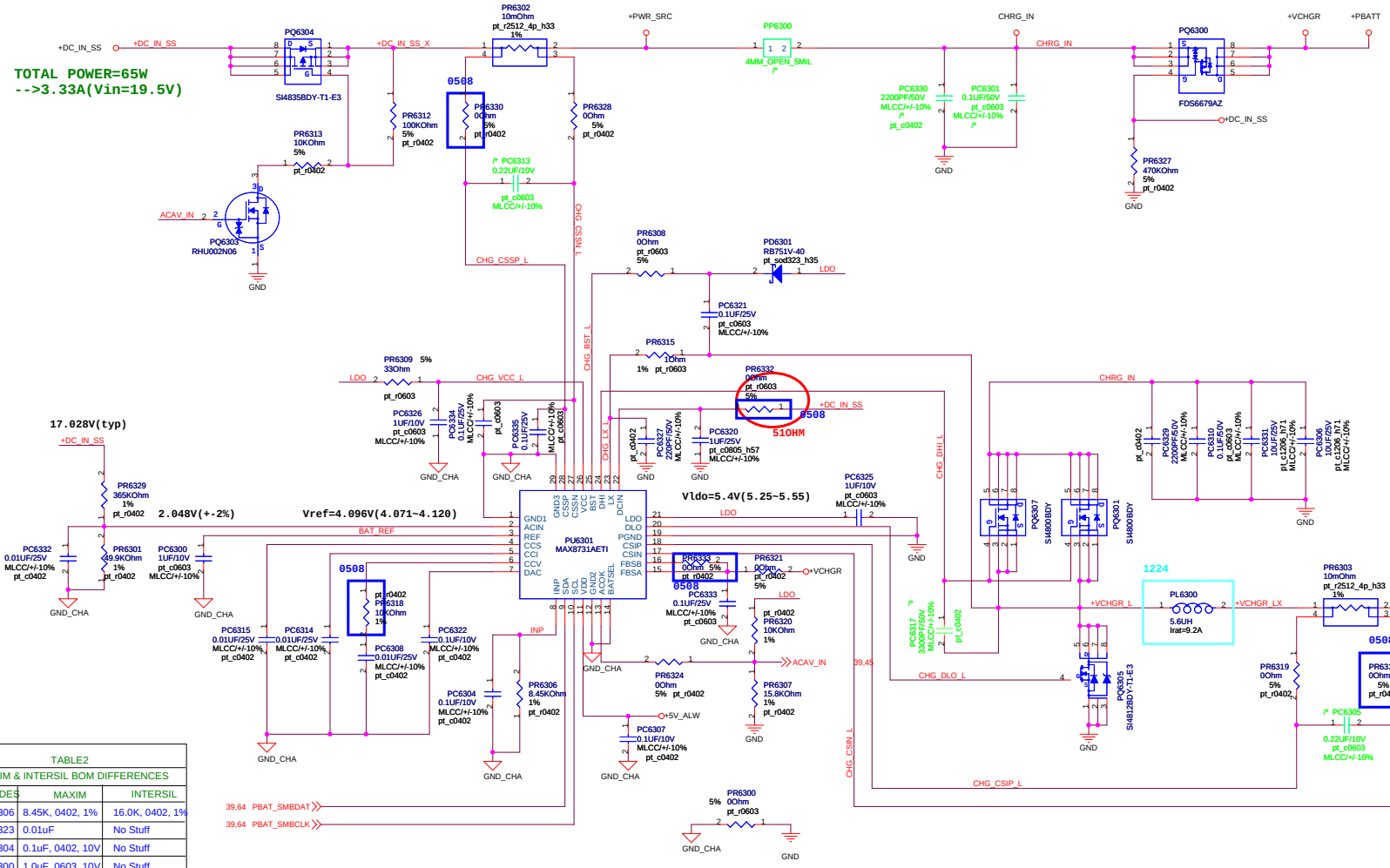

TABLE3		
PIN NAME DIFFERENCES		
PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT
"NC" means no-connect		

TABLE2		
MAXIM & INTERSIL BOM DIFFERENCES		
REF DES	MAXIM	INTERSIL
PR6306	8.45K, 0402, 1%	16.0K, 0402, 1%
PC6323	0.01uF	No Stuff
PC6304	0.1uF, 0402, 10V	No Stuff
PC6300	1.0uF, 0603, 10V	No Stuff
PR6329	365K, 0402, 1%	215K, 0402, 1%
PR6319	0, 0402, 5%	10, 0402, 5%
PR6328	0, 0402, 5%	10, 0402, 5%
PC6305	No Stuff	0.22uF
PC6313	No Stuff	0.22uF
PC6314	0.01uF	No Stuff
PC6322	0.1uF, 0402, 10V	No Stuff
PC6327	220pF, 0402, 50V	No Stuff
PD6301	RB751V-40	No Stuff
PC6317	3.3nF	No Stuff
PR6315	1, 0603, 1%	0, 0603, 5%
PR6321	100, 0402, 5%	0, 0402, 5%
PR6318	10K, 0402, 5%	4.7K, 0402, 5%
PC6308	0.01uF	0.01uF
PC6315	0.01uF	0.01uF
PD6300	1SS355	No stuff
PR6325	1K, 0603, 5%	No stuff

TABLE1					
ADAPTOR (W)	TRIP CURRENT (A)	PR6317	PR6311	PR6305	PR6326
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

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Title: POWER_CHARGER

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X03 For AFTE test Close to PCON6400

BATT+ IN 1 T180 AFTE14P-GP
Z4304 SMB_CLK 1 T181 AFTE14P-GP
Z4305 SMB_DAT 1 T182 AFTE14P-GP
Z4306 BATT_PRES# 1 T183 AFTE14P-GP
SYSPRES# 1 T184 AFTE14P-GP
BATT_VOLT 1 T185 AFTE14P-GP
BATT1- 1 T186 AFTE14P-GP
BATT2- 1 T187 AFTE14P-GP

TDC REQUSET TO CHANGE

+3.3V_ALW

ESD DIODES

PD6401 DA204U
PD6402 DA204U
PD6403 DA204U
DA204U PD6404 /*

GND

+PBATT

BATT_CON_9P
P_GND2 11
P_GND1 10
PCON6400

PC6401 pt_c0402 2200PF/50V MLCC/+/-10%
PC6402 0.1UF/50V pt_c0603 MLCC/+/-10%

BATT+ IN
Z4304 SMB_CLK
Z4305 SMB_DAT
Z4306 BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-

PR6401 100Ohm pt_r0402 5%
PR6402 100Ohm pt_r0402 5%
PR6405 100Ohm pt_r0402 5%
PR6406 100Ohm pt_r0402 5% /*

PBAT_SMBCLK 39,63
PBAT_SMBDAT 39,63
PBAT_ALARM#
PBAT_PRES# 40

+3.3V_ALW
PR6403 10KOhm 5% pt_r0402
PR6404 100KOhm 5% pt_r0402

EE request to add

Pin define differ with Lanai

PS_ID_DISABLE# 40

+5V_ALW
PR6407 15KOhm pt_r0603 5%
PD6405 MBRS2040LT3G pt_smb_h101 /*
PQ6401 PMBS3904
PR6408 10KOhm 5% pt_r0402
PR6410 10KOhm 5% /*
PD6406 DA204U /*
PR6409 100KOhm pt_r0603 5%

PL6400
1000Ohm/100MHz
pt_l0603
FERRITE BEAD(0603)1000OHM/0.1A

PQ6402 FDV301N_NL
PR6412 33Ohm 5% pt_r0402
PR6413 33Ohm 5% /* pt_r0402

PD6400 DA204U
PR6411 2.2KOhm 5% pt_r0402
PS_ID 39

+DC_IN

+DCIN_JACK
PL6401
60Ohm/100Mhz
pt_l1806
MURATA/BLM41PG600SN1L

PCON6401
P_NC3 P_NC1 NP_NC1 NP_NC2 P_NC2 P_NC4
DC_PWR_JACK_5P

PD6407 VZ0603M260APT pt_varistor_0603 /*

PC6407 0.1UF/25V pt_c0603 MLCC/+/-10% /*
PR6417 4.7Ohm pt_r0603_h22 5%
PC6408 1UF/25V pt_c0805_h53 MLCC/+/-10%
PR6400 0Ohm 5% /* pt_r0402

PQ6403 SI4835BDY-T1-E3
PC6406 0.47UF/25V pt_c0805_h53 MLCC/+/-10%
PR6415 240KOhm 1% pt_r0402
PQ6404 SI2301BDS /*
PR6416 47KOhm 5% pt_r0402

+DC_IN_SS
pt_c0402 PC6400 0.01UF/25V MLCC/+/-10%
PC6403 0.1UF/50V pt_c0603 MLCC/+/-10%
PC6404 0.1UF/50V pt_c0603 MLCC/+/-10%
PC6405 10UF/25V pt_c1206_h71 MLCC/+/-10%
PR6414 4.7KOhm pt_r0805_h24 5%

CONFIRM JAY EE REQUEST TO DE-POP

39 AC_OFF
PQ6400 DTC115EUA /*
R1 R2

GND

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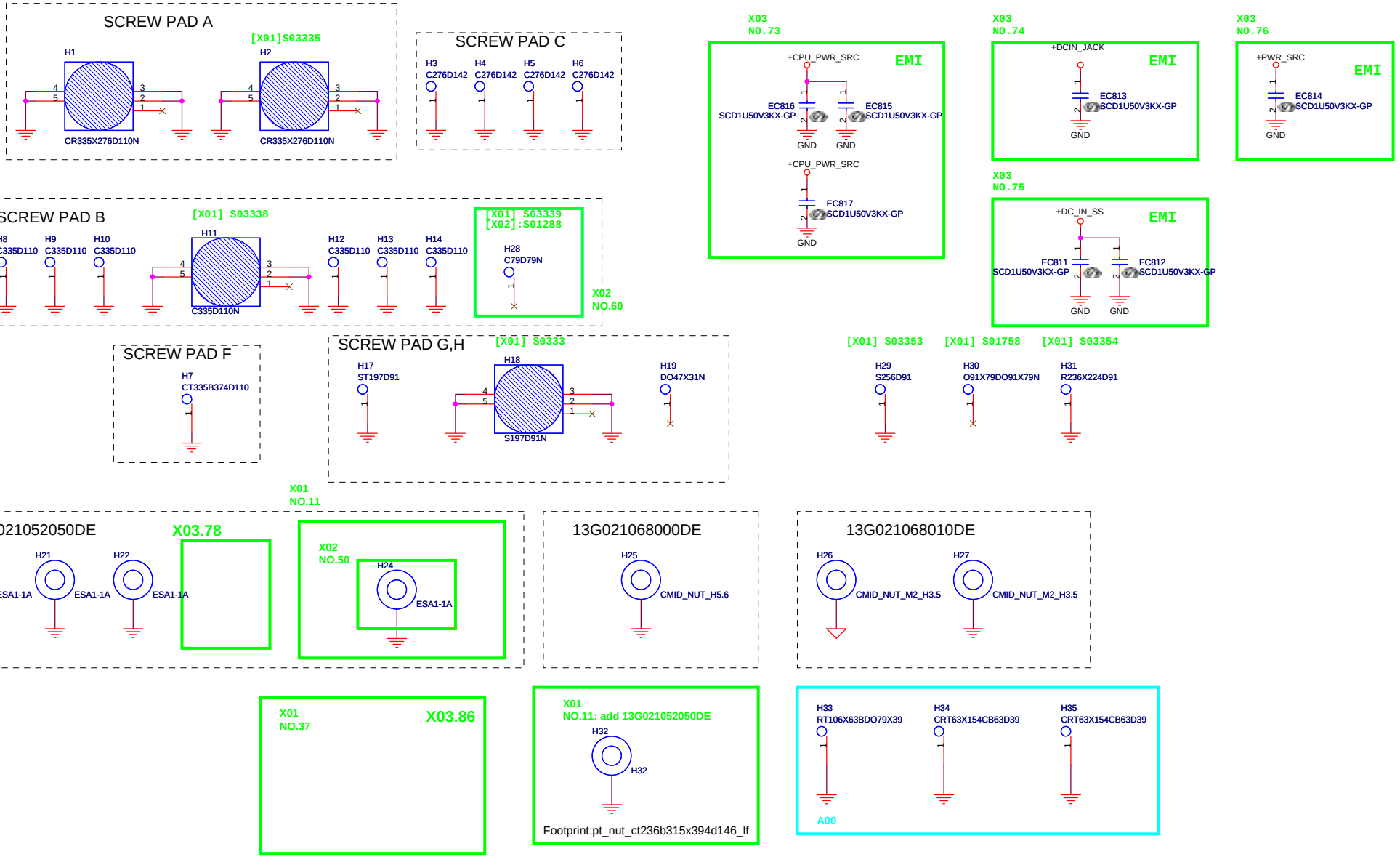

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Item	Page	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	all	X00 release	10/24/2007		X00 release		X00
2	44	Switch power pull	11/30/2007	AA EE	Change main power switch and sniffer power switch power plane to +3.3V_RTC_LDO	Change +RTC_SELL to +3.3V_RTC_LDO	X01
3	30	HDMI power	11/30/2007	AA EE	Modify power diode to MOSFET for leakage current that can lower forwad voltage and match HDMI 5V voltage range	Replace D4612 by Q19 and connect Q19 gate to RUN_ENABLE	X01
4	51	LAN LED	11/30/2007	AA EE	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	Changed LAN Jack (CON10) pin12 to +3.3V_LAN	X01
5	35	Express card power switch	11/30/2007	AA EE	Express Card power switch (U13) pin4 should be connected to +3.3V_RUN for the purpose of using RICOH/R5538 as 2nd source	Connect U13 pin4 to +3.3V_RUN	X01
6	18	ICH8	11/30/2007	AA EE	ICH8 pin AD11 VCCSUSHDA modify to +3.3V_ALW for +3.3V_RUN to solve S5 leackage issue	Connect ICH8 pin AD11 to +3.3V_ALW	X01
7	A1,A2	Audio Board	11/30/2007	AA EE	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+_U;4.AU3 pin3 rename to USBP0_D-_U	1.AH1change to NPTH;2.ACON5 change to 12G142001113DE; 3.AU3 pin1 rename to USBP0_D+_U;4.AU3 pin3 rename to USBP0_D-_U	X01
8	15,44	LED mask circuit	12/05/2007	AA EE	1.Delete sniffer LED mask circuit 2.modify SATA and WPAN LED circuit.	1.Delete R246,R247,Q43 2.modify SATA and WPAN LED circuit	X01
9	17	CLK_ICH_48M	12/06/2007	AA EE	To improve 48MHz clock signal integrity , pop R339, change C456 to 10pF from 4.7pF and make it stuff.	Pop R339, change C456 to 10pF from 4.7pF and make it stuff.	X01
10	29	CRT signals	12/06/2007	AA EE	Fine tune CRT signals	Change C6649~C6654 to 10pF.	X01
11	65	Screw Hole	12/06/2007	AA EE	Added screw hole by NB thermal solution & ME request	Added H32, changed H24	X01
12	16,35,50	Reset signals	12/06/2007	AA EE	To improve RESET signals integrity	1. Audio:ICH_AZ_CODEC_RST#, R270=100 ohm 2. HDMI:ICH_AZ_HDMI_RST#, R205=100ohm 3. RICOH:PCI_RST#, R1601=100 ohm, add C6663=10pF 4. WLAN:PLTRST#, add C696=22pF 5. WWAN:PLTRST#, add C697=22pF 6. EC:PLTRST#, add R6972=220ohm	X01
13	28	+LCDVCC	12/06/2007	AA EE	Fine tune LVDS power sequence T1 time	Change R17 to 470K ohm from 330K ohm	X01
14	21	PCI Clock	12/10/2007	AA EE	Fine tune PCI clock slew rate by EA	Swap net name: CLK_PCI_PCCARD & CLK_PCI_8512	X01
15	39	EC power	12/10/2007	AA EE	update EC pin12 net by vender request changed list for batter quality.	Added C3901=0.1uF, C3902=1uF, R3907=0 ohm	X01
16	21,28,40	EMI component	12/10/2007	AA EE	modify compoment by EMI Comm Team request.	P21: add C2107、C115、C159、C172、C194 P28: add C7110~7111、C7113、C7112 (33pF)、C7114(33pF) P28: remove R2804A/B, add L1 P40: add CN21、CN22、CN23、CN24、CN25、CN26、CN28	X01
17	40	Platform ID	12/10/2007	AA EE	add platform indicator circuit	add R4025~28, net name: PLATFORM_ID[0:1]	X01
18	54	Power Sequence	12/10/2007	AA EE	Flow power circuit.	Remove R73 & net name: 1.25V_RUN_PWRGD	X01
19	40,43	Connector	12/10/2007	AA EE	Changed Connector by ME request.	page 40 -> change CON4010 page 43 -> change CON3	X01
20	C1	CAPBTN I2C	12/12/2007	AA EE	Fine tune CAPBTN I2C timing.	1.Change I2C damping R (CBT_R795) from 330ohm to 100ohm 2.Add through holes CBT_H15(s01291) & CBT_H28(s03350)	X01
21	F1	FingerPrinter LDO	12/12/2007	AA EE	Fine tune LDO performance.	1.F_U3, Pin3(CE pin) connects with Pin1(Vin) 2.F_U3, Pin4(ECO pin) connects with Pin1(Vin)	X01
22	S1	SIM Screw Hole	12/12/2007	AA EE	ME update DXF	change screw hole SH2 & SH3 & SCON1	
23	28	Digital MIC	12/13/2007	AA EE	DMIC clock EMI solution modify	1.R2802 change to 80ohm bead(follow Lanai P/N) 2.R2803 change to 47ohm 3.Mount C748 (33P)	
24	A2	Audio Board	12/14/2007	AA EE	Update eSATA connector for USB function only.	changed ACON5 = 12G142001115DE	
25	39	IT8512E	12/15/2007	AA EE	Del C3921 (IT8512E I version pop 0ohm, J version pop 0.1uF)	Del C3921	
26	40	Platform ID	12/15/2007	AA EE	Del R4025,R4027 to force PCB platform type (Intel SR)	Del R4025,R4027	
27	21,33,39,50	XTAL	12/15/2007	AA EE	Change XTAL for better capability	(1) X4 24.576MHz change to 07G010222452DE,C453 change to 22pF,C454 change to 22pF (2) X1 25MHz change to 07G010222509DE, C47,C55 change to 33pF (3) X2 14.318MHz change to 07G01021143CDE , (4) X5 32.768KHz change to 07G01020327ADE, change C667,C654 to 15pF	
28	46~48	Audio	12/18/2007	AA EE	Modify Audio BOM	1.Unmount R4602 2.Mount R4601,Q123,R6958 3.Delete R6964,R6965,R6960,R6961,R6970,R6962,R6963,R6971 4.Add R4701,R4702,R4703,R4704,C4701,C4702	
29	50~51	LAN	12/18/2007	AA EE	Modify schematic for triple LED control & EMI solution	1.Add R5110~R5114,D5101; del T5004, add LINK_LED1000# 2.Add C5110~C5117	
30	45,47	Test Point	12/18/2007	AA EE	Add test point for factory ICT team request	Add T33 in U19.23 & T34 in U8.26	
31	41	SPI Flash	12/18/2007	AA EE	Remove SPI Flash dymp RES.	Remove R310, R316, R317, R4102	

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Taipei Hsien 221, Taiwan, R.O.C.

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32	31	HDD/ODD Power	2007/12/18	AA EE	Modify HDD/ODD power circuit by customer request	1.unmount JP4, R3101 2.POP BOM: R5, R7, R399, R400, C13, Q2, Q3, Q56	X01
33	49,A1 A2	USB charged	2007/12/19	AA EE	Remove USB charged circuit by customer request	1.Delete AU2 2.rename USBP0_D-_U & USBP0_D+_U to USBP0_D- & USBP0_D+ 3.connect CON9,ACON1 pin36 to DGND, pin29 NC.	X01
34	39,41 45,50	Test Point	2007/12/19	AA EE	Add test point by ICT factory request	1.Add T151,T152,T159,T166,T178,T179 for U27 signal pin 2.Add T222,T219,T220,T221 for U2 signal pin 3.Add T148 at U15 pin14, T150 at U8 pin3	X01
35	A2	Audio Board	2007/12/20	AA EE	Modify USB differential signals.	1.Delete AL7 2.rename USBP0_D+ & USBP0_D- to AICH_USBP0+3 & AICH_USBP0-	X01
36	44	WPAN LED	2007/12/21	AA EE	Pop BOM for WPAN LED support	POP BOM: R4411(100K Ohm)	X01
37	65	Screw Hole	2007/12/25	AA EE	add screw hole for IR Blockade	Add: H32, H33	X01
38	C1	CAPBTN	2007/12/25	AA EE	update CAPBTN Circuit by customer ID modified	Swap net SNS_REWIND & SNS_PLAY, LED_REWIND# & LED_PLAY#	X01
39	F1	FingerPrint Screw	2007/12/25	AA EE	Screw hole (NPTH) modified the internal diameter to 1.7mm and the external diameter to 3mm	Modify F_H1, F_H2	X01
40	17	WPAN CTRL	2007/12/26	AA EE	Modify WPAN detect signals by different WLAN module support.	changed net USB_WPAN_DET# to R1701 & pull up to +3.3V_RUN	X01
41	13,38	Cost Down Plan	2007/12/27	AA EE	Cost Down Plan	CE1303, CE1301 => Change to POSCAP 220U/4V De-pop => C602, C589, C590, C1302, C1312, CE7 C363 => Change 10uF/10V Y5V C1309 => Pop 0.1uF R1301 => Change to 0 ohm De-pop => CE16	X01
42	30,42	Connector	2007/12/28	AA EE	By ME connector changed list	Changed CON6610 = 12G13141108ADE Changed CON6608 = 12G24110193RDE	X01
43	40	Board ID	2008/02/14	AA EE	Changed pcb id to X02	Changed pcb id to X02	X02
44	15	XTAL	2008/02/14	AA EE	Modify C375,C377 per XTAL report	Change C375,C377 to 3.3pF	X02
45	16	ICH8 reset signal	2008/02/14	AA EE	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	U14, U30, U37: power modify to +3.3V_ALW from +3.3V_RUN	X02
46	41,C1	CapBTN	2008/02/14	AA EE	Add CapBTN IC reset signal	1. Add CBT_RESET pin,add two jumpers on the CapBtn board. 2. Sense pad modify to elliptic through hole 3. Add a reserved 10uF capacitor parallel to +5V_ALW2 on the CapBtn board	X02
47	30,37	Comm. team solution	2008/02/14	AA Comm. Team	Add comm. team solutions	1.Pop L4606, depop RN3701 by comm. team request 2.CMIU: Add C3051 39PF close to C6925	X02
48	47,A1	Audio	2008/02/14	AA EE	Modify ACON2,ACON3,ACON4 footprint. Change value of C492,C496 to improve AP performance	1.ACON4 PCB footprint change to pt_phone_j_6p_4hd_col_lf 2.ACON3,ACON2 footprint change to pt_phone_j_6p_4h_col_lf 3.C492 and C496 Bom change to 2.2U(11G236122511310DE) from 1UF	X02
49	21	Clock	2008/02/18	AA EE	Delete reserved resistors	Delete RN1, RN2, RN3, RN5, RN6, RN7, RN8, RN9, RN10, RN11	X02
50	65	Nut	2008/02/18	AA ME	Swap PN of H23,H24 base on updated DXF	Swap PN of H23,H24	X02
51	C1	CAPBTN	2008/02/19	AA EE	LED Mute/VD/VU of power rail update	LED Mute/VD/VU are connect to +5V_ALW2 power rail	X02
52	39	EC	2008/02/19	AA EE	Support CAPBTN reset signals.	modify net_name U15.109: CAP_EC_RESET, Delete: T3907	X02
53	F1	Finger Print	2008/02/19	AA EE	update F_X1 footprint	update F_X1 footprint: modify pin1 indication	X02
54	C1	CAPBTN	2008/02/19	AA EE	Modify level shift circuit & Hole	1.Add elliptic through holes for BT, WiFi, and HDD LEDs 2.Change CBT_C1 to PT footprint	X02
55	39	EC	2008/02/19	AA EE	Modify Chip version.	update Chip version: 06G042005012DE,option R3920,mount C3920	X02
56	47	Speaker gain	2008/02/21	AA EE	Fine tune gain	1.Unmount R374,R377 and Mount R379,R368 2.R4701,R4703 change 24.3Kohm and R4702,R4704 mount 100Kohm	X02
57	F1	Finger Print	2008/02/22	AA EE	Add Test Point by Factory Request	Add F_T14 Test Point	X02
58	46	Audio	2008/02/22	AA EE	Modify Audio solve pop issue	Modify Audio Circuit	X02
59	44	Switch LED	2008/02/25	AA EE	Modify LED Color by customer request	LED1 changed to 07G01520097SDE, WHITE&ORANGE	X02
60	60,61	POWER	2008/05/7	W EE	PL6001 12.4A change to 17A ;PL6101 14.3A change to 17A;Add PC6001(1u/10V)	Modify power Circuit	X02
61	58	POWER	2008/05/7	W EE	PR5817 change location to PR5837(4.7R 0805);PC5824 change location to PC5834(1000PF/50V); PR5821 change location to PR5849(4.7R 0805);PC5834 change location to PR5835(1000PF/50V);	Modify power Circuit	X02
62	61	POWER	2008/05/7	W EE	PU6101 Pin6,PIN7 swap	Modify power Circuit	X02
63	60	POWER	2008/05/7	W EE	PQ6004(SI4430BDY)change location to PQ6000 (SI4336DY) add PR6016(DY)0R 0805;PC6025(DY) 1000PF/50V;	Modify power Circuit	X02
64	60	POWER	2008/05/7	W EE	POP PC182,POP PC186,PC58 change to 3900pf	Modify power SW Circuit	X02
65	61	POWER	2008/05/7	W EE	POP PR6330(0R),POP PR6332(0R),POP PR6318(10K),POP PR6333(0R),PR6331(0R)	Modify power Circuit	X02
66		POWER	2008/05/7	W EE	DZ1 GM M/B Close GAP (J2,J3,PJP5800,PJP5801,PJP5900,PJP5901,PJP5902,PJP5903,PJP6000,PJP6001,PJP6002,PJP6003, PJP6100,PJP6101,PJP6102,PJP6103,PJP6104,PJP6105,PJP6200,PJP6201,PJP6202,PJP6203,PP6300) DZ1 GM CAPBTN Board Close GAP(CBT_JP1,CBT_JP2) DZ1 GM Audio Board Close GAP(AJ1)	Close power GAP	X02
67	29	CRT	2008/05/16	W EE	Q2901,Q2902 "BSS138N" change to "2N7002"	cahnge part X02	

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68	60,61	POWER	2008/06/30	W EE	PR6004 change to 7.87Kohm;PR6100 change to 249Kohm;PR6116 change to 5.1Kohm	cahnge part	X03
69	40	Board ID	2008/06/30	W EE	Board ID change to X03=> R534"Dummy";POP "R535"	cahnge PCB ID	X03
70	L1	Lid Board	2008/06/30	W EE	LID Board: add HALL1 connect" 20.F0866.003"	cahnge part	X03
71	A2	Aduio Board	2008/06/30	W EE	Audio Board :ACON5 change to " PN:12G142001115DE" waiting wistron P/N	cahnge part	X03
72	66~74	I/O Board	2008/07/04	W EE	I/O board schematic remove	independence I/O board shecmatic for layout ME issue	X03
73	65	For EMI	2008/07/04	W EMI	For EMI :+CPU_PWR_SRC add EC816,EC815,EC817 0.1u/50V EMI CAP	EMI solution	X03
74	65	For EMI	2008/07/04	W EMI	For EMI :+DCIN_JACK add EC813 0.1u/50V EMI CAP	EMI solution	X03
75	65	For EMI	2008/07/04	W EMI	For EMI :+DC_IN_SS add EC811,EC812 0.1u/50V EMI CAP	EMI solution	X03
76	65	For EMI	2008/07/04	W EMI	For EMI :+PWR_SRC add EC814 0.1u/50V EMI CAP	EMI solution	X03
77	37	SIM CARD	2008/07/04	W EE	For SI : UIM_CLK add R6634 0R	For SI	X03
78	65	HOLD	2008/07/07	W ME	Cost down remove H23	remove part	X03
79		For ATE	2008/07/07	W ME	all test point change to "ZZ.PAD14.001" page 7 test point T31,42 change to "ZZ.PAD14.001" page 10 test point T127,T27,T29,T28,T126,T18,T19,T21,T25,T23,T35,T37,T40,T38,T39,T36,T20,T24, T22,T26,T41,T137,T32,T135,T128,T130,T131,T30,T1002,T1001 page 11 test point T134,T136 page 15 test point T92,T91,T93,T84,T85,T80,T90,T143,T54,T96,T71,T82,T53 page 16 test point T74,T175,T77,T89,T214,T95 page 17 test point T45,T74,T56,T139,T158,T157,T177,T176,T210,T144,T156,T49,T147,T146,T48,T47 ,T140,T141,T46 page 18 test point T61,T67,T70,T72,T52,T51,T73 page 32 test point T55 page 33 test point T153 page 36 test point T160,T161,T162,T163,T164,T165 page 37 test point T168,T169,T170 page 38 test point T167 page 39 test point T148,T390,T3902,T3905,T3906,T3907,T3909,T3910,T3903,T3904 page 40 test point T4001,T4005 page 41 test point T178,T179,T159,T166,T151,T152,T154 page 45 test point T33,T17,T16,T150,T13 page 50 test point T222,T219,T220,T221,T5002,T5003 page 55 test point T118,T122,T119,T125,T117,T121,T120,T124,T116,T123,T115,T113,T112,T114,T142,T149	New ATE test point change to 14 mils	X03
80		For AFTE	2008/07/07	W ME	Add AFTE test point "ZZ.AFT14.101" Page29 add AFTE test point T311,T312,T313,T314,T315,T316,T317,T318,T171,T172 Page 40 add AFTE test point T500~T529 "ZZ.AFT14.101" for Con5&CON4010 Page 42 add AFTE test point T356~T361 "ZZ.AFT14.101" for Con6610 Page 43 add AFTE test point T347,T348,T349,T350 "ZZ.AFT14.101" for Con663 Page 43 add AFTE test point T351,T352,T353 "ZZ.AFT14.101" for Con6617 Page 44 add AFTE test point T345~T346 "ZZ.AFT14.101" for Con6614 Page 45 add AFTE test point T341,T342,T343 "ZZ.AFT14.101" for Con11 Page 48 add AFTE test point T328,T329,T336 "ZZ.AFT14.101" for Con4801 Page 48 add AFTE test point T337,T338,T339,T340 change to "ZZ.AFT14.101" for Con7 Page 48 add AFTE test point T331,T330,T332,T333,T335,T334 "ZZ.AFT14.101" for Con5301 Page 56 add AFTE test point T320,T321,T322,T323 "ZZ.AFT14.101" for Con1 Page 57 add AFTE test point T188,T189,T190,T191,T192,T193 "ZZ.AFT14.101" for Con6615 Page 64 add AFTE test point T180~T187 "ZZ.AFT14.101" for PCon6400	New AFTE test point change to 14 mils	X03
81	18	Board ID	2008/07/07	W ME	Page 18 L49 change to "68.1R090.10A" ;	change bead dimension	X03
82	29	For ME	2008/07/07	W ME	page 29 con6607 change to wisntron P/N "20.20768.015"	ME modify PCB foot pin	X03
83	29	For SI	2008/07/07	W ME	Page29 L4909,L4910,L4911 CHANGE TO "68.00143.111" BLM18BA220SN1D-GP L4610,L4611 change to "63.R0033.L03" 0R DUMMY C6649,C6650;C6651;C6652;C6653;C6654	For SI issue	X03
84	31	For EE	2008/07/07	W ME	Page 31 remvoe J4 power GAP	Sparate HDD and ODD powe plane	X03
85	40	Board Id	2008/07/07	W ME	page 40 add R538(DY),R539(DY) connect to U29 Pin43 "BID2" for next stage board ID	for board ID	X03
86	65	For ME	2008/07/07	W ME	PAGE 65 REMOVE H33,H34	IR trace issue	X03
87	15	For SI	2008/07/07	W ME	page 15 change R275 to 47R"64.47R05.6DL" for ICH_AZ_CODEC_SDOUT;	For SI issue	X03
88	39	For SI	2008/07/08	W ME	R308,R308 change to 4.7K R	For SI issue	X03
89	65	For ME	2008/08/01	W ME	Page 65 H33,H34,H35 for IR Hold	IR HOLD change	A00
90	33	For SI	2008/08/01	W EE	Page 33 R545 change to 33R	For R5C833 SI Singel	A00
91	30	For SI	2008/08/01	W EE	Page 30 R3002 change to 820R Page 52 PC192 change to 0.1u	for HDMI singel	A00
92	52	For Boot	2008/08/01	W EE	Page 40 add R106 10K and R158 20K for LED_BL_DET	Drop	A00
93	40	For KB detect	2008/08/01	W EE	Page 40 remove BID2 change Board VER to 00	add KB B/L Detect	A00
94	40	For Board ID	2008/08/01	W EE	Page 54 add R417 1KR RESET_OUT# to GND	Board change	A00
95	54	For Boot	2008/08/01	W EE	WWAN remove	for Boot	A00
96	16,21 37,57	Remove WWAN	2008/08/01	W EE	Page 16 DY R356 ,RP4 connect SB_WWAN_PCIE_RST# to +3.3V_RUN Page 16 DY C443,C439 for WWAN remove Page 21 DY R2118,R66 Page 37 DY CON6605,C6644,C6645,C6646,C6647,C6648,C6636,C6637,C6638,C6639,C6640,C6641,C6642,C6643,CE17,CE18 Page 57 DY CON6615	Remove WWAN	A00
97	13,36	For Layout	2008/08/01	W EE	Page 36 Remove J3,Page 13 remove J4	Remove J3 modify for Layout	

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Taipei Hsien 221, Taiwan, R.O.C.

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