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NSWAA/NTWAA

Liverpool 10G

Sunderland 10G

LA-5322P REV 1.0 Schematic

Intel Arrandale /IBEX PEAK

2009-12-22 Rev 1.0

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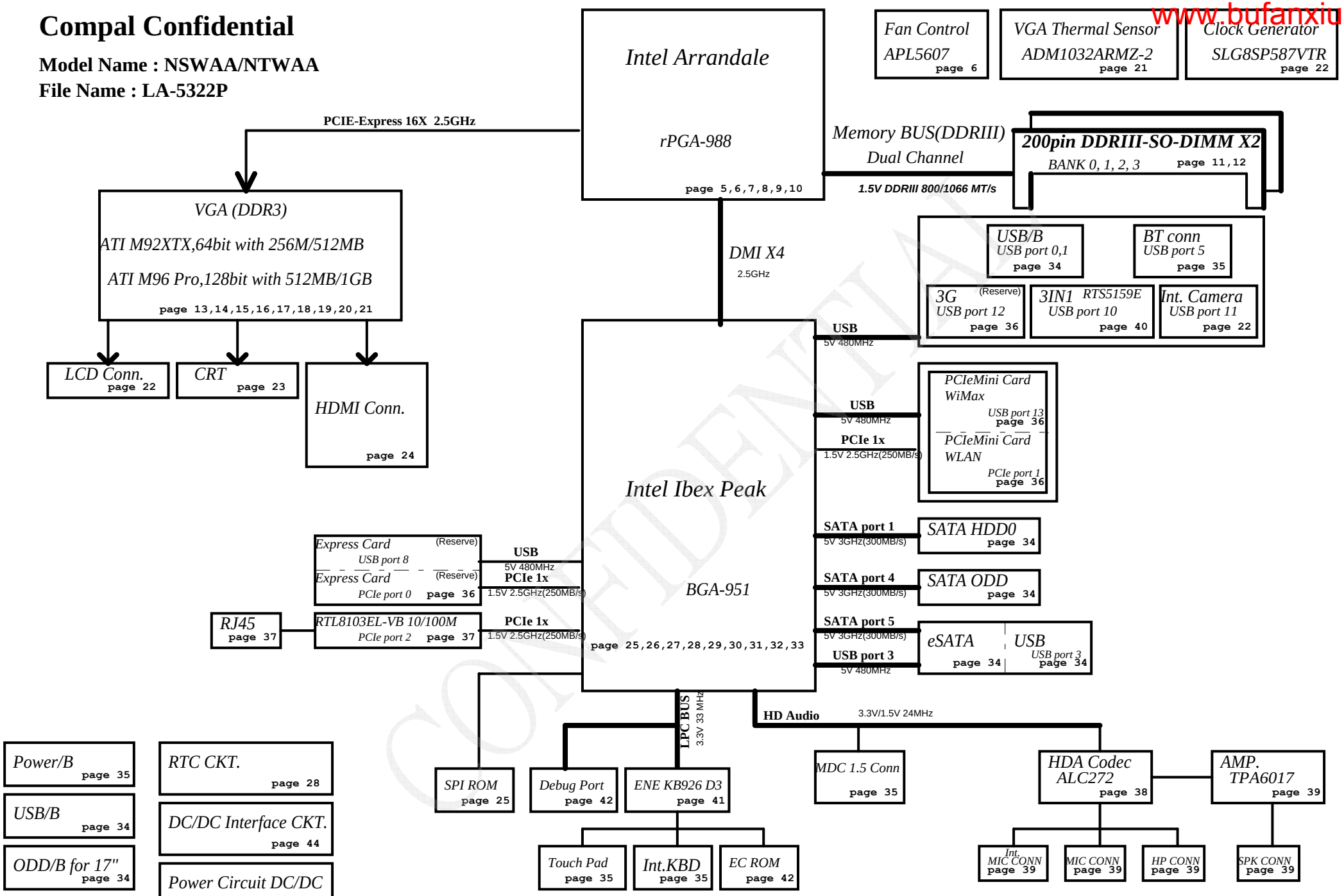
Model Name : NSWAA/NTWAA
File Name : LA-5322P



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NSWAA Liverpool Intel Arrandale (Discrete)
NTWAA Sunderland Intel Arrandale (Discrete)

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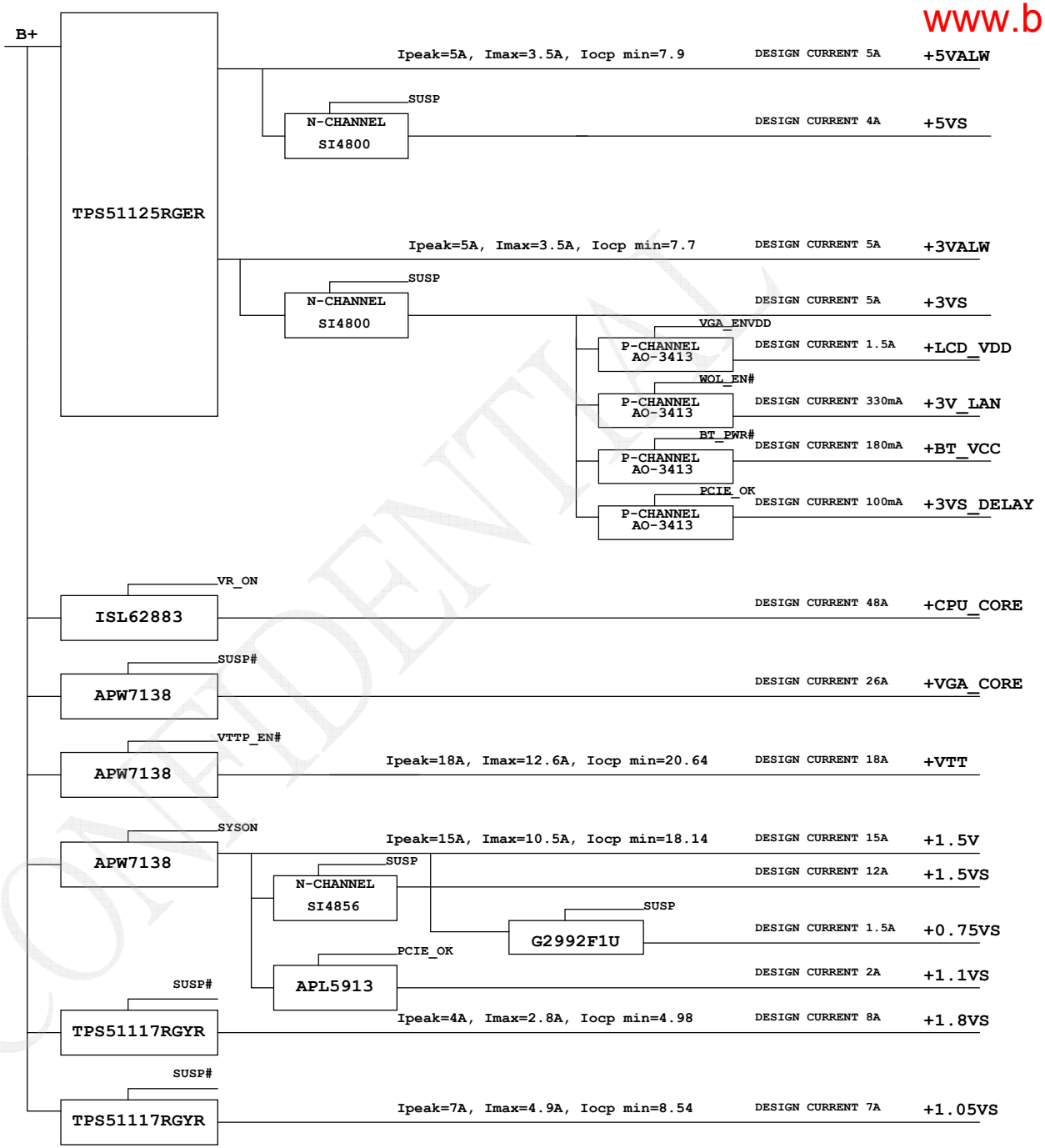

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	Express Card	MIC	HDMI	Panel		M1/M3	
description	(B)		(E)		(Y)				
explain	Bluetooth	MDC	New Card	MIC	HDMI	16"	17"	M1	M3
BTO	BT@	MDC@	NEW@	MIC@	HDMI@	16@	17@	M1@	M3@

Function	Mini Card	VRAM			GPU	
description						
explain	WIRELESS	256M	512M	1G	M92 XTX	M96 Pro
BTO	WLAN@	2PCS@	4PCS@	8PCS@	M92XTX@	M96PRO@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
+3VS	PCH	0100 110x b

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

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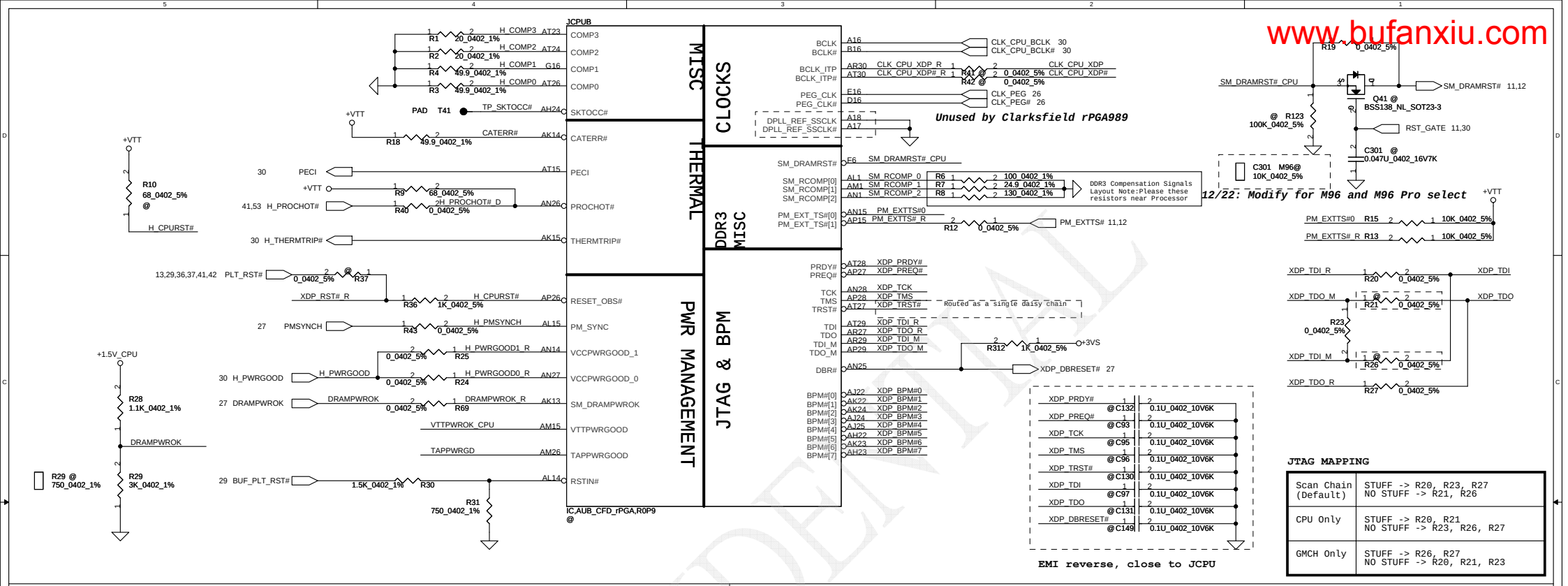

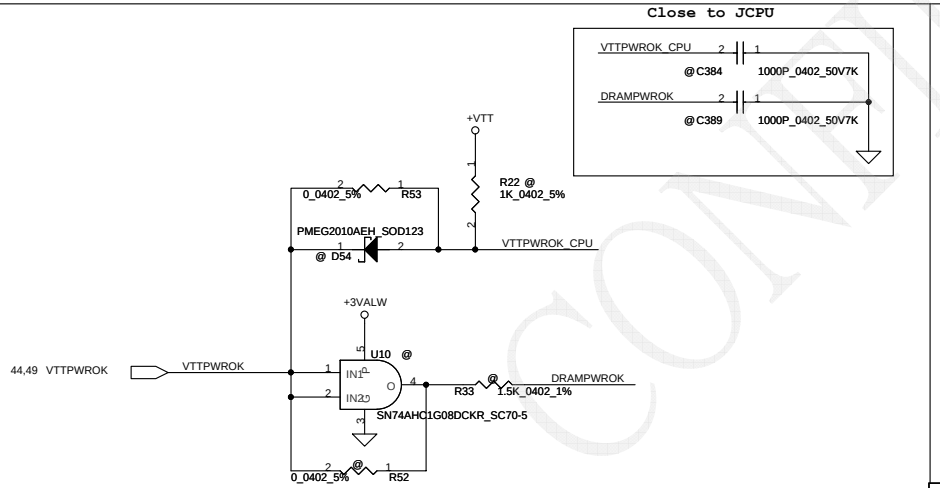

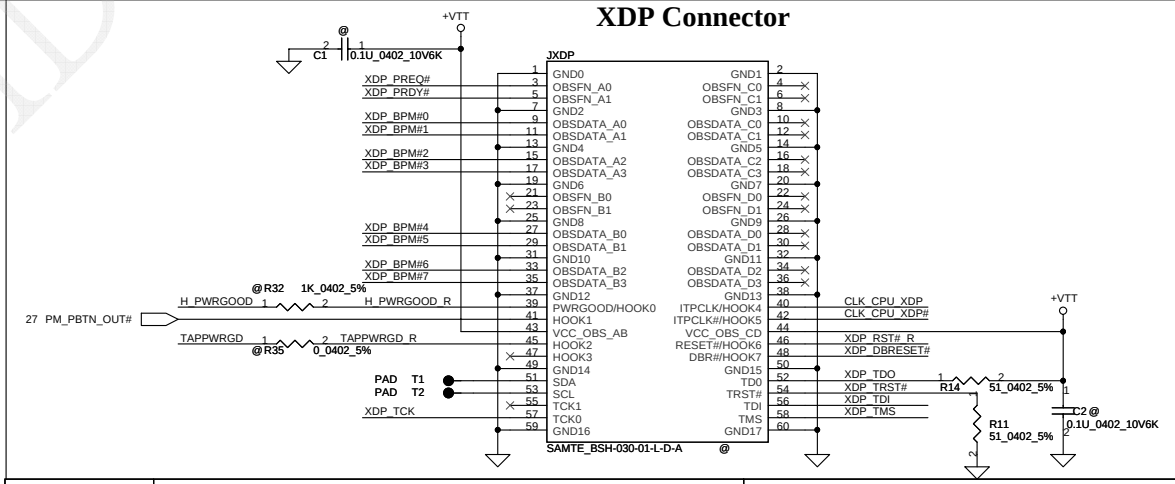

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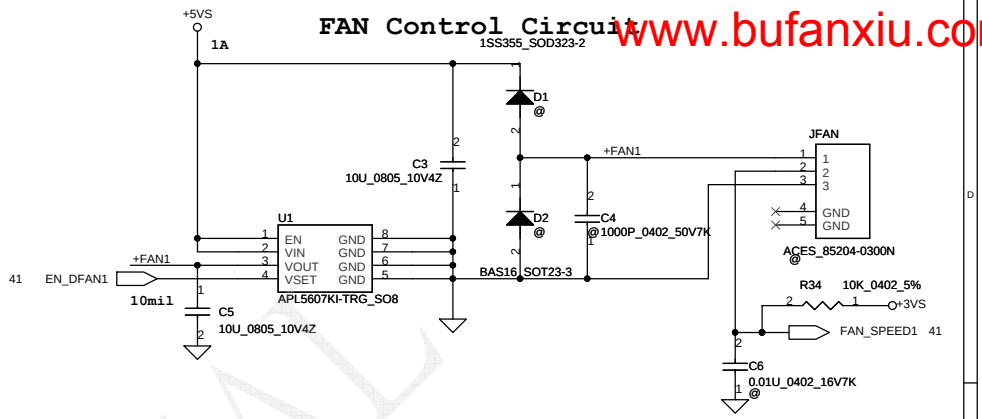
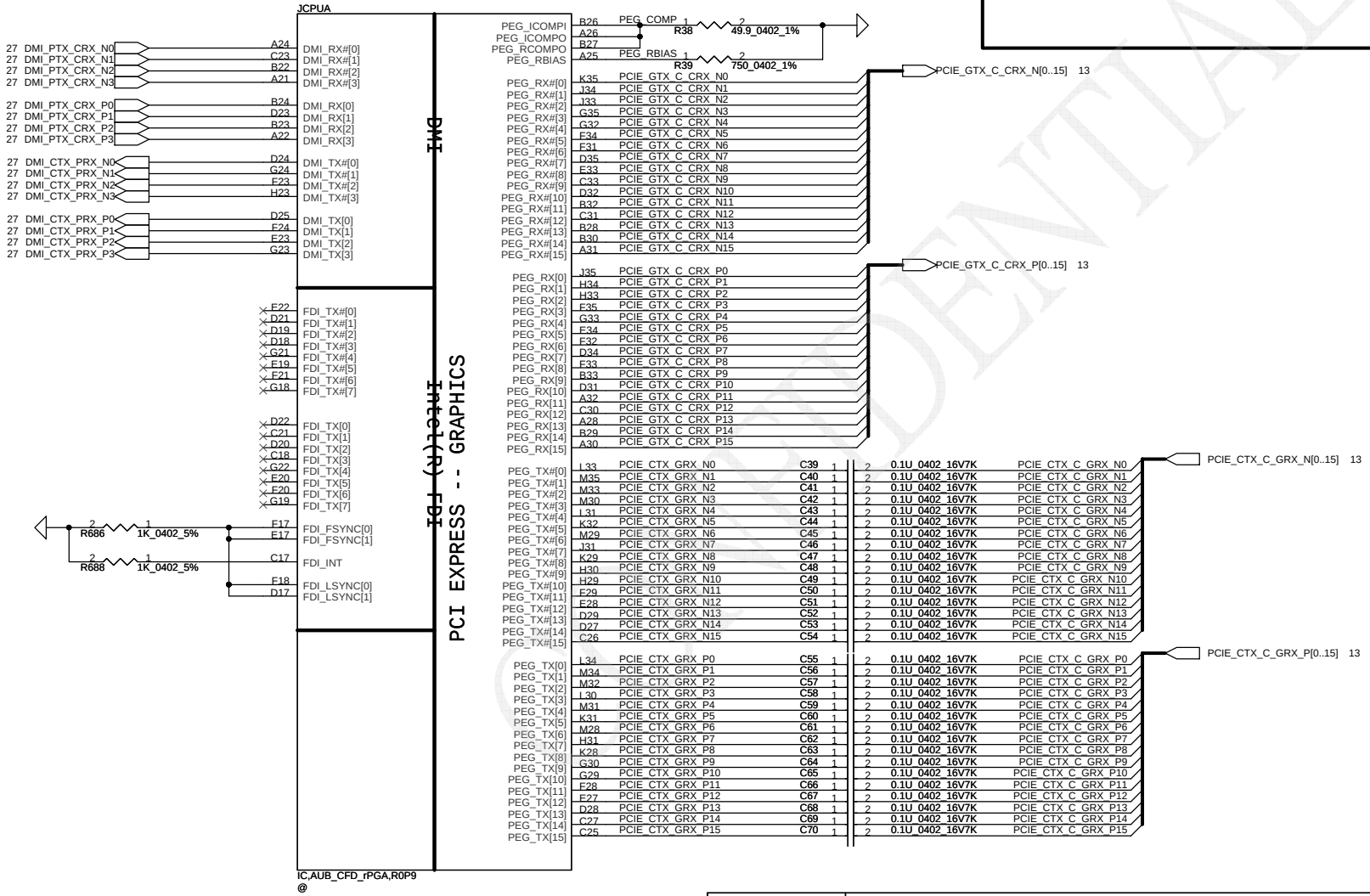
FAN Control Circuit



JCPUA



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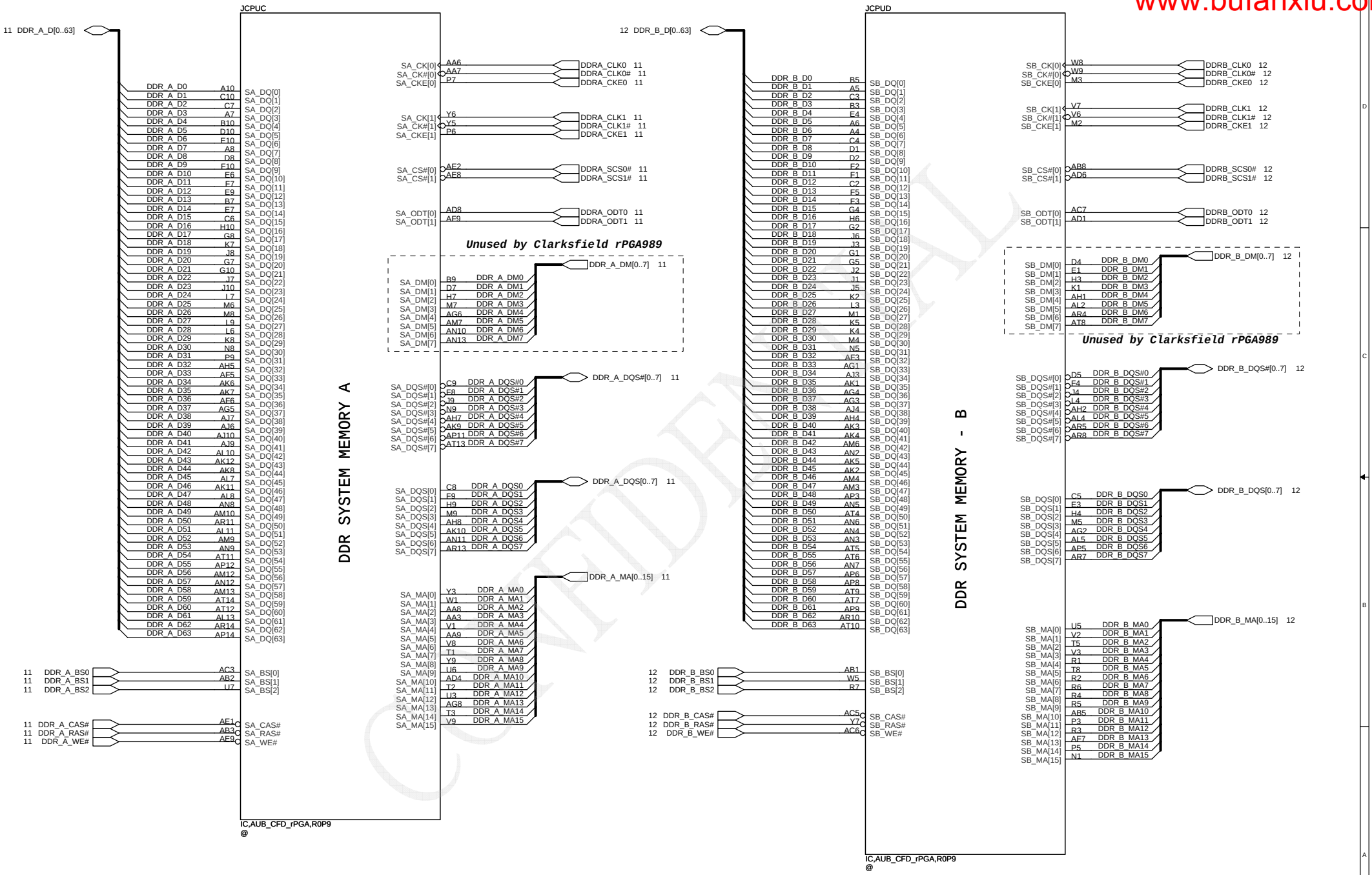

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Material Note (+VTT):
330uF/ 6mohm, number are 3,
power x1, HW x2

JCPUF

Clarksfield: 65A
Auburndale:48A

Clarksfield: 21A
Auburndale:18A

+CPU_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+VTT

@ C80 330U_D2E_2.5VM_R6M
@ C82 330U_D2E_2.5VM_R6M
@ C84 330U_D2E_2.5VM_R6M
C87 22U_0805_6.3V6M
C91 22U_0805_6.3V6M

C81 C83 C85 C89 C88 C90 C92 C94 — 10U_0805_10V4K (C94: 10U_0805_10V4K@)

(Place these capacitors under CPU socket Edge, top layer)

Co-layout with C80, C82

+VTT
C144 390U_2.5V_M_R10
C159 390U_2.5V_M_R10

5/25: Add for power team request.

+CPU_CORE
C158 @ C150 @ C128 C127 C120 C118 C119 C117 C129 — 22U_0805_6.3V6M

(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE
C71 C72 C73 C74 C75 C76 C77 C78 C79 — 10U_0805_10V4K

(Place these capacitors under CPU socket, top layer)

+CPU_CORE
C98 C99 C100 C101 C102 C103 C104 — 10U_0805_10V4K

(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE
C105 C106 C107 C108 C109 C110 — 22U_0805_6.3V6M
C111 C112 C113 C114 C115 C116 — 22U_0805_6.3V6M

TOP side (under inductor)

+CPU_CORE
C121 C124 C122 @ C123 C125 @ C126 @ — 330U_D2_2.5VY_R9M
C218 560U_2.5V_M @
Co-layout with C126

+CPU_CORE
C148 330U_D2_2.5VY_R9M

9/11: Add for power team request.

POWER

CPU VIDS

PSI# AN33 → H_PSI# 53

VID[0] AK35 → CPU_VID0 53
VID[1] AK33 → CPU_VID1 53
VID[2] AK34 → CPU_VID2 53
VID[3] AL35 → CPU_VID3 53
VID[4] AL33 → CPU_VID4 53
VID[5] AM33 → CPU_VID5 53
VID[6] AM35 → CPU_VID6 53

PROC_DPRSLPVR AM34 → H_DPRSLPVR_R R62 0_0402_5% → H_DPRSLPVR 53

VTT_SELECT G15 → H_VTTSELECT 49

CRB default setting:
VID[6:0]=[0100111]

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V

SENSE LINES

ISENSE AN35 → IMVP_IMON 53

VCC_SENSE AJ34 VCCSENSE_R R65 0_0402_5% → VCCSENSE 53
VSS_SENSE AJ35 VSSSENSE_R R66 0_0402_5% → VSSSENSE 53

R64 100_0402_1% → +CPU_CORE
R67 100_0402_1%

VTT_SENSE B15 → VTT_SENSE 49
VSS_SENSE_VTT A15 → VSS_SENSE_VTT 49

near CPU

IC,AUB_CFD_rPGA,R0P9
@

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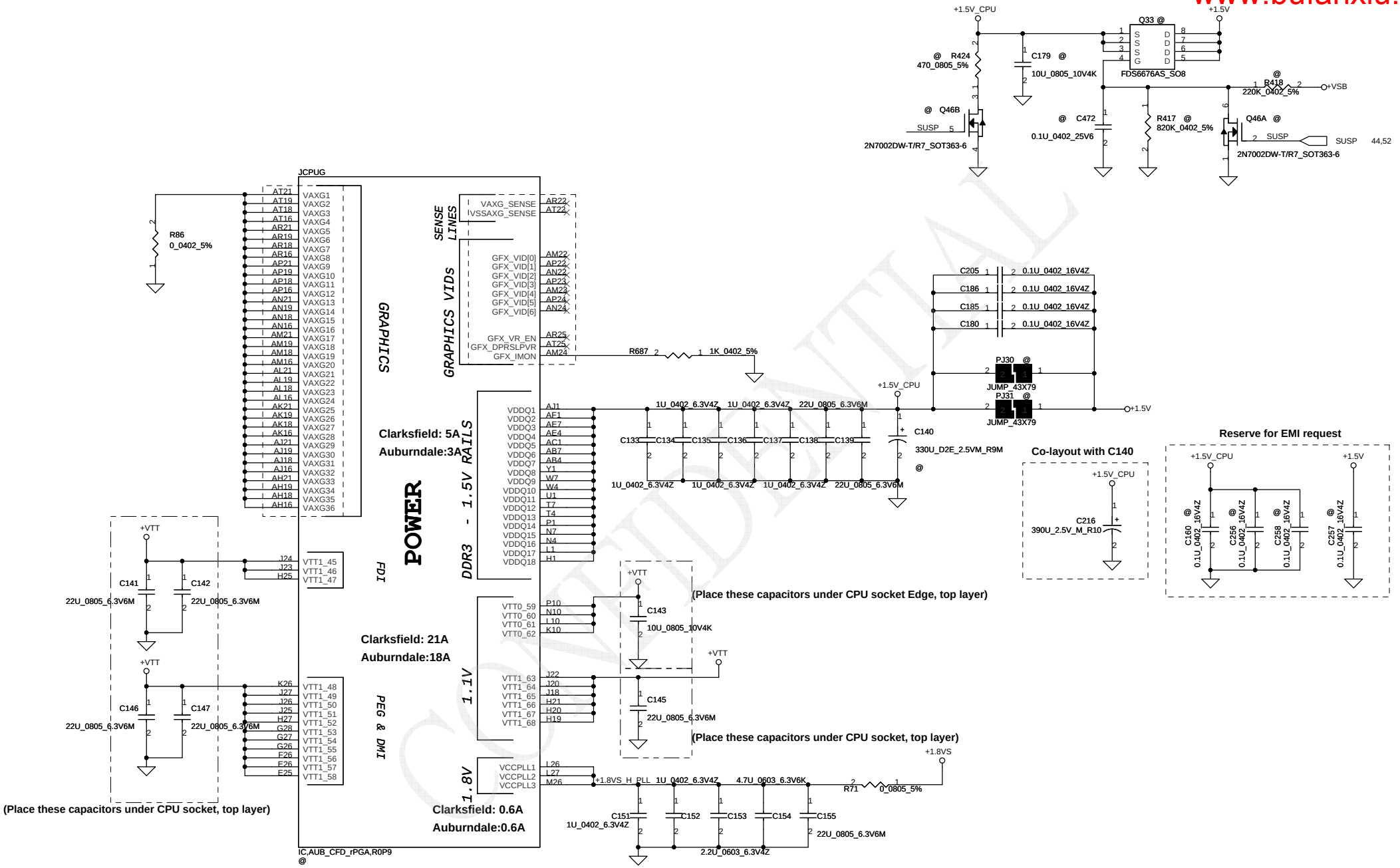

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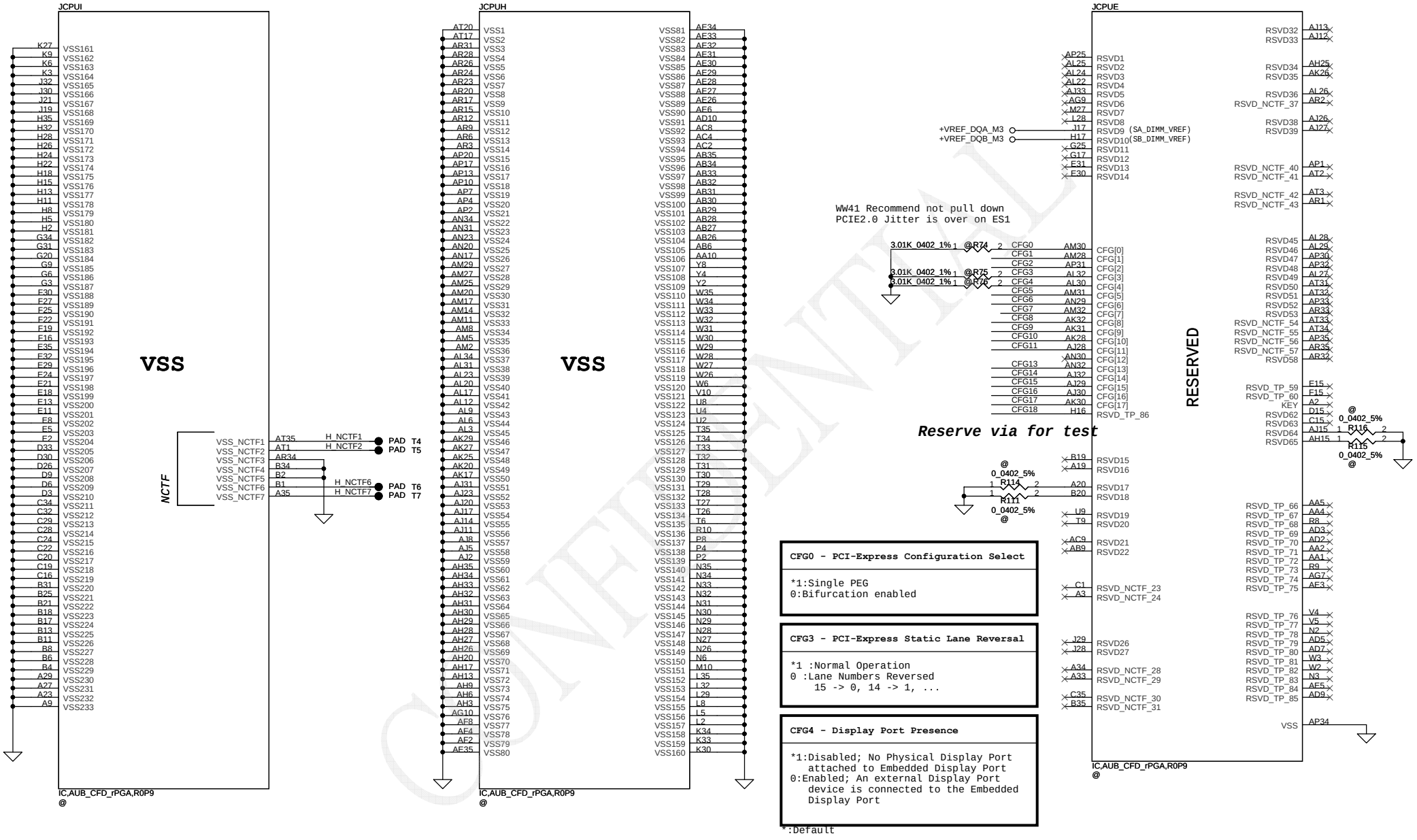

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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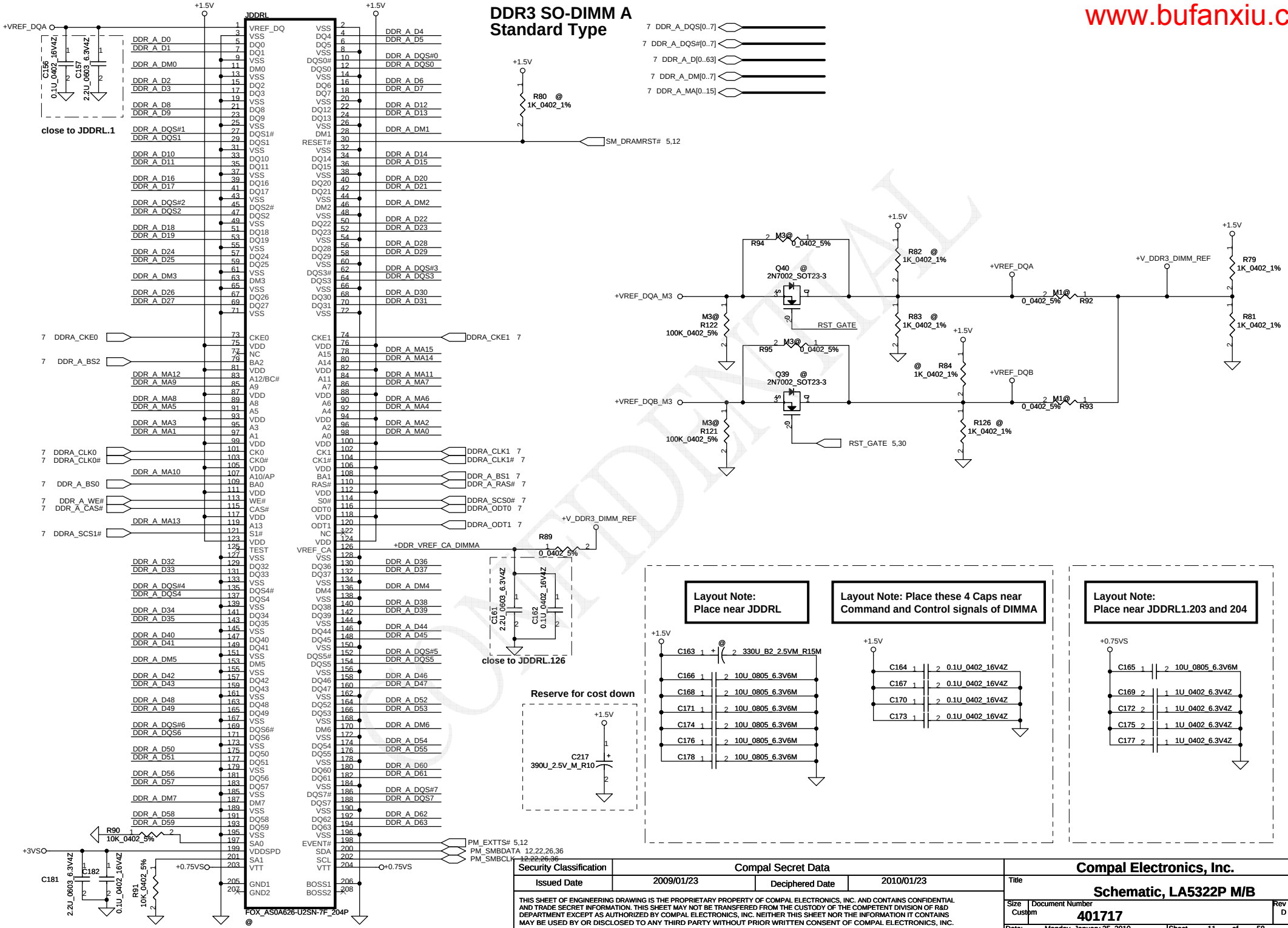
DDR3 SO-DIMM A
Standard Type



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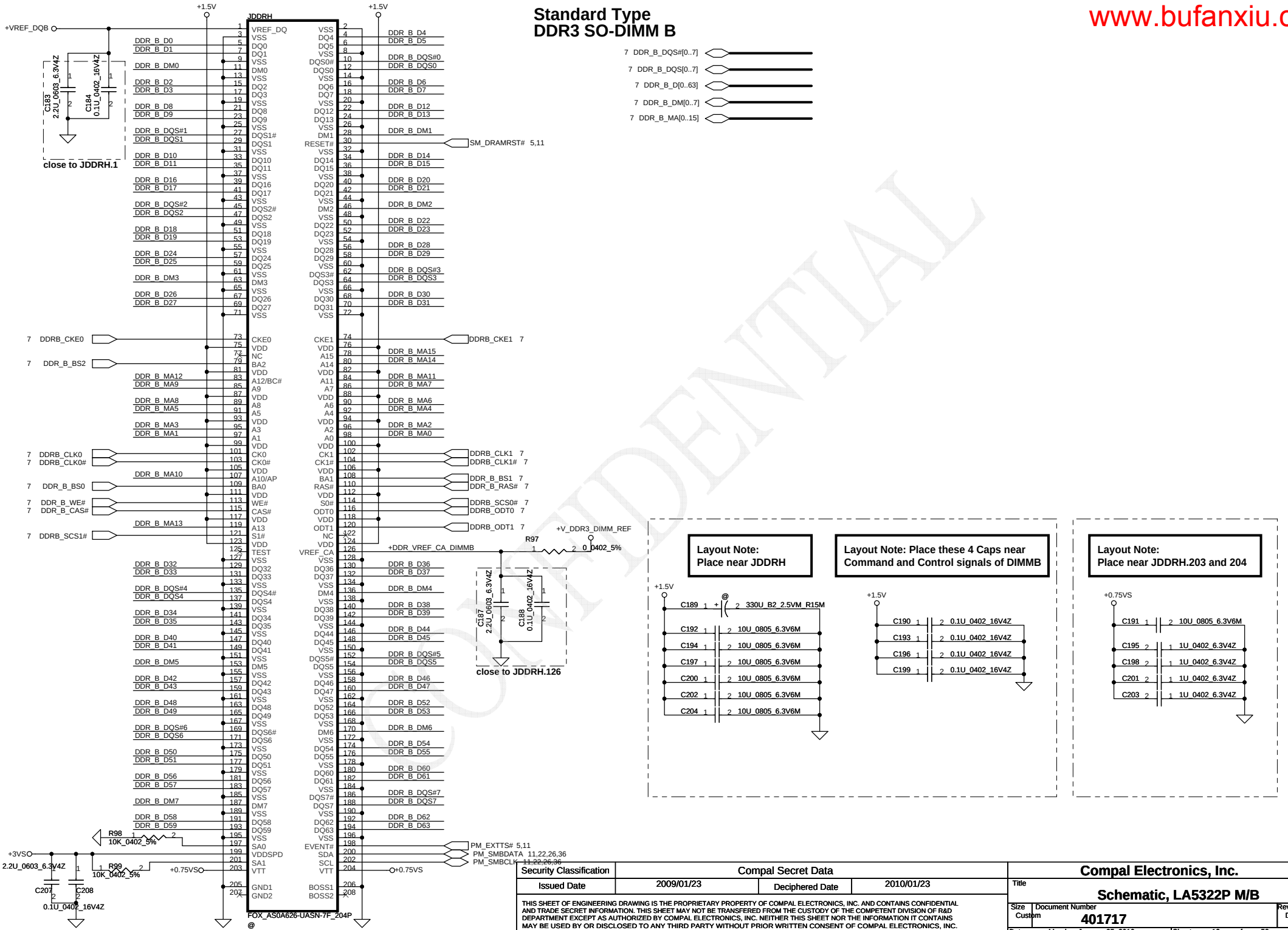
Standard Type
DDR3 SO-DIMM B

7 DDR_B_DQS#[0..7]
7 DDR_B_DQS[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DM[0..7]
7 DDR_B_MA[0..15]



Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

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6 PCIE_GTX_C_CRX_P[0..15] → PCIE_GTX_C_CRX_P[0..15]
6 PCIE_GTX_C_CRX_N[0..15] → PCIE_GTX_C_CRX_N[0..15]
6 PCIE_CTX_C_GRX_P[0..15] → PCIE_CTX_C_GRX_P[0..15]
6 PCIE_CTX_C_GRX_N[0..15] → PCIE_CTX_C_GRX_N[0..15]

UV1A

LANE Reversal

PCIE_CTX_C_GRX_P15	AA38	PCIE_RX0P	
PCIE_CTX_C_GRX_N15	Y37	PCIE_RX0N	
PCIE_CTX_C_GRX_P14	Y35	PCIE_RX1P	
PCIE_CTX_C_GRX_N14	W36	PCIE_RX1N	
PCIE_CTX_C_GRX_P13	W38	PCIE_RX2P	
PCIE_CTX_C_GRX_N13	V37	PCIE_RX2N	
PCIE_CTX_C_GRX_P12	V35	PCIE_RX3P	
PCIE_CTX_C_GRX_N12	U36	PCIE_RX3N	
PCIE_CTX_C_GRX_P11	U38	PCIE_RX4P	
PCIE_CTX_C_GRX_N11	T37	PCIE_RX4N	
PCIE_CTX_C_GRX_P10	T35	PCIE_RX5P	
PCIE_CTX_C_GRX_N10	R36	PCIE_RX5N	
PCIE_CTX_C_GRX_P9	R38	PCIE_RX6P	
PCIE_CTX_C_GRX_N9	P37	PCIE_RX6N	
PCIE_CTX_C_GRX_P8	P35	PCIE_RX7P	
PCIE_CTX_C_GRX_N8	N36	PCIE_RX7N	
PCIE_CTX_C_GRX_P7	N38	PCIE_RX8P	
PCIE_CTX_C_GRX_N7	M37	PCIE_RX8N	
PCIE_CTX_C_GRX_P6	M35	PCIE_RX9P	
PCIE_CTX_C_GRX_N6	L36	PCIE_RX9N	
PCIE_CTX_C_GRX_P5	L38	PCIE_RX10P	
PCIE_CTX_C_GRX_N5	K37	PCIE_RX10N	
PCIE_CTX_C_GRX_P4	K35	PCIE_RX11P	
PCIE_CTX_C_GRX_N4	J36	PCIE_RX11N	
PCIE_CTX_C_GRX_P3	J38	PCIE_RX12P	
PCIE_CTX_C_GRX_N3	H37	PCIE_RX12N	
PCIE_CTX_C_GRX_P2	H35	PCIE_RX13P	
PCIE_CTX_C_GRX_N2	G36	PCIE_RX13N	
PCIE_CTX_C_GRX_P1	G38	PCIE_RX14P	
PCIE_CTX_C_GRX_N1	F37	PCIE_RX14N	
PCIE_CTX_C_GRX_P0	F35	PCIE_RX15P	
PCIE_CTX_C_GRX_N0	E37	PCIE_RX15N	

PCI EXPRESS INTERFACE

LANE Reversal

PCIE_TX0P	Y33	PCIE_GTX_CRX_P15	C38	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P15
PCIE_TX0N	Y32	PCIE_GTX_CRX_N15	C22	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N15
PCIE_TX1P	W33	PCIE_GTX_CRX_P14	C37	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P14
PCIE_TX1N	W32	PCIE_GTX_CRX_N14	C21	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N14
PCIE_TX2P	U33	PCIE_GTX_CRX_P13	C36	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P13
PCIE_TX2N	U32	PCIE_GTX_CRX_N13	C20	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N13
PCIE_TX3P	U30	PCIE_GTX_CRX_P12	C35	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P12
PCIE_TX3N	U29	PCIE_GTX_CRX_N12	C19	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N12
PCIE_TX4P	T33	PCIE_GTX_CRX_P11	C34	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P11
PCIE_TX4N	T32	PCIE_GTX_CRX_N11	C18	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N11
PCIE_TX5P	T30	PCIE_GTX_CRX_P10	C33	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P10
PCIE_TX5N	T29	PCIE_GTX_CRX_N10	C17	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N10
PCIE_TX6P	P33	PCIE_GTX_CRX_P9	C32	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P9
PCIE_TX6N	P32	PCIE_GTX_CRX_N9	C16	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N9
PCIE_TX7P	P30	PCIE_GTX_CRX_P8	C31	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P8
PCIE_TX7N	P29	PCIE_GTX_CRX_N8	C15	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N8
PCIE_TX8P	N33	PCIE_GTX_CRX_P7	C30	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P7
PCIE_TX8N	N32	PCIE_GTX_CRX_N7	C14	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N7
PCIE_TX9P	N30	PCIE_GTX_CRX_P6	C29	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P6
PCIE_TX9N	N29	PCIE_GTX_CRX_N6	C13	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N6
PCIE_TX10P	L33	PCIE_GTX_CRX_P5	C28	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P5
PCIE_TX10N	L32	PCIE_GTX_CRX_N5	C12	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N5
PCIE_TX11P	L30	PCIE_GTX_CRX_P4	C27	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P4
PCIE_TX11N	L29	PCIE_GTX_CRX_N4	C11	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N4
PCIE_TX12P	K33	PCIE_GTX_CRX_P3	C26	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P3
PCIE_TX12N	K32	PCIE_GTX_CRX_N3	C10	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N3
PCIE_TX13P	J33	PCIE_GTX_CRX_P2	C25	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P2
PCIE_TX13N	J32	PCIE_GTX_CRX_N2	C9	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N2
PCIE_TX14P	K30	PCIE_GTX_CRX_P1	C24	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P1
PCIE_TX14N	K29	PCIE_GTX_CRX_N1	C8	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N1
PCIE_TX15P	H33	PCIE_GTX_CRX_P0	C23	0.1U_0402_16V7K	PCIE_GTX_C_CRX_P0
PCIE_TX15N	H32	PCIE_GTX_CRX_N0	C7	0.1U_0402_16V7K	PCIE_GTX_C_CRX_N0

CLOCK

26 CLK_PCIE_VGA → AB35 PCIE_REFCLKP
26 CLK_PCIE_VGA# → AA36 PCIE_REFCLKN

Reserve for Park and Madison support.

AJ21 NC#1
AK21 NC#2
AH16 NC_PWRGOOD

RV54 10K_0402_5%

5,29,36,37,41,42 PLT_RST# → AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 — RV1 1.27K_0402_1%
PCIE_CALRN Y29 — RV2 2K_0402_1% — +1.1VS

216-0729002 A12 M96_BGA962

M96PRO@

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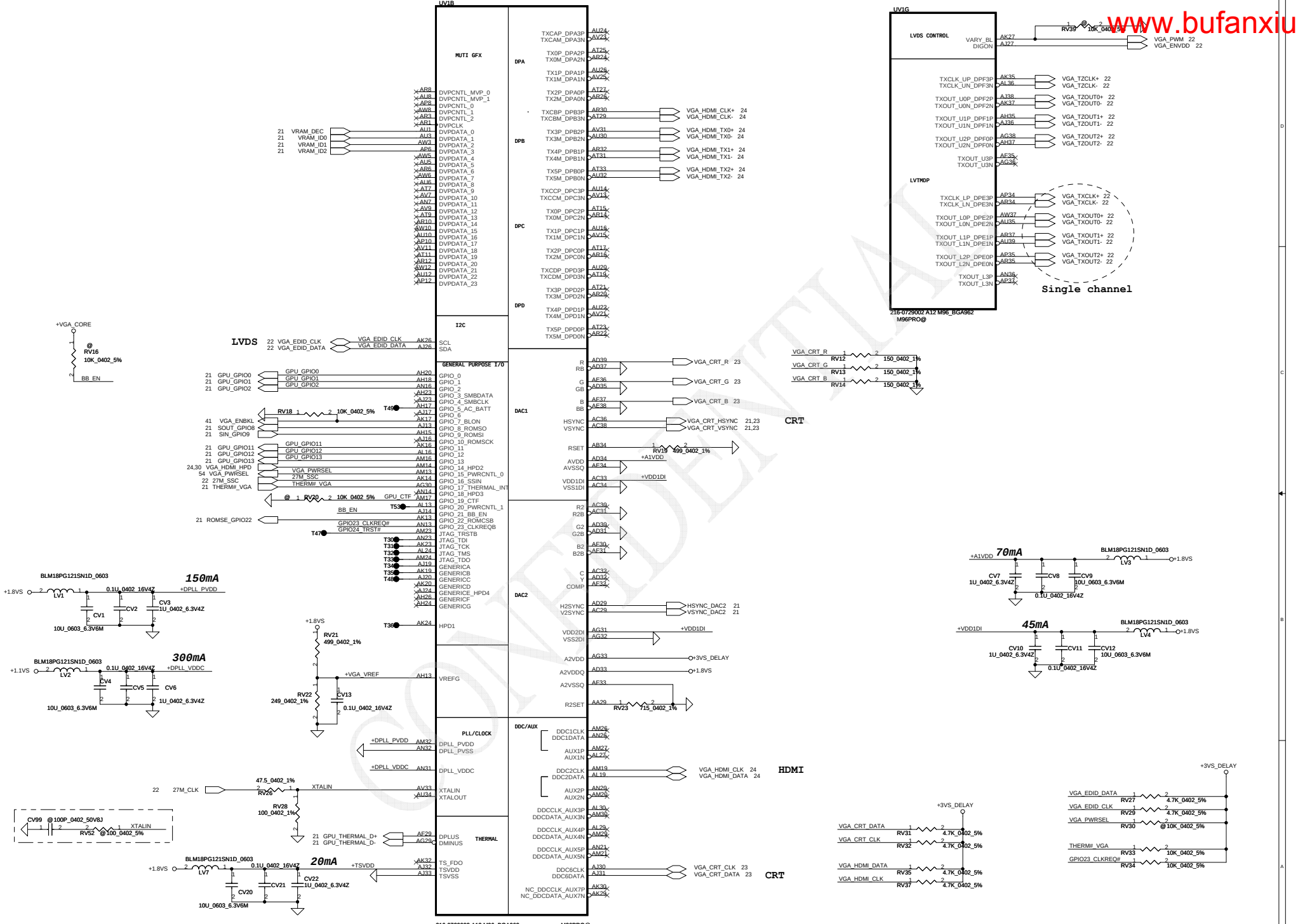

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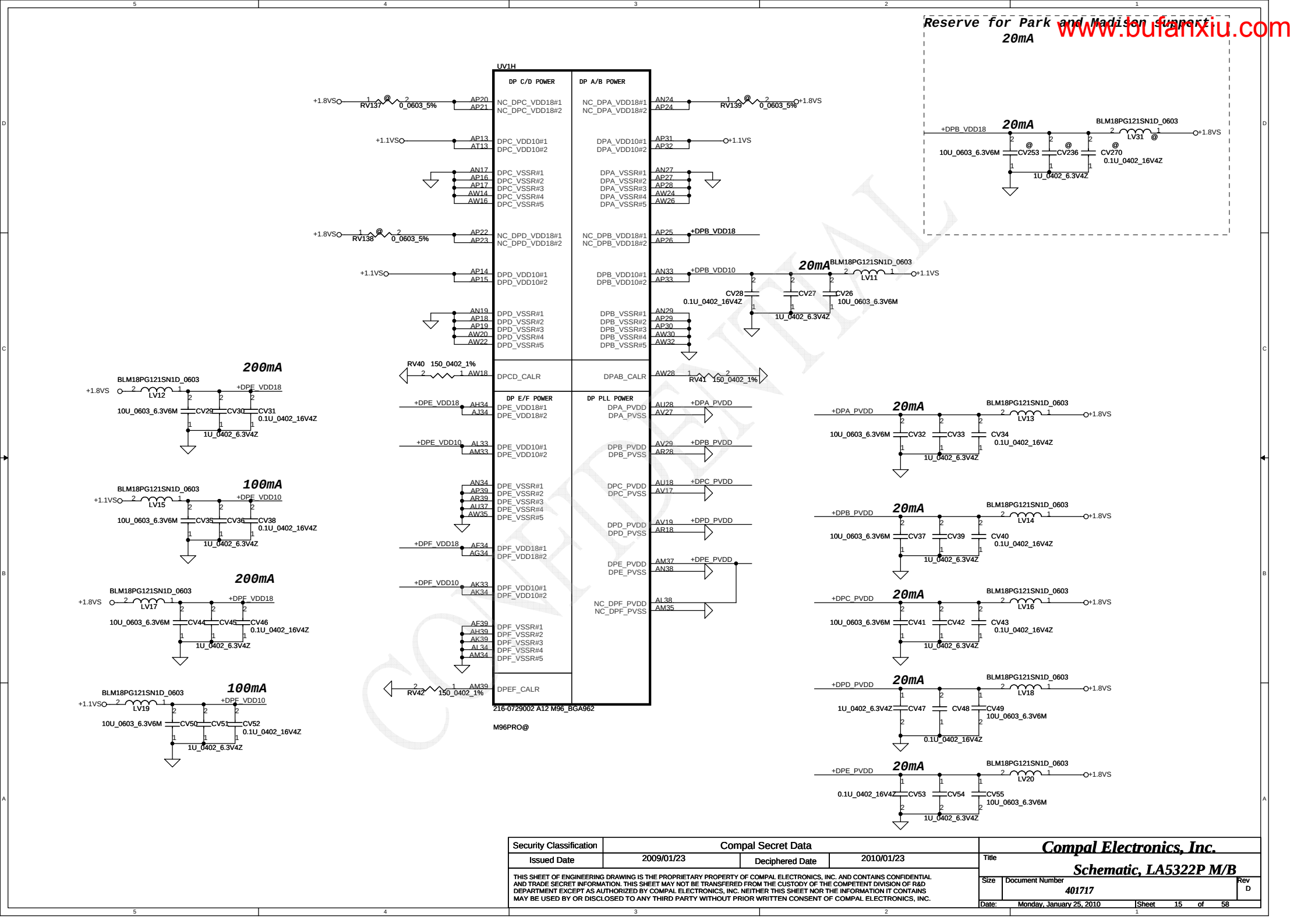

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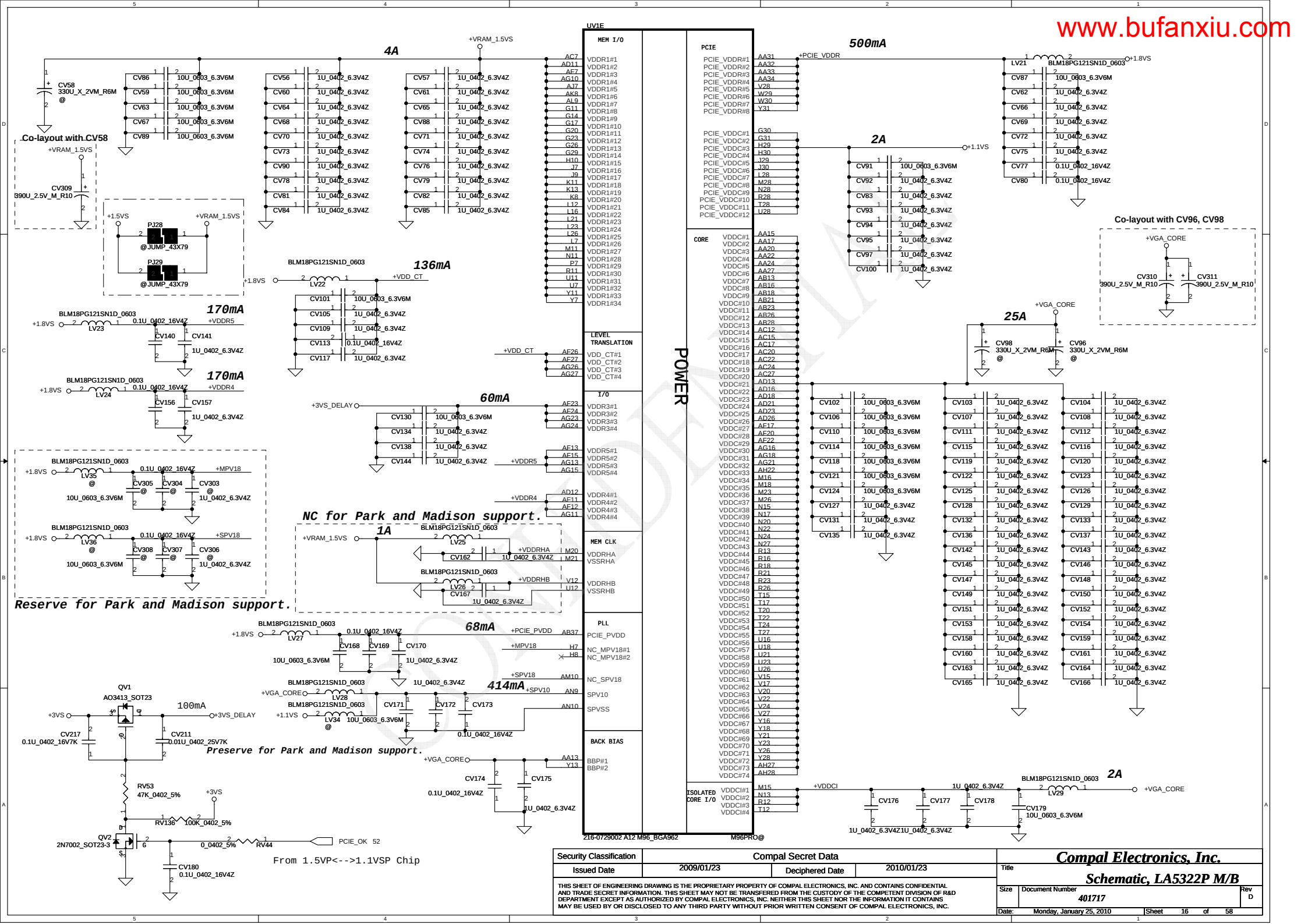

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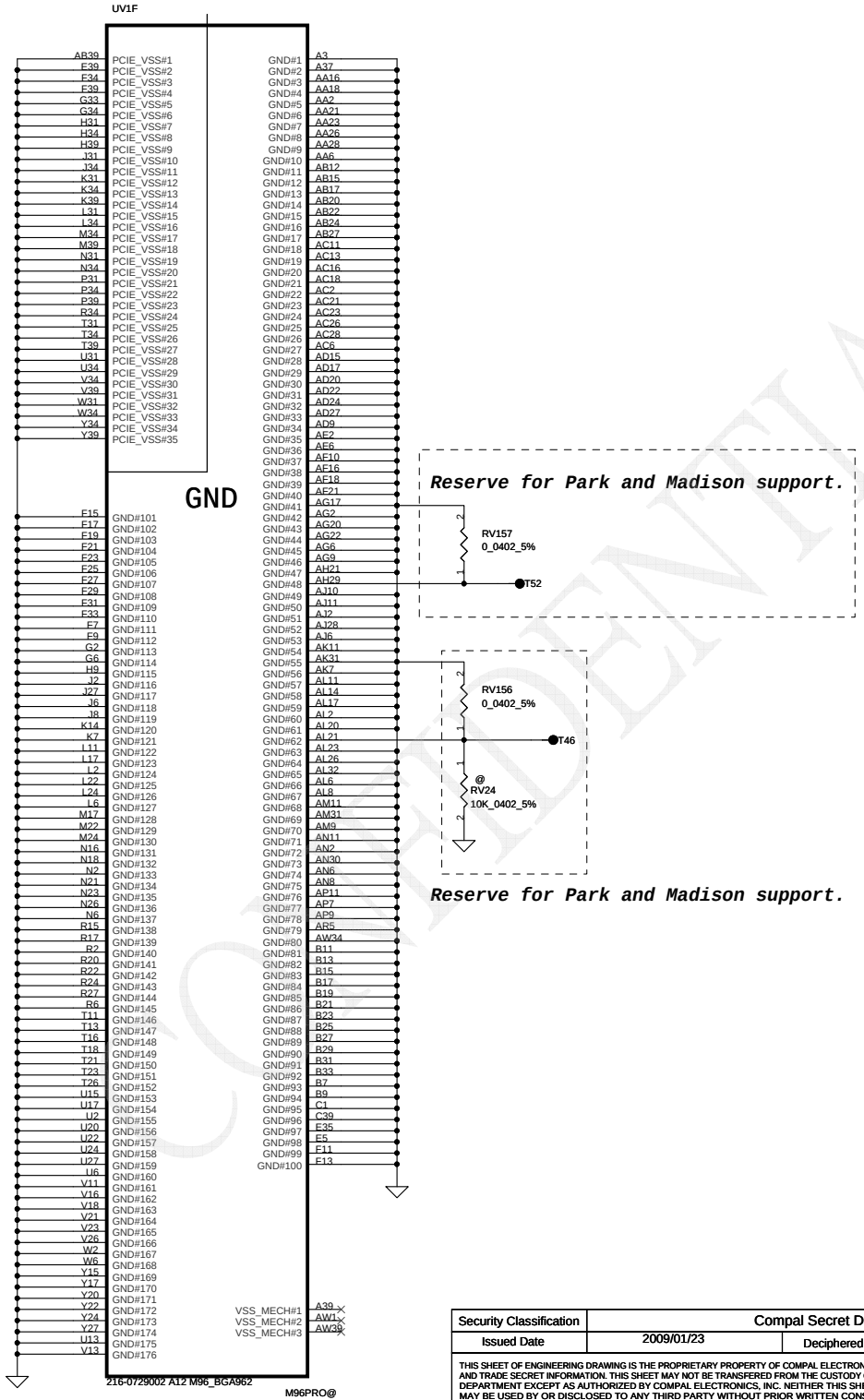

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M92-M2 uses memory group B only

UV1C

MEMORY INTERFACE A

UV1D

MEMORY INTERFACE B

Close to pin L18

Close to pin L20

Close to pin Y12

Close to pin AA12

Reserve for Park and Madison support.

Reserve for Park and Madison support.

216-0729002 A12 M96_BGA962

M96PRO@

216-0729002 A12 M96_BGA962

M96PRO@

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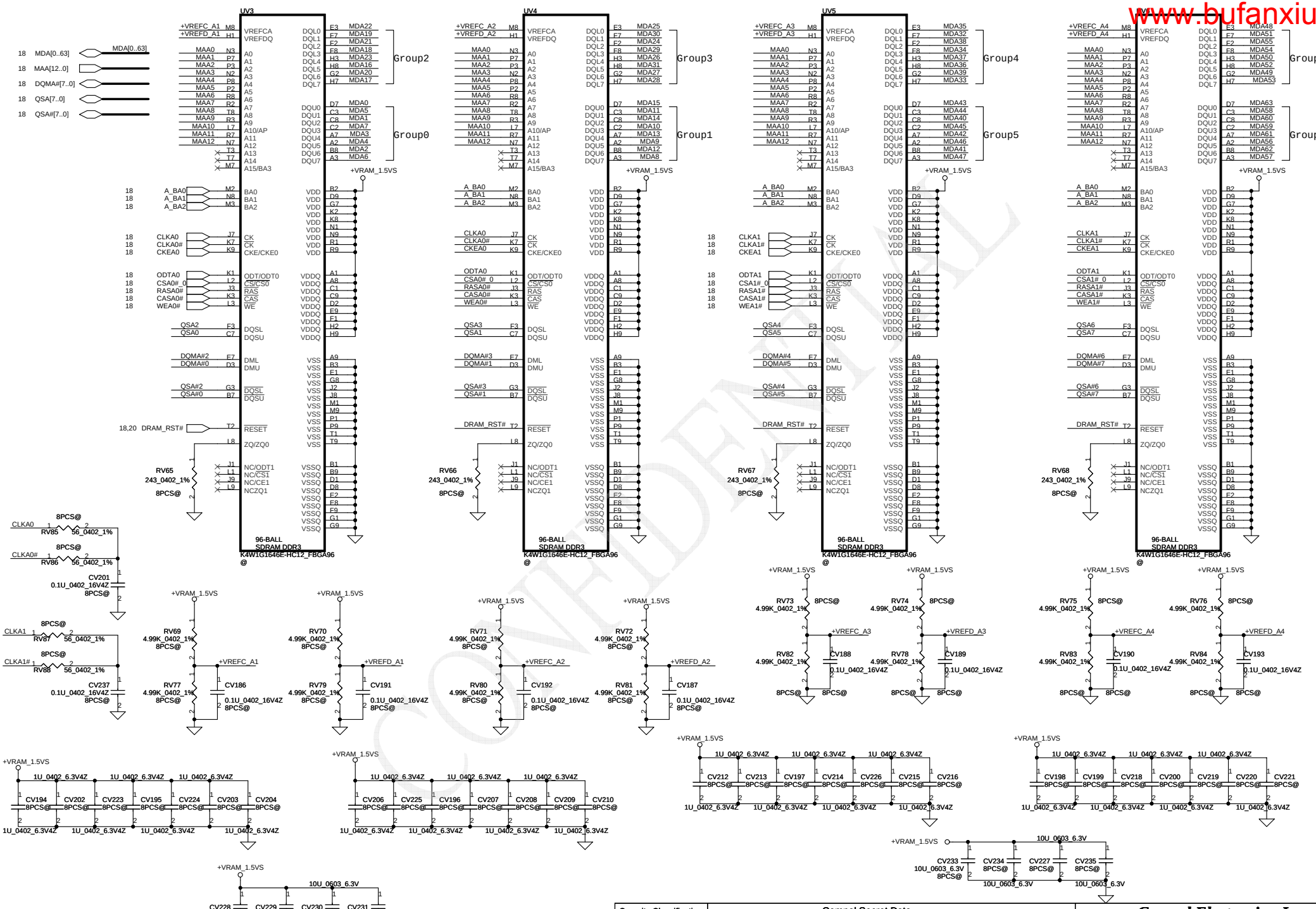

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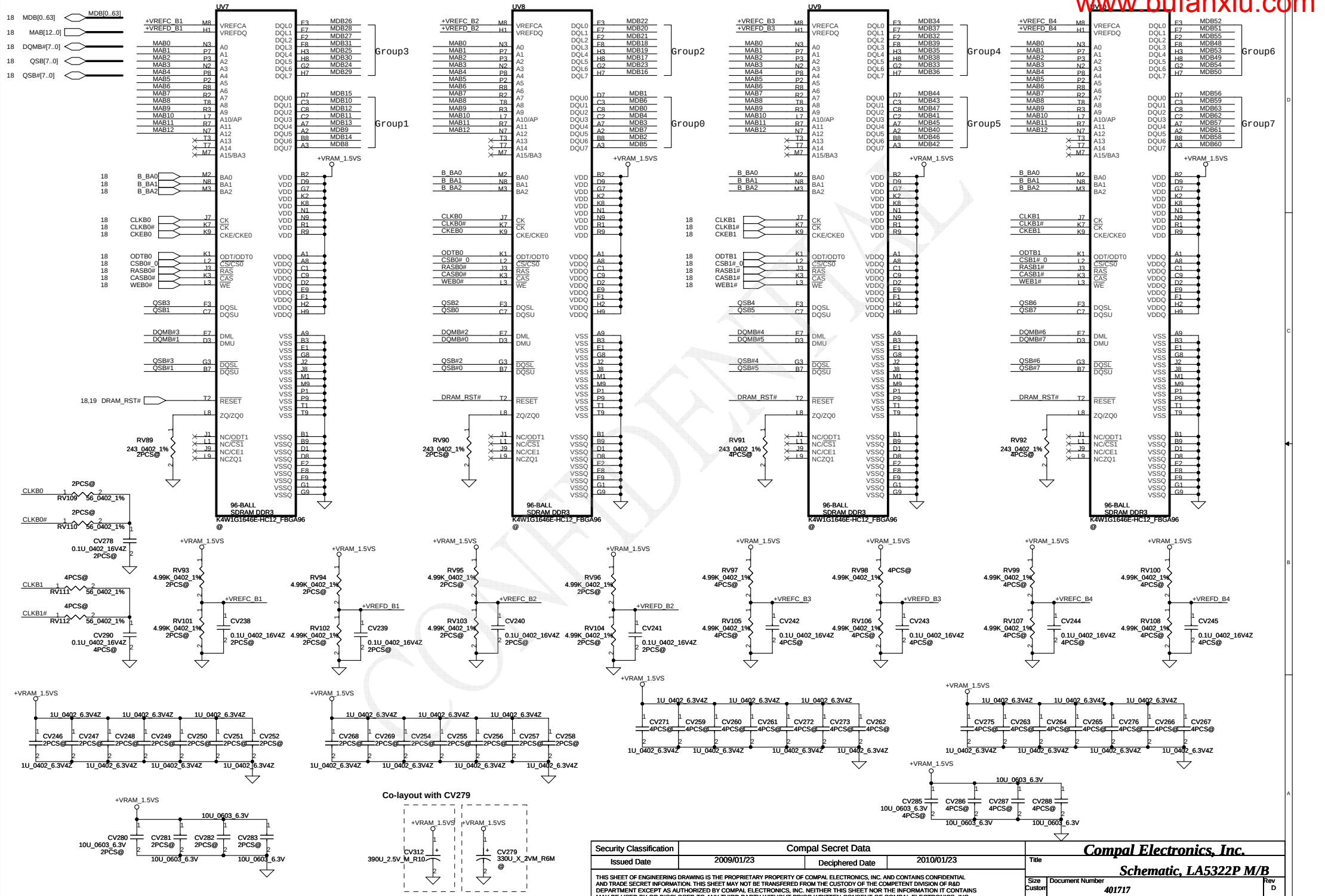

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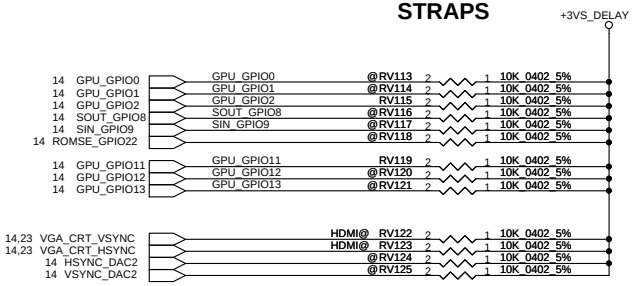
STRAPS

GPU by the system BIOS		GPU by VBIOS
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]
0 0 0	128MB	1 0 0 (M25P05A)
0 0 1	256MB	
0 1 0	64MB	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSYNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
RSVD	HSYNC_DAC2		0
RSVD	GENERICC		0

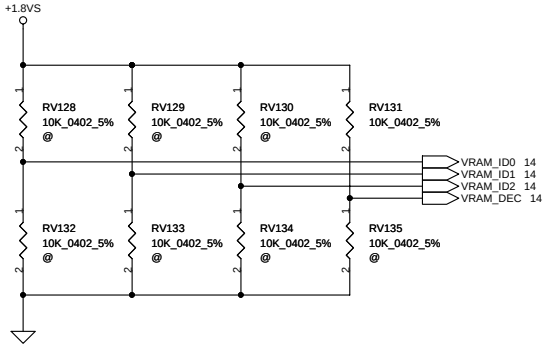
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSYNC_DAC2	GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

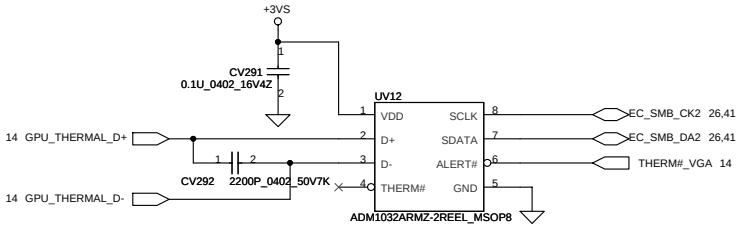
GPIO_28_TDO	GPIO21_BB_EN



DDR3	
VRAM_DEC	1

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
		M96-M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 1
		M92-M2 XT	256M 64Mx16 (x2)	HYN H5TQ1G63BFR-12C	SA000032400	0 1 0
		M96-M2	1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	0 1 1
		M92-M2 XT	512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 0
		M92-M2 XT	256M 64Mx16 (x2)	SAM K4W1G1646E-HC12	SA000035700	1 0 1

External VGA Thermal Sensor



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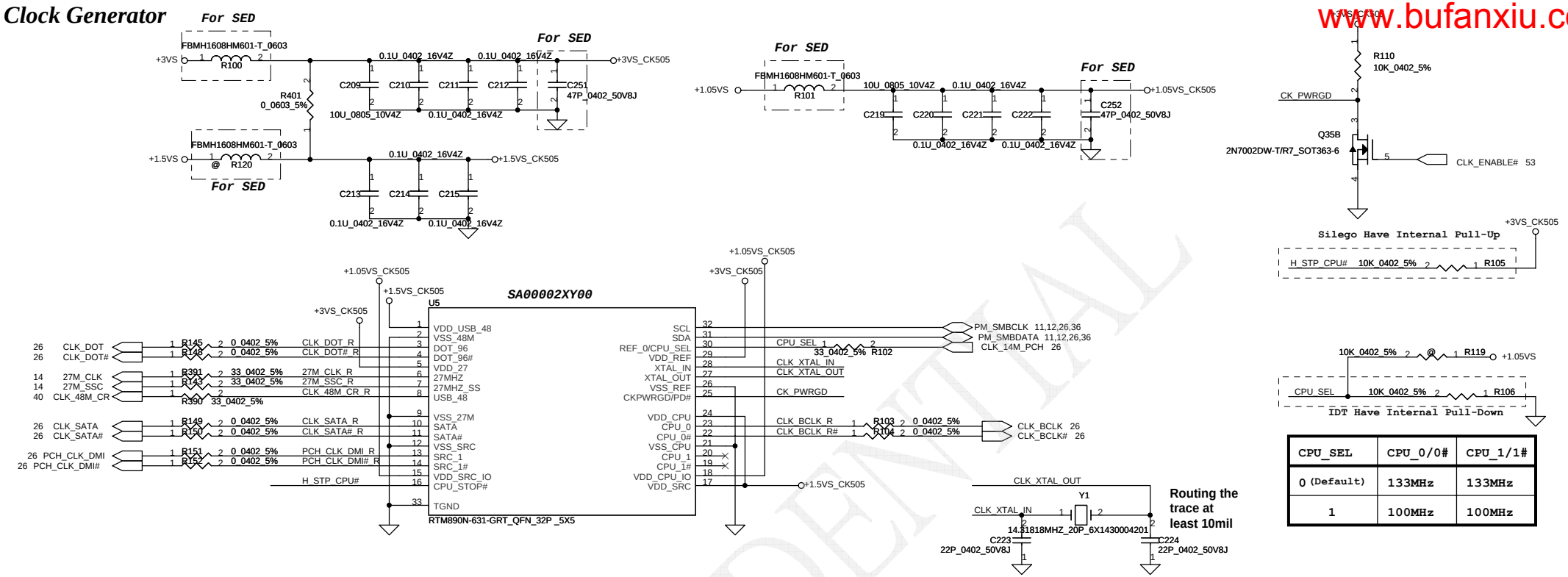
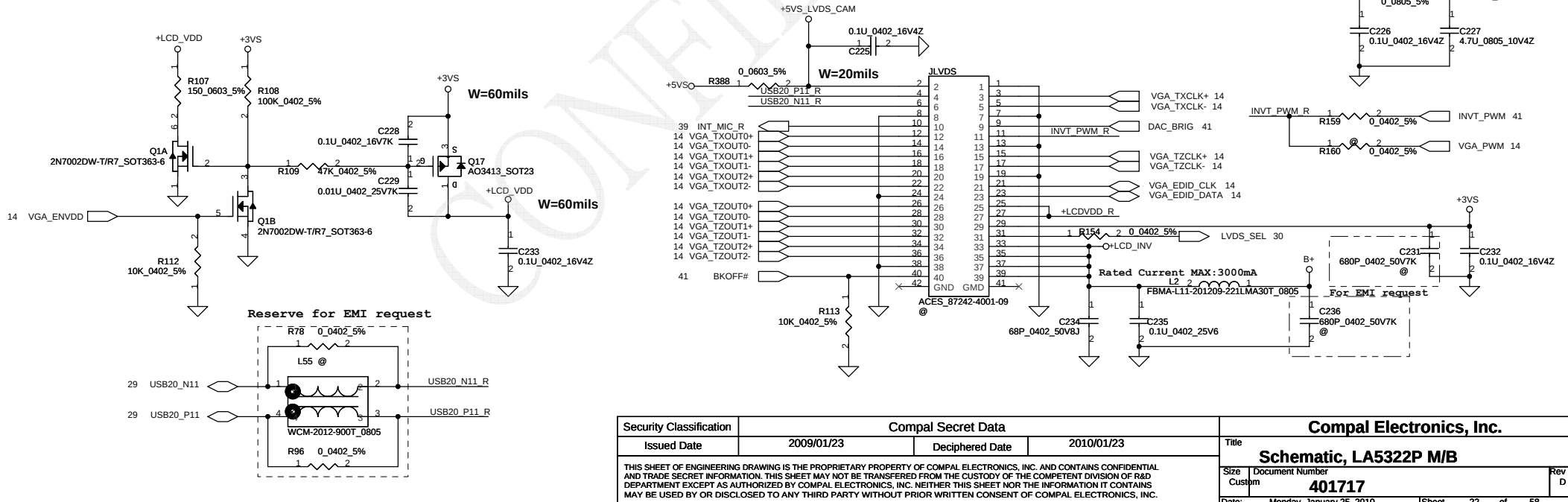
Clock Generator



CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LCD/PANEL BD. Conn.



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CRT CONNECTOR

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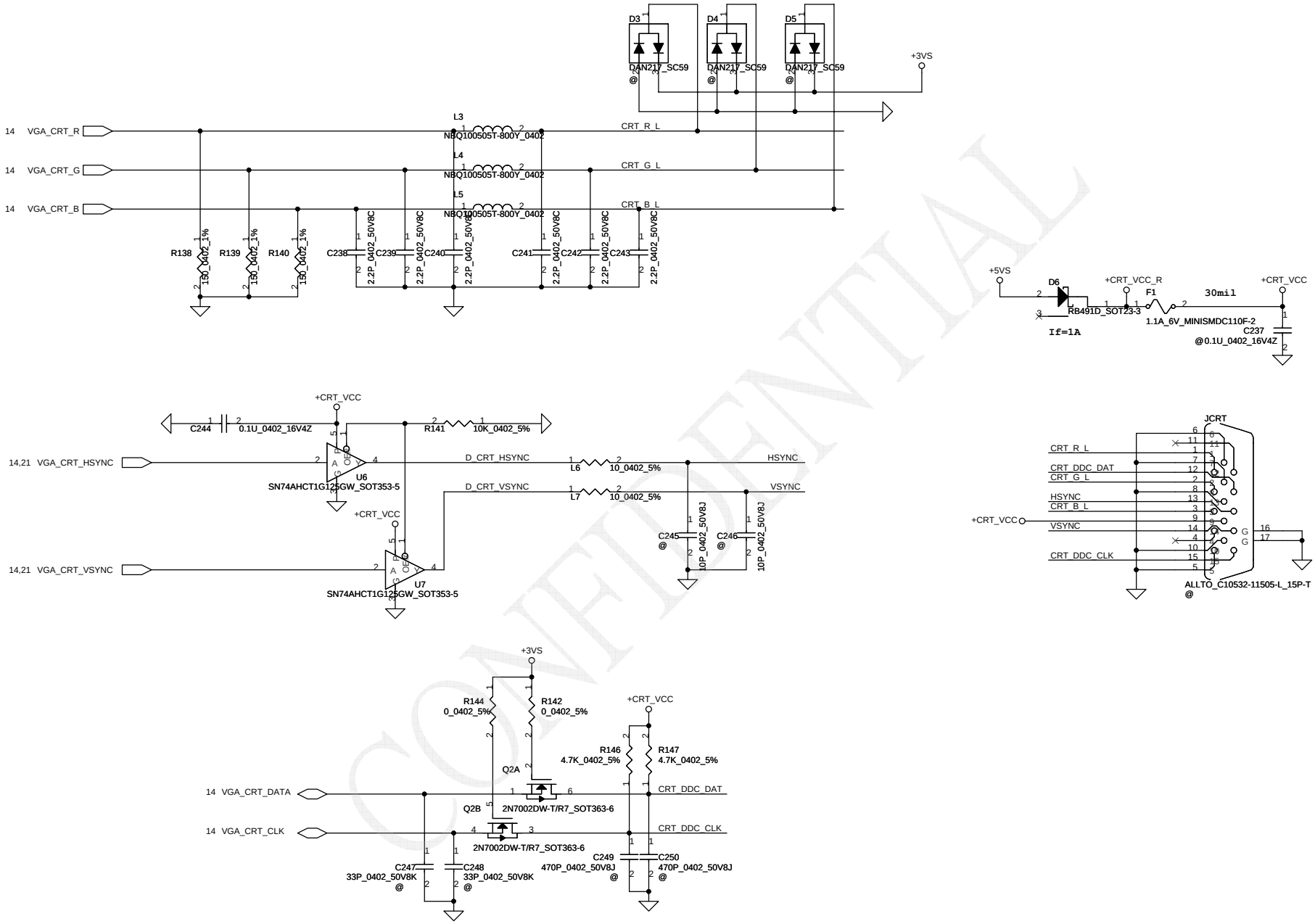

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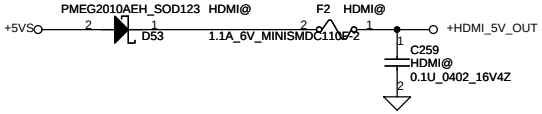
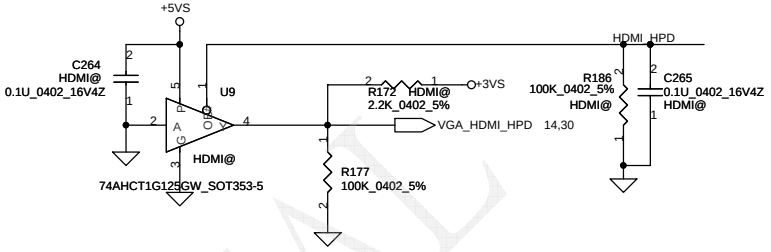
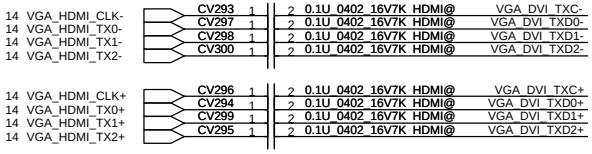
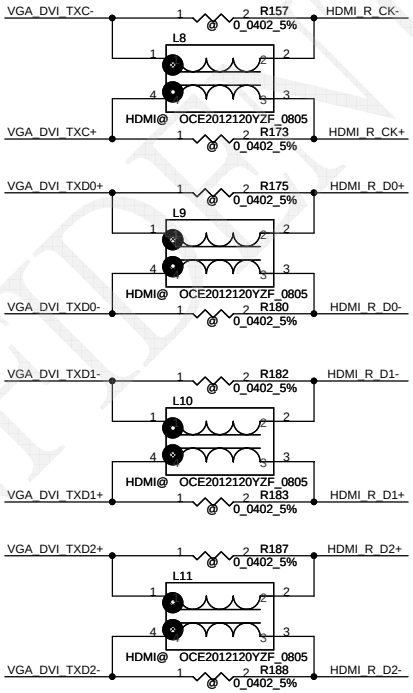
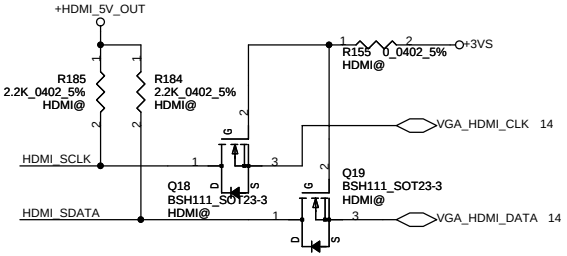
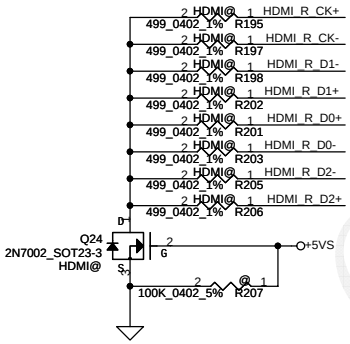




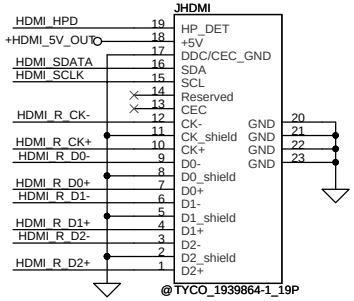








HDMI Connector



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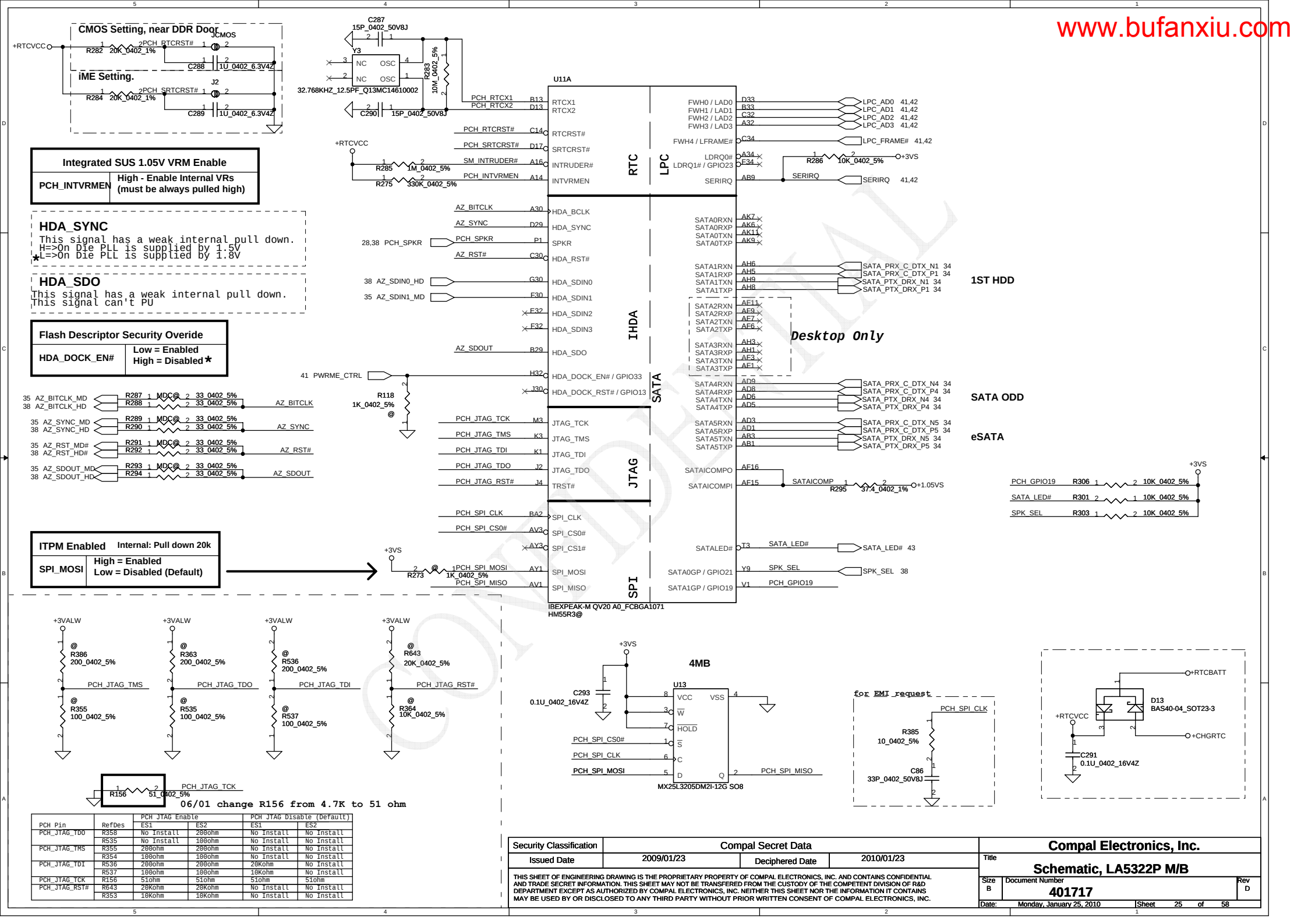

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
	R353	10Kohm	10Kohm	No Install	No Install

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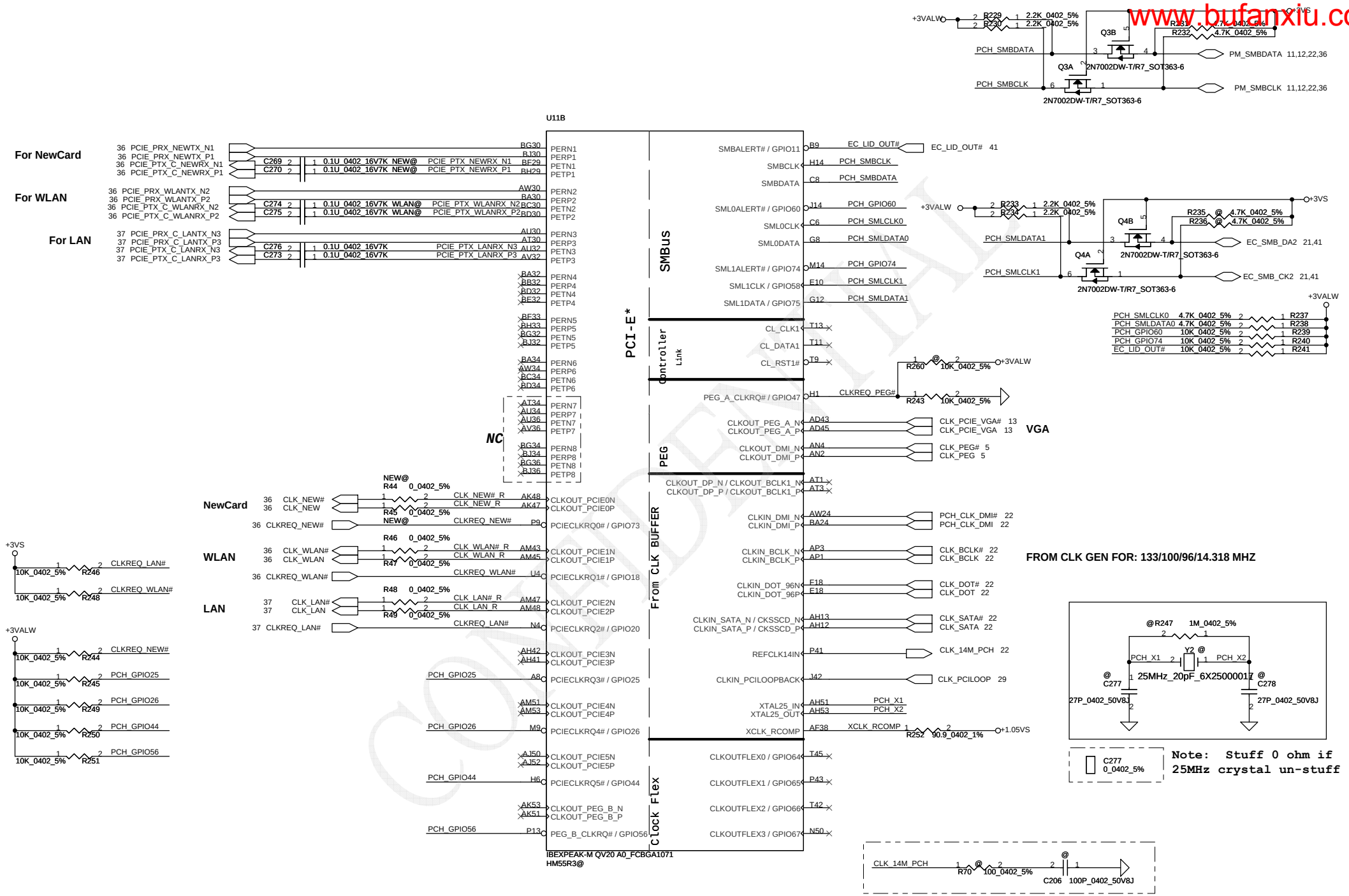

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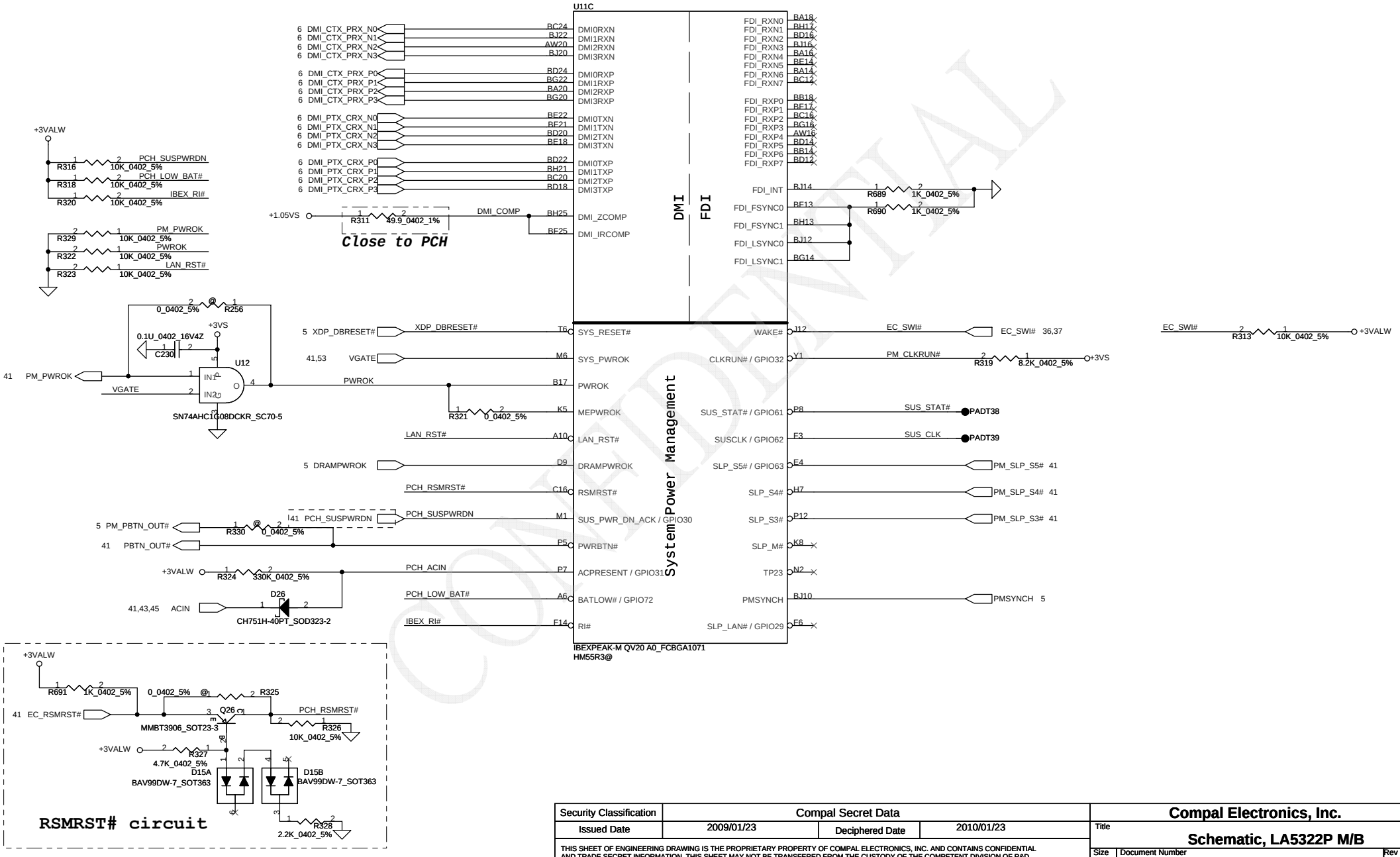

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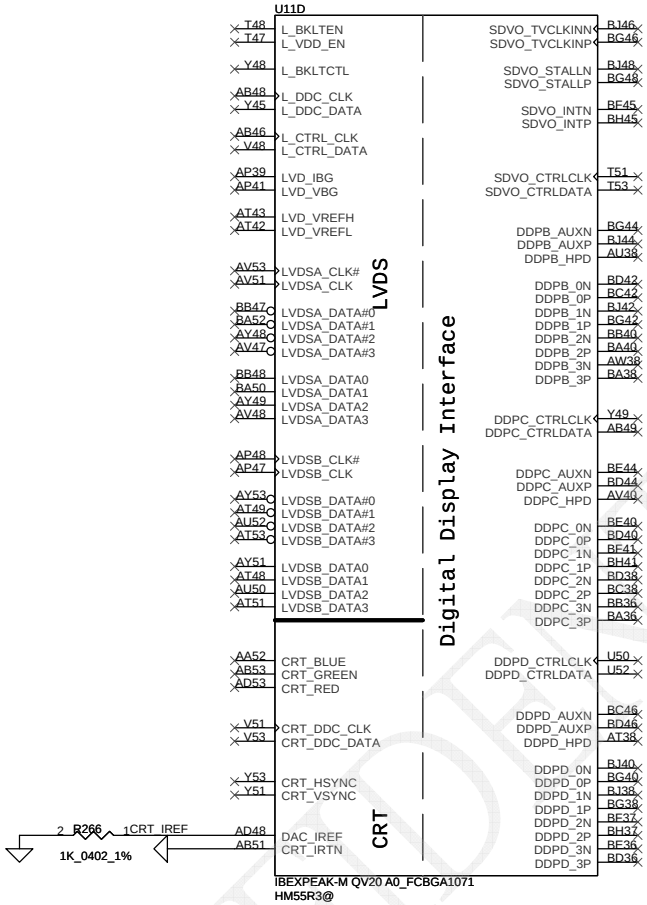
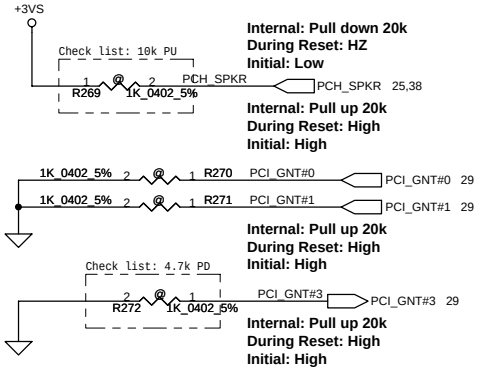


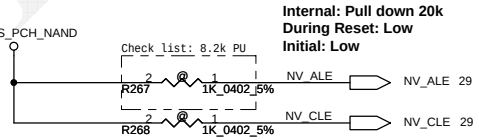
PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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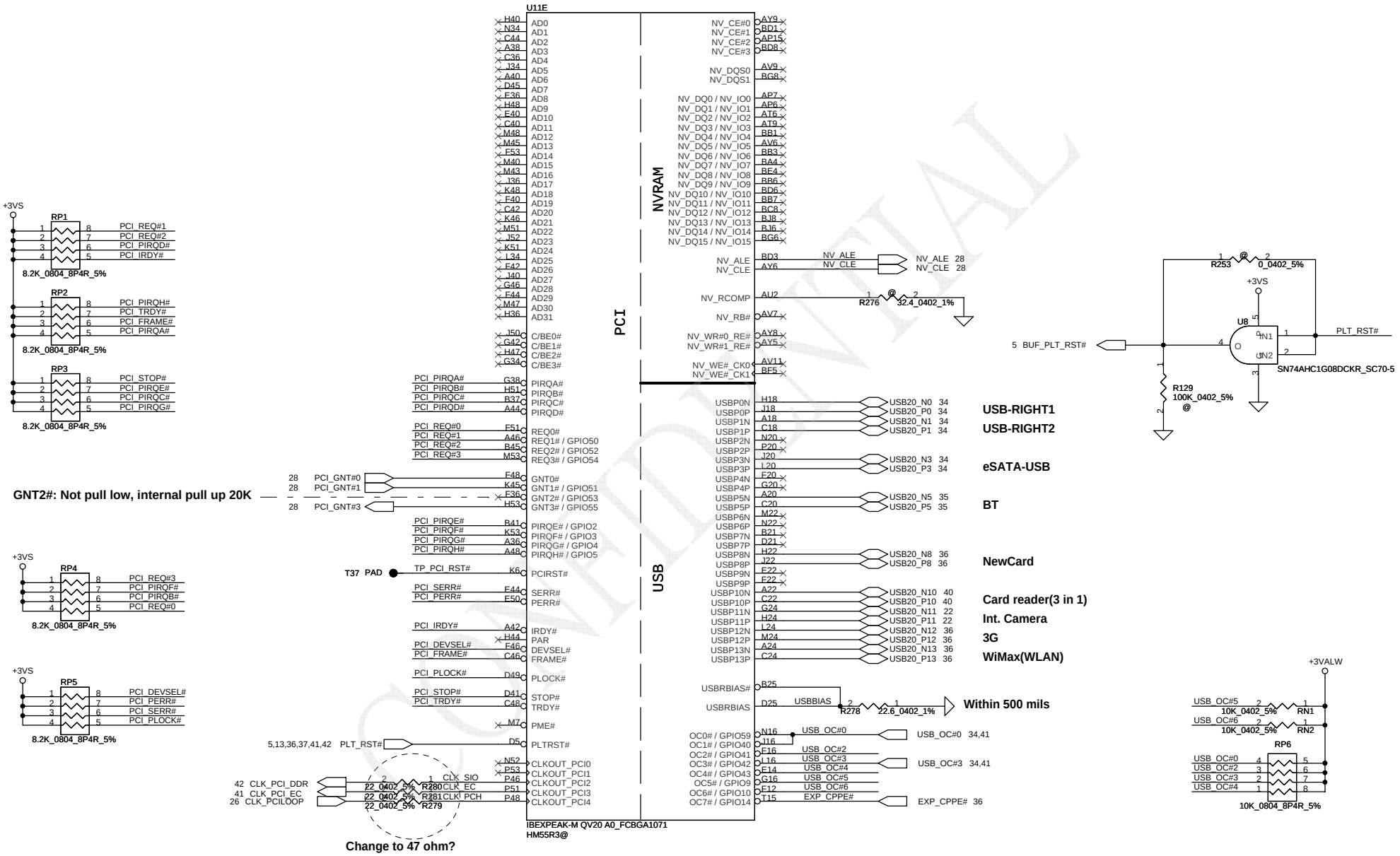

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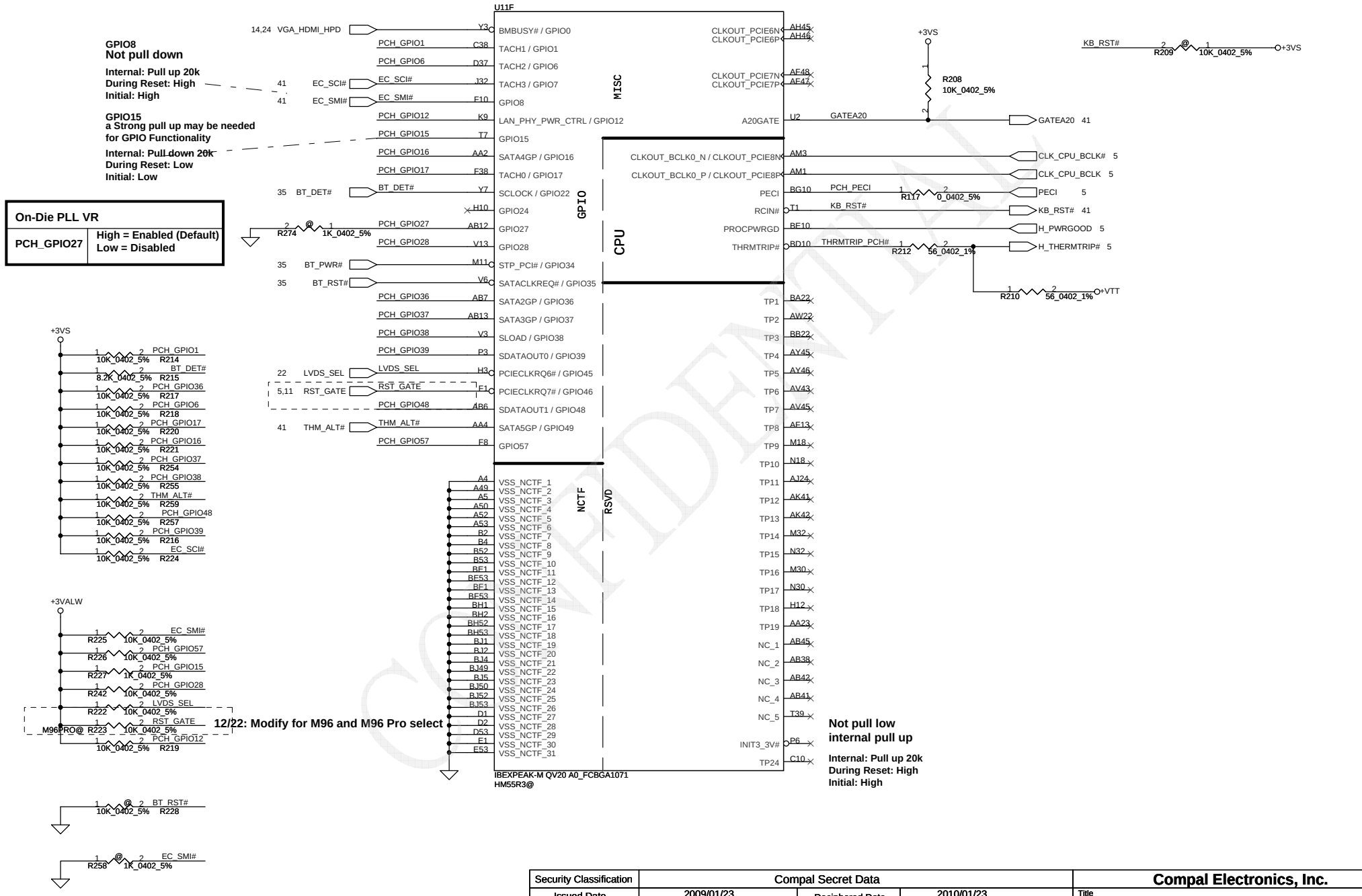

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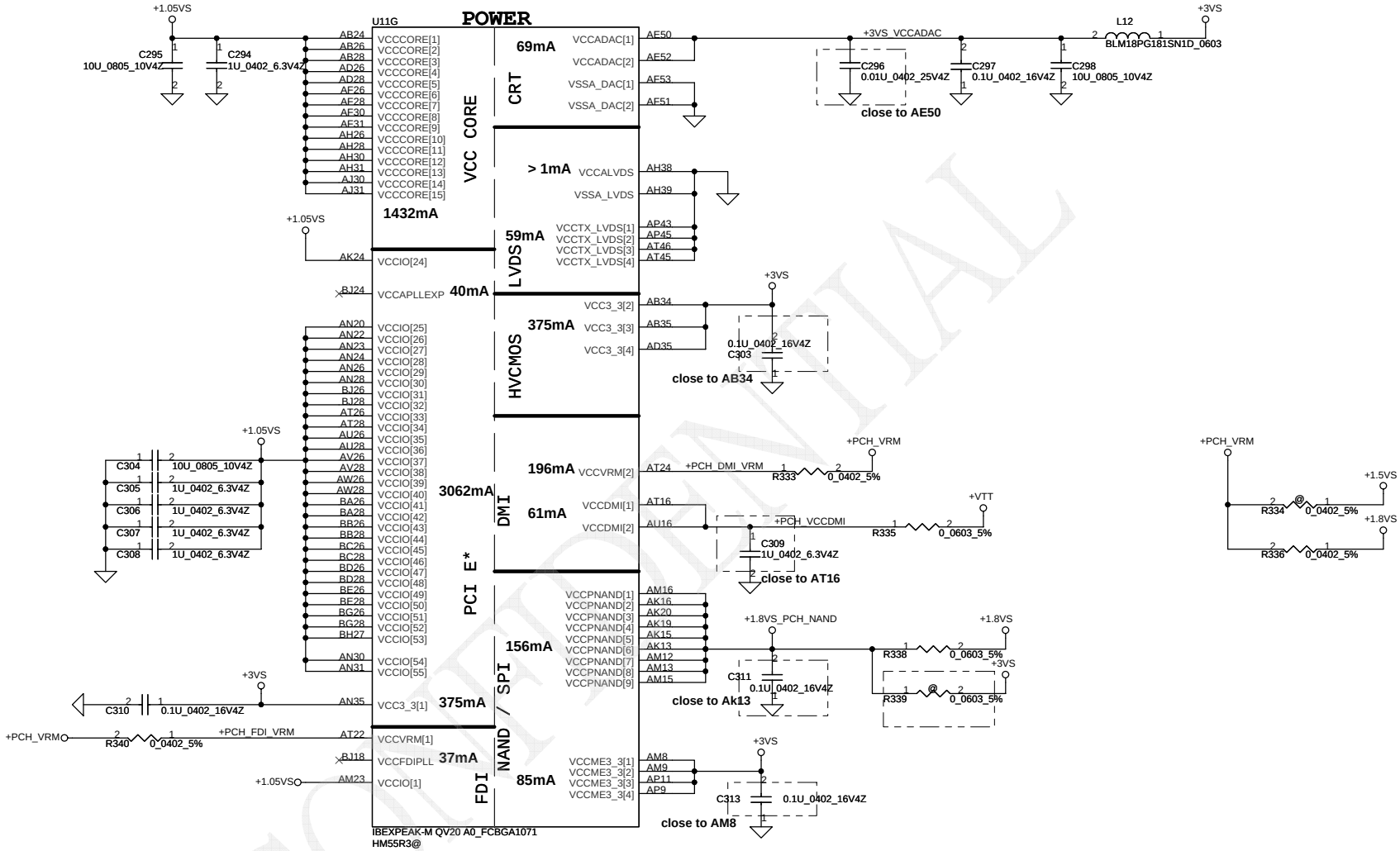

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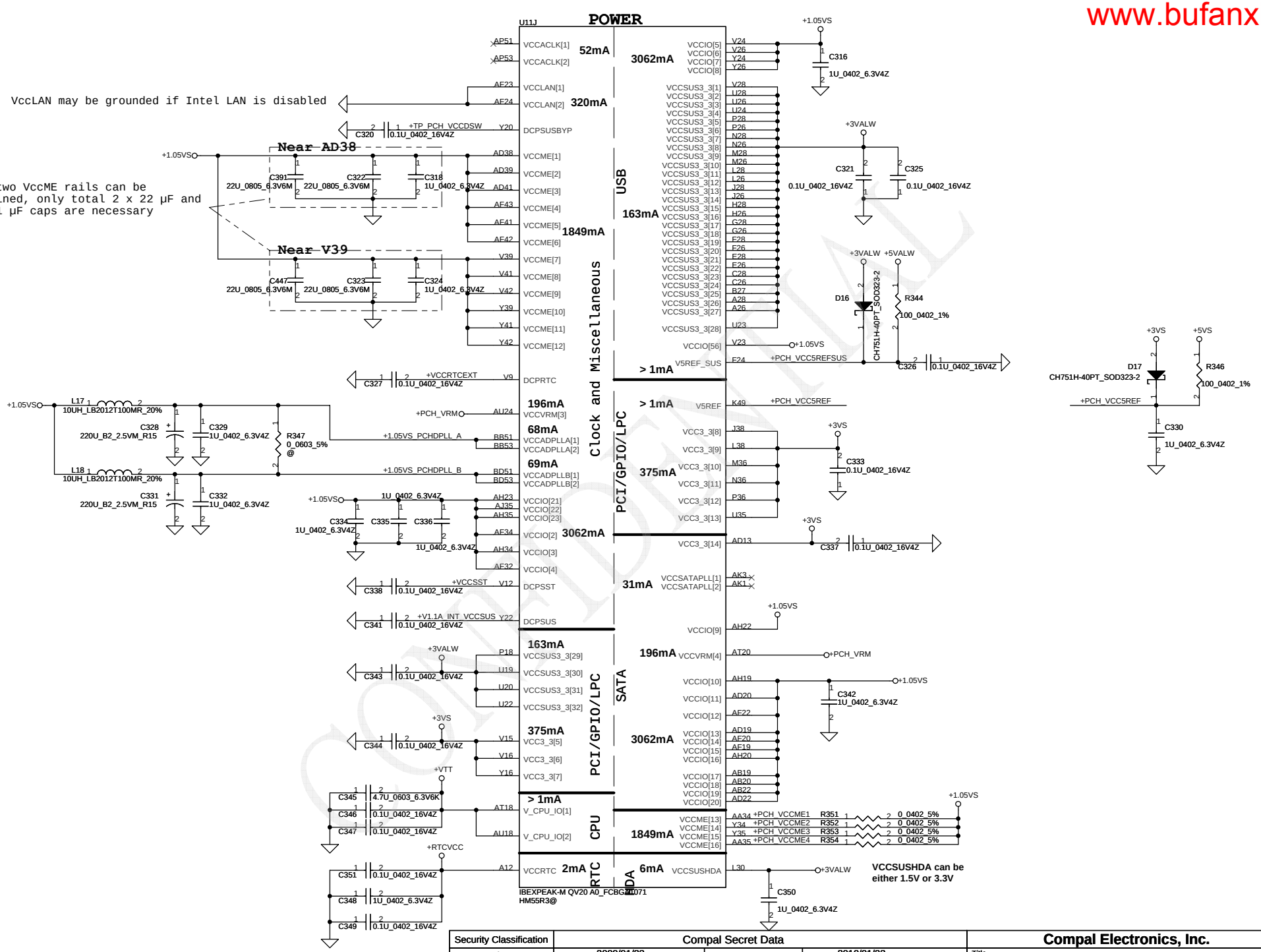

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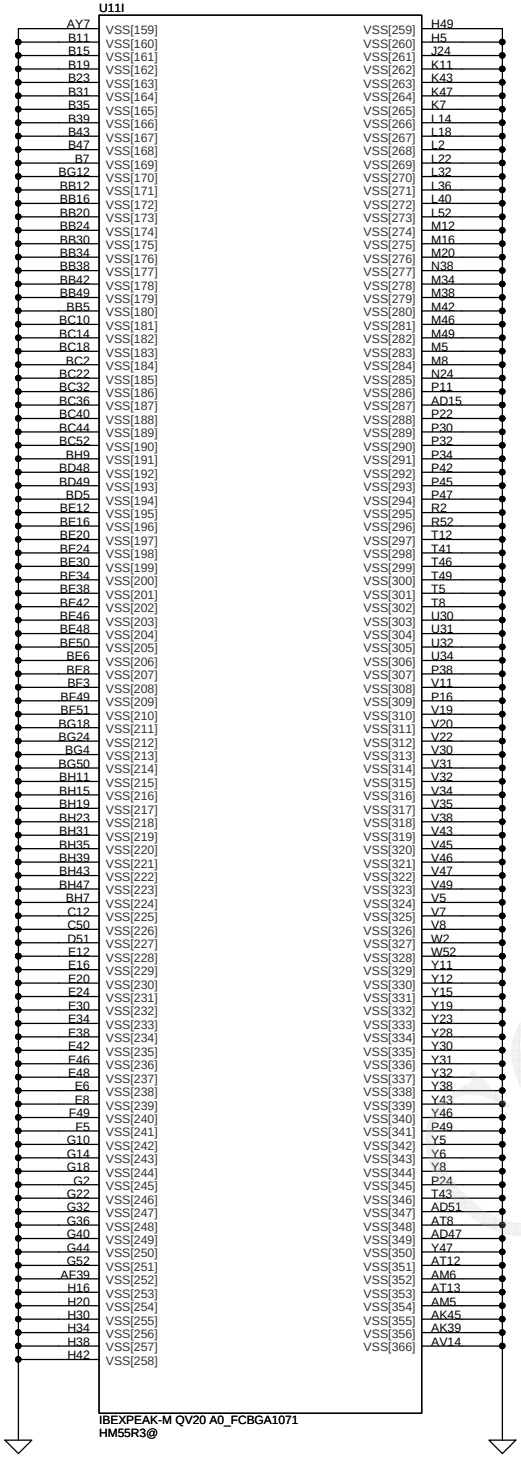

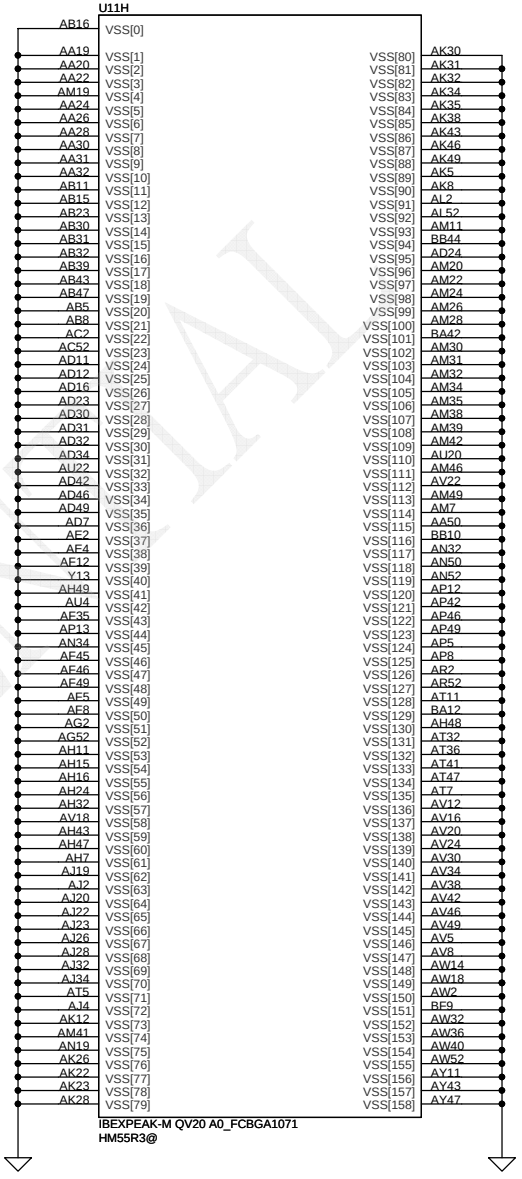

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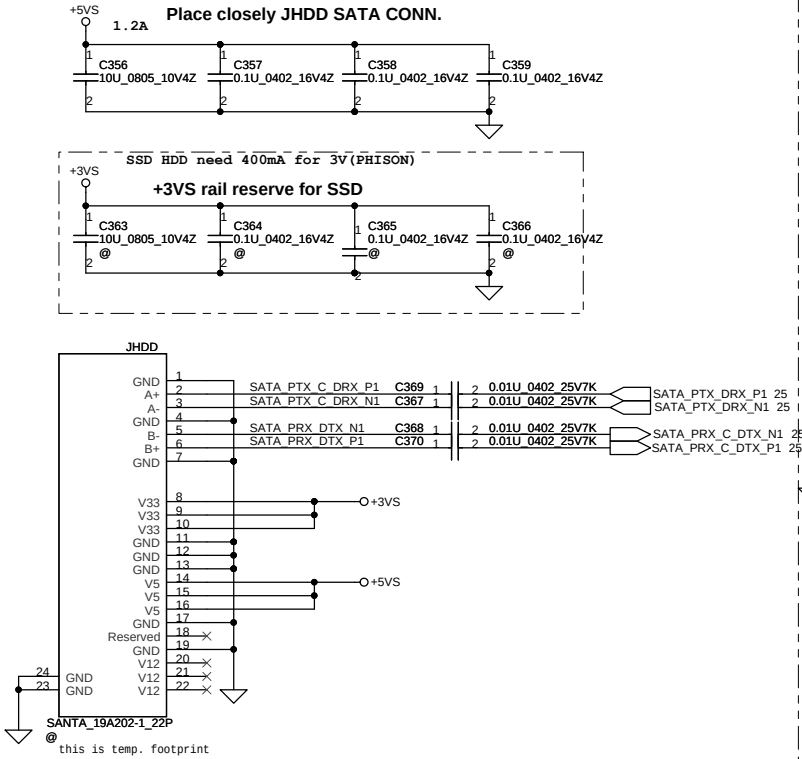
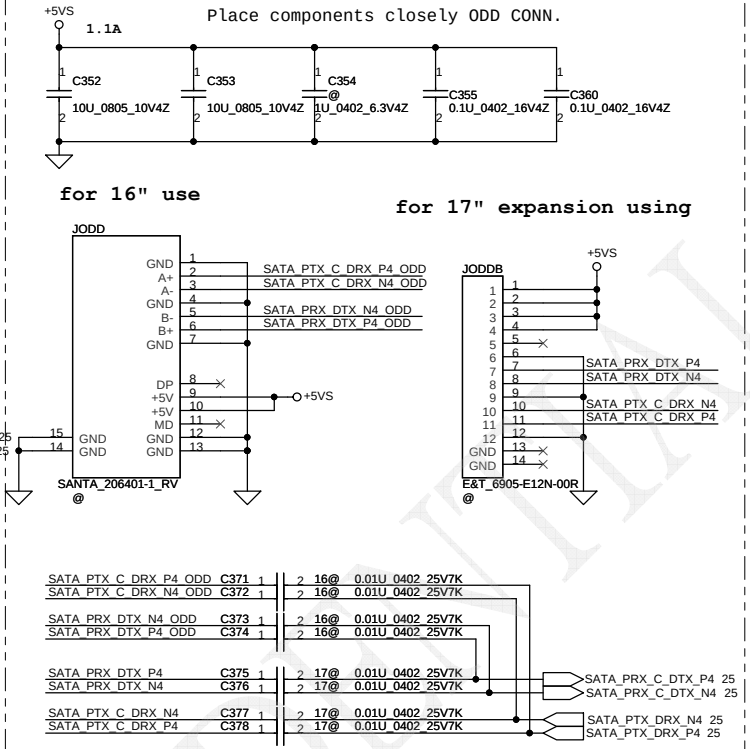
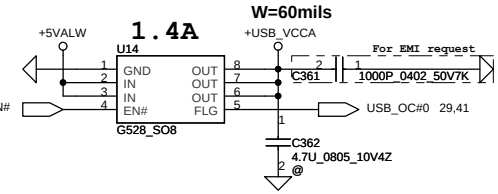
SATA HDD Conn.

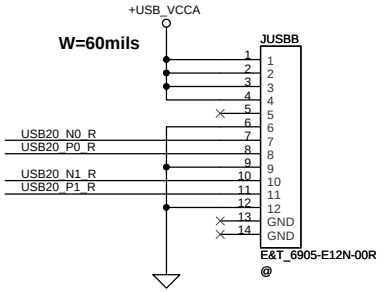


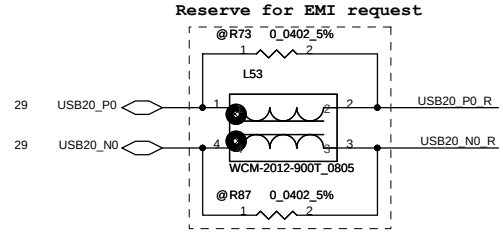
SATA ODD Conn

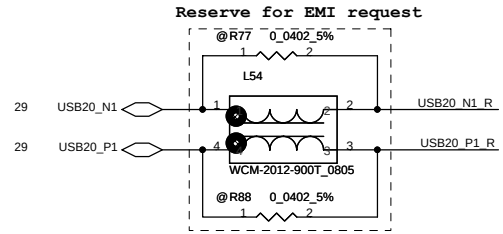


USB Board

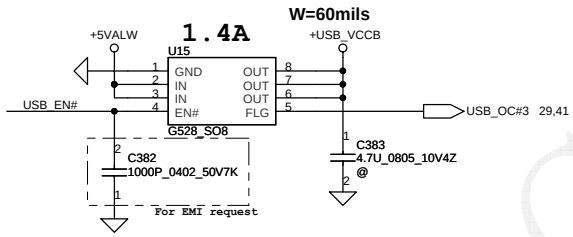


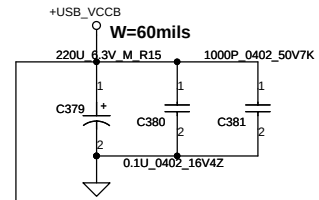


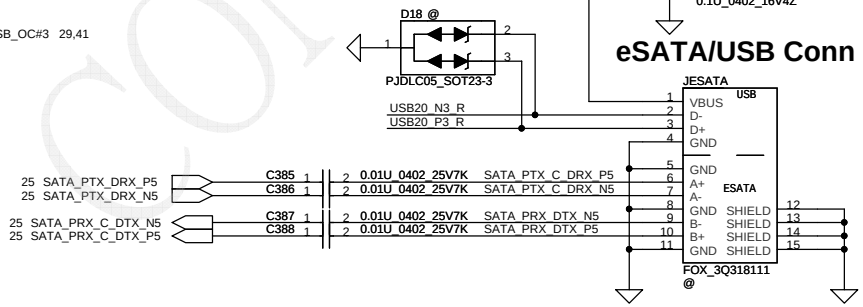


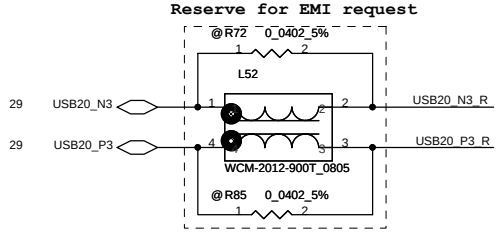


eSATA/USB









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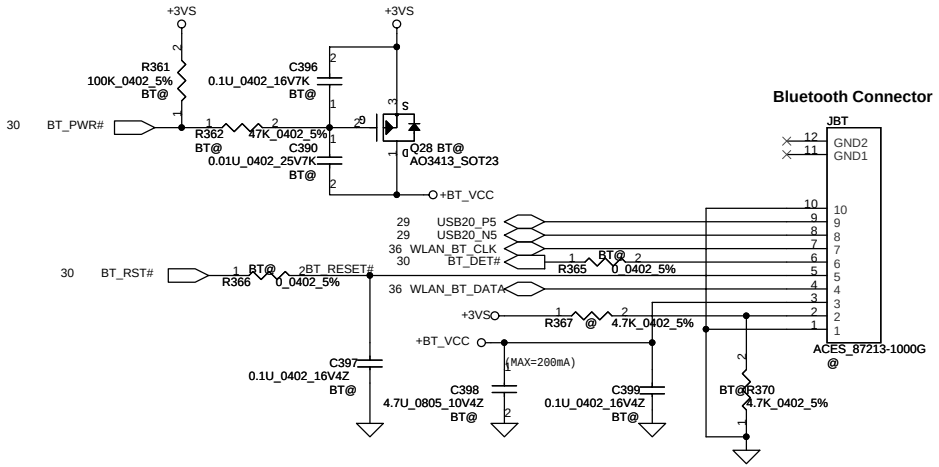
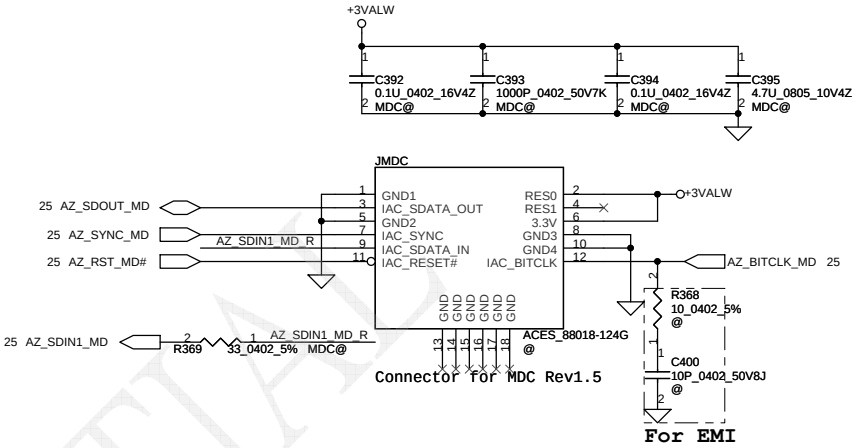
BlueTooth Interface

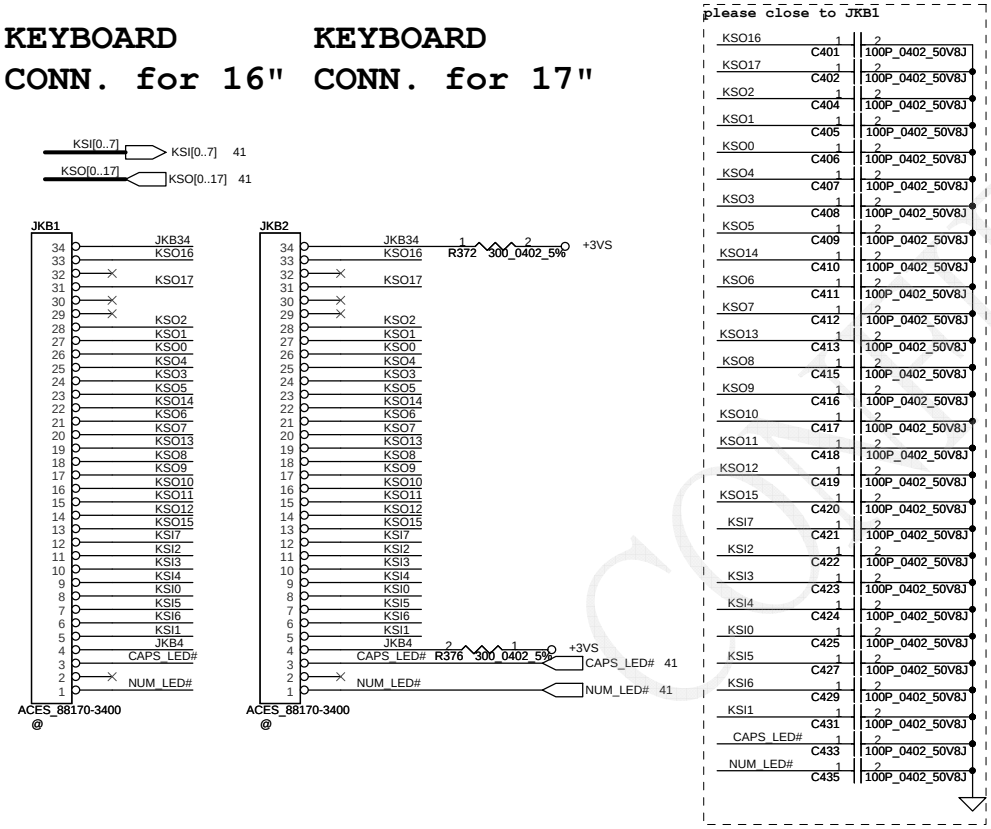


MDC 1.5 Conn.

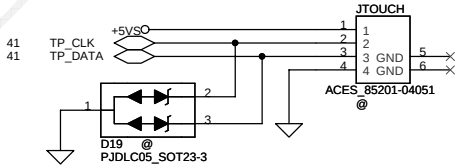


KEYBOARD CONN. for 16"

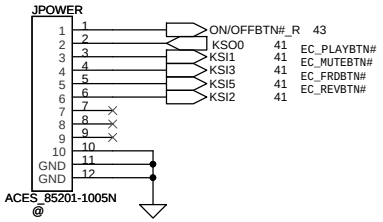
KEYBOARD CONN. for 17"

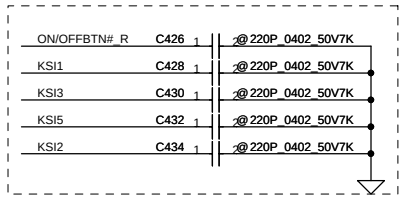


Touch/B Connector



SW/B Connector





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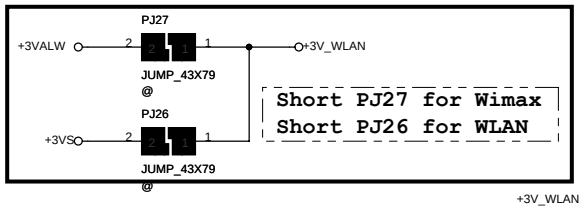
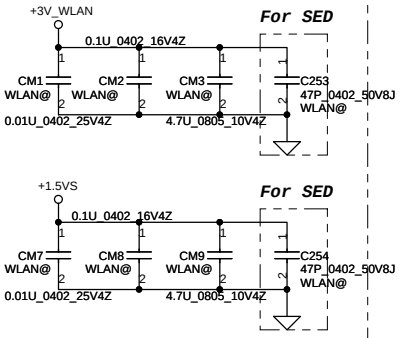
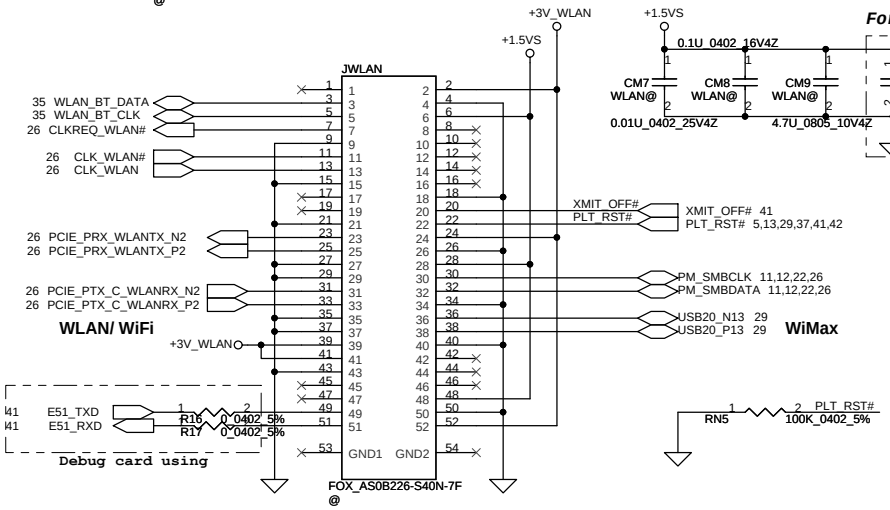
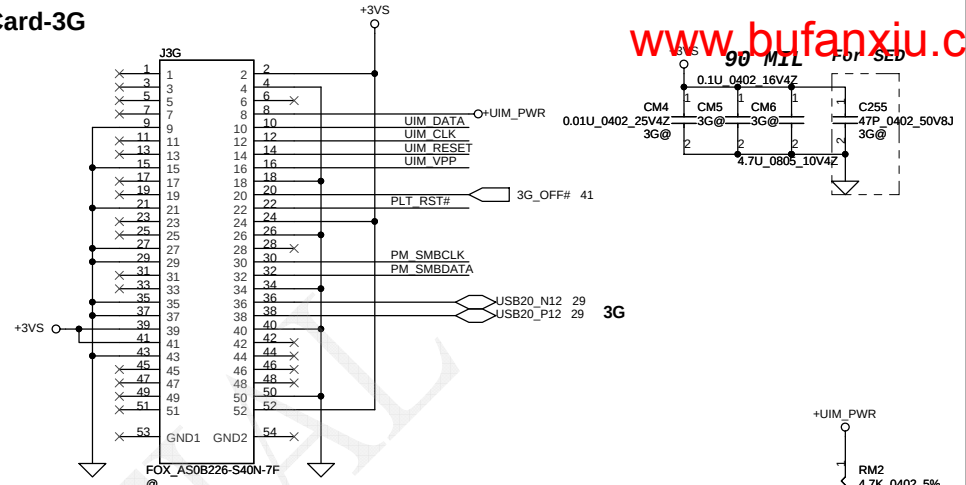
PCIe Mini Card-WLAN/WiMax

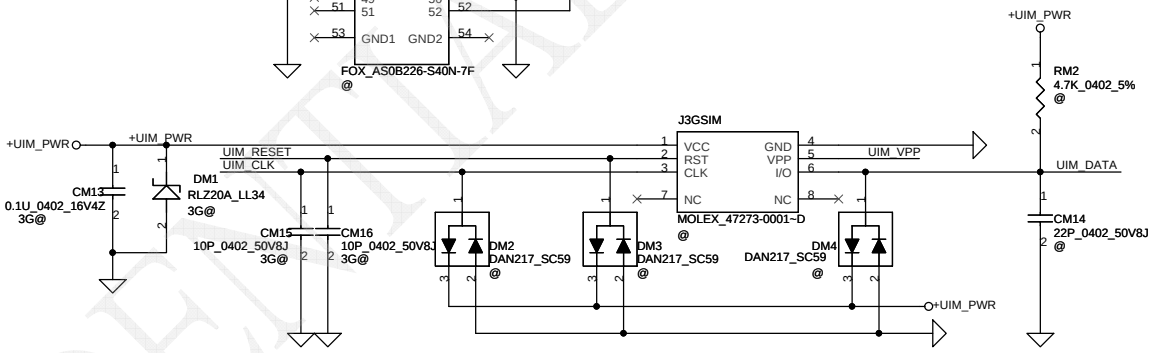


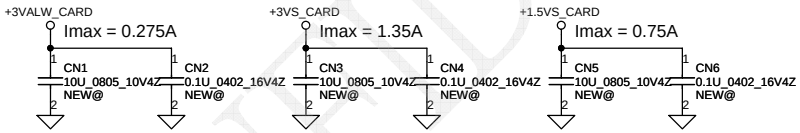


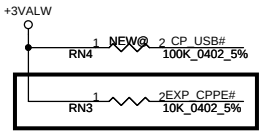


PCIe Mini Card-3G

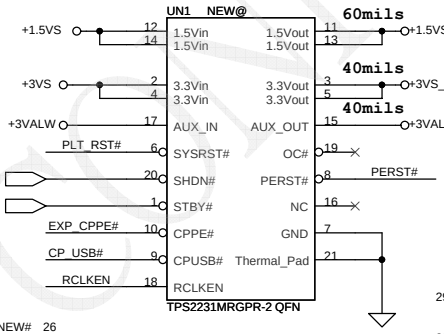


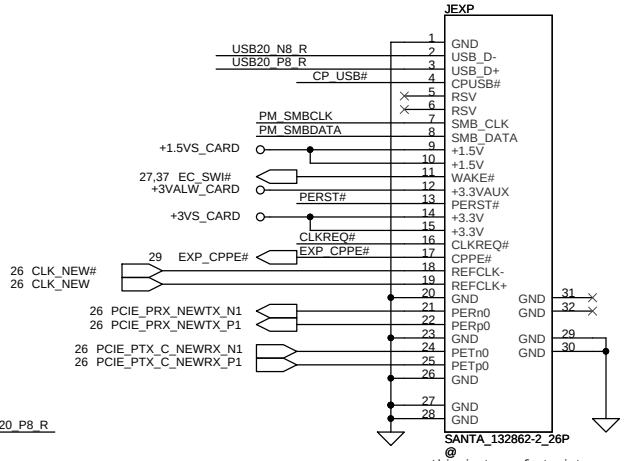


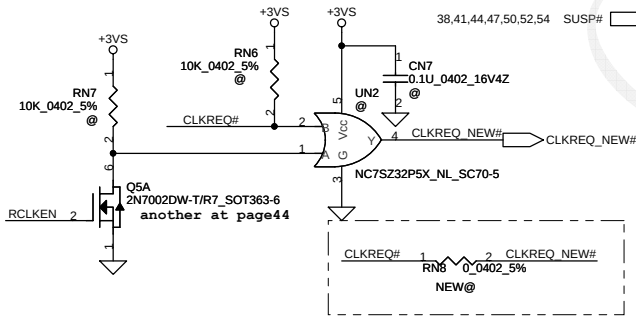


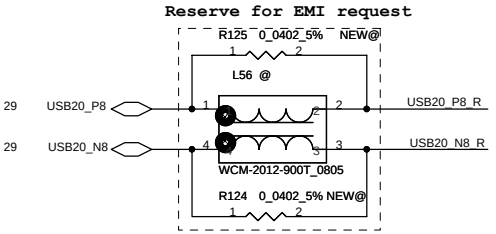


share with USB OC PIN
need always pull high









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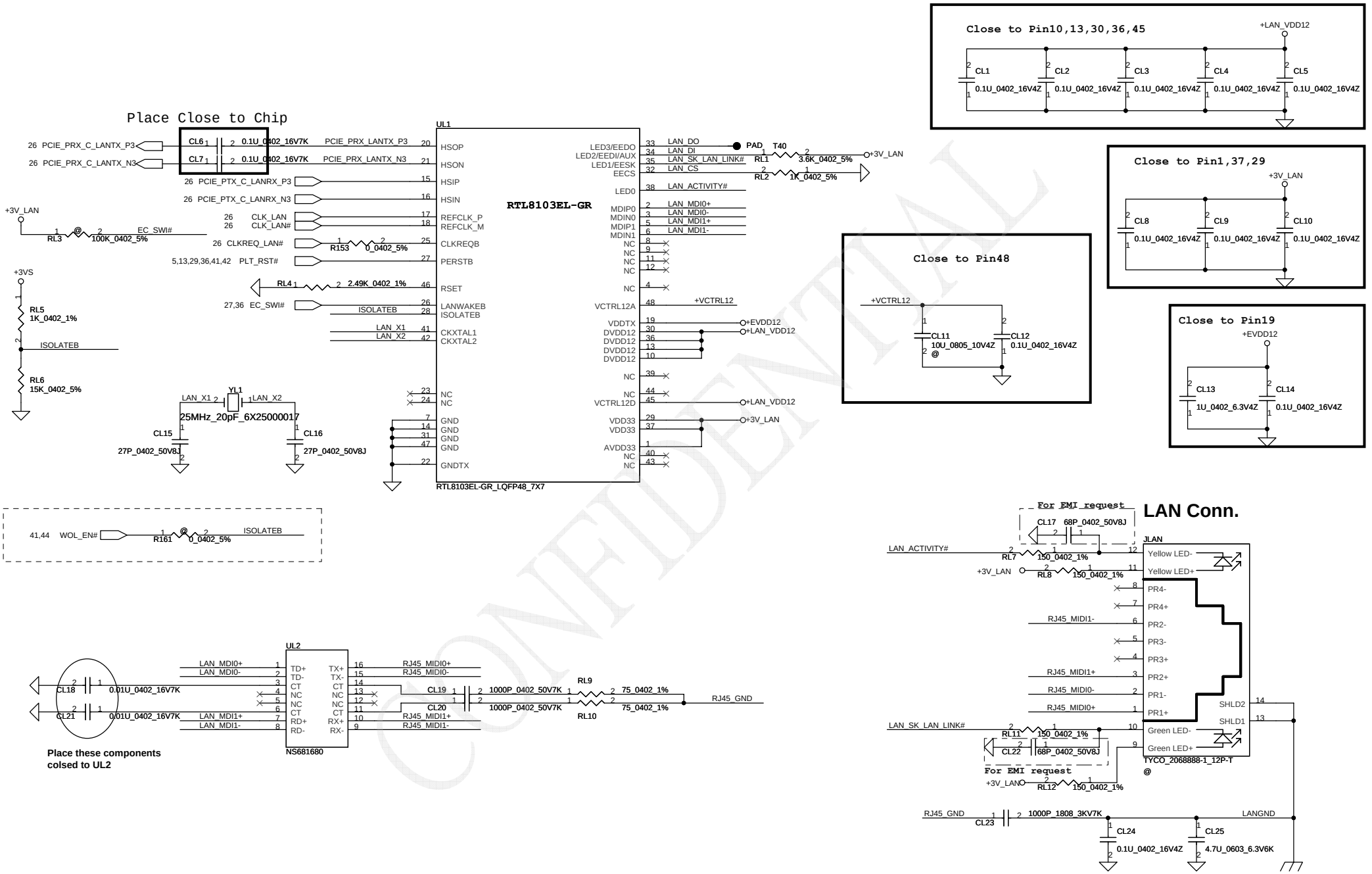

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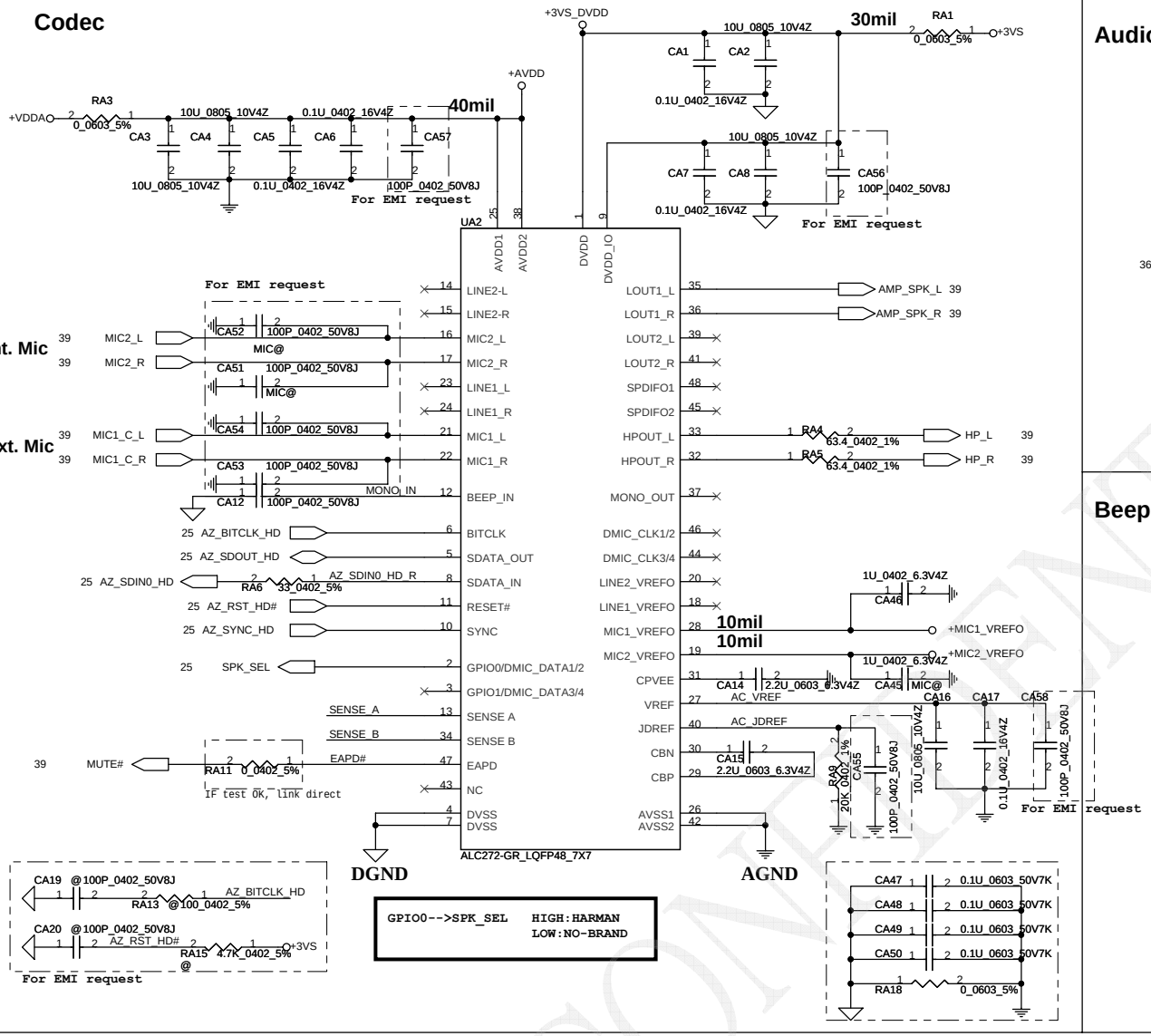
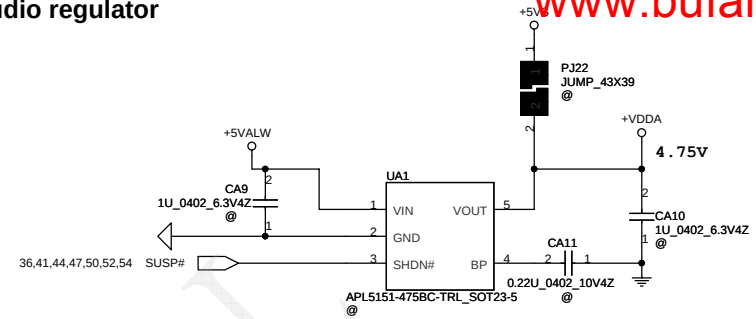
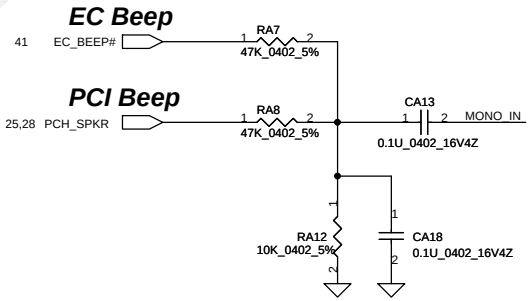
Codec



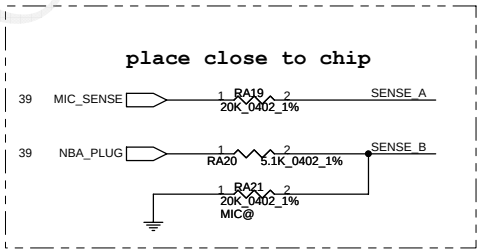
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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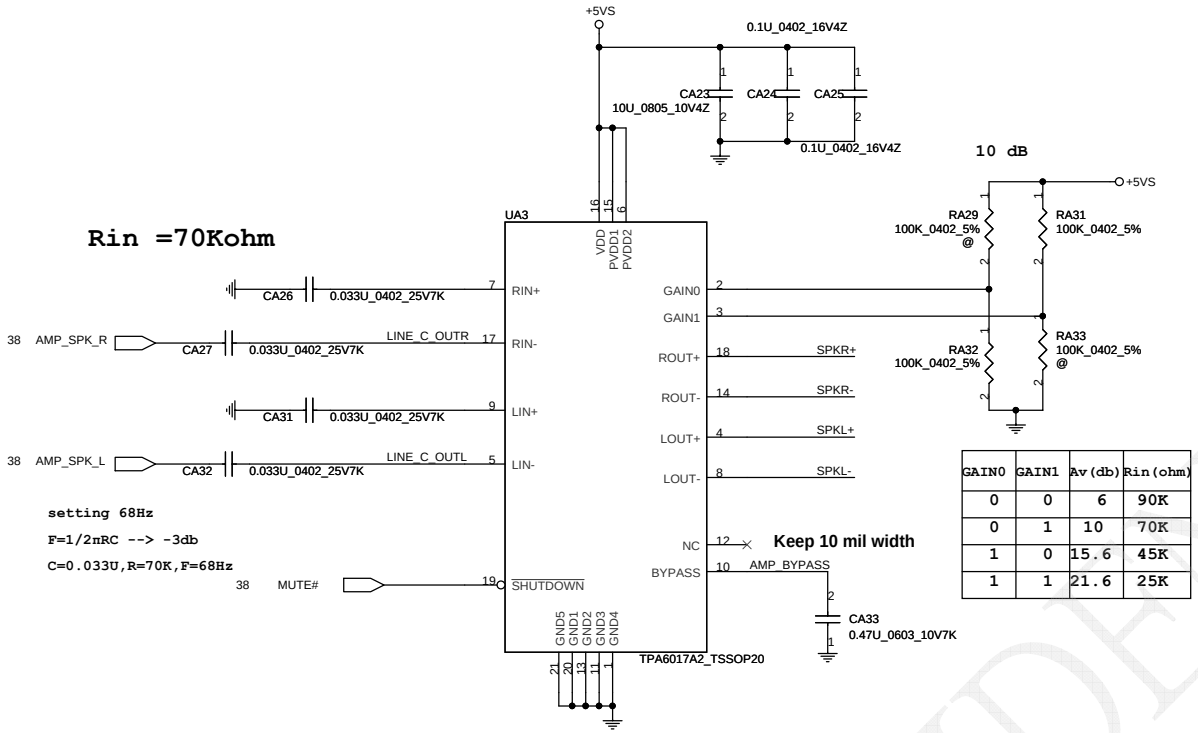
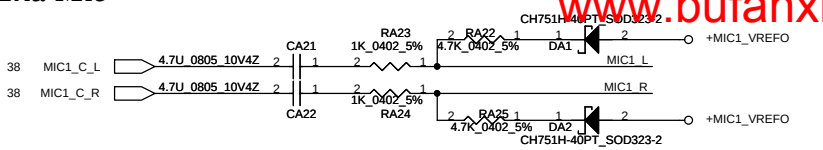
TPA6017 Medium Range Amplifier

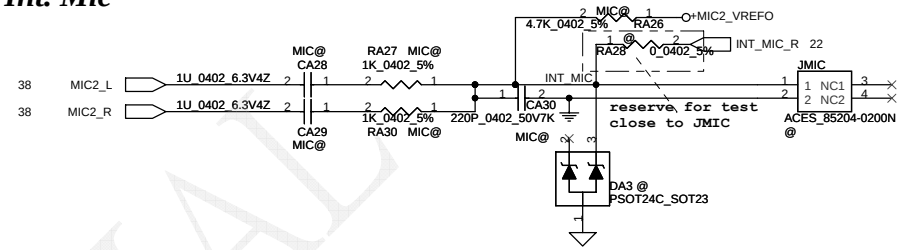


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

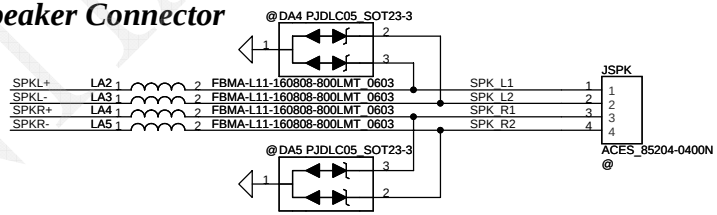
Ext. Mic



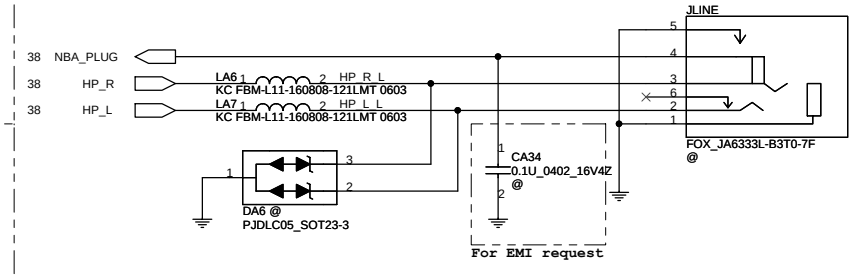
Int. Mic



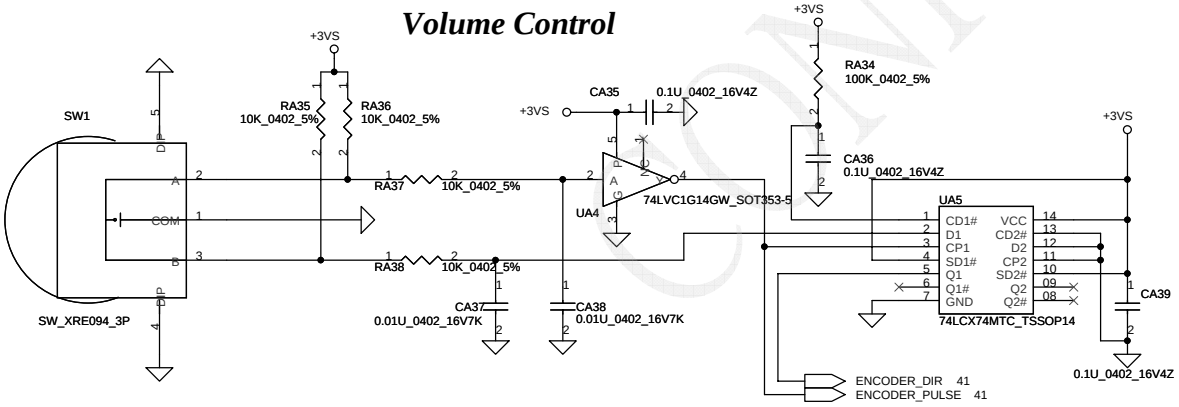
Speaker Connector



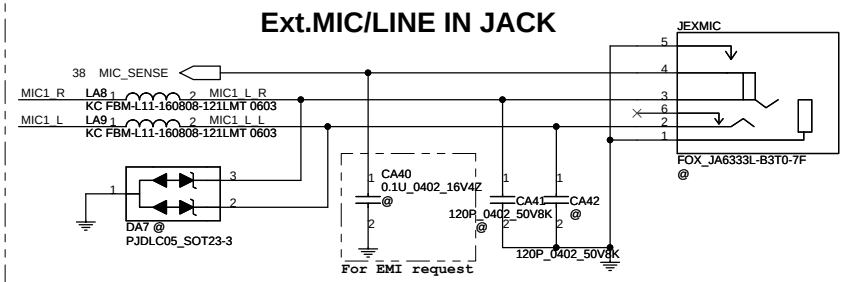
HeadPhone/LINE Out JACK



Volume Control



Ext.MIC/LINE IN JACK



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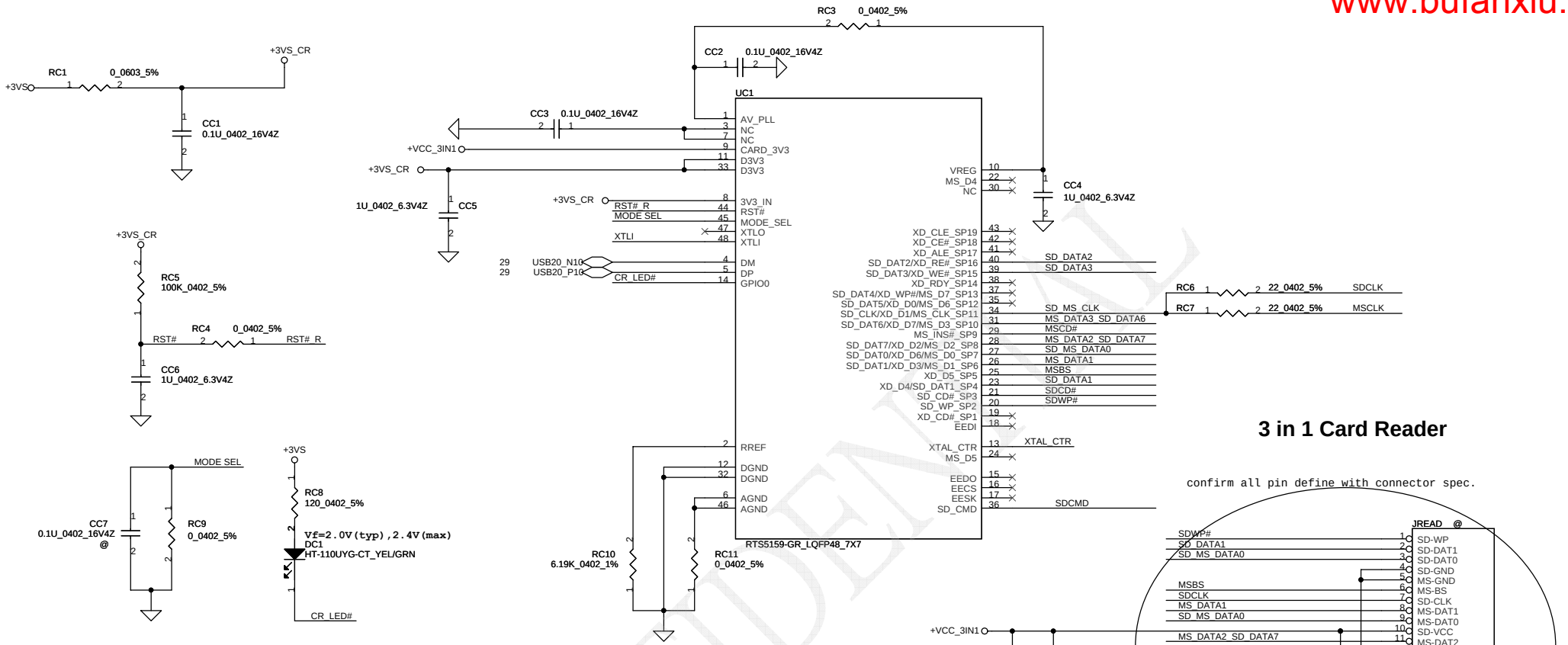
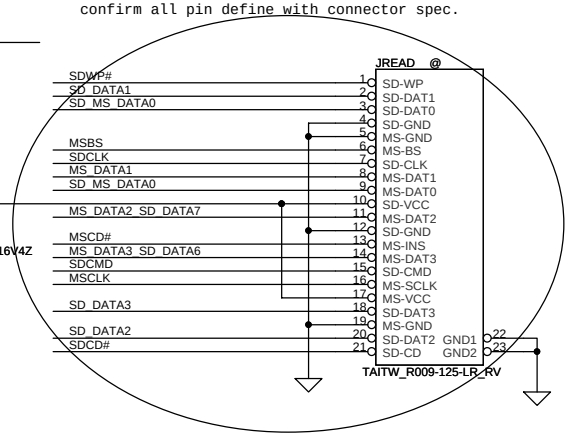
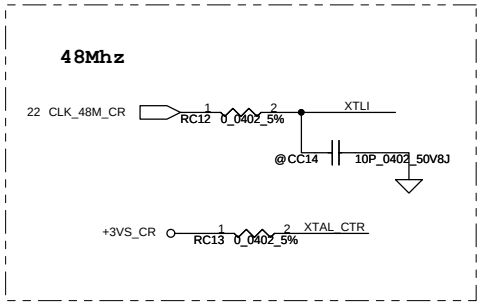


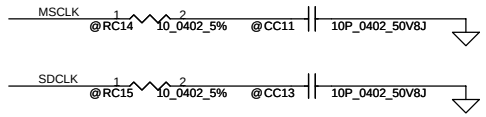
3 in 1 Card Reader

confirm all pin define with connector spec.





R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	



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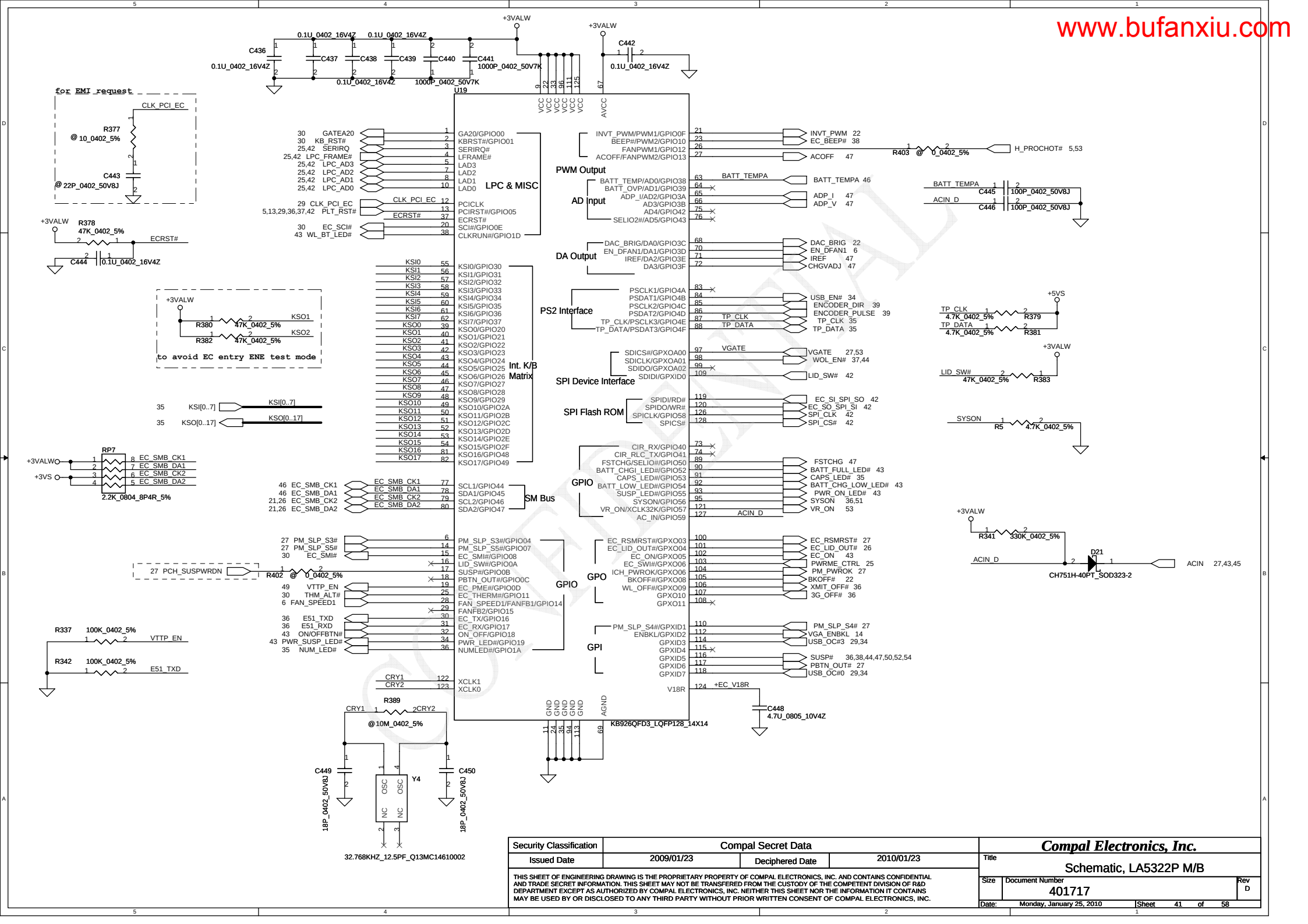

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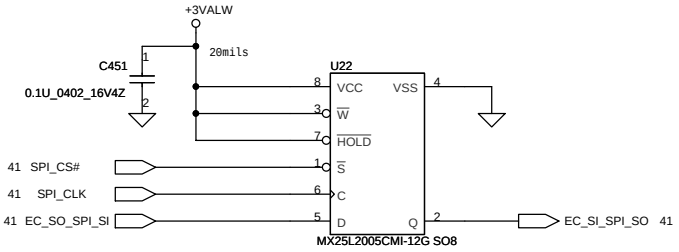
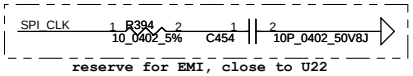
SPI Flash (256KB)

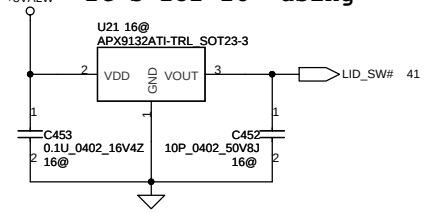
Socket: SP07000F500 & SP07000H900



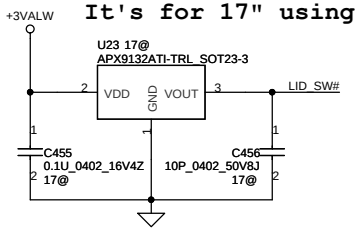


Lid SW

It's for 16" using

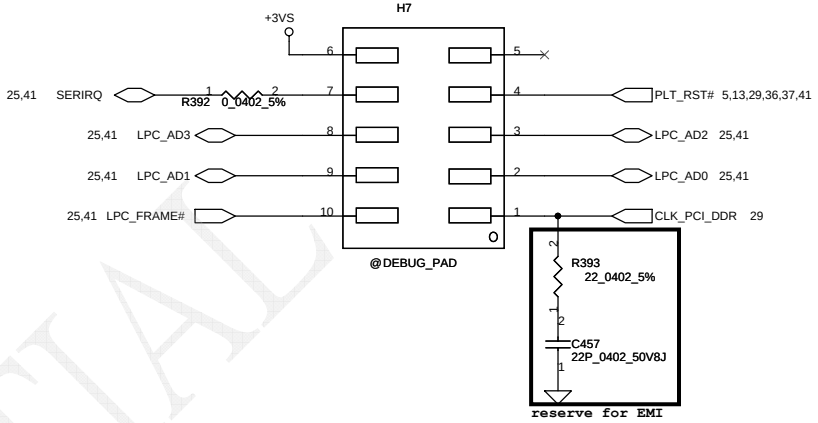


It's for 17" using



LPC Debug Port

Please place the PAD under DDR DIMM.



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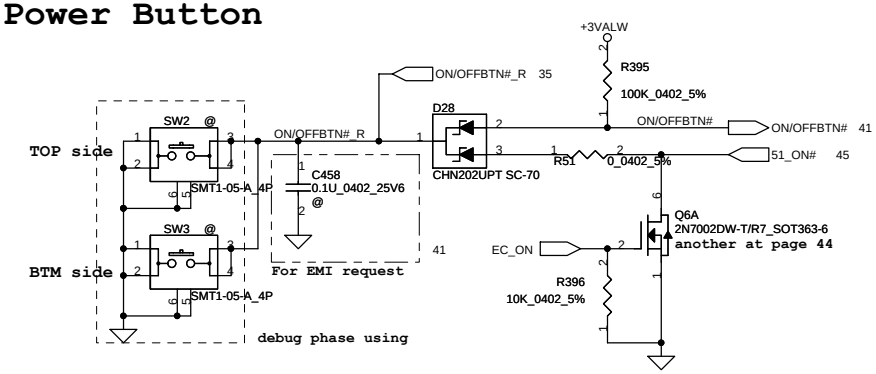
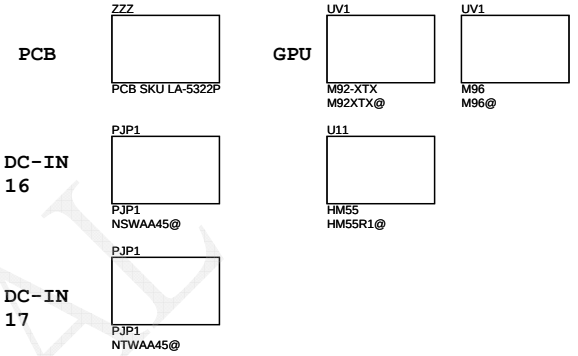
Power Button

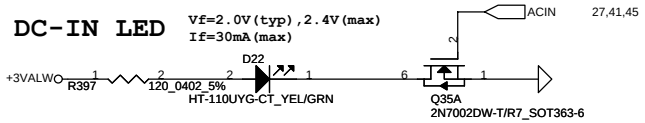


ISPD

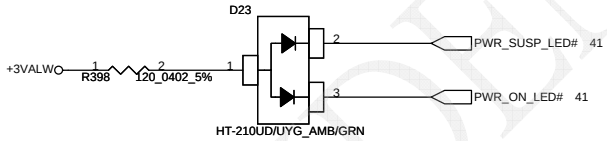


DC-IN LED

Vf=2.0V(typ),2.4V(max)
If=30mA(max)

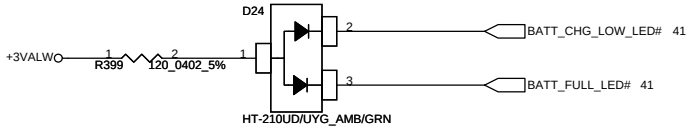


POWER/SUSPEND LED

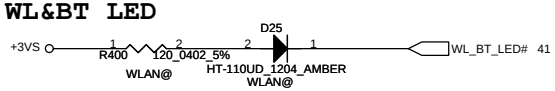


BATT CHARGE/FULL LED

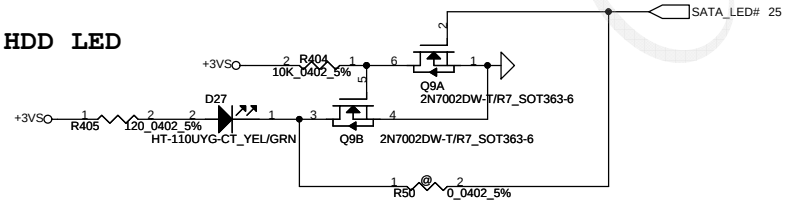
Vf=1.9V(typ),2.4V(max) for amber
Vf=2.0V(typ),2.4V(max) for green
If=30mA(max)



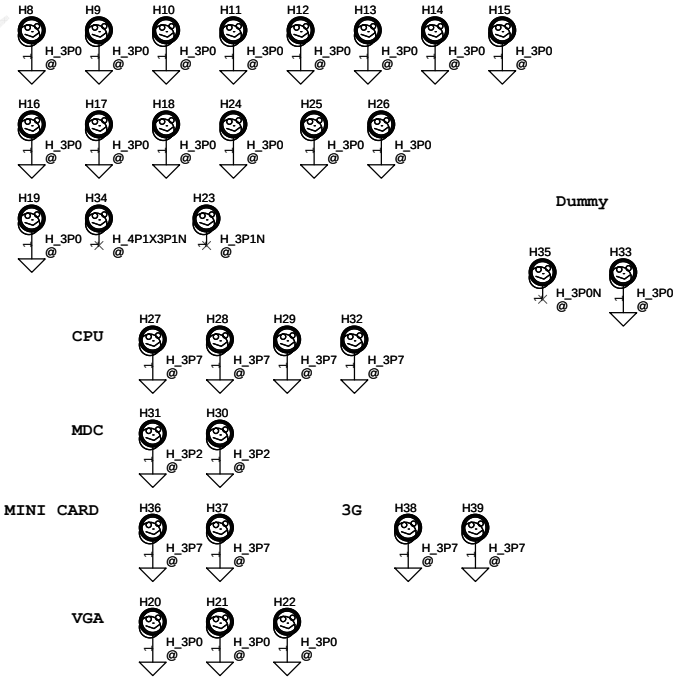
WL&BT LED



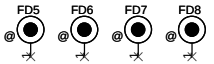
HDD LED



Screw Hole



PCB Fedical Mark PAD



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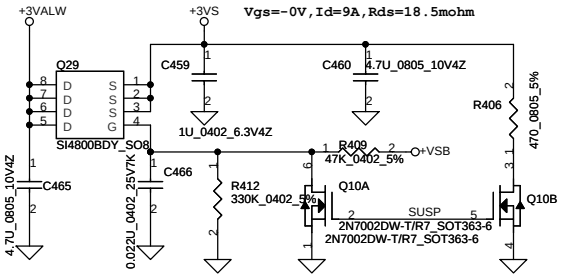
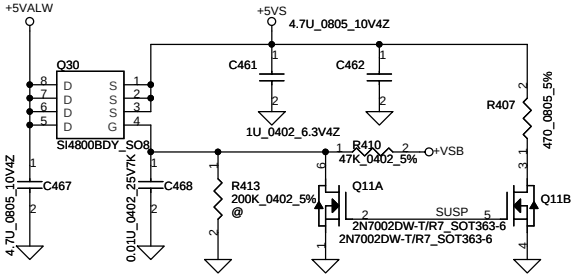
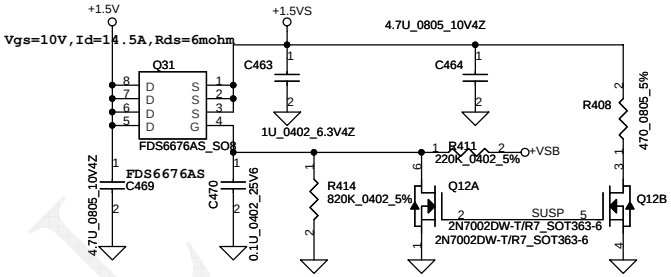
+3VALW TO +3VS



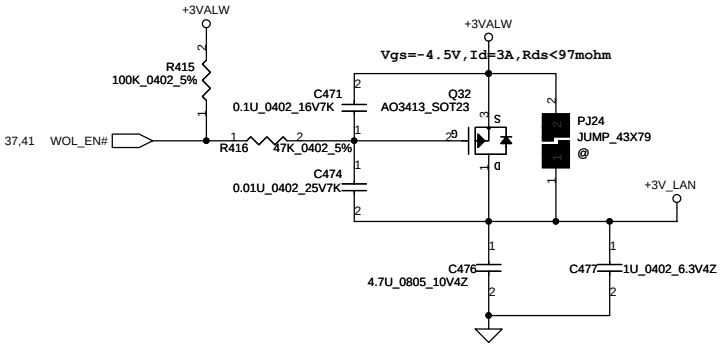
+5VALW TO +5VS

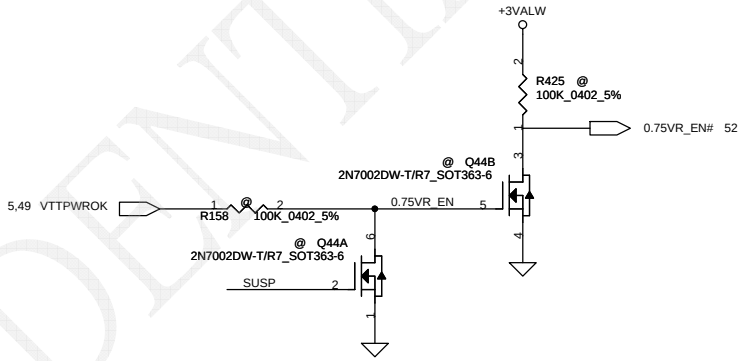


+1.5V to +1.5VS

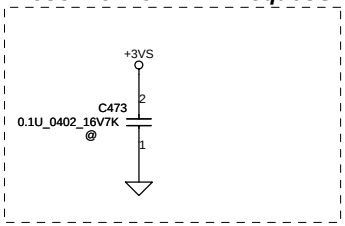


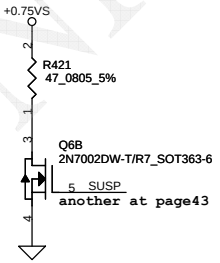
+3VALW TO +3V_LAN

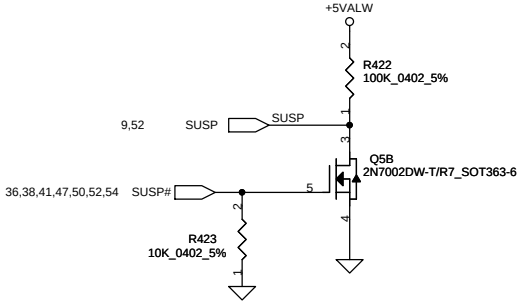




Reserve for EMI request







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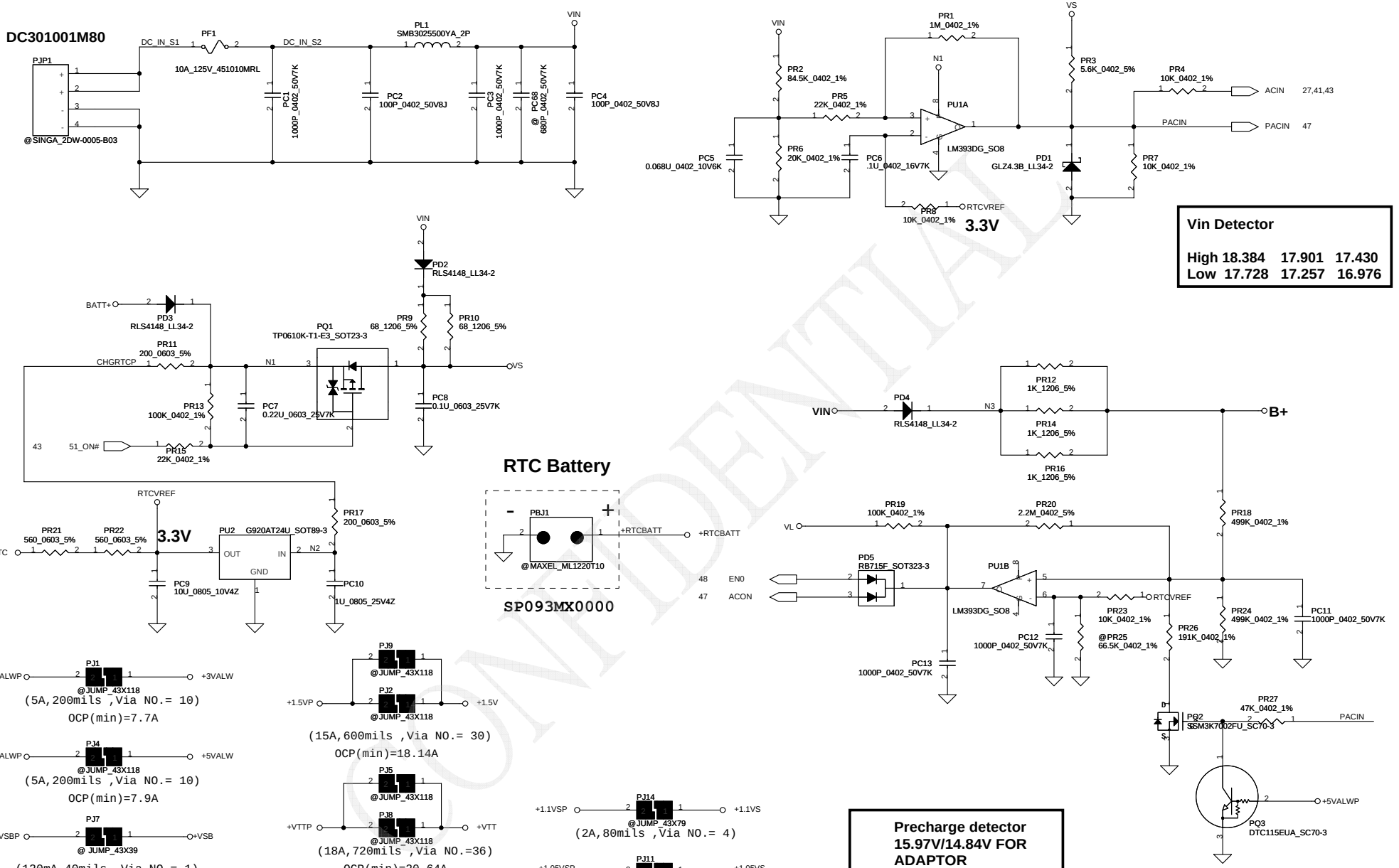

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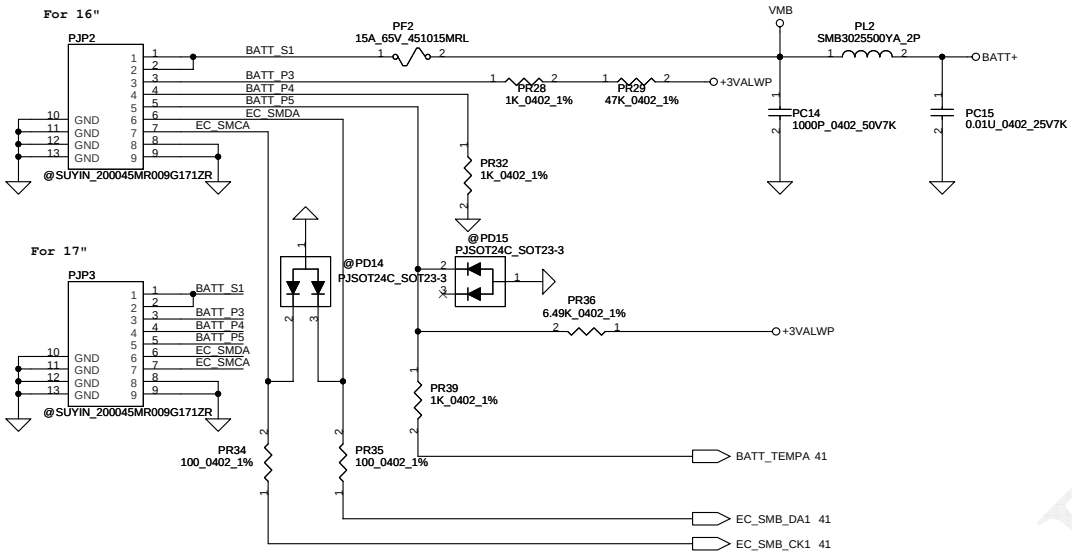
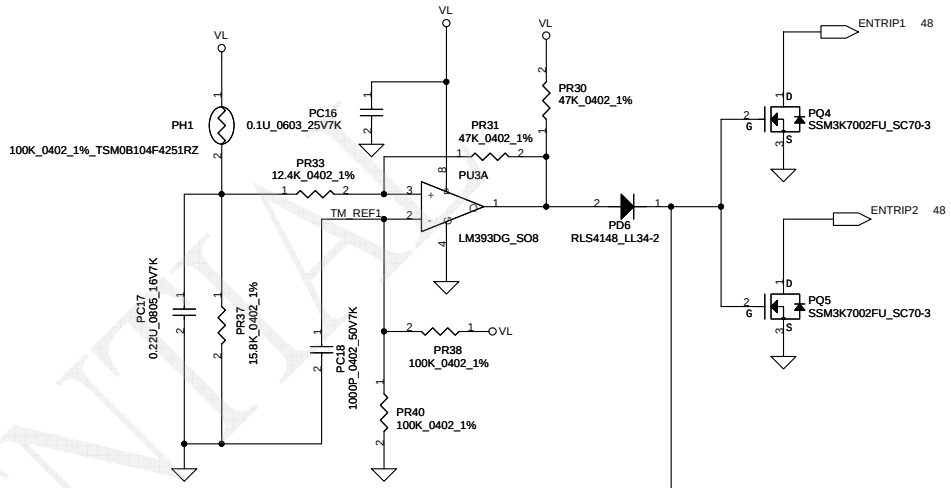
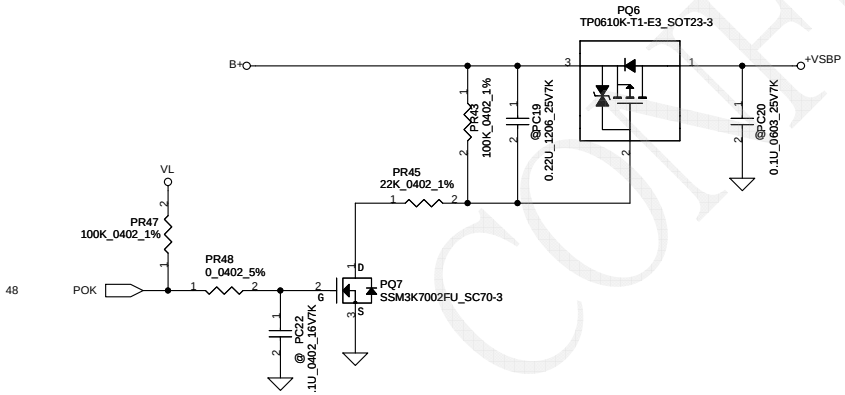
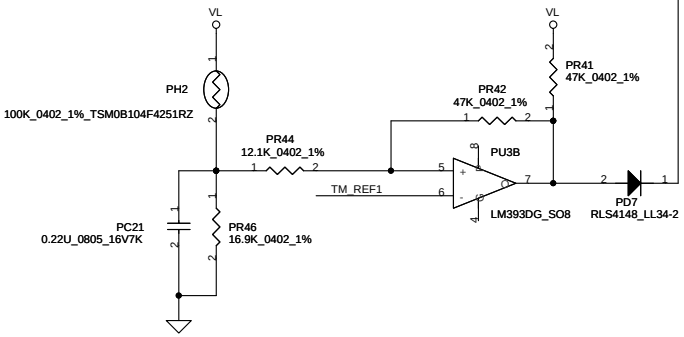
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 55 degree C





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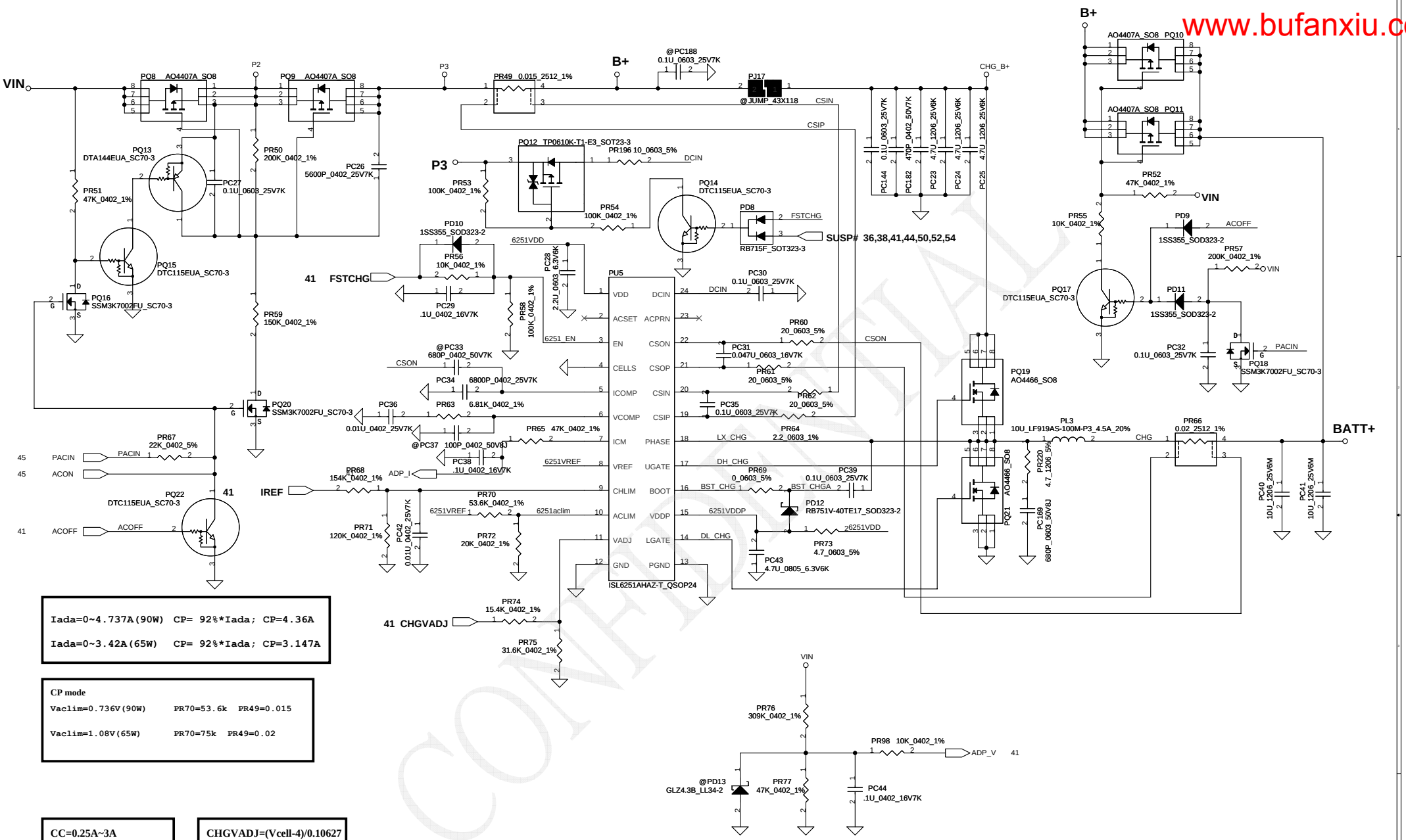

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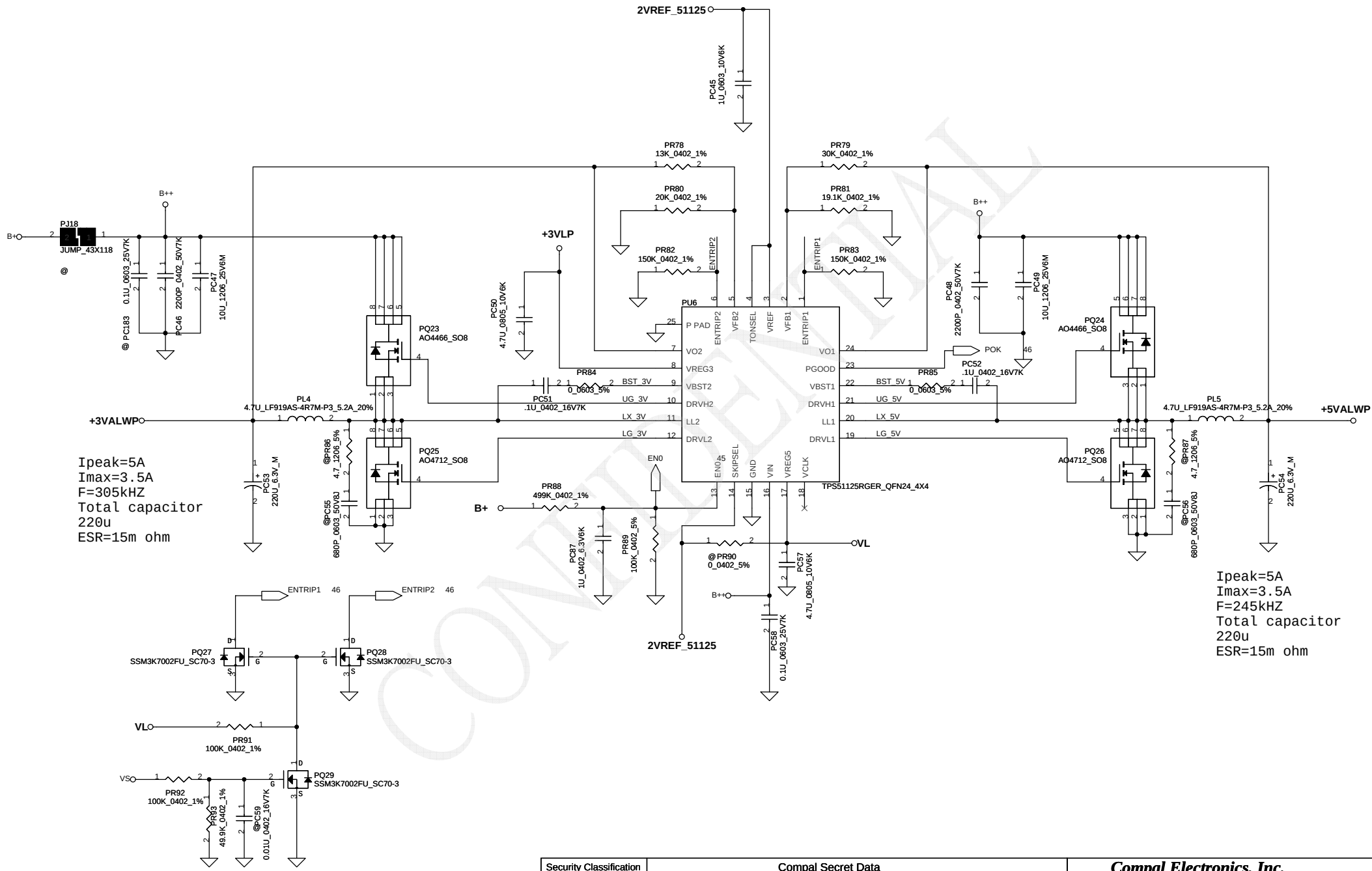

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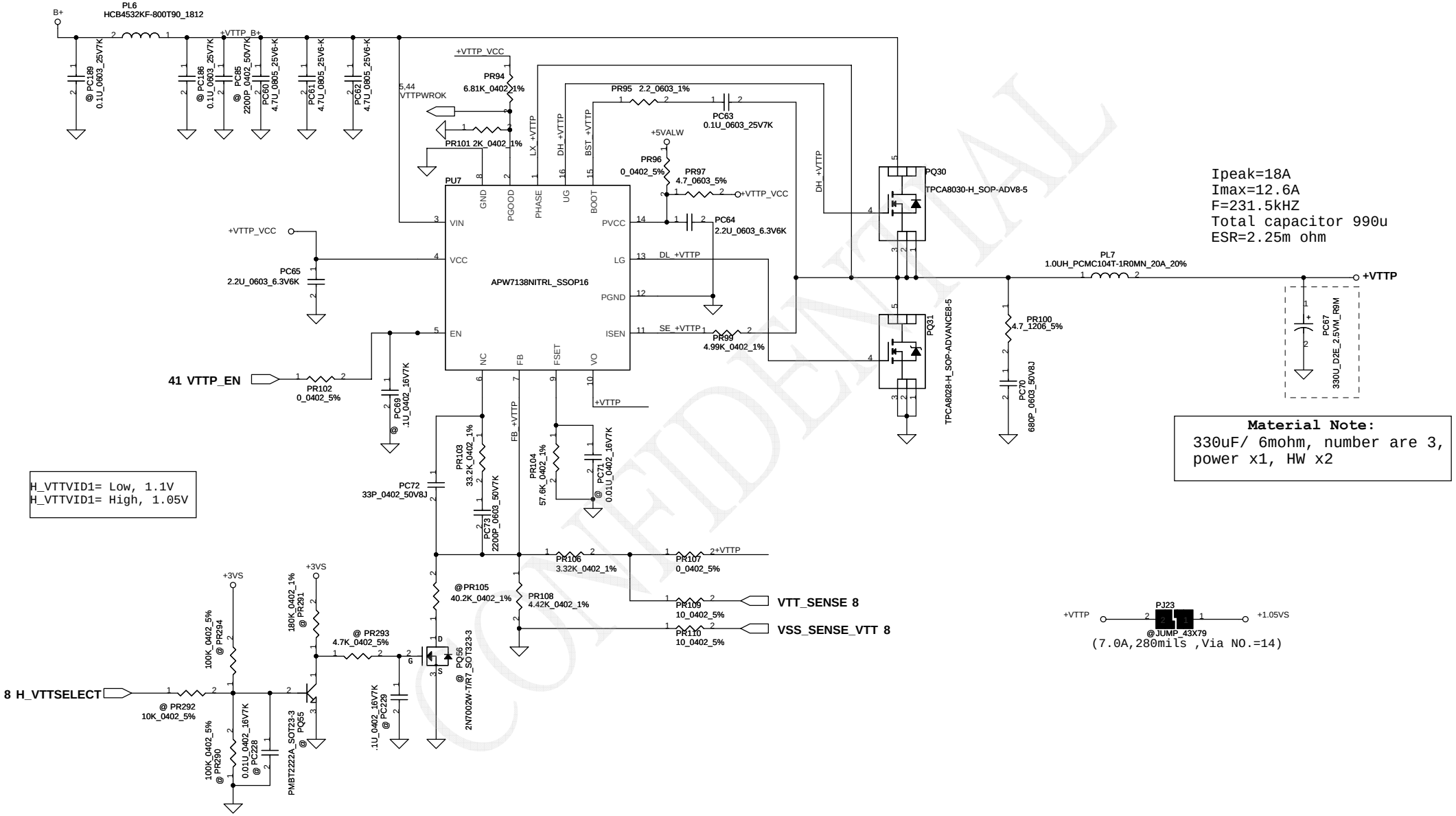

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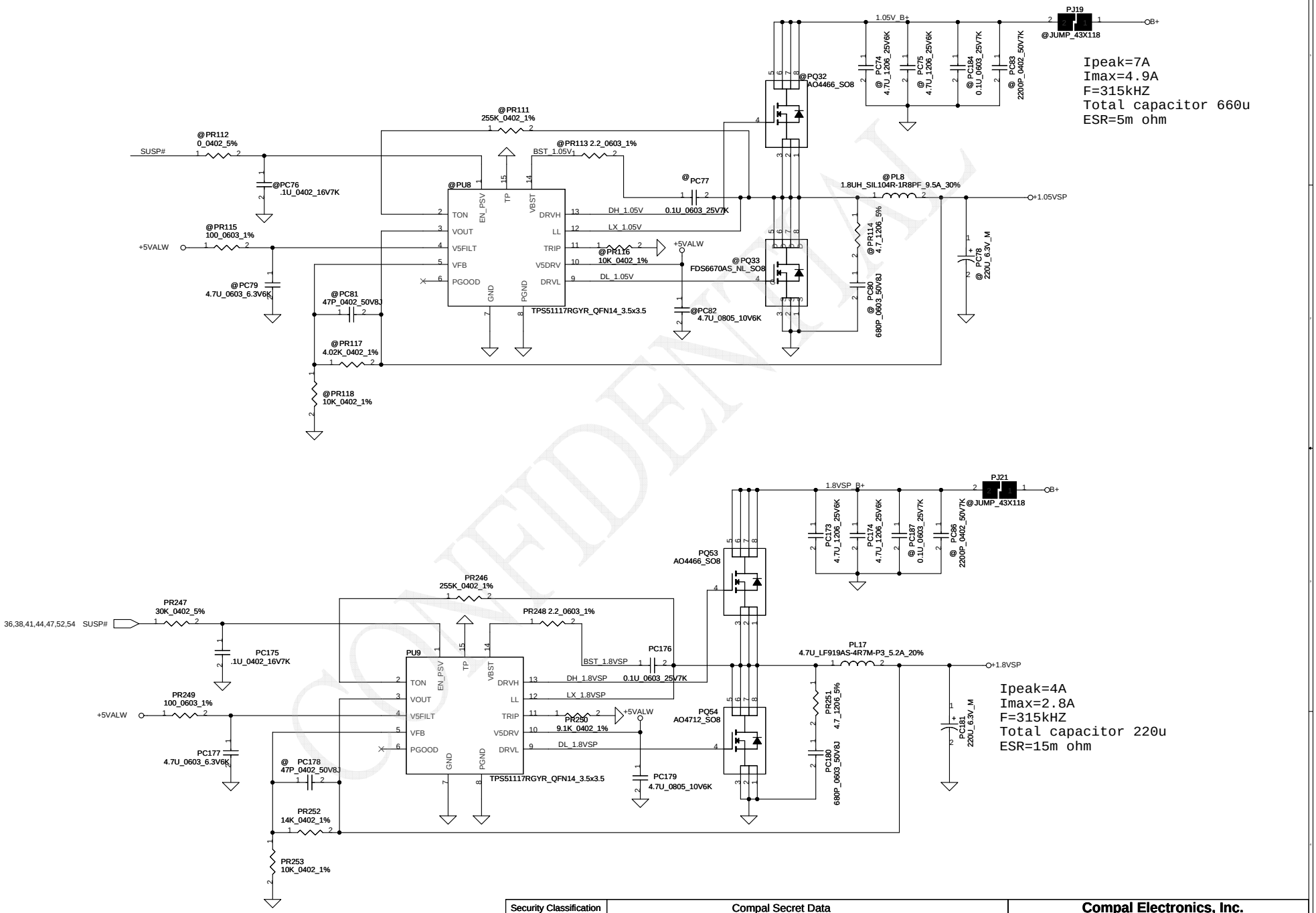

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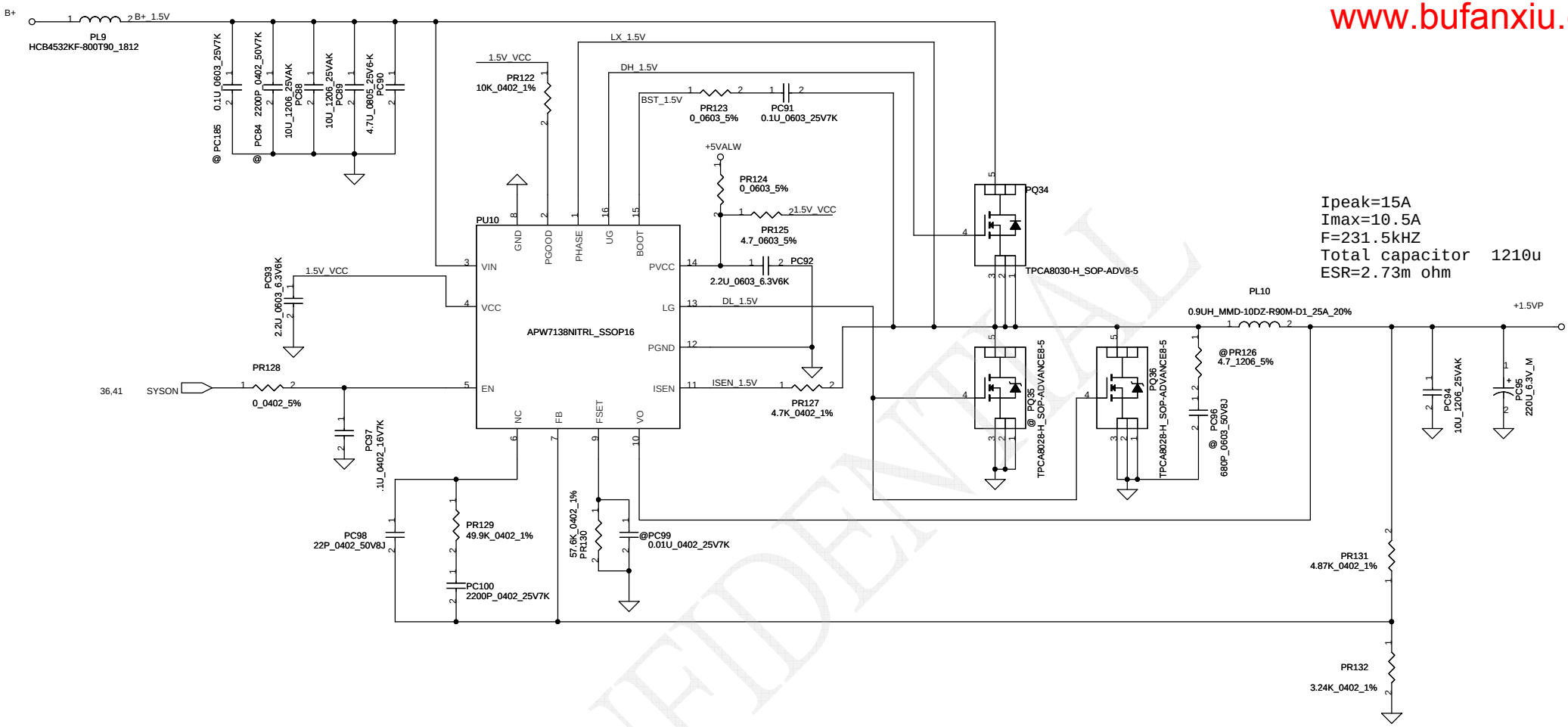

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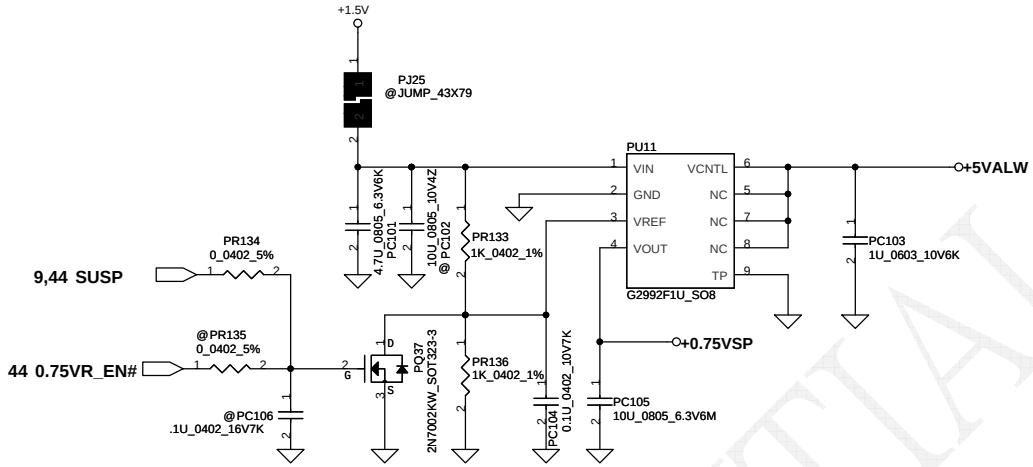

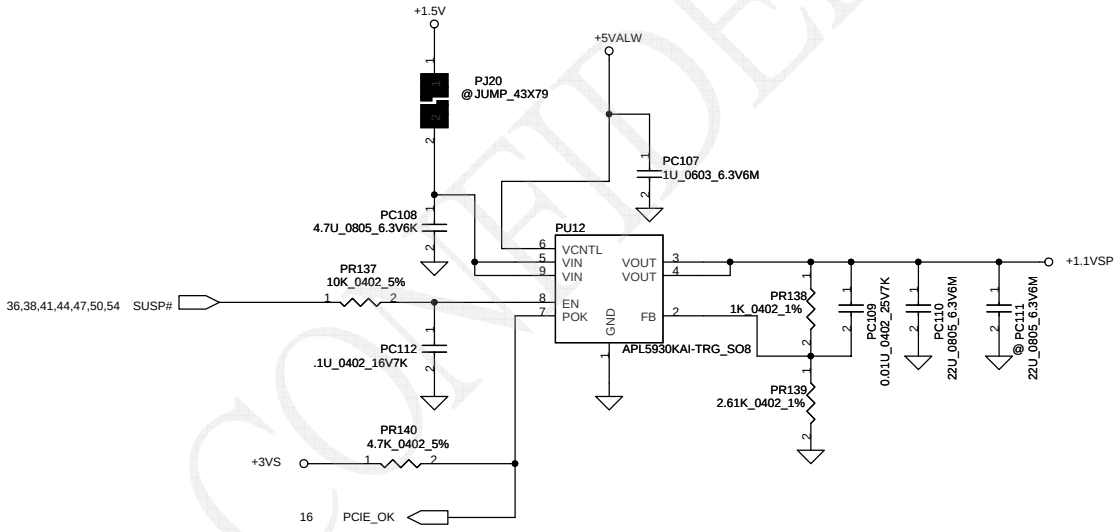

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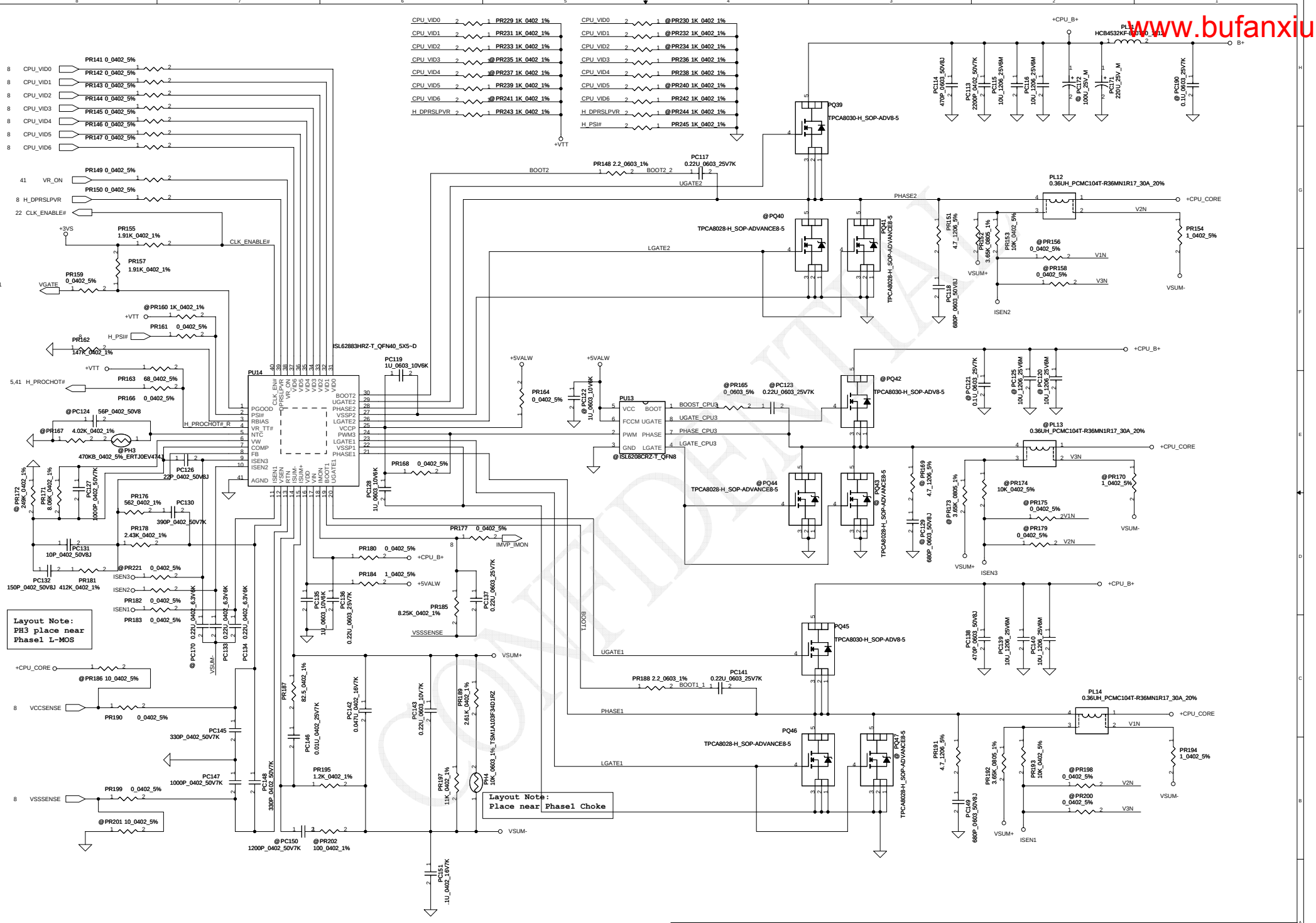

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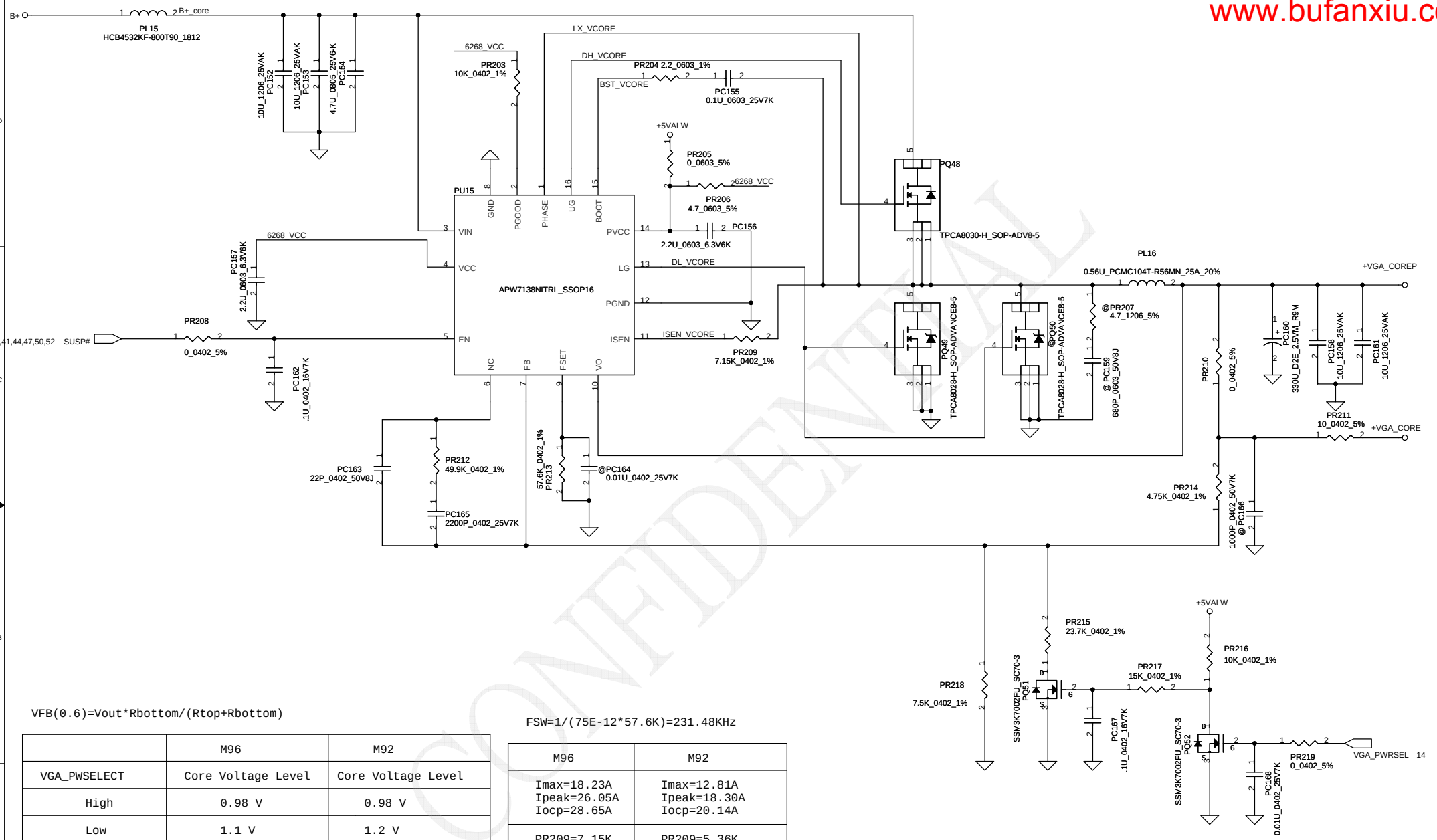

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

	M96	M92
VGA_PWSELECT	Core Voltage Level	Core Voltage Level
High	0.98 V	0.98 V
Low	1.1 V	1.2 V
resistor setting	PR214 = 4.75K PR218 =7.5K PR215 =23.7K	PR214 = 4.75K PR218 = 7.5K PR215 = 13K

FSW=1/(75E-12*57.6K)=231.48KHz

M96	M92
Imax=18.23A Ipeak=26.05A Iocp=28.65A	Imax=12.81A Ipeak=18.30A Iocp=20.14A
PR209=7.15K PQ50=unpop	PR209=5.36K PQ50=unpop

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PIR (Product Improve Record)

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NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	3/25	31,32	DEL L14,C302,L15,C312,L16,C314,C315,L19,C339,C340	DG1.5: these pins have internal VRM

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	6/29	11	Add R92,R93	To support M1 mode
	6/29	27	Change R324 from 10K to 330K	To solve ACIN LED issue
	7/02	30	Change BT_PWR# from GPIO0 to GPIO34, add VGA_HDMI_HPD on GPIO0.	For common design with NSKAA
	7/02	35	DEL JCAM (R431,R432,C403,R371,R373,R374,R375,L20)	CAM cable combine with LVDS
	7/02	22	DEL R387	Remove +5VALW power to camera
	7/02	40	DEL YC1,CC10,CC12	Remove 12MHz crystal to cardreader
	7/02	40	DEL RC2	Remove +3VALW to cardreader
	7/02	15~18	Add LV31,CV253,CV236,CV270,LV35,LV36,CV303,CV304, CV305,CV306,CV307,CV308,LV34,RV157,RV156,RV24,RV56 RV59,RV60,RV126,RV127	Reserve for support Park/Madsion
	7/03	22	Add R120,R401	Reserve +1.5VS to clk gen for low power clk gen test
	7/03	22,30	Add R154	Reserve LVDS_SEL on PCH GPIO45
	7/03	30,41	Connect PCH GPIO33 to EC pin 103 as PWRME_CTRL Change 3G_OFF# from EC pin 103 to pin 107	To reflash ME BIOS
	7/17	43	Add R50 on SATA_LED#	Reserve for cost down plan
	7/17	29	DEL R277,D12, Connect USB_OC#3_D to USB_OC#3	
	7/17	27,41,43	DEL R384, D14. Add R331	Modify ACIN circuit
	7/17	22,43	Change Q7,Q34 to Dual Q35	For cost down
	7/20	5,9,11, 30,44	Add Q41,R19,R123,R22,D54,U10,R33,R52,Q33,R424,R417, C179,Q46,C472,R417,R418,C205,C186,C185,C180,PJ30,PJ31, R80,Q44,R425,R158,Q39,Q40,R94,R95,R122,R121 Add RST_GATE on PCH GPIO46	Reserve S3 power reduction circuit
	7/27	41	Add R5	To solve SYSON glitch issue
	7/27	30,41	Connect PCH GPIO49 to EC pin25 as THM_ALT#	Reserve for test
	7/27	8,9,11, 16,20	Add C144,C159,C218,C216,C217,CV309,CV310,CV311,CV312	For cost down
	7/30	9,44	Add C160,C256,C257,C258,C473,C475	For EMI request
	7/30	25,42	Change U13 to 8MB, U22 to 1MB	For SW and EC request

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PIR (Product Improve Record)

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	8/19	14,22	Add R159,R160 for VGA BKL control	Reserve for deep green test
	9/1		Change +3VL to +3VALW, DEL PJ12	.
	9/1	25,42	Change EC ROM to 256KB and PCH ROM to 4MB	For PVT test
	9/1	34	Add L52,R72,R85,L53,R73,R87,L54,R77,R88	For EMI request
	9/9	37	Connect WOL_EN# to LAN IC	For PVT test

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	9/30	25	Change C287,C290 from 18p to 15p	To fine tune RTC timing
	9/30	5	Change R22 from 10k to 1k	Modify S3 circuit
	10/28	5	Reserve C301,C384,C389	Reserve for S3 power saving circuit

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P47-PWR_CHARGER	Change PR65 100 to 47k	For CPU throtting setting (2009/05/20)
EVT		P48-PWR_3VALWP/5VALWP	Change PR81 19.6k to 19.1k	modify +5VALWP voltage to 5.14V (2009/05/20)
EVT		P49-PWR_+1.1V_VTTP	Add PR290 100K, PR291 180K, PR292 10K, PR293 4.7K, PR294 100K, PC228 0.01U, PC229 0.1U, PQ55,PQ56	Add switching circuit for H_VTTSELECT function (2009/05/20)
EVT		P49-PWR_+1.1V_VTTP	Change PR94 10K to 3.4K Add PR101 1K	Set VTTPWROK voltage level to 1.1V (2009/05/20)
EVT		P53-PWR_CPU_CORE	Remove PR186,PR201 10 Ohm	Modify CPU_CORE circuit (2009/05/27)
EVT		P46-PWR_BATTERY CONN / OTP	Change PH1,PH2 0603 sizt to 0402 size	For cost down (2009/05/27)
EVT		P50-PWR_1.05VSP/1.8VSP	Change PR115,PR249 422Ohm to 100 Ohm Change PC79,PC177 1U to 4.7U	avoid 2nd source RT8209B can no power on (2009/06/05)
EVT		P52-PWR_0.75VSP/1.1VSP	Change PU12 APL5913 to APL5930	For cost down (2009/06/05)
EVT		P45-PWR_DCIN/DECTOR	Remove DC301000F00	Remove DC IN JACK((2009/06/05))
EVT		P54-PWR_VGA_COREP	Change PR210 10 Ohm to 0 Ohm Change PR211 0 Ohm to 10 Ohm	Change VGA_CORE sense from HW terminal to PWR (2009/06/05)
EVT		P54-PWR_VGA_COREP	Change PL16 0.36U to 0.56U	Change CPU_CORE CHOKE to 0.56U(2009/06/05)
EVT		P50-PWR_1.05VSP/1.8VSP	Change PR116 14.7k to 10k Change PR250 15.4k to 9.1k	Set 1.05V OCP to 8.54A(2009/06/05) Set 1.8V OCP to 4.93A(2009/06/05)
EVT		P51-PWR_1.5VP	Change PR127 7.15k to 2.1k	Set 1.5V OCP to 17A(2009/06/05)
EVT		P49-PWR_+VTTP	Change PR99 5.9k to 2.43k	Change VTT OCP to 19.7A(2009/06/05)
DVT		P50-PWR_1.05VSP/1.8VSP	Add PC175 0.1U Change PR247 0 to 30k	For power sequence(2009/07/07)
DVT		P49-PWR_+VTTP	Change PR99 2.43k to 4.99k	Set OCP(2009/07/07)
DVT		P51-PWR_1.5VP	Change PR127 2.1k to 4.7k	Set OCP(2009/07/07)
DVT		P45-PWR_CPU_CORE	PC133, PC134 SE083224Z80 to SE124224K80	PC133, PC134 tolerance Y5V to X5R(2009/0/07)
DVT		P50-PWR_1.05VSP/1.8VSP	Change PC79, PC177 SE00000MAN0 to SE107475K80	Change part number(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC87 1U_0402_6.3V6K	Avoid pre-charge can not finish(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC45 0.22U to 1U	Prevent +3VALW/+5VALW can't boot up (2009/07/07)
DVT		P45-PWR_CPU_CORE	Change PR229~PR245 and PR160 10k to 1k	Change VID, PSI# and DPRSLPVR select resistor from 10k to 1k (2009/07/17)
DVT		P45-PWR_CPU_CORE	Change PR157 10k to 1.91k	Change PGOOD pull high resistor 10k to 1.91k(2009/07/17)
DVT		P45-PWR_CPU_CORE	Remove PH3, PC124, PR167 Change PC133, PC134, PC170 pin 2 from GND to VSUM- Change PR152, PR192 0402 size to 0805 size	Modify circuit for CPU_CORE(2009/07/17)
DVT		P39-PWR_BATTERY CONN / OTP	Change +3VLP to +3VALWP	Remove +3VLP power rail (2009/07/17)

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
DVT		P47-PWR_CHARGER	Reserve PC188 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P49-PWR_+VTTP	Reserve PC189 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P49-PWR_+VTTP	Change PR95 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P49-PWR_+VTTP	Add PR100 4.7 ohm, PC70 680P	Add snubber (2009/07/23)
DVT		P49-PWR_+VTTP	Change PR94 3.4k to 1.5k, PR101 1k to 3k	For HW solution(S3 power reduction) (2009/07/23)
DVT		P49-PWR_+VTTP	Add PJ23	For power test(2009/07/23)
DVT		P52-PWR_0.75VSP/1.1VSP	Add 0.75VR_EN control signal	For HW solution(S3 power reduction) (2009/07/23)
DVT		P53-PWR_CPU_CORE	Add PR151, PR191 4.7 ohm, PC118, PC149 680P	Add snubber (2009/07/23)
DVT		P53-PWR_CPU_CORE	Change PR148, PR188 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P53-PWR_CPU_CORE	Add PC190 0.1U	Reserve for EMI solution (2009/07/23)
DVT		P45-PWR_CPU_CORE	Remove PQ40, PQ47	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC101 10U to 4.7U	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC106 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PC151 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT			Change PC53, PC54, PC78, PC95, PC181 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PR195 1.1k to 1.2k	Change Ri for load line (2009/08/03)
DVT		P45-PWR_CPU_CORE	Remove PR202 100 ohm, PC150 1200P	Modify CPU_CORE circuit (2009/08/03)
DVT		P49-PWR_+VTTP	Change PU7 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC71 0.01U	For APW7138 solution (2009/08/03)
DVT		P51-PWR_1.5VP	Change PU10 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC99 0.01U	For APW7138 solution (2009/08/03)
DVT		P54-PWR_VGA_COREP	Change PU15 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC164 0.01U	For APW7138 solution (2009/08/03)
DVT		P51-PWR_1.5VP	Change PL9 SM01000DJ00 to SM010018210	Use same PN bead (2009/08/03)
DVT		P53-PWR_CPU_CORE	Change PL11 SM010020720 to SM010018210	Use same PN bead (2009/08/03)
DVT		P54-PWR_VGA_COREP	Change PL15 SM01000DJ00 to SM010018210	Use same PN bead (2009/08/03)
DVT		P39-PWR_BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Set OTP (2009/08/03)
			Change PR37 15.4k to 15.8k	
DVT		P47-PWR_CHARGER	Add PR220 4.7 ohm, PC169 680P	Add charger snubber(RF solution) (2009/08/03)
			Add PC144 0.1U, PC182 470P	Add charger snubber(RF solution) (2009/08/03)
DVT		P45-PWR_CPU_CORE	Add PC113 2200P, PC114 470P, PC138 470P	RF solution (2009/08/03)
PVT		P42-PWR_+VTTP	Change PL7 0.47U to 1U	Design change (2009/09/04)
PVT		P42-PWR_+VTTP	Remove PC66, PC68 10U	Design change (2009/09/04)
PVT		P47-PWR_CHARGER	Change PR70 8.25k to 53.6k, PR72 26.7k to 20k	Set 90W CP (2009/09/04)
PVT		P45-PWR_DCIN/DECTOR	Add PC68 680P	For EMI solution (2009/09/14)
PVT		P46-PWR_BATTERY CONN / OTP	Add PD14, PD15	Reserve for EMI(ESD diode) (2009/09/14)
PVT		P42-PWR_+VTTP	Remove PR290, PR291, PR292, PR293, PR105, PC228, PC229, PQ55, PQ56	Remove VTTP voltage switch circuit(arrandale only) (2009/09/14)
PVT		P47-PWR_CHARGER	Change PR64 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P49-PWR_+VTTP	Change PR95 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P50-PWR_1.05VSP/1.8VSP	Change PR113, PR248 0 ohm to 2.2 ohm	Add boot trap resistor (2009/09/14)
			Add PR114, PR251 4.7 ohm, PC80, PC180 680P	Add snubber (2009/09/14)
PVT		P45-PWR_CPU_CORE	Change PR148, PR188 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P54-PWR_VGA_COREP	Change PR204 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P50-PWR_1.05VSP/1.8VSP	Change PR117 8.25k to 4.02k	Avoid FB trace noise (2009/09/18)
			Change PR118, PR253 20.5k to 10k	
			Change PR252 28.7k to 14k	
PREMP		P45-PWR_DCIN/DECTOR	Change PC7 SE041224K80 to SE000005Z80	Change CAP size from 1206 to 0603 (2009/10/09)
PREMP		P46-PWR_BATTERY CONN / OTP	Change PR44 13.7k to 12.1k	Modify OTP setting (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change PL12, PL14 SH000005680 to SH12036BM00	Use 5% tolerance DCR choke (2009/10/09)
PREMP		P51-PWR_1.5VP	Change PR131 4.75k to 4.87k	Adjust voltage divided resistor (2009/10/27)
PREMP		P49-PWR_+VTTP	Change PR94 1.5k to 39.2k	Adjust VTTPWROK voltage 3.3V to 1.05V (2009/10/27)
			Change PR101 3k to 10.5k	
PREMP		P50-PWR_1.05VSP/1.8VSP	Remove 1.05V component	Cost down (2009/11/3)
MP		P49-PWR_+VTTP	Change PR94 39.2k to 6.81k	Modify resistor for VTTPWROK voltage (2009/11/26)
			PR101 10.5k to 2k	

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