

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM+ICH9-M SFF core logic

ULV core logic HDI board

DISCRETE VGA M92

2009-06-19 V.03

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Model Name : NAW20

File Name : LS-5588P

ULV

Thermal Sensor

page 4

Mobile Peryn

LV/ULV Dual Core
uFCPGA-956 CPU - SFF

page 4, 5, 6, 7

CK505

Clock Generator
ICS9LPRS387BKLFT
MLF 72P

page 16



DISCRETE VGA HDI BRD
page 17,18,19,20,21

ATI M92 S2

600MHz

VRAM DDR3
512MB(64Mx16)

RGB
Single Channel

H_A#(3..35)
H_D#(0..63)

FSB

667/800/1066MHz 1.05V

Intel Cantiga GS

FCBGA 1363 - SFF

page 8,9,10,11,12,13

DDR3 1066MHz 1.5V

Dual Channel

DDR3-SO-DIMM X 2

BANK 0, 1, 2, 3

page 14,15

DMI X4

Intel ICH9-M

WBMMAP-569 - SFF

page 22,23,24,25

HDA

Golden finger

HDI to I/O board

page 26

HDMI

CRT

LVDS

LPC

PCIE

USB

SATA

ODD

HDD

ESATA

CardReader

USB*2

BT

CMOS

minIPCE*2

LAN

minIPCE*1

I/O BRD PORTION

EC

HDA

AUDIO

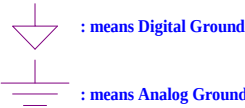
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Block Diagram		
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Voltage Rails (0 MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75VS +VCCP +CPU_CORE +VGA_CORE +1.1VS +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
ME@ : means ME part.
45@ : means install after SMT.

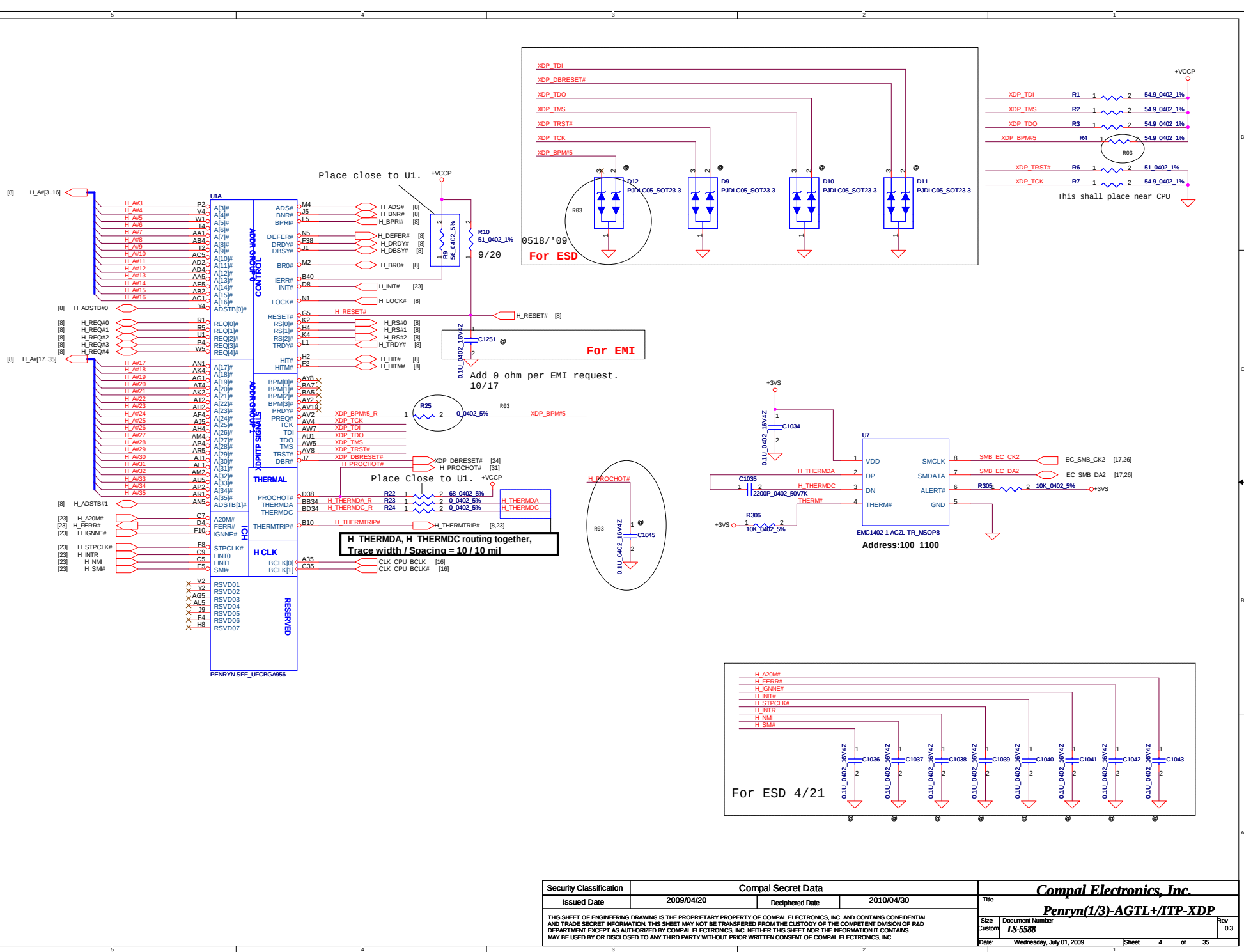
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CLK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CLK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CLK_CLK1 SMB_CLK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

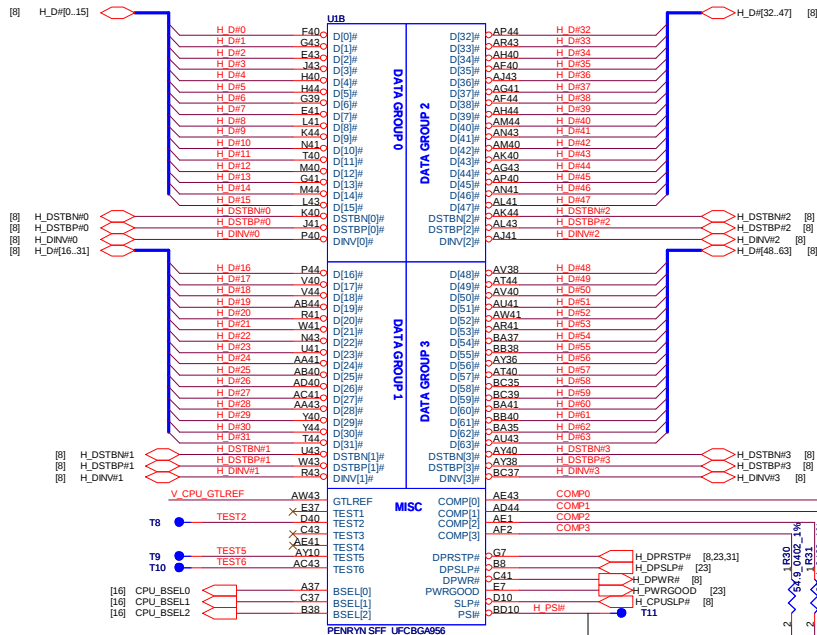
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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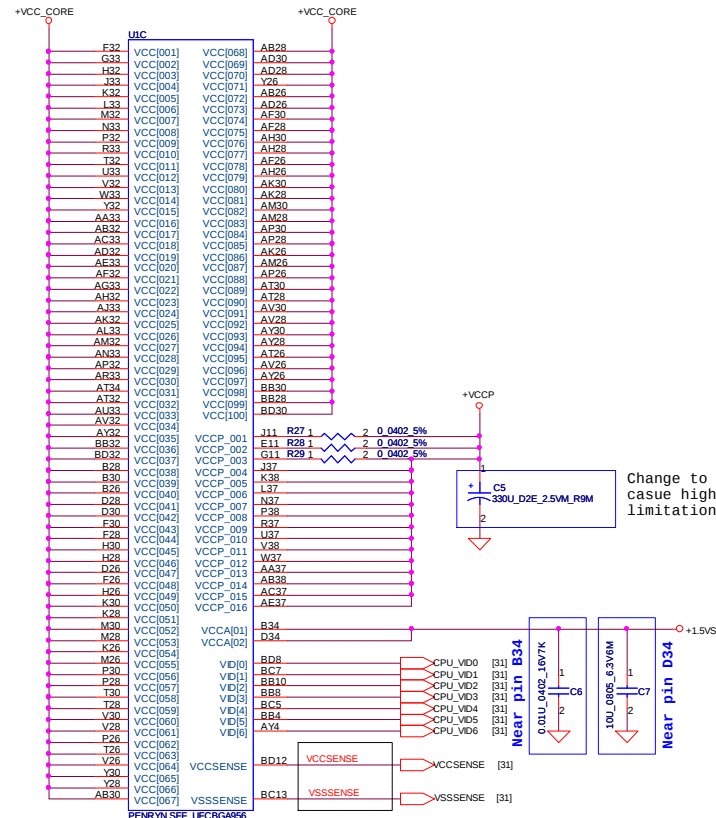


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

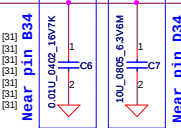
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

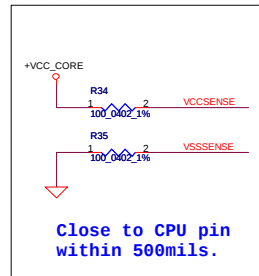
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



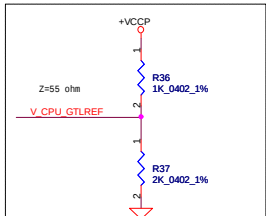
Change to 330u_R9, casue high limitation. 12/14



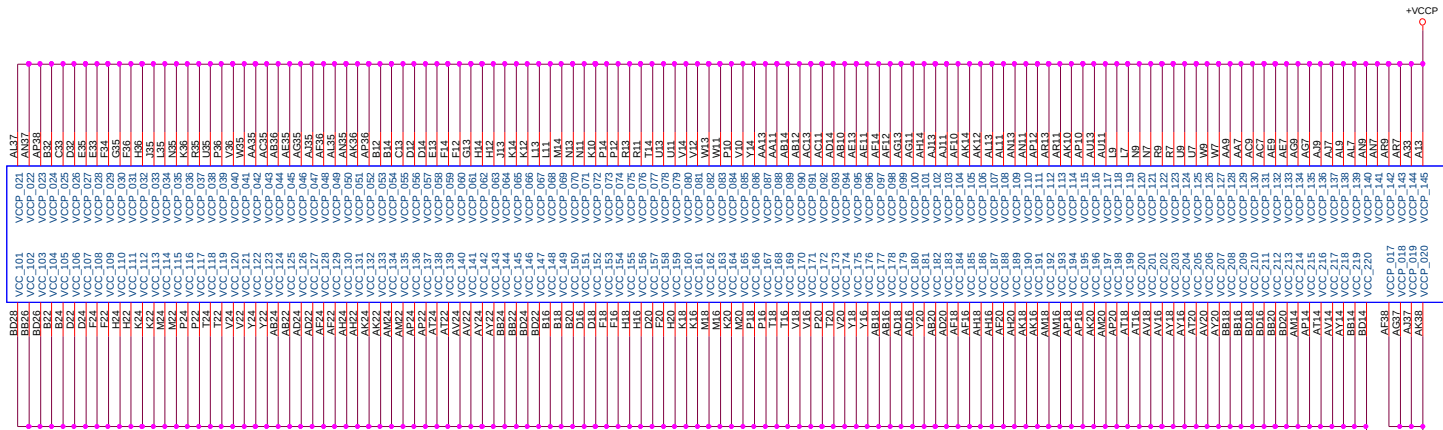
Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin within 500mils.

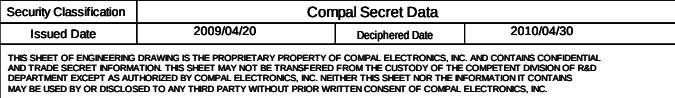


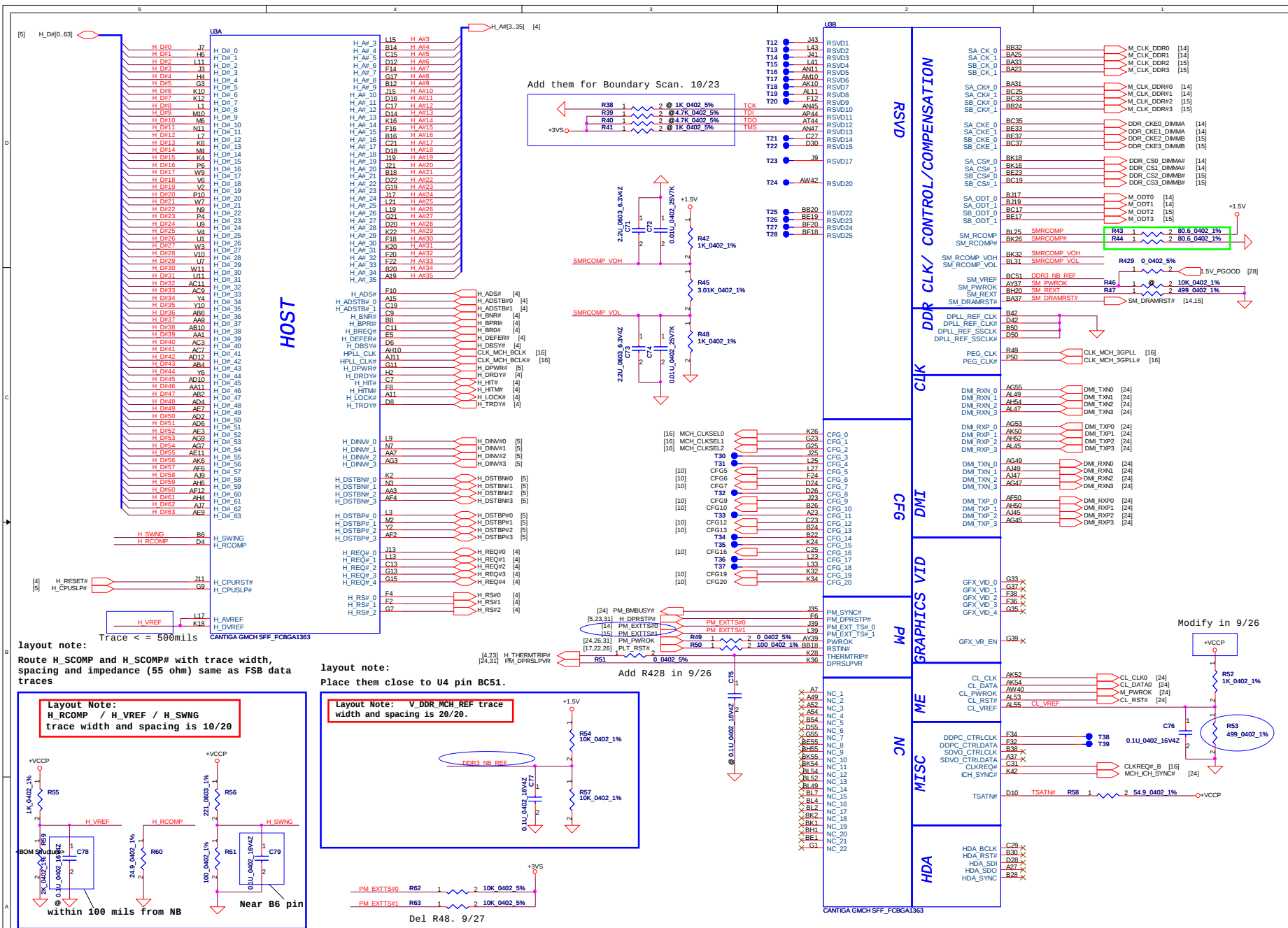
Close to CPU pin AW43 within 500mils.



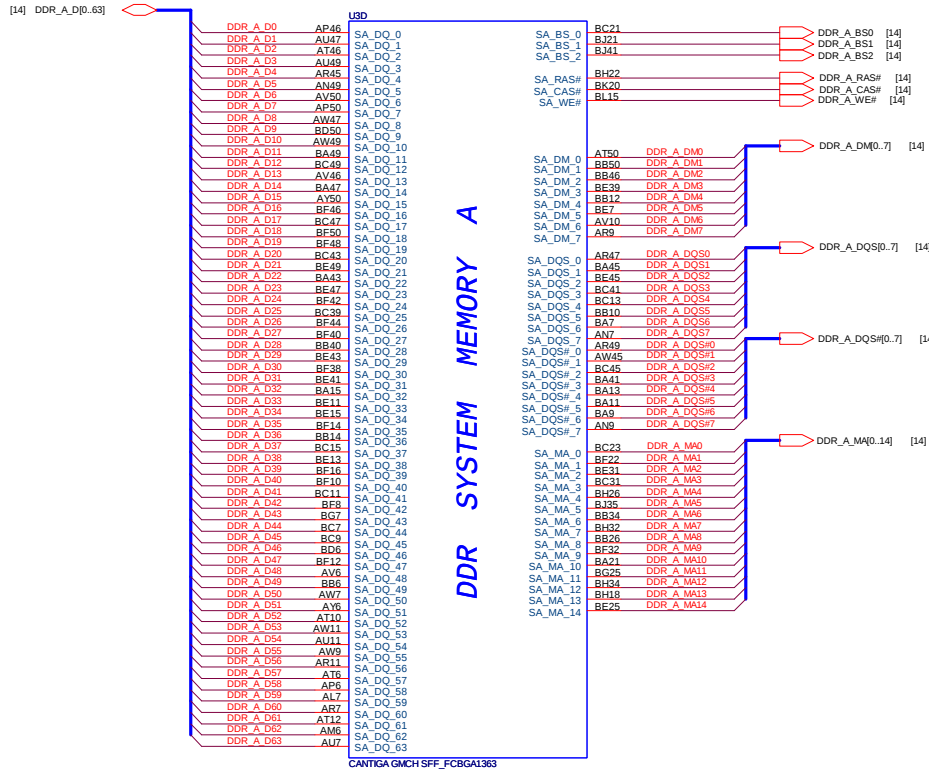
U1F
PENRYN SFF_UFCBG956

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				Penryn(3/3)-Power	
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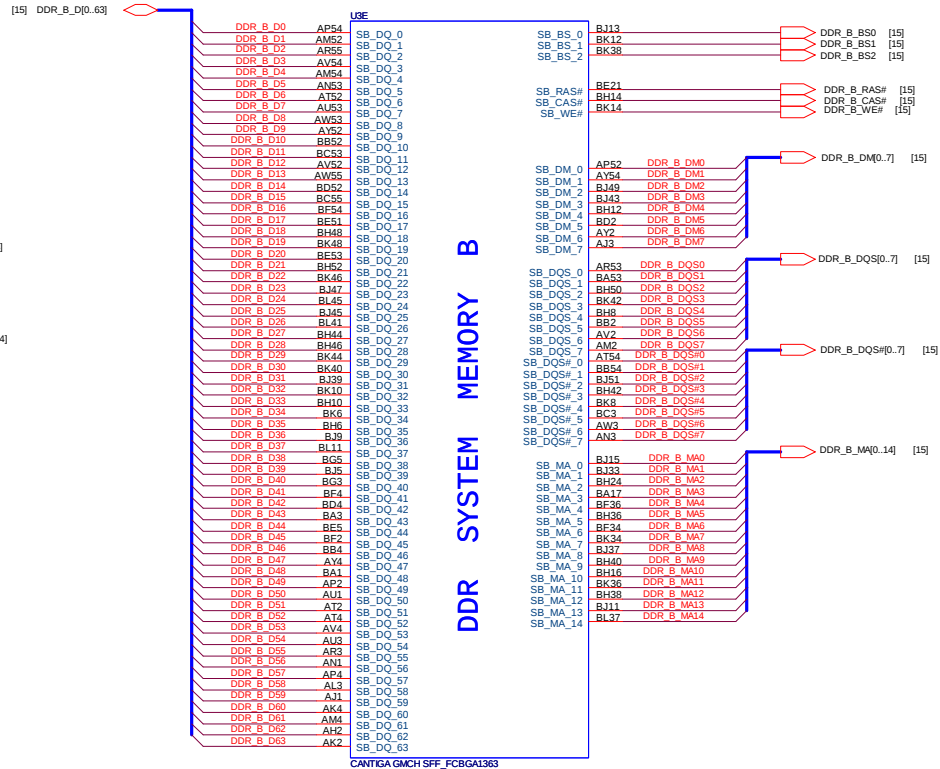


DDR SYSTEM MEMORY A



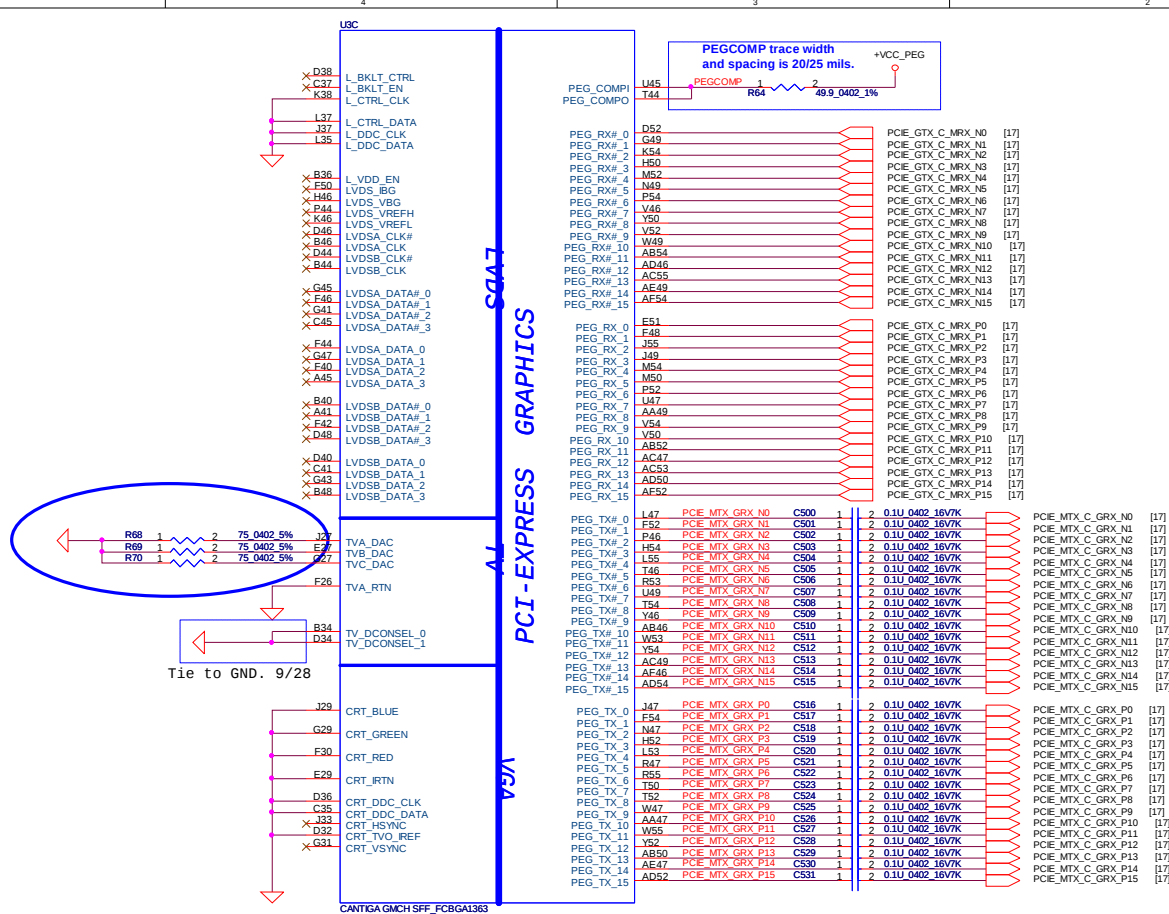
CANTIGA GMCH SFF_FCBGA1363

DDR SYSTEM MEMORY B



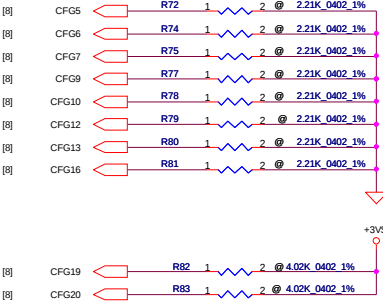
CANTIGA GMCH SFF_FCBGA1363

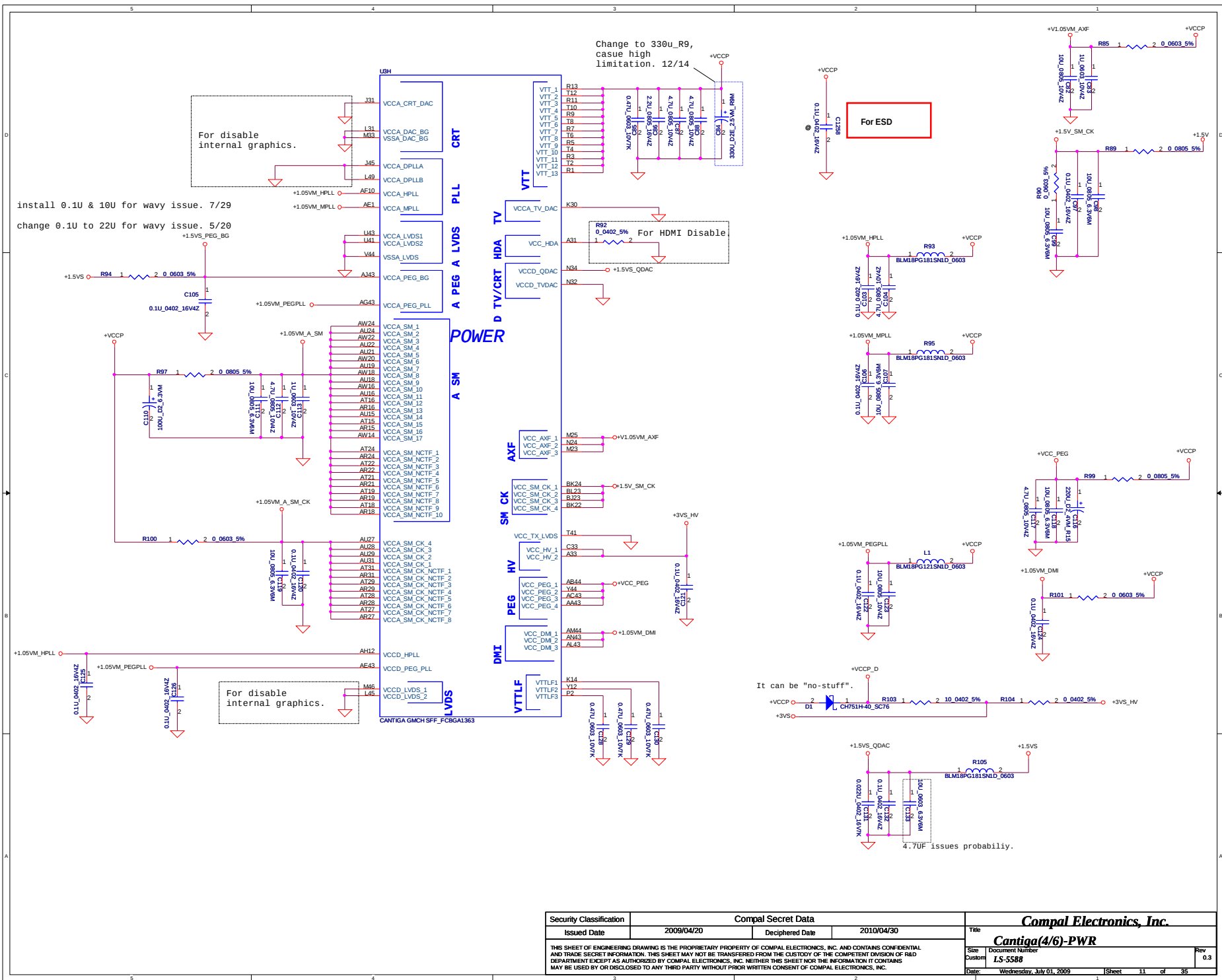
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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 =(TLS)chiper suite with no confidentiality 1 =(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.





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U3

BA55	VSS_1	C43
AU55	VSS_2	A43
AN55	VSS_3	BD42
AJ55	VSS_4	H42
AE55	VSS_5	BG41
AA55	VSS_6	AY41
VSS_6	VSS_6	AM41
U55	VSS_7	AL41
BD54	VSS_8	AG41
BG53	VSS_9	AE41
AJ53	VSS_10	AA41
AE53	VSS_11	R41
AA53	VSS_12	M41
N53	VSS_13	E41
U53	VSS_14	BD40
N53	VSS_15	AU40
JS3	VSS_16	AR40
GS3	VSS_17	AM40
ES3	VSS_18	W40
K52	VSS_19	U40
BG51	VSS_20	T40
BA51	VSS_21	R40
AM51	VSS_22	K40
AU51	VSS_23	H40
AR51	VSS_24	BL39
AN51	VSS_25	BG39
AL51	VSS_26	BA39
AJ51	VSS_27	E39
AE51	VSS_28	C39
AC51	VSS_29	M37
AA51	VSS_30	E37
W51	VSS_31	BD36
U51	VSS_32	AM36
R51	VSS_33	H36
N51	VSS_34	BL35
LS1	VSS_35	BG35
JS1	VSS_36	AY35
GS1	VSS_37	AL35
C51	VSS_38	AG35
BK50	VSS_39	AE35
AM50	VSS_40	AA35
K50	VSS_41	Y35
BG49	VSS_42	M35
E49	VSS_43	E35
C49	VSS_44	A35
BD48	VSS_45	BD34
BB48	VSS_46	AU34
AY48	VSS_47	AN34
AV48	VSS_48	H34
AT48	VSS_49	BL33
AP48	VSS_50	BG33
AM48	VSS_51	AY33
AK48	VSS_52	E33
AH48	VSS_53	BD32
AF48	VSS_54	AJ32
AD48	VSS_55	AG32
AB48	VSS_56	AC32
Y48	VSS_57	Y32
V48	VSS_58	H32
T48	VSS_59	B32
P48	VSS_60	BJ31
M48	VSS_61	BC31
K48	VSS_62	AY31
H48	VSS_63	AN31
BL47	VSS_64	M31
BG47	VSS_65	E31
E47	VSS_66	N30
C47	VSS_67	H30
A47	VSS_68	AN29
BD46	VSS_69	AJ29
AY46	VSS_70	M29
AM46	VSS_71	A29
AK46	VSS_72	AW28
AH46	VSS_73	AN28
BG46	VSS_74	AD28
AE46	VSS_75	AC28
AC46	VSS_76	Y28
AA46	VSS_77	W28
W46	VSS_78	H28
R45	VSS_79	E28
N45	VSS_80	AN27
E45	VSS_81	AJ27
BD44	VSS_82	BF26
BB44	VSS_83	BD26
AK44	VSS_84	N26
AH44	VSS_85	H26
AF44	VSS_86	BJ25
AD44	VSS_87	AY25
K44	VSS_88	AU25
H44	VSS_89	
BL43	VSS_90	
BG43	VSS_91	
E43	VSS_92	
C43	VSS_93	
A43	VSS_94	
BD42	VSS_95	
H42	VSS_96	
BG41	VSS_97	
AY41	VSS_98	
AM41	VSS_99	

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U3J

AN25	VSS_199	VSS_300	AM8
AG25	VSS_200	VSS_301	AK8
AE25	VSS_201	VSS_302	AH8
AA25	VSS_202	VSS_303	AF8
Y25	VSS_203	VSS_304	AD8
E25	VSS_204	VSS_305	AB8
A25	VSS_205	VSS_306	V8
BD24	VSS_206	VSS_307	V8
AN24	VSS_207	VSS_308	P8
AL24	VSS_208	VSS_309	M8
H24	VSS_209	VSS_310	K8
BG23	VSS_210	VSS_311	H8
AY23	VSS_211	VSS_312	B177
E23	VSS_212	VSS_313	E7
BD22	VSS_213	VSS_314	BF6
BR22	VSS_214	VSS_315	BC5
AN22	VSS_215	VSS_316	BA5
Y22	VSS_216	VSS_317	AW5
W22	VSS_217	VSS_318	AU5
H22	VSS_218	VSS_319	AR5
BL21	VSS_219	VSS_320	AN5
BG21	VSS_220	VSS_321	AL5
AY21	VSS_221	VSS_322	AJ5
AN21	VSS_222	VSS_323	AG5
AE21	VSS_223	VSS_324	AE5
E21	VSS_224	VSS_325	AC5
M21	VSS_225	VSS_326	AA5
C21	VSS_226	VSS_327	W5
A21	VSS_227	VSS_328	U5
BD20	VSS_228	VSS_329	N5
H20	VSS_229	VSS_330	L5
BG19	VSS_230	VSS_331	J5
AY19	VSS_231	VSS_332	G5
AL19	VSS_232	VSS_333	C5
H19	VSS_233	VSS_334	BH4
BD18	VSS_234	VSS_335	BE3
N18	VSS_235	VSS_336	U3
H18	VSS_236	VSS_337	E3
BL17	VSS_237	VSS_338	BC1
BG17	VSS_238	VSS_339	AW1
AY17	VSS_239	VSS_340	AR1
AN17	VSS_240	VSS_341	AL1
E17	VSS_241	VSS_342	AG1
AL17	VSS_242	VSS_343	AE1
BD16	VSS_243	VSS_344	W1
AN16	VSS_244	VSS_345	N1
AG16	VSS_245	VSS_346	J1
Y16	VSS_246	VSS_347	AU13
W16	VSS_247	VSS_348	BB42
H16	VSS_248	VSS_349	AW38
BG15	VSS_249	VSS_350	BA35
AY15	VSS_250	VSS_351	I29
AN15	VSS_251	VSS_352	N28
AD15	VSS_252	VSS_353	N22
AC15	VSS_253	VSS_354	N20
R15	VSS_254	VSS_355	N14
M15	VSS_255	VSS_356	AL13
E15	VSS_256	VSS_357	B10
BD14	VSS_257	VSS_358	AN13
H14	VSS_258		
BL13	VSS_259	VSS_359	M42
BG13	VSS_260	VSS_360	N38
AY13	VSS_261	VSS_361	M39
AN13	VSS_262		
E13	VSS_263		
BD12	VSS_264		
AL12	VSS_265		
H12	VSS_266		
BG11	VSS_267		
AY11	VSS_268		
AN11	VSS_269		
AD11	VSS_270		
AC11	VSS_271		
R11	VSS_272		
M11	VSS_273		
E11	VSS_274		
BD11	VSS_275		
AL11	VSS_276		
H11	VSS_277		
BG10	VSS_278		
AY10	VSS_279		
AN10	VSS_280		
AD10	VSS_281		
AC10	VSS_282		
R10	VSS_283		
M10	VSS_284		
E10	VSS_285		
BD10	VSS_286		
AL10	VSS_287		
H10	VSS_288		
BG9	VSS_289		
AY9	VSS_290		
AN9	VSS_291		
AD9	VSS_292		
AC9	VSS_293		
R9	VSS_294		
M9	VSS_295		
E9	VSS_296		
BD9	VSS_297		
AL9	VSS_298		
H9	VSS_299		

CANTIGA GMCH SFF_FCBGA1363

VSS

VSS

VSS NCTF

VSS SCB

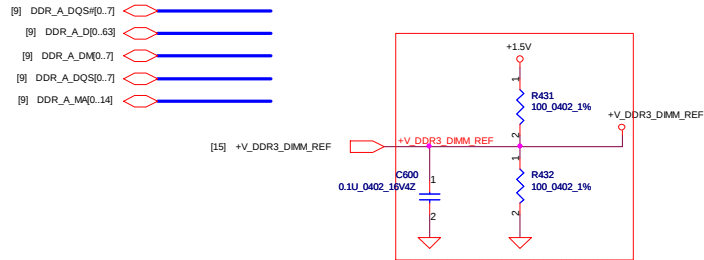
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VSS_NCTF_2
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VSS_NCTF_8
VSS_NCTF_9
VSS_NCTF_10
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VSS_NCTF_23

AJ38
AH38
AO38
AC38
T35
R35
A132
AR32
U32
R32
T28
AR25
T24
R24
AN19
AJ19
AA19
Y19
T19
R19
AN18

VSS_SCB_1
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VSS_SCB_4
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VSS_SCB_6
VSS_SCB_7

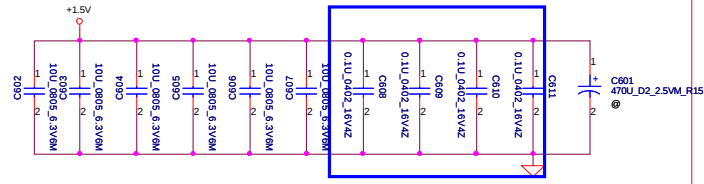
BL55
BL1
A55
D1
B55
B2
A4

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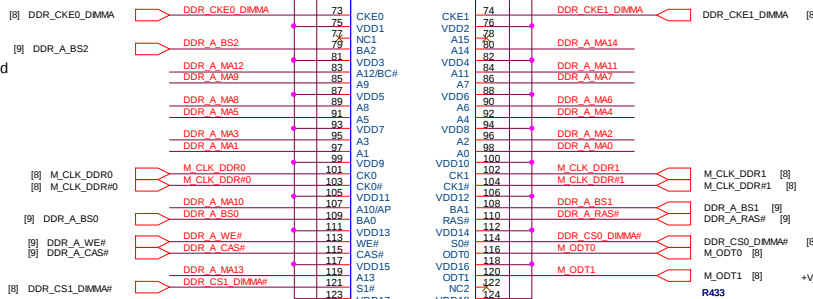
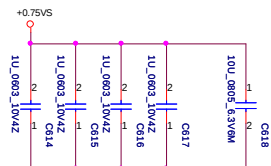


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA

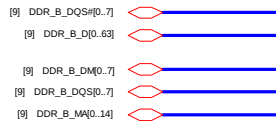


Layout Note:
Place near JP4.203 & JP4.204



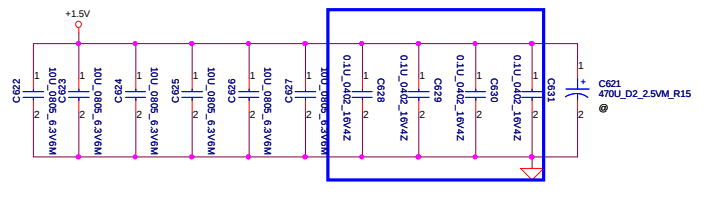
DDR3 SO-DIMM A Standard 4.2mm

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				DDR3-SODIMM SLOT1	
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				Custom	LS-5588
				Rev	0.3
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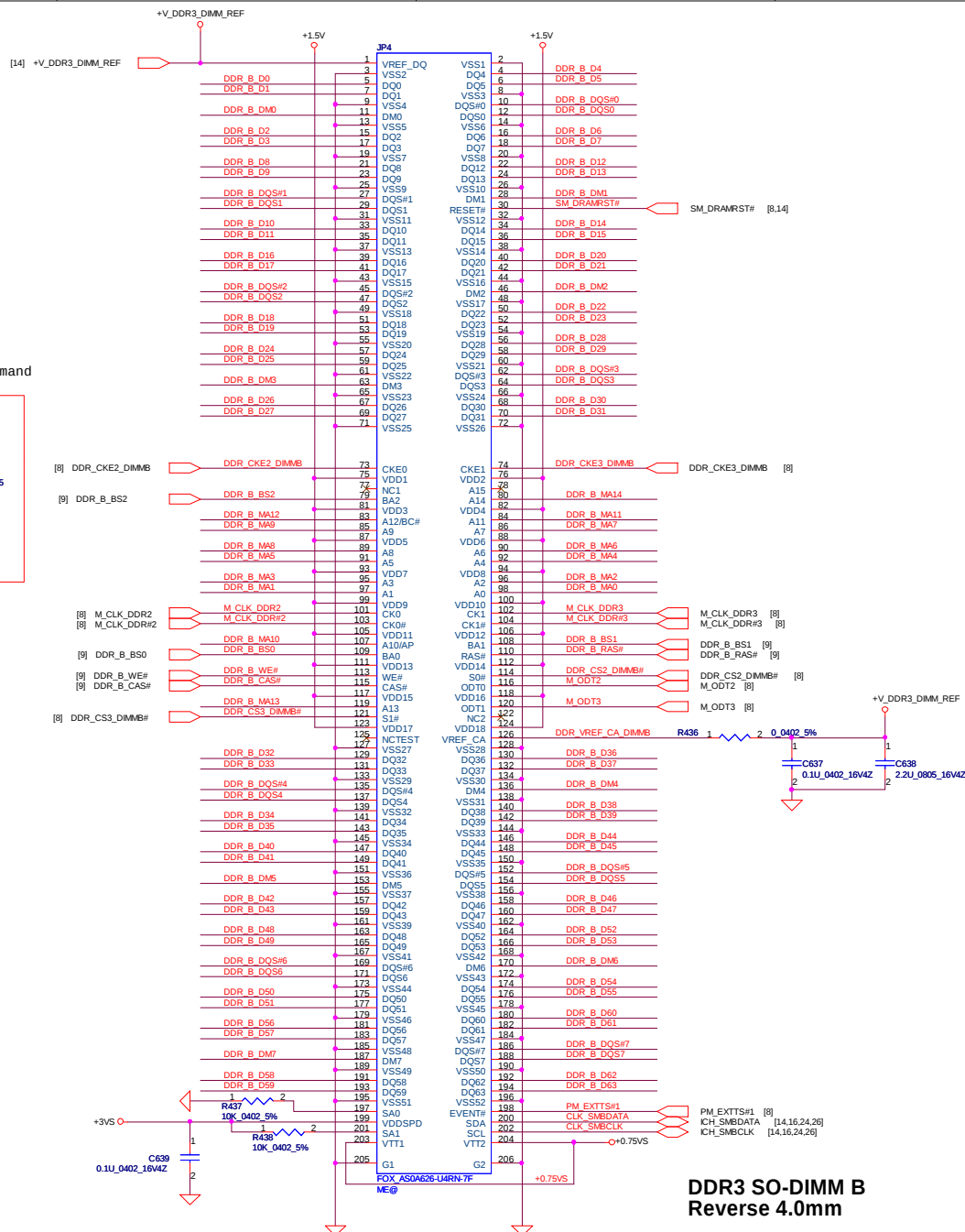
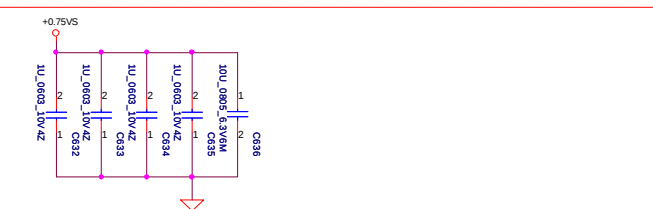


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



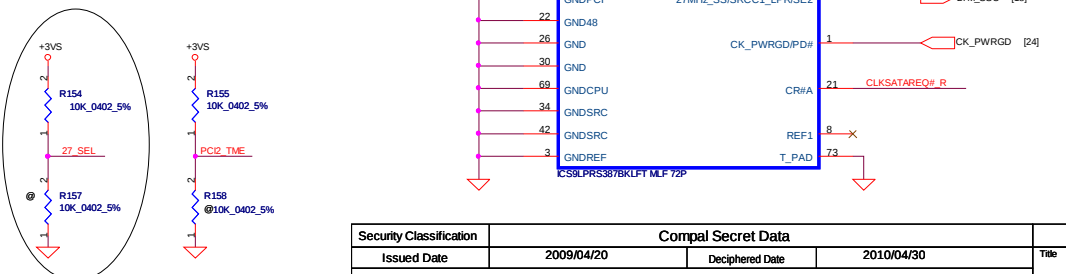
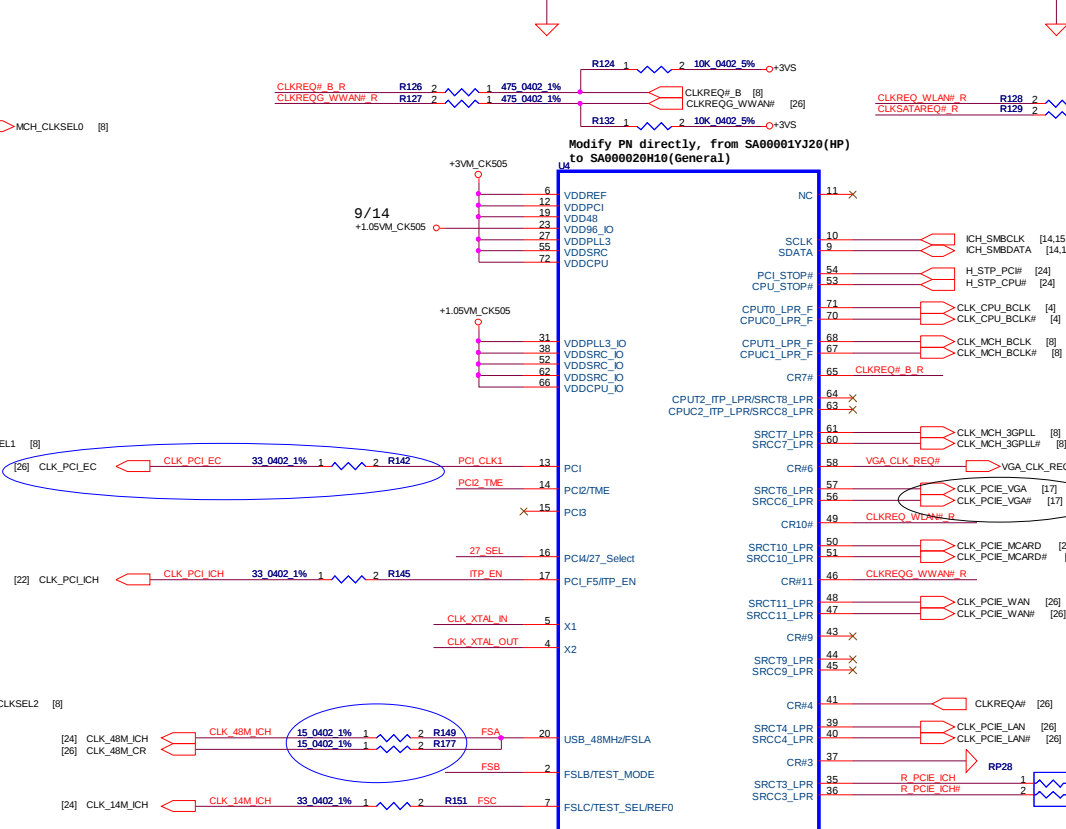
Layout Note:
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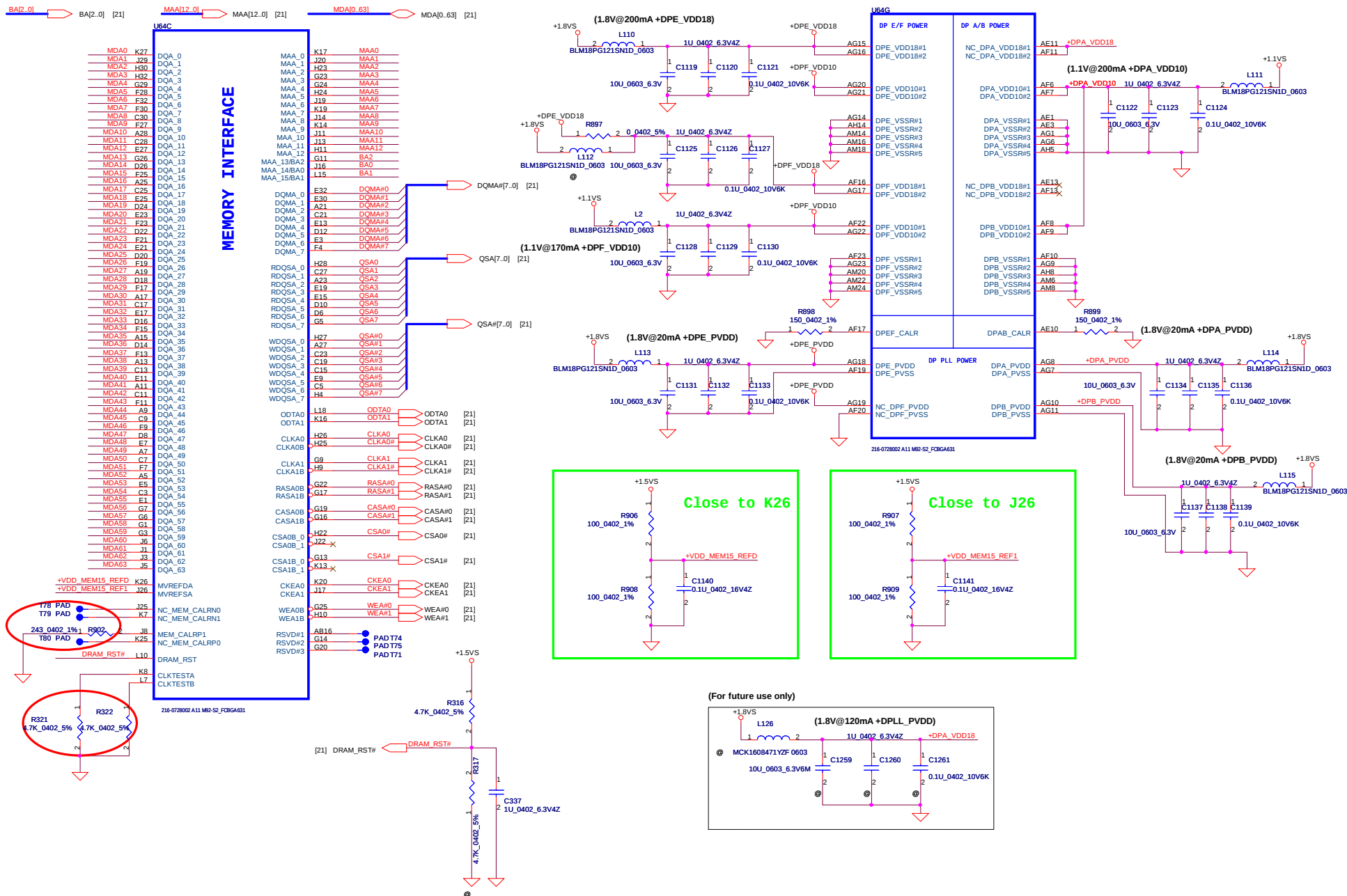
DDR3 SO-DIMM B
Reverse 4.0mm

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Title		DDR3-SODIMM SLOT2			
Size	Document Number	LS-5588			Rev 0.1
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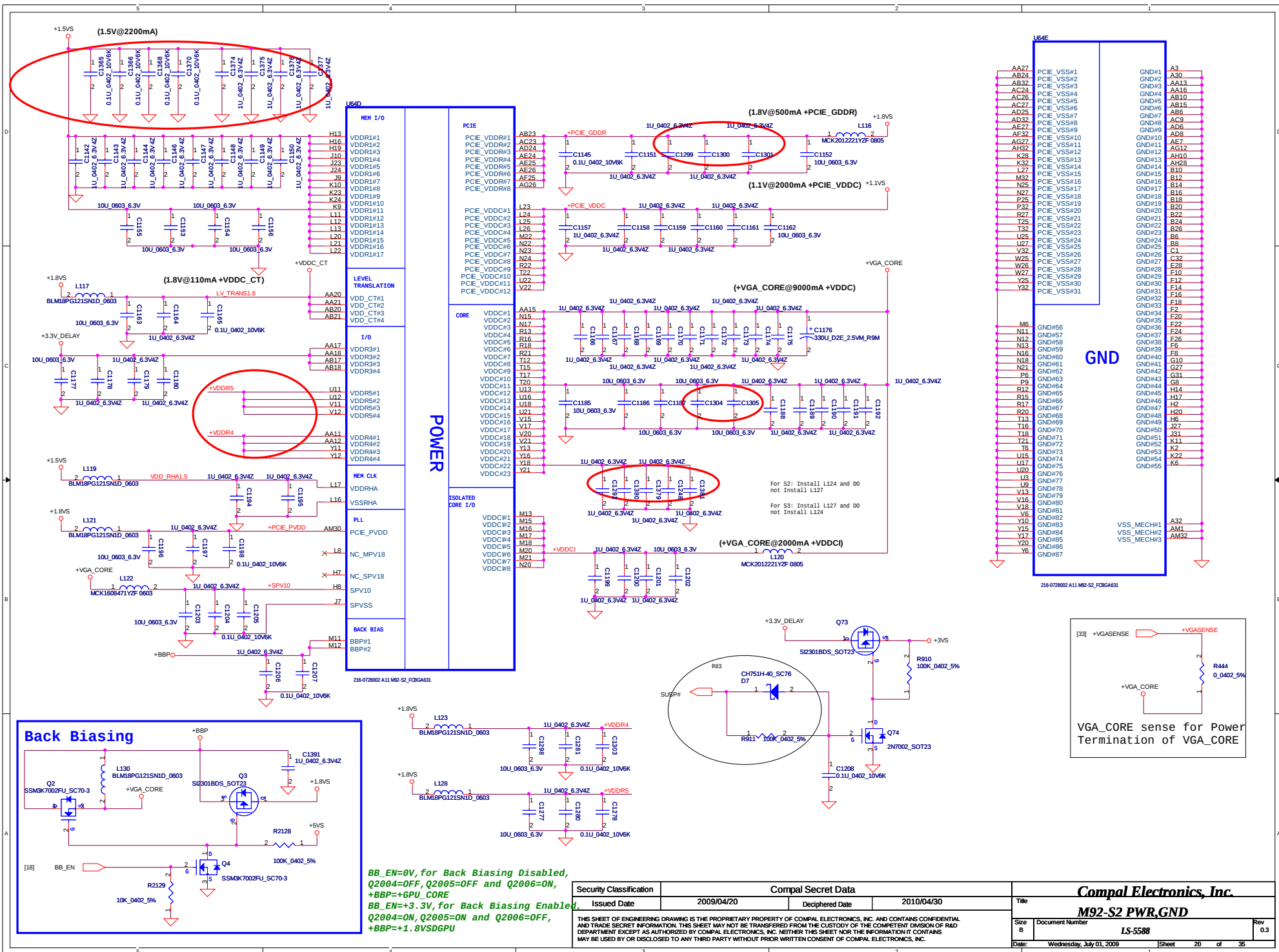
Figure 1 shows two schematic diagrams of 10-bit DACs. Diagram (a) is a 10-bit DAC with inputs +3V5 and +3VM_CK505. It features a ladder network of resistors (R121, R122) and capacitors (C216, C217, C218, C219, C220, C221, C222) connected to a common output node. Diagram (b) is a 10-bit DAC with inputs +VCCP and +1.05VM_CK505. It also features a ladder network of resistors (R122) and capacitors (C223, C224, C225, C226, C227, C228) connected to a common output node.

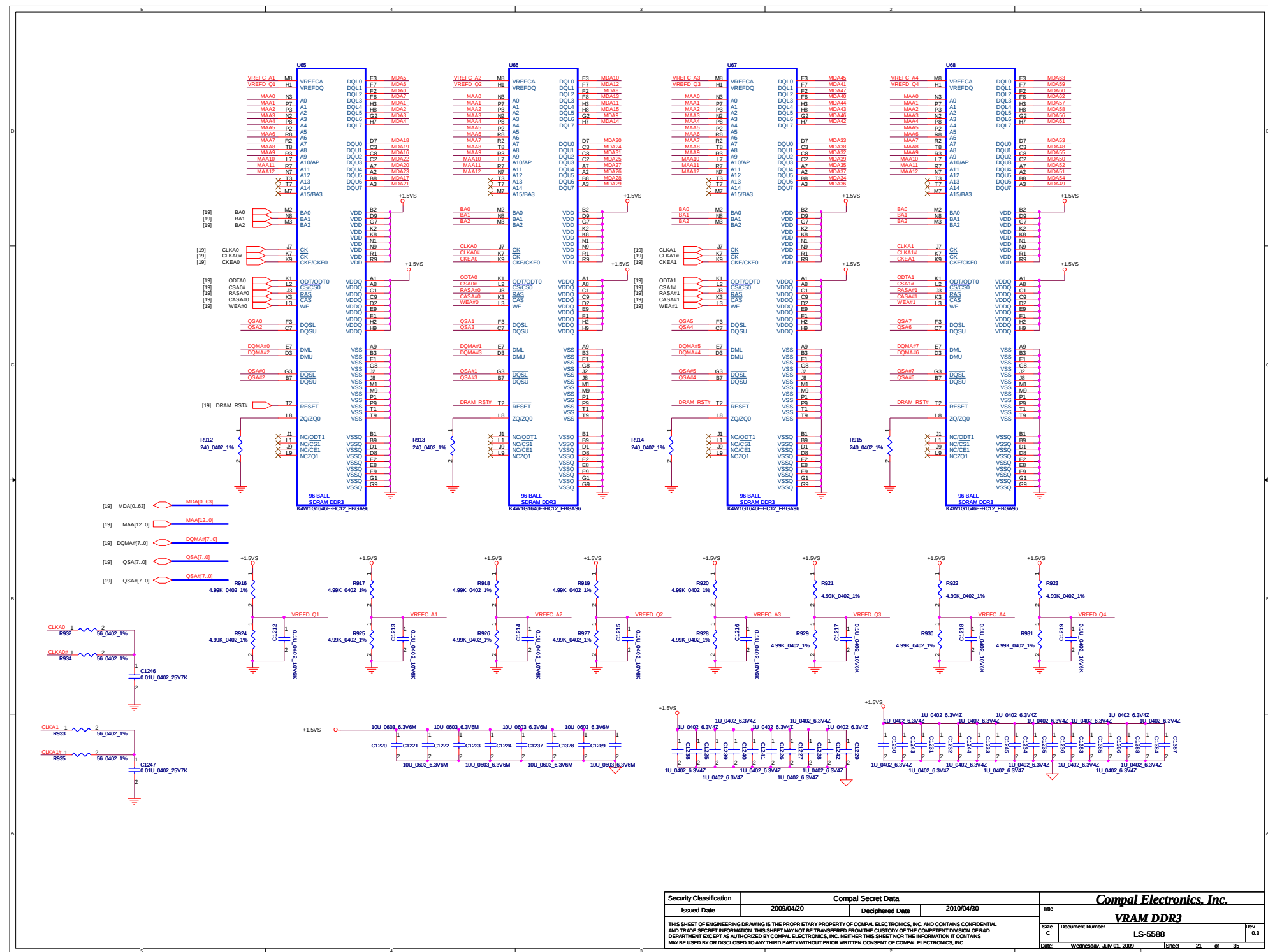


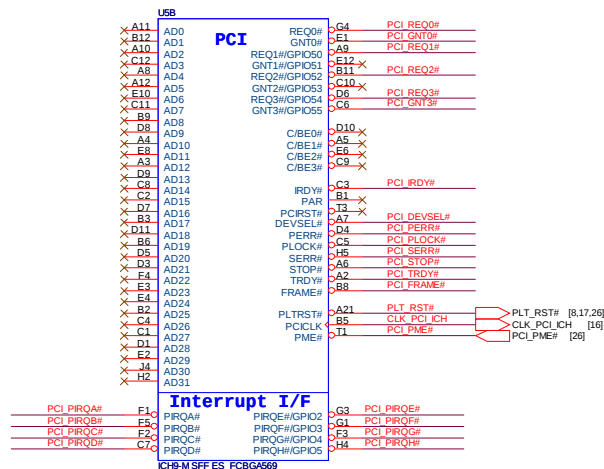
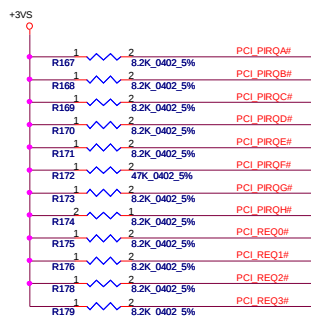
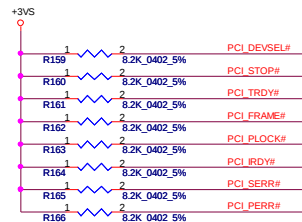
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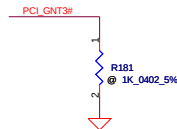
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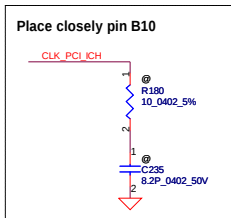
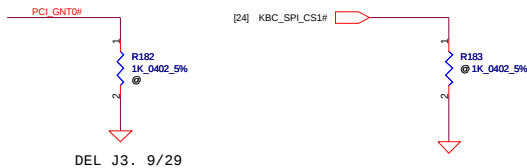




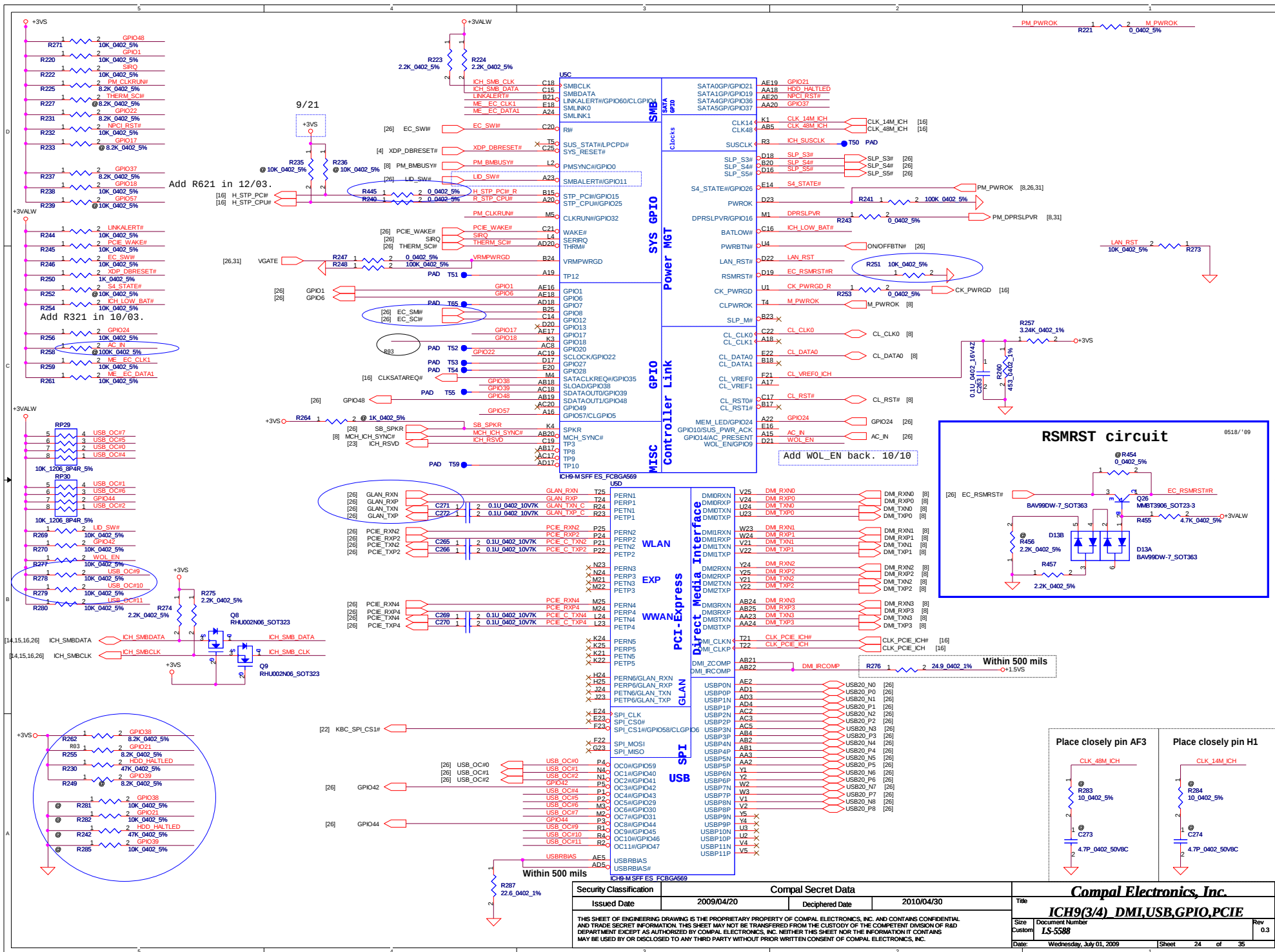
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



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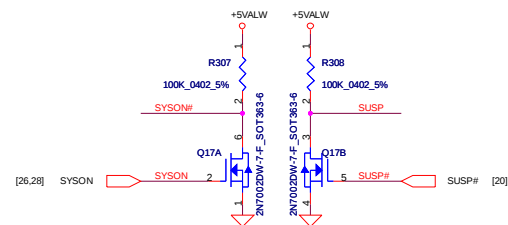
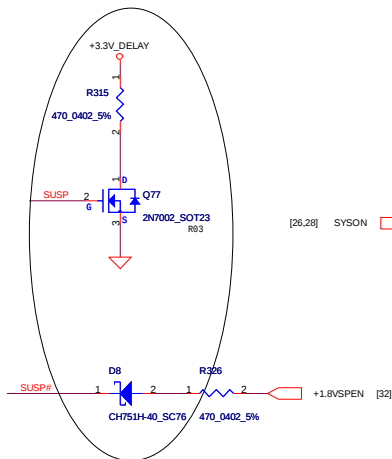
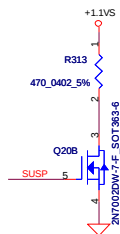
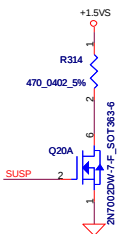
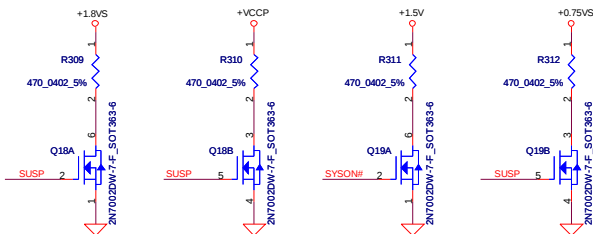
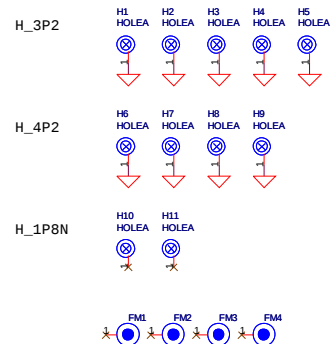
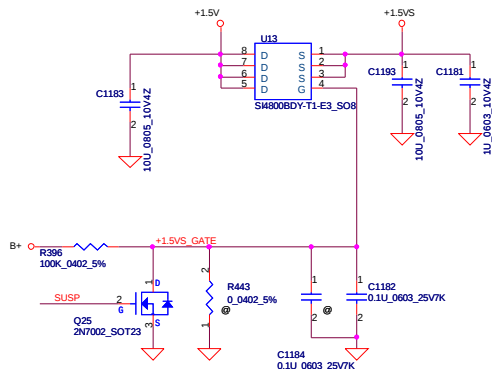
ICH9(3/4)_DMI,USB,GPIO,PCIE

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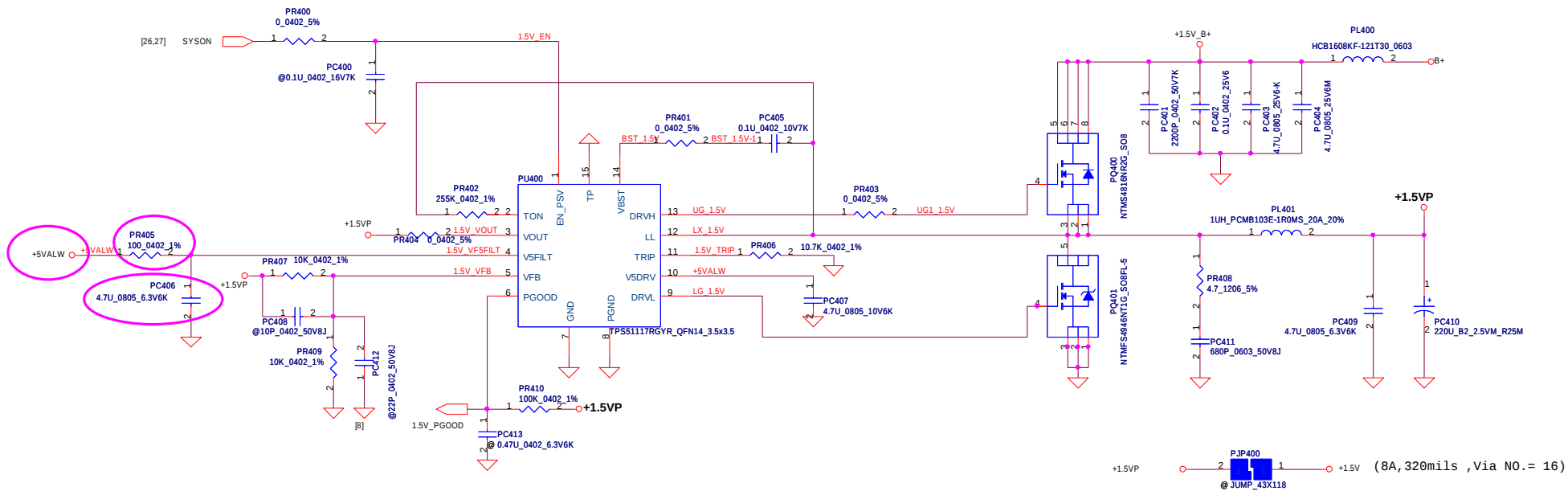


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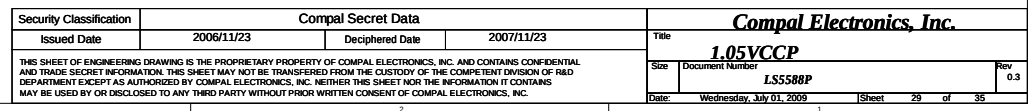
+1.5V to +1.5VS

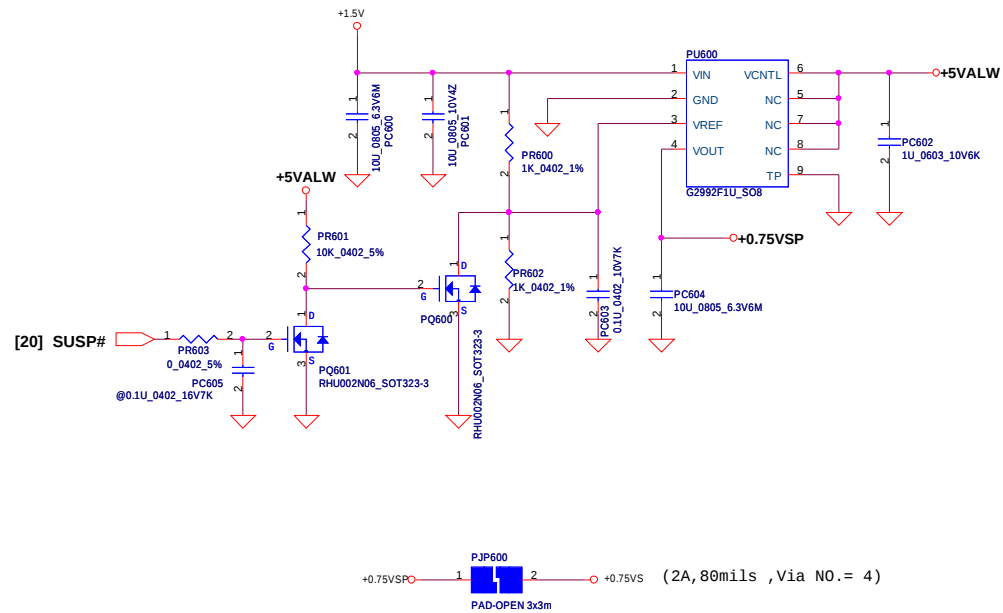


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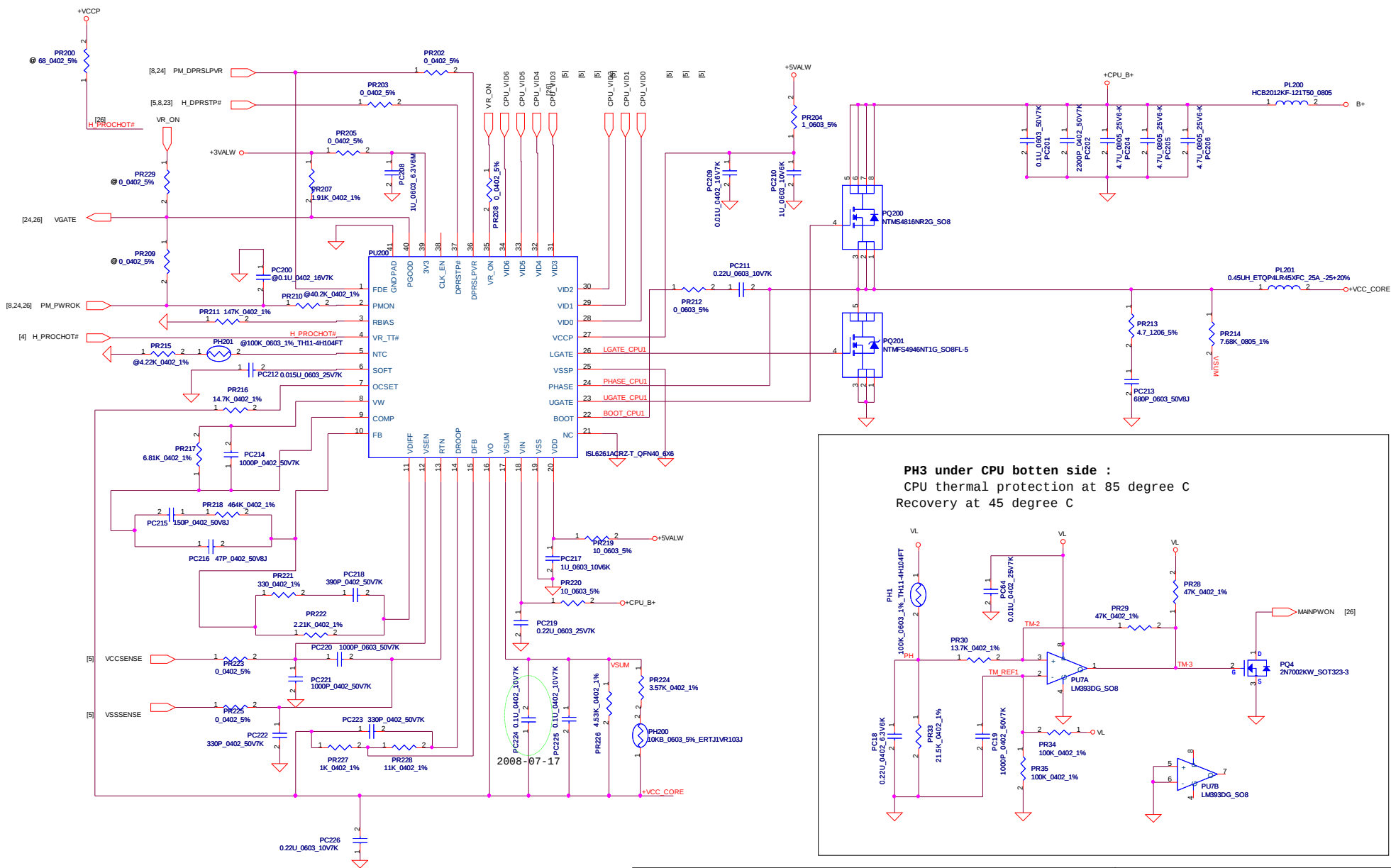


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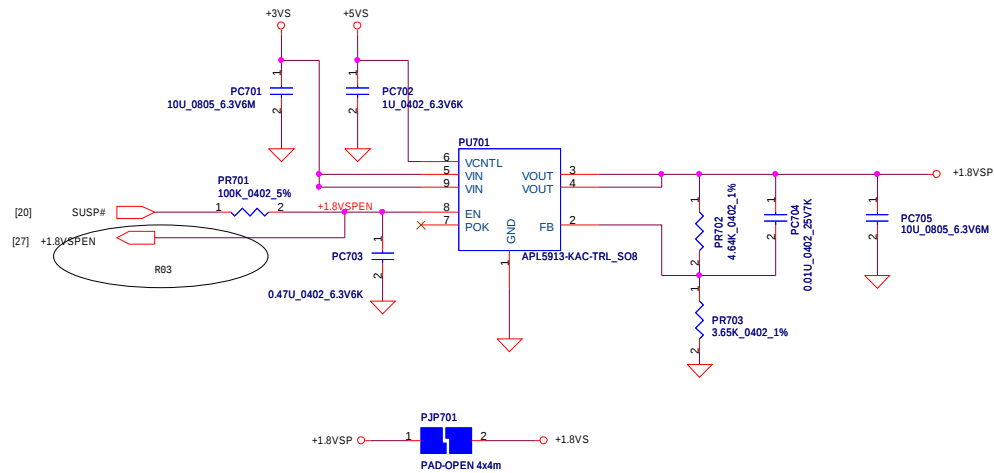




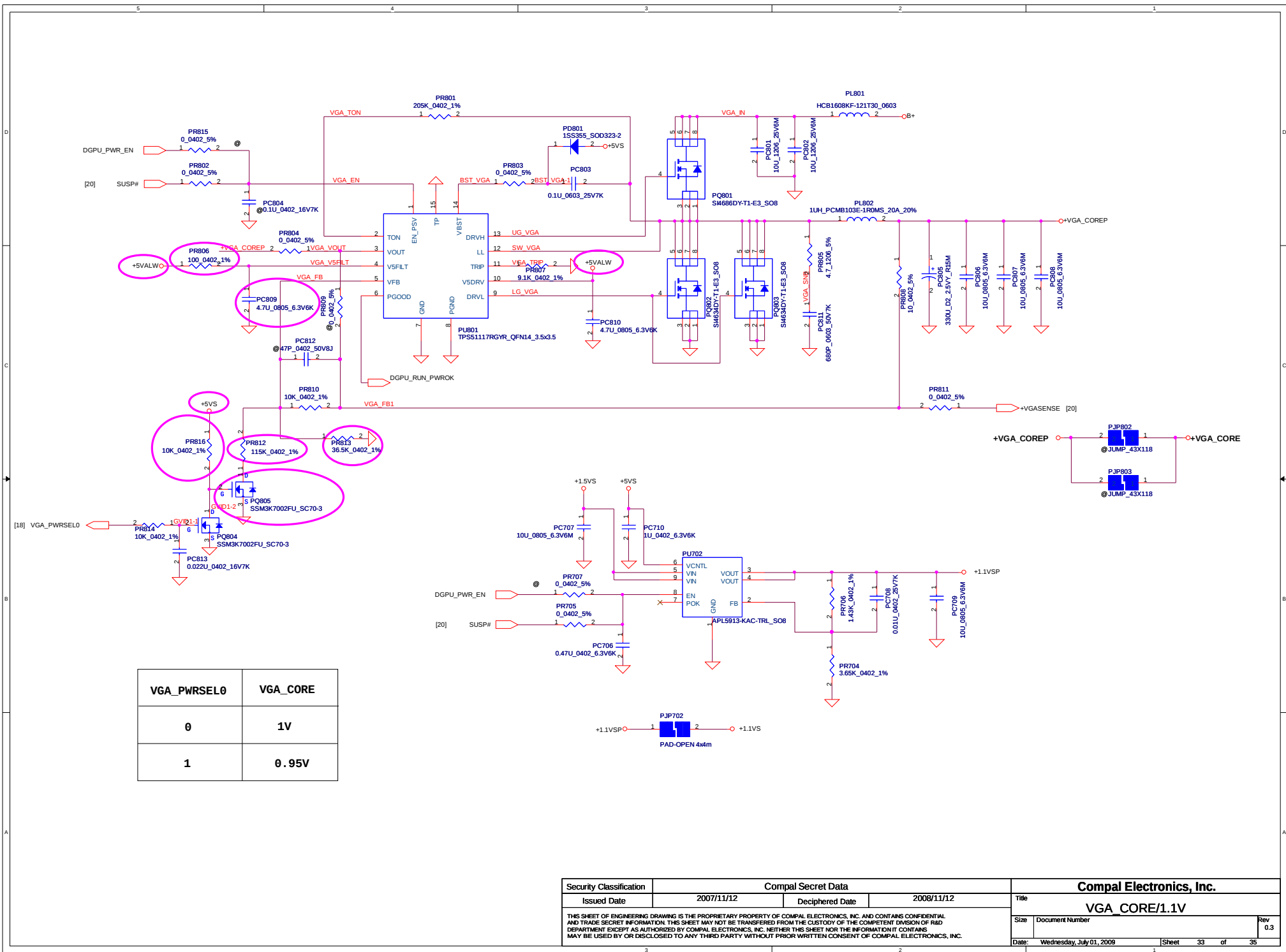
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change OVT Circuit		1.0		add PU7, PH1, PC18, PC19, PC64, PR33, PR30, PR34, PR35, PR29, PR28, PQ4		
2							
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