MODEL NAME : *Viking 18*

PCB NO : *LA-9332P*

BOM P/N : *4619KU31L01*

Compal Confidential

Viking 18

Schematic Document

Rev: X02

2012-11-19

@ : Nopop Component

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Title: *Cover Sheet*

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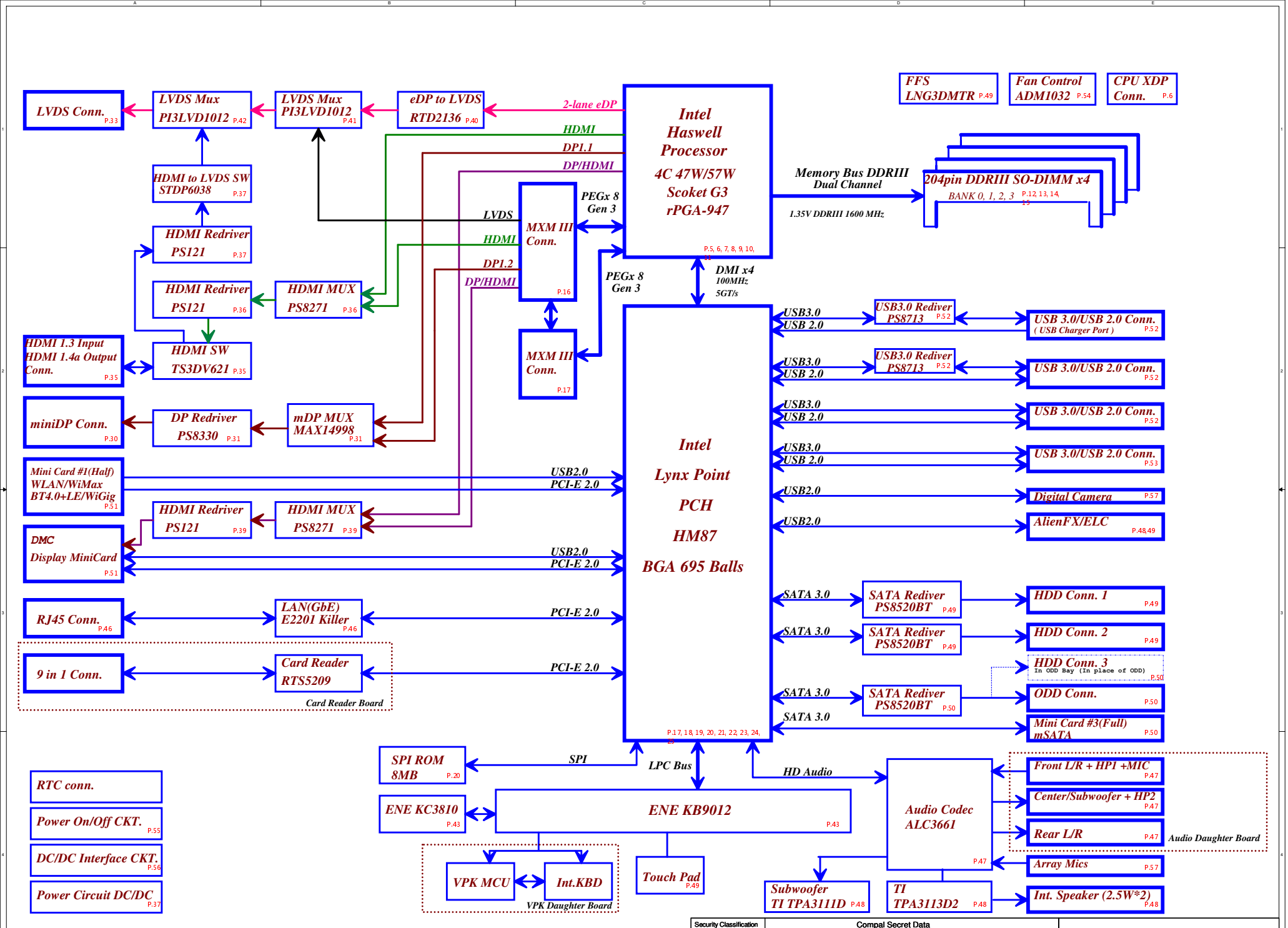

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Title: **Block Diagram**

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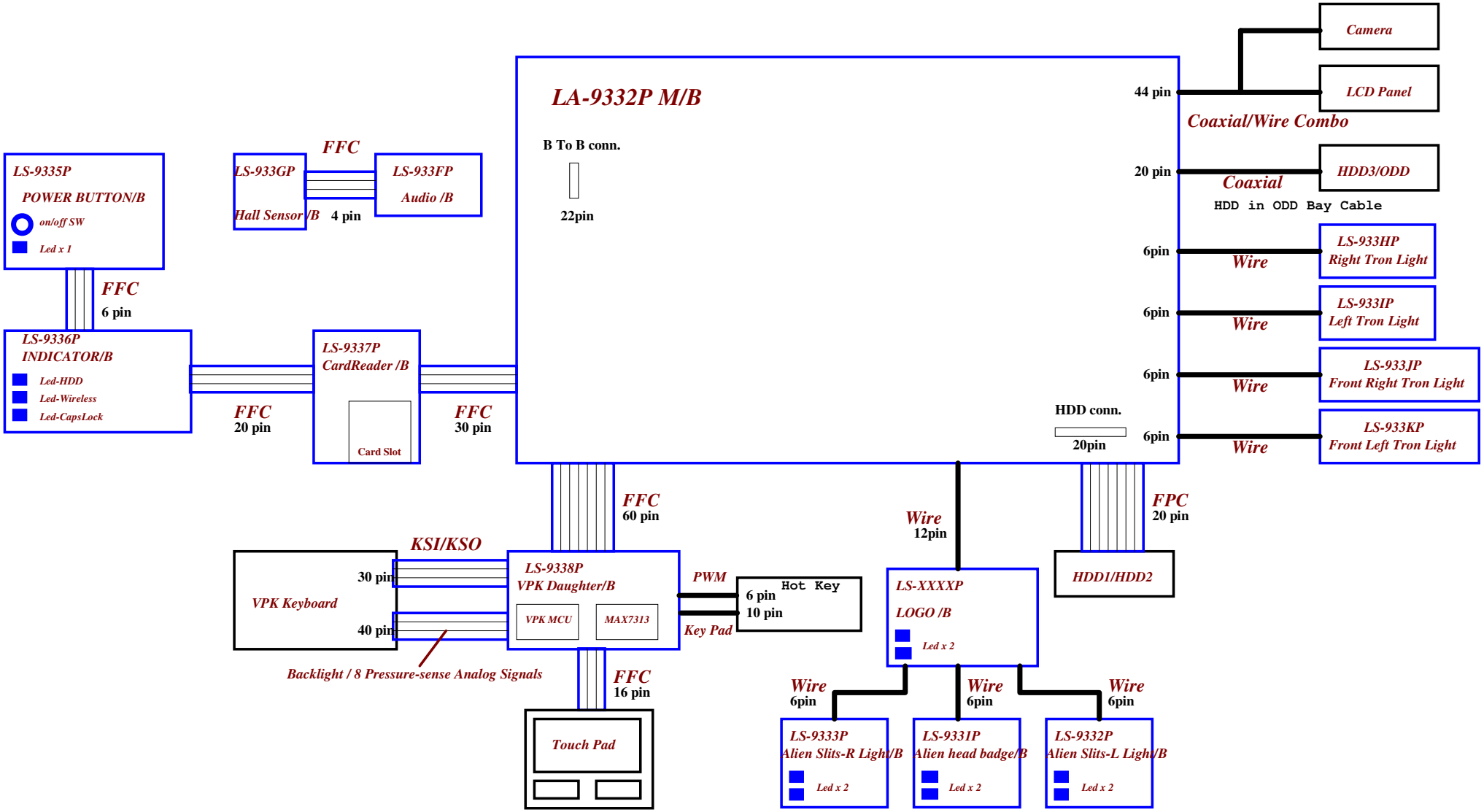
Project Code : VAS10

File Name : LA-9332P



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Title: **Block Diagram**

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (QT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connetion
1	JUSB1 (Right side)
2	JUSB2 (Right side)
3	NA
4	NA
5	JUSB3 (Left side)
6	JUSB4 (Left side)

	USB PORT#	DESTINATION
USB2.0	0	JUSB1(USB3.0 P1)
	1	JUSB2(USB3.0 P2)
	2	JUSB3(USB3.0 P5)
	3	JUSB4(USB3.0 P6)
	4	JMINI1 (WLAN)
	5	JMINI2 (DMC)
	6	AlienFX/ELC
	7	None
	8	None
	9	None
	10	None
	11	None
	12	LVDS CAMERA
	13	VPK K/B

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Symbol Note :

: means Digital Ground

: means Analog Ground

PM TABLE

State \ power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	MXM		

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SMBUS Control Table

	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V		V		
EC_SMB_CK2 EC_SMB_DA2	KB9012					V	V	V		V	V					
PCH_SML0CLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		V		V				V				V		V	V

Link

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Title: Notes List

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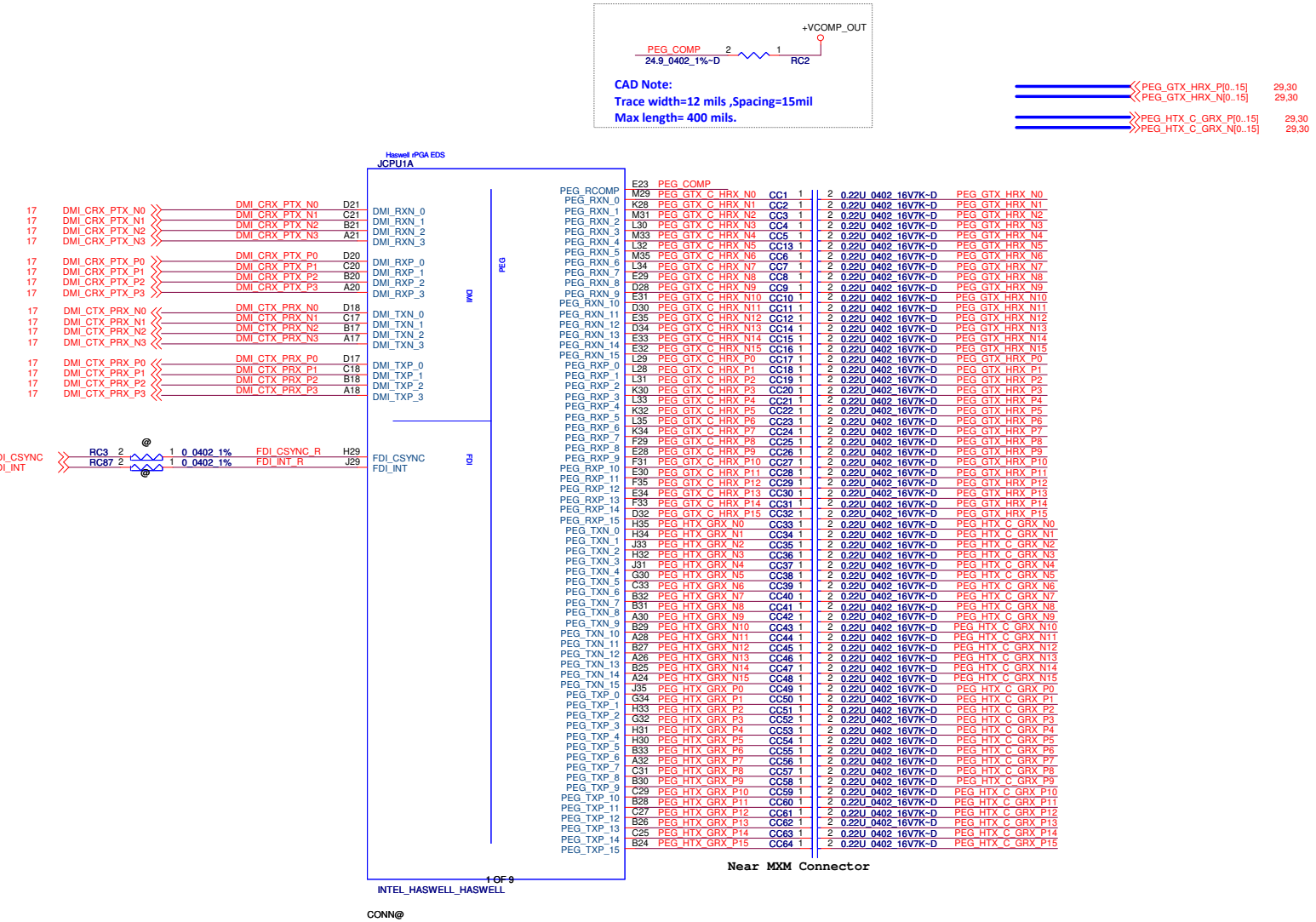
Date: Friday, December 14, 2012 | Sheet 4 of 56



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Compal Electronics, Inc.

Title: CPU (1/7) DMI,PEG

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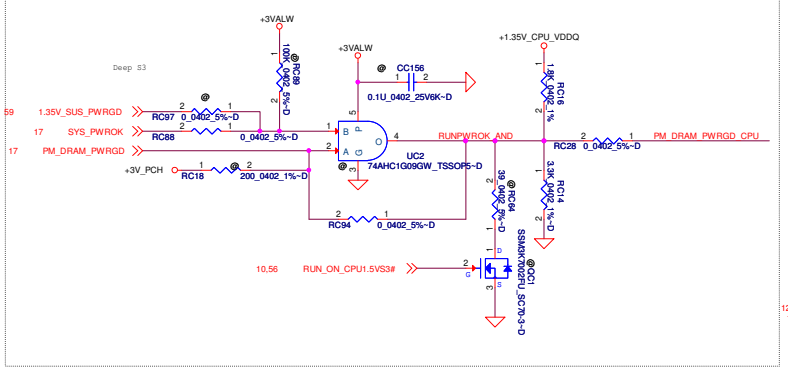
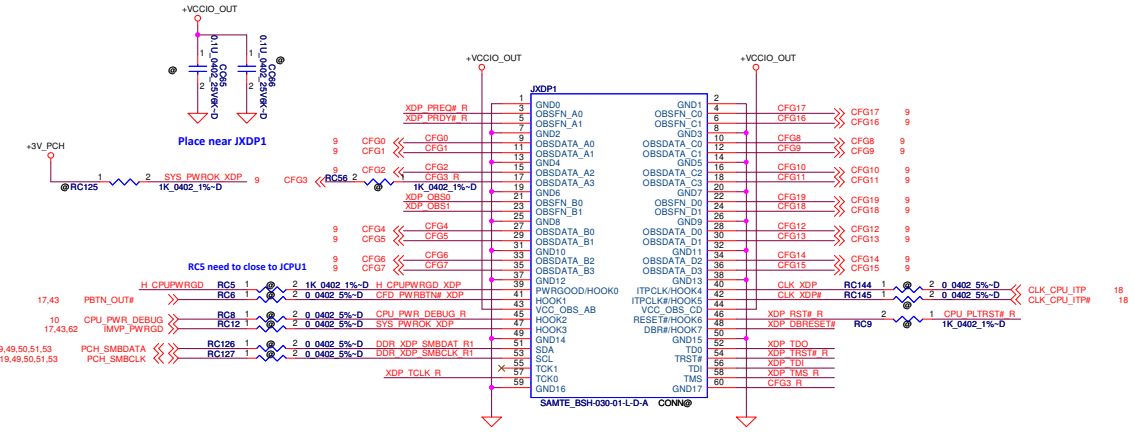
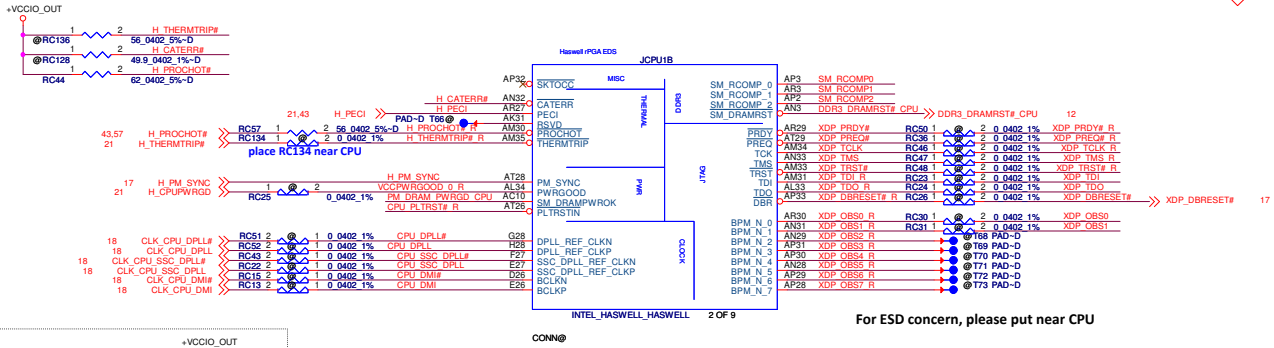
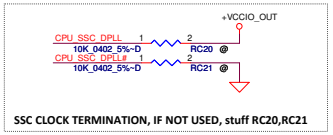
SM_DRAMPWROK with DDR Power Gating Topology

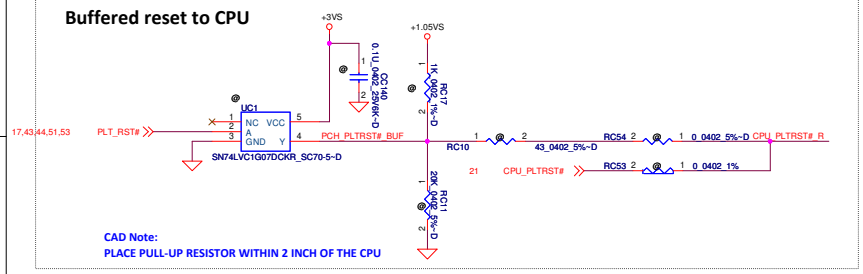


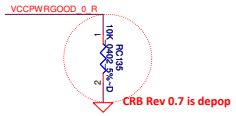






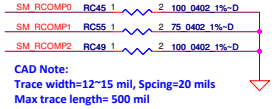
Buffered reset to CPU





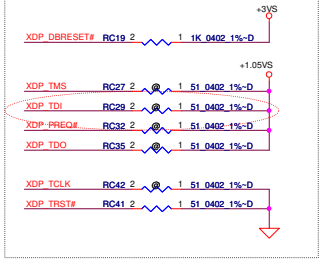
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

DDR3 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

PU/PD for JTAG signals



CRB Rev 0.7 no pull up

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Compal Electronics, Inc.

Title: CPU (2/7) PM,XDP,CLK

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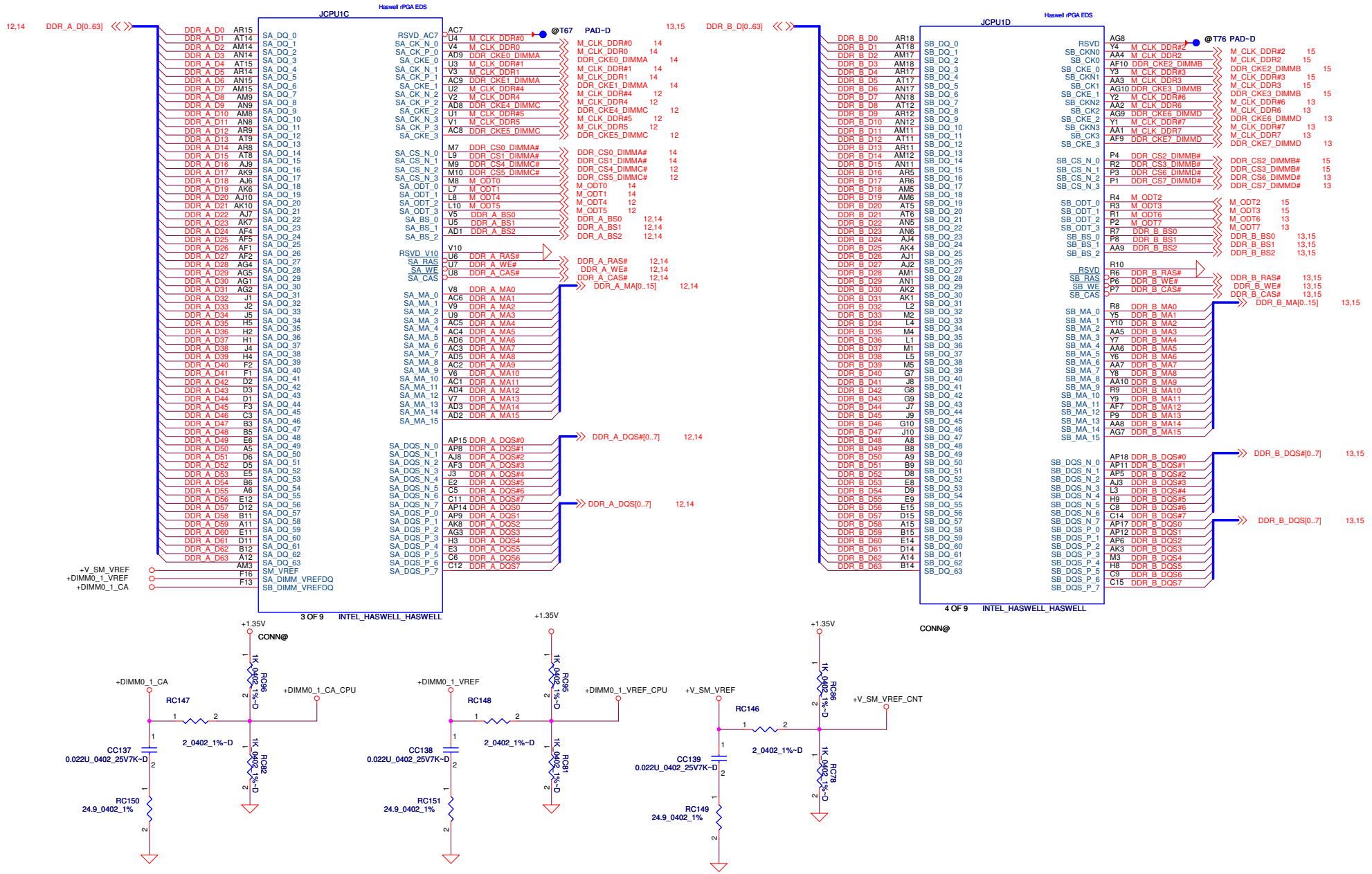
Date: Friday, December 14, 2012 | Sheet 6 of 56



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Compal Electronics, Inc.

Title: **CPU (3/7) DDRIII**

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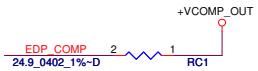
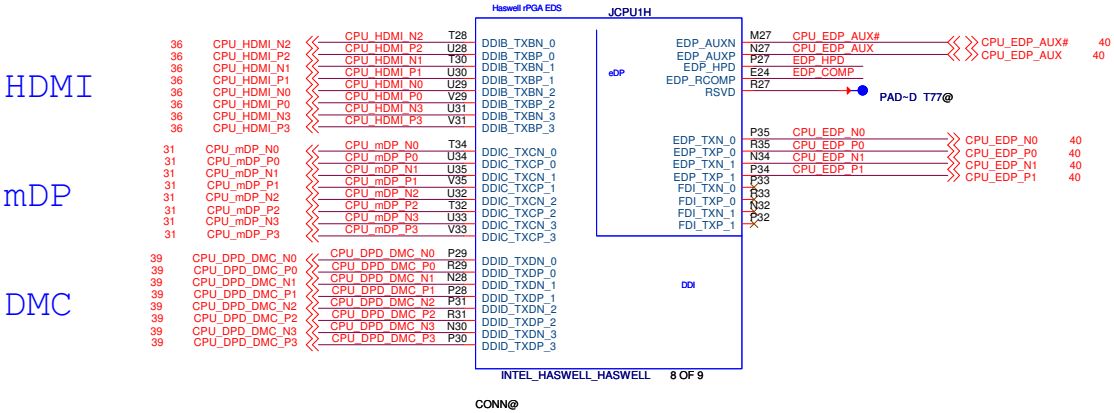
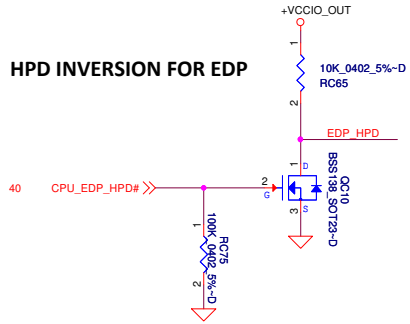
COMPENSATION PU FOR eDP



CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.



HPD INVERSION FOR EDP



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Compal Electronics, Inc.

Title: CPU (4/7) FDI,eDP,DDI

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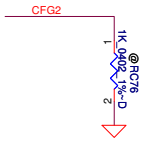
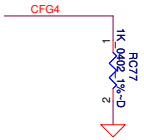
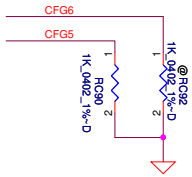
CFG STRAPS for CPU



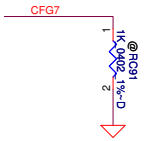
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



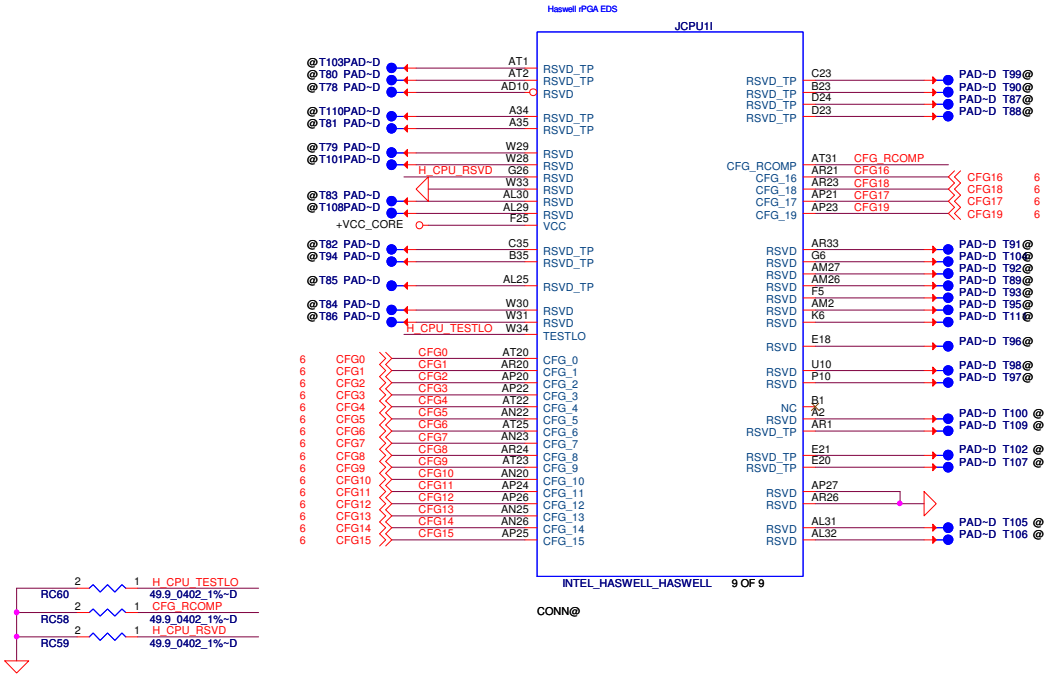
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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Title: CPU (5/7) RSVD,CFG

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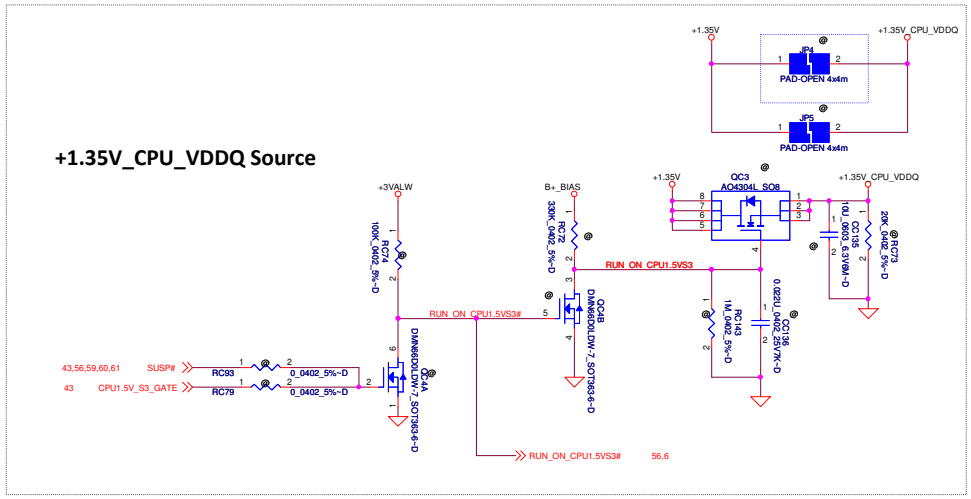

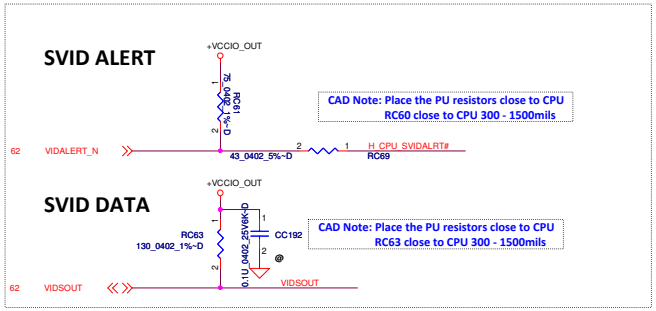

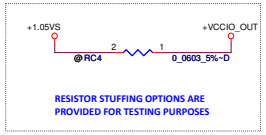

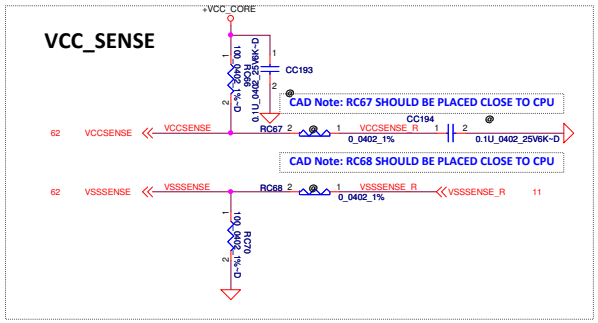

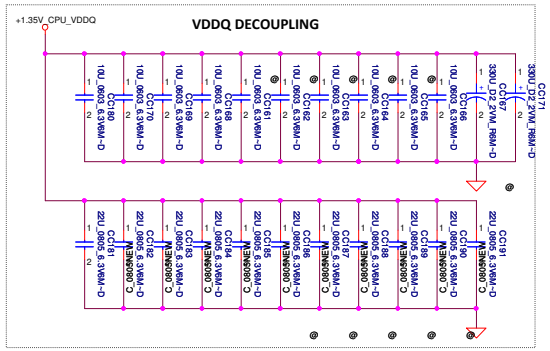

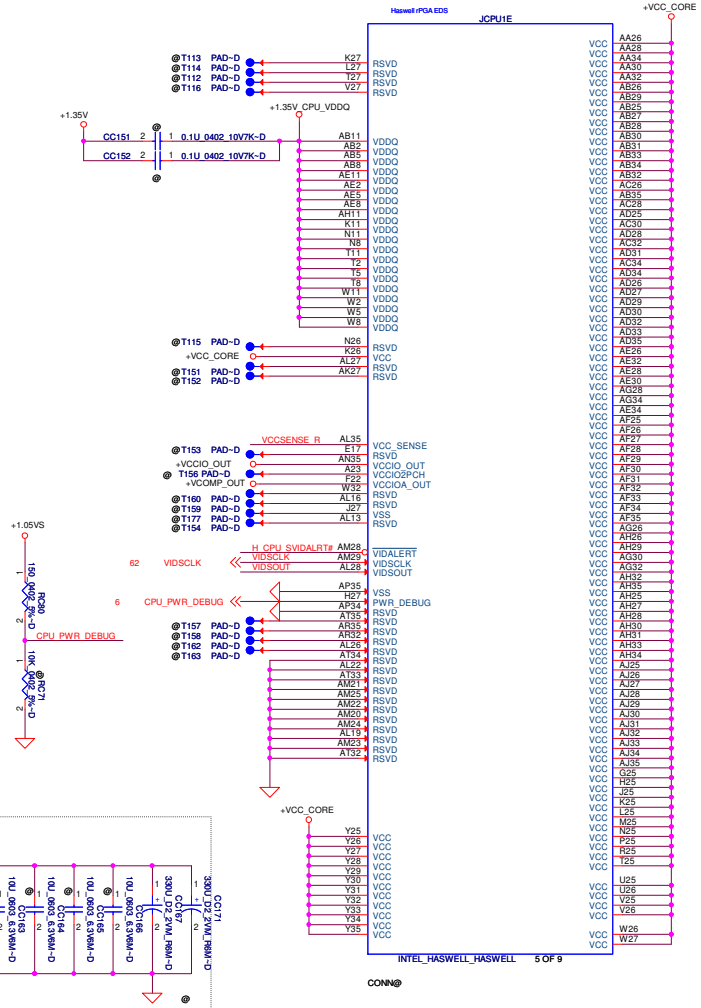

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Compal Electronics, Inc.

Title: CPU (6/7) PWR

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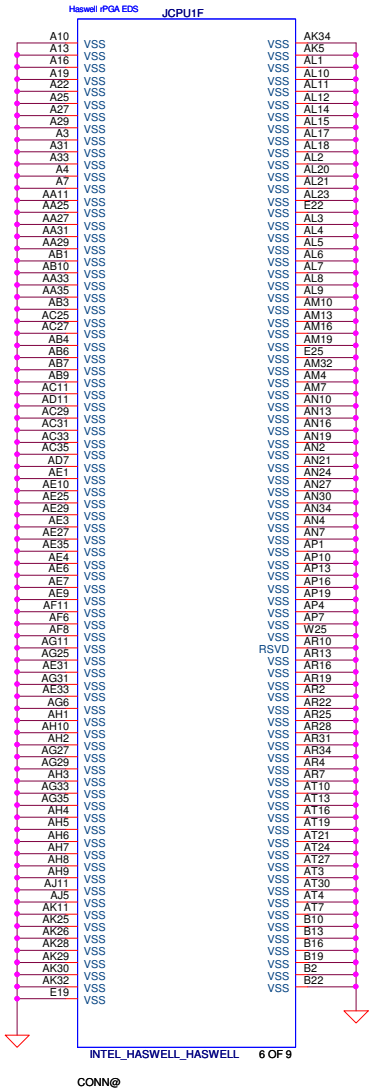

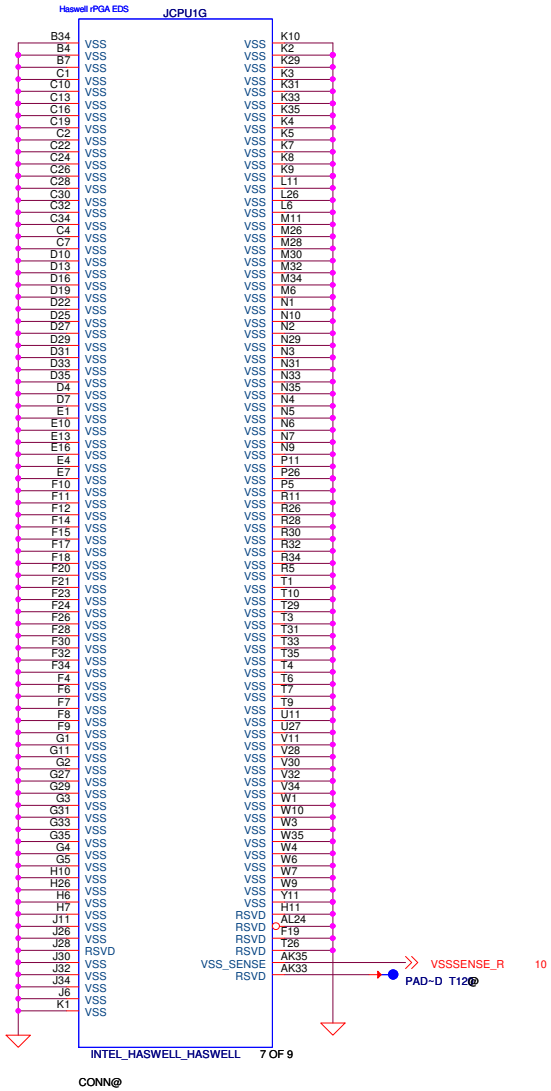

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Compal Electronics, Inc.

Title: **CPU (7/7) VSS**

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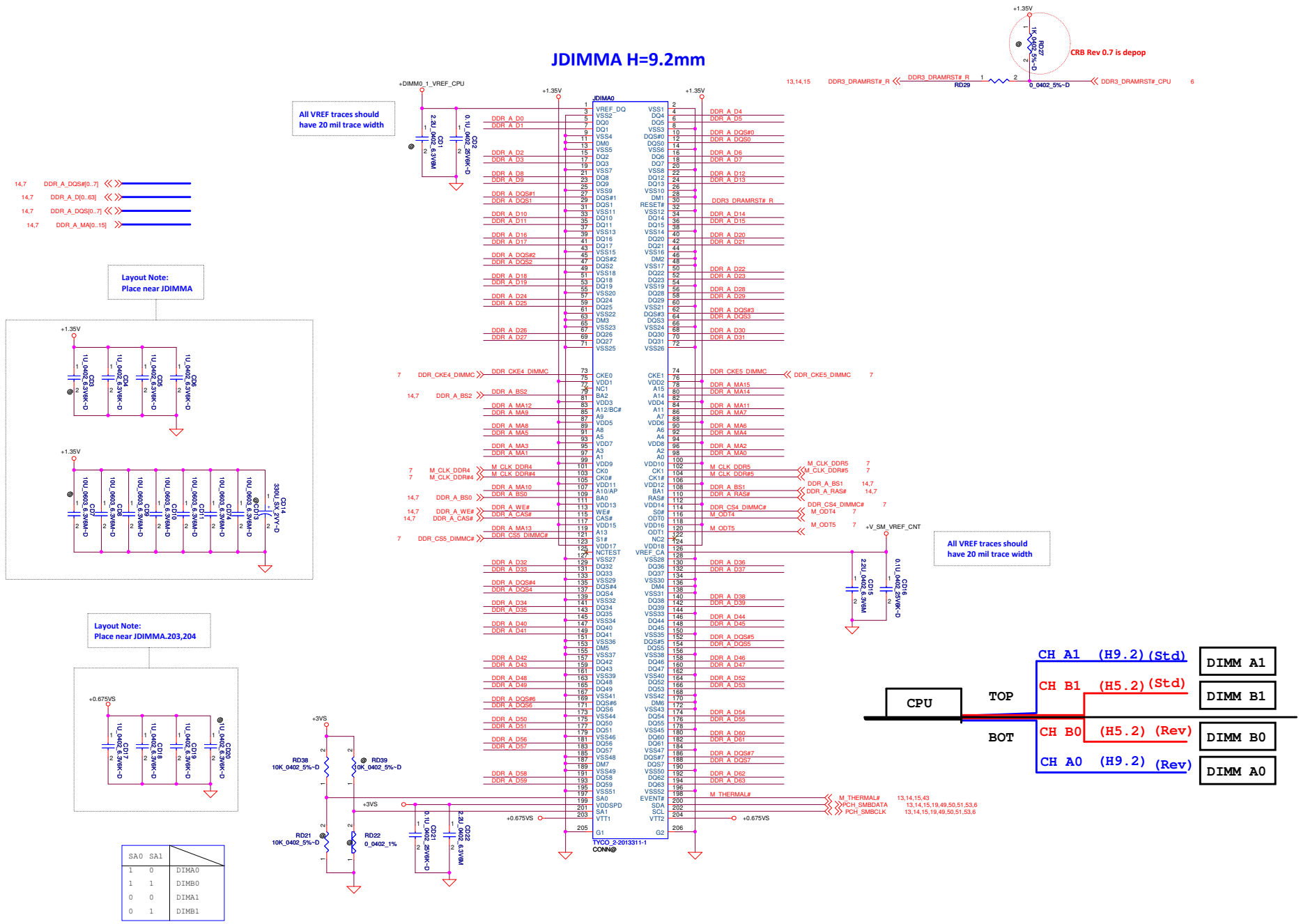
Date: Friday, December 14, 2012 | Sheet 11 of 56

JDIMMA H=9.2mm



SA0	SA1	
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1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

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Issued Date	2012/05/28	Deciphered Date	2013/05/27

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Compal Electronics, Inc.

Title: **DDRIII DIMMA**

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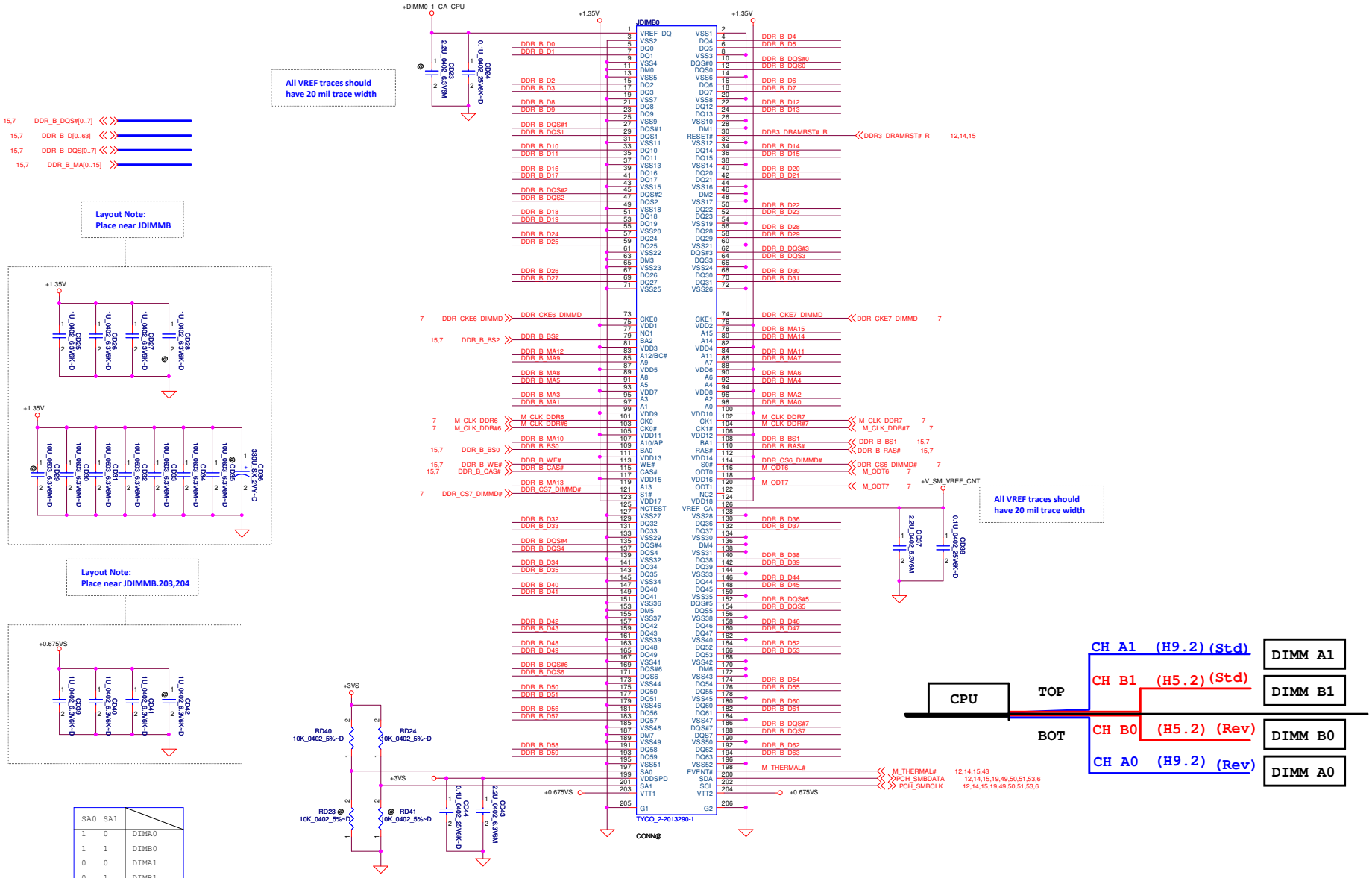
JDIMMB H=5.2mm



SA0	SA1	
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1	1	DIMB0
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0	1	DIMB1

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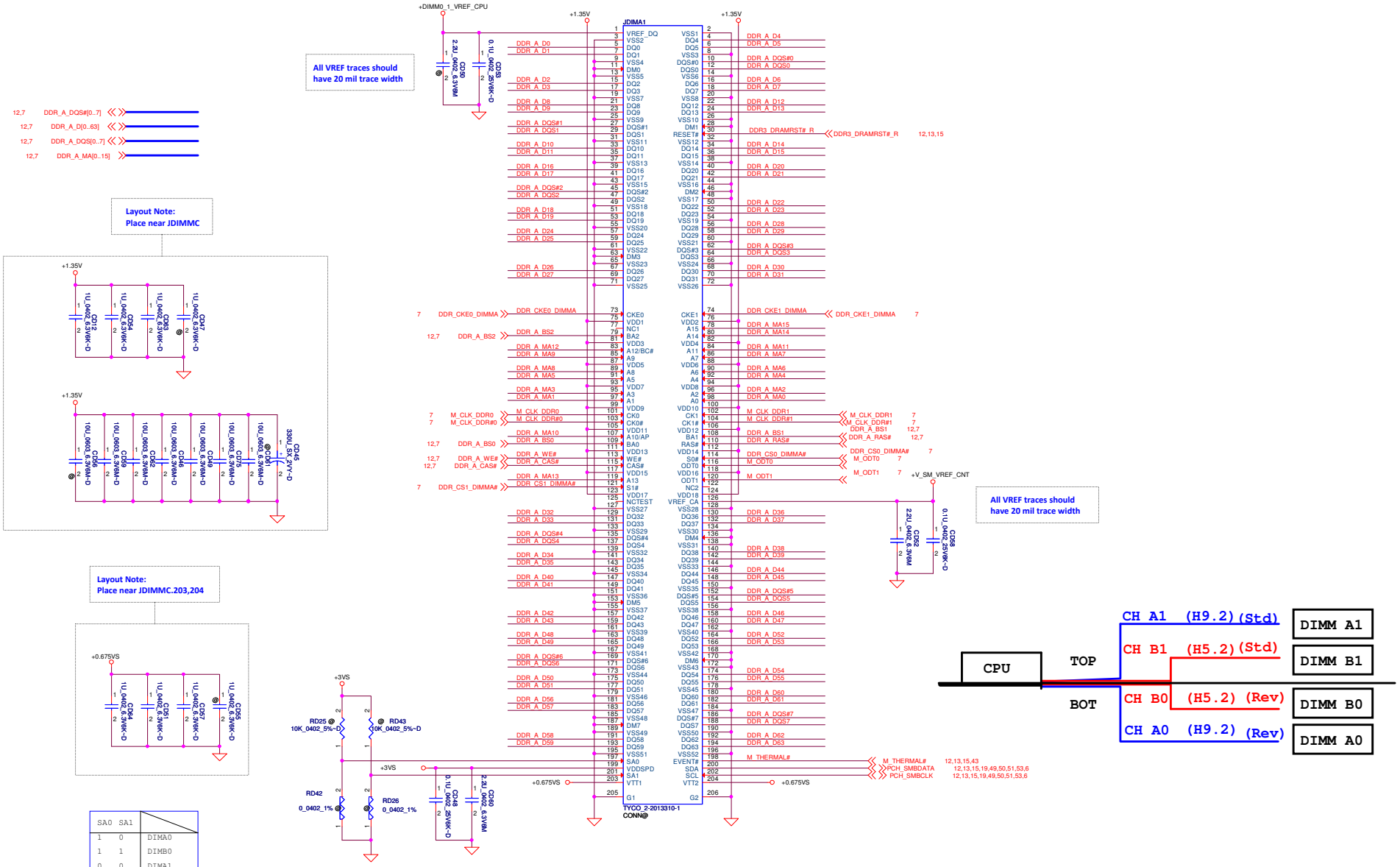
Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 13 of 56

JDIMMC H=9.2mm



SA0	SA1	
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1	1	DIMB0
0	0	DIMA1
0	1	DIMB1

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Compal Electronics, Inc.

Title: DDRIII DIMMC

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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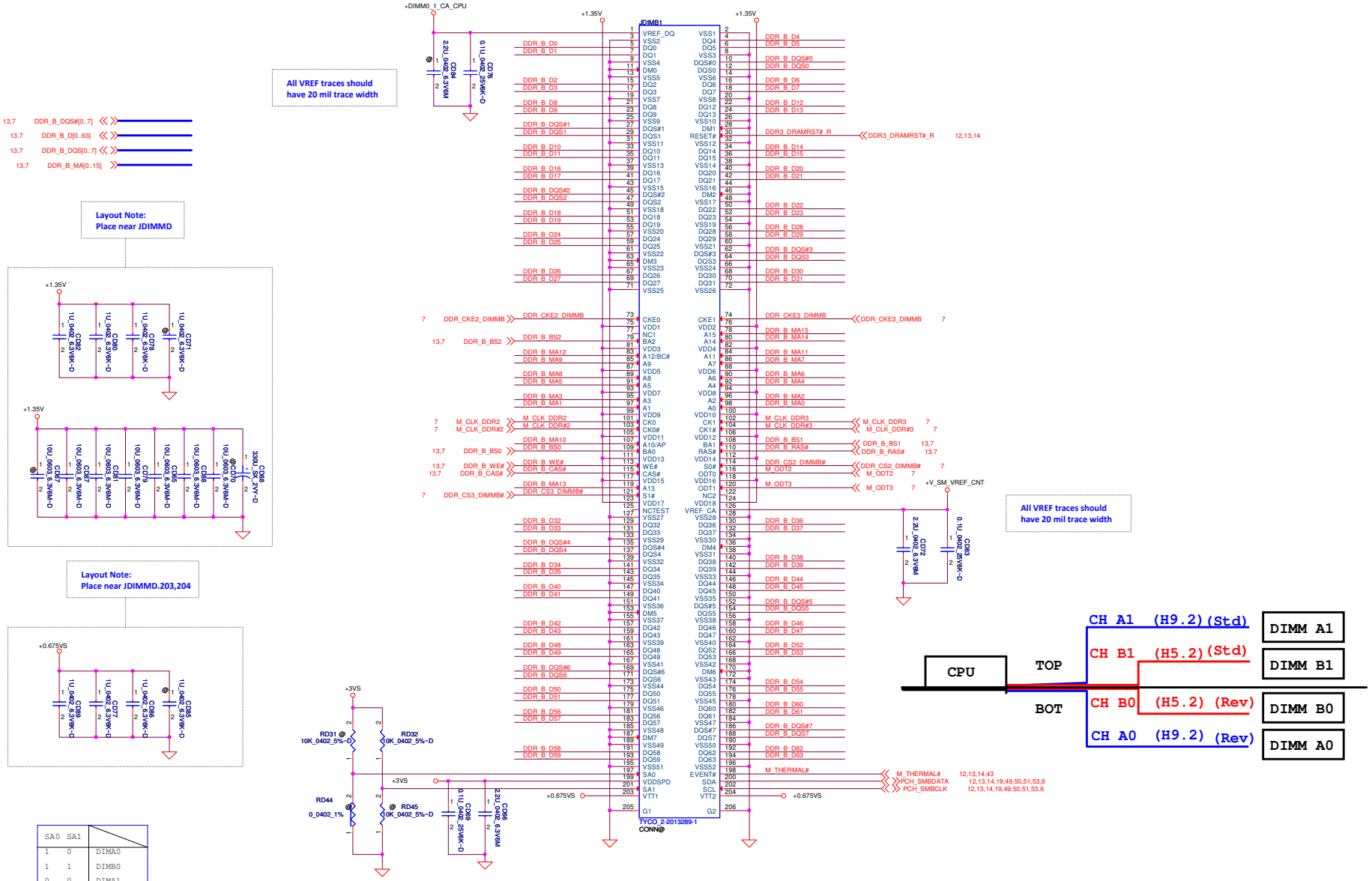
JDIMMD H=5.2mm



SA0	SA1	
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1	1	DIMB0
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Compal Electronics, Inc.

Title: DDRIII DIMMD

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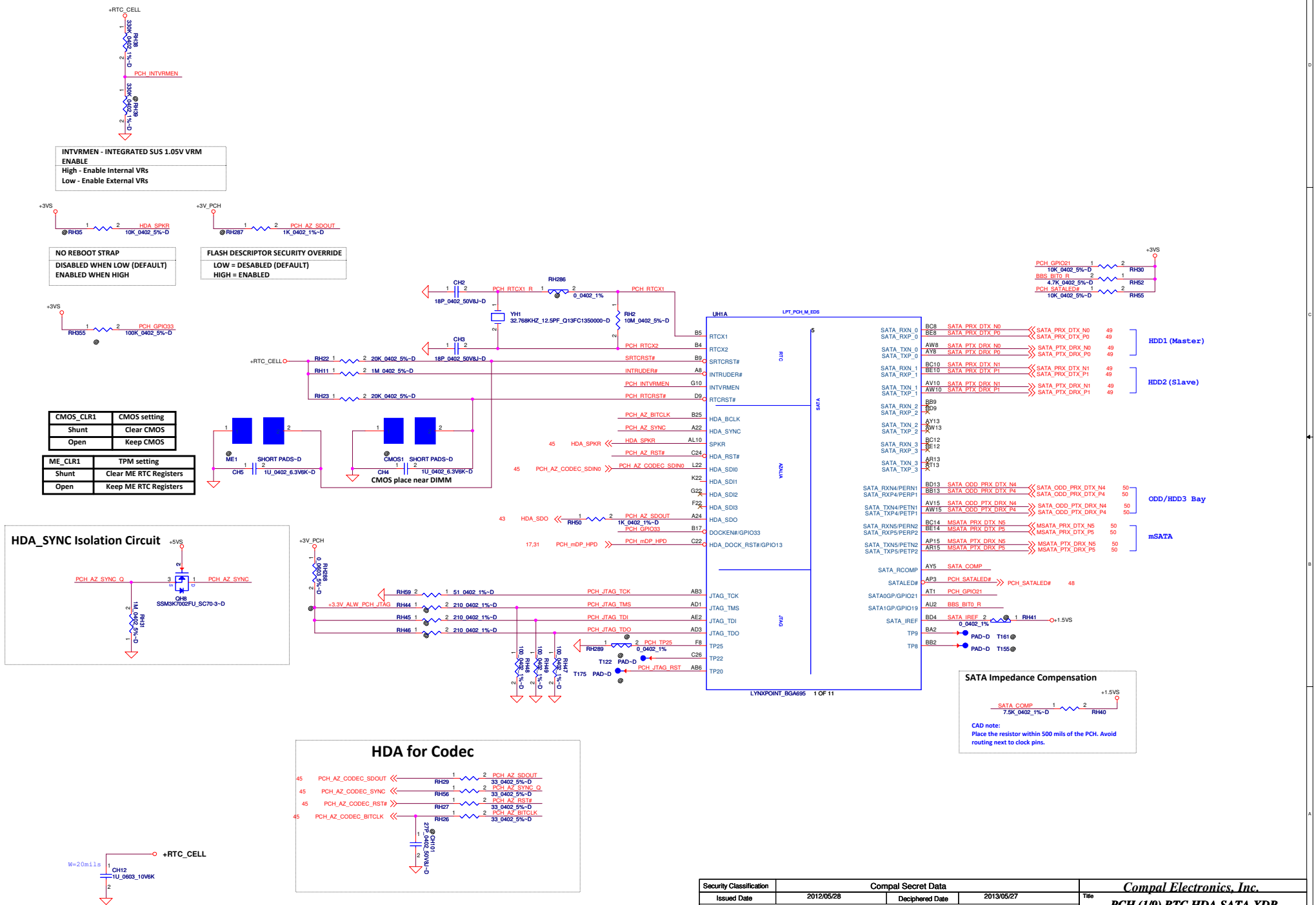
Date: Friday, December 14, 2012 | Sheet 15 of 56



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Compal Electronics, Inc.

Title: PCH (1/9) RTC,HDA,SATA,XDP

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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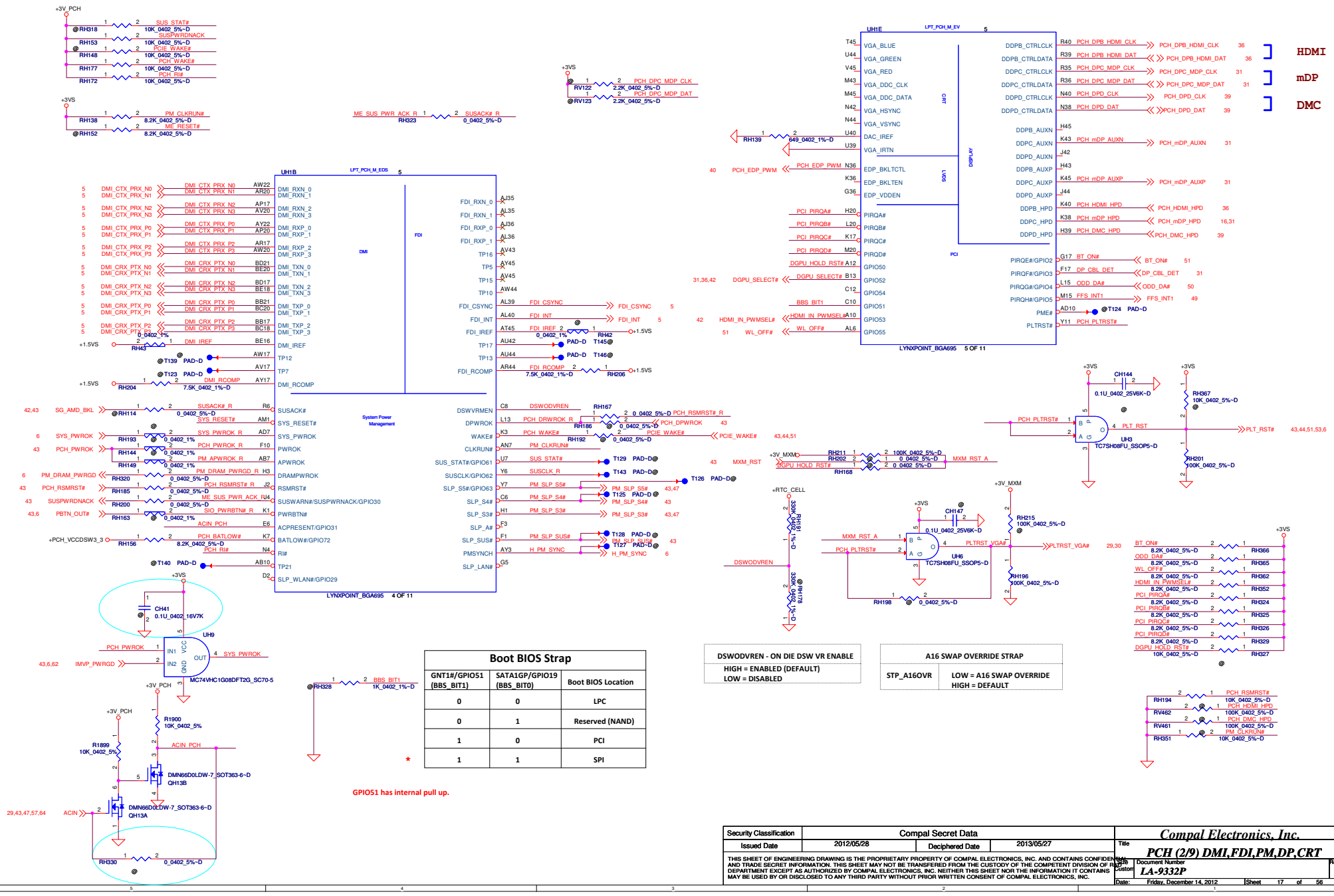

Boot BIOS Strap

GNT1#/GPIO51 (BBS_BIT1)	SATA1GP/GPIO19 (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

GPIO51 has internal pull up.

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

A16 SWAP OVERRIDE STRAP	
STP_A16OVR	LOW = A16 SWAP OVERRIDE HIGH = DEFAULT

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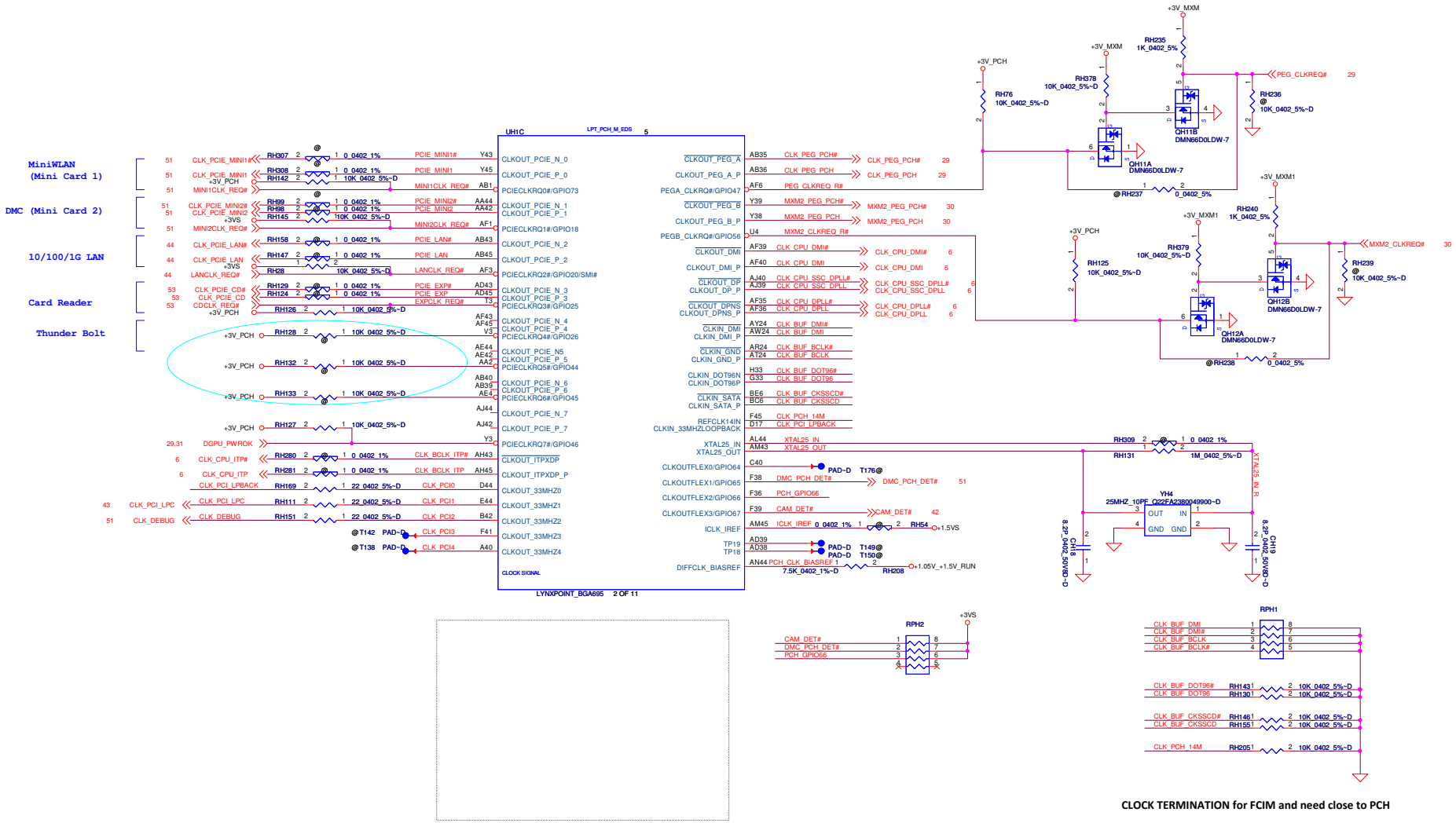
Compal Electronics, Inc.

Title: PCH (2/9) DMI,FDI,PM,DP,CRT

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 17 of 56



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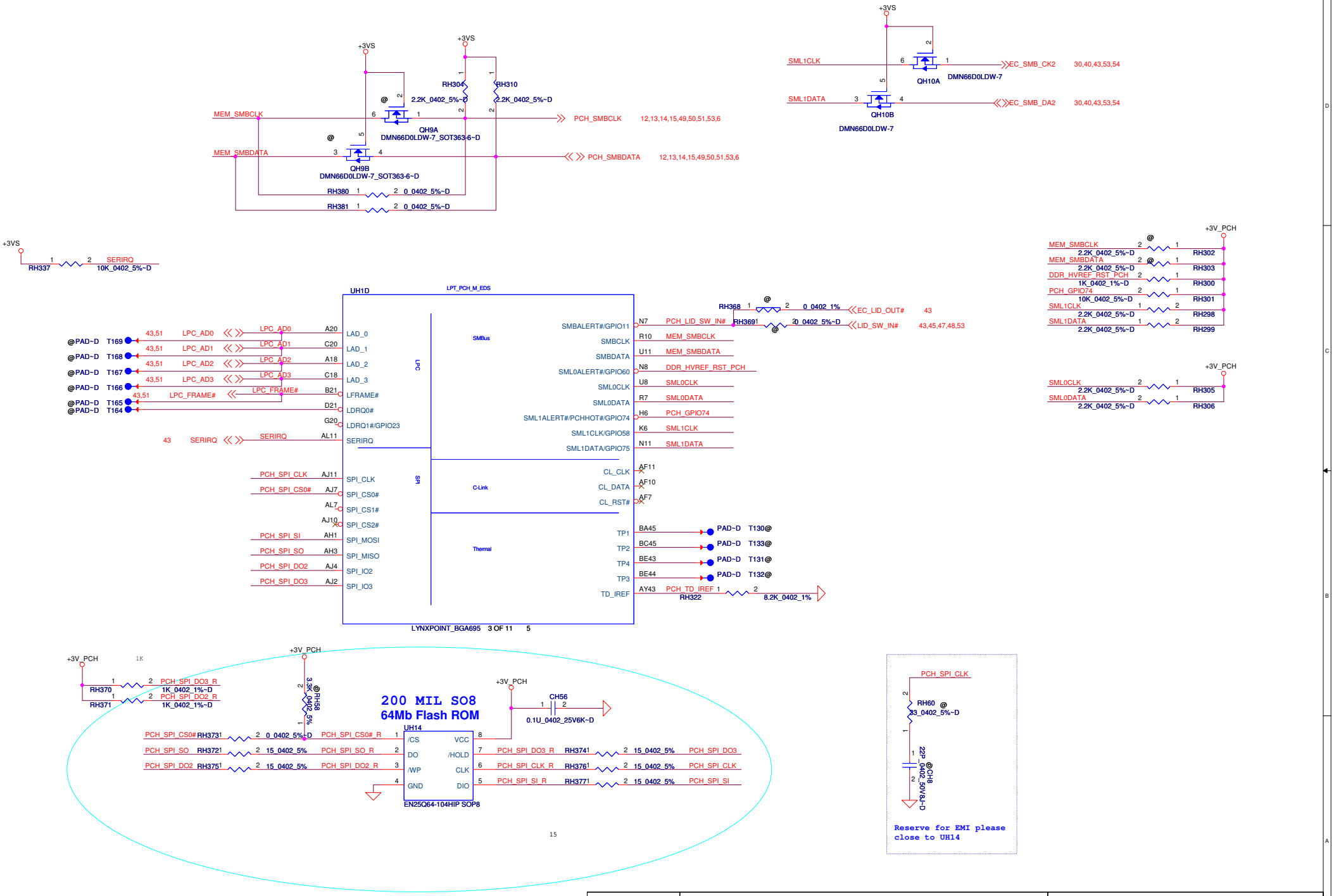
Compal Electronics, Inc.

Title: PCH (3/9) CLK

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 18 of 56



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Title: **PCH (4/9) SPI, SMBUS,LPC**

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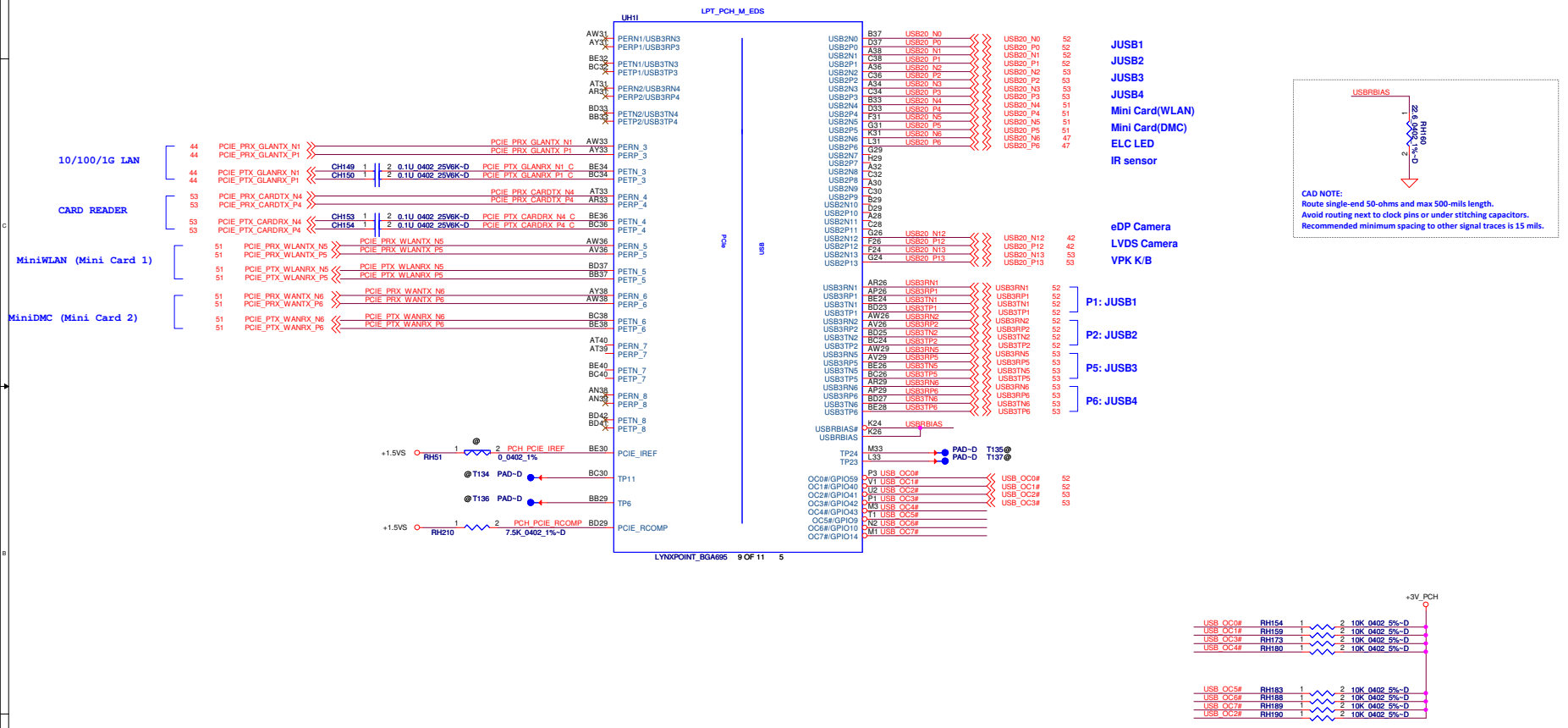

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Compal Electronics, Inc.

Title: PCH (5/9) PCIE,USB

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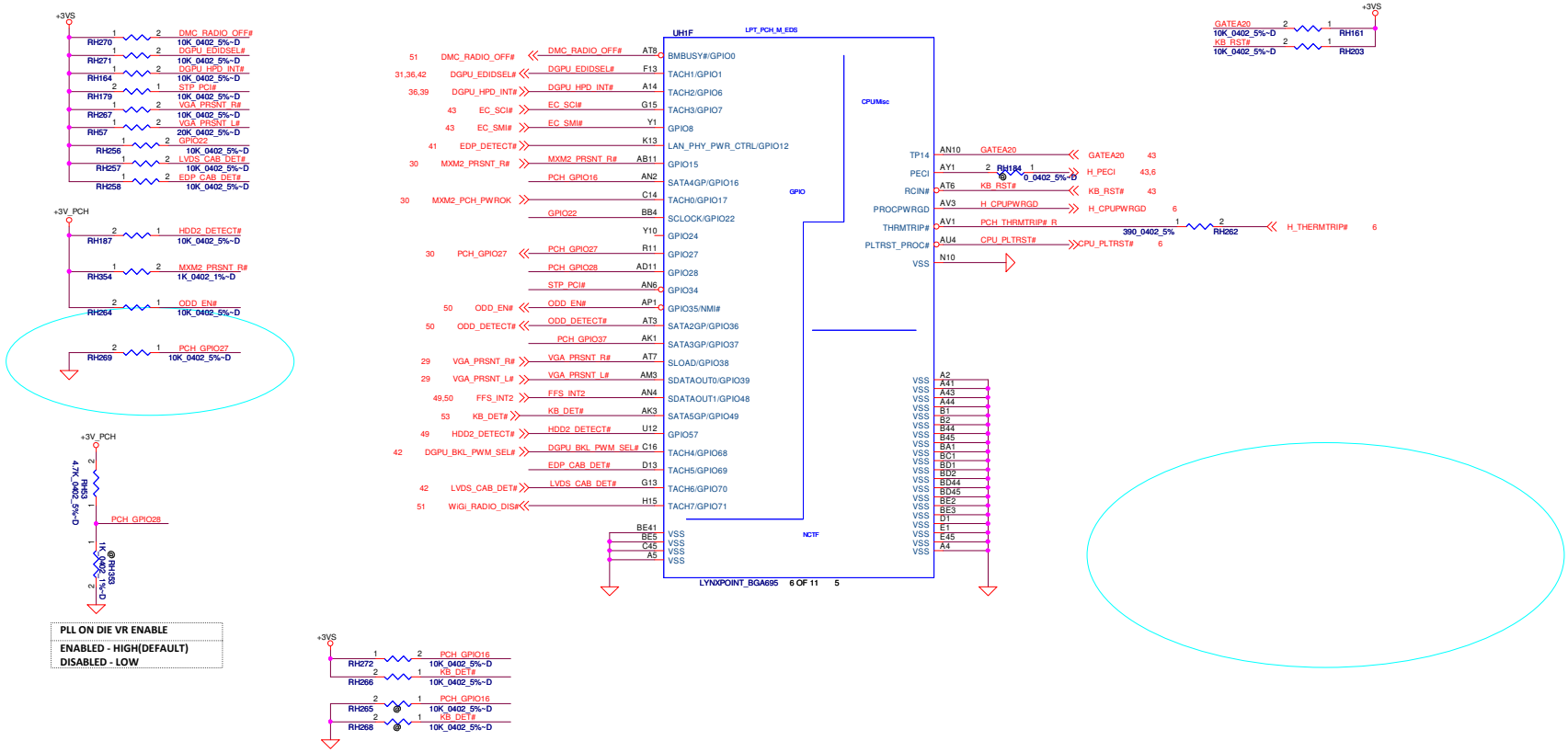
Date: Friday, December 14, 2012 | Sheet 20 of 56

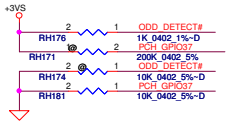


PLL ON DIE VR ENABLE

ENABLED - HIGH(DEFAULT)

DISABLED - LOW

Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
* USB X6,PCIEX8,SATAX4	01



SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO,MISC,NTFC

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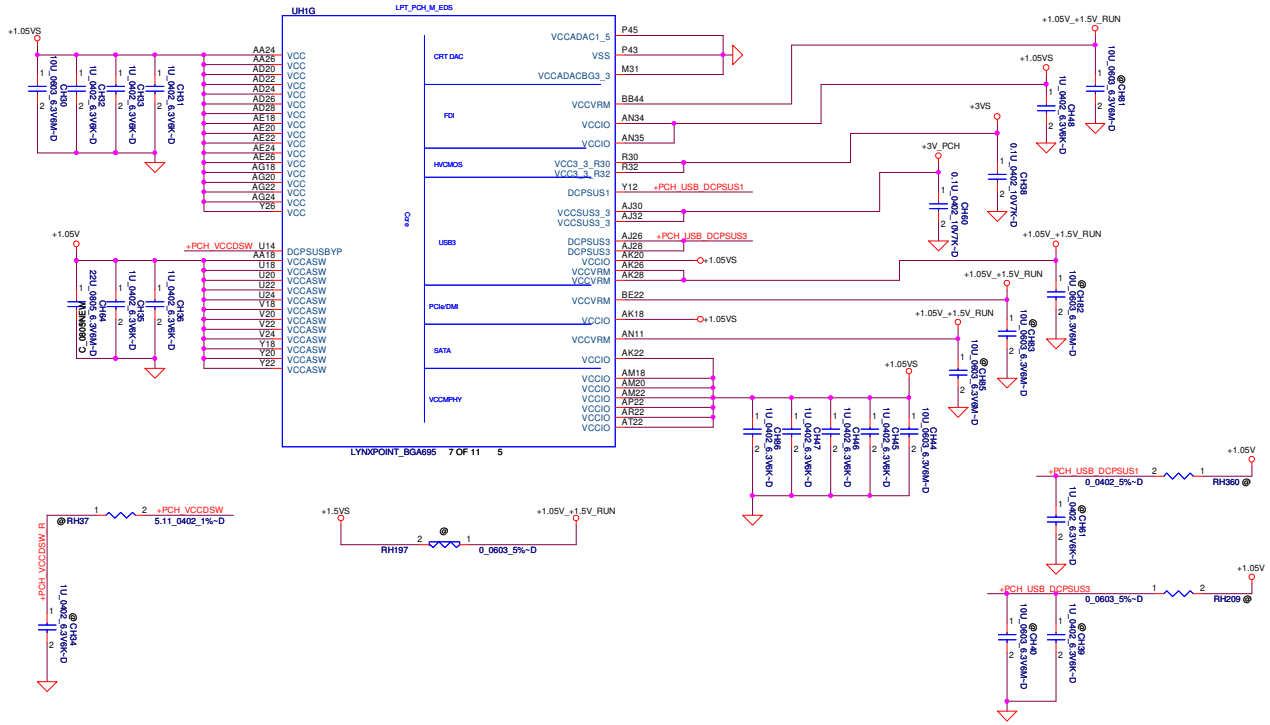

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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Compal Electronics, Inc.

Title: PCH (7/9) Power

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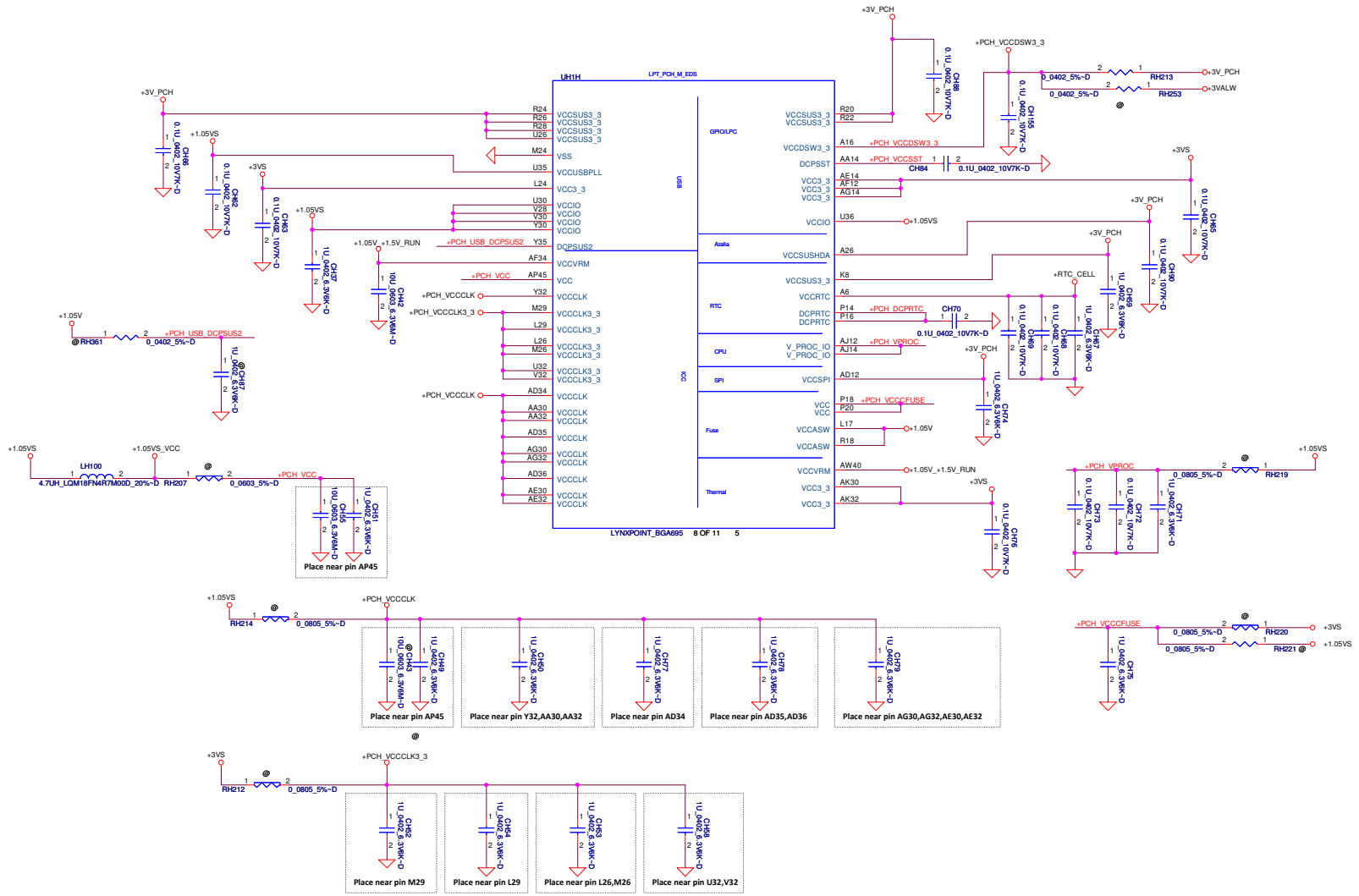

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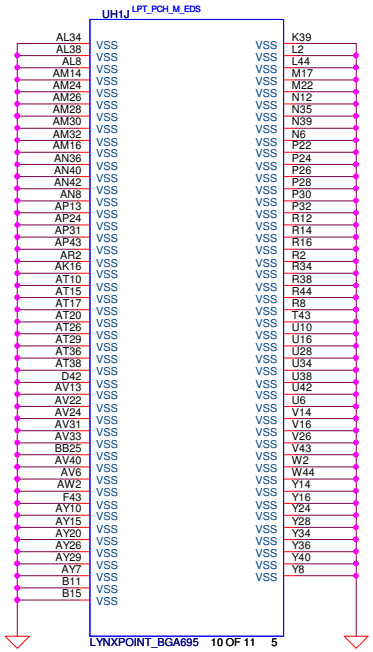
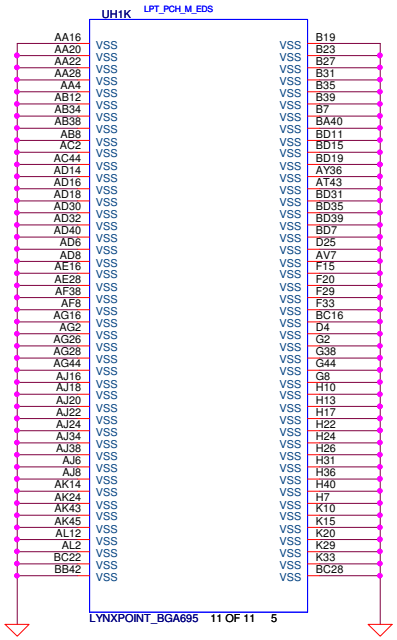
Compal Electronics, Inc.

Title: PCH (8/9) Power

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 23 of 56





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Compal Electronics, Inc.

Title: **PCH (9/9) Power**

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Compal Electronics, Inc.

Title: Cactus (1/4) DP/PCIE

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Compal Electronics, Inc.

Title: Cactus (2/4) CIO

Size	Document Number	Rev
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Compal Electronics, Inc.

Title: Cactus (3/4) PWR/VSS/DC-DC

Size	Document Number	Rev
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Compal Electronics, Inc.

Title: A

Size: Custom | Document Number: LA-9332P | Rev: 0.1

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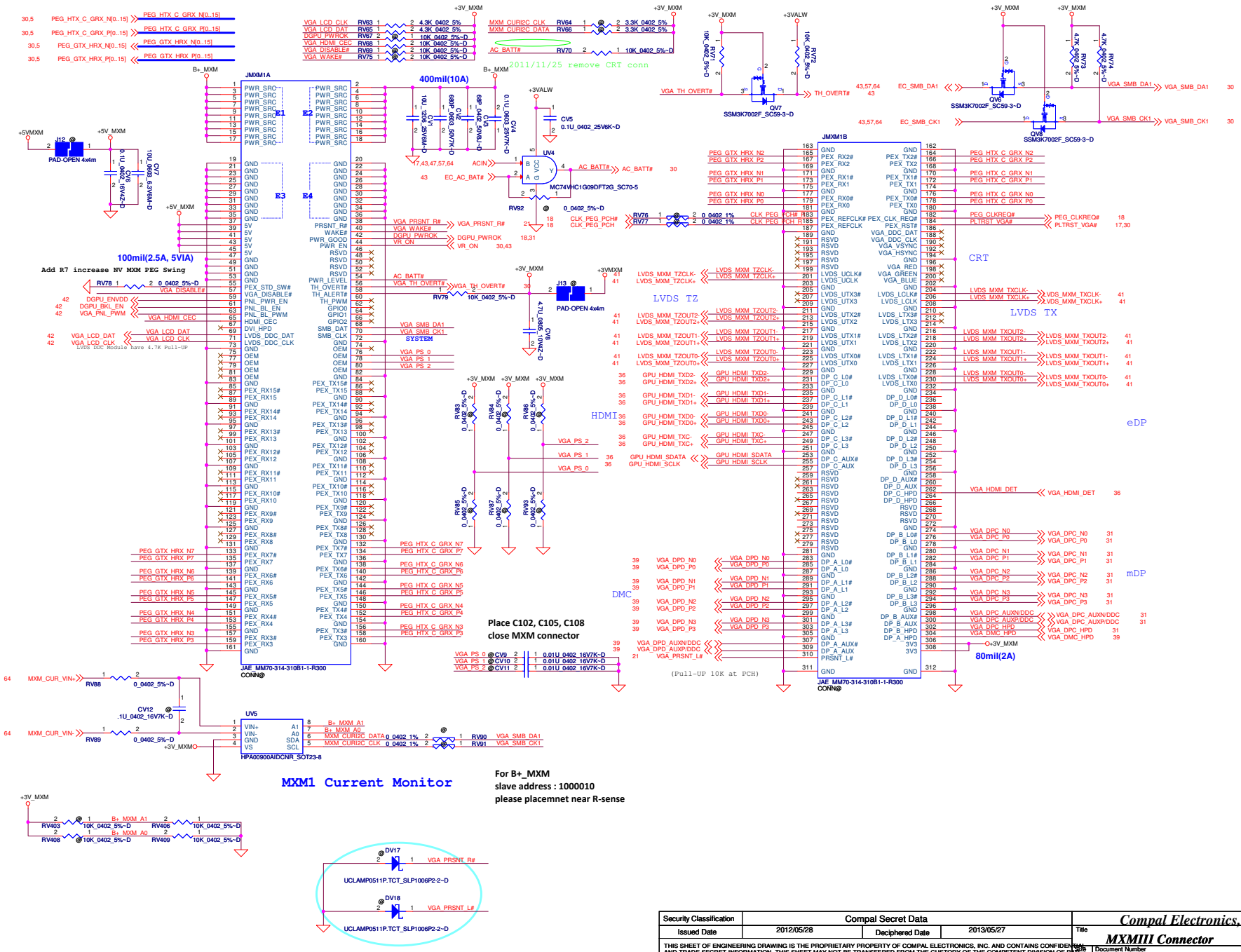

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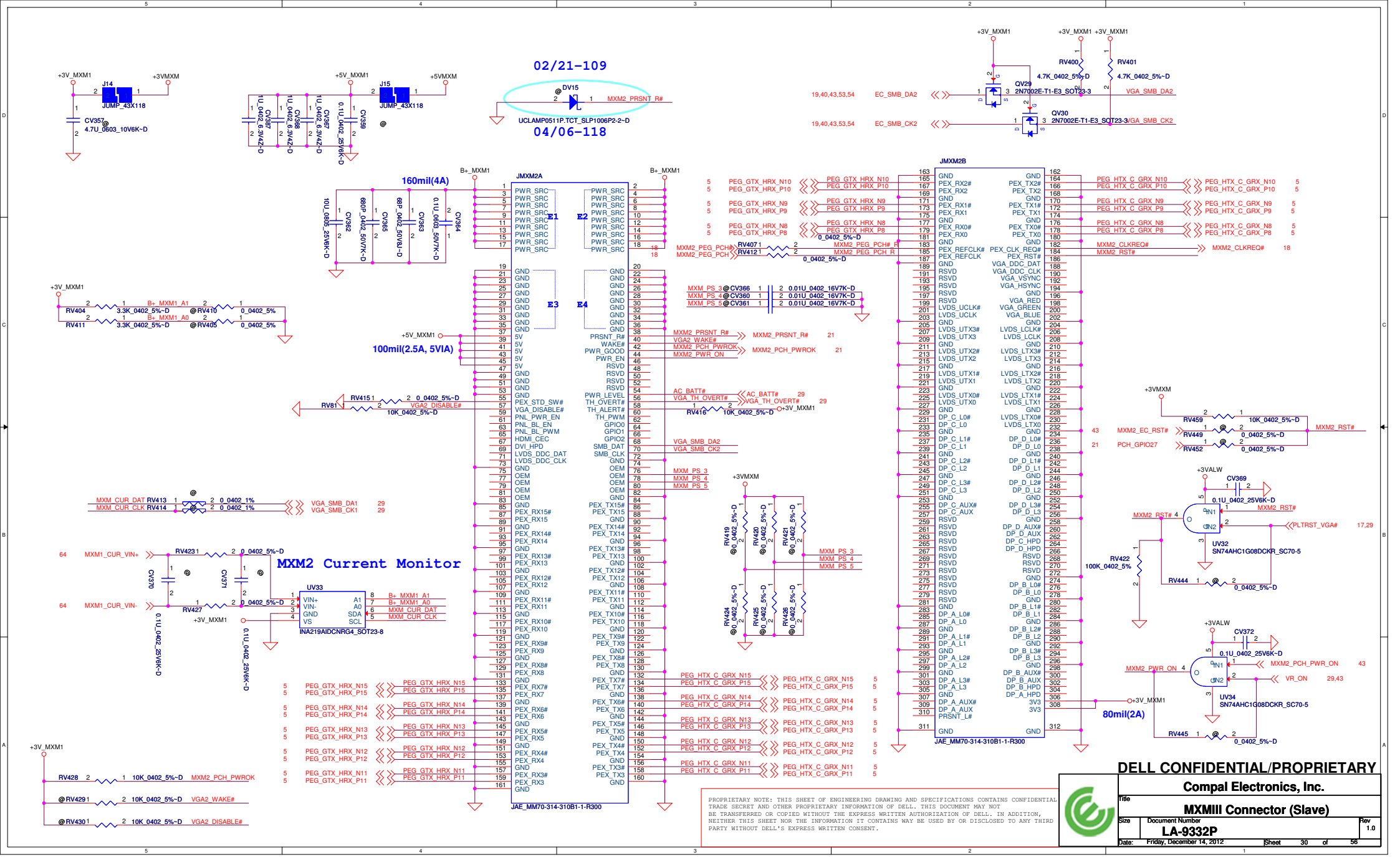
Compal Electronics, Inc.

Title: MXMIII Connector

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 29 of 56



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DELL CONFIDENTIAL/PROPRIETARY

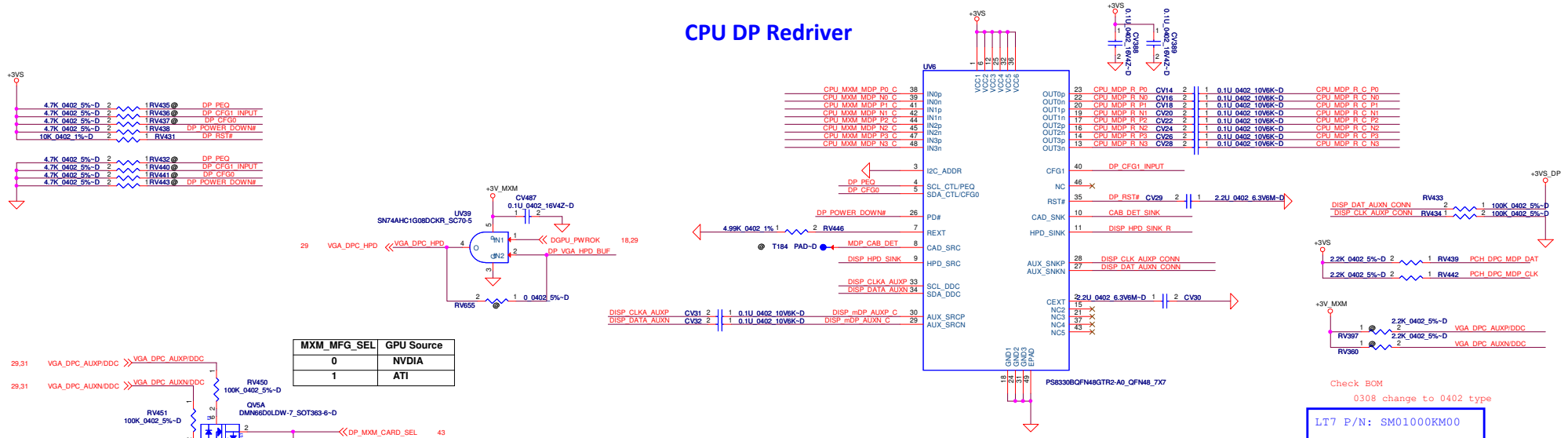
Compal Electronics, Inc.

Title: MXMIII Connector (Slave)

Size: | Document Number: LA-9332P | Rev: 1.0

Date: Friday, December 14, 2012 | Sheet 30 of 56

CPU DP Redriver



MXM_MFG_SEL	GPU Source
0	NVDIA
1	ATI

Check BOM

0308 change to 0402 type

LT7 P/N: SM01000KM00

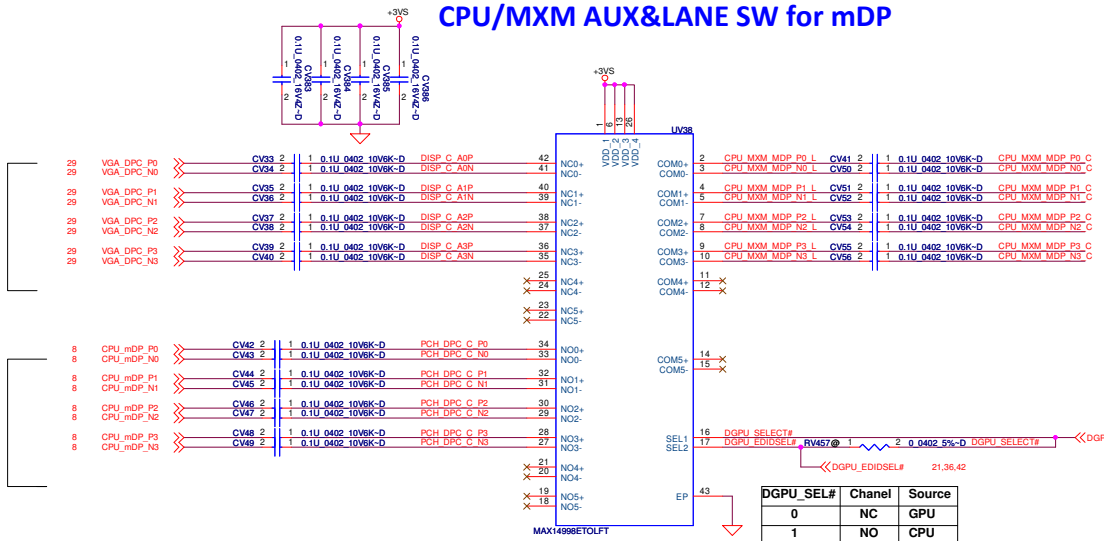
waiting to change new symbol

Need apply CIS part

Mini DP CONN

DGPU_SEL#	Chanel	Source
0	B1	GPU
1	B2	CPU

CPU/MXM AUX&LANE SW for mDP



S1	S0	1A 2A	Y
0	0	1B1 2B1	MXM_AUX
0	1	1B2 2B2	MXM_DDC
1	0	1B3 2B3	PCH_AUX
1	1	1B4 2B4	PCH_DDC

DGPU_SEL#	Chanel	Source
0	NC	GPU
1	NO	CPU

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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Compal Electronics, Inc.

Title: Mini DP/Thunder Bolt power

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 31 of 56

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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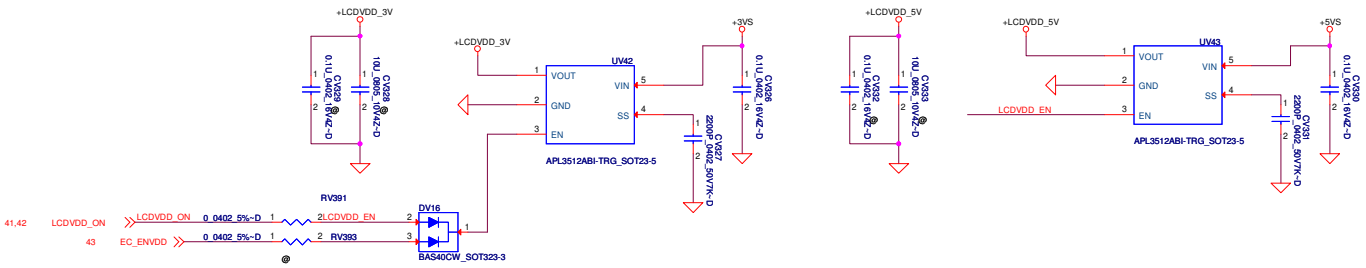
Compal Electronics, Inc.

Title: ***eDP SW-CPU & MXM***

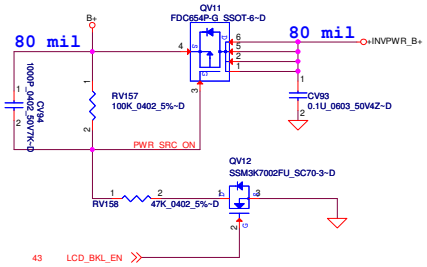
Size: Custom | Document Number: ***LA-9332P*** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 32 of 56

LCD POWER



Back light power



FDC654P: P CHANNAL

Panel backlight power control by EC

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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Compal Electronics, Inc.

Title: *eDP SW-eDP CONN*

Size: Custom | Document Number: *LA-9332P* | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 33 of 56

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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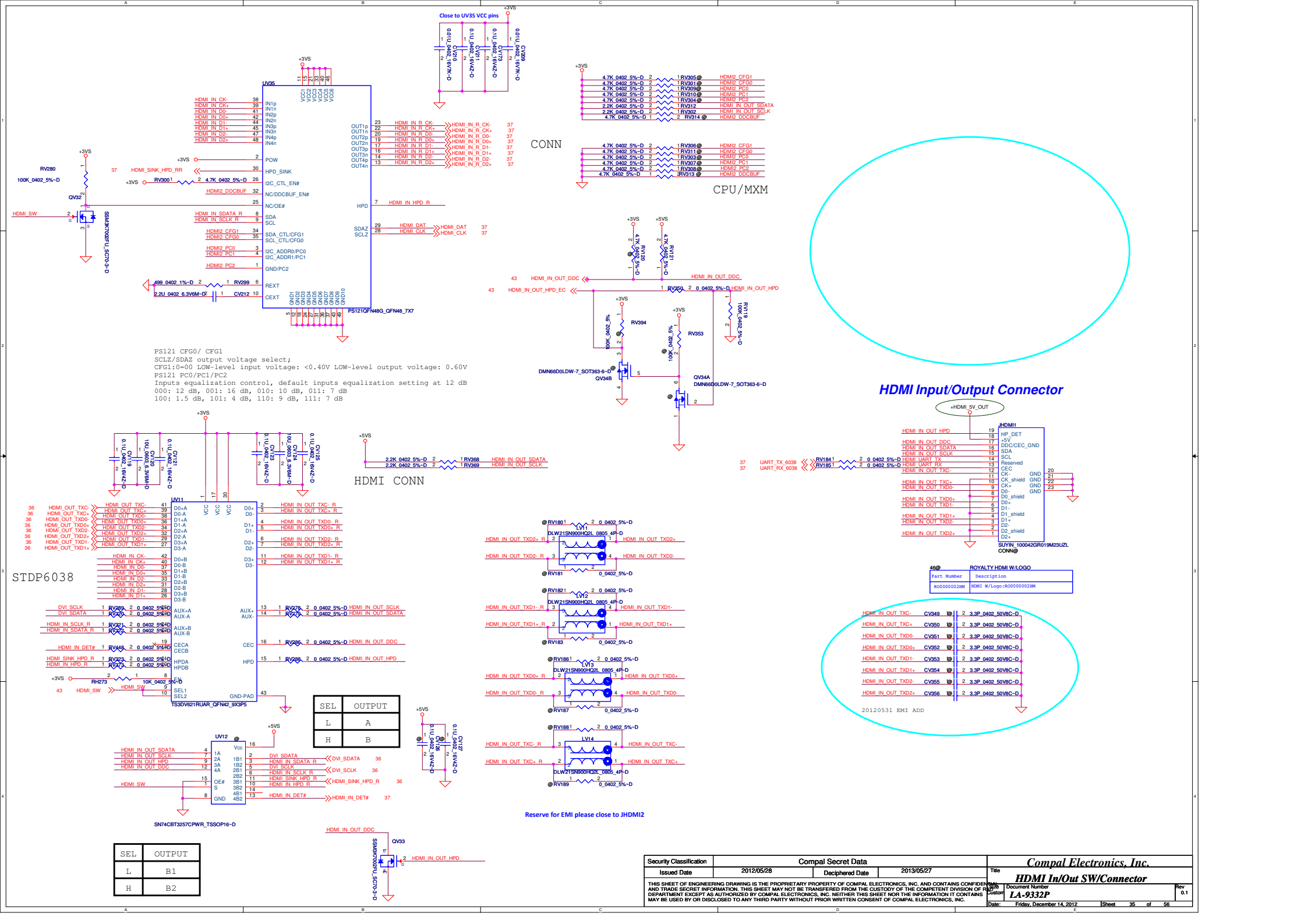
Title: *reserved*

Size: Custom | Document Number: *LA-9332P* | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 34 of 56



PS121 CFG0/ CFG1
SCLZ/SDAZ output voltage select;
CFG1:0=00 LOW-level input voltage: <0.40V LOW-level output voltage: 0.60V
PS121 PC0/PC1/PC2
Inputs equalization control, default inputs equalization setting at 12 dB
000: 12 dB, 001: 16 dB, 010: 10 dB, 011: 7 dB
100: 1.5 dB, 101: 4 dB, 110: 9 dB, 111: 7 dB

SEL	OUTPUT
L	A
H	B

SEL	OUTPUT
L	B1
H	B2

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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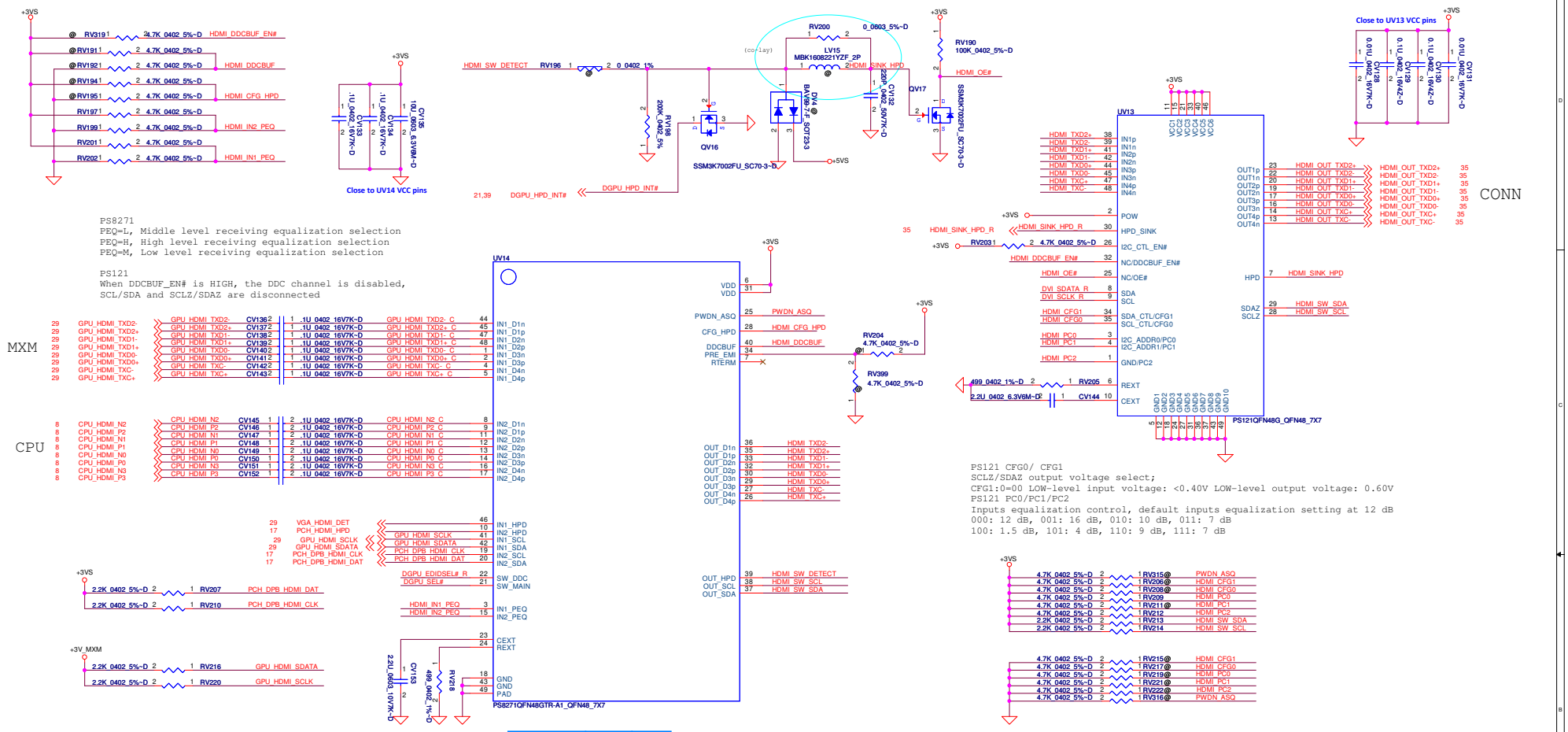
Compal Electronics, Inc.

Title: HDMI In/Out SW/Connector

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 35 of 56



HDMI_SW_DET	0	1
Y	IN1	IN2
	MXM	PCH

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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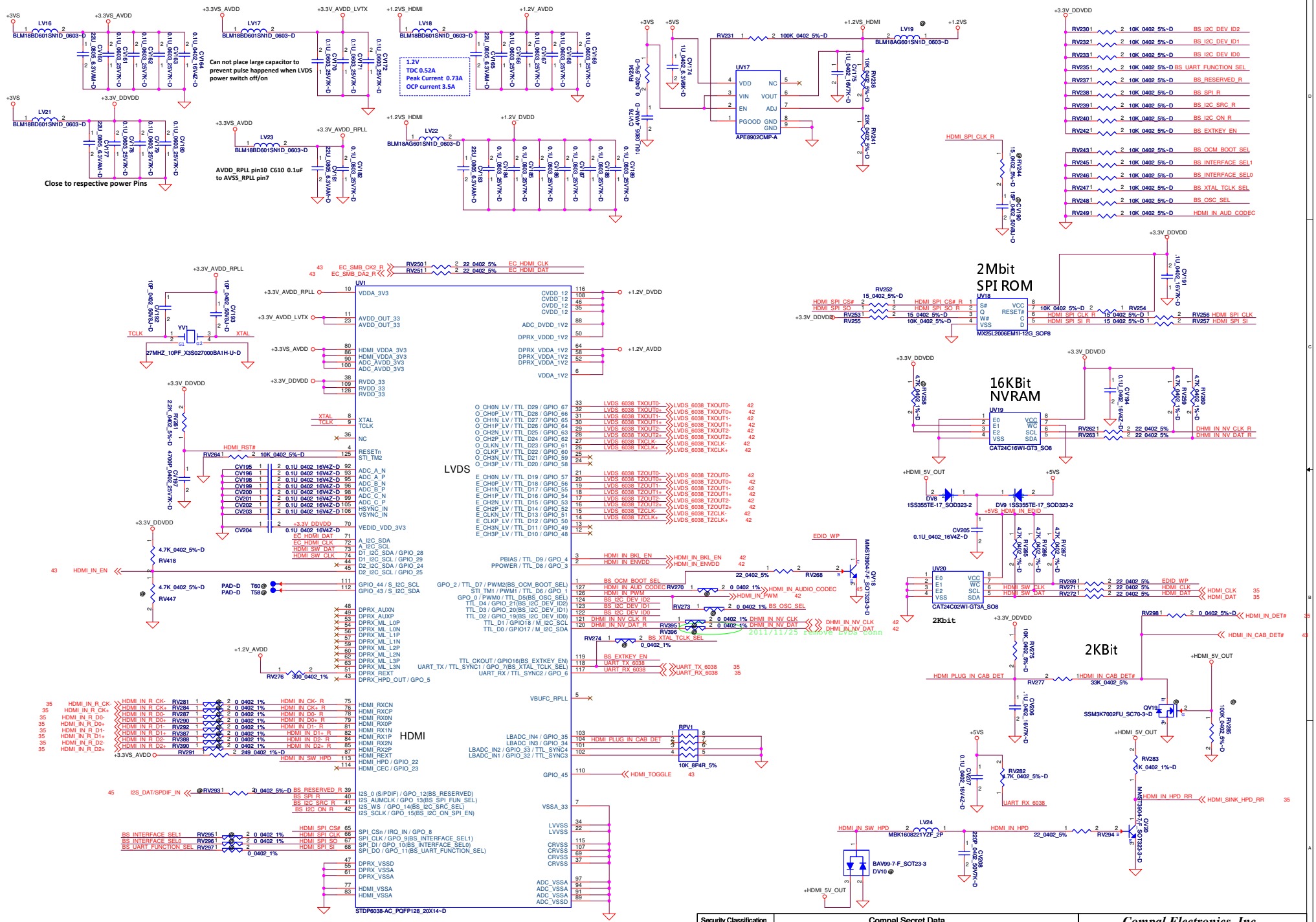
Compal Electronics, Inc.

Title: HDMI SW-CPU & MXM/Re-driver

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 36 of 56



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Compal Electronics, Inc.

Title: HDMI to LVDS-STDP6038

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 37 of 56

Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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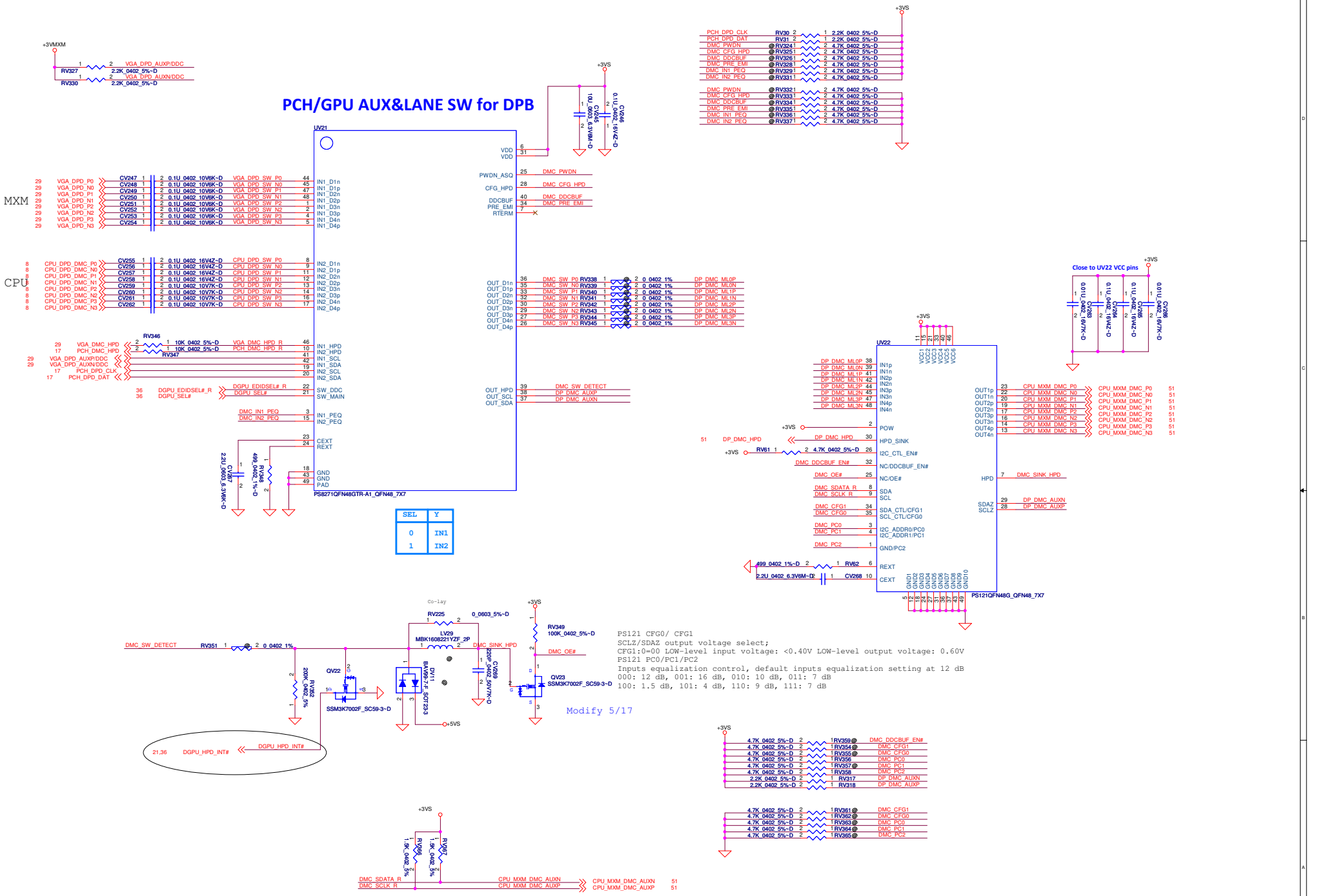
Compal Electronics, Inc.

Title: *LVDS to eDP-STDP4028*

Size: Custom | Document Number: *LA-9332P* | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 38 of 56

PCH/GPU AUX&LANE SW for DPB



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Issued Date	2012/05/14	Deciphered Date	2013/05/13

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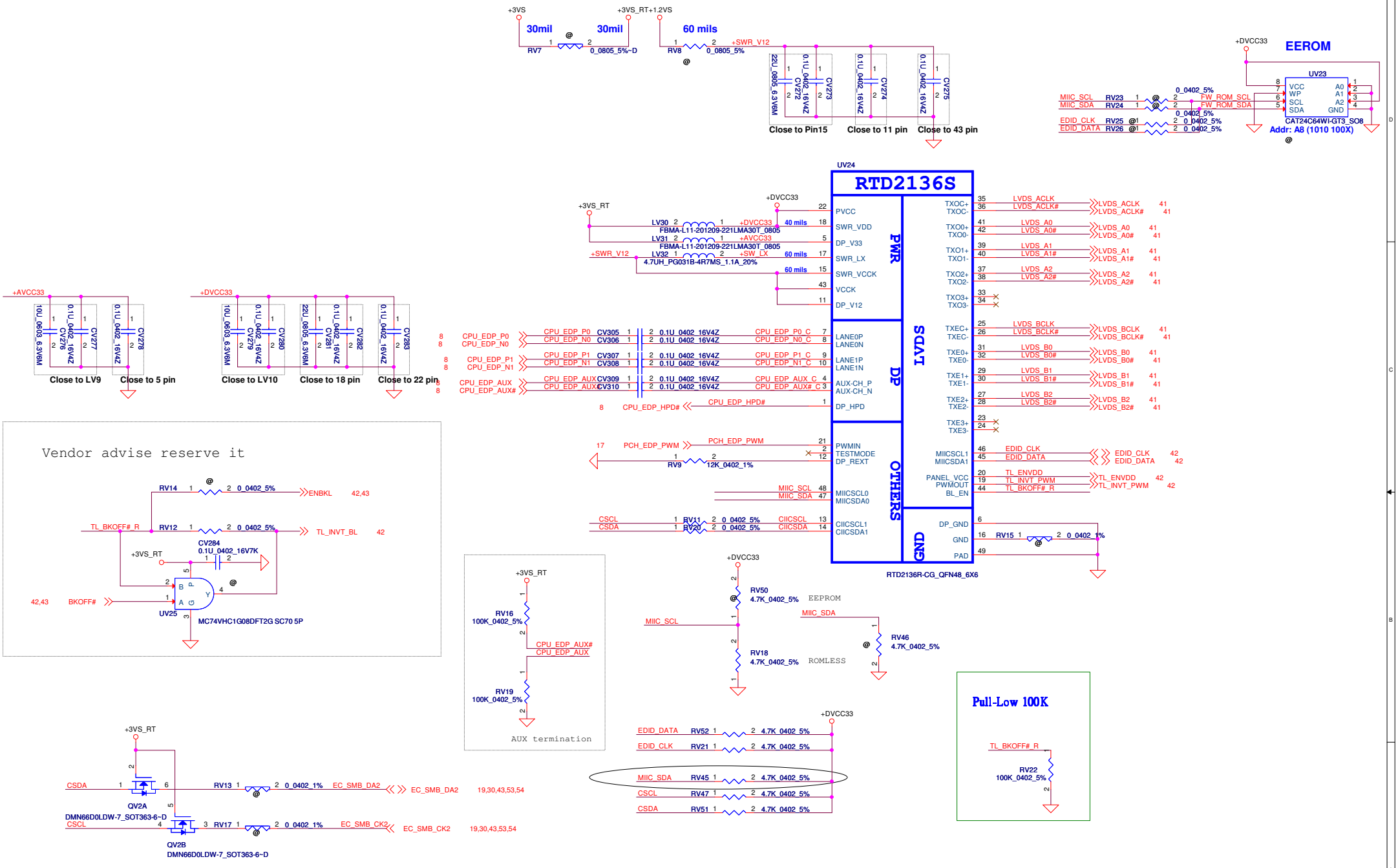
Compal Electronics, Inc.

Title: DP SW for DMC

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 39 of 56



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Issued Date	2012/05/14	Deciphered Date	2013/05/13

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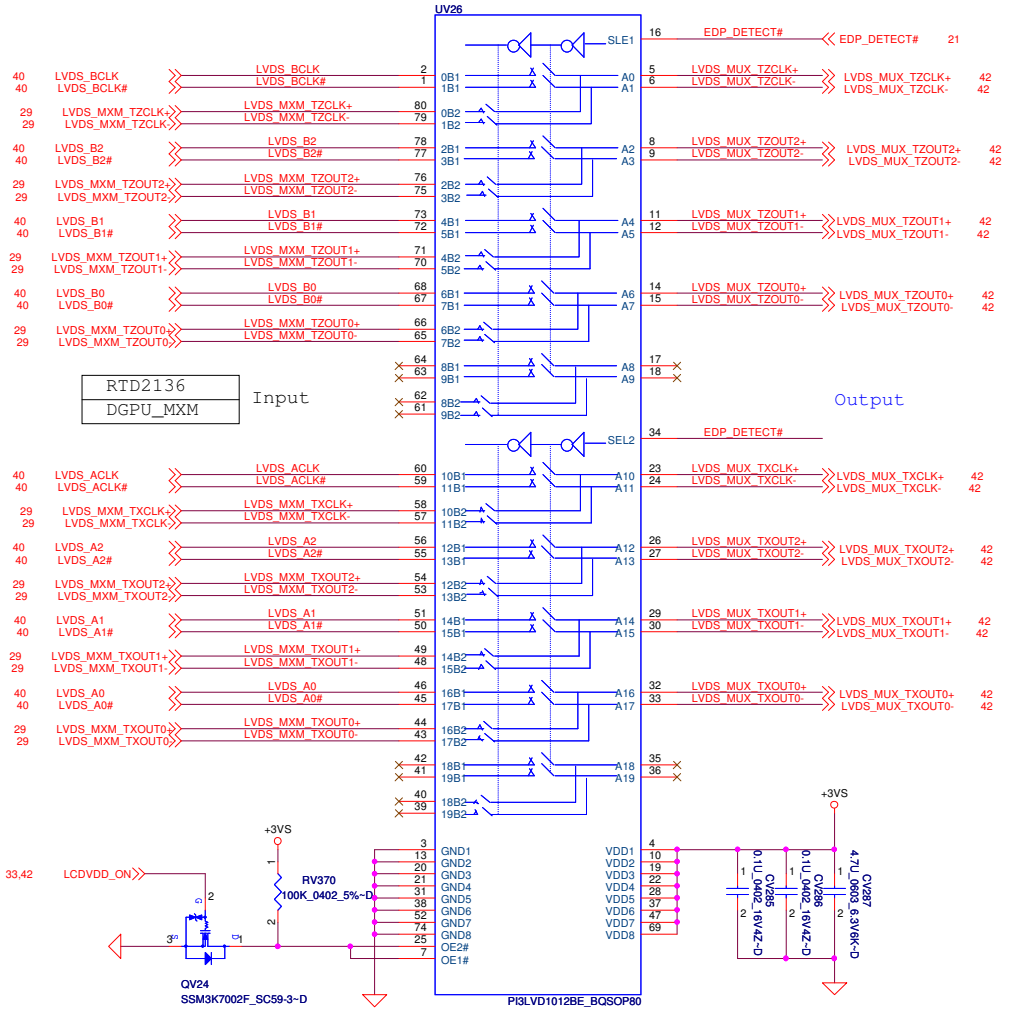
Title: *Translator RTD2136R*

Size: Custom | Document Number: *LA-9332P* | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 40 of 56

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS



SEL	Y
L	RTD2136
H	DGPU_MXM

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/05/14	Deciphered Date 2013/05/13	Title LVDS SW- 1 to 2 & GPU/PCH
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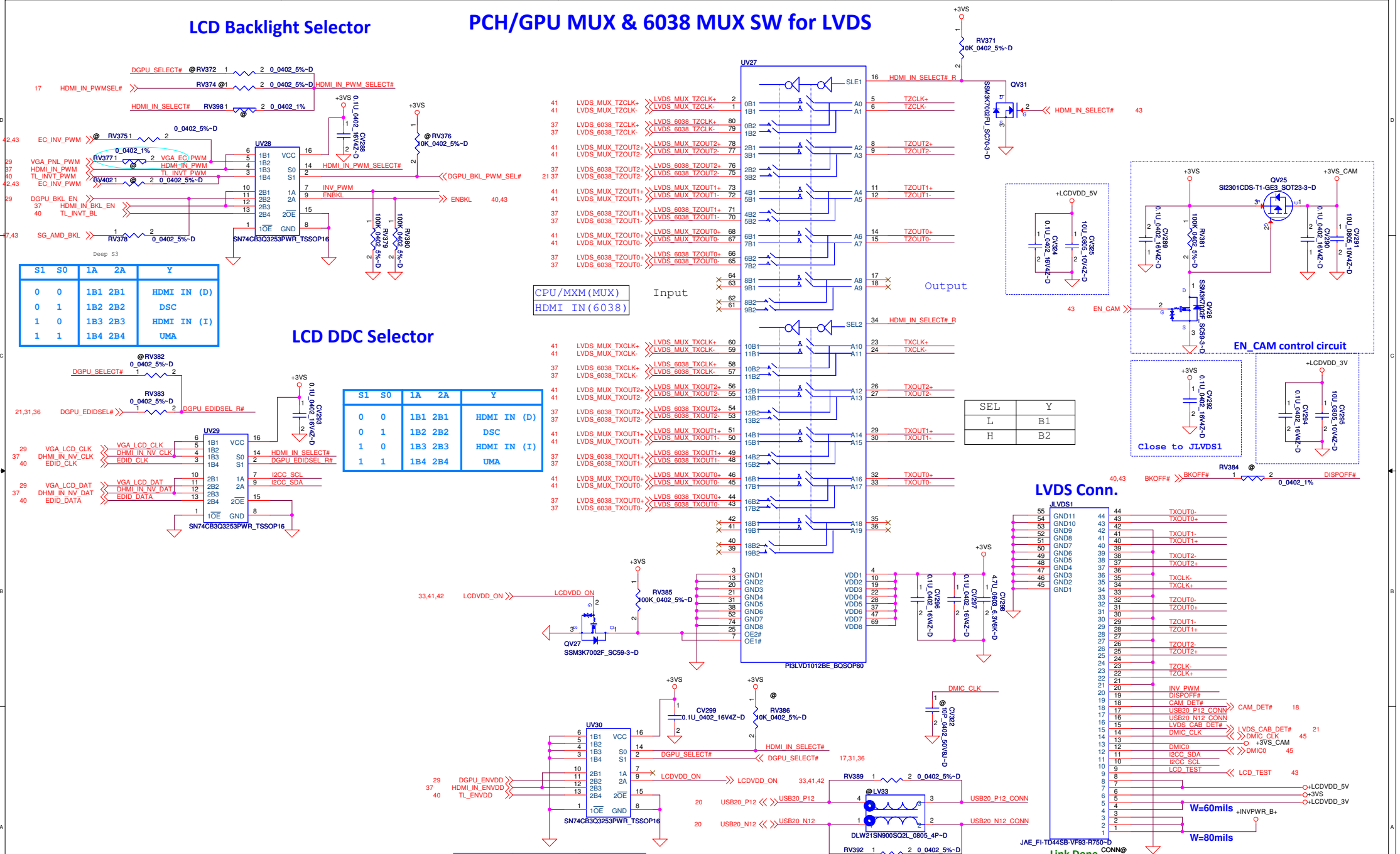
			Date: Friday, December 14, 2012 / Sheet 41 of 56

LCD Backlight Selector

PCH/GPU MUX & 6038 MUX SW for LVDS



S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA

CPU/MXM(MUX)	Input
HDMI IN(6038)	

SEL	Y
L	B1
H	B2

LCD DDC Selector

S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN (D)
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN (I)
1	1	1B4 2B4	UMA

S1	S0	1A 2A	Y
0	0	1B1 2B1	HDMI IN
0	1	1B2 2B2	DSC
1	0	1B3 2B3	HDMI IN
1	1	1B4 2B4	UMA

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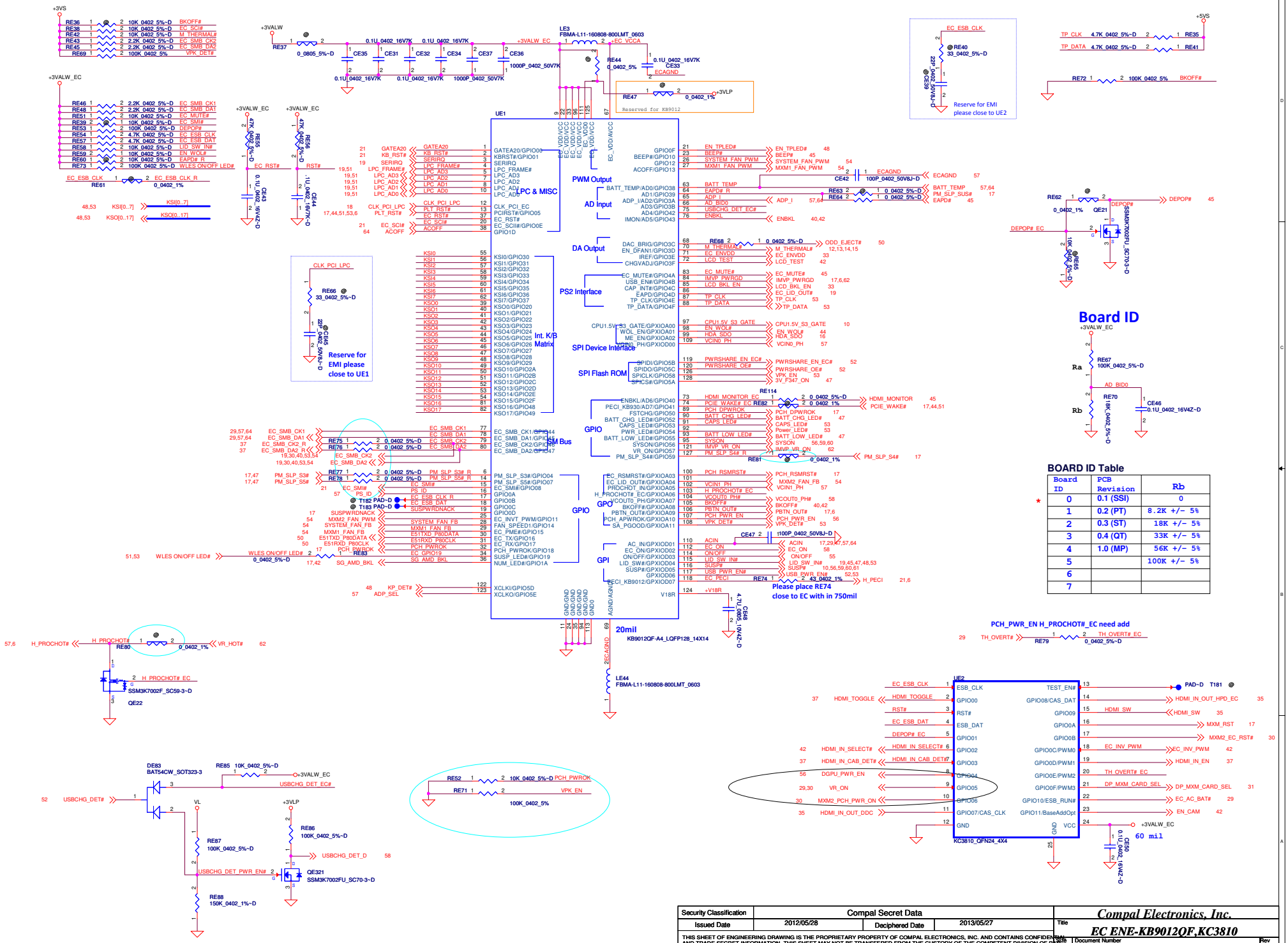
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: LVDS SW- 6038/SYSTEM & CONN

Size | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 42 of 56



Board ID	PCB Revision	Rb
0	0.1 (SSI)	0
1	0.2 (PT)	8.2K +/- 5%
2	0.3 (ST)	18K +/- 5%
3	0.4 (QT)	33K +/- 5%
4	1.0 (MP)	56K +/- 5%
5		100K +/- 5%
6		
7		

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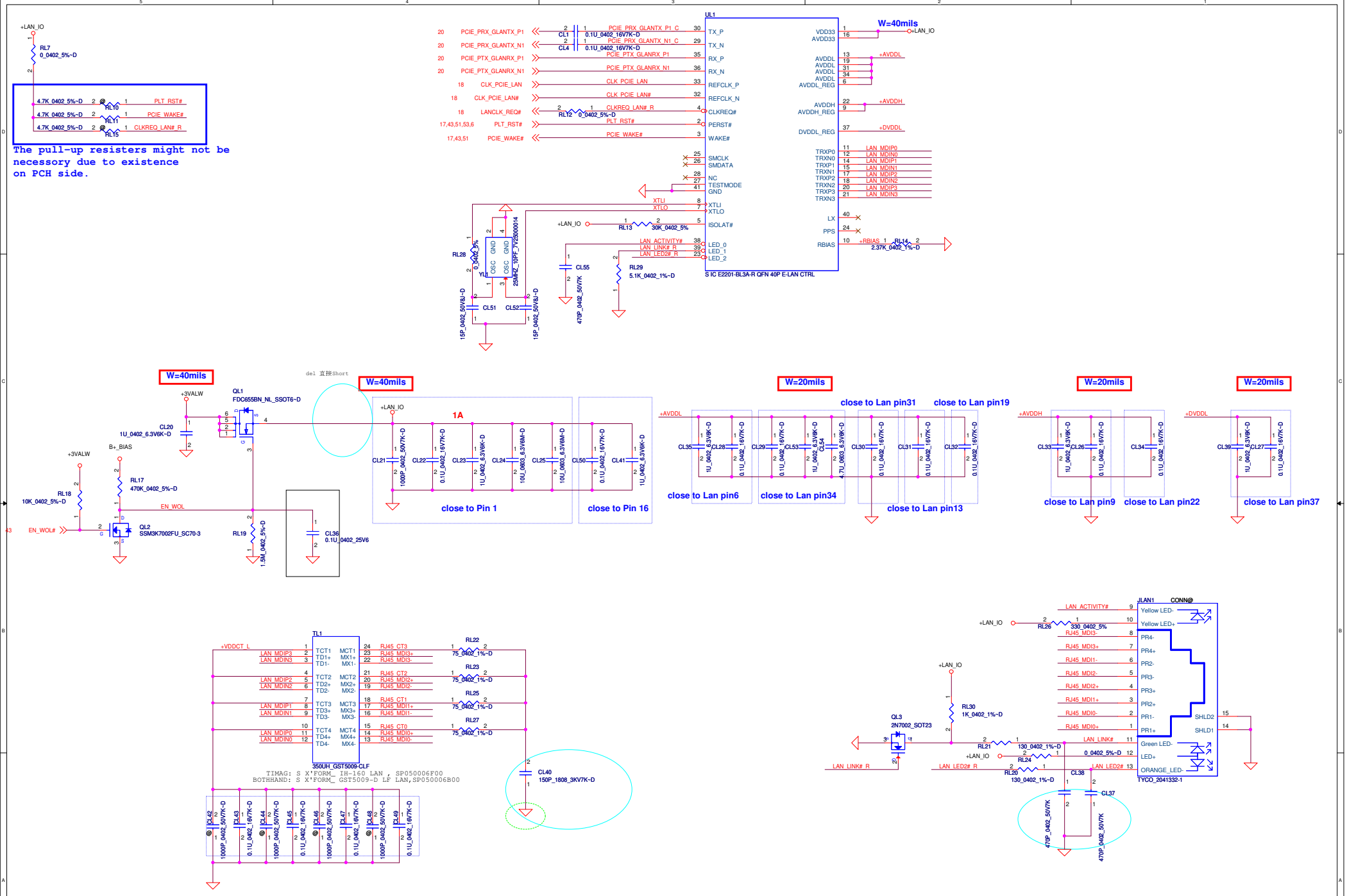

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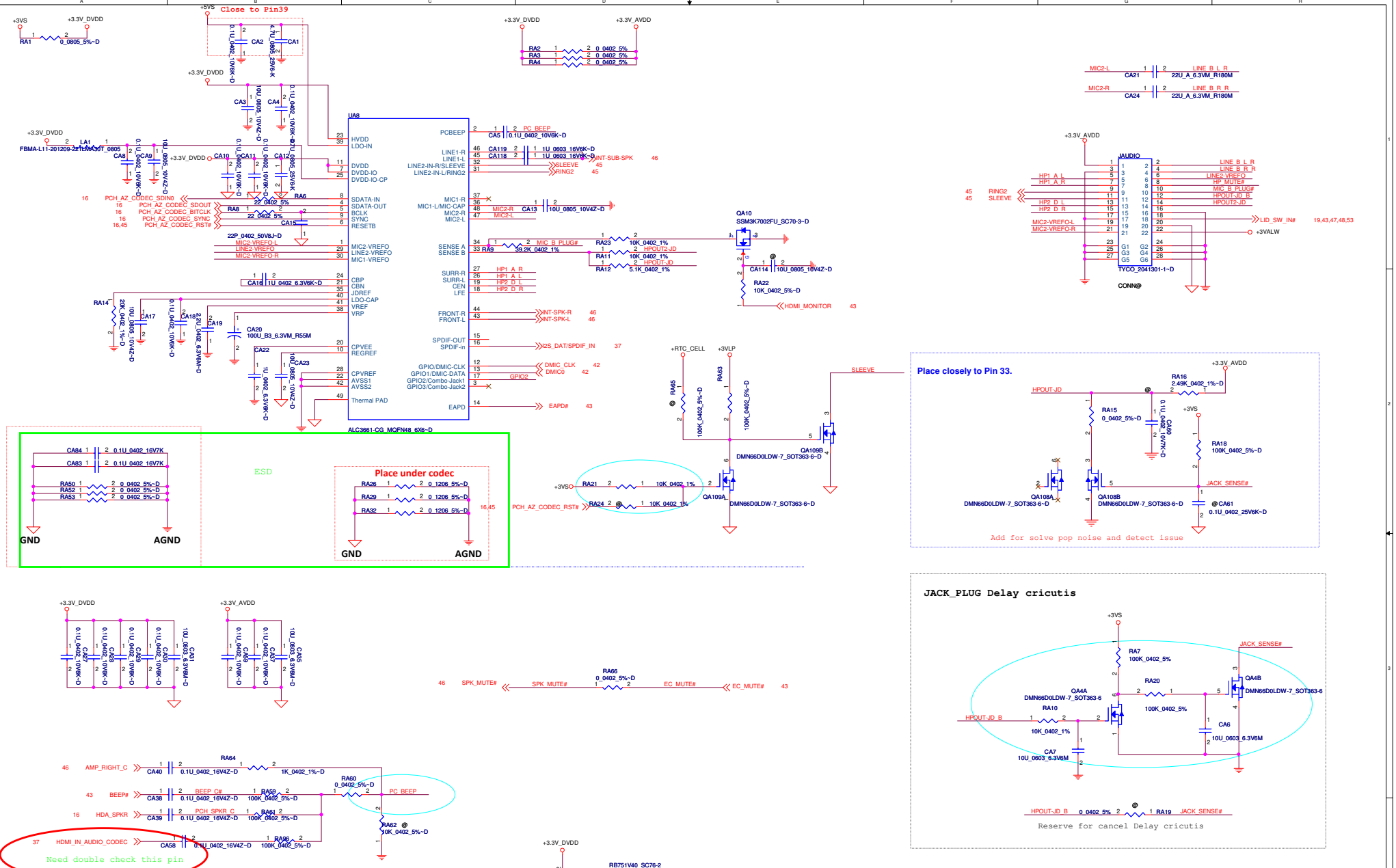
Compal Electronics, Inc.

Title: **GLAN AR8151 AL1A/ RJ45**

Size | Document Number: **LA-9332P** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 44 of 56



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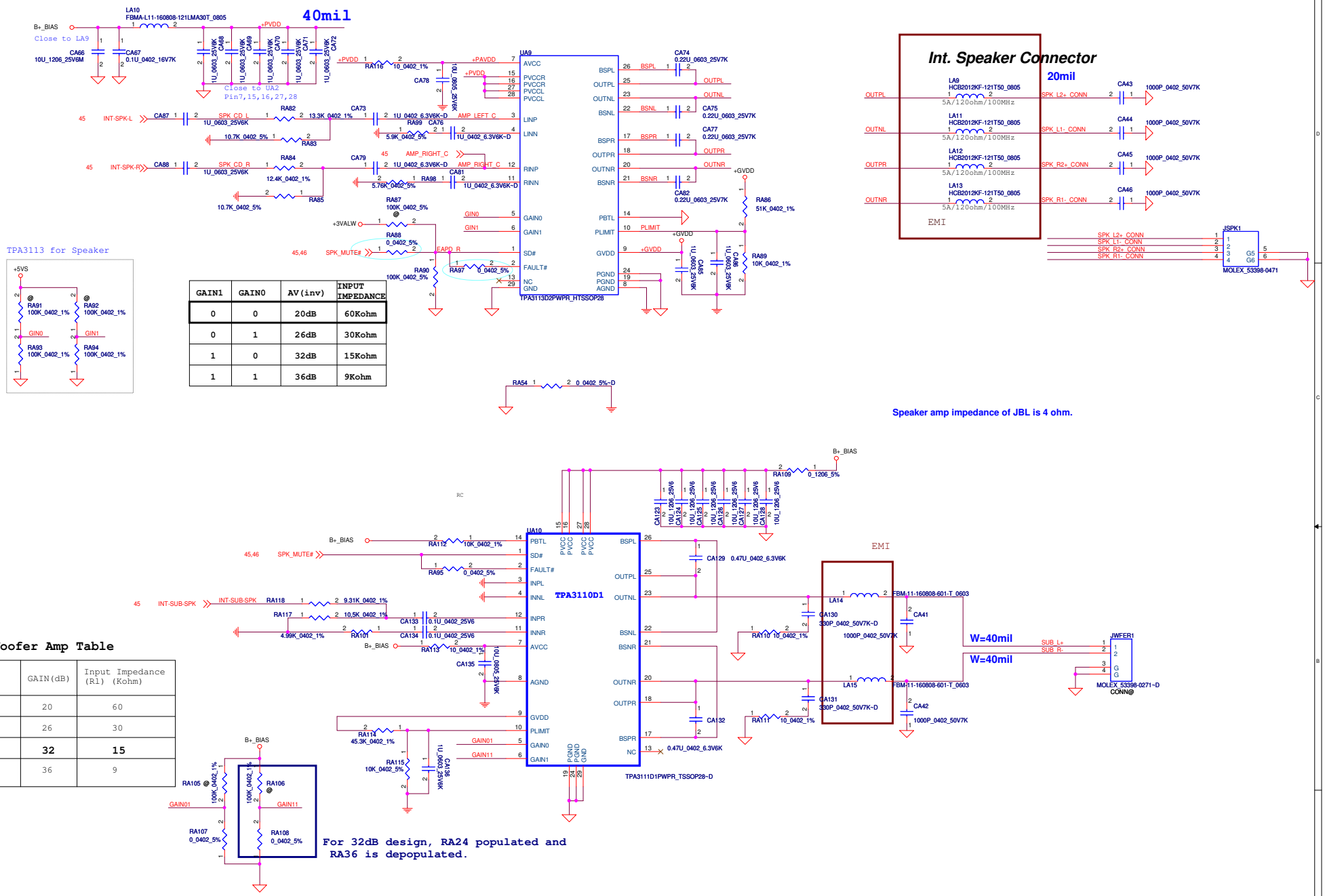
Compal Electronics, Inc.

Title: HD Audio ALC3661

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 45 of 56



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

Woofer Amp Table

G1	G0	GAIN(dB)	Input Impedance (Rl) (Kohm)
0	0	20	60
0	1	26	30
1	**0**	**32**	**15**
1	1	36	9

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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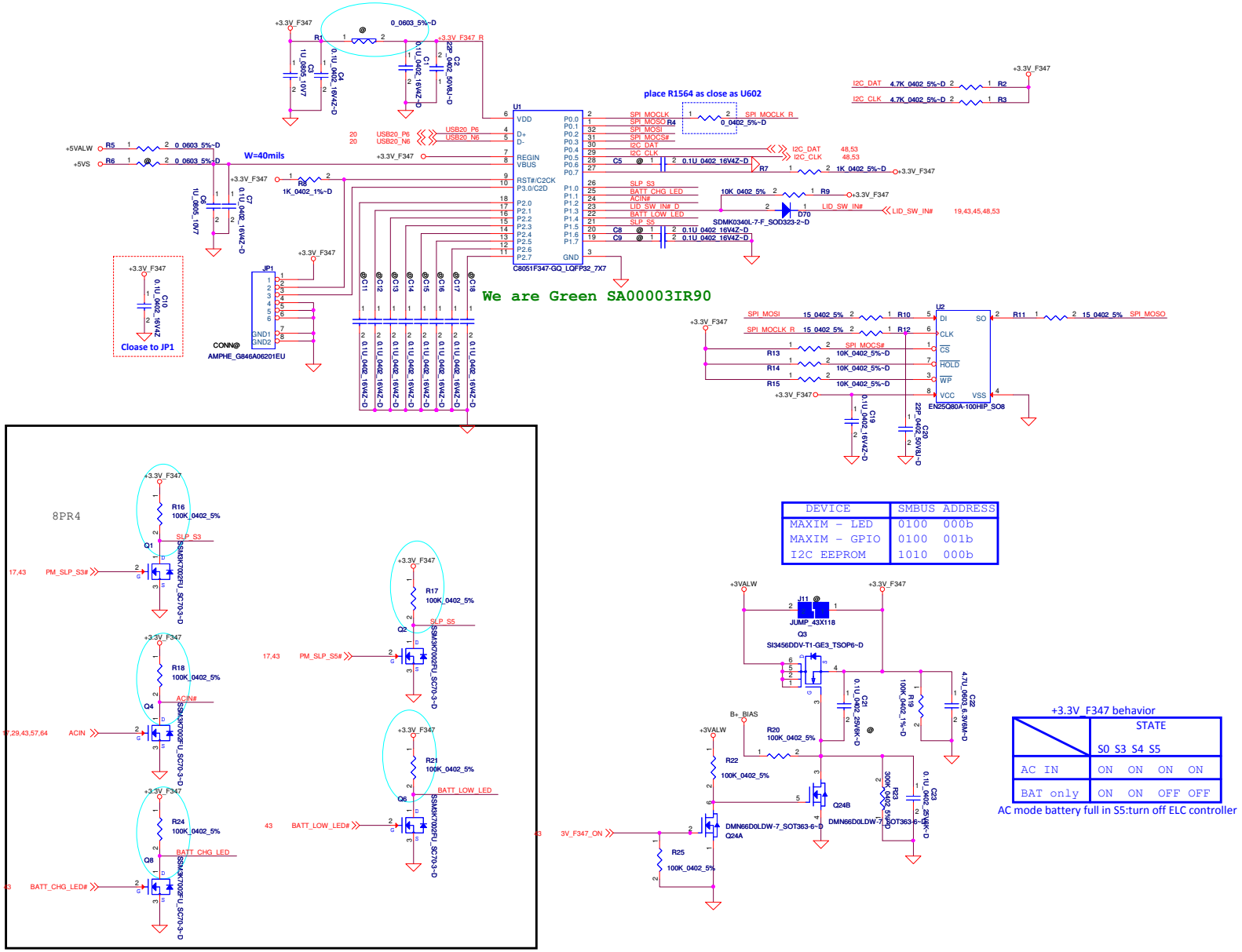
Compal Electronics, Inc.

Title: **Amp TPA6017/subwoofer/ Audio Jack**

Size | Document Number: **LA-9332P** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 46 of 56



DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b

+3.3V_F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5:turn off ELC controller

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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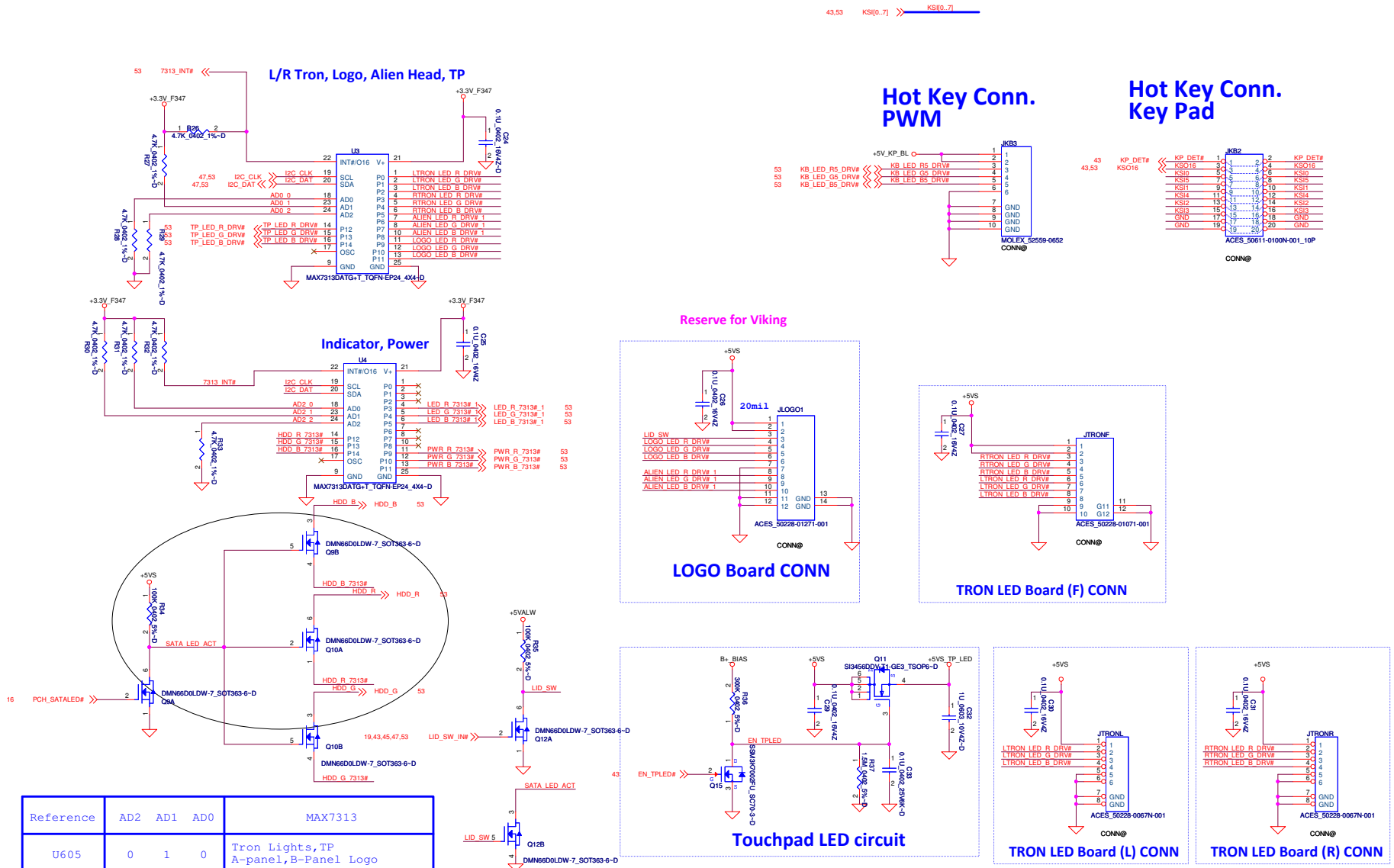
Compal Electronics, Inc.

Title: ELC (1)

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 47 of 56



Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights,TP A-panel,B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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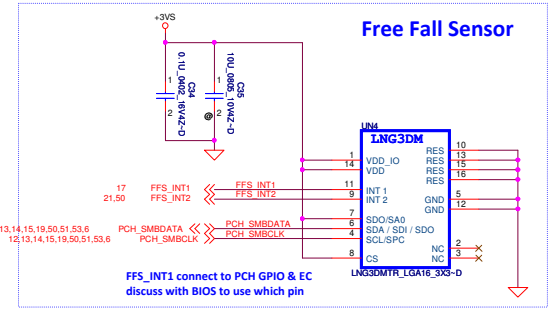
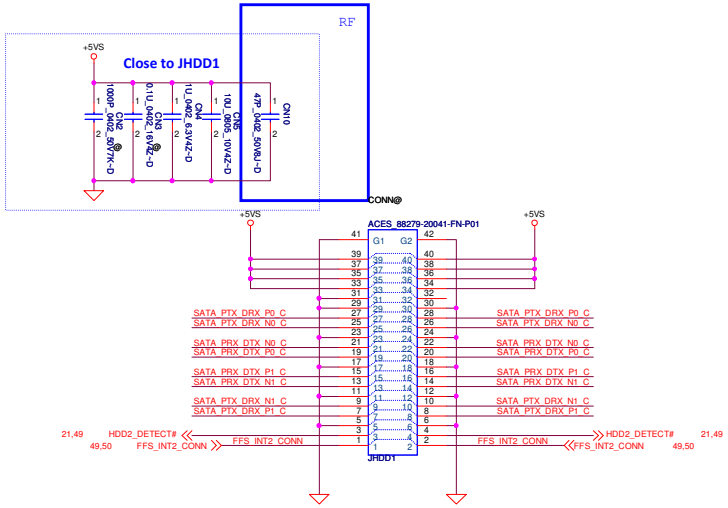
Compal Electronics, Inc.

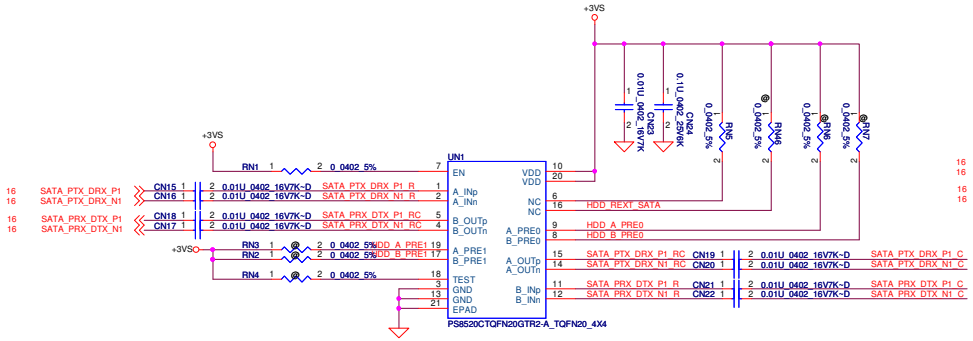
Title: ELC (2)

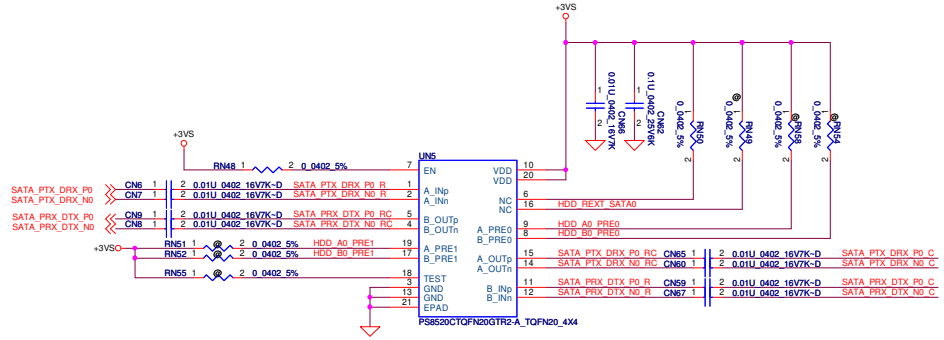
Size: Custom | Document Number: LA-9332P | Rev: 0.1

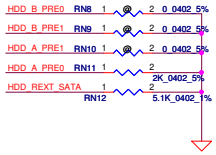
Date: Friday, December 14, 2012 | Sheet 48 of 56

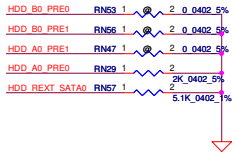












Pin 20:
PARADE PS8250B:
Reserve RN46, Mount RN12

PERICOM PI3EQX6741ST:
Mount RN46, Reserve RN12

ASMEDIA ASM1466:
Mount RN46, Reserve RN12

Pin 9:
PARADE PS8250B:
Reserve RN11.

PERICOM PI3EQX6741ST:
Reserve RN11

ASMEDIA ASM1466:
Mount RN11 to pull down

Pin 20:
PARADE PS8250B:
Reserve R49, Mount R57

PERICOM PI3EQX6741ST:
Mount R49, Reserve R57

ASMEDIA ASM1466:
Mount R49, Reserve R57

Pin 9:
PARADE PS8250B:
Reserve R29.

PERICOM PI3EQX6741ST:
Reserve R29

ASMEDIA ASM1466:
Mount R29 to pull down

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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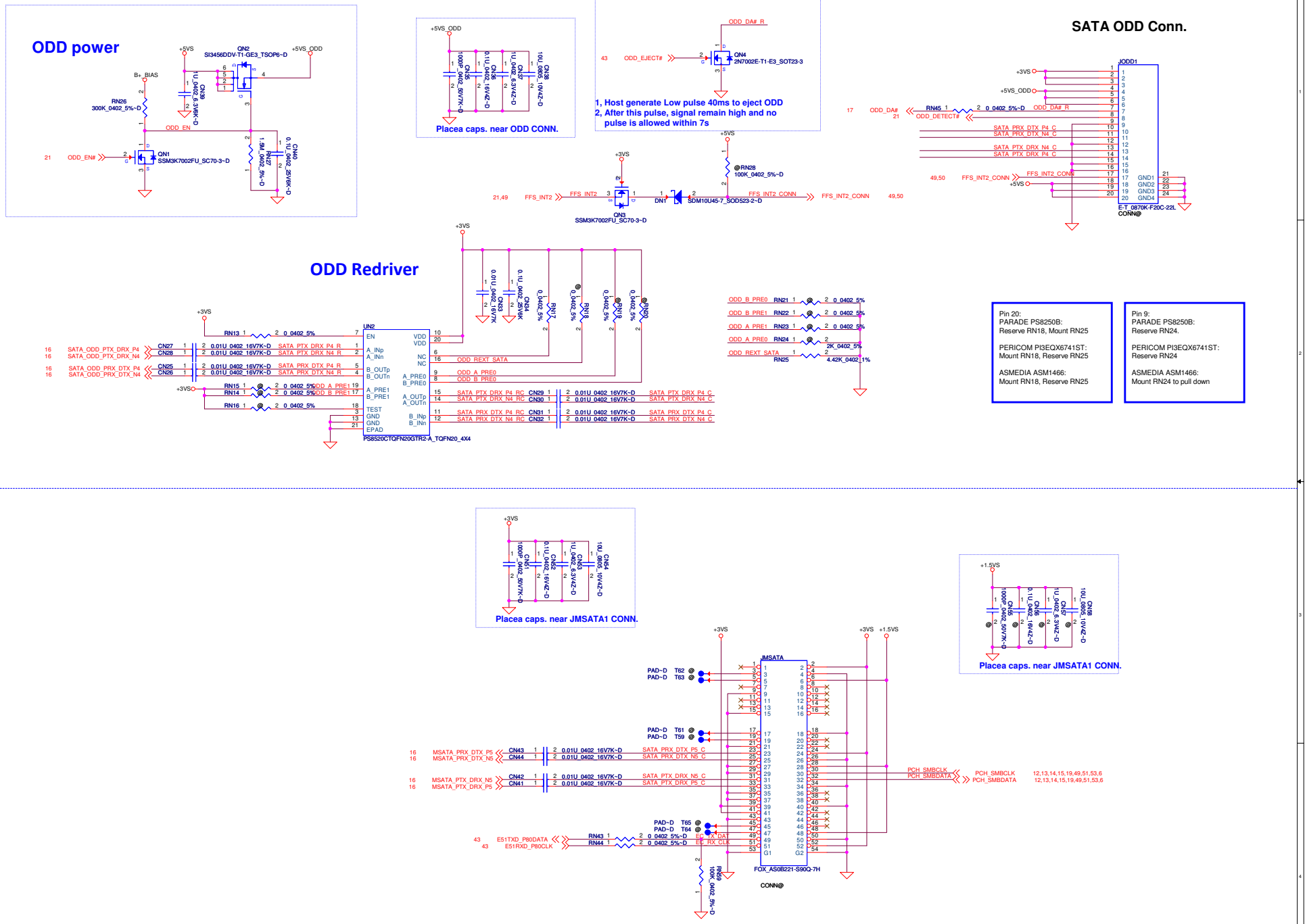
Compal Electronics, Inc.

Title: SATA HDD1 & HDD2/FFS

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 49 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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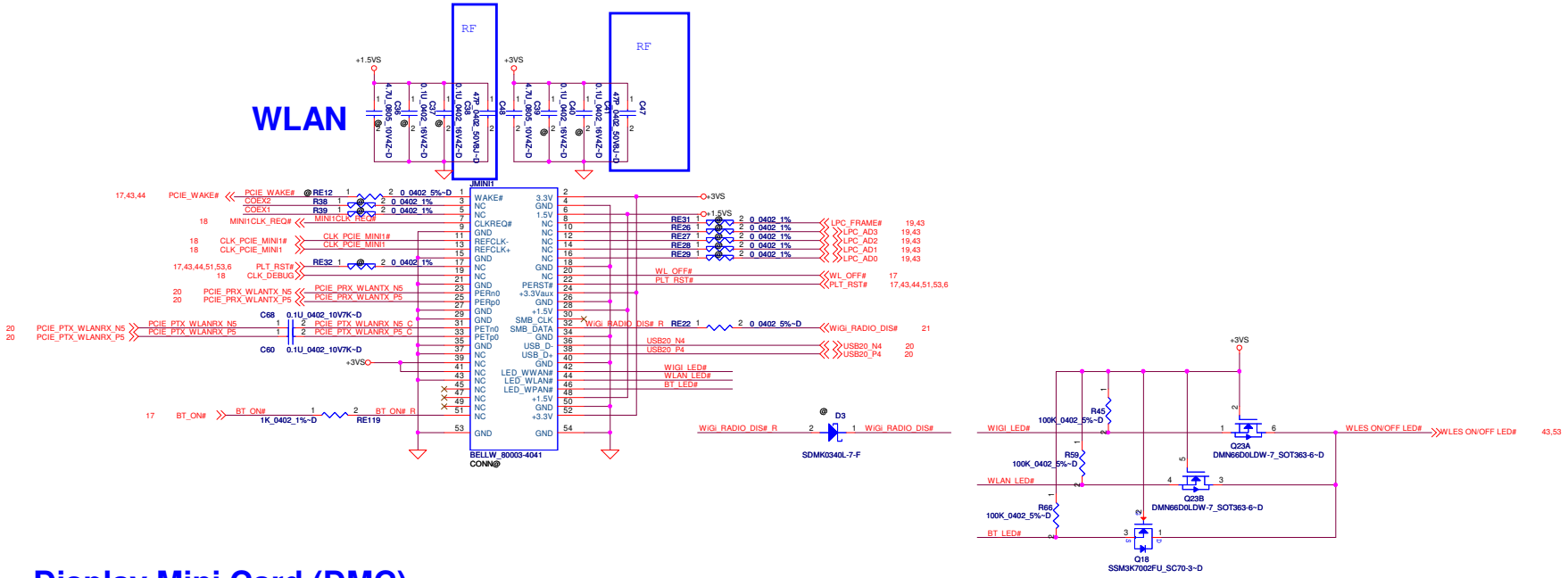
Compal Electronics, Inc.

Title: SATA ODD/mSATA

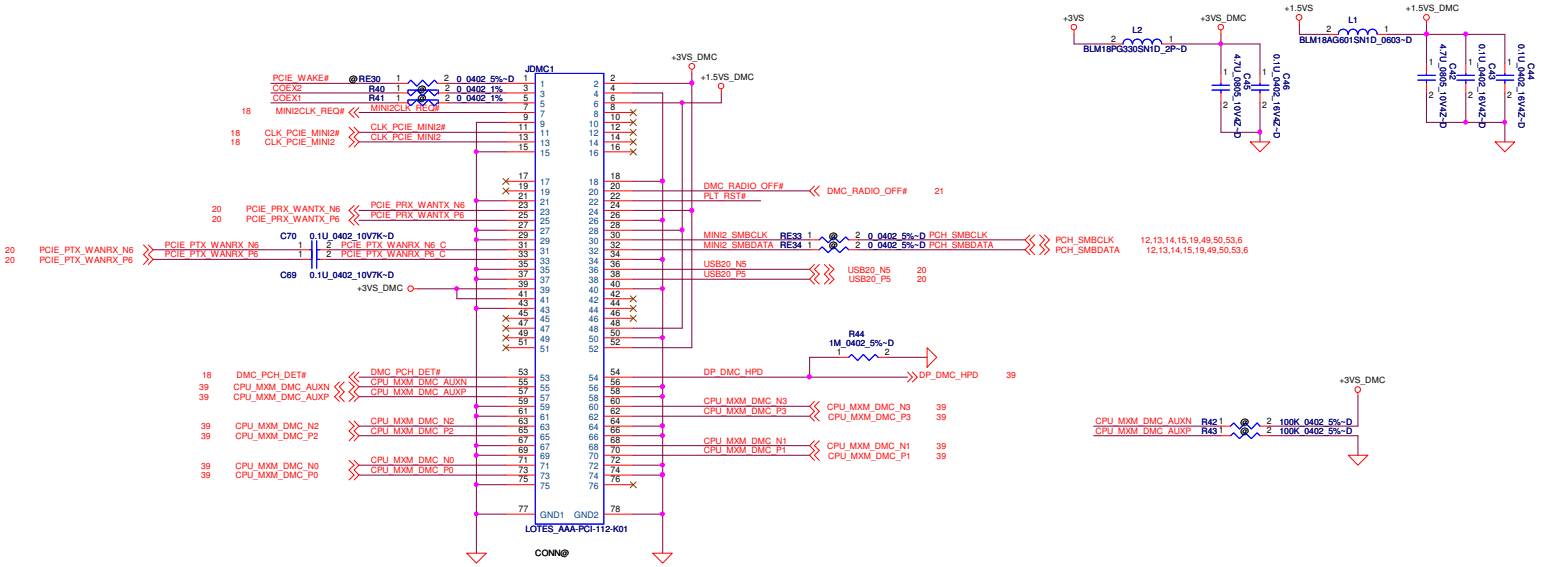
Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 50 of 56

WLAN



Display Mini Card (DMC)



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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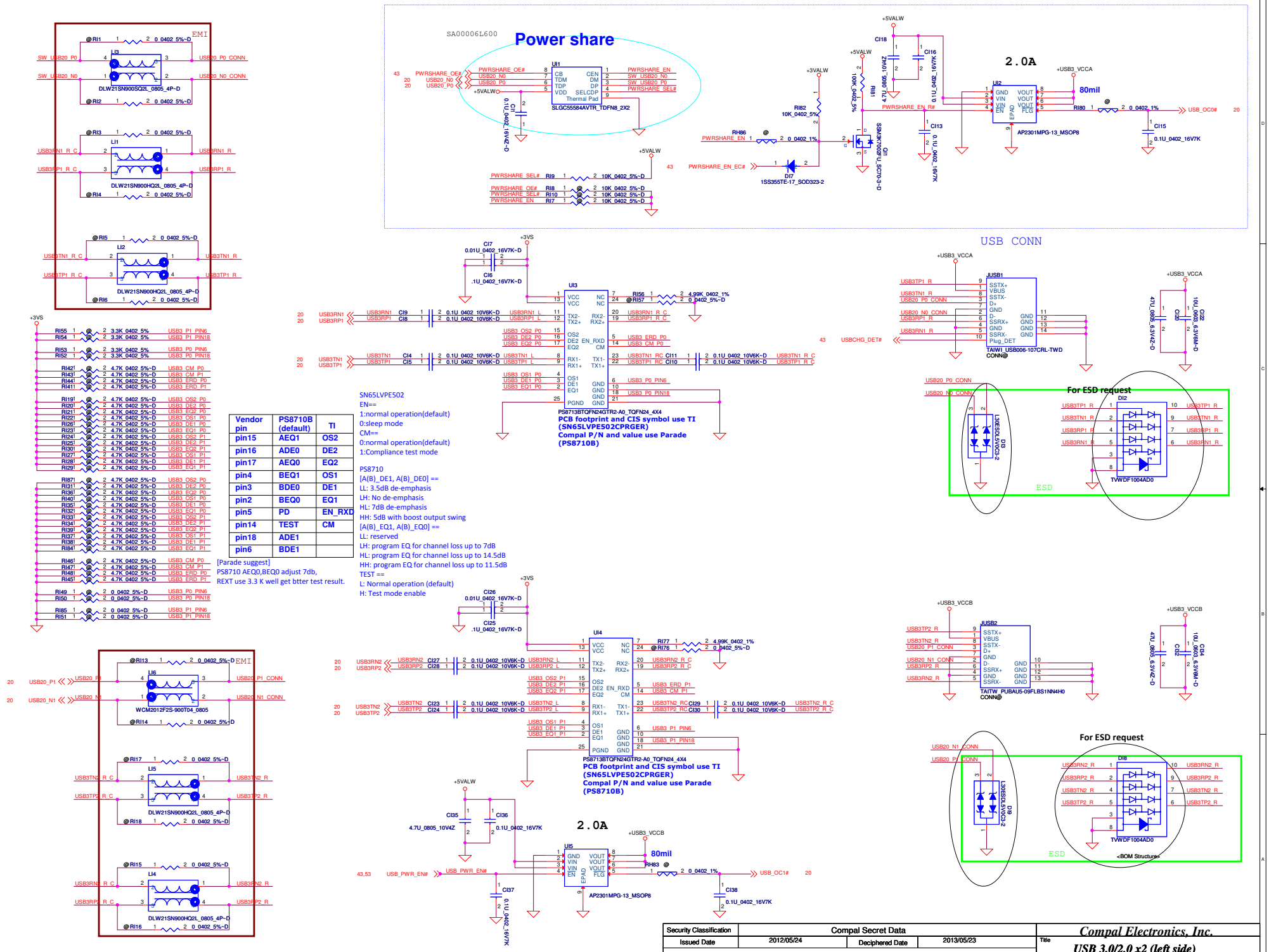
Compal Electronics, Inc.

Title: *Mini Card -WLAN/DMC/BT*

Size: Custom | Document Number: *LA-9332P* | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 51 of 56



Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

Security Classification	Compal Secret Data		
Issued Date	2012/05/24	Deciphered Date	2013/05/23

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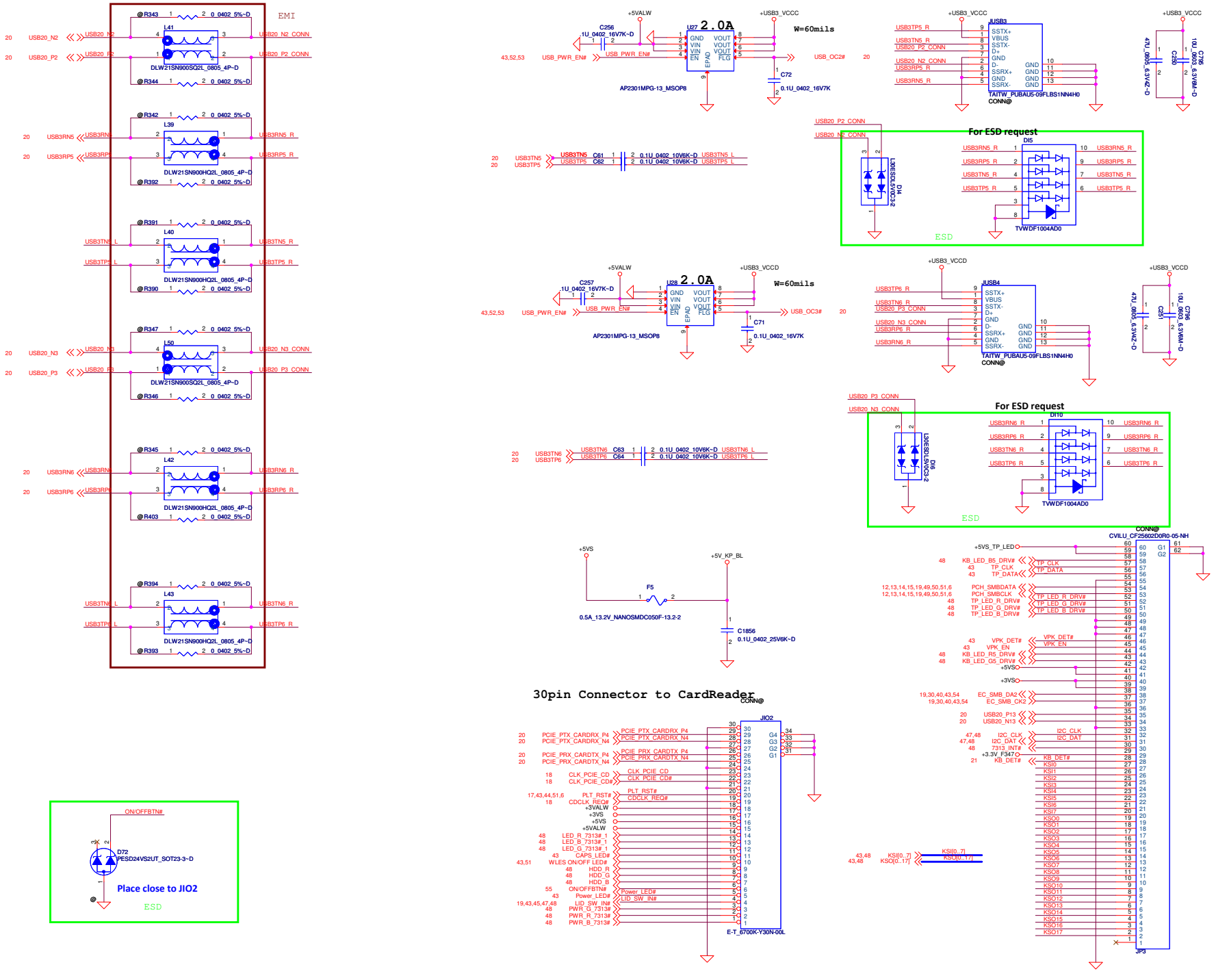
Compal Electronics, Inc.

Title: USB 3.0/2.0 x2 (left side)

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 52 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/02/28	Deciphered Date	2013/02/27

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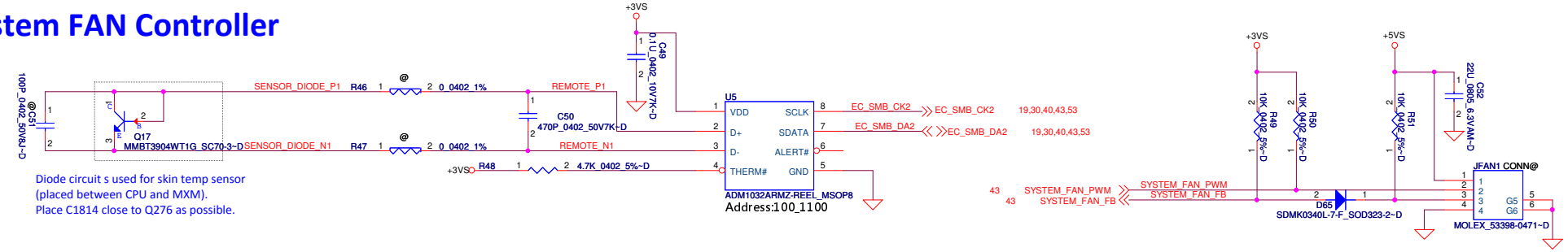
Compal Electronics, Inc.

Title: IO BTB CONN

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 53 of 56

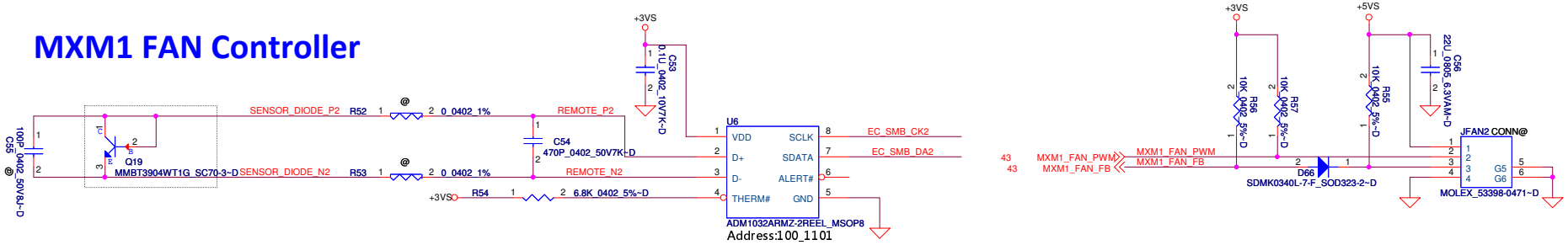
System FAN Controller



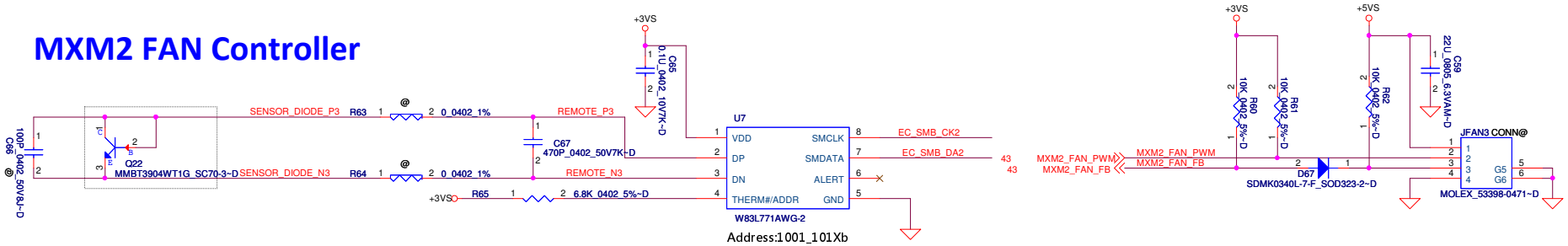
Diode circuit s used for skin temp sensor
(placed between CPU and MXM).
Place C1814 close to Q276 as possible.

Pull up resistor on thermtrip pin	SMBUS address
4.7k	1111
6.8k	1011
10k	1001
15k	1101
22k	0011
33k	0111

MXM1 FAN Controller



MXM2 FAN Controller



Security Classification	Compal Secret Data		
Issued Date	2012/05/14	Deciphered Date	2013/05/13

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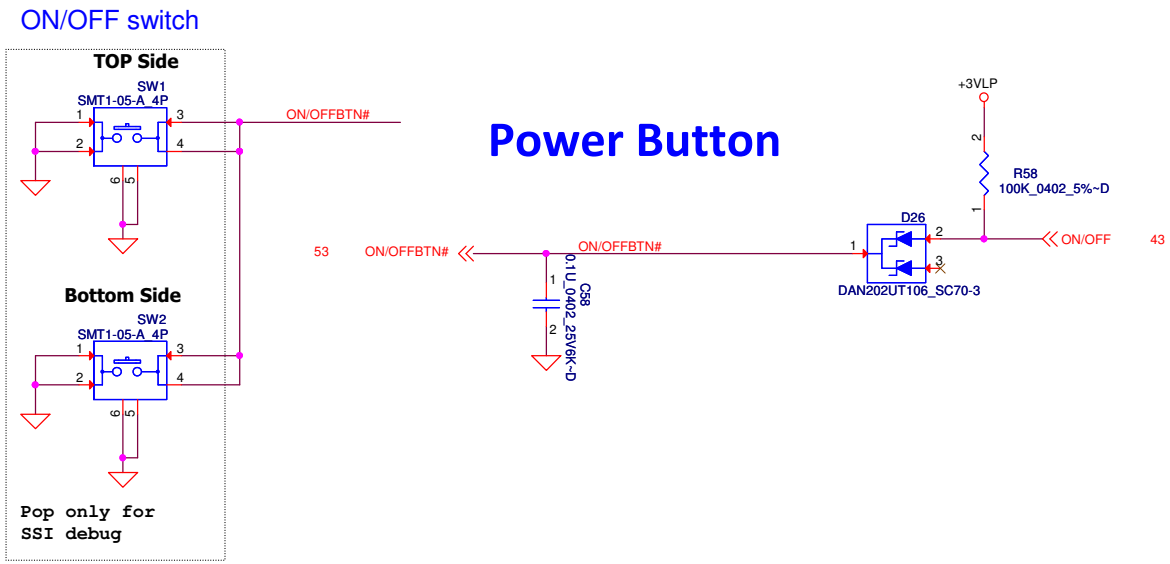
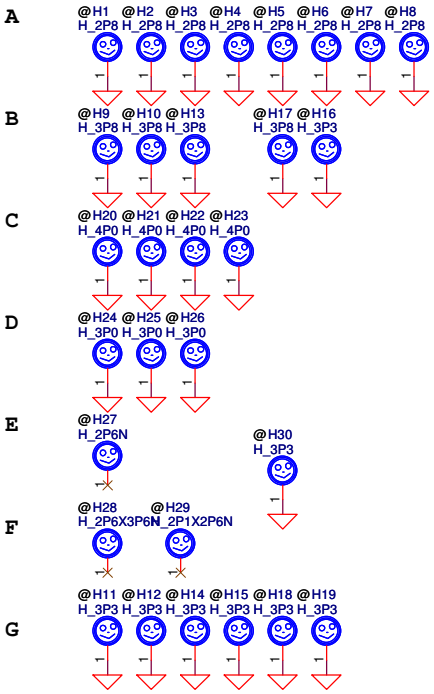
Compal Electronics, Inc.

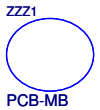
Title: Thermal Sensor & FAN

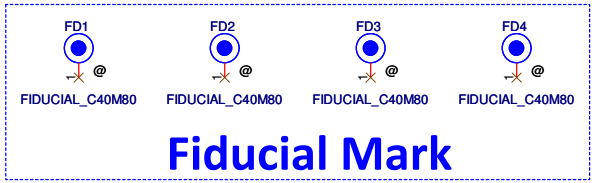
Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 54 of 56









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Issued Date	2012/05/28	Deciphered Date	2013/05/27

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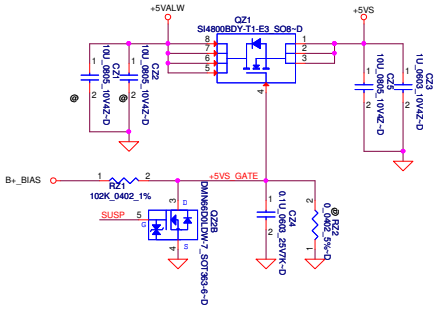
Title: **KB & Power Button & IR**

Size: B | Document Number: LA-9332P | Rev: 0.1

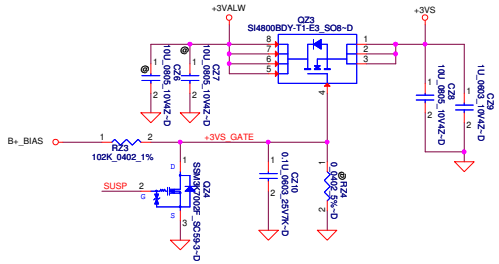
Date: Friday, December 14, 2012 | Sheet 55 of 56

DC to DC

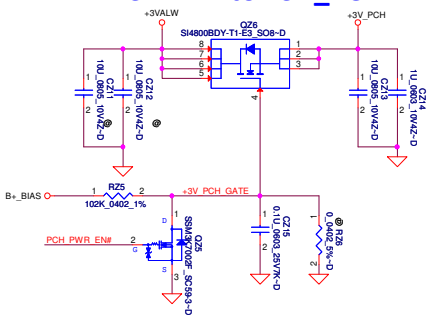
+5VALW to +5VS



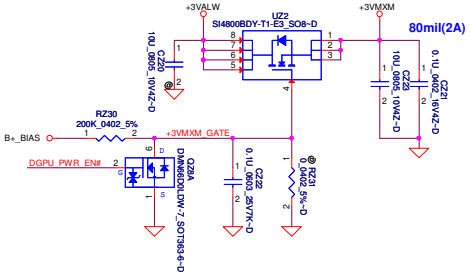
+3VALW to +3VS



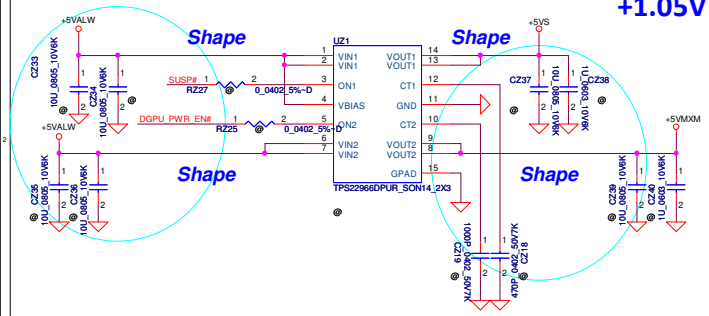
+3VALW to +3V_PCH



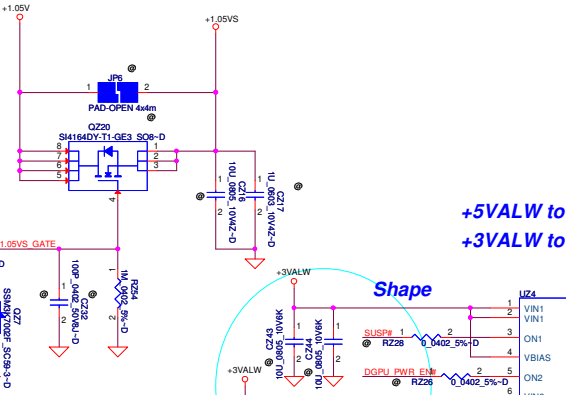
+3VALW to +3VMXM Transfer



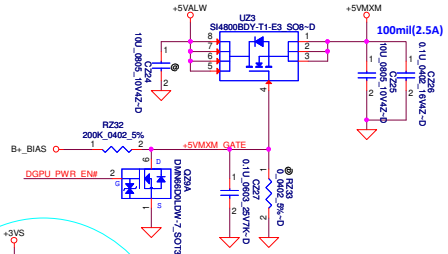
+5VALW to +5VS
+3VALW to +3VS



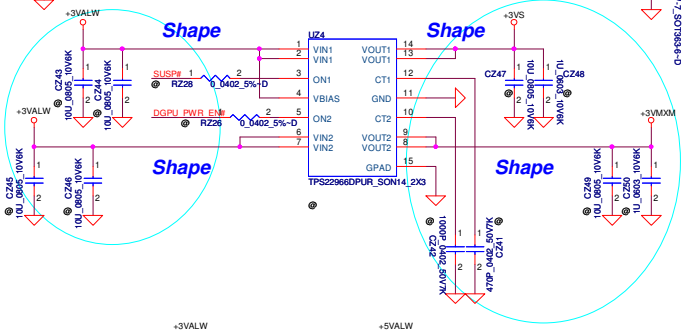
+1.05V to +1.05VS



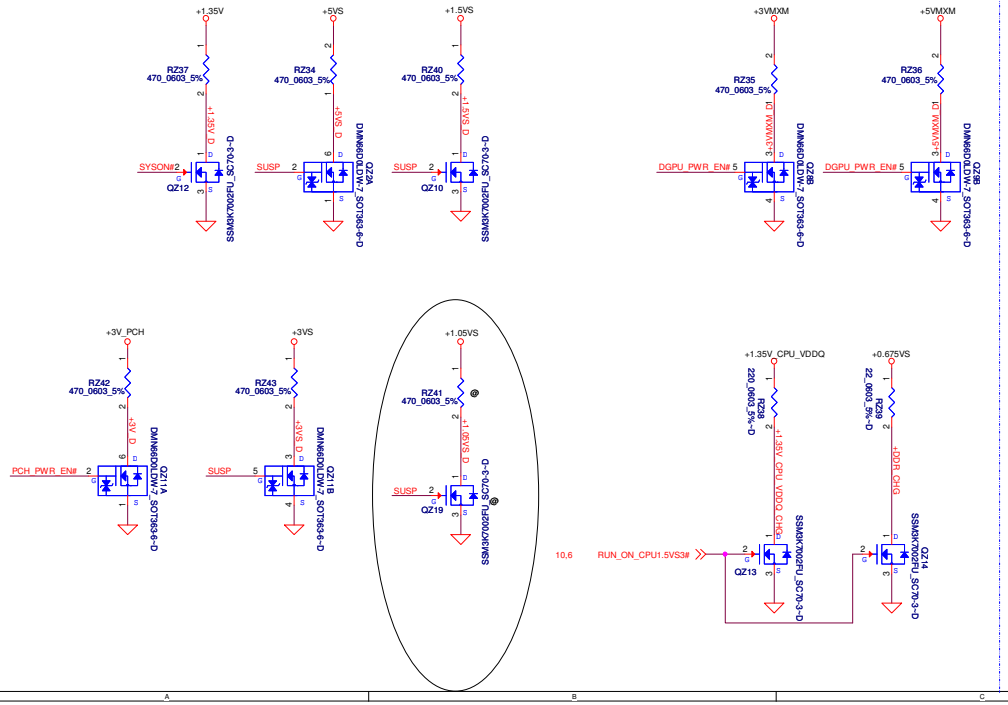
+5VALW to +5VMXM

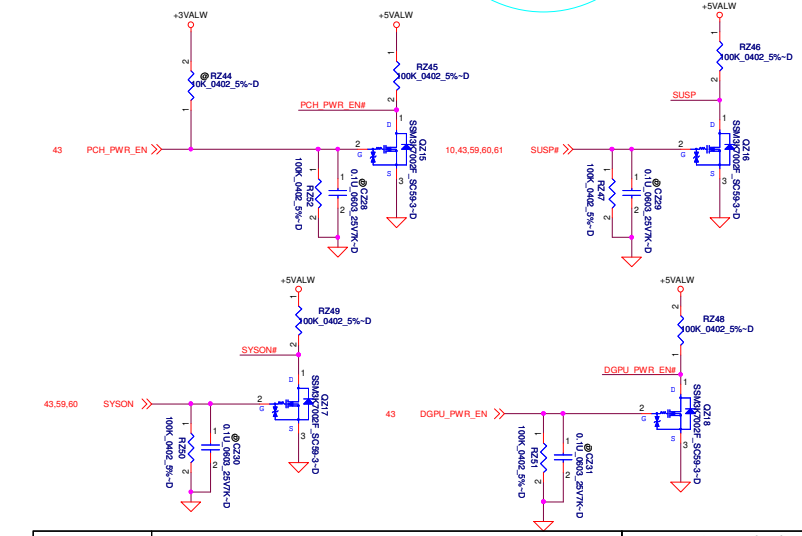


+5VALW to +5VMXM
+3VALW to +3VMXM



Discharge Circuit





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Issued Date	2012/05/28	Deciphered Date	2013/05/27

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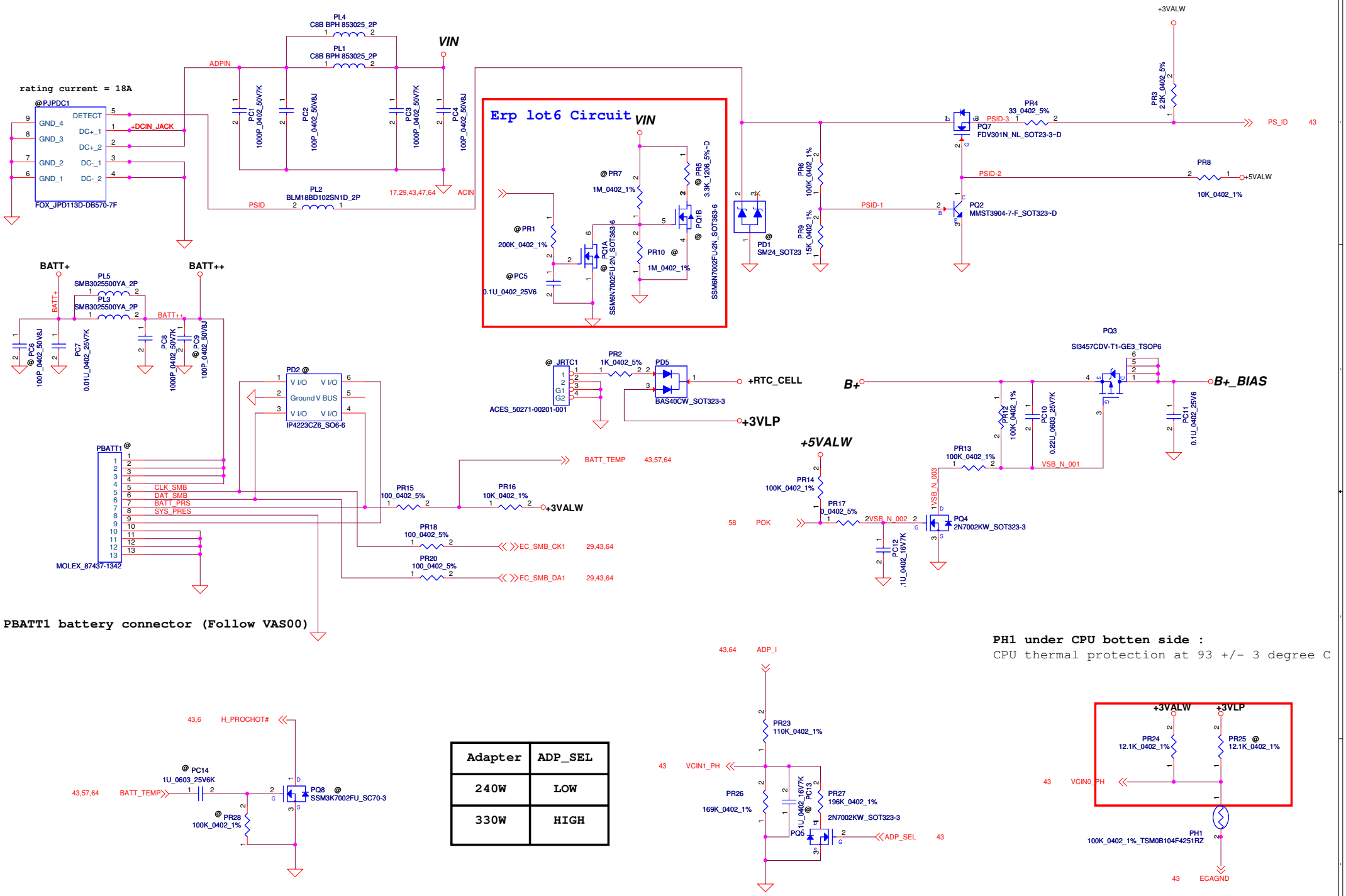
Compal Electronics, Inc.

Title: DC/DC Interface

Size: Custom | Document Number: LA-9332P | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 56 of 56



Adapter	ADP_SEL
240W	LOW
330W	HIGH

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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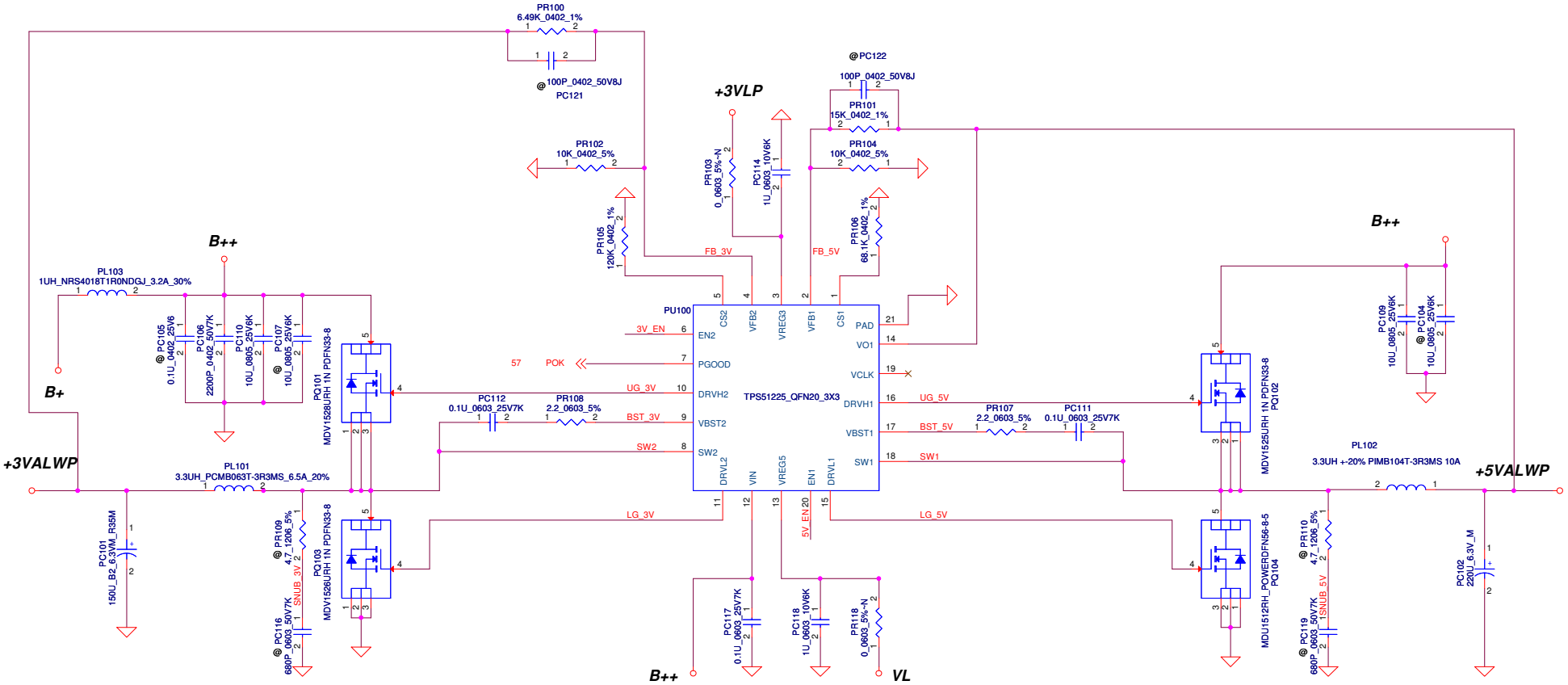
Compal Electronics, Inc.

Title: **PWR-DCIN / BATT CONN / OTP**

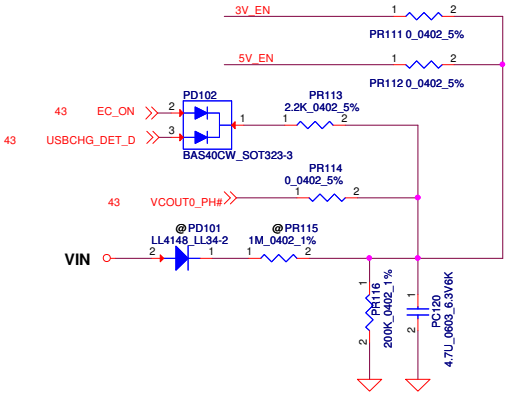
Size: | Document Number: **LA-9332P** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 57 of 66



3VALWP
TDC 6.08A
Peak Current 8.11A
OCP current 9.73A

	TYP		MAX
H/S Rds(on)	11.2mohm	,	14mohm
L/S Rds(on)	3.7mohm	,	5mohm



5VALWP
TDC 11A
Peak Current 16A
OCP current 20A

	TYP		MAX
H/S Rds(on)	11.2mohm	,	14mohm
L/S Rds(on)	3.7mohm	,	5mohm

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Document Number: LA-9332P

Rev: 0.1

Date: Friday, December 14, 2012

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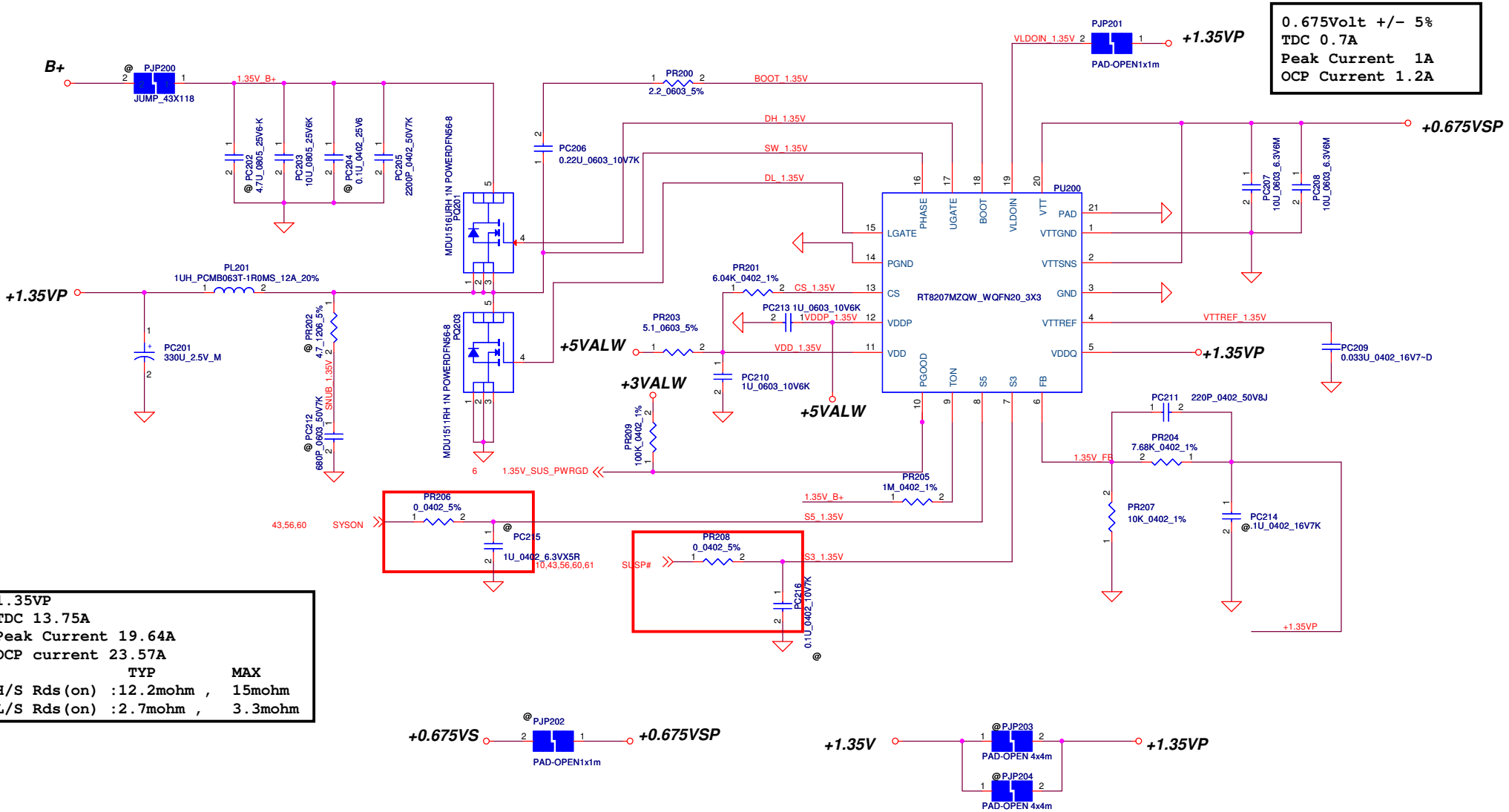

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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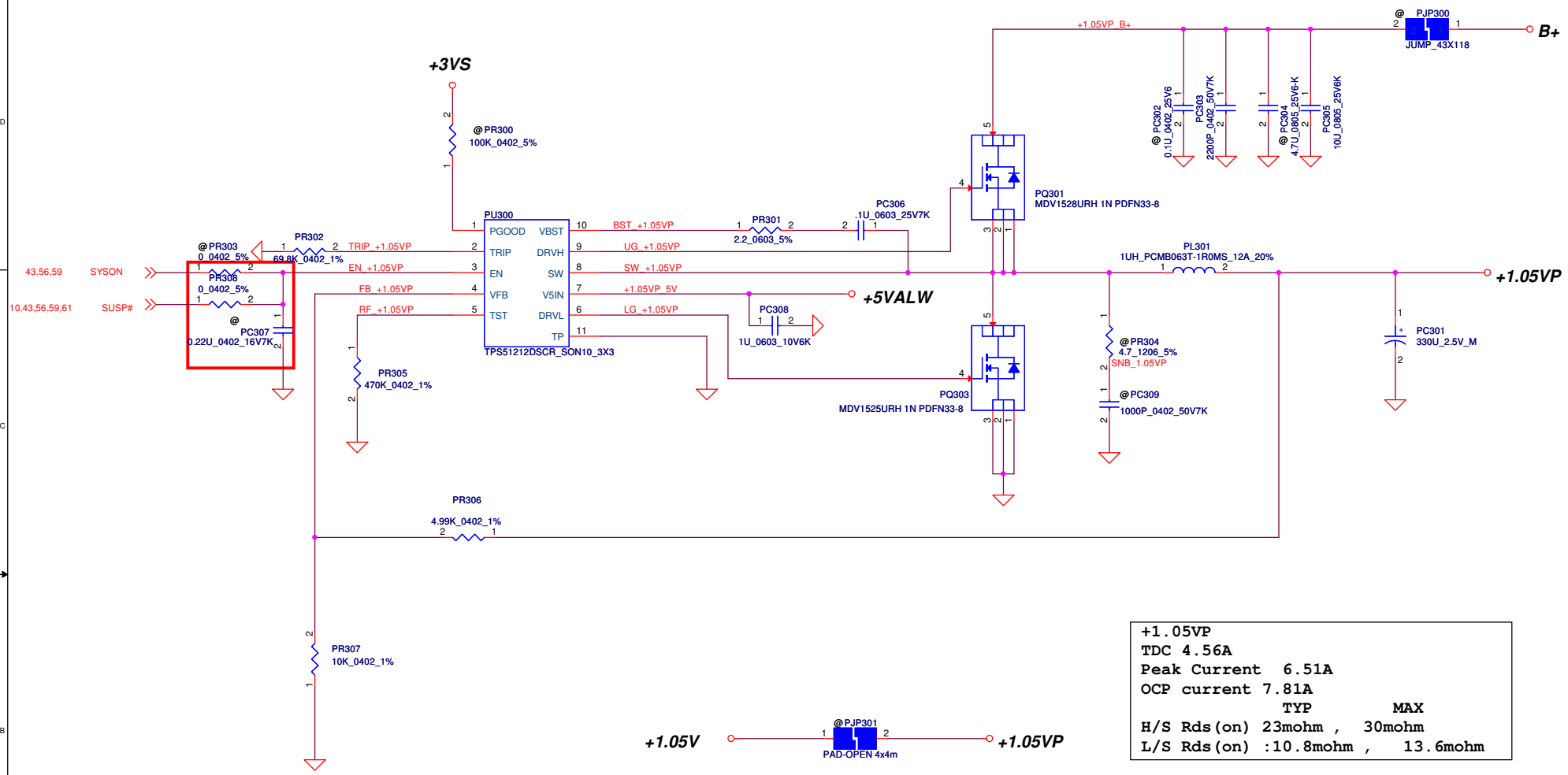
Compal Electronics, Inc.

Title: **PWR-1.35VP/0.675VSP**

Size | Document Number: **LA-9332P** | Rev: 0.1

Date: Friday, December 14, 2012 | Sheet 59 of 66




```
+1.05VP
TDC 4.56A
Peak Current  6.51A
OCP current 7.81A
                TYP          MAX
H/S Rds(on) 23mohm ,   30mohm
L/S Rds(on) :10.8mohm ,    13.6mohm
```

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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Title: **PWR-+1.05VP**

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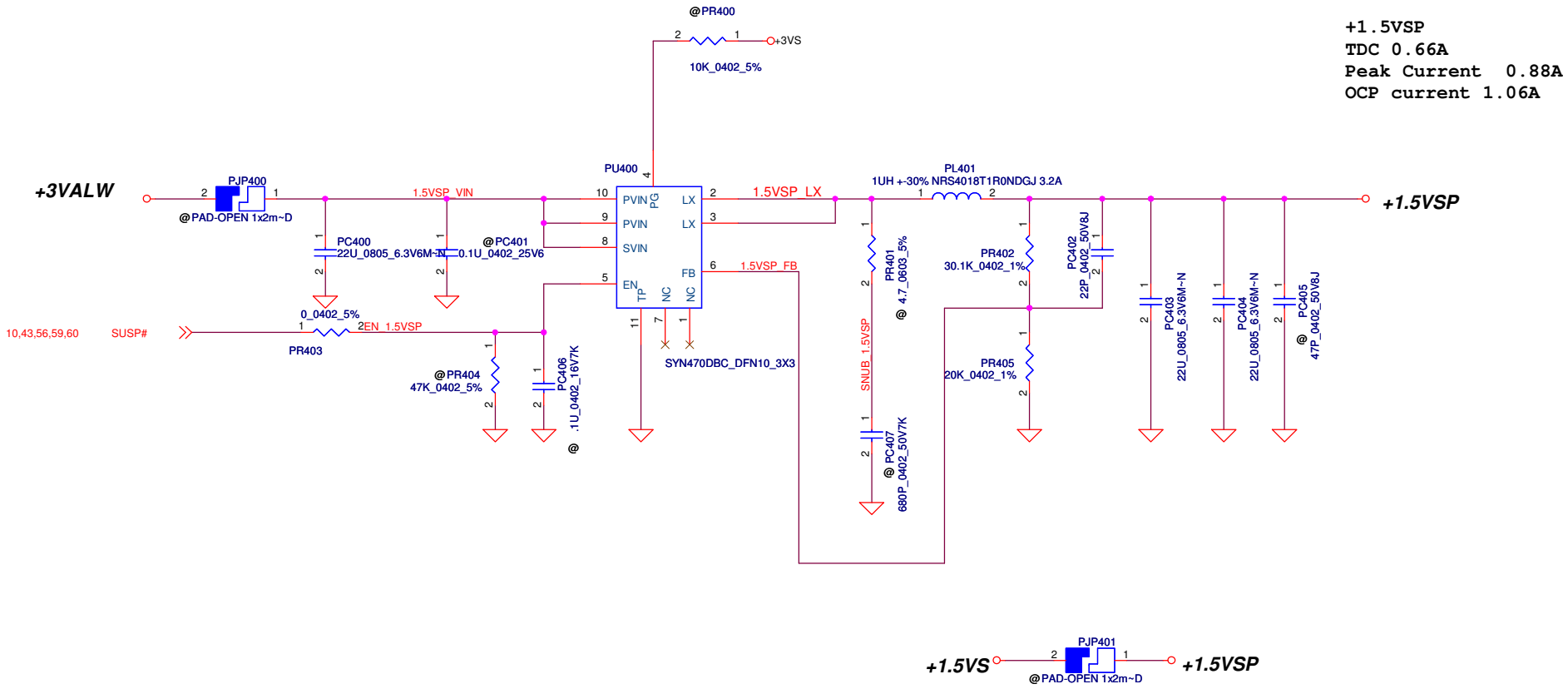
Date: Friday, December 14, 2012 | Sheet 60 of 66



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Issued Date	2012/05/28	Deciphered Date	2013/05/27	Title: PWR-1.5VSP
				Size / Document Number: LA-9332P / Rev: 0.1
				Date: Friday, December 14, 2012 / Sheet 61 of 66

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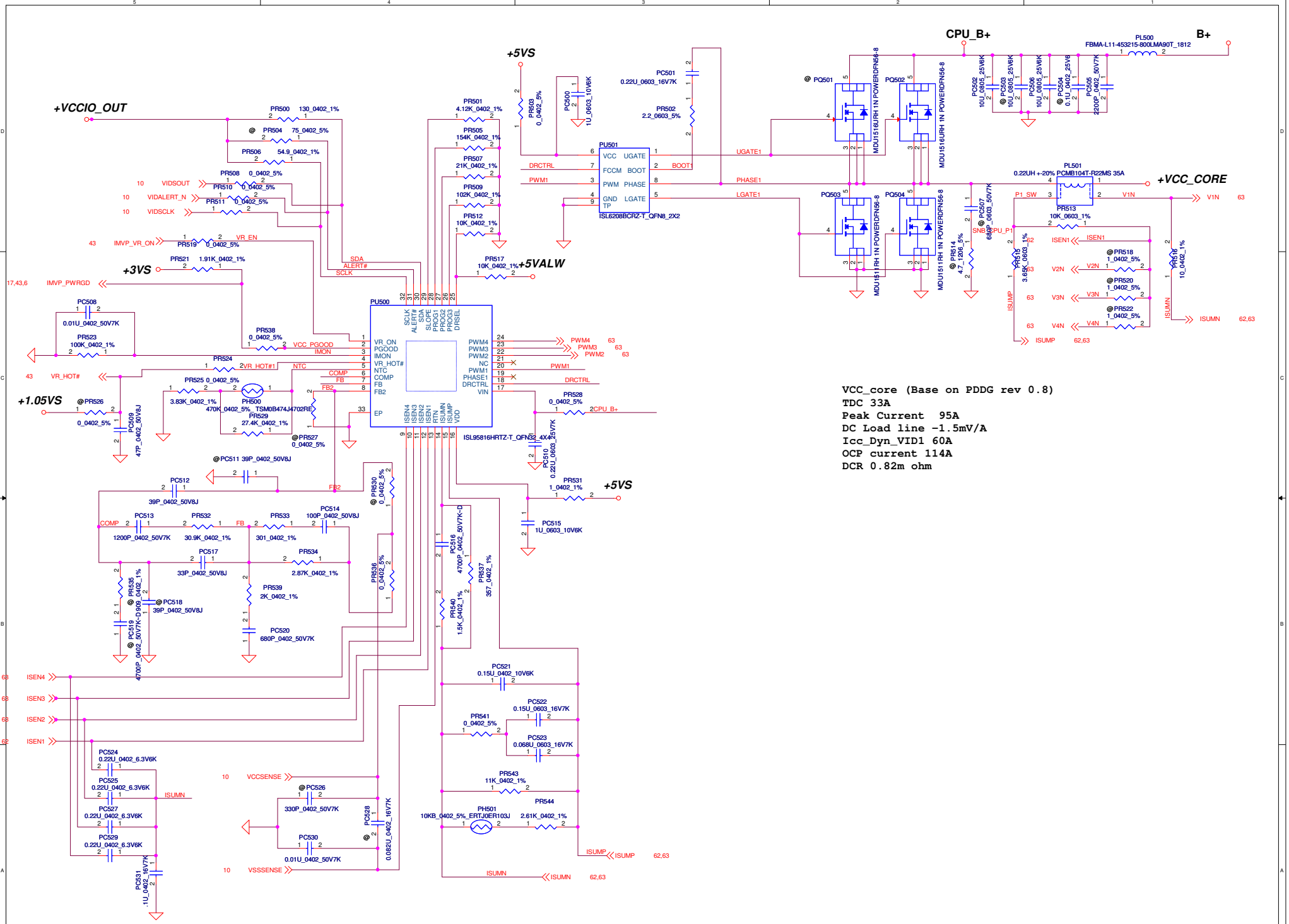

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Issued Date	2012/05/28	Deciphered Date	2013/05/27

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Title: **PWR_VCORE_ISL95816**

Size | Document Number: **LA-9332P** | Rev: 0.1

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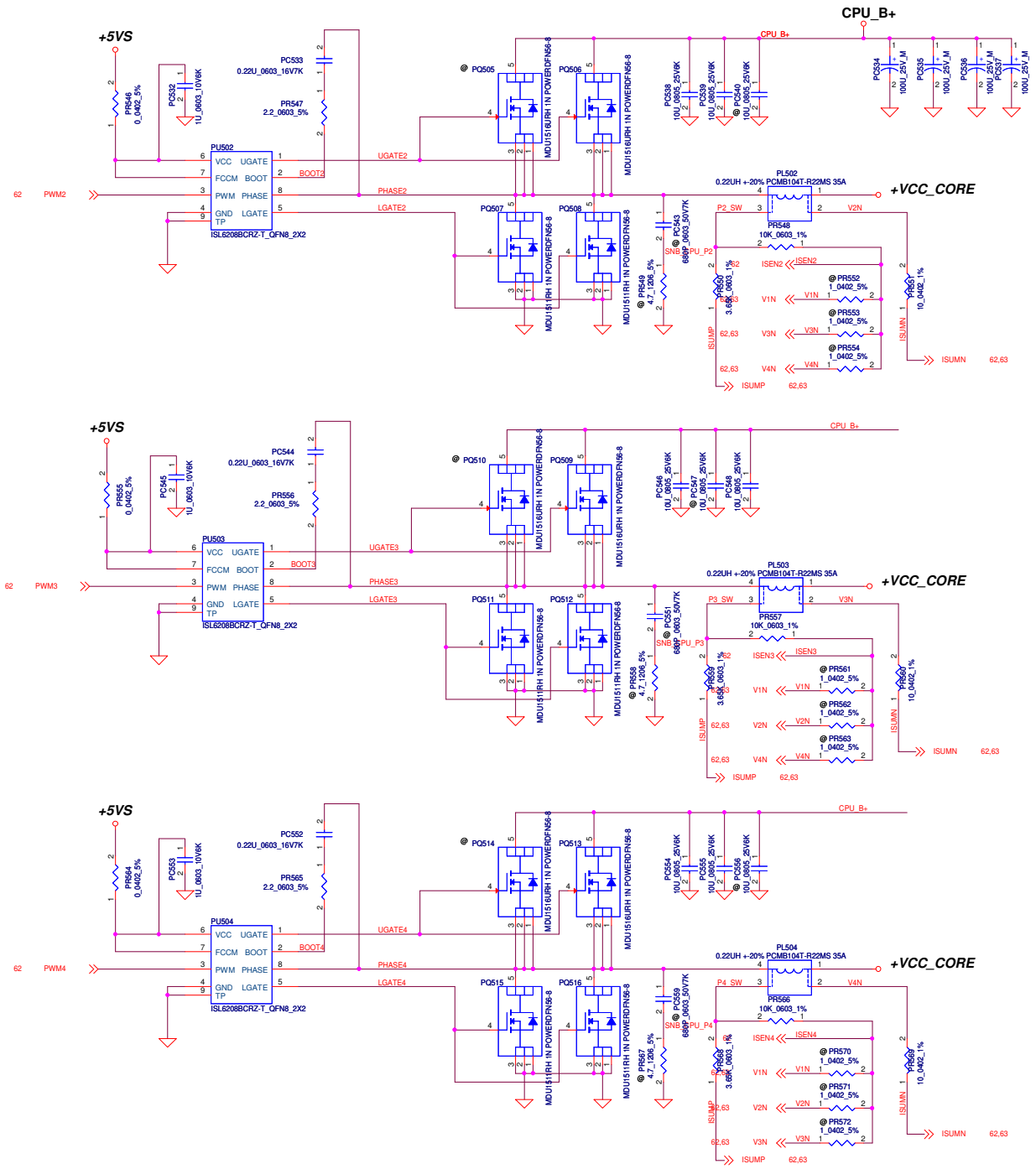

Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

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Compal Electronics, Inc.

Title: **PWR_VCORE_ISL6208**

Size: | Document Number: **LA-9332P** | Rev: 0.1

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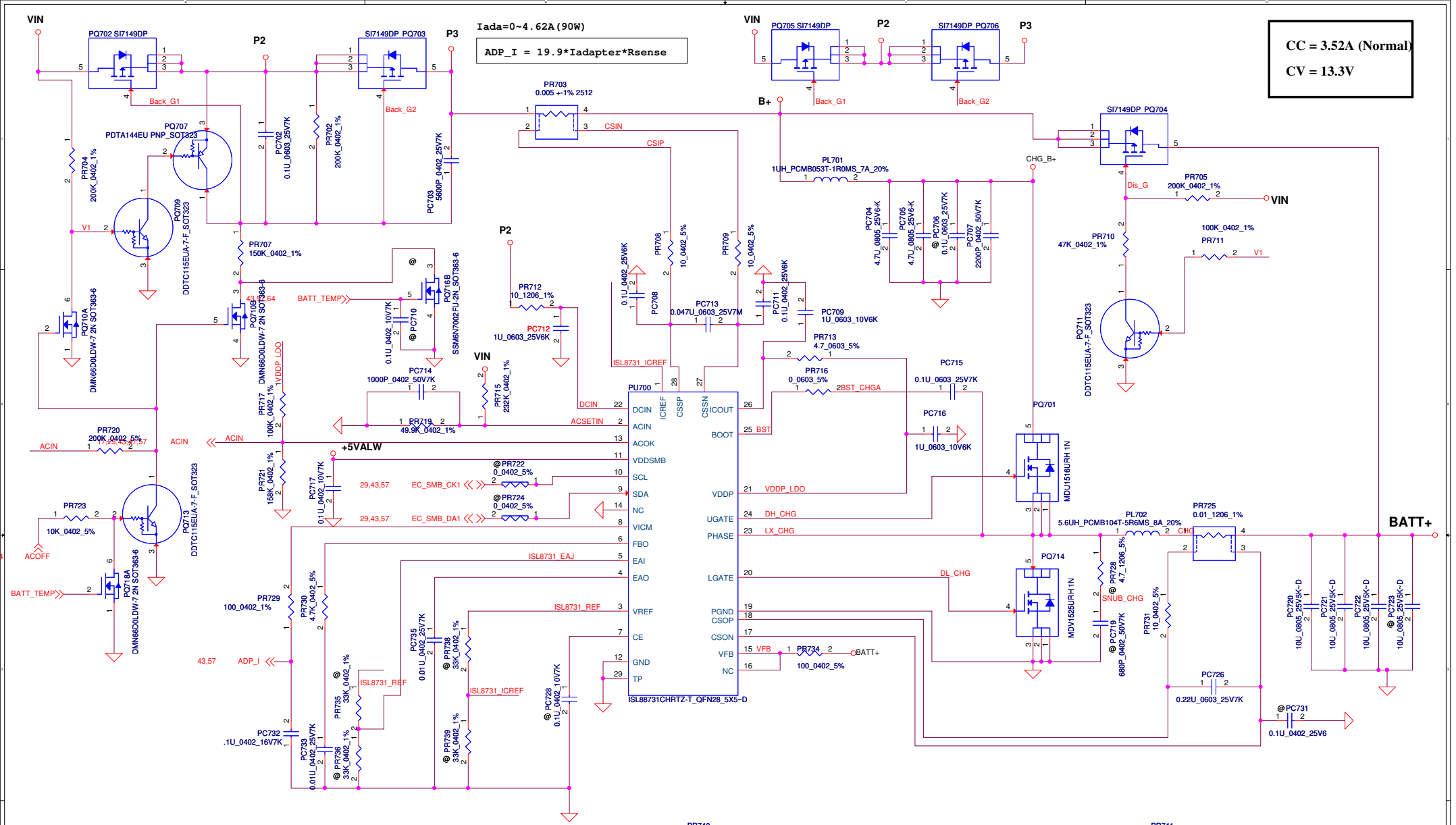

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Compal Electronics, Inc.

Title: **PWR-Charger**

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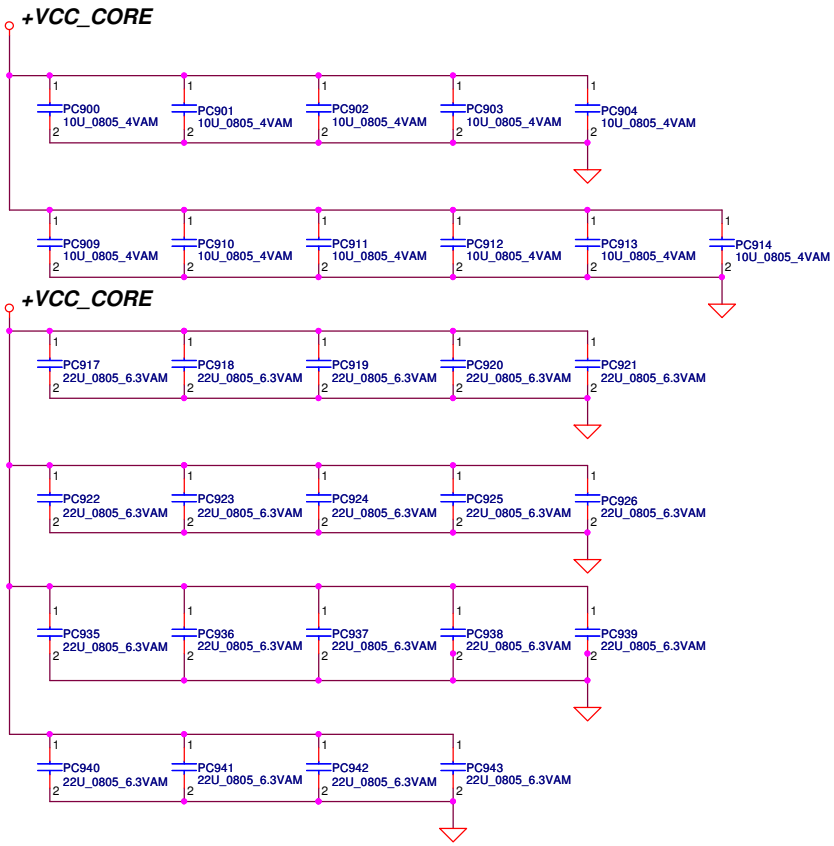
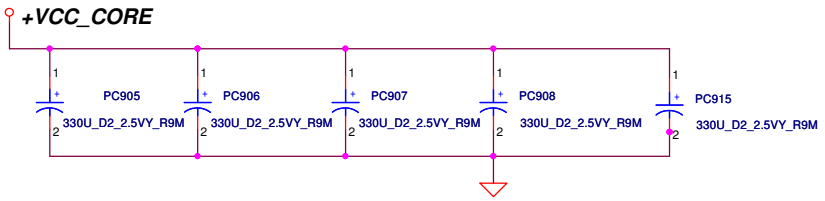
Based on PDDG rev 0.8 Table 5-1.





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Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

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Version change list (P.I.R. List)

Item	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Adjust 1.5V output volatge		P61	change PR402 to 30.1K_0402_1% PR405 to 20K_0402_1%	2012.7.30	SSI
2	Adjust 3.3V OCP seeting		P58	change PR105 to 120K_0402_1%.	2012.7.30	SSI
3	Adjust 3V/5V always OTP seeting		P58	modify PD100 to PR114 0_0402_1%.	2012.7.30	SSI
4	Adjust Vcore OTP seeting		P62	PR531 connect to +5VS	2012.7.30	SSI
5	Add PD3 PD4 for EMD requirement		P57	add PD3 PD4 to PESD24VS2UT_SOT23-3	2012.8.16	SSI
6	hiccup mode issue is not happen so we haven't need solution.		P57	remove Erp lot6 Circuit	2012.8.16	SSI
7	change diode for EMI requirement		P57	use PD2 (6 PIN) to combine combine PD3(2PIN) PD4(2PIN).	2012.8.31	SSI
8	adjust the component for the 88731 schematic		P64	change PR722 and PR724 to short footprint remove PR701 PR706 PC701 PC734 PR732	2012.9.10	SSI
9	adjust RTC circuit for safety concern		P57	add PR2 1K_0402_5%	2012.9.10	SSI
10	change ACIN bead for current limit rating		P57	change PL1 PL4 to C8B BPH 853025_2P	2012.9.10	SSI
11	add PR116 for 3v 5v_EN delay time solution		P58	add PR116 402K_0402_1%	2012.9.18	SSI
12	change output choke to improve efficiency		P59	change PL201 to 1UH_PCMC063T-1R0MN	2012.9.18	SSI
13	change PR500 value to meet INTEL SPEC.		P62	change PR500 to 130_0402_1%~D	2012.10.4	SSI
			P67			
14						
15						
16						
17						

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Title: PWR_PIR 1

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