

QIQY6

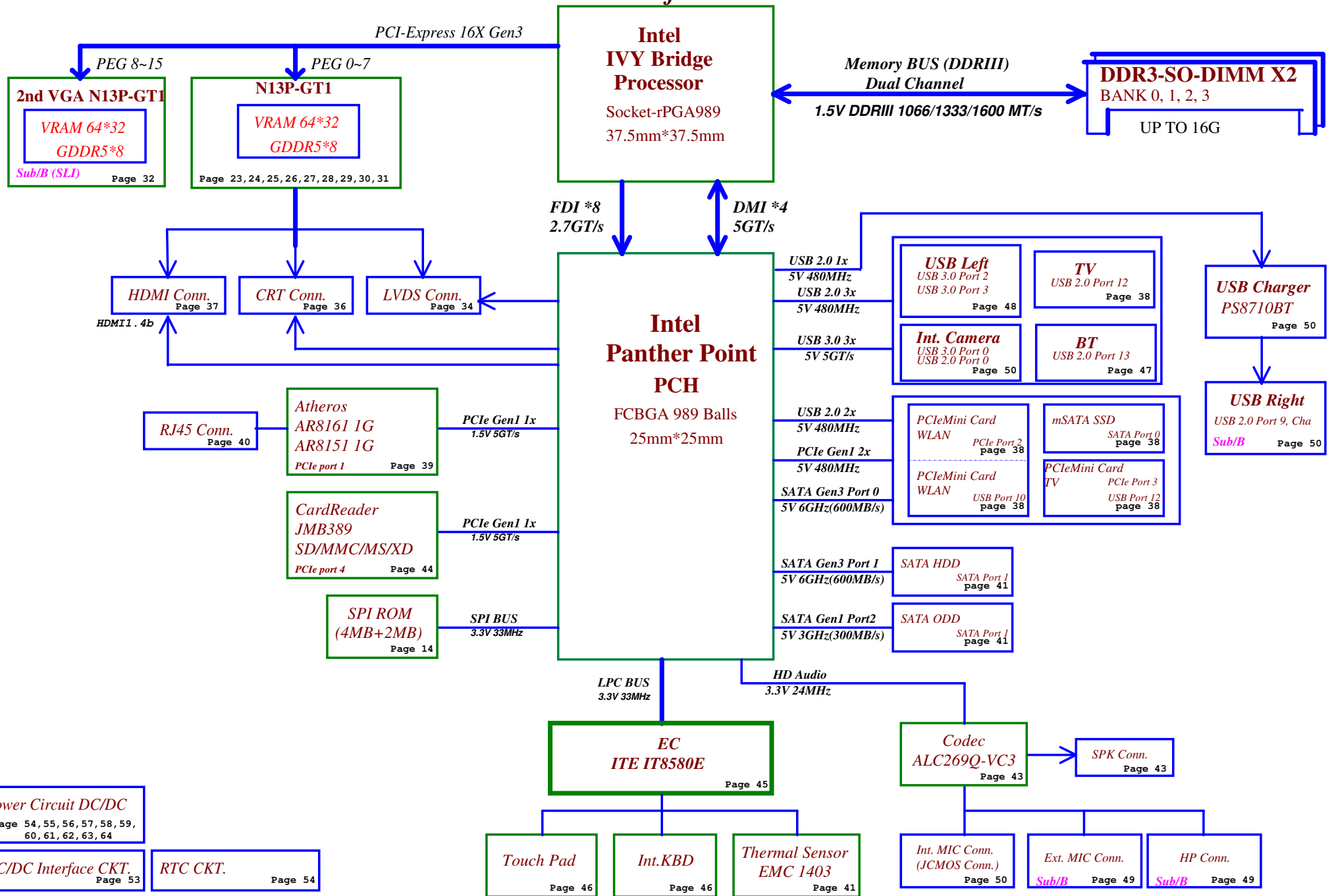
Brandy3.0 (Y500)

LA-8692P Rev0.2 Schematic

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT-1 + 2nd VGA N13P GT-1
2012-02-05 Rev0.2

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Chief River



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power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI	0	Camera Camera
		1	
		2	USB Port (Left Side)
		3	USB Port (Left Side)
		4	USB Port (Left Side)
		4	
		5	
		6	
EHCI2		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	Mini Card(TV)
		13	Blue Tooth

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	IT8580E +3VALW	X	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	V +3VS	X	V +3VS	X	X	V +3VS	X

Device	Address	Device	Address
Smart Battery	0001_011X b	Thermal Sensor EMC1403-2	1001_101xb
		Master VGA	0x9E
		Slave VGA	0x9C

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	



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Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	GPIO16
GPIO17	IN	N/A	GPIO17
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	GPIO19

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

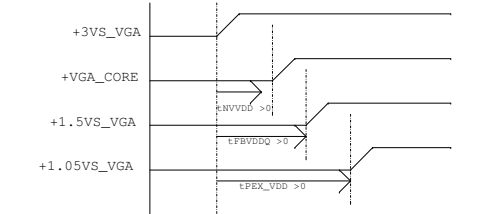
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

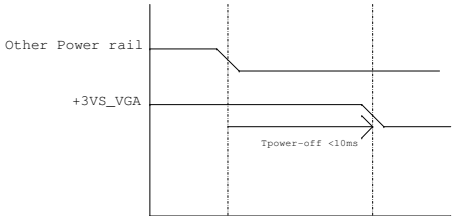
	Device ID		setting	I2C Slave addresses ID
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	PU 25K GC6@					PU 5K SLI@	
	PU 10K	PU 5K OPT@, SLI@	PU 45K	PD 5K	PD 10K	PD 5K OPT@	PD 45K

GPU	N13P-GT		
FB Memory (GDDR5)	ROM_SI		
Samsung 2500MHz	K4G10325FD-FC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24AFR-T2C		
	64Mx32	PD 25K	



1. all power rail ramp up time should be larger than 40us

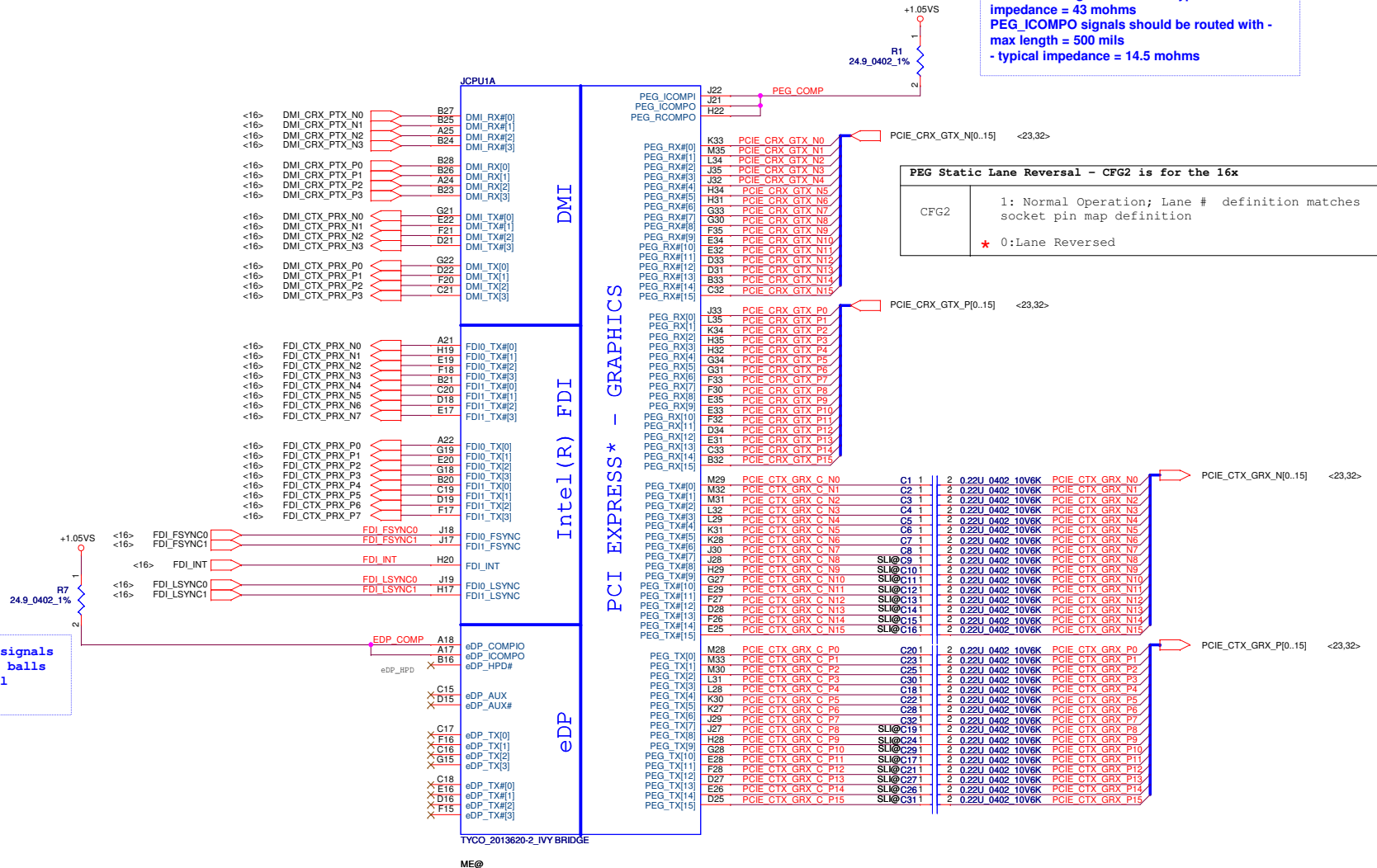


1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

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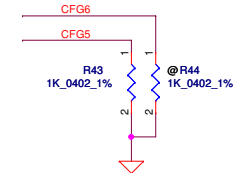
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



A schematic diagram showing a resistor labeled R41 with a value of 1K_0402_1%. The resistor is connected between a signal line labeled CFG2 and a ground symbol (a triangle pointing down). The connection points are labeled 1 and 2.

Display Port Presence Strap	
CFG4	★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

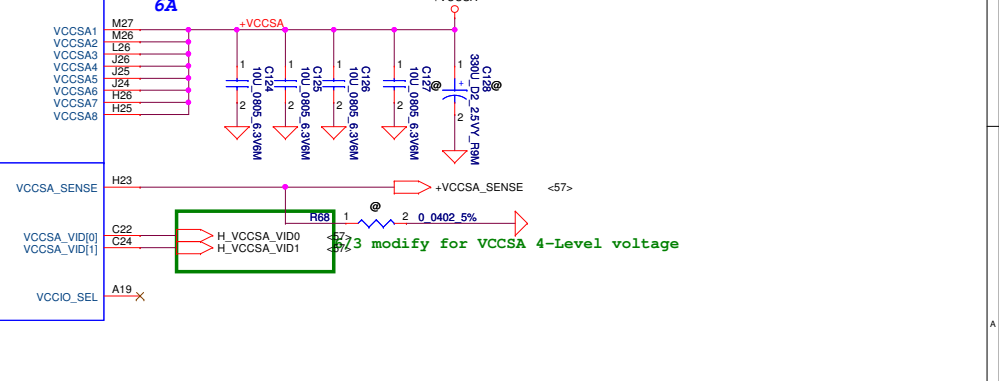
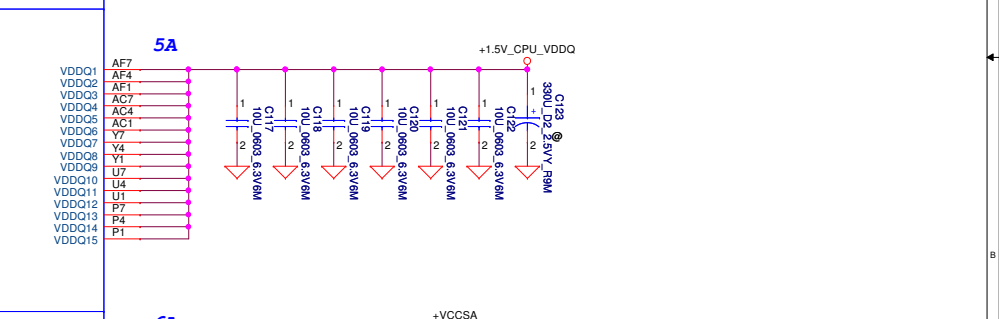
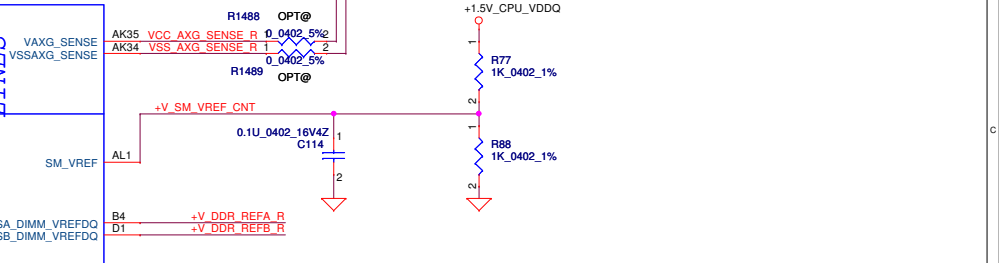
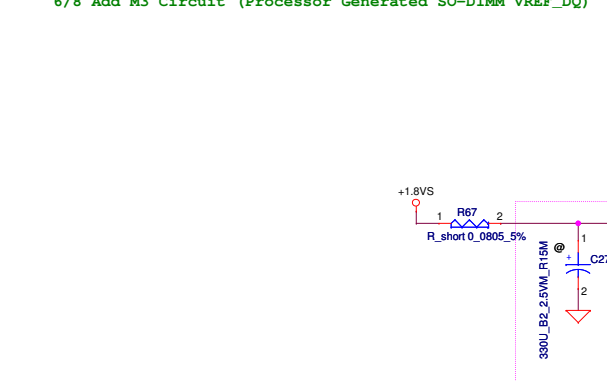
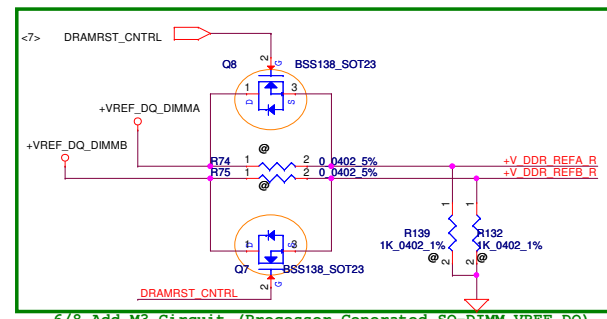
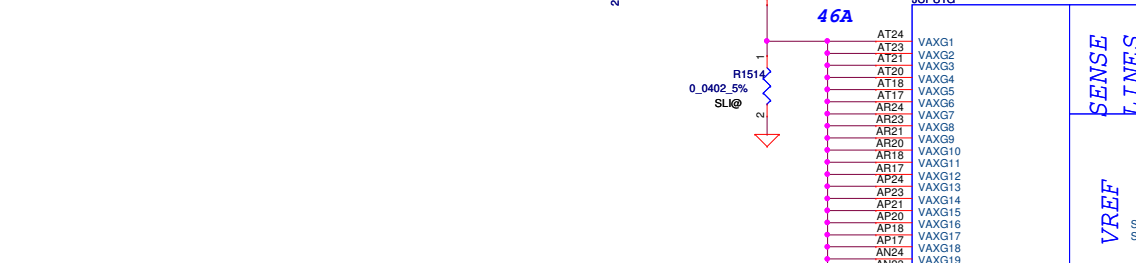
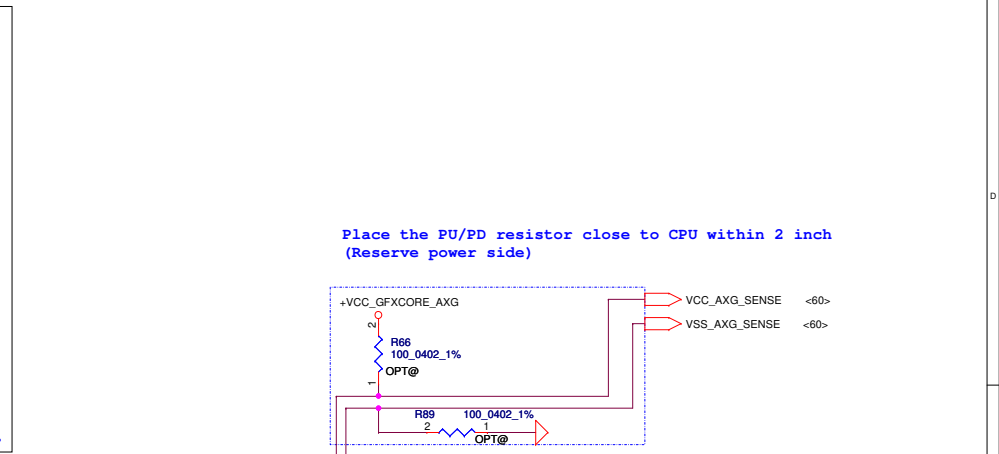
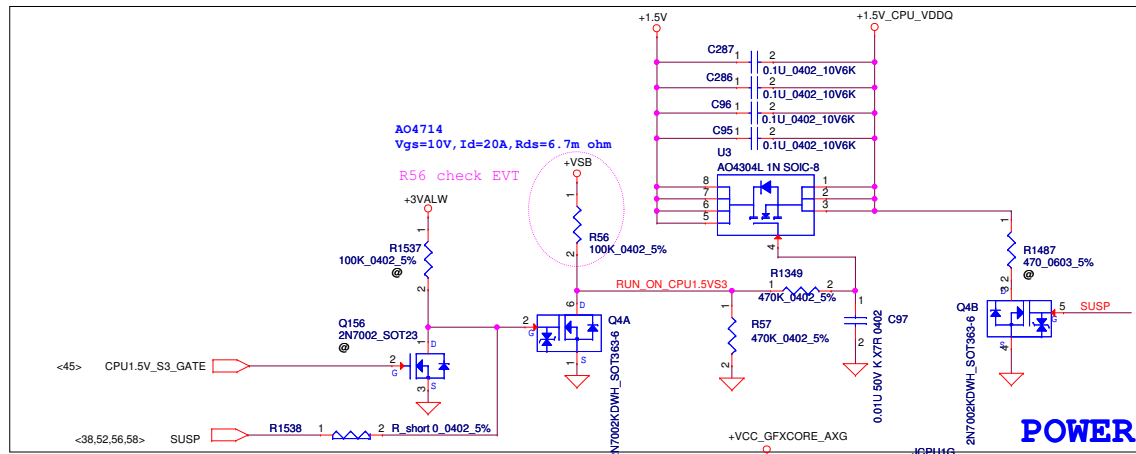


11/24 Intel recommend to reserve test point

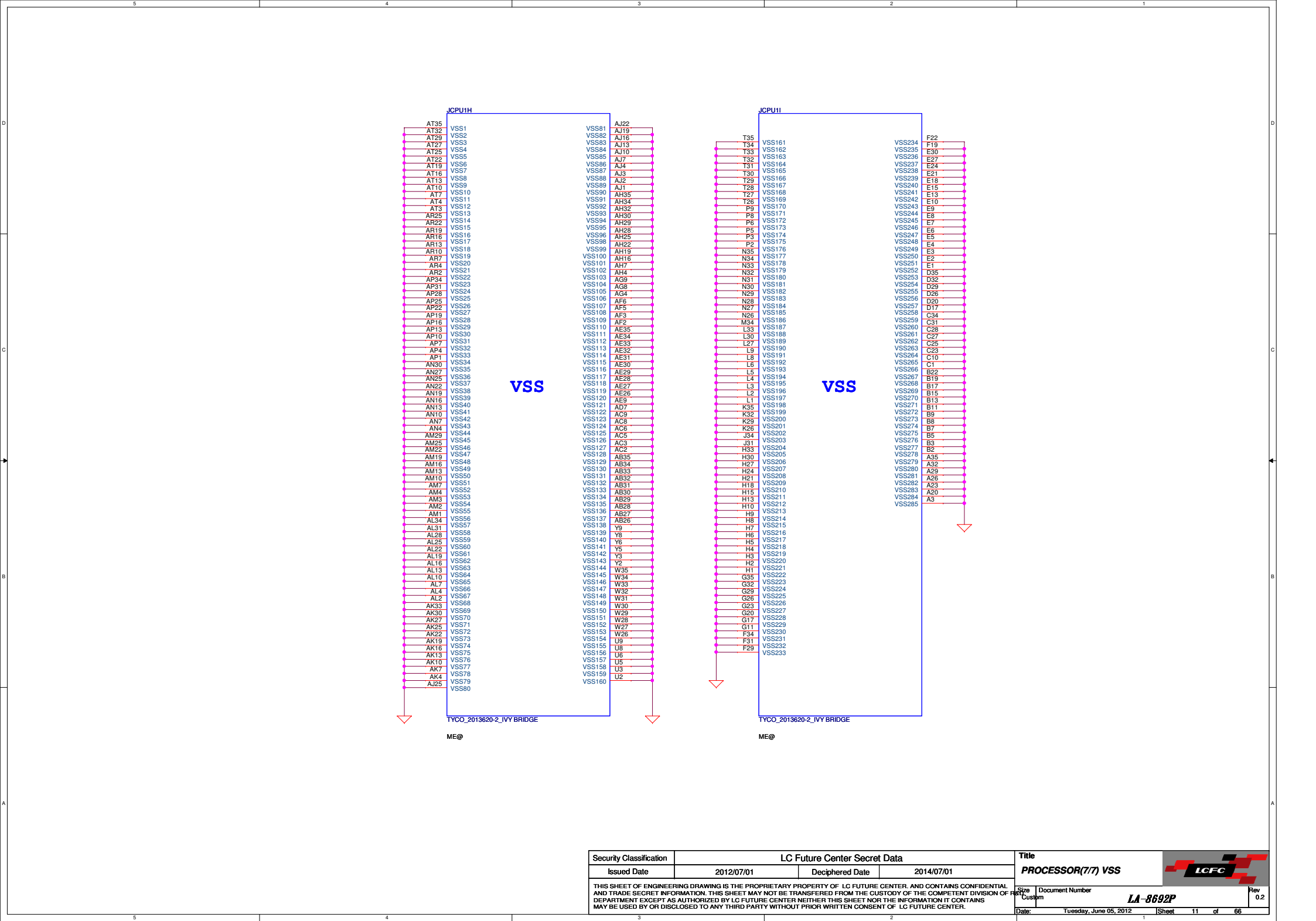
KEY

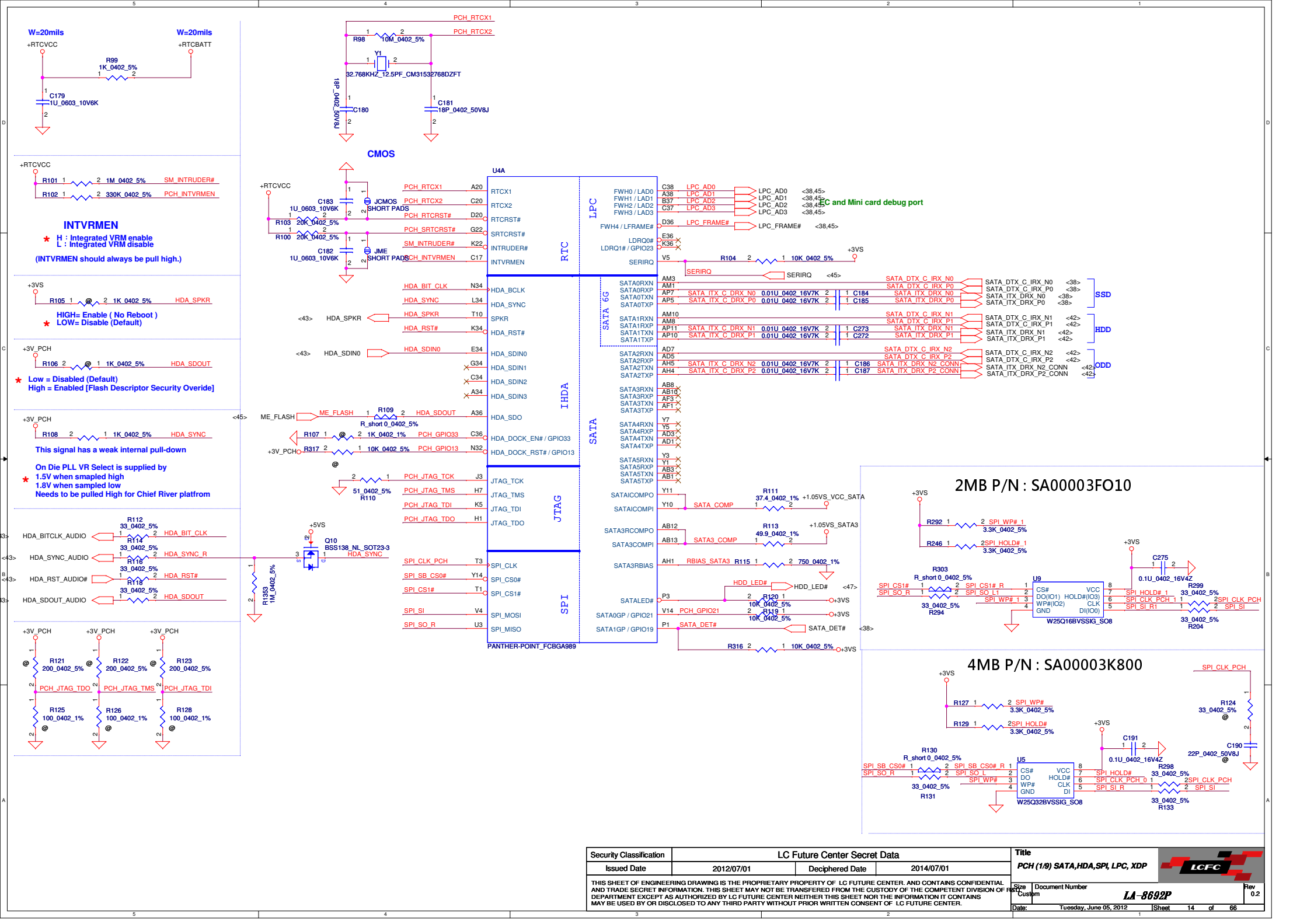
TYCO_2013620-2 IVY BRIDGE

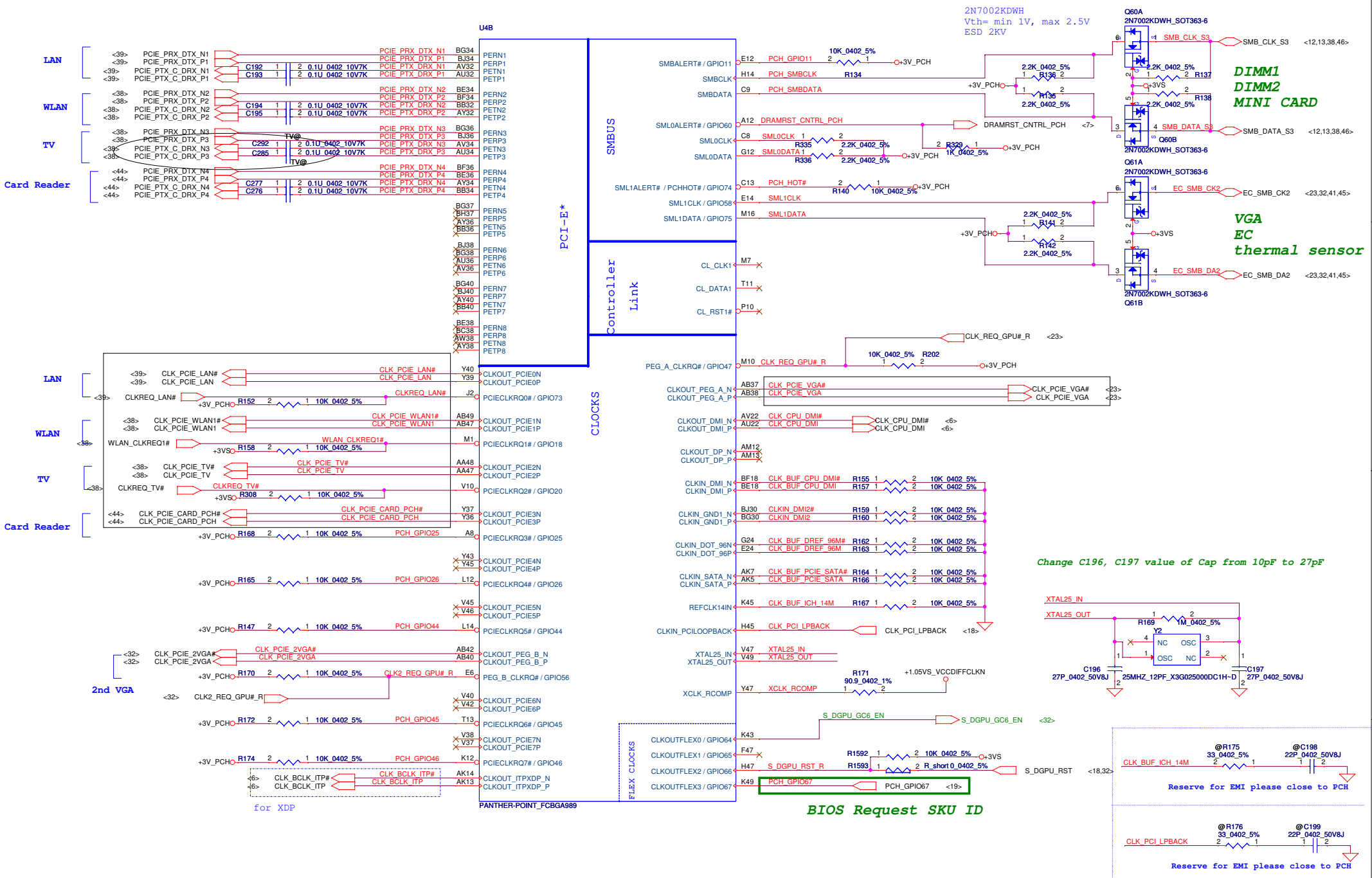
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PROCESSOR(4/7) RSVD,CFG			
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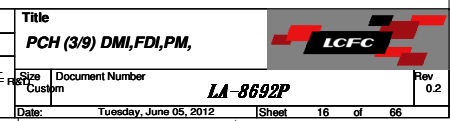


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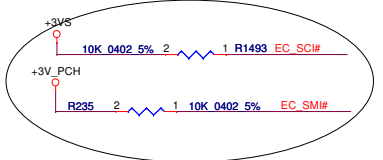






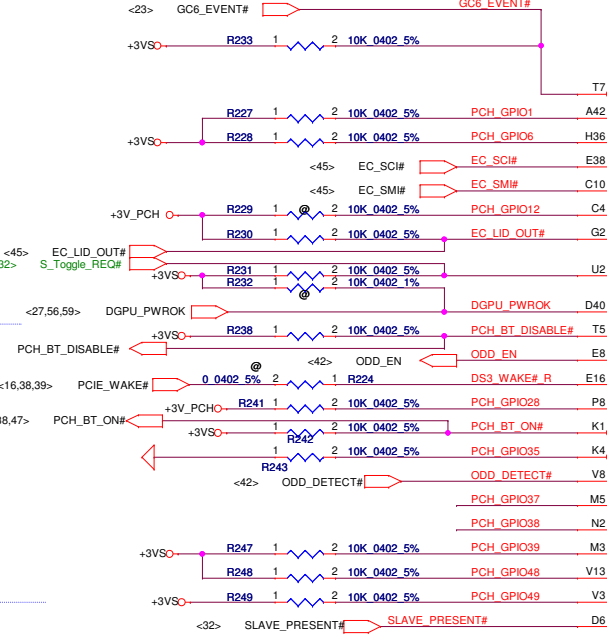
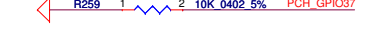
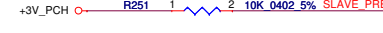
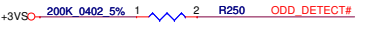
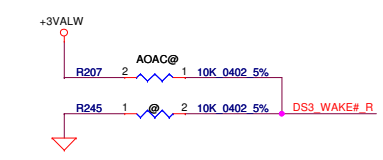




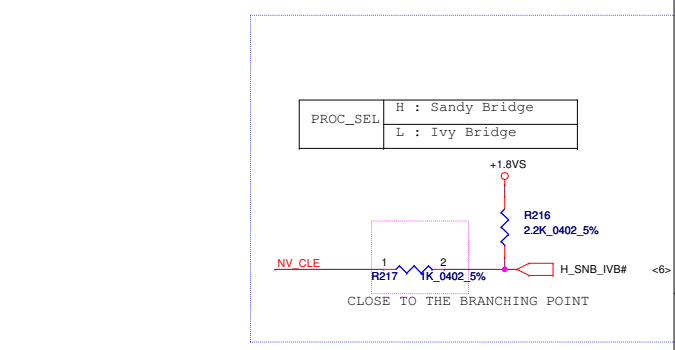
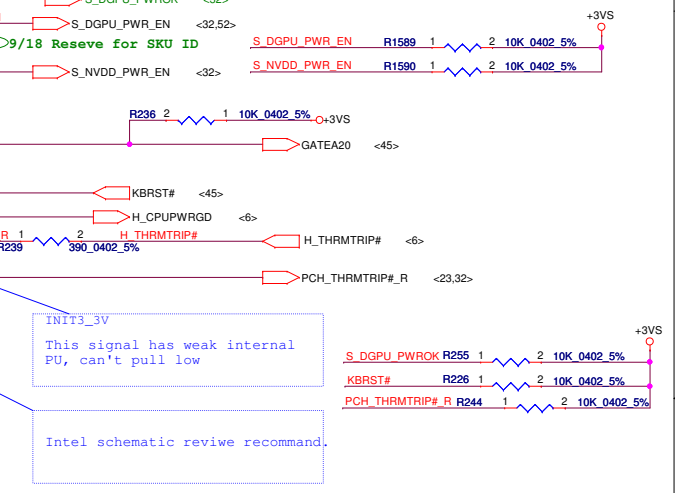
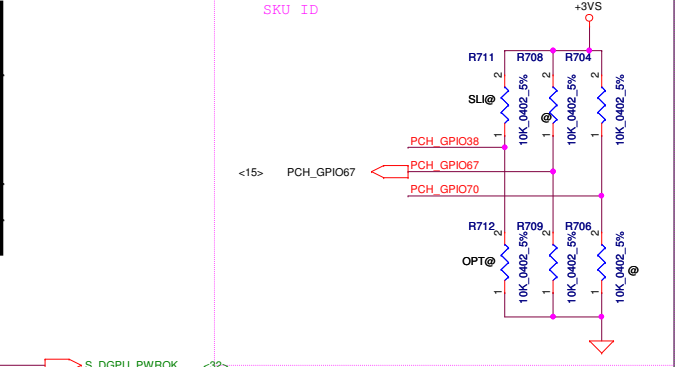
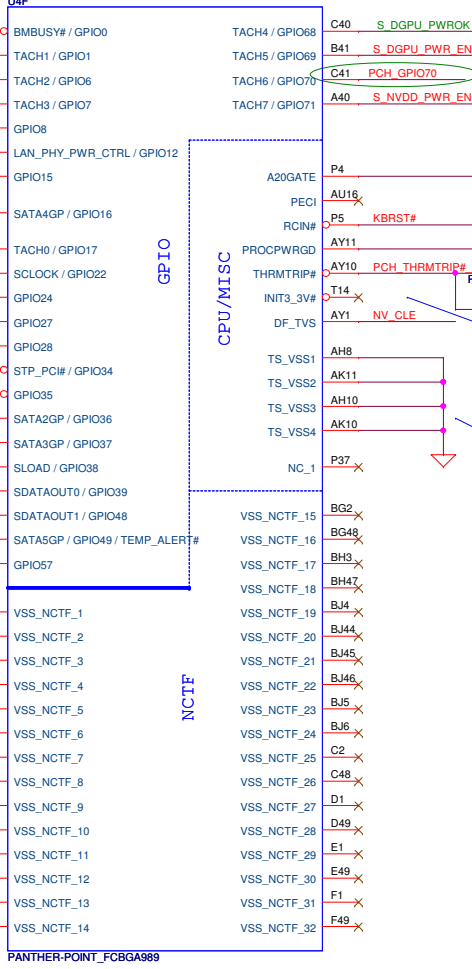


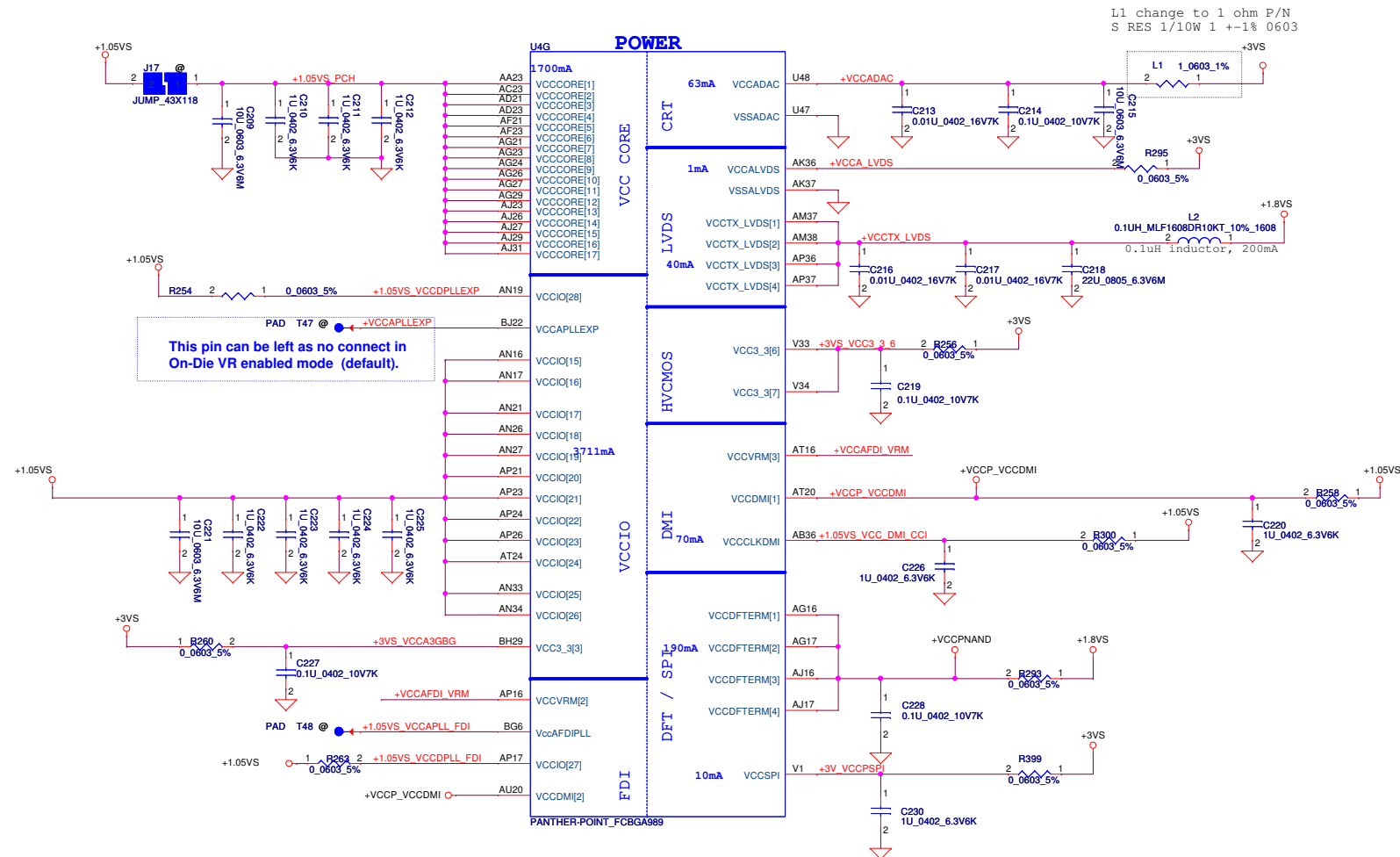
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

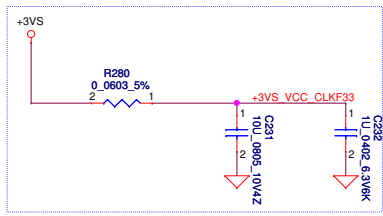


Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

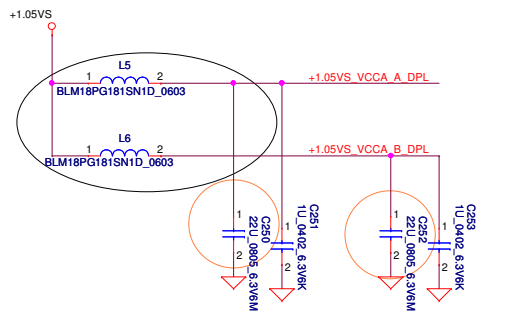




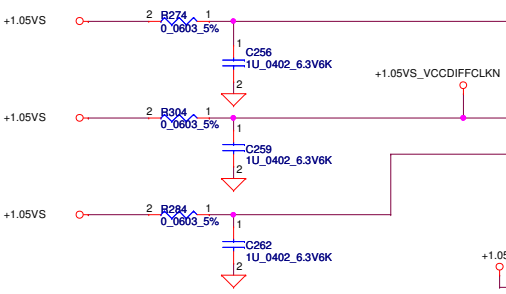
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



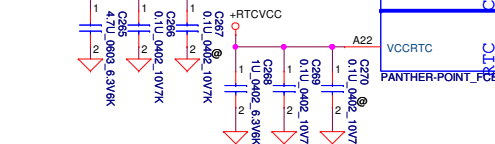
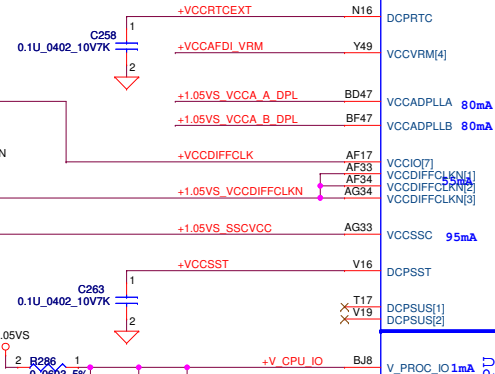
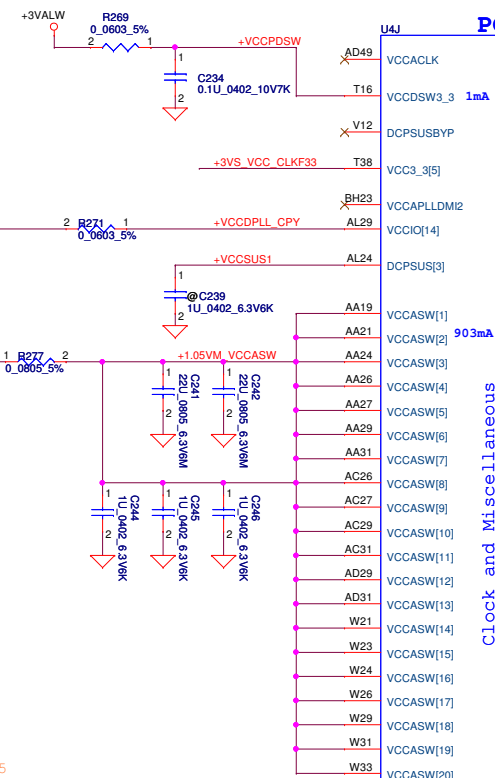
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA



Before gerber out change to 22u_0805



Have internal VRM



POWER

USB

PCI/GPIO/LPC

SATA

MISC

CPU

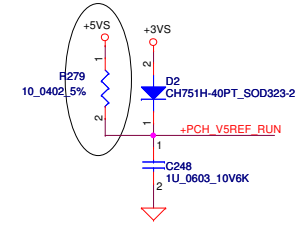
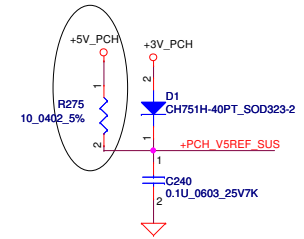
Clock and Miscellaneous

RTC

IC

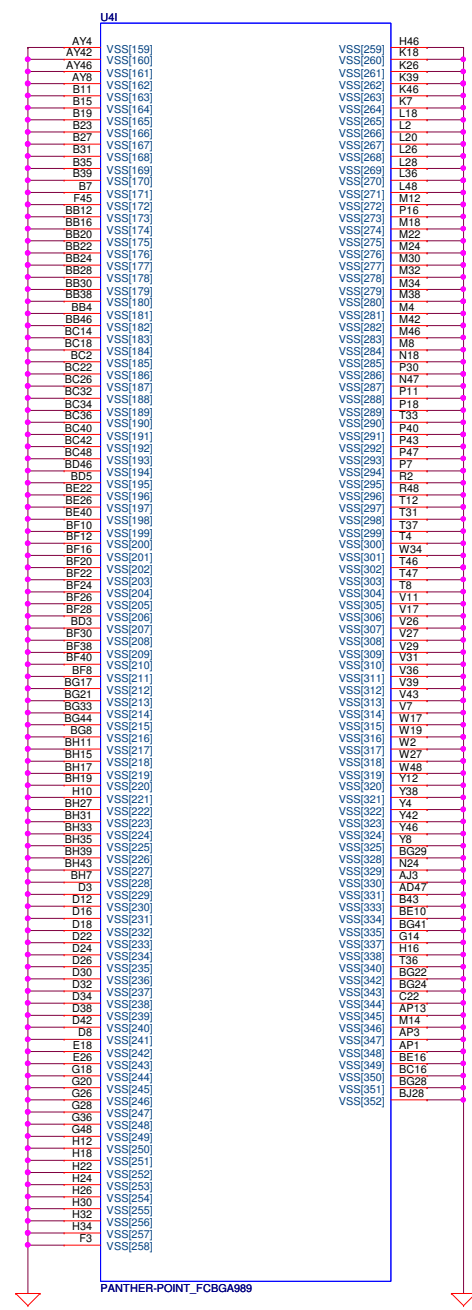
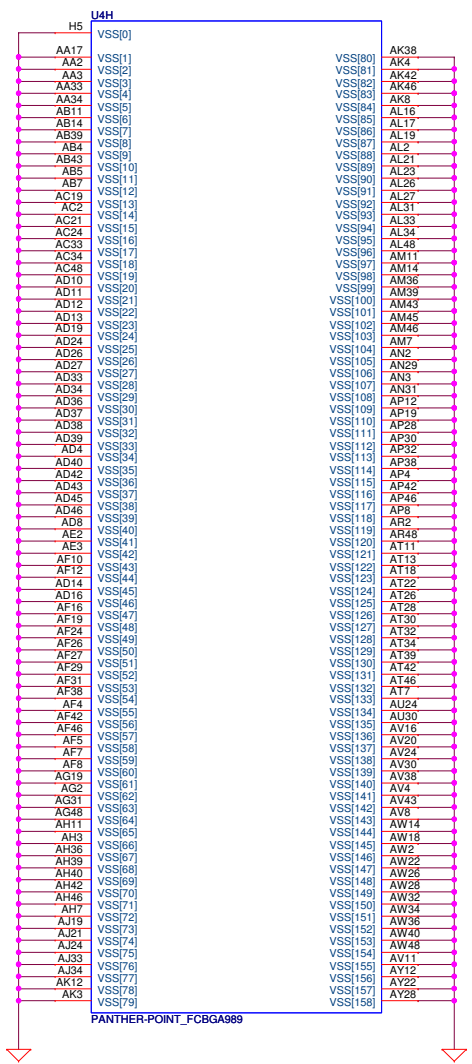
PANTHER-POINT_FCBGA985H

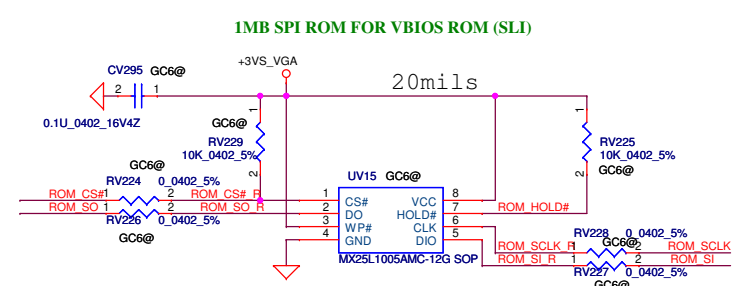
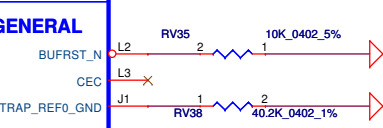
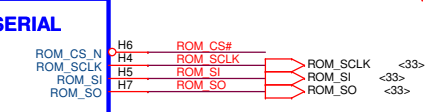
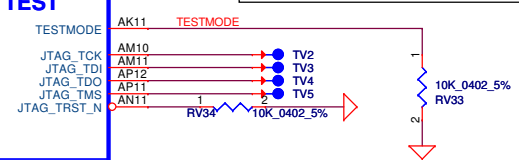
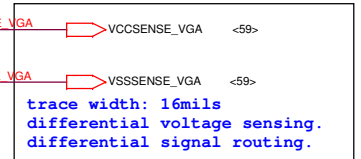
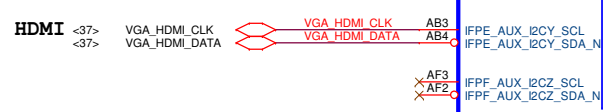
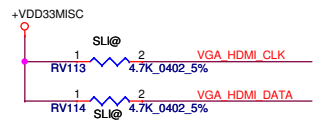
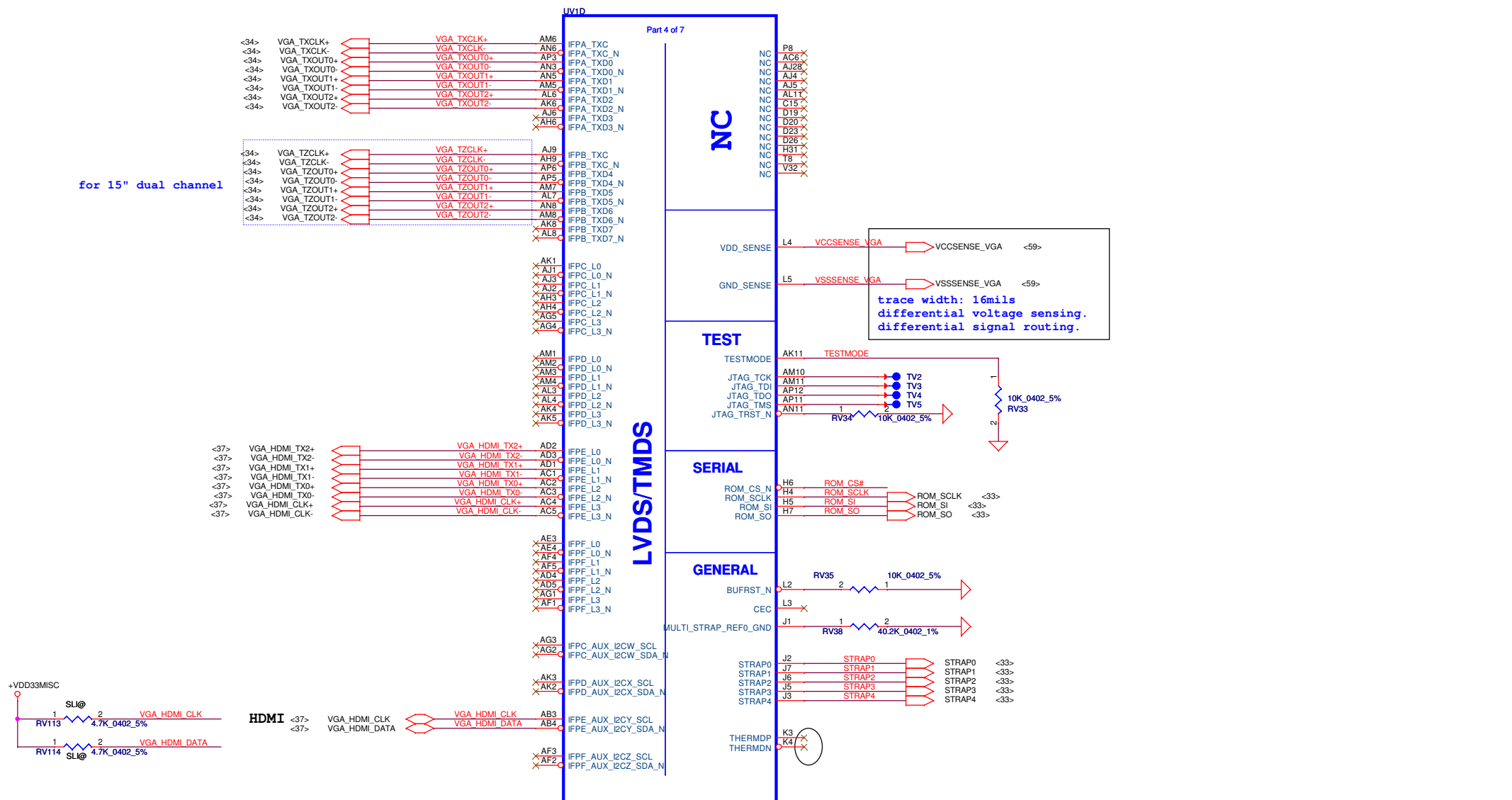
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec



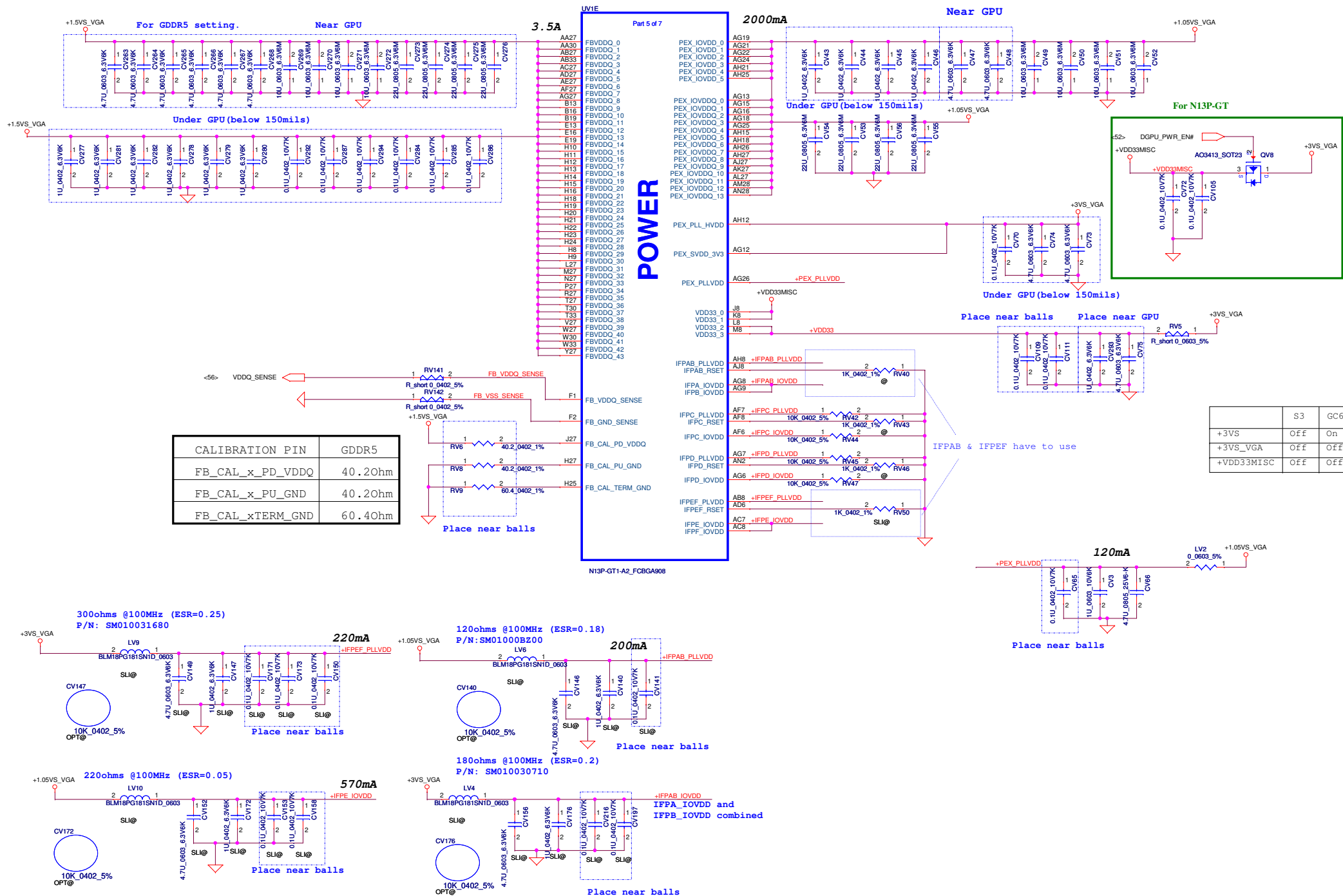
On-Die PLL Voltage Regulator
H: On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

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Size		Document Number		Date		Tuesday, June 05, 2012		Sheet 21 of 66	
Custom		Rev		0.2		LA-8692P			



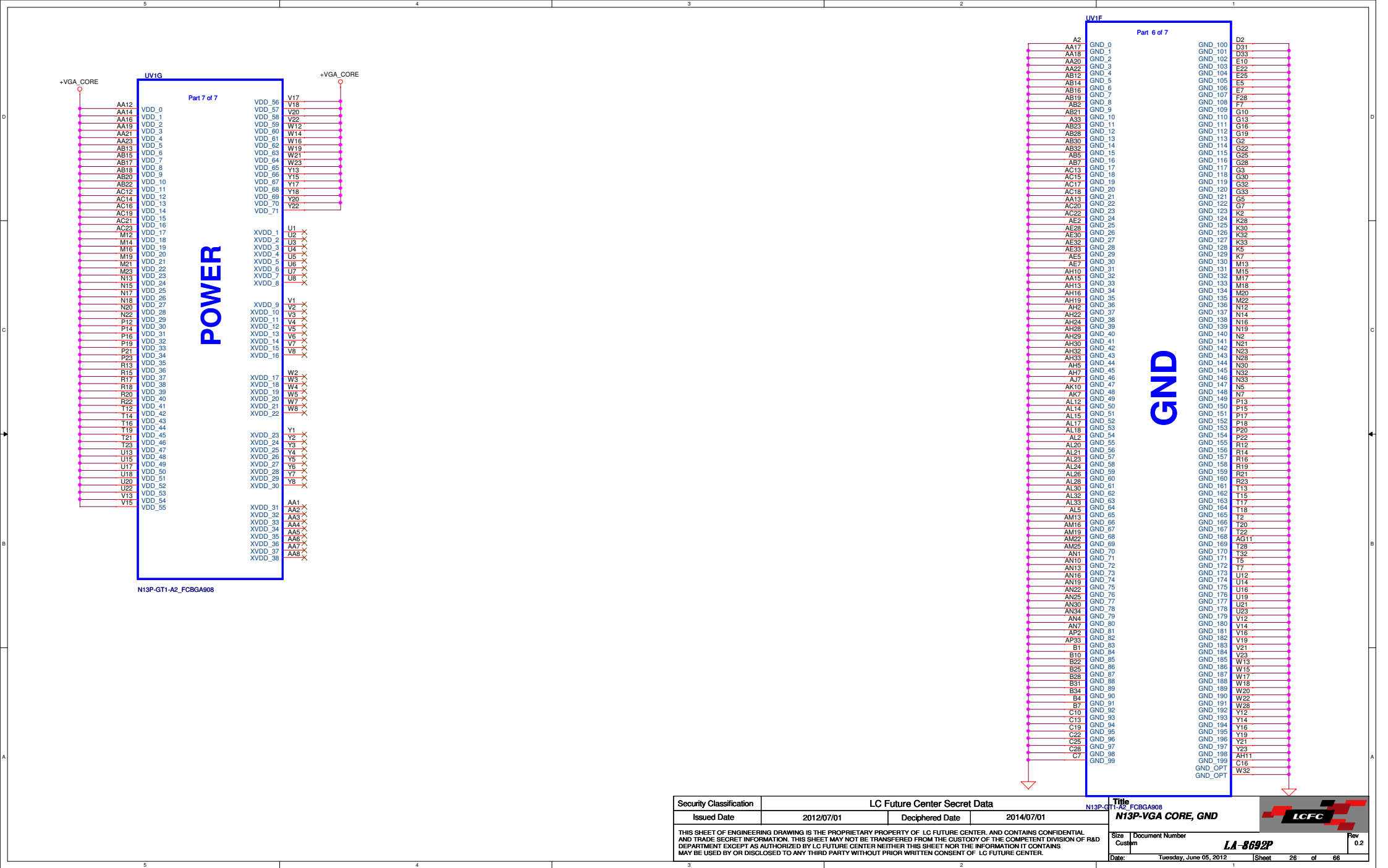


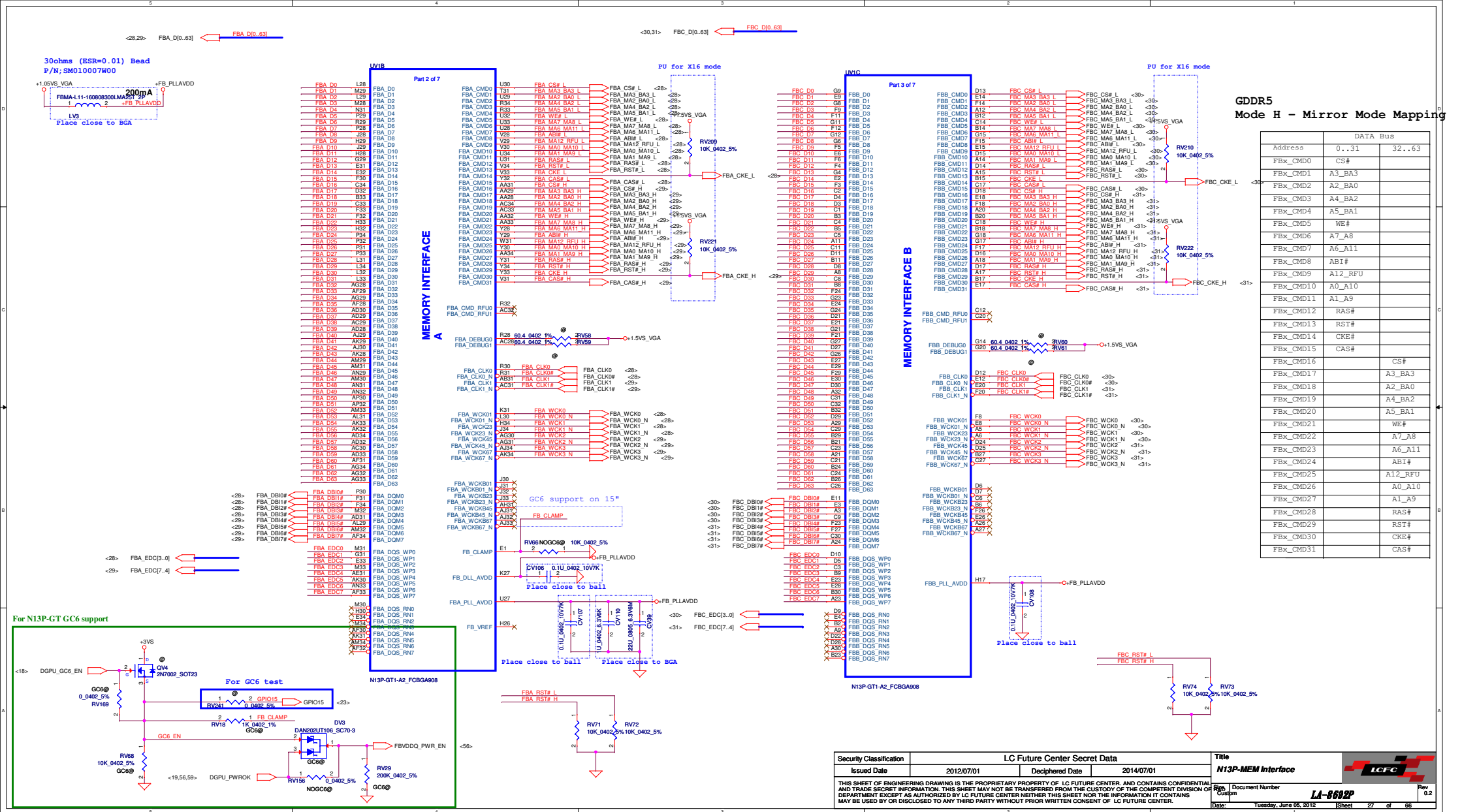
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Issued Date		2012/07/01		Deciphered Date		2014/07/01			
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Date:		Tuesday, June 05, 2012				Sheet 24 of 66			



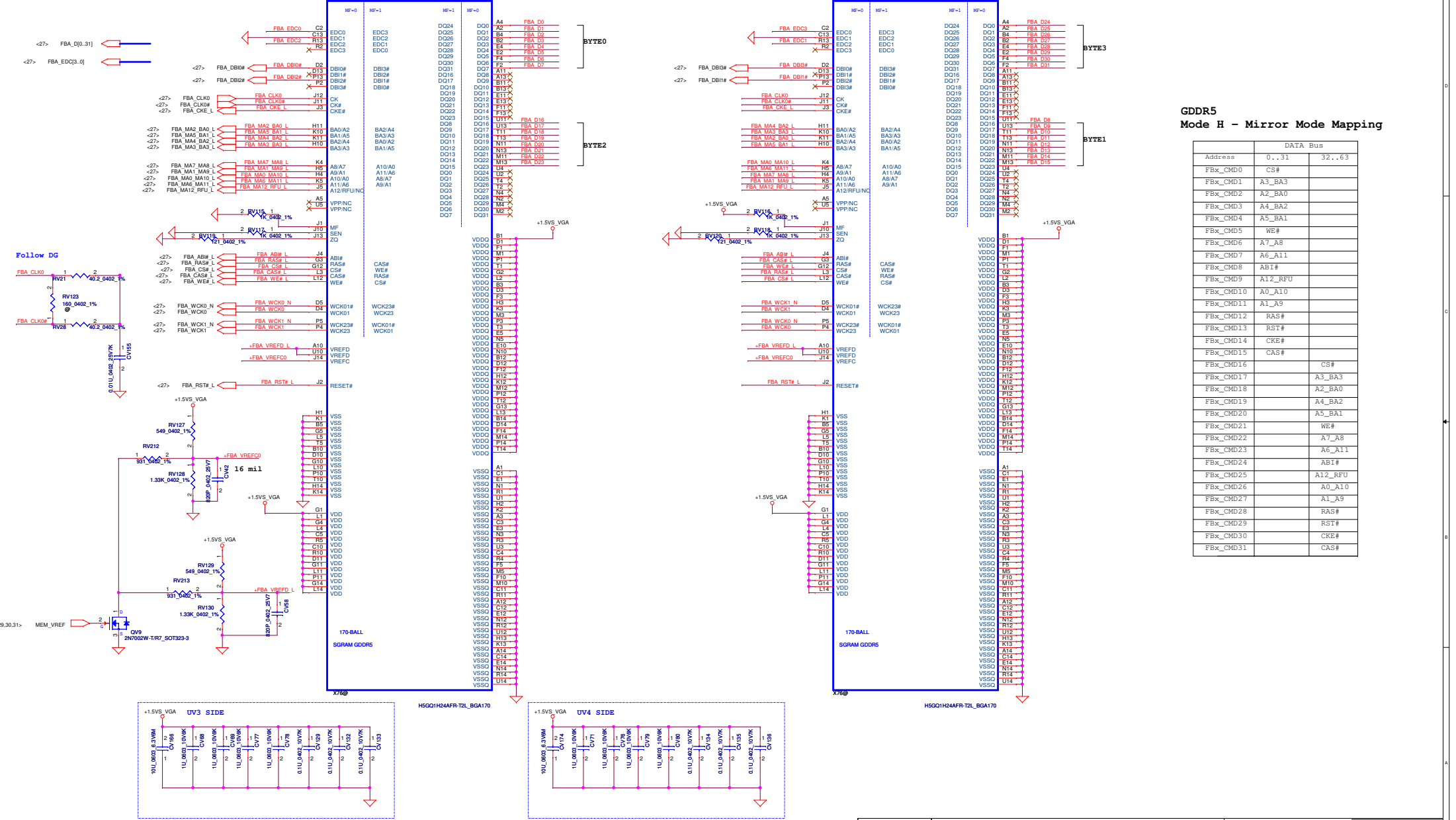
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	40.20hm
FB_CAL_xTERM_GND	60.40hm

	S3	GC6
+3VS	OFF	On
+3VS_VGA	OFF	OFF
+VDD33MISC	OFF	OFF

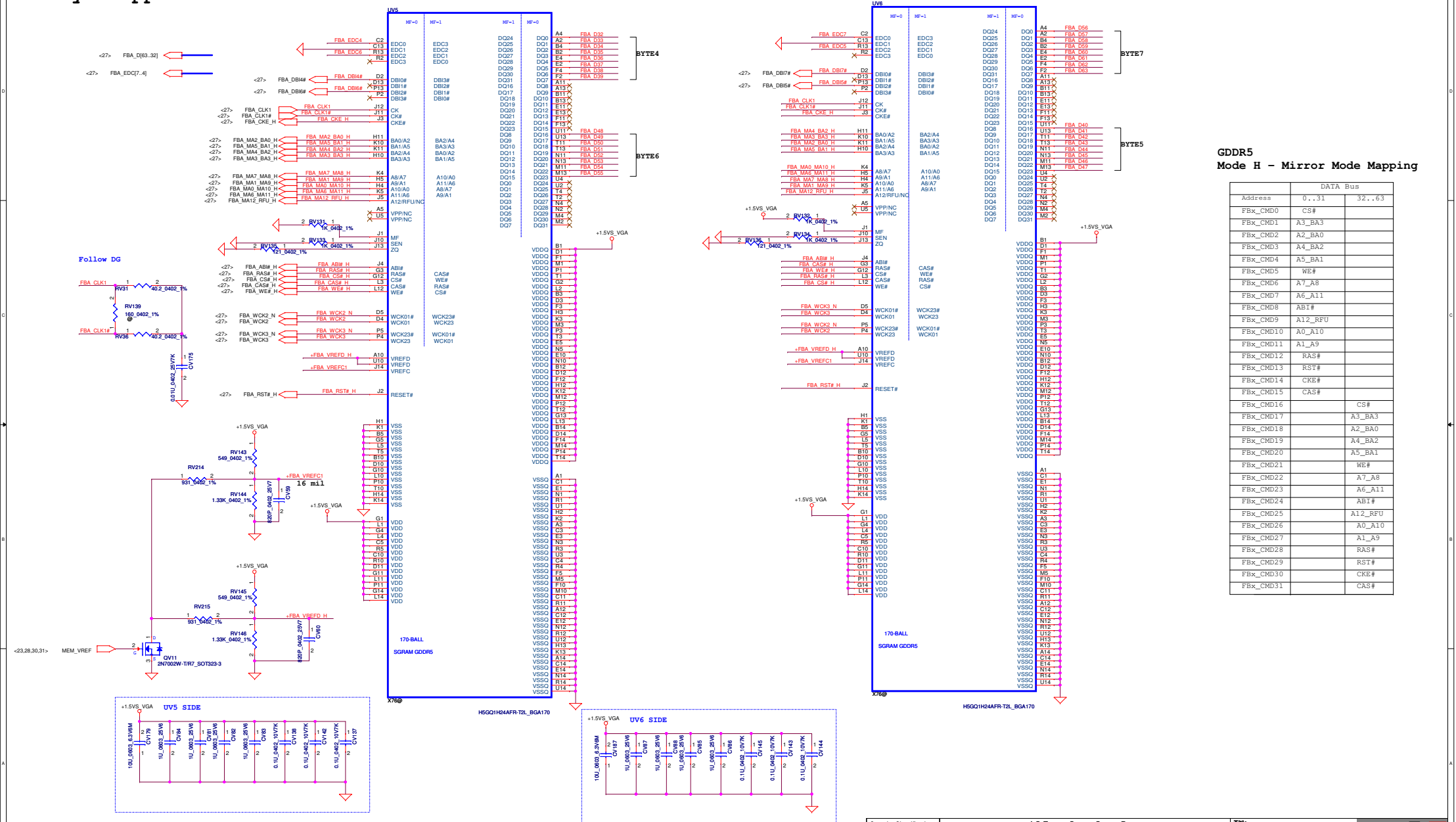




Memory - Lower 32 bits



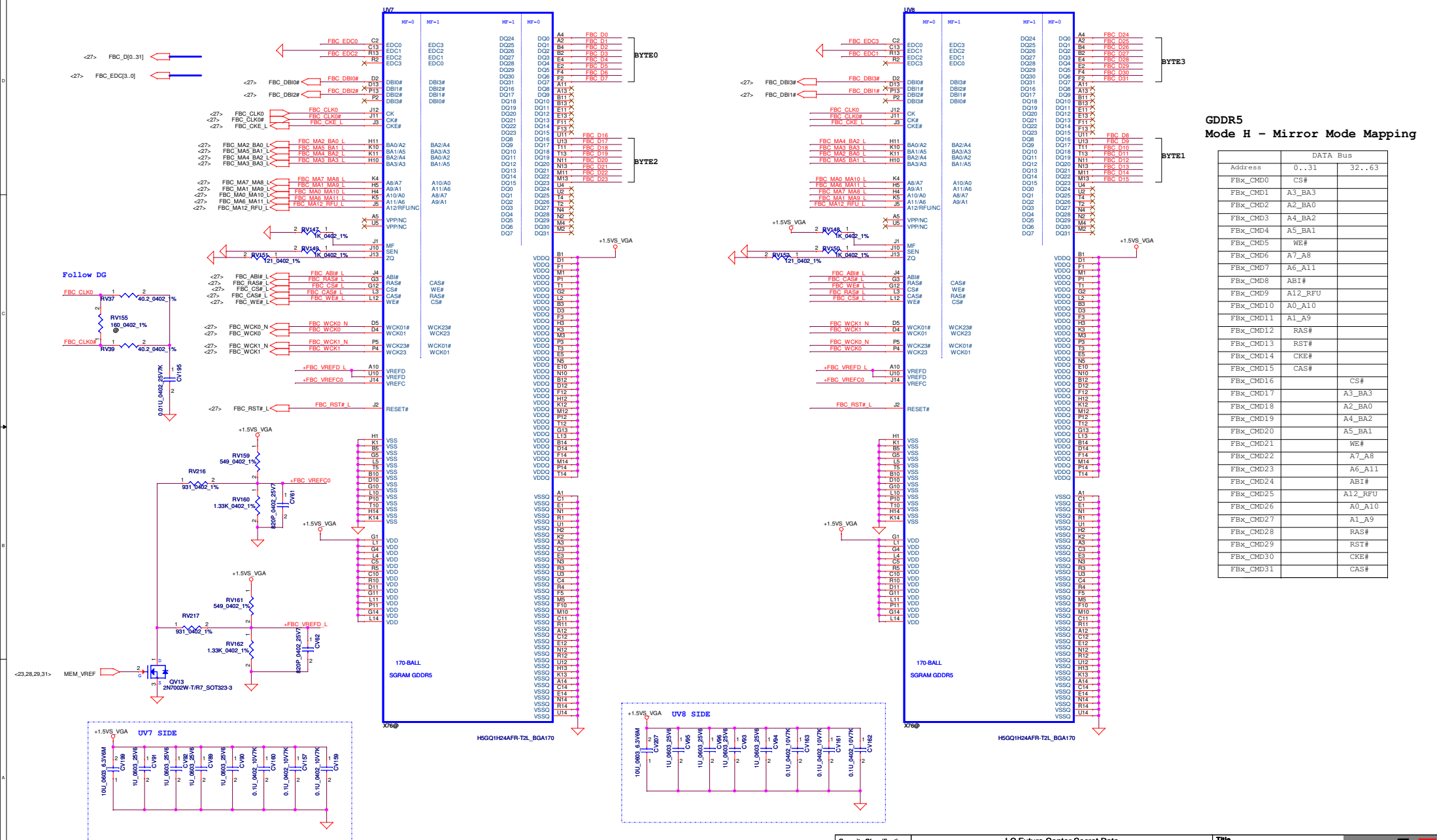
Memory – Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FbX_CMD0	CS#	
FbX_CMD1	A3_BA3	
FbX_CMD2	A2_BA0	
FbX_CMD3	A4_BA2	
FbX_CMD4	A5_BA1	
FbX_CMD5	WE#	
FbX_CMD6	A7_A8	
FbX_CMD7	A6_A11	
FbX_CMD8	AB1#	
FbX_CMD9	A12_RFU	
FbX_CMD10	A0_A10	
FbX_CMD11	A1_A9	
FbX_CMD12	RA5#	
FbX_CMD13	RST#	
FbX_CMD14	CKE#	
FbX_CMD15	CAS#	
FbX_CMD16		CS#
FbX_CMD17		A3_BA3
FbX_CMD18		A2_BA0
FbX_CMD19		A4_BA2
FbX_CMD20		A5_BA1
FbX_CMD21		WE#
FbX_CMD22		A7_A8
FbX_CMD23		A6_A11
FbX_CMD24		AB1#
FbX_CMD25		A12_RFU
FbX_CMD26		A0_A10
FbX_CMD27		A1_A9
FbX_CMD28		RAS#
FbX_CMD29		RST#
FbX_CMD30		CKE#
FbX_CMD31		CAS#

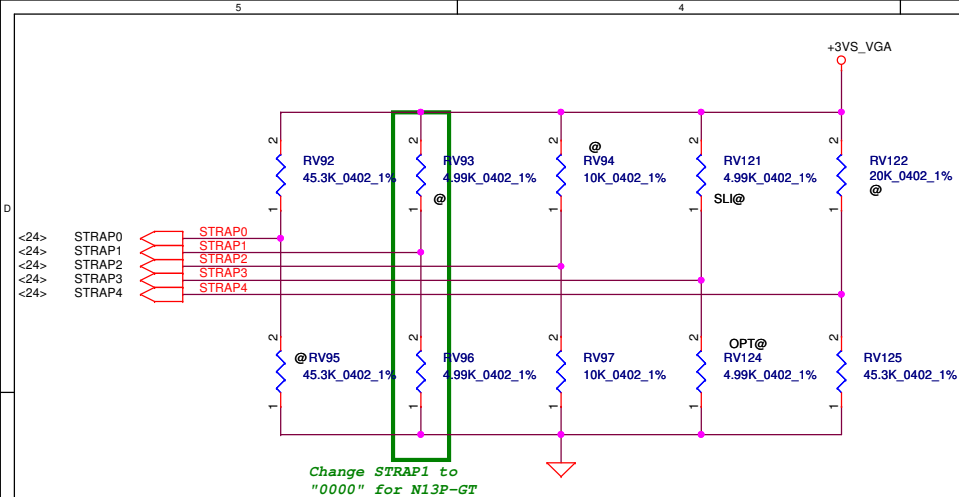
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	LC #	
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Memory Partition C - Lower 32 bits



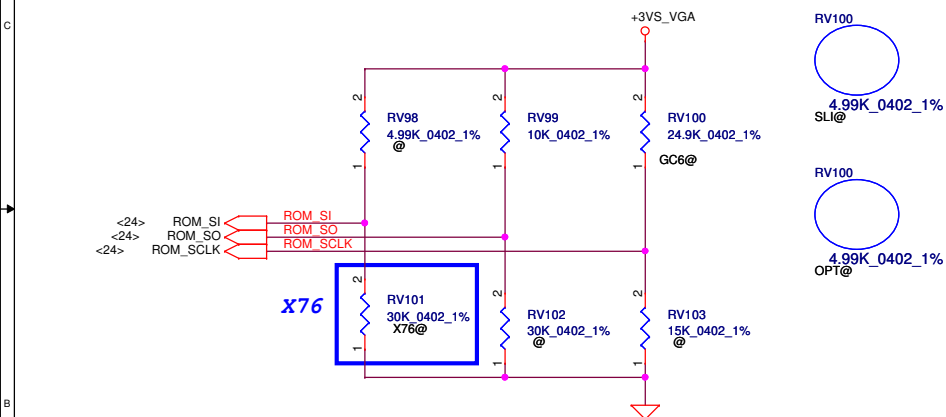
Mode H - Mirror Mode Mapping

DATA Bus		
Address	0...31	32...63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABT#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABT#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



3GIO_PADCFG		XCLK_417	
3GIO_PADCFG[3:0]		0	277MHz (Default)
0000	Notebook Default	1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

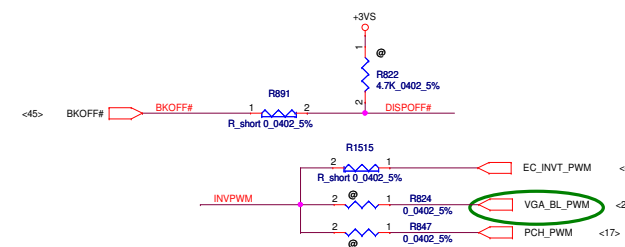
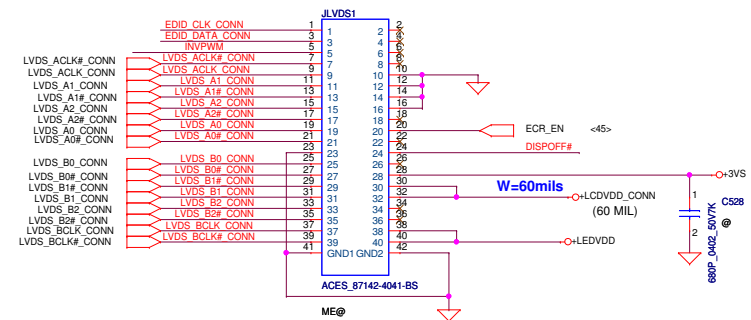
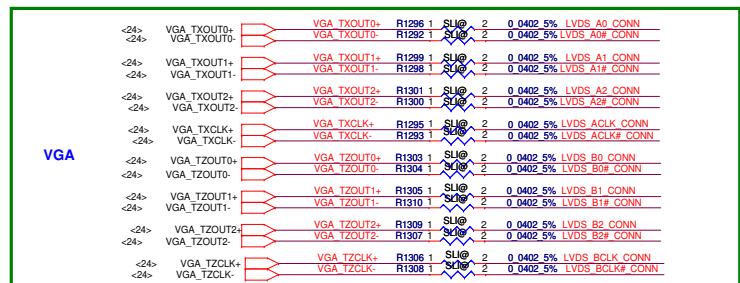
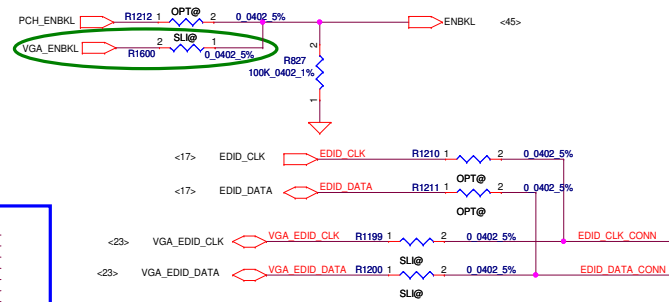
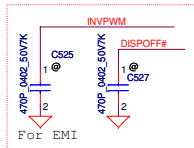
FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

GPU		FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	Samsung	K4G20325FD-FC04	2G	PD 30K	PU 25K GC6@		PU 5K SLI@		PU 5K SLI@		64Mx32	
		K4G10325FG-HC04	1G	PD 45K	PU 10K		PU 45K	PD 5K	PD 10K	PD 45K	32Mx32	
	Hynix	H5GQ2H24AFR-T2C	2G	PD 25K	PU 5K		PD 5K OPT@, SLI@		PD 5K OPT@		64Mx32	
		H5GQ1H24BFR-T2C	1G	PD 35K	OPT@, SLI@		PD 5K OPT@		32Mx32			

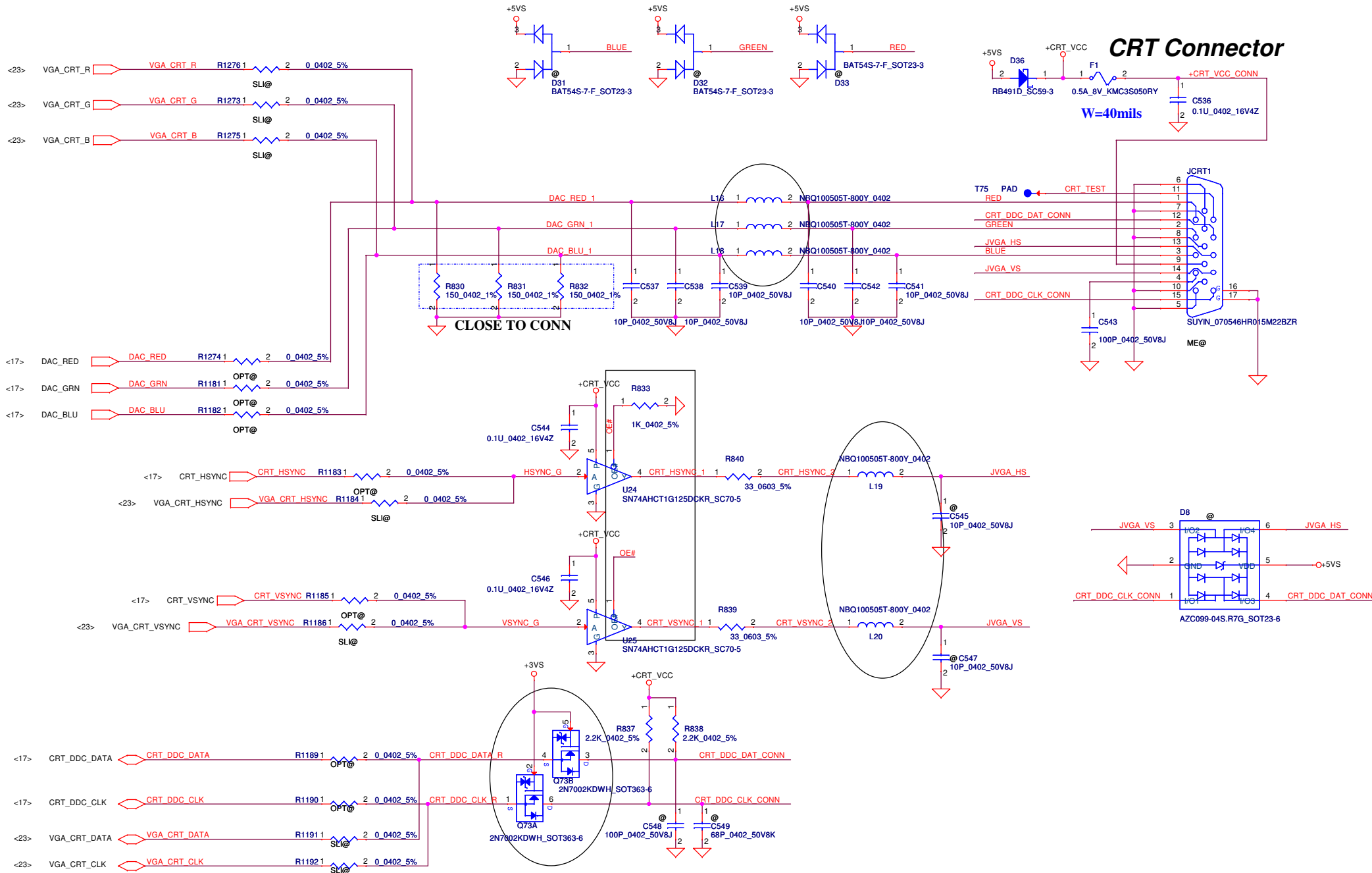
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	N13P_MISC	
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Size	Document Number			Rev	
Custom	LA-8692P			0.2	
Date:	Thursday, June 07, 2012		Sheet	33	of 66

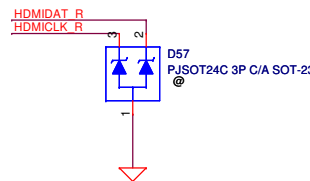
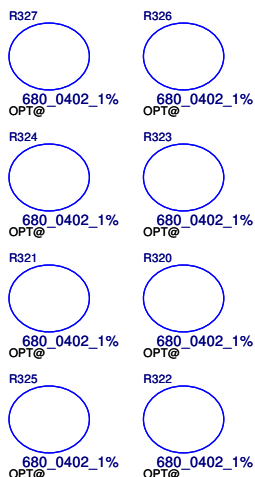
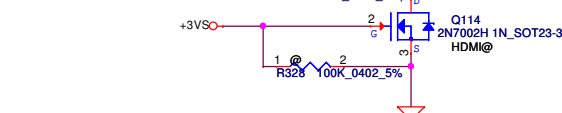
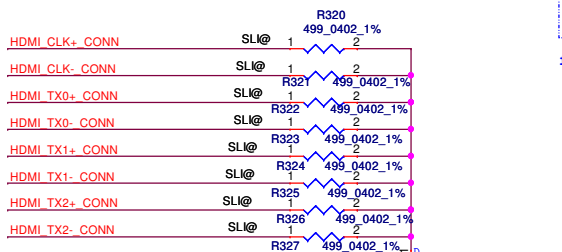
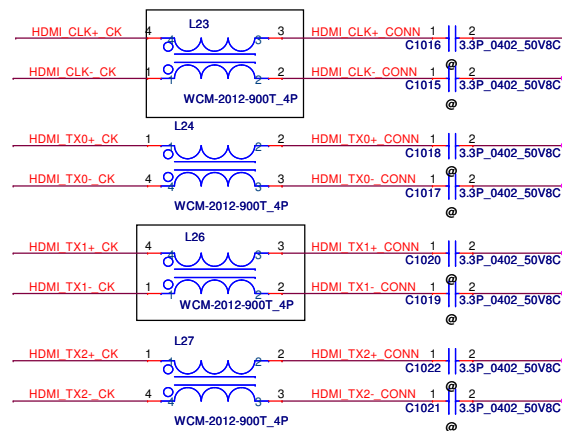


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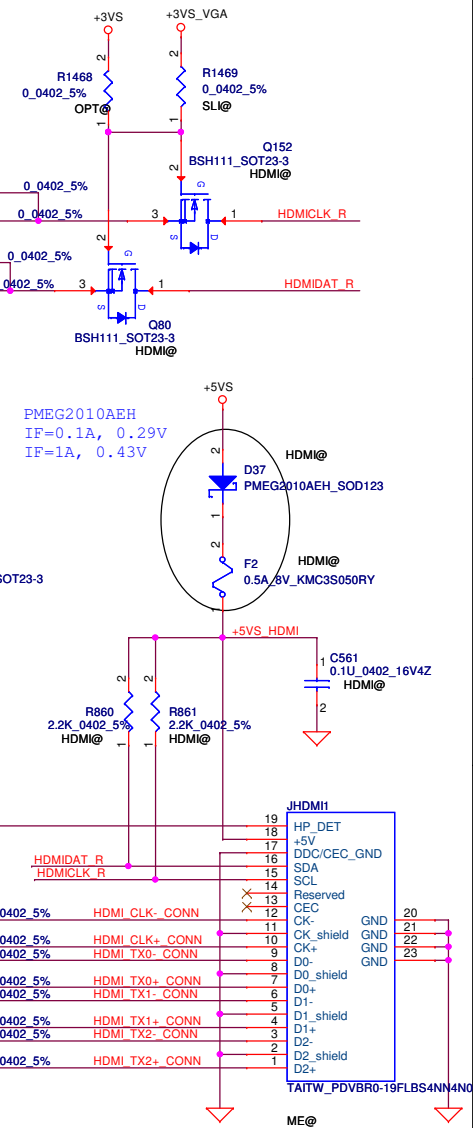
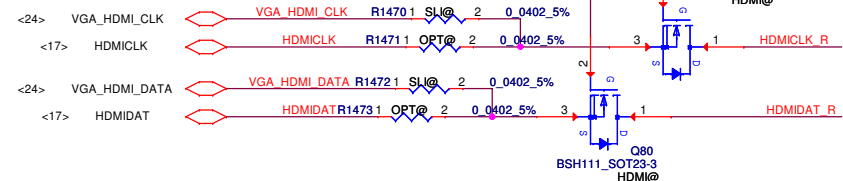
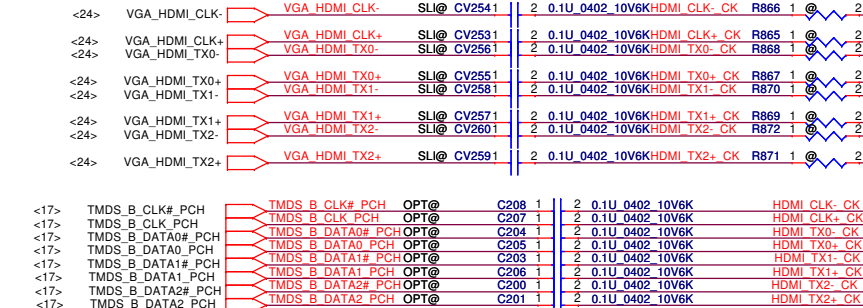
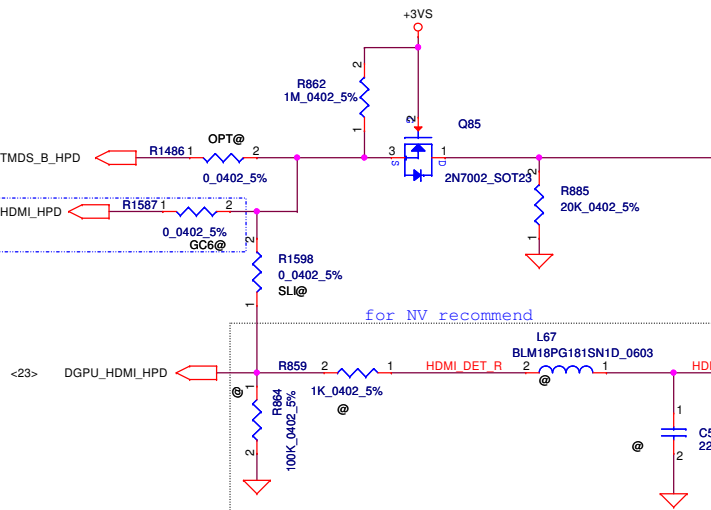
No use NVSR chip for DVT

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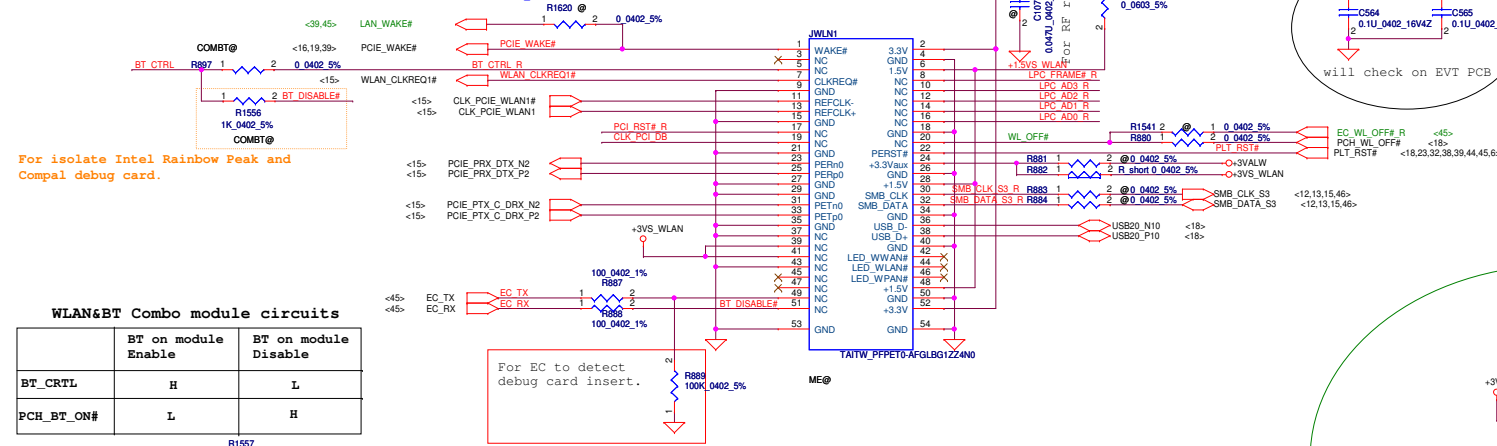
<17> TMD5_B_HPD
<18> HDMI_HPD
for NVSR



Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

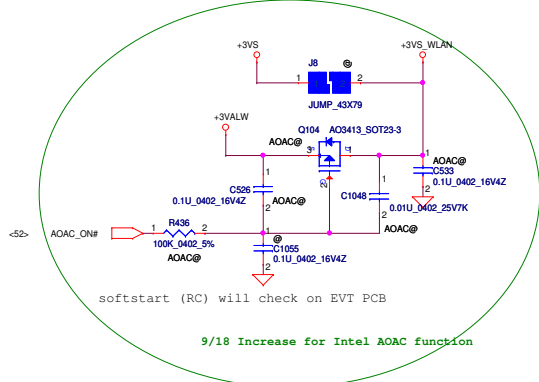
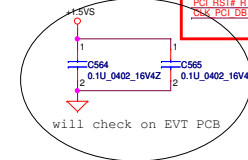
9/18 JPI Pin2,24,52 contact to +3VS_WLAN for AOAC function

Mini-Express Card(WLAN/WiMAX)



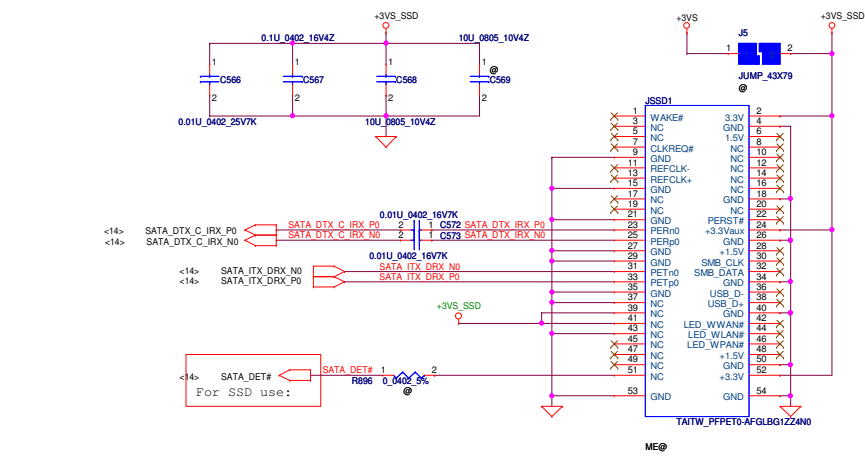
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R873	1	2	0	0402_5%	LPC_FRAME#	LPC_FRAME#	<14,45>
LPC_ADS3_R	R874	1	2	0	0402_5%	LPC_ADS3	LPC_ADS3	<14,45>
LPC_ADS2_R	R875	1	2	0	0402_5%	LPC_ADS2	LPC_ADS2	<14,45>
LPC_ADS1_R	R876	1	2	0	0402_5%	LPC_ADS1	LPC_ADS1	<14,45>
LPC_ADS0_R	R877	1	2	0	0402_5%	LPC_ADS0	LPC_ADS0	<14,45>
LPC_RST#_R	R878	1	2	0	0402_5%	LPC_RST#	LPC_RST#	<18>
CLK_PDI_DB	R879	1	2	0	0402_5%	CLK_PDI_DB	CLK_PDI_DB	<18>

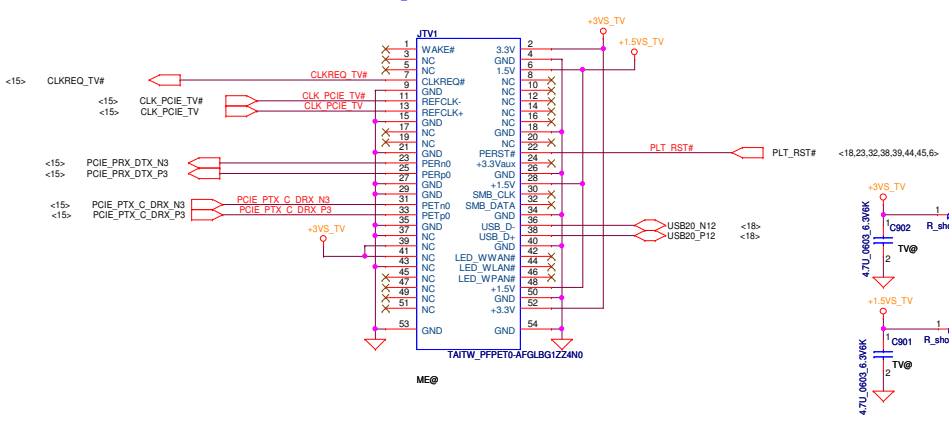


Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)

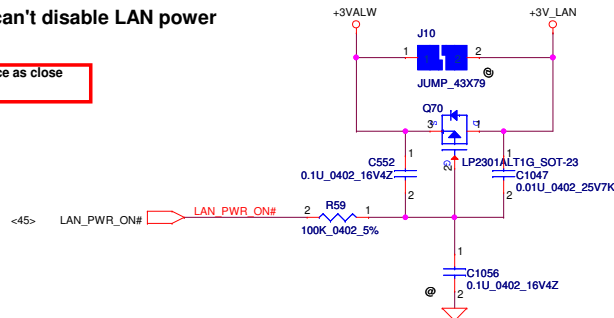


Mini-Express Card(TV)

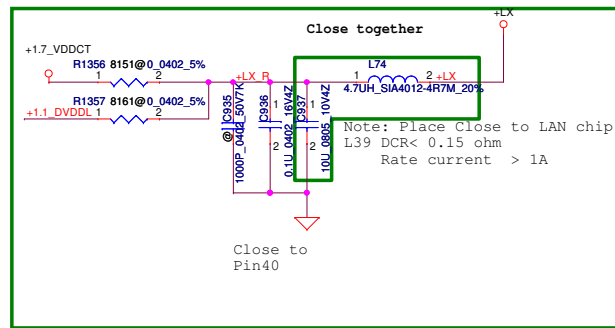
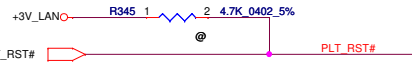


Atheros request can't disable LAN power

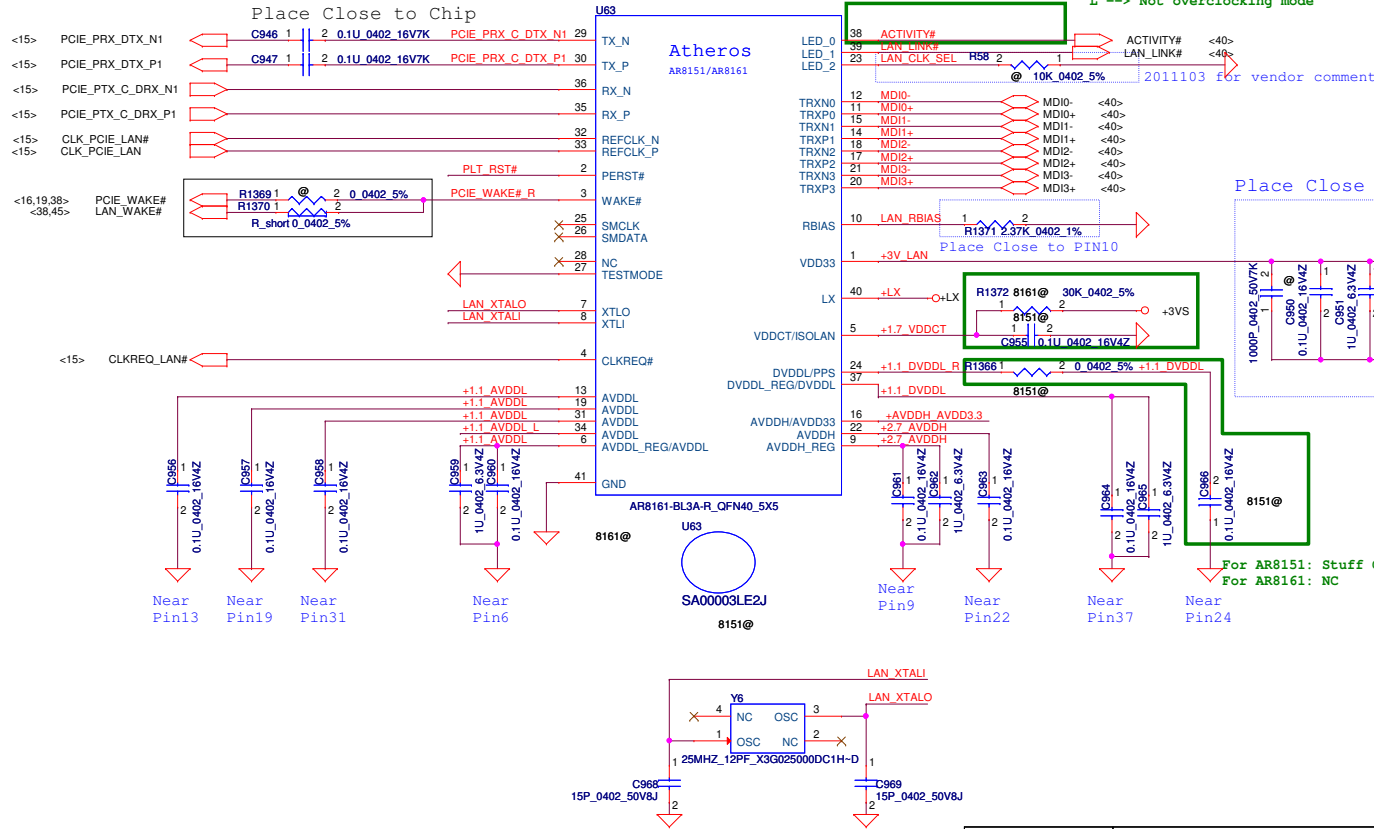
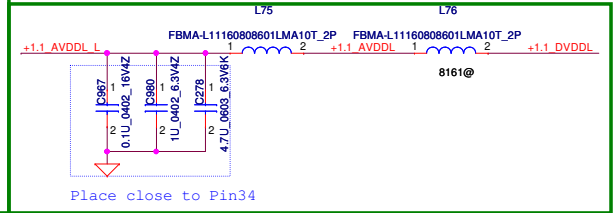
**Layout Notice : Place as close
chip as possible.**



Vendor recommend reseve the
PU resistor close LAN chip

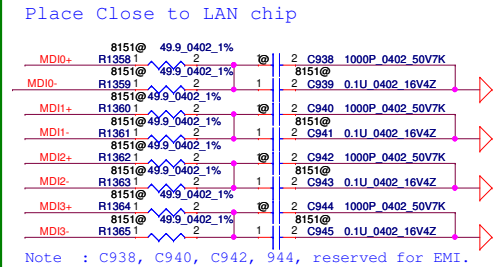


	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76

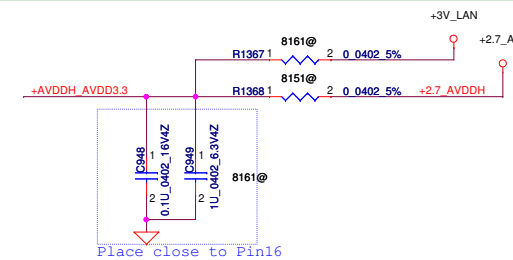


```
H --> Overclocking mode
L --> Not overclocking mode
```

Place Close to PIN1



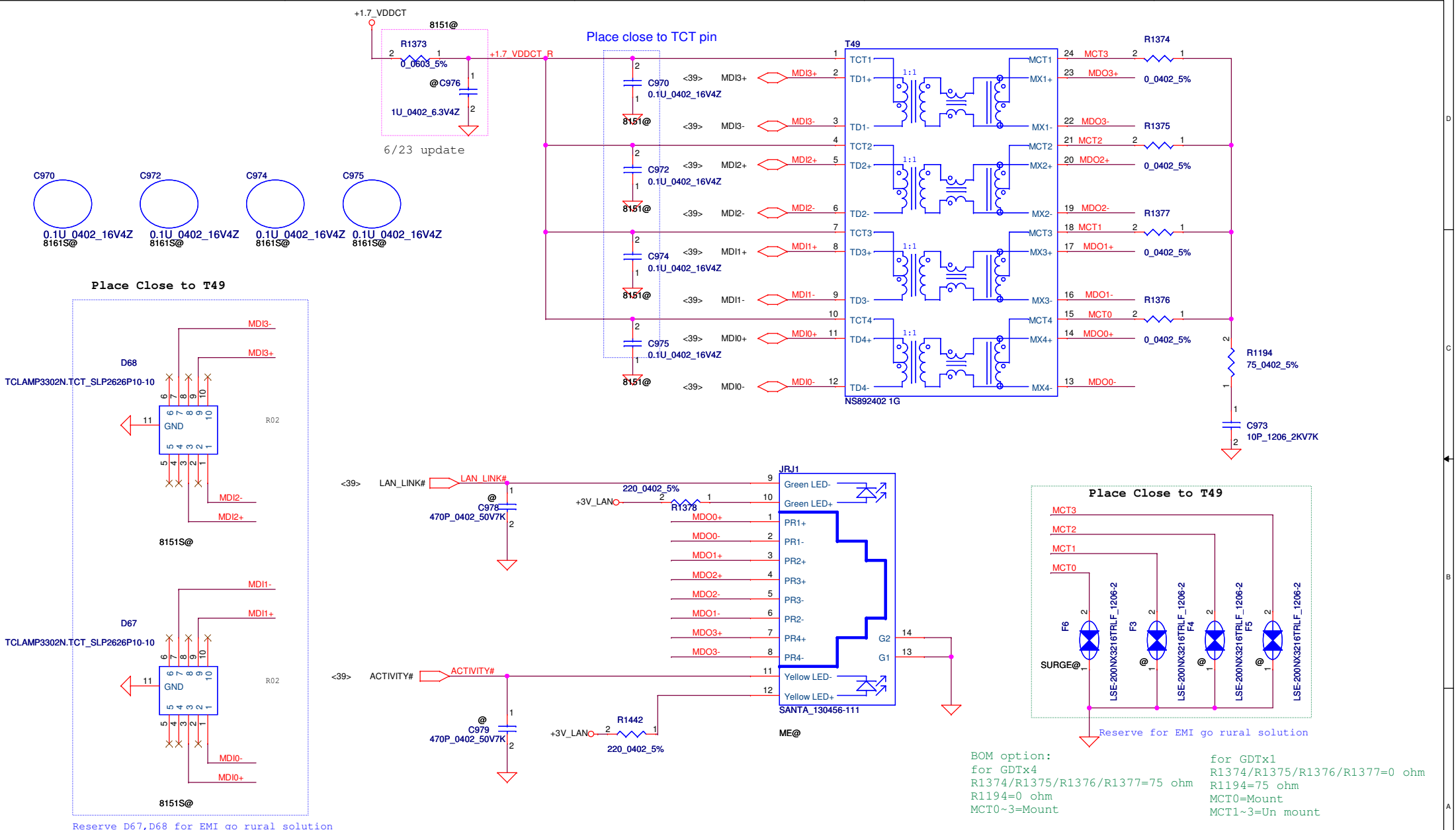
```
For AR8151: Stuff 49.9K and 0.1u
For AR8161: NC
```



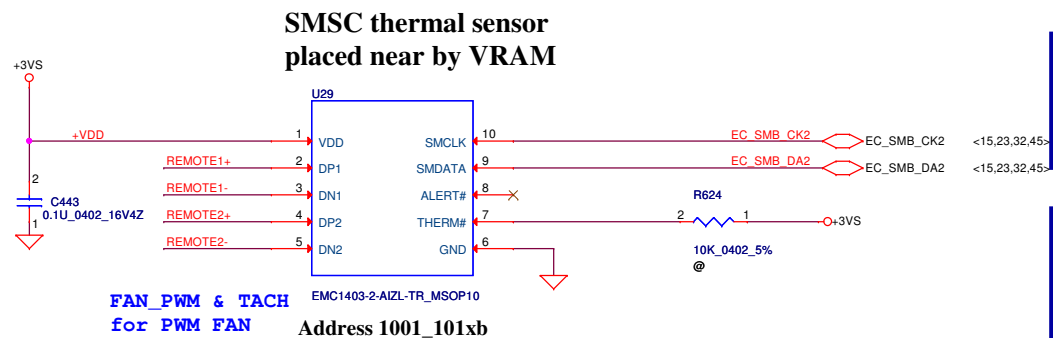
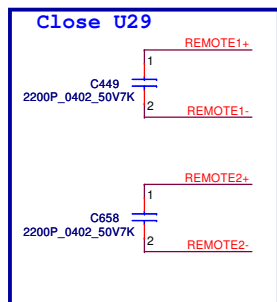
```
For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367,C949 for +AVDDH
```

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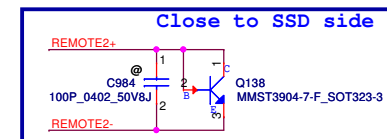
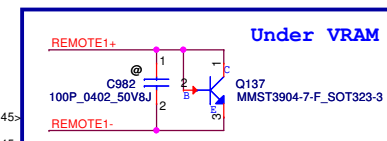
R&D	Title			
	LAN-AR8151/8161			
R&D	Size	Document Number	Rev	
	Custom	LA-8692P	0.2	
	Date:	Tuesday, June 05, 2012	Sheet	39 of 66



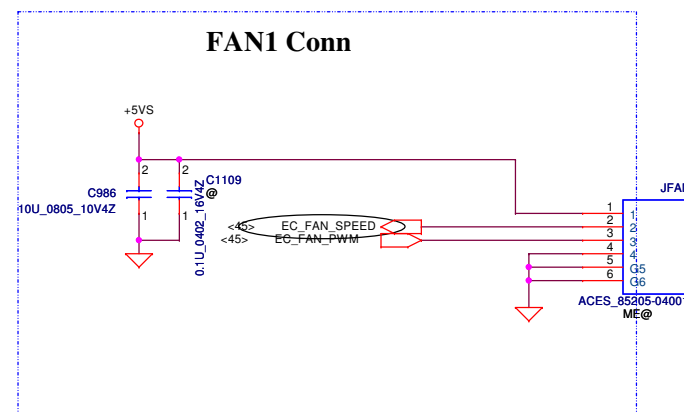
Security Classification		LC Future Center Secret Data				Title					
Issued Date		2012/07/01		Deciphered Date		2014/07/01			LAN_Transformer		
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								LA-8692P			
Date:		Tuesday, June 05, 2012				Sheet		40 of 66			



internal pull up 1.2K to 1.5V
R for initial thermal
shutdown temp

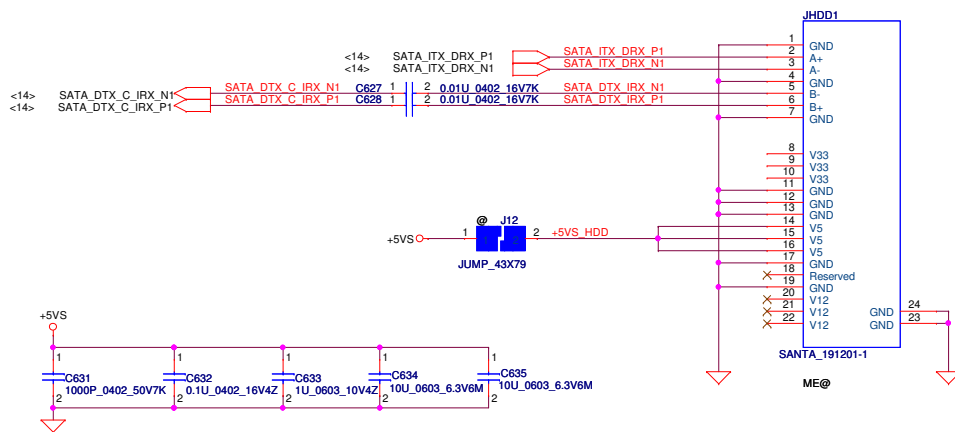


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

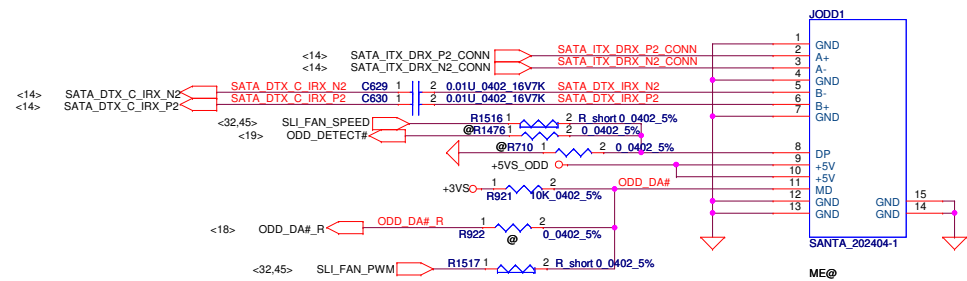


Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	EMC1403/2103_Thermal sensor/FAN			
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				Custom			
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						Rev	0.2

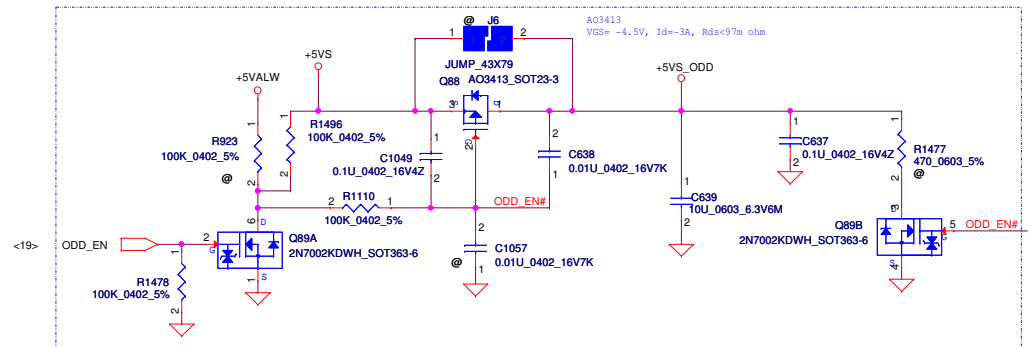
SATA HDD Conn.



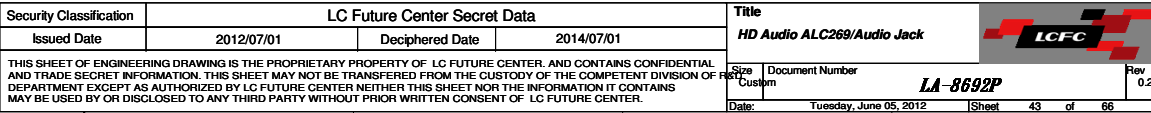
SATA ODD Conn.



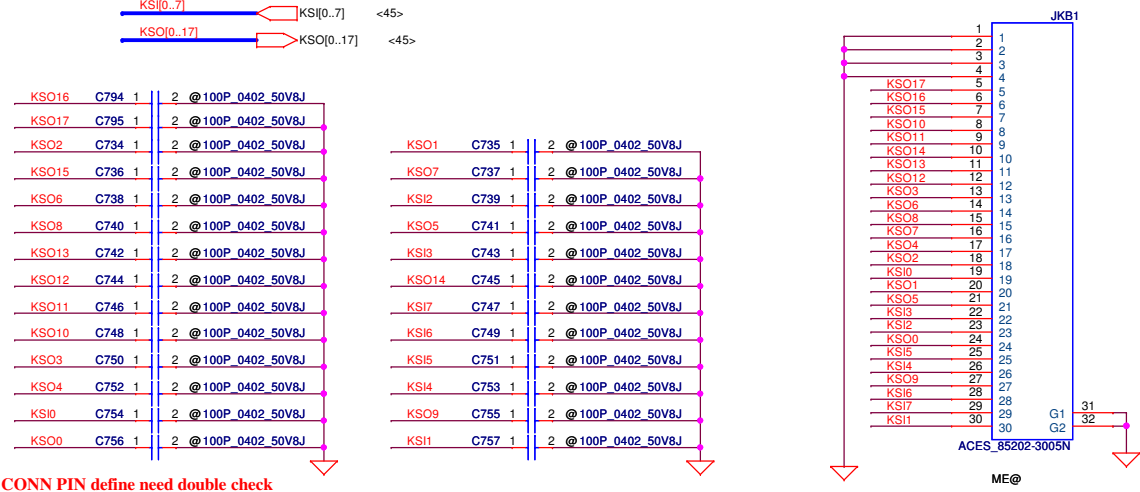
ODD Power Control



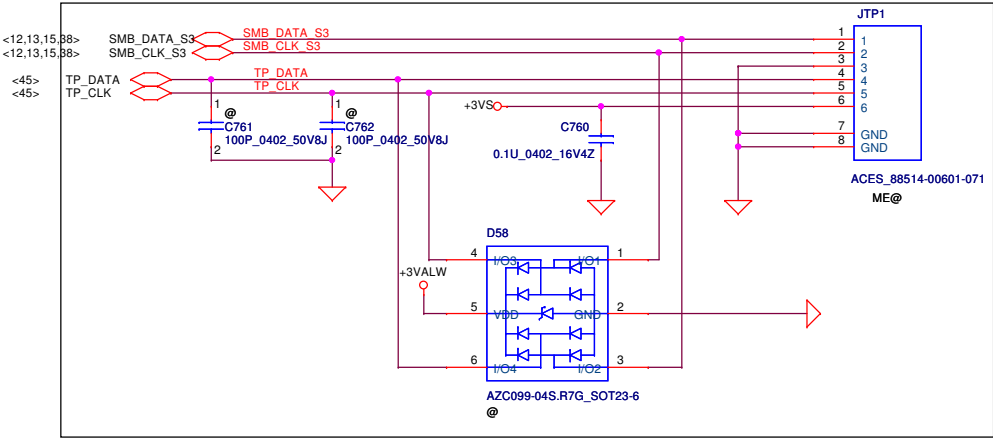
Security Classification	LC Future Center Secret Data		Title	HDD/ODD Connector	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Document Number
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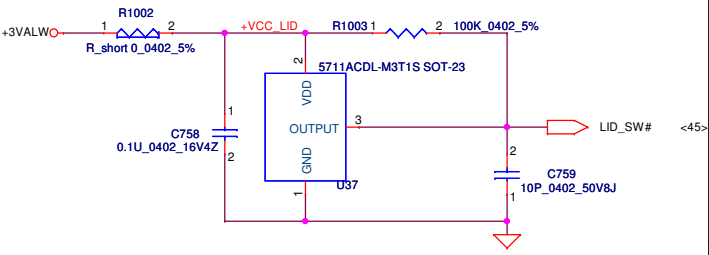
15" INT_KBD Conn.



To TP/B Conn.

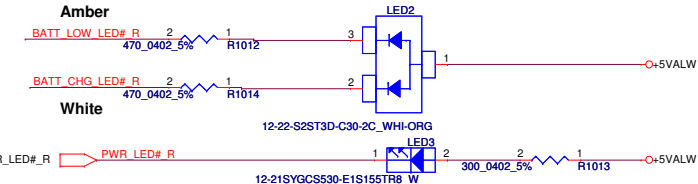


Lid Switch

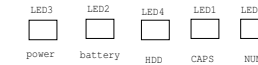
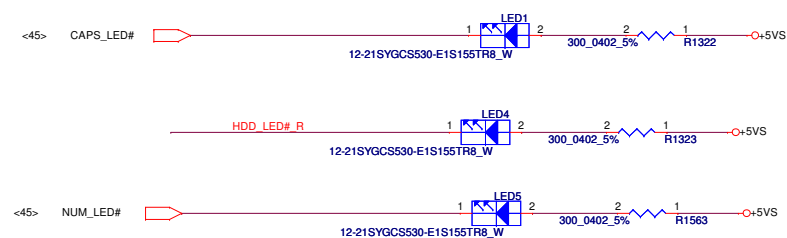


LED

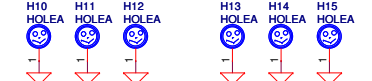
White



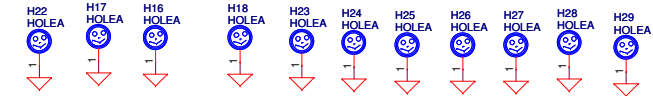
White



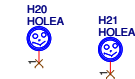
CPU:H_3P8X 3 GPU:H_3P8 X 3



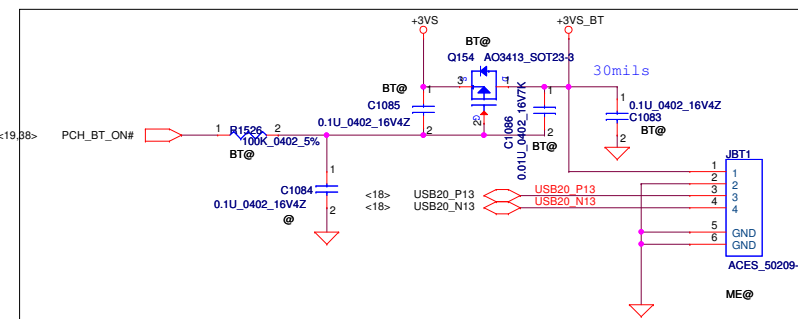
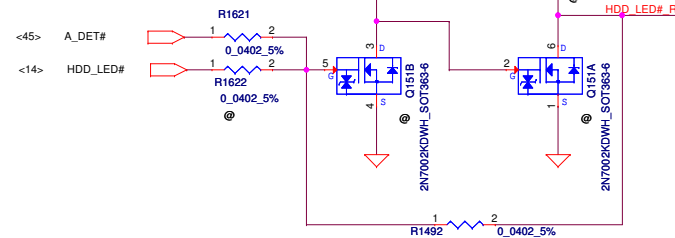
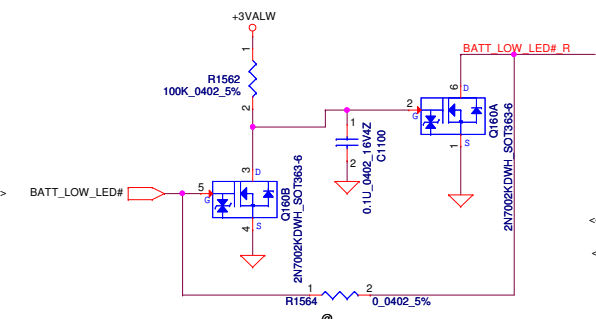
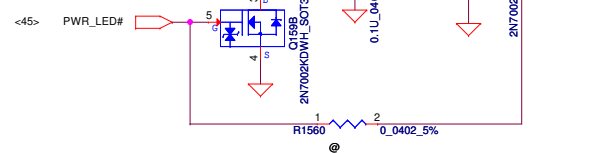
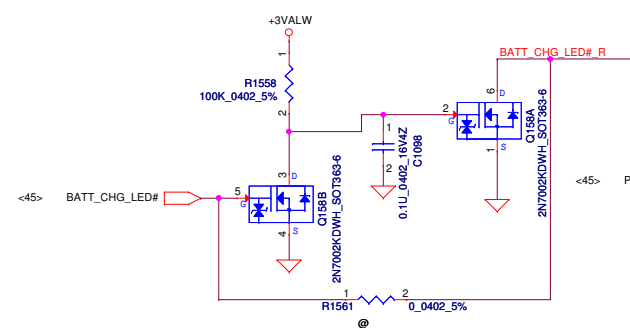
MIN PCIE:H_3P3 X 3 H_3P0 X 9



H_4P0X2P8N X 2

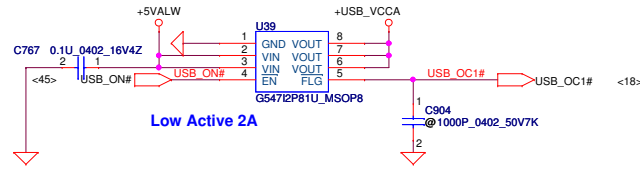


Keyboard:H_2P8X3

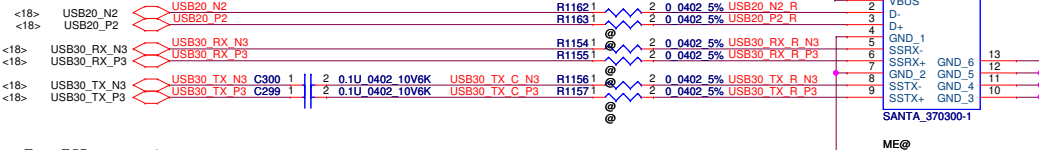
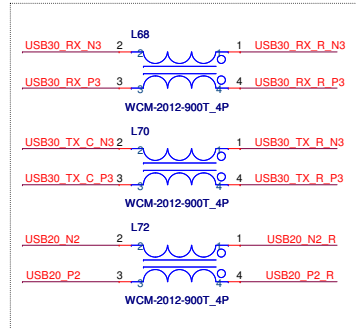


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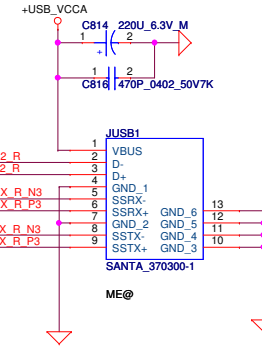
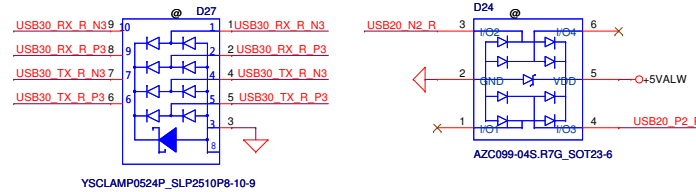
LEFT SIDE USB3.0 PORT X1



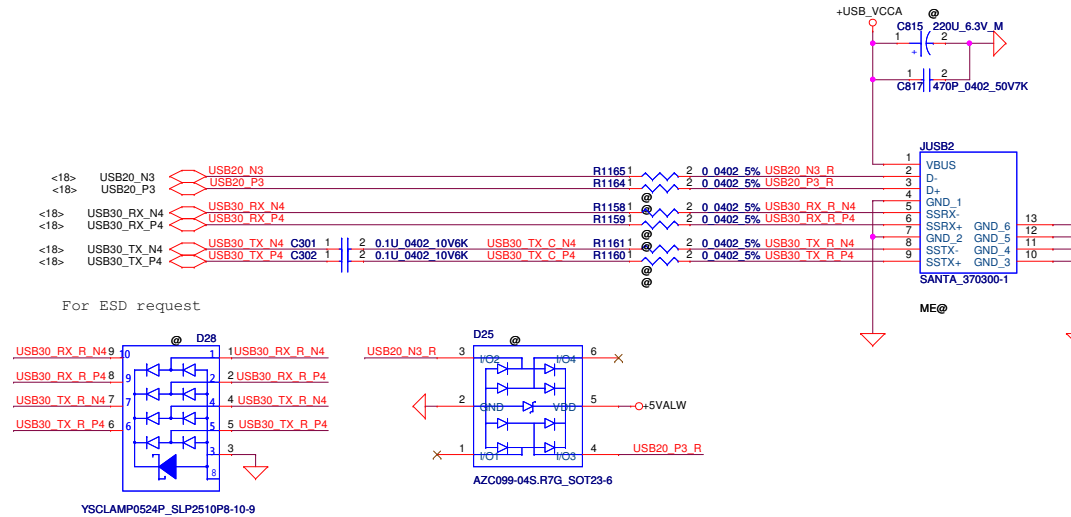
For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00



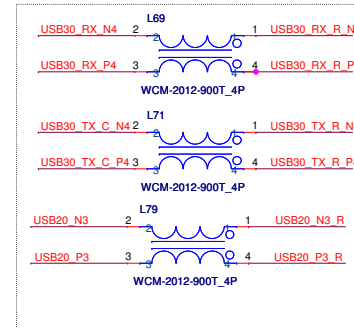
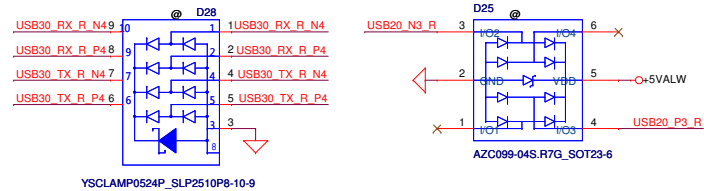
For ESD request



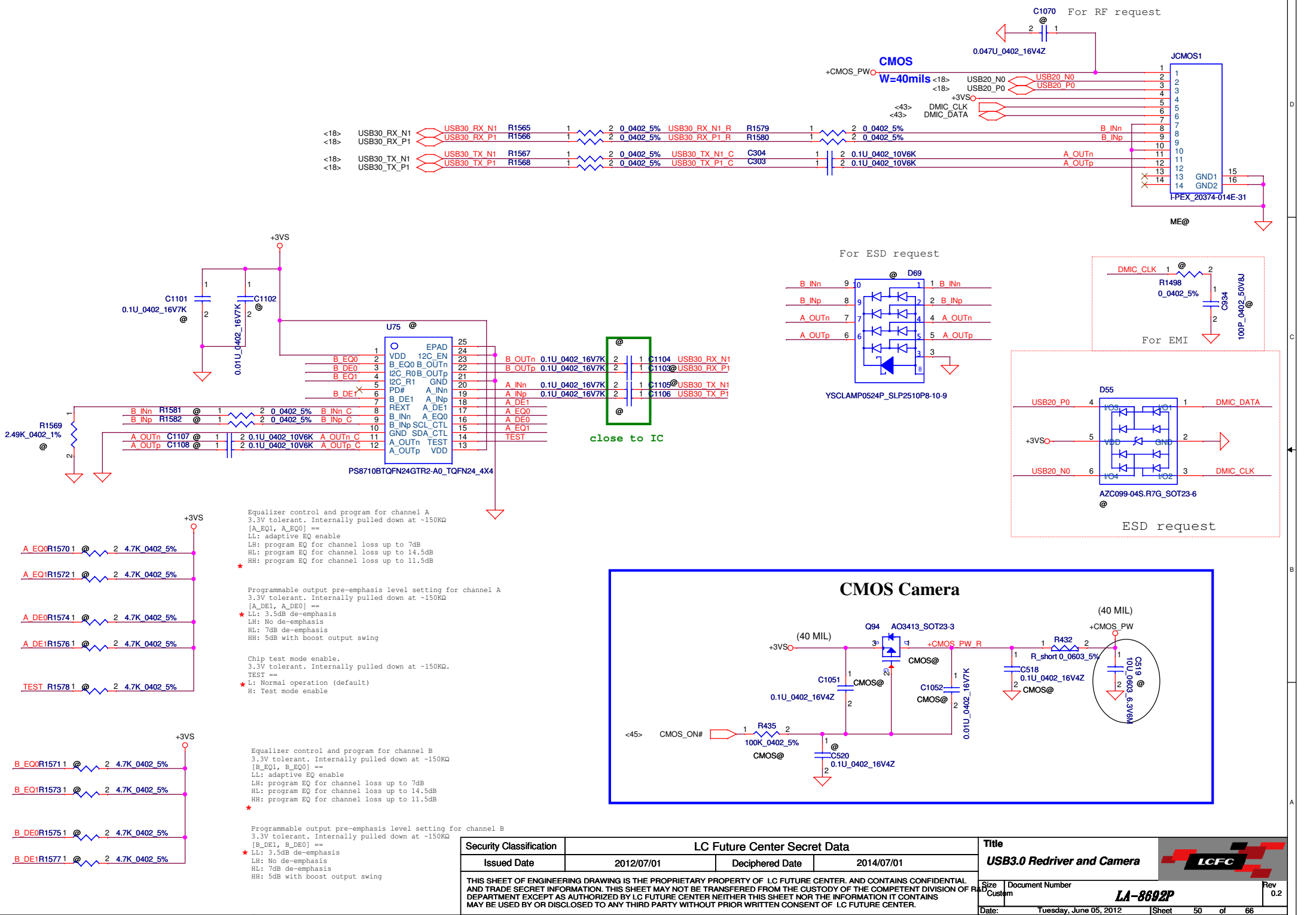
For EMI request
USB2.0 choke --> SM070000I00
USB3.0 Choke --> SM070001U00



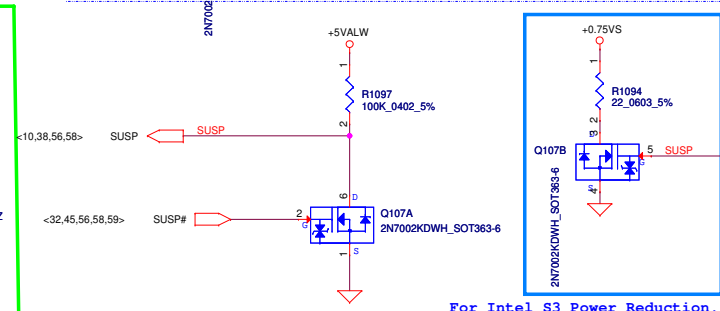
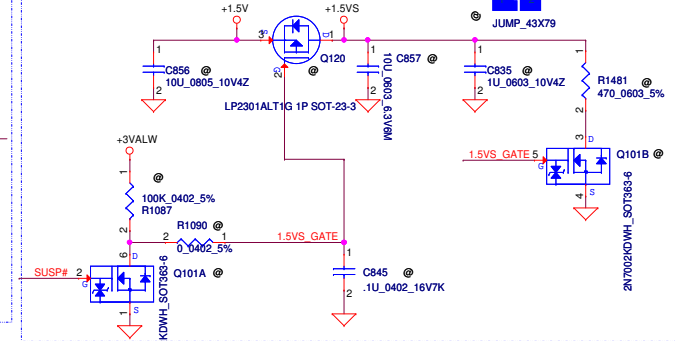
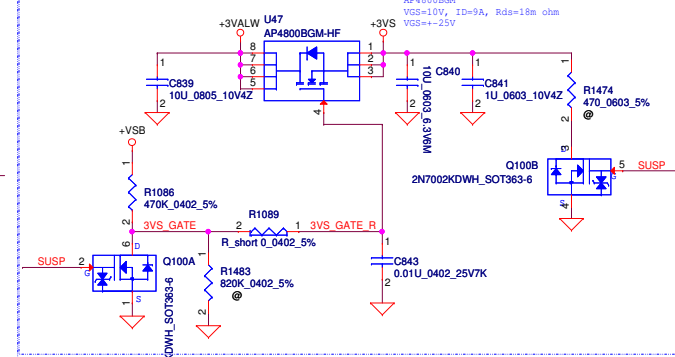
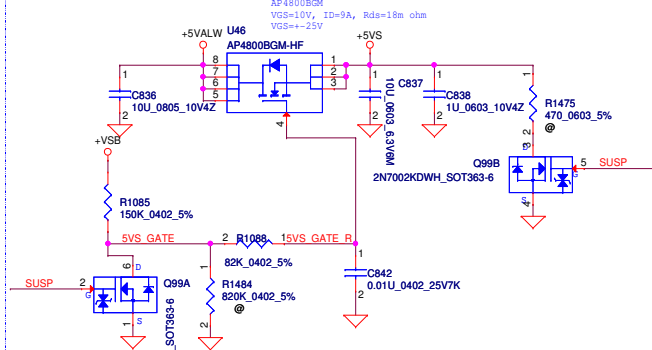
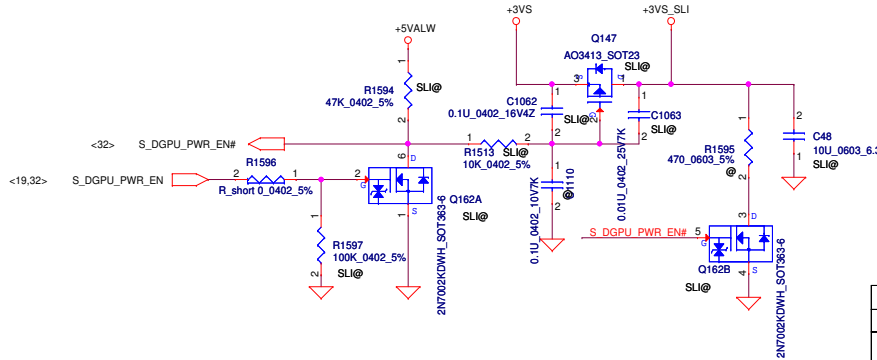
For ESD request



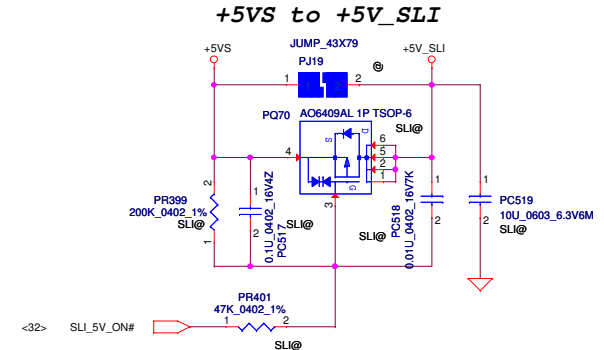
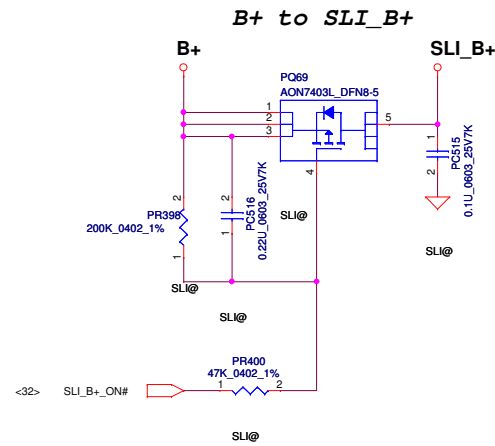
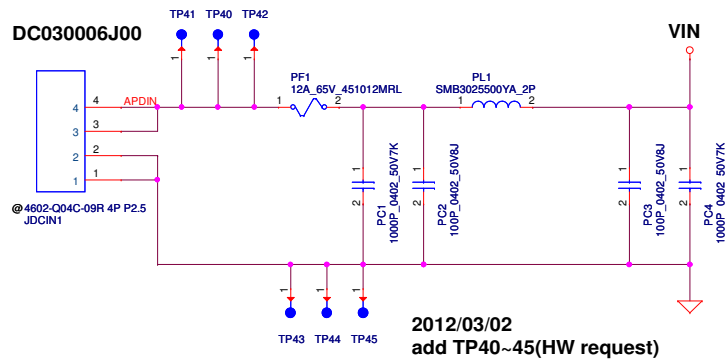
Security Classification	LC Future Center Secret Data			Title	USB3.0 ports		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Document Number	LA-8692P	Rev 0.2
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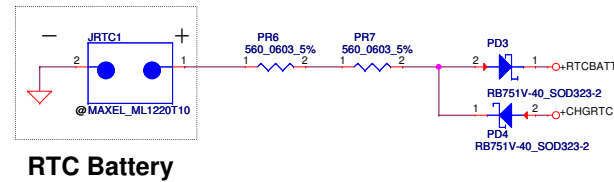
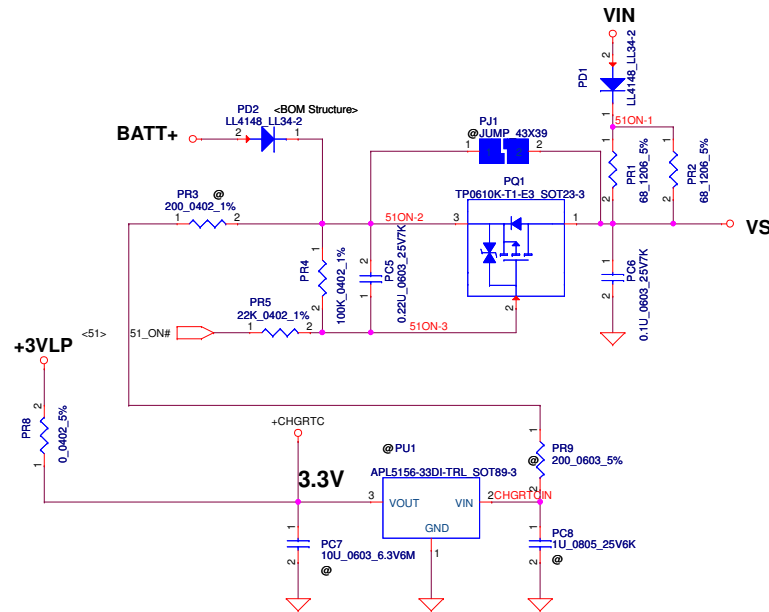
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/07/01	Deciphered Date	2014/07/01	other IO connector		
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				Date:	Tuesday, June 05, 2012	Sheet 51 of 66

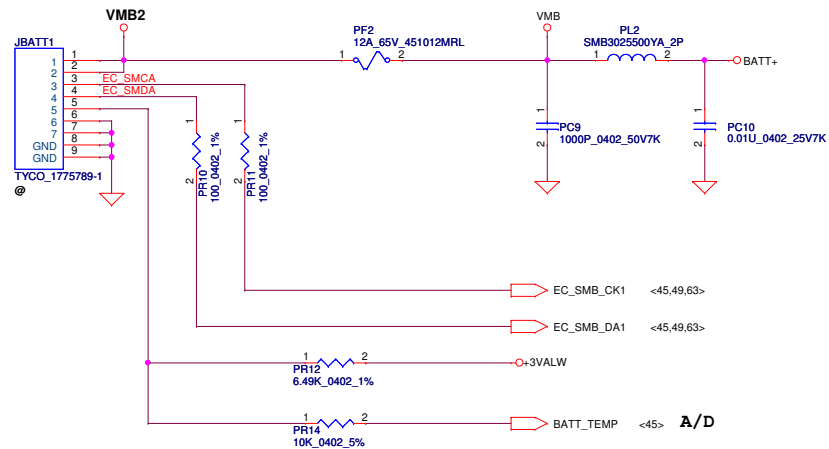
[illegible]

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/07/01	Deciphered Date	2014/07/01	DC Interface			
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2012/05/25
change Netname from +5VALW
to +5VS

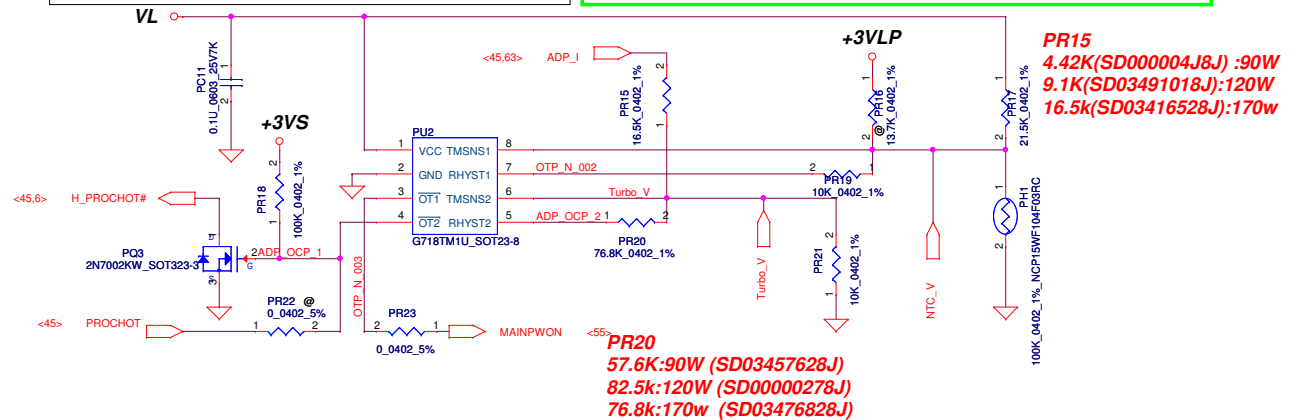




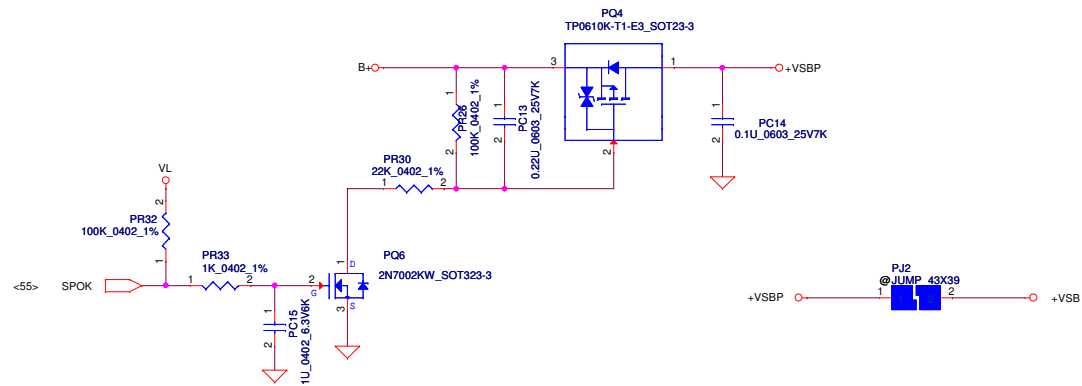
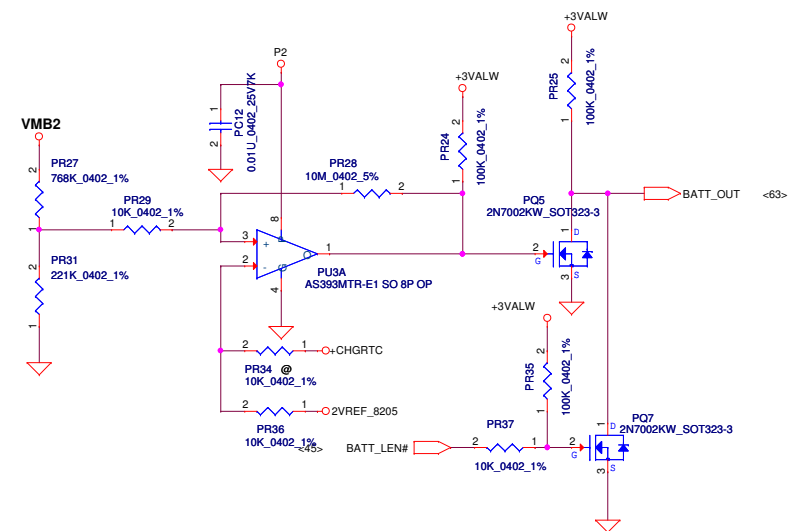
PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +/3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



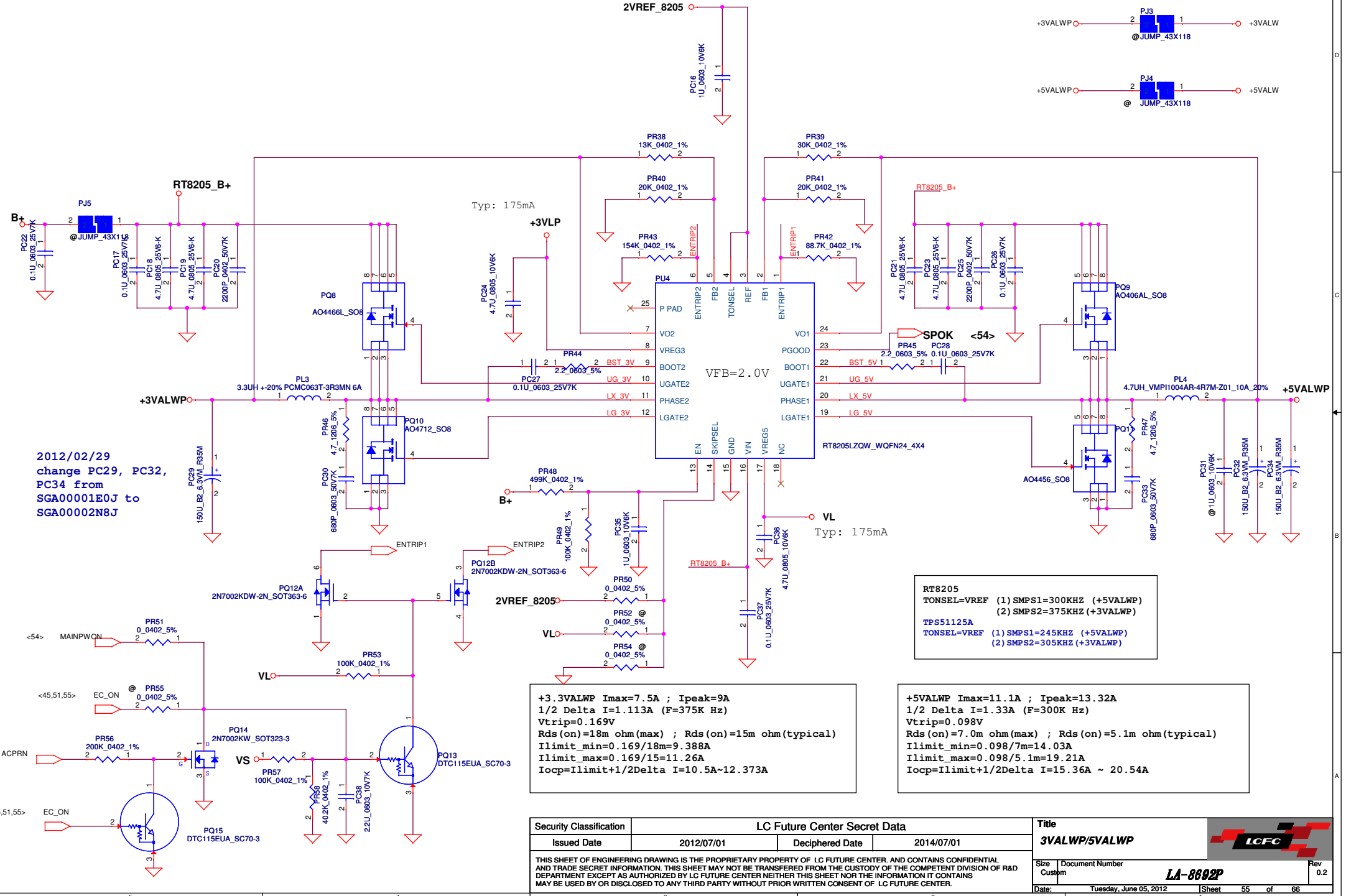
for power adapter ID
3V--- 90W
1.5V--- 120W
0V--- 170W



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		2014/07/01
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Title	Size	Document Number	Rev
BATTERY CONN/OTP	Custom	LA-8692P	0.2
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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



2012/02/29
change PC29, PC32,
PC34 from
SGA00001E0J to
SGA00002N8J

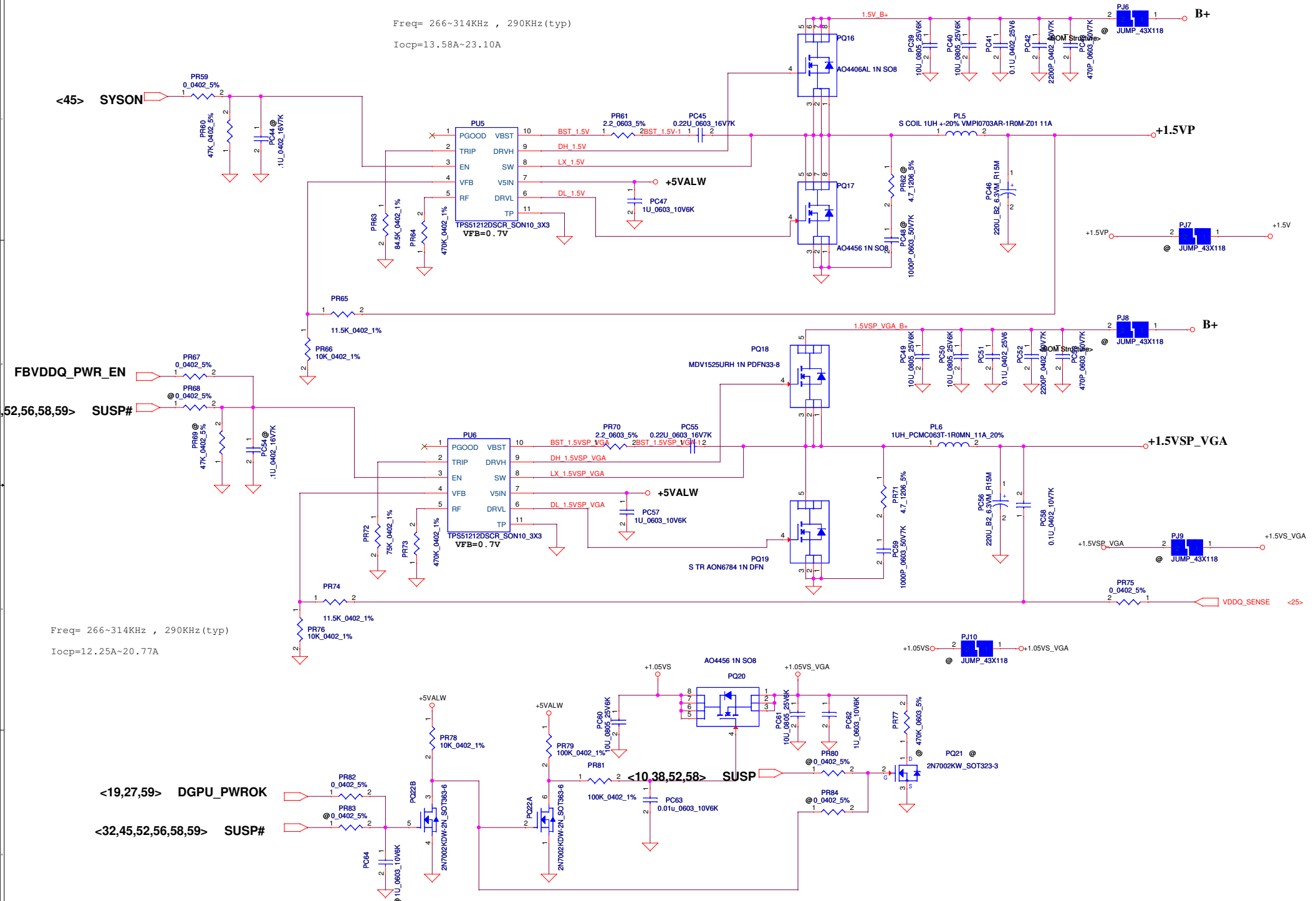
RT8205
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

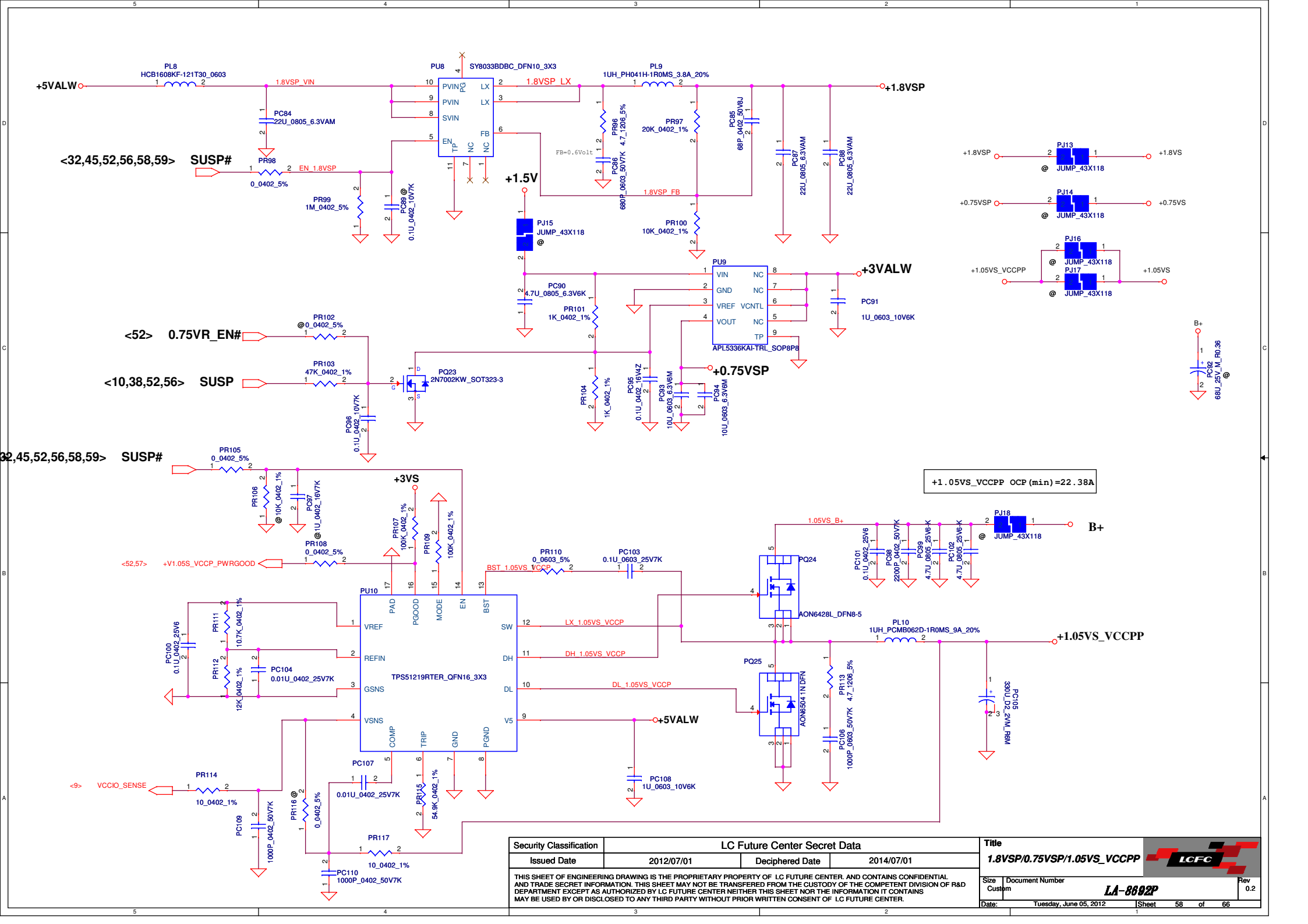
+3.3VALWP I_{max}=7.5A ; I_{peak}=9A
1/2 Delta I=1.113A (F=375K Hz)
V_{trip}=0.169V
R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
I_{limit_min}=0.169/18m=9.388A
I_{limit_max}=0.169/15=11.26A
I_{ocp}=I_{limit}+1/2Delta I=10.5A~12.373A

+5VALWP I_{max}=11.1A ; I_{peak}=13.32A
1/2 Delta I=1.33A (F=300K Hz)
V_{trip}=0.098V
R_{ds(on)}=7.0m ohm(max) ; R_{ds(on)}=5.1m ohm(typical)
I_{limit_min}=0.098/7m=14.03A
I_{limit_max}=0.098/5.1m=19.21A
I_{ocp}=I_{limit}+1/2Delta I=15.36A ~ 20.54A

Security Classification		LC Future Center Secret Data		Title	
Issued Date		2012/07/01	Deciphered Date	2014/07/01	3VALWP/5VALWP
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Freq= 266~314KHz , 290KHz(typ)
Iocp=13.58A~23.10A





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Title		1.8VSP/0.75VSP/1.05VS_VCCPP	
Size	Document Number	LA-8892P	
Custom			
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GL1:0.9V(110000)
GT:0.975V(101010)

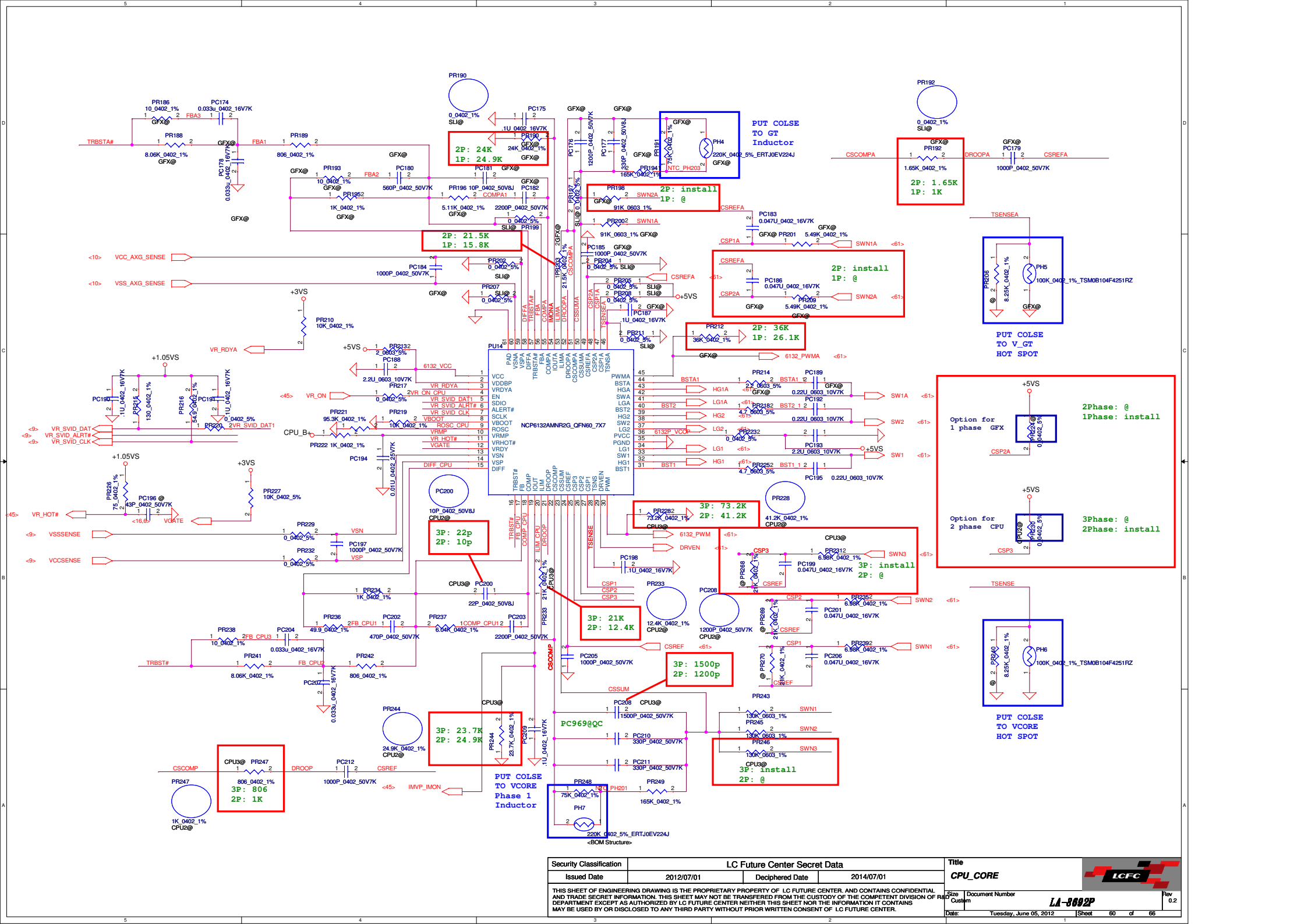
2012/04/26
change PC352 from 0
to Mount
2012/04/26
change PR313 from 0
to 75K

PQ801@GL1
PQ802@GL1

PQ806@GL1
PQ808@GL1

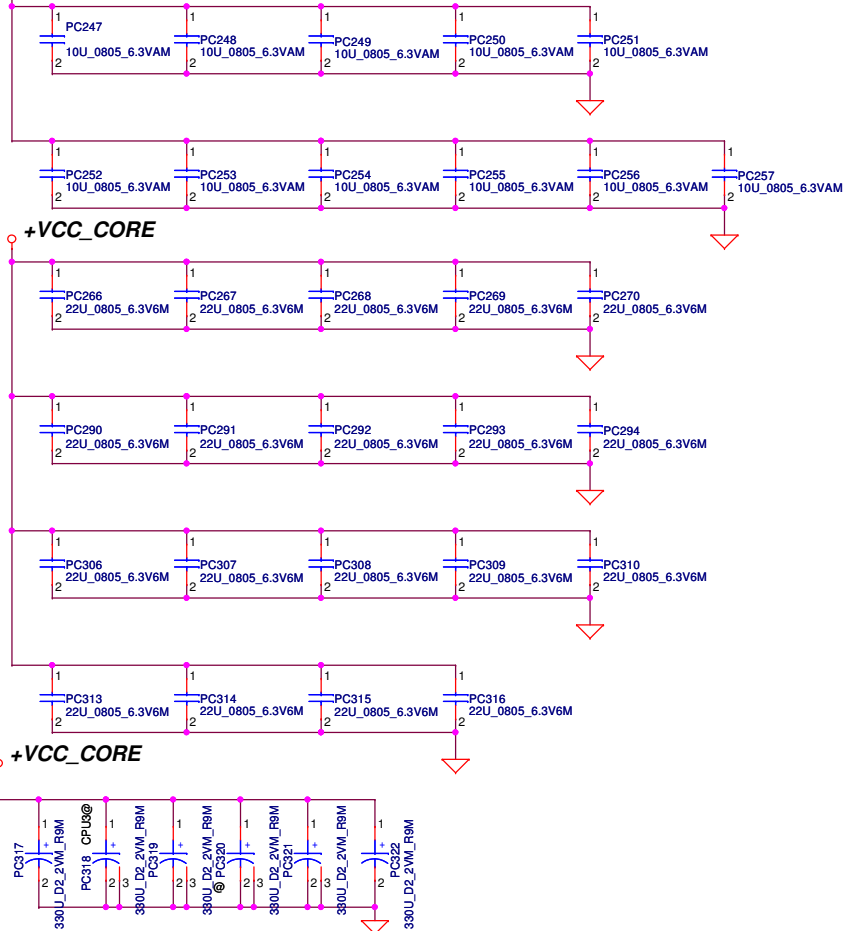
Layout Note:
Place near Phase1 Choke

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	Size	Document Number
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+VCC_CORE

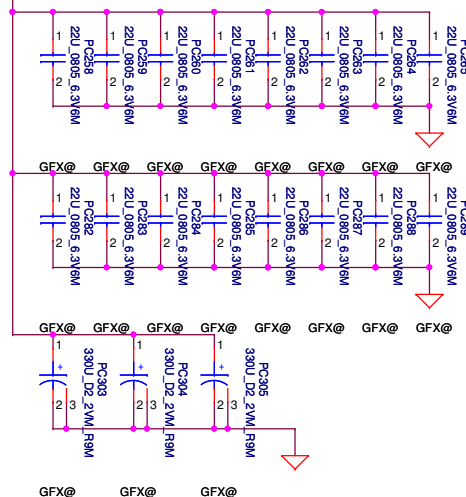
+CPU_CORE



2012/02/29
DC:PC317, PC319, PC321, PC322 (330uF/9m +-20% *4)
QC:PC317, PC318, PC319, PC321, PC322 (330uF/9m +-20% *5)
P/N:SGA0000610J (no link)

+VCC GFXCORE_AXG

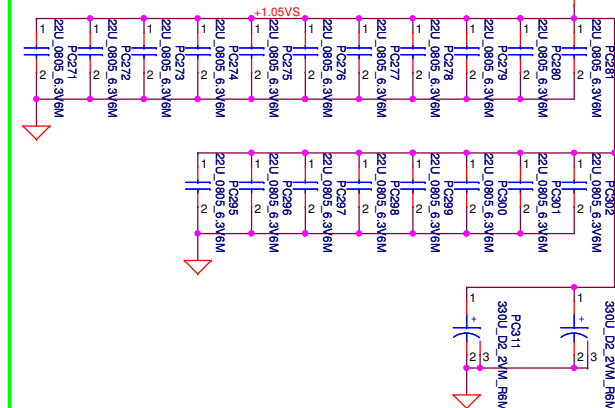
+VCC GFXCORE_AXG

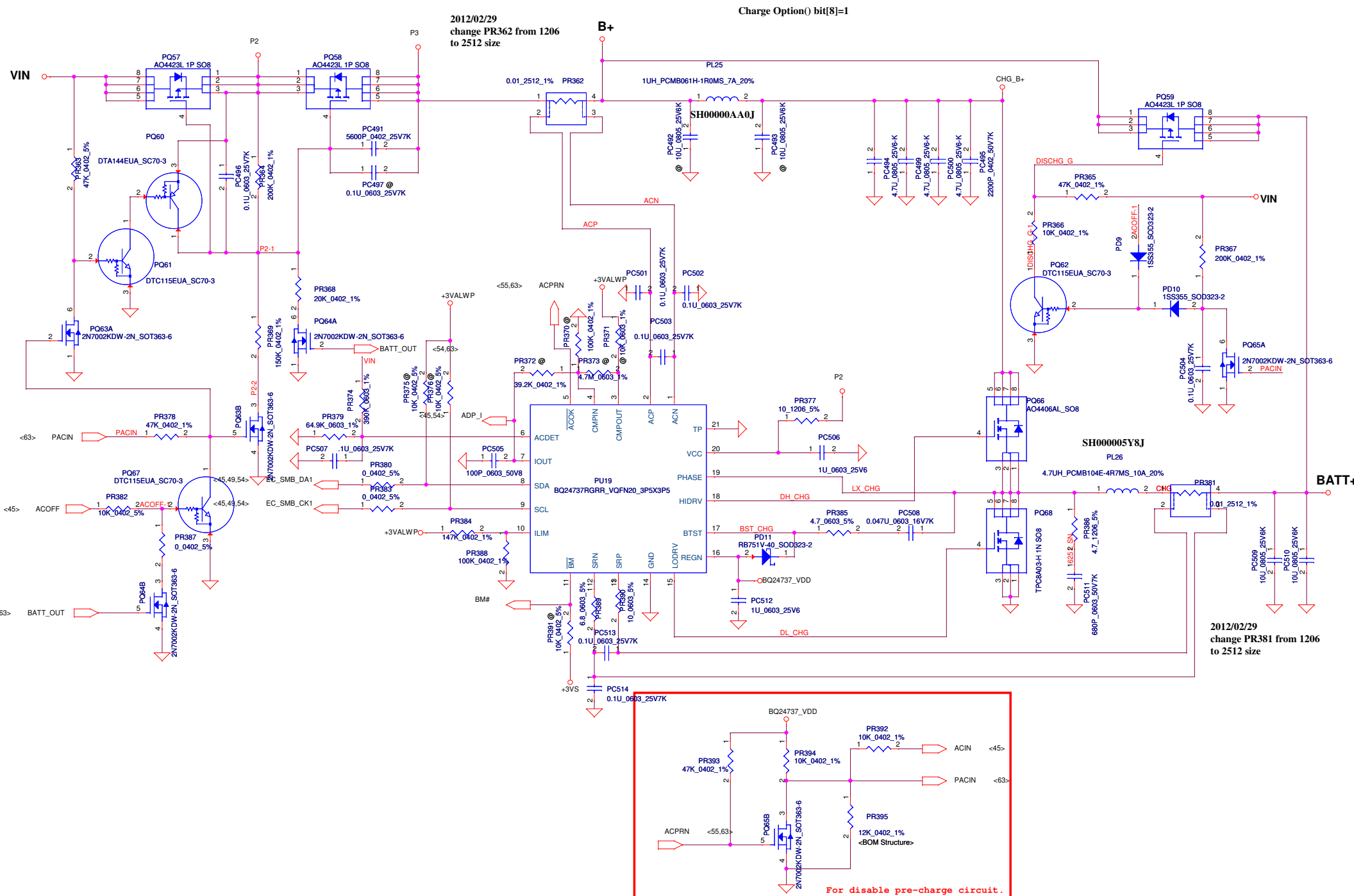


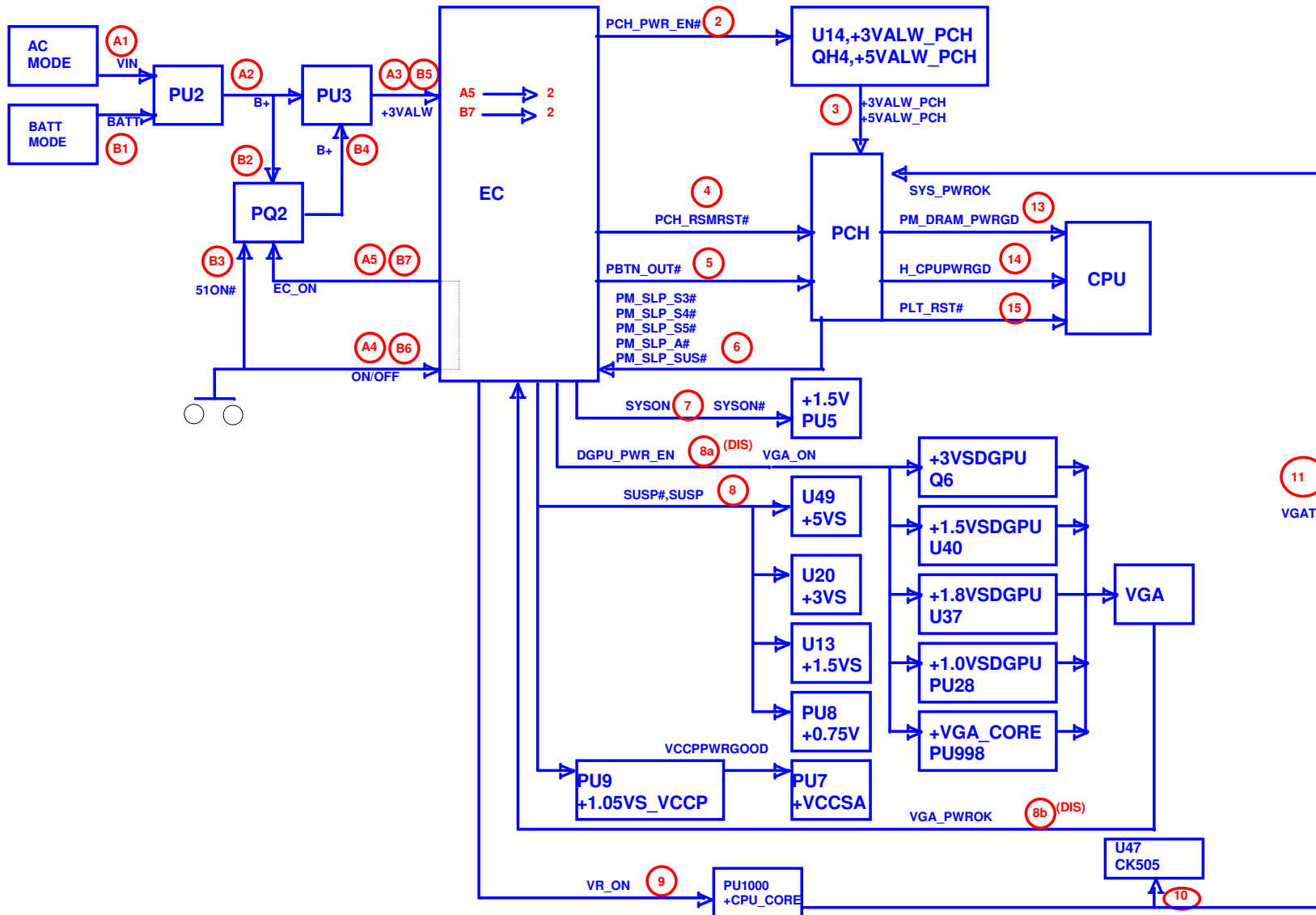
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS







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Title	Size	Document Number	Rev
Power sequence	Custom	LA-8692P	0.2
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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10	for VGA VID R-short	59	change PR318,PR319,PR320,PR321,PR322,PR323 footprint	201205/31	B test
11	Charger boost resistor For EMI	63	Change PR385 from 2.2ohm to 4.7ohm	201206/04	B test
12					
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16					
17					

Security Classification		LC Future Center Secret Data		Title			
Issued Date		2012/07/01		Deciphered Date			
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QIWEY3 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT TO DVT				
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457, R1455, R1447	Reserve SUSACK#, SUSWARN#, SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118, R1120, R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8, Q104, C533, C526, R436	Reserve for AOAC function
7		P36	Change JP1 pin2, 24, 52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18, 71, 72, 126, 128)	For DeepS3/AOAC function
9		P48	Reserve J11, J14, Q148, Q149, C38, C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For Dfx issue
11		P46	change U40, U69 symbol (without GND pad)	For Dfx issue
12		P47	change JP10 type to SP01001B800	For Dfx issue
13		P19	Reserve R207, R224 to contact WLAN wake even	Reserve for AOAC function
14		P41	Change JSPK1 type to SP02000H700	For Dfx issue
14		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
15		P23	Change CV37, CV38 to 22P	For Crystal EA request
16		P37	Change C968, C969 to 33P	For Crystal EA request