QIQY5

Whisky3.0 (Y490)

LA-8691P Rev0.2 Schematic

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT1-A2 + 2nd VGA N13P GT1-A2

2012-02-05 Rev0.2

Security Classification	Compal Secret Data		
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Title: *Cover Page*

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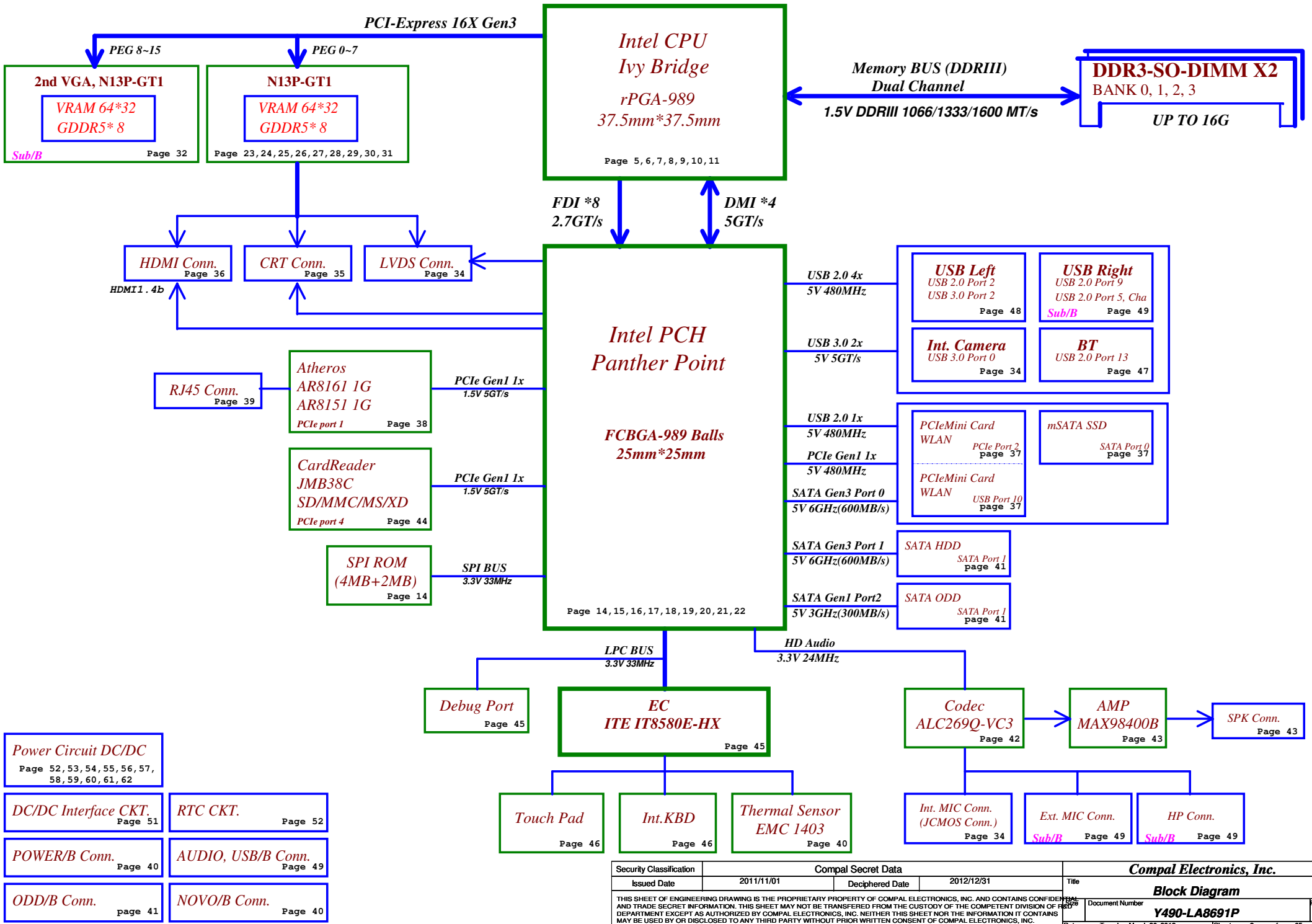

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Title: **Block Diagram**

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI 1	0	Camera
	XHCI 2	1	
		2	USB Port (Left Side)
	XHCI 3	3	
	XHCI 4	4	
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000T10J

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Title: *Notes List*

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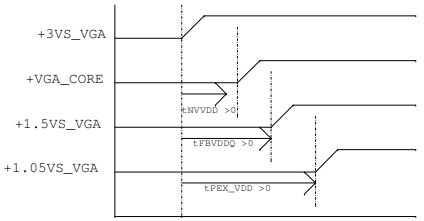
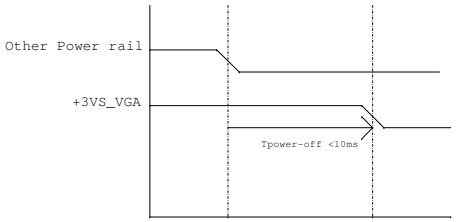
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	_	VGA_ENVDD
GPIO4	OUT	_	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	_	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	_	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	_	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	_	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

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Title: VGA Notes List

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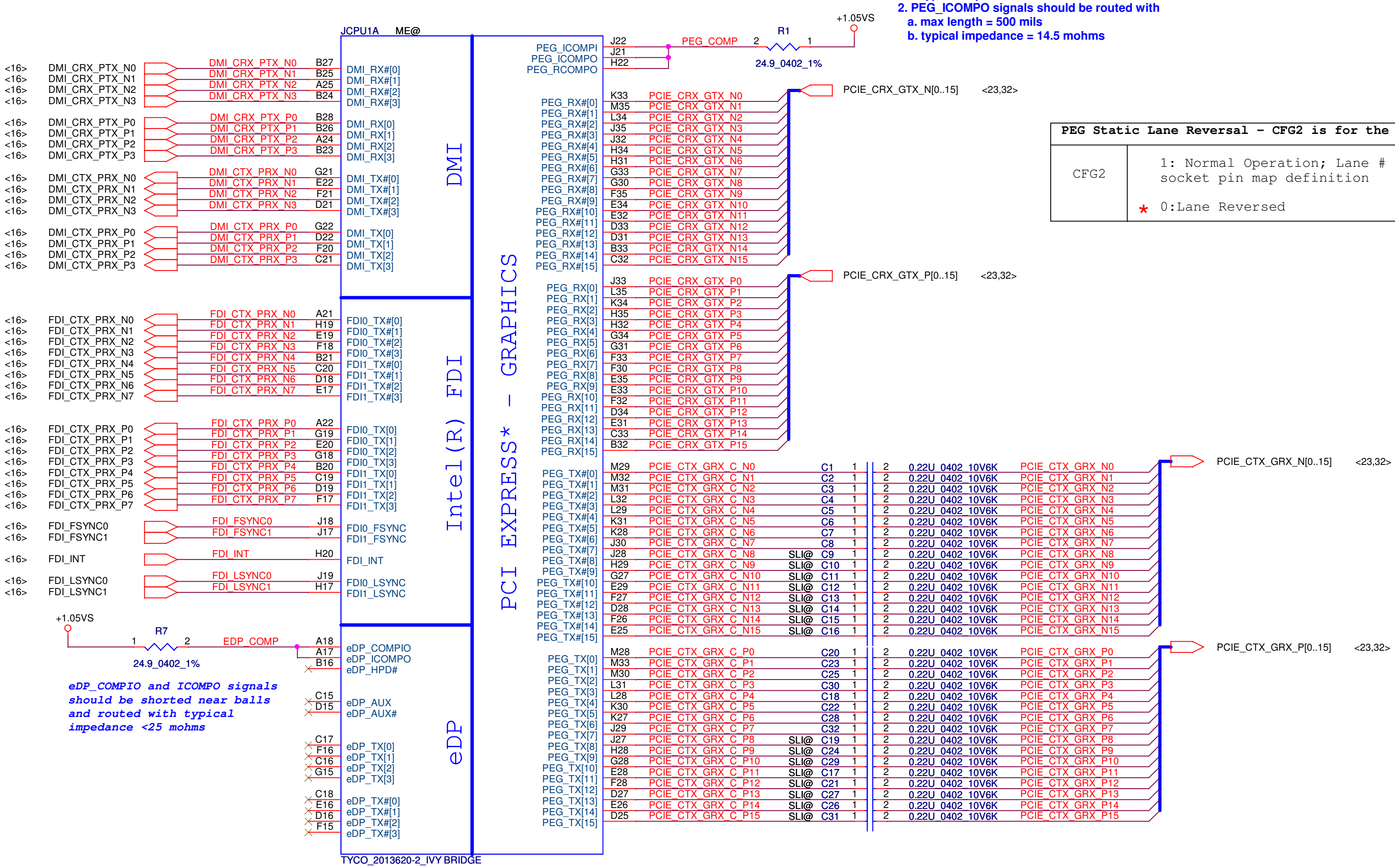
1. PEG_ICOMPI and RCOMPO signals should be shorted and routed with
   a. max length = 500 mils
   b. typical impedance = 43 mohms
2. PEG_ICOMPO signals should be routed with
   a. max length = 500 mils
   b. typical impedance = 14.5 mohms



JCPU1A ME@
DMI
Intel(R) FDI
eDP
PCI EXPRESS* - GRAPHICS
TYCO_2013620-2_IVY BRIDGE
+1.05VS
R1
24.9_0402_1%
PEG_COMP
PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22
R7
24.9_0402_1%
EDP_COMP
eDP_COMPIO A18
eDP_ICOMPO A17
eDP_HPD# B16
eDP_AUX C15
eDP_AUX# D15
eDP_TX[0] C17
eDP_TX[1] F16
eDP_TX[2] C16
eDP_TX[3] G15
eDP_TX#[0] C18
eDP_TX#[1] E16
eDP_TX#[2] D16
eDP_TX#[3] F15
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
<16> DMI_CRX_PTX_N0 B27 DMI_RX#[0]
<16> DMI_CRX_PTX_N1 B25 DMI_RX#[1]
<16> DMI_CRX_PTX_N2 A25 DMI_RX#[2]
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<16> FDI_CTX_PRX_N2 E19 FDI0_TX#[2]
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<16> FDI_CTX_PRX_P5 C19 FDI1_TX[1]
<16> FDI_CTX_PRX_P6 D19 FDI1_TX[2]
<16> FDI_CTX_PRX_P7 F17 FDI1_TX[3]
<16> FDI_FSYNC0 J18 FDI0_FSYNC
<16> FDI_FSYNC1 J17 FDI1_FSYNC
<16> FDI_INT H20 FDI_INT
<16> FDI_LSYNC0 J19 FDI0_LSYNC
<16> FDI_LSYNC1 H17 FDI1_LSYNC
PEG_RX#[0] K33 PCIE_CRX_GTX_N0
PEG_RX#[1] M35 PCIE_CRX_GTX_N1
PEG_RX#[2] L34 PCIE_CRX_GTX_N2
PEG_RX#[3] J35 PCIE_CRX_GTX_N3
PEG_RX#[4] J32 PCIE_CRX_GTX_N4
PEG_RX#[5] H34 PCIE_CRX_GTX_N5
PEG_RX#[6] H31 PCIE_CRX_GTX_N6
PEG_RX#[7] G33 PCIE_CRX_GTX_N7
PEG_RX#[8] G30 PCIE_CRX_GTX_N8
PEG_RX#[9] F35 PCIE_CRX_GTX_N9
PEG_RX#[10] E34 PCIE_CRX_GTX_N10
PEG_RX#[11] E32 PCIE_CRX_GTX_N11
PEG_RX#[12] D33 PCIE_CRX_GTX_N12
PEG_RX#[13] D31 PCIE_CRX_GTX_N13
PEG_RX#[14] B33 PCIE_CRX_GTX_N14
PEG_RX#[15] C32 PCIE_CRX_GTX_N15
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PEG_RX[3] H35 PCIE_CRX_GTX_P3
PEG_RX[4] H32 PCIE_CRX_GTX_P4
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PEG_TX#[8] J28 PCIE_CTX_GRX_C_N8 SLI@ C9 0.22U_0402_10V6K PCIE_CTX_GRX_N8
PEG_TX#[9] H29 PCIE_CTX_GRX_C_N9 SLI@ C10 0.22U_0402_10V6K PCIE_CTX_GRX_N9
PEG_TX#[10] G27 PCIE_CTX_GRX_C_N10 SLI@ C11 0.22U_0402_10V6K PCIE_CTX_GRX_N10
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PEG_TX[6] K27 PCIE_CTX_GRX_C_P6 C28 0.22U_0402_10V6K PCIE_CTX_GRX_P6
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PEG_TX[13] D27 PCIE_CTX_GRX_C_P13 SLI@ C27 0.22U_0402_10V6K PCIE_CTX_GRX_P13
PEG_TX[14] E26 PCIE_CTX_GRX_C_P14 SLI@ C26 0.22U_0402_10V6K PCIE_CTX_GRX_P14
PEG_TX[15] D25 PCIE_CTX_GRX_C_P15 SLI@ C31 0.22U_0402_10V6K PCIE_CTX_GRX_P15
PCIE_CTX_GRX_P[0..15] <23,32>

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

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Title: **PROCESSOR(1/7) DMI,FDI,PEG**

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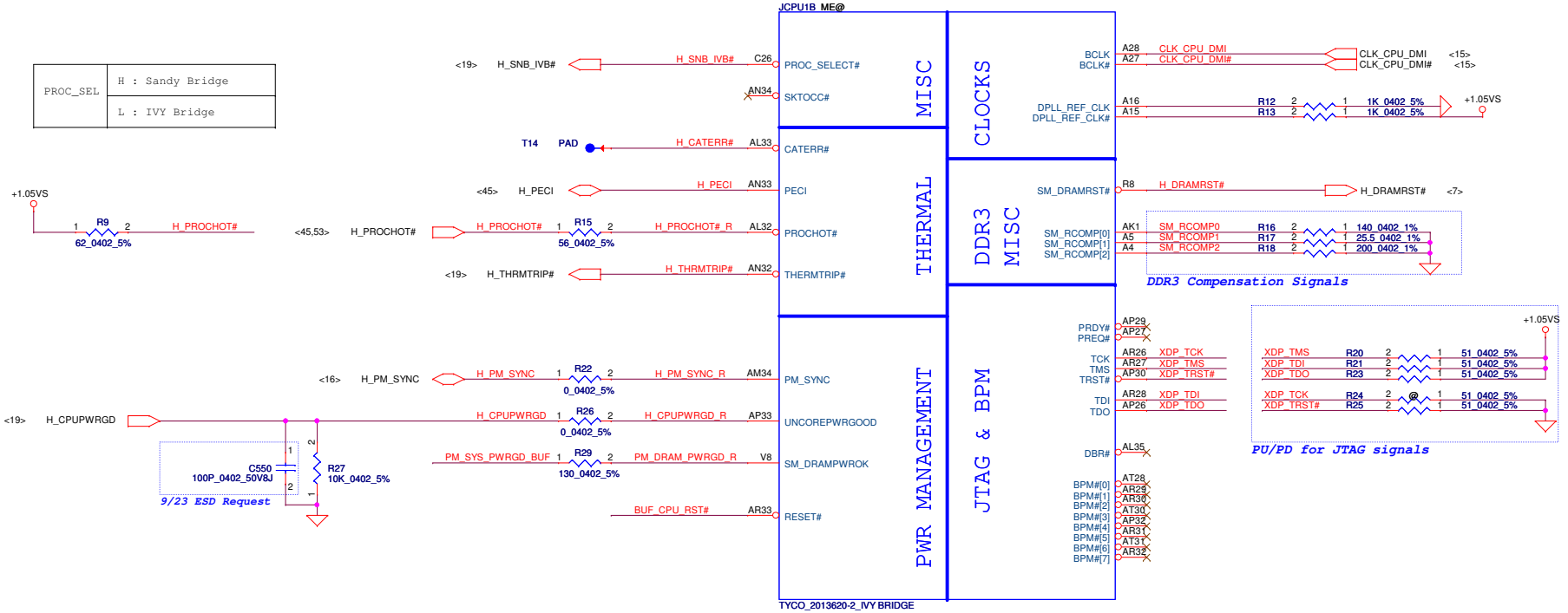
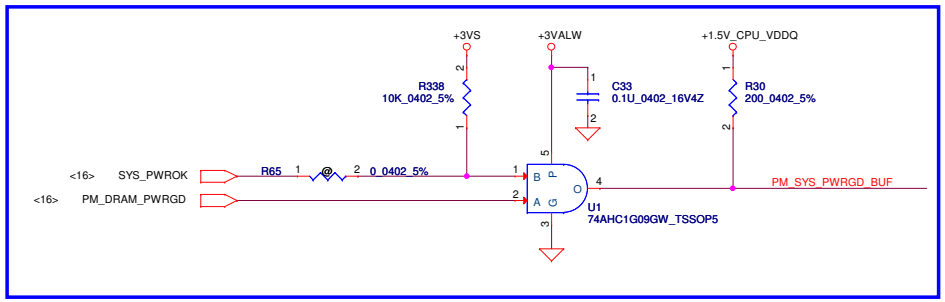
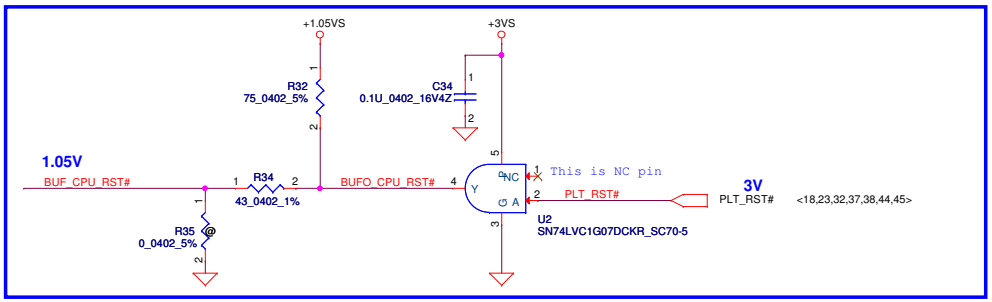




Buffered Reset to CPU



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Title: PROCESSOR(2/7) PM,XDP,CLK

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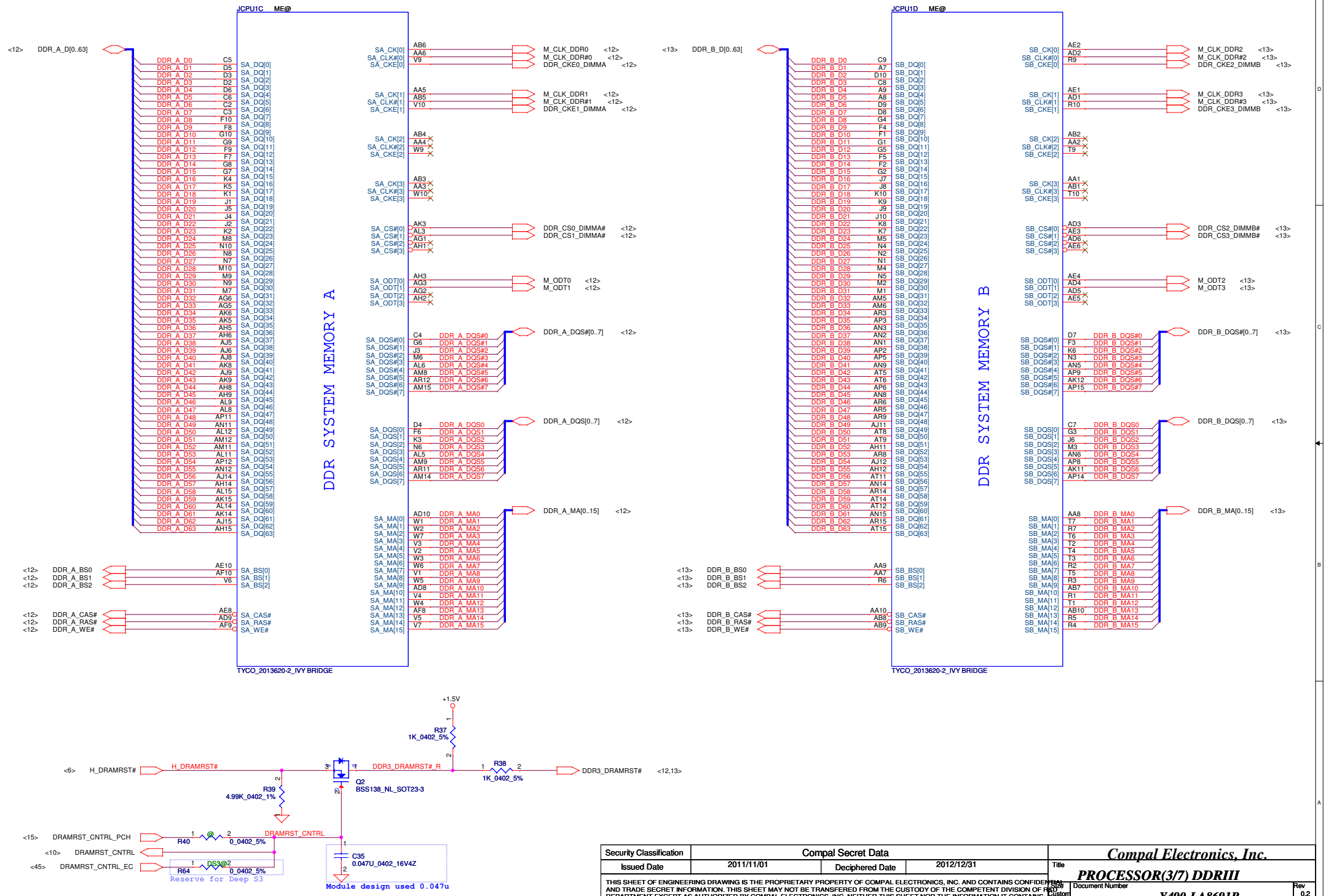

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Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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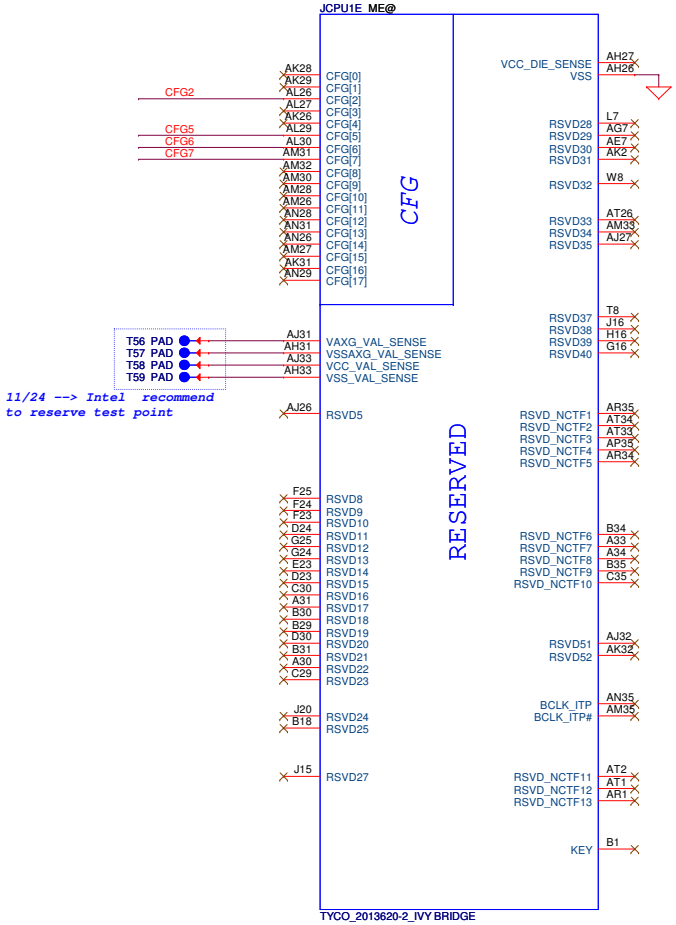
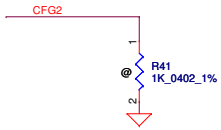
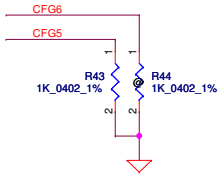


CFG Straps for Processor

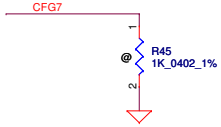


PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
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POWER

JCPU1F ME@

+VCC_CORE

QC=94A
DC=53A

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

+1.05VS

8.5A

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

PEG AND DDR

SVID

+1.05VS

C36 0.1U_0402_10V7K @

R46 75_0402_5%

Reserve 0.1u to avoid noise

Place the PU resistor close to CPU

VIDALERT# VIDSCLK VIDSOUT

AJ29 H_CPU_SVIDALRT# R47 43_0402_5%
AJ30 H_CPU_SVIDCLK R48 0_0402_5%
AJ28 H_CPU_SVIDDAT R49 0_0402_5%

VR_SVID_ALRT# <59>
VR_SVID_CLK <59>
VR_SVID_DAT <59>

R50 130_0402_5% +1.05VS

Place the PU resistor close to CPU

SENSE LINES

+VCC_CORE

R51 100_0402_1%

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

VCC_SENSE VSS_SENSE

AJ35 VCCSENSE_R R52 0_0402_5% VCCSENSE
AJ34 VSSSENSE_R R53 0_0402_5% VSSSENSE

VCCSENSE <59>
VSSSENSE <59>

+1.05VS

VCCIO_SENSE VSS_SENSE_VCCIO

B10 VCCIO_SENSE R1294 10_0402_1%
A10 VSSIO_SENSE R1297 10_0402_1%

VCCIO_SENSE <57>

R54 100_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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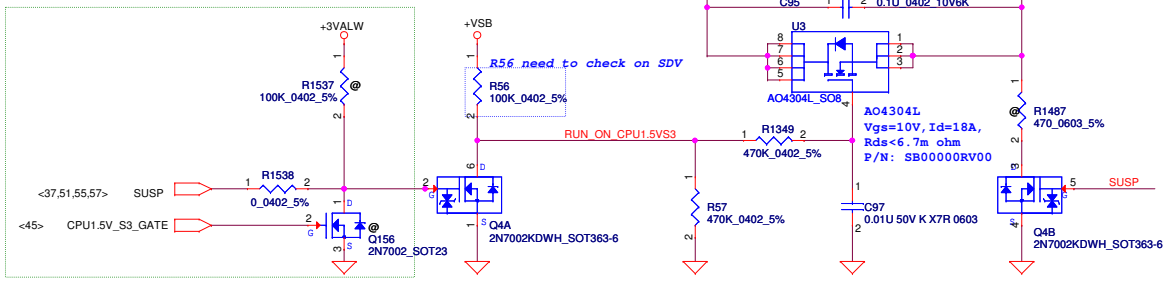
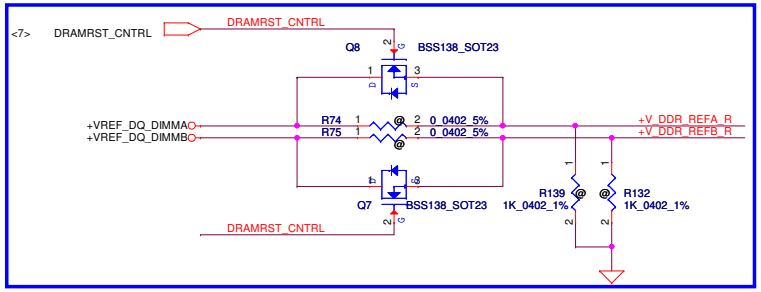
+1.5V_CPU_VDDQ

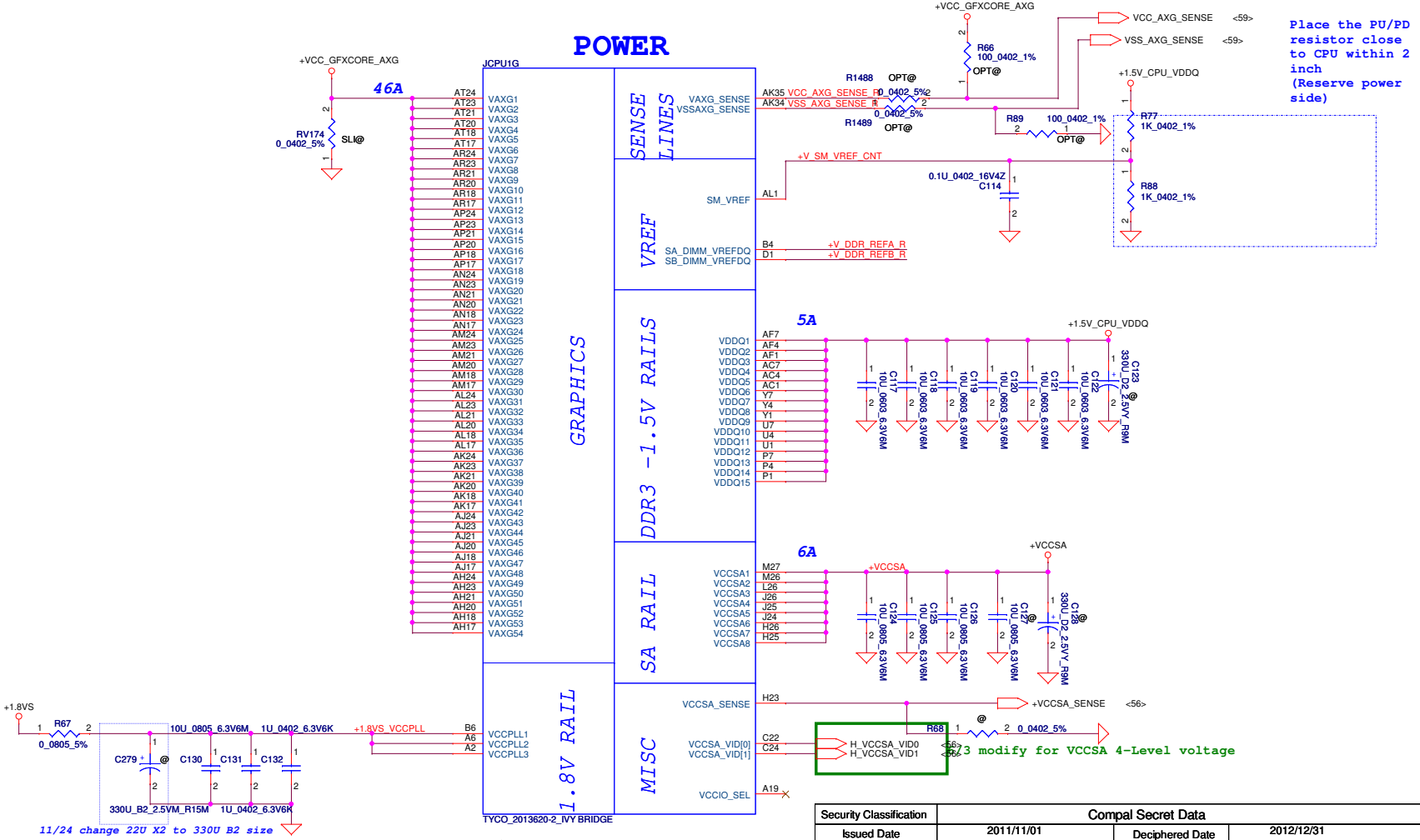
For Deep S3





6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

POWER



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **PROCESSOR(6/7) PWR**

Size: Custom | Document Number: **Y490-LA8691P** | Rev: 0.2

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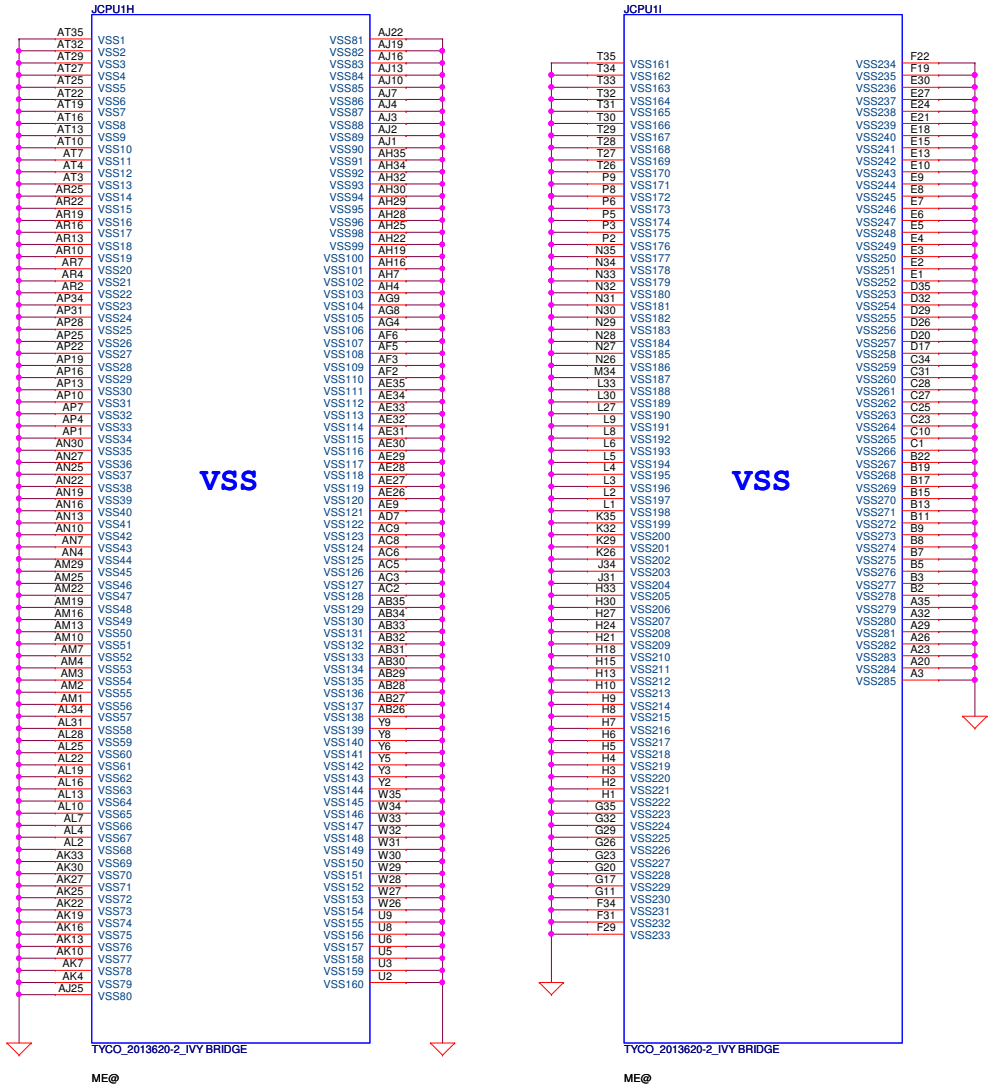

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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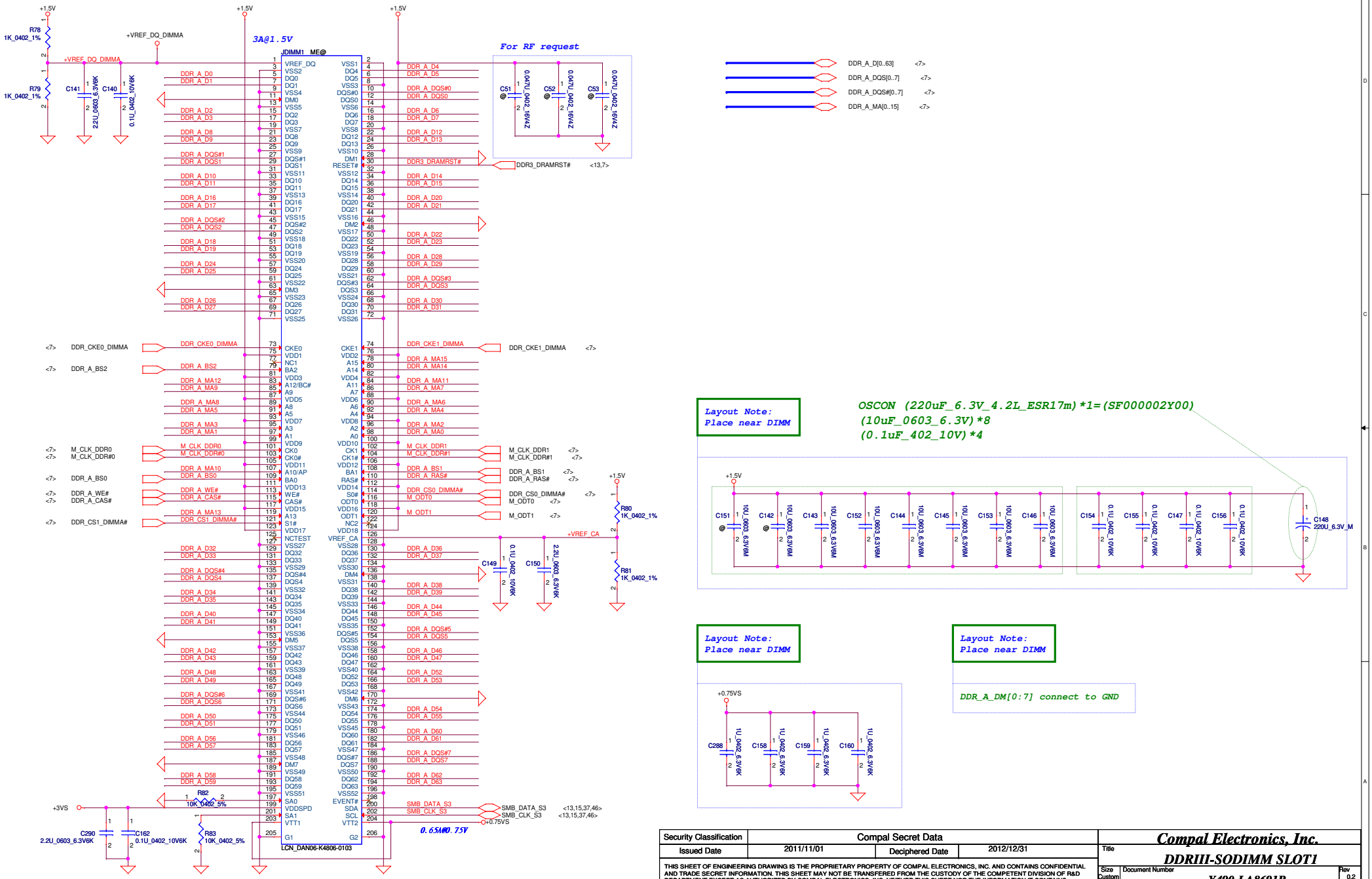
DDR3 SO-DIMM A



Layout Note:
Place near DIMM

OSCON (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

DDR_A_DM[0:7] connect to GND

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

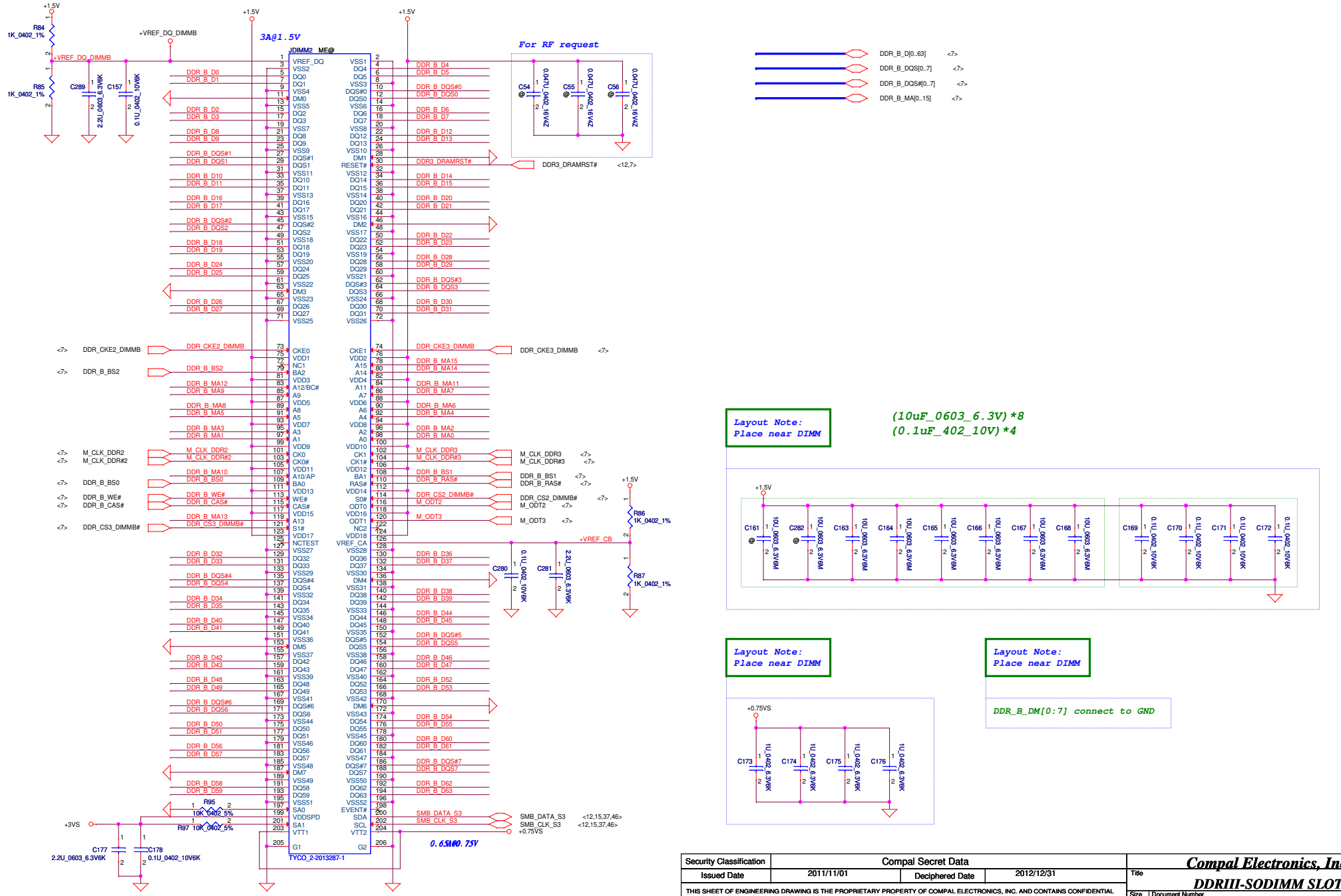
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 12 of 65

DDR3 SO-DIMM B



DDR_B_D[0..63] <7>
DDR_B_DQS[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_MA[0..15] <7>

Layout Note:
Place near DIMM

*(10uF_0603_6.3V)*8*
*(0.1uF_402_10V)*4*

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

DDR_B_DM[0:7] connect to GND

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size | Document Number: **Y490-LA8691P** | Rev: 0.2

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W=20mils W=20mils
+RTCBATT R99 1K_0402_5% +RTCVCC
C179 1U_0603_10V4Z

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN
* H : Integrated VRM enable (Default)
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS
R105 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3V_PCH
R106 1K_0402_5% HDA_SDOUT

* Low = Disabled (Default)
High = Enabled
[Flash Descriptor Security Overide]

+3V_PCH
R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
* 1.5V when smapled high (Default)
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

+RTCVCC
C183 1U_0603_10V4Z @ JCMOS SHORT PADS
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z @ JME SHORT PADS

CMOS

U4A

PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
<42> HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<42> HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
<45> ME_FLASH R109 0_0402_5% HDA_SDOUT A36 HDA_SDO
R107 1K_0402_1% PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
+3V_PCH R317 10K_0402_5% PCH_GPIO13 N32 HDA_DOCK_RST# / GPIO13
IHDA

R110 51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SPI_CLK_PCH_0 R298 33_0402_5%
SPI_CLK_PCH_1 R299 33_0402_5%
SPI_CLK_PCH T3 SPI_CLK
SPI_SB_CS0#_R R130 0_0402_5% SPI_SB_CS0# Y14 SPI_CS0#
SPI_CS1#_R R303 0_0402_5% SPI_CS1# T1 SPI_CS1#
SPI_SI_R R133 33_0402_5%
SPI_SI_R1 R204 33_0402_5% SPI_SI V4 SPI_MOSI
SPI_SO_L R131 33_0402_5%
SPI_SO_L1 R294 33_0402_5% SPI_SO_R U3 SPI_MISO
SPI

PANTHER-POINT_FCBGA989

EC and Mini card debug port

LPC
FWH0 / LAD0 C38 LPC_AD0 — LPC_AD0 <37,45>
FWH1 / LAD1 A38 LPC_AD1 — LPC_AD1 <37,45>
FWH2 / LAD2 B37 LPC_AD2 — LPC_AD2 <37,45>
FWH3 / LAD3 C37 LPC_AD3 — LPC_AD3 <37,45>
FWH4 / LFRAME# D36 LPC_FRAME# — LPC_FRAME# <37,45>
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5 SERIRQ — R104 10K_0402_5% +3VS — SERIRQ <45>

SATA 6G
SATA0RXN AM3 SATA_DTX_C_IRX_N0
SATA0RXP AM1 SATA_DTX_C_IRX_P0
SATA0TXN AP7 SATA_ITX_C_DRX_N0 C184 0.01U_0402_16V7K SATA_ITX_DRX_N0
SATA0TXP AP5 SATA_ITX_C_DRX_P0 C185 0.01U_0402_16V7K SATA_ITX_DRX_P0
SSD
SATA_DTX_C_IRX_N0 <37>
SATA_DTX_C_IRX_P0 <37>
SATA_ITX_DRX_N0 <37>
SATA_ITX_DRX_P0 <37>

SATA1RXN AM10 SATA_DTX_C_IRX_N1
SATA1RXP AM8 SATA_DTX_C_IRX_P1
SATA1TXN AP11 SATA_ITX_C_DRX_N1 C273 0.01U_0402_16V7K SATA_ITX_DRX_N1
SATA1TXP AP10 SATA_ITX_C_DRX_P1 C272 0.01U_0402_16V7K SATA_ITX_DRX_P1
HDD
SATA_DTX_C_IRX_N1 <41>
SATA_DTX_C_IRX_P1 <41>
SATA_ITX_DRX_N1 <41>
SATA_ITX_DRX_P1 <41>

SATA2RXN AD7 SATA_DTX_C_IRX_N2
SATA2RXP AD5 SATA_DTX_C_IRX_P2
SATA2TXN AH5 SATA_ITX_C_DRX_N2 C186 0.01U_0402_16V7K SATA_ITX_DRX_N2_CONN
SATA2TXP AH4 SATA_ITX_C_DRX_P2 C187 0.01U_0402_16V7K SATA_ITX_DRX_P2_CONN
ODD
SATA_DTX_C_IRX_N2 <41>
SATA_DTX_C_IRX_P2 <41>
SATA_ITX_DRX_N2_CONN <41>
SATA_ITX_DRX_P2_CONN <41>

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1

SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11 — +1.05VS_VCC_SATA
SATAICOMPI Y10 — SATA_COMP R111 37.4_0402_1%
SATA3RCOMPO AB12 — +1.05VS_SATA3
SATA3COMPI AB13 — SATA3_COMP R113 49.9_0402_1%
SATA3RBIAS AH1 — RBIAS_SATA3 R115 750_0402_1%
SATALED# P3 — HDD_LED# R120 10K_0402_5% +3VS — HDD_LED# <47>
SATA0GP / GPIO21 V14 — PCH_GPIO21 R119 10K_0402_5% +3VS
SATA1GP / GPIO19 P1 — SATA_DET# R316 10K_0402_5% +3VS — SATA_DET# <37>
SATA

HDA AUDIO

<42> HDA_BITCLK_AUDIO — R112 33_0402_5% — HDA_BIT_CLK
<42> HDA_SYNC_AUDIO — R114 33_0402_5% — HDA_SYNC_R
<42> HDA_RST_AUDIO# — R116 33_0402_5% — HDA_RST#
<42> HDA_SDOUT_AUDIO — R118 33_0402_5% — HDA_SDOUT

+5VS
R1353 1M_0402_5%
Q10 BSS138_NL_SOT23-3
HDA_SYNC

PCH_RTCX1 — R98 10M_0402_5% — PCH_RTCX2
Y1 32.768KHZ_12.5PF_CM31532768DZFT
C180 18P_0402_50V8J
C181 18P_0402_50V8J

For EMI
SPI_CLK_PCH — R124 33_0402_5% @ — C190 22P_0402_50V8J @

+3V_PCH
R121 200_0402_5% @ — PCH_JTAG_TDO — R125 100_0402_1% @
R122 200_0402_5% @ — PCH_JTAG_TMS — R126 100_0402_1% @
R123 200_0402_5% @ — PCH_JTAG_TDI — R128 100_0402_1% @

4MB P/N : SA00003K800

+3VS
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#

U5 W25Q32BVSSIG_SO8
SPI_SB_CS0#_R — CS#
SPI_SO_L — DO
SPI_WP# — WP#
GND
VCC — +3VS — C191 0.1U_0402_16V4Z
HOLD# — SPI_HOLD#
CLK — SPI_CLK_PCH_0
DI — SPI_SI_R

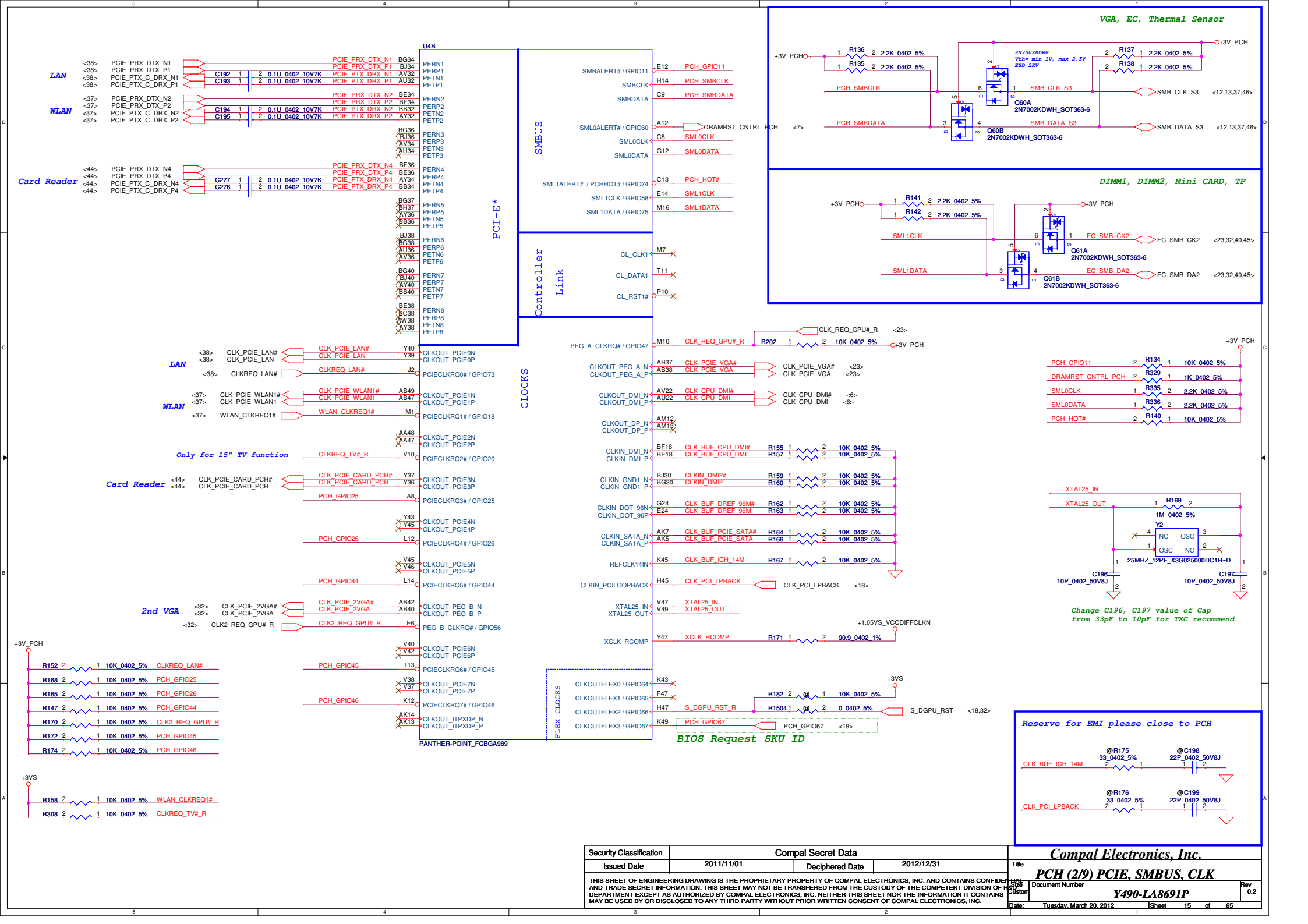
2MB P/N : SA00003FO10

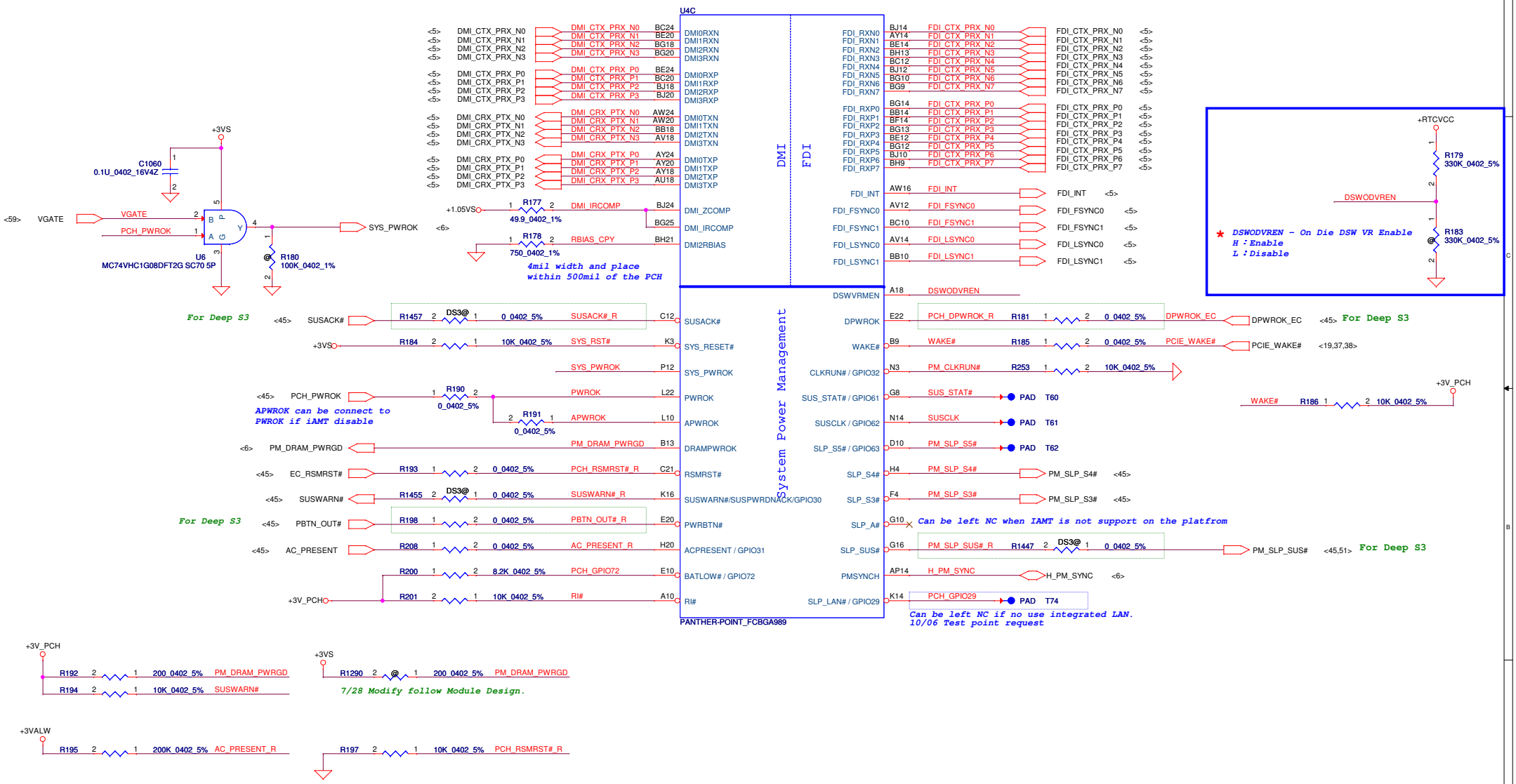
+3VS
R292 3.3K_0402_5% SPI_WP#_1
R246 3.3K_0402_5% SPI_HOLD#_1

U9 W25Q16BVSSIG_SO8
SPI_CS1#_R — CS#
SPI_SO_L1 — DO(IO1)
SPI_WP#_1 — WP#(IO2)
GND
VCC — +3VS — C275 0.1U_0402_16V4Z
HOLD#(IO3) — SPI_HOLD#_1
CLK — SPI_CLK_PCH_1
DI(IO0) — SPI_SI_R1

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2
Date: Tuesday, March 20, 2012 | Sheet 14 of 65


VGA, EC, Thermal Sensor
DIMM1, DIMM2, Mini CARD, TP
U4B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PANTHER-POINT_FCBGA989
LAN
WLAN
Card Reader
2nd VGA
Only for 15" TV function
BIOS Request SKU ID
Reserve for EMI please close to PCH
Change C196, C197 value of Cap from 33pF to 10pF for TXC recommend
Compal Electronics, Inc.
PCH (2/9) PCIE, SMBUS, CLK
Y490-LA8691P
Compal Secret Data
2011/11/01
2012/12/31
Tuesday, March 20, 2012



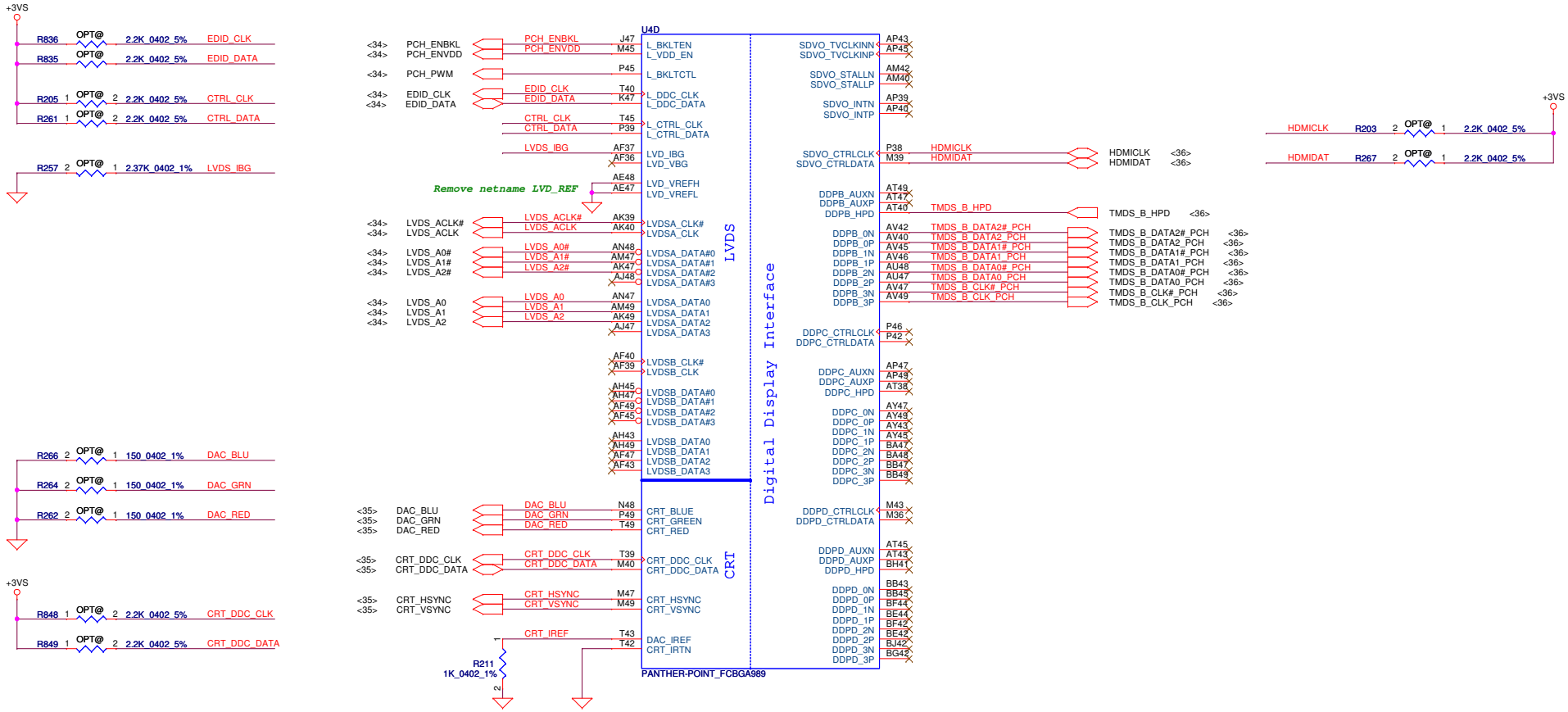
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 16 of 65

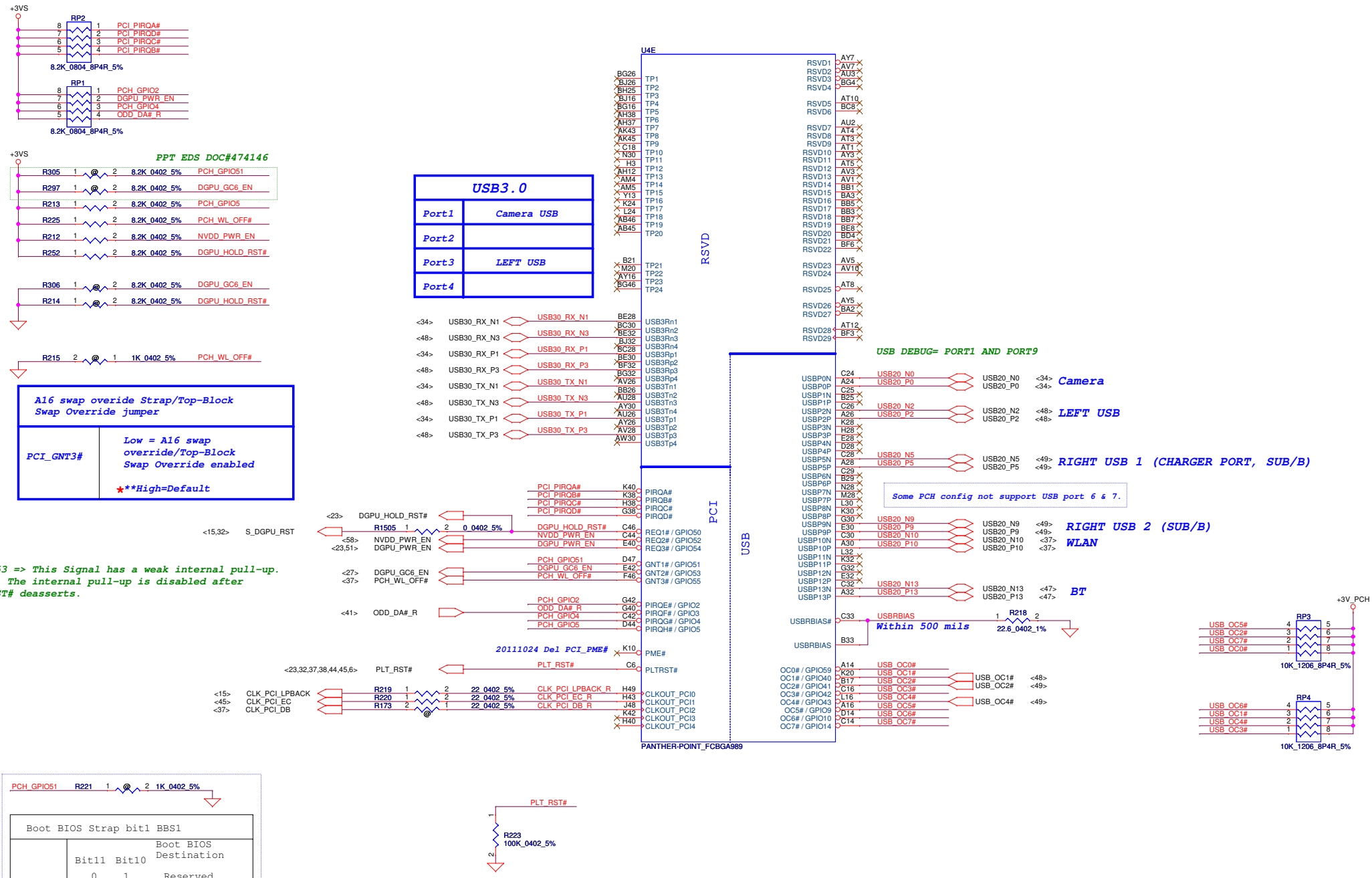


Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 17 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 18 of 65

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

SKU ID

+3VS
R711 10K_0402_5% SLI@
R708 10K_0402_5% @
R704 10K_0402_5% @
PCH_GPIO38
<15> PCH_GPIO67
PCH_GPIO67
PCH_GPIO70
R712 10K_0402_5% OPT@
R709 10K_0402_5%
R706 10K_0402_5%

9/18 Reseve for SKU ID

+3VS
10K_0402_5% R1493 EC_SCI#
+3V_PCH
R235 10K_0402_5% EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 @ 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

+3VALW
DS3@ R207 10K_0402_5%
R245 @ 10K_0402_5% DS3_WAKE#_R

+3VS
200K_0402_5% R250 ODD_DETECT#
+3V_PCH
10K_0402_5% R251 SLAVE_PRESENT#
R259 10K_0402_5% PCH_GPIO37

<23,32> GC6_EVENT# GC6_EVENT#
+3VS R233 10K_0402_5%

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 S_DGPU_PWR_EN → S_DGPU_PWR_EN <32,51>
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 S_NVDD_PWR_EN → S_NVDD_PWR_EN <32>
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15	A20GATE	P4
U2	SATA4GP / GPIO16	PECI	AU16
D40	TACH0 / GPIO17	RCIN#	P5 KBRST# → KBRST# <45>
T5	SCLOCK / GPIO22	PROCPWRGD	AY11 → H_CPUPWRGD <6>
E8	GPIO24	THRMTRIP#	AY10 PCH_THRMTRIP#_R 1 R239 390_0402_5% 2 H_THRMTRIP# → H_THRMTRIP# <6>
E16	GPIO27	INIT3_3V#	T14
P8	GPIO28	DF_TVS	AY1 NV_CLE
K1	STP_PCI# / GPIO34	TS_VSS1	AH8
K4	GPIO35	TS_VSS2	AK11
V8	SATA2GP / GPIO36	TS_VSS3	AH10
M5	SATA3GP / GPIO37	TS_VSS4	AK10
N2	SLOAD / GPIO38	NC_1	P37
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48		
V3	SATA5GP / GPIO49 / TEMP_ALERT#		
D6	GPIO57		

GPIO | CPU/MISC

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

NCTF

PANTHER-POINT_FCBGA989

<27,32,55,58> DGPU_PWROK DGPU_PWROK
+3VS R238 10K_0402_5% PCH_BT_DISABLE#
<37> PCH_BT_DISABLE# ODD_EN <41> ODD_EN
<16,37,38> PCIE_WAKE# 0_0402_5% @ R224 DS3_WAKE#_R
+3V_PCH R241 10K_0402_5% PCH_GPIO28
<37,47> PCH_BT_ON# +3VS R242 10K_0402_5% PCH_BT_ON#
R243 10K_0402_5% PCH_GPIO35
<41> ODD_DETECT# ODD_DETECT#
PCH_GPIO37
PCH_GPIO38
+3VS R247 10K_0402_5% PCH_GPIO39
R248 10K_0402_5% PCH_GPIO48
+3VS R249 10K_0402_5% PCH_GPIO49
<32> SLAVE_PRESENT# SLAVE_PRESENT#

R236 1 2 10K_0402_5% +3VS
GATEA20 <45>

S_DGPU_PWR_EN R268 10K_0402_5% +3VS
S_NVDD_PWR_EN R237 10K_0402_5% +3VS

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

+3VS
PCH_GPIO68 R255 10K_0402_5%
KBRST# R226 10K_0402_5%
PCH_THRMTRIP#_R R244 10K_0402_5%

PROC_SEL	H : Sandy Bridge
	L : IVY Bridge

+1.8VS
R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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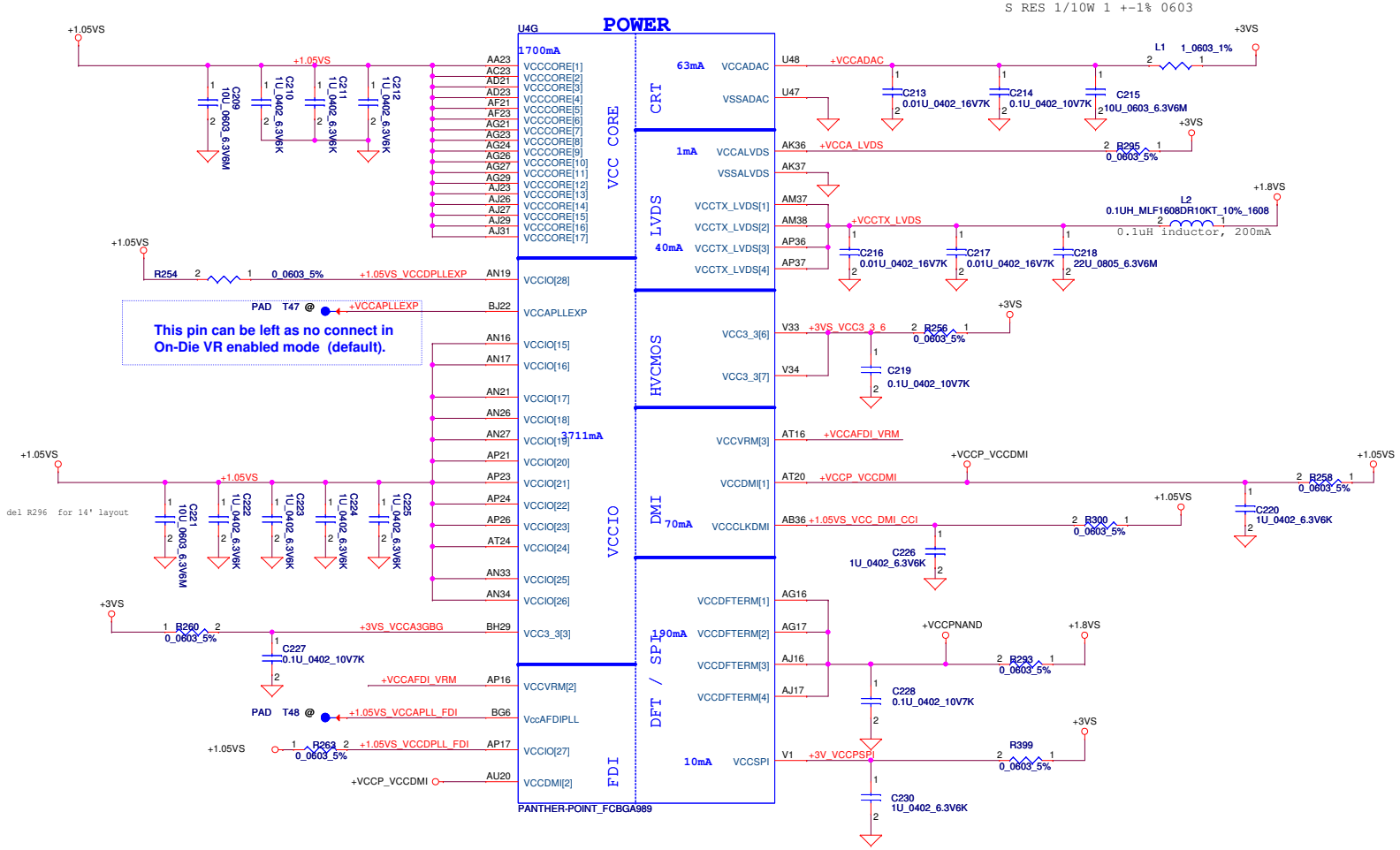

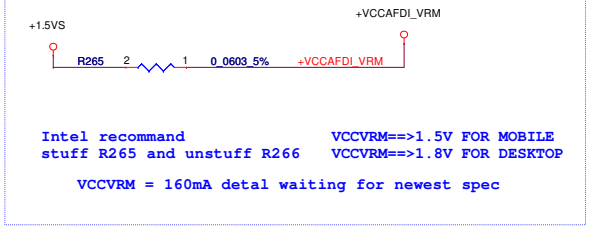

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

+3VS
R280 0_0603_5% +3VS_VCC_CLKF33
C231 10U_0805_10V4Z
C232 1U_0402_6.3V6K

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA

+3VALW R269 0_0603_5% +VCCPDSW
C234 0.1U_0402_10V7K

+1.05VS R271 0_0603_5% +VCCDPLL_CPY

+VCCSUS1
@C239 1U_0402_6.3V6K

+1.05VS R277 0_0805_5% +1.05VM_VCCASW
C241 22U_0805_6.3V6M
C242 22U_0805_6.3V6M
C244 1U_0402_6.3V6K
C245 1U_0402_6.3V6K
C246 1U_0402_6.3V6K

+1.05VS
L5 BLM18PG181SN1D_0603 +1.05VS_VCCA_DPL
L6 BLM18PG181SN1D_0603 +1.05VS_VCCA_DPL
C250 22U_0805_6.3V6M
C251 1U_0402_6.3V6K
C252 22U_0805_6.3V6M
C253 1U_0402_6.3V6K

Before gerber out change to 22u_0805

C258 0.1U_0402_10V7K +VCCRTCEXT
+VCCAFDI_VRM

+1.05VS R274 0_0603_5% C256 1U_0402_6.3V6K +1.05VS_VCCA_DPL
+1.05VS R304 0_0603_5% C259 1U_0402_6.3V6K +1.05VS_VCCDIFFCLKN
+1.05VS_VCCDIFFCLKN
+1.05VS R284 0_0603_5% C262 1U_0402_6.3V6K +1.05VS_VCCDIFFCLK
+1.05VS_SSCVCC

C263 0.1U_0402_10V7K +VCCSST

+1.05VS R286 0_0603_5% +V_CPU_IO
C265 4.7U_0603_6.3V6K
C266 0.1U_0402_10V7K
C267 0.1U_0402_10V7K
+RTCVCC
C268 1U_0402_6.3V6K
C269 0.1U_0402_10V7K
C270 0.1U_0402_10V7K

U4J

AD49	VCCACLK		
T16	VCCDSW3_3	1mA	
V12	DCPSUSBYP		
T38	VCC3_3[5]		
BH23	VCCAPLLDMI2		
AL29	VCCIO[14]		
AL24	DCPSUS[3]		
AA19	VCCASW[1]		
AA21	VCCASW[2]	903mA	
AA24	VCCASW[3]		
AA26	VCCASW[4]		
AA27	VCCASW[5]		
AA29	VCCASW[6]		
AA31	VCCASW[7]		
AC26	VCCASW[8]		
AC27	VCCASW[9]		
AC29	VCCASW[10]		
AC31	VCCASW[11]		
AD29	VCCASW[12]		
AD31	VCCASW[13]		
W21	VCCASW[14]		
W23	VCCASW[15]		
W24	VCCASW[16]		
W26	VCCASW[17]		
W29	VCCASW[18]		
W31	VCCASW[19]		
W33	VCCASW[20]		
N16	DCPRTC		
Y49	VCCVRM[4]		
BD47	VCCADPLLA	80mA	
BF47	VCCADPLLB	80mA	
AF17	VCCIO[7]		
AF33	VCCDIFFCLKN[1]	52mA	
AF34	VCCDIFFCLKN[2]		
AG34	VCCDIFFCLKN[3]		
AG33	VCCSSC	95mA	
V16	DCPSST		
T17	DCPSUS[1]		
V19	DCPSUS[2]		
BJ8	V_PROC_IO	1mA	
A22	VCCRTC		

PANTHER-POINT_FCBGA989

Clock and Miscellaneous

USB

N26	VCCIO[29]		
P26	VCCIO[30]		
P28	VCCIO[31]		
T27	VCCIO[32]		
T29	VCCIO[33]		
T23	VCCSUS3_3[7]	228mA	
T24	VCCSUS3_3[8]		
V23	VCCSUS3_3[9]		
V24	VCCSUS3_3[10]		
P24	VCCSUS3_3[6]		
T26	VCCIO[34]		
M26	V5REF_SUS	1mA	
AN23	DCPSUS[4]		
AN24	VCCSUS3_3[1]		

+1.05VS_VCCUSBCORE R270 0_0603_5% C233 1U_0402_6.3V6K
+3V_PCH +3V_VCCPUSB R272 0_0603_5% C236 0.1U_0402_10V7K
+3V_VCCAUBG R273 0_0603_5% C238 0.1U_0402_10V7K
+1.05VS_VCCAUPLL R276 0_0603_5%
+PCH_V5REF_SUS
+VCCA_USBSUS C243 @ 1U_0402_6.3V6K
+3V_VCCPSUS

PCI/GPIO/LPC

P34	V5REF	1mA	
N20	VCCSUS3_3[2]		
N22	VCCSUS3_3[3]		
P20	VCCSUS3_3[4]		
P22	VCCSUS3_3[5]		
AA16	VCC3_3[1]		
W16	VCC3_3[8]		
T34	VCC3_3[4]		

+PCH_V5REF_RUN
+3V_VCCPSUS R278 0_0603_5% C247 1U_0402_6.3V
+3VS_VCCPCORE R281 0_0603_5% C249 0.1U_0402_10V7K
+3VS_VCCPPCI R282 0_0603_5% C254 0.1U_0402_10V7K

SATA

AJ2	VCC3_3[2]		
AF13	VCCIO[5]		
AH13	VCCIO[12]		
AH14	VCCIO[13]		
AF14	VCCIO[6]		
AK1	VCCAPLLSATA		
AF11	VCCVRM[1]		
AC16	VCCIO[2]		
AC17	VCCIO[3]		
AD17	VCCIO[4]		

+VCC3_3_2 R283 0_0603_5% C255 0.1U_0402_10V7K
+1.05VS_SATA3 R285 0_0603_5% C257 1U_0402_6.3V6K
+VCCAFDI_VRM
+1.05VS_VCC_SATA R288 0_0603_5% C261 1U_0402_6.3V6K

On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2 , VCCAPLLSATA

MISC

T21	VCCASW[22]		
V21	VCCASW[23]		
T19	VCCASW[21]		

CPU

RTC

HDA

P32	VCCSUSHDA	10mA	

+VCCSUSHDA R287 0_0603_5% C271 0.1U_0402_16V4Z

+5V_PCH +3V_PCH R275 10_0402_5% D1 CH751H-40PT_SOD323-2 +PCH_V5REF_SUS C240 0.1U_0603_25V7K

+5VS +3VS R279 10_0402_5% D2 CH751H-40PT_SOD323-2 +PCH_V5REF_RUN C248 1U_0603_10V6K

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (8/9) PWR

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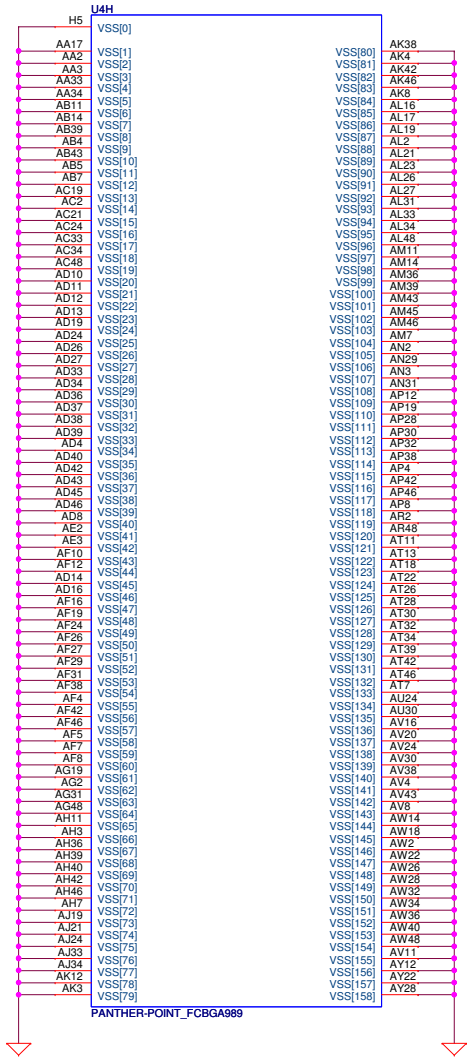
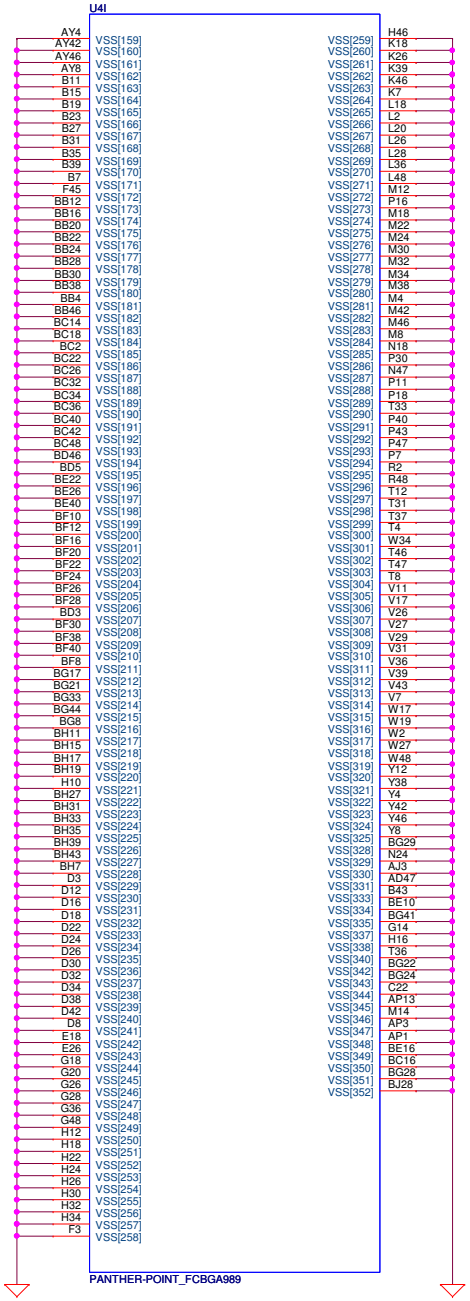




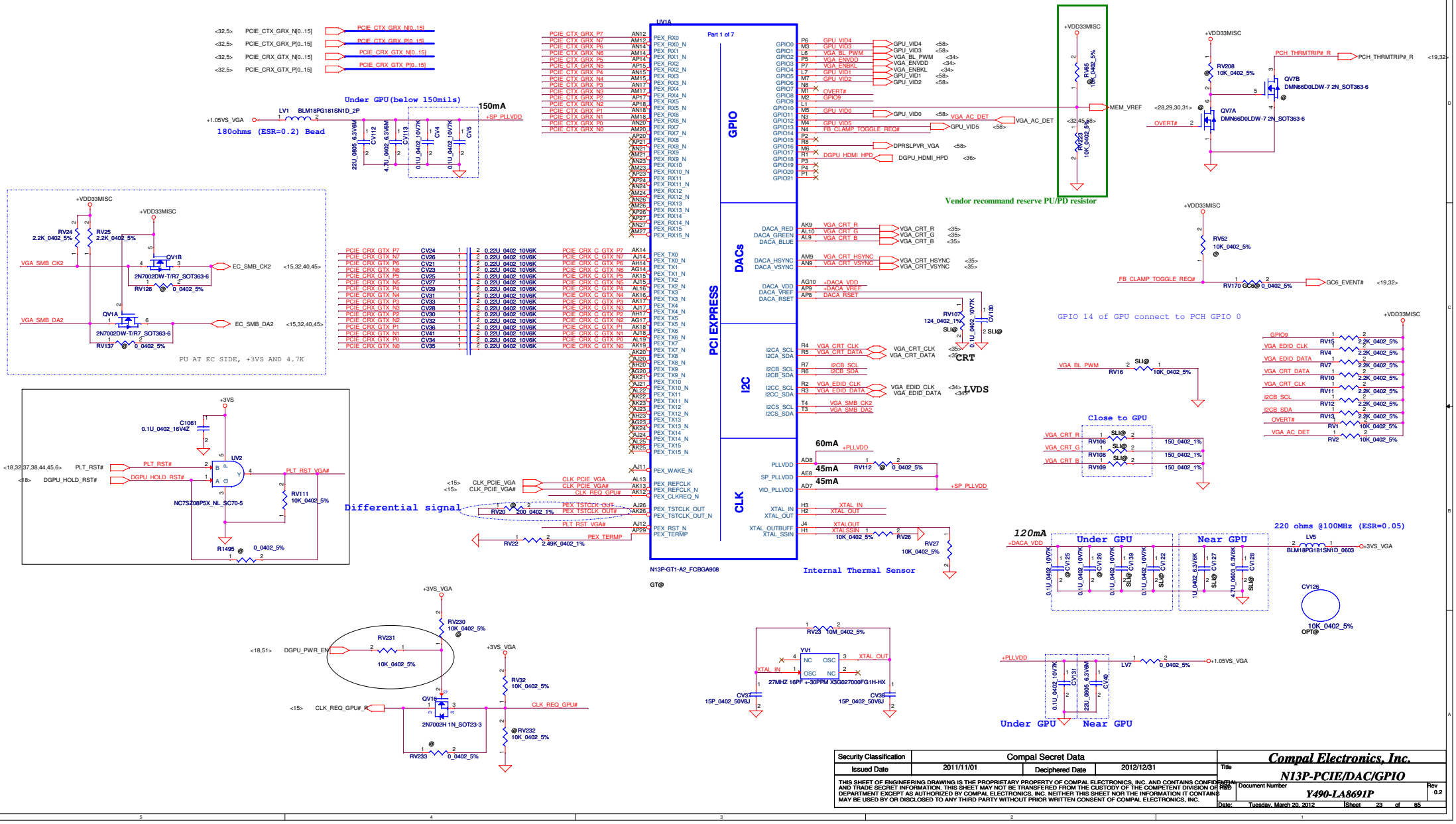
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 22 of 65



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/01	Deciphered Date	2012/12/31
Title	N13P-PCIE/DAC/GPIO		
Size	Document Number		Rev
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UV1D

Part 4 of 7

N13P-GT1-A2_FCBGA908

for 15" dual channel

LVDS/TMDS

NC

TEST

SERIAL

GENERAL

trace width: 16mils
differential voltage sensing.
differential signal routing.

1MB SPI ROM FOR VBIOS ROM (SLI)

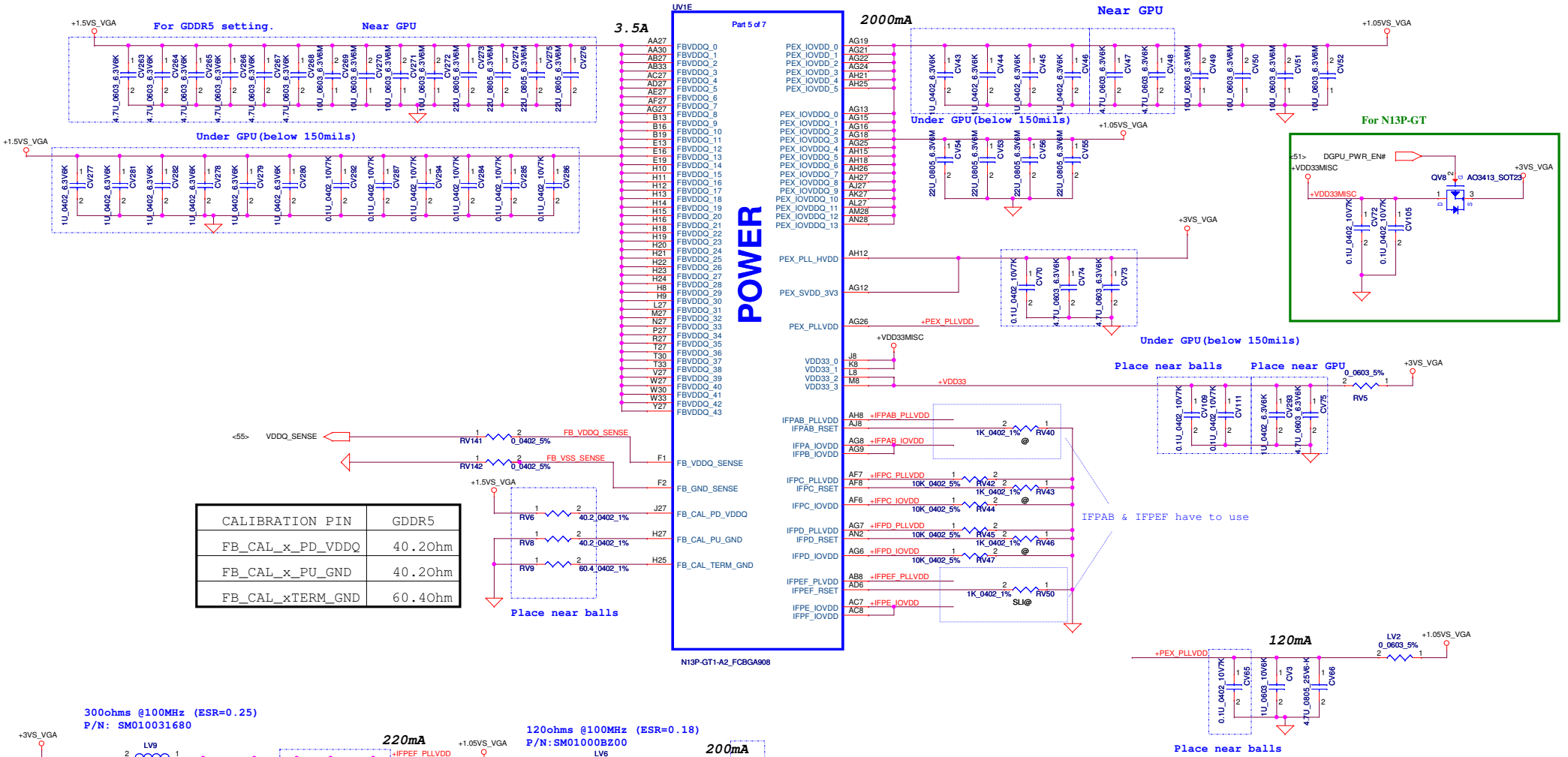
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-LVDS/HDMI/DP/THM

Size | Document Number: Y490-LA8691P | Rev: 0.2

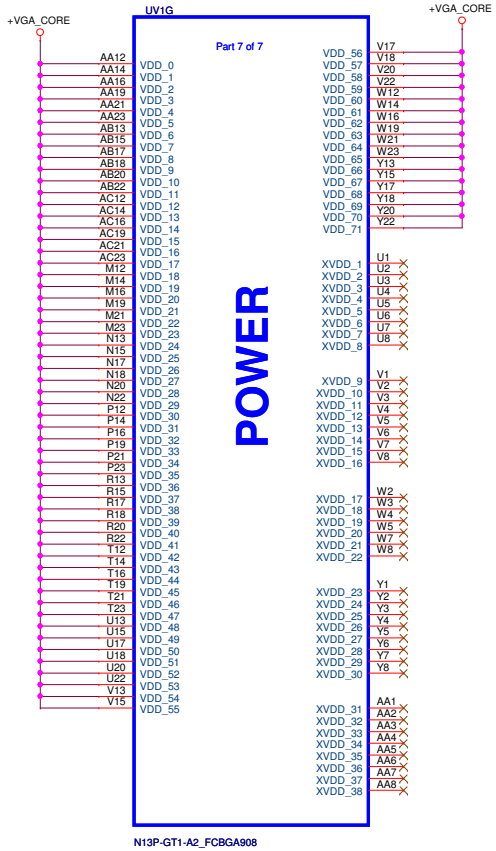
Date: Tuesday, March 20, 2012 | Sheet 24 of 65

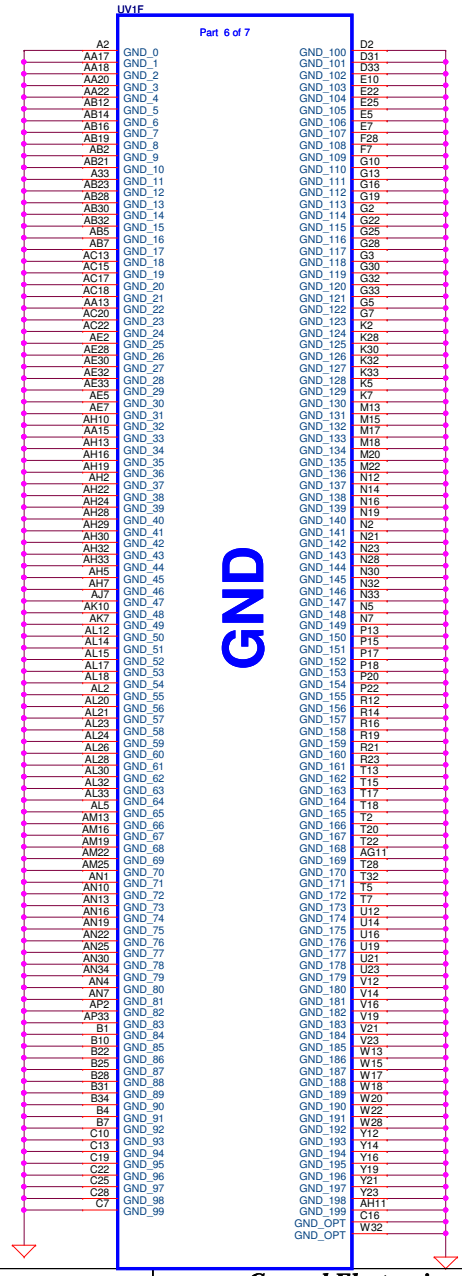


CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: N13P-POWER			
Size	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 25 of 65		





Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VGA CORE, GND

Size	Document Number	Rev
	Y490-LA8691P	0.2

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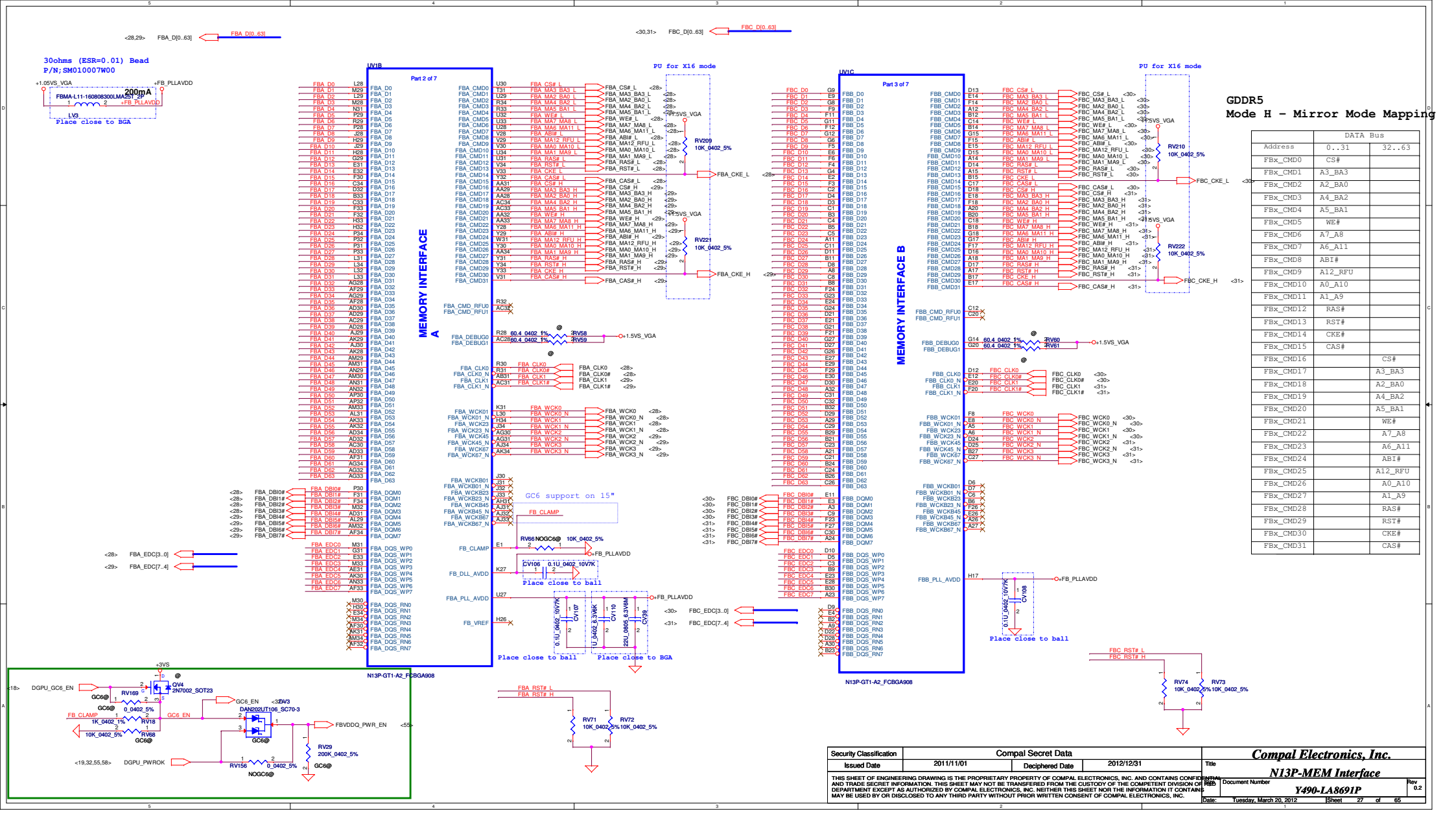

GDDR5
Mode H - Mirror Mode Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **N13P-MEM Interface**

Size: D | Document Number: **Y490-LA8691P** | Rev: 0.2

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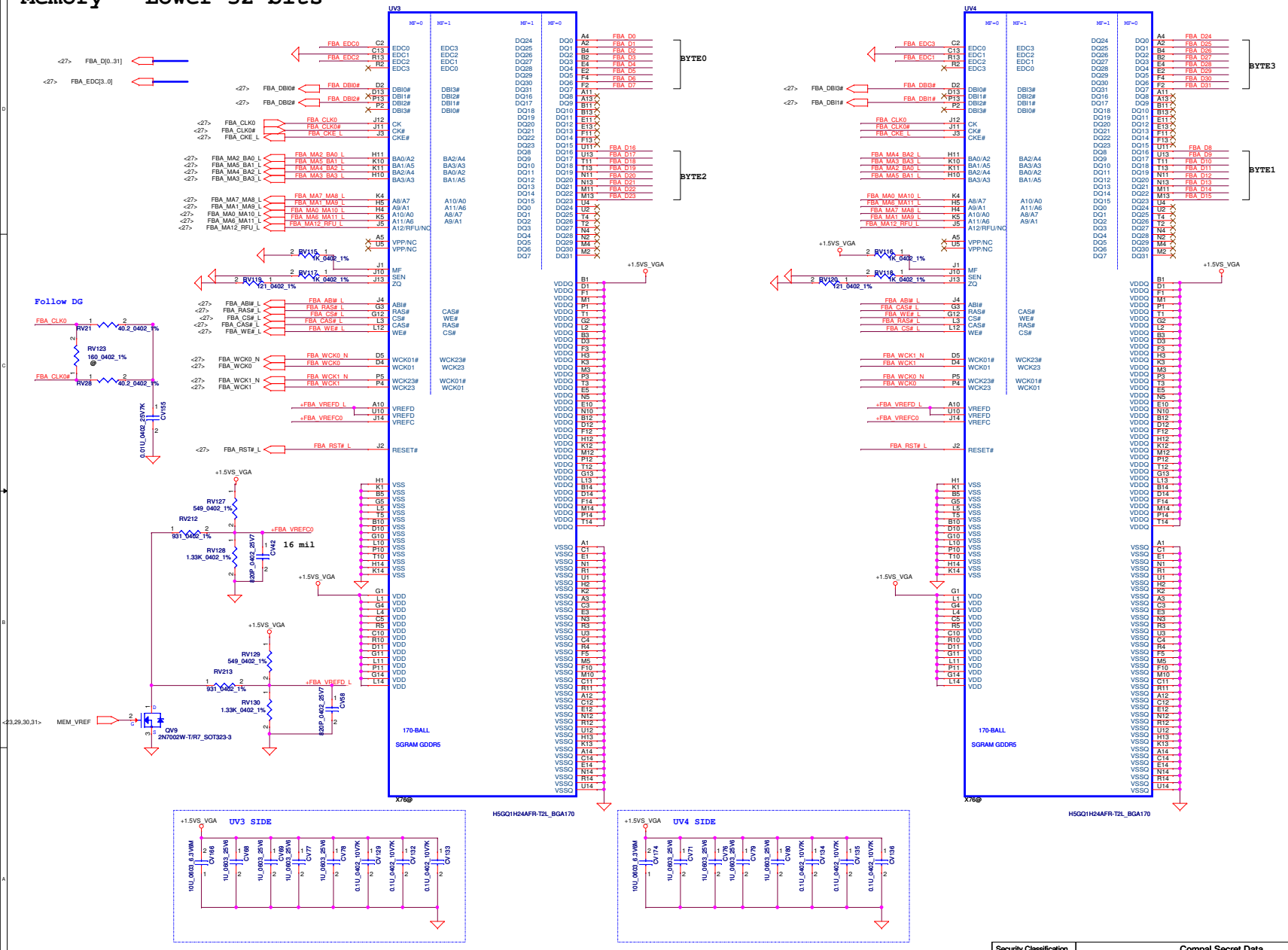
Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VRAM A Lower

Size | Document Number: Y490-LA8691P | Rev: 0.2

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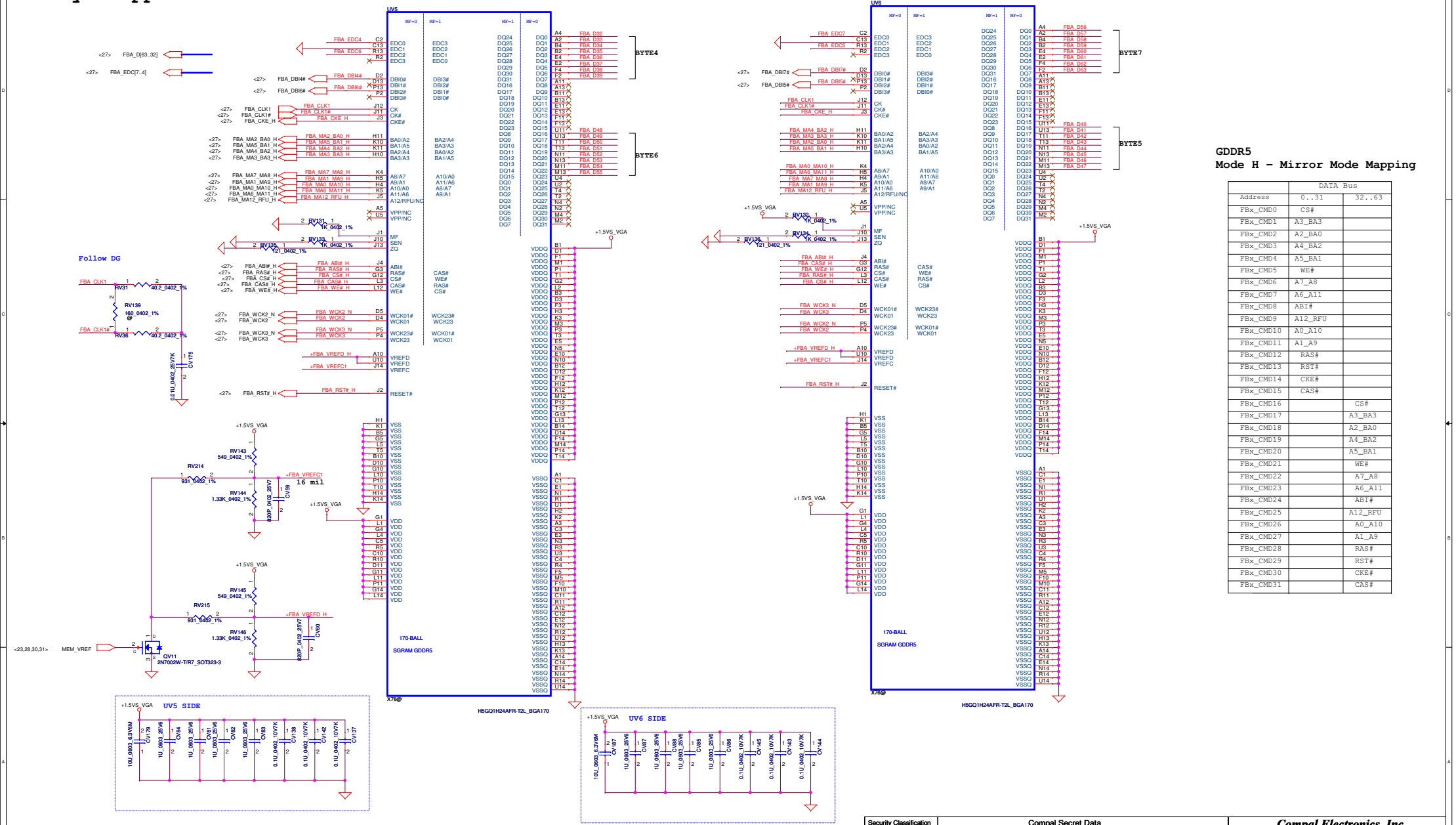
Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

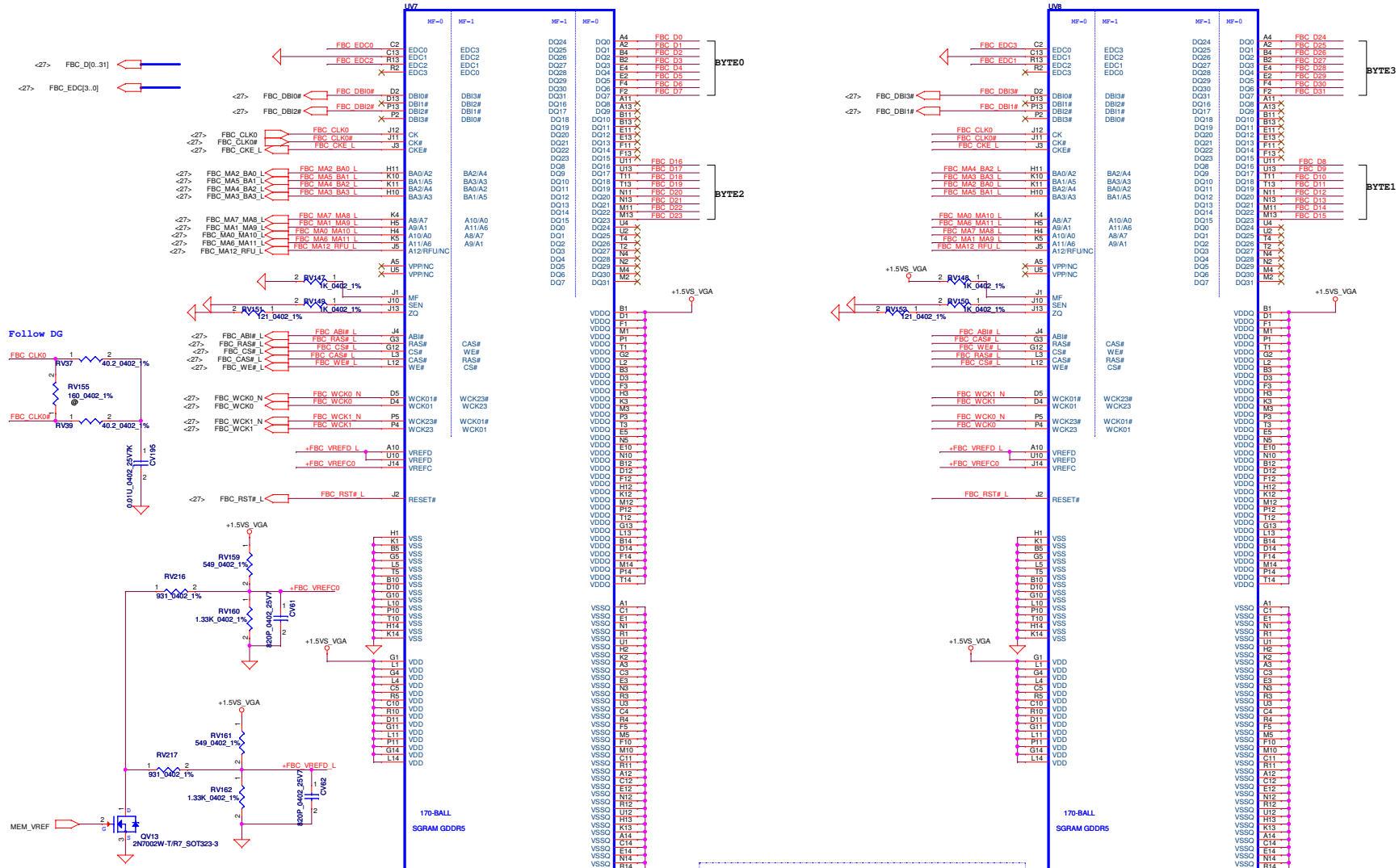
Compal Electronics, Inc.

Title: **N13P-VRAM A Upper**

Size: | Document Number: **Y490-LA8691P** | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 29 of 65

Memory Partition C – Lower 32 bits

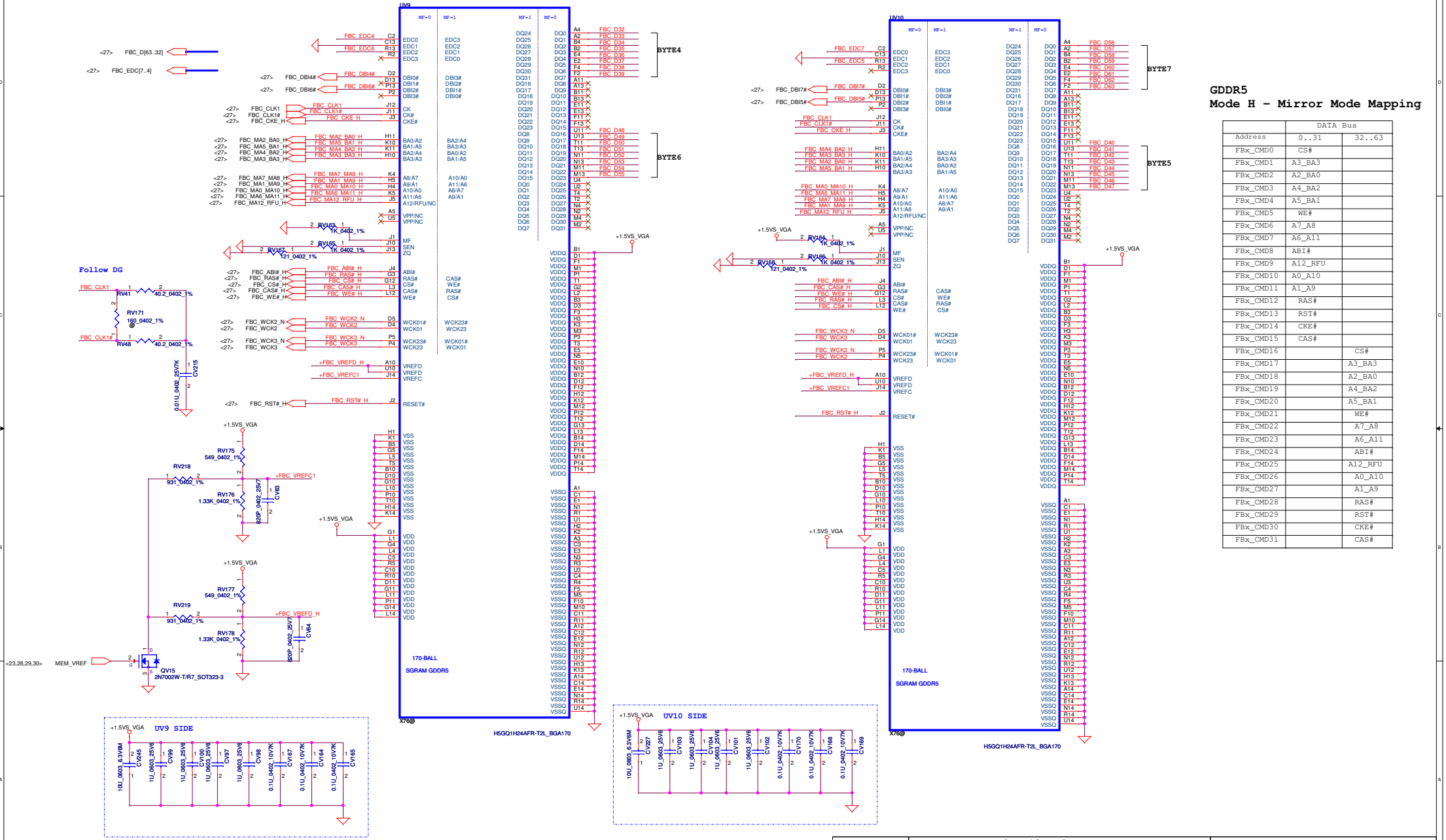


GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Compal Electronics, Inc.		
Title: N12P-VRAM C Lower		
Size: C	Document Number: Y490-LA8691P	Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 30 of 65	

Memory Partition C – Upper 32 bits

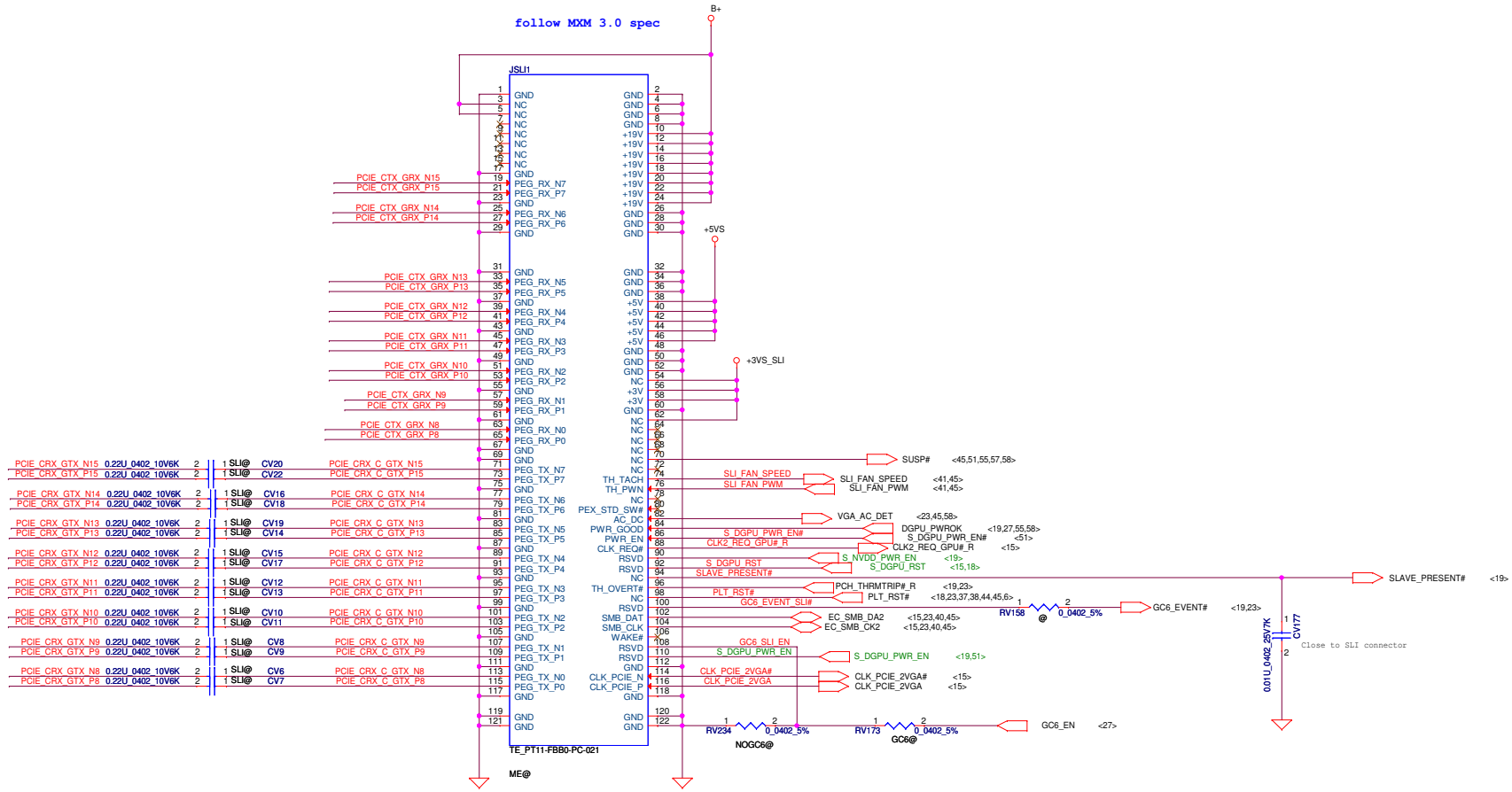


GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2011/12

Compal Electronics, Inc.			
Title: N12P-VRAM C Upper			
Size: C	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 31 of 65		



11/11 for 2nd VGA fan need to notic EC

<23,5> PCIE_CTX_GRX_N[0..15] PCIE_CTX_GRX_N[0..15]
<23,5> PCIE_CTX_GRX_P[0..15] PCIE_CTX_GRX_P[0..15]
<23,5> PCIE_CRX_GTX_N[0..15] PCIE_CRX_GTX_N[0..15]
<23,5> PCIE_CRX_GTX_P[0..15] PCIE_CRX_GTX_P[0..15]

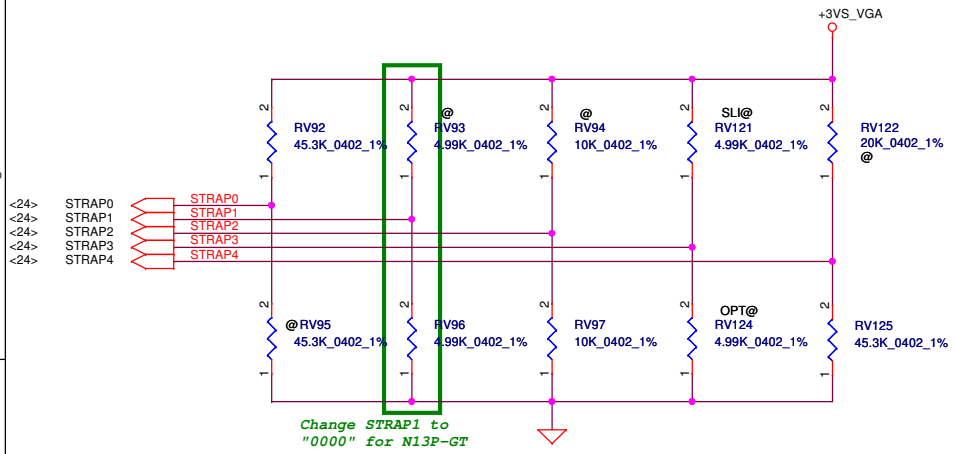
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

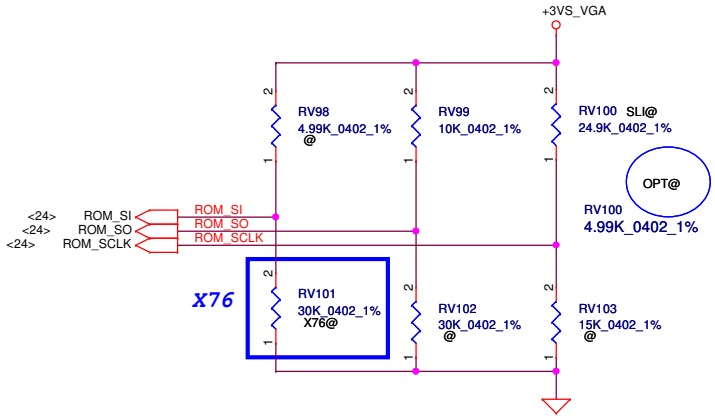
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 32 of 65





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PU 25K (SLI) PU 5K (OPT)	PU 45K	PD 5K	PD 10K	PU 5K	PD 10K
		K4G10325FG-HC04 1G 32Mx32	PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32	PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32	PD 35K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J

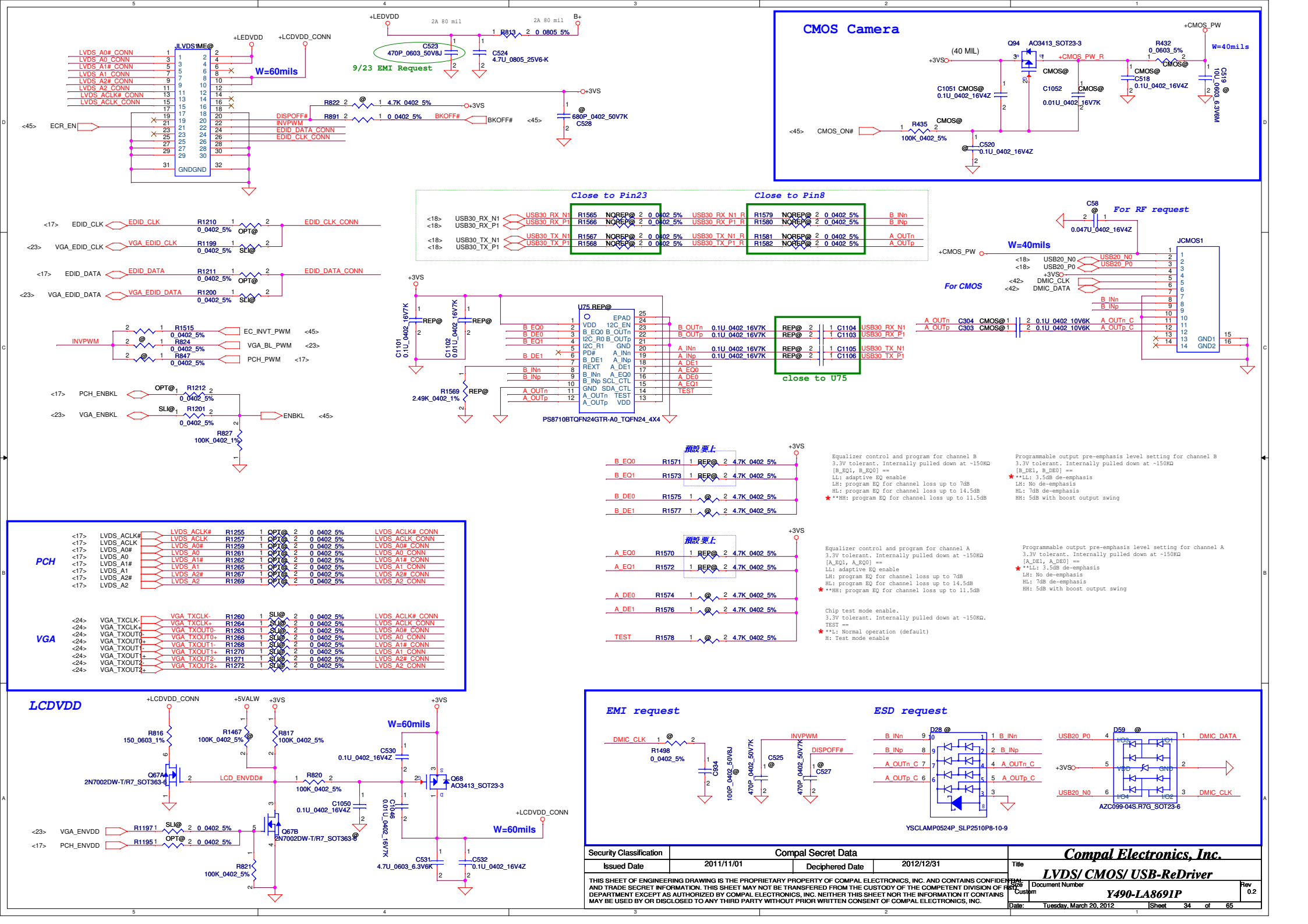
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

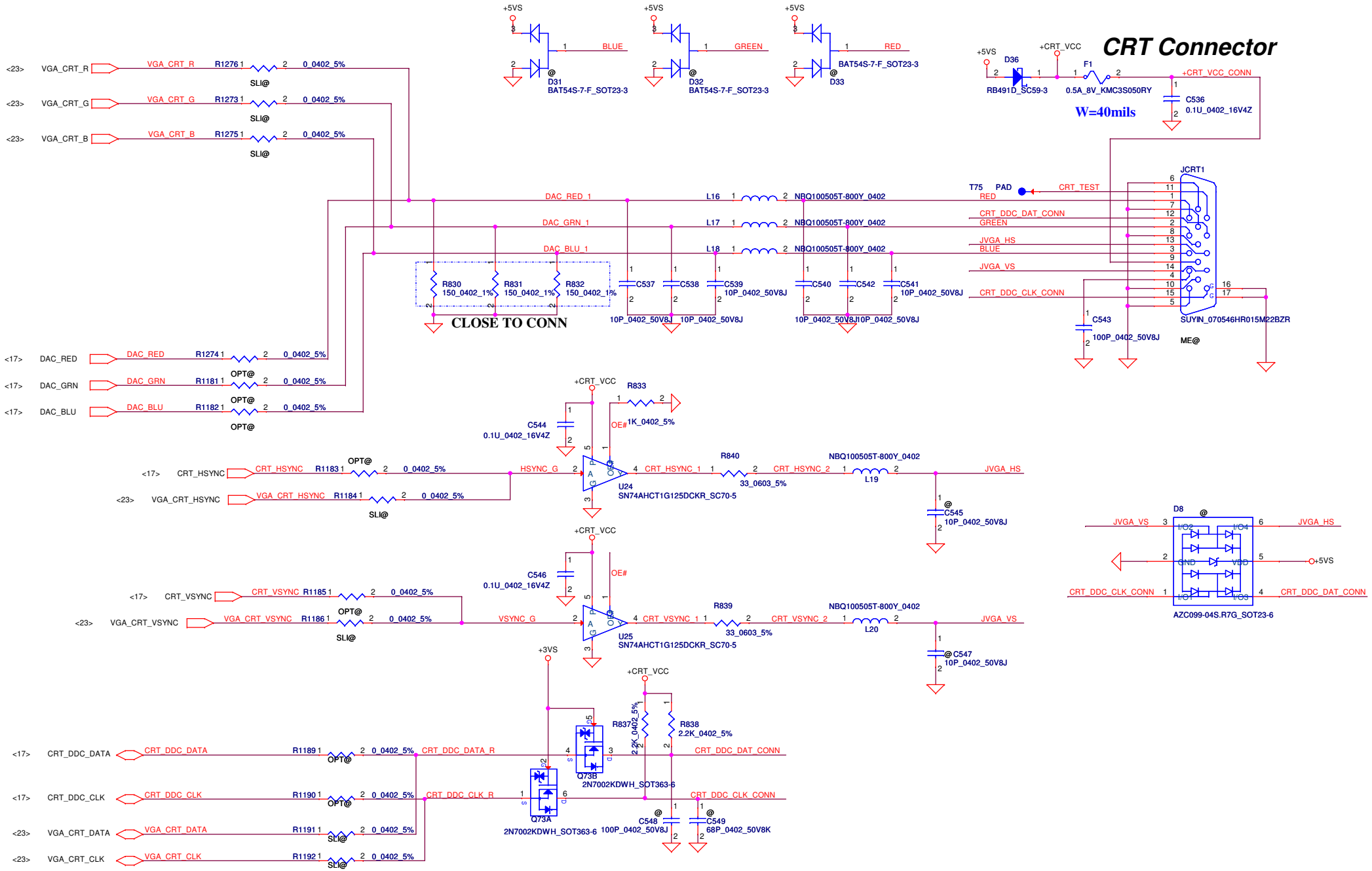
Title: N13P_MISC

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 33 of 65


CMOS Camera
Close to Pin23
Close to Pin8
For RF request
For CMOS
close to U75
PCH
VGA
LCDVDD
EMI request
ESD request
9/23 EMI Request
W=60mils
W=40mils
JLVDS1
JCMOS1
U75 REP@
PS8710BTQFN24GTR-A0_TQFN24_4X4
YSCLAMP0524P_SLP2510P8-10-9
AZC099-04S.R7G_SOT23-6
Compal Secret Data
Issued Date 2011/11/01
Deciphered Date 2012/12/31
Compal Electronics, Inc.
LVDS/ CMOS/ USB-ReDriver
Y490-LA8691P
Rev 0.2
Tuesday, March 20, 2012
Sheet 34 of 65

CRT Connector



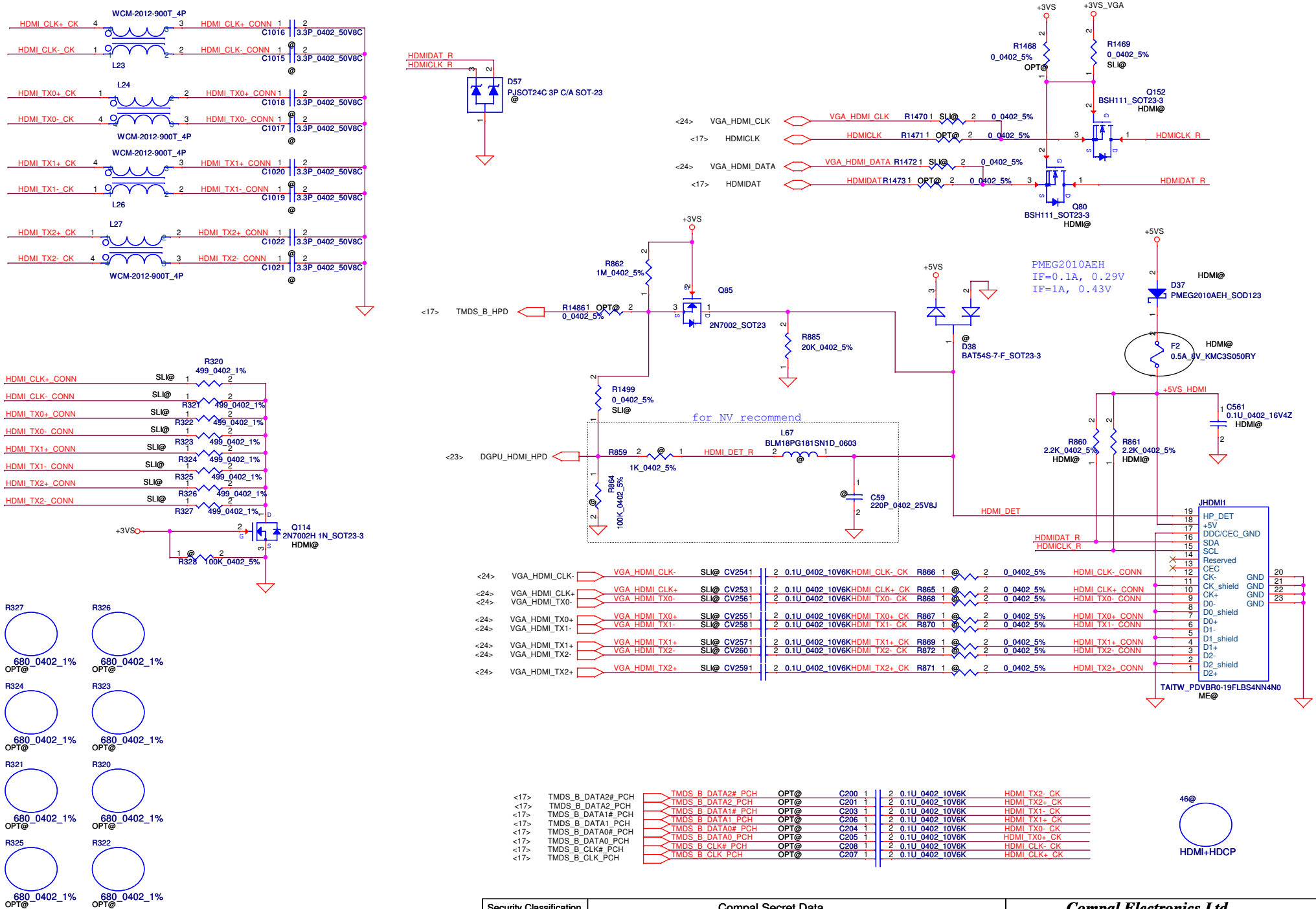
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 35 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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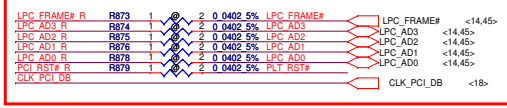
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

Mini-Express Card(WLAN/WiMAX)

For isolate Intel Rainbow Peak and Compal debug card.

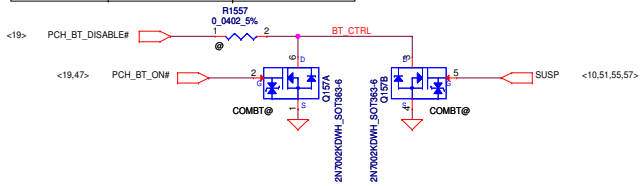
For EC to detect debug card insert.

softstart (RC) will check on EVT PCB

9/18 Increase for Intel AOAC function

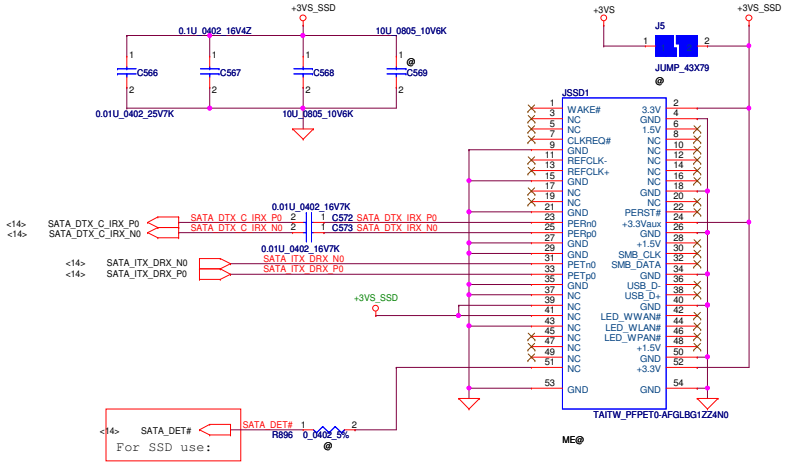
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
PCH_BT_ON#	L	H



Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)

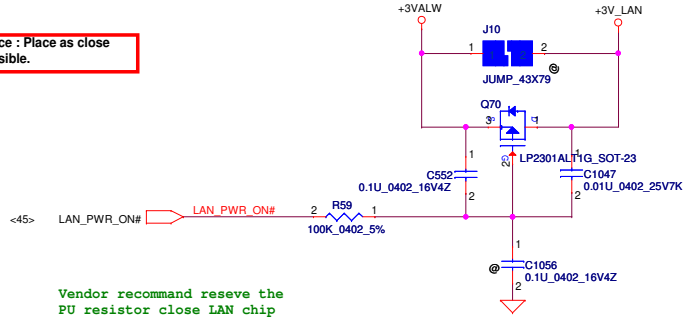


Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

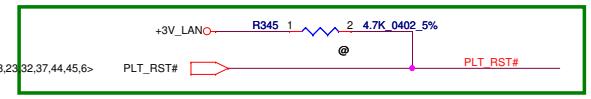
Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012		Sheet 37 of 65	

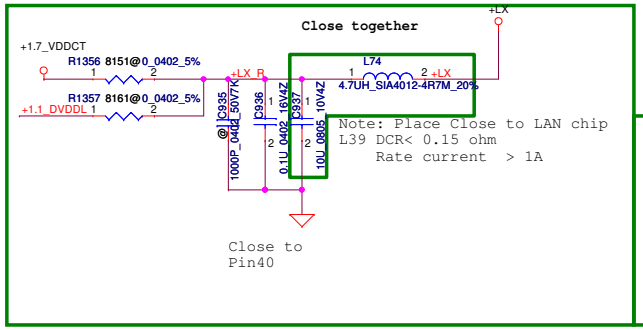
Atheros request can't disable LAN power

Layout Notice : Place as close chip as possible.

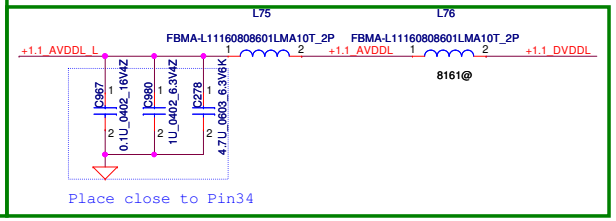


Vendor recommand reseve the PU resistor close LAN chip

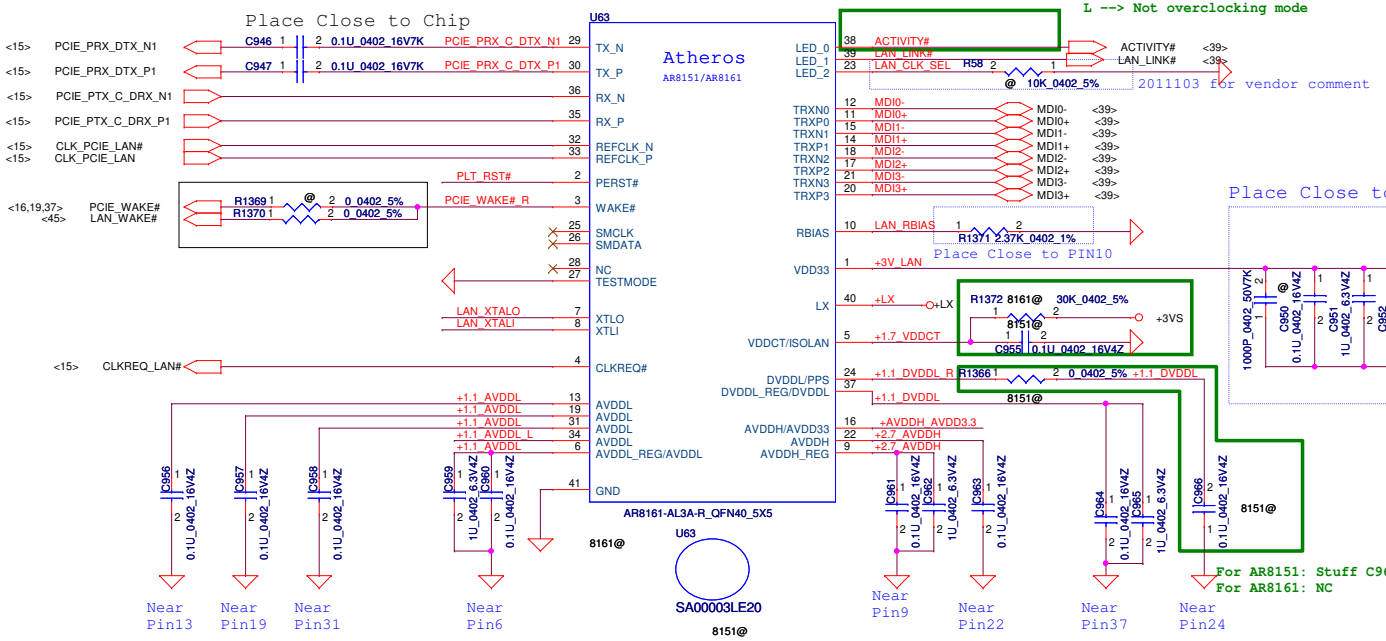


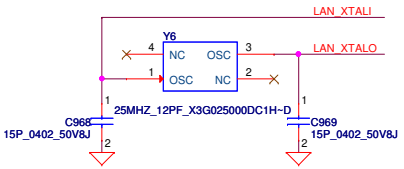


	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356,C955
AR8161	+1.1V <DVDDL,AVDDL>	R1357,R1372,L76

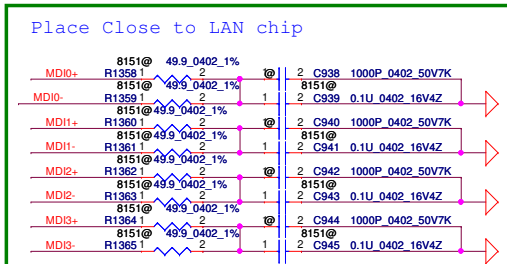


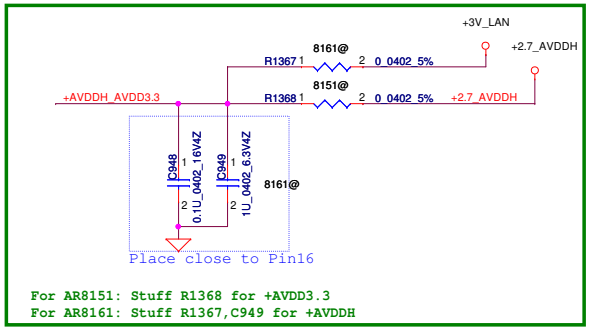
H --> Overclocking mode
L --> Not overclocking mode





Change C968, C969 value of Cap from 33pF to 15pF for TXC recommend





Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LAN-AR8151/8161

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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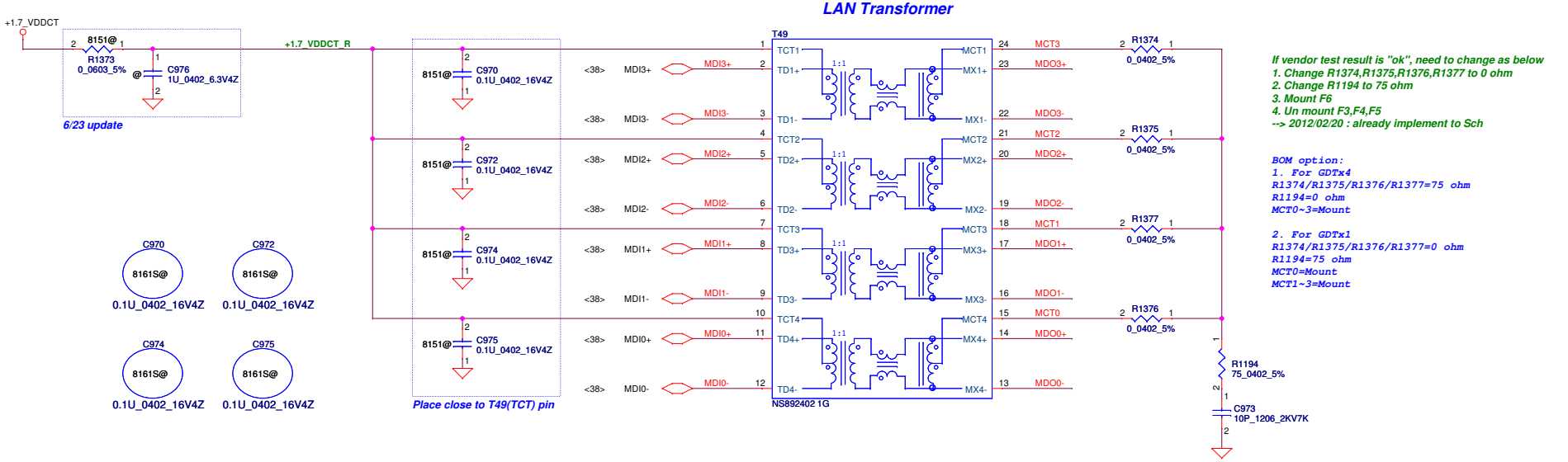
LAN Transformer

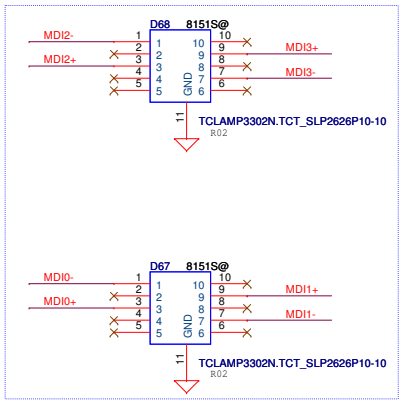


If vendor test result is "ok", need to change as below
1. Change R1374,R1375,R1376,R1377 to 0 ohm
2. Change R1194 to 75 ohm
3. Mount F6
4. Un mount F3,F4,F5
--> 2012/02/20 : already implement to Sch

BOM option:
1. For GDTx4
R1374/R1375/R1376/R1377=75 ohm
R1194=0 ohm
MCT0~3=Mount

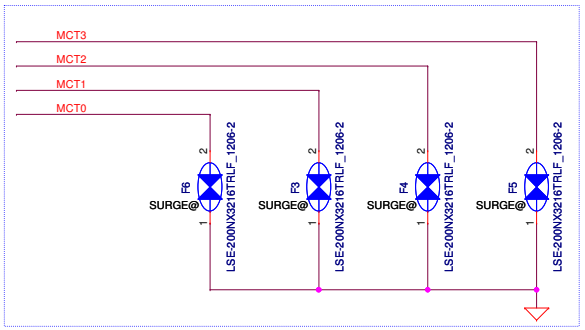
2. For GDTx1
R1374/R1375/R1376/R1377=0 ohm
R1194=75 ohm
MCT0=Mount
MCT1~3=Mount

Place Close to T49



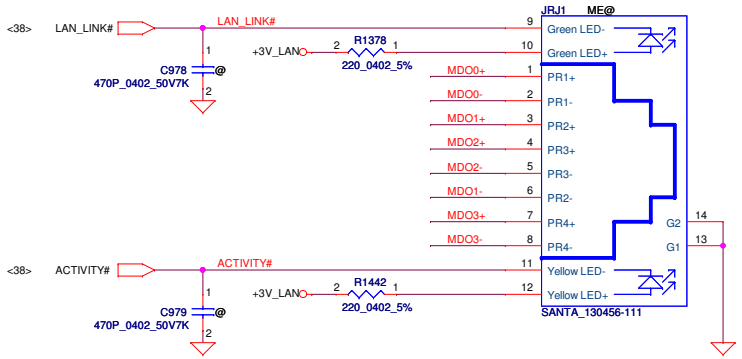
Reserve D67,D68 for EMI go rural solution

Place Close to T49



Reserve for EMI go rural solution

LAN Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

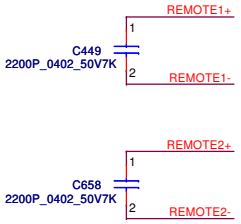
Compal Electronics, Inc.

Title: **LAN Transformer**

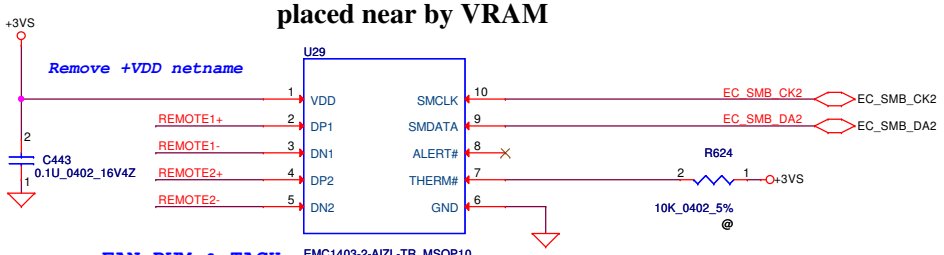
Size: Custom | Document Number: **Y490-LA8691P** | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 39 of 65

Close U29



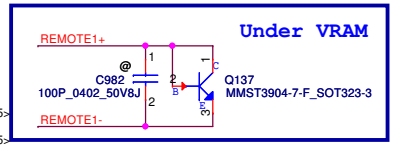
SMSC thermal sensor placed near by VRAM

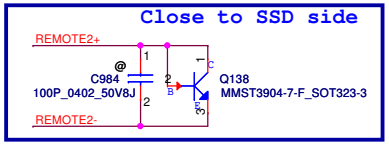


FAN_PWM & TACH for PWM FAN

Address 1001_101xb

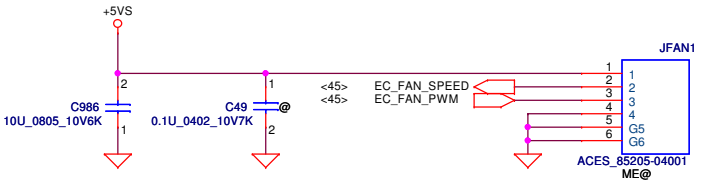
internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp





REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

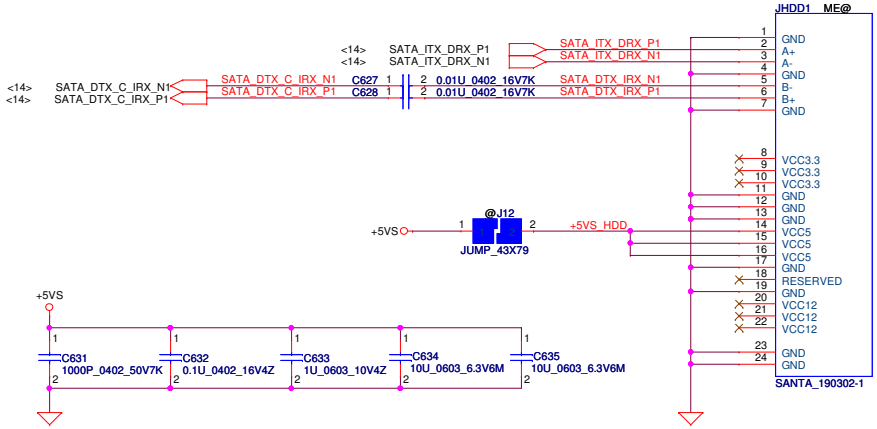
Compal Electronics,Ltd.

Title: EMC1403/2103_Thermal sensor/FAN

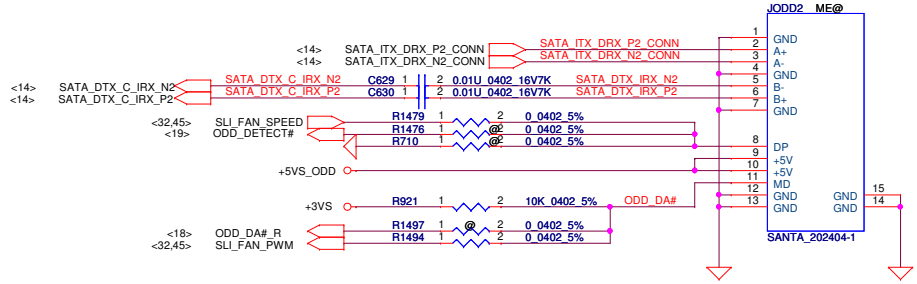
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 40 of 65

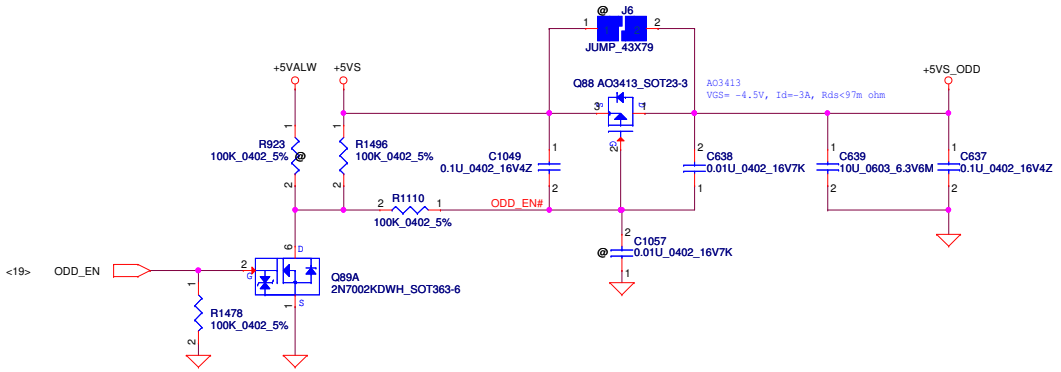
SATA HDD Conn.



SATA ODD Conn.

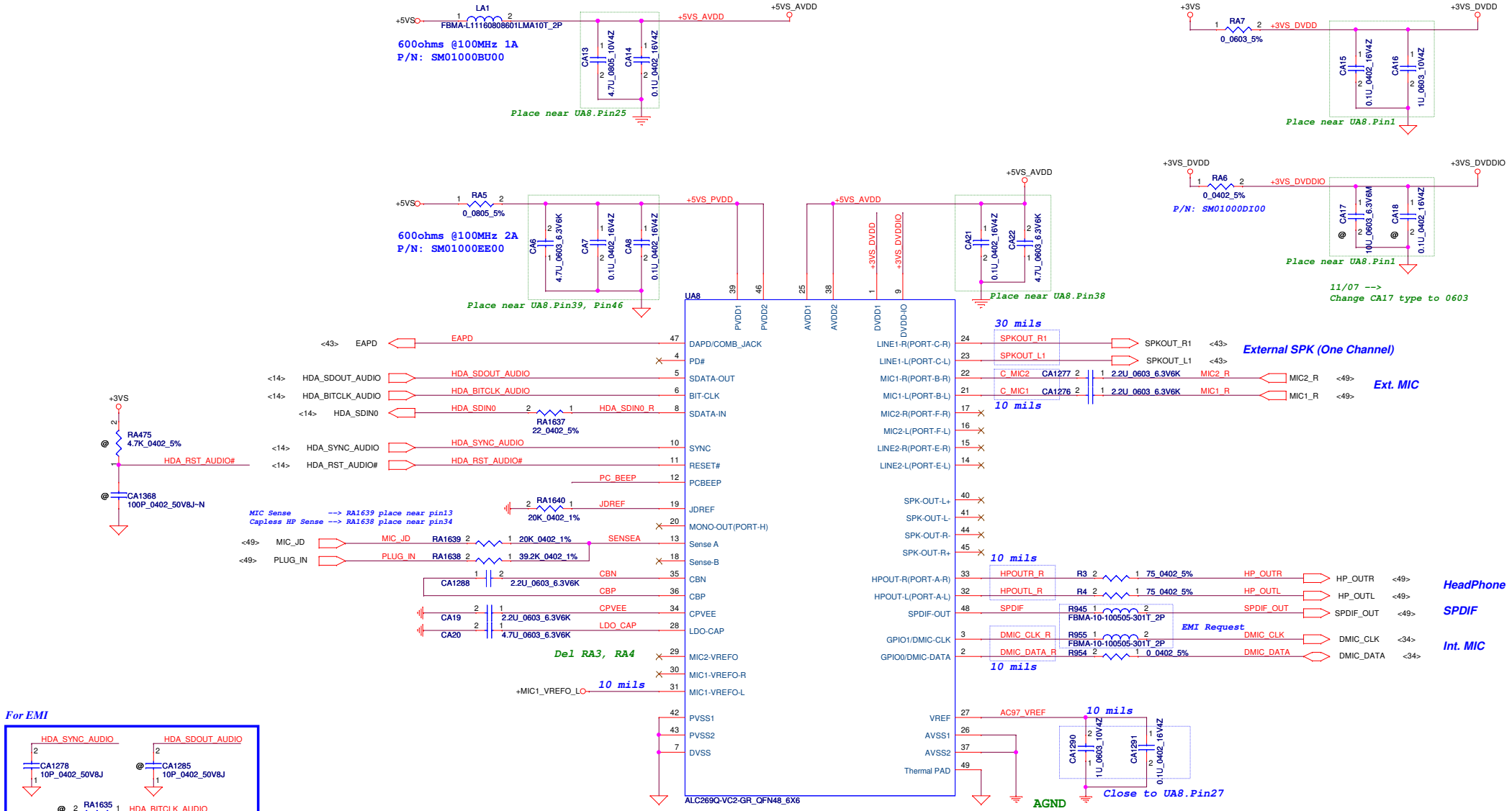


ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 41 of 65		



Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

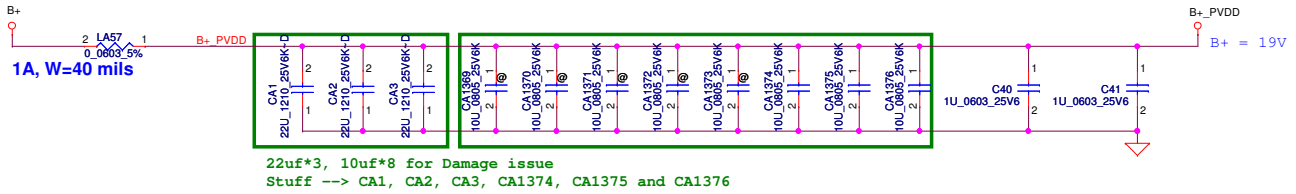
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/03/09

Compal Electronics, Inc.

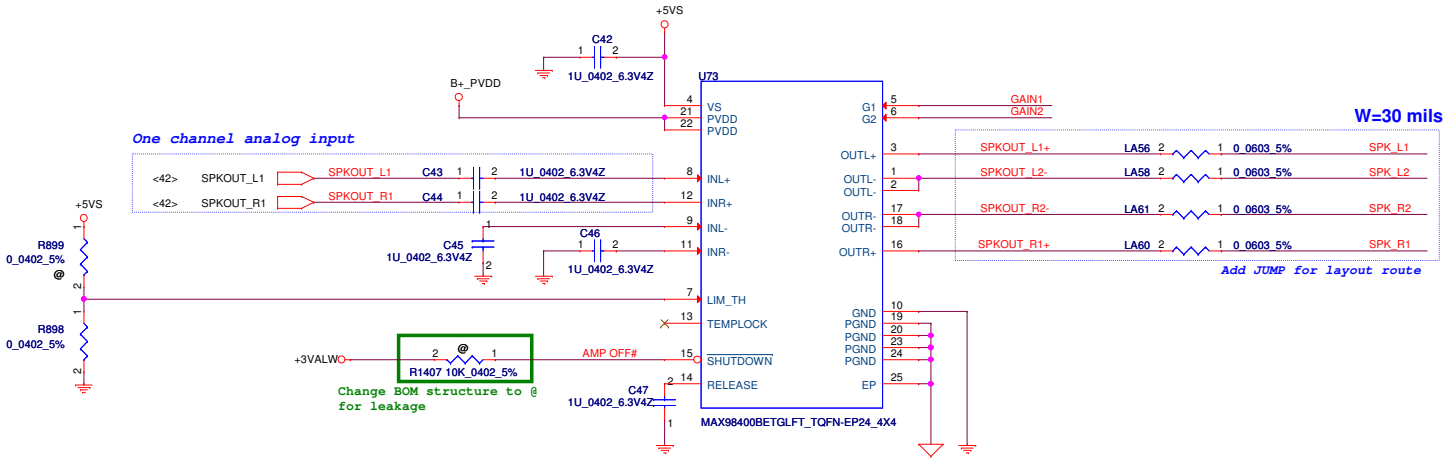
Title: HD Audio ALC269Q-VC3

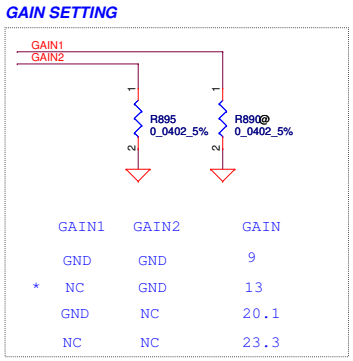
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

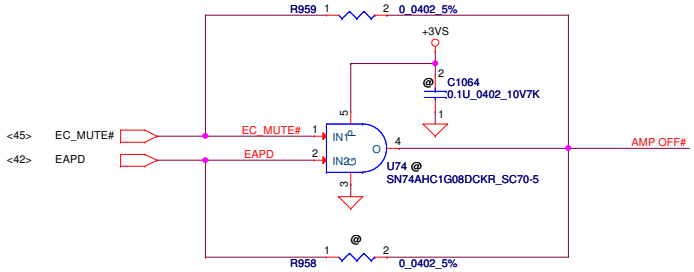
Date: Tuesday, March 20, 2012 | Sheet 42 of 65

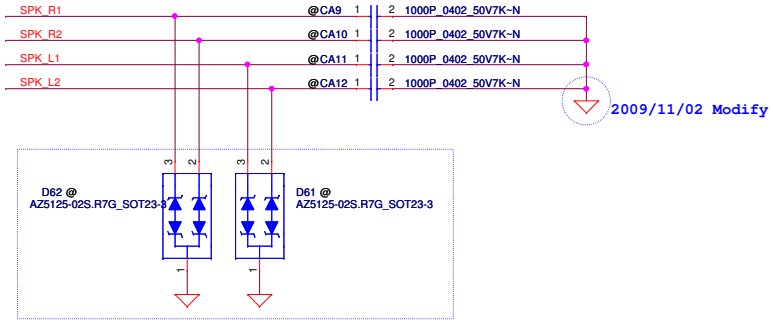


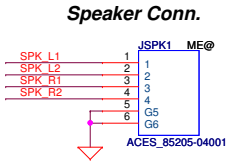
22uf*3, 10uf*8 for Damage issue
Stuff --> CA1, CA2, CA3, CA1374, CA1375 and CA1376











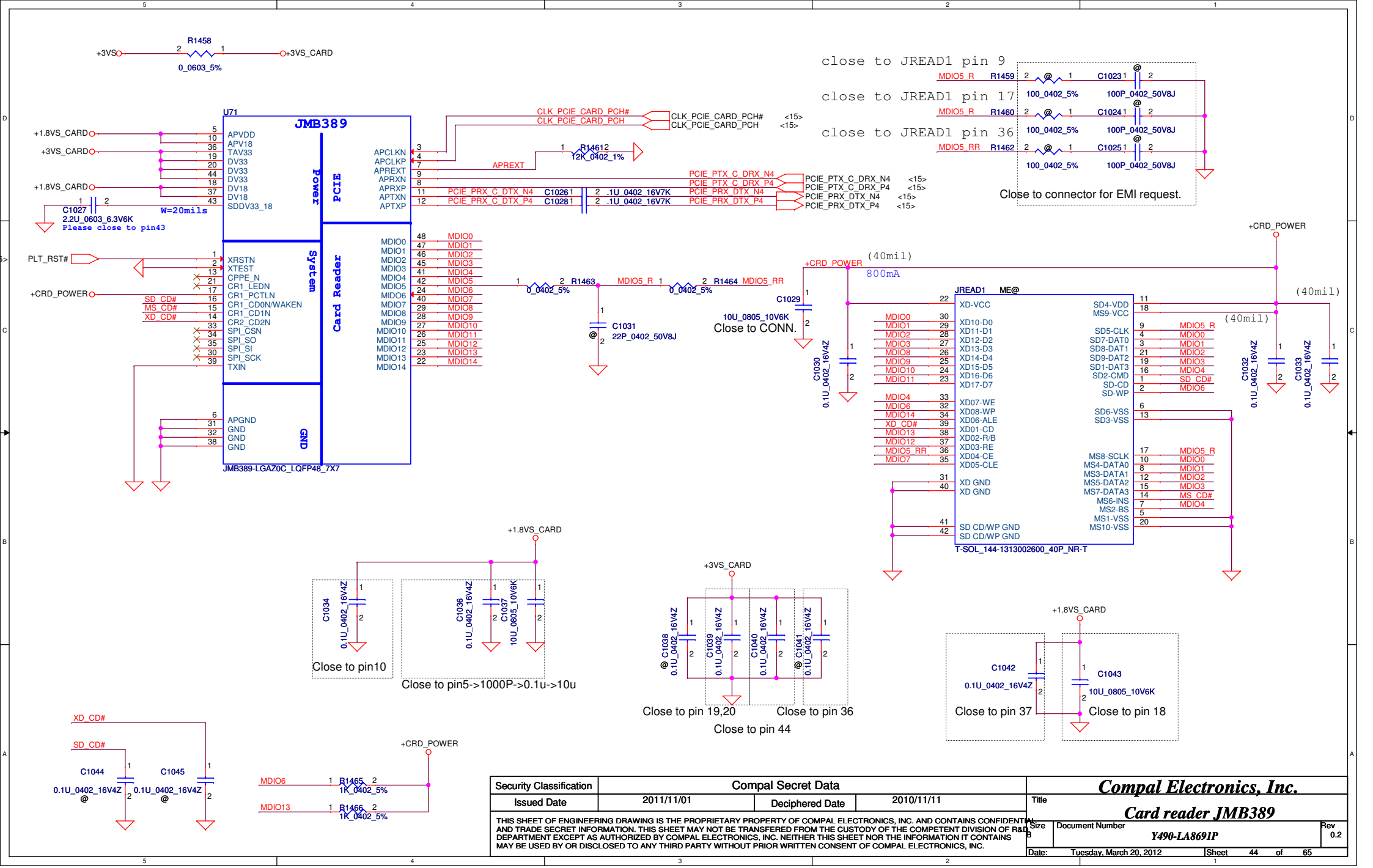
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/03/09

Compal Electronics, Inc.

Title: AMP-MAX98400BETG+T

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 43 of 65



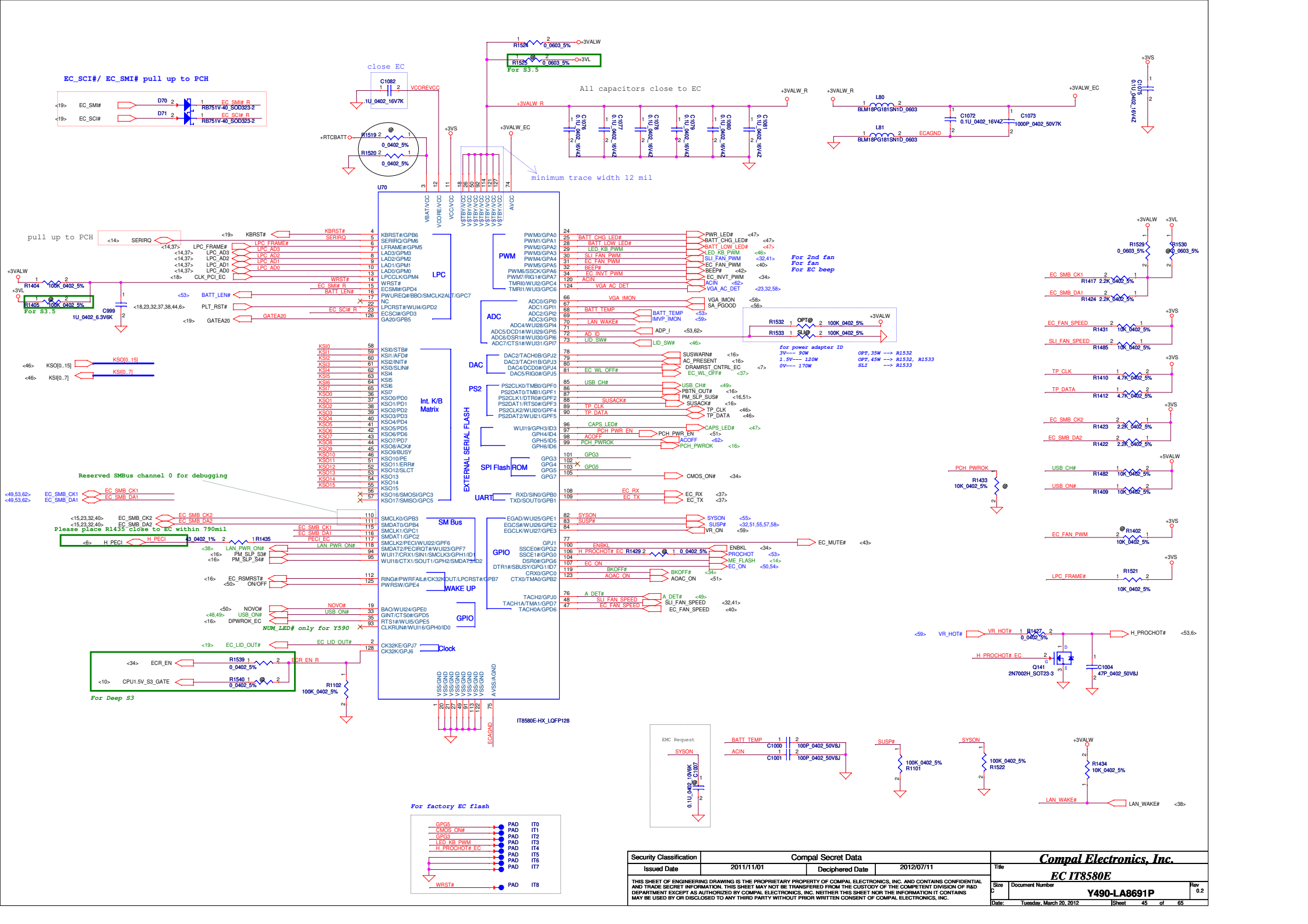
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2010/11/11

Compal Electronics, Inc.

Title: **Card reader JMB389**

Size	Document Number	Rev
B	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 44 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **EC IT8580E**

Size	Document Number	Rev
C	Y490-LA8691P	0.2

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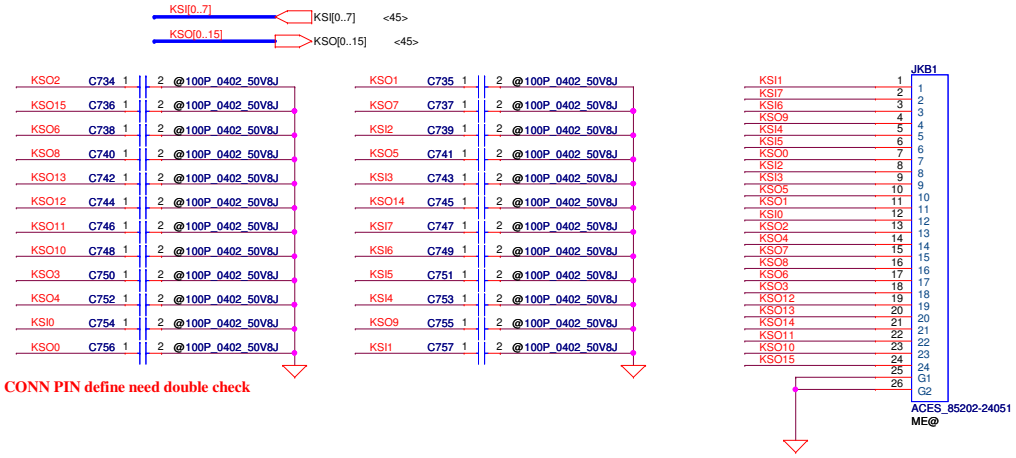
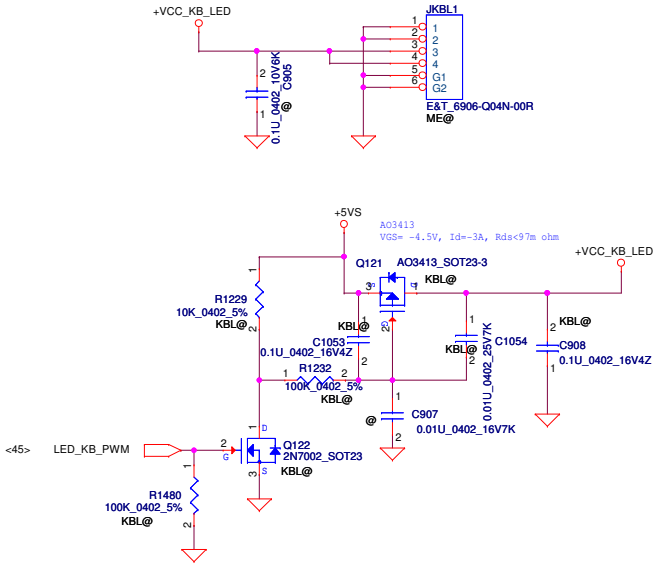
14" INT_KBD Conn.

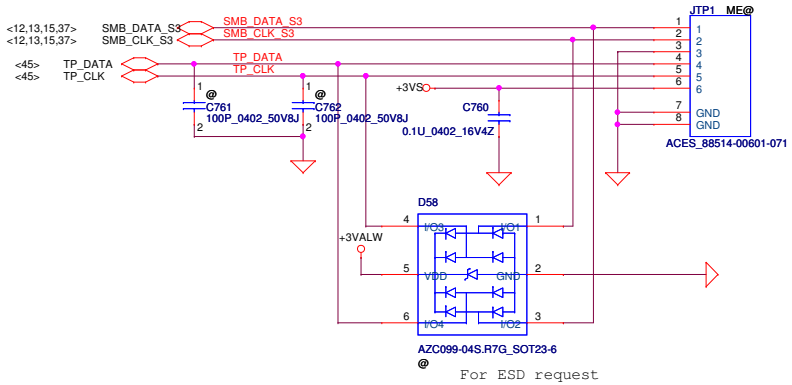


CONN PIN define need double check

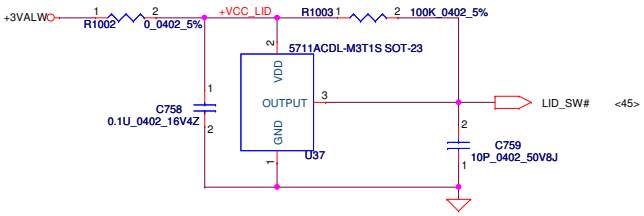
KB Lighting CONN.4pin



To TP/B Conn.

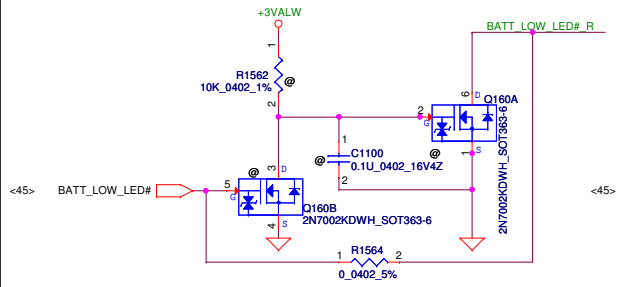


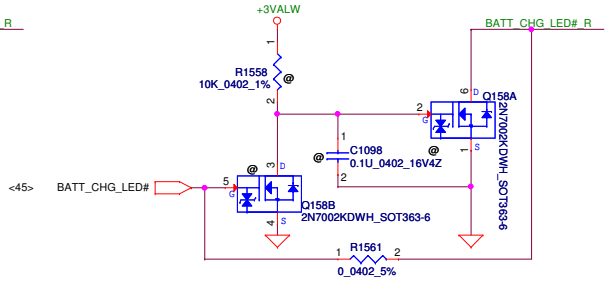
Lid Switch



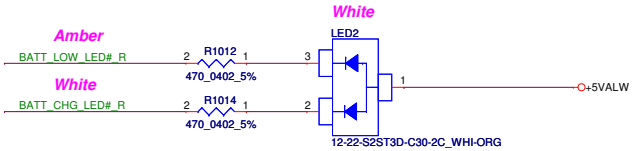
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

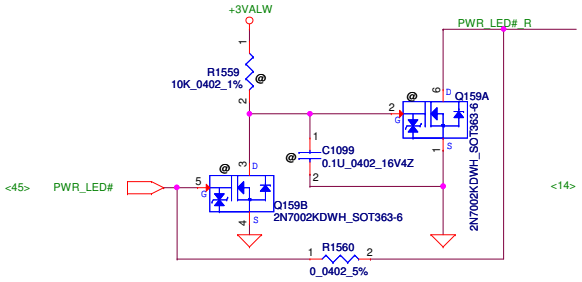
Compal Electronics, Inc.			
Title	KB /SW /LPC Debug Conn.		
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 46 of 65		

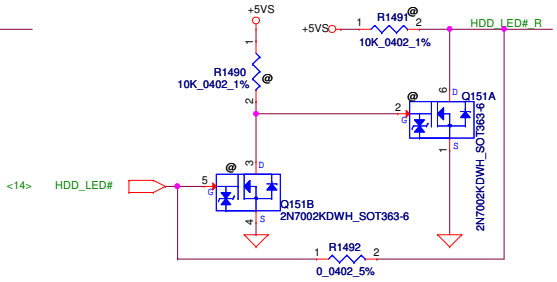




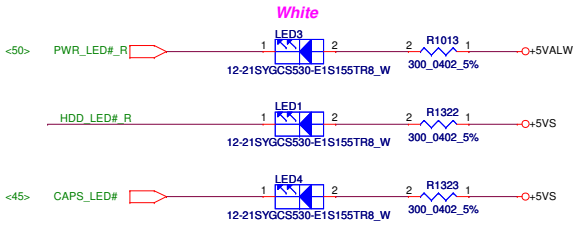
BATT CHARGE/LOW LED

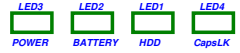




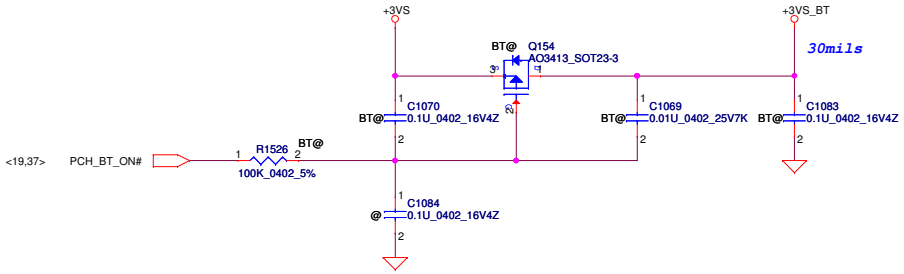


PWR LED HDD LED CapsLK LED

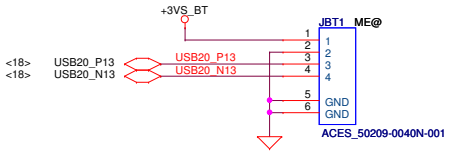




BlueTooth DC



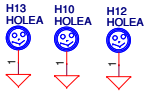
BT Conn.



Screw Hole

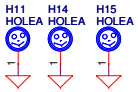
CPU and GPU: H_3P8X 6

C: H_3P8X 3



CPU

B: H_3P8X 3



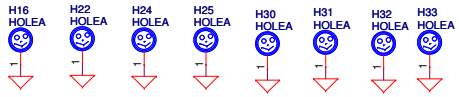
GPU

MIN PCIE: H_3P3 X 1

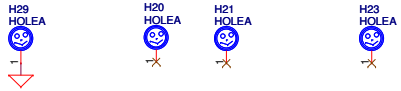
E: H_3P3X 1

ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

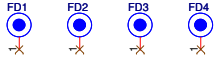
A: H_2P8X 8



E: H_3P3X 1 **H_4P0X3P0NX 3** **H_2P0X 2**



PCB Fedical Mark PAD



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LED/EC SPI ROM/BT

Size: Custom	Document Number: Y490-LA8691P	Rev: 0.2
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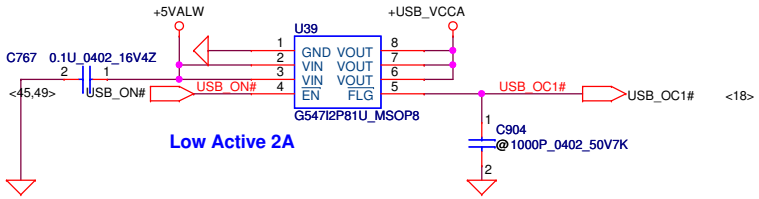
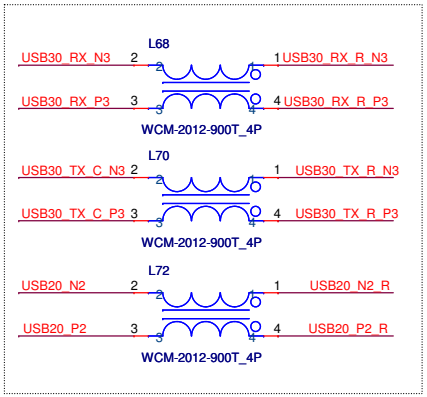
LEFT SIDE USB3.0 PORT X1

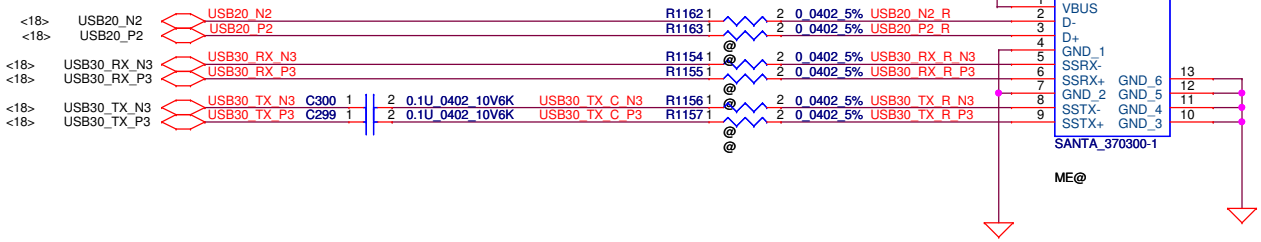


For EMI request

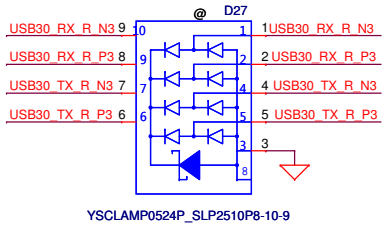
USB2.0 choke --> SM070000I00

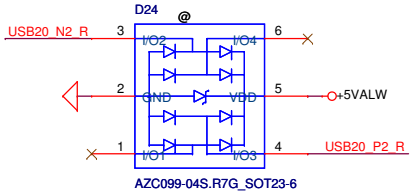
USB3.0 Choke --> SM070001U00





For ESD request





Security Classification	Compal Secret Data For EMI request		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: USB3.0 ports			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
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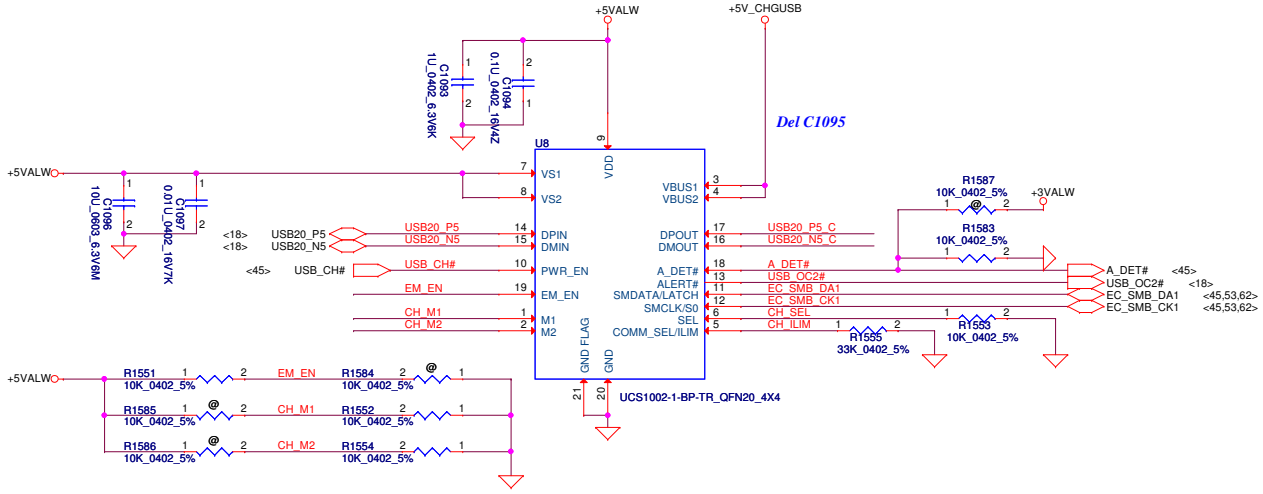
Sleep & Charge
Right side USB Charger Port (USB_Port5, near JMIC1)



Active Mode Selection:

	M1	M2	EM_EN	ACTIVE MODE
*	0	0	1	Dedicated Charger Emulation Cycle
	0	1	0	Date Pass-through
	0	1	1	BC1.2 DCP
	1	0	0	BC1.2 SDP
	1	0	1	Dedicated Charger Emulation Cycle
	1	1	0	Date Pass-through
	1	1	1	BC1.2 CDP

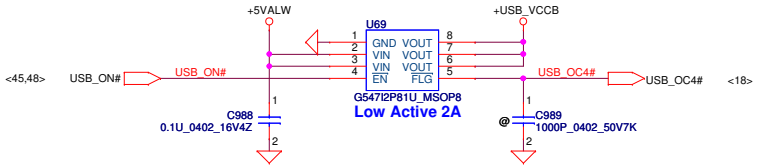
ILIM SETTING

Pull Low
0R-500mA
10K-900mA
12K-1000mA
15K-1200mA
18K-1500mA
22K-1800mA
27K-2000mA
* 33K-2500mA

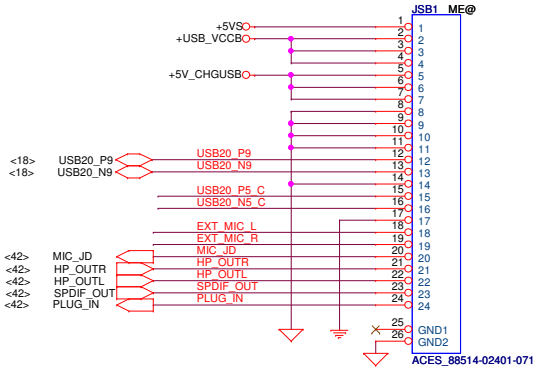
SEL Pin Decode

Pull Low
0R -1010_000
* 10K-1010_000
12K-1010_000
15K-1010_000
18K-0110_000
22K-0110_000
27K-0110_000
33K-0110_000

USB Power (USB20_P9)

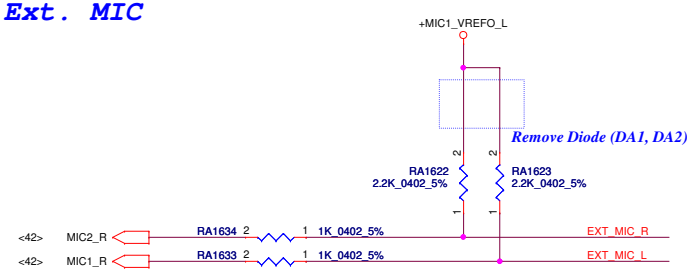


AUDIO/B Conn.



need change to 新貨 material
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

Ext. MIC



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Audio B Conn/USB charger

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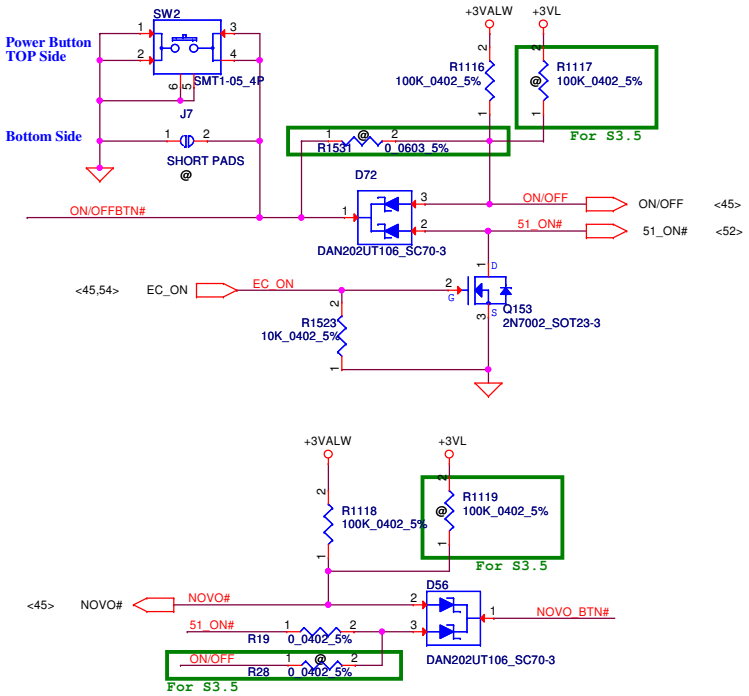
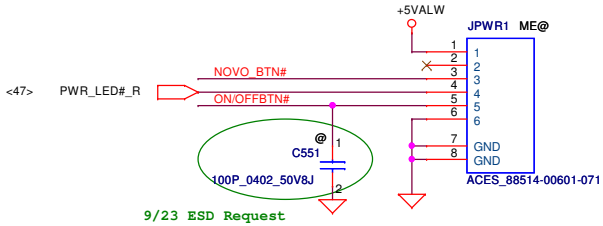
ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **other IO connector**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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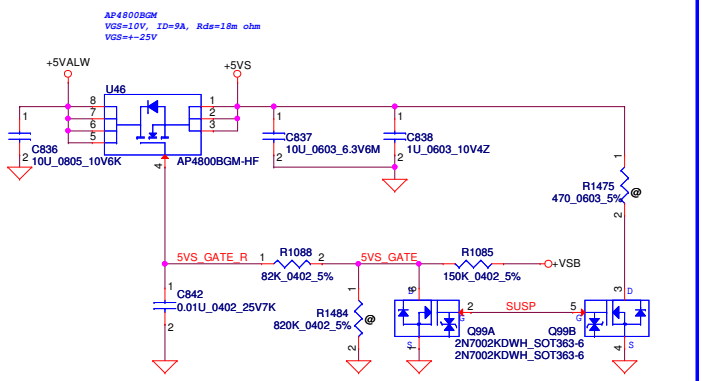
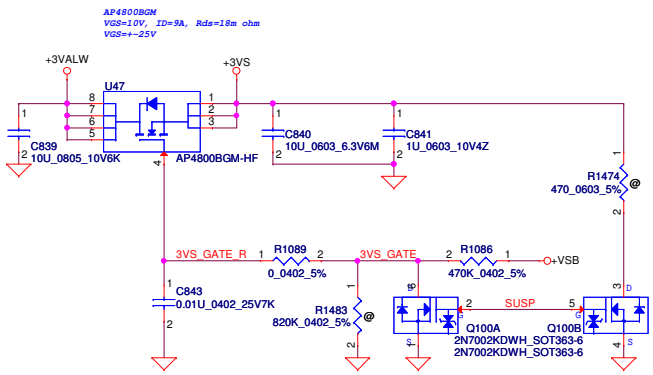
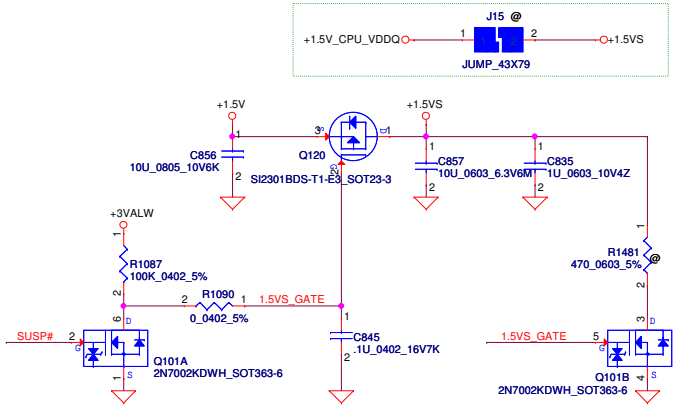
+5VALW to +5VS

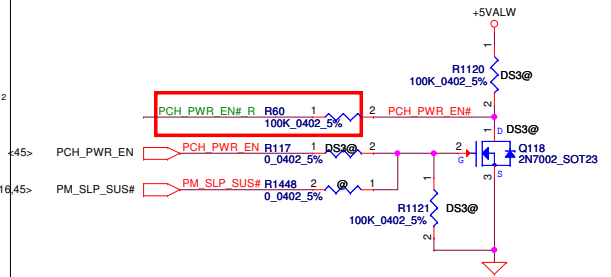


+3VALW to +3VS

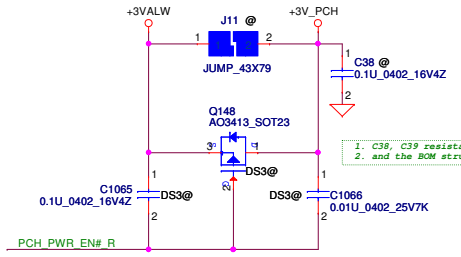


+1.5V to +1.5VS

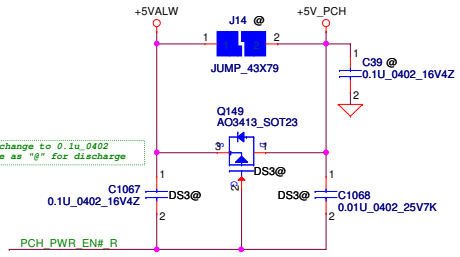


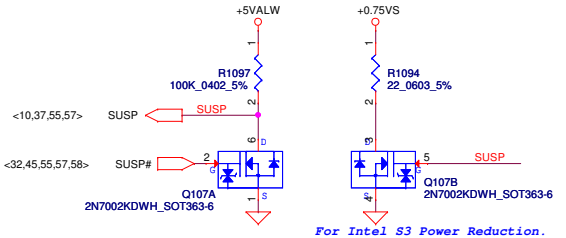


+3VALW to +3V_PCH

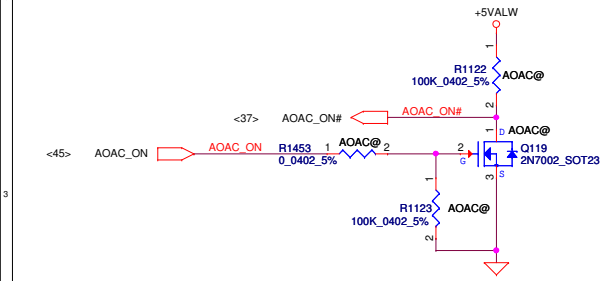


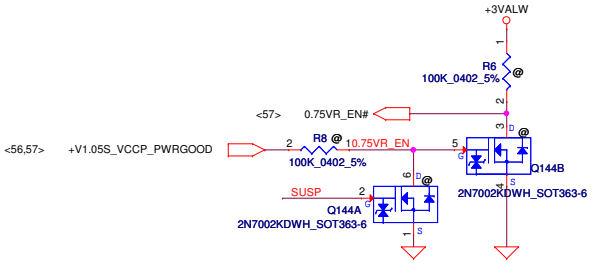
+5VALW to +5V_PCH





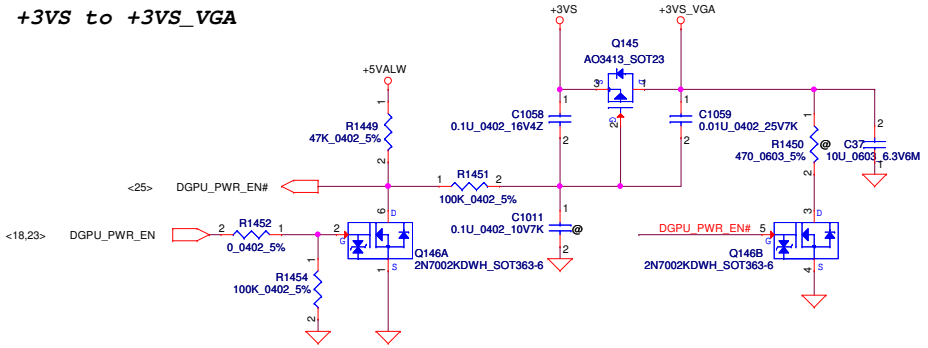
For Intel S3 Power Reduction.



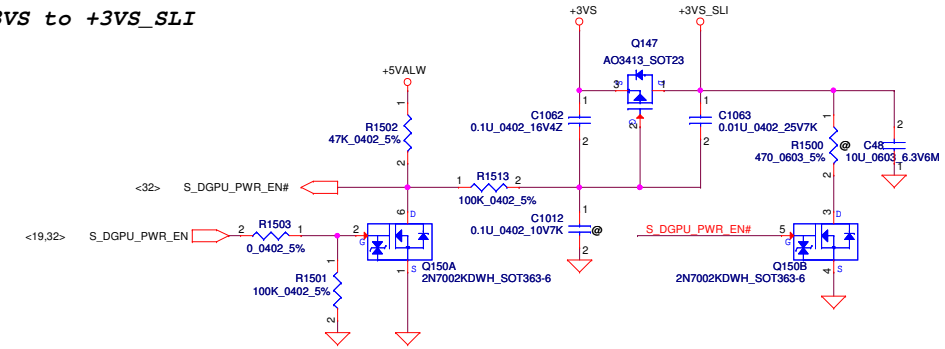


For S3 CPU Power Saving

+3VS to +3VS_VGA



+3VS to +3VS_SLI



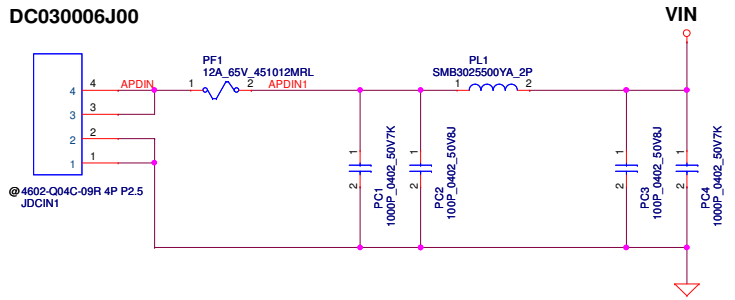
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

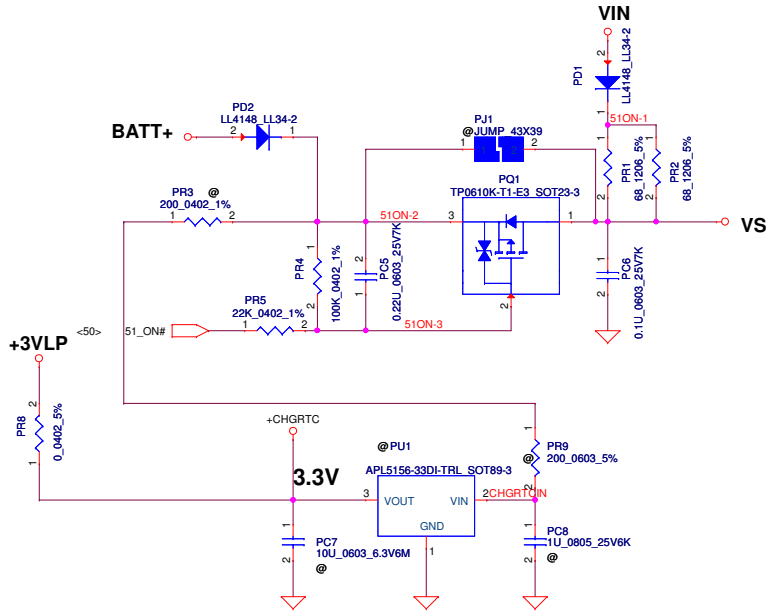
Compal Electronics, Inc.

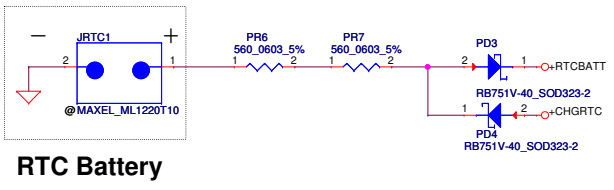
Title: **DC Interface**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 51 of 65







RTC Battery

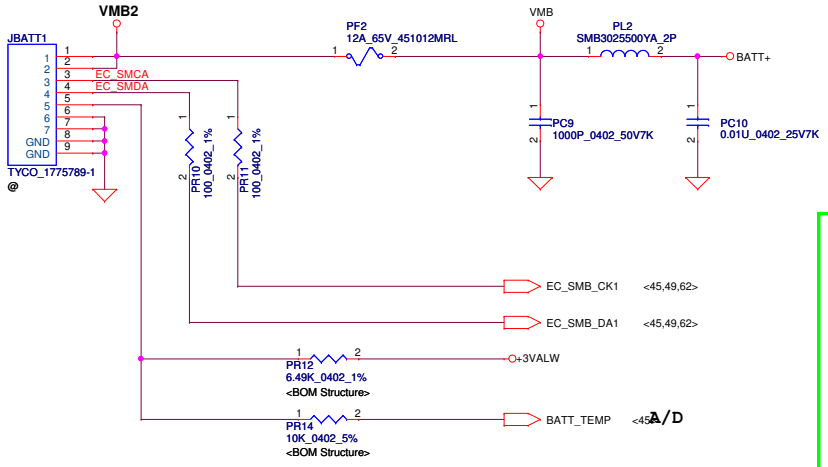
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Vin Detector

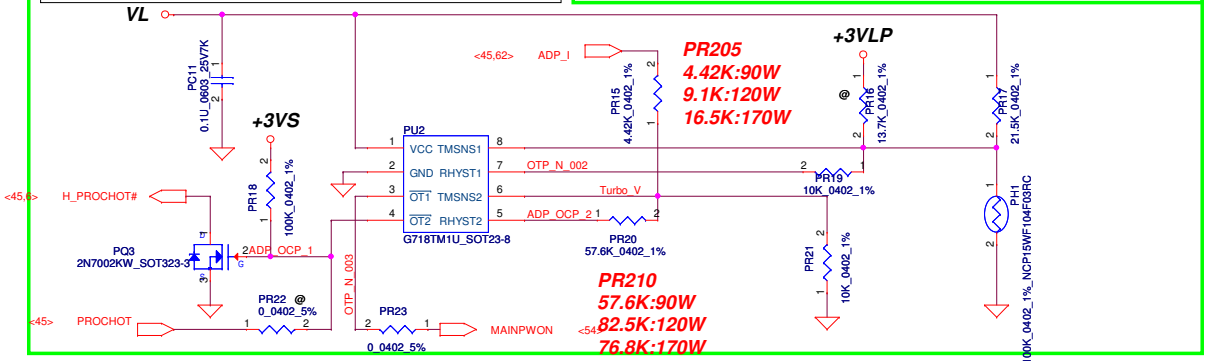
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.1

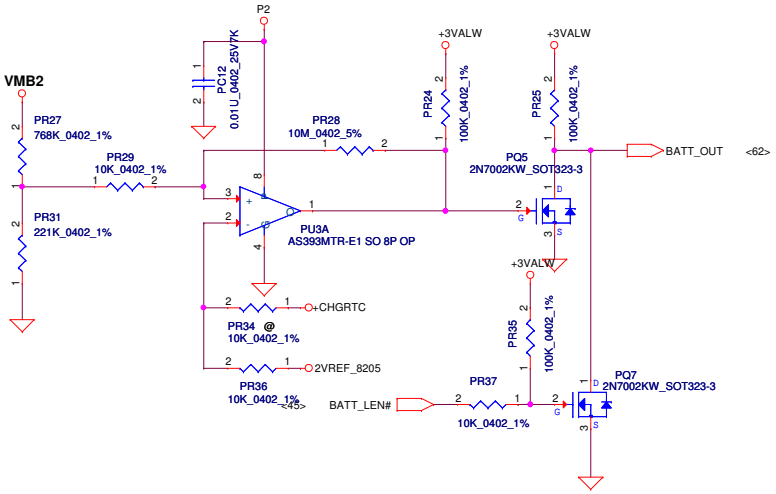
Date: Tuesday, March 20, 2012 | Sheet 52 of 65

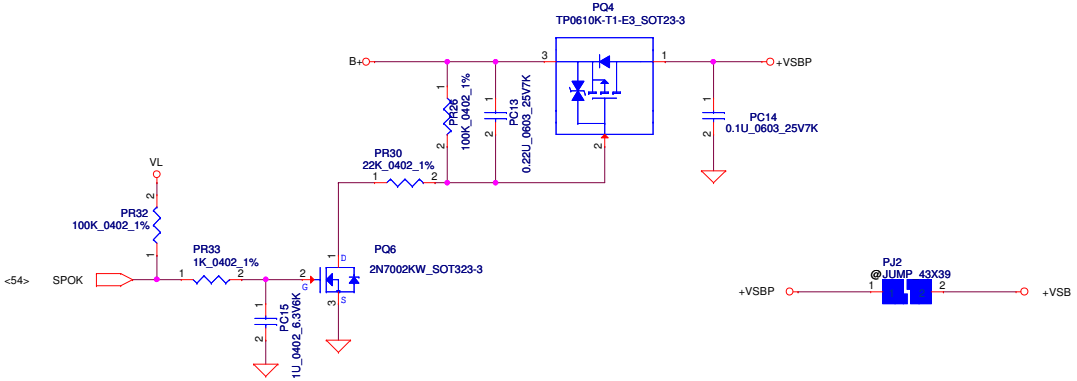


PH1 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206
PH201, PR205,PR211,PQ201,PR208,PR212



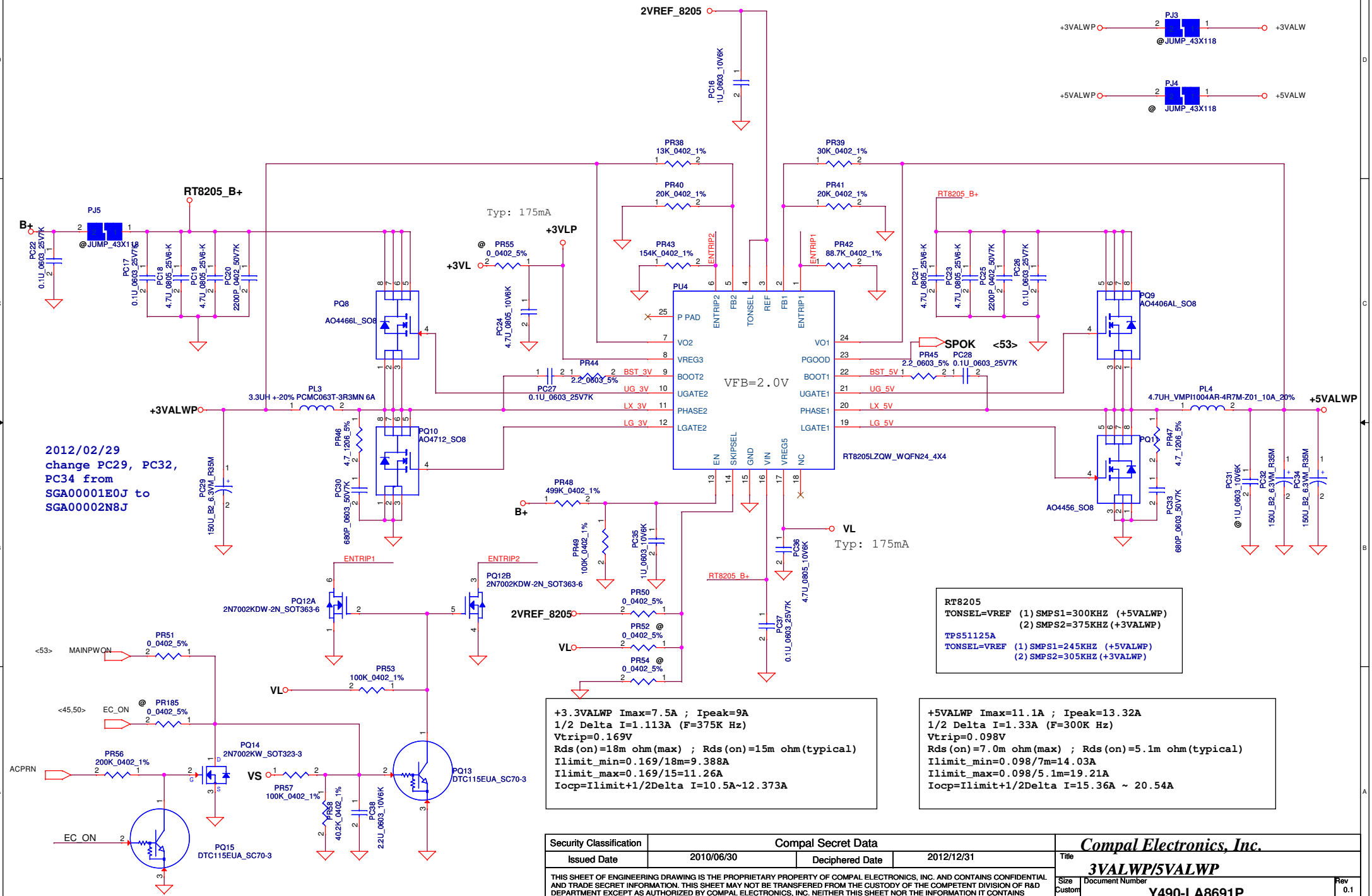




Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: BATTERY CONN/OTP			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.1
Date: Tuesday, March 20, 2012	Sheet 53 of 65		

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)
TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)

+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

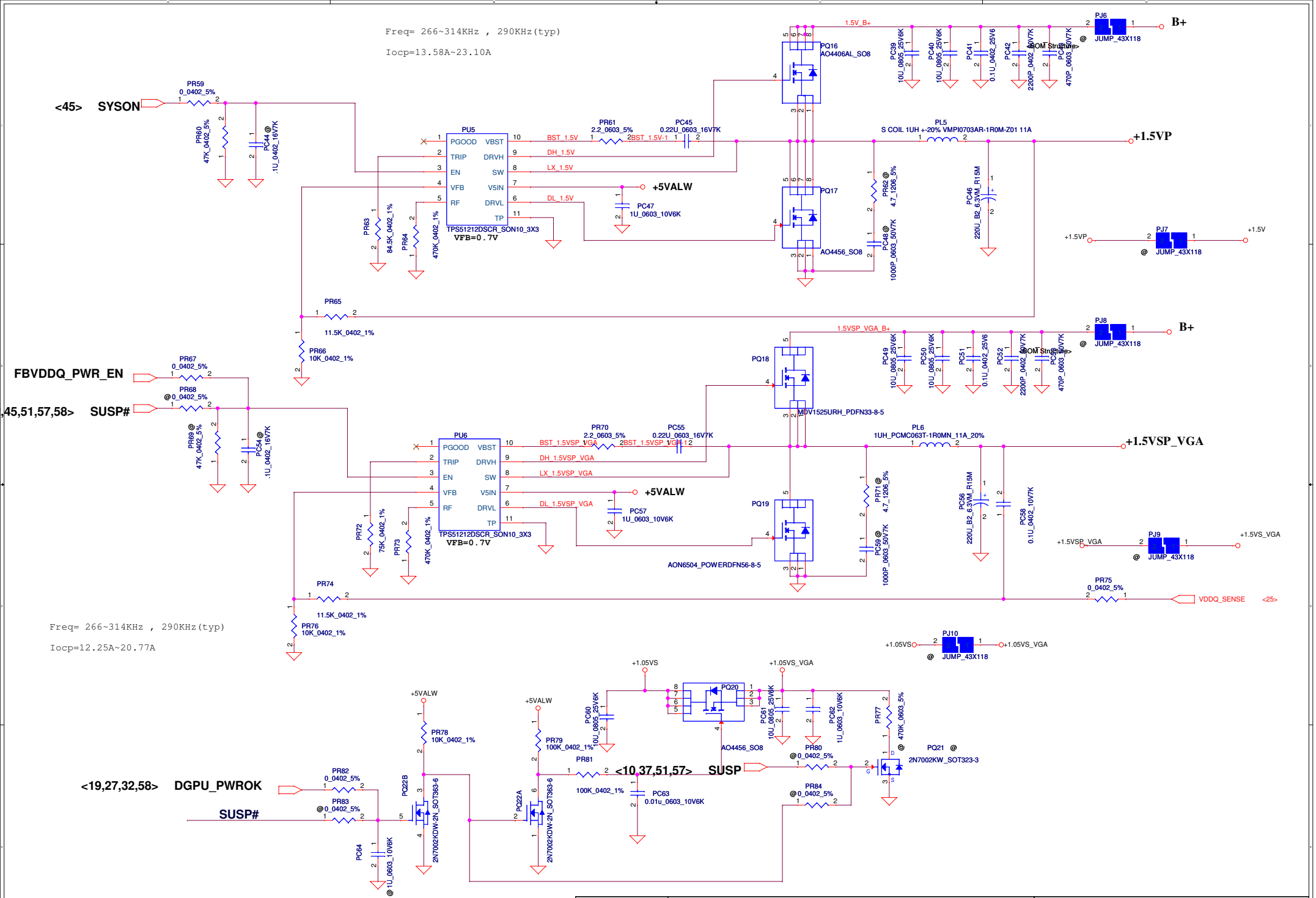
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	Y490-LA8691P	0.1

Date: Tuesday, March 20, 2012 Sheet 54 of 65



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: *1.5VP/1.5VSP_VGA/1.05VSP_VGA*

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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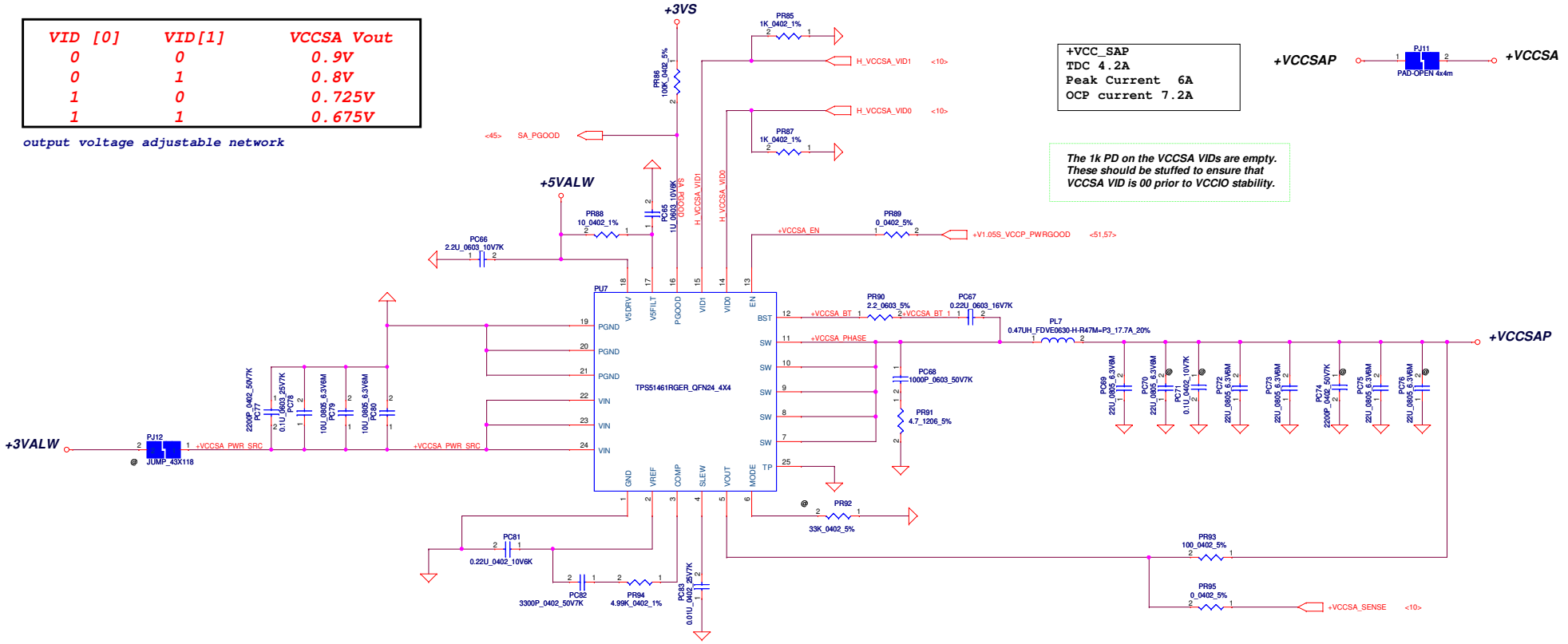
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



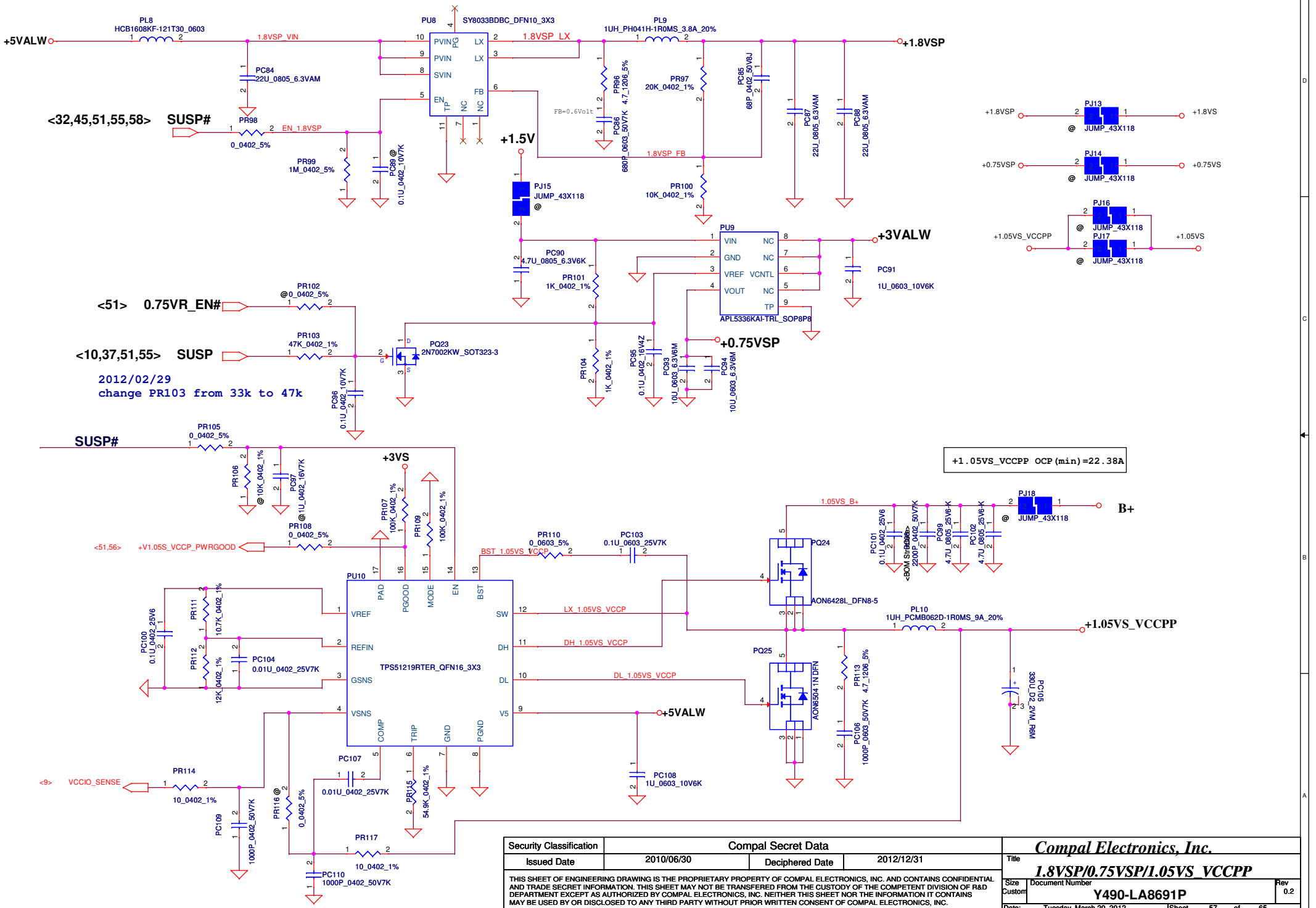
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: VCCSAP/1.05S_VCCPP

Size	Document Number	Rev
C	Y490-LA8691P	0.1

Date: Tuesday, March 20, 2012 Sheet 56 of 65



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 1.8VSP/0.75VSP/1.05VS_VCCPP

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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I_TDC=33.6A
Iccmax= 45A
OCP min=54A
Load line : -1.9 mV/A
FSW=600KHz

<23> GPU_VID5
<23> GPU_VID4
<23> GPU_VID3
<23> GPU_VID2
<23> GPU_VID1
<23> GPU_VID0
<18> NVDD_PWR_EN
<32,45,51,55,57> SUSP#

Place PH2 close to hot spot

Place PH4 close to PHASE1 inductor on the same layer

2012/02/29
change PR164
from 5.49k to
7.87k

+VGA_CORE Near VGA Core

+VGA_CORE Under VGA Core

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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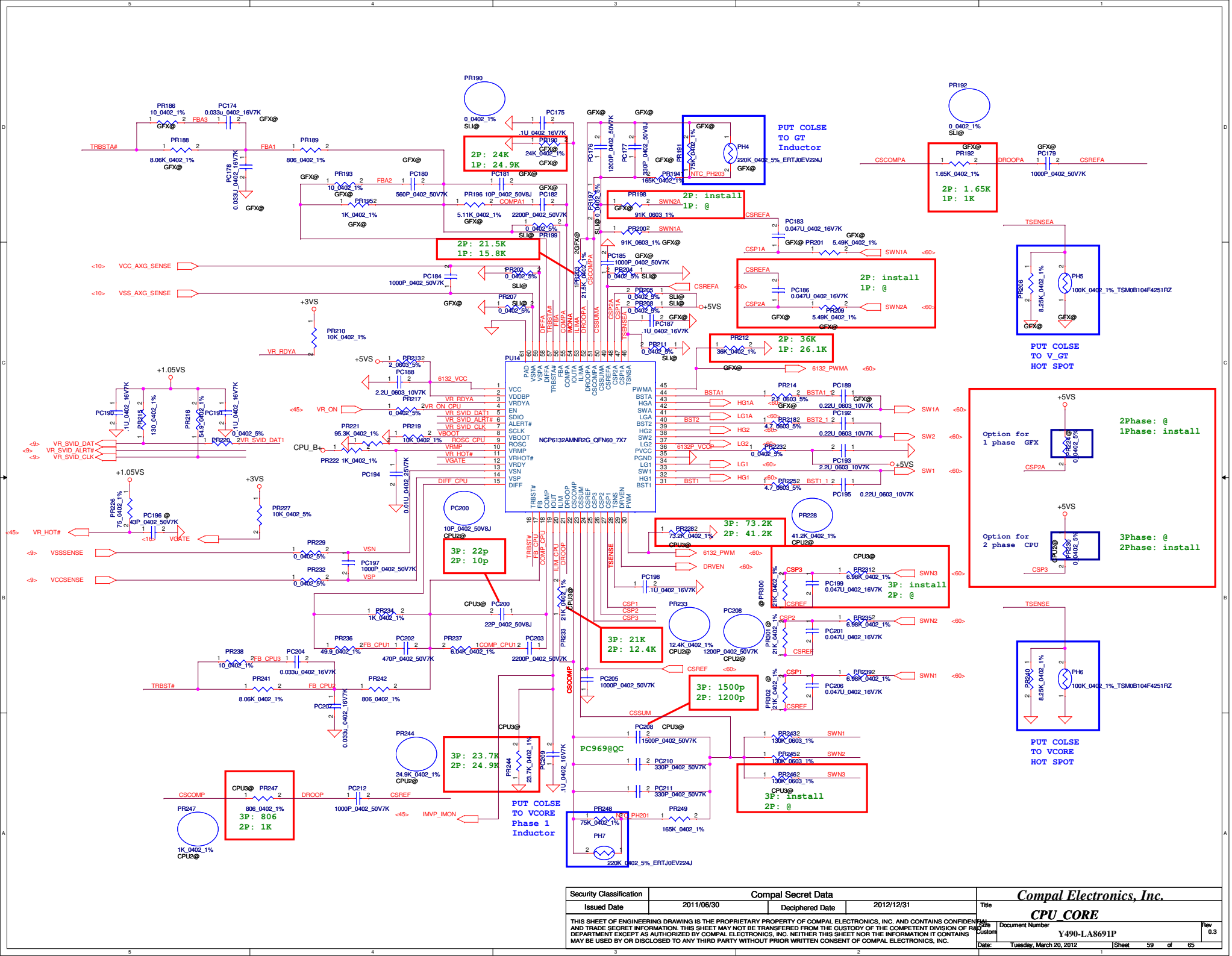
Compal Electronics, Inc.

Title: VGA_COREP

Size	Document Number	Rev
	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 58 of 65



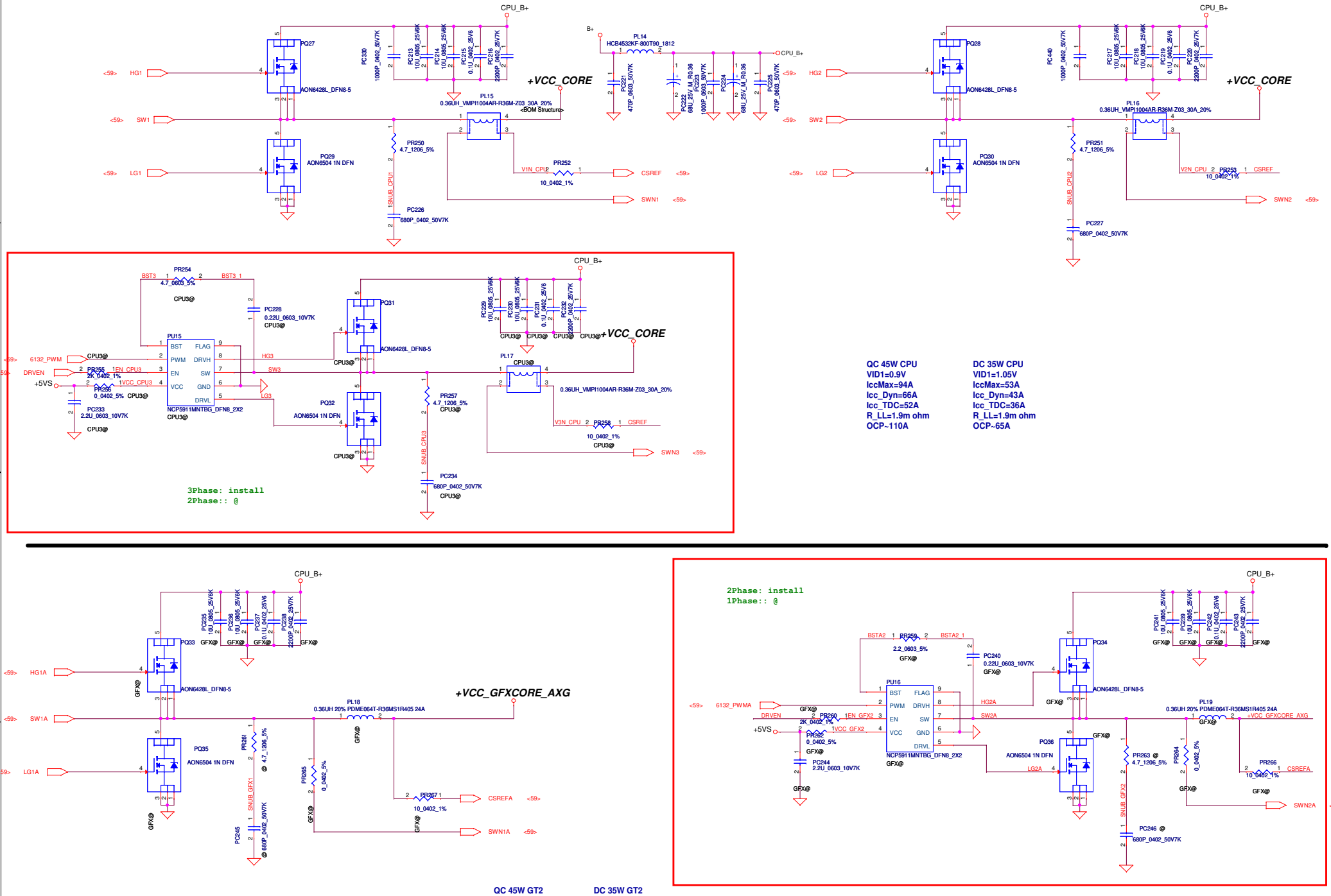
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	Y490-LA8691P	0.3

Date: Tuesday, March 20, 2012 | Sheet 59 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
C	Y490-LA8691P	0.3

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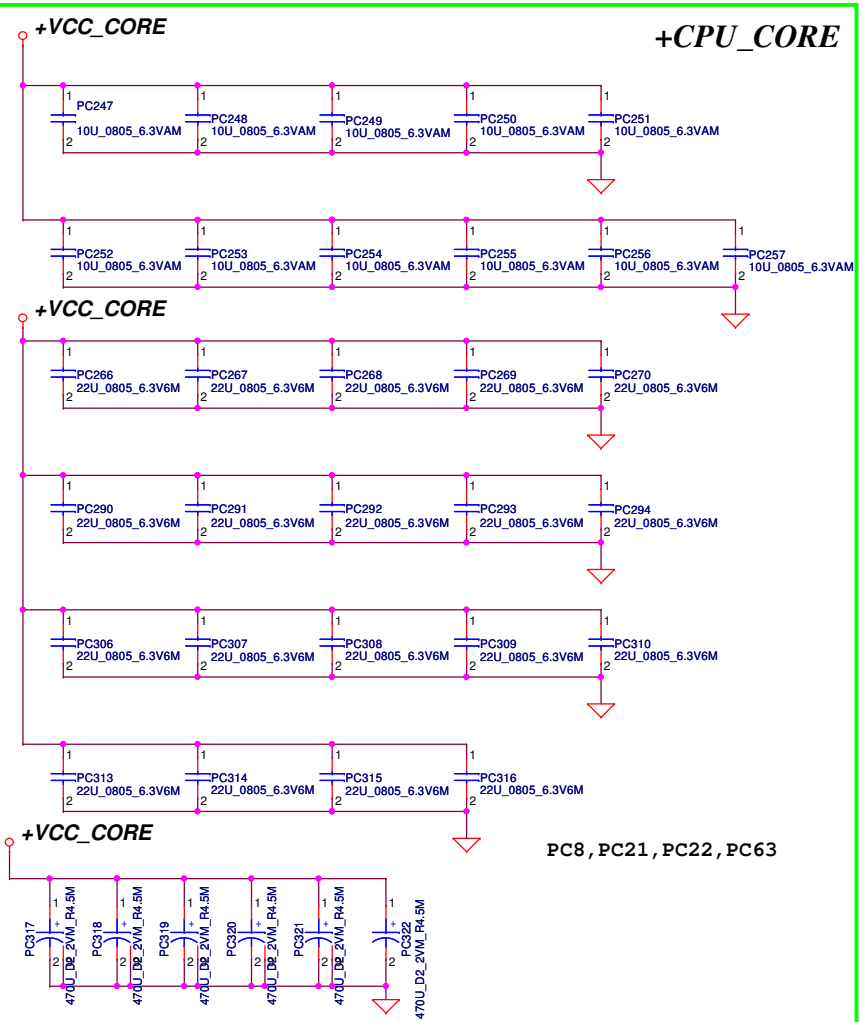
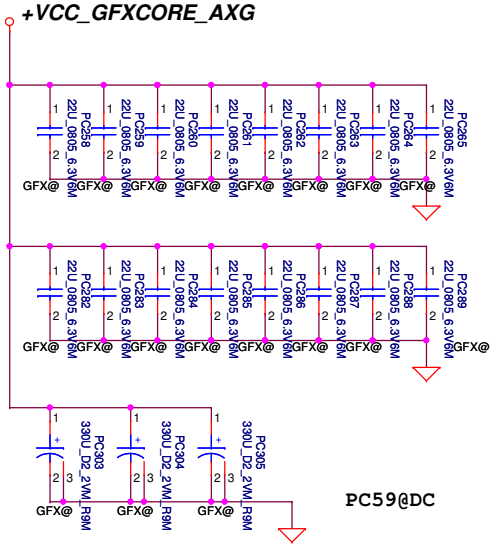
+CPU_CORE



PC8,PC21,PC22,PC63

DC:PC73,PC74,PC75,PC76,PC77,PC78(330uF/9m)
QC:PC76,PC78(470uF/4.5m),PC73,PC74,PC75(330uF/9m)

+VCC_GFXCORE_AXG



PC59@DC

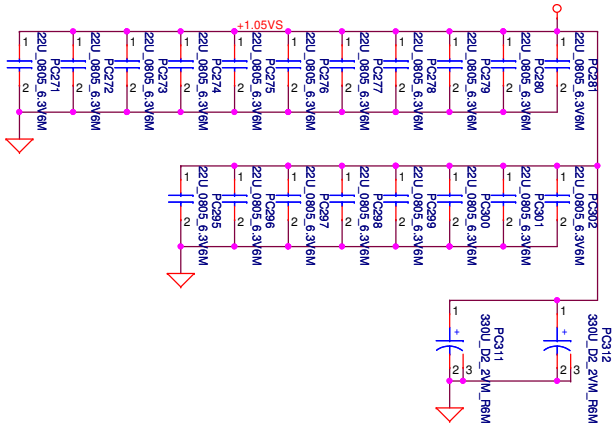
PC38,PC39,PC40,PC41

PC38,PC39,PC40,PC41

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS



PC32,PC49,PC54,PC55,PC56

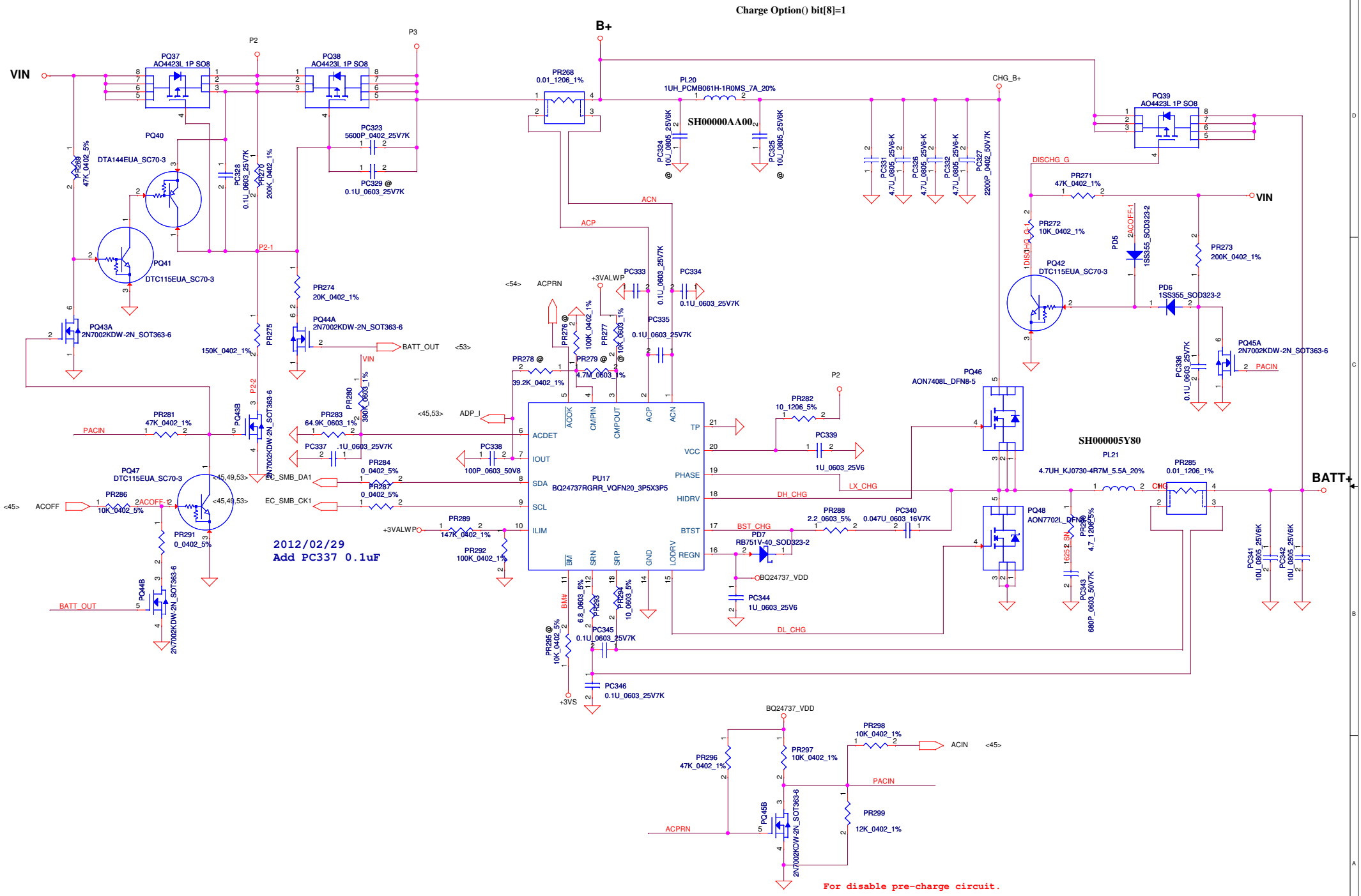
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE1

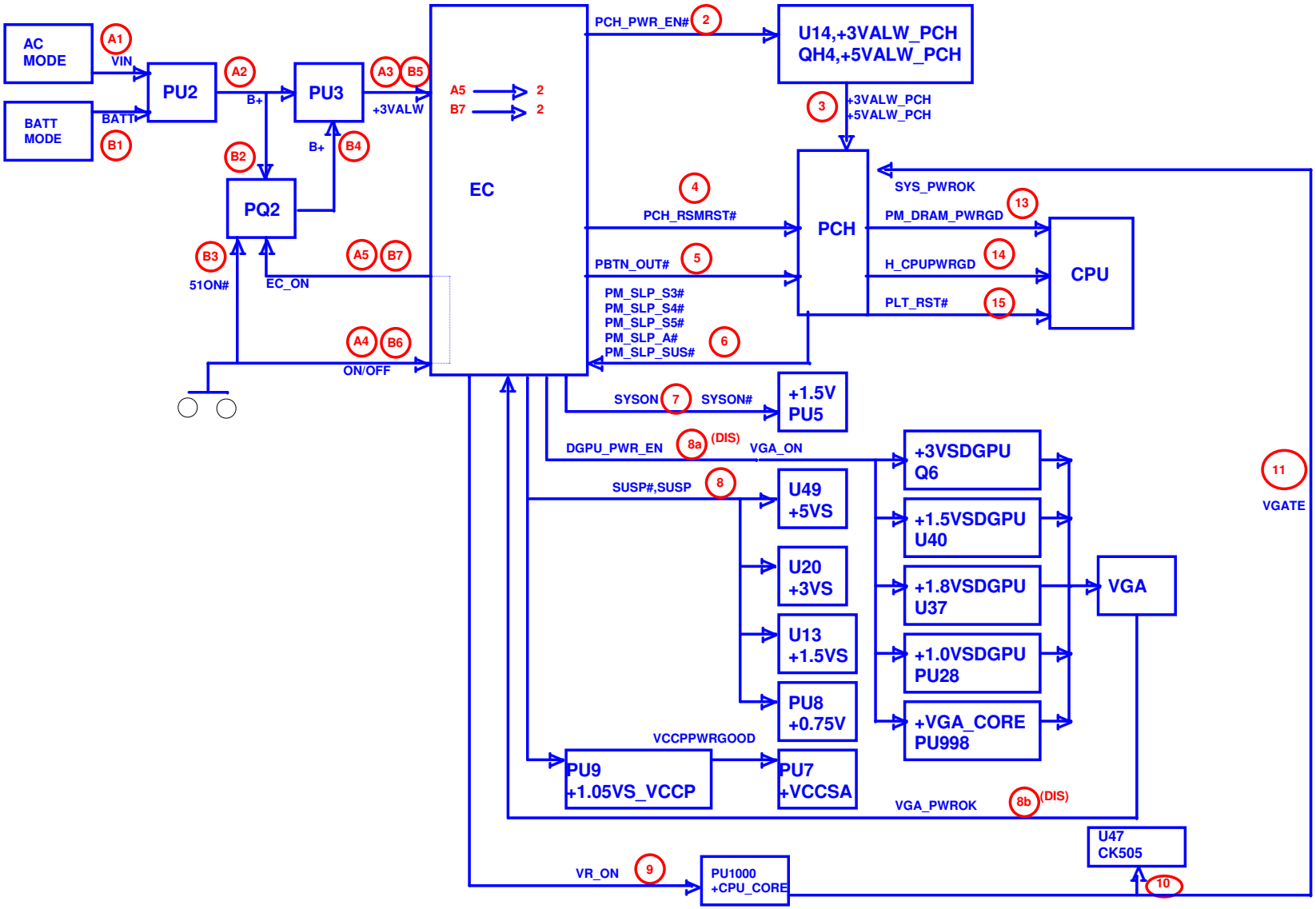
Size | Document Number: Y490-LA8691P | Rev: 0.1

Date: Tuesday, March 20, 2012 | Sheet 61 of 65



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	CHARGER
Size	Document Number: Y490-LA8691P
Rev	0.2
Date: Tuesday, March 20, 2012	Sheet 62 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: LA-8691P | Rev: 0.1

Date: Tuesday, March 20, 2012 | Sheet 63 of 65

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.1
Date: Tuesday, March 20, 2012 | Sheet 64 of 65

HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/21	Deciphered Date 2012/12/31	Title: LA-6882P PIR (HW)
			Size: Custom; Document Number; Rev: 0.1
			Date: Tuesday, March 20, 2012; Sheet 65 of 65