

Compal Confidential

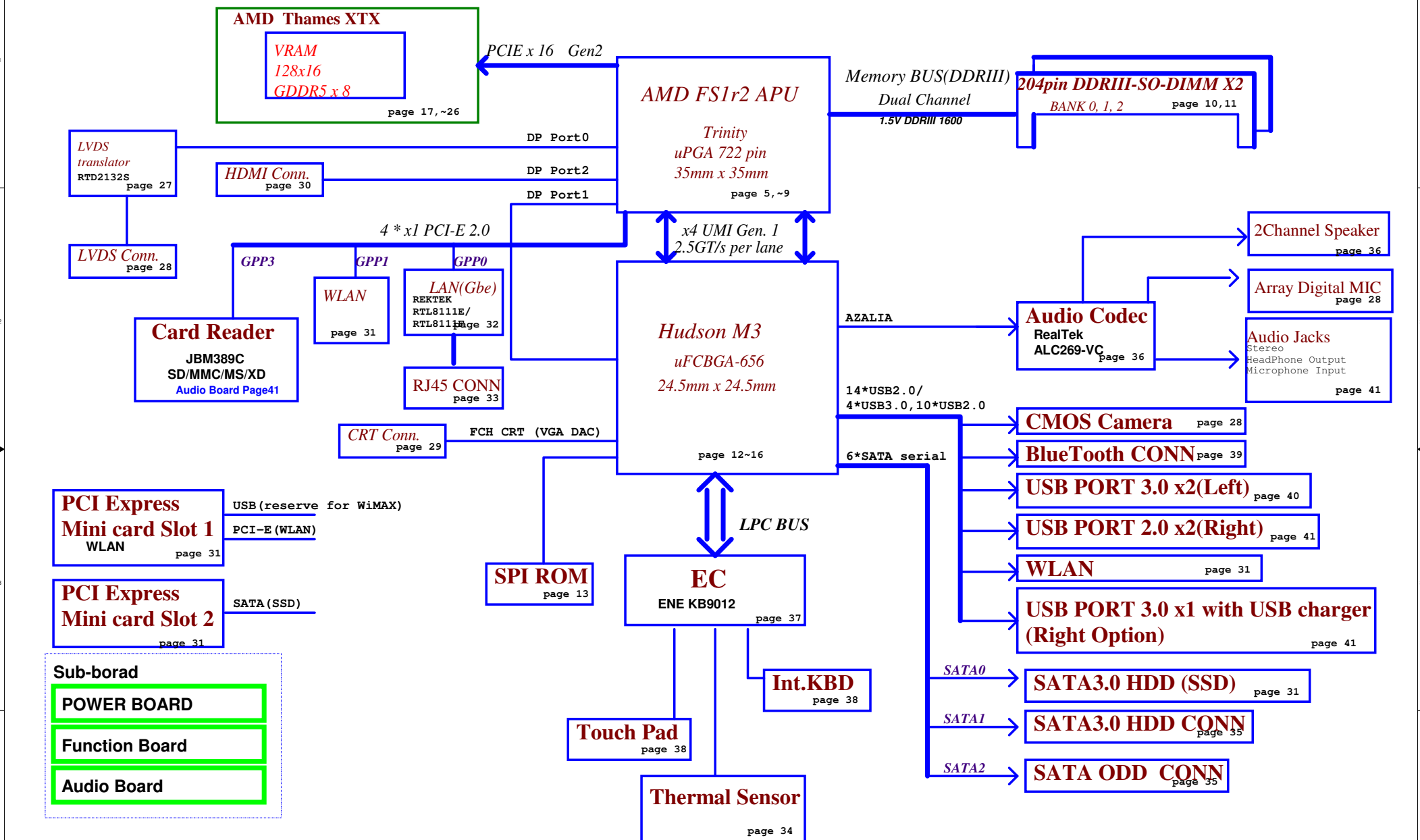
QAWYA M/B Schematics Document

AMD Fs1r2 Processor with DDRIII + Husdon M3 FCH
AMD VGA ThamesXTX

2011-12-05

REV : 0 . 2

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Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title		
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Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	MB Block Diagram	
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power plane State	+B	+5VALW +3VALW +1.1VALW	+1.5V +1.5V_APU	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +VGA_CORE +3.3VGS +1.8VGS +1.5VGS +1.0VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	
5	
6	
7	

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Ra = R310
Rb = R311

USB 2.0	USB 3.0	Port	4 External USB Port
		0	USB Port (Right Side)
		1	USB Port (Right Side/option)
		2	Mini Card(WLAN)
		3	Camera
		4	Blue Tooth
		5	
		6	
		7	
		8	
		9	
		10	USB Port (Left Side)
		11	USB Port (Left Side)
	XHCI	12	USB Port (Right Side/option)
		13	

[illegible]

OC#	USB Port	
0	USB20 port10,port11	USB30 port0,port1
1	USB20 port0	
2	USB20 port1,port12	USB30 port2
3		

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader

Port	Device
1	
2	
3	
4	

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X	X
SMB_EC_CK2_SUS SMB_EC_DA2_SUS	KB9012 +3VALW	X	X	X	X	X	X	X	V +1.5V	X
FCH_SCLK0 FCH_SDATA0	FCH +3VS	X	X	X	V +3VS	V +3VS	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS (LV shifter)	V	X	X	X	X	V	X	X	V

EC SM Bus2 address

Device	Device	Address
Smart Battery	0001_011X b	1001_101xb
	Thermal Sensor	1001_100xb
	SB-TS1(default)	1000_001xb
	VGA(thermal)	1010_1000b
	RTD2132S	

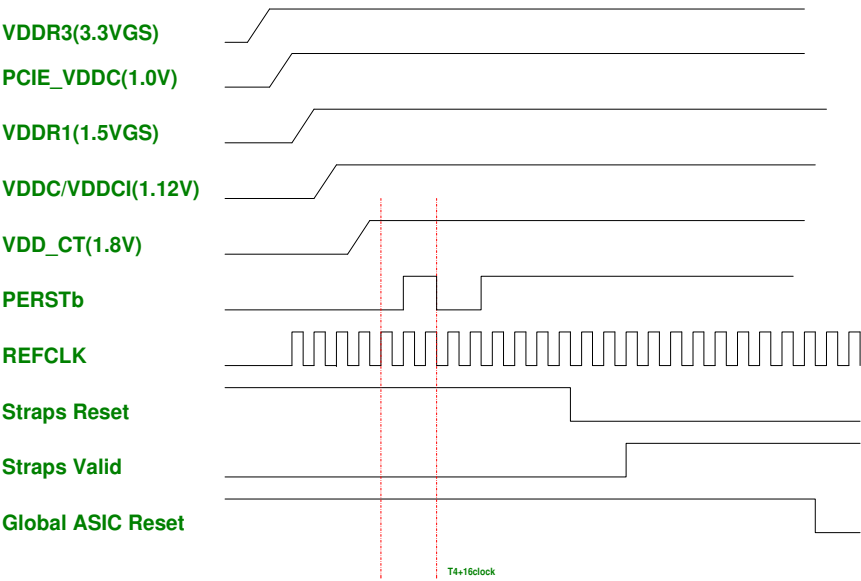
Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

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Power-Up/Down Sequence

"Thames" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa). For BACO enabled designs, VDDC must ramp up before VDD_CT at system power up.
- For power down, reversing the ramp-up sequence is recommended



Without BACO option :

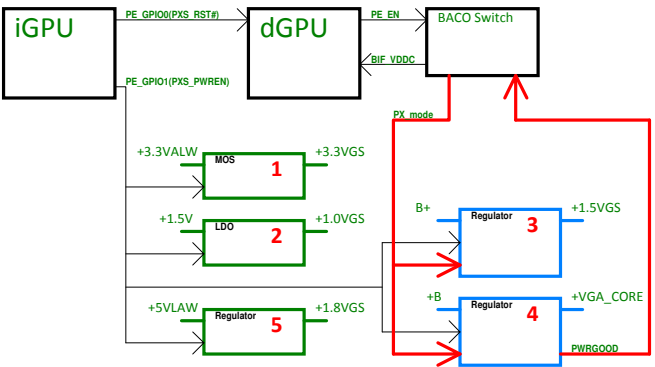
PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

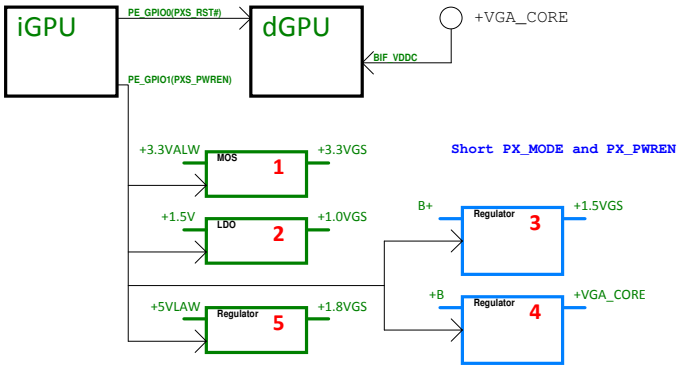
PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	775mA
PCIE_VDDC	1.0V	OFF	ON	1.1A
VDDR3	3.3V	OFF	ON	60mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	1.2A
VDDC/VDDCI	TBD	OFF	OFF	28

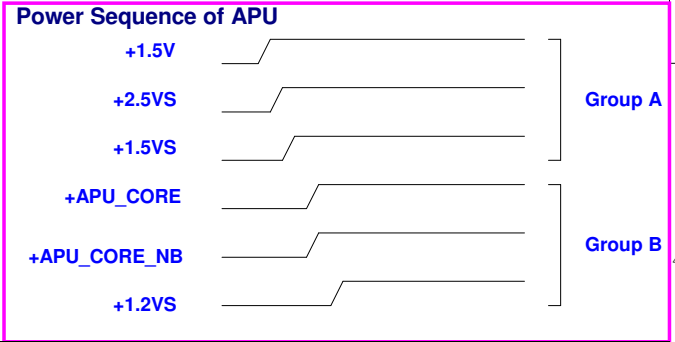
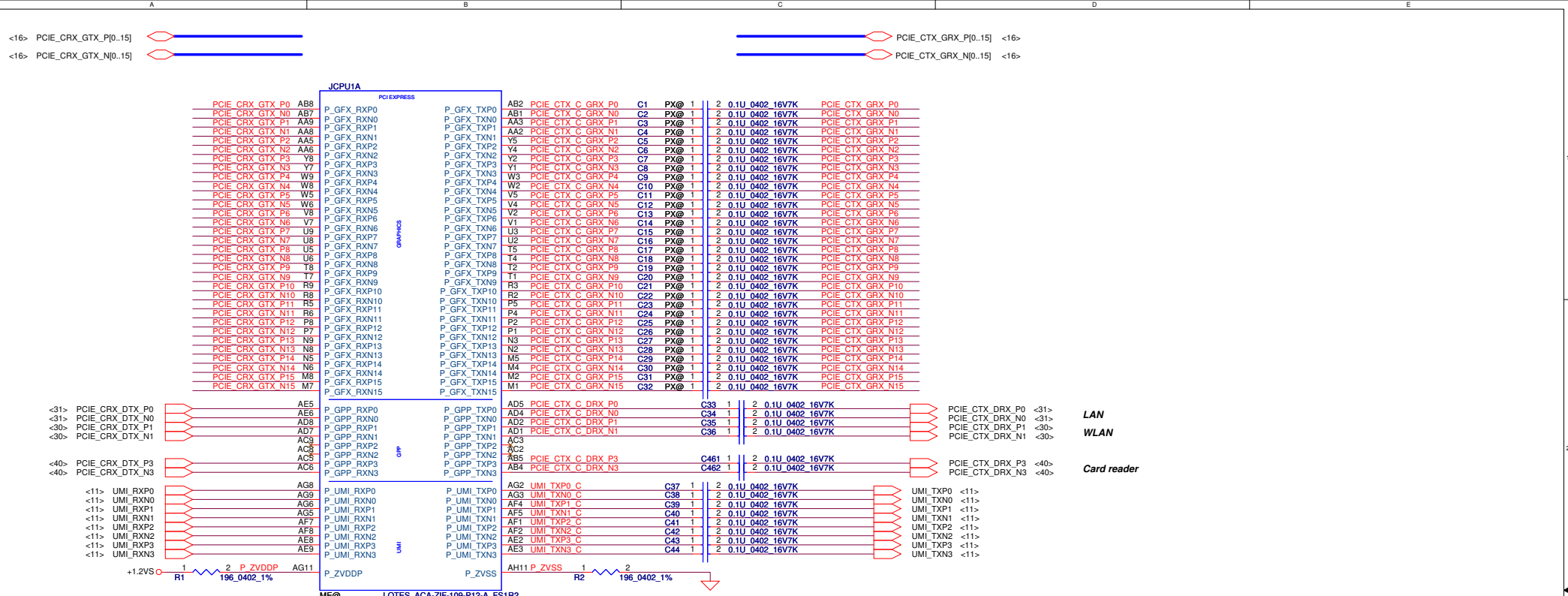
PX4.0



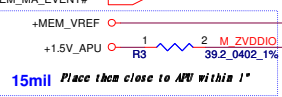
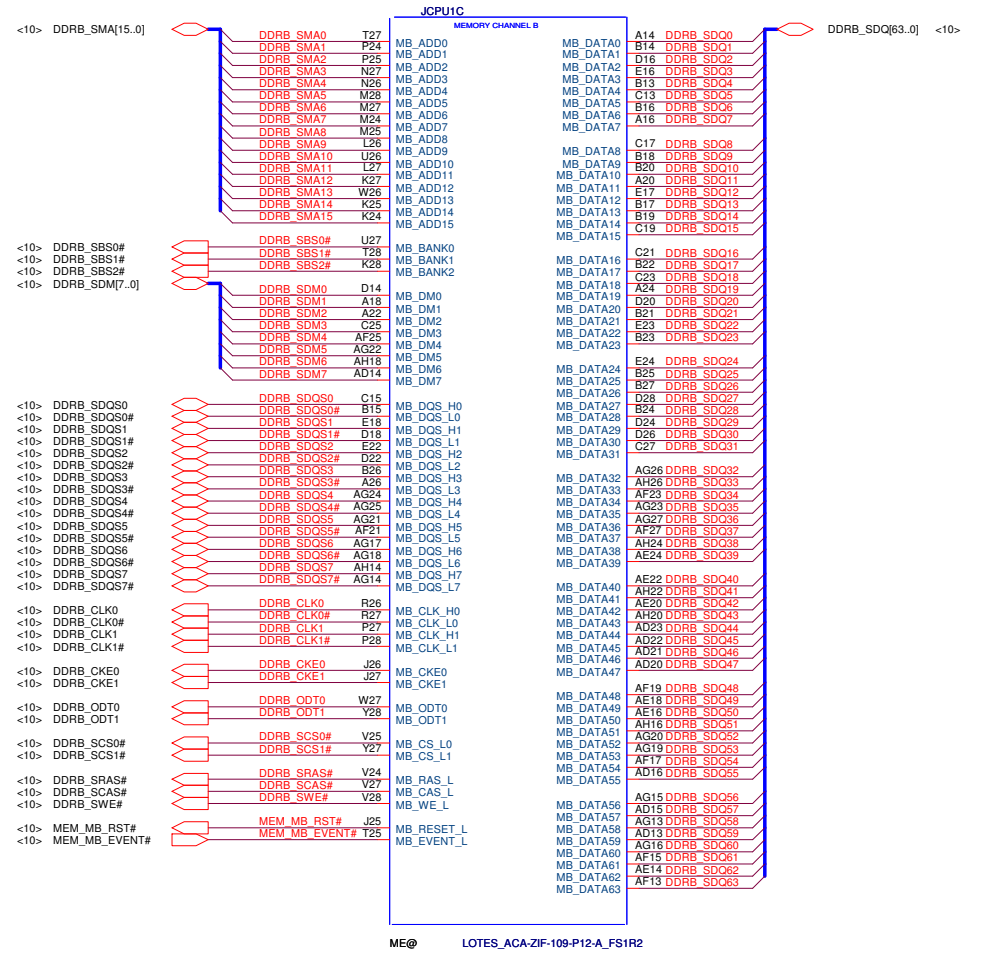
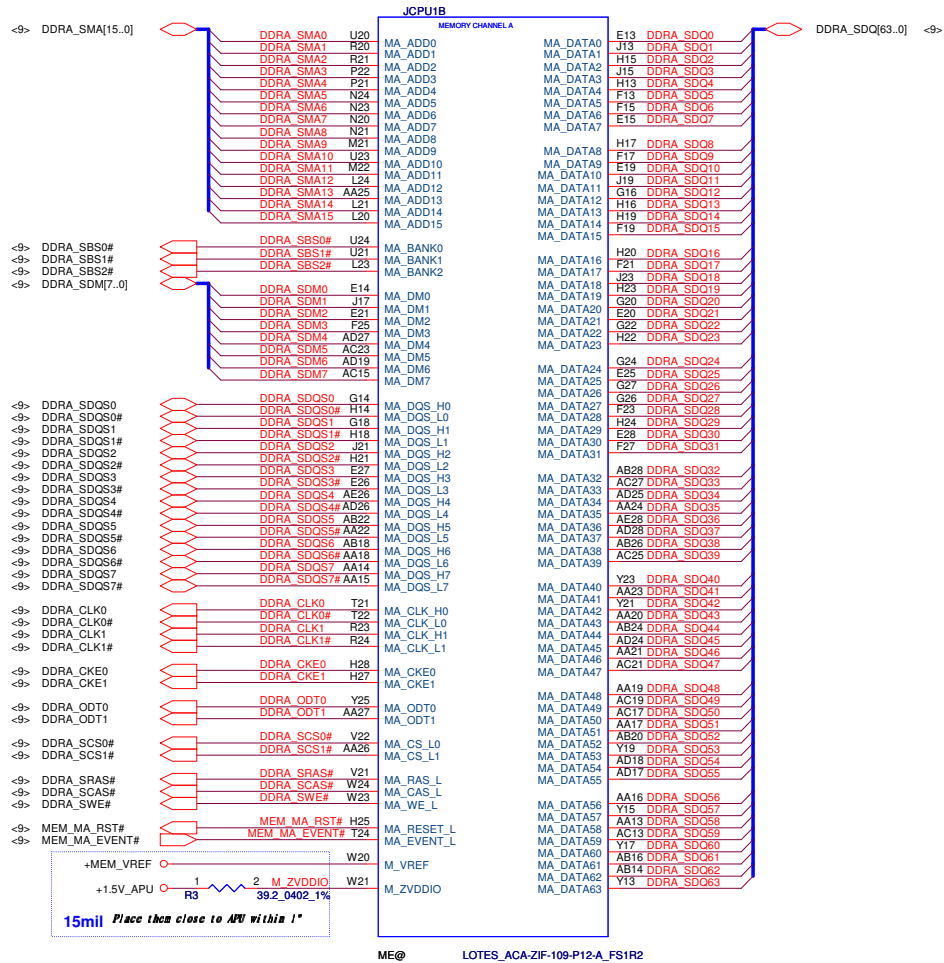
PX5.0



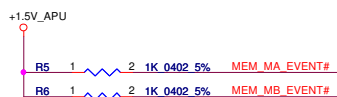
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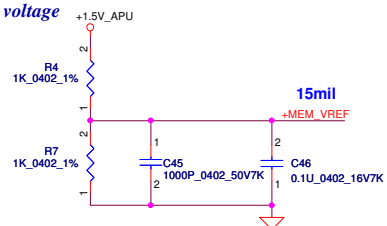
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EVENT# pull high



0.75V reference voltage



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Fs1r2 DDRIII Memory I/F

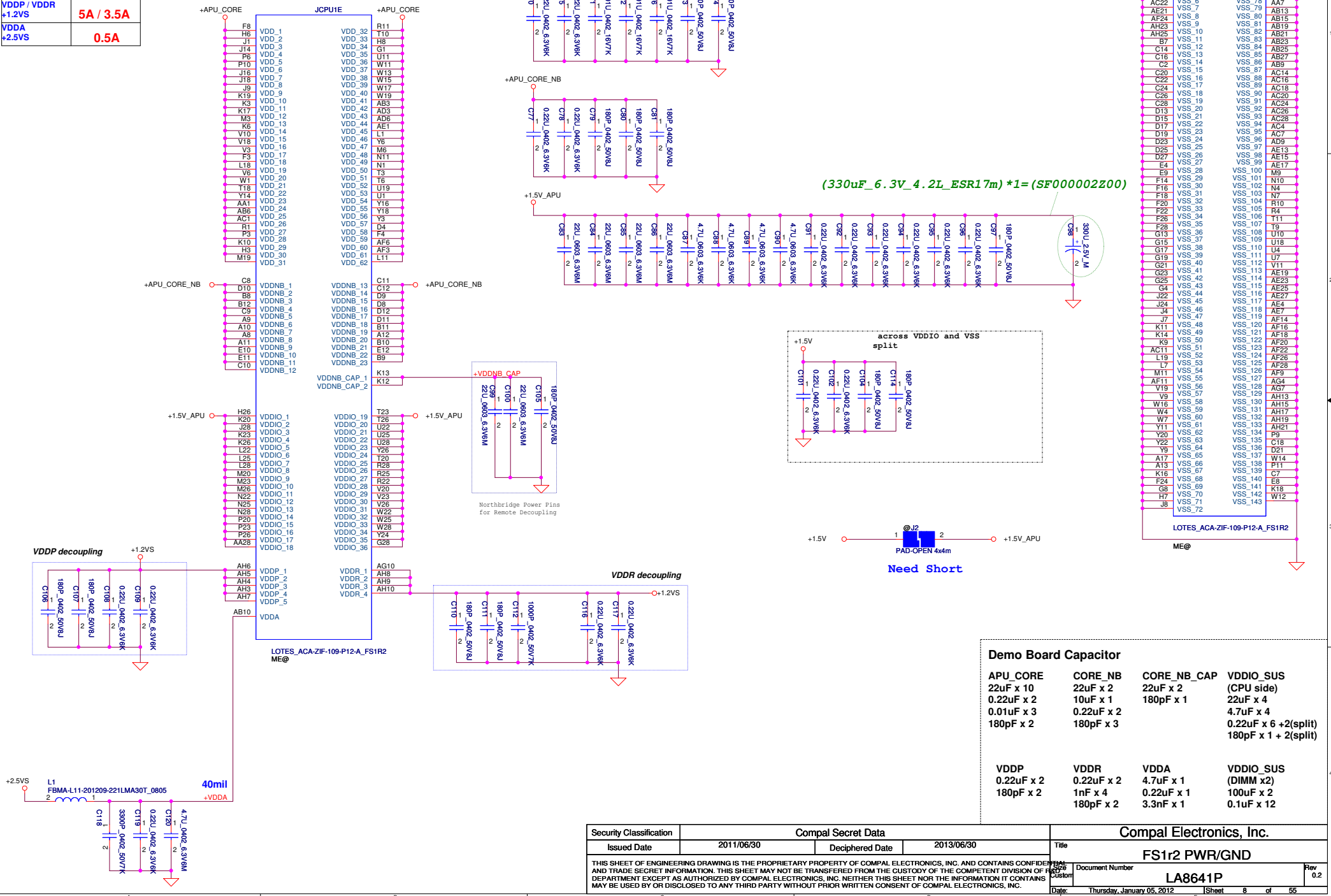
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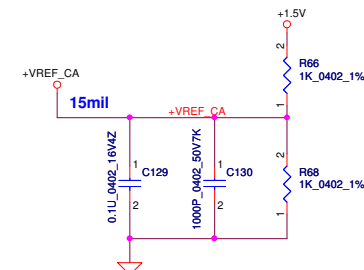
Rev

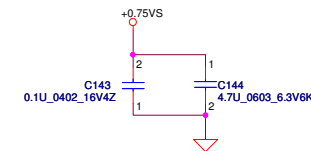
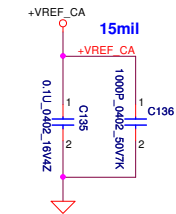
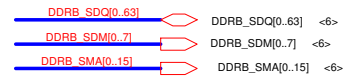
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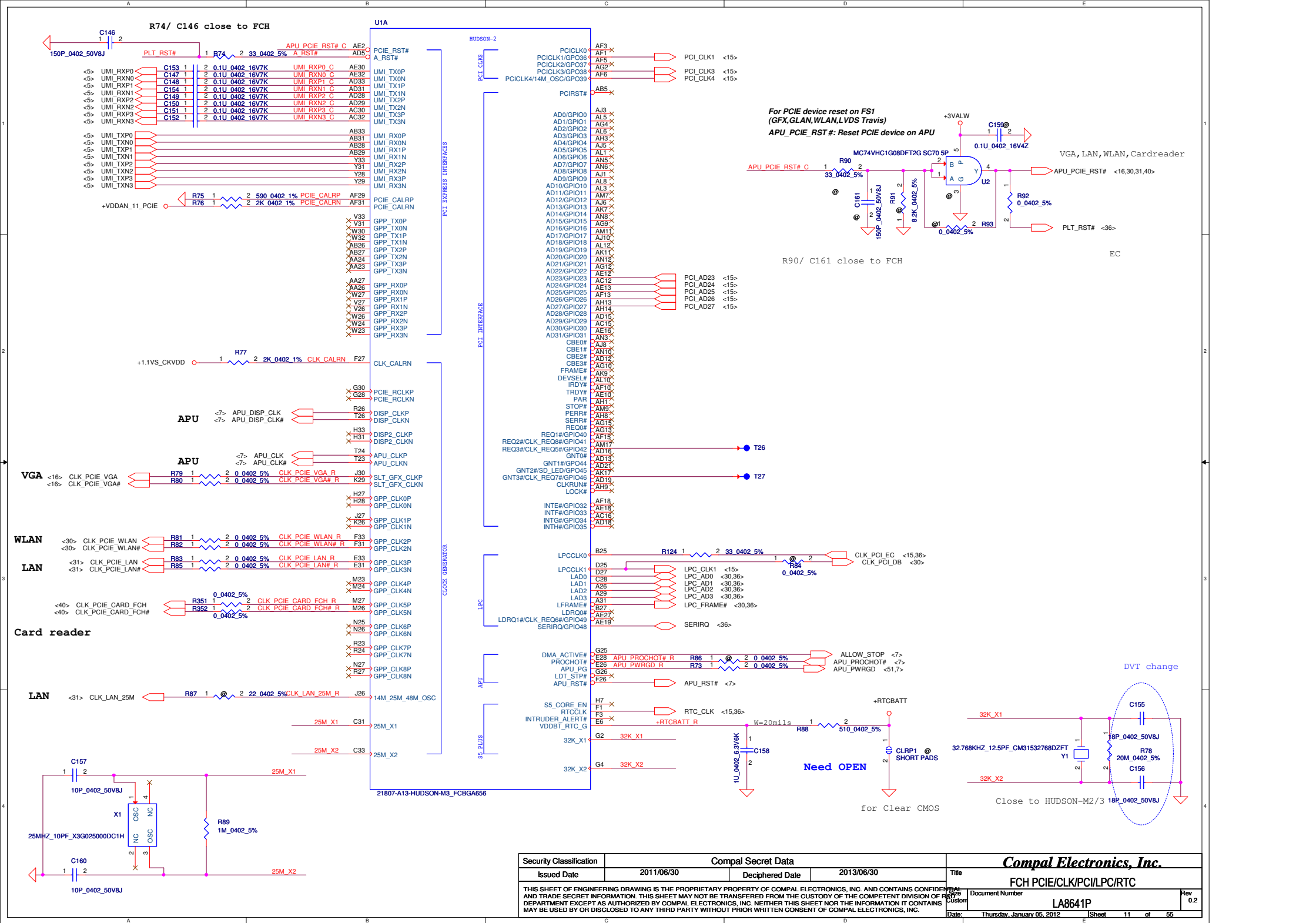
Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	29A
VDDP +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A





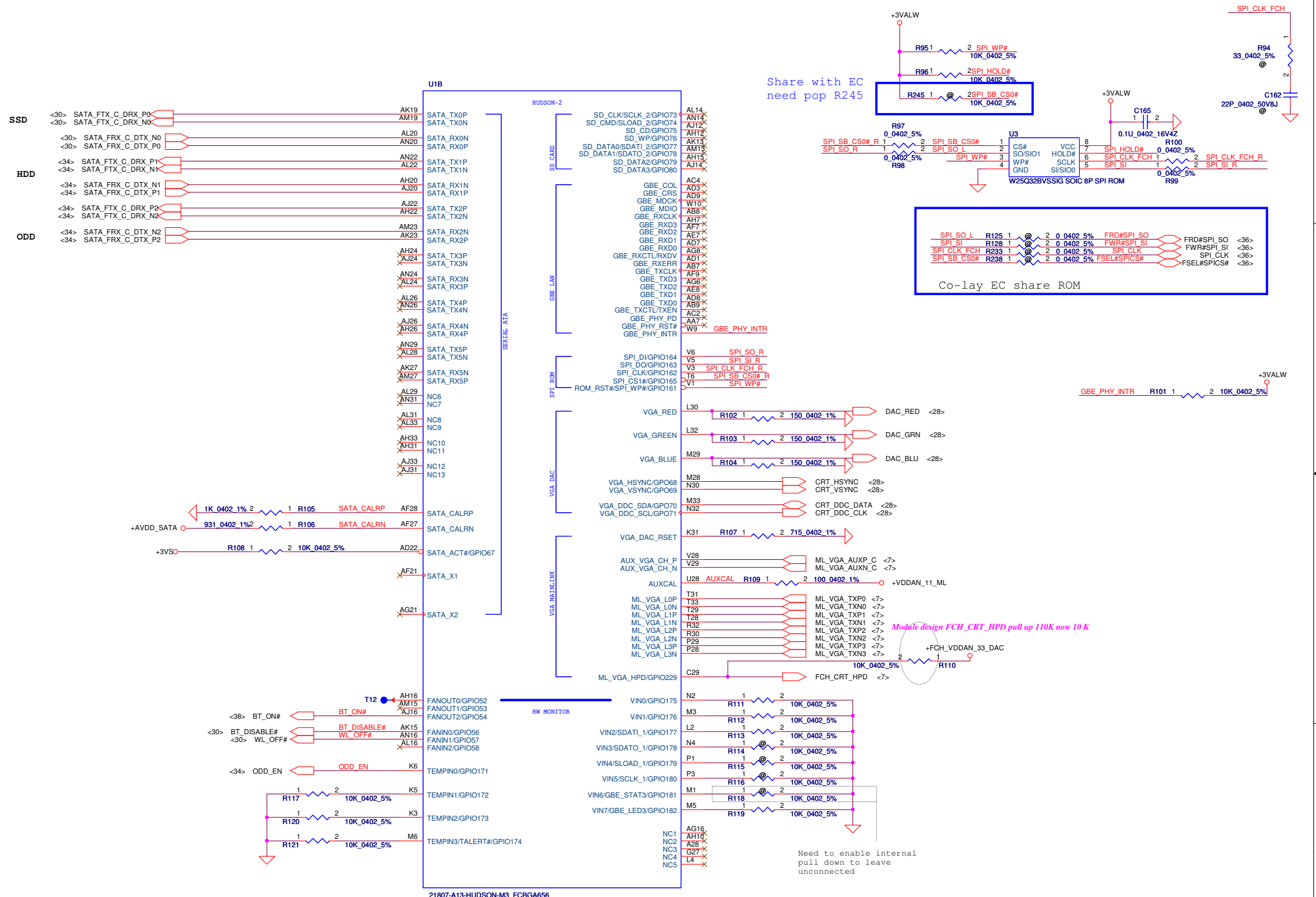


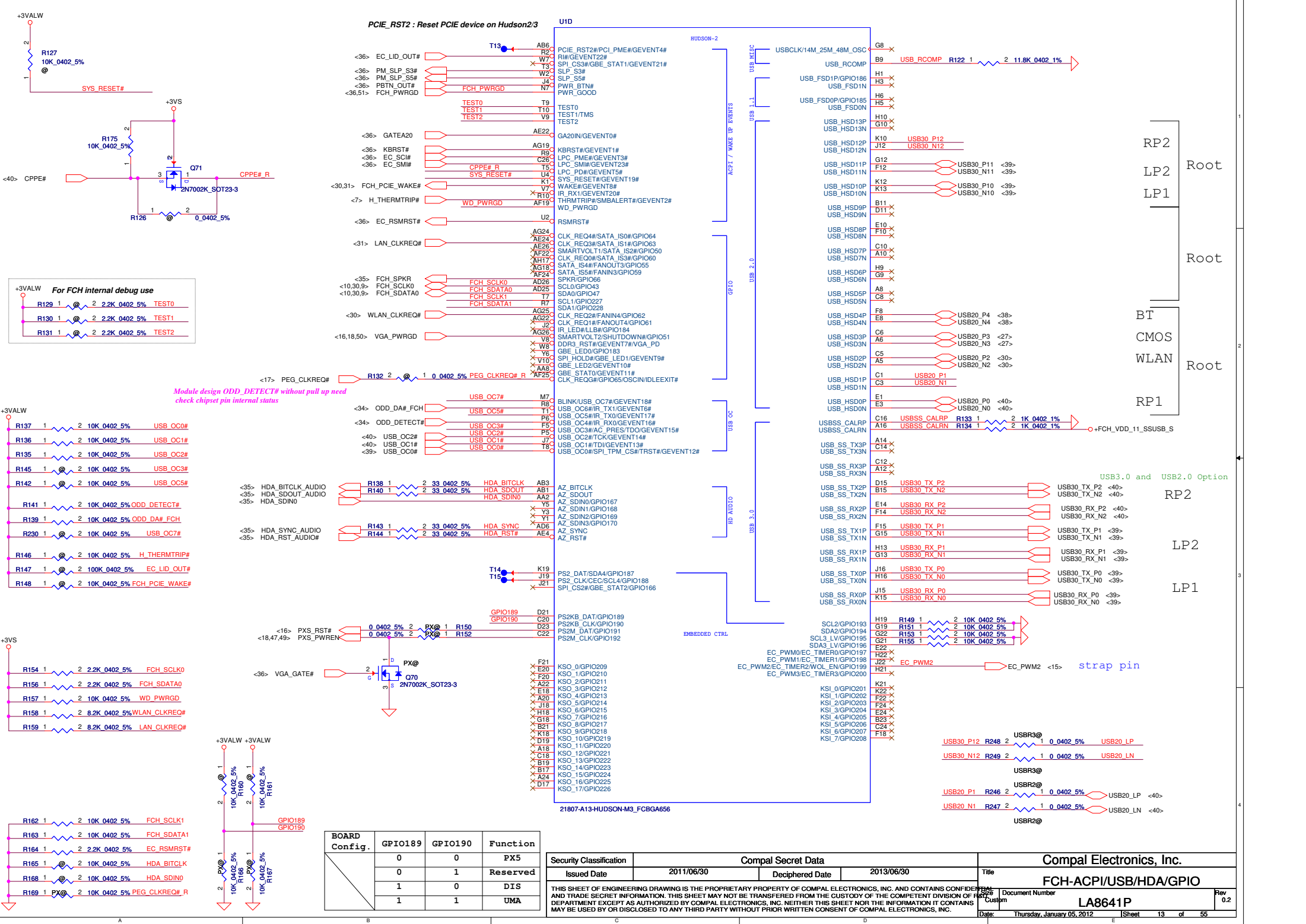
Standard H:4mm
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4MB SPI ROM





PCIE_RST2 : Reset PCIE device on Hudson2/3

UID

HUDSON-2

ACPI / MAKE UP EVENTS

GPIO

USB OC

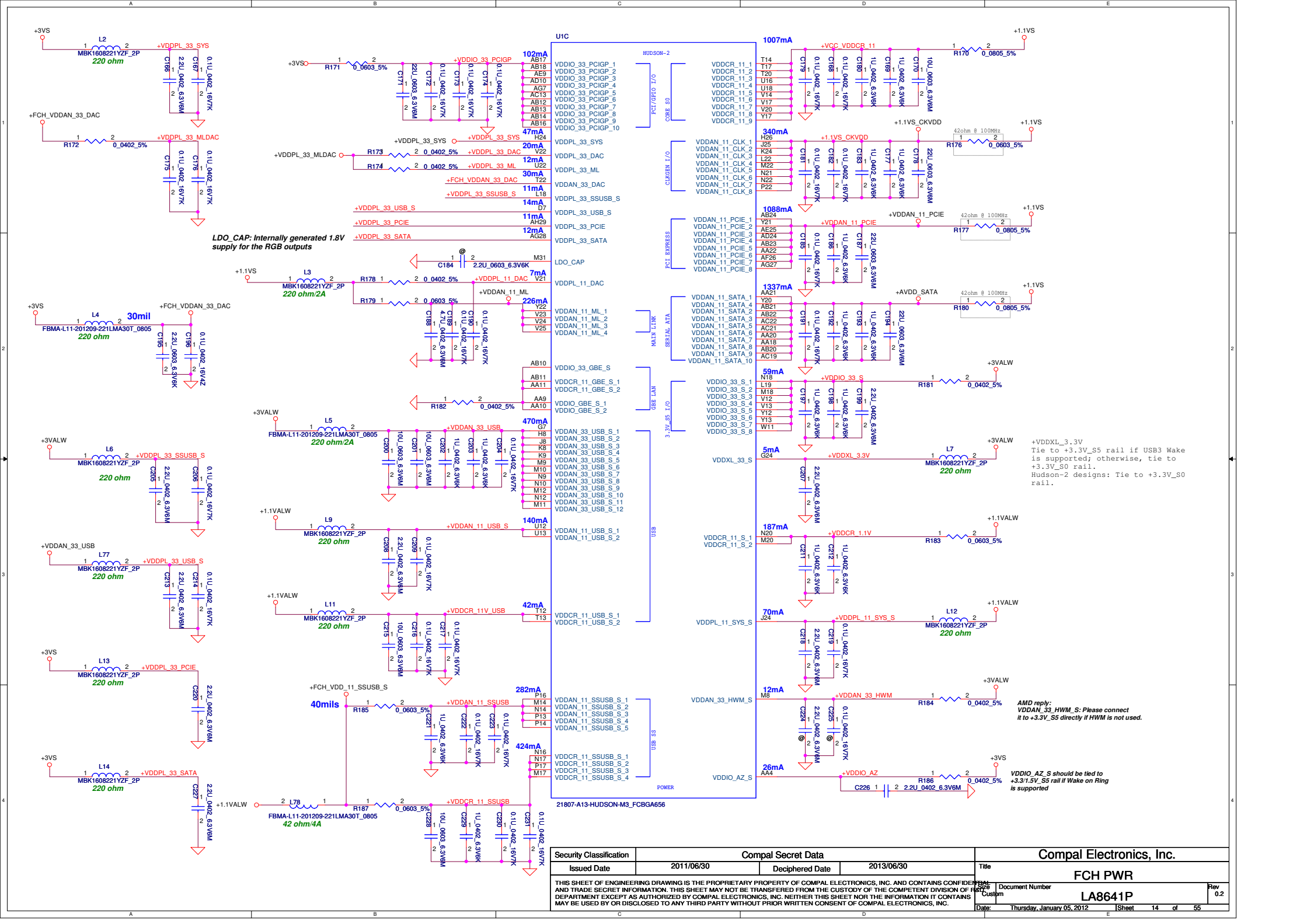
HDA AUDIO

EMBEDDED CTRL

BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX5
	0	1	Reserved
	1	0	DIS
	1	1	UMA

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FCH-ACPI/USB/HDA/GPIO				Document Number	Rev
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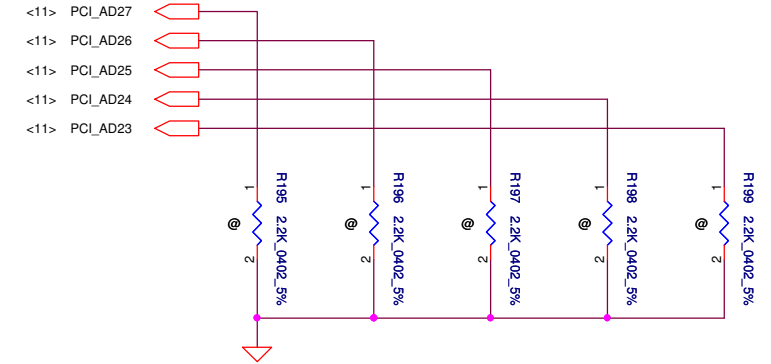
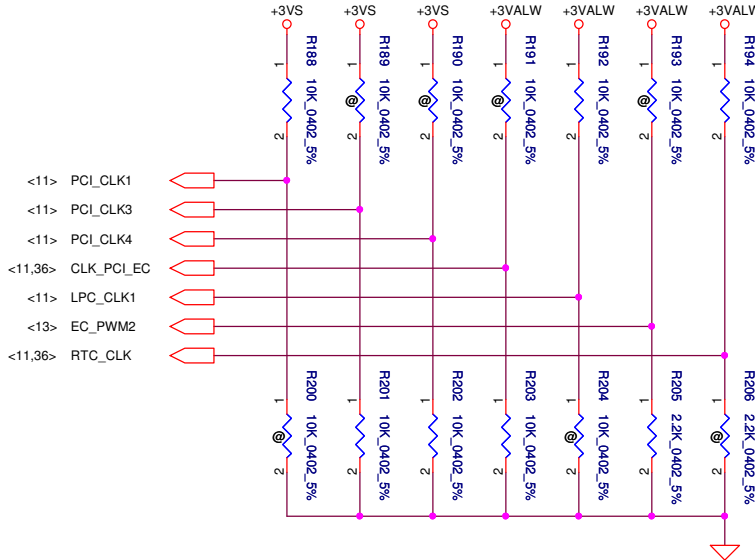
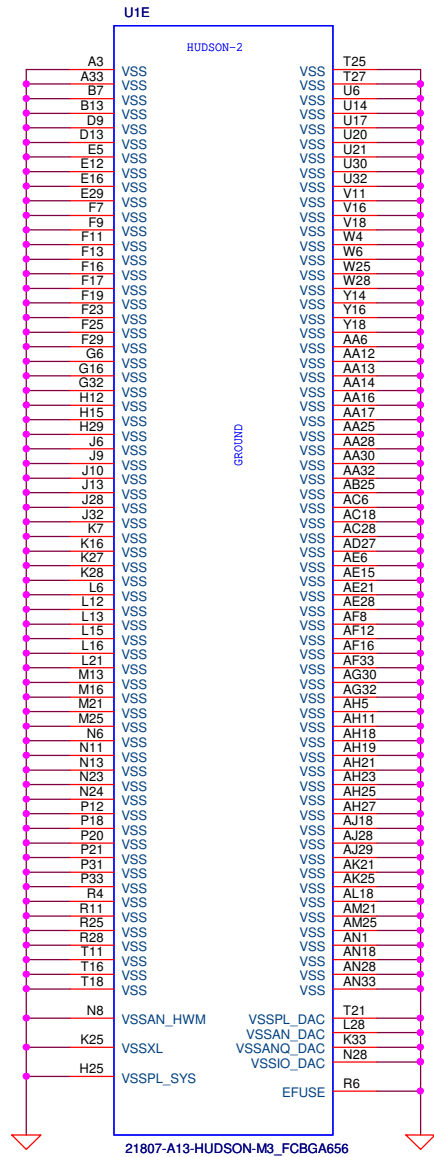
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

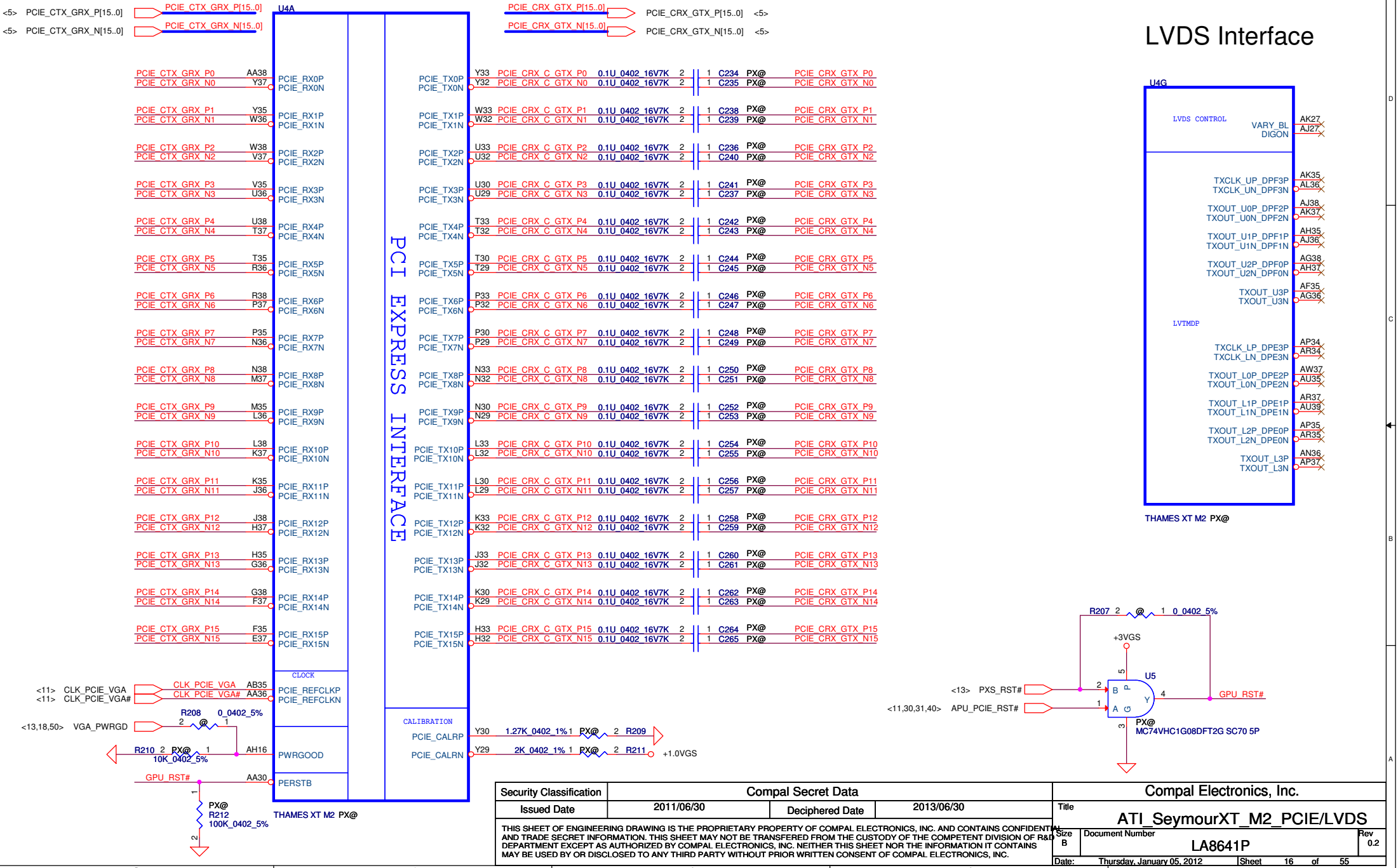
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



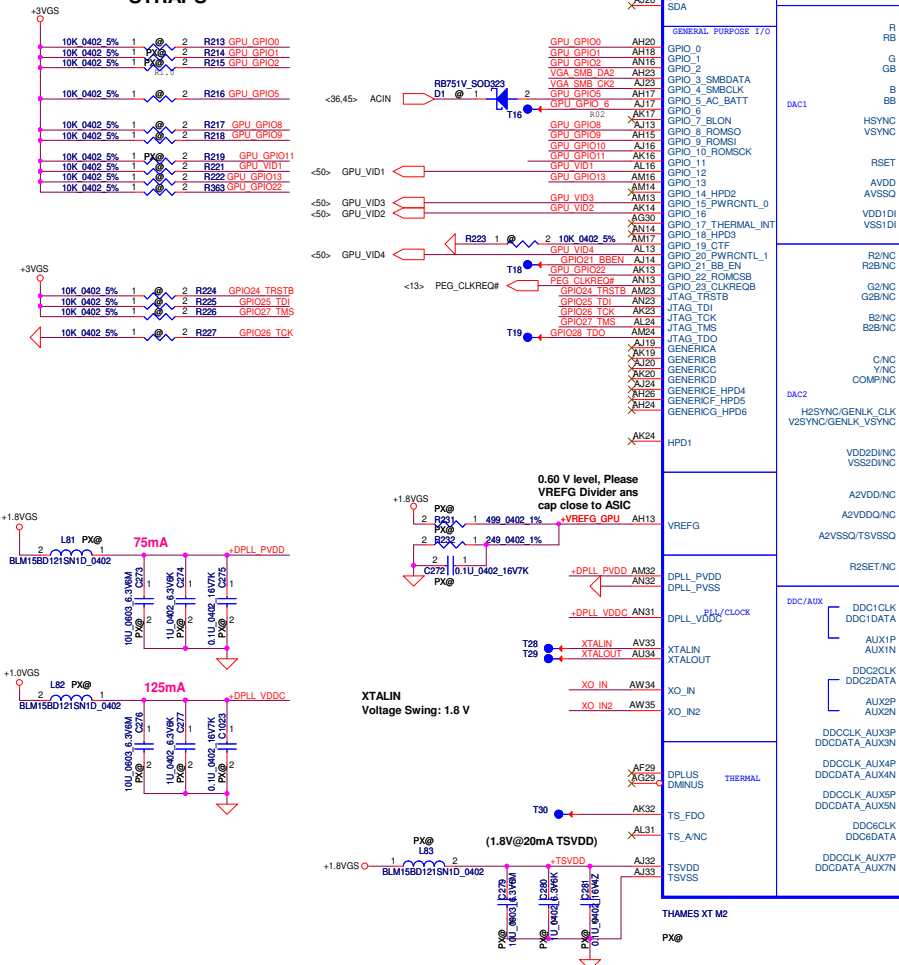
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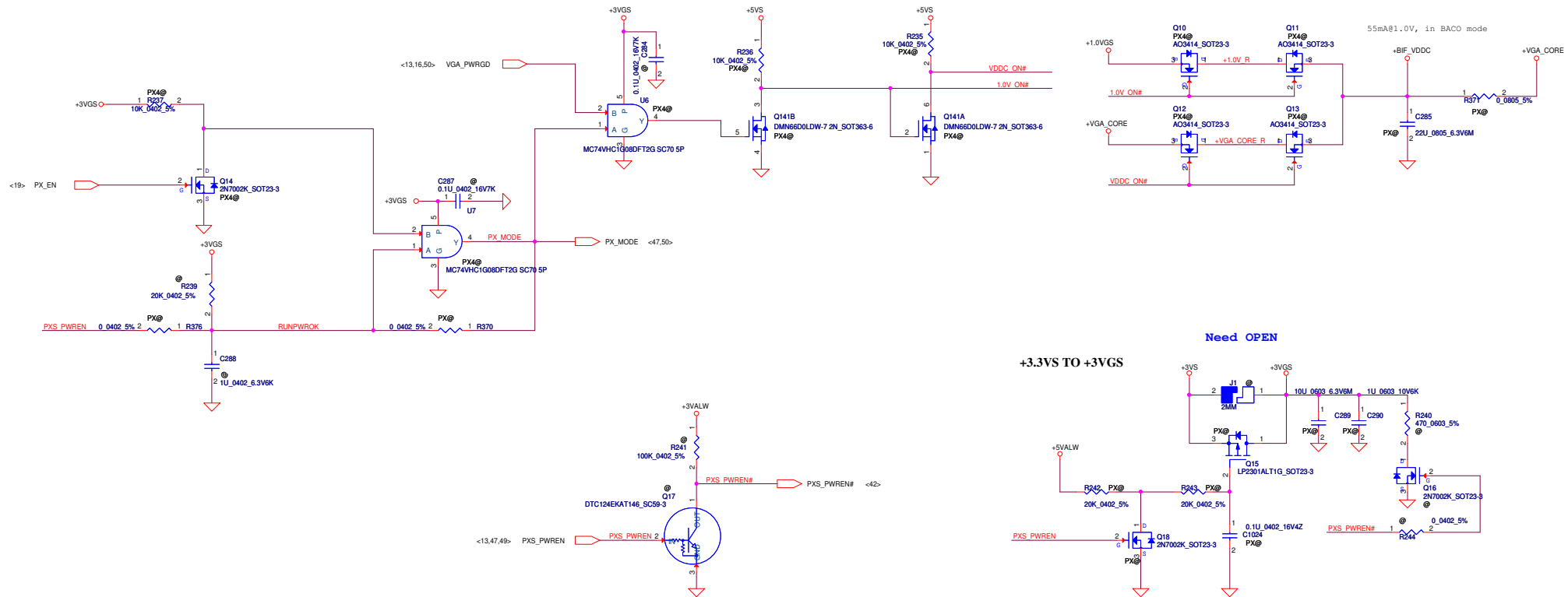


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CONFIGURATION STRAPS				RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X	
RSVD	GPIO2	Advertises PCIe speed when compliance test 0: 2.5Gt/s 1: 5Gt/s	0	
RSVD	GPIO8	RESERVED	0	
BIF_VGA_DIS	GPIO9	VGA ENABLED	0	
RSVD	GPIO21	RESERVED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX	
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0	
RSVD	H2SYNC		0	
RSVD	GENERICC		0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11	
AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET				
GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

STRAPS





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VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

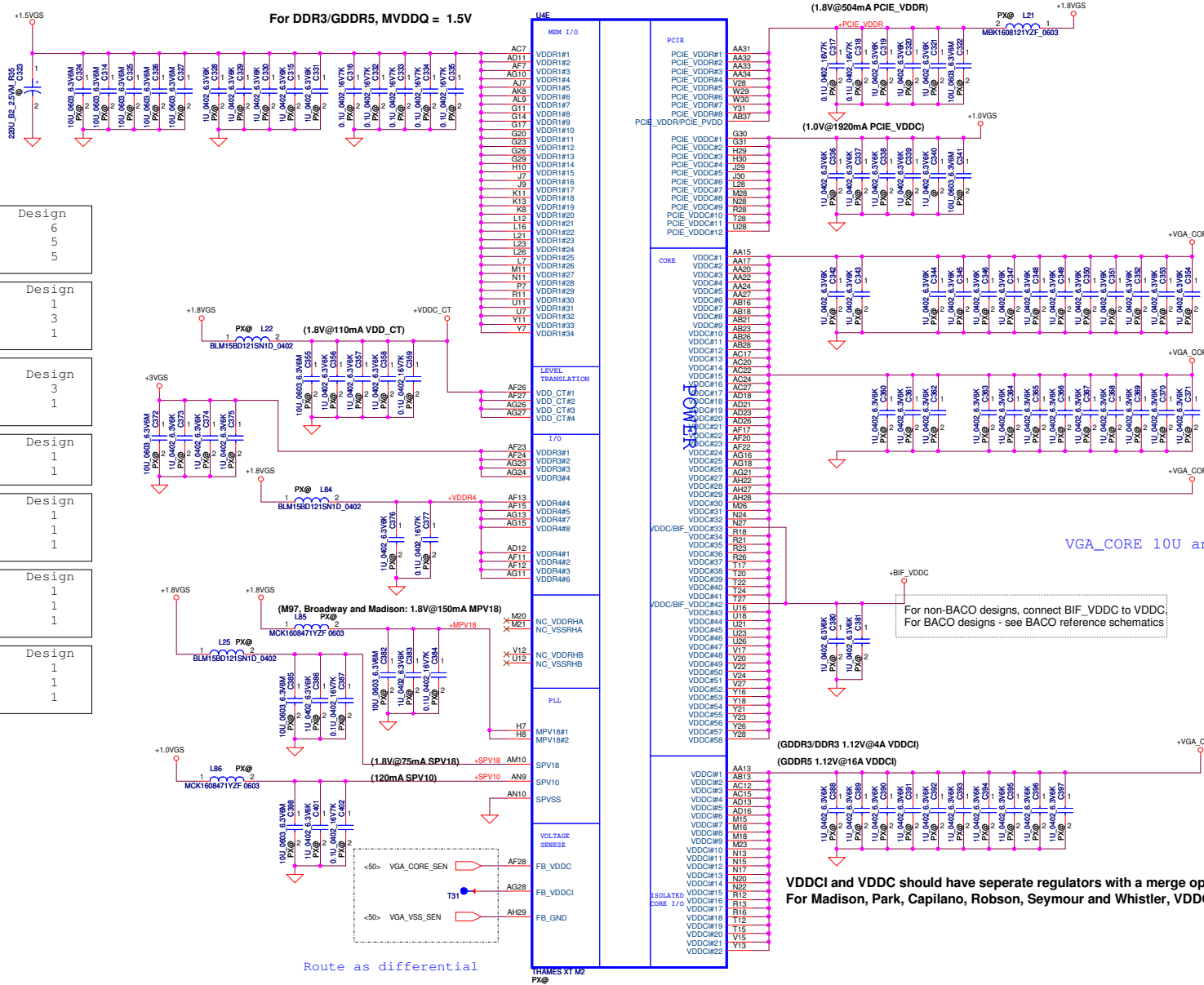
VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1



PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

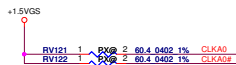
VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VGA_CORE 10U and 22U Cap in power side sheet

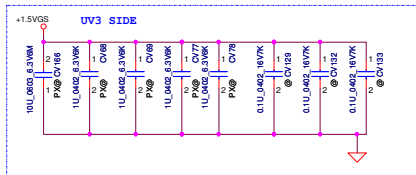
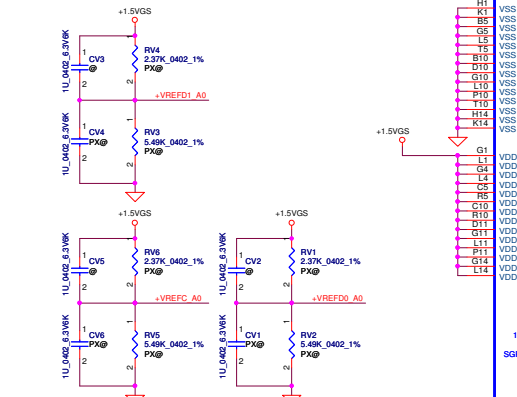
For non-BACO designs, connect BIF_VDDC to VDDC.
For BACO designs - see BACO reference schematics

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

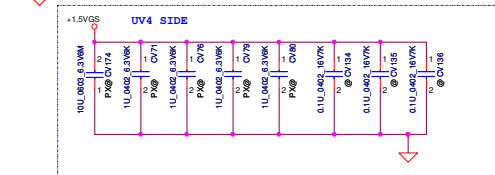
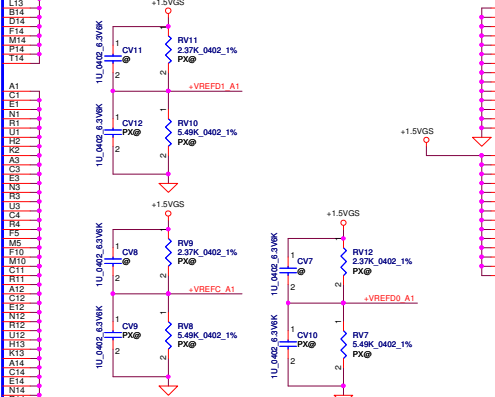
VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

$MF=0$ 

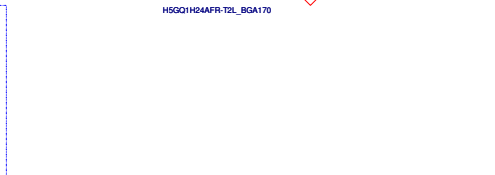
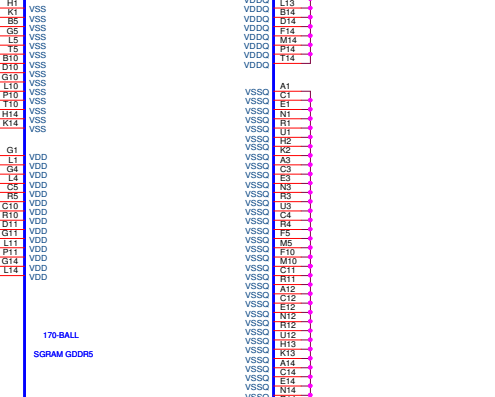
Close UV3,U4



M10	DQA0_20
M11	DQA0_16
M13	DQA0_23

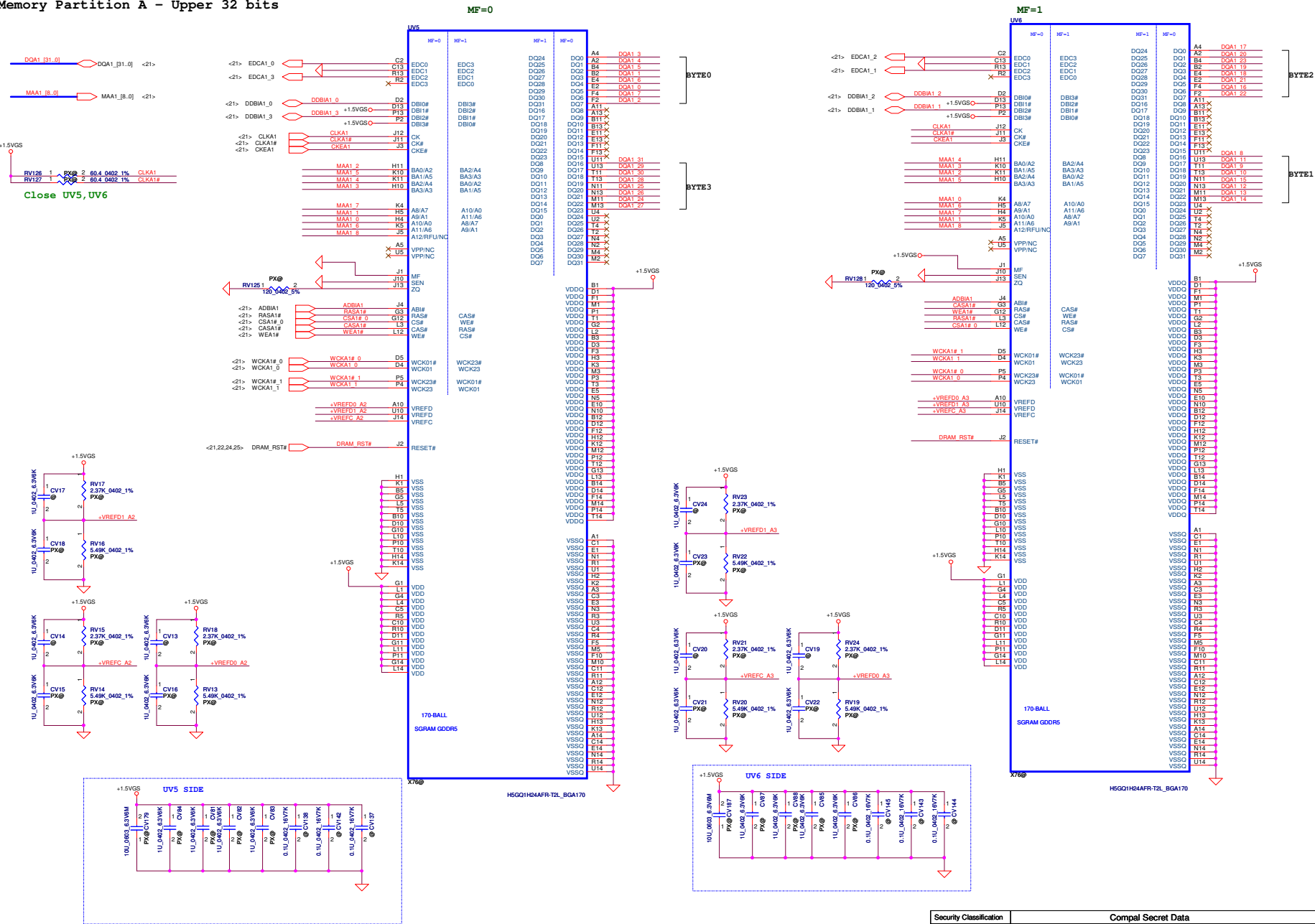


K4



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				LA8641P		
				Size	Document Number	Rev
Date: Thursday, January 05, 2012				15ppt	22	of 58

Memory Partition A - Upper 32 bits

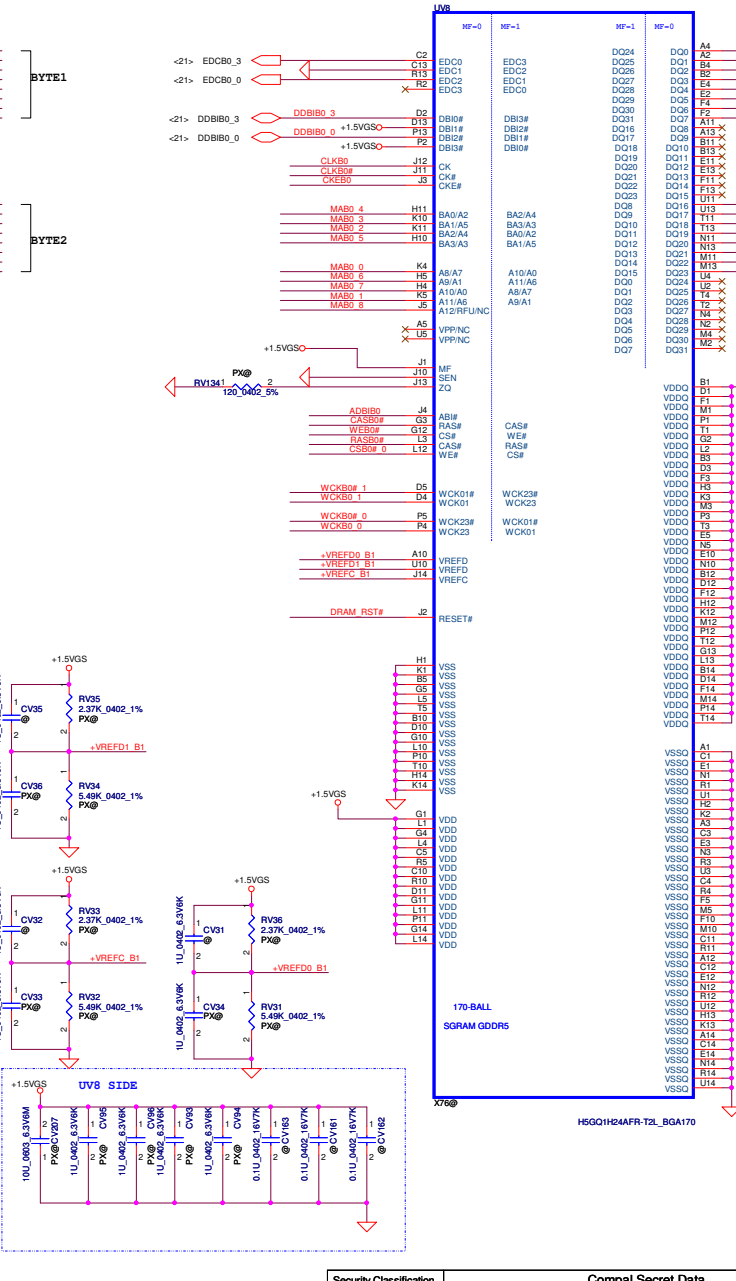
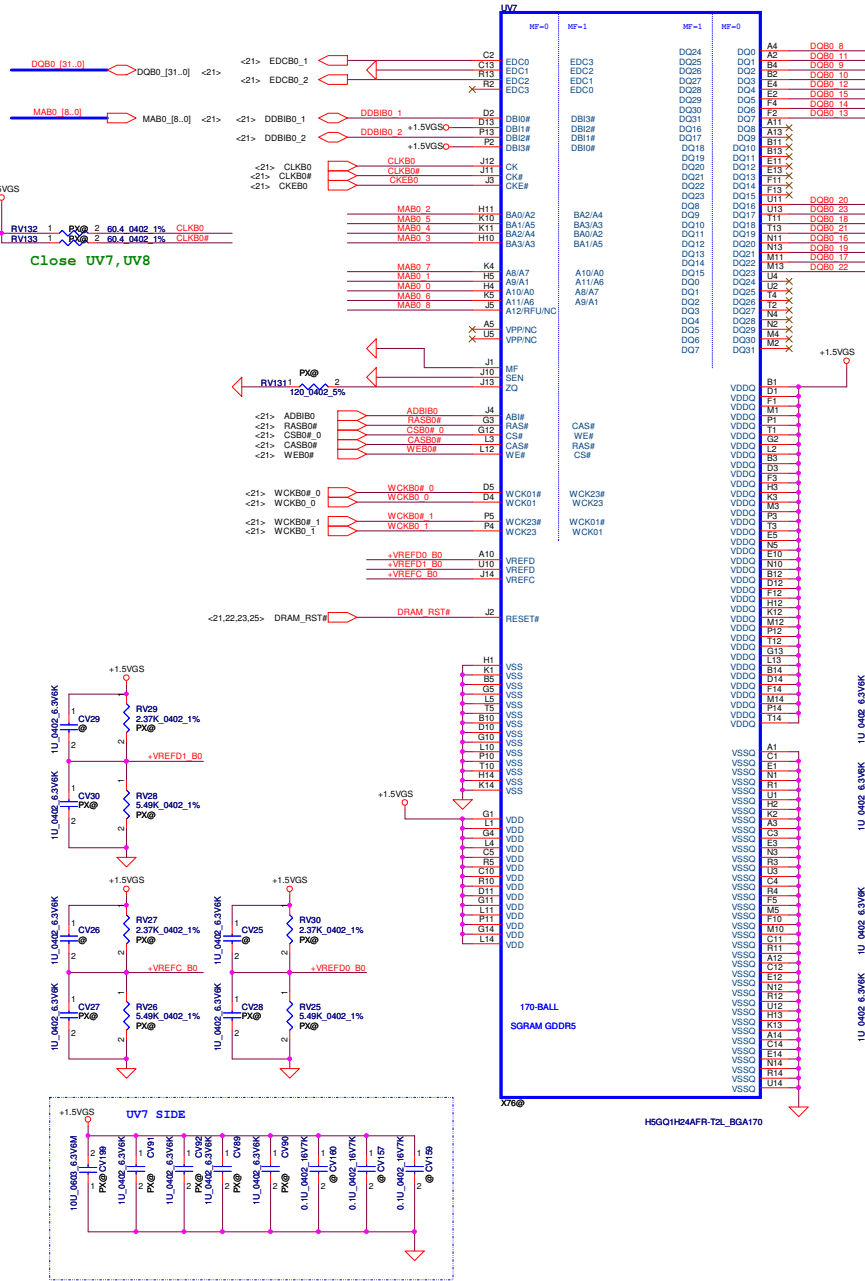


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Size	Document Number	LA8641P			Rev 0.2
Date	Thursday, January 05, 2012	Sheet	29	of	56

Memory Partition C - Lower 32 bits

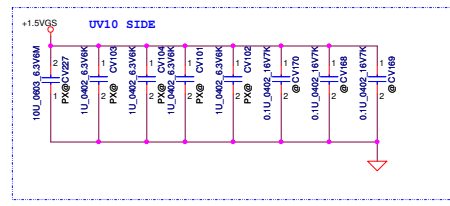
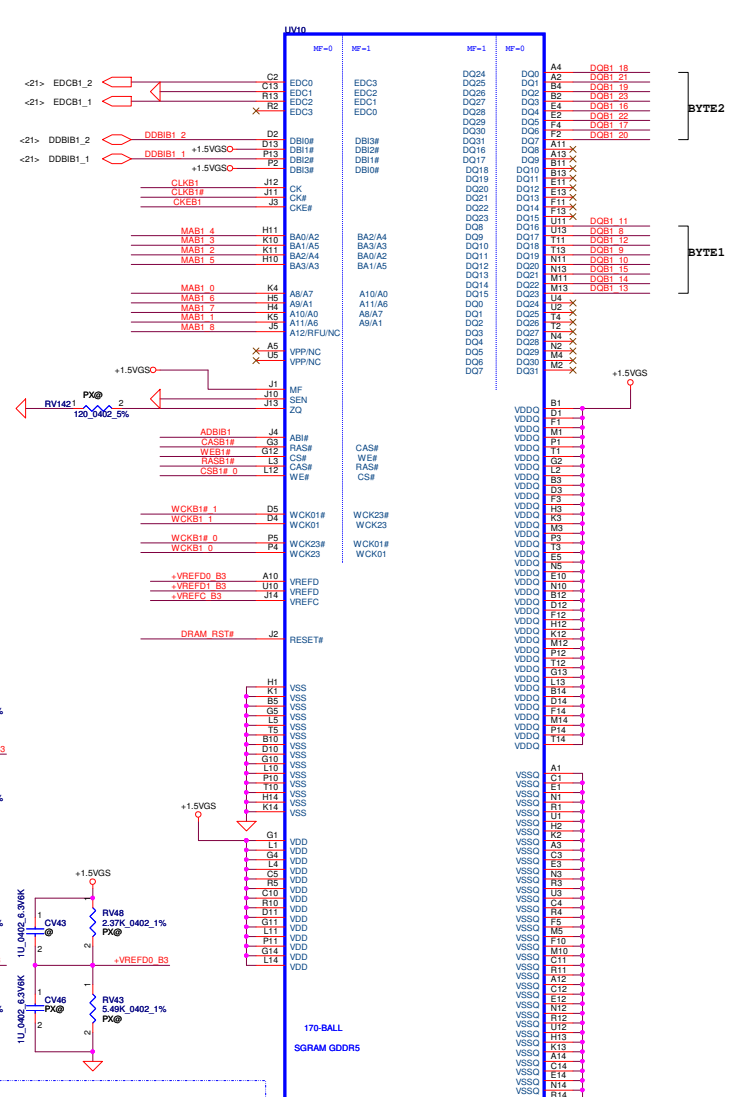
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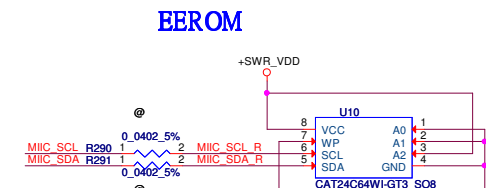
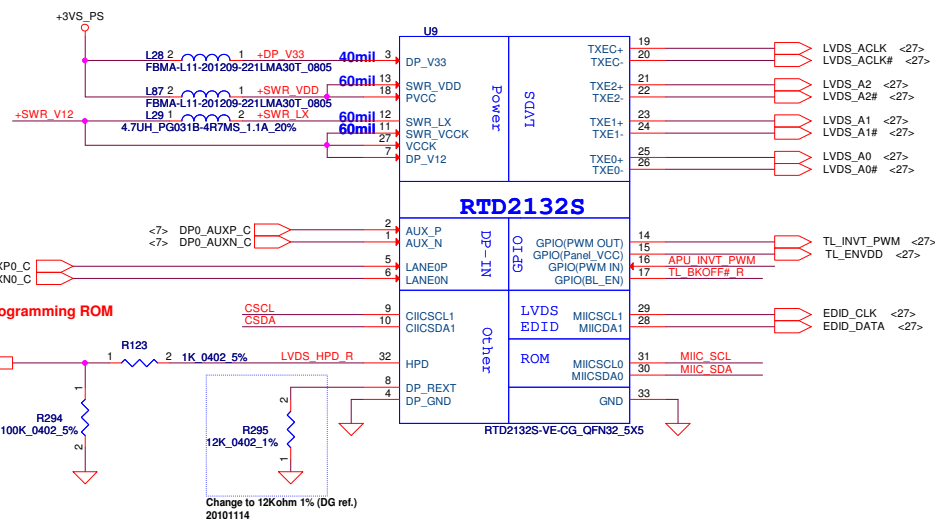
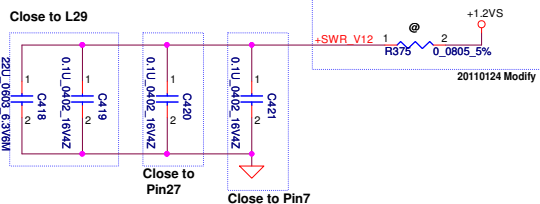


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		LA8641P		0.2	
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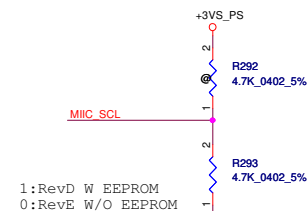
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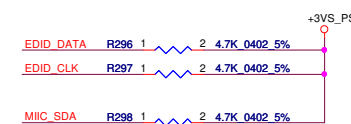
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Issued Date	2011/07/21	Deciphered Date	2012/12/31		
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			Date:	Thursday, January 05, 2012	Sheet 25 of 55



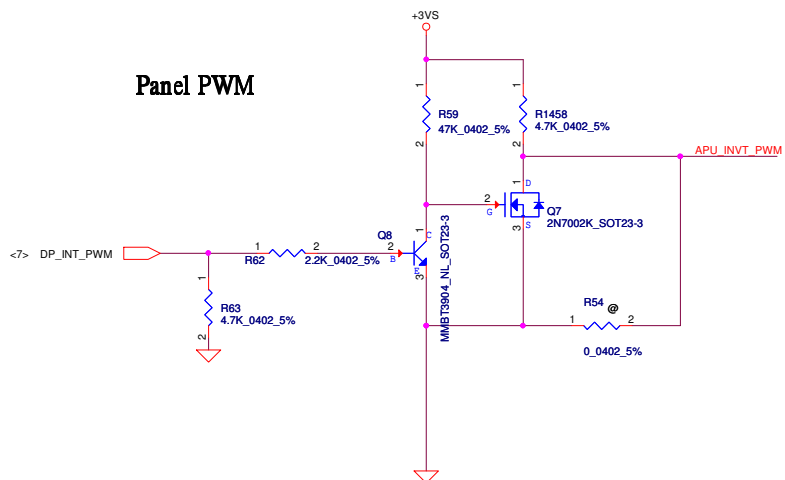
A phase pop EEPROM ,without 0 ohm



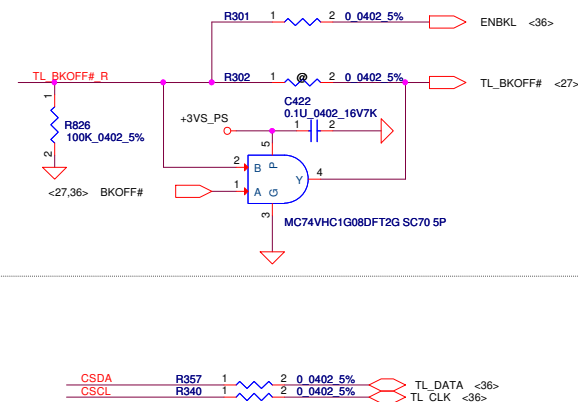
EDID DATA R296 1 2 4.7K 0402 5%

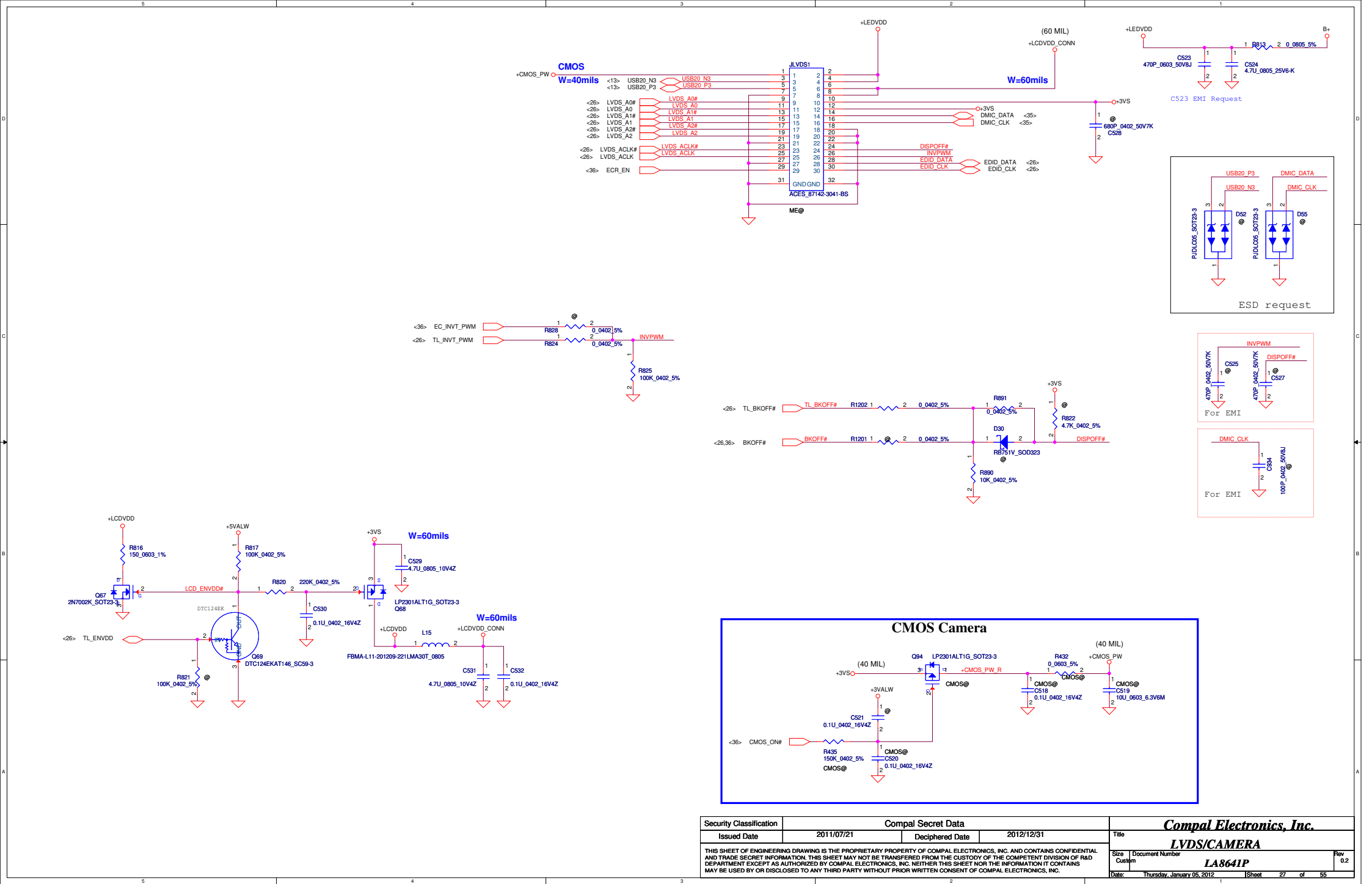


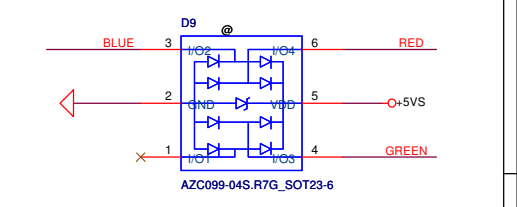
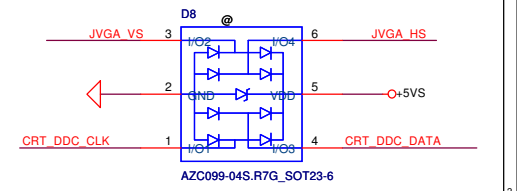
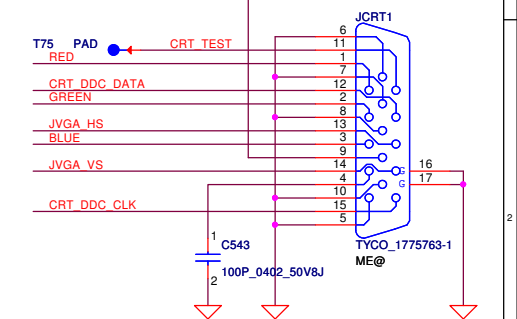
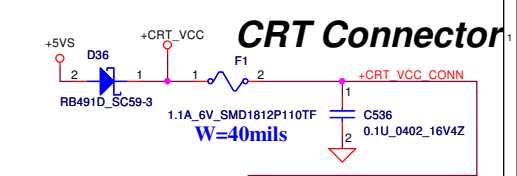
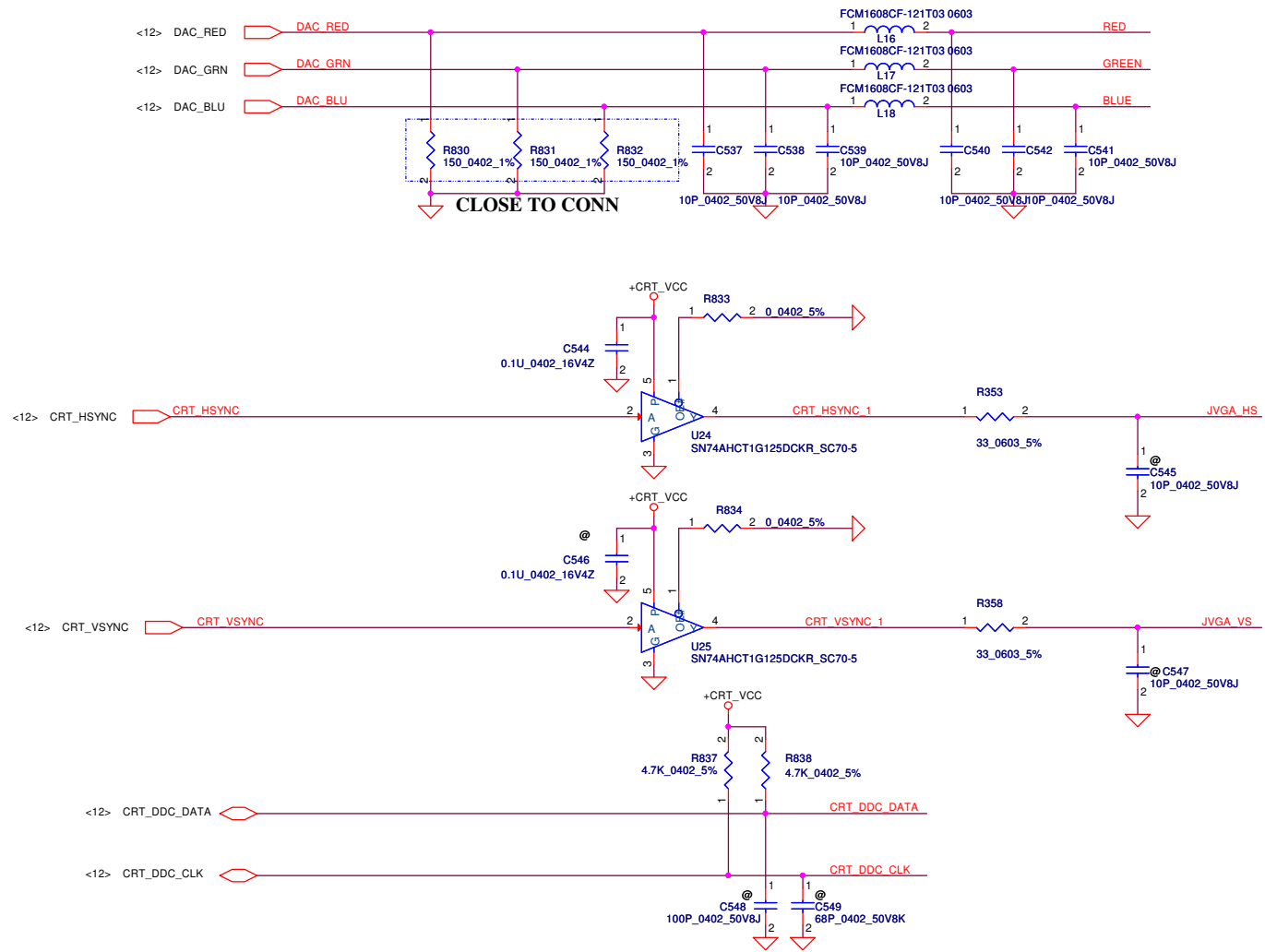
Panel PWM



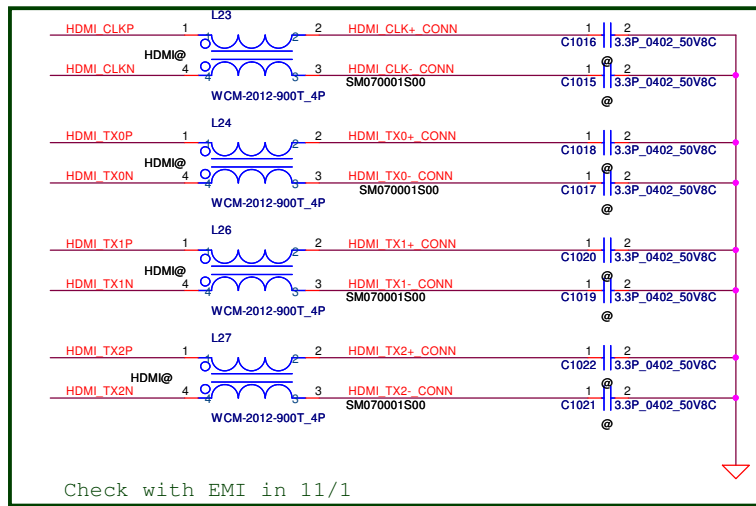
Vendor advise reserve it



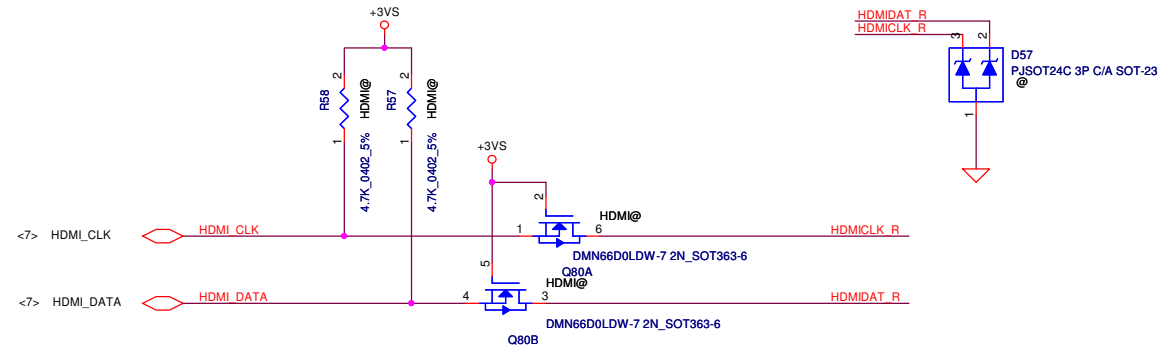




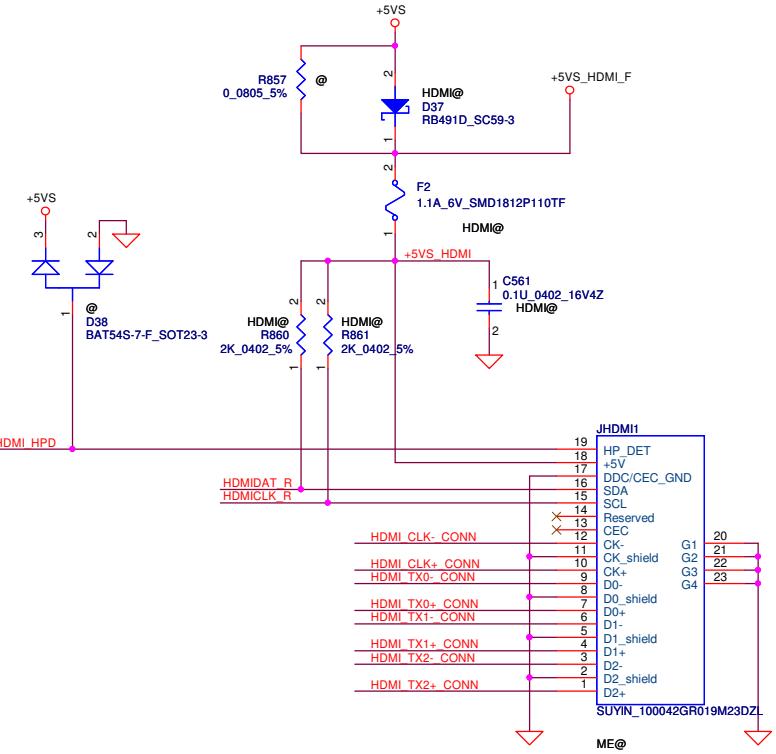
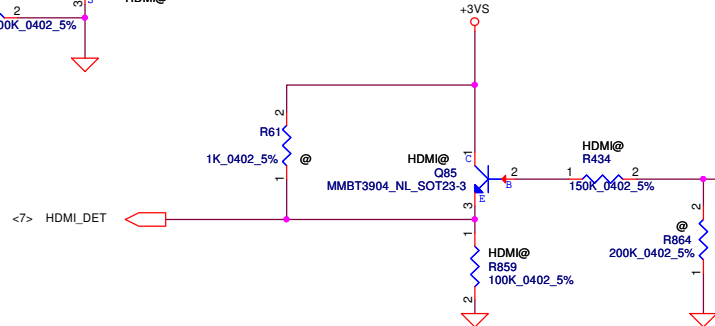
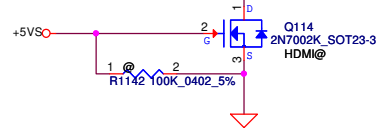
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<7>	HDMI_CLKP	R865	1	2	0	0402	5%	HDMI_CLK+ CONN
<7>	HDMI_CLKN	R866	1	2	0	0402	5%	HDMI_CLK- CONN
<7>	HDMI_TX0P	R867	1	2	0	0402	5%	HDMI_TX0+ CONN
<7>	HDMI_TX0N	R868	1	2	0	0402	5%	HDMI_TX0- CONN
<7>	HDMI_TX1P	R869	1	2	0	0402	5%	HDMI_TX1+ CONN
<7>	HDMI_TX1N	R870	1	2	0	0402	5%	HDMI_TX1- CONN
<7>	HDMI_TX2P	R871	1	2	0	0402	5%	HDMI_TX2+ CONN
<7>	HDMI_TX2N	R872	1	2	0	0402	5%	HDMI_TX2- CONN

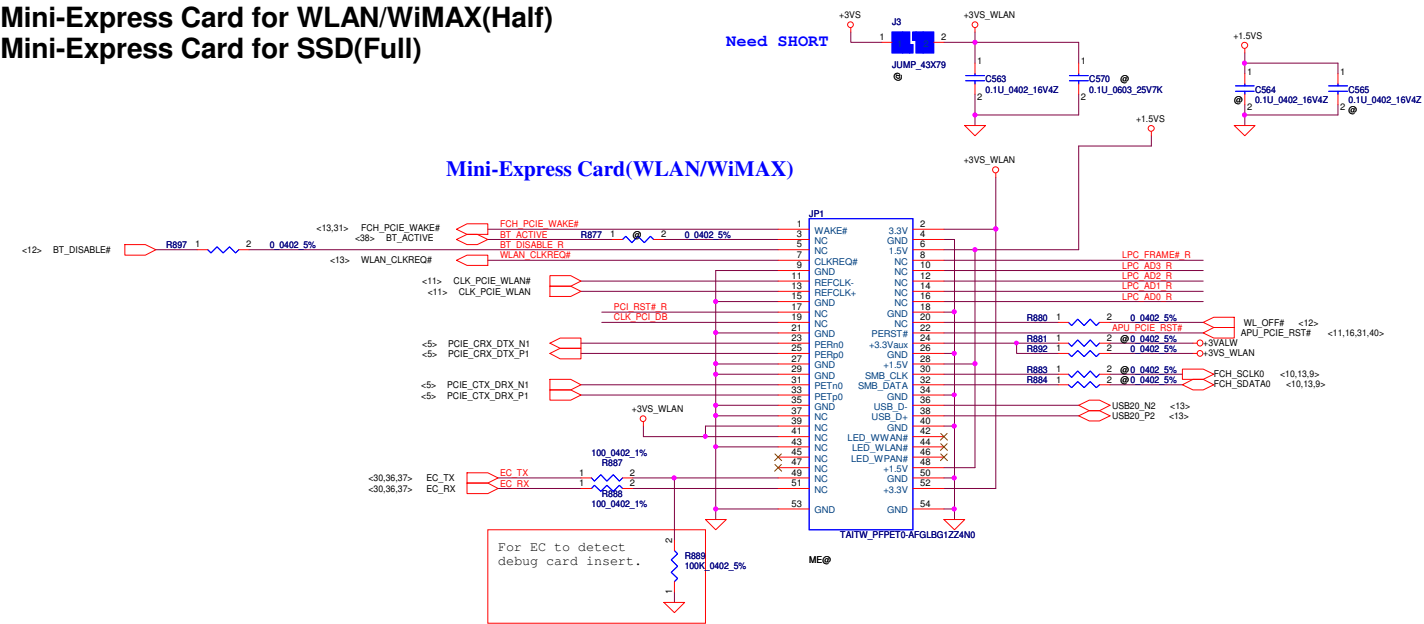


HDMI_CLK- CONN	R882	1	HDMI@	2	604	0402	1%
HDMI_CLK+ CONN	R885	1	HDMI@	2	604	0402	1%
HDMI_TX1- CONN	R886	1	HDMI@	2	604	0402	1%
HDMI_TX1+ CONN	R895	1	HDMI@	2	604	0402	1%
HDMI_TX0- CONN	R898	1	HDMI@	2	604	0402	1%
HDMI_TX0+ CONN	R899	1	HDMI@	2	604	0402	1%
HDMI_TX2- CONN	R900	1	HDMI@	2	604	0402	1%
HDMI_TX2+ CONN	R901	1	HDMI@	2	604	0402	1%



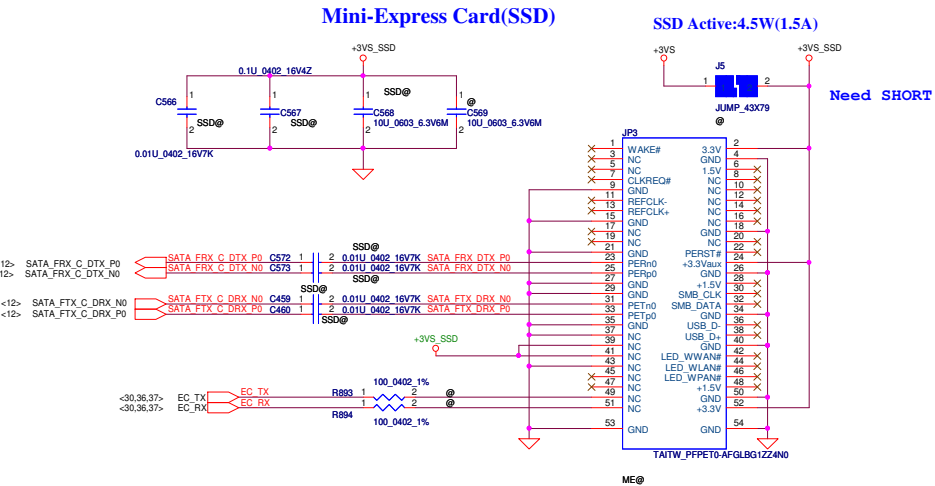
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Issued Date	2011/07/21	Deciphered Date	2012/12/31	HDMI CONN	
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				Date	Thurs, January 05, 2012
				Sheet	29 of 55

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R873	1	2	0.0402_5%	LPC_FRAME#	LPC_FRAME#	<11,36>
LPC_AD3_R	R874	1	2	0.0402_5%	LPC_AD3	LPC_AD3	<11,36>
LPC_AD2_R	R875	1	2	0.0402_5%	LPC_AD2	LPC_AD2	<11,36>
LPC_AD1_R	R876	1	2	0.0402_5%	LPC_AD1	LPC_AD1	<11,36>
LPC_AD0_R	R877	1	2	0.0402_5%	LPC_AD0	LPC_AD0	<11,36>
LPC_RST#_R	R878	1	2	0.0402_5%	APU_PCIE_RST#	CLK_PCIE_DB	<11>
CLK_PCIE_DB	R879	1	2	0.0402_5%			



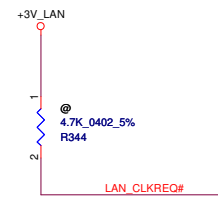
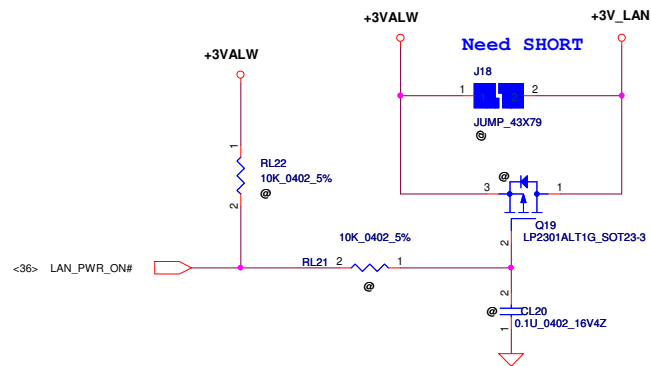
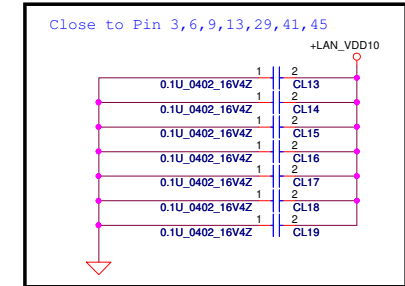
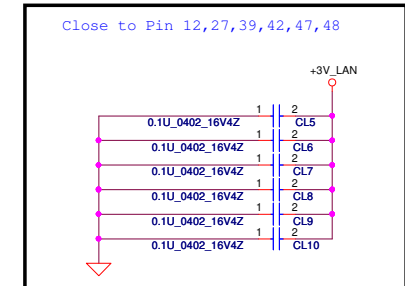
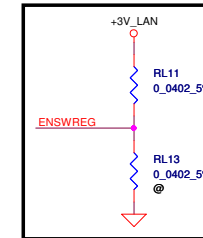
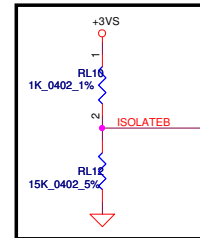
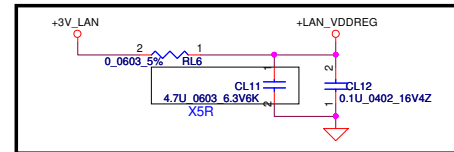
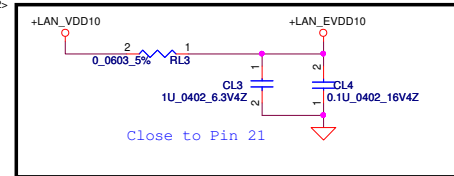
U63 8111E@

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 SA00004LR00

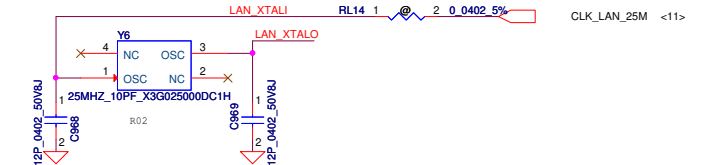


Layout Note: L39 must be within 20mm to Pin36, C700, C738 must be within 20mm to L11

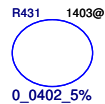
+LAN_REGOUT: Width =60mm



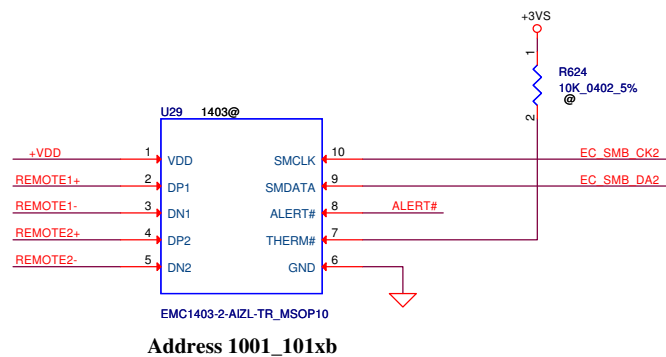
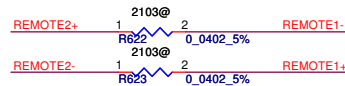
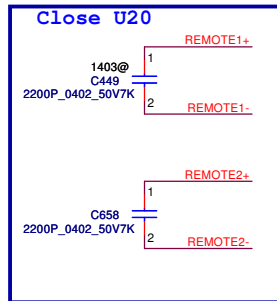
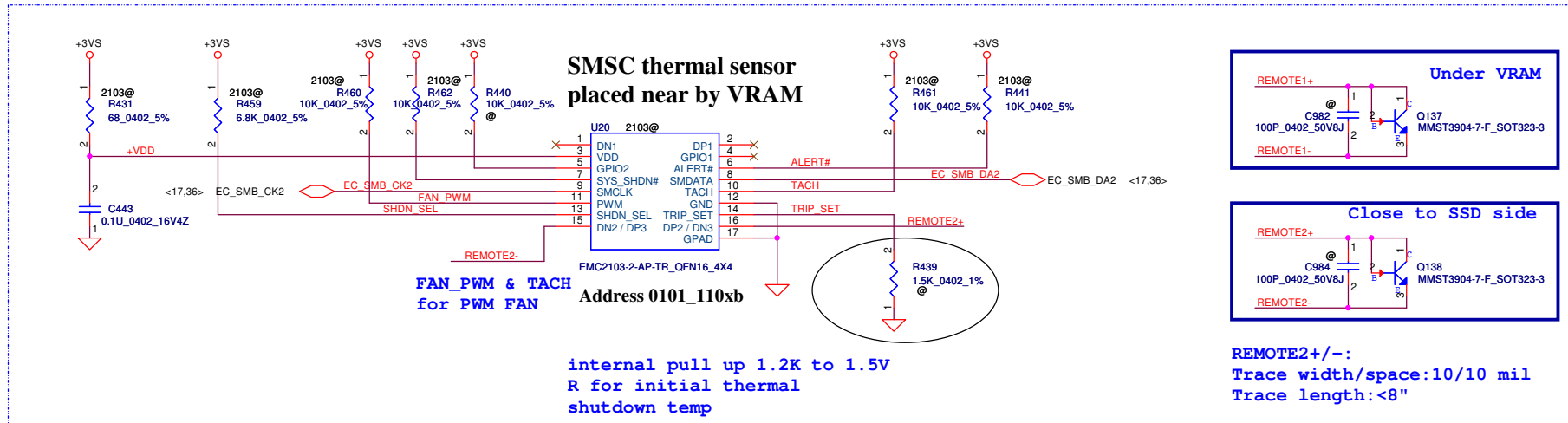
Vendor recommend resew the
PU resistor close LAN chip



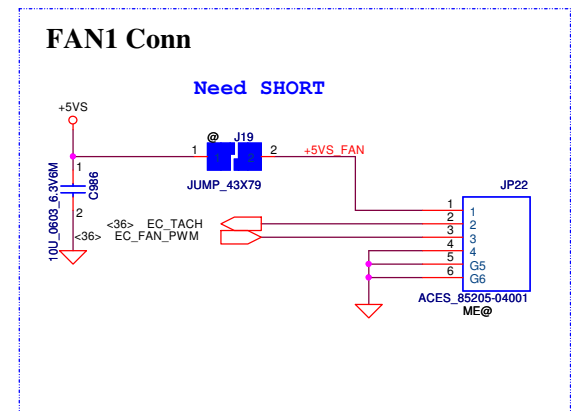
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1403:
@C982/@C984=100p



Shutdown Temp	TRIP_SET R1387 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm



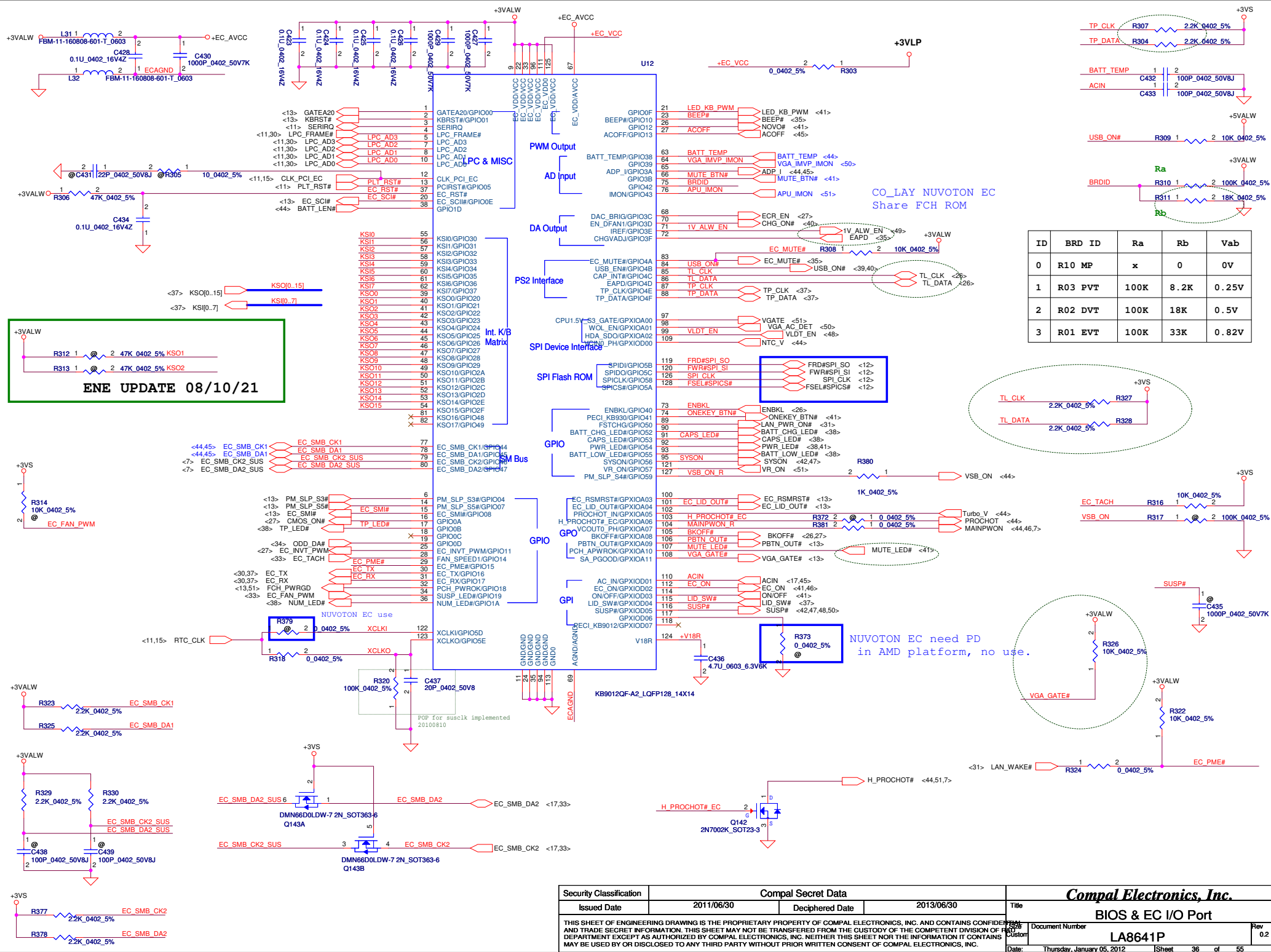
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Size	Custom	Document Number	LA8641P	Rev	0.2
Date	Thursday, January 05, 2012	Sheet	33	of	55

The diagram illustrates the SATA controller connections for the H340 board. It shows the connection of the SATA_FTX_C_DRX_P1, SATA_FTX_C_DRX_N1, SATA_FRX_C_DTX_N1, and SATA_FRX_C_DTX_P1 pins to the SATA_FTX_C_DRX_P1, SATA_FTX_C_DRX_N1, SATA_FRX_C_DTX_N1, and SATA_FRX_C_DTX_P1 pins of the H340. The diagram also shows the connection of the SATA_FTX_C_DRX_P1, SATA_FTX_C_DRX_N1, SATA_FRX_C_DTX_N1, and SATA_FRX_C_DTX_P1 pins to the SATA_FTX_C_DRX_P1, SATA_FTX_C_DRX_N1, SATA_FRX_C_DTX_N1, and SATA_FRX_C_DTX_P1 pins of the H340. The diagram includes a note "Need SHORT" and a warning "FOX_LD2822F-SAQ1.6".

SATA ODD Conn.

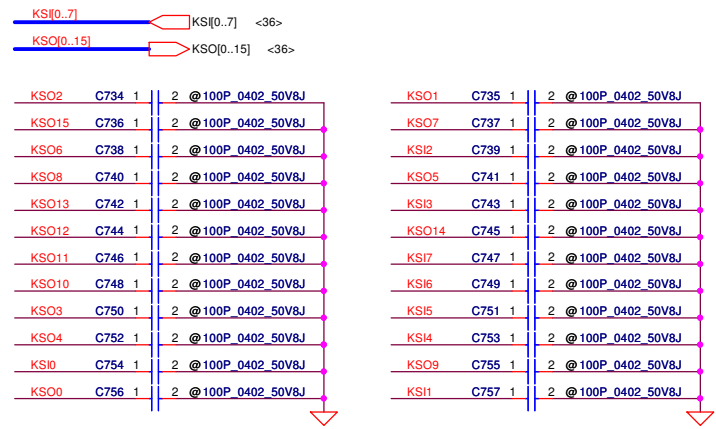
The diagram shows a 5V regulator circuit. The input is +5VALW, which passes through a resistor R923 (10K_0402_5%) to the input of the regulator. The regulator's output is +5V_S, which is connected to a jumper J6. The jumper J6 is labeled "Need OPEN". The output of the regulator is +5V_ODD, which is connected to a MOSFET Q89 (DTC124EKAT146_SC59-3). The MOSFET's gate is connected to the output of the regulator through a resistor R1110 (200K_0402_5%). The MOSFET's drain is connected to the output of the regulator through a resistor R1110 (200K_0402_5%). The MOSFET's source is connected to ground. The MOSFET's gate is also connected to the output of the regulator through a capacitor C638 (0.1U_0402_16V4Z). The MOSFET's drain is also connected to the output of the regulator through a capacitor C639 (10U_0603_6.3V6M). The MOSFET's source is also connected to the output of the regulator through a capacitor C637 (0.1U_0402_16V4Z).

Security Classification		Compal Secret Data		Compal Electronics, Inc. HDD/ODD Connector	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	
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Date: Thursday, January 05, 2012				Sheet 34 of 55	

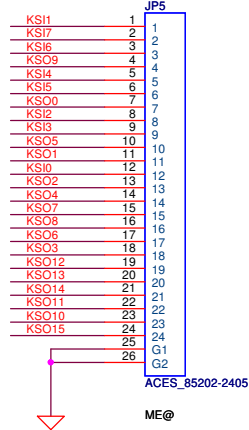


ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

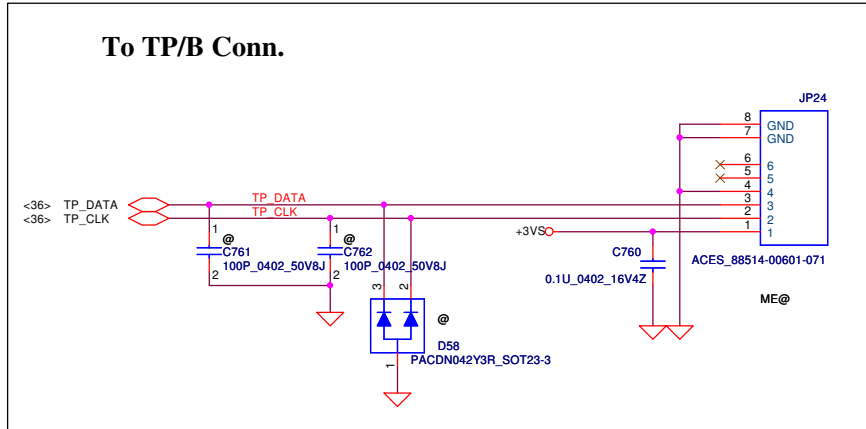
INT_KBD Conn.



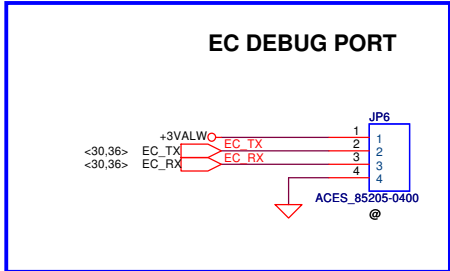
CONN PIN define need double check



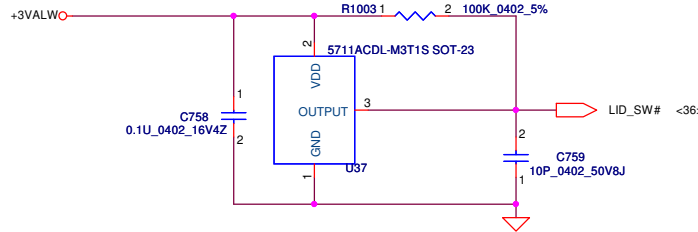
To TP/B Conn.



EC DEBUG PORT

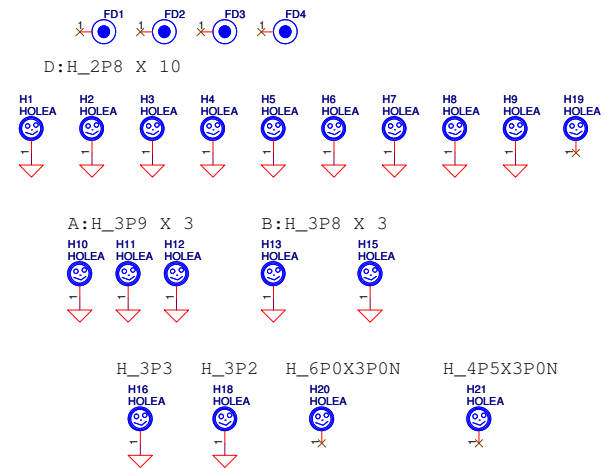
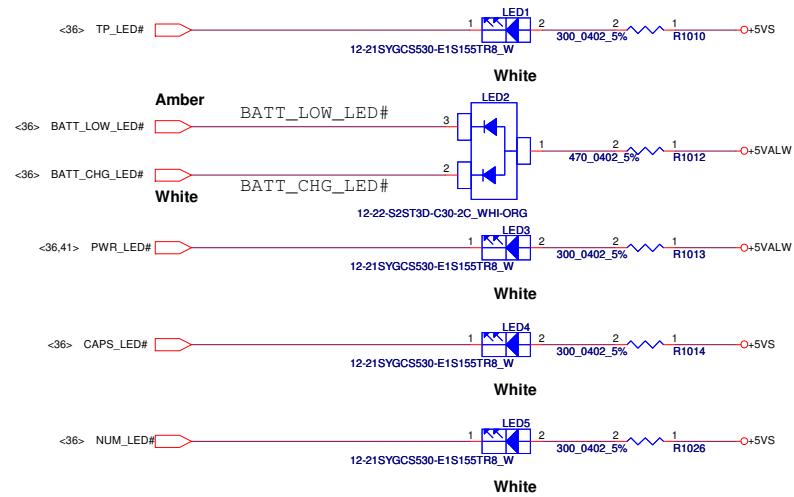


Lid Switch

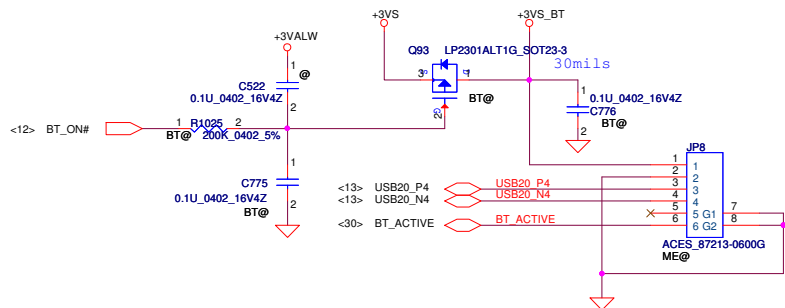


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2011/07/21				KB /SW /LPC Debug Conn.			
Deciphered Date				2012/12/31				LA8641P			
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LED

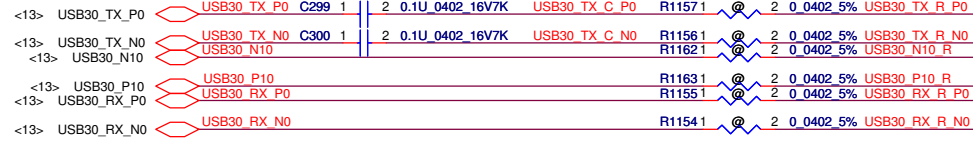
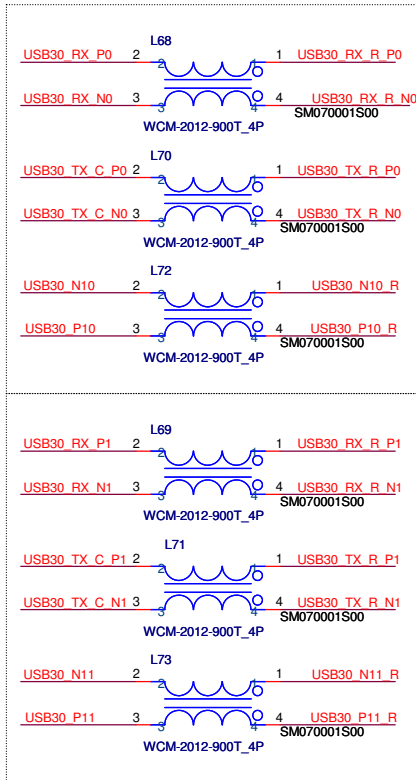
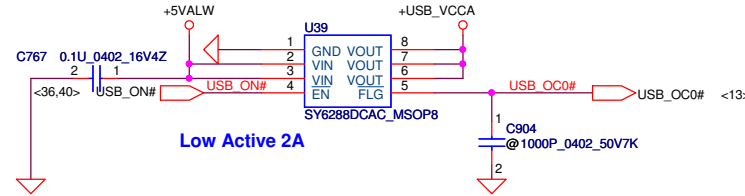


BT MODULE CONN

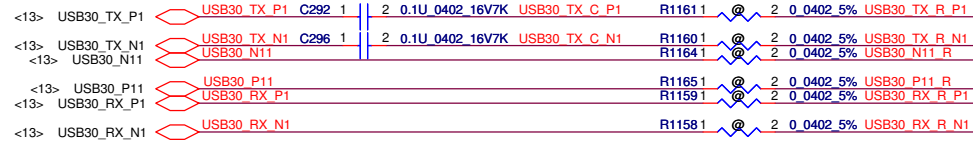
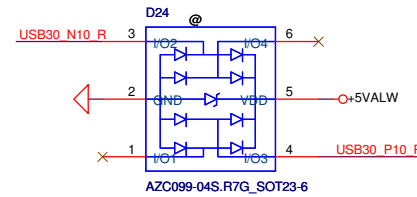
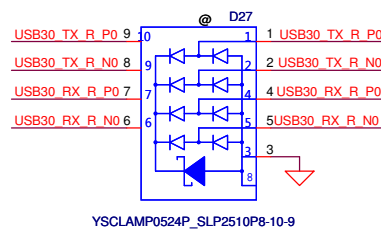


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	LED/EC SPI ROM/BT
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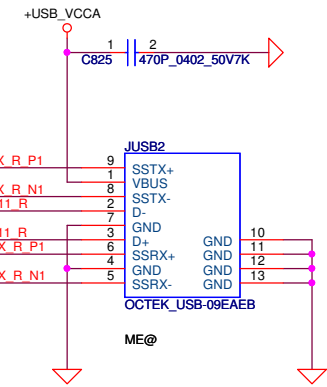
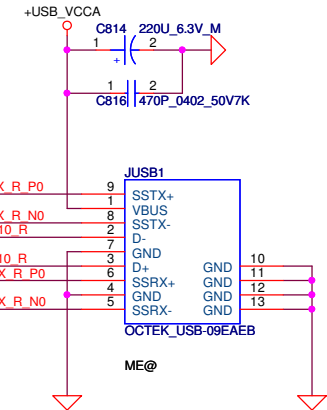
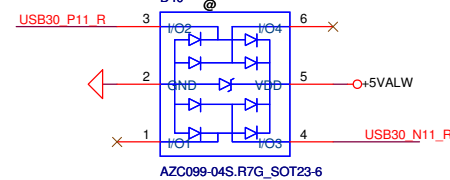
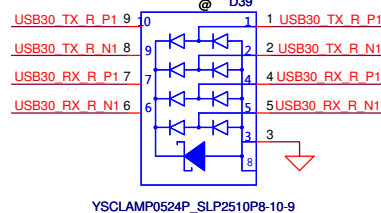
LEFT SIDE USB3.0 PORT X2



For ESD request



For ESD request



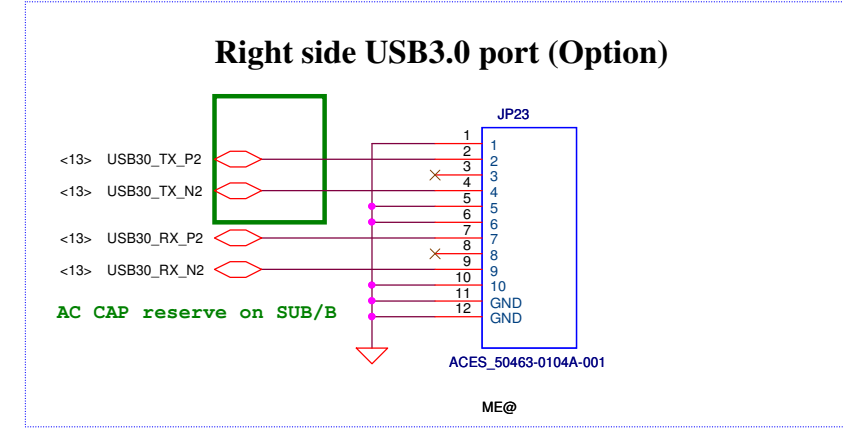
Security Classification		Compal Secret Data For EMI request		Compal Electronics, Inc.	
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title	USB3.0 ports
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Low Active 2A

Support Charge should use another pin for Power switch control

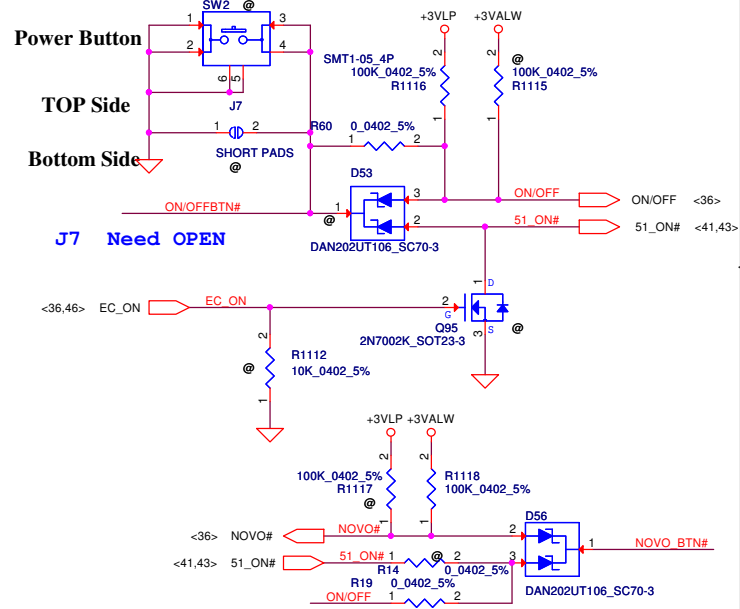
CB	Function
L	auto detection charger identification active
H	DP/DM=TDP/TDM

USB2.0/3.0 choke and ESD diode at sub-B.



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title Audio B Conn/USB charger			
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				Custom	LA8641P	0.2	
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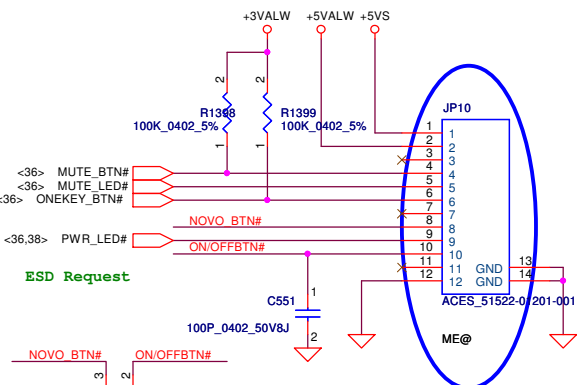
Power Button



```
<36> MUTE_BTN#
<36> MUTE_LED#
<36> ONEKEY_BTN#

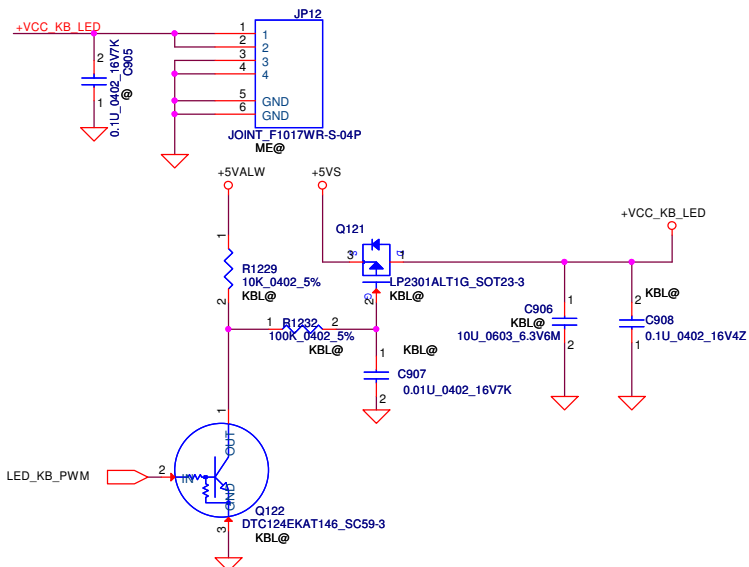
<36,38> PWR_LED#

ESD Request
```

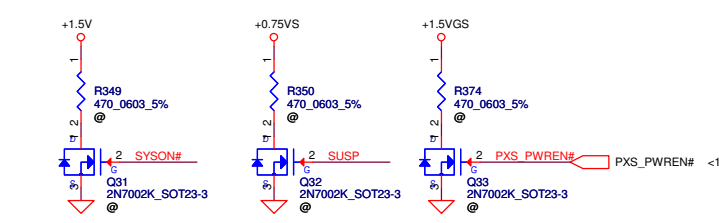
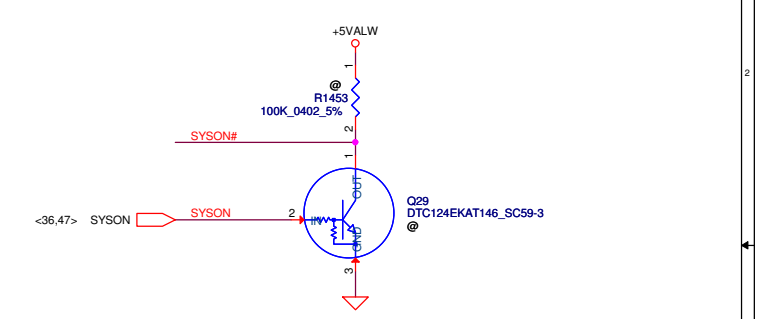
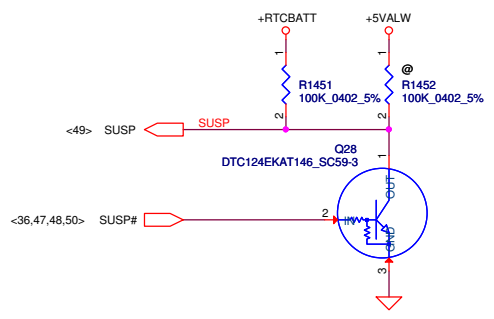
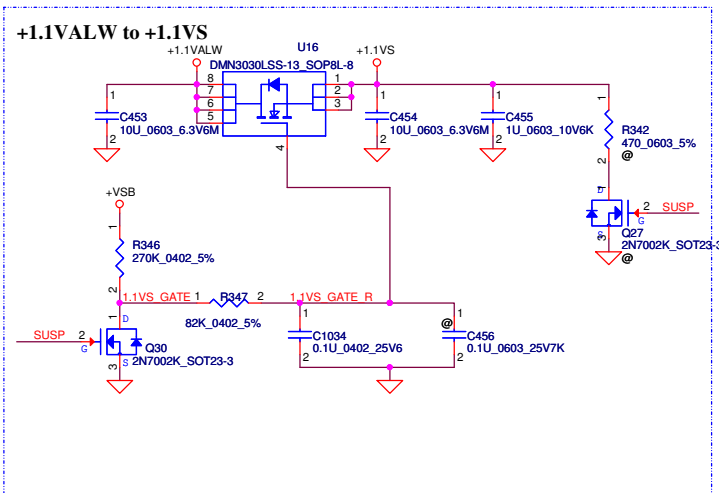
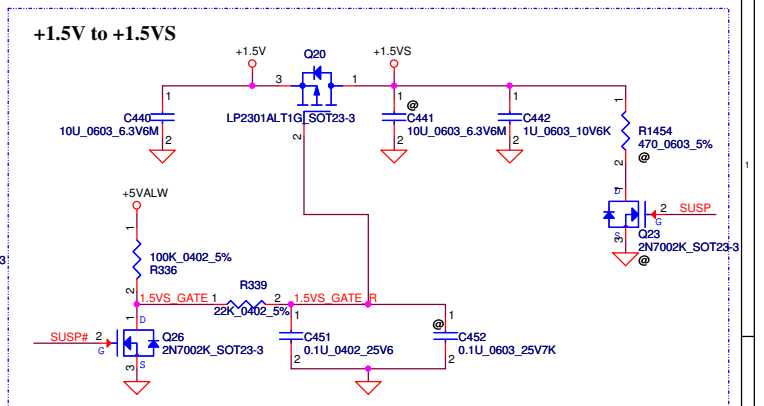
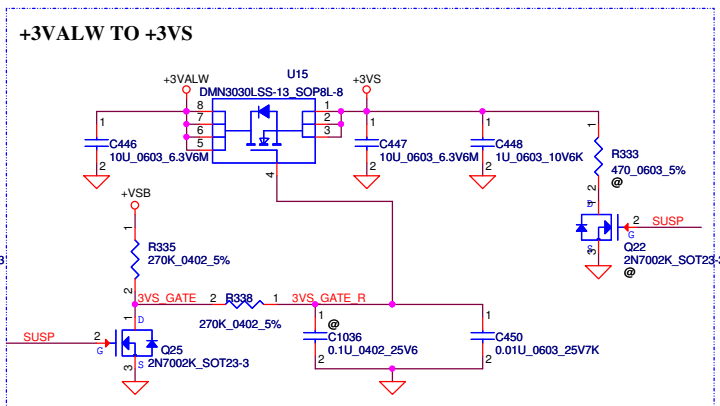
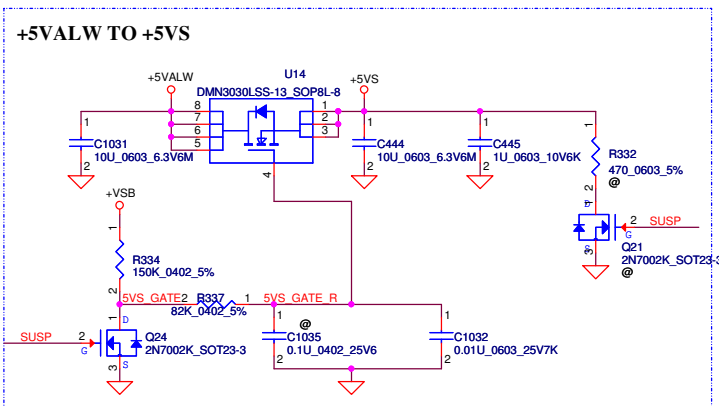


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

+VCC_KB_LED

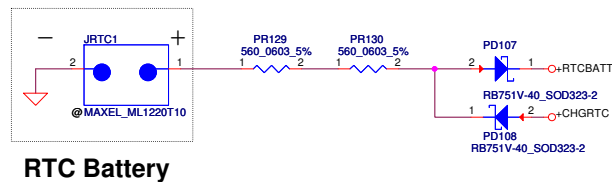
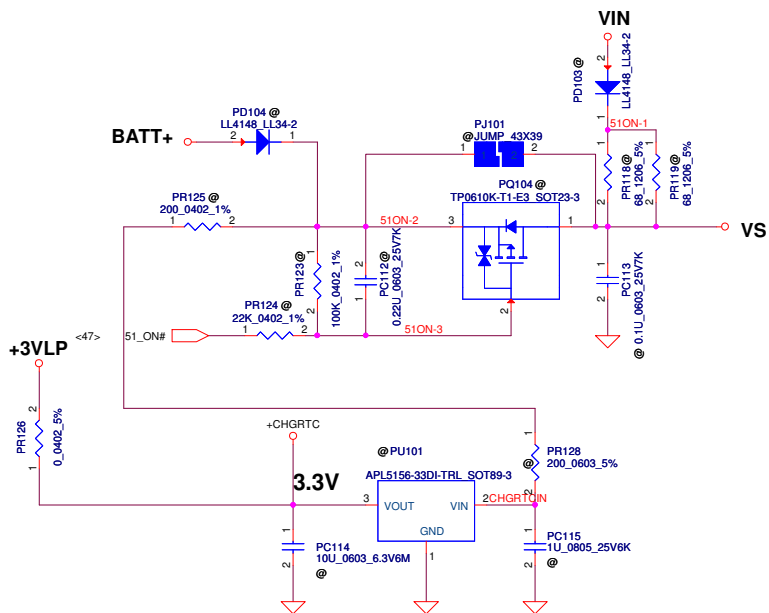
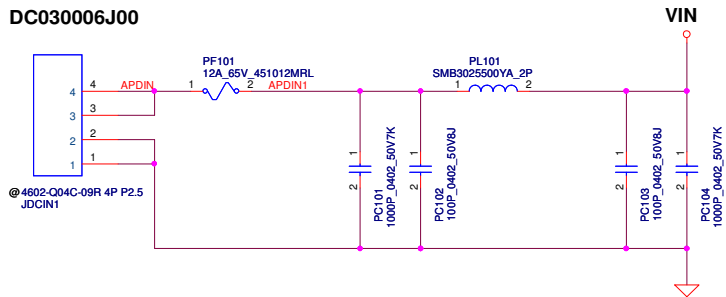


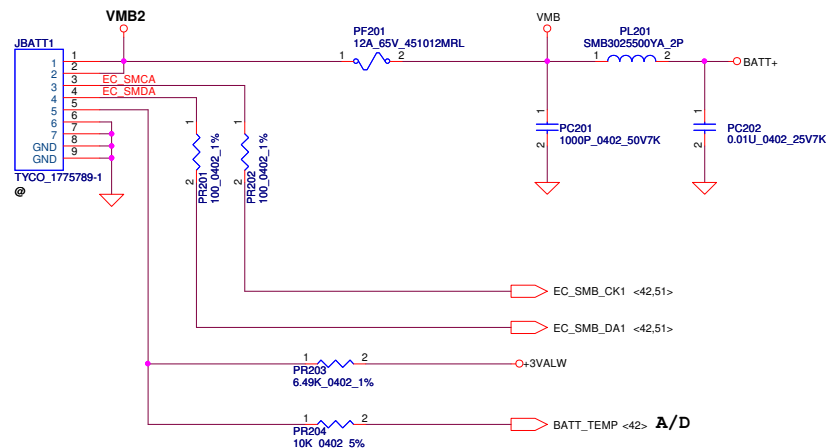
Security Classification	Compal Secret Data			Compal Electronics, Ltd.		
Issued Date	2011/07/21	Deciphered Date	2012/12/31	Title other IO connector		
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Issued Date	2011/06/30	Deciphered Date	2013/06/30	Title	DC Interface
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DC030006J00





For 90w adapter set 100w PR205 use 4.42k
PR211 use 10k ->

ADP_I need to write Charge Options Register (0x12H)=> bit6=1

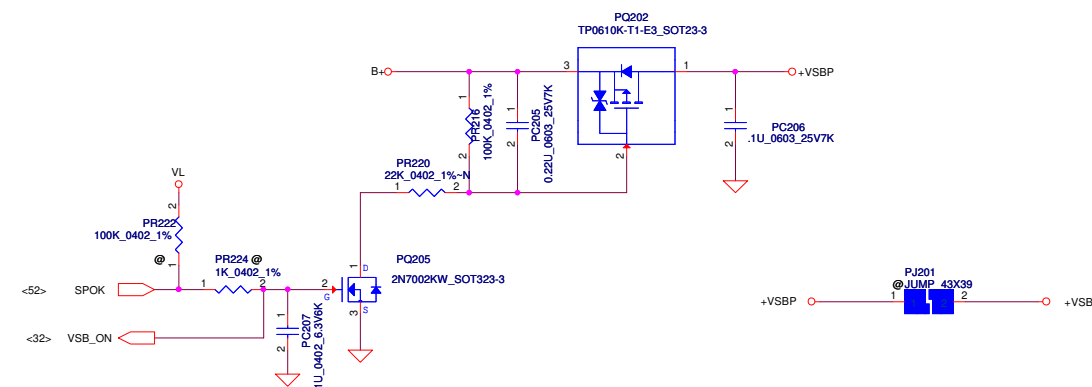
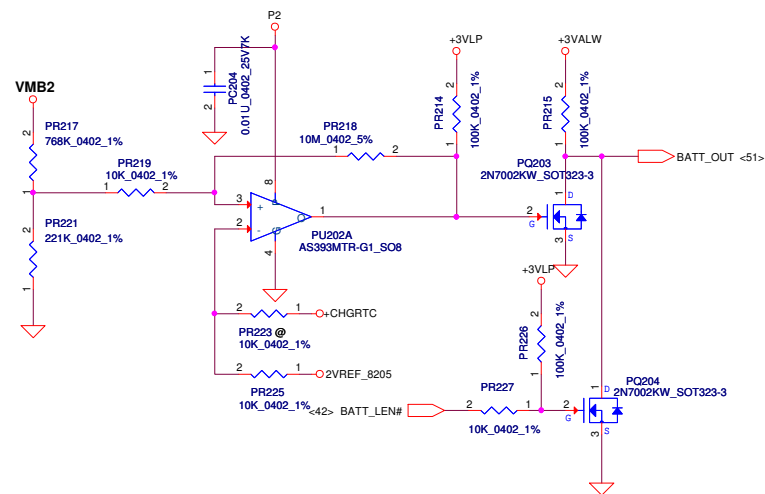
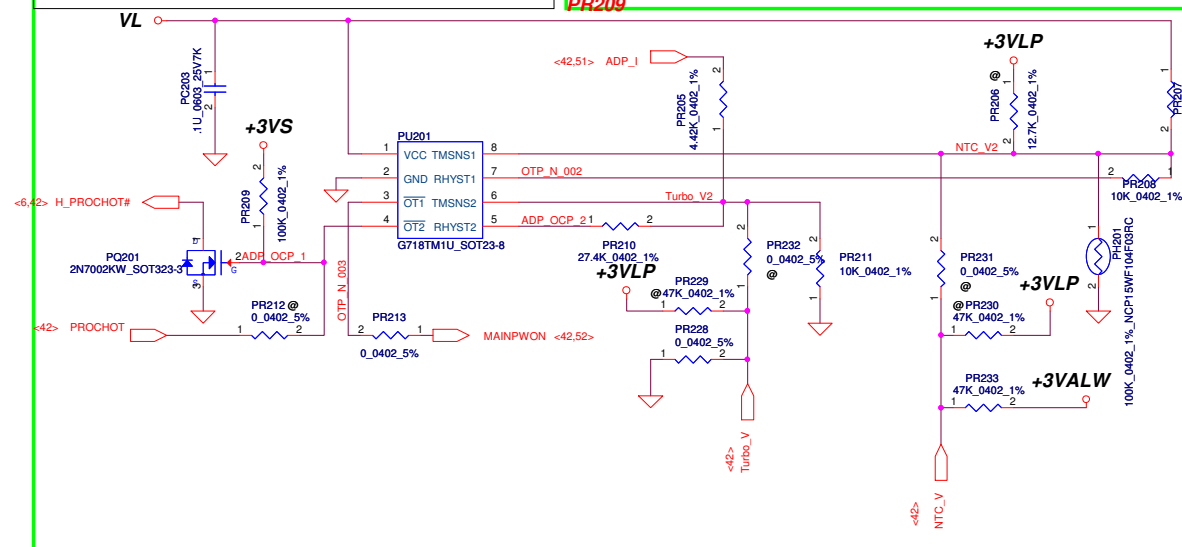
0: IOUT is the 20x current amplifier output <default @ POR>

1: IOUT is the 40x current amplifier output

PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +/3 degree C

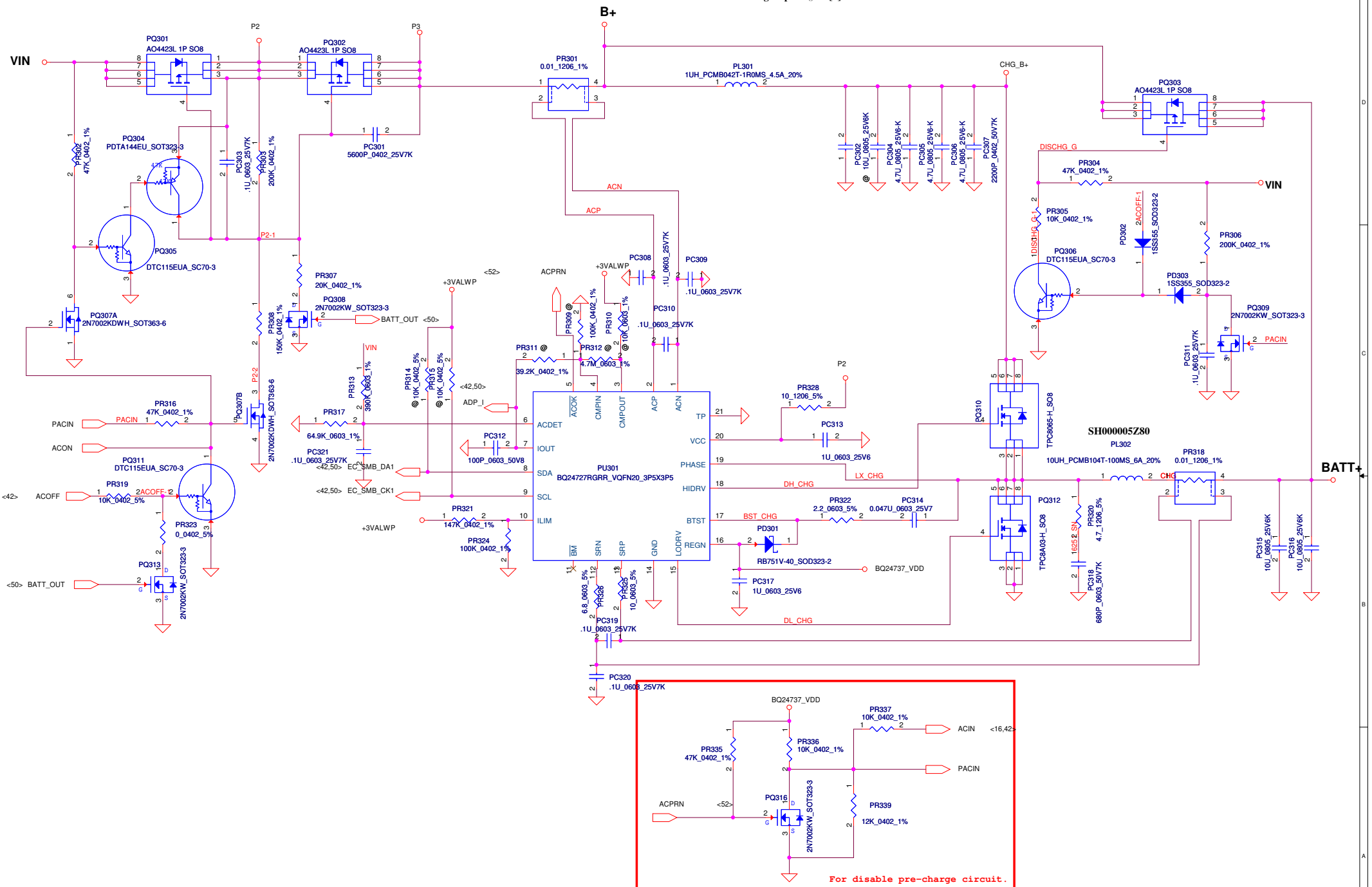
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 (Red square) --> Remove PU1 circuit, but keep PR205
PR211, PH201, PU201, PC203, PQ201, PR213, PR210, PR207, PR208,
PR209



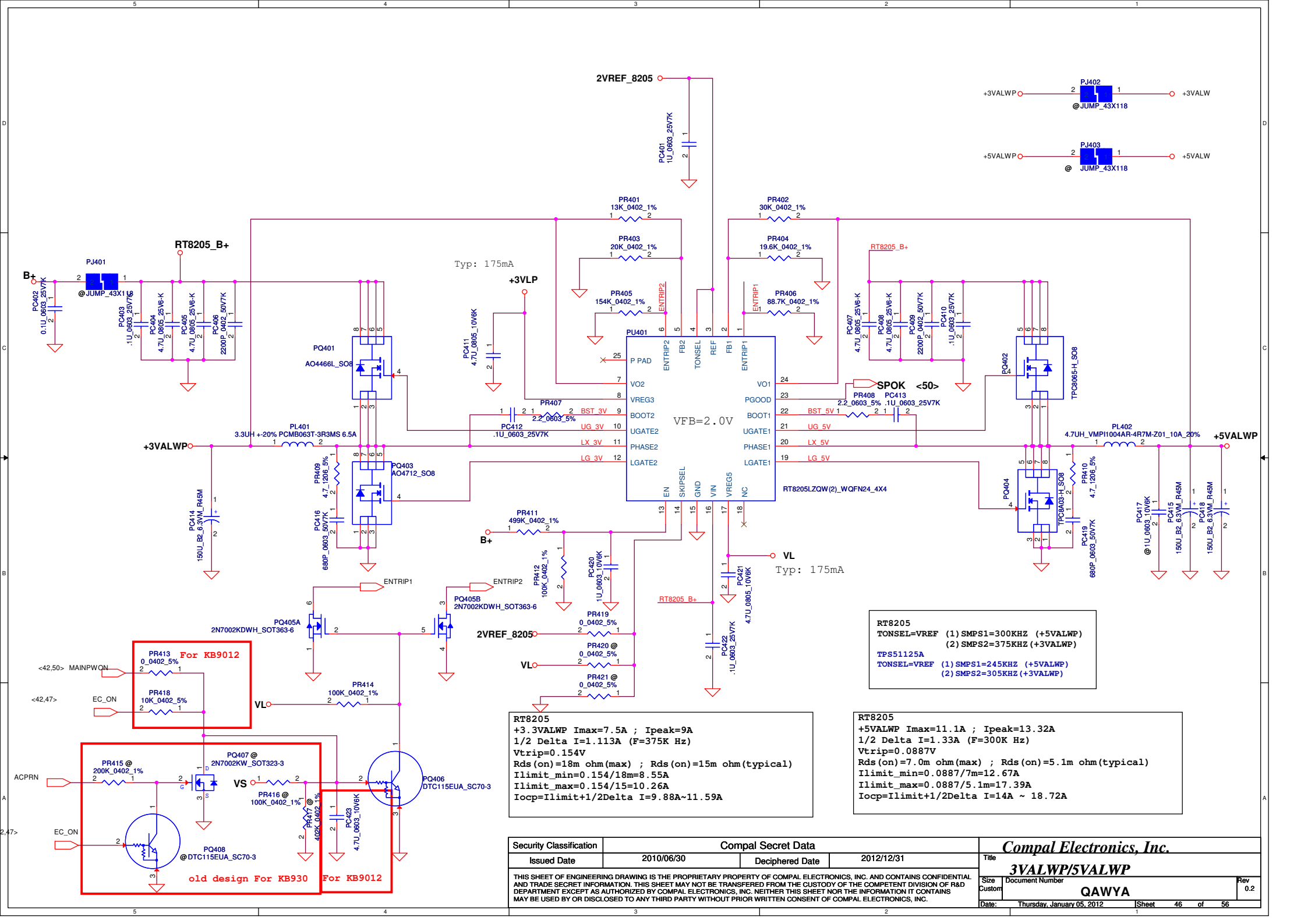
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	BATTERY CONN/IOTP
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				Date	Thursday, January 05, 2012
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Charge Option() bit[8]=1



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Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	
				CHARGER	
				QAWYA	
				Rev 0.2	
				Date: Thursday, January 05, 2012	
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RT8205
+3.3VALWP I_{max}=7.5A ; I_{peak}=9A
1/2 Delta I=1.113A (F=375K Hz)
V_{trip}=0.154V
R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
I_{limit_min}=0.154/18m=8.55A
I_{limit_max}=0.154/15=10.26A
I_{ocp}=I_{limit}+1/2Delta I=9.88A~11.59A

RT8205
TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)
TPS51125A
TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
(2) SMPS2=305KHZ (+3VALWP)

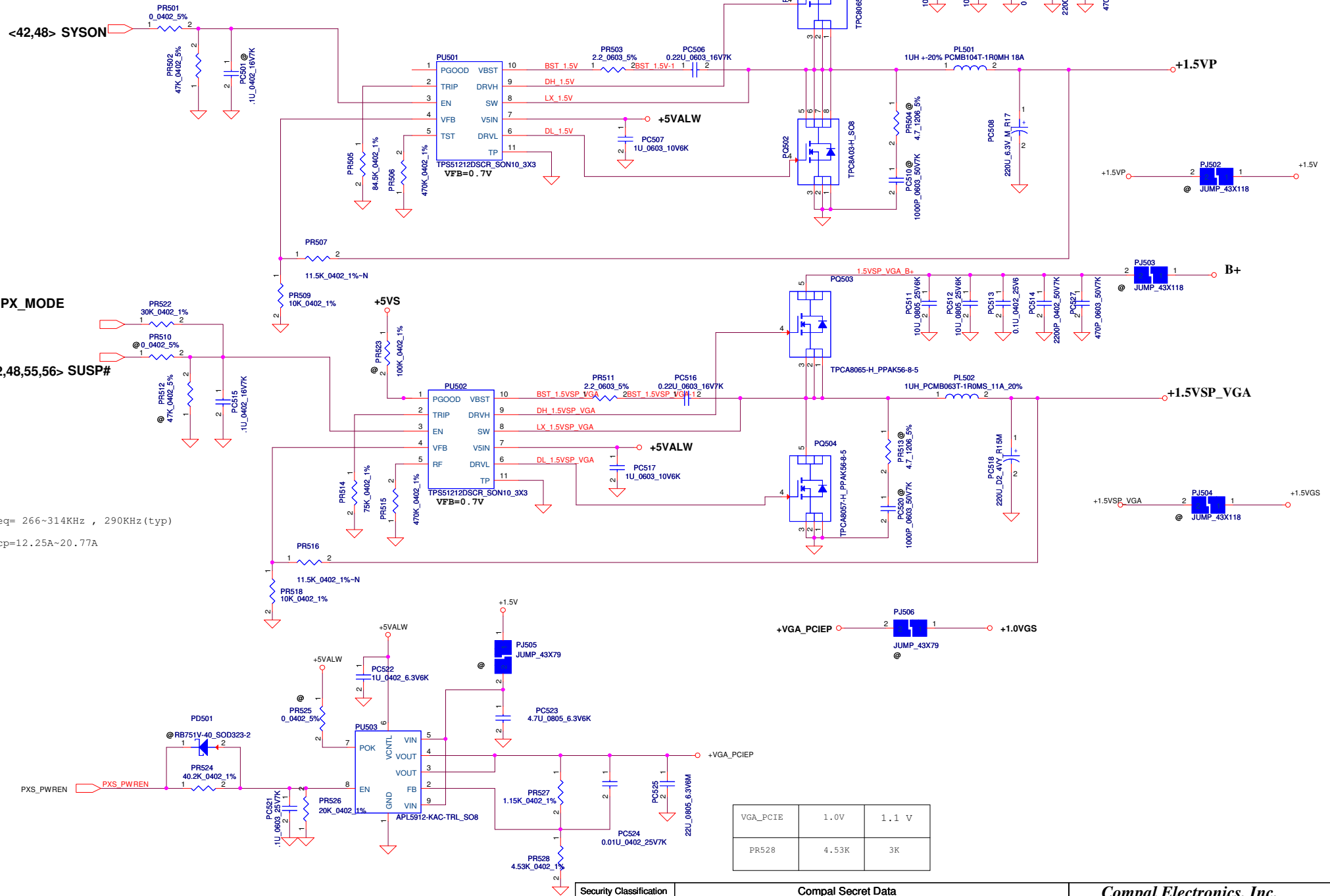
RT8205
+5VALWP I_{max}=11.1A ; I_{peak}=13.32A
1/2 Delta I=1.33A (F=300K Hz)
V_{trip}=0.0887V
R_{ds(on)}=7.0m ohm(max) ; R_{ds(on)}=5.1m ohm(typical)
I_{limit_min}=0.0887/7m=12.67A
I_{limit_max}=0.0887/5.1m=17.39A
I_{ocp}=I_{limit}+1/2Delta I=14A ~ 18.72A

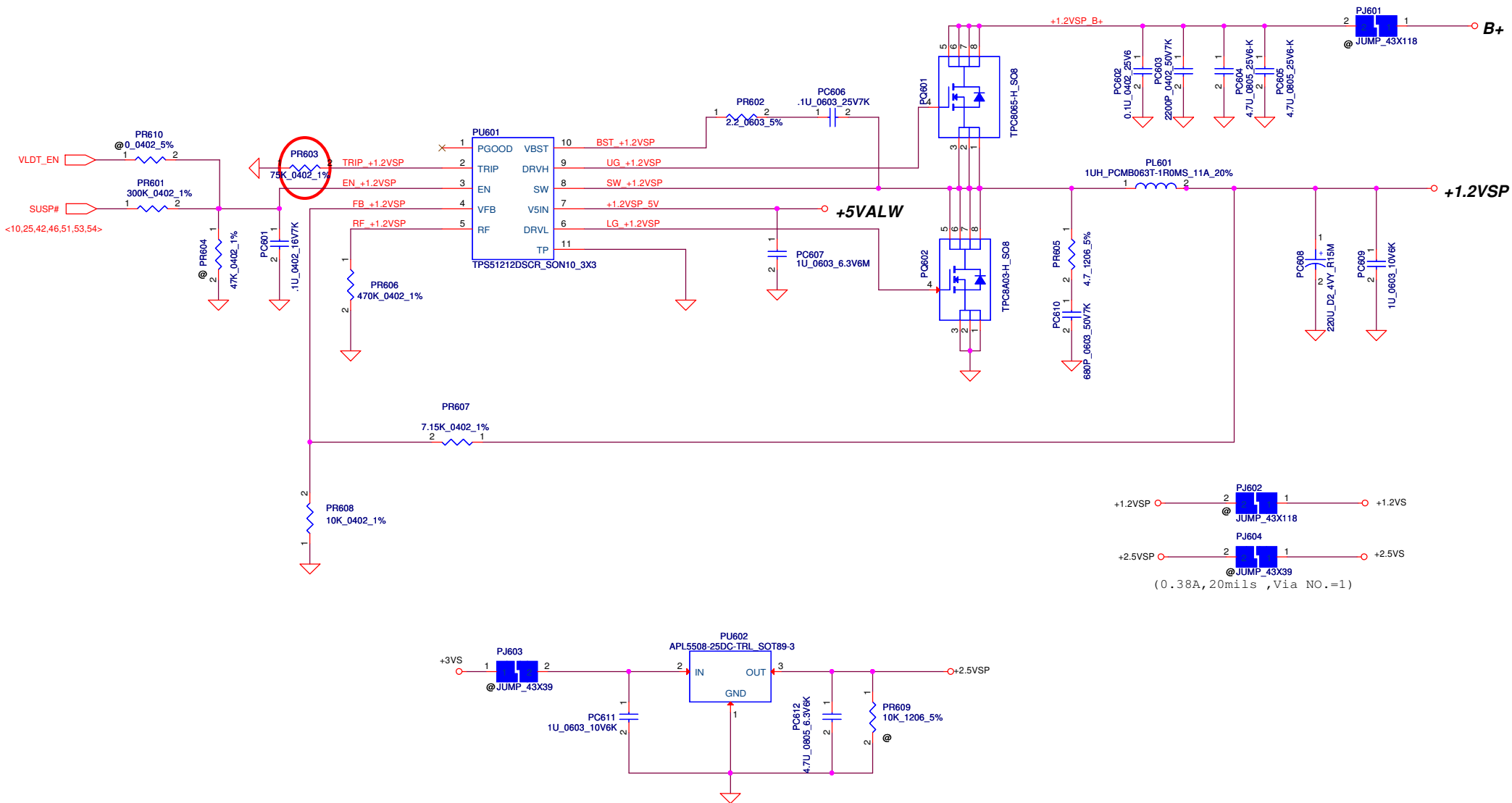
Security Classification		Compal Secret Data	
Issued Date	2010/06/30	Deciphered Date	2012/12/31
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Compal Electronics, Inc.			
Title		3VALWP/5VALWP	
Size	Document Number	Rev	
Custom	QAWYA	0.2	
Date:	Thursday, January 05, 2012	Sheet	46 of 56

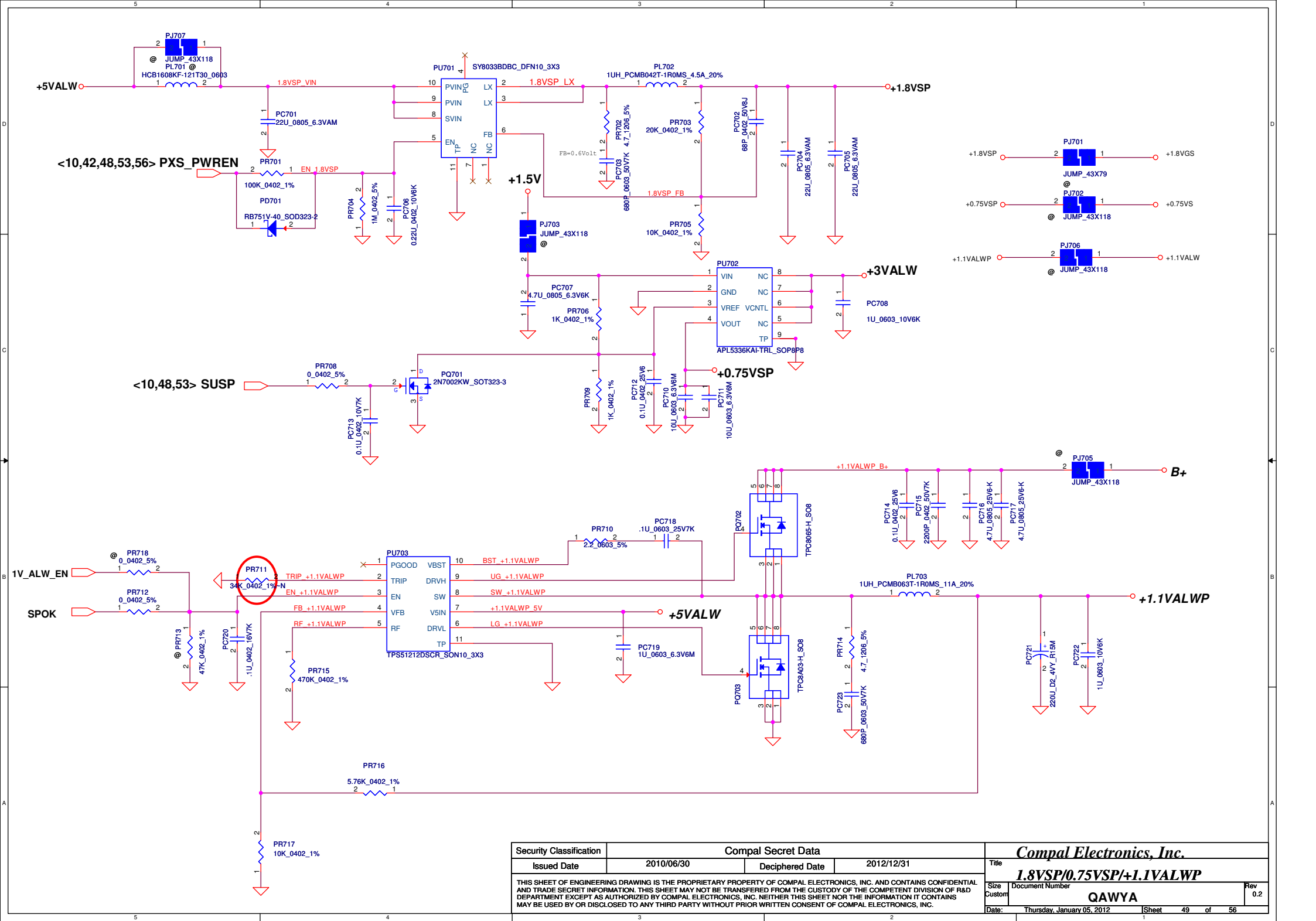
Freq= 266~314KHz , 290KHz(typ)

Iocp=13.58A~23.10A





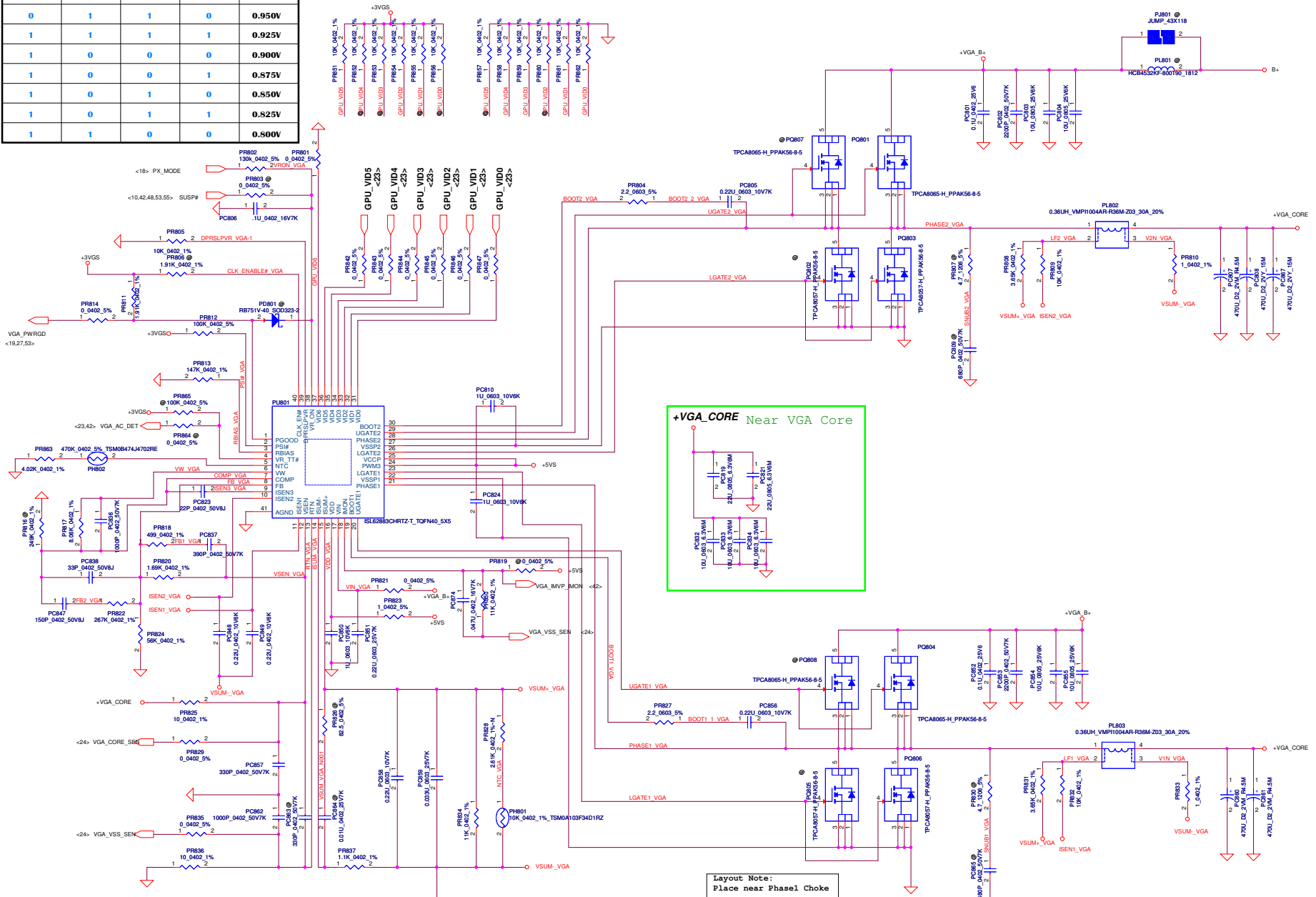
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2011/06/30		Deciphered Date		2012/12/31		Title	
								+1.2VSP/+2.5VSP	
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						Custom	QAWYA		0.2
						Date:	Thursday, January 05, 2012		Sheet 48 of 56



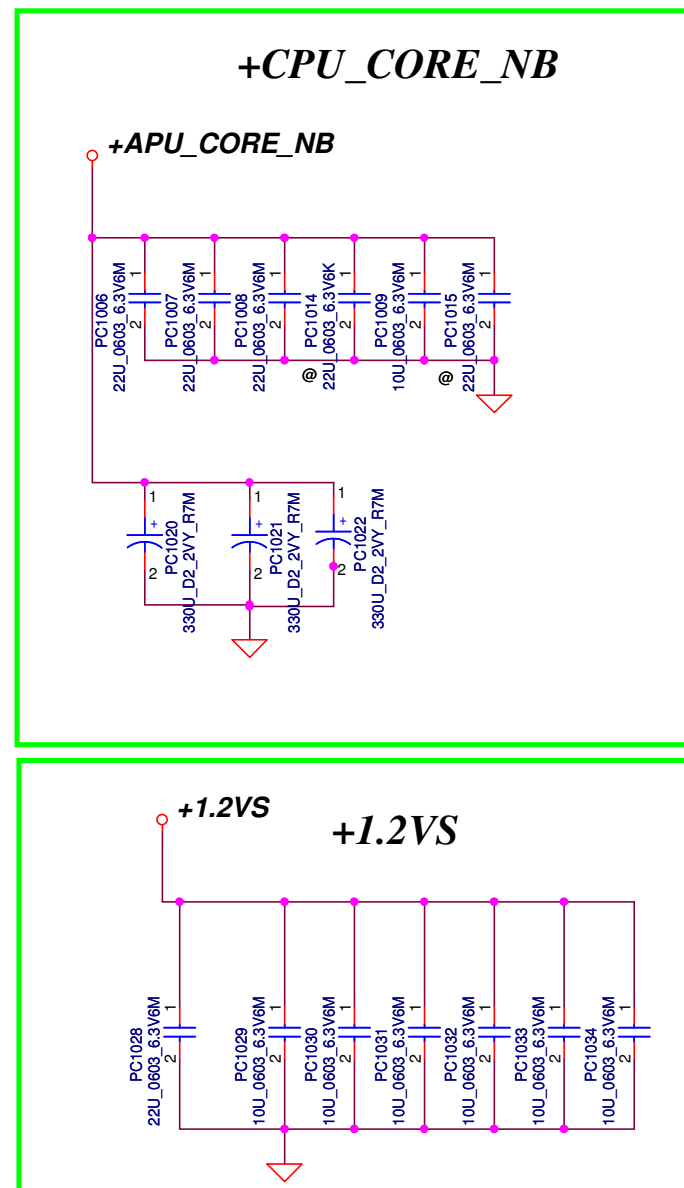
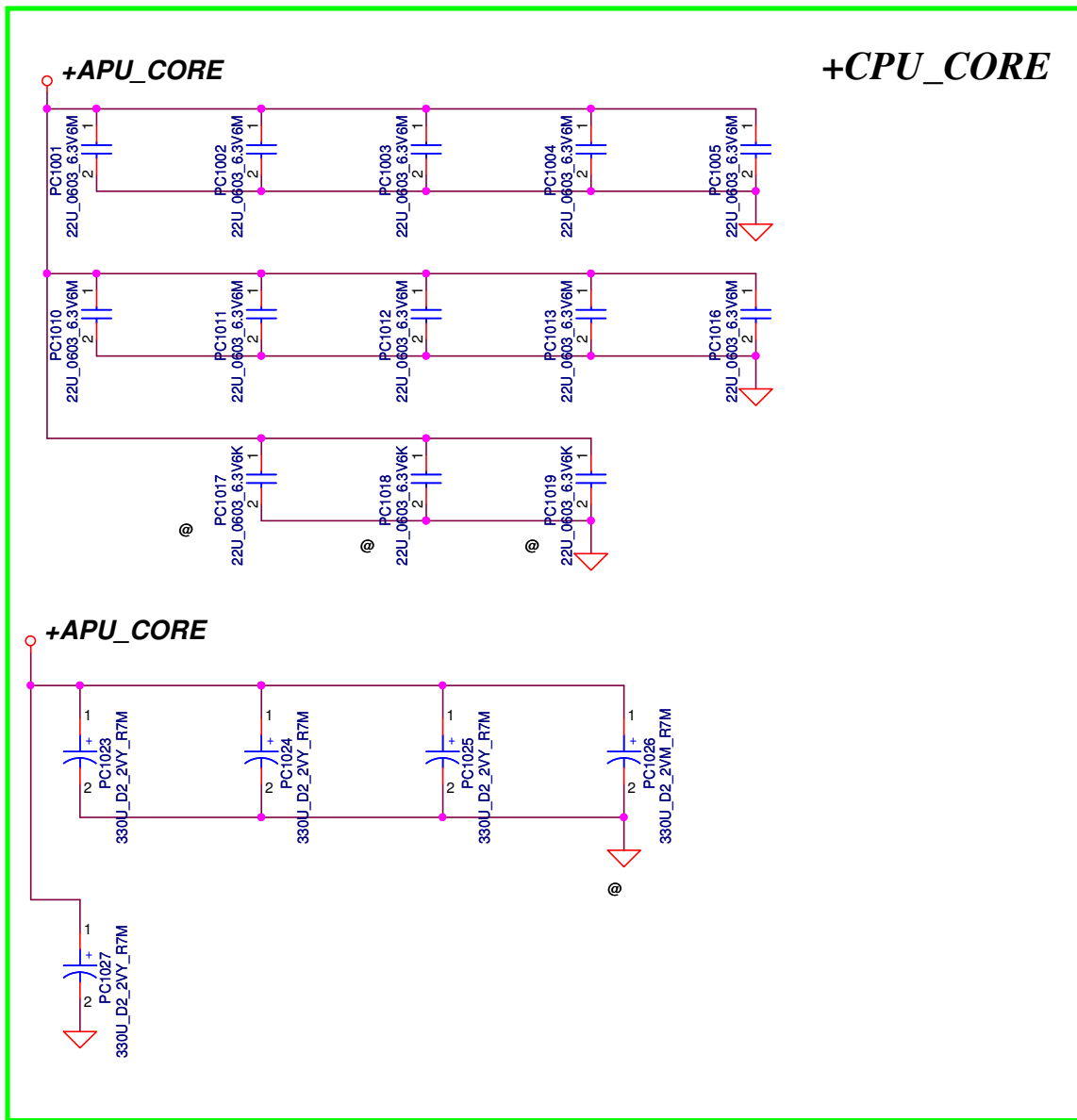
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/06/30	Deciphered Date	2012/12/31	Title	1.8VSP/0.75VSP/+1.1VALWP
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				Date	Thursday, January 05, 2012
				Sheet	49 of 56
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GPIO20	GPIO15	GPIO16	GPIO12
VID4	VID3	VID2	VID1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
1	1	1	1
1	0	0	0
1	0	1	0
1	0	1	1
1	0	0	0
1	1	0	0

Default



Layout Note:
Place near Phasel Choke



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/30	Deciphered Date	2012/12/31	Title	PROCESSOR DECOUPLING
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				QAWYA	
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Item	Reason for change	PG#	Modify List	Date	Phase
1	Change net name	1.FB added to PX_MODE 2.VSSSENSE_VGA to VGA_VSS_SEN 3.VCCSENSE_VGA to VGA_CORE_SEN 4.NVDD_PWR_EN to PX_MODE	5+1.5V_VGA to +1.5VGS 6.+1.8VS to +1.8VGS 7.APU_VDDNB_SEN to APU_VDDNB_SEN_H	10/11	
2	Don't need VDDQ_SENSE , 0.75VVR_EN# , DPRSIPVR_VGA , 1.5V_VGA_PWROK	1.remove pr517 pc519 and net VDDQ_SENSE 2.remove pr707 and net 0.75VVR_EN# 3.remove pr815 pr838 4.remove net 1.5V_VGA_PWROK		10/11	
3	Change net name	1.H_PROCHOT#_EC to H_PROCHOT#		10/13	
4	Change & add power component	1.add pc947 2.pc901 pc941 remove BOM structure 4.pr913 change 0603 to 0402	3.pc913 pc942 change value 50v to 25v	10/14	
5	Change net name	1.change 1.8VGS EN PIN SUSP# to PXS_PWREN		10/14	
6	Add power component & Net	1.add PR965 2.add net APU_IMON		10/18	
7	Change power component (For EMI)	1.change PR602,PR710 to 2.2 ohm 2.PR605 PC610 remove BOM structure 3.PR714 PC723 remove BOM structure		10/19	
8	Remove & add & change power component	1.add PR610 for VR_ON 2.remove PC811, PC812, PC813, PC814, PC815, PC816, PC817, PC818, PC820, PC822, PC825, PC826, PC827, PC828, PC829, PC830, PC831, PC835, PC839, PC840, PC841, PC842, PC843, PC844, PC845, PC846 3.Remove PR327 and net BM# 4.change PC819, PC821 to 22U PC832, PC833, PC834 to 10U		10/21	
9	Change power component	1.change PR306 to 200k 2.PC322 remove BOM structure 3.change PC947 to PL901 right side		10/24	
10	Change power component	1.PR502 remove BOM structure		10/26	
11	Change power component	1.change PL501, PL601, PL703 to 1UH_PCBM063T-1R0M5_11A 2.change PL901 _20%		10/27	
12	Add power component & Net	1.add PR718 and NET IV_ALW_EN 2.NET VR_ON change to VLDT_EN		10/27	
13	Change power component	1.move PR960, PR962 to near APU_VDD_SEN_Hand APU_VDD_SEN_L		10/28	
14	update footprint	1.update PL901 footprint		10/31	
15	Change power component	1.change PR404 to 19.6k		11/03	
16	Change & Add power component	1.add PR966, PR967 2.change PC712 to 0.1U_0402_25V6		11/07	
17	Change power component	1.change PQ316 to 2N7002KW_SOT323-3		11/09	
18	Change power component	1.change PQ302 to AO4423L		11/11	
19	Change page number	change P44~P54 to P43~P53		11/15	
20	Change power component	1.change PQ301, PQ303 to AO4423L		11/16	
21	Change power component & Add BOM structure	1.PQ802 PQ805 PQ807 PQ808 add BOM structure 2.change PR701 to 100K, PC706 to 0.22U, PR524 to 120K 3.change PR522 to 169K, PR802 to 130K 4.PC515 remove BOM structure		11/17	
22	Change power component	1.change PC314 to SE042473M80 0.047U 25V M X7R 0603		11/18	
23	Change power component	2.change PR524 to 40.2K		11/21	
24	Change & Add power component	1.change PC508 (SF000002N00) to (SF000002Y00) 2.add PU201, PR207, PR208, PR209, PR210, PR213, PC203, PQ201 remove PR206		11/22	
25	Change power component	1.change PC832, PC833, PC834 to 0603 size		11/30	
26	Change power component	1.change PR824 to 56k 2.move PC947 to connect CPU_B+ 3.change PR837 to 1.1k 4. PR525 add BOM structure		12/8	
27	Add Net	1.Add V5B_ON		12/9	
28	Change power component	1.6277 pin30 connect to +5VALW		12/12	
29	Change power component	1.PL302 change to 10u (SH000005280) 2.PQ503, PQ504 change to power pak-5-6 3.PR228, PR229, PR230, PR231, PR232		12/13	
30	Change power component	1.PR918, PR932 change to 133k PR924, PR943 change to 10.5k		12/20	
31	Change & Add power component	1.add PD701 for HW turn off time 2.change PR601 to 300k		12/22	
32	Change power component	1.change PJ301 to PL301		12/23	
33	Change power component	1.change PL301 and PL702 to SH000001W00		12/26	
34	Change & Add power component	1.add PR233		12/28	
35	Change power component	1.change PR522 to 30k		1/4	

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QAWYA HW PIR List

NO DATE		PAGE		MODIFICATION LIST	PURPOSE	EVT TO DVT				NOTE
1	23,25			pin D13,P2 of UV5,UV9 connect to +1.5VGS	correct it to follow AMD CRB					
2	36			Pin127, add VSB_ON function,reserve R380	Power consumption					reserve R380 (1K)
3	41			Update JP10 symbol	DFB highlight the wrong symbol with material					
4	36			Change 1V_ALW_EN from pin107 to pin 71	FOR RTL2132 EC CODE ISSUE					
	36			Change MUTE_LED# from pin85 to pin107						
	36			Change EAPD from pin86 to pin72						add R327,R328 pull high to +3VS
	36			Reserver TL_CLK and TL_DATA on EC pin 85 and Pin86						POP R357 and R340 0ohm
	26			Reserve TL_CLK and TL_DATA path to RTD2132S						
5	35			Correct Head phone R/L connection	Correct Head phone R/L connection					
6	36			Change TP_CLK and TP_DATA pull high from +5VS to +3VS	Only +3VS TP module					change R307 anf R304 from 4.7K to 2.2K
7	11			ADD R73 0 ohm for APU_PWRGD	for power test					12/12 update to FCH side
8	36			Change BRDID setting to DVT	Change BRDID setting to DVT					Change R311 to 18K
9	17			Change Y2 to small package (standard part)	Standard part (SJ10000DK00)					SJ10000CV00
10	26			Remove R299,R300,R353,R326,Q144	Remove unuse path					
11	38			Del H14	ME Update					
12	40			Change USB3.0 DB pin define	Follow QiWY3					JP23
13	11~15			Change FCH PN to A14 version	Change FCH PN to A14 version					Change FCH PN from SA000043IH0 to SA000043IK0
14	32			LAN surge solution update	LAN surge solution update					No change ,BACK to R01 sch
15	36			Add 0 ohm on Mainpower on at EC side	Power test					
16	40			Change JP21 symbol						Swap Pin1 to pin 30 by connector foot print
17	36			Reserve 100k pull down for VSB_ON						R317
18	28			Change L19 ->R353 L20->358	For CRT EA					33 ohm 0603 5%(SD013330A80)
19	11			Change R124 to 33 ohm	For EA					
20	42			Modify power sequence value						R334 ->150K R337 ->82K C1032 ->0.01u C1035 ->@ R335 ->270K R338 ->270K C450 ->0.01u C1036 ->@ R339 ->22K R346 ->270k R347 ->82K
21	18			Update U7,Q11 BOM structure to PX4@						
22	26			Del R64	remove no use part					
				Reserver pull high to +3VALW of VGA_GATE#						POP R326
24	29			HDMI pop common choke	EMI test result					POP UNPOP L23,L24,L26,L27 R865~R872
25	39,40			USB pop common choke	EMI test result					POP UNPOP L64,L68~L73 R1154~R1165,R1108,R1109
26	35			Swap EXT_MIC_R and EXT_MIC_L	Correct					
27	11,17,31			Update crystal part	Vendor test result					C155 -> 18p C156 -> 18p X1->SJ10000E800 C157->10p C160->10p Y6->SJ10000E800 C968->12p C969->12p Y2->SJ100009700 C283->10p C282->10p
28	32			Update CL22 ->@ ADD CL26 (10p_0603_50V)	EMI request					
29	30			Update R893,R894->@ Update C572,C573,C459,C460,C566,C567,C568->SSD@						

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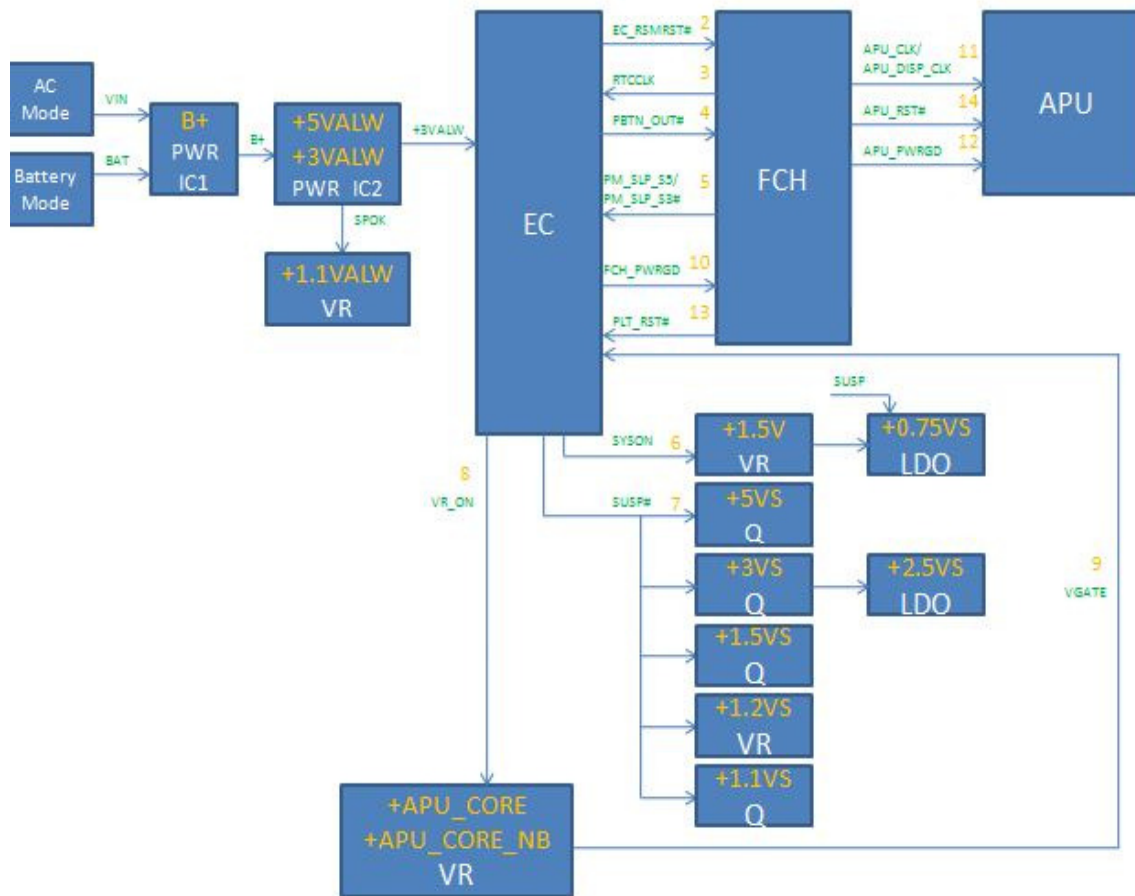
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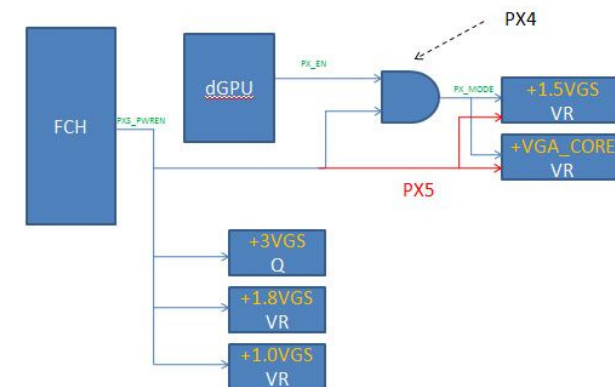
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SYSTEM



VGA



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