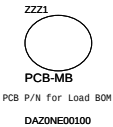


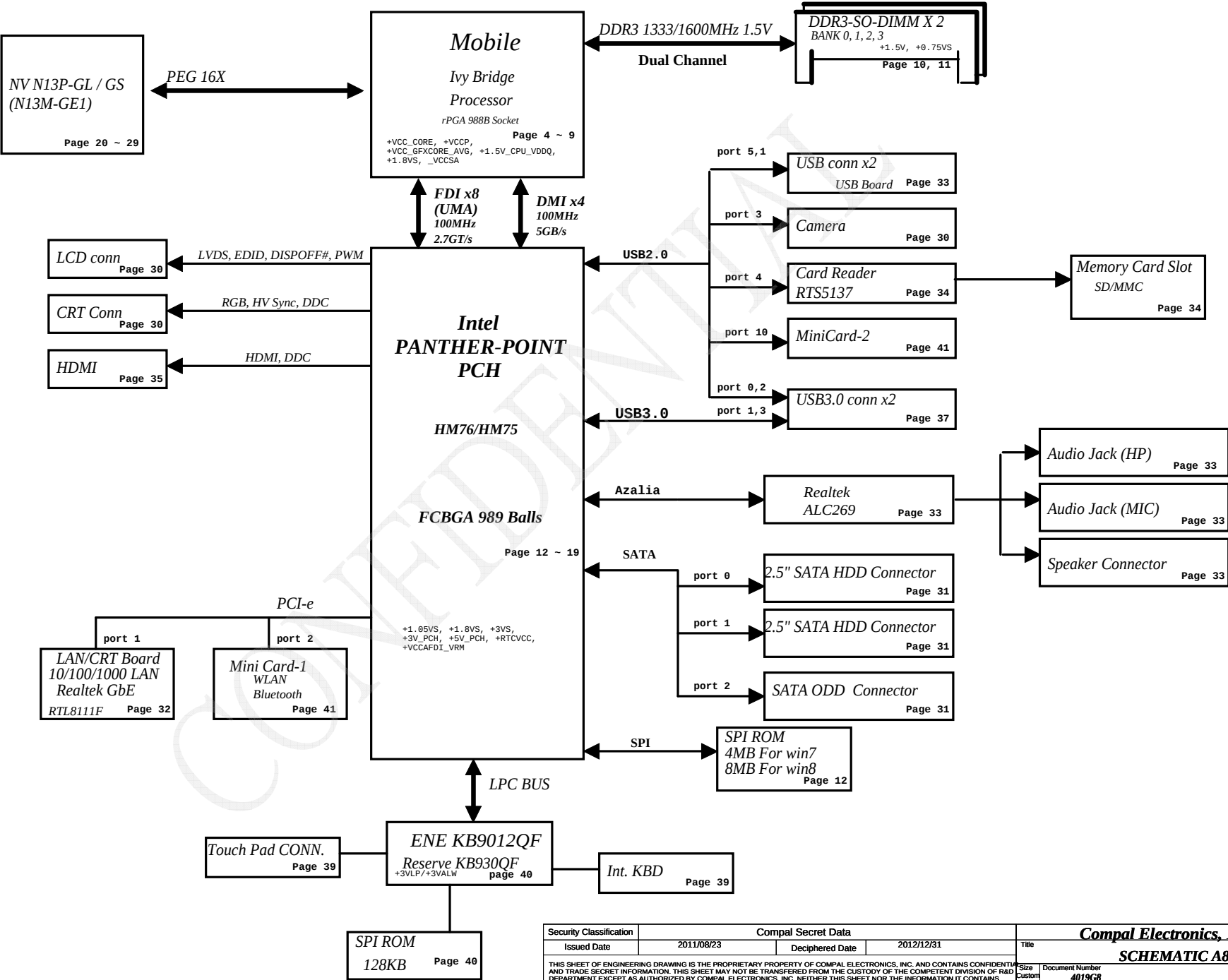
Compal Confidential
QCL70 MB Schematic Document
LA - 8222P

Rev: 1.0
2012.01.09

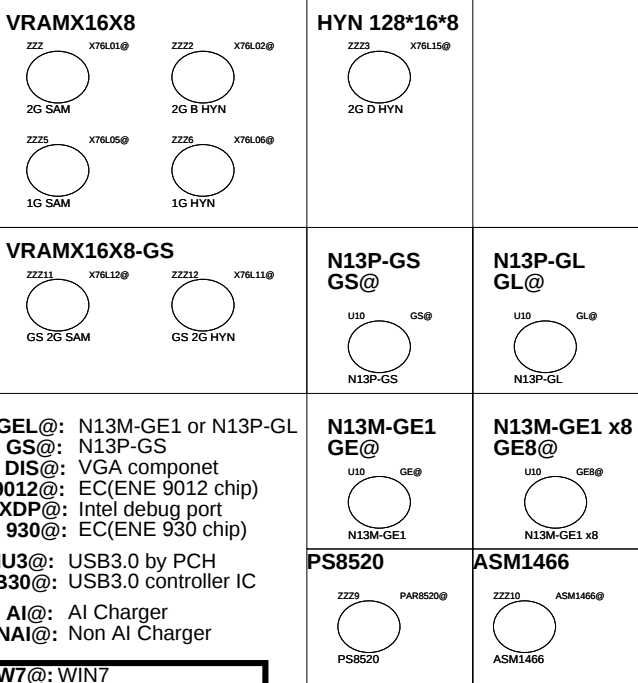
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				Document Number 4019G8	Rev B
Date: Monday, February 13, 2012				Sheet 1 of 61	

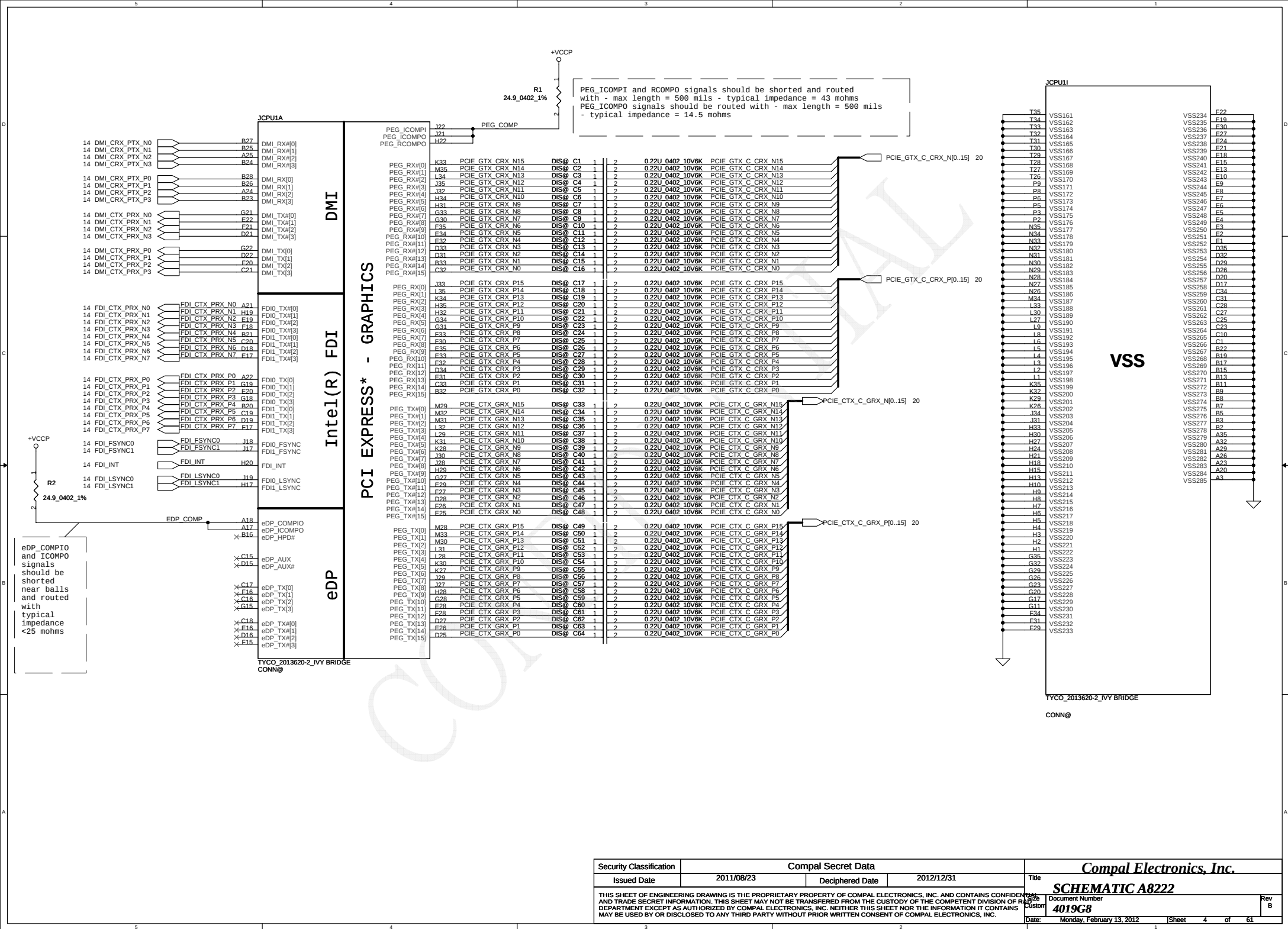


QCL70

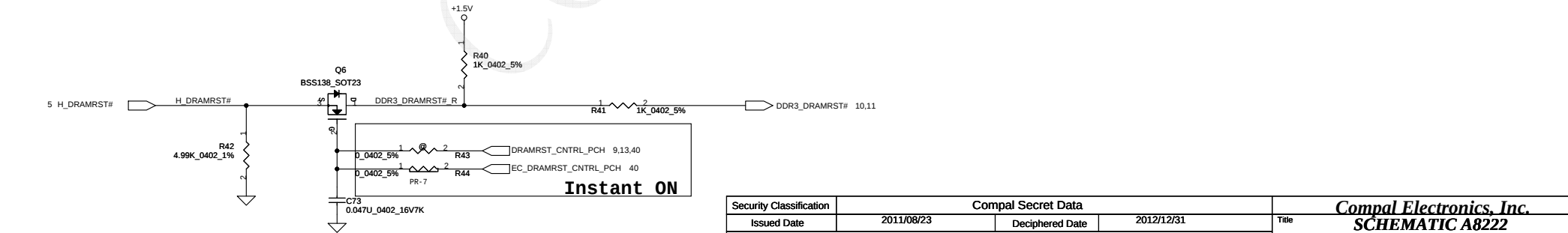
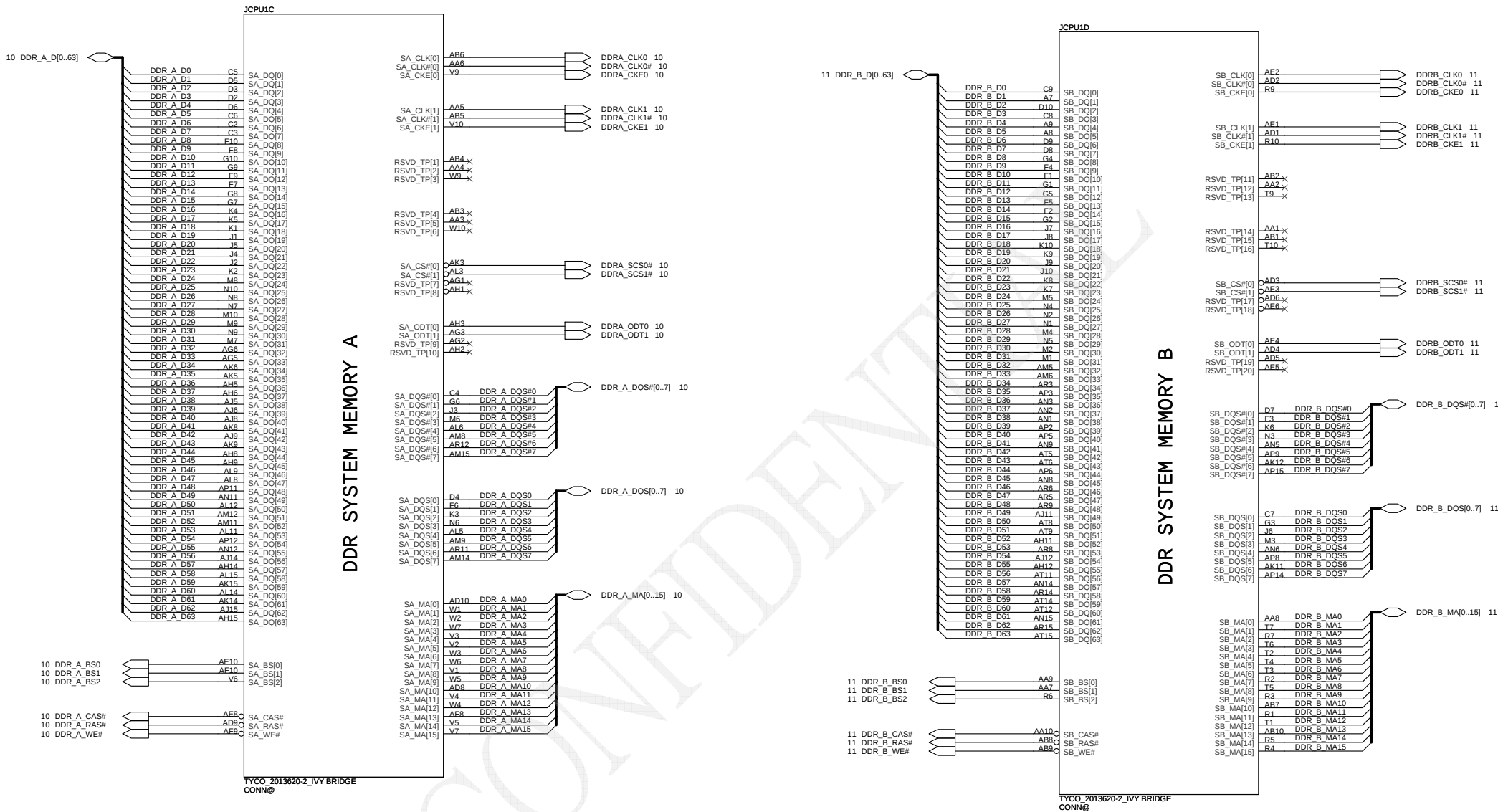


X76@:



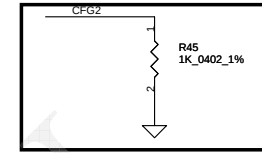
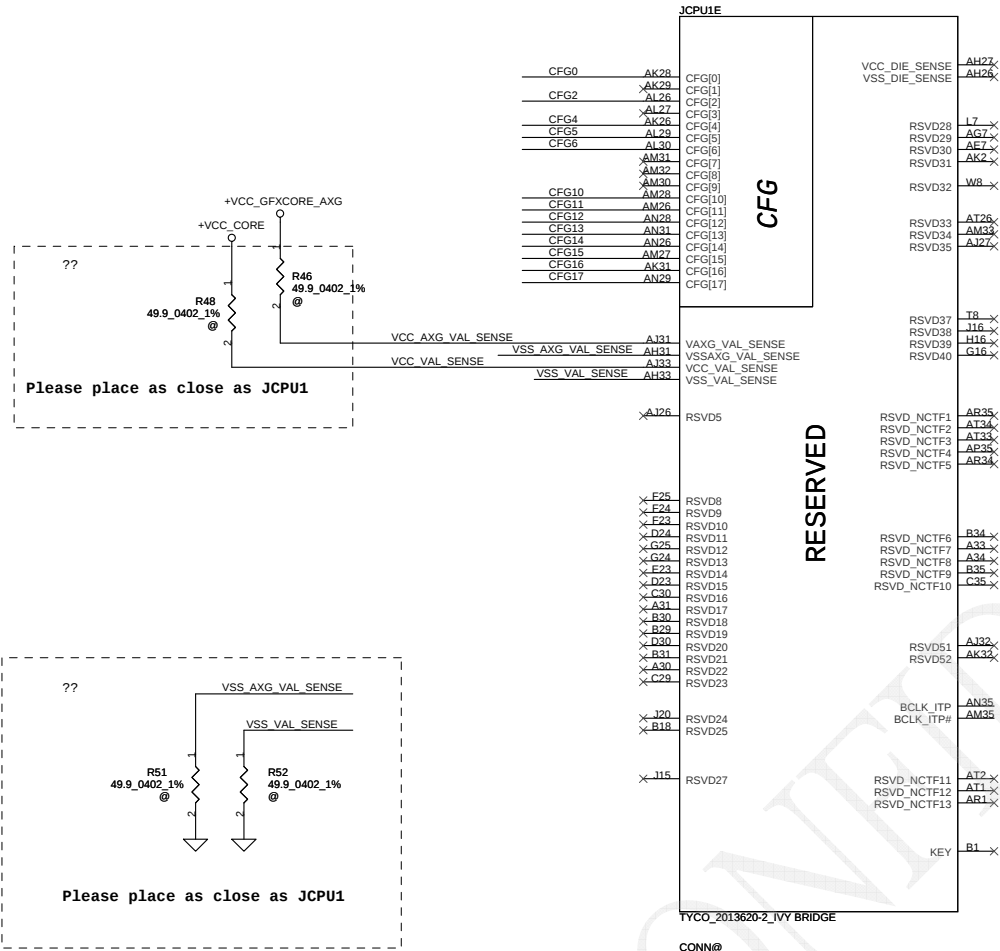


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			Sheet	4 of 61



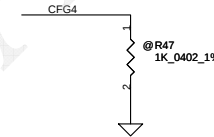
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CFG Straps for Processor



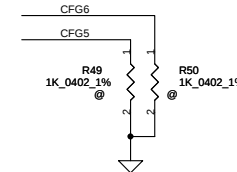
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed
------	--



Display Port Presence Strap

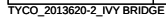
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



PCIE Port Bifurcation Straps

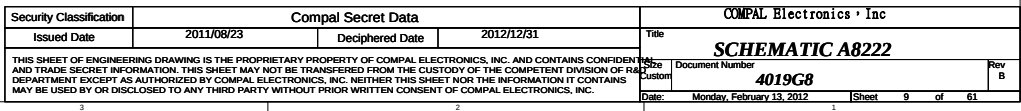
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--

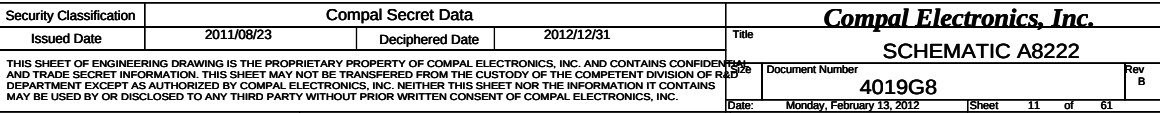
JCPU1F

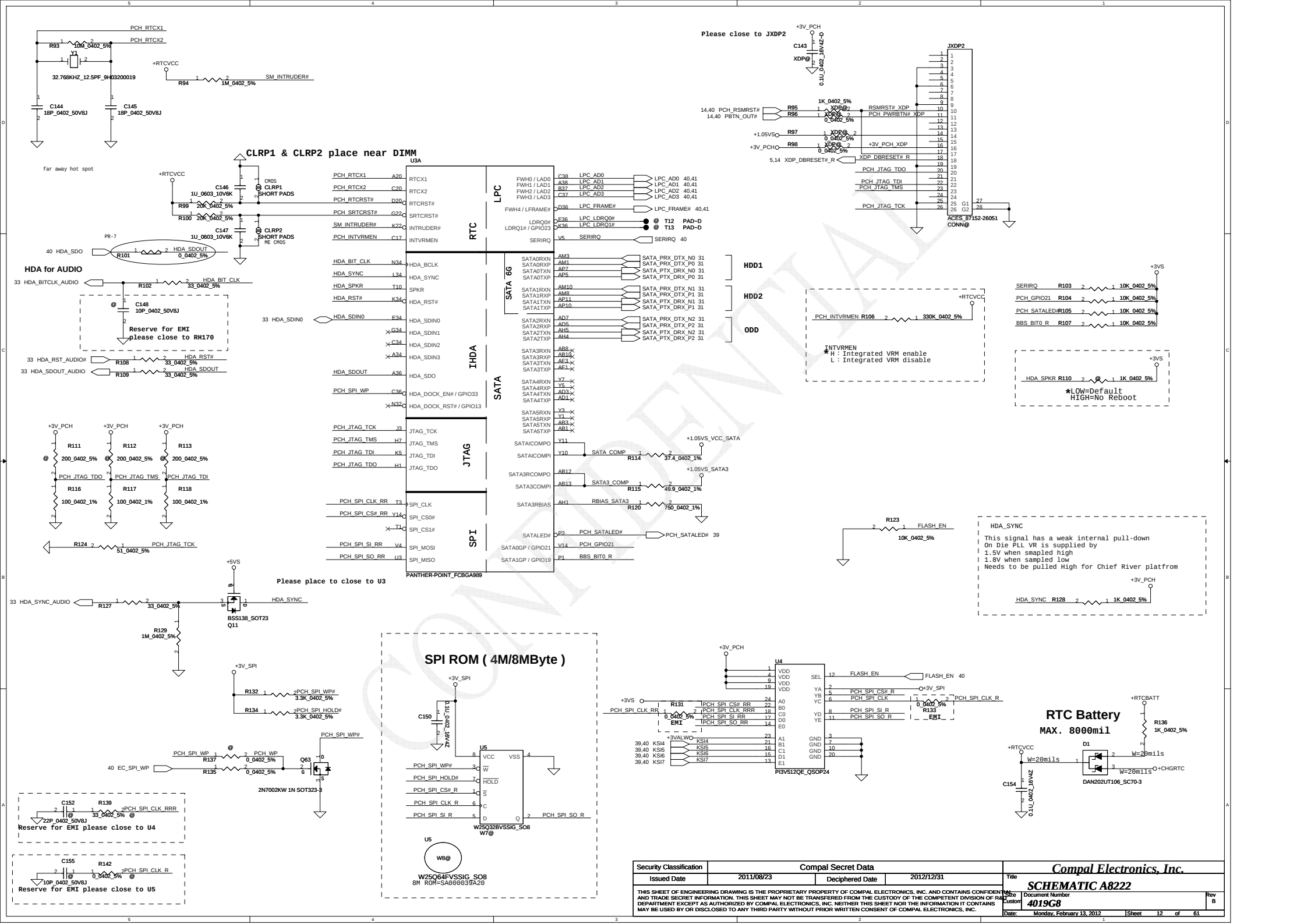


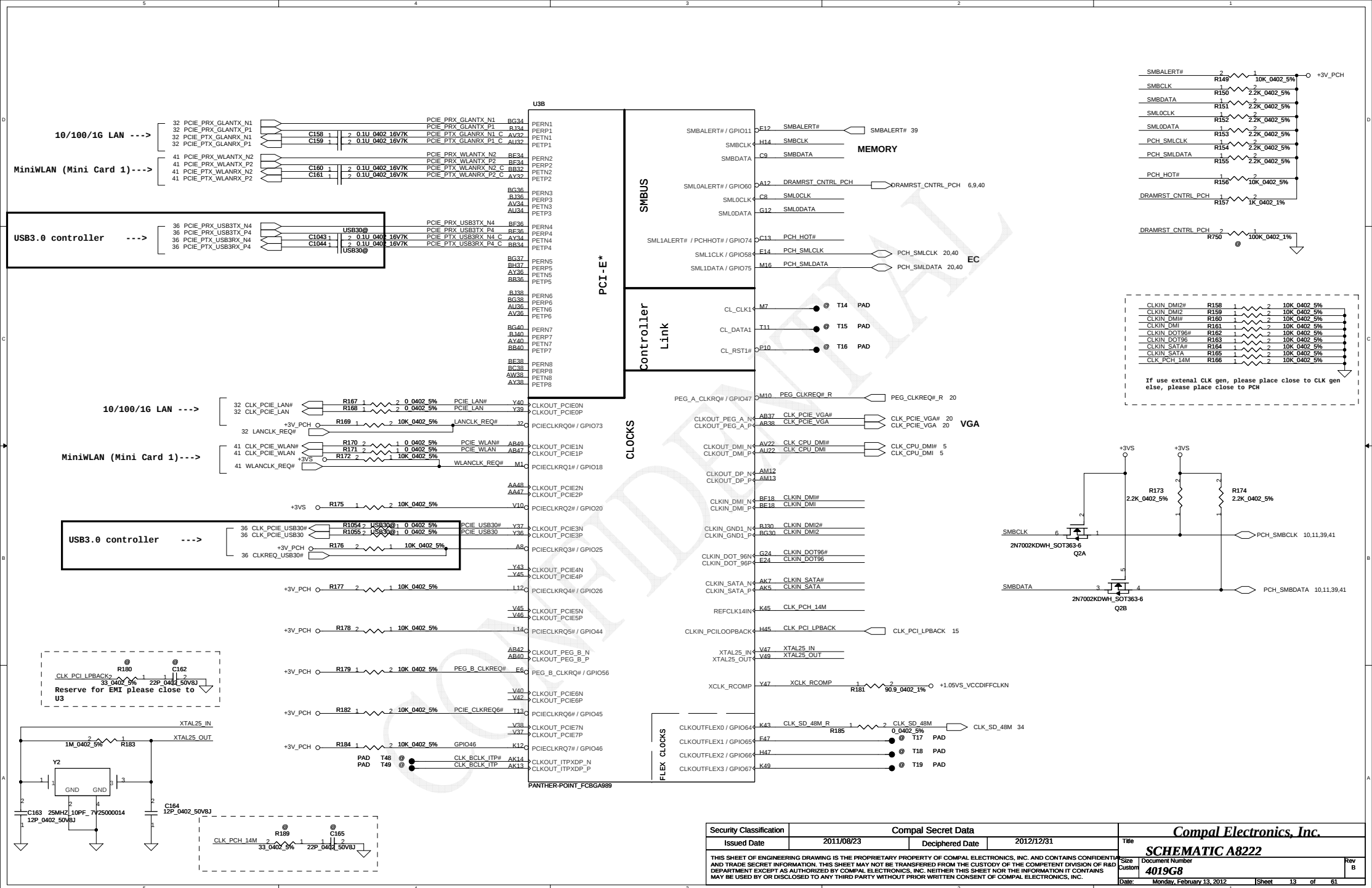
CONN@

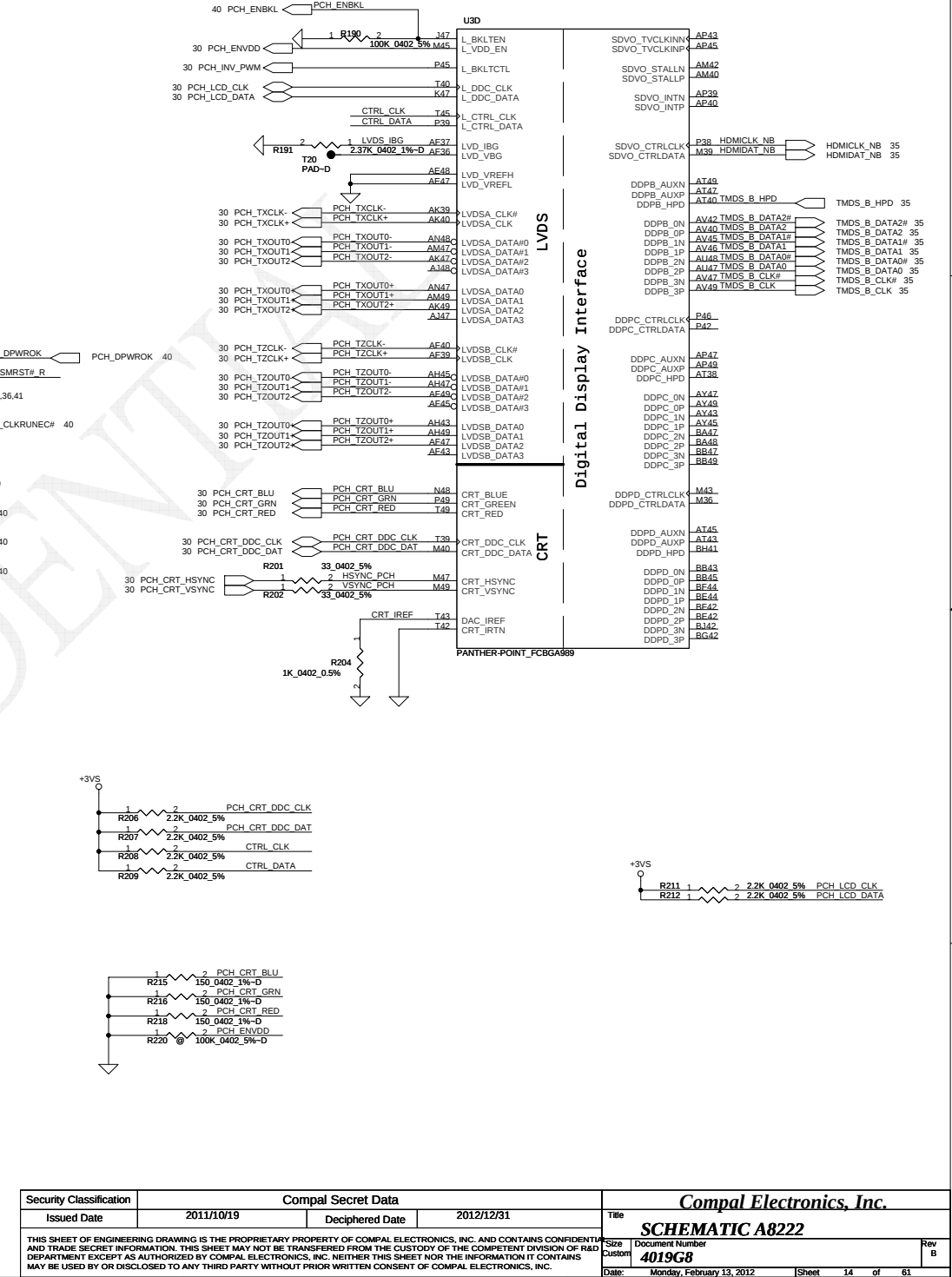
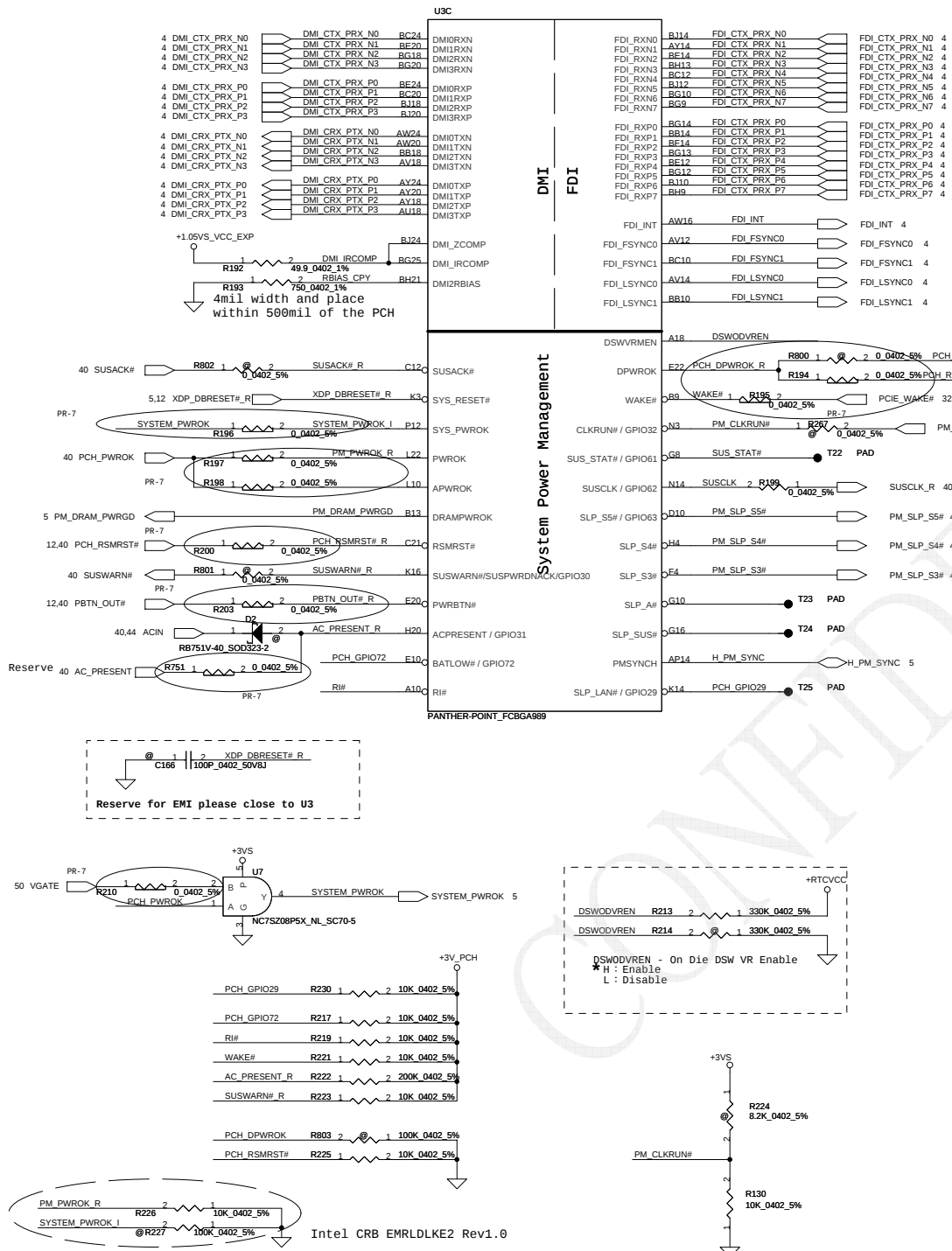
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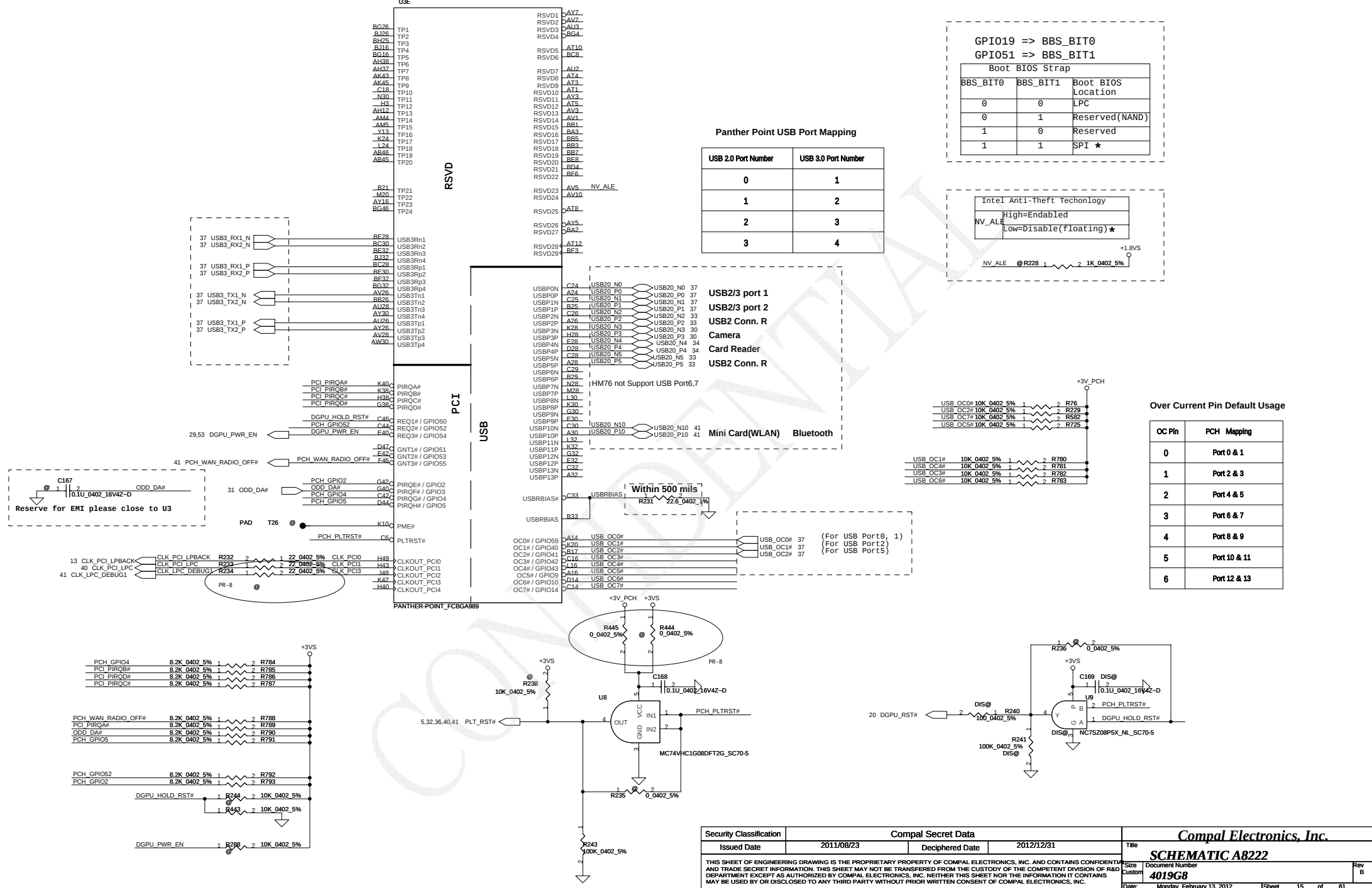


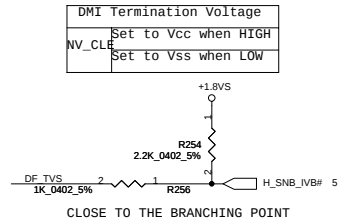
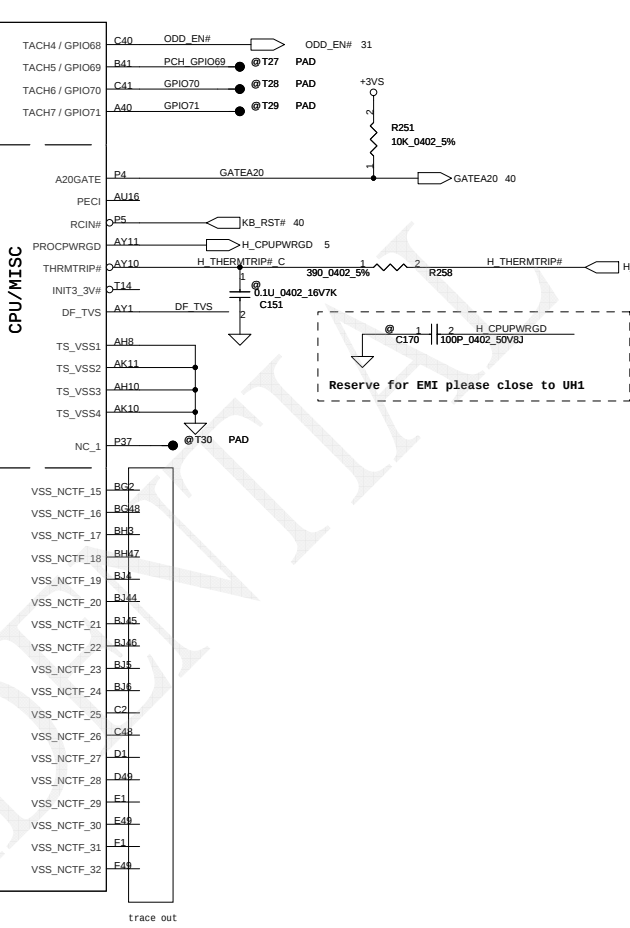
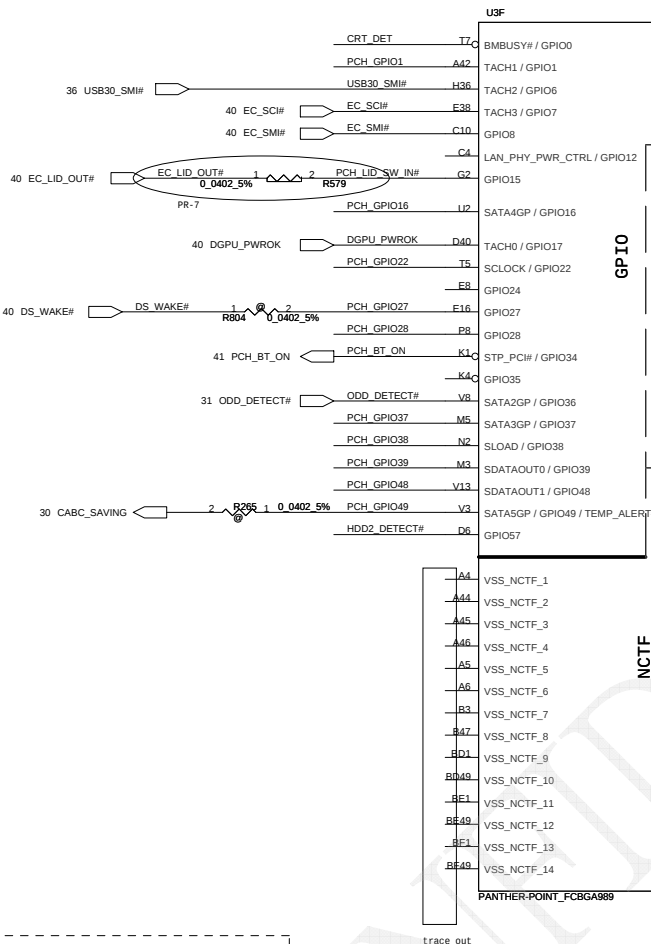
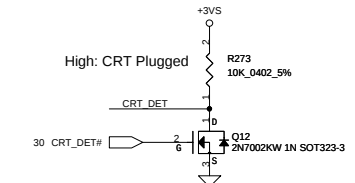
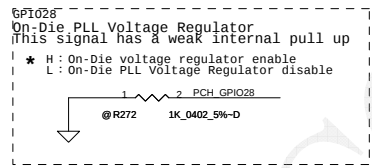
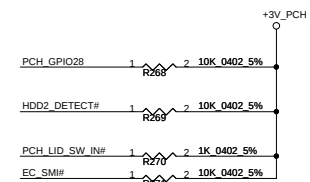
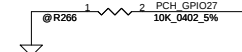
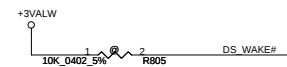
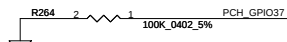
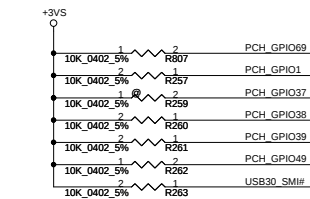
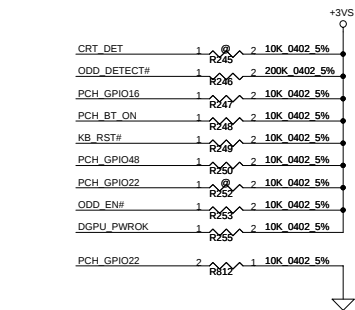




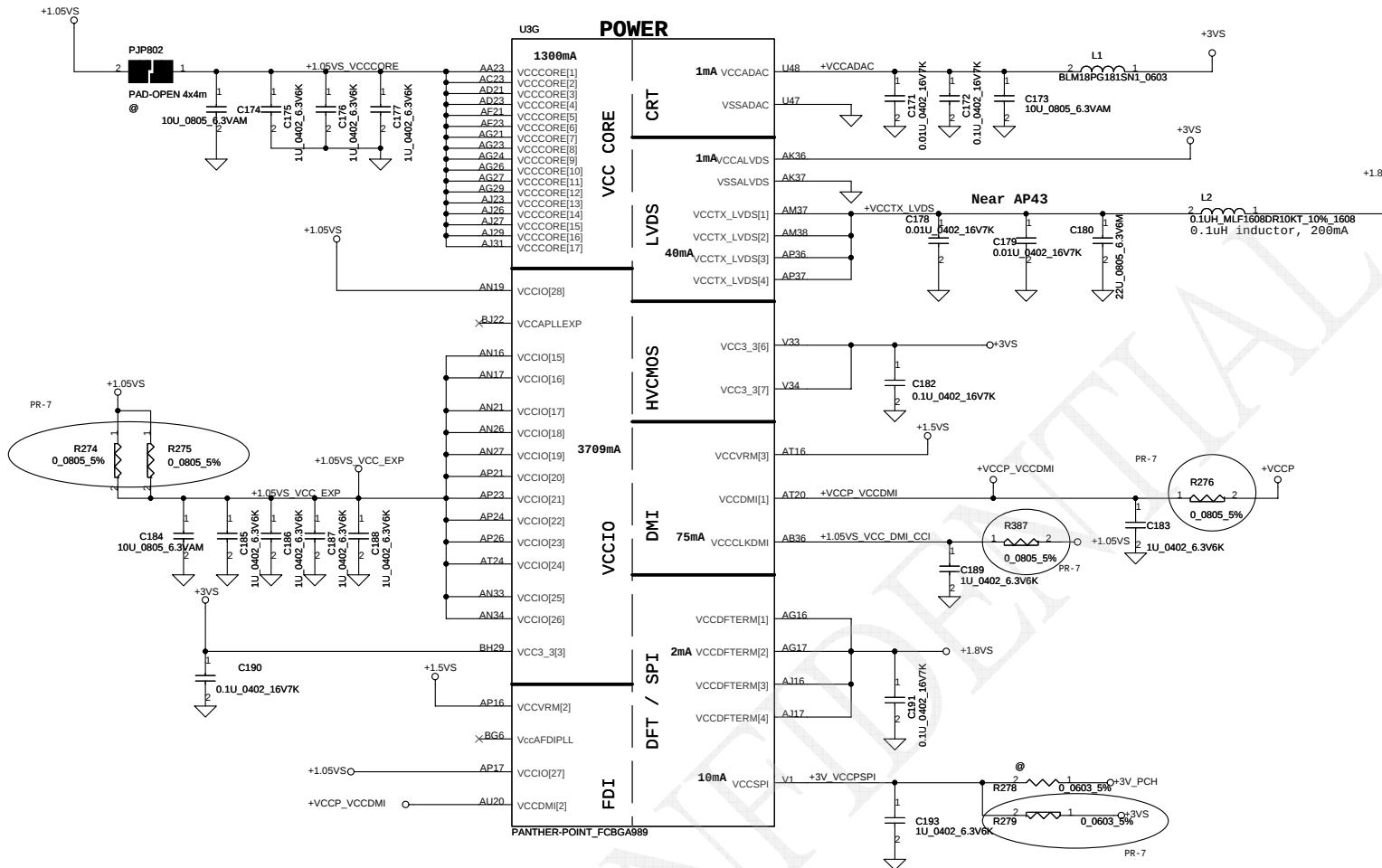


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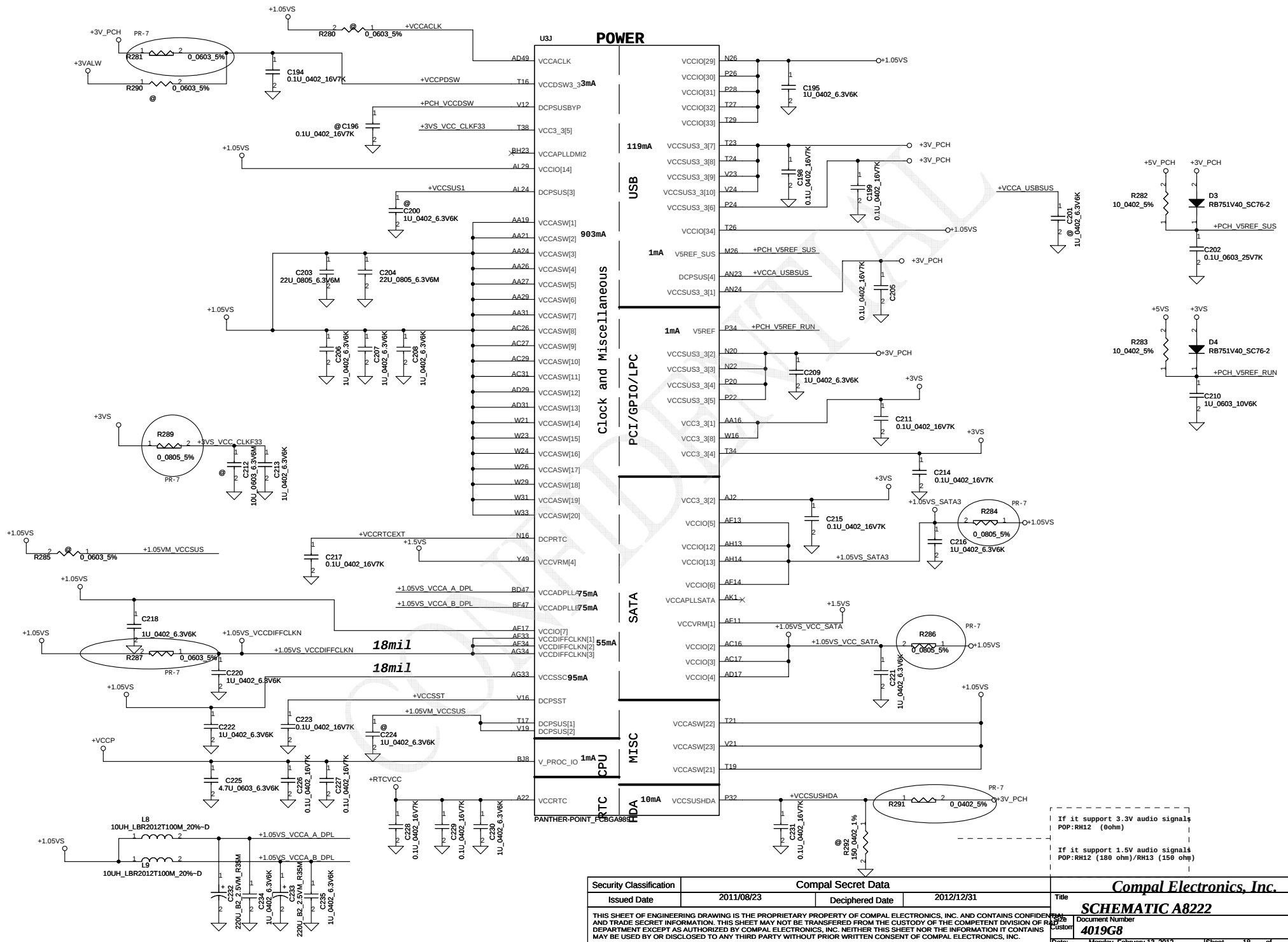


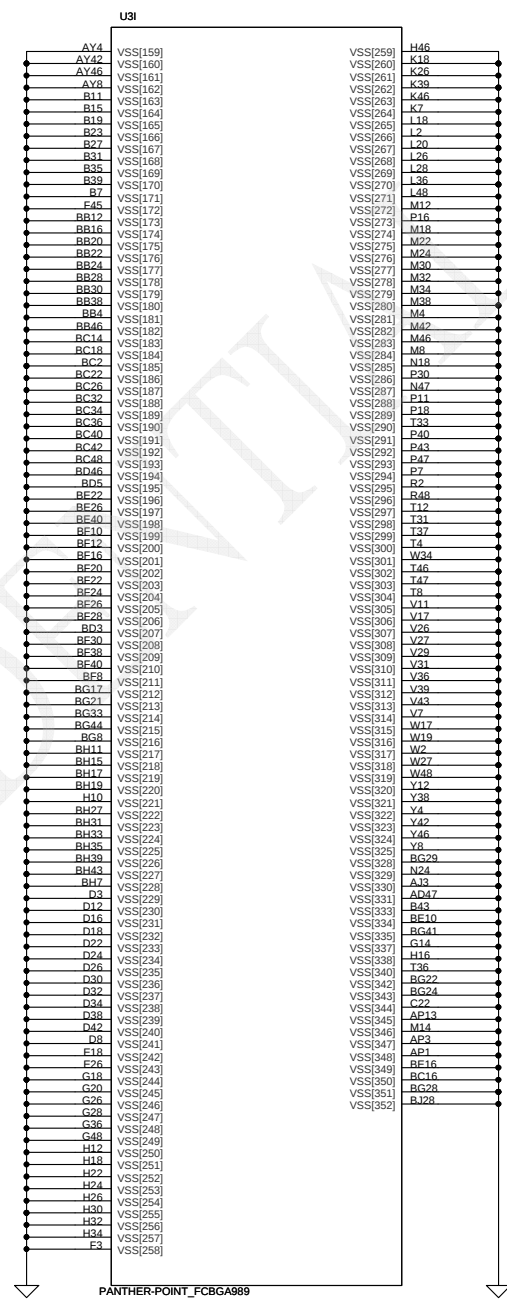
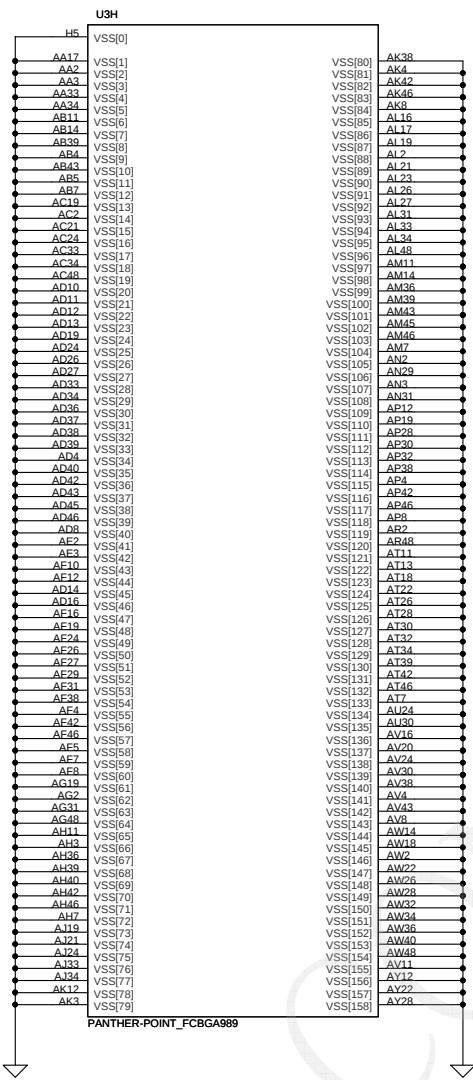


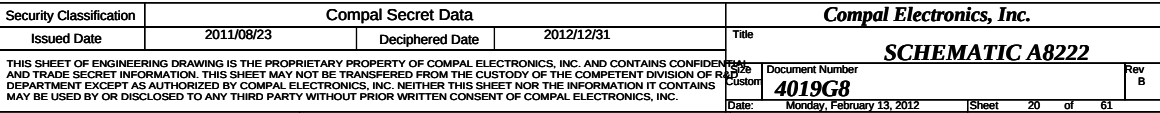
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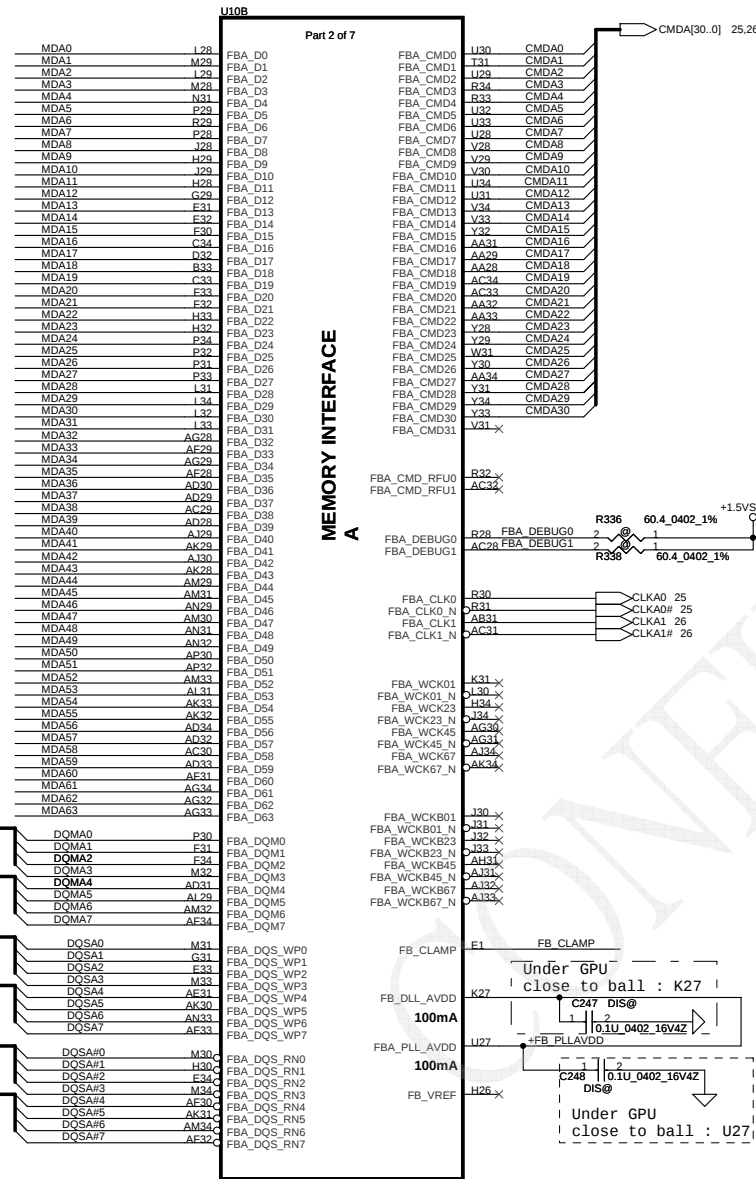
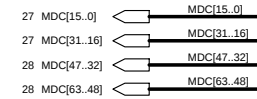
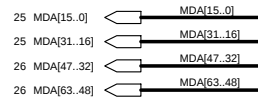
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_I0	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLb	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



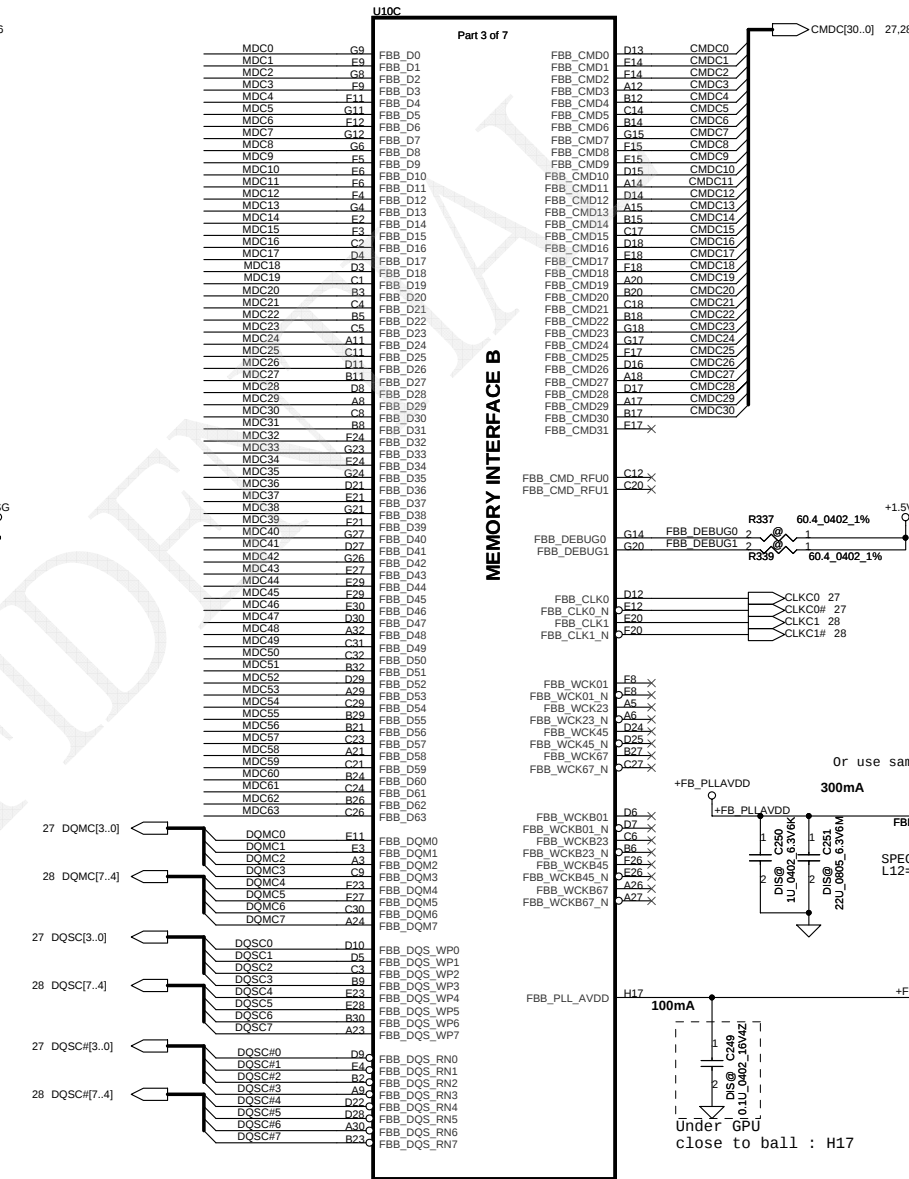
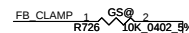




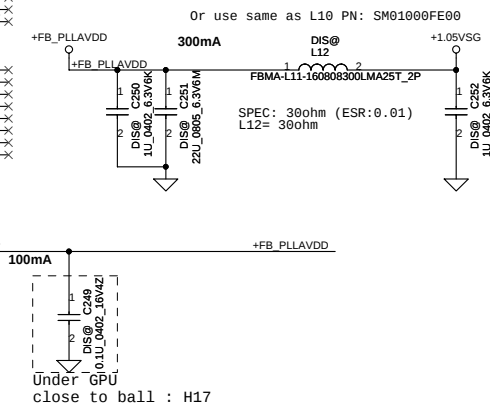
VRAM Interface



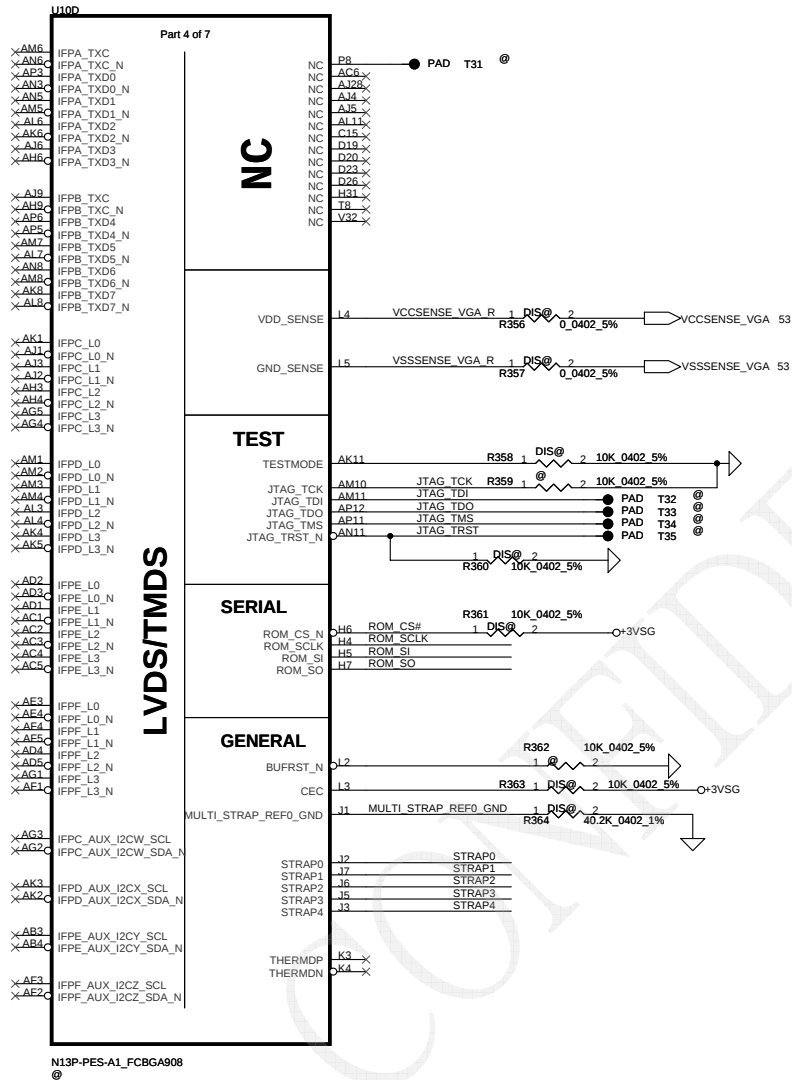
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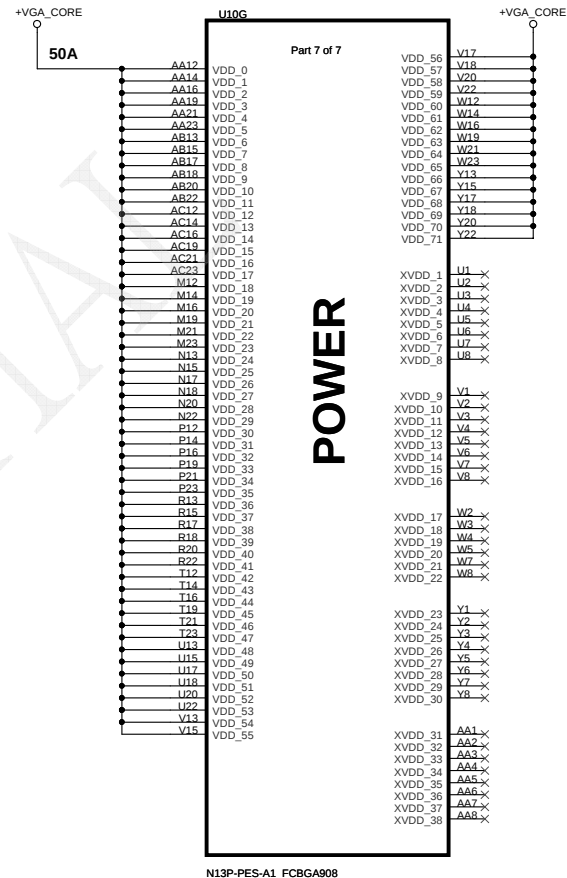
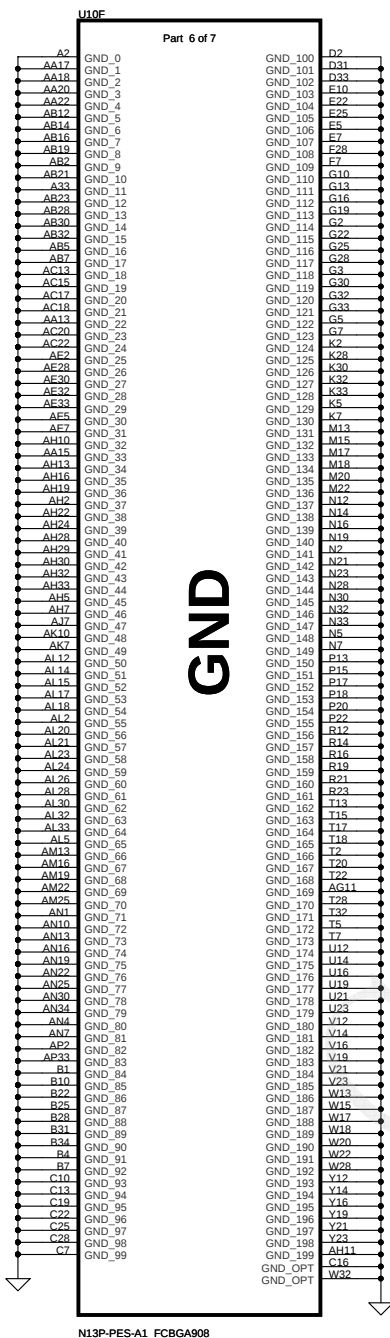


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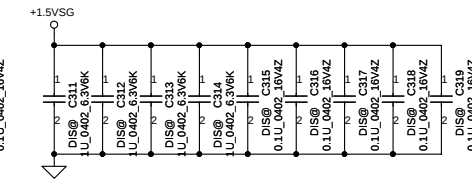
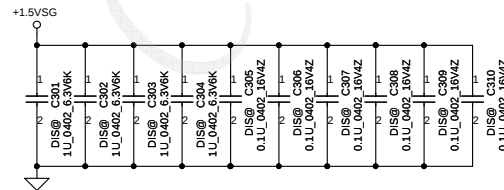
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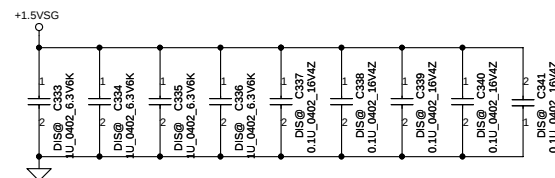
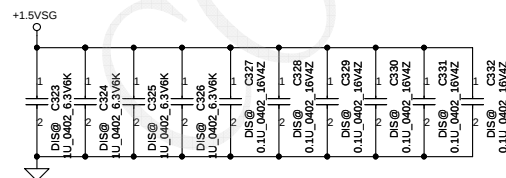
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

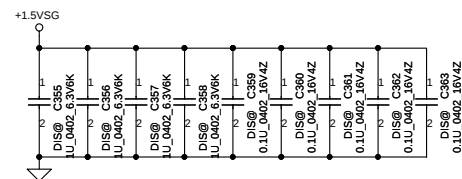
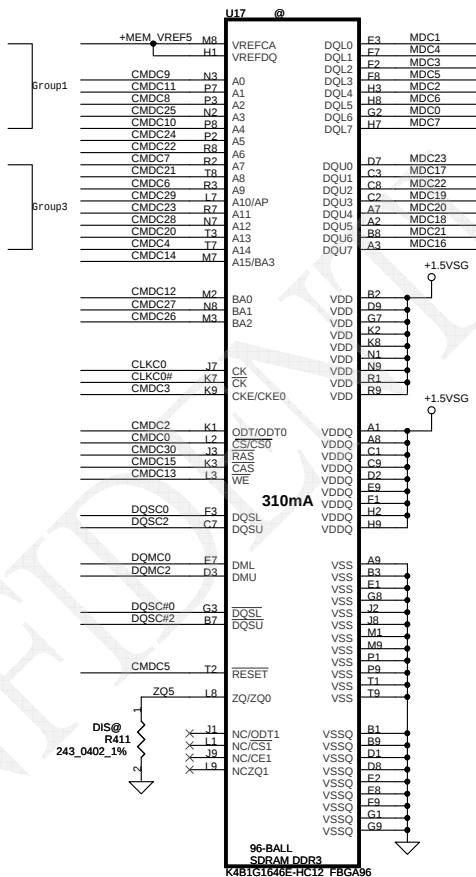
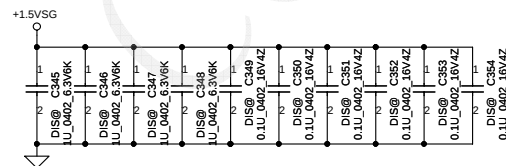
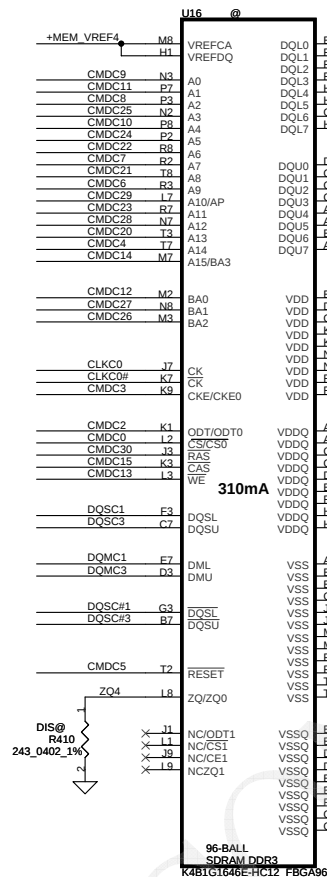
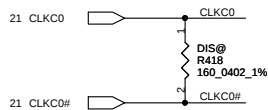
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

128Mx16 DDR3 *8==>2GB



LOW HIGH

128Mx16 DDR3 *8==>2GB



LOW HIGH

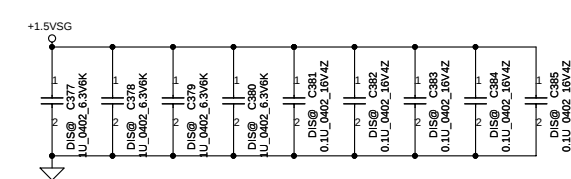
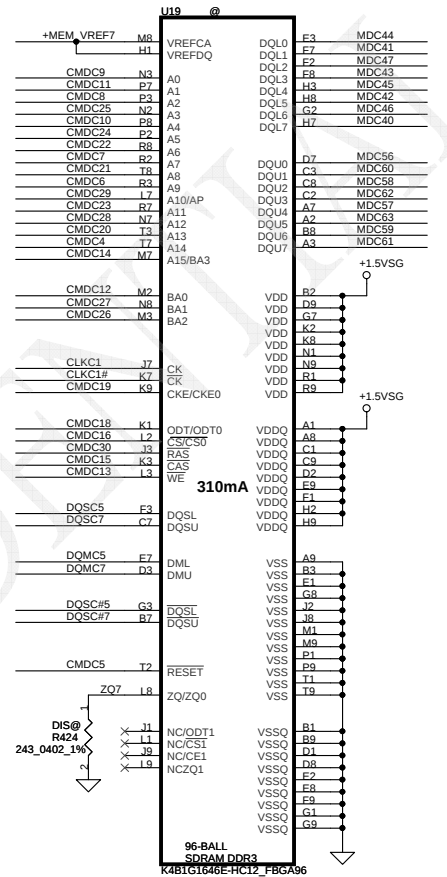
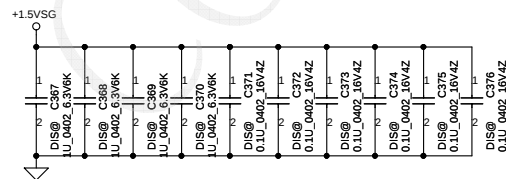
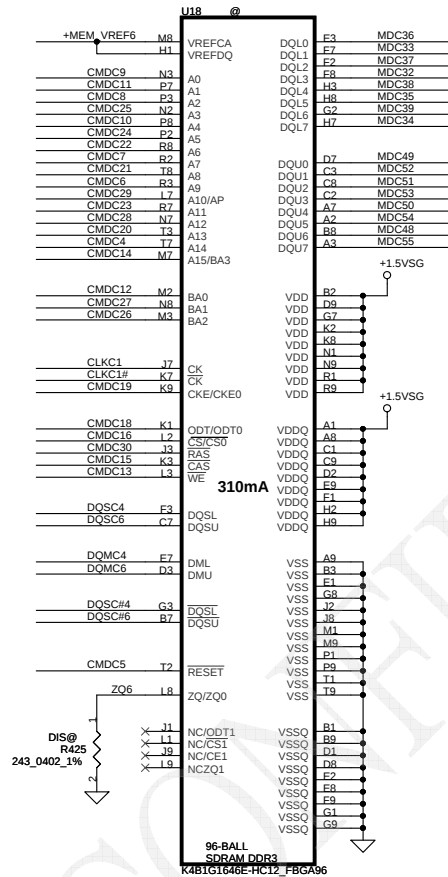
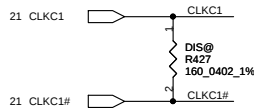
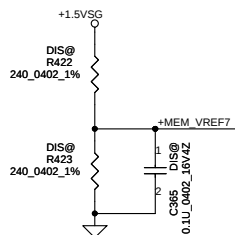
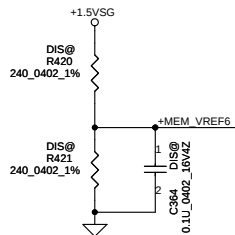
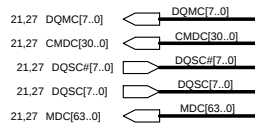
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

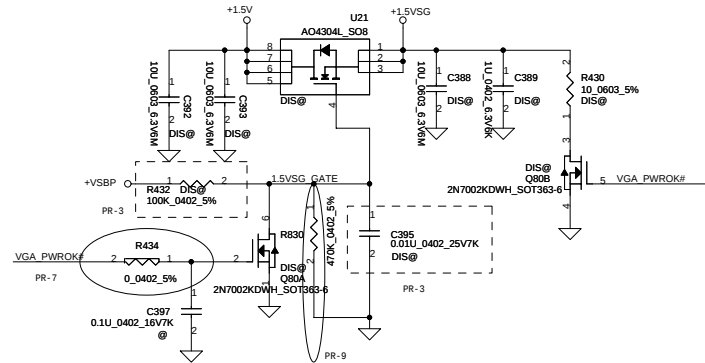


Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

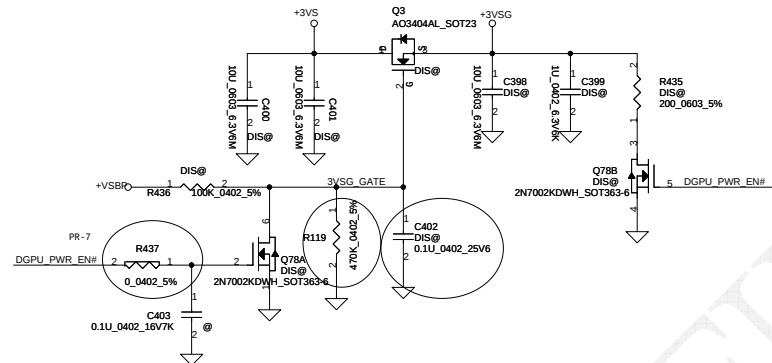
LOW HIGH

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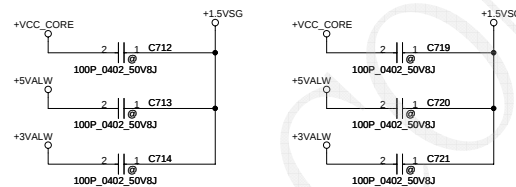
+1.5V to +1.5VSG



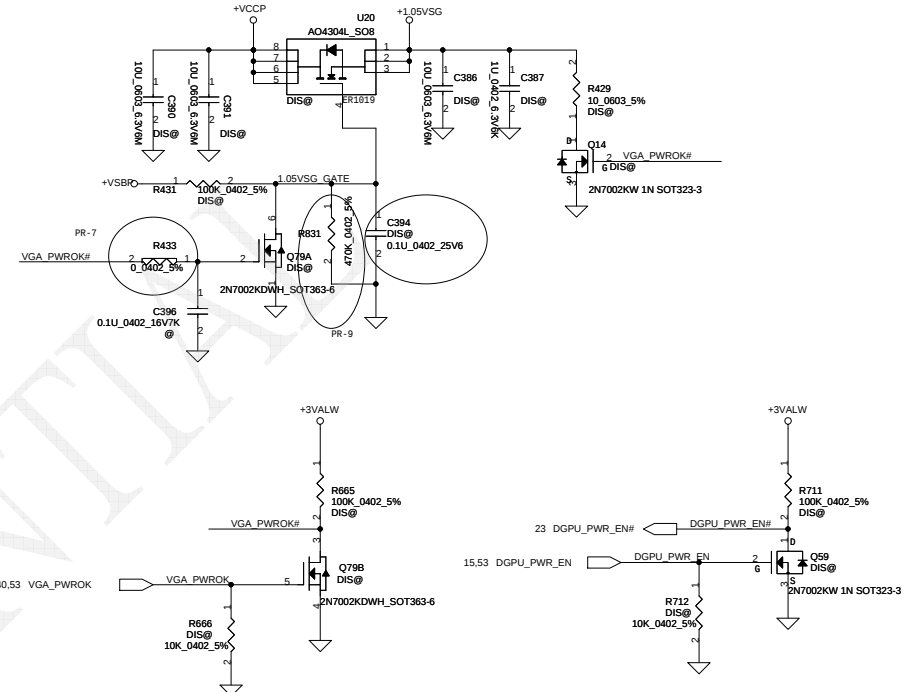
+3VS to +3VSG



For EMI

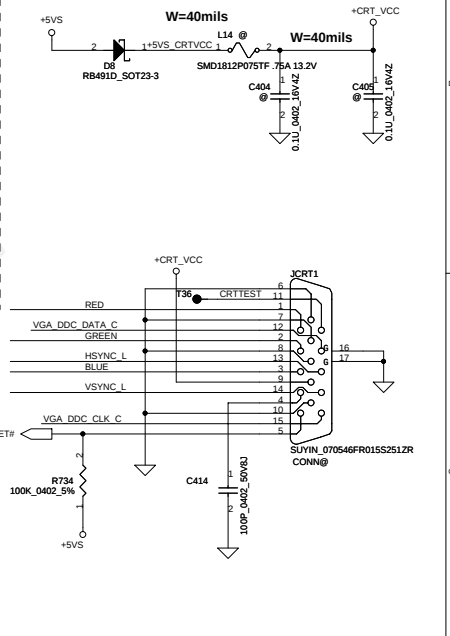
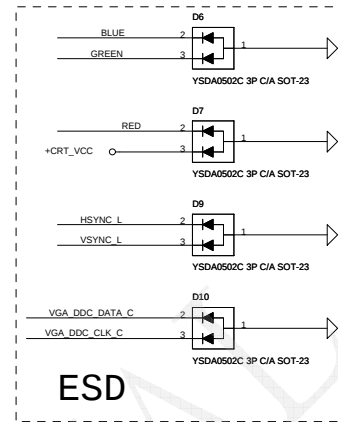
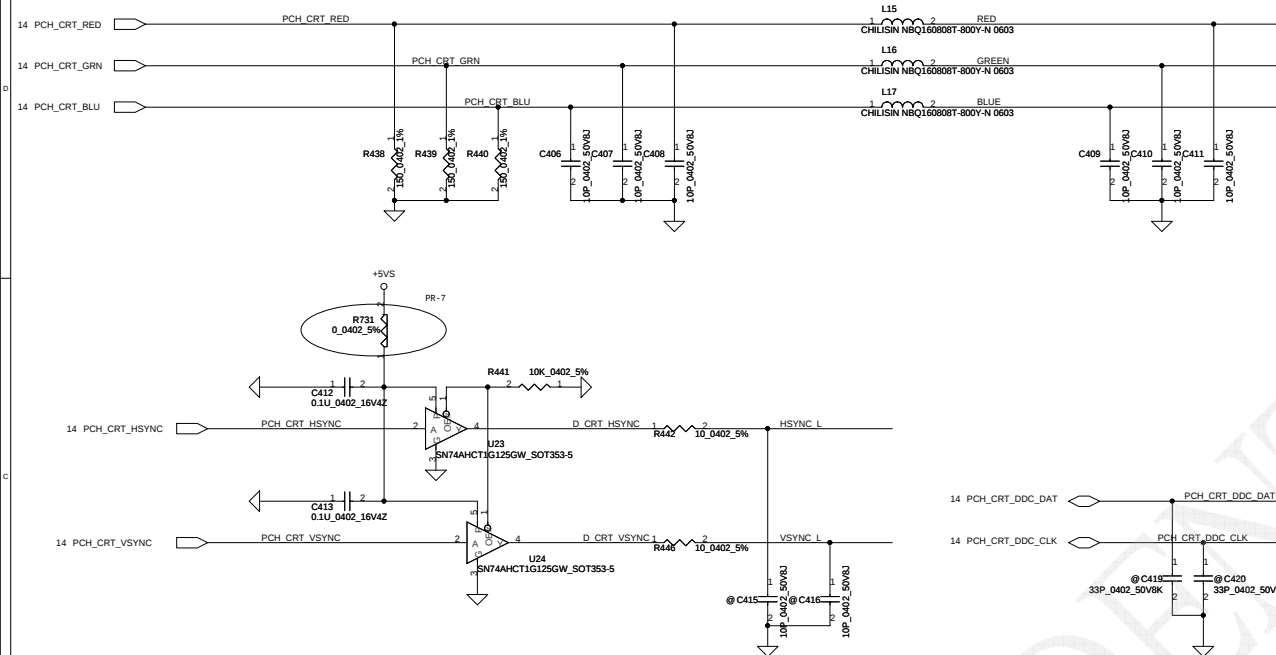


+VCCP to +1.05VSG

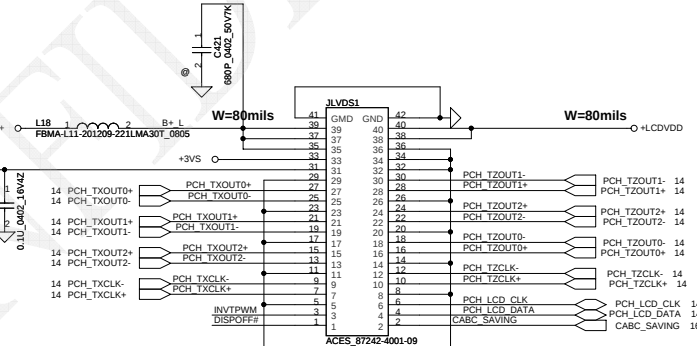
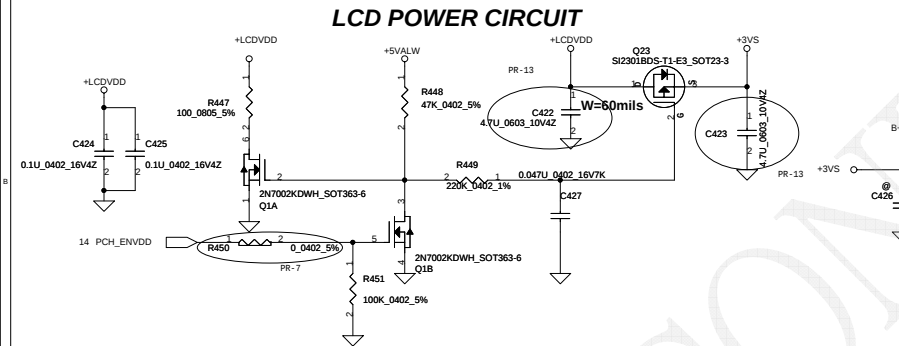


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				Custom	4019G8	B
				Date:	Monday, February 13, 2012	Sheet 29 of 61

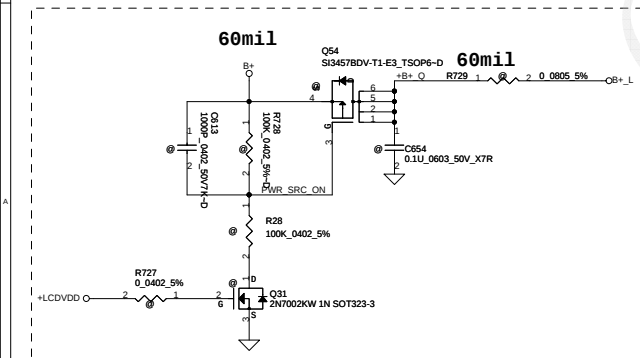
CRT



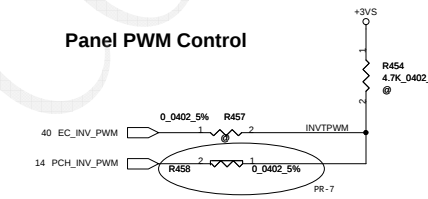
LCD POWER CIRCUIT



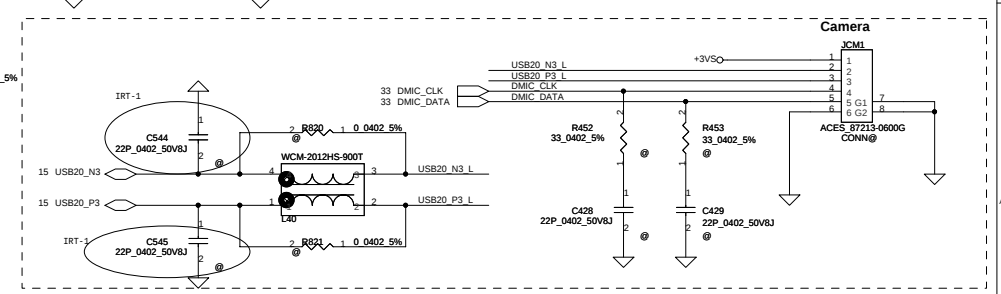
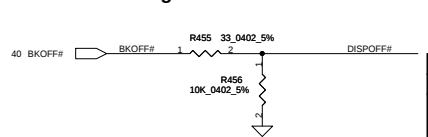
60mil



Panel PWM Control

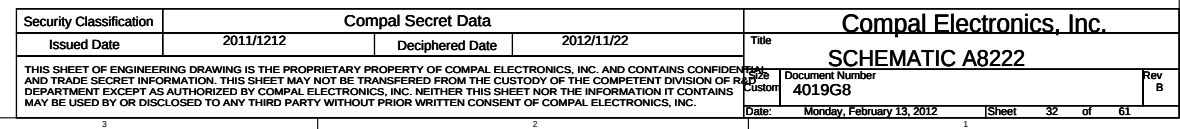
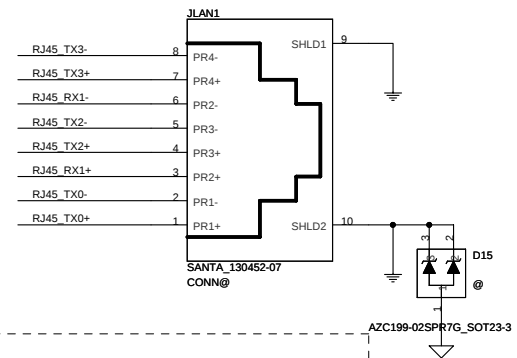
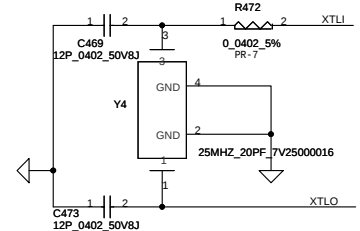
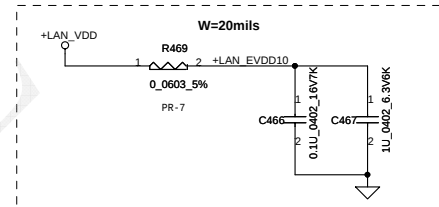


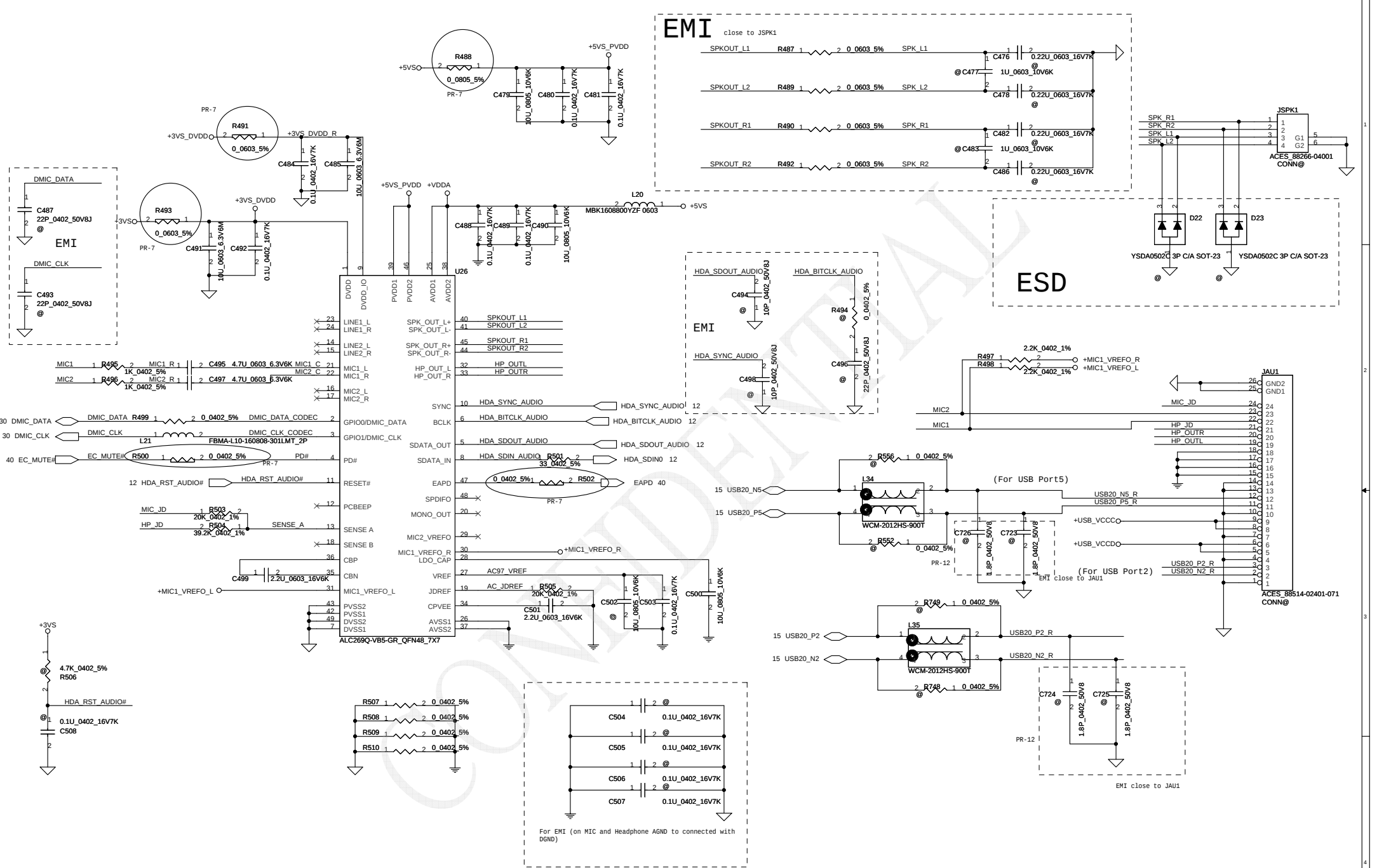
Panel Backlight Control



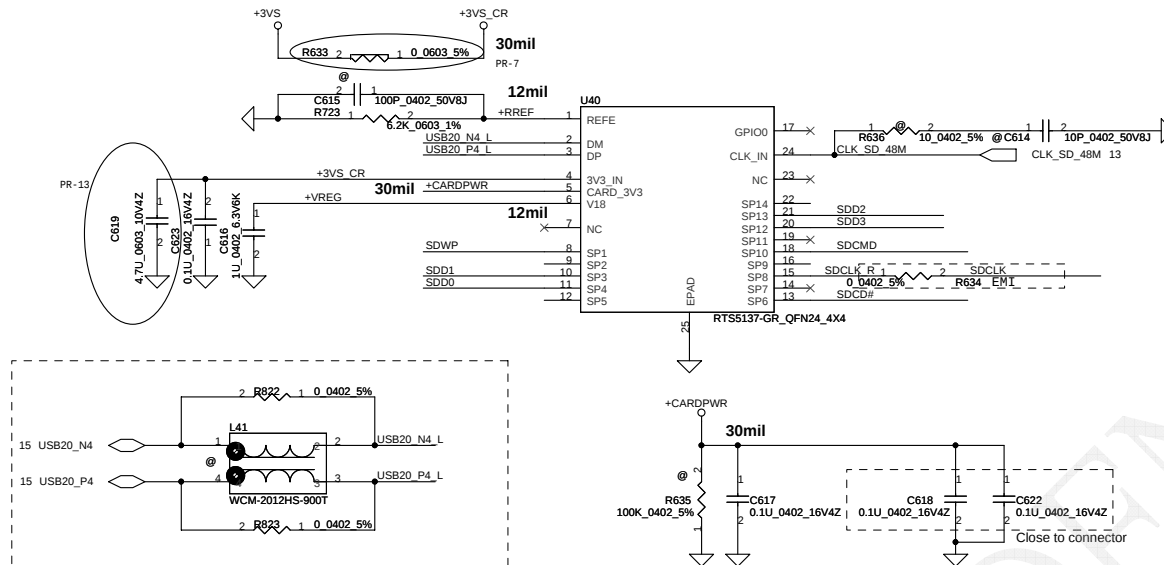
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Issued Date		Deciphered Date		SCHEMATIC A8222	
2011/08/23		2012/12/31		4019G8	
Size		Document Number		Rev B	
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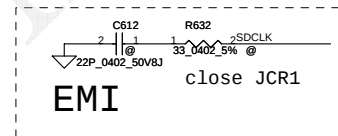
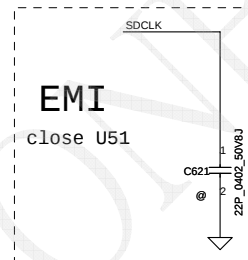
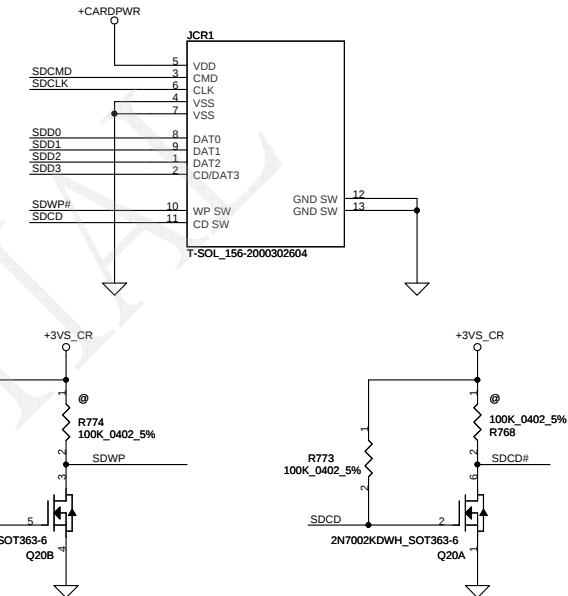




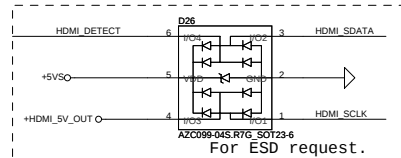
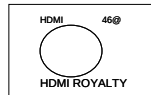
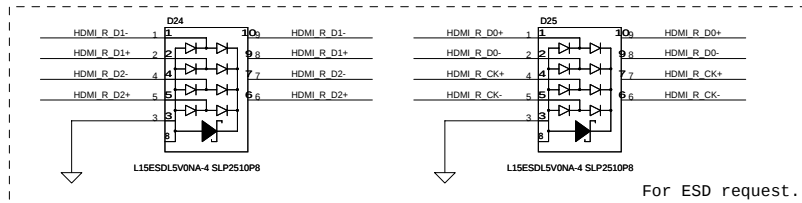
Card Reader RTS5137 (only SD/MMC/MS function)



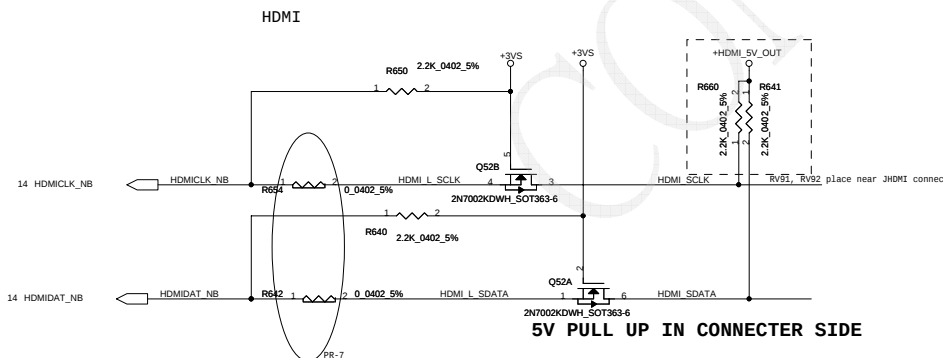
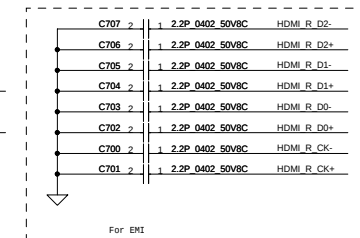
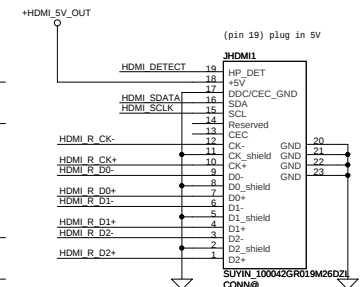
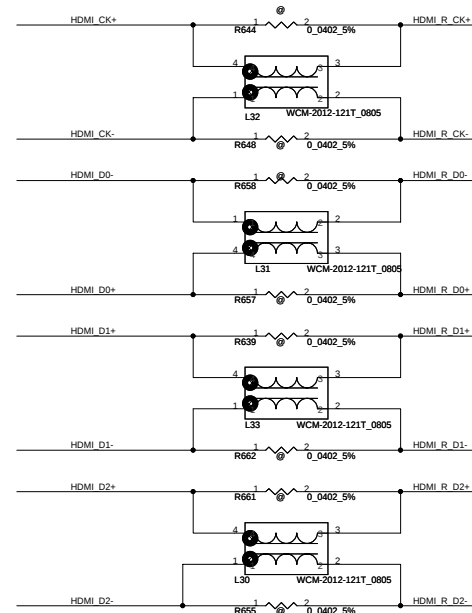
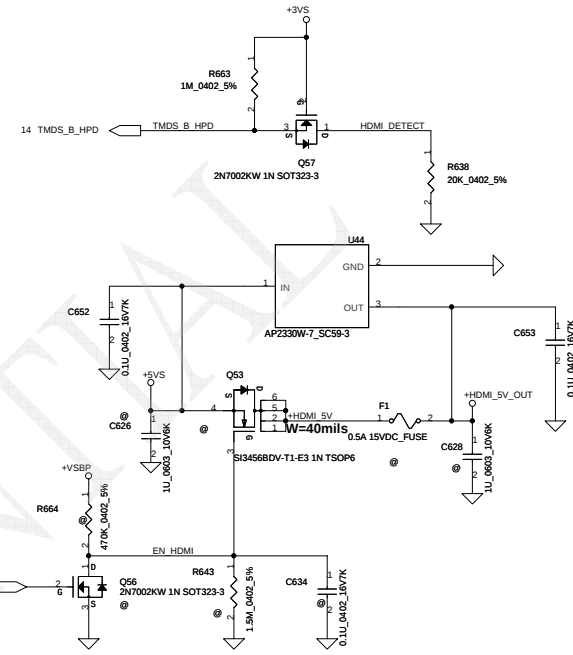
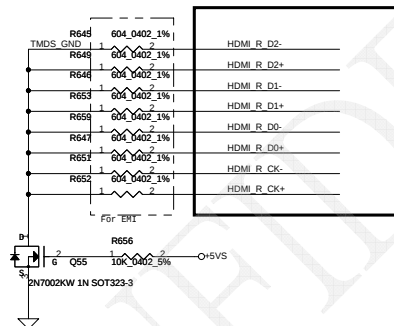
Card Reader Connector



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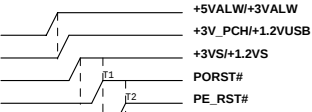
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14	TMDS_B_CLK#	0.1U 0402 18V7K	2	1	C625 HDMI CK-
	TMDS_B_DATA0	0.1U 0402 18V7K	2	1	C624
14	TMDS_B_DATA0#	0.1U 0402 18V7K	2	1	C630 HDMI D0+
	TMDS_B_DATA1	0.1U 0402 18V7K	2	1	C631
14	TMDS_B_DATA1#	0.1U 0402 18V7K	2	1	C633 HDMI D1+
	TMDS_B_DATA2	0.1U 0402 18V7K	2	1	C627
14	TMDS_B_DATA2#	0.1U 0402 18V7K	2	1	C629 HDMI D2+
	TMDS_B_DATA3	0.1U 0402 18V7K	2	1	C632



	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

Power Sequence

ASM1042



T1: 2-80ms
T2: >200ms

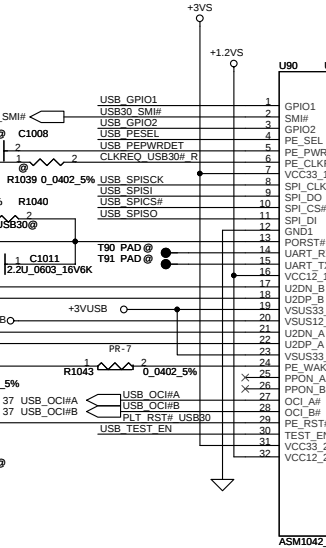
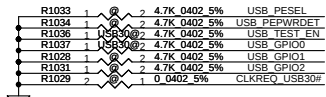
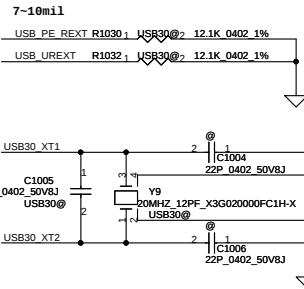
For WAKE Function

USB_PEPWRDET

	R1034	R1022
S1	Mount	@
* S3	@	Mount

USB_PESL

	R1033
* Other application	@
Express Card/Mini Card	Mount



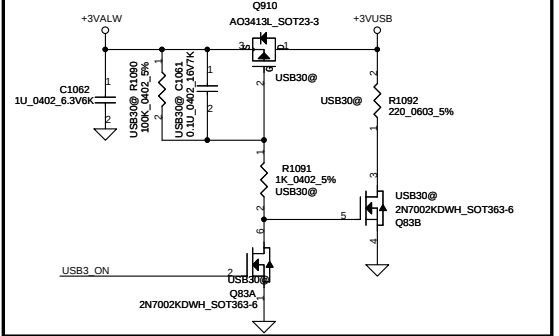
ASM1042
(TQFN 64)

ASM1042_TQFN64_9x9

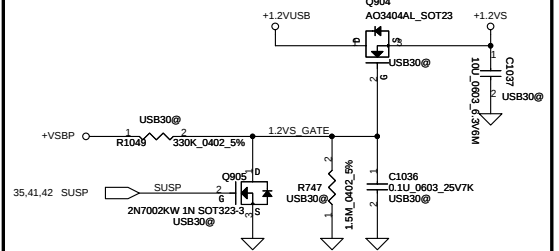
Close to ASM1042

EMC Caps C1045, C1046 should be placed at board(-8430.00 -3530.00)

PR-11

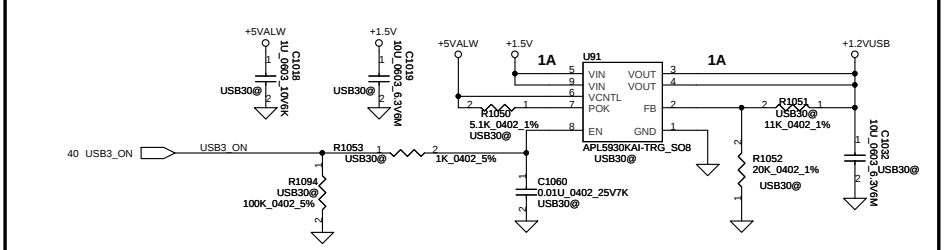


+1.2VUSB TO +1.2VS

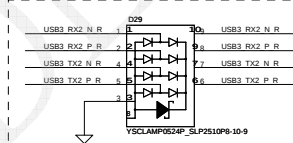
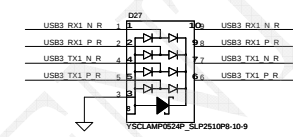
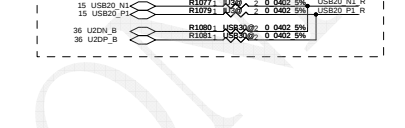
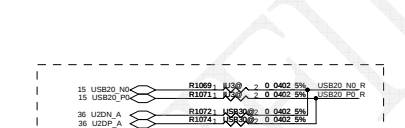
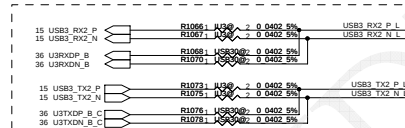
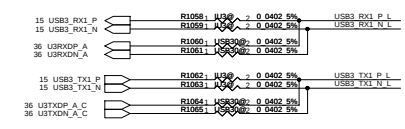
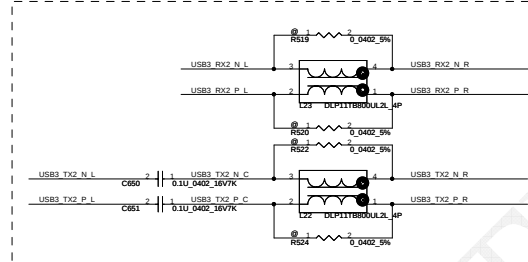
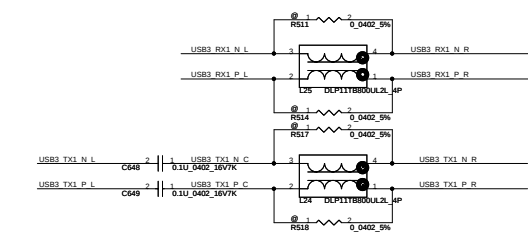
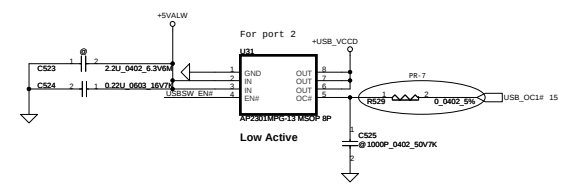
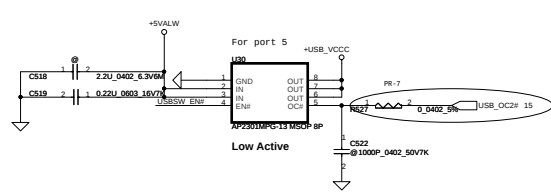
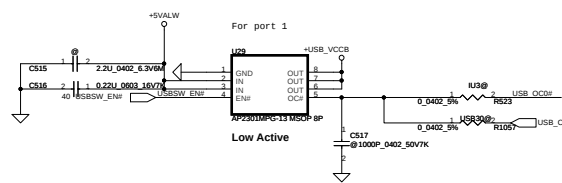
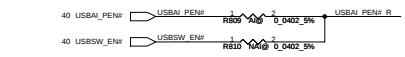
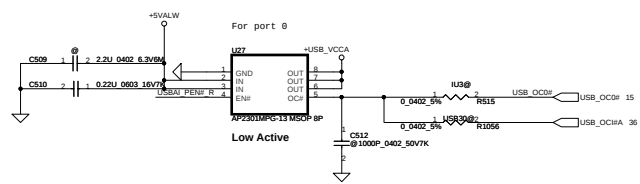


PR-11

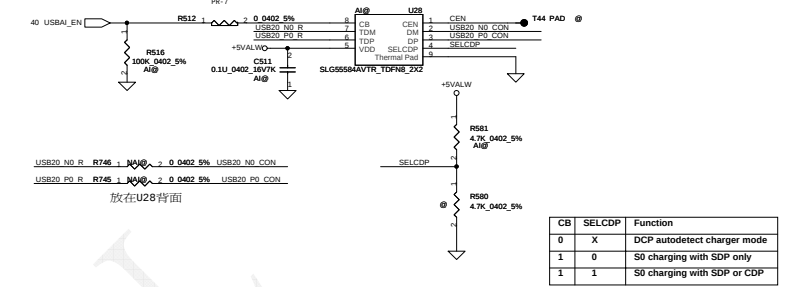
+1.5Vto +1.2VUSB Transfer



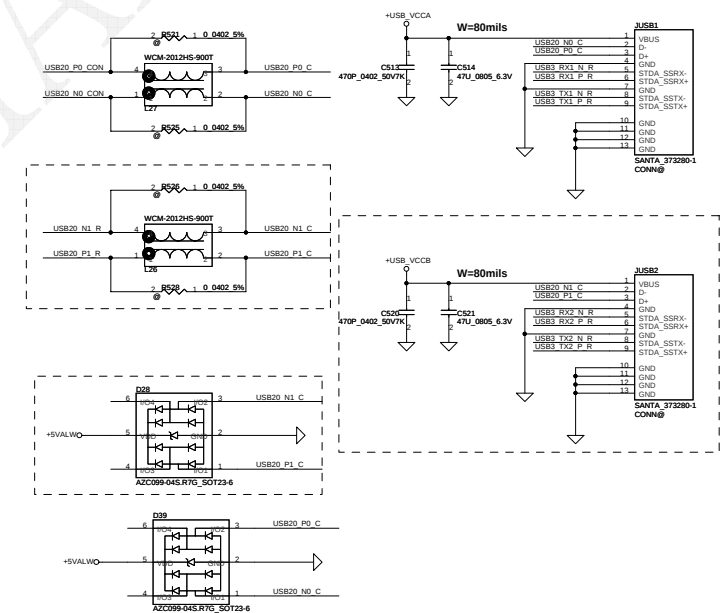
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AI CHARGER

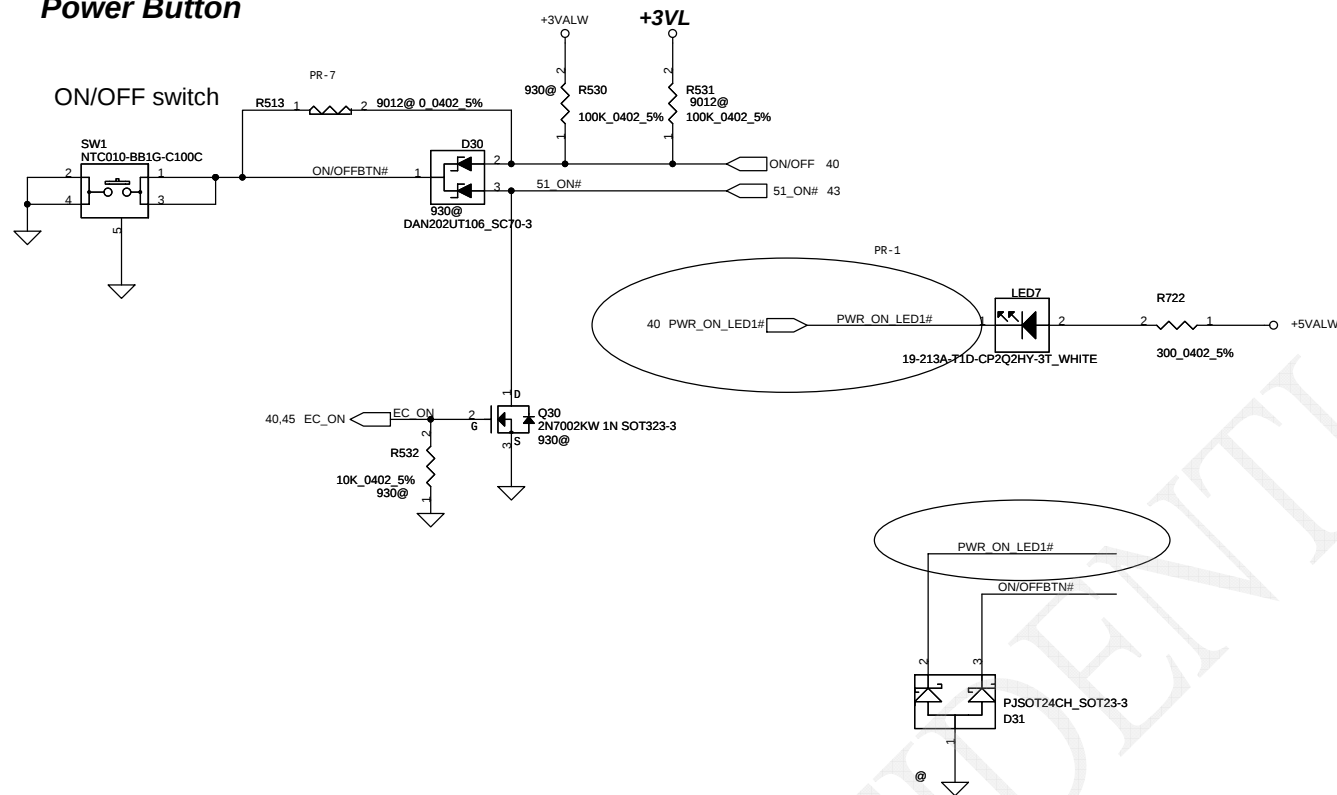


charger port: left side & near user

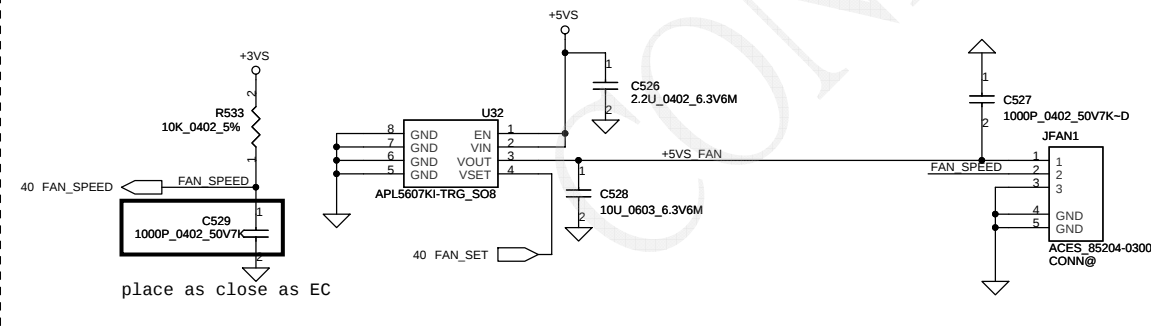


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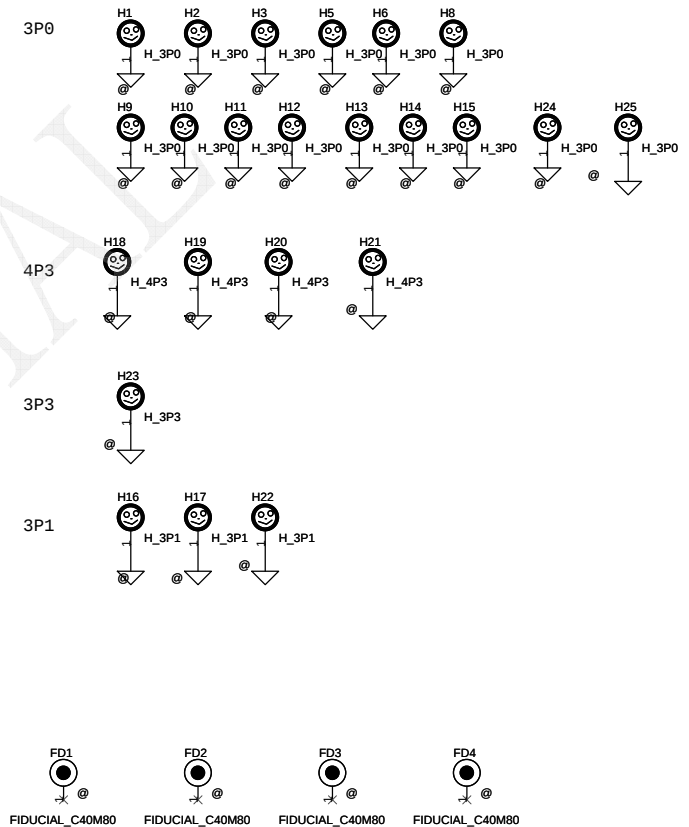
Power Button



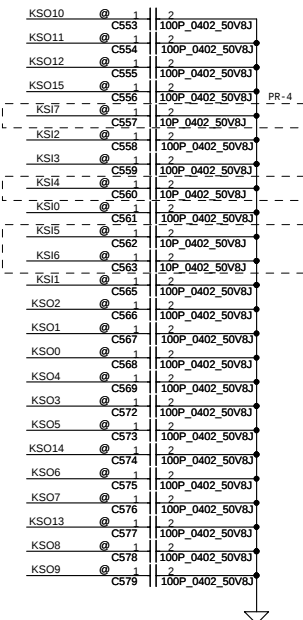
Fan Control Circuit



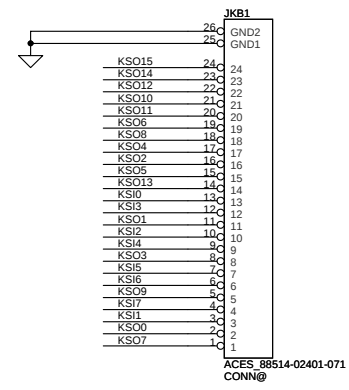
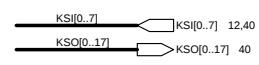
Screw Hole



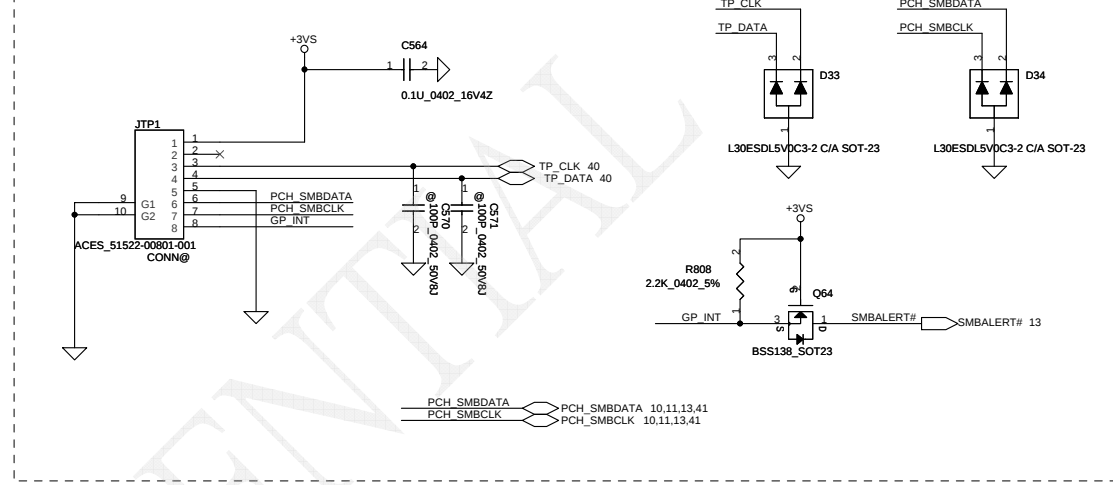
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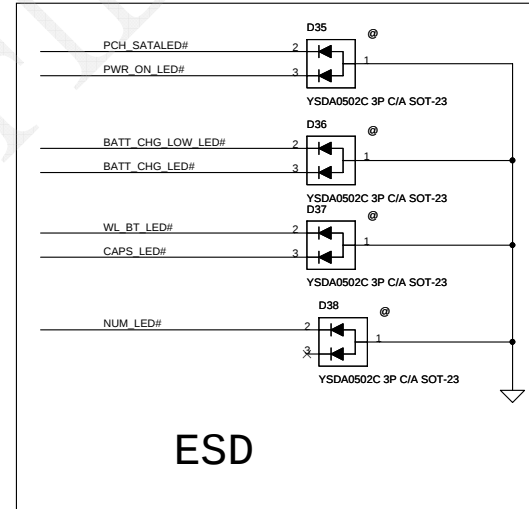
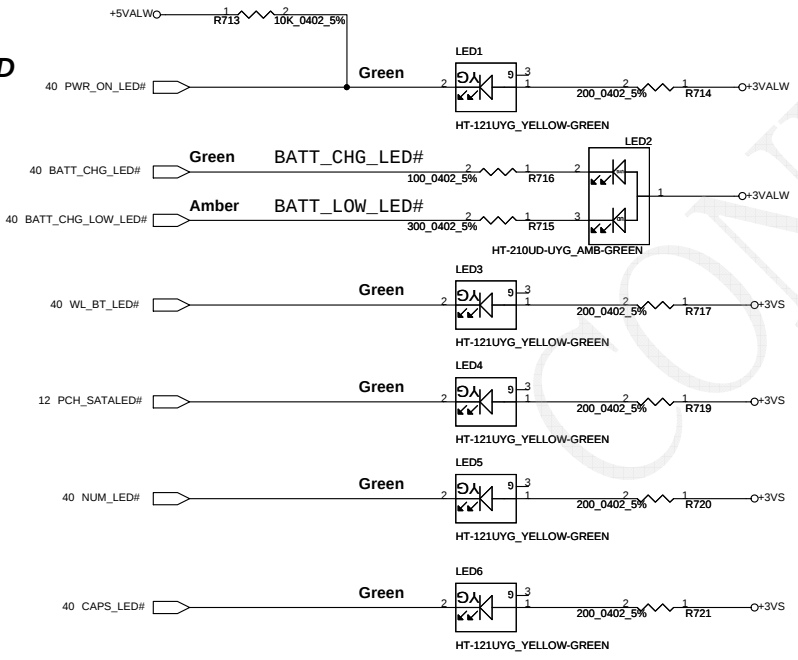
INT_KBD Conn.



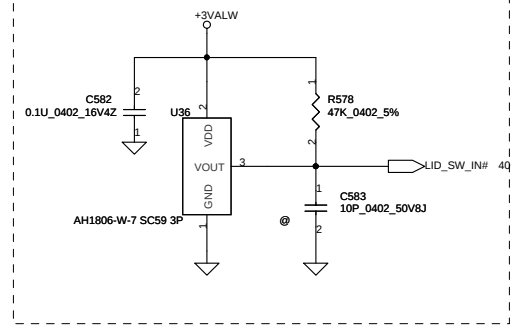
Touch/B Connector



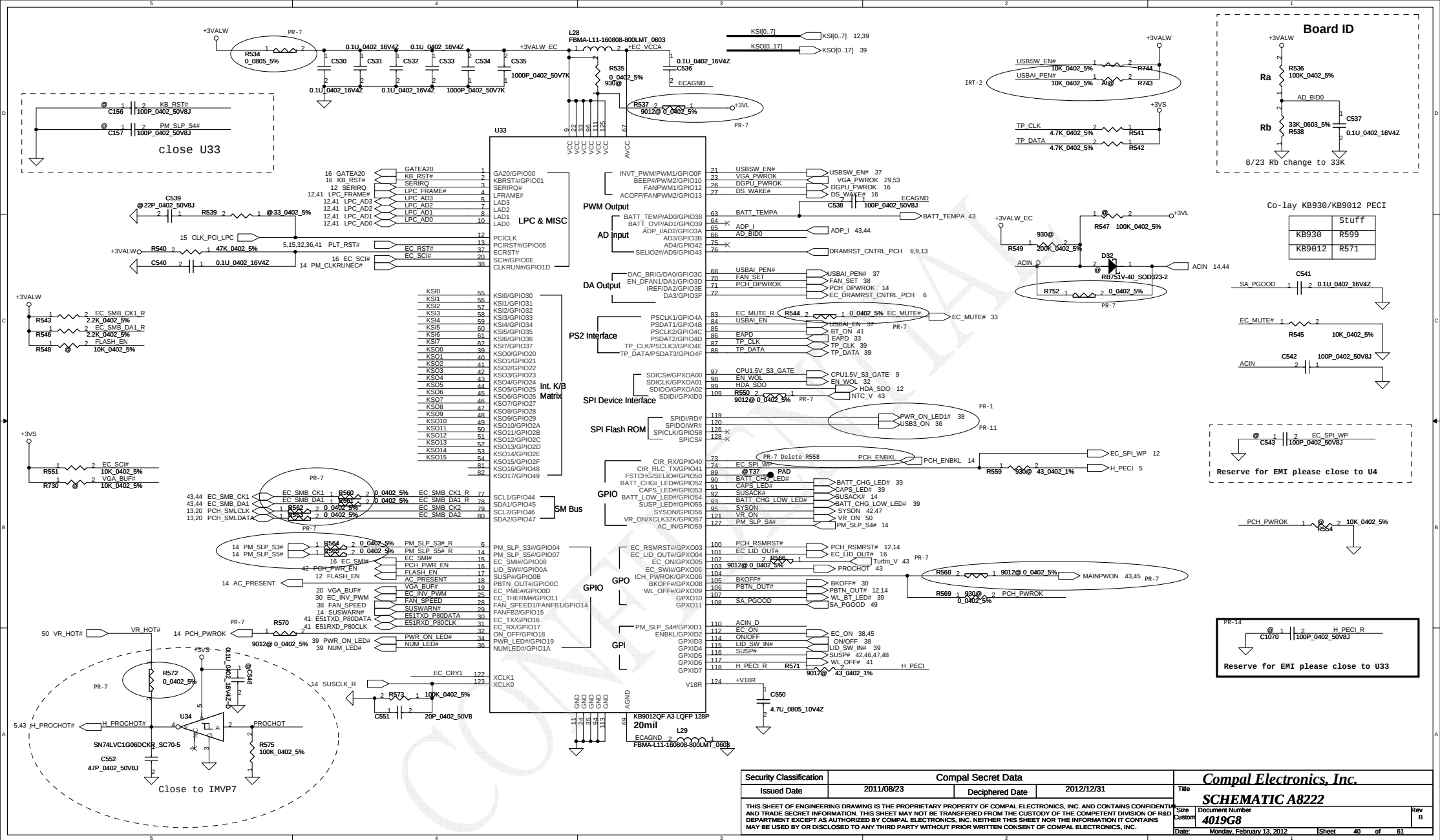
LED



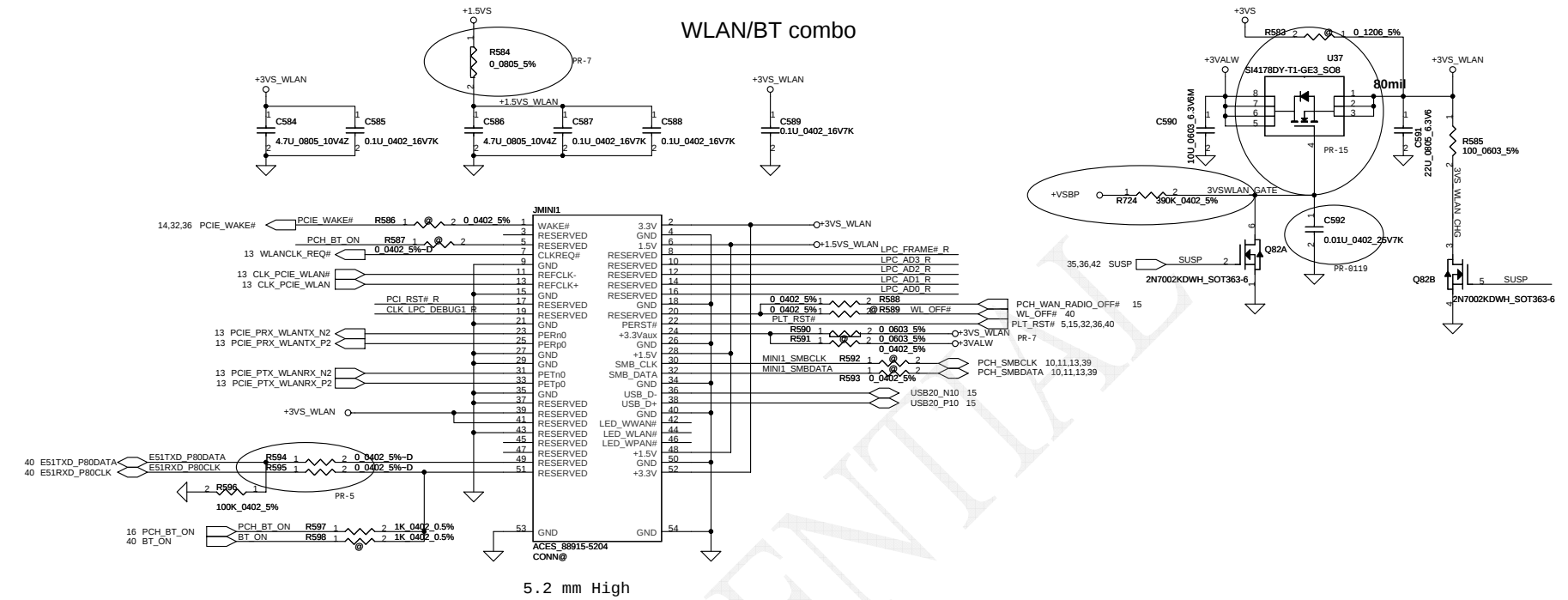
Lid Switch (Hall Effect Switch)



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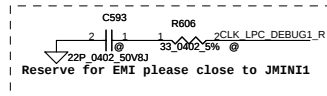


WLAN/BT combo



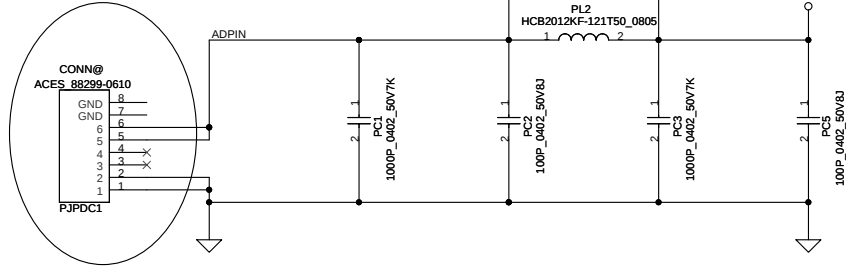
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R599	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME#	12.40
LPC_AD3 R	R600	1	2	0.0402 5%	LPC_AD3	LPC_AD3	12.40
LPC_AD2 R	R601	1	2	0.0402 5%	LPC_AD2	LPC_AD2	12.40
LPC_AD1 R	R602	1	2	0.0402 5%	LPC_AD1	LPC_AD1	12.40
LPC_AD0 R	R603	1	2	0.0402 5%	LPC_AD0	LPC_AD0	12.40
PCI_RST# R	R604	1	2	0.0402 5%	PLT_RST#	PLT_RST#	5.15,32,36,40
CLK_LPC_DEBUG1 R	R605	1	2	0.0402 5%	CLK_LPC_DEBUG1	CLK_LPC_DEBUG1	15

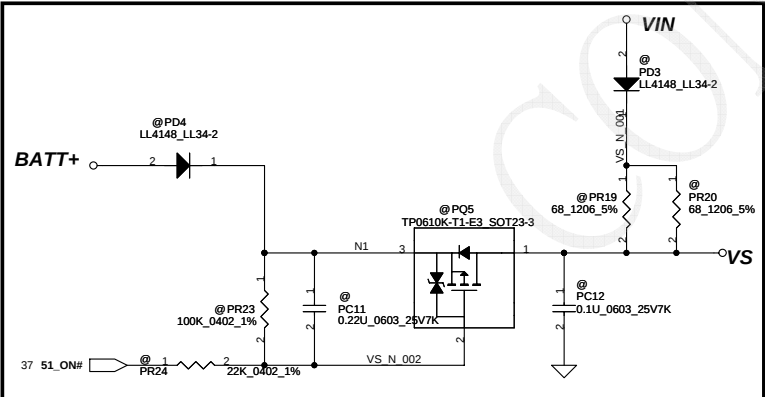
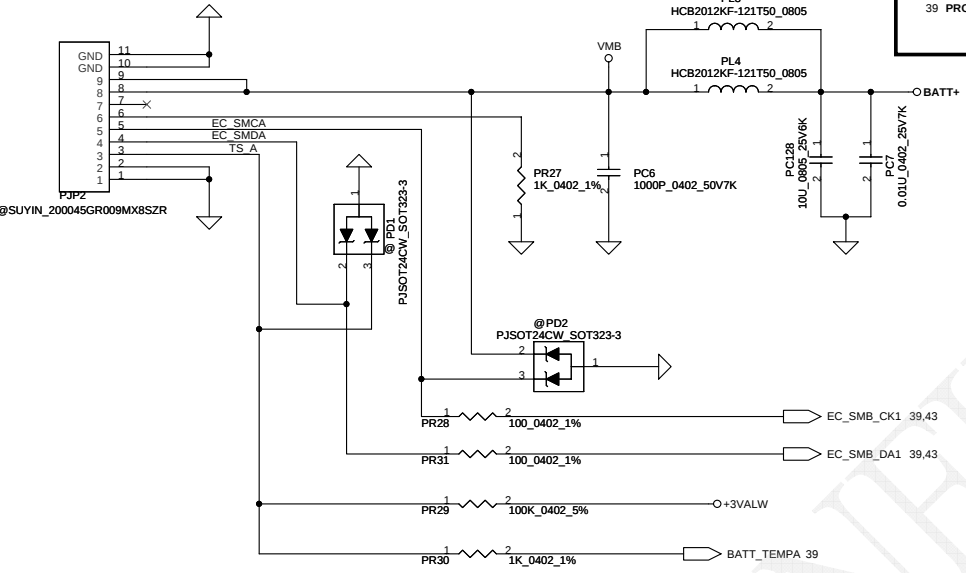


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DCIN jack P/N:SP02000N000,
need dble confirm P/N with ME

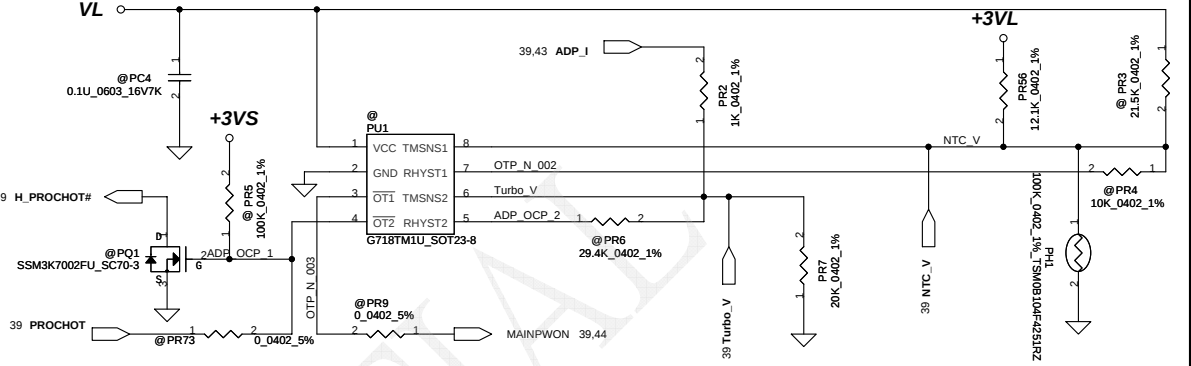


Change DC040007T0L to DC041112050

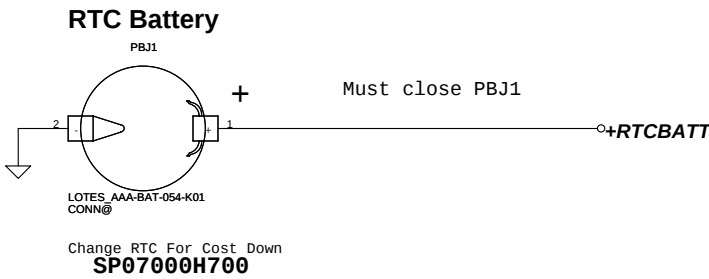
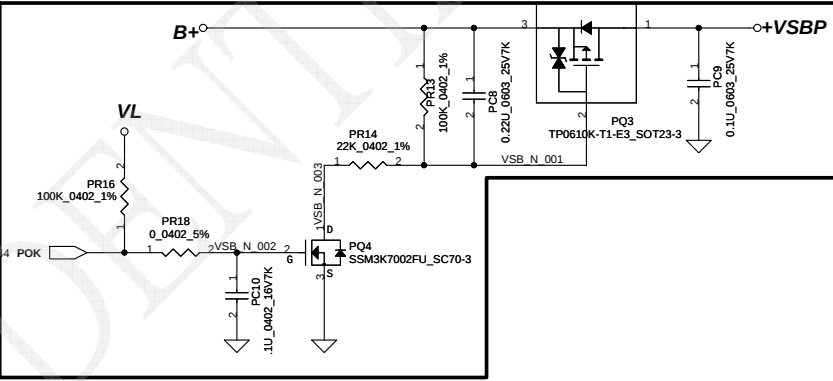


For KB9012 --> Remove all 51_ON# circuit

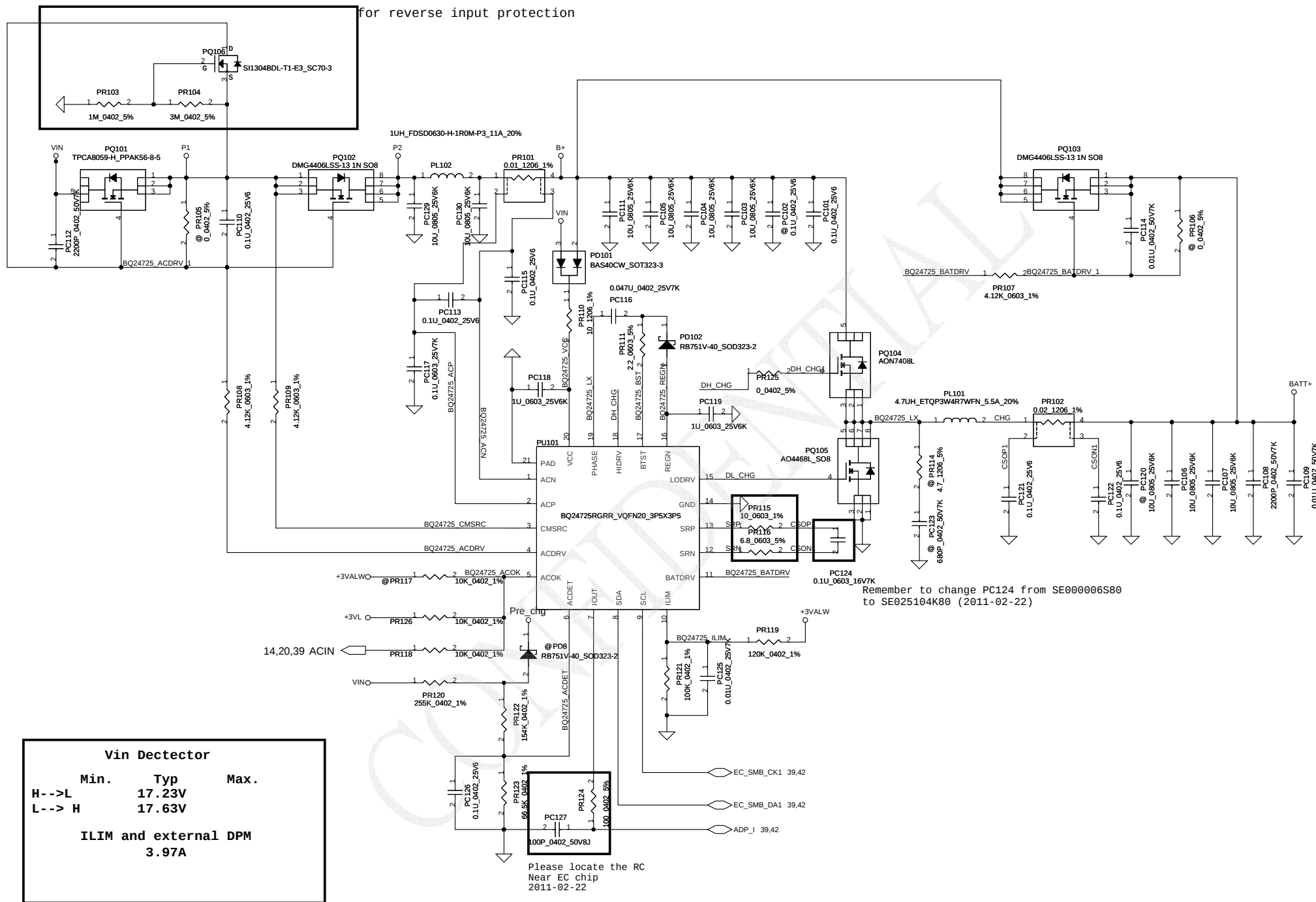
PH1 under CPU botten side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C

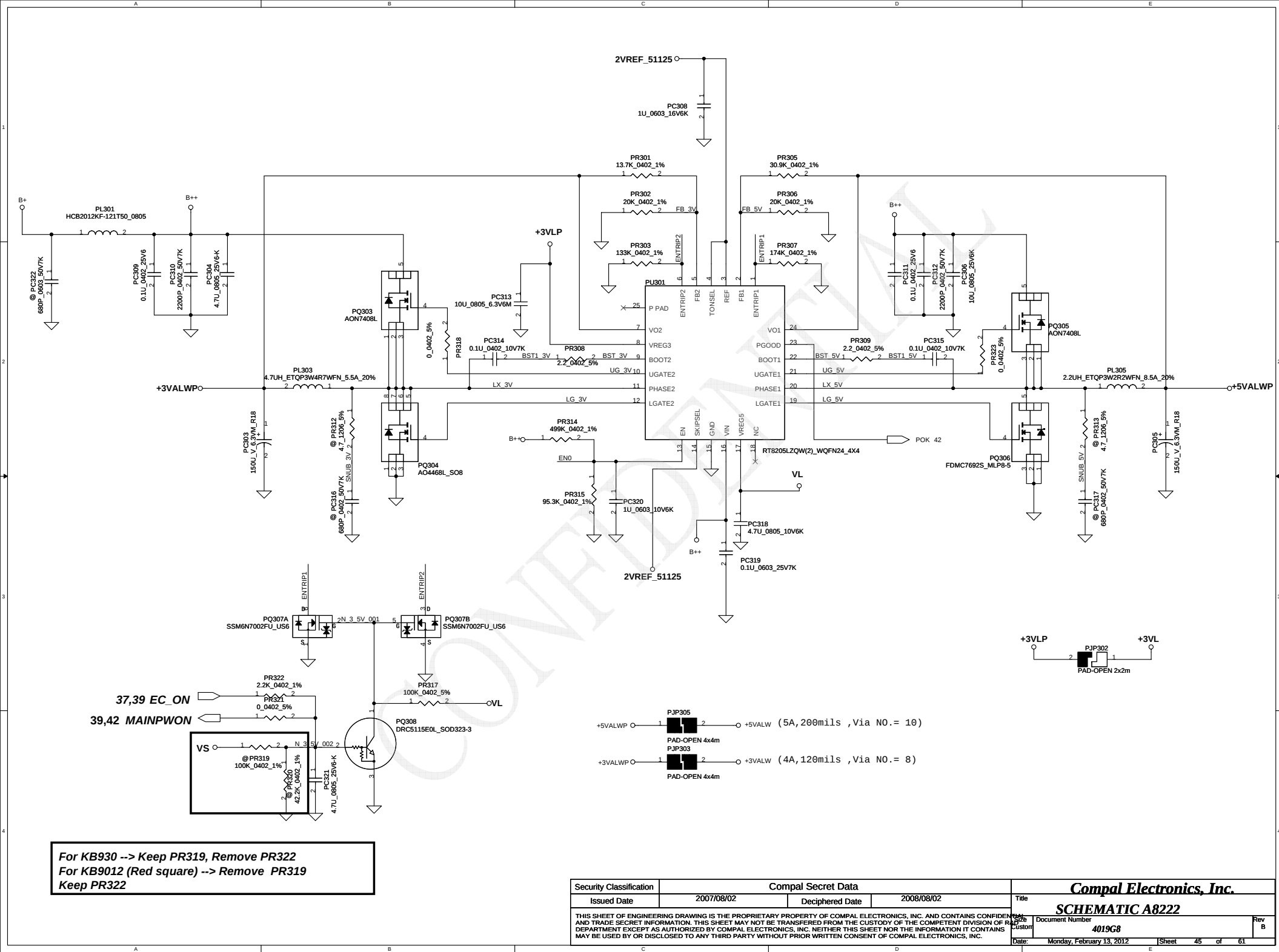


For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7, PQ15, PR73, PR56



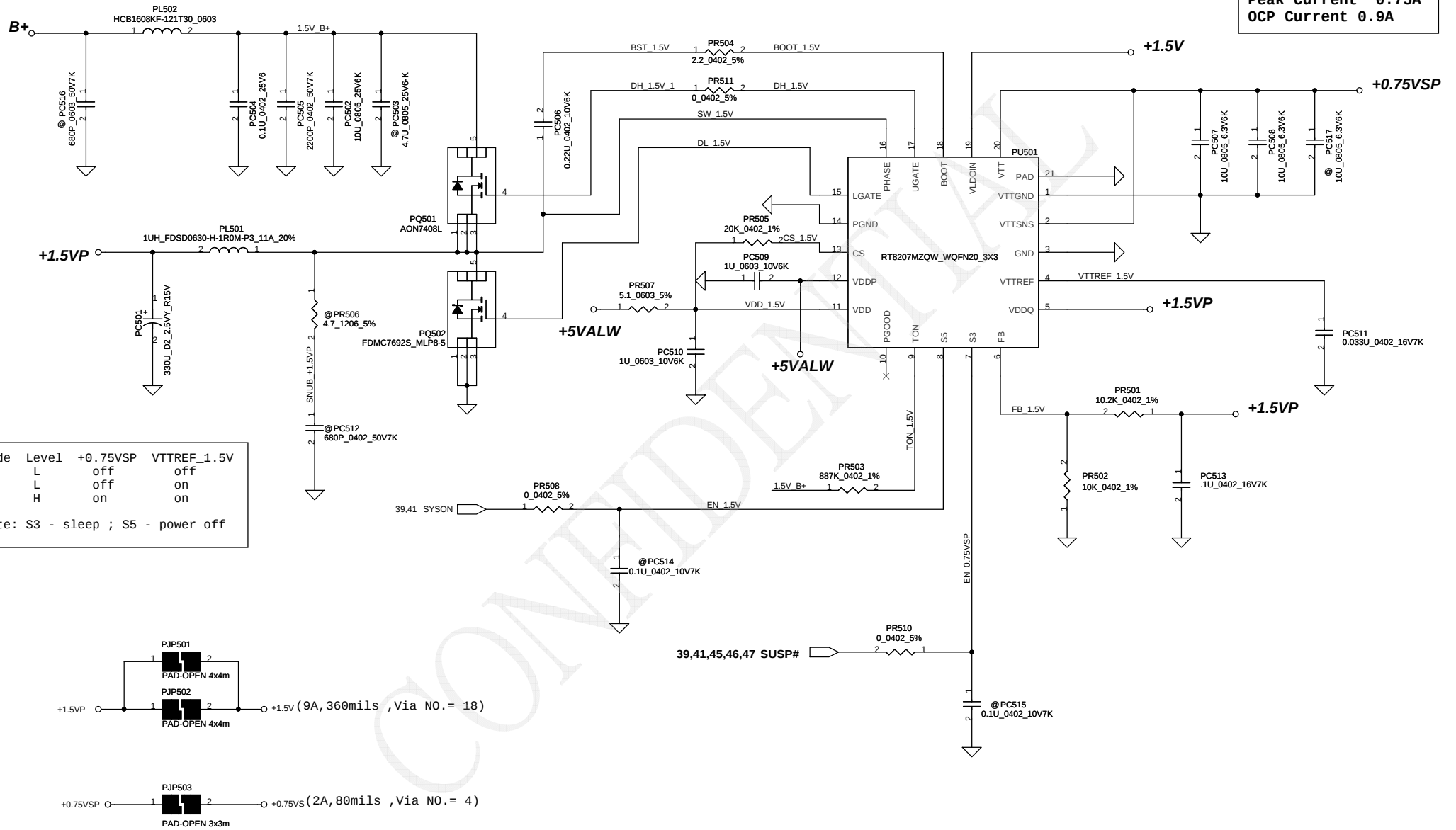
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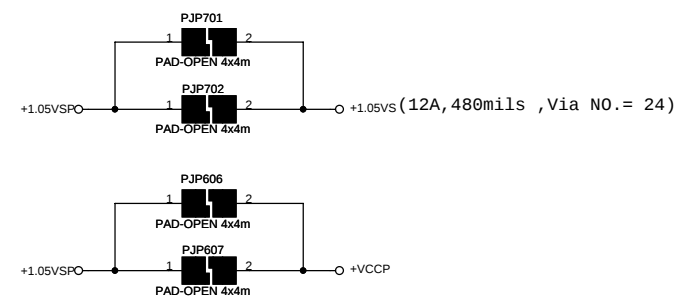
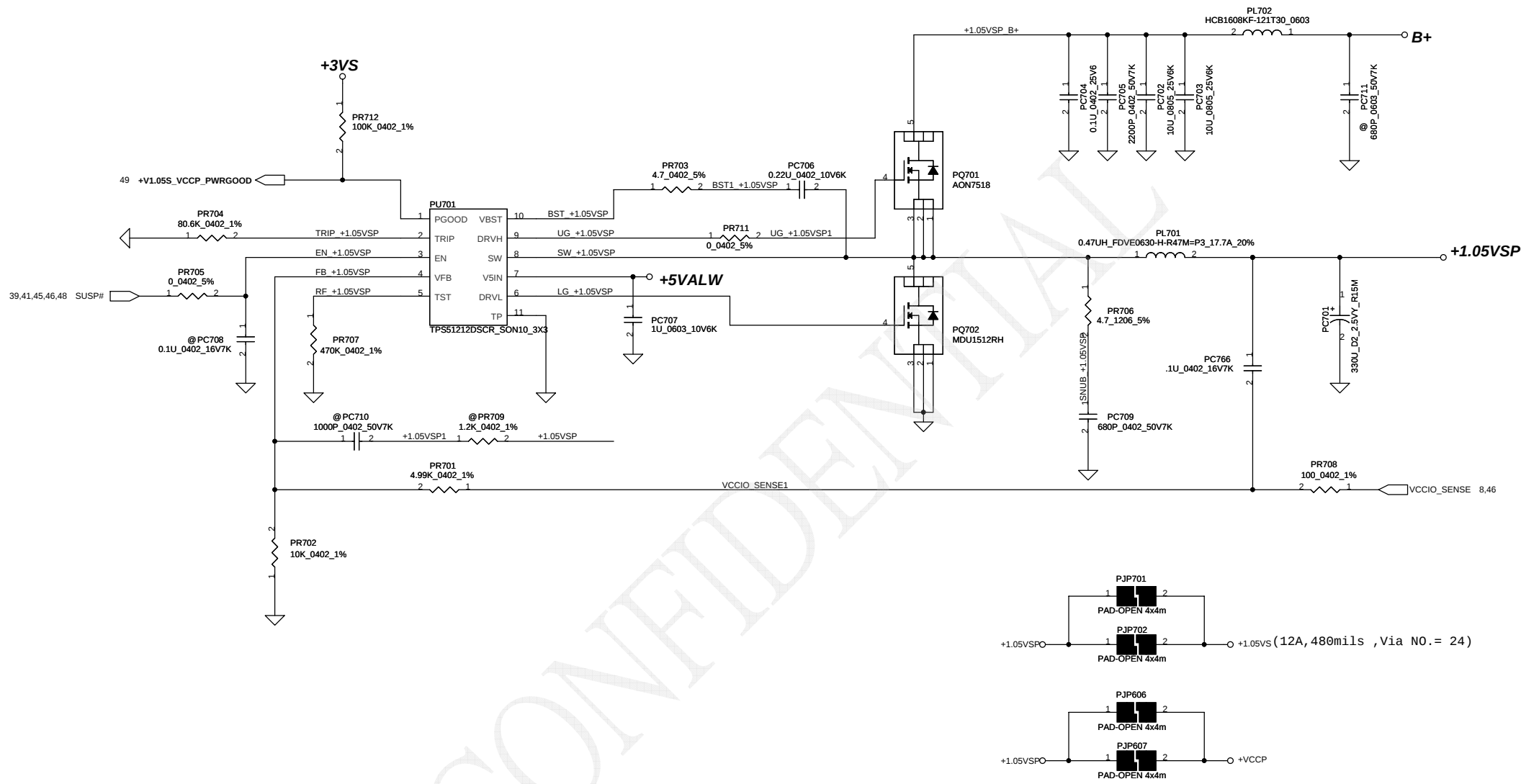




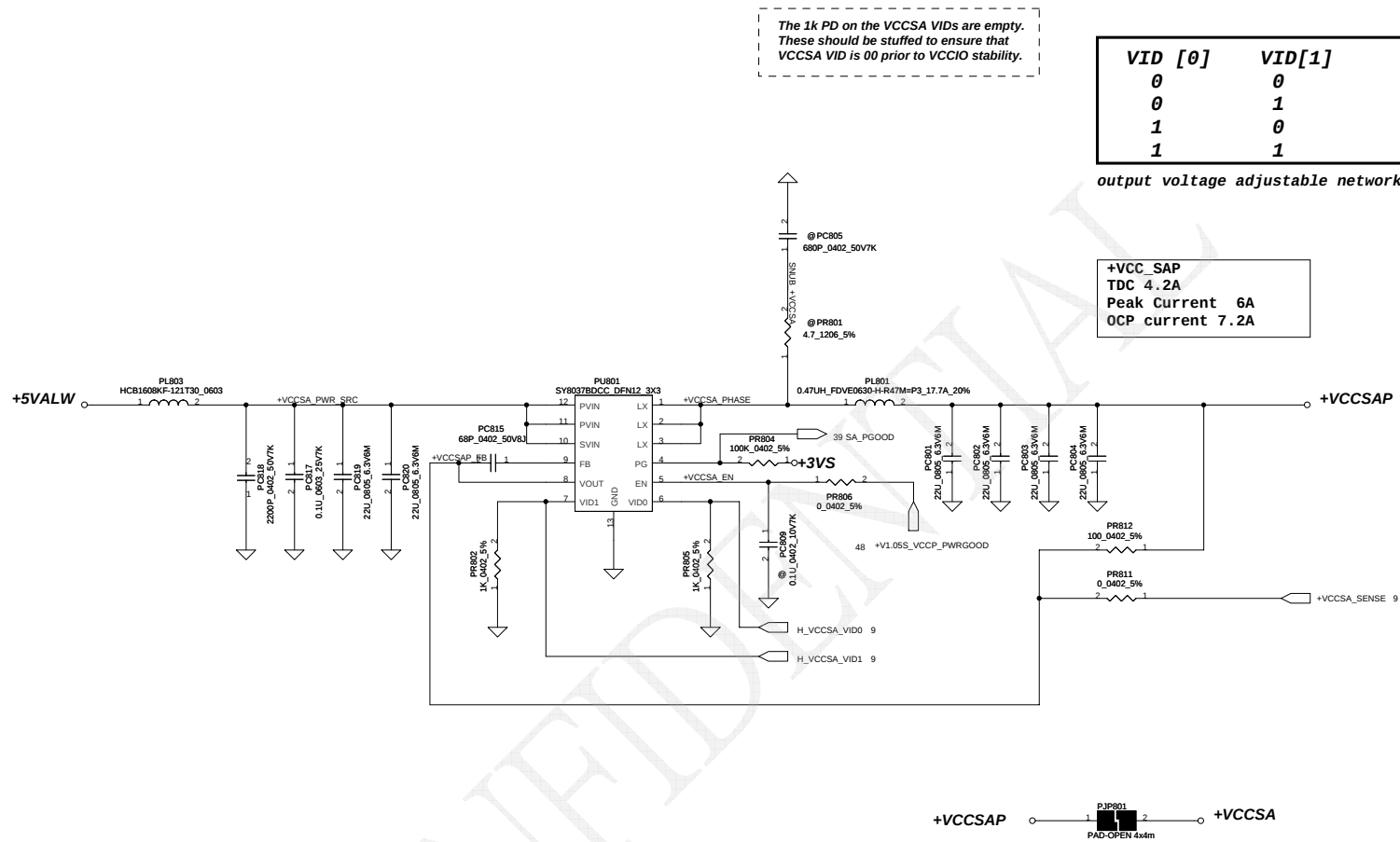
For KB930 --> Keep PR319, Remove PR322
For KB9012 (Red square) --> Remove PR319
Keep PR322

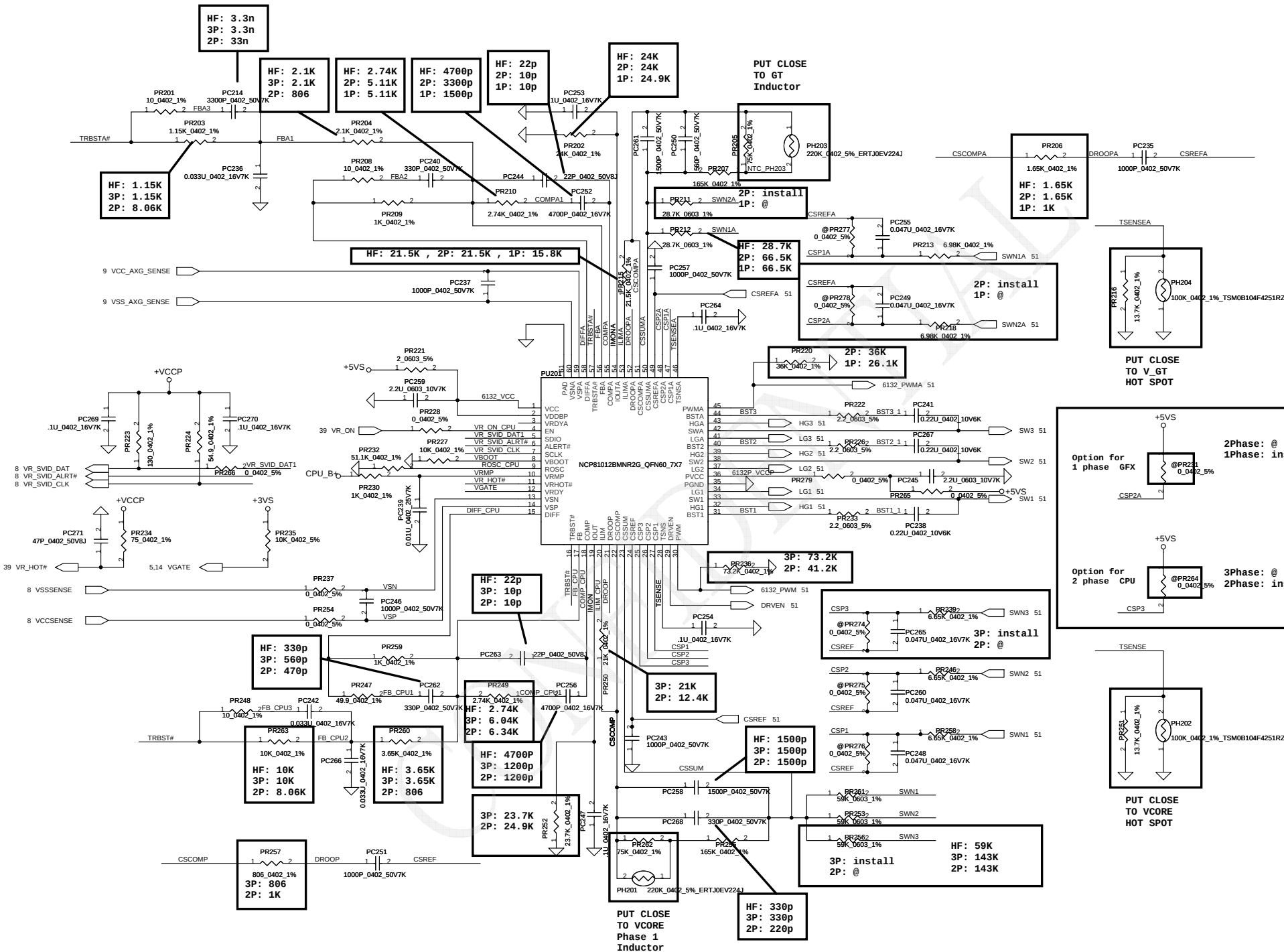
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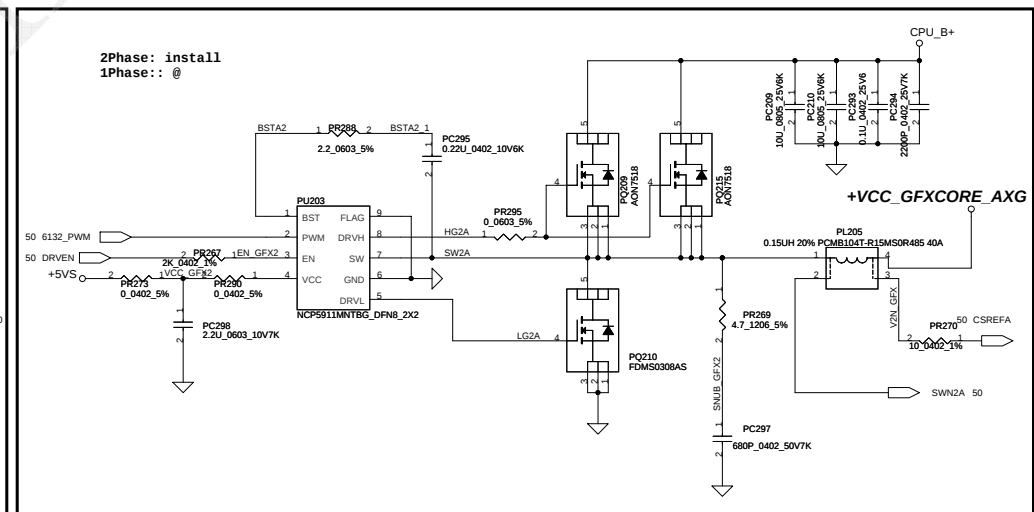
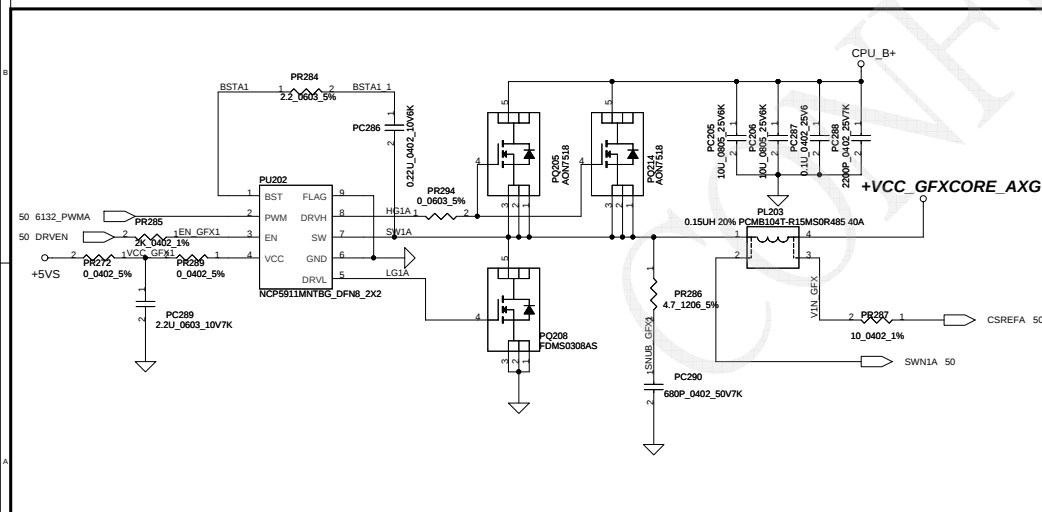
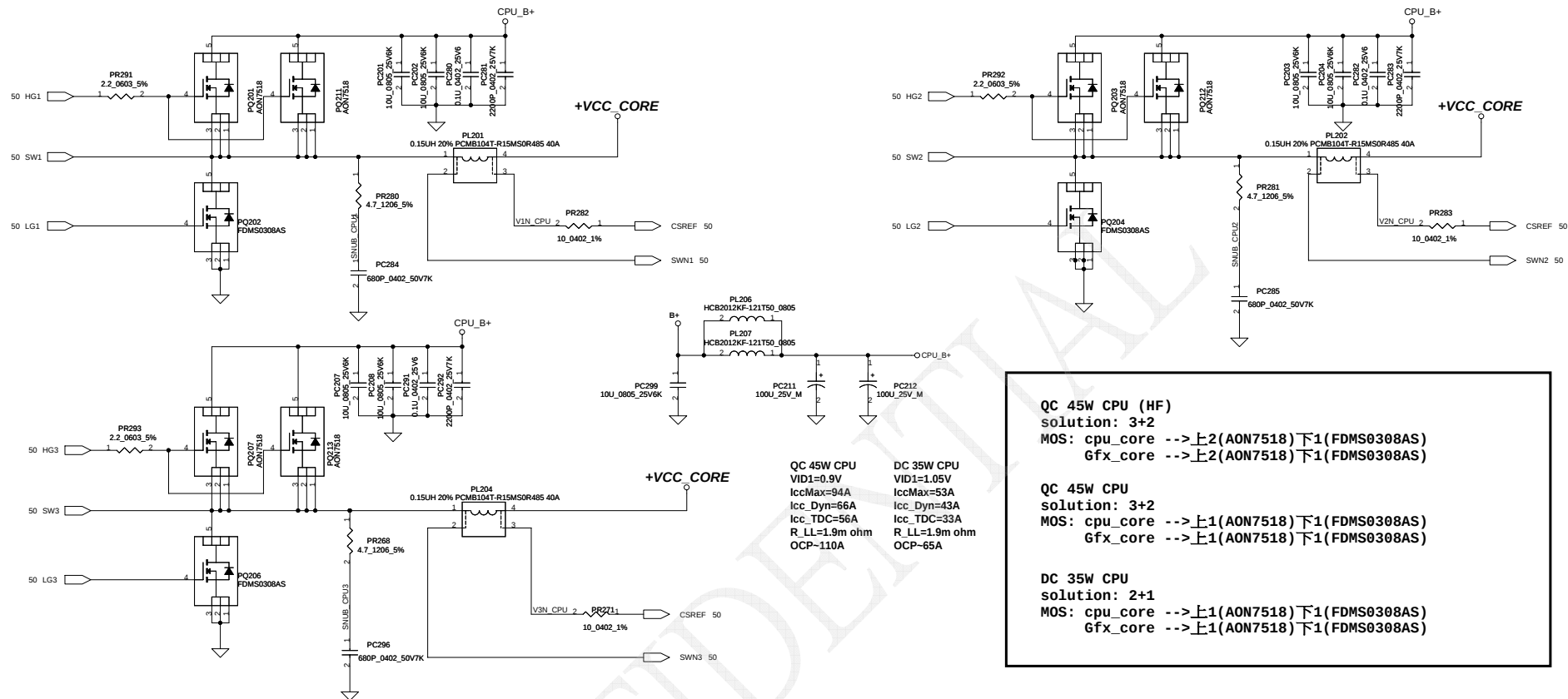




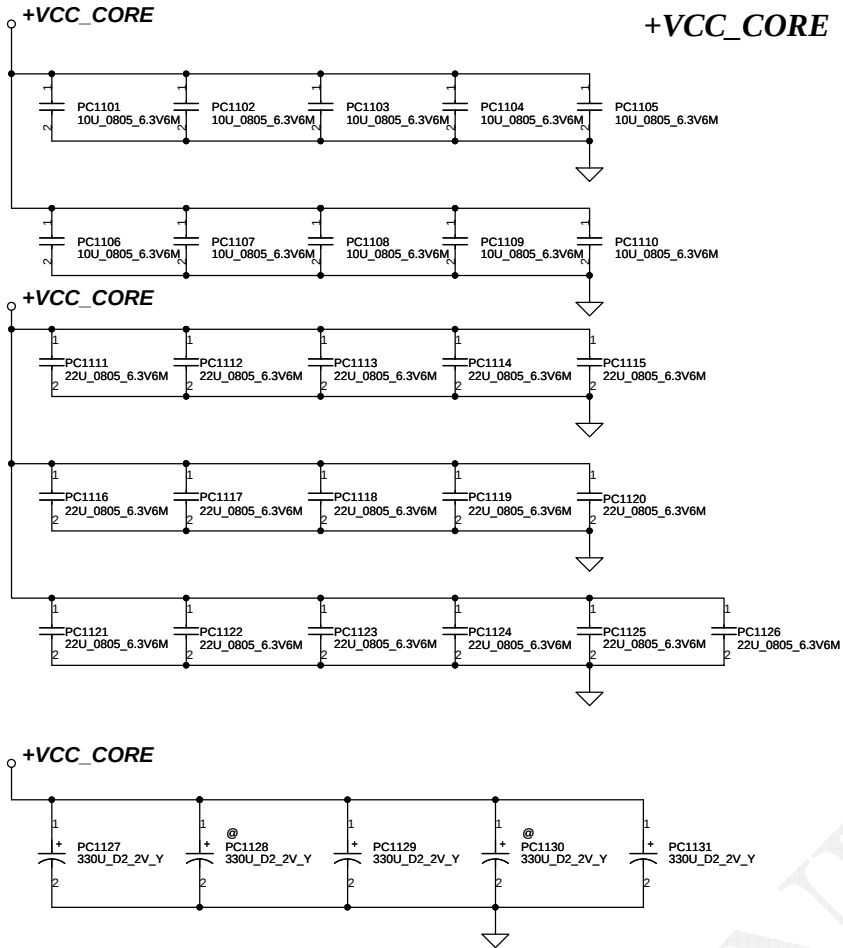
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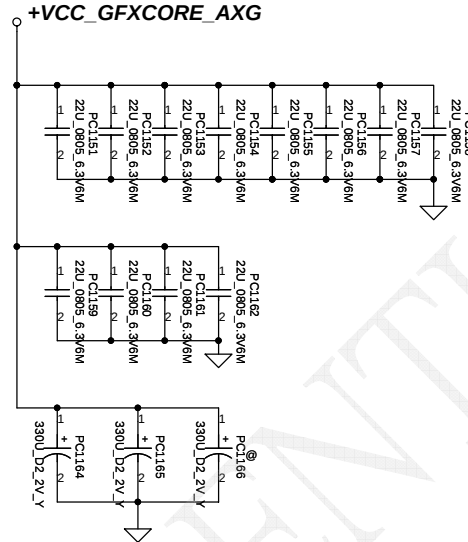




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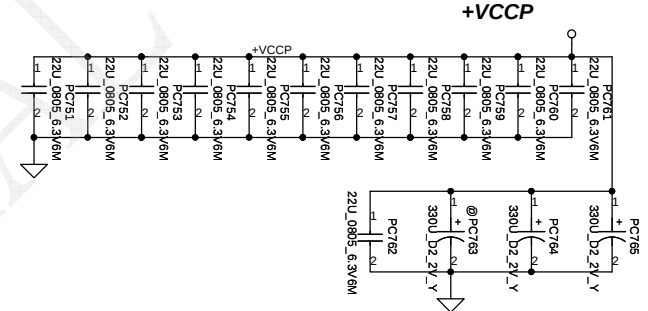


+VCC_GFXCORE_AXG



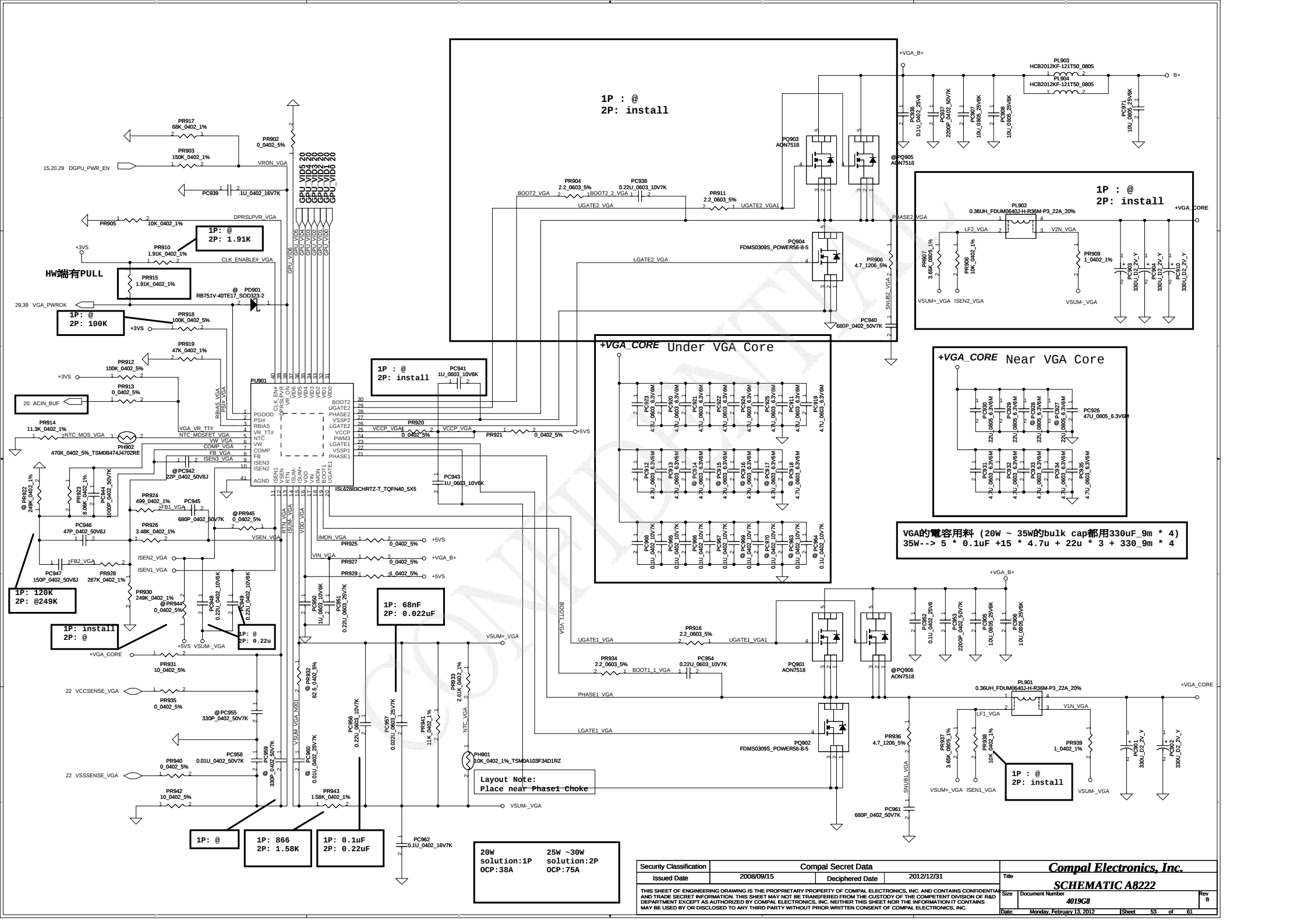
Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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1P : @
2P: install

1P : @
2P: install

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

VGAの電容用料 (20W ~ 35wのbulk cap都用330uF_9m * 4)
35W -> 5 * 0.1uF + 15 * 4.7u + 22u * 3 + 330_9m * 4

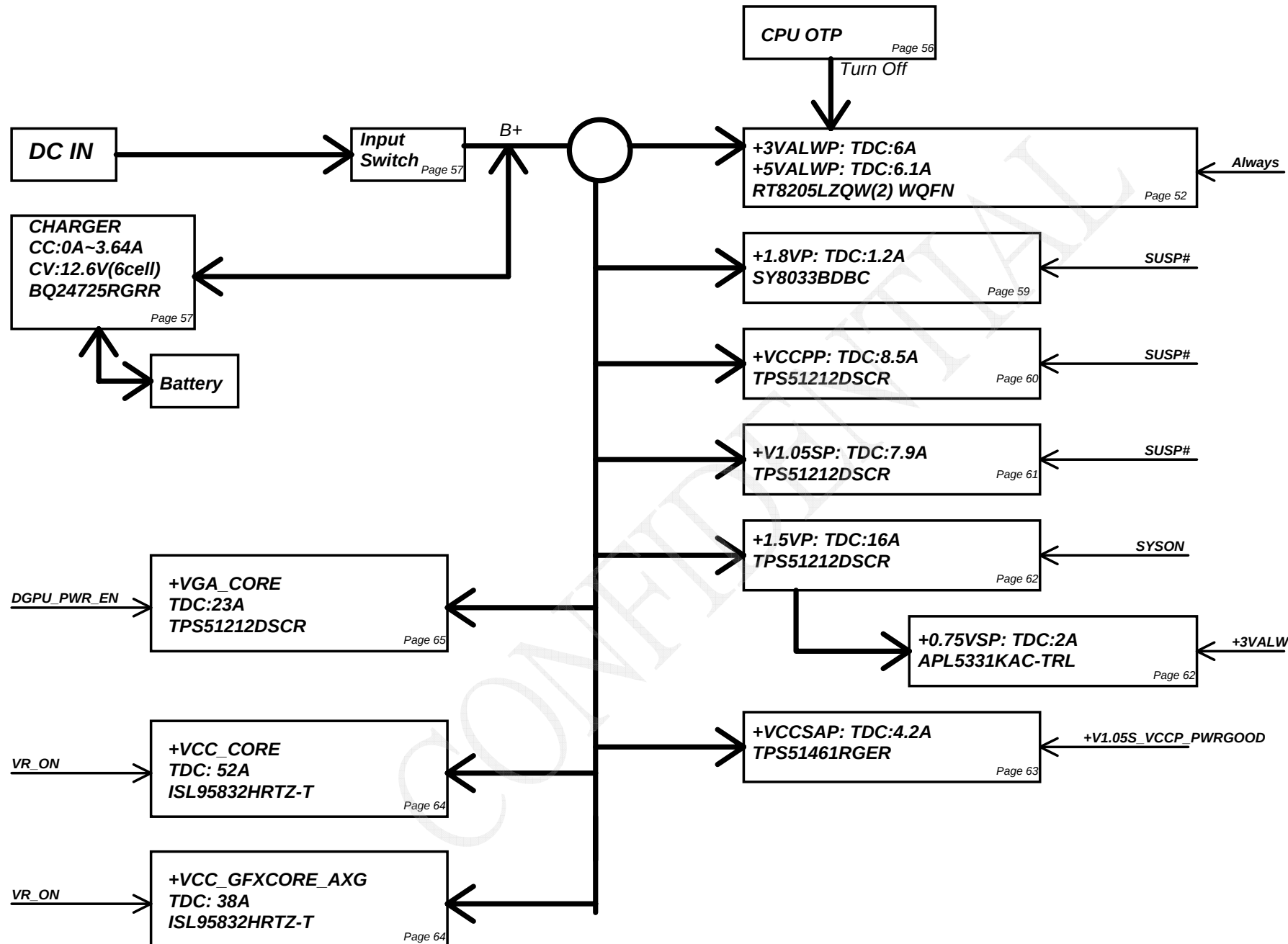
Layout Note:
Place near Phase1 Choke

20W
solution:1P
OCP:38A

25W ~30W
solution:2P
OCP:75A

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Power block



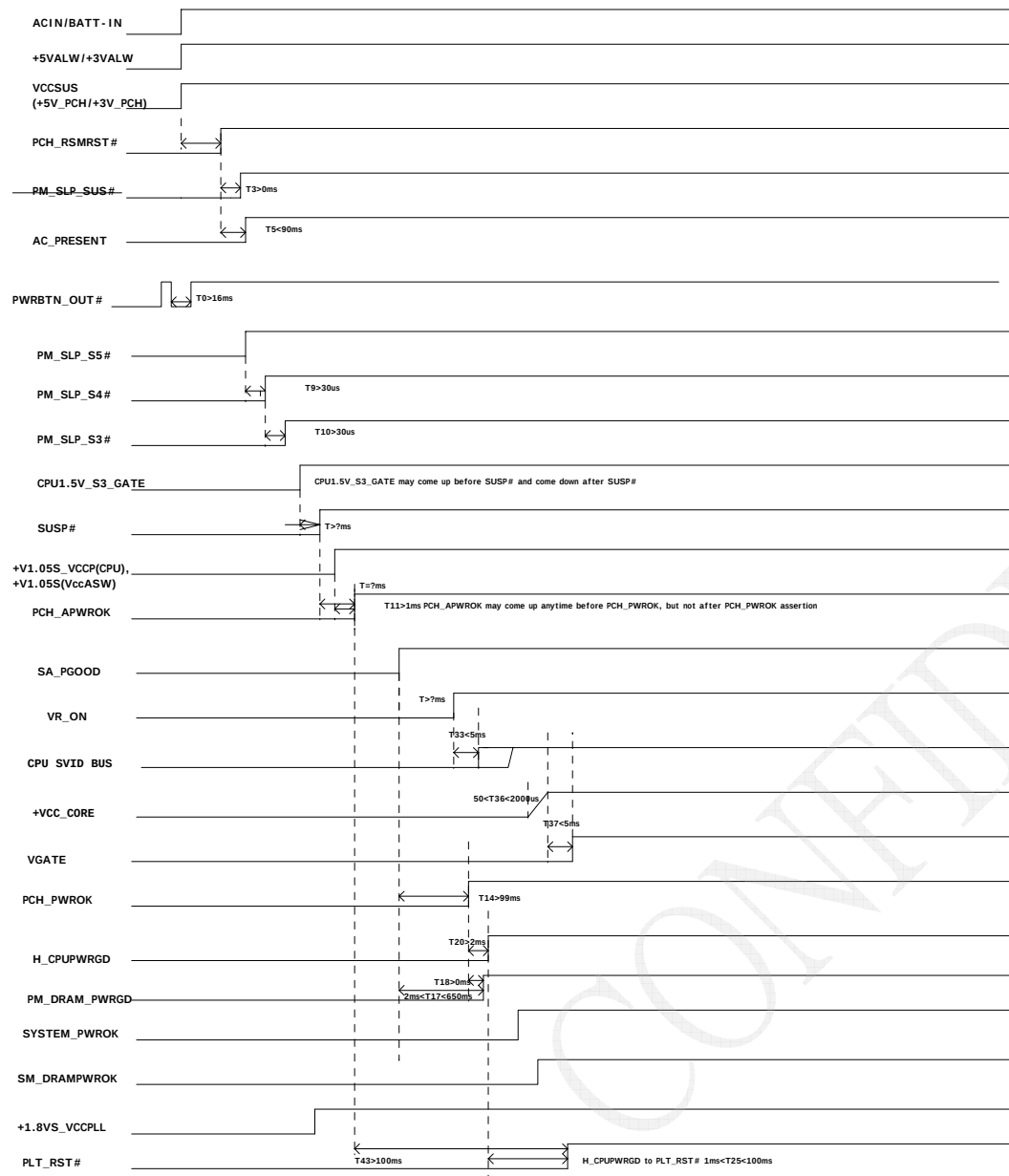
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by Intel® MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design	0.2	14 05	Delete R205 Un-stuff R577, Stuff R576	09/21	
ER02		For non AI co-lay	0.2	37	Add R745, R746 for non AI AI parts change to AI0	09/21	
ER03	+3VS Leakage	HW Design	0.2	15 13 40	Change R132/R134 PU power to +3V SPI Delete Q3 A/B, Add R135, R137 Delete R552, R556	09/21	
ER04	Can't detect USB30 (JUSB2)	HW Design	0.2	36	Swap U90.36/40 to U90.36/37 net Change R1040 to 47K from 4.7K ohm Add Reserve R1029	09/21	
ER05		Design change for card reader	0.2	34	Add Q20, R773, R775 Reserve R768, R774 Change Card reader Conn	09/22	(10/73 - follow K45 change Dual FET location from Q63 to Q20)
ER06		HW Design / VGA sequence	0.2	29	Change to Q3(A03404L) from U22(A04430L) Change R433 to 0 ohm, R432 to 10K ohm Un stuff C396	09/21	
ER07		HW Design	0.2	36	Change R1049 to 330K Change Q904 to A03404L from AP2301GN Delete R1046, Add R747	09/21	
ER08		HW Design	0.2	42	Change Q33 to A03413L from AP2301GN	09/21	
ER09		HW Design	0.2	18	Add un stuff R290	09/23	
ER10		Refer to ORB	0.2	05	Change R577.2 power rail from +3VS to +3V_PCH	10/04	
ER11		Refer to ORB	0.2	13	Del R135, R137. Change SML1CLK to PCH_SML1CLK Change SML1DATA to PCH_SML1DATA	10/04	
ER12		HW Design	0.2	40	Del Y5 , C545 , C546	10/04	
ER13		Refer to purchaser suggestion	0.2	15	Replace R230 NR with R780-R783. Replace R237 NR with R784-R787. Replace R242 NR with R792, R793, R288.	10/04	
ER14		Refer to purchaser suggestion	0.2	29 31 42	Change C387, C389, C399, C447, C602 PN	10/04	
ER15		HW Design	0.2	40	Del U33.123 EC_CRY2 net name	10/04	
ER16	DRAMRST_CNTRL_PCH signal timing	Reserved for Instant-On function.	0.2	13	Add R750	10/04	(10/06 - Change location from R1082 to R750, And Change its tolerance from 1% to 5%).
ER17		EMC request to reserve these caps.	0.2	36	Add C1045-C1048	10/04	
ER18			0.2	43-55	Update Power circuit (1003)	10/04	
ER19		Instant-On function - DRAMRST control by PCH.	0.2	13	Un-stuff R157, Stuff R750	10/06	
ER20		ME Design Change.	0.2	38	Change H16, H17, H22 screw hole type to 3P5. (dGPU & VRAM)	10/07	
ER21			0.2	43-55	Update Power circuit (1011) - Del PC1163.	10/11	
ER22		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/13	
ER23		Fine-tune timing.	0.2	29 42	change R432 from 100R to 10K. change R435 from 10R to 200R. change R607 from 220R to 10R.	10/13	

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER24		Follow to ORB	0.2	05	Un-stuff R576, Stuff 0R to R577.	10/13	
ER25		change for GPU H/W strapping STRAP1 to PL 45k ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/13	
ER26		Refer to Intel review feedback item 5.	0.2	09	Add R277 0R 0805 5%	10/13	
ER27		Refer to Intel review feedback item 11.	0.2	09	Add 149	10/13	
ER28		Refer to Intel review feedback item 33.	0.2	31	Revise SATA P/N signals.	10/13	
ER29		Refer to Intel review feedback item 37.	0.2	18	Del L6, Add R289	10/13	
ER30		Refer to Intel review feedback item 40.	0.2	17	Del L4, Add R293	10/13	
ER31		Refer to Intel review feedback item 42.	0.2	42	Add R230	10/13	
ER32		Refer to Intel review feedback item 43.	0.2	42	on Stuff R244	10/18	
ER33		Refer test report to fine-tune oscillation frequency	0.2	12	Change Y1 P/N, Change C144, C145 to 18pF.	10/14	
ER34		Refer test report to fine-tune oscillation frequency	0.2	13	Change Y2 P/N, Change C163, C164 to 12pF.	10/14	
ER35		Refer test report to fine-tune oscillation frequency	0.2	20	Change Y3 P/N, Change C901, C900 to 12pF.	10/14	
ER36		Refer test report to fine-tune oscillation frequency	0.2	32	Change Y4 P/N, Change C469, C4735 to 12pF.	10/14	
ER37		Refer test report to fine-tune oscillation frequency	0.2	36	Change Y9 P/N.	10/14	
ER38			0.2	43-55	Update Power circuit (1014) - Modify Choke footprint.		
ER39		For EMI request	0.2	32	R484 and R486 change to C219 and C300 to 0.1u.	10/17	
ER40		For LED issue	0.2	39	change LED2 footprint to LED_HT-210UD-UYG_3P	10/17	
ER41		For EMI request	0.2	05	Add R12 0 ohm at H_CPUPWRGD	10/17	
ER42		For SATA GEN2 EA pass.	0.2	31	change R671 to 3.3k ohm.	10/17	
ER43		For EMI request	0.2	16	Add C151 0.1uF to GND on H_THERMTRIP#	10/17	
ER44		For EMI request	0.2	33	1.GND pin3-pin1, USBN9 pin1-Pin2, USBP9 pin2-Pin3 2.GND pin5-pin7, +USB_VCCD pin6, 7-pin5, 6	10/17	
ER45		For EMI request	0.2	33	Add L34 , L35 , reserve R552, R556 , R748 , R749	10/17	
ER46		For EMI request	0.2	5 7	remove T2, T3, T4, T5, T6, T7, T8, T9, T46, T47 T38, T39, T40, T41, T42, T43, T10, T11, T45	10/17	
ER47		For Power request	0.2	38 40	Change +3VLP to +3VL	10/17	
ER48		SATA Re-driver 2nd source.	0.2	38	PAR8520@ : U41-U43, R671=3.3K ASM1466@ : 1) Add R426, R405, R419, R403, R396, R417 U41-U43. 2) R459, R669, R672 = 4.7K 3) R682, R690, R698 = 2K	10/17	

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ER49		For EMI request	0.2	34	remove C620 , C611 , C631	10/18	
ER50		for HW design	0.2	39	change U36 PN to SA00003B900 and C583 unpop	10/18	
ER51		For EMI request.	0.2	05	H_CPUPWRGD net name change to H_CPUPWRGD_R	10/20	
ER52		For T88 request for ROM WP function	0.2	12	Reserve R137 , Q63, pop R135 change EC_PECI to EC_SPI_WP	10/26	
ER53		For EMI request	0.2	13	Add R185	10/20	
ER54		to prevent +3VSG leakage when Optimus.	0.2	20 40	Change ACIN_BUF circuit unstuff R730	10/20	
ER55		For remove MS fuction	0.2	34	Delete R637	10/20	
ER56		For AP2301 EOS issue	0.2	37	change C510,C516,C519,C524 PN to SE026224K80	10/20	
ER57		for EMI request	0.2	40	Add C156 , C157	10/21	
ER58		Reserve for Deep Sx	0.2	14 40	Add unstuff R800,R801,R802,R803,R804,R805 Add PCH_DPWROK,DS_WAKE#,SUSACK#,SUSWARN#	10/19	
ER59		for EMI request	0.2	35	Change L31-L33 PN to SM070000N00	10/26	
ER2-1		For SATA signal driving	0.3	31	Change R668,R671 to 2K ohm for PAR8520 Add 10k ohm (R675,R677,R683,R685) for PAR8520 Unstuff R396,R417,R698,U43 for Asm1466 Unstuff C644,C645,C646	11/22	
ER2-2		For EMI request	0.3	32	Add 0.1uF (C219,C300) Change TS1 to SP050007G00 from SP050006L00	11/22	
ER2-3		For Card reader function	0.3	34	Change SDD2 to U40.21 and SDD3 to U40.20	11/22	
ER2-4		For USB charge & wake function	0.3	37	Add 0 ohm (R809,R810)	11/22	
ER2-5		For WIN8	0.3	12	Add U5 SPI ROM 8M for Win8	11/22	
ER2-6		For change Click Pad from Glide Pad.	0.3	13 39 40 39	Connect SMBUS to click pad. Del SW3,SW4. change JTP1 Add 064 , R808 Change PU to +3VS TP CLK.TP_DATA Update JTP1(SP01001AE00) connector 8 pin	12/12	
ER2-7		For HDMI LOYALTY	0.3	35	Add 460 HDMI LOYALTY	11/22	
ER2-8		Change Main source for HDMI power switch	0.3	35	Change U44 SA00004ZB00 to SA00004ZA00	11/22	
ER2-9		For +3VSG leakag when boot first time	0.3	15	Add R443 10k pull down , unstuff R244	12/01	
ER2-		For N13M-GS DID	0.3	22	Update strap pin table	12/01	

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ER2-10		HW Design	0.3	42	Change 2N7002 single to dual channel< Q71-Q77> Del R625, R084 Change Q38 S14178DY to A03404AL Add R813 PD 1.5M ohm	12/12	
ER2-11		For USB3.0 chip sequence	0.3	36	Change C1011 to 2.2uf from 1uF << 0402 to 0603 Change R1040 to 51.1k +-1% ohm	12/05	
ER2-12		HW Design	0.3	29 41	Change 2N7002 single to dual channel <Q78-Q80> Change 2N7002 single to dual channel <Q81> Change 2N7002 single to dual channel <Q82>	12/05	
ER2-13		HW Design for power saving	0.3	12	Un stuff R111-R113	12/05	
ER2-14		HW Design	0.3	06 42 17	Change C73 SE070473Z80 to SE076473K80 Change C690 SE027224Z80 to SE026224K80 Change C180 SE000006L80 to SE000006I10	12/07	
ER2-15		HW Design	0.3	12 35 42	Change 1U(0603) SE052105Z80 to SE080105K80 Page PCH,HDMI,DCDC,DIIMM	12/07	
ER2-16	EMI	EMI request	0.3	15 30 33 34 37 41	Change USB2.0 port & OC#	12/15	
ER2-17		HW Design	0.3	16	Add R812 to GPIO22 PD 10k ohm , Unstuff R252	12/09	
ER2-18		HW Design	0.3	14 40	Un-Stuff R554, Stuff R226 (Change to 10k)	12/12	
ER2-19		Intel New chip of PCH HM76 rev.C1	0.3	PCH	Change U3 PN to SA00005FH10	12/12	
ER2-20		HW Design	0.3		Change AII 2n7002 to SB00009Q80 from SB00009620 Change 0.1uF SE102104K00 to SE076104K80	12/12	
ER2-21		EMI request	0.3	35 30	Add 2pF C706-C707 Add R820,R821 & L40(Unstuff)	12/12	
ER2-22		HW Design	0.3	20	Change Q900.2 control pin to +3VSG	12/12	
ER2-23		For EMI request	0.3	39	Change U36 to SA000058600	12/14	
ER2-24		For EMI request	0.3	29	Add Reverse 100pf C710-C715,C717-C723 to +1.5VSG and other power plan	12/15	
ER2-25		For EMI request	0.3	05	Add R12 1k ohm and C640 0.1u Capacitor	12/19	
PR-1		For ASUS request	1.0	40 38	Add PWR_ON_LED1# on U33 Pin 119	01/02	
PR-2		For EMI request	1.0	05	R12 change to 33ohm (SD028330A80) and C640 change to 100p(SE071101J80)	01/03	
PR-3		For power consumption @ AC S5	1.0	29	R432 change to 100K(SD028100380) and C395 change to 0.01u (SE075103K80)	01/03	
PR-4		For ENE request	1.0	39	reserve KSI4,5,6,7 cap 10p to GND	01/06	
PR-5		For debug function	1.0	41	stuff R595	01/06	
PR-6		For GS gen3 support	1.0	22	R352 ,R349 bom structure change to @	01/06	
PR-7		For HW design	1.0	41	change 0 ohm footprint to R_short change R584 footprint 1206 to 0805 R_short	01/06	
PR-8		For PLT_RST# leakage when power on	1.0	15	Add R445 and reserve R444 unstuff R234	01/06	
PR-9		For Mos max Vgs voltage tolerance	1.0	29 42	Add R830 and R831 470K ohm to GND Add R813 1M ohm to GND	01/19	
PR-10		For Asmedia SATA redriver	1.0	31	Change R690 to 1.5K ohm to GND	01/06	

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PR-11		For power consumption	1.0	36 40	modify asmedia power schematic Add USB3_ON at U33 pin 120	01/09	
PR-12		For EMI	1.0	33	Reserve C723-C726 1.8P capacitor to GND	01/13	
PR-13		For HW design	1.0	30 34	C422,C423,C619 footprint change to 0603 from 0805	01/13	
PR-14		For EMI	1.0	42 40	Change C1047 and C606 to 0.1uF Add Reserve C1070	01/17	
PR-15		For HW design	1.0	41	Change U37 to Si4178DY-T1-GE3 from A04478 (WLAN power MOS)	01/17	
PR-16		For power consumption @ AC S5	1.0	42 41	Change R610,R724 to 390k from 47k ohm C599,C592 change to 0.01uF.	01/19	
PR-17		For EMI	1.0	32 5	Change C475 to 10P (SE00000U000) Change C72 to 12P Add C647	01/30	
IRT-1		For EMI	1.A	30	Add C544 C545	02/08	
IRT-1		For check AI charger exit or not	1.A	40	Change R743 bom structure to AI@	02/10	

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