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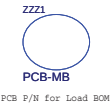
QCL40 MB Schematic Document

LA-8221P

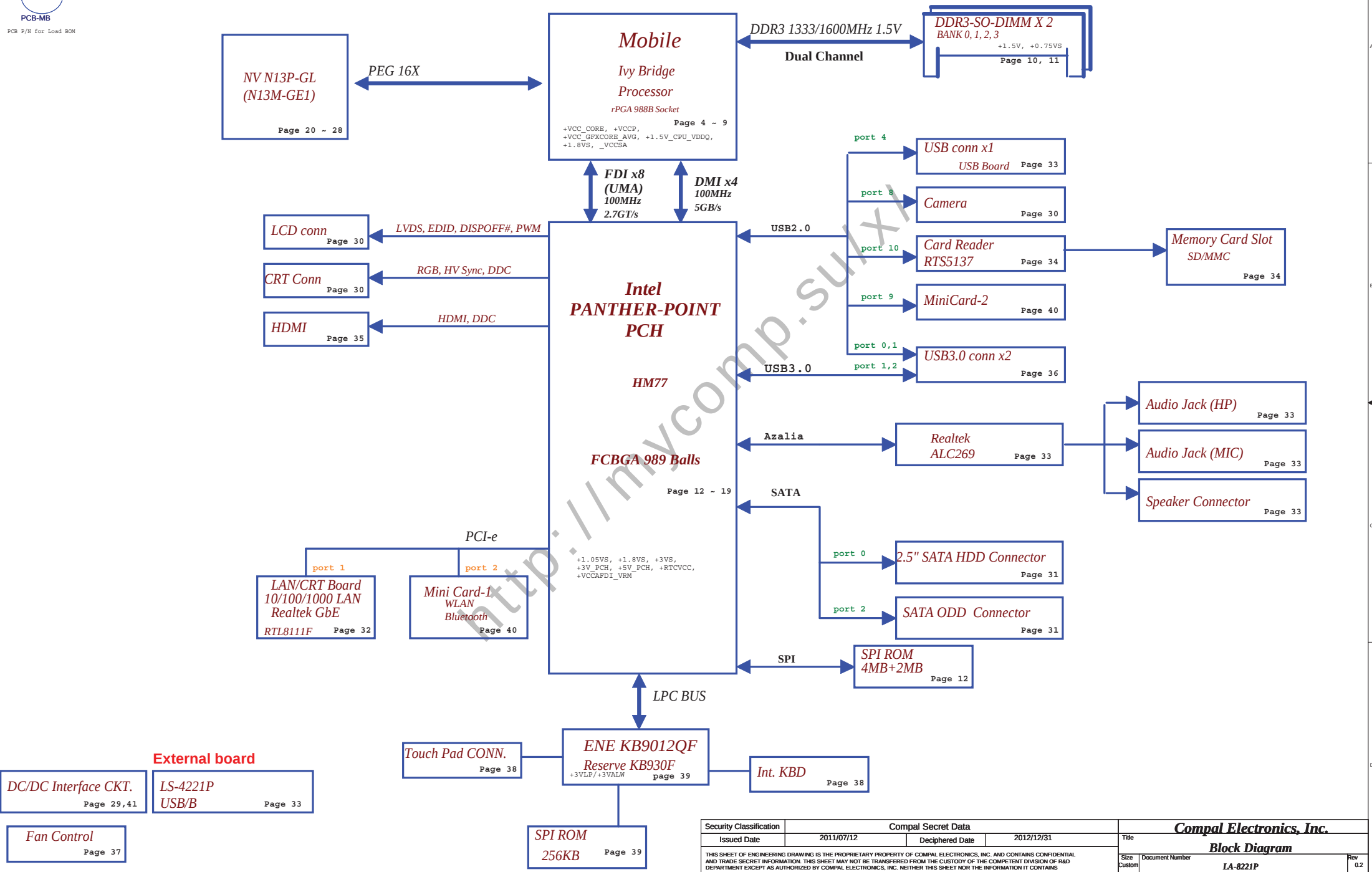
Rev: 0.2

2011.09.28

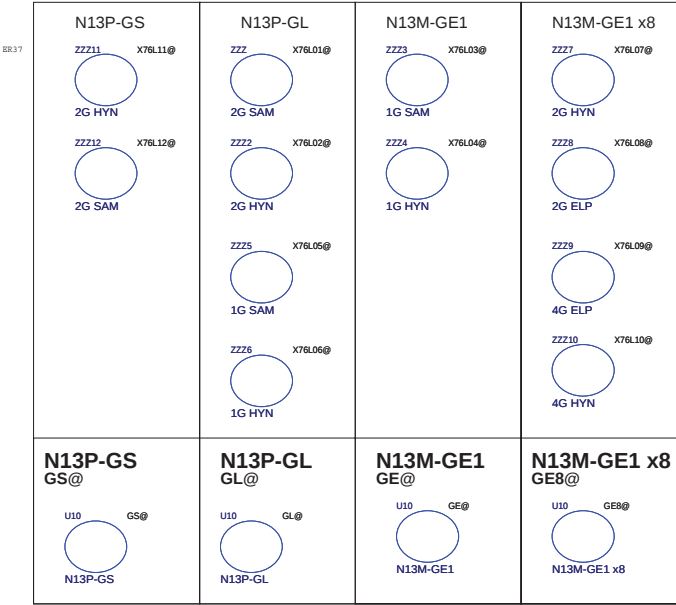
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	Cover Sheet
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QCL40



X76@: VRAMX16X8 VRAMX16X4 VRAMX8X8



DIS@: VGA componet
GEL@: N13P-GL or N13M-GE1
GSL@: N13P-GL or N13P-GS
GS@: N13P-GS

930@: EC(ENE 930 chip)
XDP@: Intel debug port

IU3@: USB3.0 by PCH
USB30@:USB3.0 controller IC

AI@: AI Charger
NAI@: Non AI Charger

9012@: EC(ENE 9012 chip)

SMBUS Control Table							
	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC SMB CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC SMB CK2 EC_SMB_DA2	KB930	X	X	V	X	X	V
PCH SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	USB3.0 controller	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

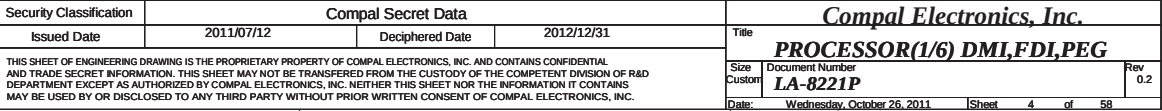
Voltage Rails

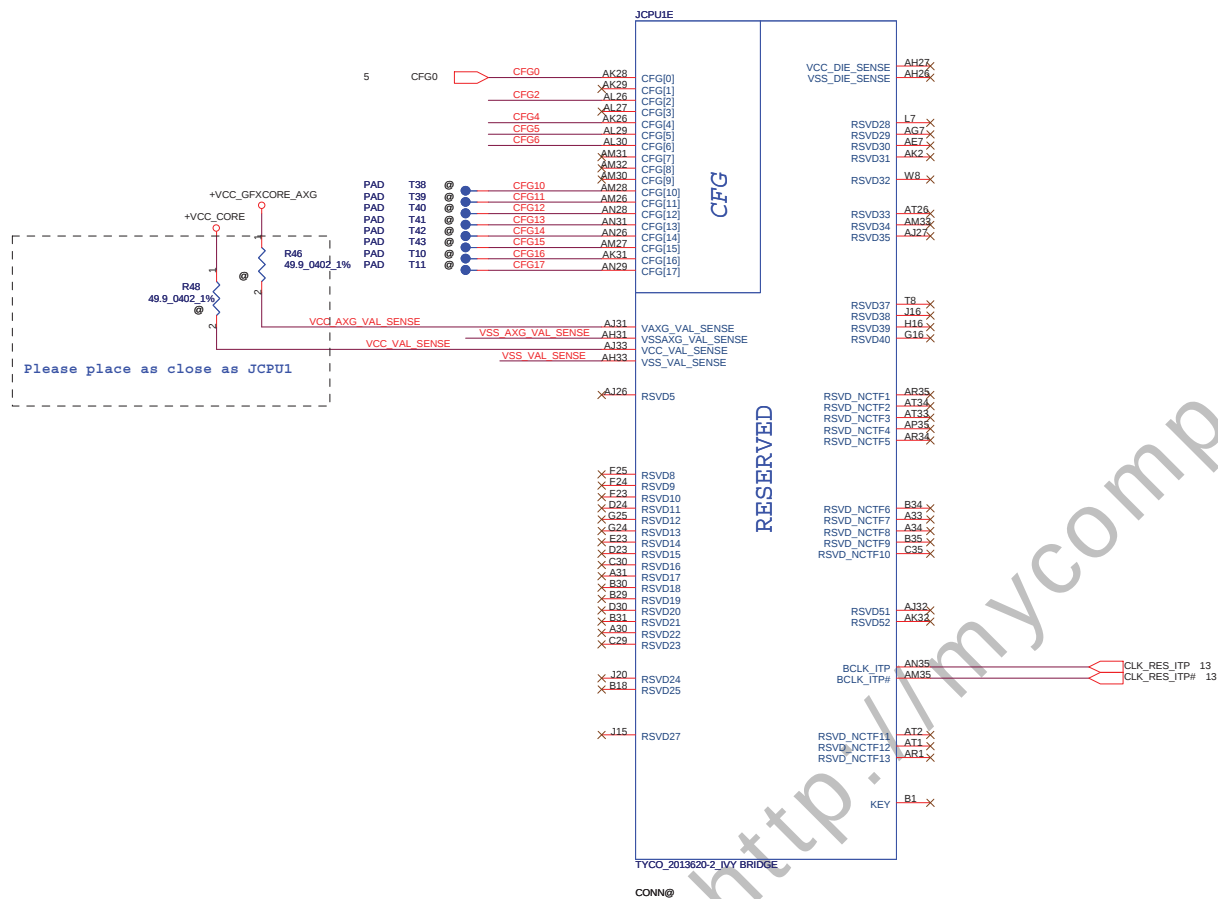
Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

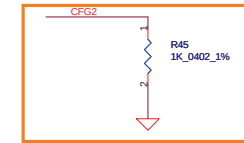
PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None
	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	None
	3	None
	4	JMINI1 (WLAN) Bluetooth
	5	None
	6	None
	7	None
	8	CAMERA
	9	USB2
	10	Card Reader
	11	None
	12	None
	13	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	USB3.0 controller
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None



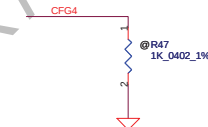


CFG Straps for Processor



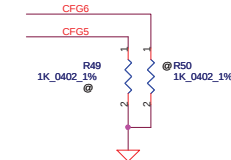
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	--



Display Port Presence Strap

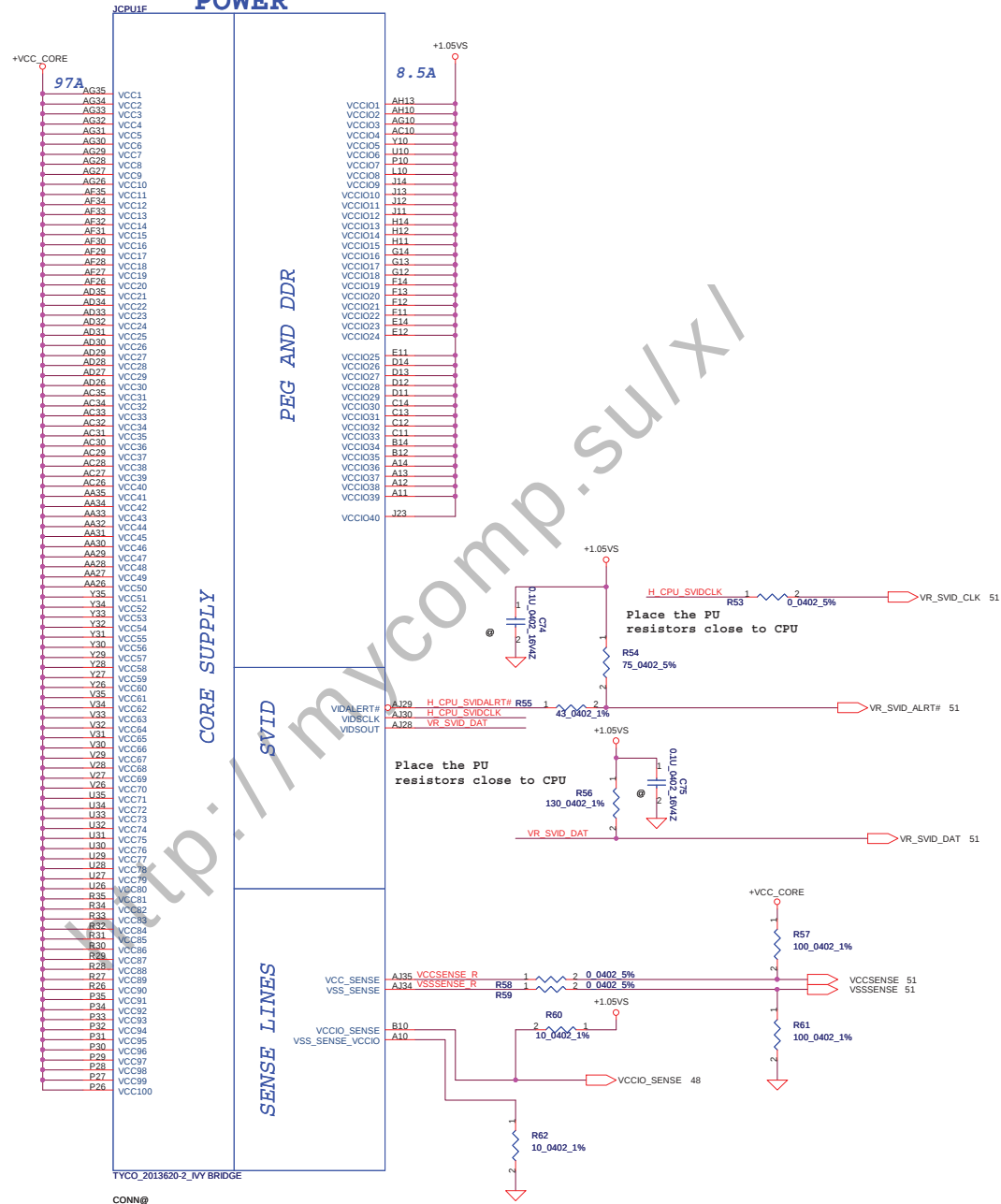
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
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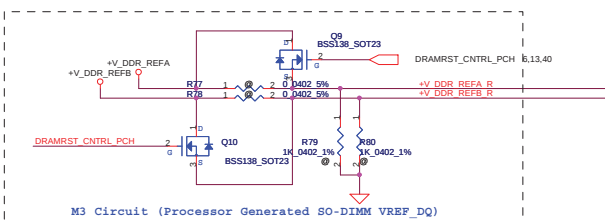
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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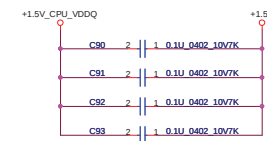
POWER

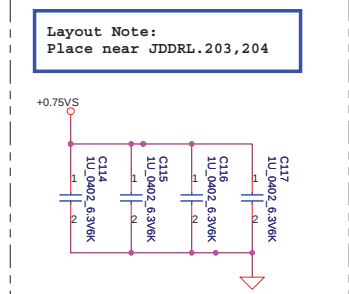
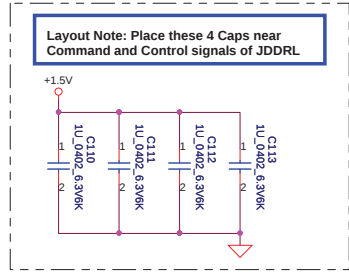
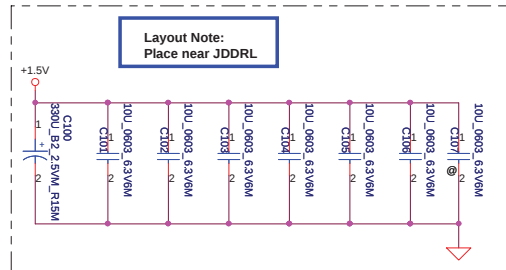
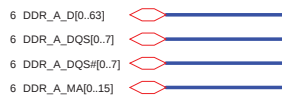
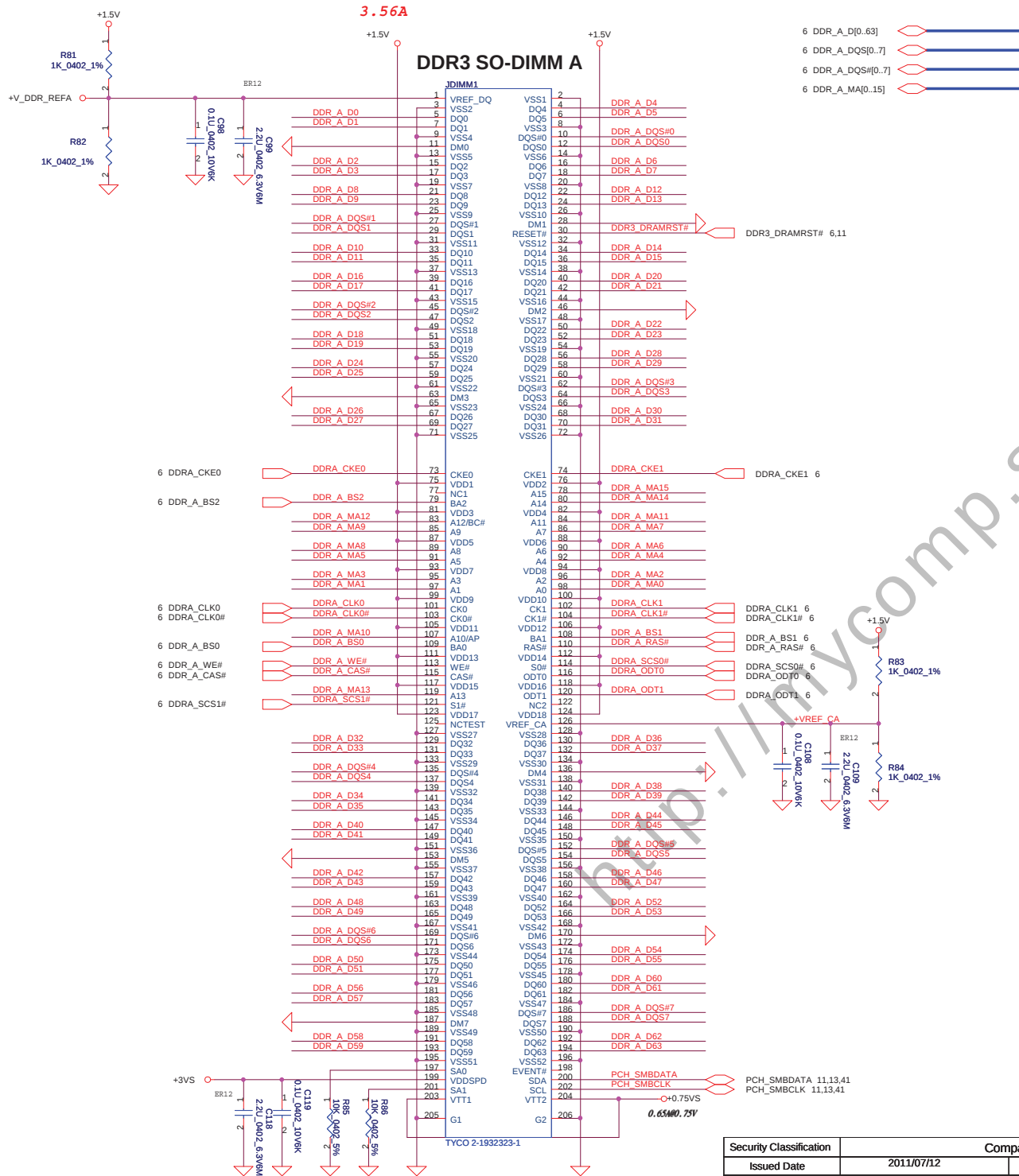


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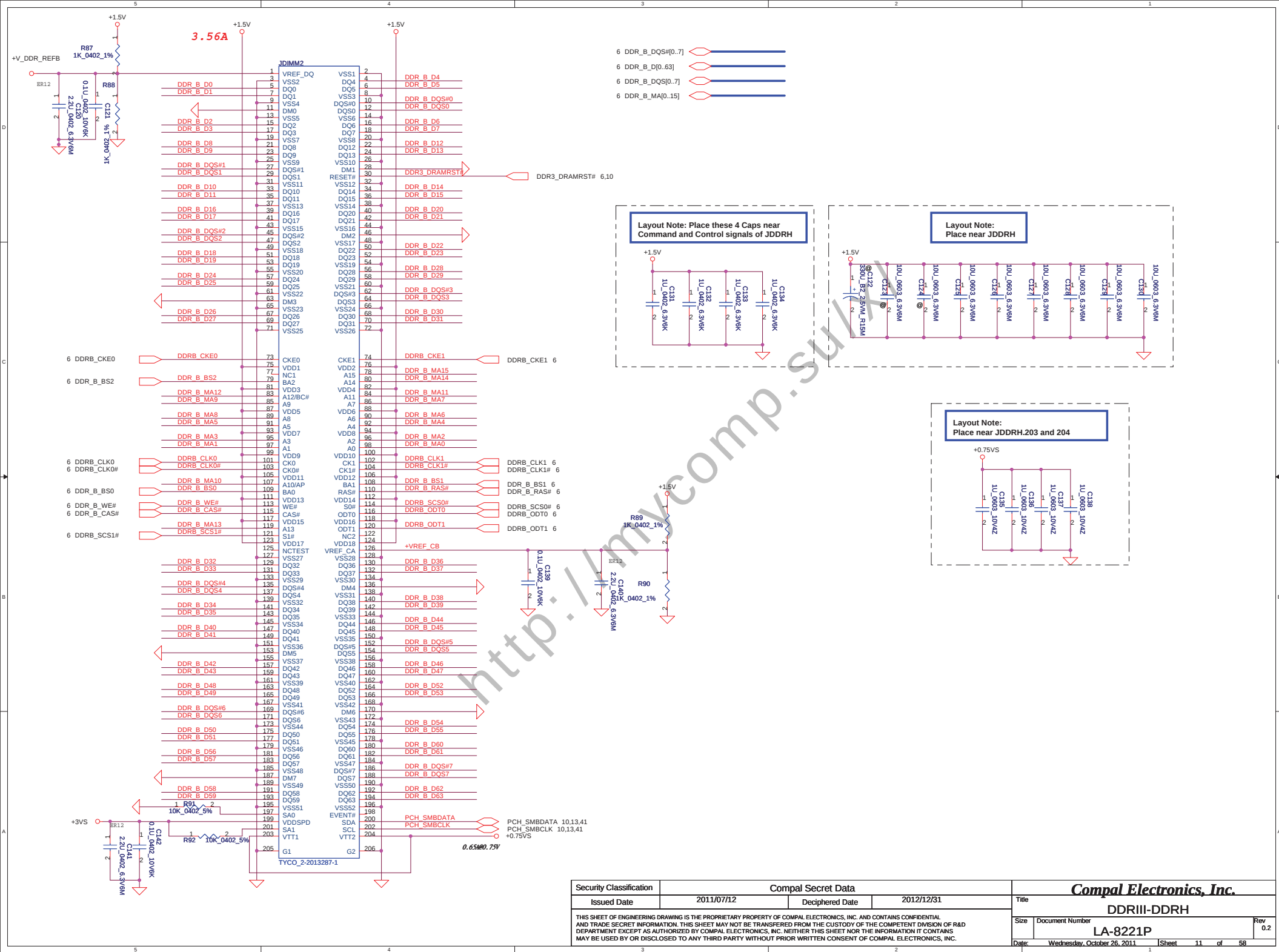


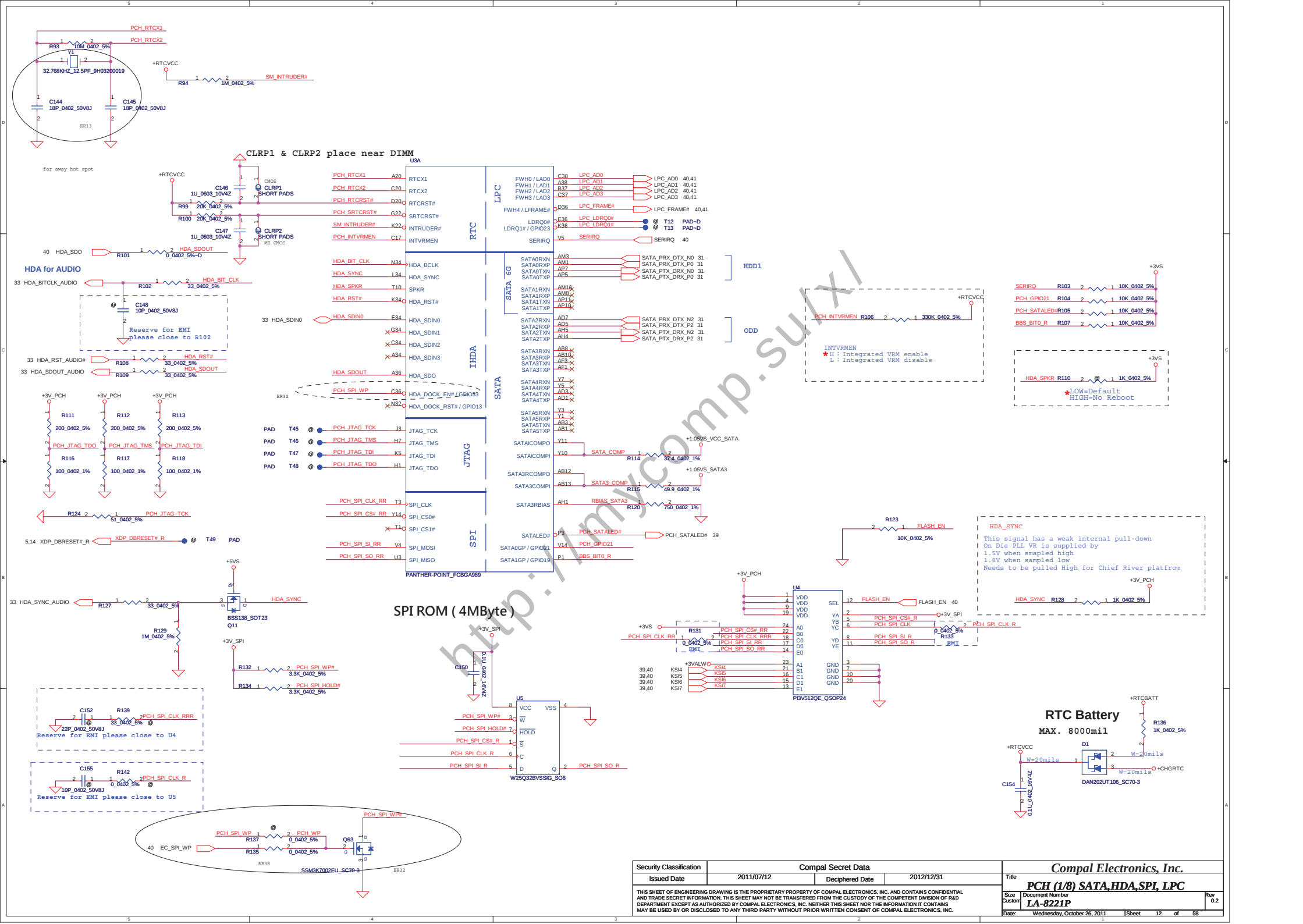
A135	VSS1	VSS81	A122
A132	VSS2	VSS82	A115
A128	VSS3	VSS83	A118
VSS4	VSS4	VSS84	A119
VSS5	VSS5	VSS85	A110
A122	VSS6	VSS86	A127
A116	VSS7	VSS87	A14
A113	VSS8	VSS88	A13
A110	VSS9	VSS89	A12
A110	VSS10	VSS90	A11
A17	VSS11	VSS91	A10
A7A	VSS12	VSS92	A9
A7B	VSS13	VSS93	A8
A7C	VSS14	VSS94	A7
A7D	VSS15	VSS95	A6
A7E	VSS16	VSS96	A5
A7F	VSS17	VSS97	A4
A7G	VSS18	VSS98	A3
A7H	VSS19	VSS99	A2
A7I	VSS20	VSS100	A1
A7J	VSS21	VSS101	A0
A7K	VSS22	VSS102	A99
A7L	VSS23	VSS103	A98
A7M	VSS24	VSS104	A97
A7N	VSS25	VSS105	A96
A7O	VSS26	VSS106	A95
A7P	VSS27	VSS107	A94
A7Q	VSS28	VSS108	A93
A7R	VSS29	VSS109	A92
A7S	VSS30	VSS110	A91
A7T	VSS31	VSS111	A90
A7U	VSS32	VSS112	A89
A7V	VSS33	VSS113	A88
A7W	VSS34	VSS114	A87
A7X	VSS35	VSS115	A86
A7Y	VSS36	VSS116	A85
A7Z	VSS37	VSS117	A84
A7A	VSS38	VSS118	A83
A7B	VSS39	VSS119	A82
A7C	VSS40	VSS120	A81
A7D	VSS41	VSS121	A80
A7E	VSS42	VSS122	A79
A7F	VSS43	VSS123	A78
A7G	VSS44	VSS124	A77
A7H	VSS45	VSS125	A76
A7I	VSS46	VSS126	A75
A7J	VSS47	VSS127	A74
A7K	VSS48	VSS128	A73
A7L	VSS49	VSS129	A72
A7M	VSS50	VSS130	A71
A7N	VSS51	VSS131	A70
A7O	VSS52	VSS132	A69
A7P	VSS53	VSS133	A68
A7Q	VSS54	VSS134	A67
A7R	VSS55	VSS135	A66
A7S	VSS56	VSS136	A65
A7T	VSS57	VSS137	A64
A7U	VSS58	VSS138	A63
A7V	VSS59	VSS139	A62
A7W	VSS60	VSS140	A61
A7X	VSS61	VSS141	A60
A7Y	VSS62	VSS142	A59
A7Z	VSS63	VSS143	A58
A7A	VSS64	VSS144	A57
A7B	VSS65	VSS145	A56
A7C	VSS66	VSS146	A55
A7D	VSS67	VSS147	A54
A7E	VSS68	VSS148	A53
A7F	VSS69	VSS149	A52
A7G	VSS70	VSS150	A51
A7H	VSS71	VSS151	A50
A7I	VSS72	VSS152	A49
A7J	VSS73	VSS153	A48
A7K	VSS74	VSS154	A47
A7L	VSS75	VSS155	A46
A7M	VSS76	VSS156	A45
A7N	VSS77	VSS157	A44
A7O	VSS78	VSS158	A43
A7P	VSS79	VSS159	A42
A7Q	VSS80	VSS160	A41

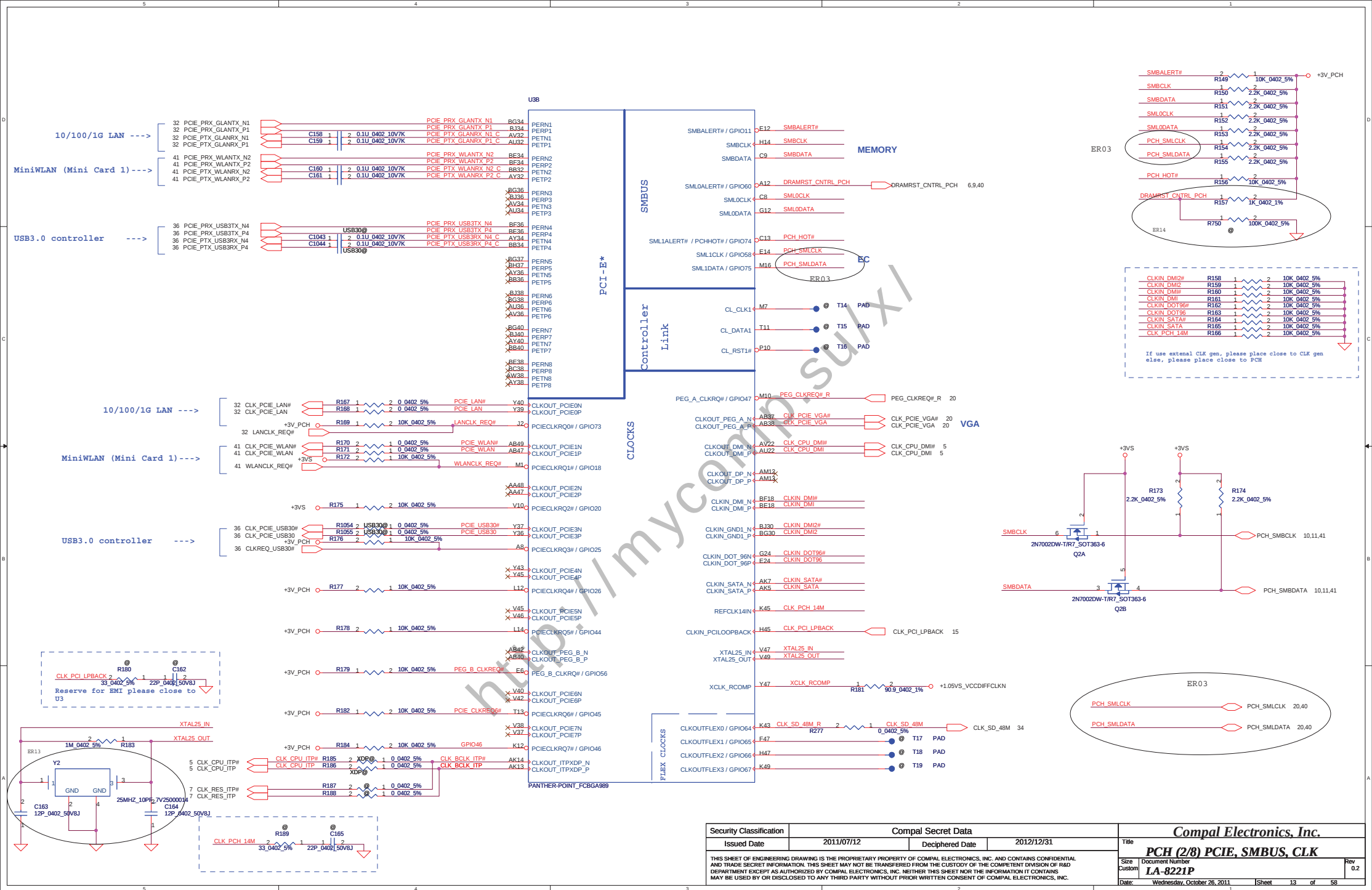


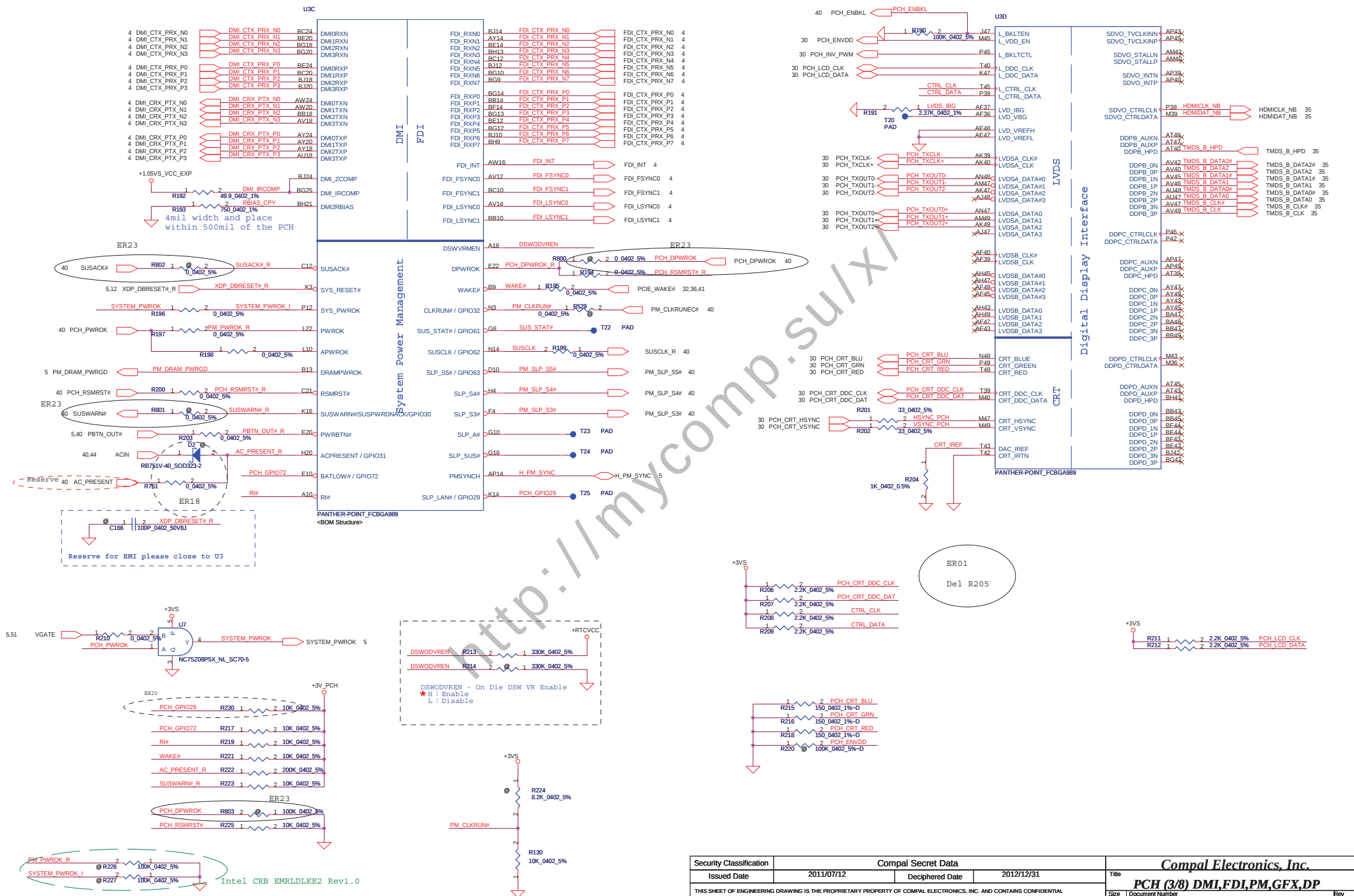


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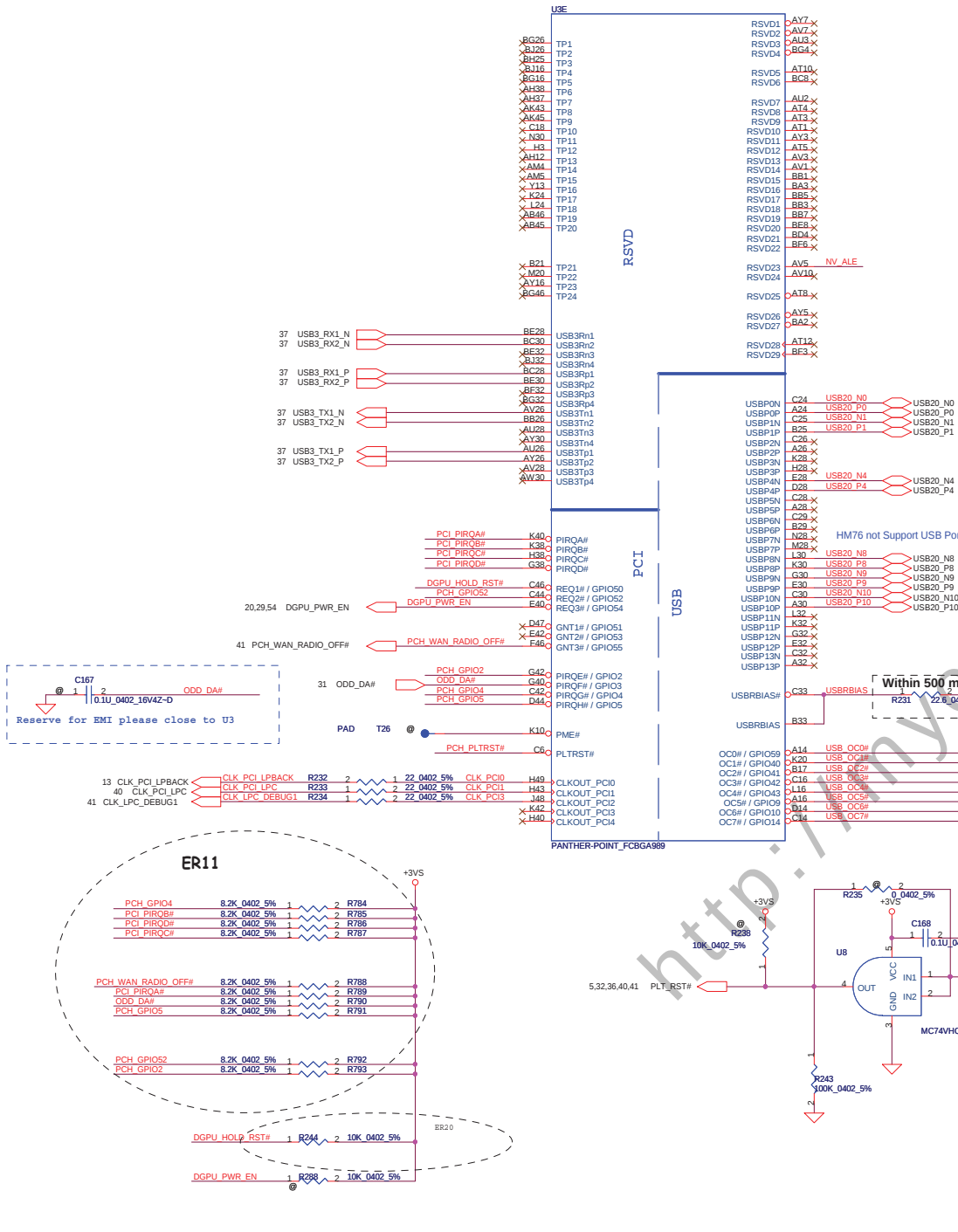








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Panther Point USB Port Mapping

USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap

BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI *

Intel Anti-Theft Technology

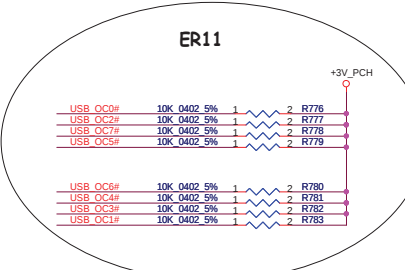
NV_ALE	High-Enabled
Low=Disable(floating) *	

NV_ALE @R228 1 2 1K 0402 5%

USB2/3 port 1
USB2/3 port 2

Mini Card(WLAN) Bluetooth

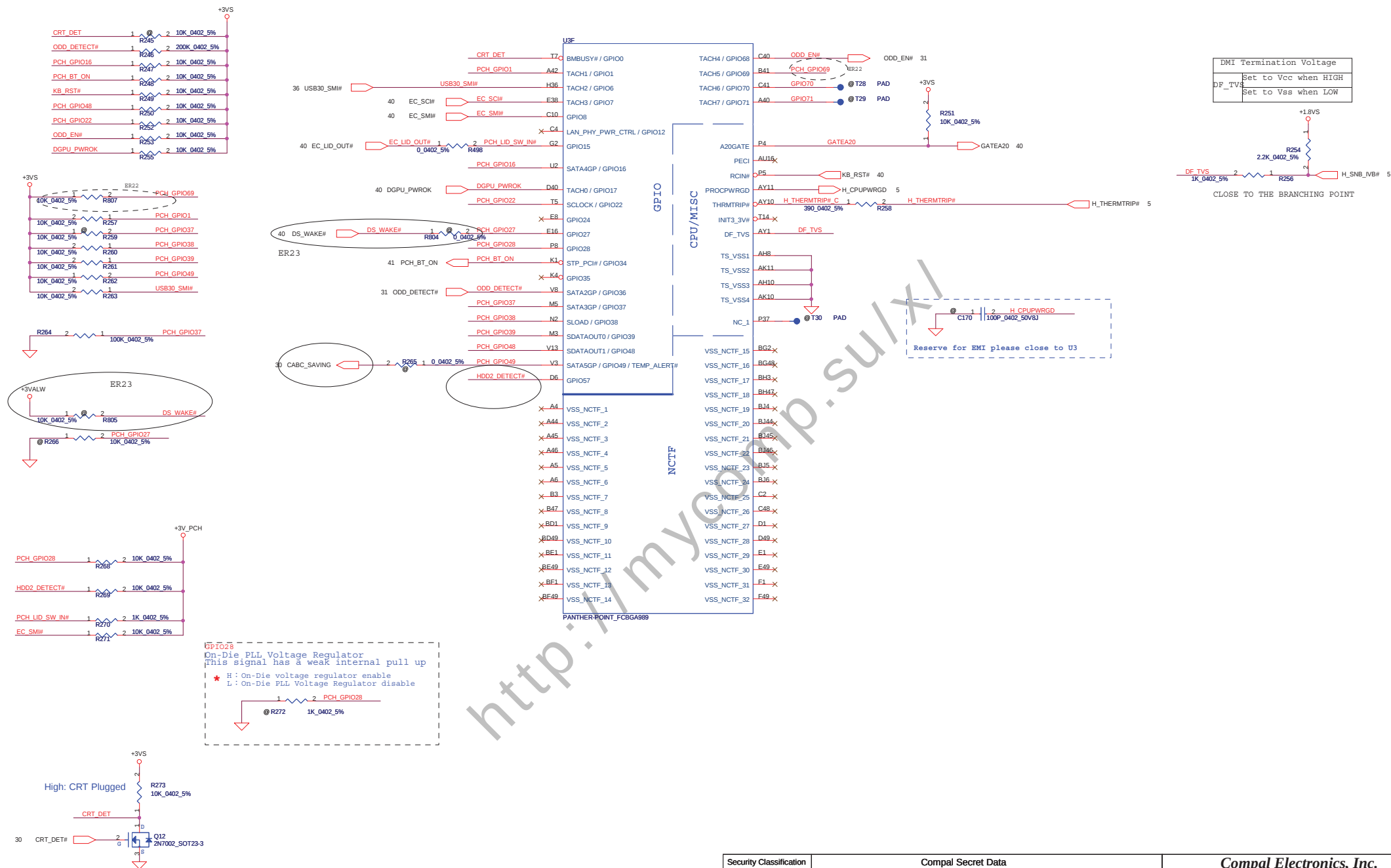
Camera
USB2 Conn. R
Card Reader



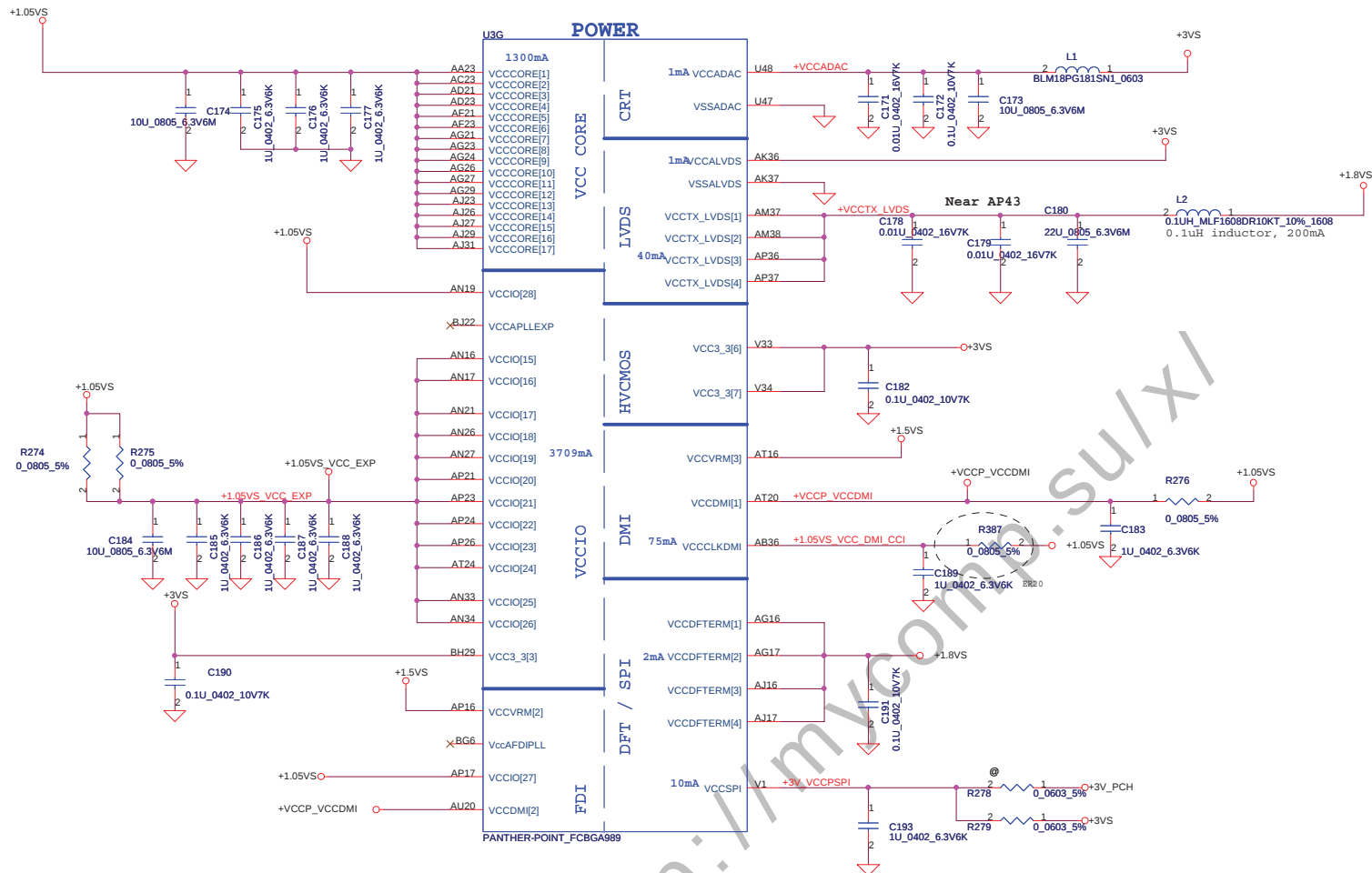
Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13

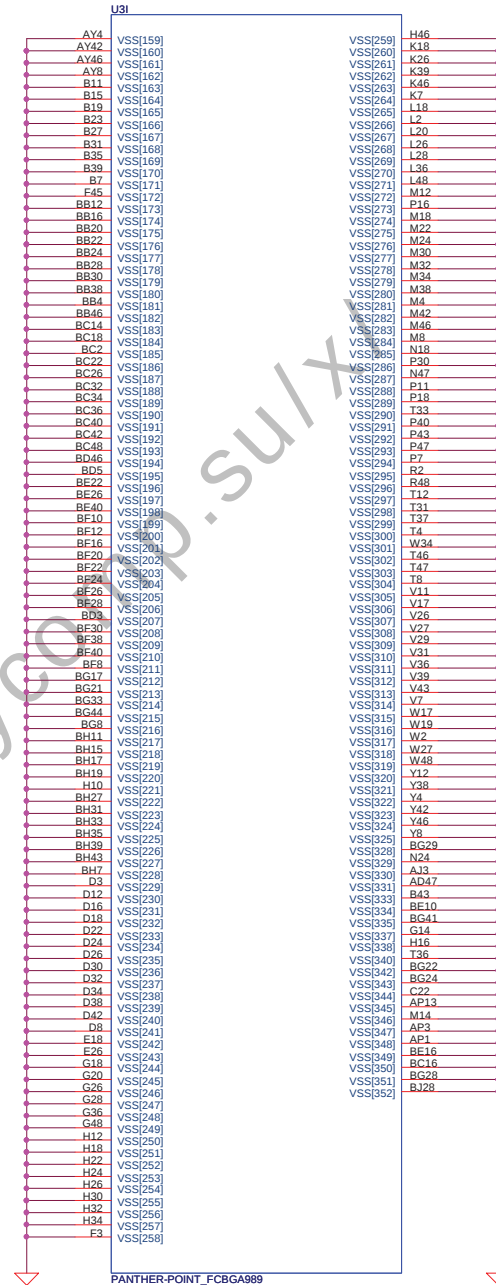
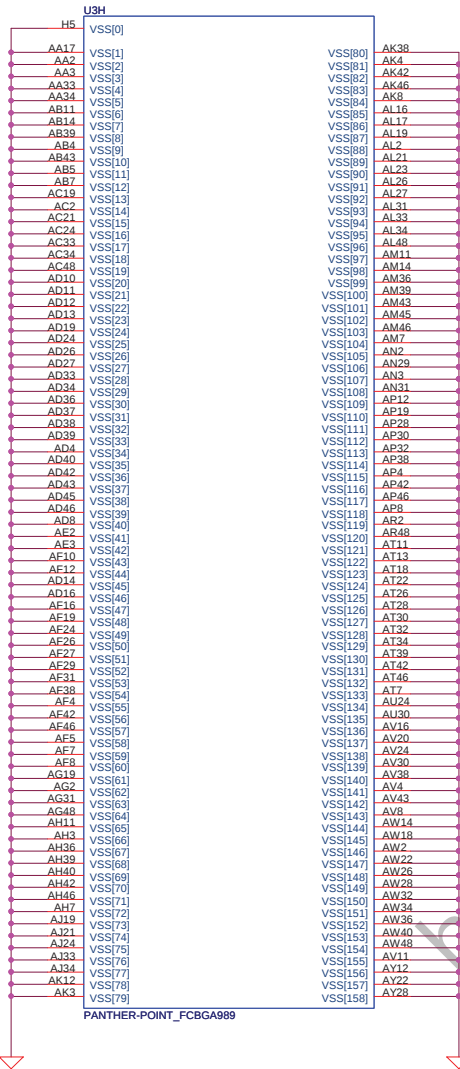


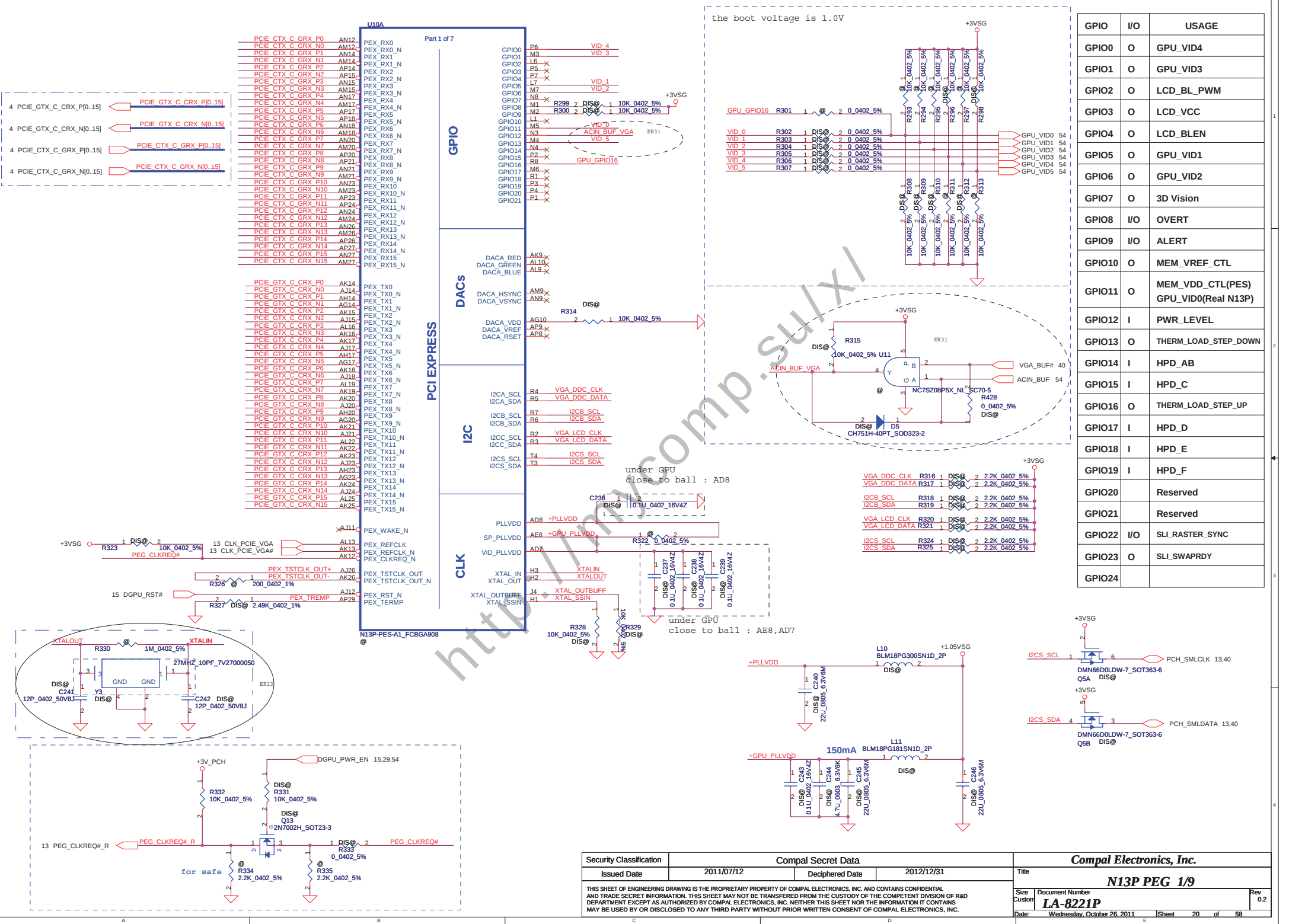


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PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

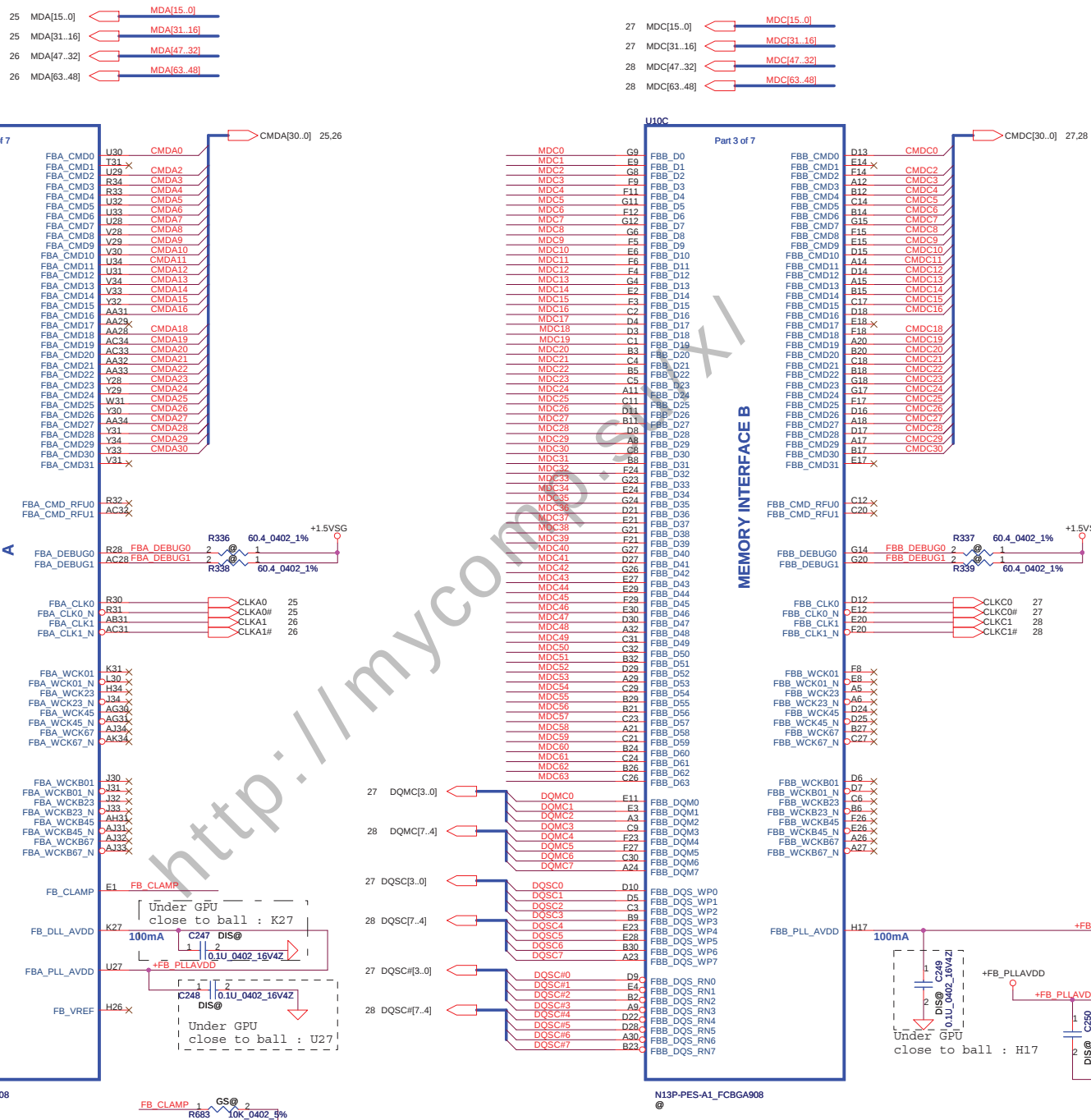




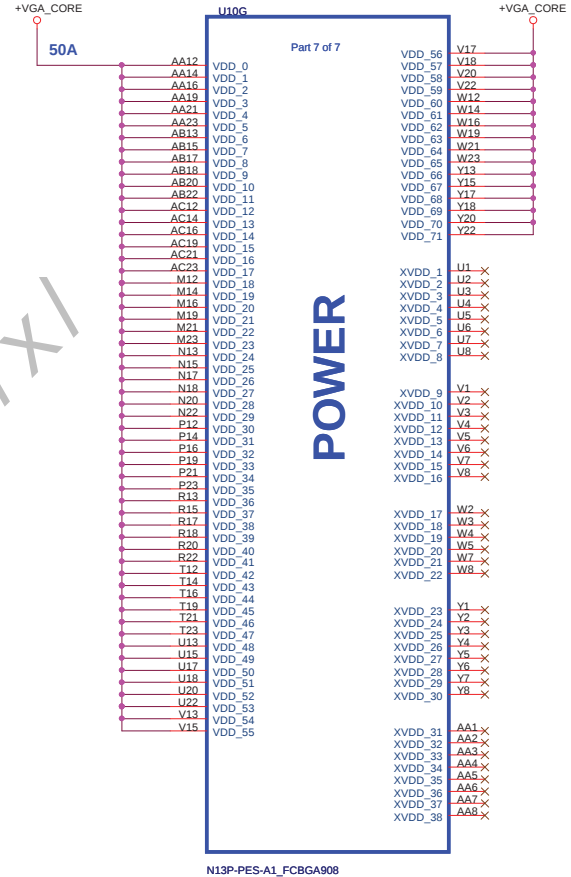
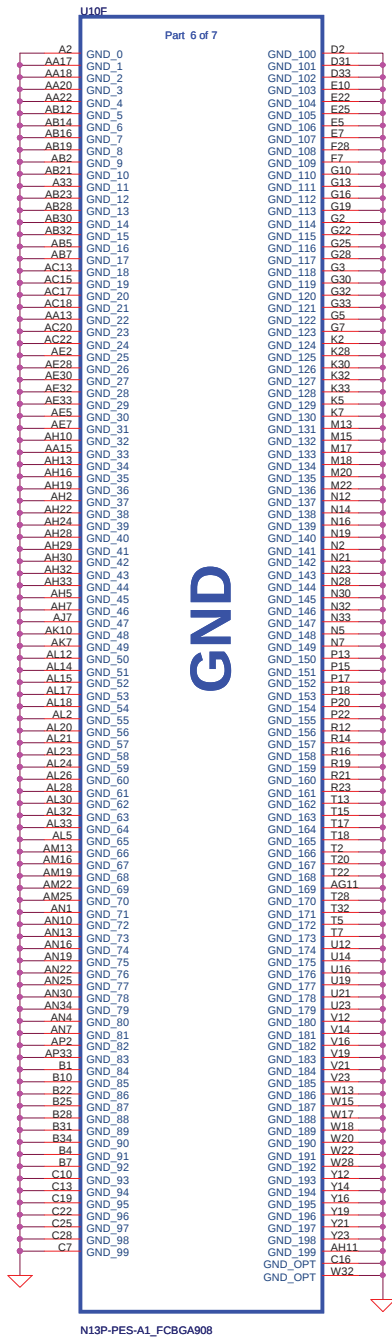
GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

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VRAM Interface



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				LA-8221P			0.2
				Date:	Wednesday, October 26, 2011	Sheet	21

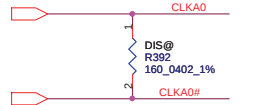
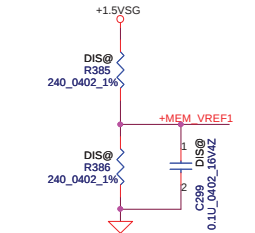
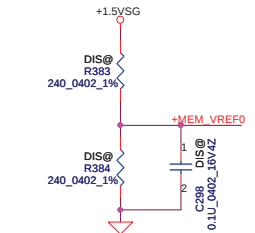


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				Size	Document Number		Rev 0.2
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				Sheet	24 of 58		

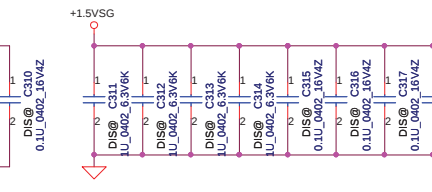
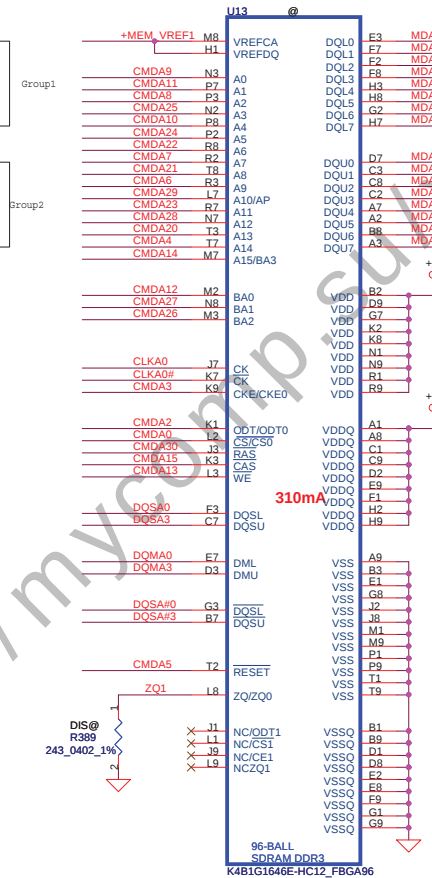
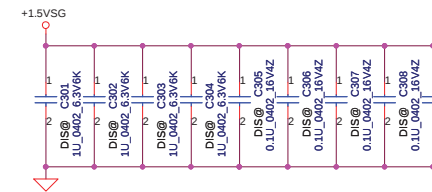
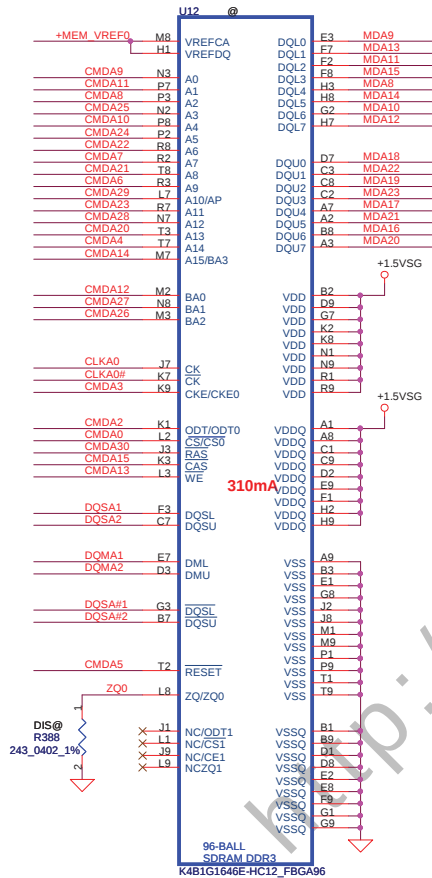
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

21.26 DQSA[7..0] DQSA[7..0]
21.26 DQSA[17..0] DQSA[17..0]
21.26 DQMA[7..0] DQMA[7..0]
21.26 MDA[63..0] MDA[63..0]
21.26 CMDA[30..0] CMDA[30..0]



NV recommend 0720



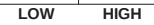
CMDA2	R390	DIS@	2	10K	0402	5%
CMDA3	R391	DIS@	2	10K	0402	5%
CMDA5	R393	DIS@	2	10K	0402	5%
CMDA18	R394	DIS@	2	10K	0402	5%
CMDA19	R395	DIS@	2	10K	0402	5%

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD : SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		ODT_H
CMD18		CKE_H
CMD19		
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

128Mx16 DDR3 *8==>2GB

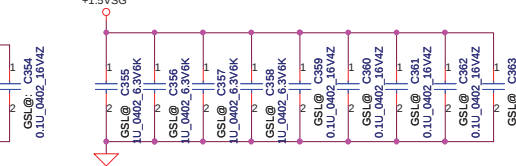
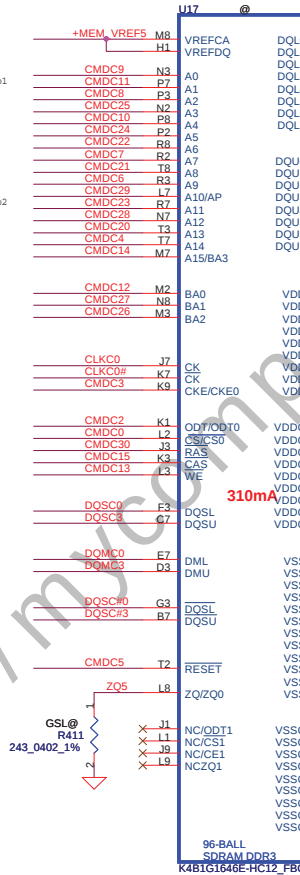
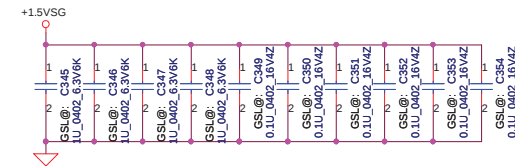
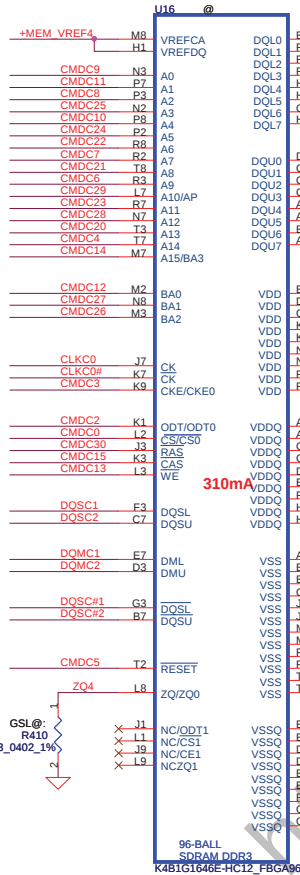
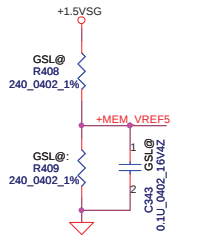
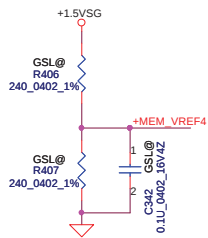


VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB

21.28 DQSC[7..0] DQSC[7..0]
21.28 DQSC# [7..0] DQSC# [7..0]
21.28 DQMC[7..0] DQMC[7..0]
21.28 MDC[63..0] MDC[63..0]
21.28 CMDC[30..0] CMDC[30..0]



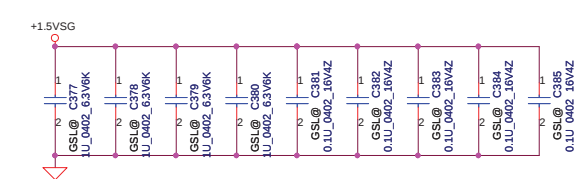
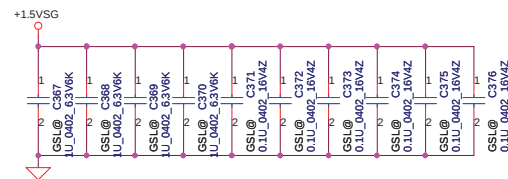
CMDC2 R412 1 GSL@ 2 10K 0402 5%
CMDC3 R413 1 GSL@ 2 10K 0402 5%
CMDC5 R414 1 GSL@ 2 10K 0402 5%
CMDC18 R415 1 GSL@ 2 10K 0402 5%
CMDC19 R416 1 GSL@ 2 10K 0402 5%

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

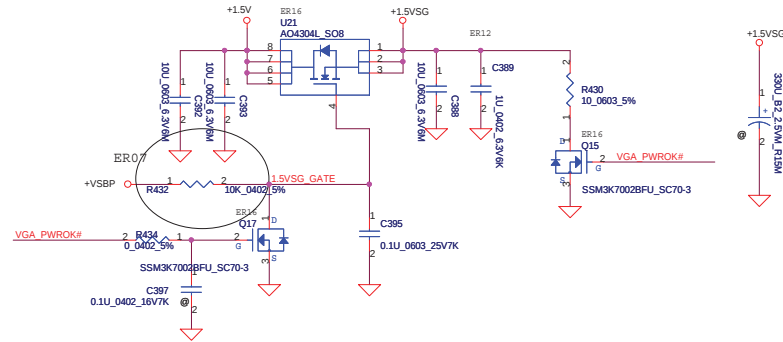
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				Date	Wednesday, October 26, 2011
				Sheet	27 of 58
				Rev	0.2

128Mx16 DDR3 *8==>2GB

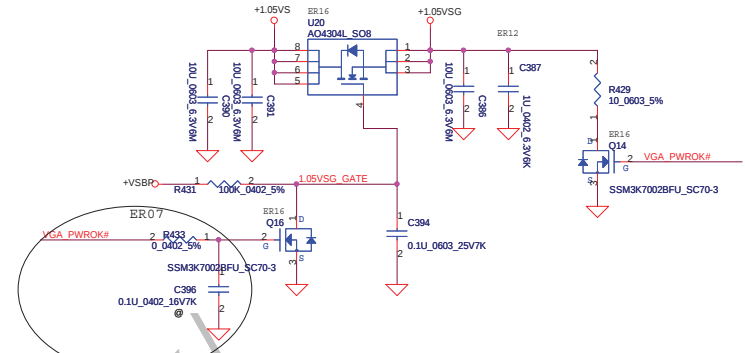


LOW HIGH

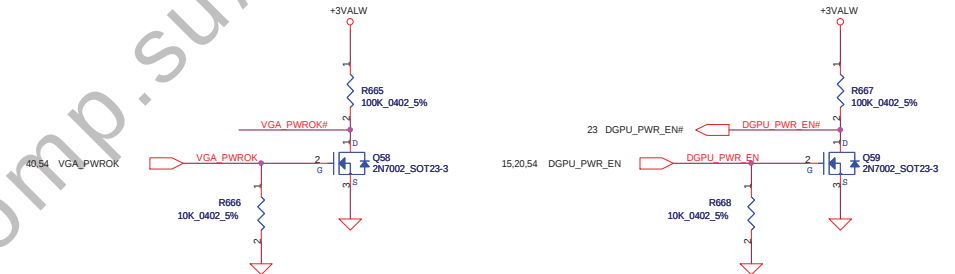
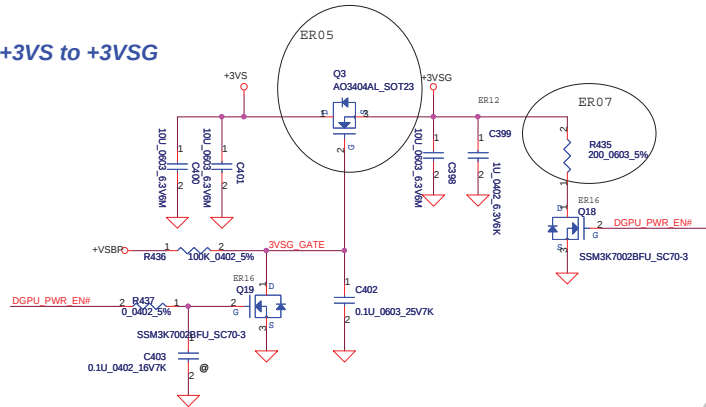
+1.5V to +1.5VSG



+VCCP to +1.05VSG

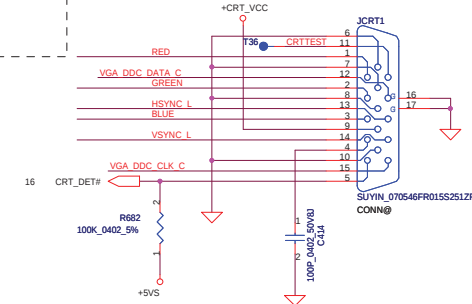
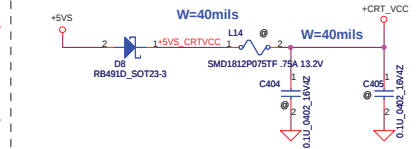
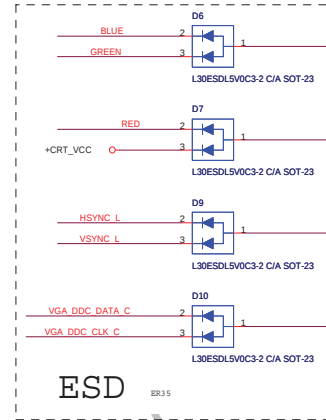
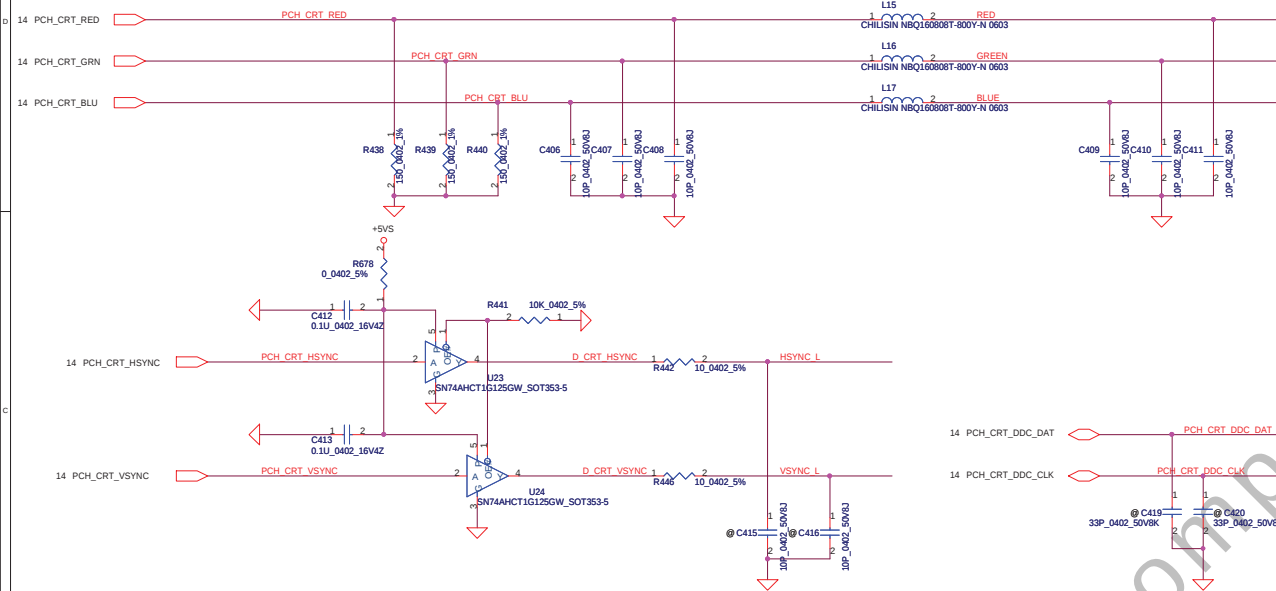


+3VS to +3VSG

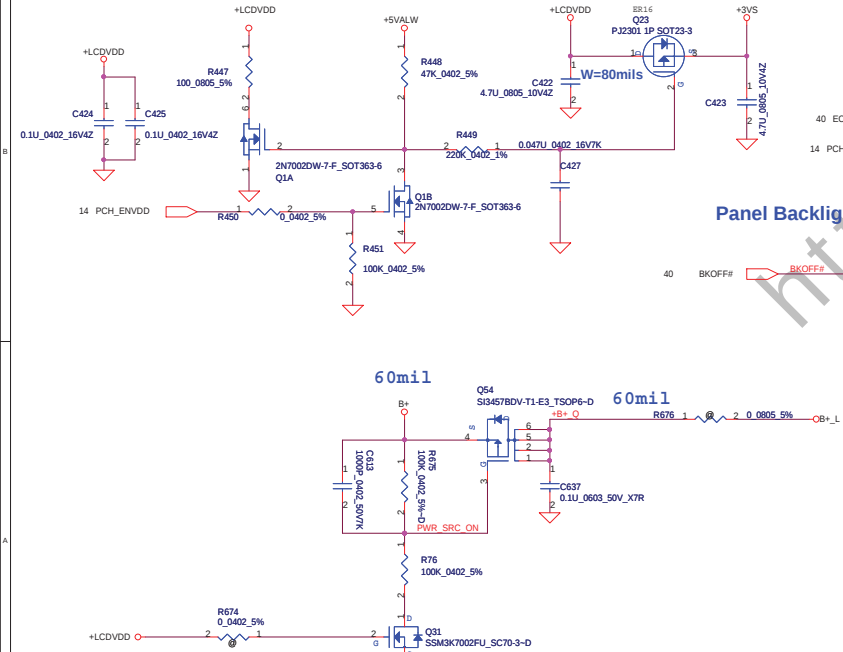


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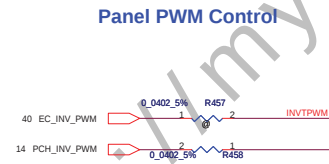
CRT



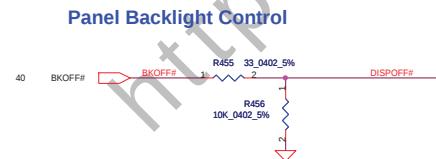
LCD POWER CIRCUIT



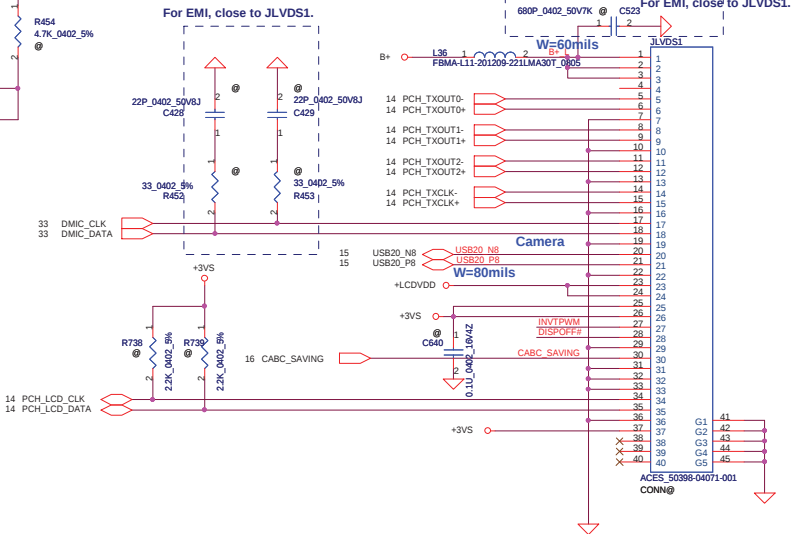
Panel PWM Control



Panel Backlight Control

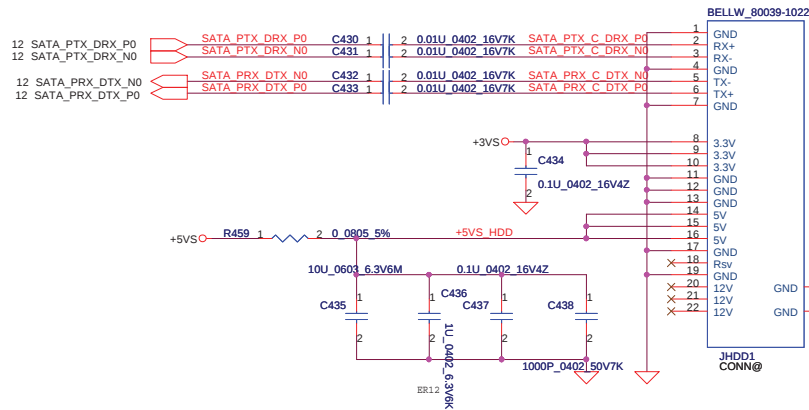


For EMI, close to JLVDS1.

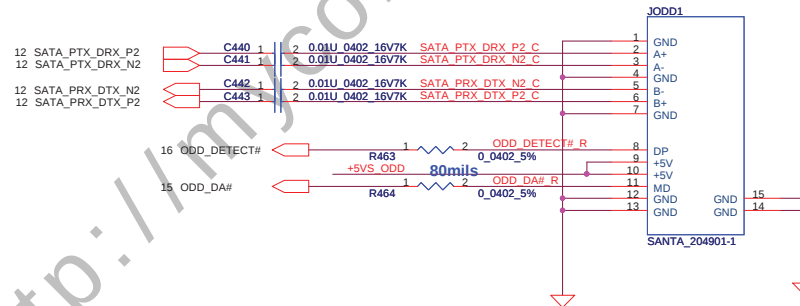


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Size	Document Number	Rev		0.2
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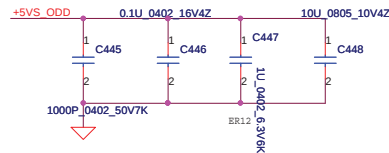
SATA HDD Conn.



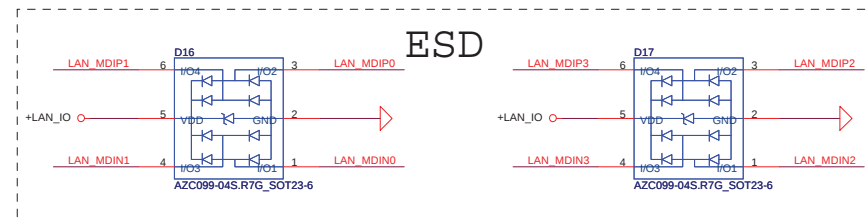
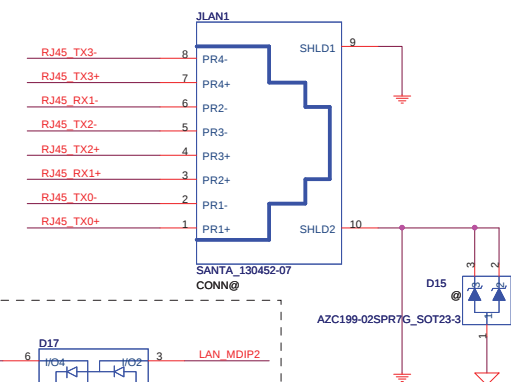
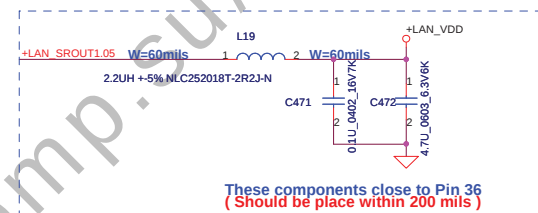
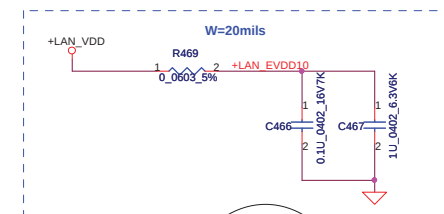
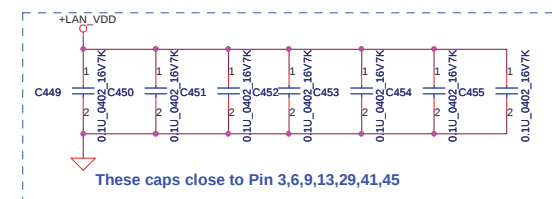
SATA ODD Conn.



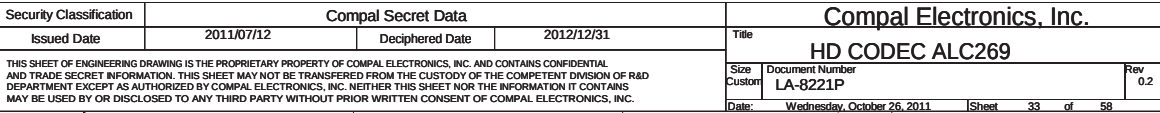
Place caps. near ODD CONN.

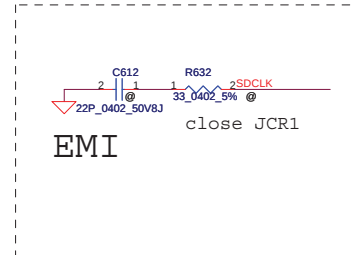
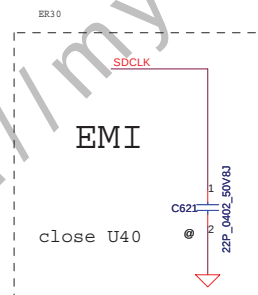
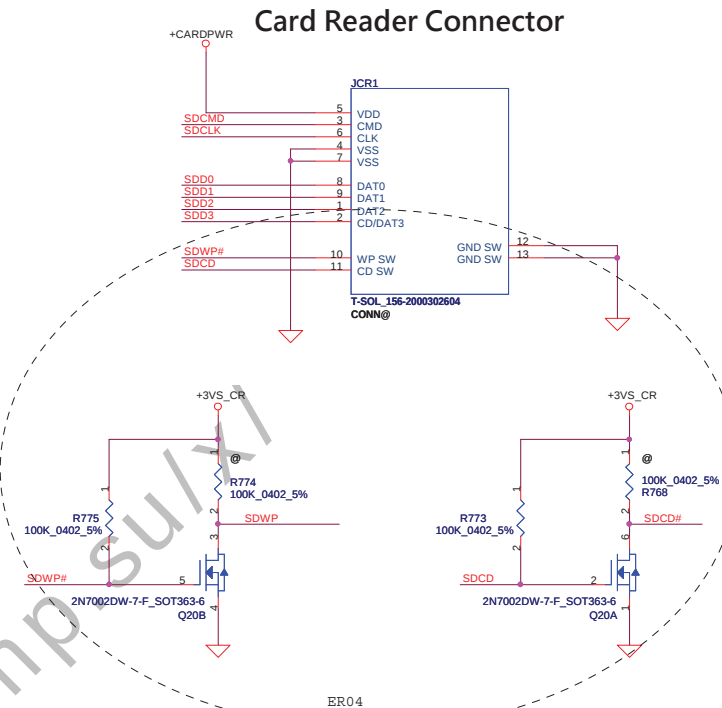
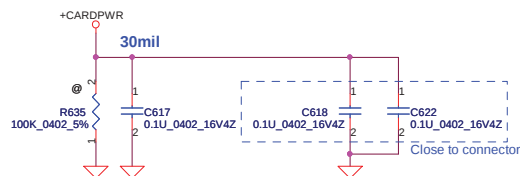
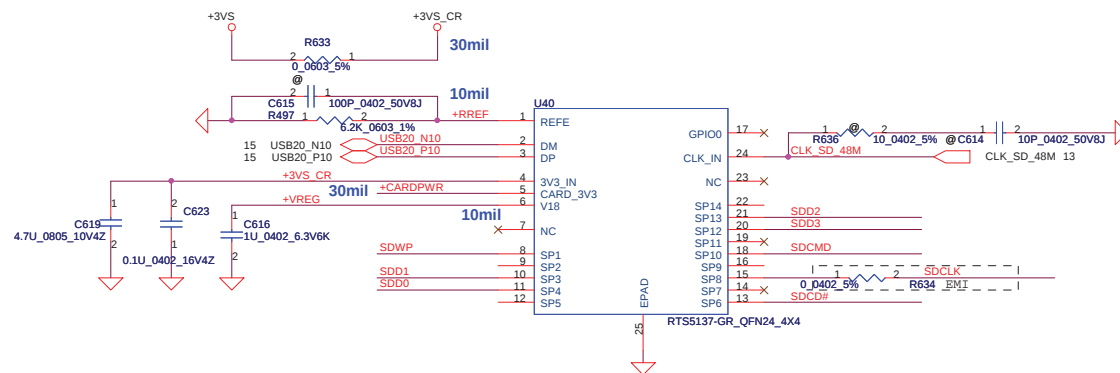


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				Date: Wednesday, October 26, 2011	Sheet 31 of 58

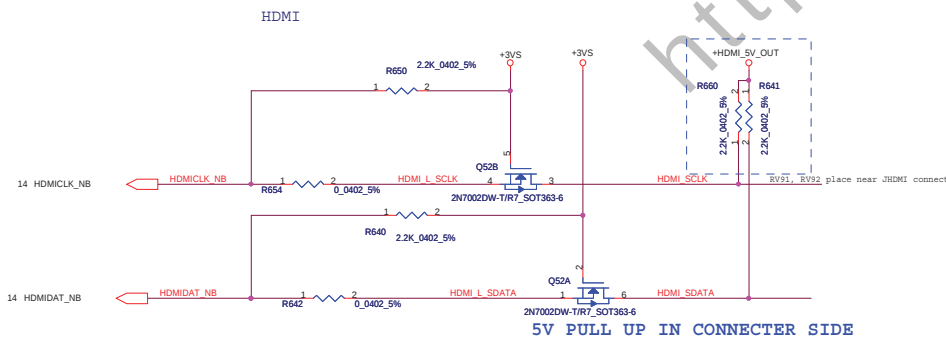
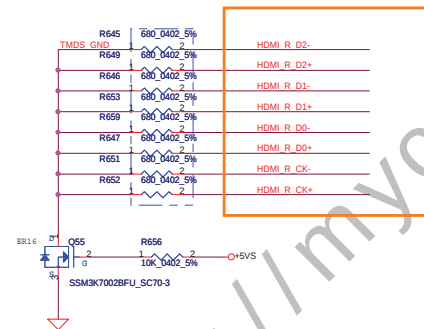
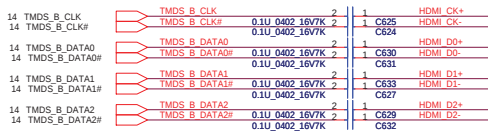
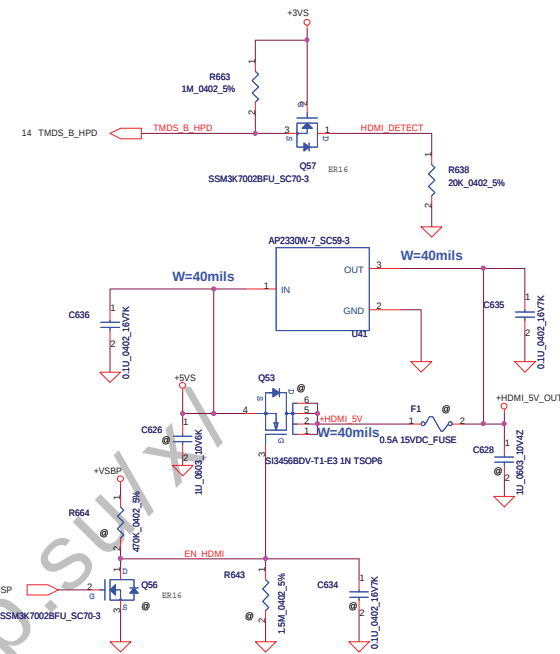
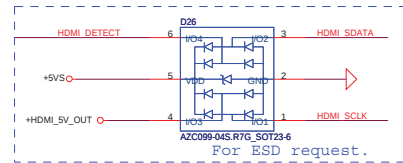


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5V PULL UP IN CONNECTER SIDE

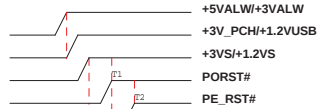
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title	HDMI Connector	
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				LA-8221P		0.2
				Date:	Wednesday, October 26, 2011	Sheet

ER02 Add USB3.0 (ASM1042)

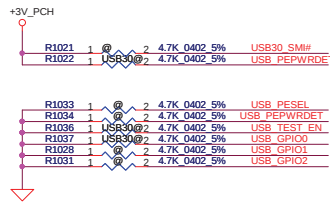
	S3	S4/S5
+3V_PCH	V	X
+3VS	X	X
+1.2VUSB	V	X
+1.2VS	X	X

Power Sequence

ASM1042



T1: 2-80ms
T2: >200ms



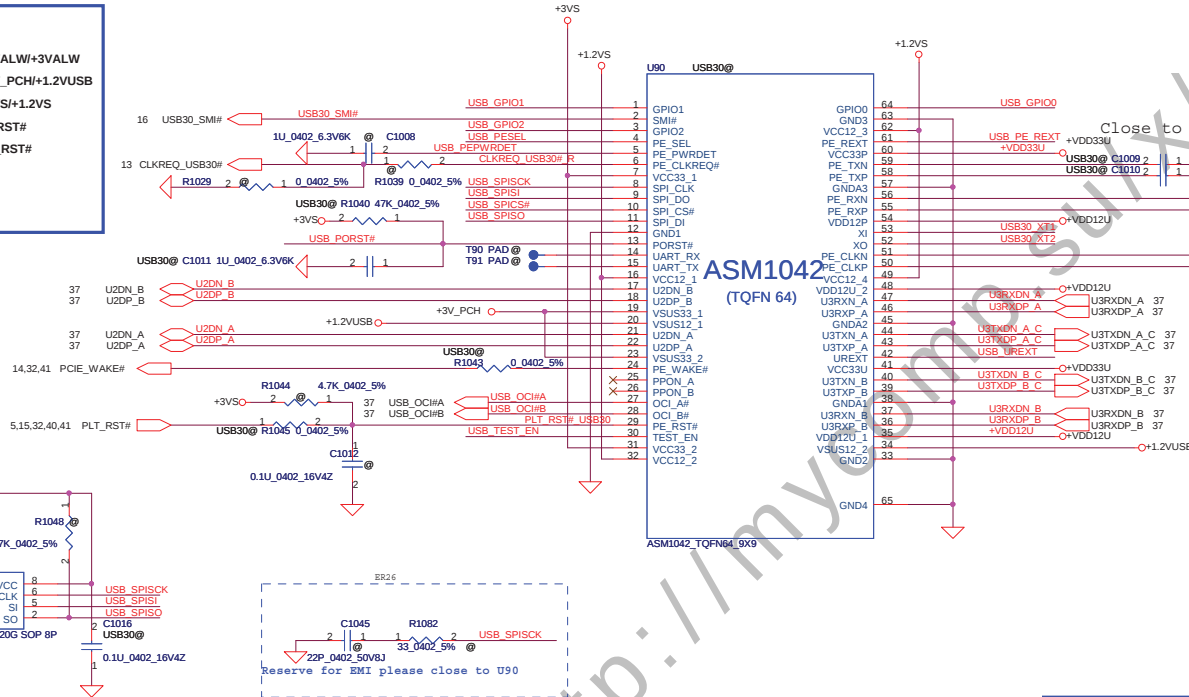
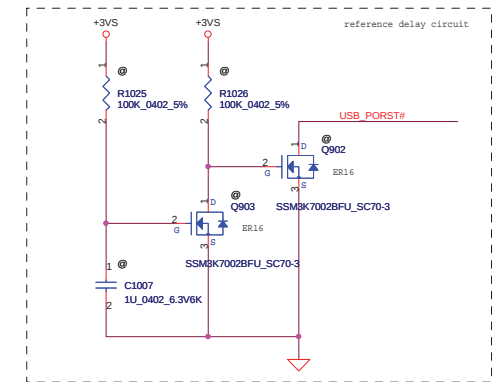
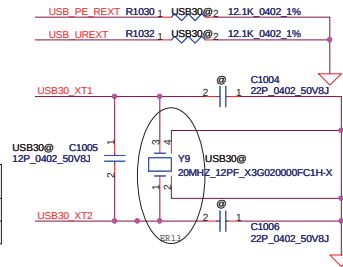
For WAKE Function

USB_PEPWRDET

	R1034	R1022
S1	Mount	@
* S3	@	Mount

USB_PESL

	R1033
* Other application	@
Express Card/Mini Card	Mount



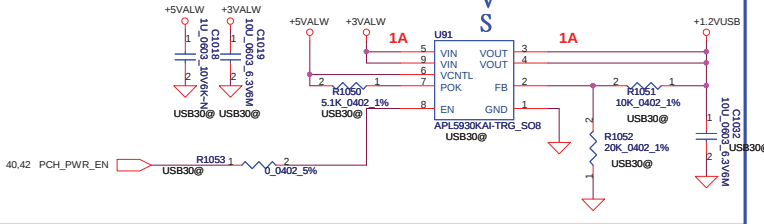
ASM1042 (TQFN 64)

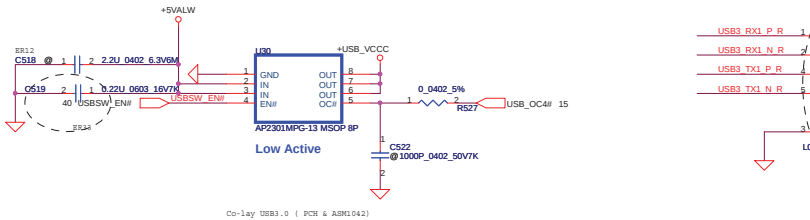
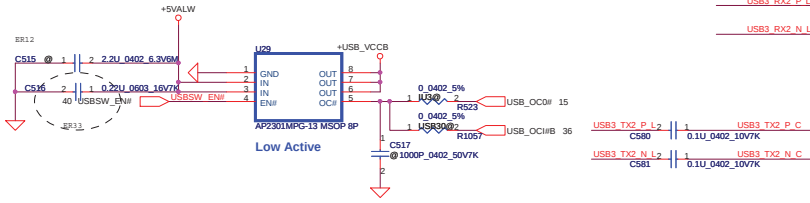
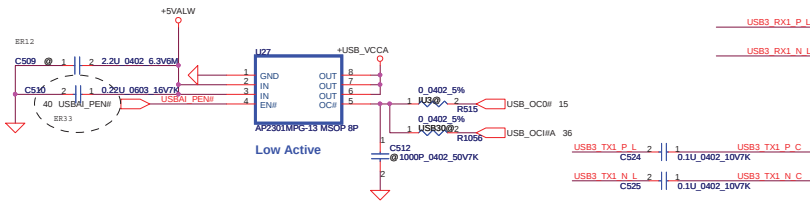
ASM1042 TQFN64 0X9

Close to ASM1042

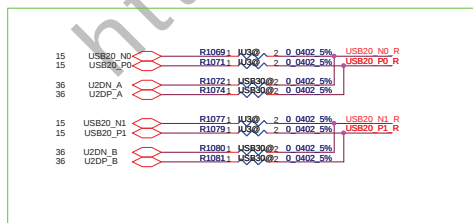
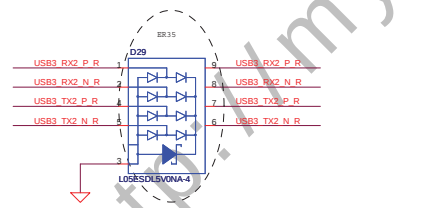
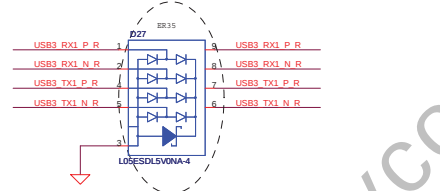
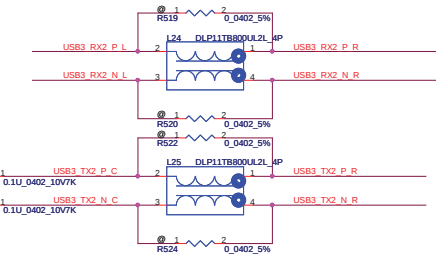
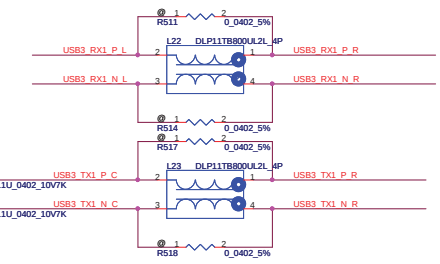
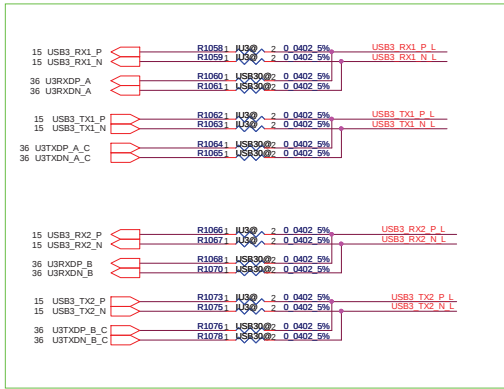
+1.2VUSB

+3VALW to +1.2V Transfer

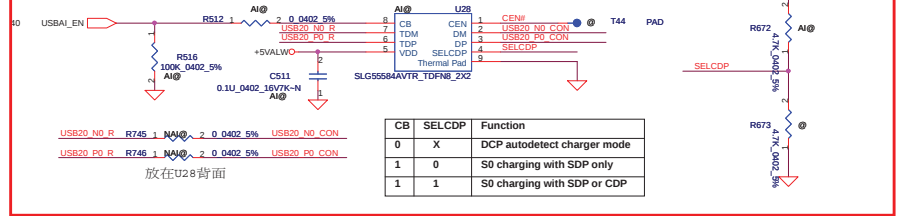




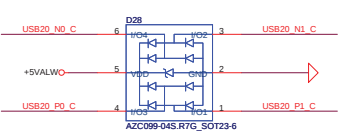
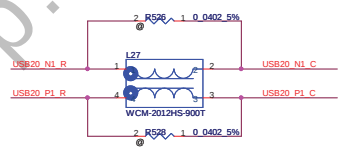
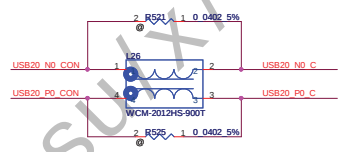
Co-Lay USB3.0 (PCH & ASM1042)



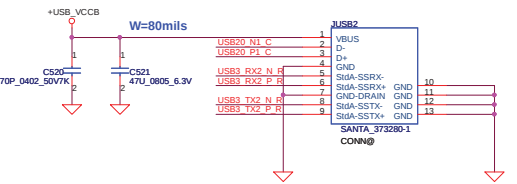
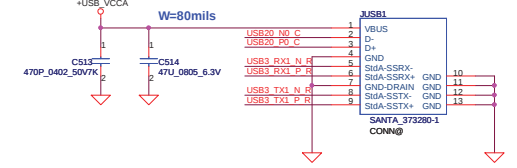
AI CHARGER



放在U28背面



charger port: left side & near user

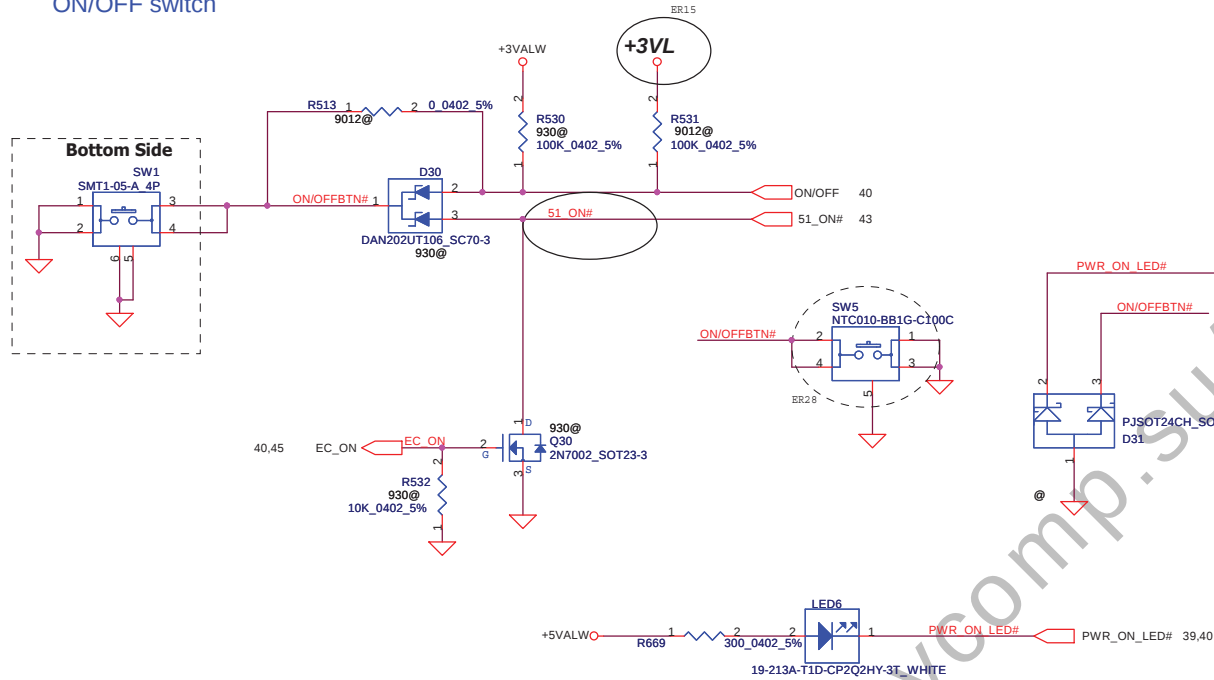


ER02 Add USB3.0 (ASM1042)

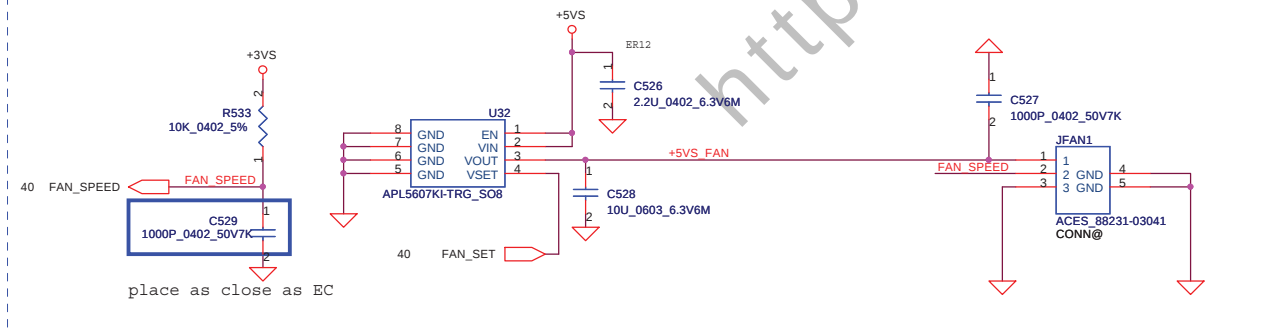
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Issued Date	2011/07/12	Deciphered Date	2012/12/31	Title
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Power Button

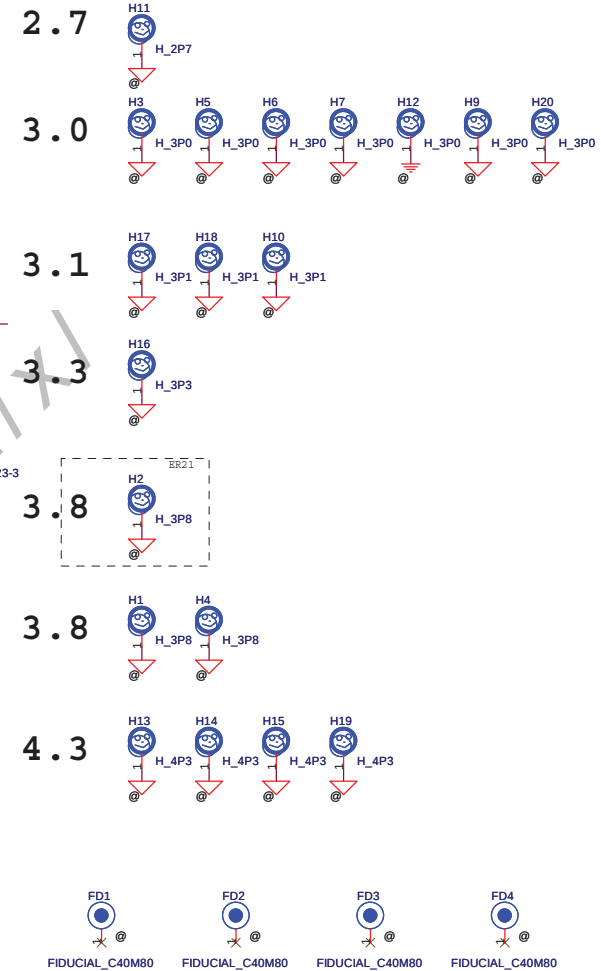
ON/OFF switch



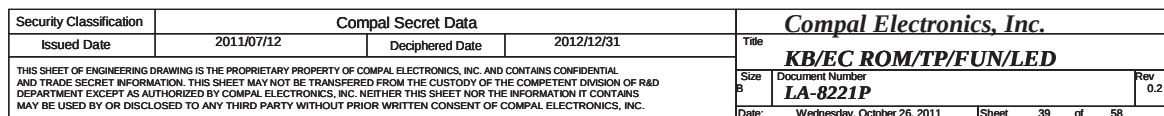
Fan Control Circuit

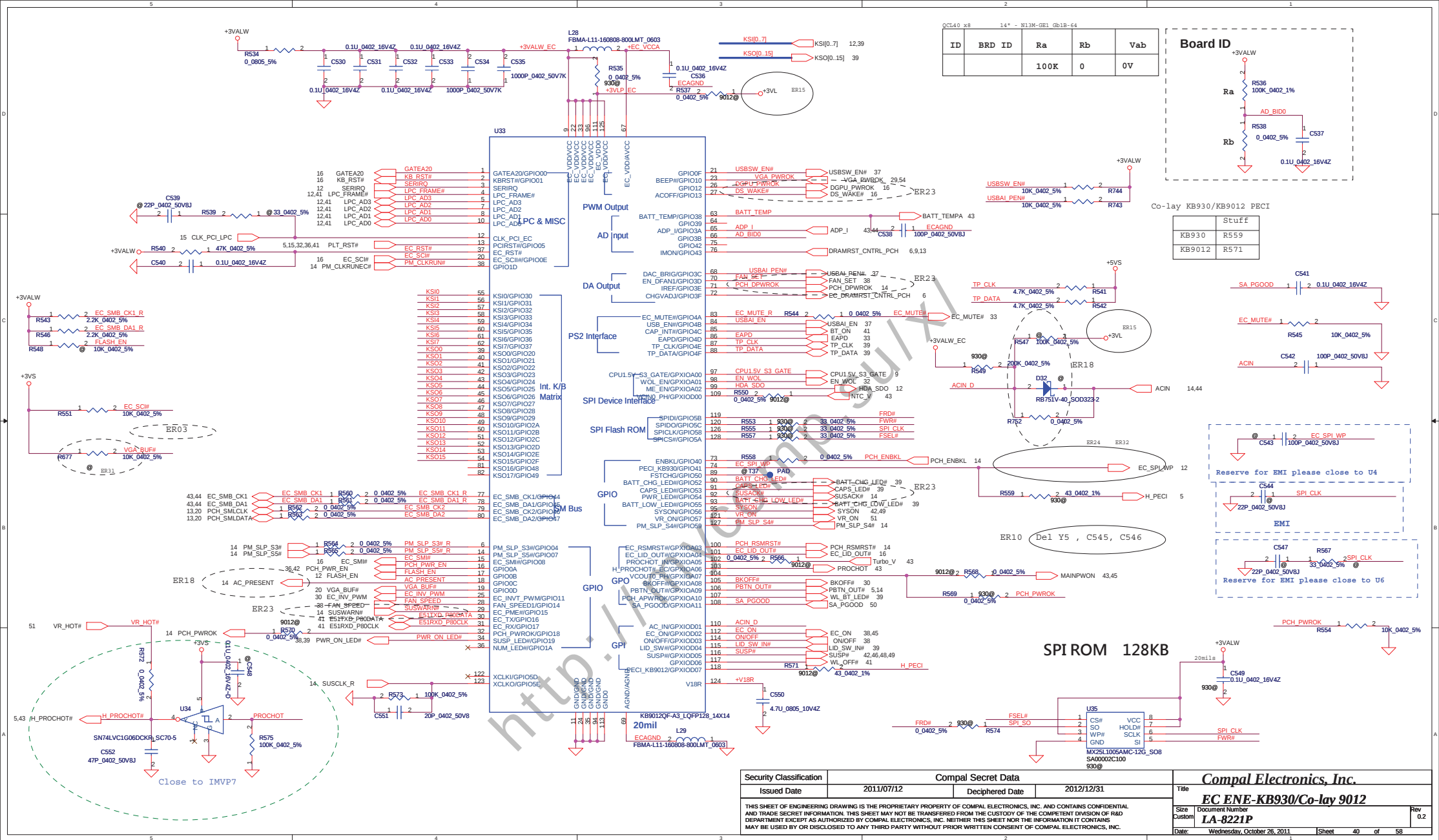


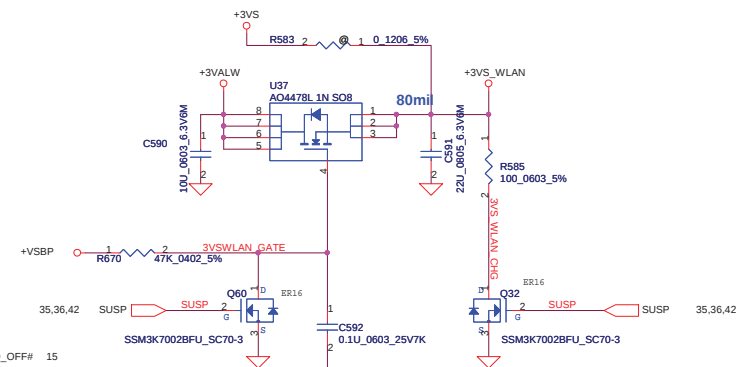
Screw Hole



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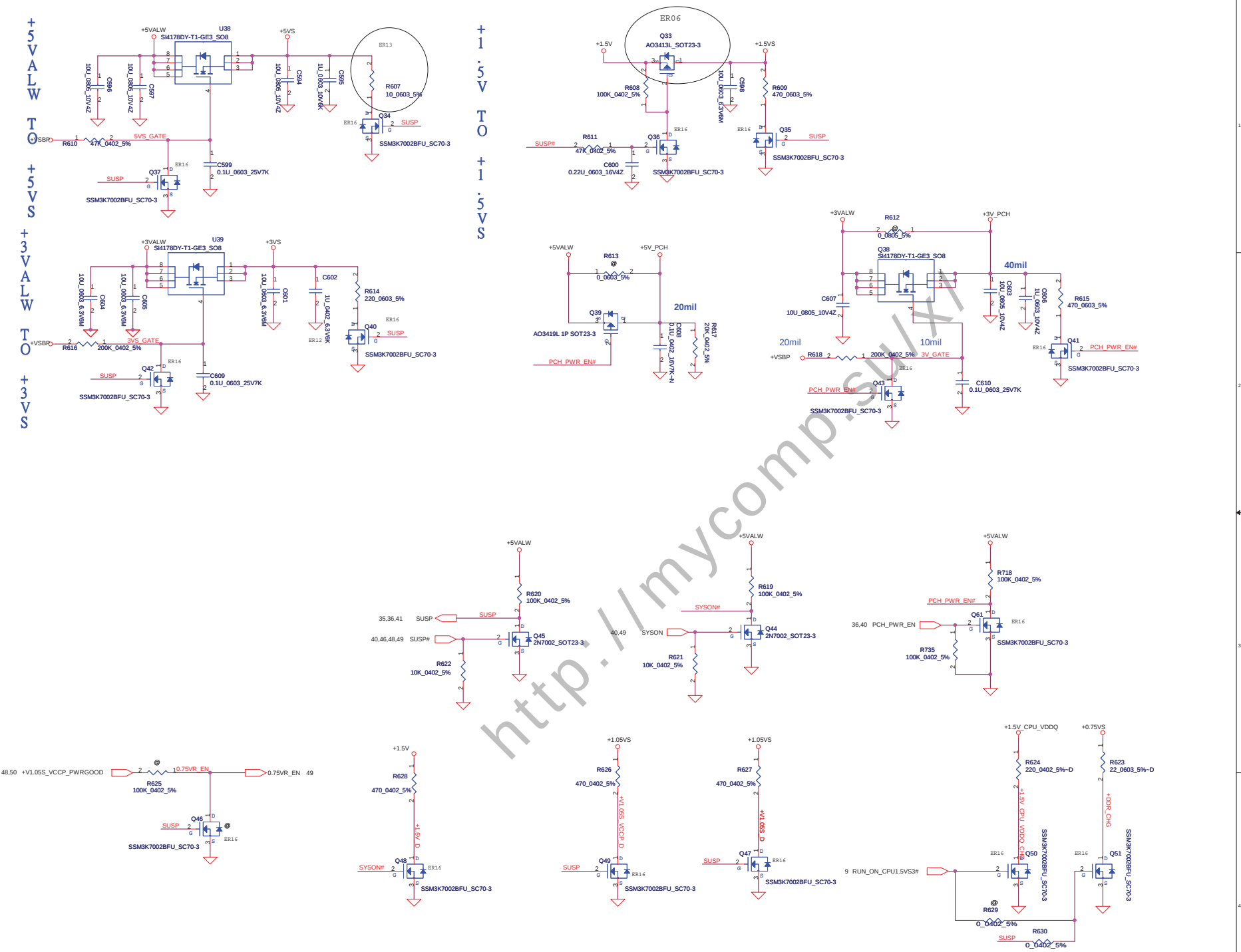


Reserve for EMI please close to JMINI1

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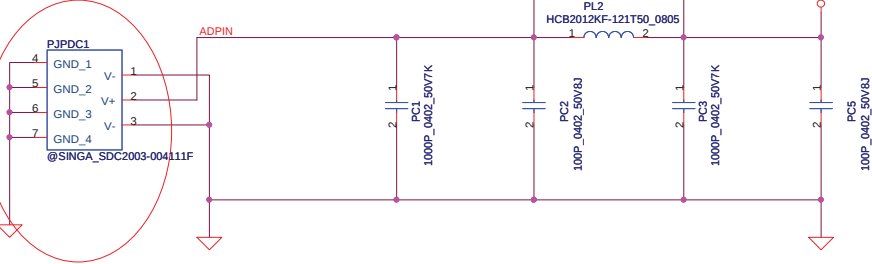
+5VALW
TO
+5VS
+3VALW
TO
+3VS

+1.5V
TO
+1.5VS

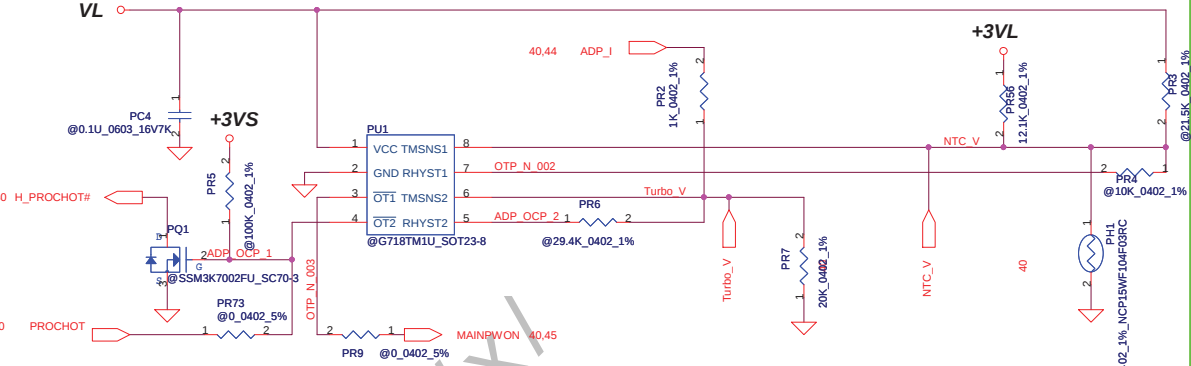


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Size	Custom	Document Number	LA-8221P	Rev 0.2
Date	Wednesday, October 26, 2011	Sheet	42	of 58

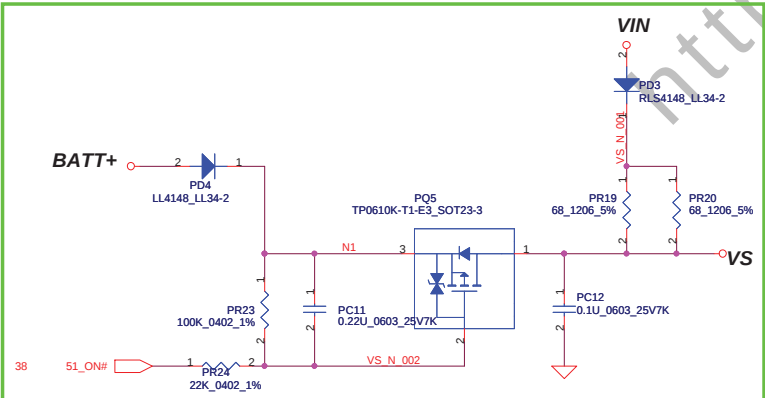
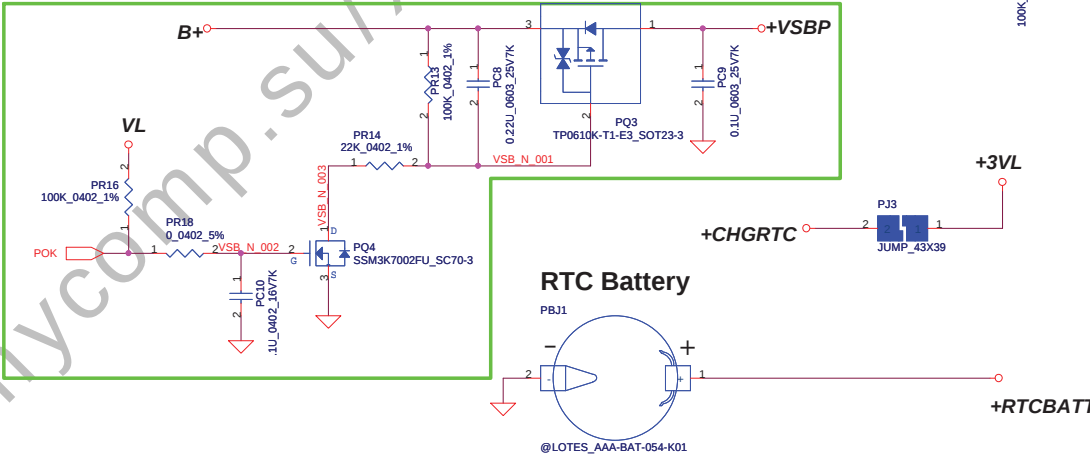
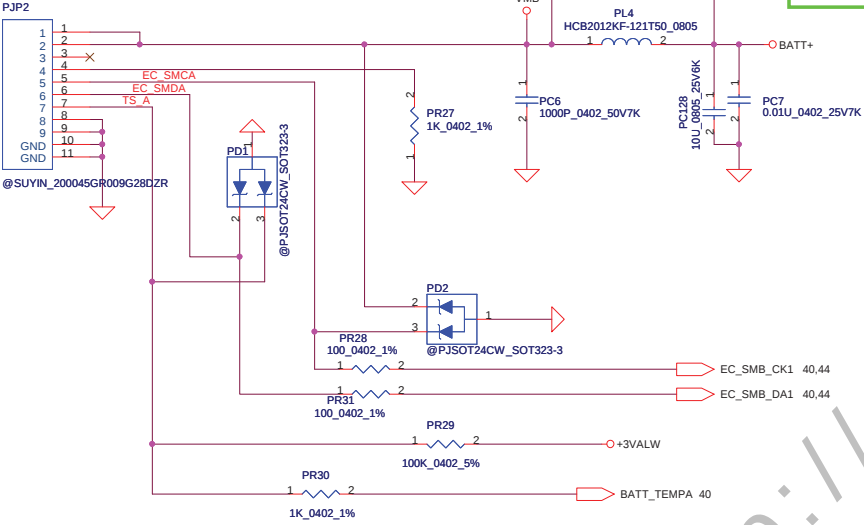
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



PH1 under CPU botten side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



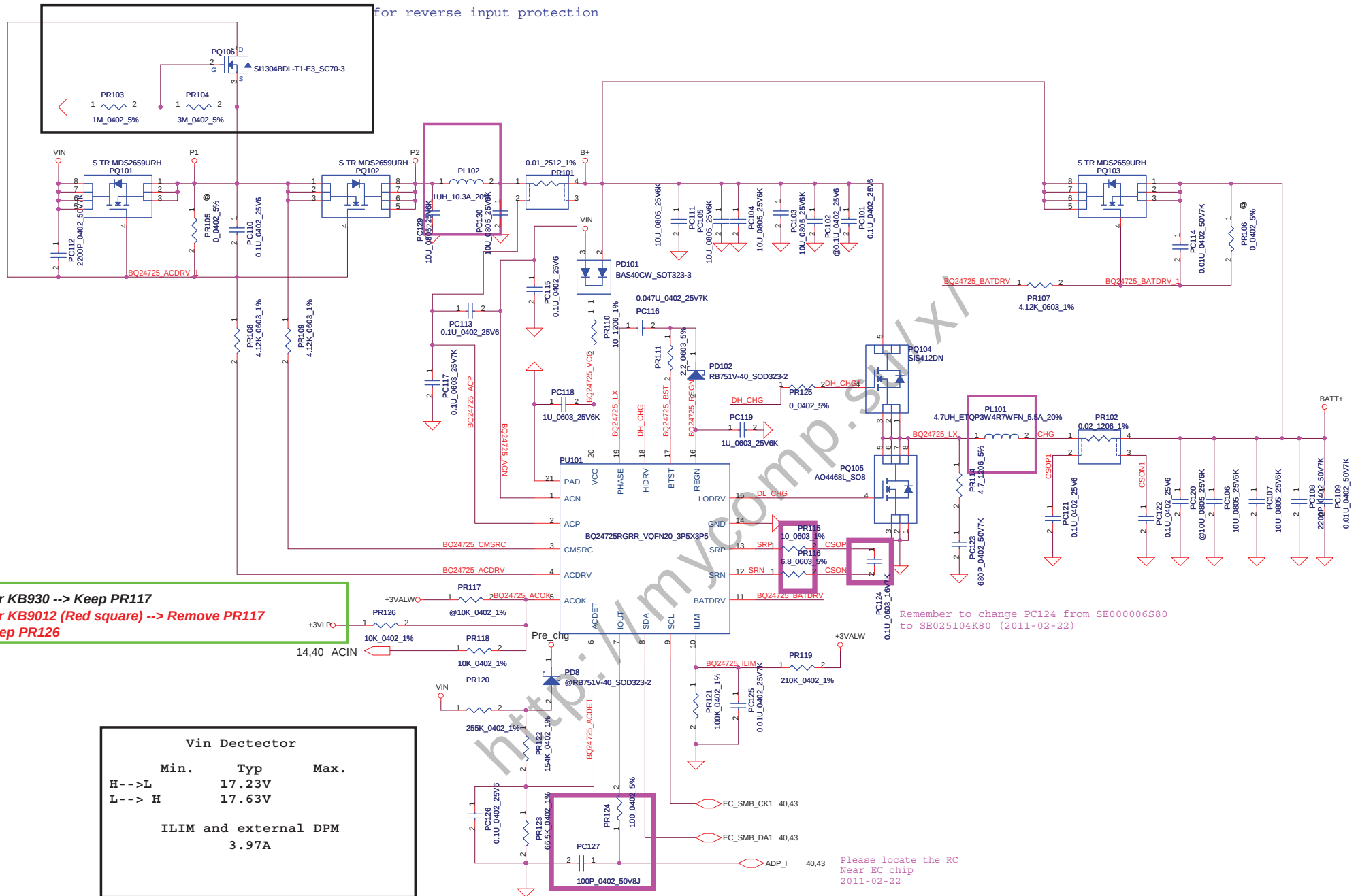
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



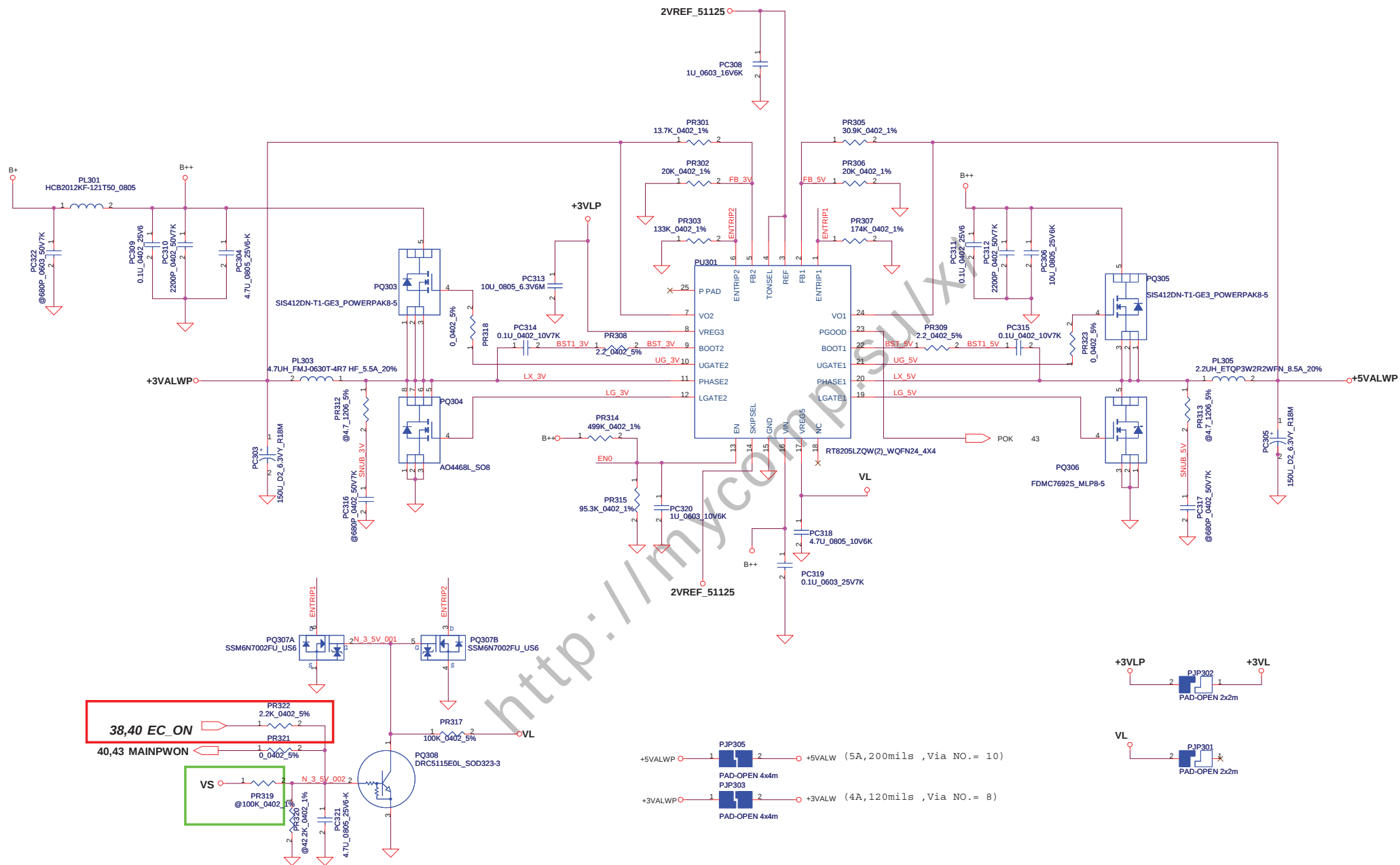
For KB9012 --> Remove all 51_ON# circuit

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Deciphered Date				2010/01/23				PBL22 LA-7391P M/B			
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for reverse input protection

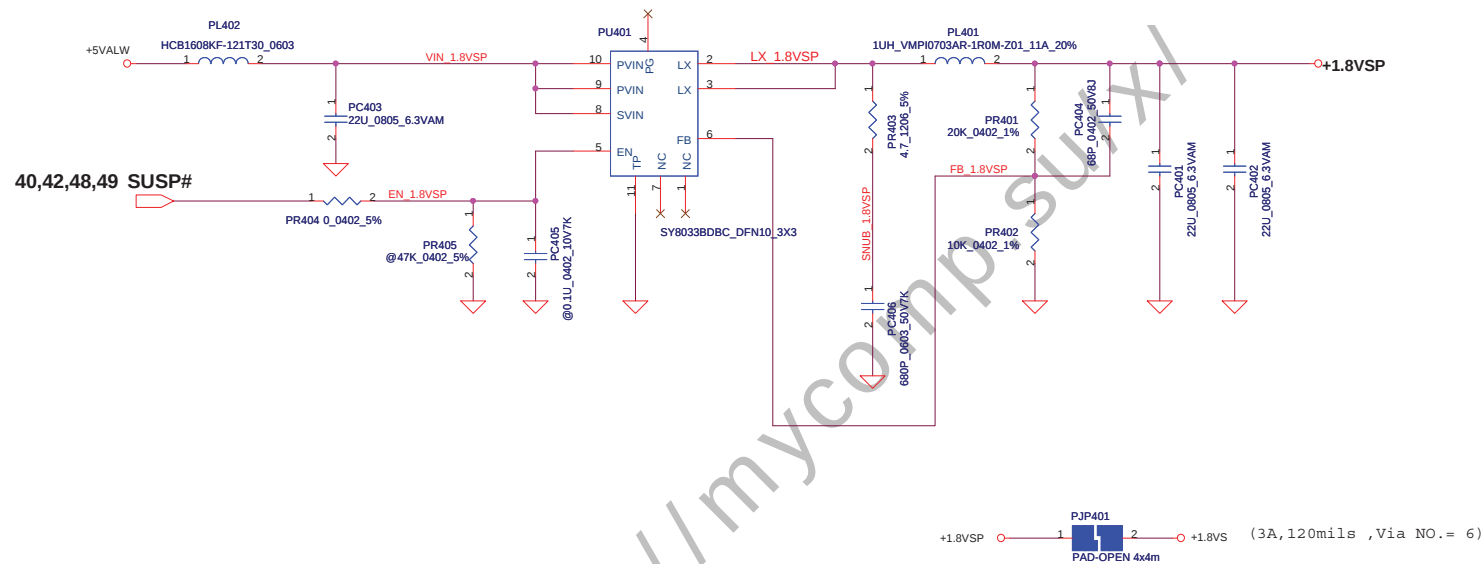


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For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

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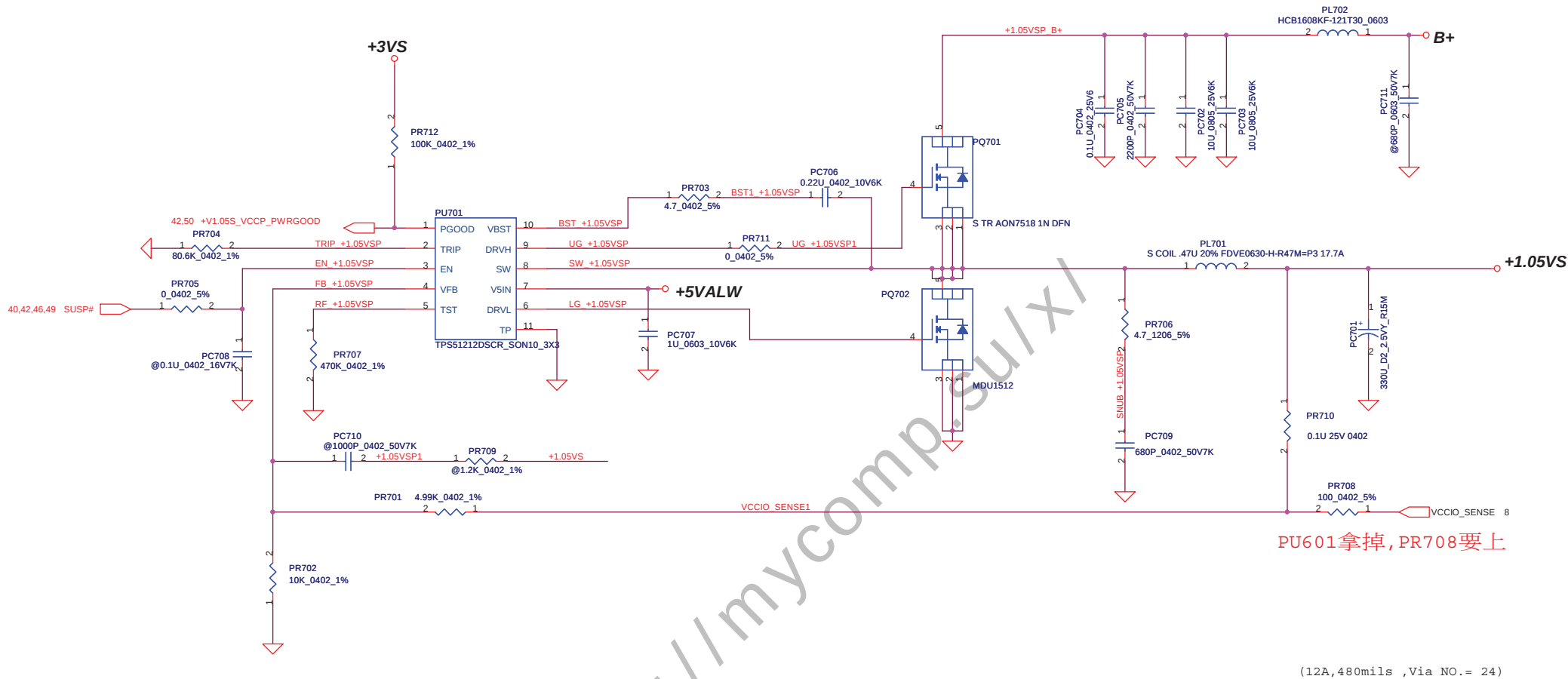
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Issued Date	2009/01/23	Deciphered Date	2012/12/31	Title	
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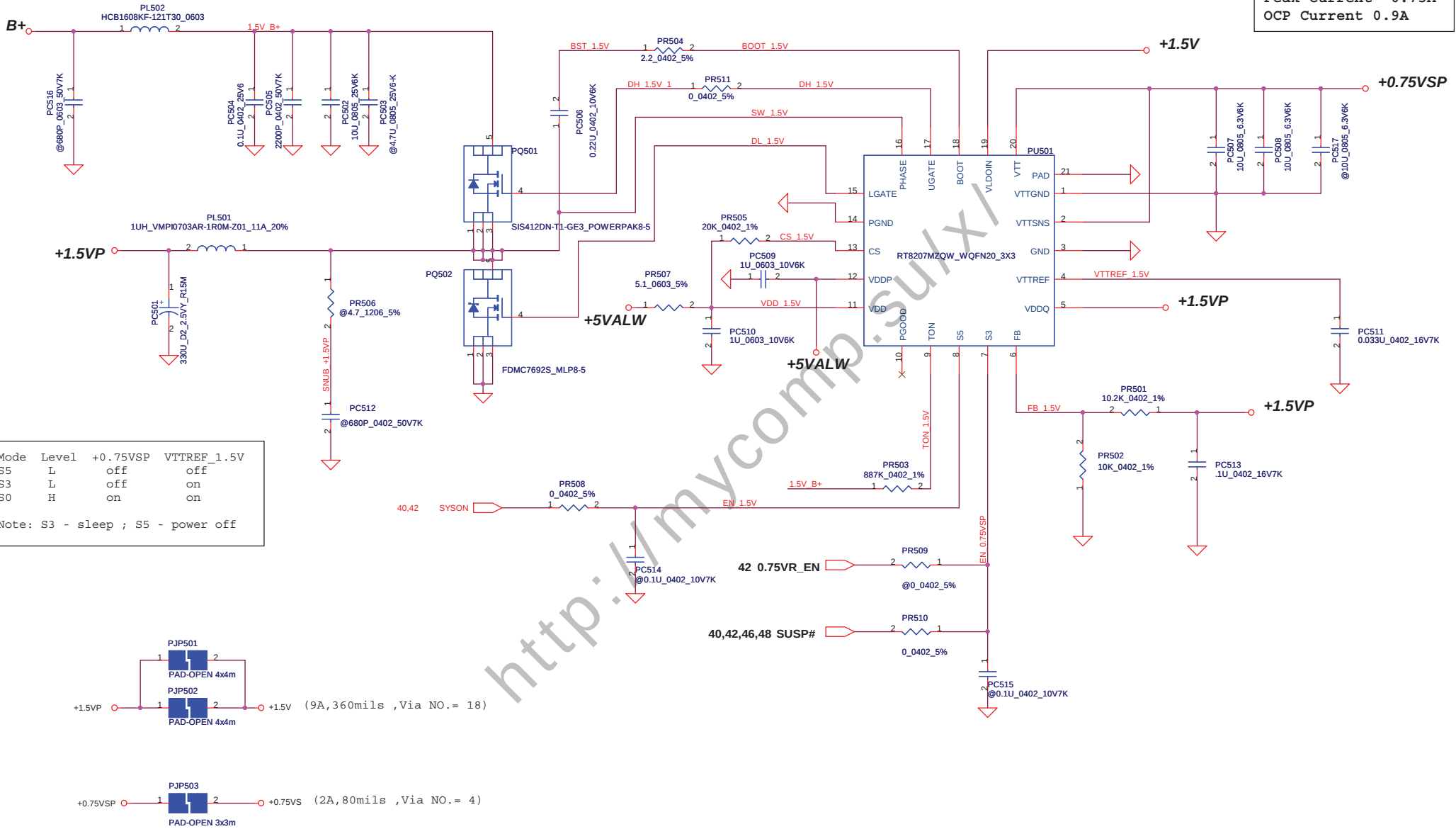
(8.5A,360mils ,Via NO.= 17)

PJP606 ,PJP607先斷開,確定拿掉PU605再接上

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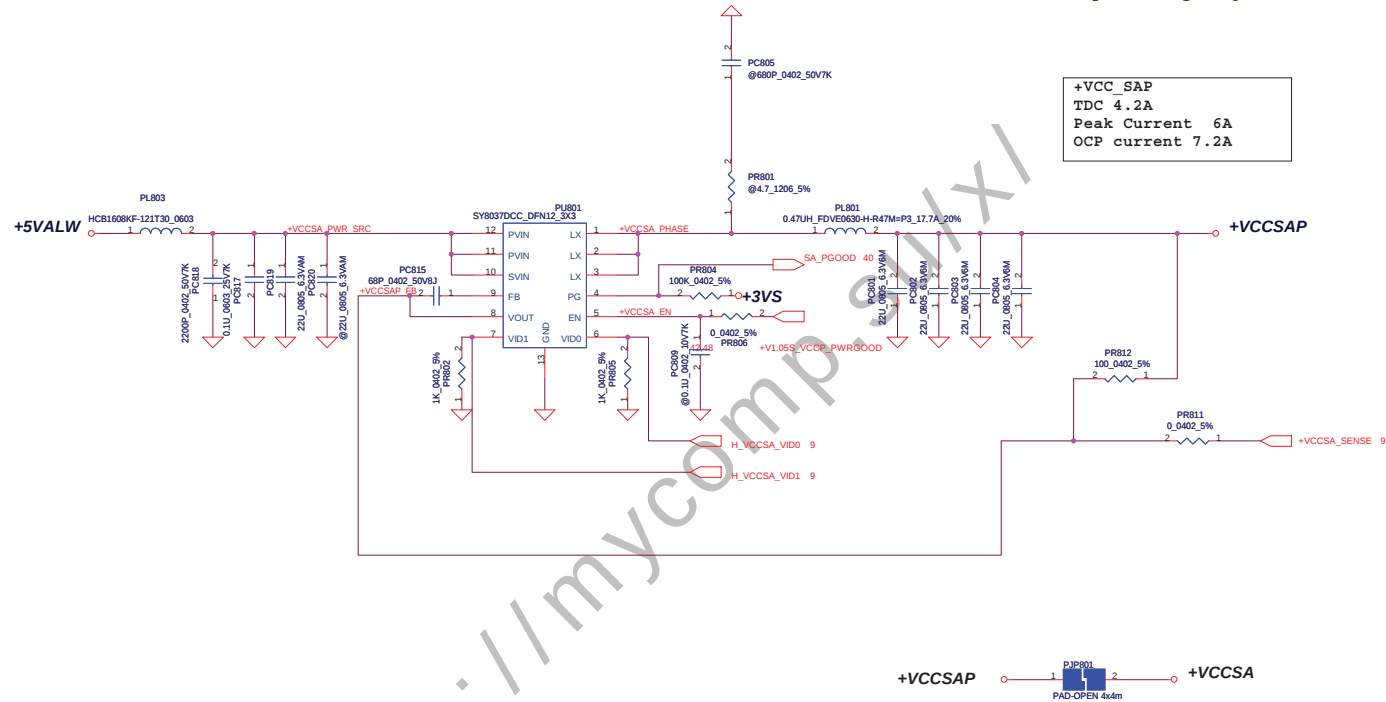


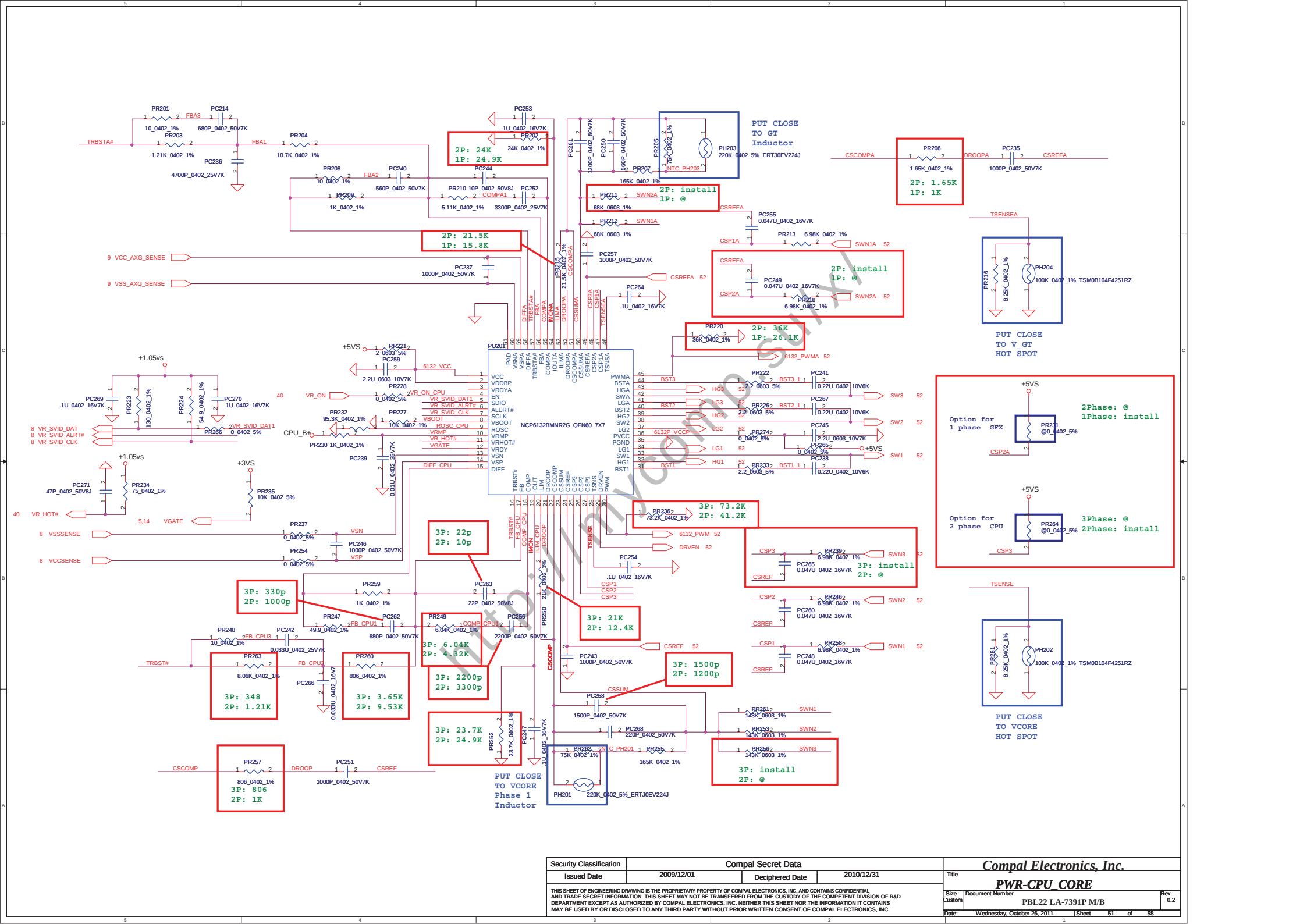
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Issued Date	2010/07/20	Deciphered Date	2012/12/31	Title	
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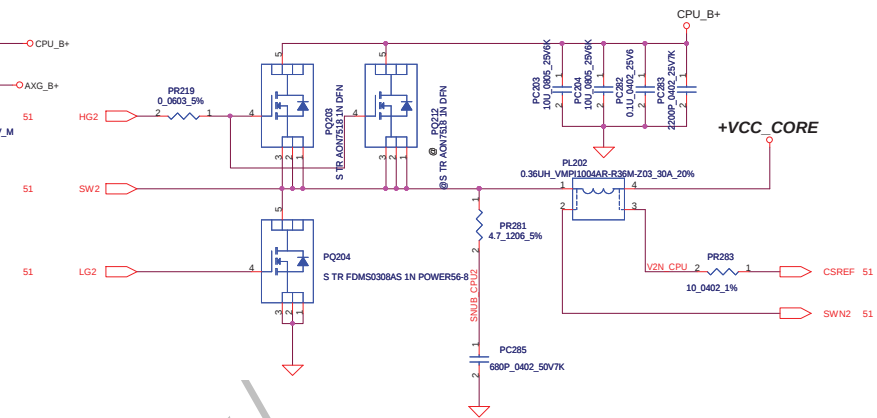
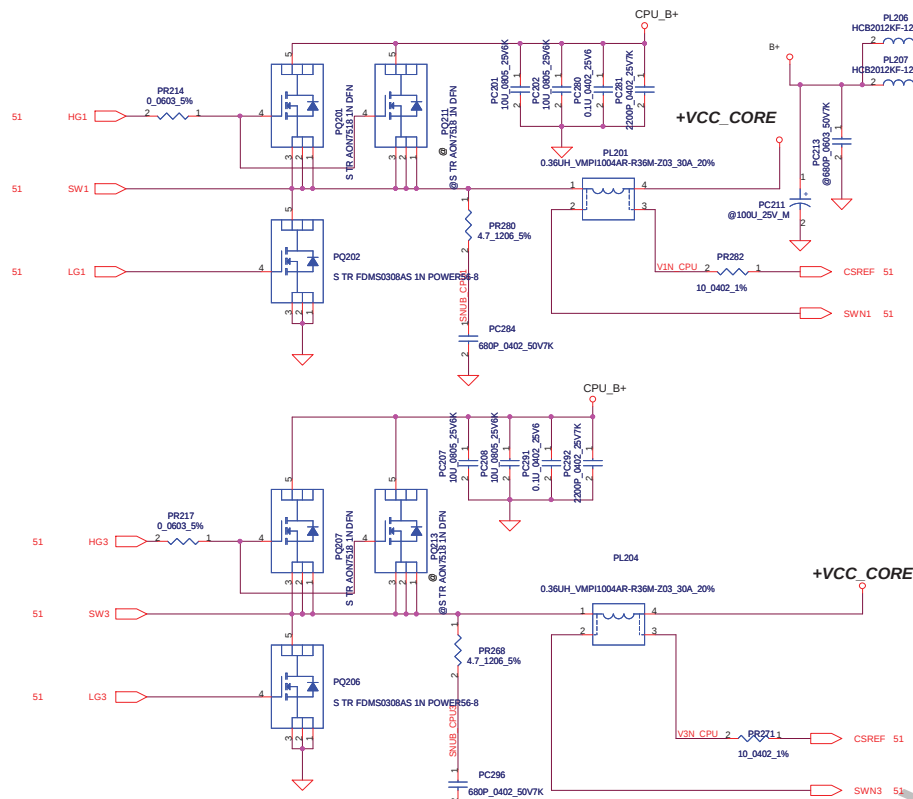


VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```





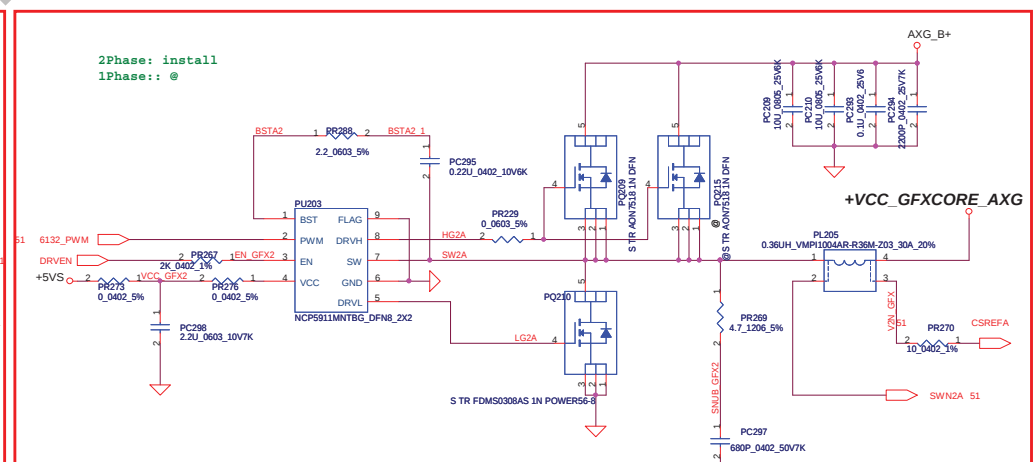
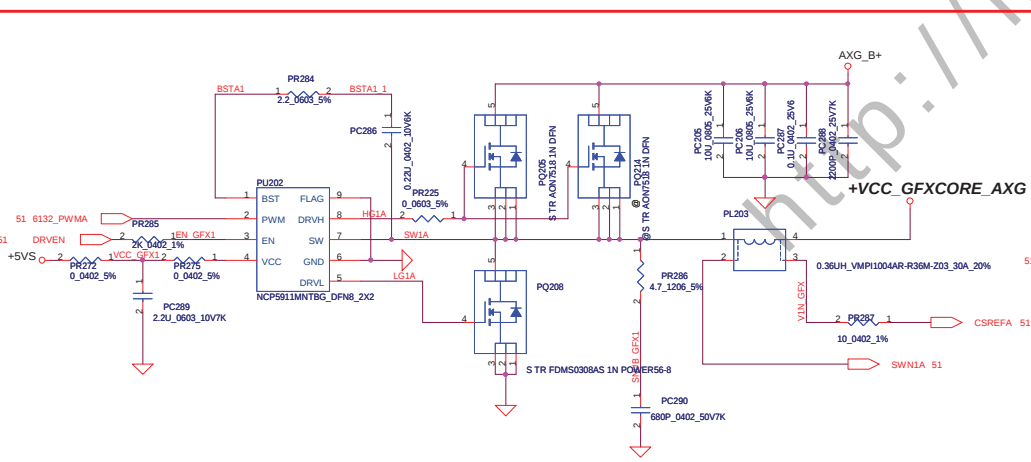


QC 45W CPU
solution: 3+2
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8059)

DC 35W CPU
solution: 2+1
MOS: cpu_core -->上1(CSD17308)下1(TPCA8059)
Gfx_core -->上1(CSD17308)下1(TPCA8057)

QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=56A
R_LL=1.9m ohm
OCP=110A

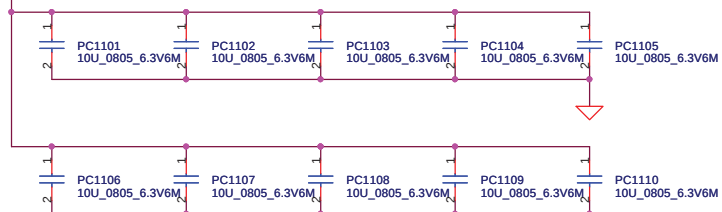
DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=33A
R_LL=1.9m ohm
OCP=65A



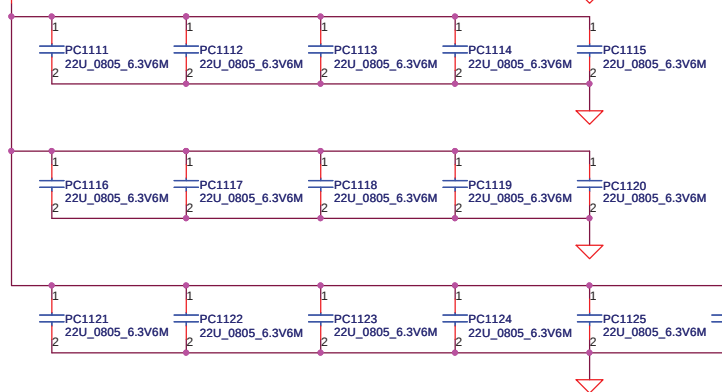
QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP=55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP=40A

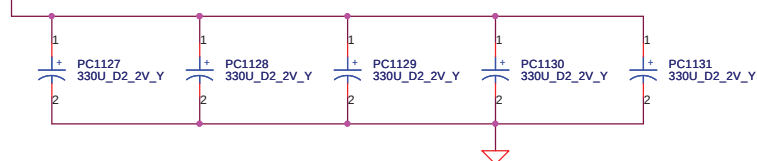
+VCC_CORE



+VCC_CORE



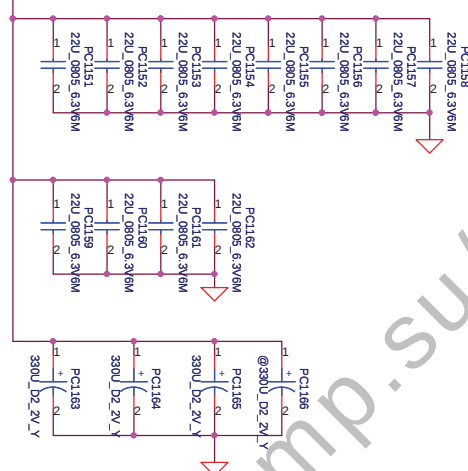
+VCC_CORE



+VCC_CORE

+VCC_GFXCORE_AXG

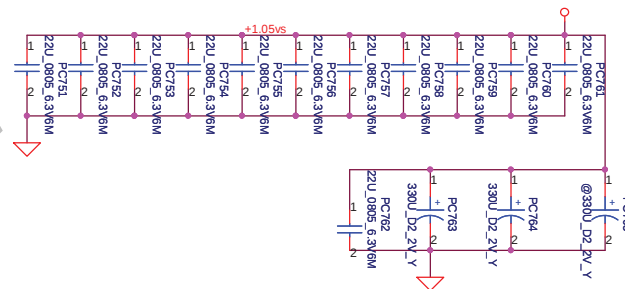
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

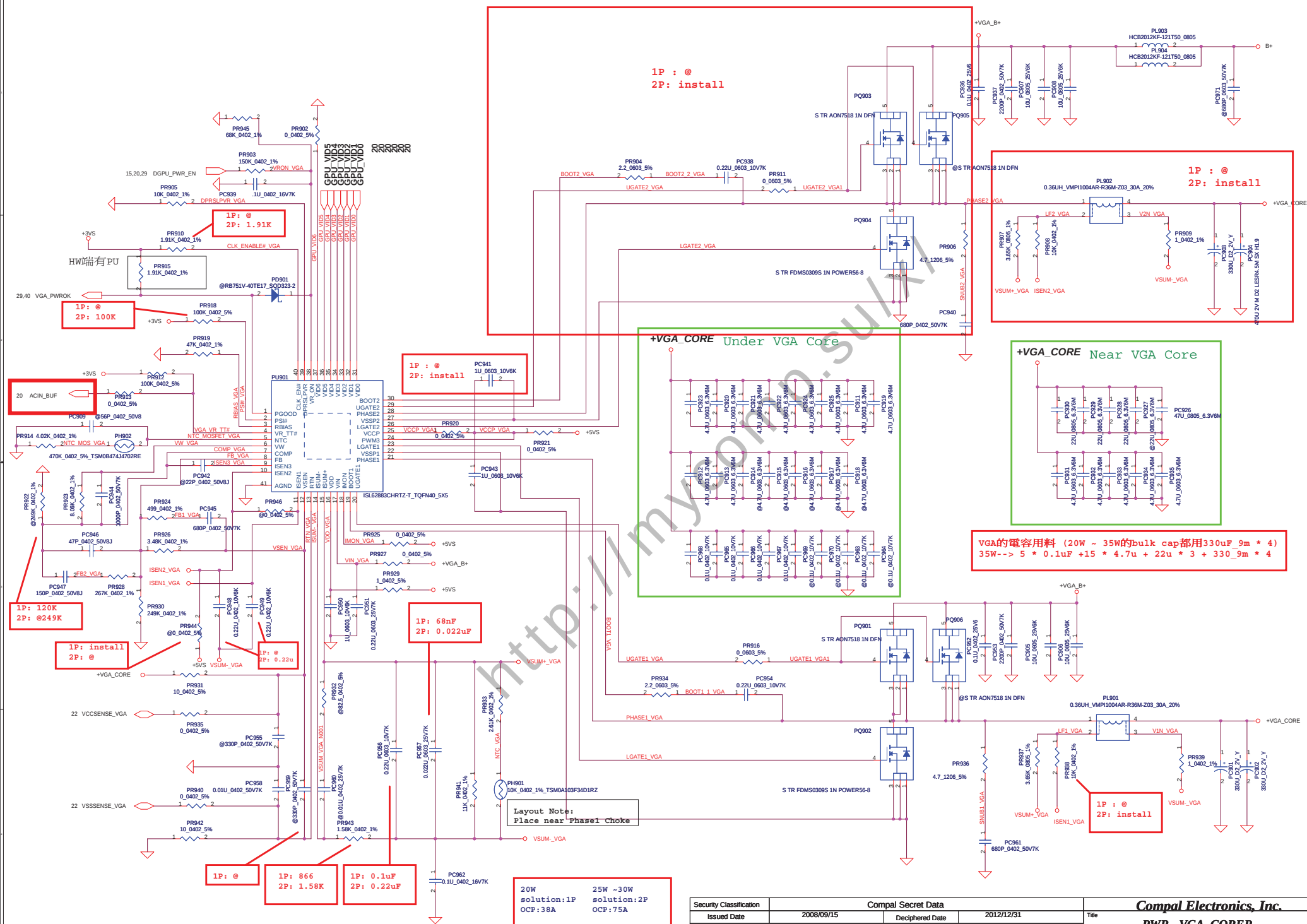
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05vs



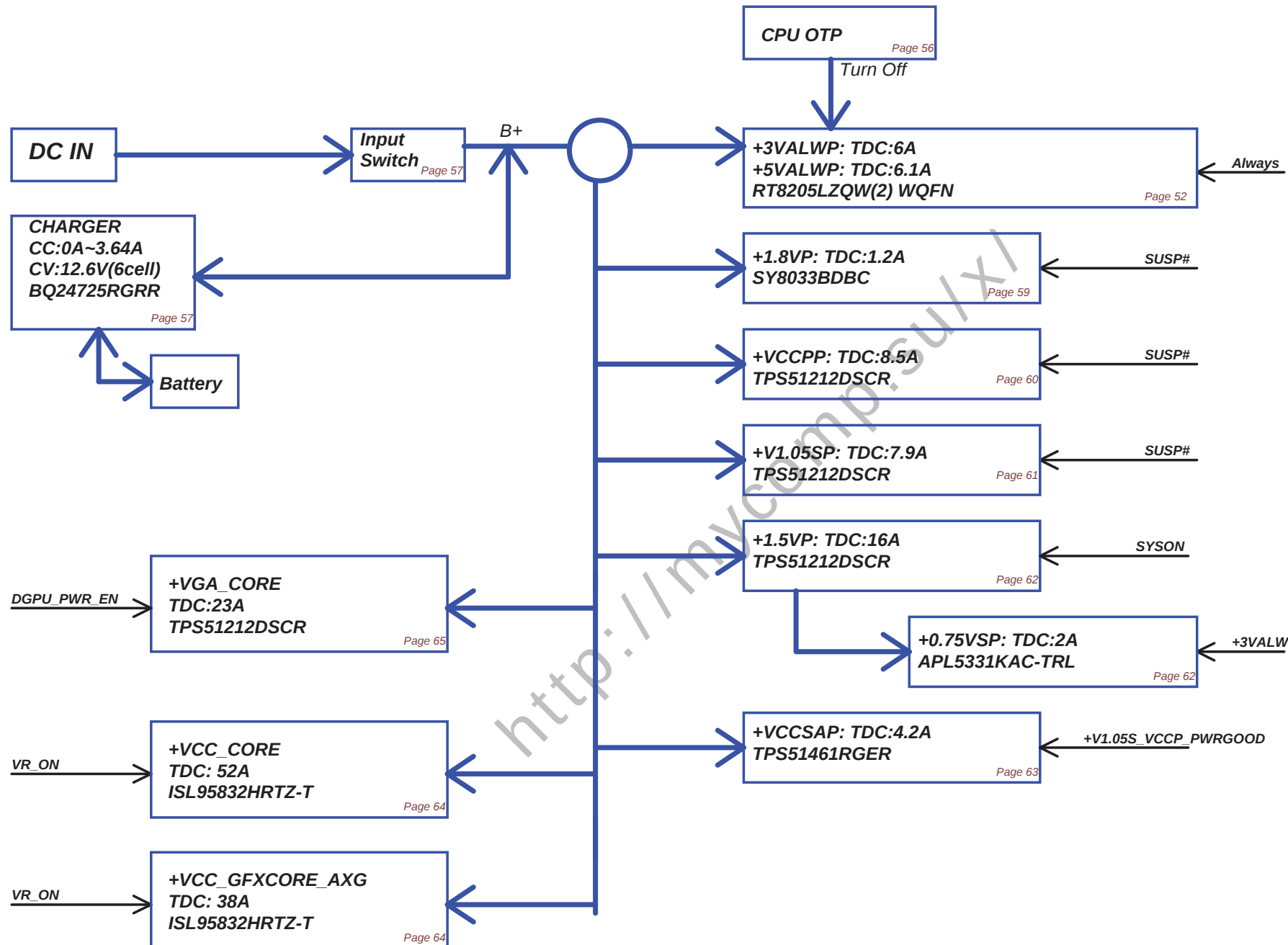
Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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				PWR - VGA CORE	
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Power block



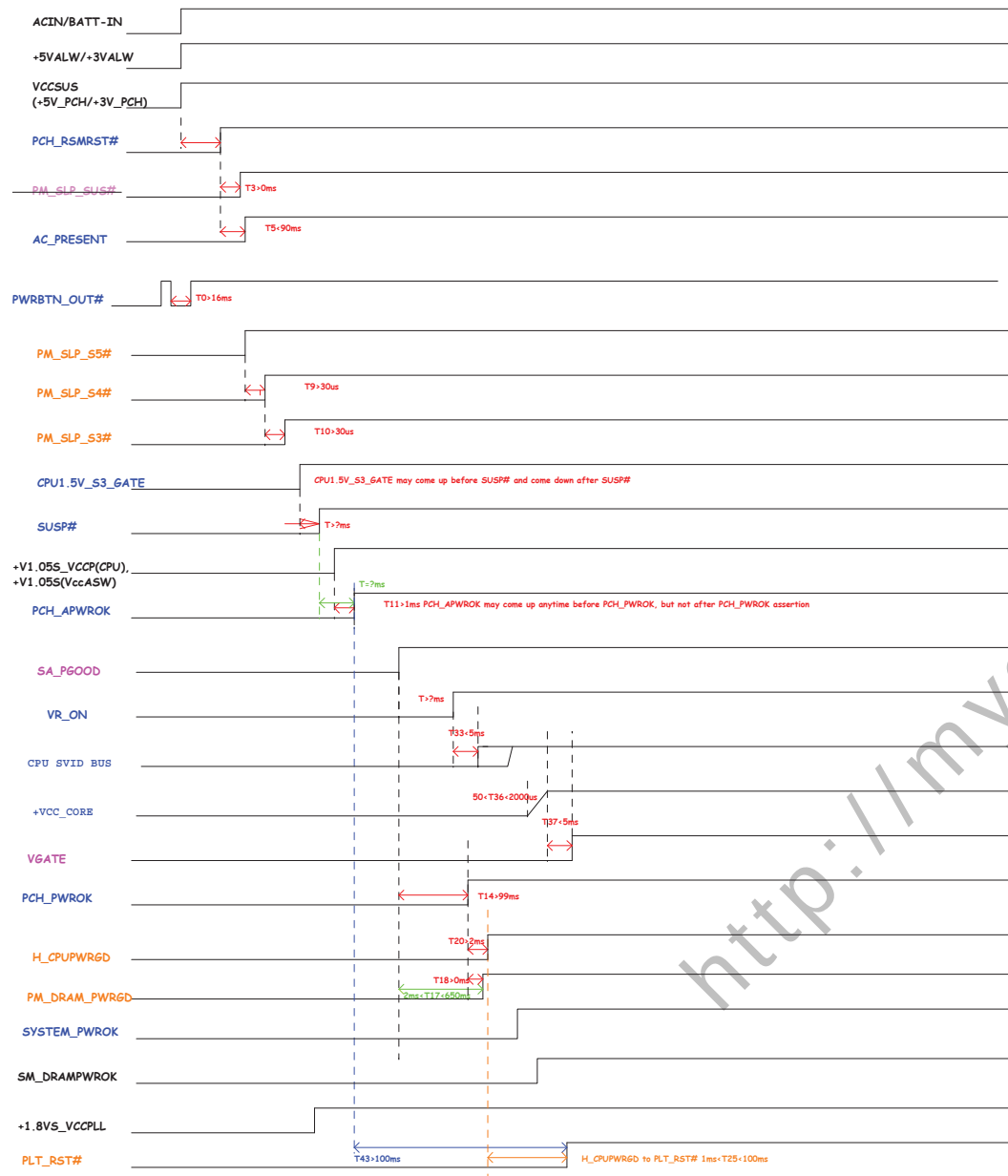
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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
ER01		HW Design (TMDS_B_HPD)	0.2	14	Delete R205	09/21	
ER02		Add USB3.0(ASM1042) & non AI co-lay	0.2	36	Add ASM1042 co-lay	09/21	
ER03	+3VS Leakage	HW Design (SMBus leakage)	0.2	13	Delete Q3. (connect pin S & D) remove R135, R137	09/21	
ER04		Design change for card reader	0.2	40	Del R552, R556	09/21	
ER05		HW Design (PURC demand)	0.2	34	Add Q20, R773, R775 Reserve R768, R774. Change Net name at Card reader Conn	09/21	
ER06		HW Design (PURC demand)	0.2	29	Change to Q3(A03404L) from U22(A04430L)	09/21	
ER07		Fine-tune GPU timing	0.2	42	Change Q33 to A03413L from AP2301GN	09/21	
ER08		HW Design (reserve)	0.2	29	Change R433 to 0 ohm un-stuff C396 Change R432 to 10K Change R435 to 200 ohm	09/21	
ER09	KB connector reverse	HW Design (change)	0.2	18	Reverse R290	09/21	
ER10		HW Design (change)	0.2	39	Reverse JKB1 connector	09/30	
ER11		HW Design	0.2	40	Del Y5 , C545 , C546	09/30	
ER12		HW Design (PURC demand)	0.2	15	Del R229, R230 (10K) Add R776-R783 (10K) Del R237, R239, R242 (8.2K) Add R784-R793 (8.2K)	09/30	
ER13		HW Design (PURC demand)	0.2	29, 31 10, 11	Change P/N C387, C389, C399, C436, C447, C602 Change C315, C518, C526. (0402) Change P/N C99, C109, C118, C120, C140, C141. (0402)	10/03	
ER14		HW Design(XTAL fine-tune)	0.2	42, 12 13, 12 20, 36	Change R607 to 10 ohm Change Y3, C241, C242. Change Y1, C144, C145 Change Y4, C469, C473. Change Y2, C163, C164 Change Y9	10/07	
ER15		HW Design for instant on function	0.2	13 5	Reserve R750 R576 pin2 change to +3V_PCH from +3VS Change R576 to 0	10/07	
ER16		HW Design (power jumper change to +3VL)	0.2	38 40	jumper PJP302 (change +3VLP to +3VL @P38, P40)	10/07	
ER17		HW Design (PURC demand)	0.2		Change P/N Q7, U20, U21. Change P/N Q14-Q19, Q25, Q27-Q29, Q32, Q34-Q37, Q40-Q43, Q46-Q51, Q55-Q57, Q60, Q61, Q902, Q903, Q905. Change P/N Q23	10/14	
ER18		EMI solution	0.2	5	Add R684 to 0 (H_CPUPWRGD)	10/14	
ER19		Refer to ORB design	0.2	14 40	un-stuff D2, Add R751 un-stuff D32, R547, Add R752 Assign U33.18 to AC_PRESENT signal.	10/14	
ER20		change for GPU H/W strapping STRAP1 to PL 45K ohm to enhanced the PCIe PEG driving.	0.2	22	Change R349 from 34.8K to 45.3K	10/14	
ER21		modify parts for Intel review feedback message.	0.2	09 18 17 14 15	Add R242 Add C149 0.1uF Del L6, Add R289 , un-stuff C212 Del L4, Add R387 Add R230 Stuff R244	10/14	
ER22		Modify H2 size	0.2	38	Modify H2 size	10/17	

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