

Compal Confidential

PBL22 MB Schematic Document

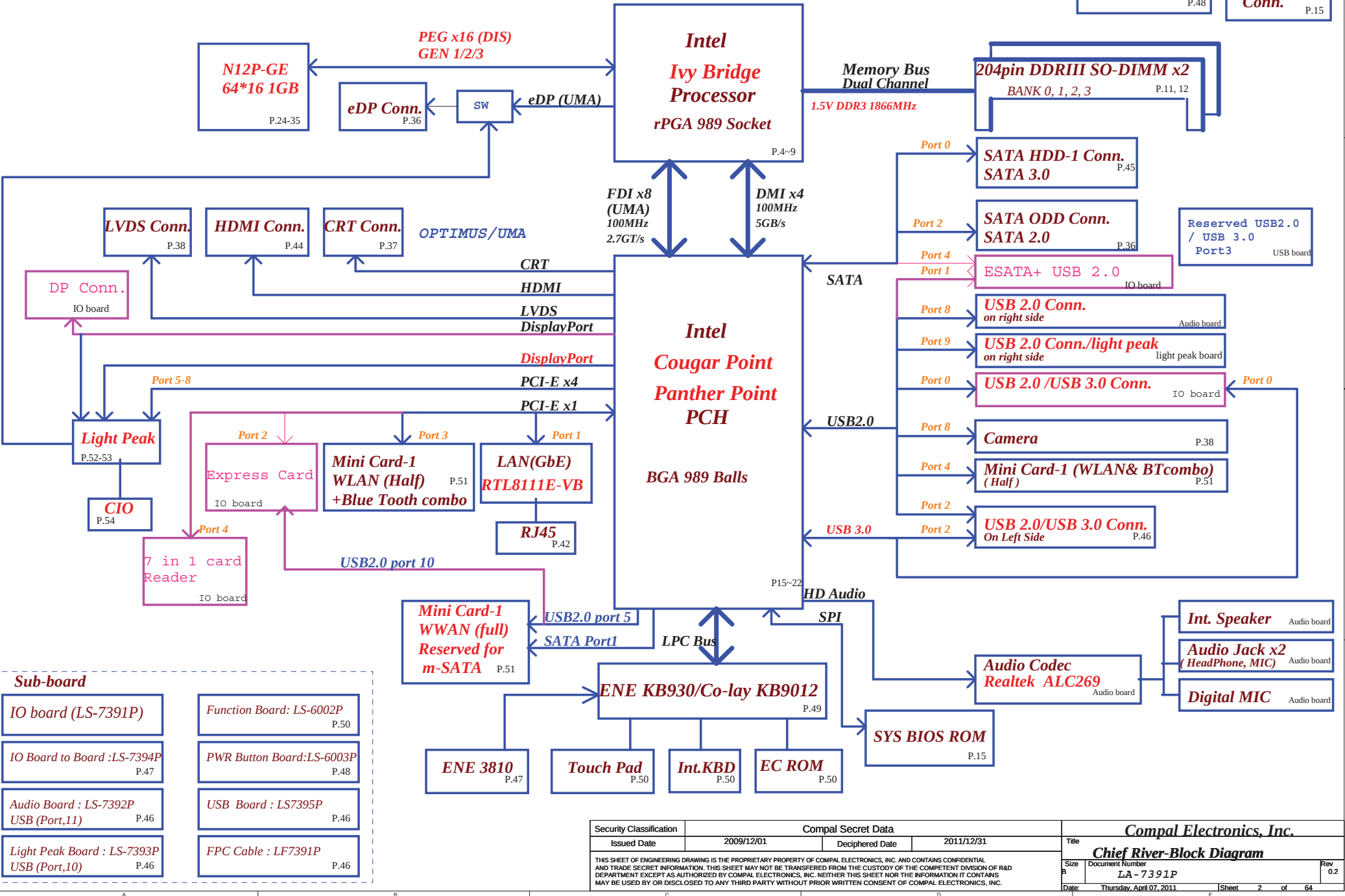
LA-7391P

Rev: 0.2

2011.04.07

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/12/01	Deciphered Date	2011/12/31	Title Cover Sheet	
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Chief River



Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MIINI1	BATT	MINI2	EXPRESS CARD	SODIMM	DGPU Internal Thermal sensor	JXDP1 JXDP2
EC SMB CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X	X
EC SMB CK2 EC_SMB_DA2	KB930	X	X	X	X	X	V	X
PCH SMBCLK PCH_SMBDATA	PCH	V	X	V	V	V	X	V
PCH SMLCLK PCH_SMLDATA	PCH	X	X	X	X	X	V	X

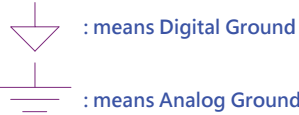
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	Debug Port
PCI3	LPC Debug Port
PCI4	None

PCH	USB PORT#	DESTINATION
	0	USB2/3 (Ext Right Side Up)
	1	ESATA (Ext Right Side Up)
	2	USB2/3 (Ext Left Side Down)
	3	USB2/3 (Ext FPC board)
	4	JMINI1 (WLAN) Bluetooth
	5	JMINI2 (WWAN)
	6	None
	7	None
	8	CAMERA
	9	JUSB3 (Ext Right Side Down)
	10	EXPRESS CARD
	11	JUSB4 (Ext Right Side Down)
	12	None
	13	None

UMA : UMA@/XDP@/UO@
OPTIMUS : XDP@/D@/UO@
DISCRETE : XDP@D@/DIS@

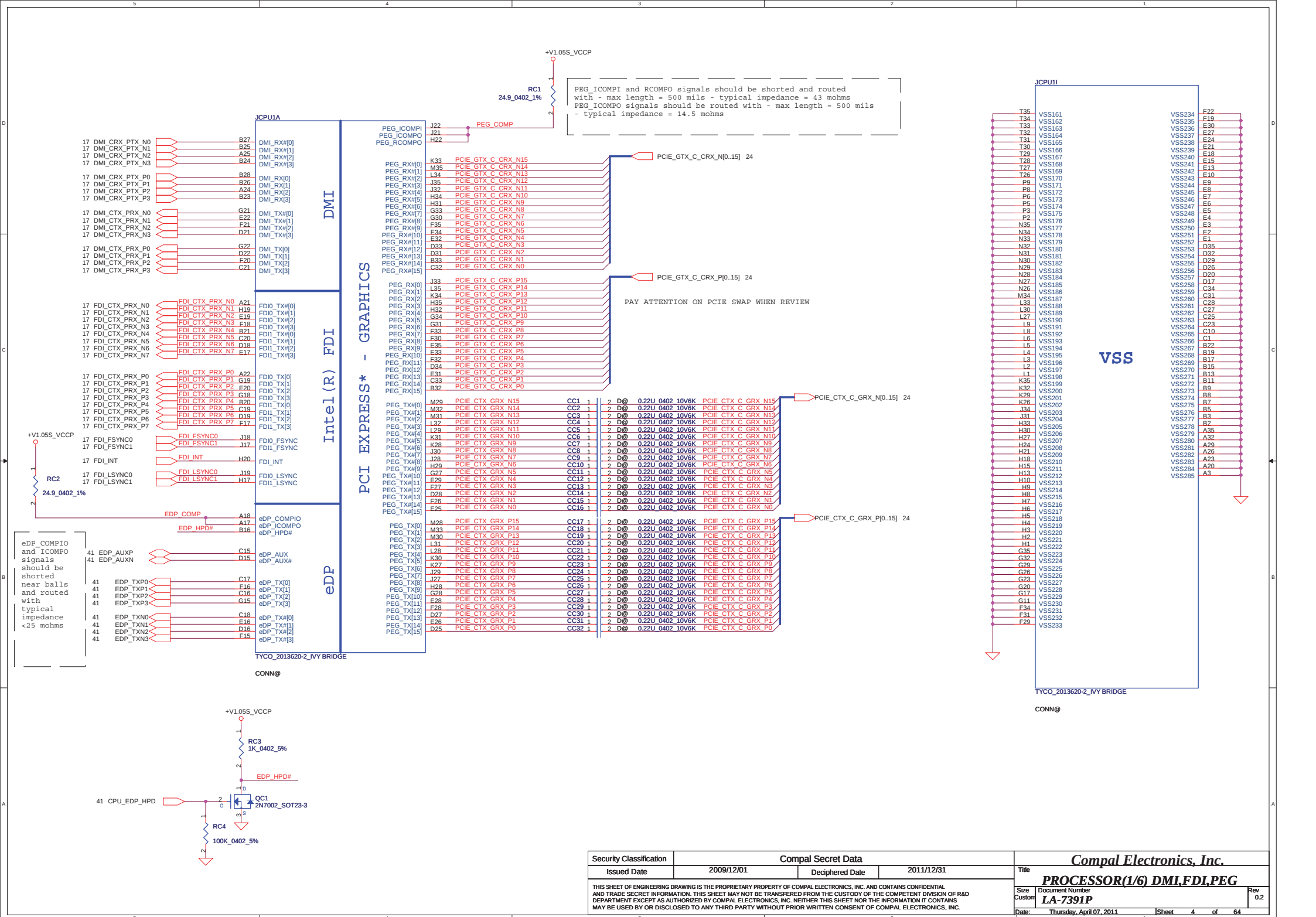
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-1 WLAN	CLKOUTFLEX1	CLK_14M
	CLKOUT_PCIE2	EXPRESS CARD	CLKOUTFLEX2	27M_CLK
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	27M_SSC
	CLKOUT_PCIE4	Light Peak		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

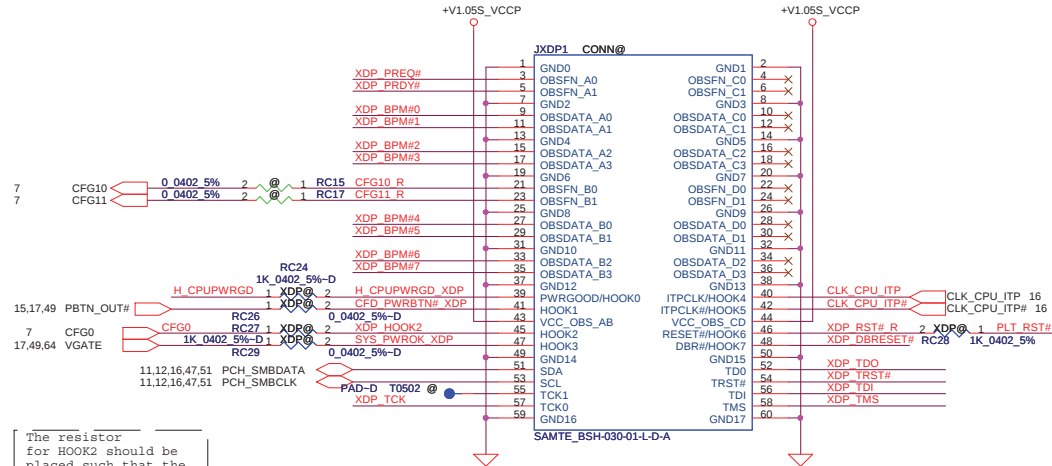
Symbol Note :



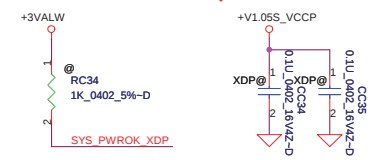
SATA	DESTINATION
SATA0	HDD
SATA1	m-SATA
SATA2	ODD
SATA3	None
SATA4	ESATA
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-1 WLAN
Lane 3	EXPRESS CARD
Lane 4	CARD READER
Lane 5	Light Peak
Lane 6	Light Peak
Lane 7	Light Peak
Lane 8	Light Peak

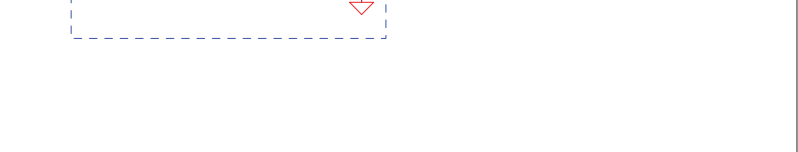
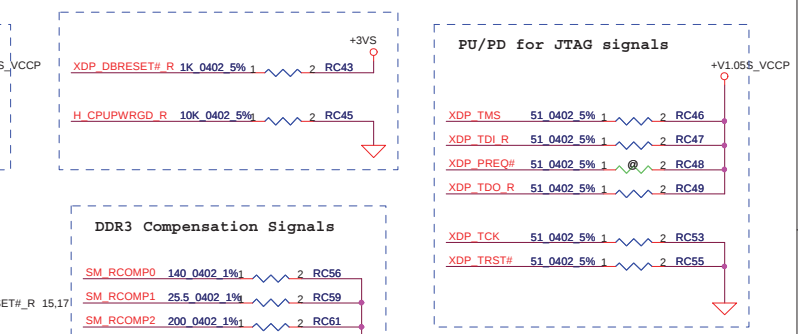
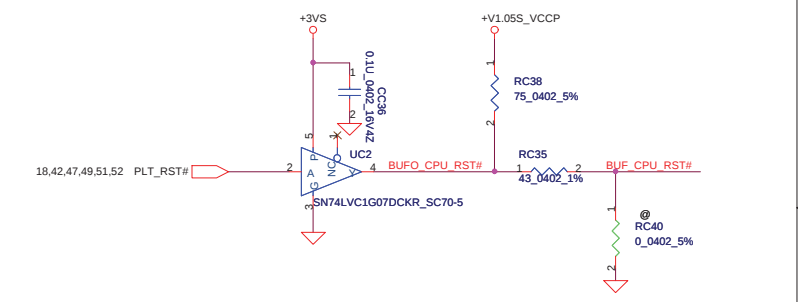
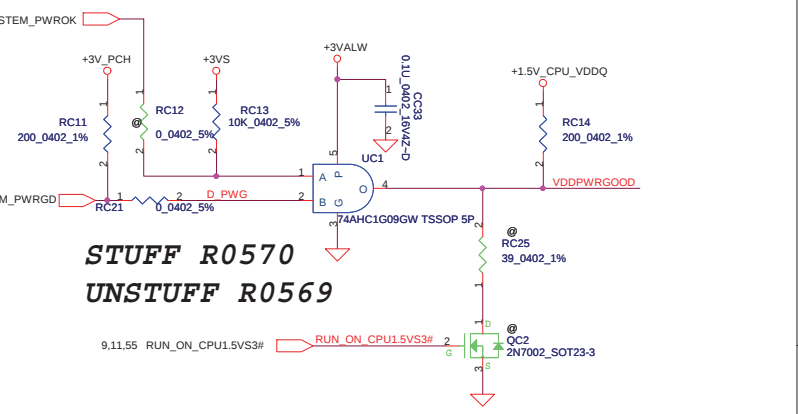
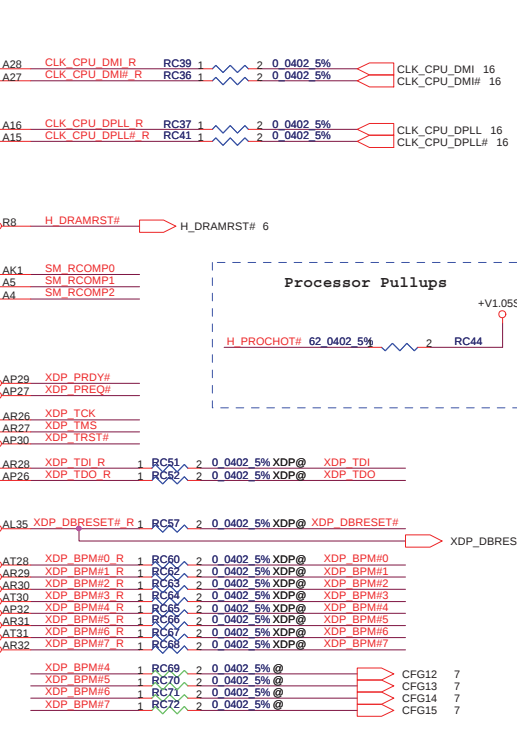
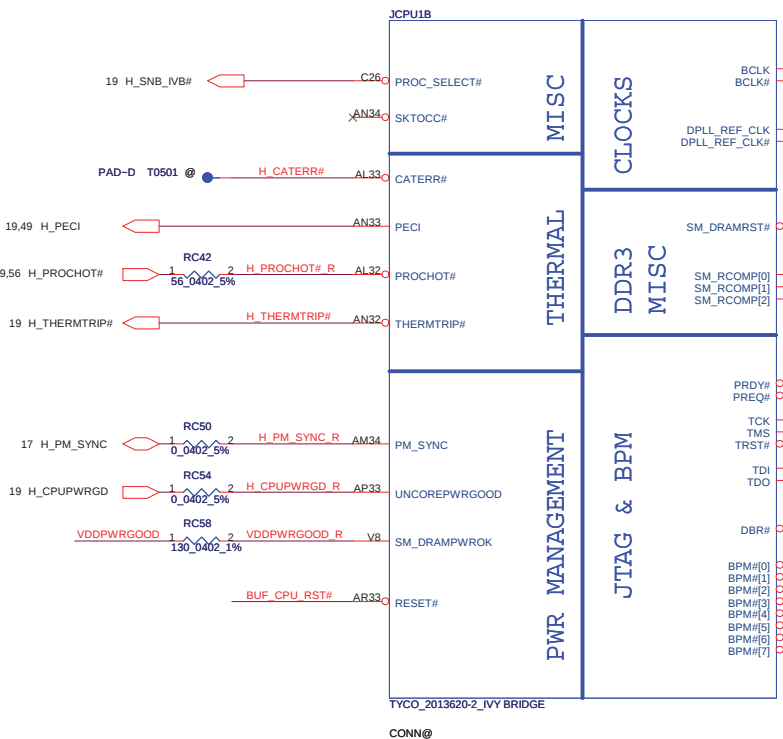




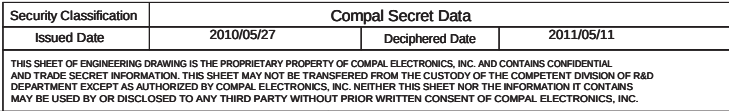
The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

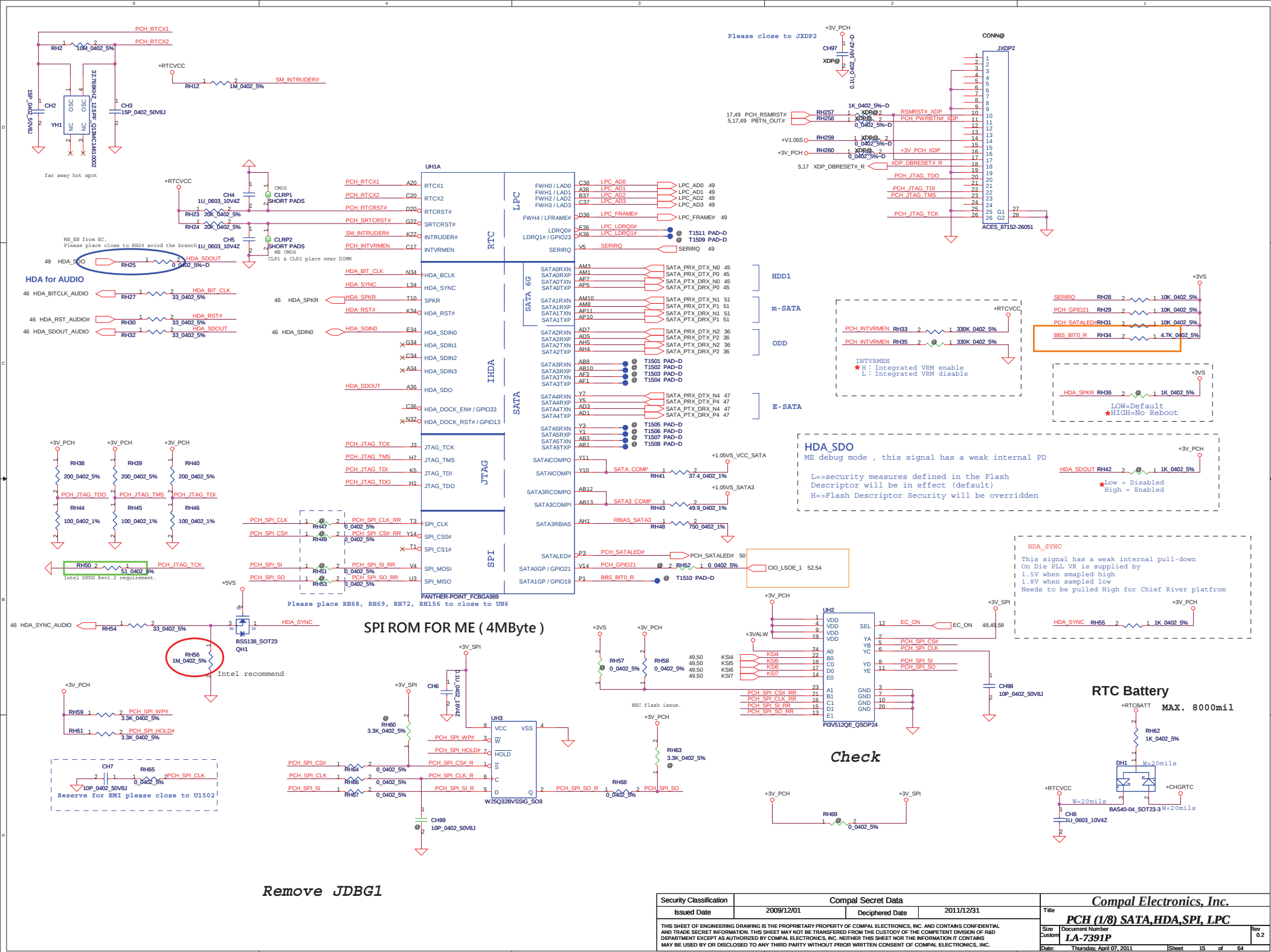


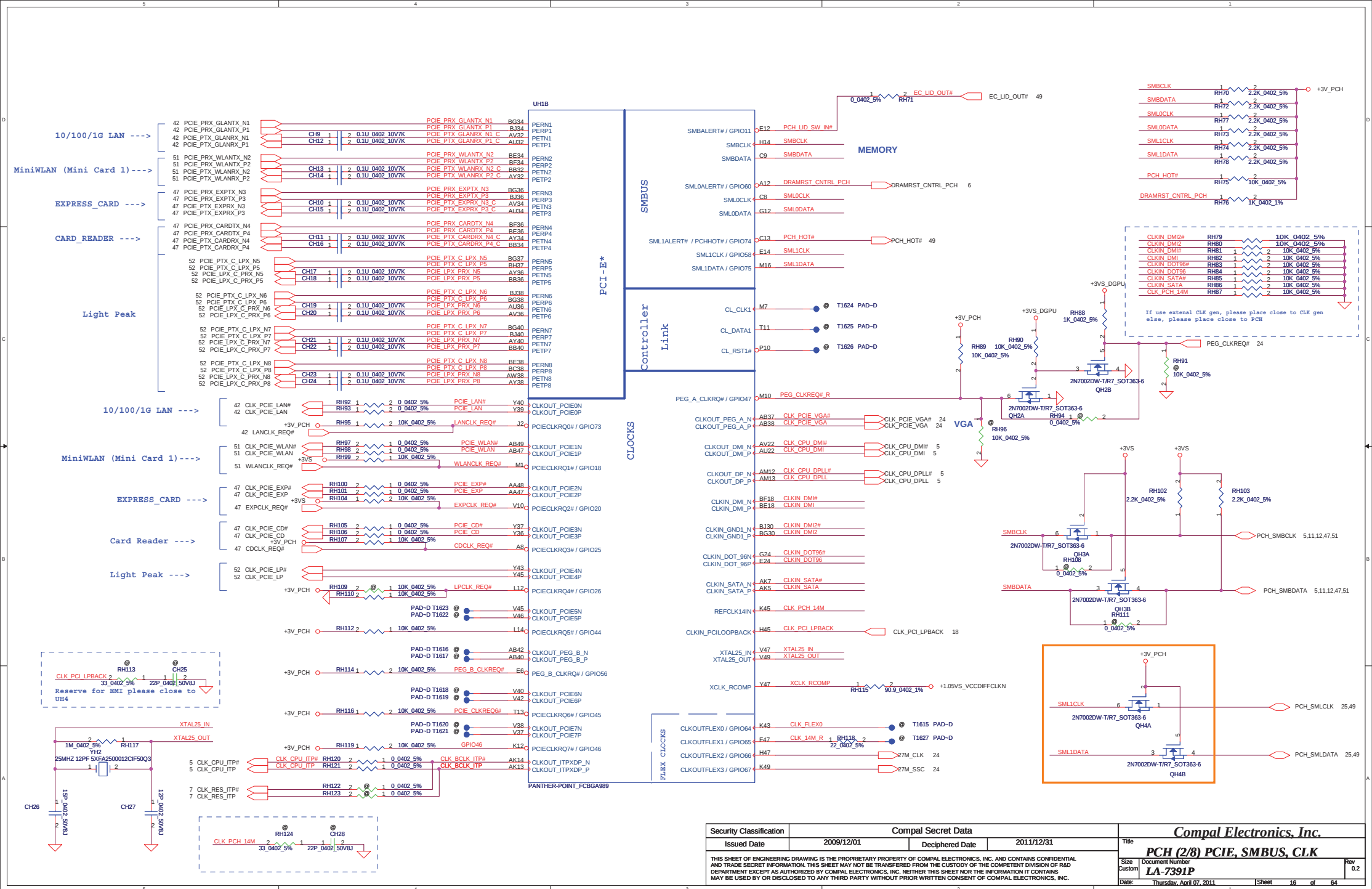
Place near JXDP1



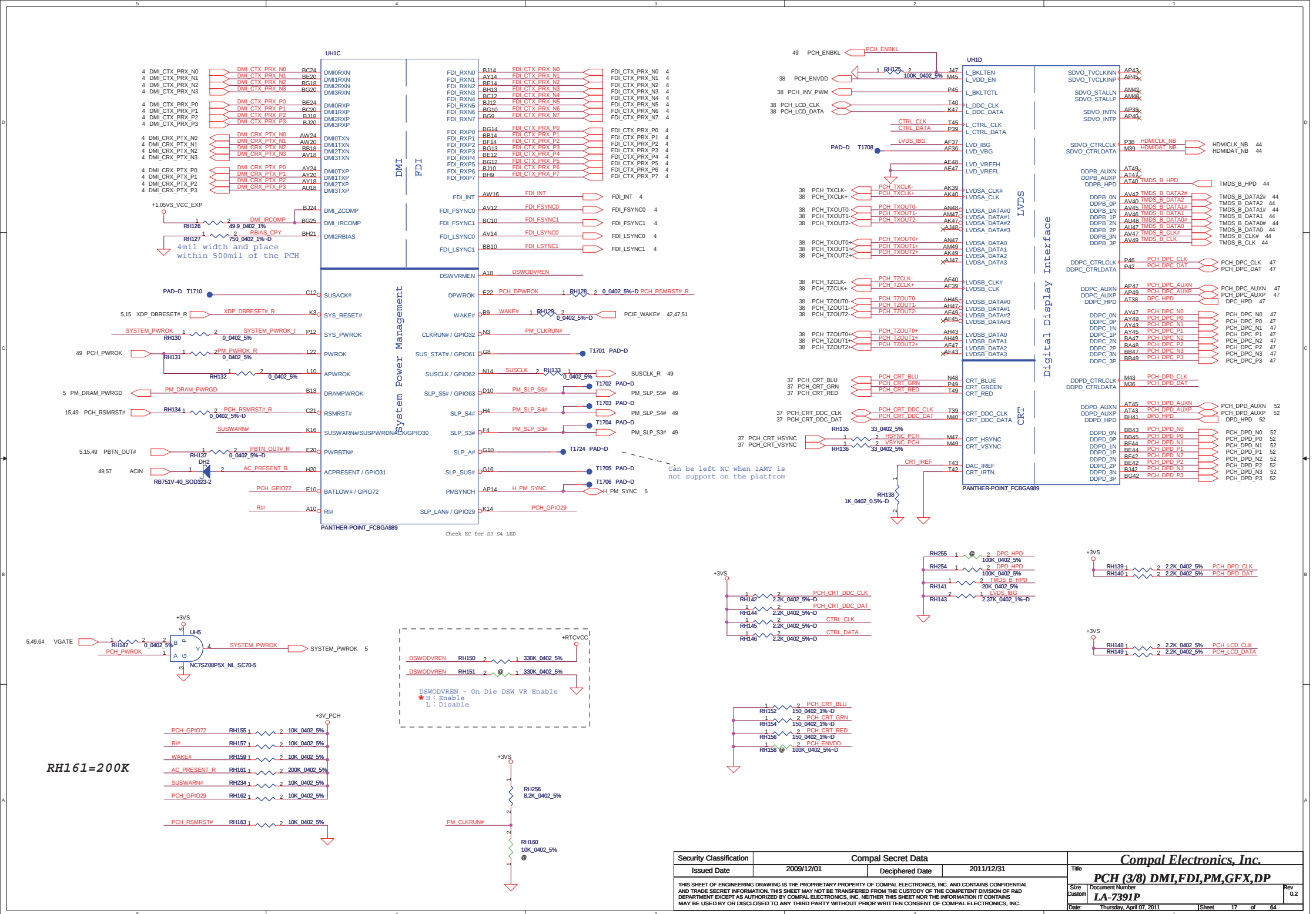
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				PROCESSOR(2/6) PM,XDP,CLK					
				Size		Document Number		Rev	
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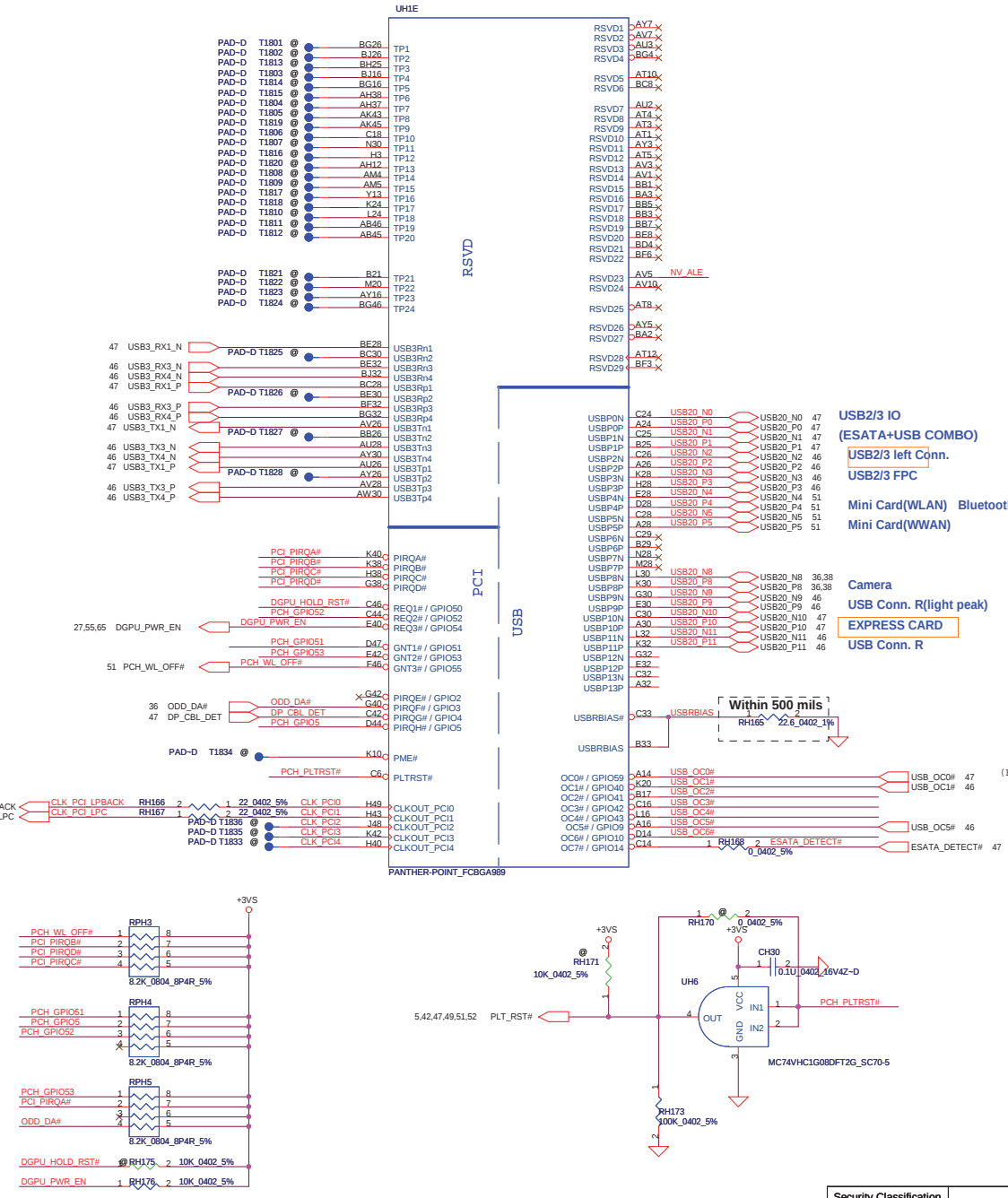






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GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

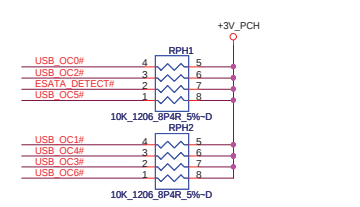
Boot BIOS Strap

BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI *

Intel Anti-Theft Technology

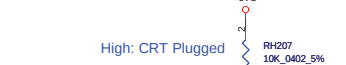
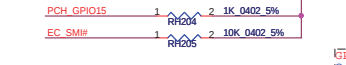
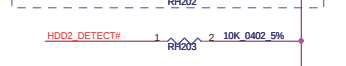
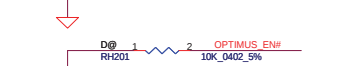
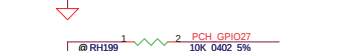
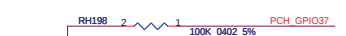
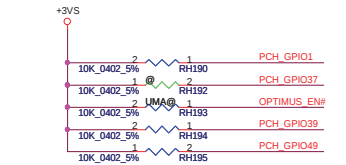
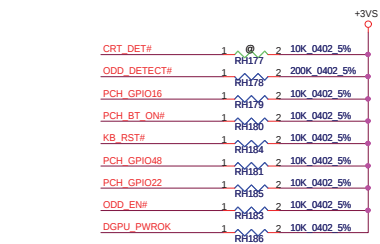
NV_ALE	High=Enabled
Low=Disable(floating) *	

NV_ALE @ RH164 1 2 1K 0402 5%



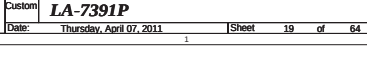
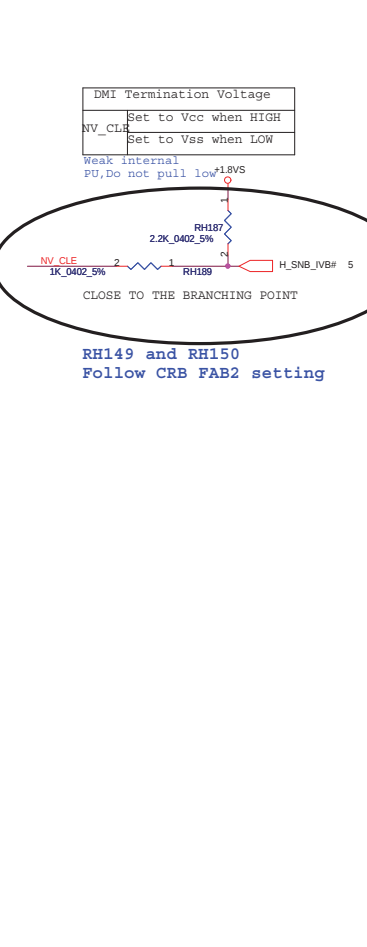
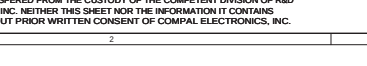
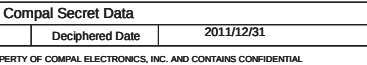
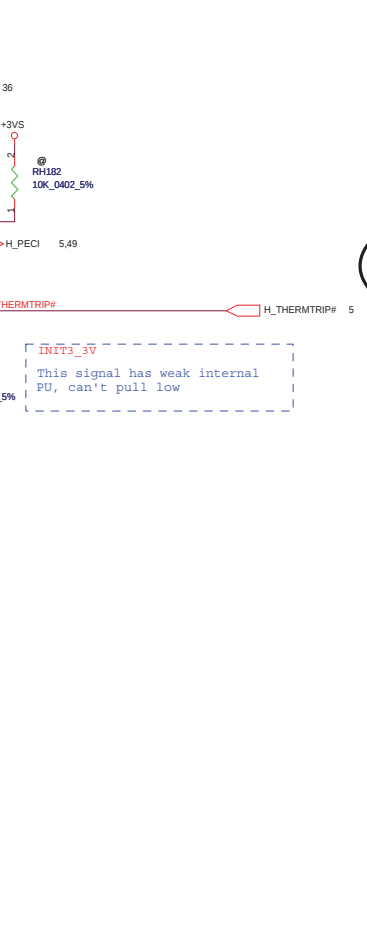
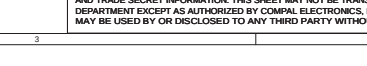
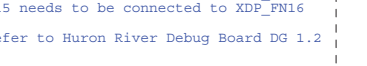
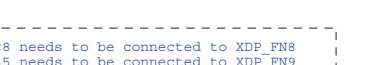
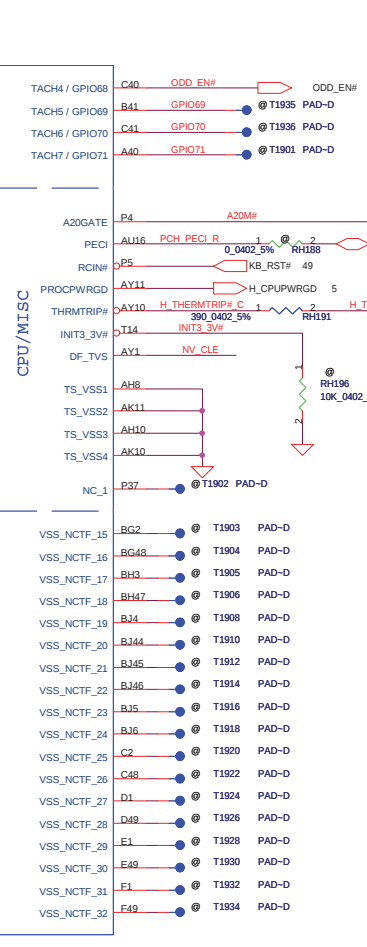
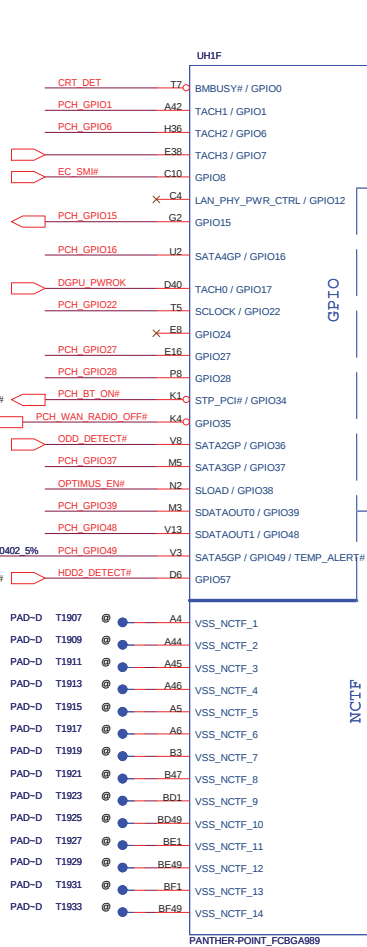
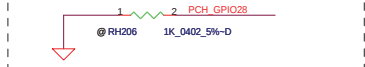
(For USB Port0, 1)
(For USB Port 6,7)

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OPTIMUS_EN# H: Disable optimus
OPTIMUS_EN# L: Enable optimus

On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H: On-Die voltage regulator enable
L: On-Die PLL Voltage Regulator disable



DMI Termination Voltage
NV_CLE# Set to Vcc when HIGH
Set to Vss when LOW

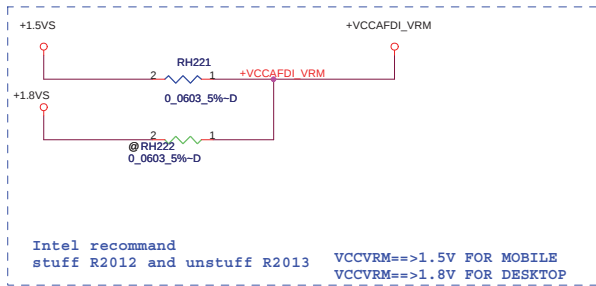
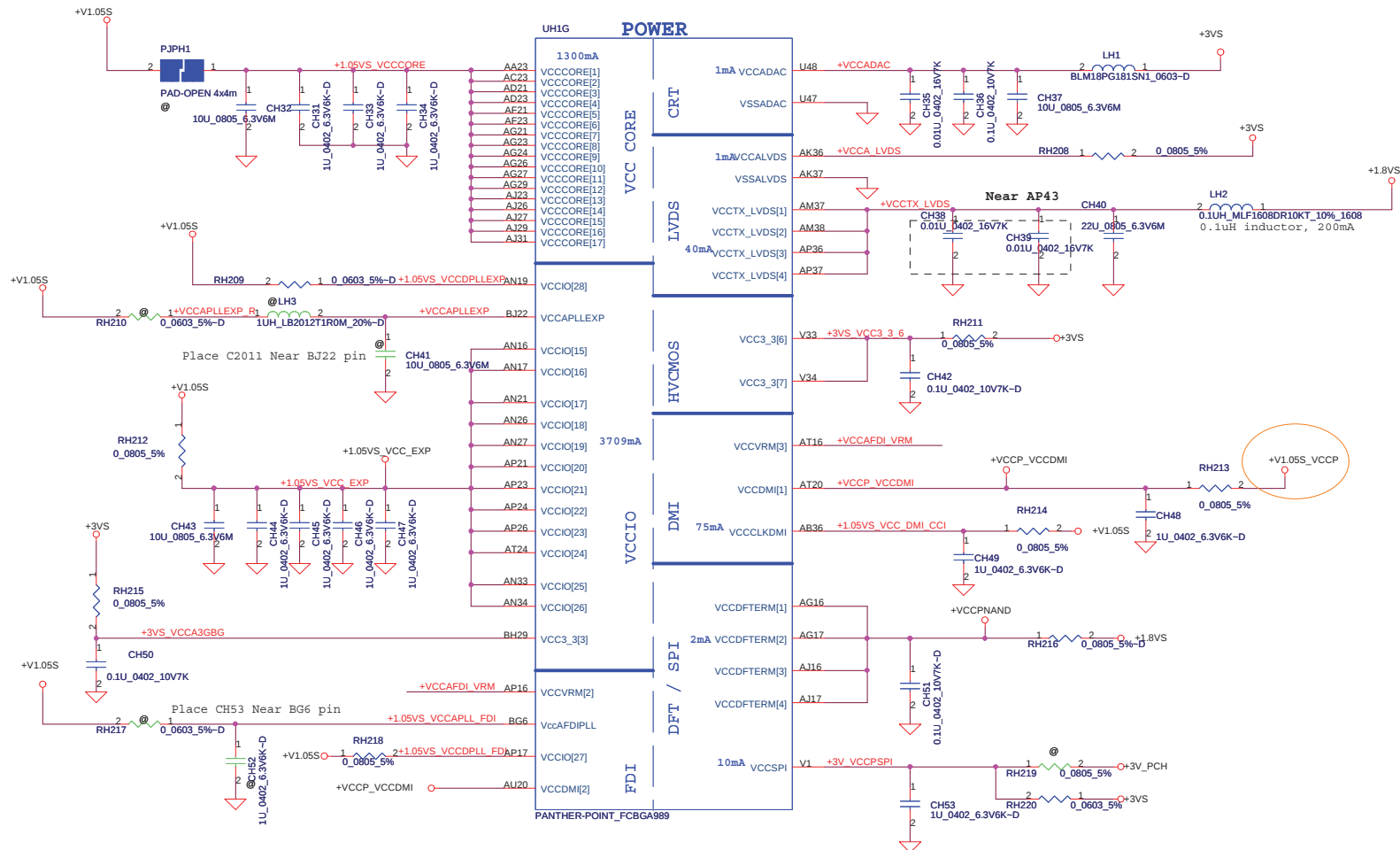
Weak internal
PU, Do not pull low

2.2K 0402 5%
H_SNB_VB# 5

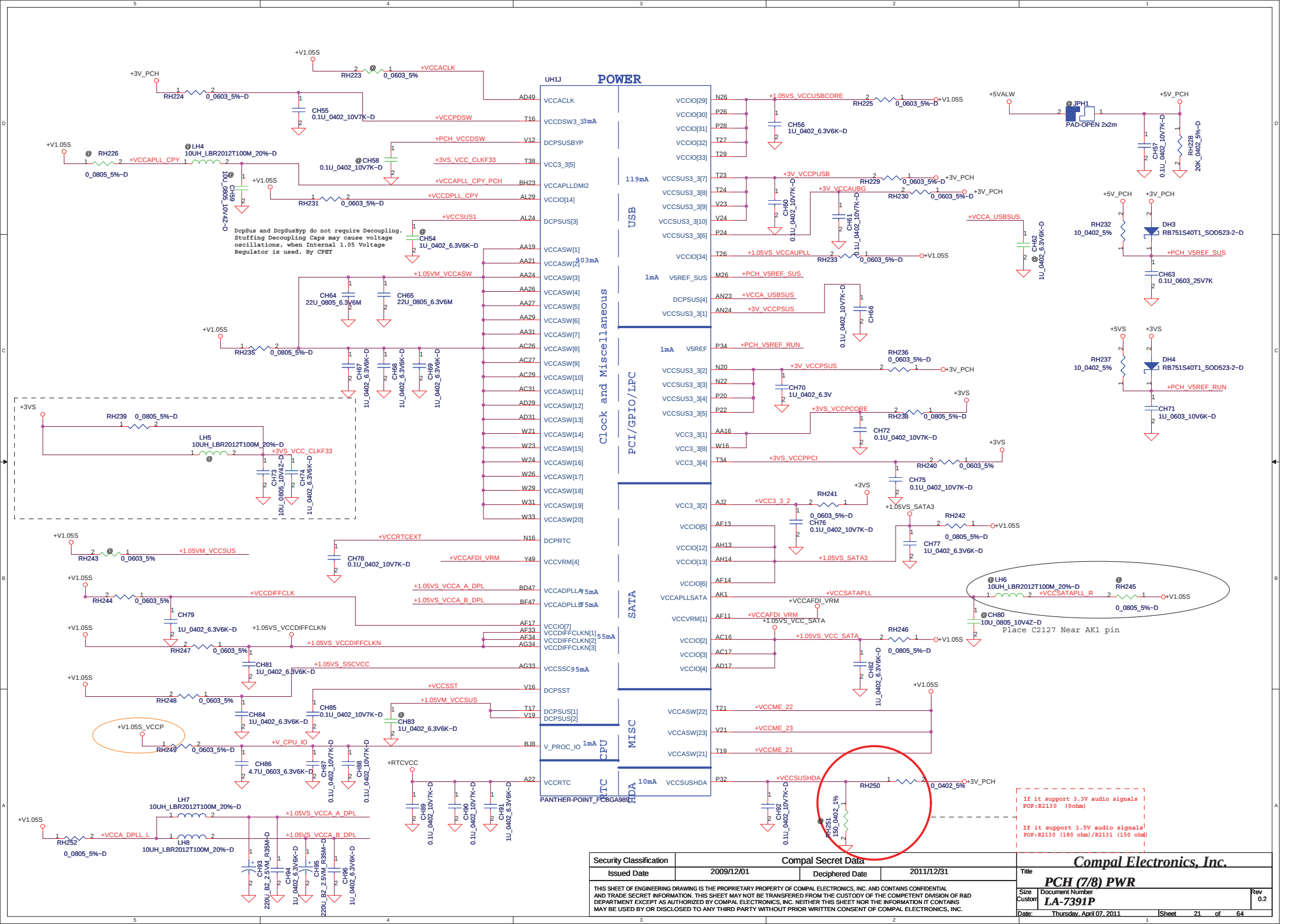
CLOSE TO THE BRANCHING POINT

RH149 and RH150
Follow CRB FAB2 setting

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PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	50 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



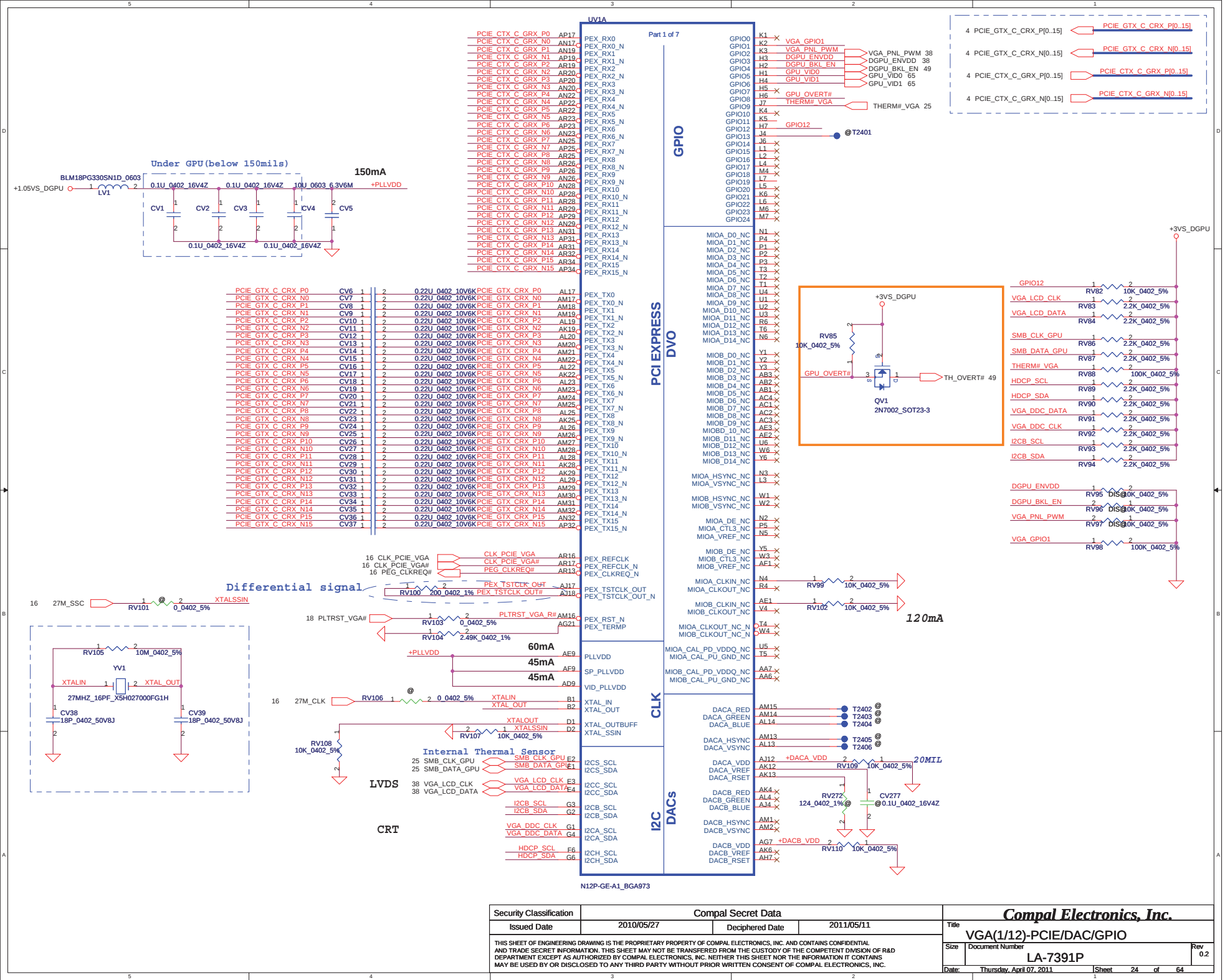
UH1H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AD10	VSS[19]	VSS[98] AM14
AD11	VSS[20]	VSS[99] AM36
AD12	VSS[21]	VSS[100] AM39
AD13	VSS[22]	VSS[101] AM43
AD19	VSS[23]	VSS[102] AM45
AD24	VSS[24]	VSS[103] AM46
AD26	VSS[25]	VSS[104] AM7
AD27	VSS[26]	VSS[105] AN2
AD33	VSS[27]	VSS[106] AN29
AD34	VSS[28]	VSS[107] AN3
AD36	VSS[29]	VSS[108] AN31
AD37	VSS[30]	VSS[109] AP12
AD38	VSS[31]	VSS[110] AP19
AD40	VSS[32]	VSS[111] AP28
AD42	VSS[33]	VSS[112] AP30
AD43	VSS[34]	VSS[113] AP32
AD45	VSS[35]	VSS[114] AP38
AD46	VSS[36]	VSS[115] AP4
AD8	VSS[37]	VSS[116] AP42
AE2	VSS[38]	VSS[117] AP46
AE3	VSS[39]	VSS[118] AP8
AE10	VSS[40]	VSS[119] AR2
AE12	VSS[41]	VSS[120] AR48
AE16	VSS[42]	VSS[121] AT11
AE19	VSS[43]	VSS[122] AT13
AE24	VSS[44]	VSS[123] AT18
AE26	VSS[45]	VSS[124] AT22
AF16	VSS[46]	VSS[125] AT26
AF19	VSS[47]	VSS[126] AT28
AF24	VSS[48]	VSS[127] AT30
AF26	VSS[49]	VSS[128] AT32
AF27	VSS[50]	VSS[129] AT34
AF29	VSS[51]	VSS[130] AT39
AF31	VSS[52]	VSS[131] AT42
AF38	VSS[53]	VSS[132] AT46
AF4	VSS[54]	VSS[133] AT7
AF42	VSS[55]	VSS[134] AU24
AF46	VSS[56]	VSS[135] AU30
AG19	VSS[57]	VSS[136] AV16
AG2	VSS[58]	VSS[137] AV20
AG31	VSS[59]	VSS[138] AV24
AG48	VSS[60]	VSS[139] AV30
AH11	VSS[61]	VSS[140] AV38
AH3	VSS[62]	VSS[141] AV4
AH36	VSS[63]	VSS[142] AV43
AH40	VSS[64]	VSS[143] AV8
AH42	VSS[65]	VSS[144] AW14
AH46	VSS[66]	VSS[145] AW18
AJ19	VSS[67]	VSS[146] AW2
AJ21	VSS[68]	VSS[147] AW22
AJ24	VSS[69]	VSS[148] AW26
AJ34	VSS[70]	VSS[149] AW28
AK12	VSS[71]	VSS[150] AW32
AK3	VSS[72]	VSS[151] AW34
	VSS[73]	VSS[152] AW36
	VSS[74]	VSS[153] AW40
	VSS[75]	VSS[154] AW48
	VSS[76]	VSS[155] AV11
	VSS[77]	VSS[156] AY12
	VSS[78]	VSS[157] AY22
	VSS[79]	VSS[158] AY28

PANTHER-POINT_FCBGA989

UH1I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] M16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P20
BC26	VSS[187]	VSS[287] N47
BC32	VSS[188]	VSS[288] P11
BC34	VSS[189]	VSS[289] P18
AN2	VSS[190]	VSS[290] T33
BC40	VSS[191]	VSS[291] P40
BC42	VSS[192]	VSS[292] P43
BC48	VSS[193]	VSS[293] P47
BD46	VSS[194]	VSS[294] P7
BD5	VSS[195]	VSS[295] R2
BE22	VSS[196]	VSS[296] R48
BE26	VSS[197]	VSS[297] T12
BE40	VSS[198]	VSS[298] T31
BE10	VSS[199]	VSS[299] T37
BE12	VSS[200]	VSS[300] T4
BE16	VSS[201]	VSS[301] W34
BE20	VSS[202]	VSS[302] T46
AP8	VSS[203]	VSS[303] T47
BE22	VSS[204]	VSS[304] T8
BE24	VSS[205]	VSS[305] V11
BE26	VSS[206]	VSS[306] V17
BE28	VSS[207]	VSS[307] V26
BD3	VSS[208]	VSS[308] V27
BE30	VSS[209]	VSS[309] V29
BE38	VSS[210]	VSS[310] V31
BE40	VSS[211]	VSS[311] V36
BE4	VSS[212]	VSS[312] V39
BG17	VSS[213]	VSS[313] V43
BG21	VSS[214]	VSS[314] V7
BG33	VSS[215]	VSS[315] W17
BG44	VSS[216]	VSS[316] W19
BG8	VSS[217]	VSS[317] W2
BH11	VSS[218]	VSS[318] W27
BH17	VSS[219]	VSS[319] W48
BH19	VSS[220]	VSS[320] Y12
H10	VSS[221]	VSS[321] Y38
BH27	VSS[222]	VSS[322] Y4
BH31	VSS[223]	VSS[323] Y42
AV30	VSS[224]	VSS[324] Y8
BH35	VSS[225]	VSS[325] BG29
BH39	VSS[226]	VSS[326] N24
BH43	VSS[227]	VSS[327] A33
BH7	VSS[228]	VSS[328] AD47
D3	VSS[229]	VSS[329] B43
D12	VSS[230]	VSS[330] BE10
D16	VSS[231]	VSS[331] BG41
D18	VSS[232]	VSS[332] G14
D22	VSS[233]	VSS[333] H16
D24	VSS[234]	VSS[334] T36
D26	VSS[235]	VSS[335] BG22
D30	VSS[236]	VSS[336] BG24
D32	VSS[237]	VSS[337] C22
D34	VSS[238]	VSS[338] AP13
D38	VSS[239]	VSS[339] M14
D42	VSS[240]	VSS[340] AP3
D8	VSS[241]	VSS[341] AP1
E18	VSS[242]	VSS[342] BE16
E26	VSS[243]	VSS[343] BC16
G18	VSS[244]	VSS[344] BG28
G20	VSS[245]	VSS[345] BJ28
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

PANTHER-POINT_FCBGA989

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PCIE CTX_C GRX P0	AP17
PCIE CTX_C GRX N0	AN17
PCIE CTX_C GRX P1	AP18
PCIE CTX_C GRX N1	AN18
PCIE CTX_C GRX P2	AP19
PCIE CTX_C GRX N2	AN19
PCIE CTX_C GRX P3	AP20
PCIE CTX_C GRX N3	AN20
PCIE CTX_C GRX P4	AP21
PCIE CTX_C GRX N4	AN21
PCIE CTX_C GRX P5	AP22
PCIE CTX_C GRX N5	AN22
PCIE CTX_C GRX P6	AP23
PCIE CTX_C GRX N6	AN23
PCIE CTX_C GRX P7	AP24
PCIE CTX_C GRX N7	AN24
PCIE CTX_C GRX P8	AP25
PCIE CTX_C GRX N8	AN25
PCIE CTX_C GRX P9	AP26
PCIE CTX_C GRX N9	AN26
PCIE CTX_C GRX P10	AP27
PCIE CTX_C GRX N10	AN27
PCIE CTX_C GRX P11	AP28
PCIE CTX_C GRX N11	AN28
PCIE CTX_C GRX P12	AP29
PCIE CTX_C GRX N12	AN29
PCIE CTX_C GRX P13	AP30
PCIE CTX_C GRX N13	AN30
PCIE CTX_C GRX P14	AP31
PCIE CTX_C GRX N14	AN31
PCIE CTX_C GRX P15	AP32
PCIE CTX_C GRX N15	AN32

PCIE GTX_C CRX P0	CV6	1	2	0.22U_0402_10V6K	PCIE GTX CRX P0	AL17
PCIE GTX_C CRX N0	CV7	1	2	0.22U_0402_10V6K	PCIE GTX CRX N0	AN17
PCIE GTX_C CRX P1	CV8	1	2	0.22U_0402_10V6K	PCIE GTX CRX P1	AL18
PCIE GTX_C CRX N1	CV9	1	2	0.22U_0402_10V6K	PCIE GTX CRX N1	AN18
PCIE GTX_C CRX P2	CV10	1	2	0.22U_0402_10V6K	PCIE GTX CRX P2	AL19
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PCIE GTX_C CRX P15	CV36	1	2	0.22U_0402_10V6K	PCIE GTX CRX P15	AL32
PCIE GTX_C CRX N15	CV37	1	2	0.22U_0402_10V6K	PCIE GTX CRX N15	AN32

16 CLK_PCIE_VGA	AR16
16 CLK_PCIE_VGA#	AR17
16 PEG_CLKREQ#	AR13
PEX_TSTCLK_OUT#	AJ17
PEX_TSTCLK_OUT#	AJ18

18 PLTRST_VGA#	RV103	1	2	0.0402_5%	PLTRST_VGA R#	AM16
	RV104	1	2	2.49K_0402_1%		AG21

16 27M_CLK	RV106	1	2	0.0402_5%	XTALIN	B1
					XTAL_OUT	B2

16 27M_CLK	RV106	1	2	0.0402_5%	XTALIN	B1
					XTAL_OUT	B2

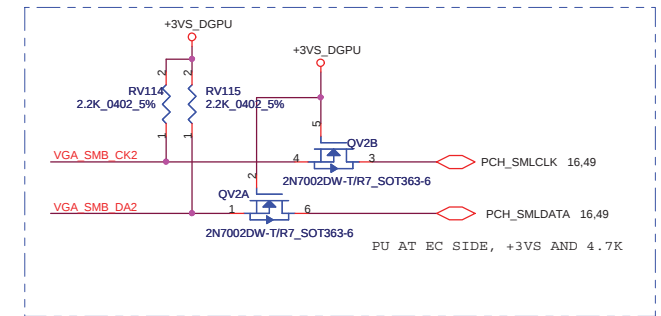
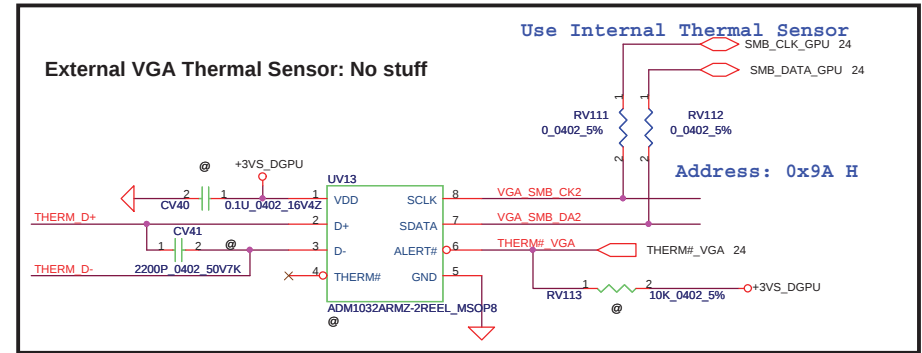
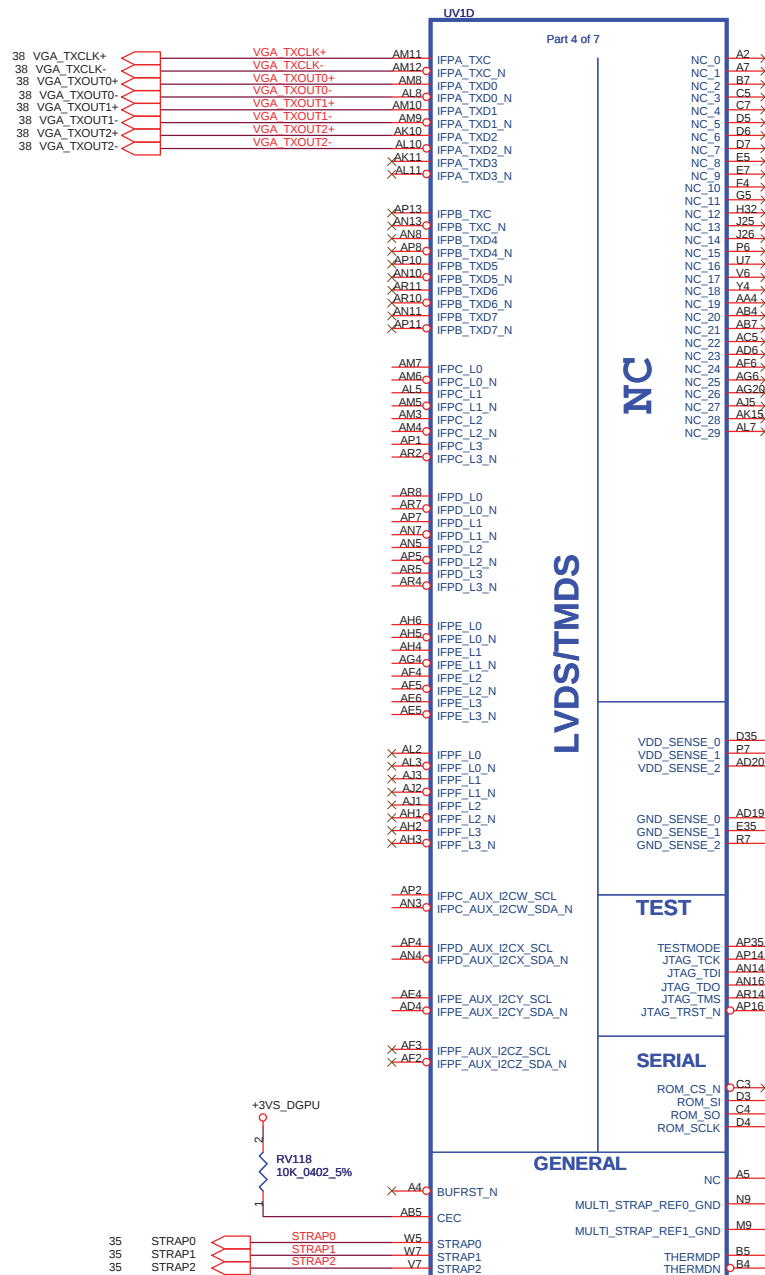
25 SMB_CLK_GPU	SMB_CLK_GPU E2
25 SMB_DATA_GPU	SMB_DATA_GPU E1
38 VGA_LCD_CLK	VGA_LCD_CLK E3
38 VGA_LCD_DATA	VGA_LCD_DATA E4

I2CB_SCL	G3
I2CB_SDA	G2
VGA_DDC_CLK	G1
VGA_DDC_DATA	G4

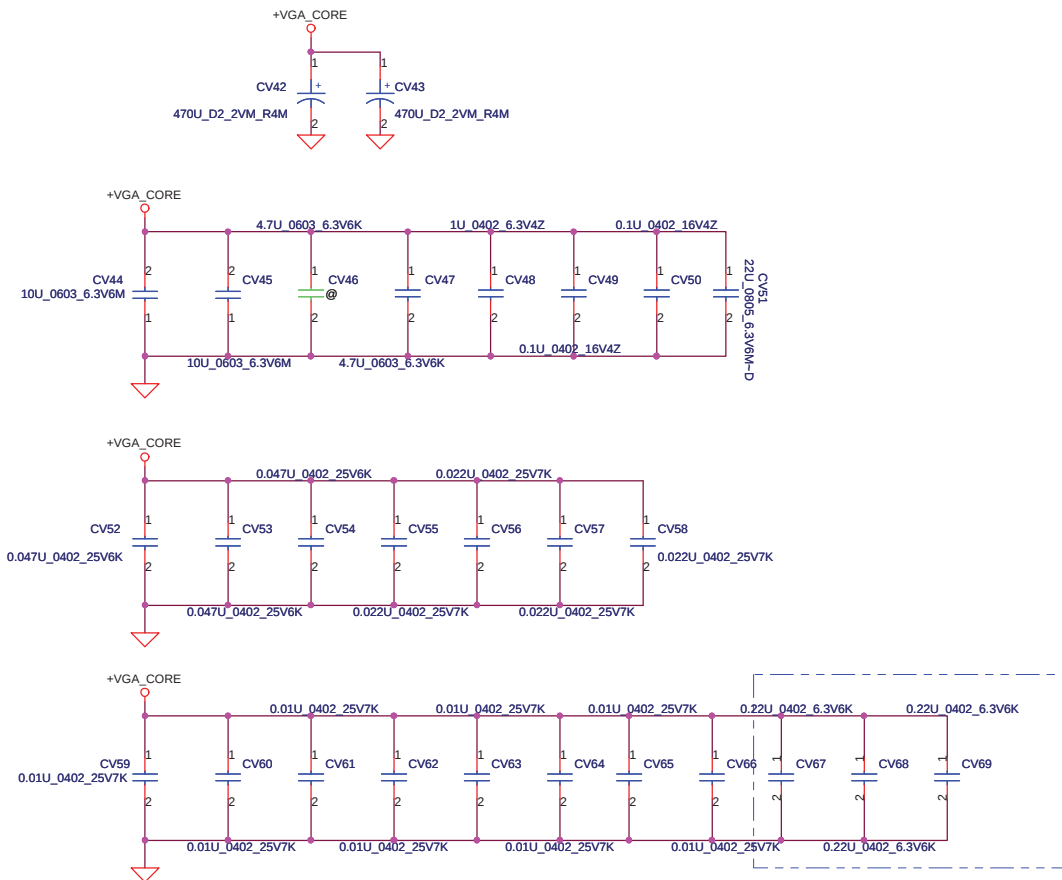
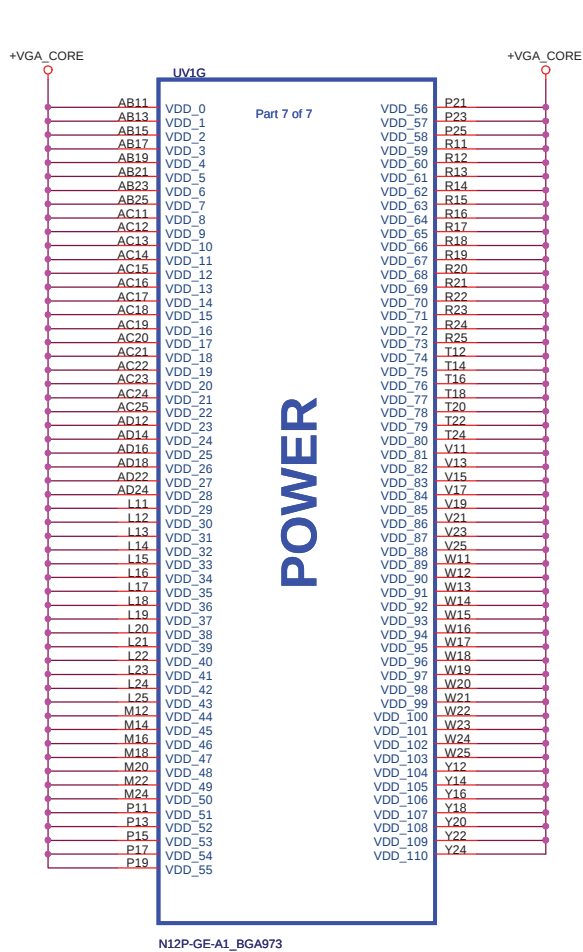
HDCP_SCL	F6
HDCP_SDA	G6

N12P-GE-A1_BGA973

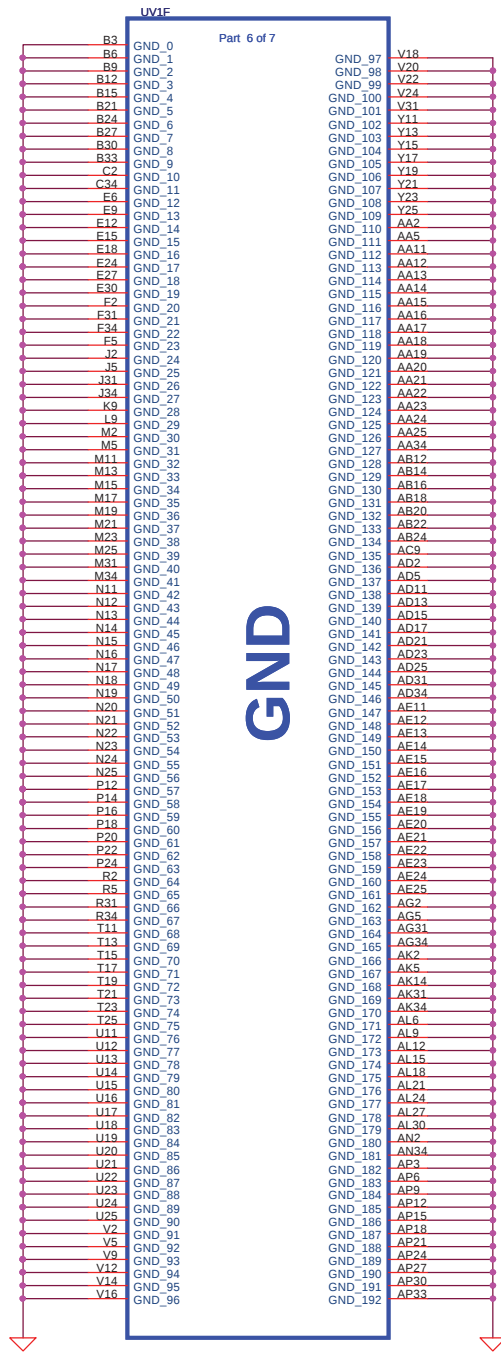
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Compal Electronics, Inc.		VGA(1/12)-PCIE/DAC/GPIO	
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								LA-7391P			
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								Date: Thursday, April 07, 2011			
								Sheet 25 of 64			

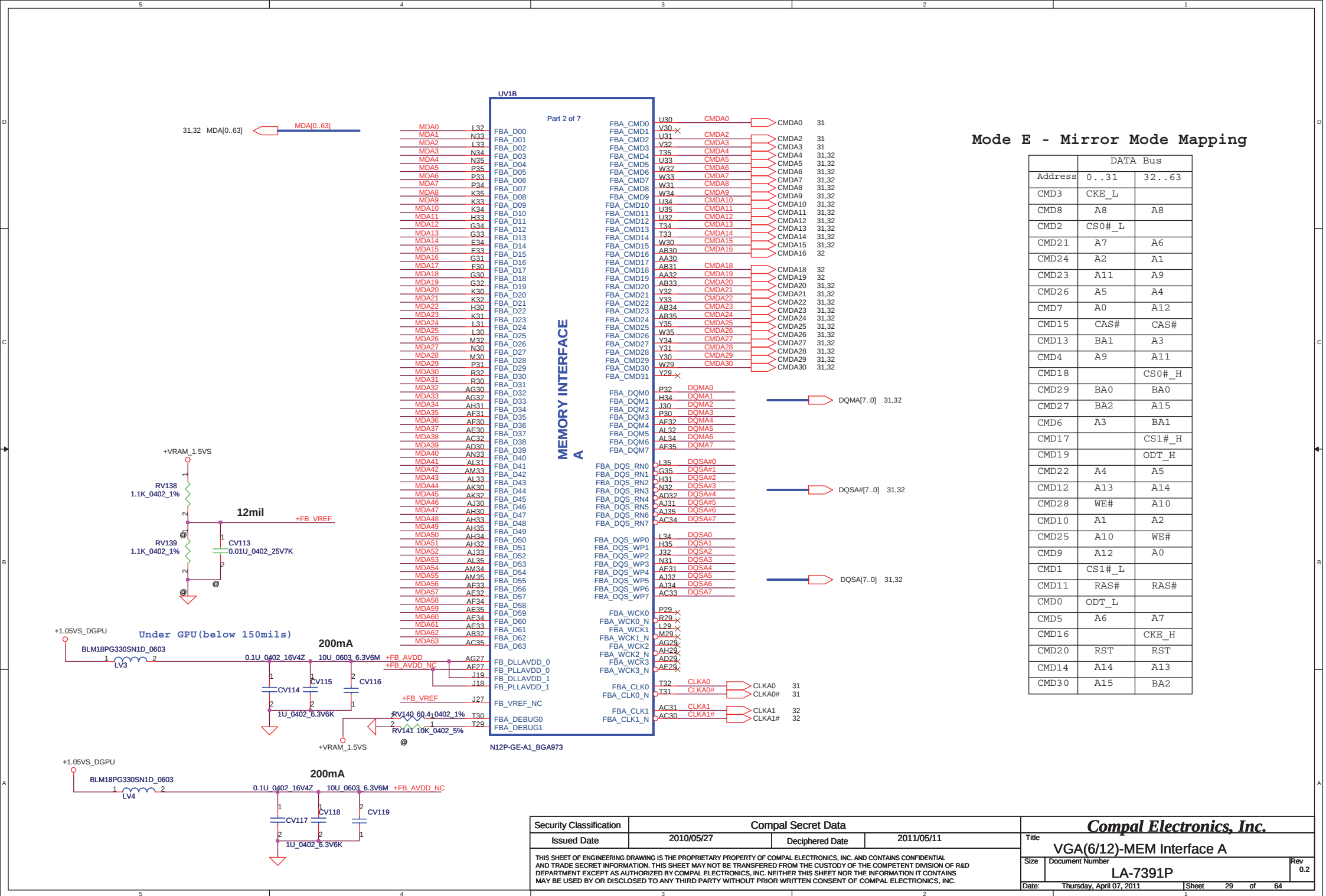


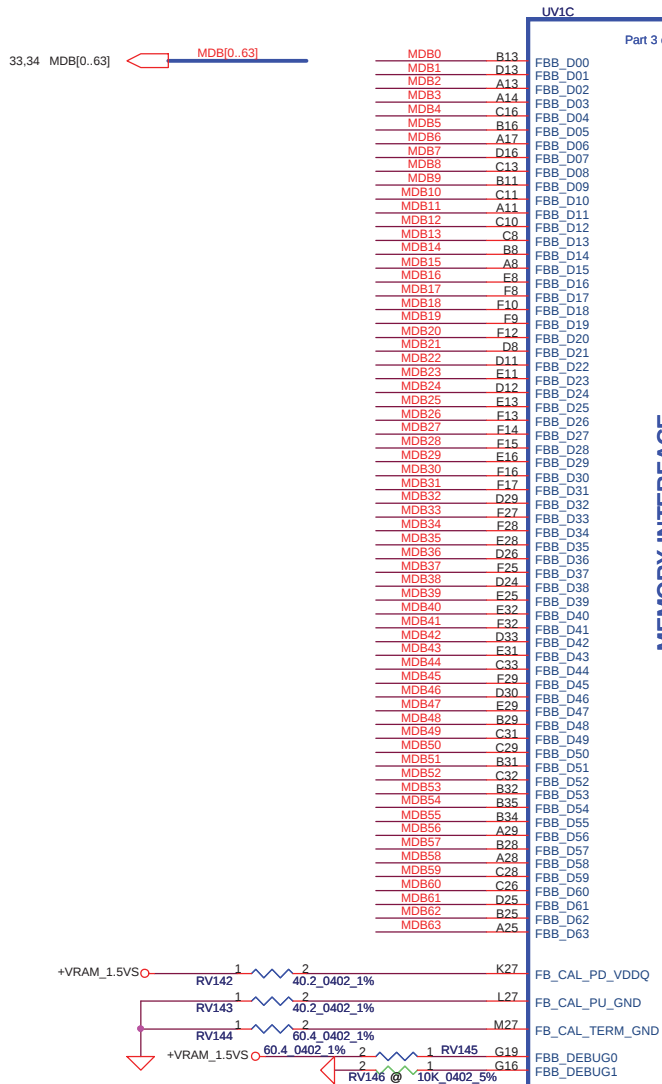
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				Date:	Thursday, April 07, 2011	Sheet 26 of 64



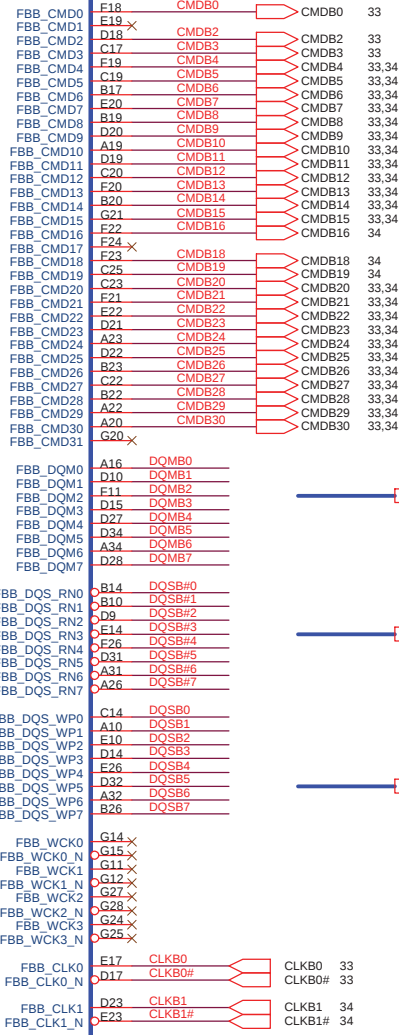
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				Date:	Thursday, April 07, 2011
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				Rev	0.2





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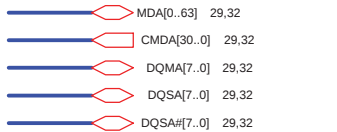
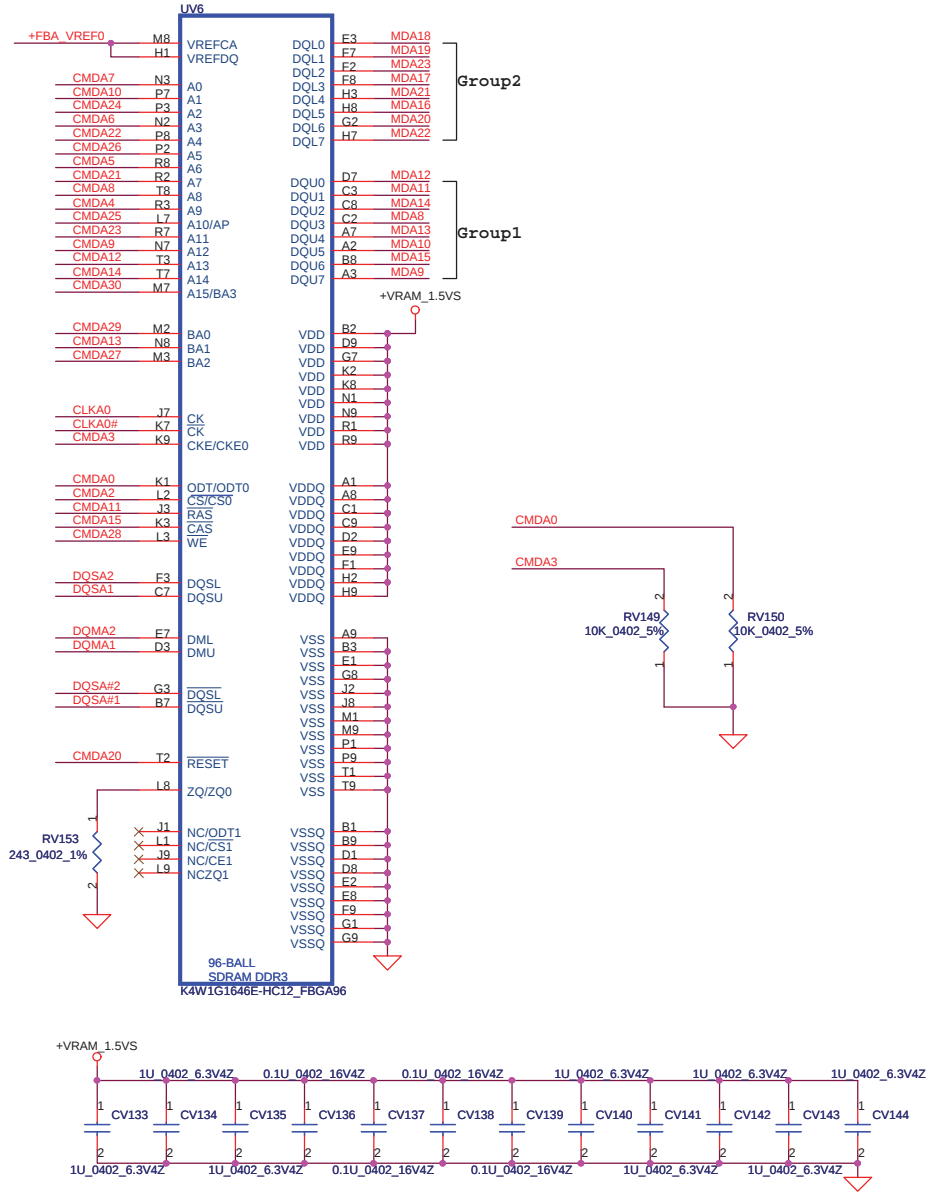
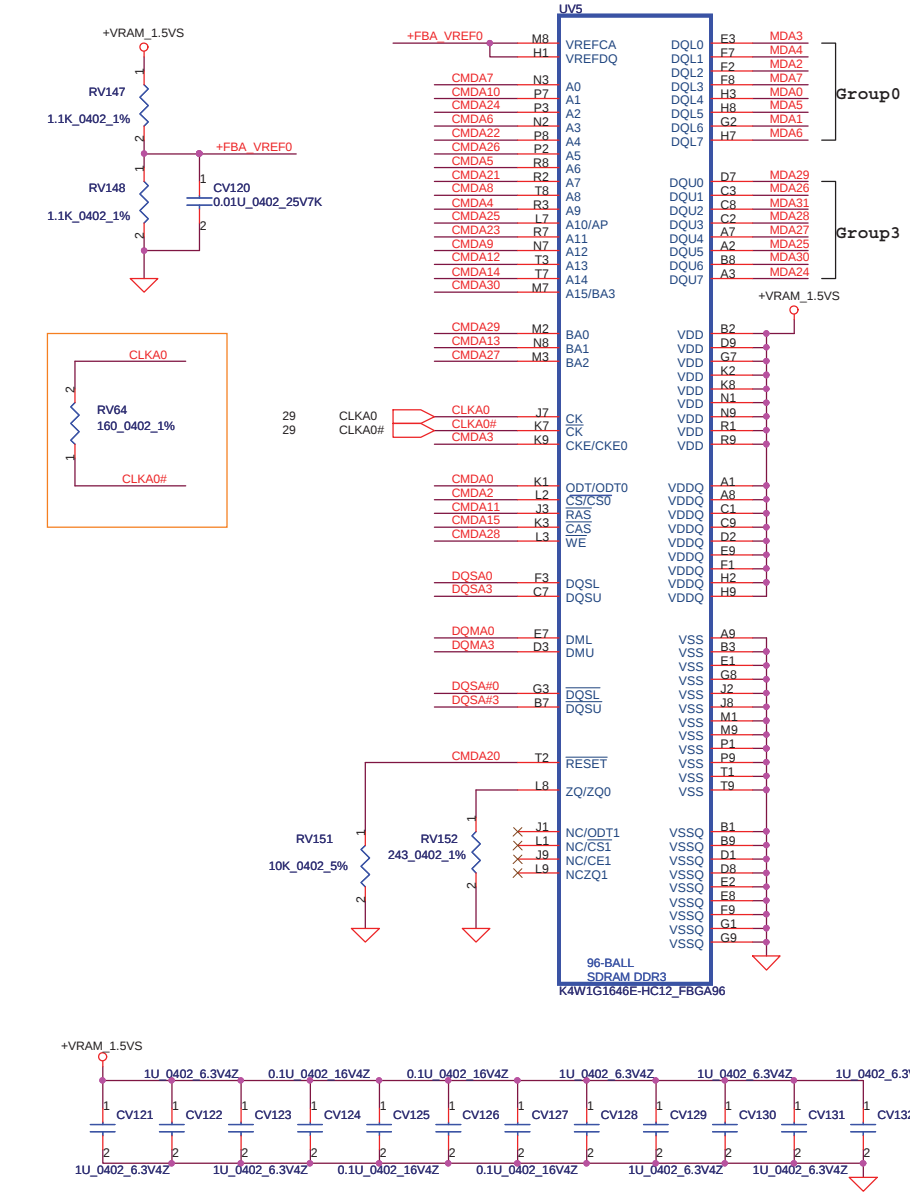


Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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						Size		Document Number		Rev	
								LA-7391P		0.2	
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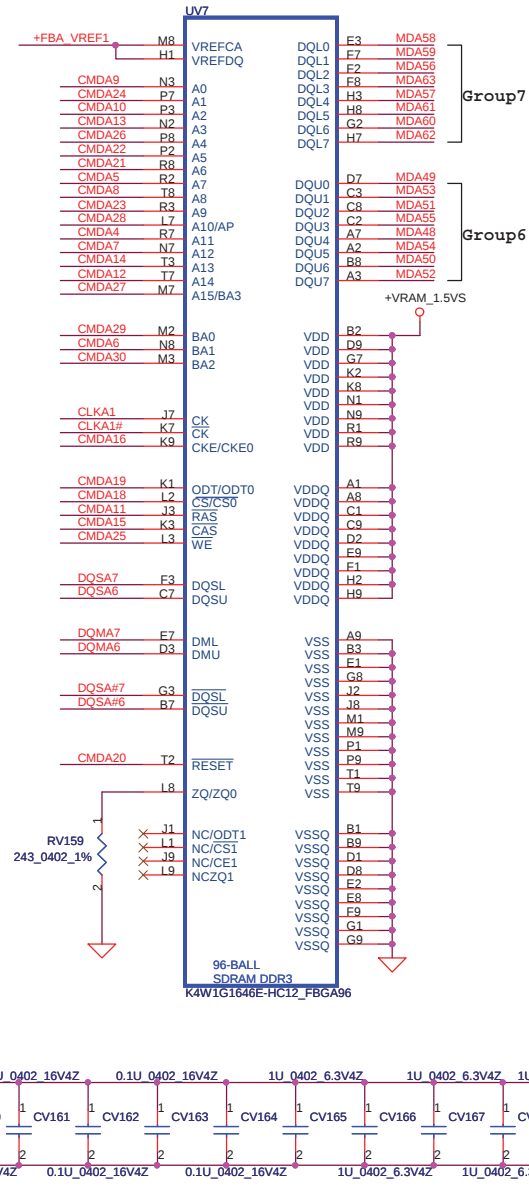
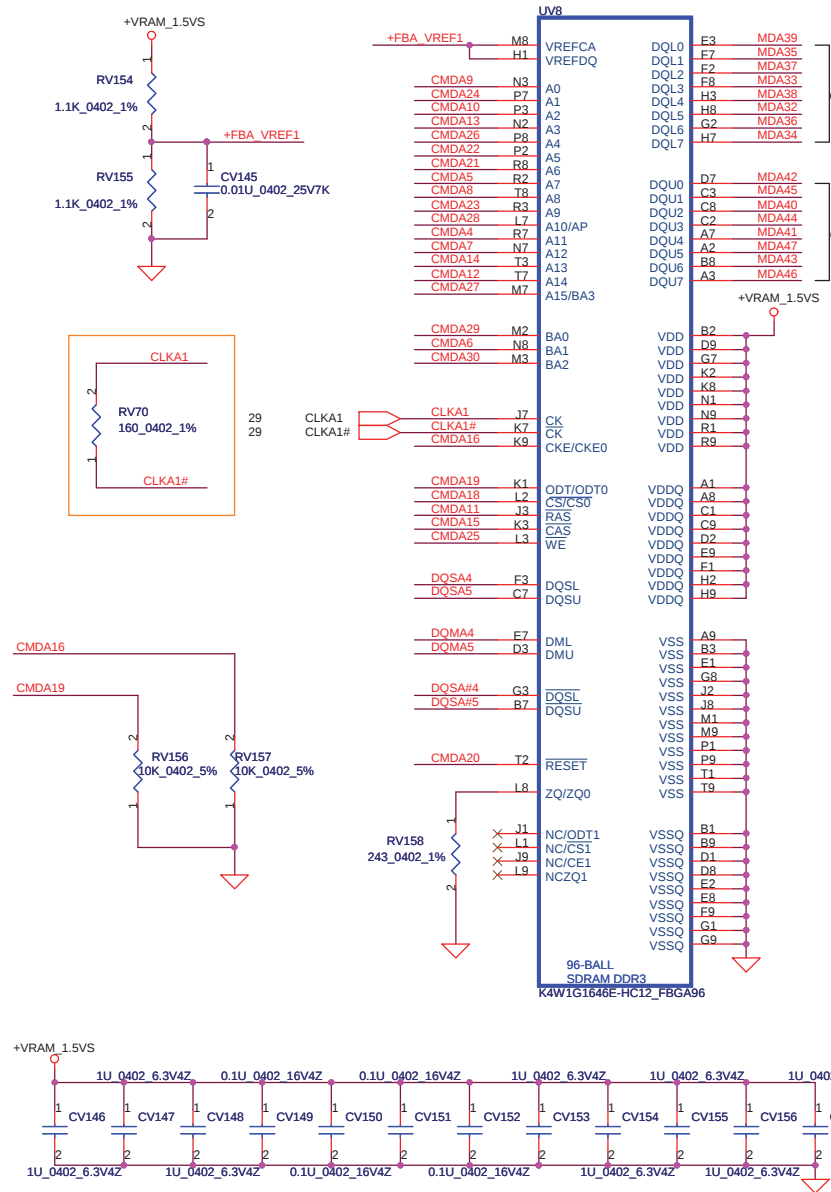
Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

Address		DATA Bus	
		0..31	32..63
CMD3	CKE_L		
CMD8	A8		A8
CMD2	CS0#_L		
CMD21	A7		A6
CMD24	A2		A1
CMD23	A11		A9
CMD26	A5		A4
CMD7	A0		A12
CMD15	CAS#		CAS#
CMD13	BA1		A3
CMD4	A9		A11
CMD18			CS0#_H
CMD29	BA0		BA0
CMD27	BA2		A15
CMD6	A3		BA1
CMD17			CS1#_H
CMD19			ODT_H
CMD22	A4		A5
CMD12	A13		A14
CMD28	WE#		A10
CMD10	A1		A2
CMD25	A10		WE#
CMD9	A12		A0
CMD1	CS1#_L		
CMD11	RAS#		RAS#
CMD0	ODT_L		
CMD5	A6		A7
CMD16			CKE_H
CMD20	RST		RST
CMD14	A14		A13
CMD30	A15		BA2

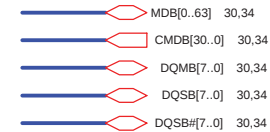
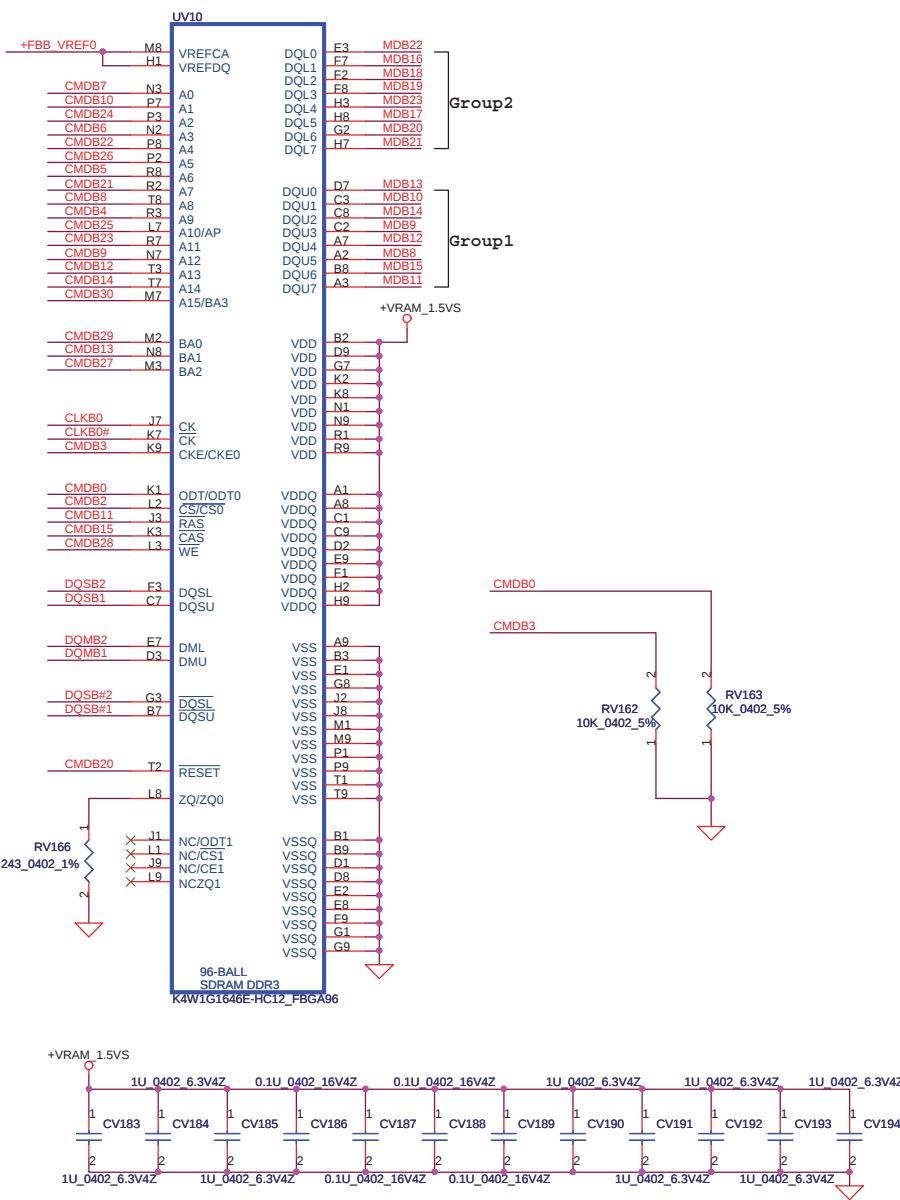
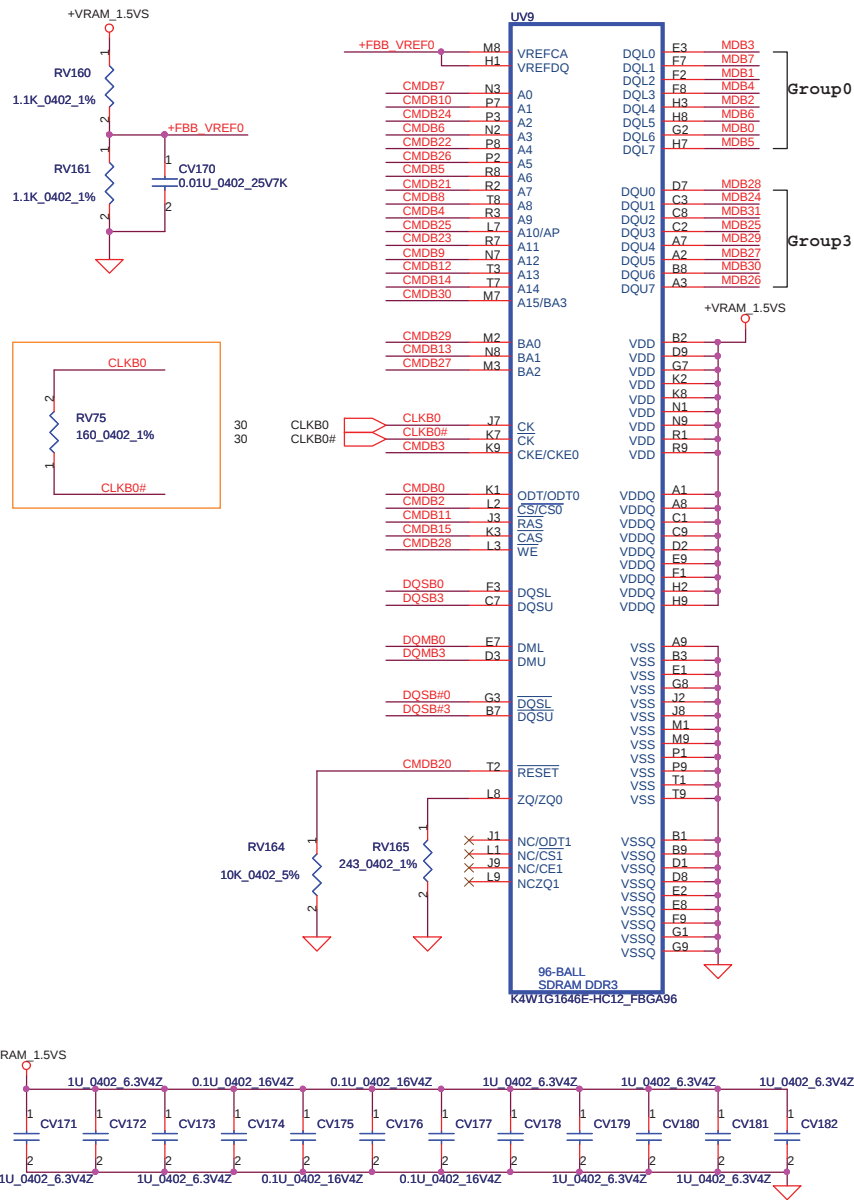
Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0...31	32...63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

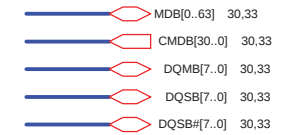
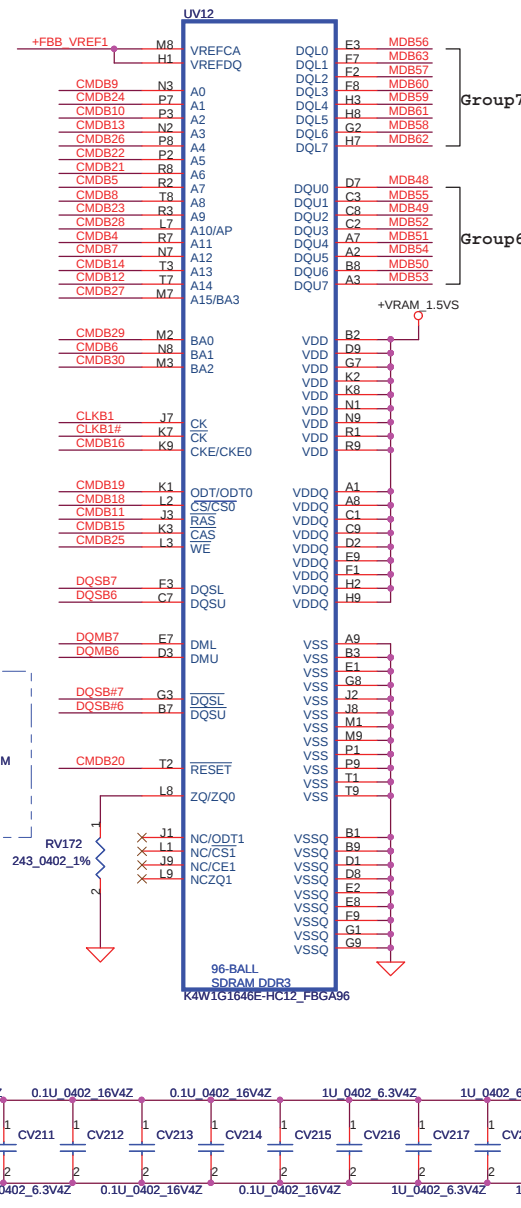
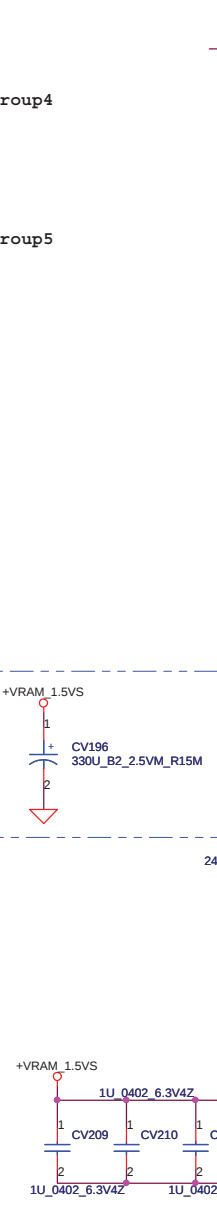
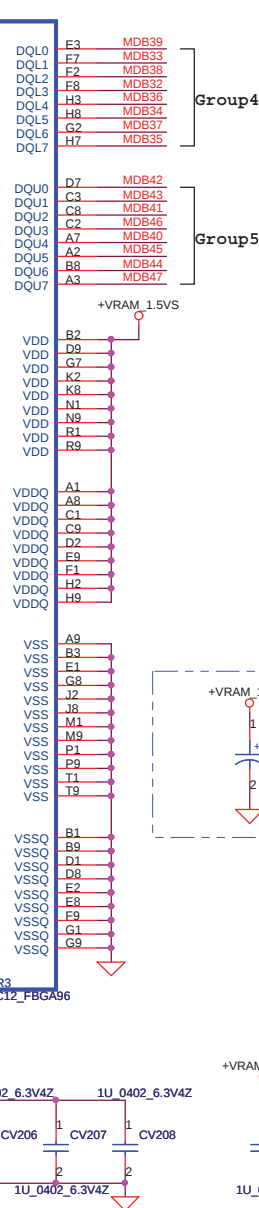
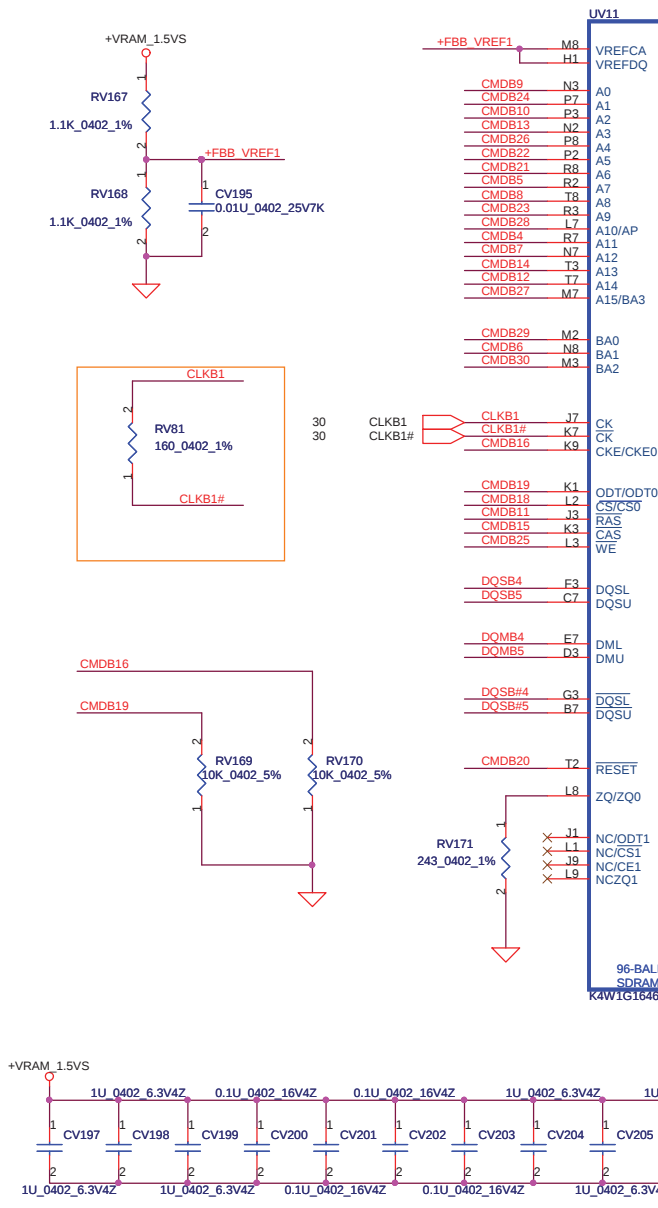
Memory Partition C - Lower 32 bits



Mode E - Mirror Mode Mapping

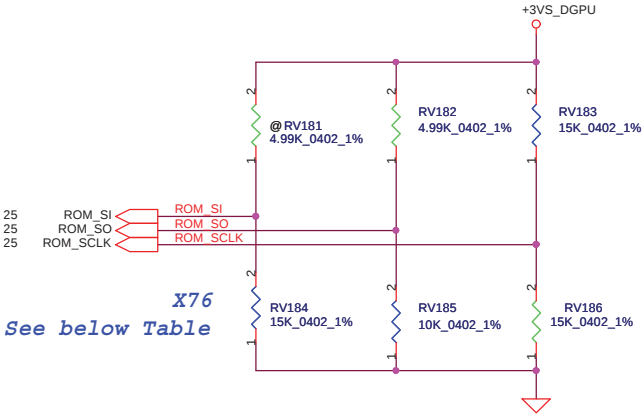
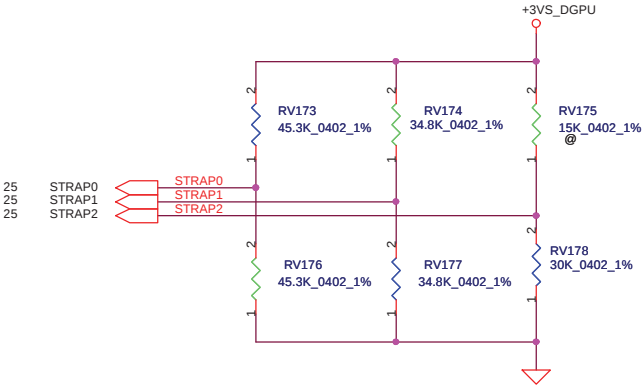
DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

Memory Partition C - Upper 32 bits



Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



X76
See below Table

ROM_SO : PL10K
Strap1 : PL35K
Strap0 : PH45K

Hynix	64Mx16 H5TQ1G63DFR-11C SA0000324E0	0010	PD 15K
	128MX16 H5TQ2G63BFR-11C SA00003Y000	0110	PD 35K
Samsung	64MX16 K4W1G1646E-HC11 SA000041T00	0011	PD 20K
	128M16 K4W2G1646C-HC11 SA000047Q00	0111	PD 45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GV1		Pull up 15K	Pull down 45K
N12P-GE		Pull up 15K	Pull down 30K
N12P-GS		Pull up 15K	Pull down 25K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

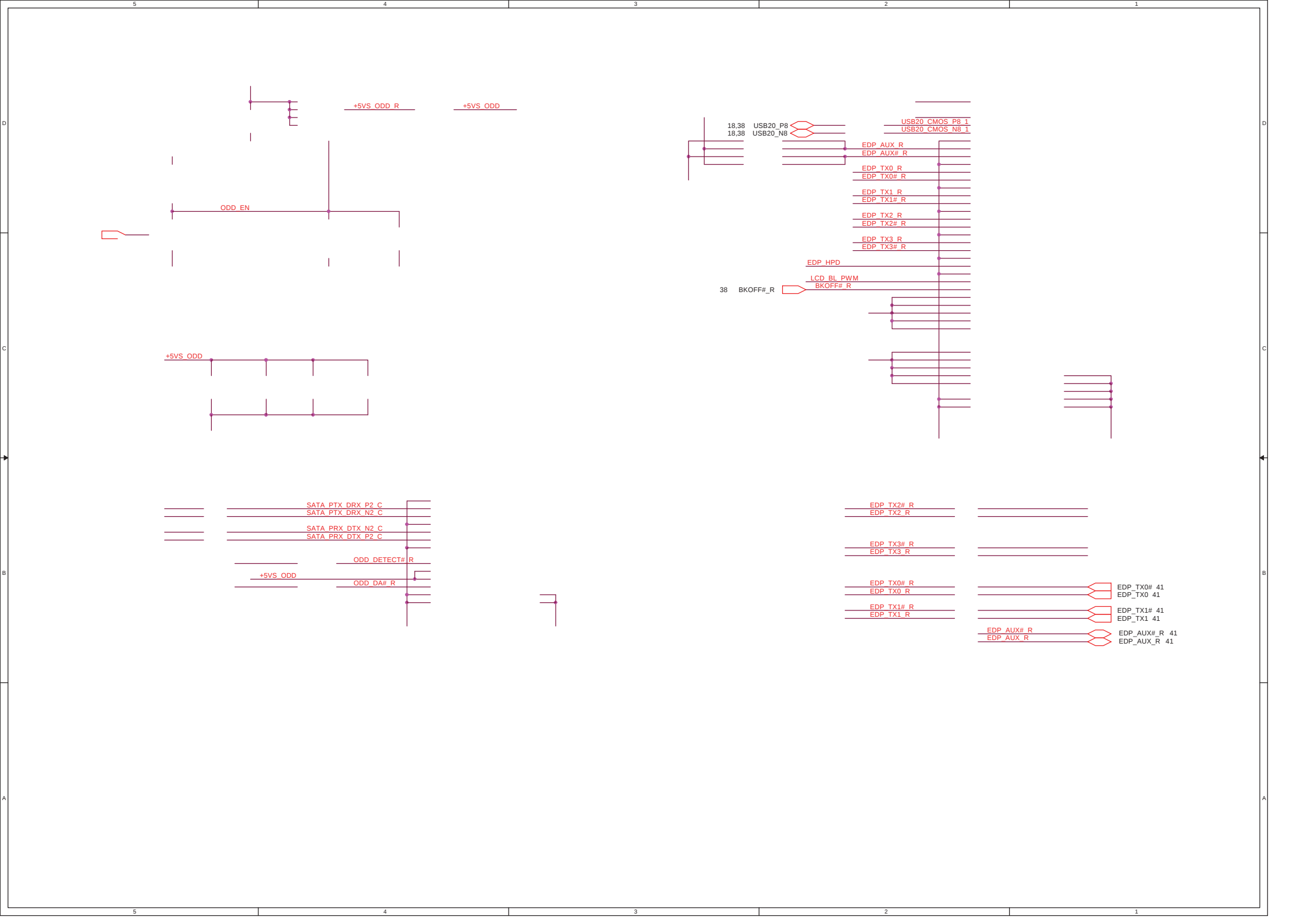
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

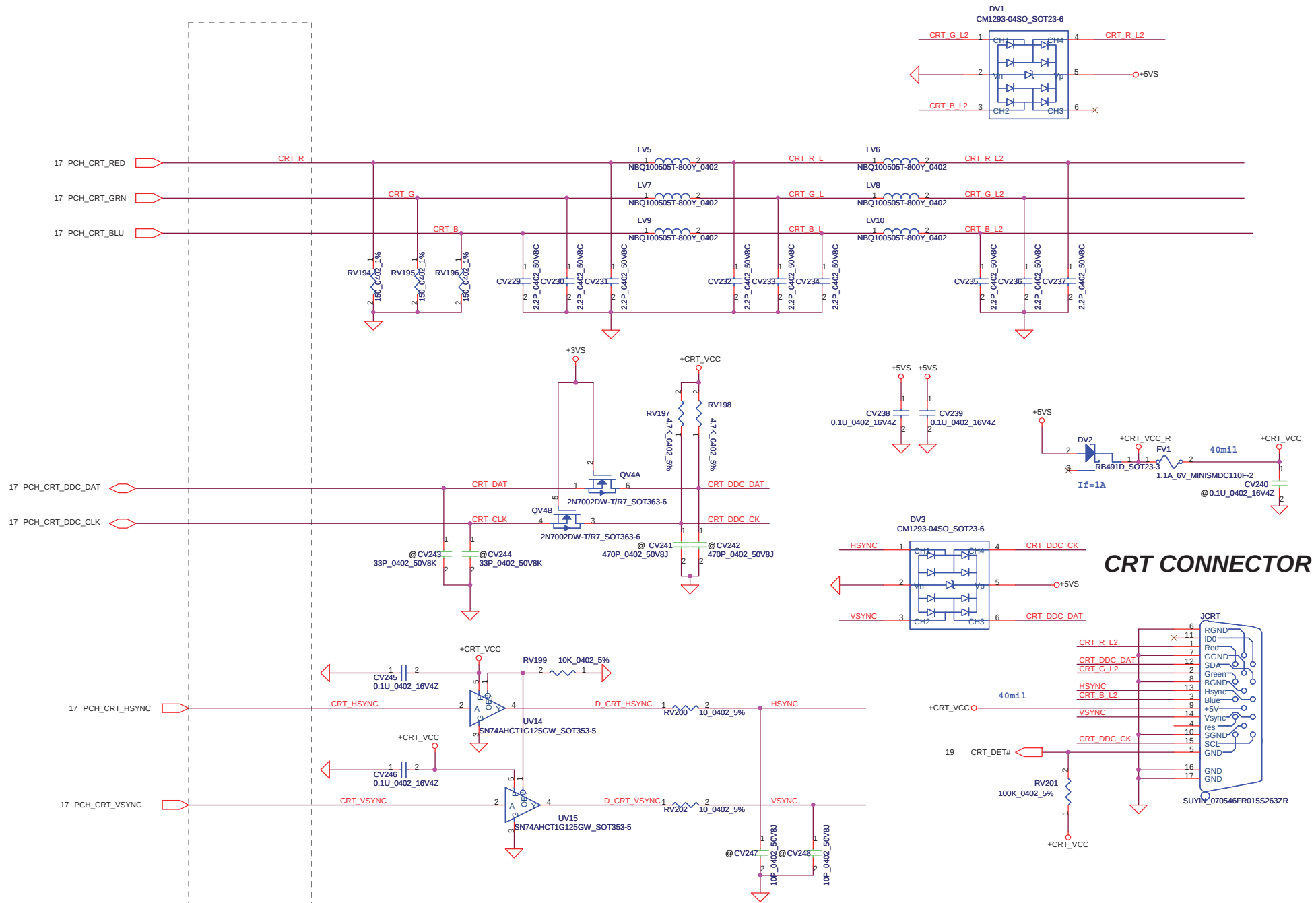
SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

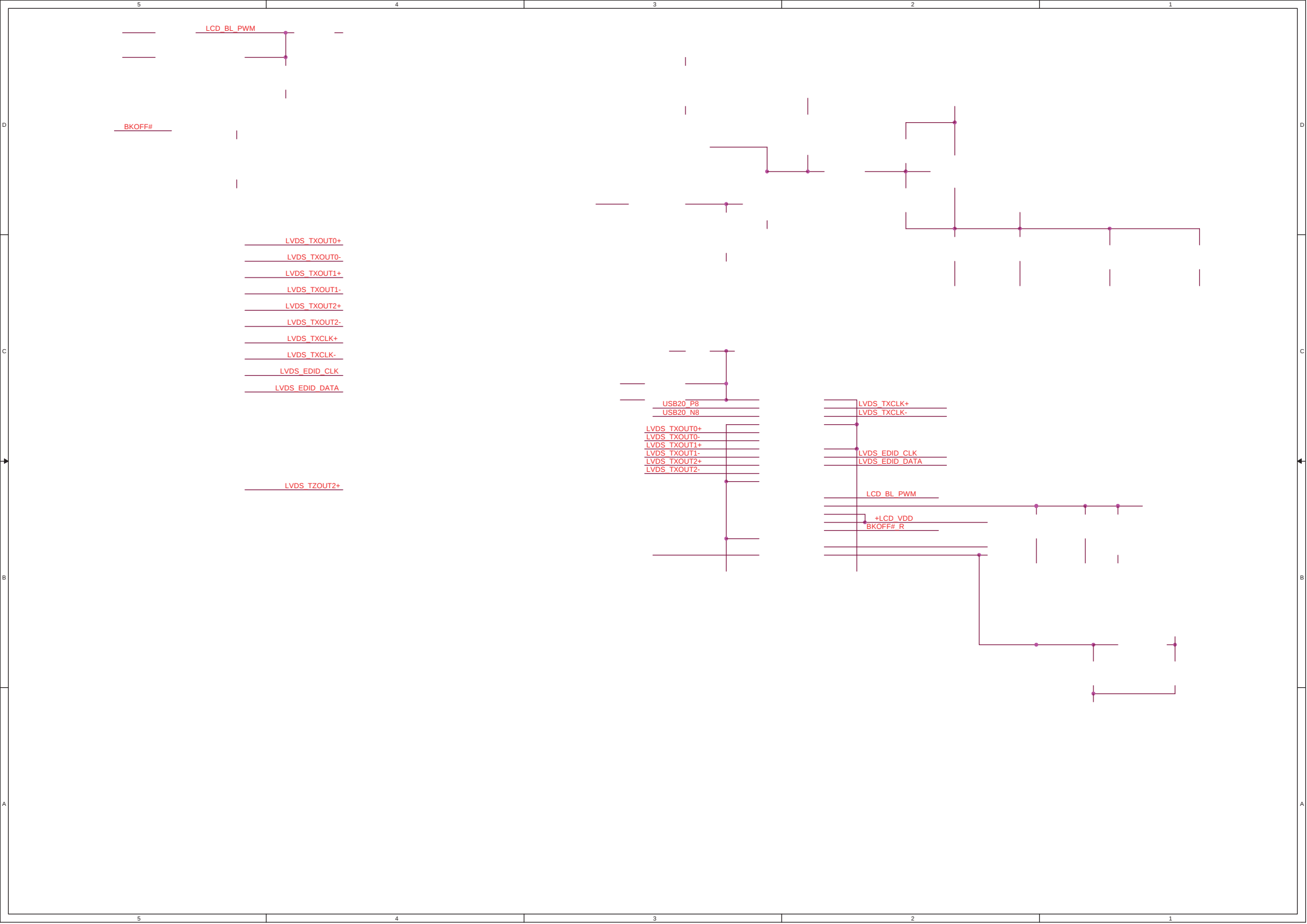
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Issued Date	2010/05/27	Deciphered Date	2011/05/11		Title VGA(12/12)-MISC		
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					Date:	Thursday, April 07, 2011	Sheet 35 of 64

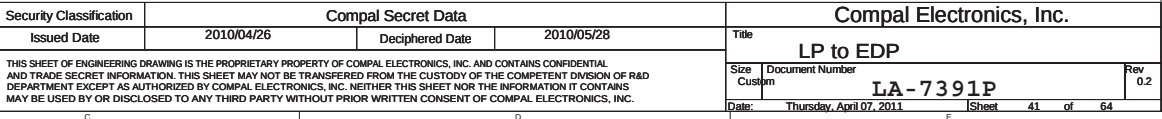




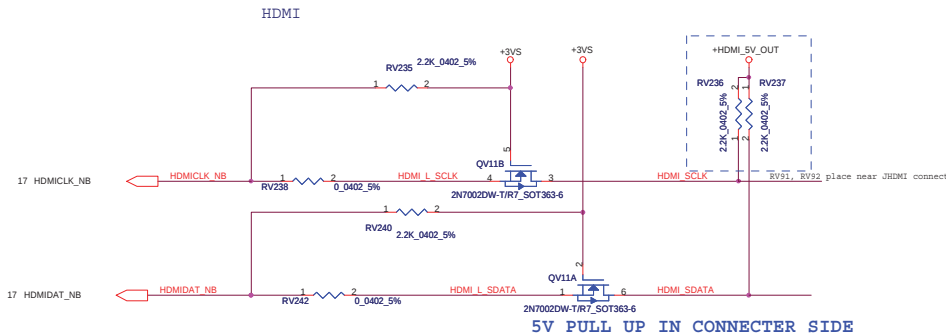
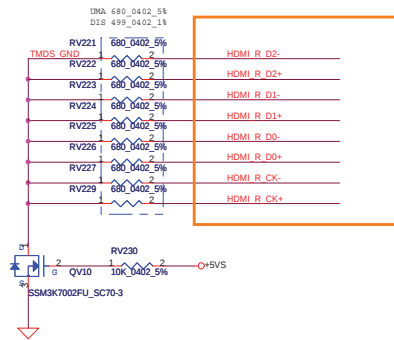
Close to CRT Connector

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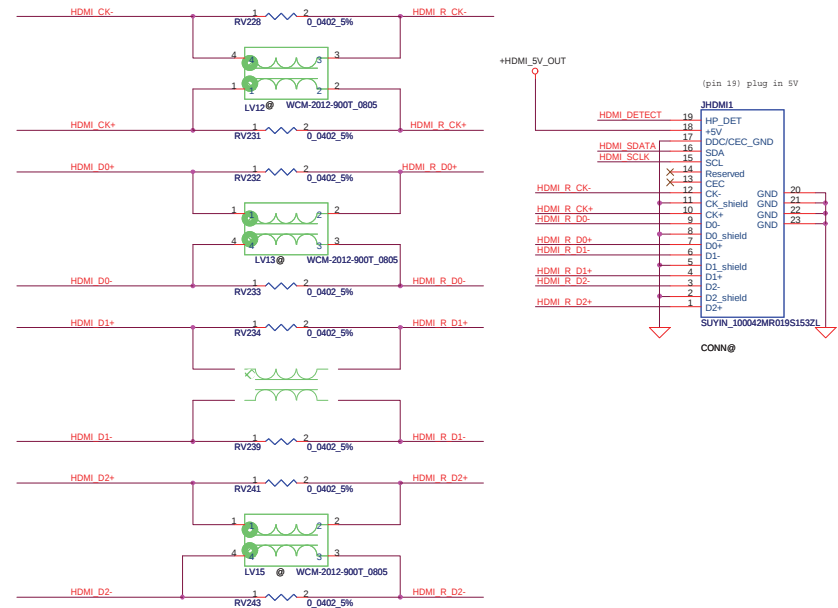
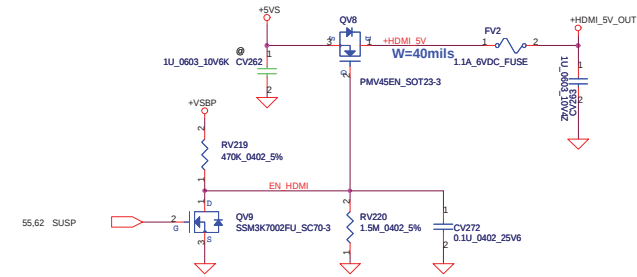
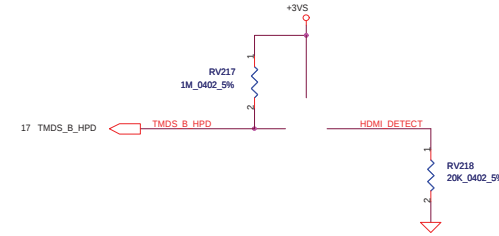




17	TMDS_B_CLK	1	2	1	HDMI CK+
17	TMDS_B_CLK#	1	2	1	HDMI CK-
17	TMDS_B_DATA0	1	2	1	HDMI D0+
17	TMDS_B_DATA0#	1	2	1	HDMI D0-
17	TMDS_B_DATA1	1	2	1	HDMI D1+
17	TMDS_B_DATA1#	1	2	1	HDMI D1-
17	TMDS_B_DATA2	1	2	1	HDMI D2+
17	TMDS_B_DATA2#	1	2	1	HDMI D2-



5V PULL UP IN CONNECTOR SIDE

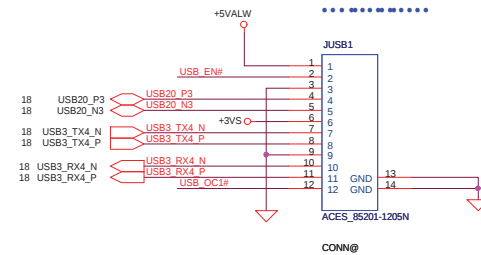
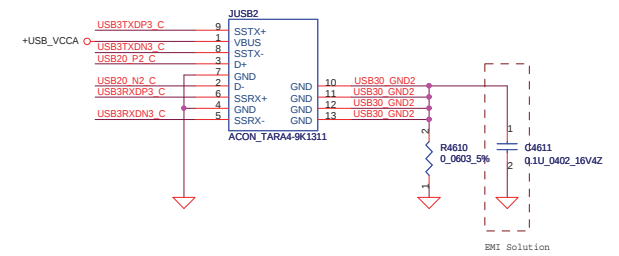
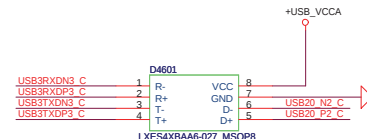
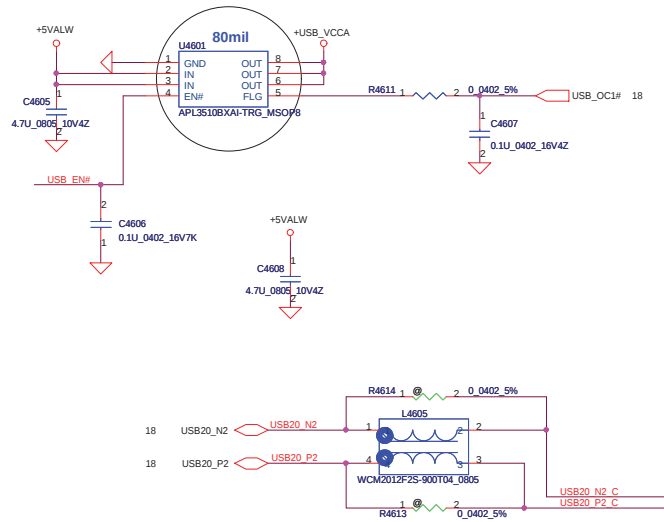
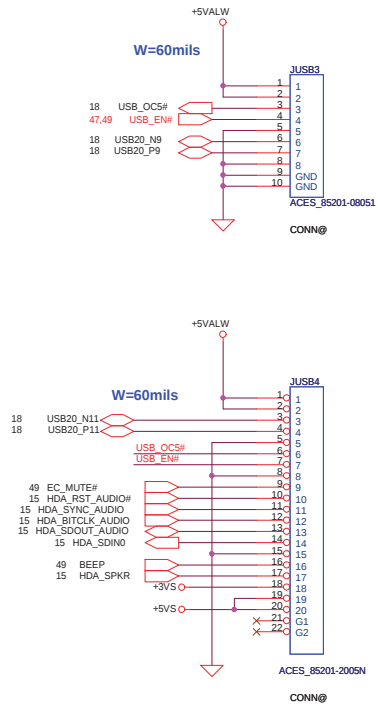


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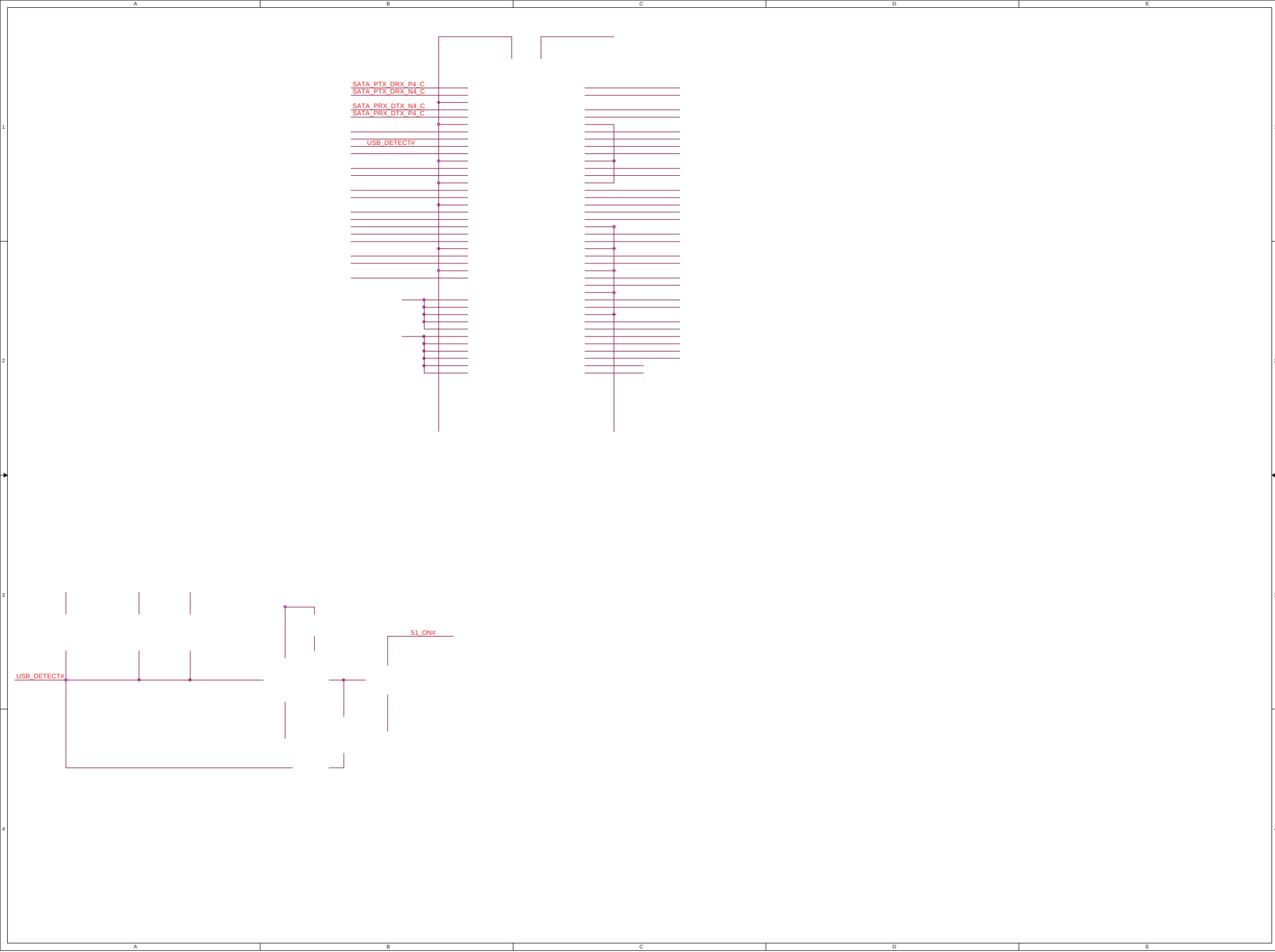
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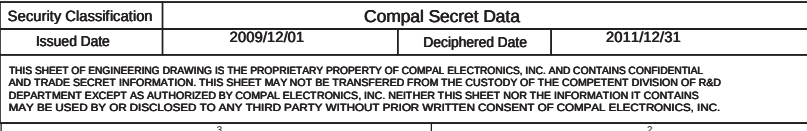
HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK

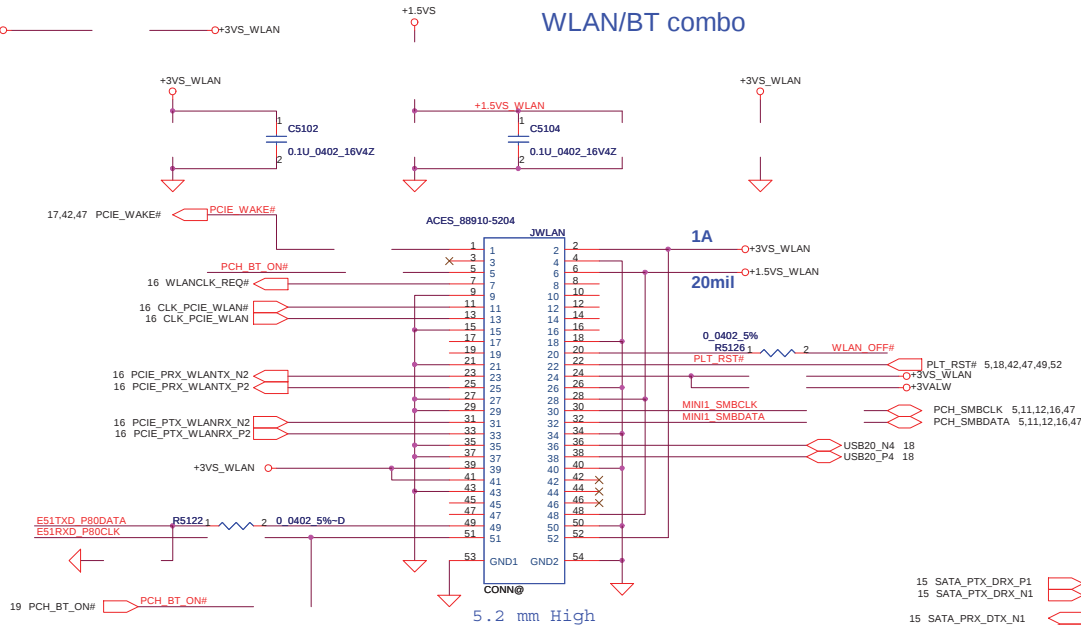


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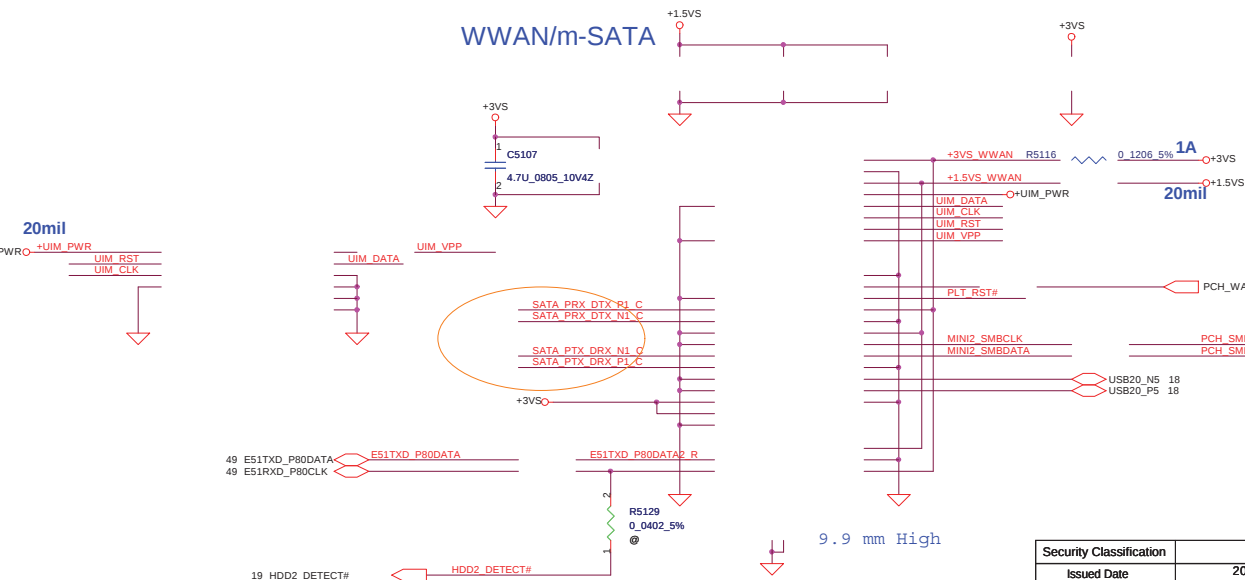




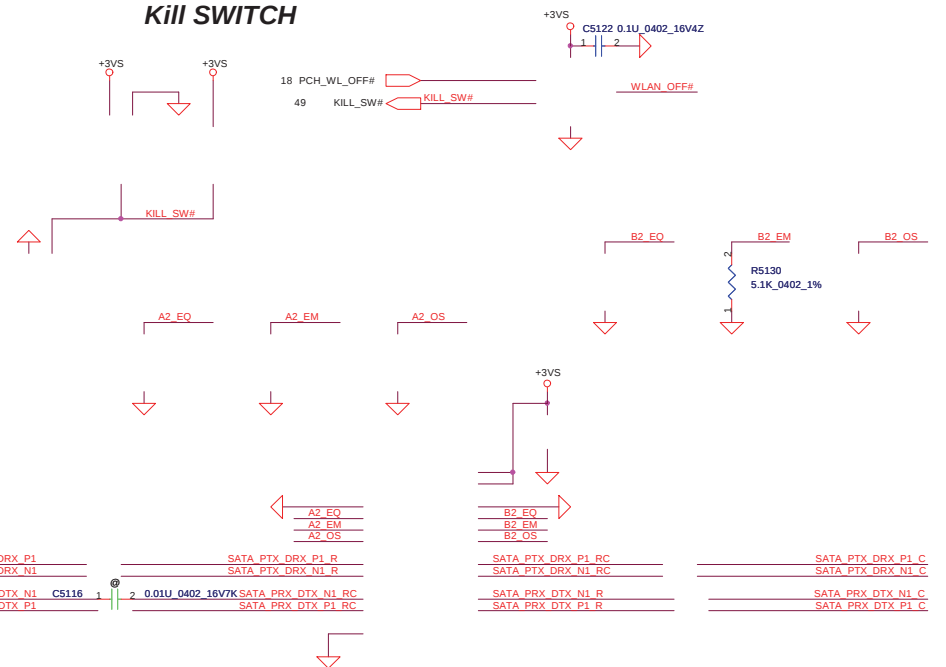
WLAN/BT combo



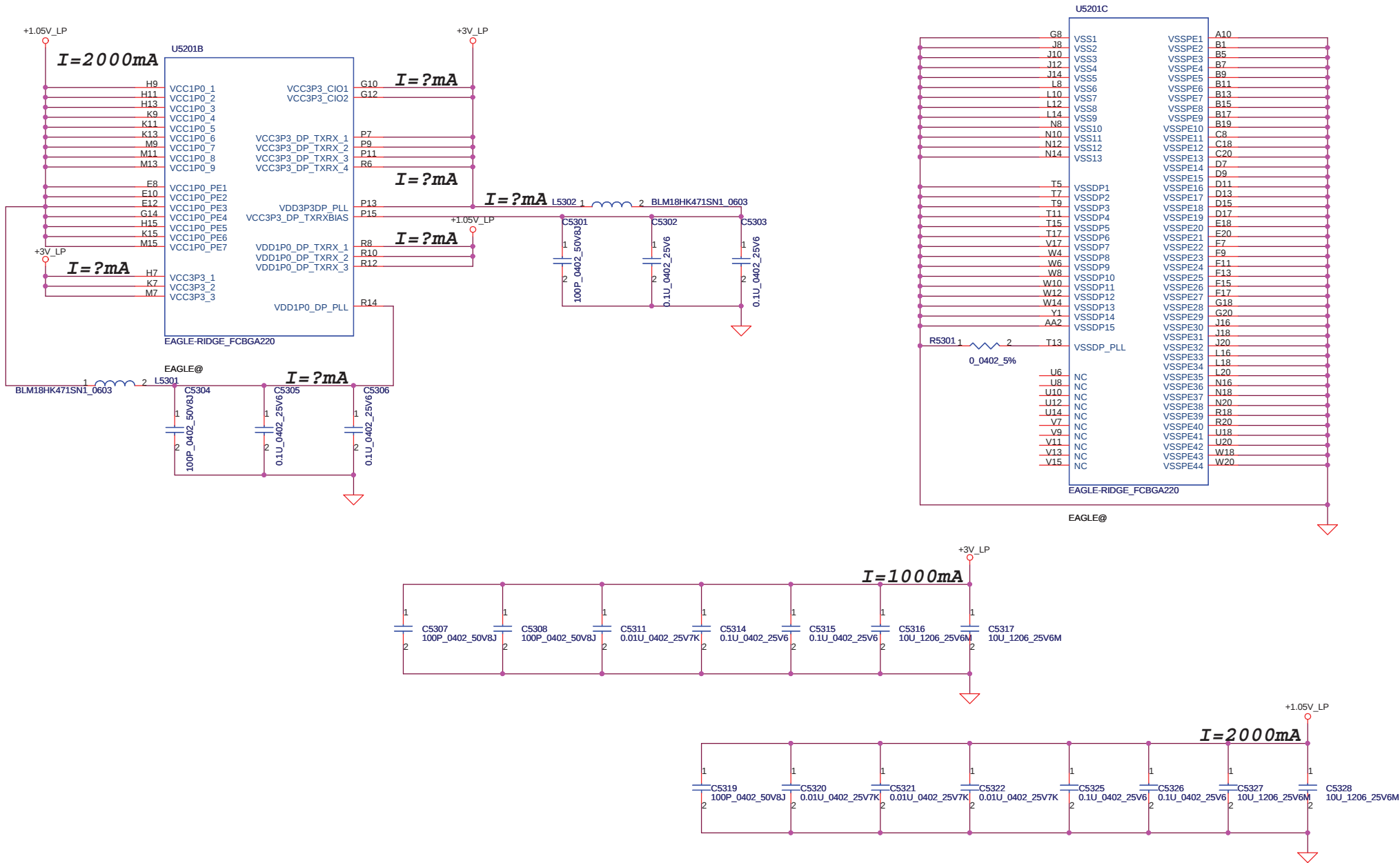
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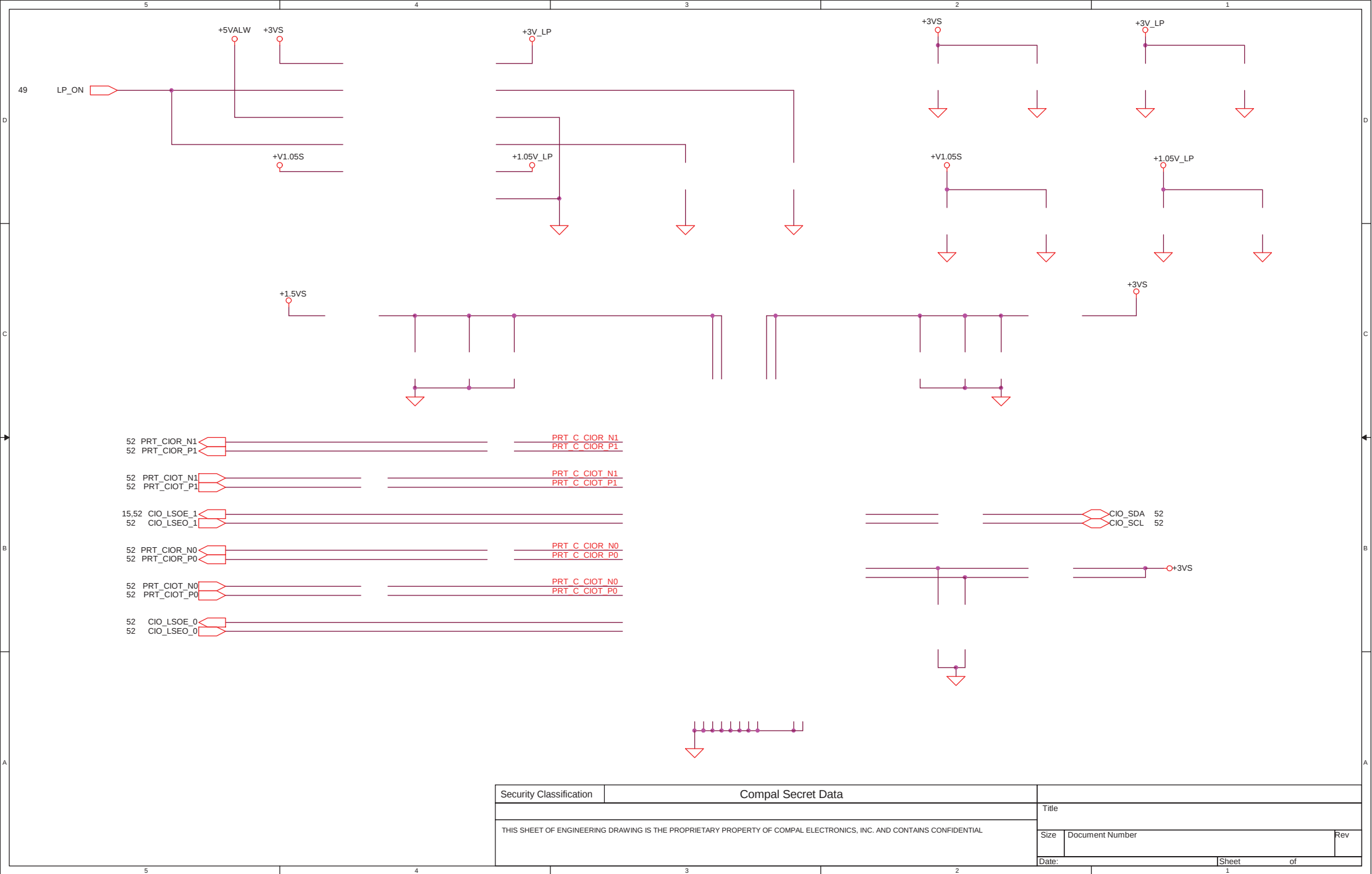
Kill SWITCH



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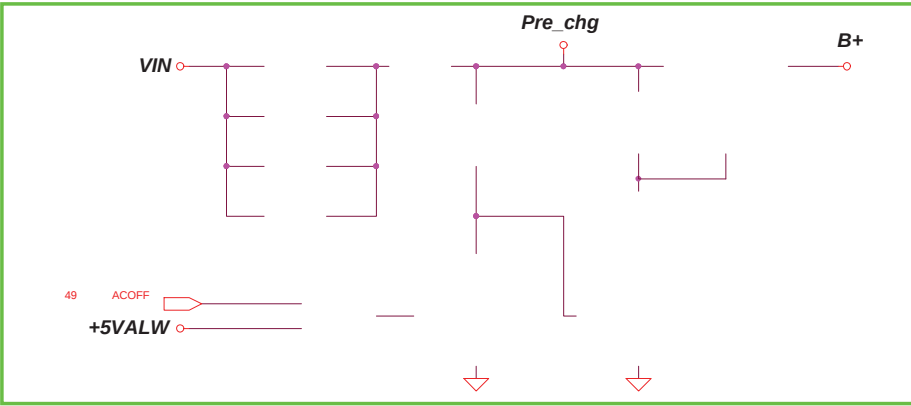
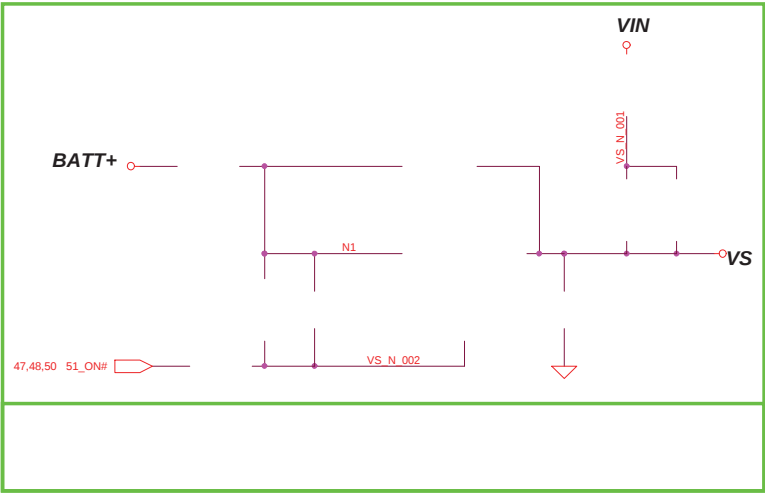
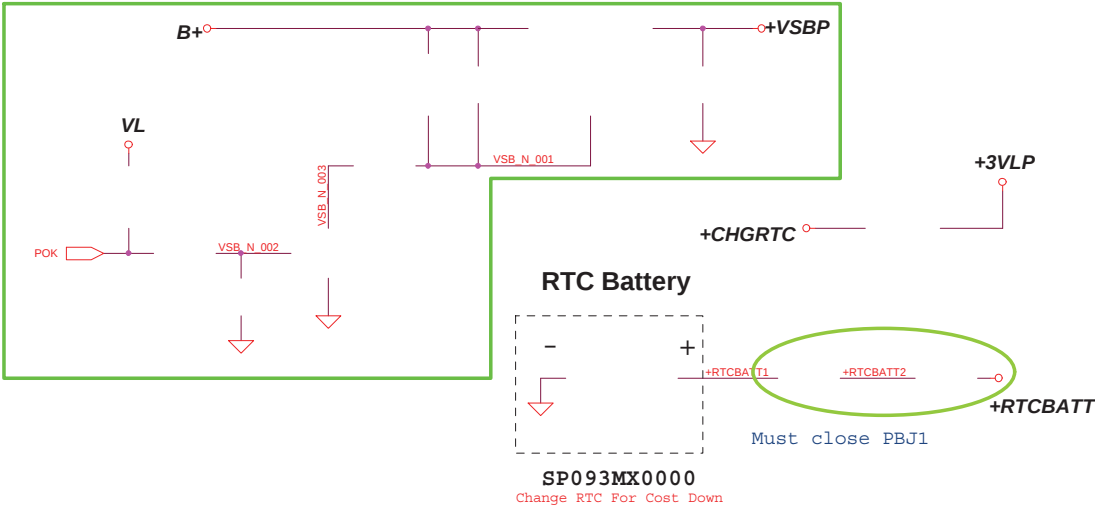
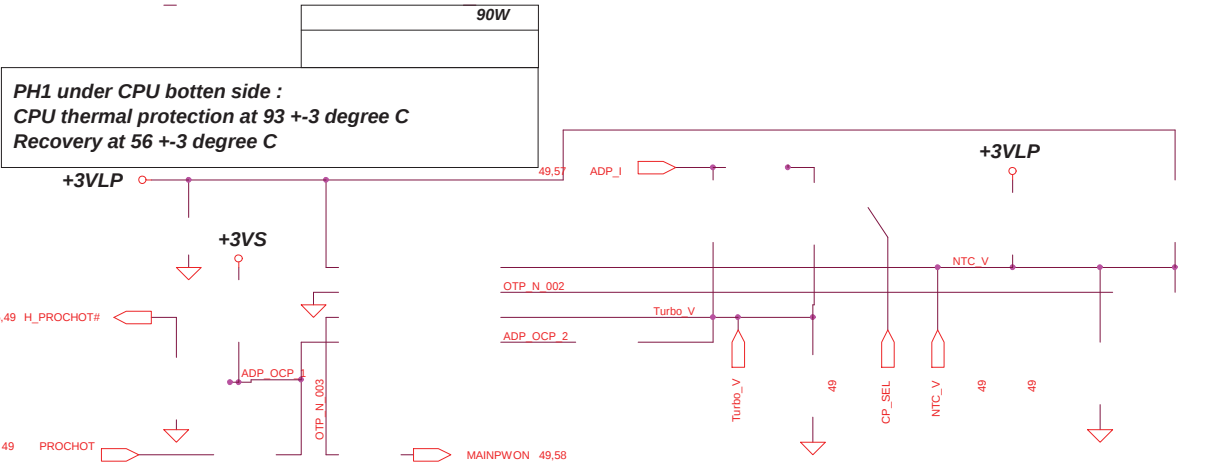
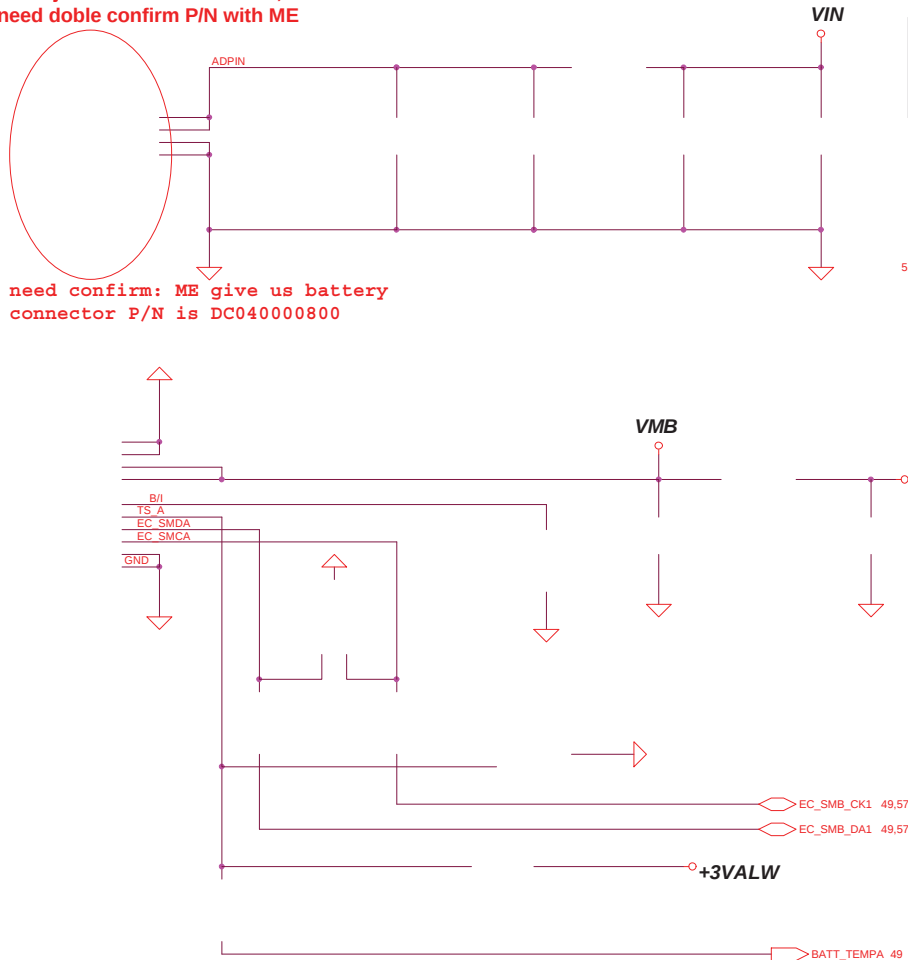


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Size		Document Number		Rev	
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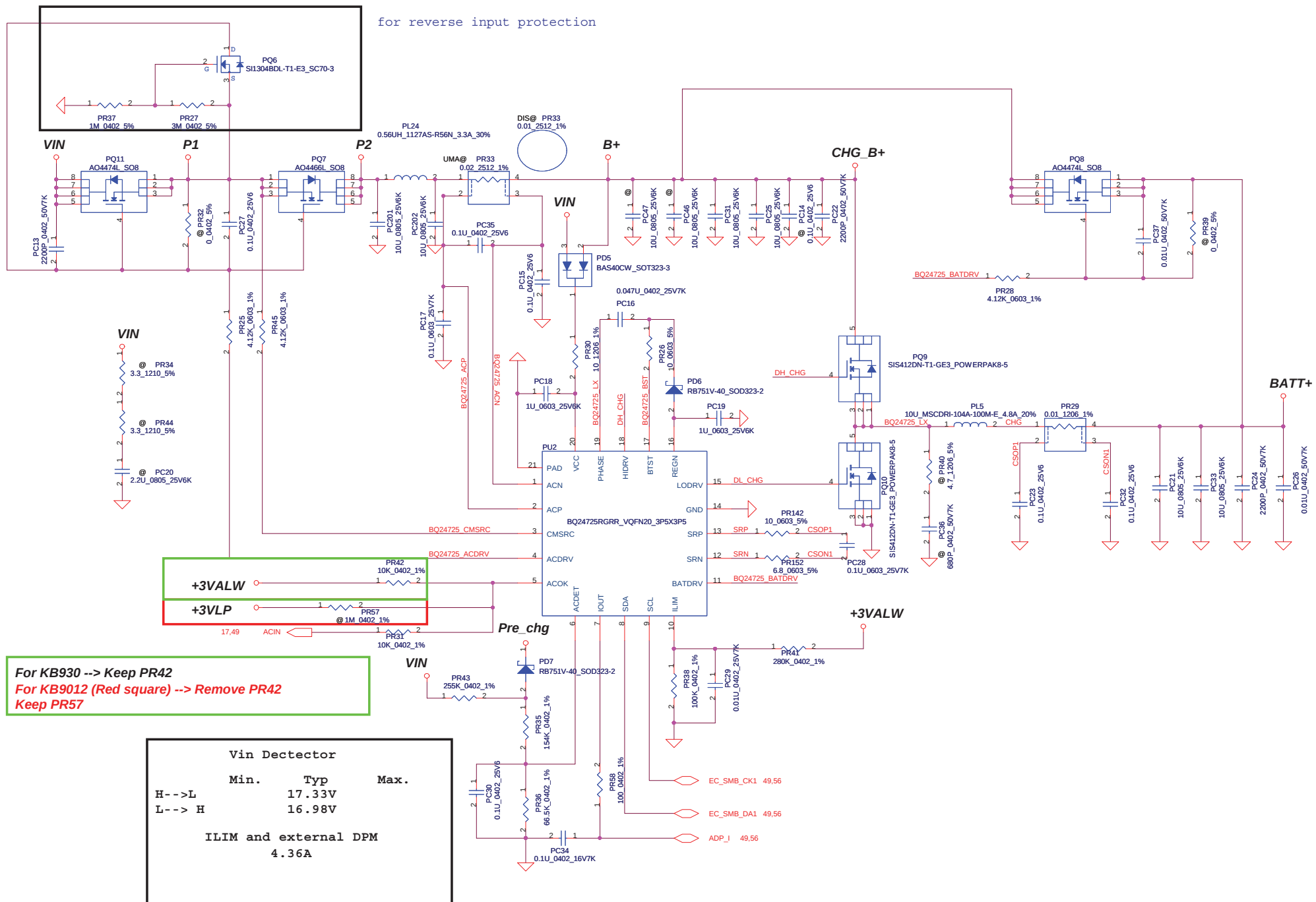


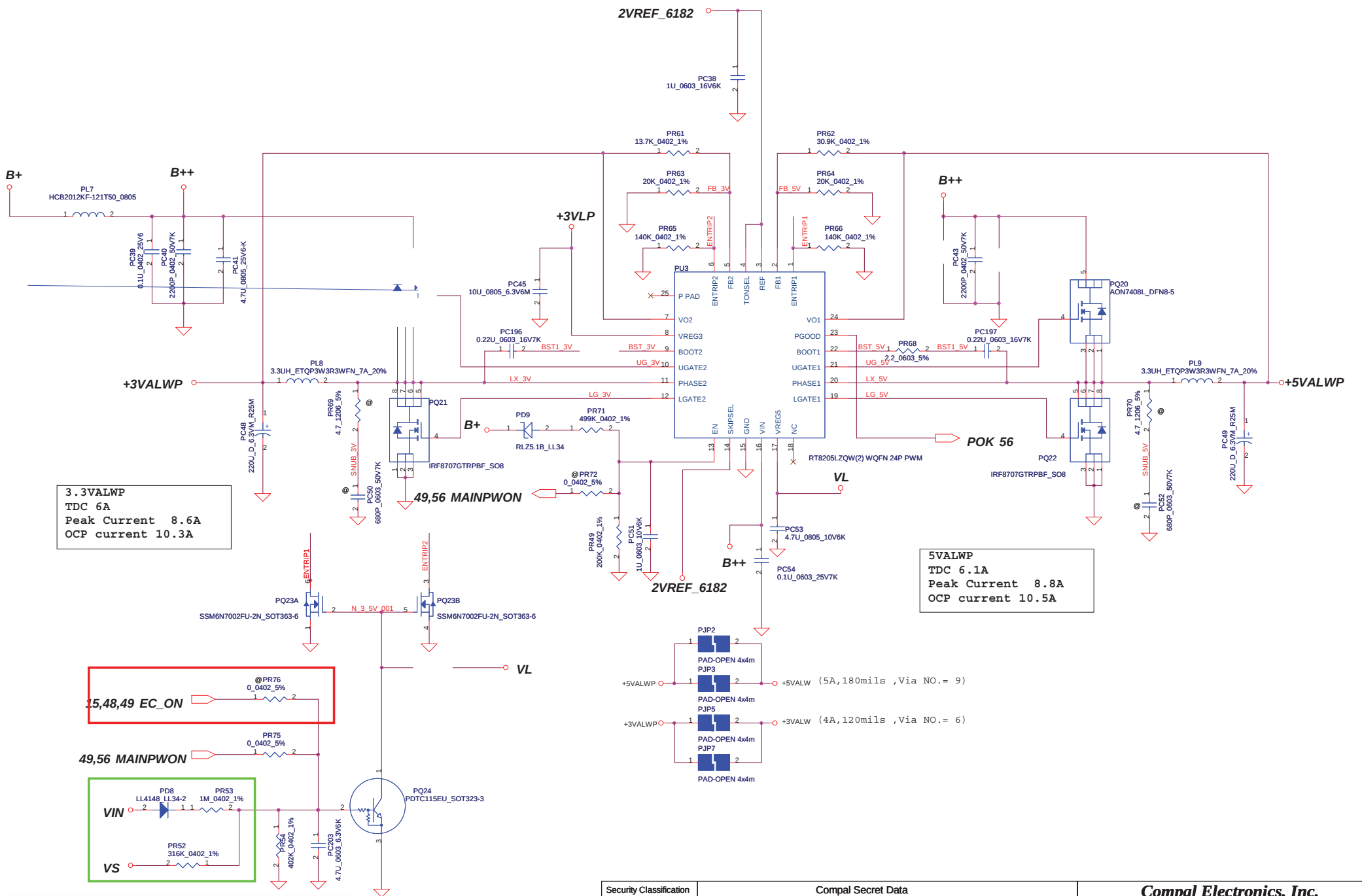
DCIN jack P/N:DC301008L00,
need dogle confirm P/N with ME

need confirm: ME give us battery
connector P/N is DC040000800



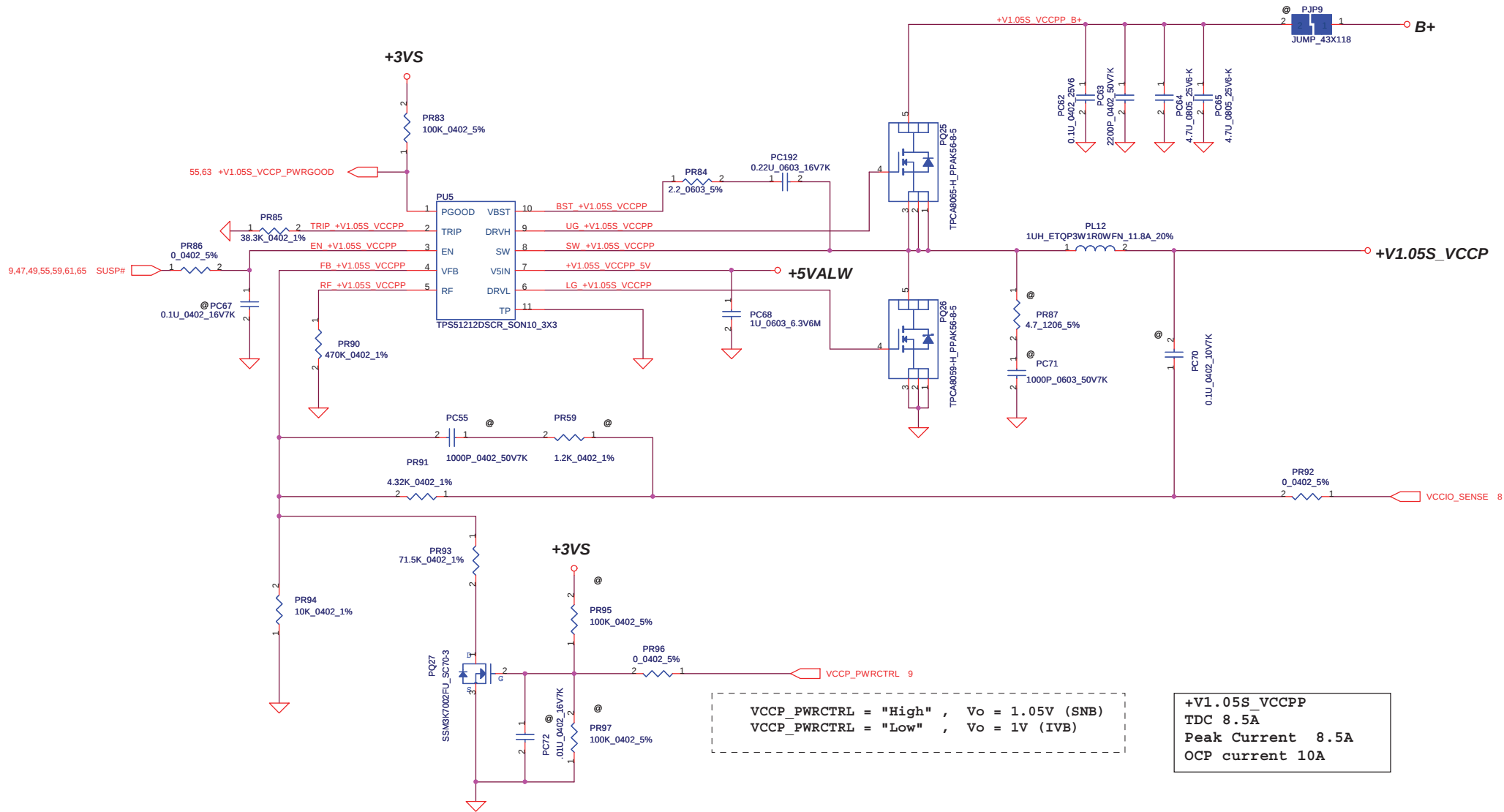
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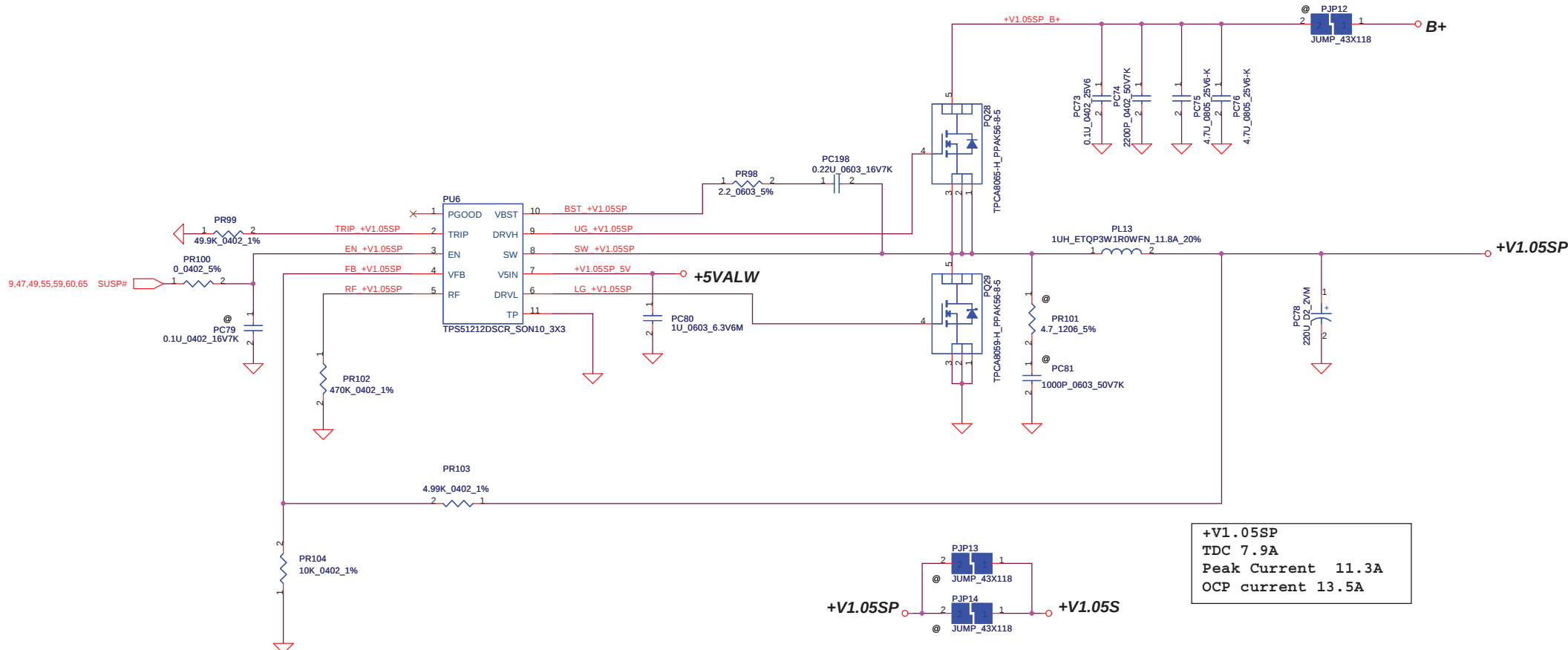


For KB930 --> Keep PD8, PR53, PR52, Remove PR76
For KB9012 (Red square) --> Remove PD8, PR53, PR52
Keep PR76

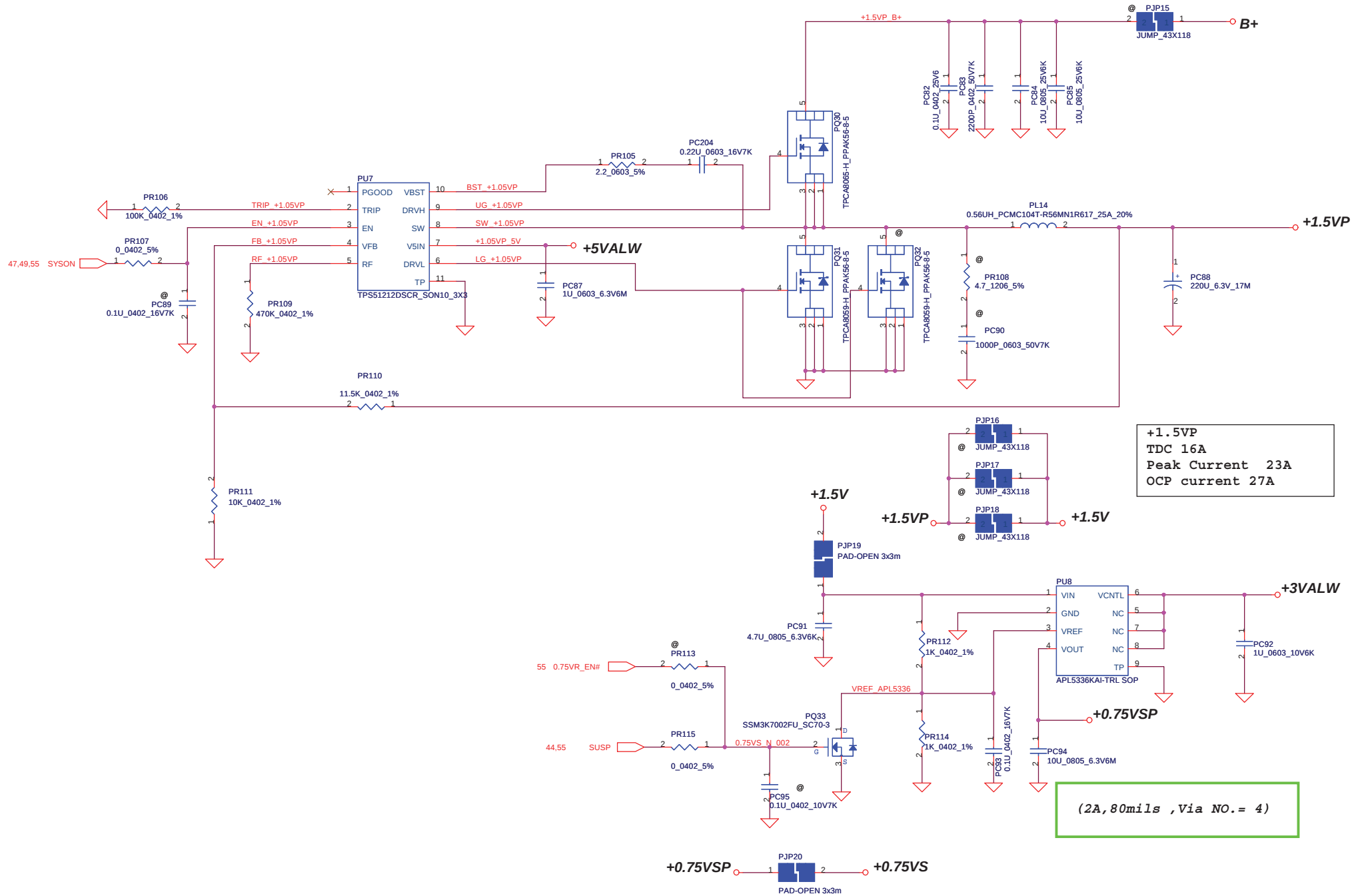
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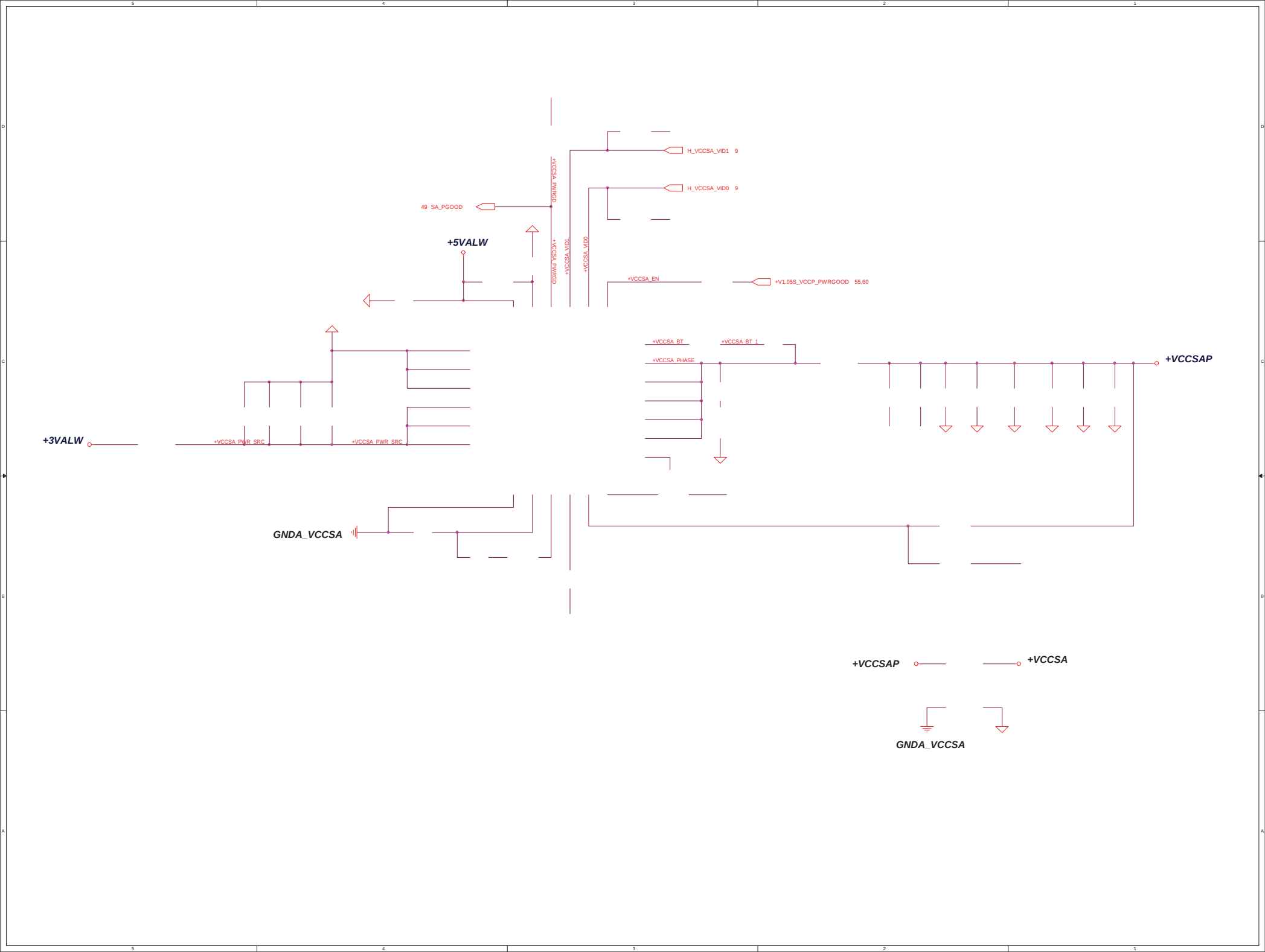
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Size	Custom	Document Number	PBL22 LA-7391P M/B		Rev
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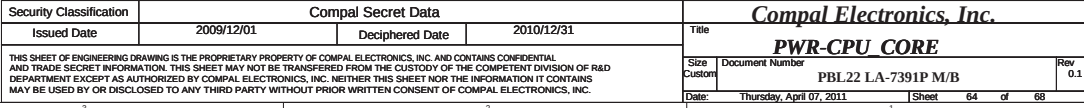


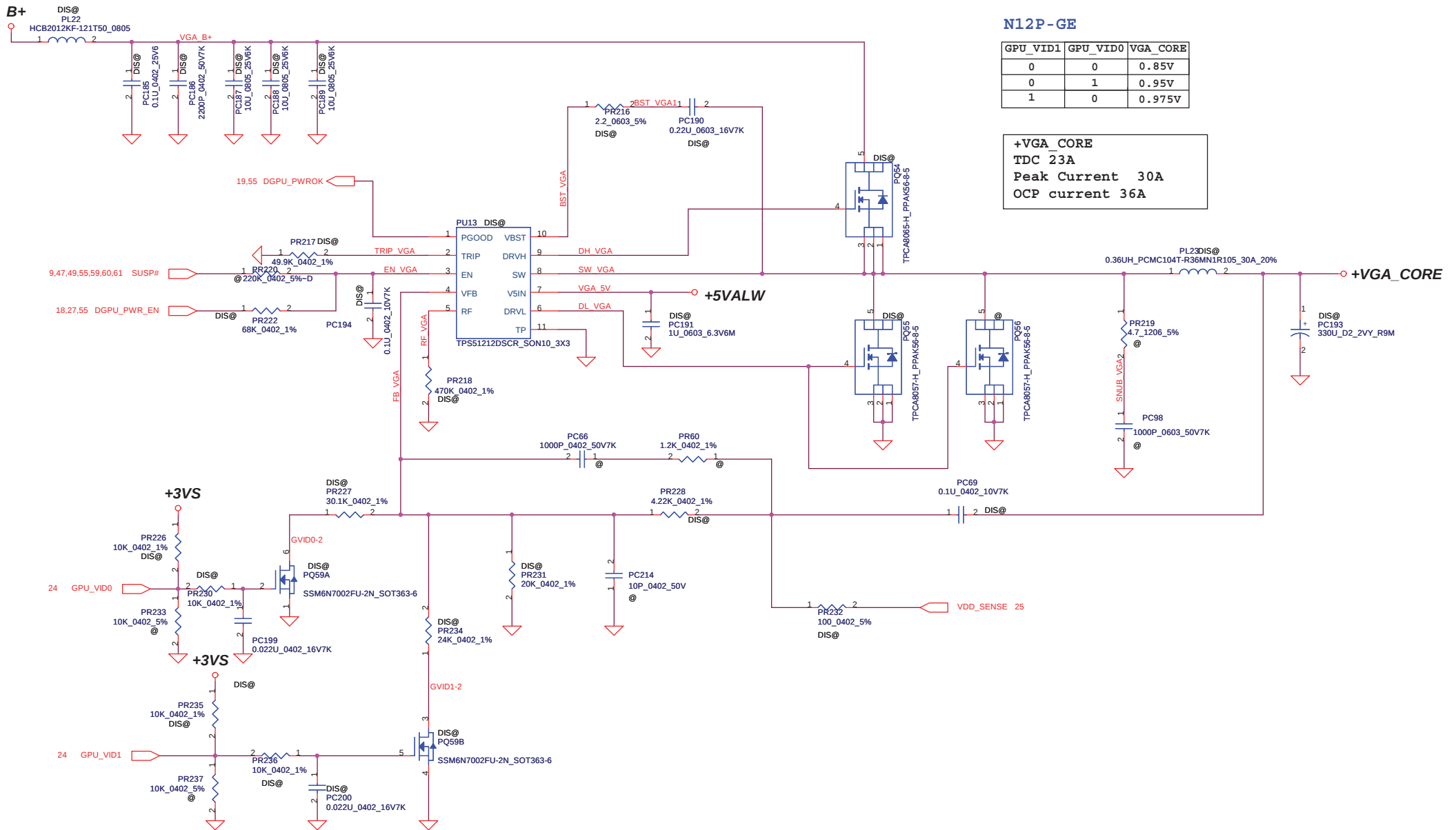
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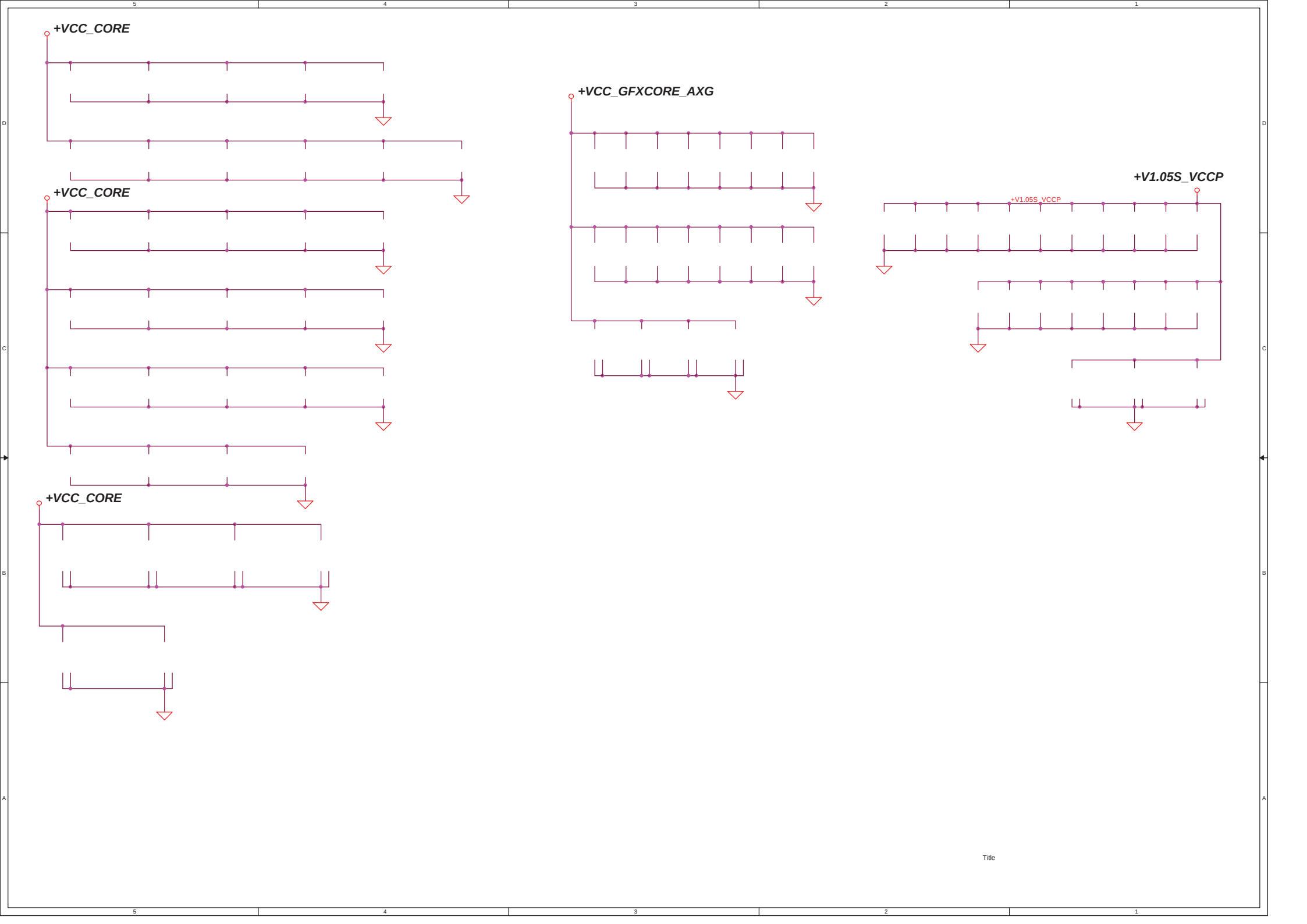


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Size	Custom	Document Number	PBL22 LA-7391P M/B	Rev	0.1
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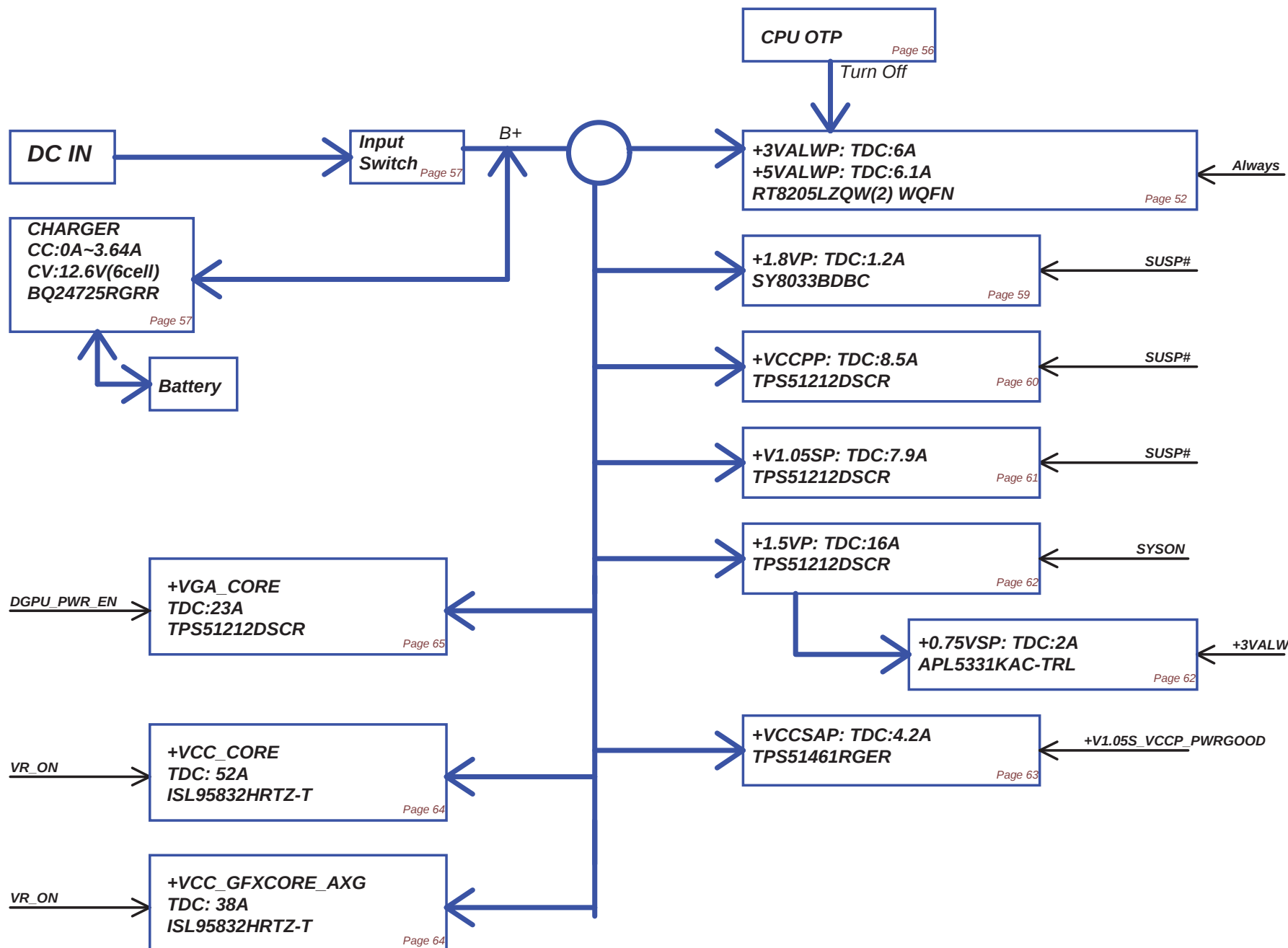








Power block



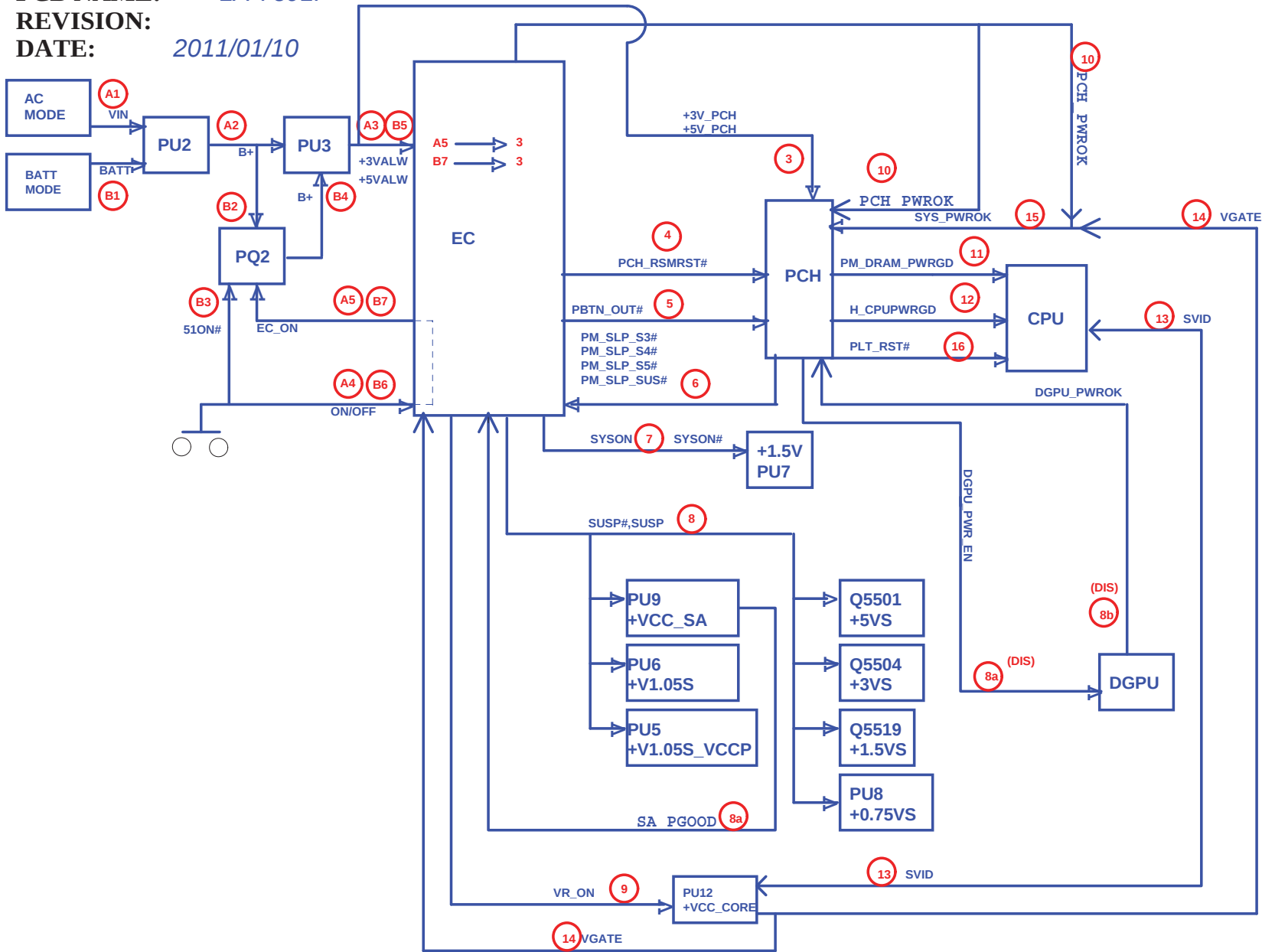
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Issued Date	2010/08/03	Deciphered Date	2011/08/03	Title	POWER BLOCK DIAGRAM
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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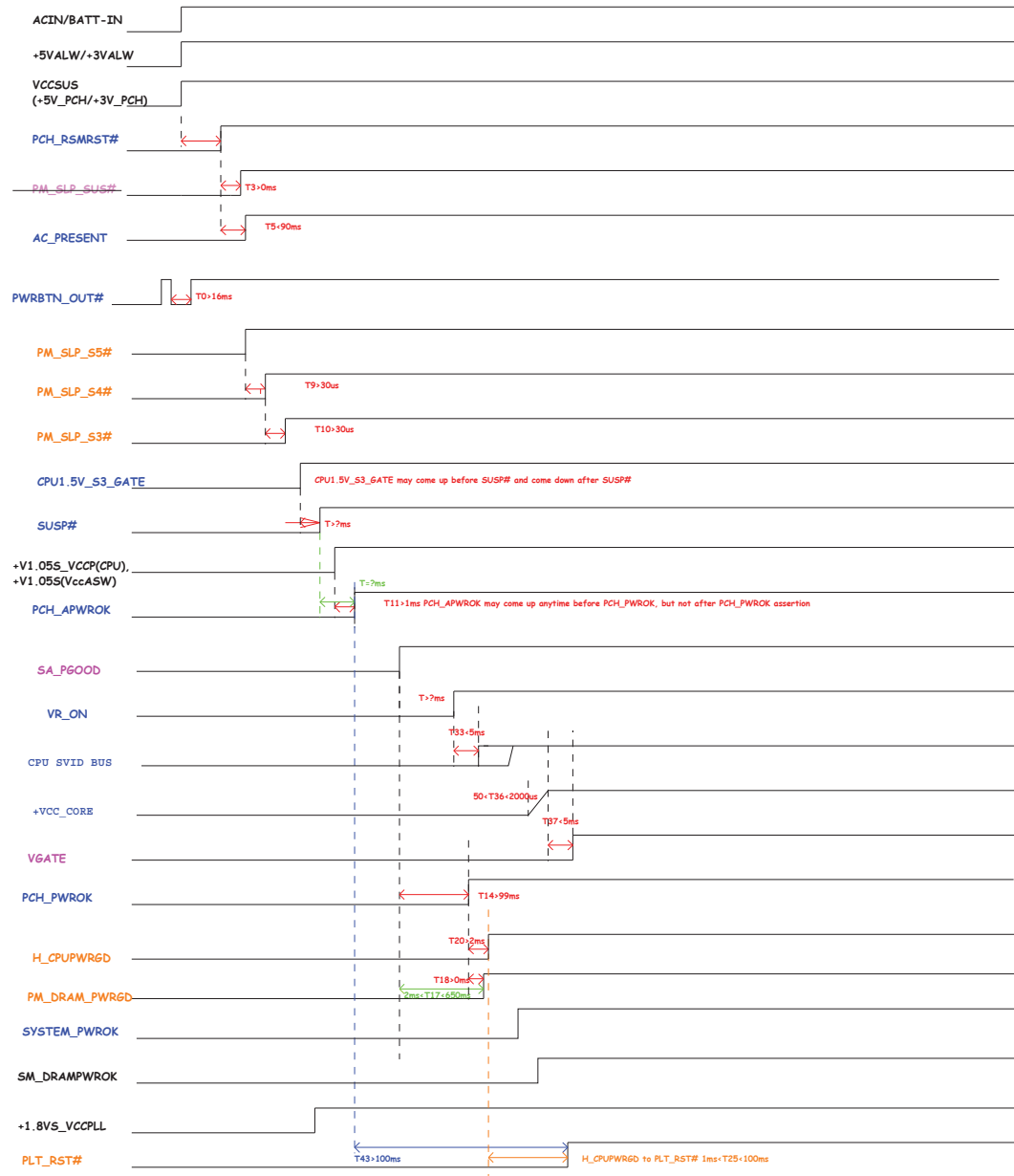
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MODEL NAME: Power Sequence Block Diagram
PCB NAME: LA-7391P
REVISION:
DATE: 2011/01/10



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Timing Diagram for G3 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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