ZZZ

PCB

Part Number = DAZ0J200100

Compal Confidential

K73 Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M1 + GPU Seymour XT-M2

2010-02-22

REV:0.22

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: P01-Cover Page		
Size: B	Document Number: LA7323P	Rev: 0.22
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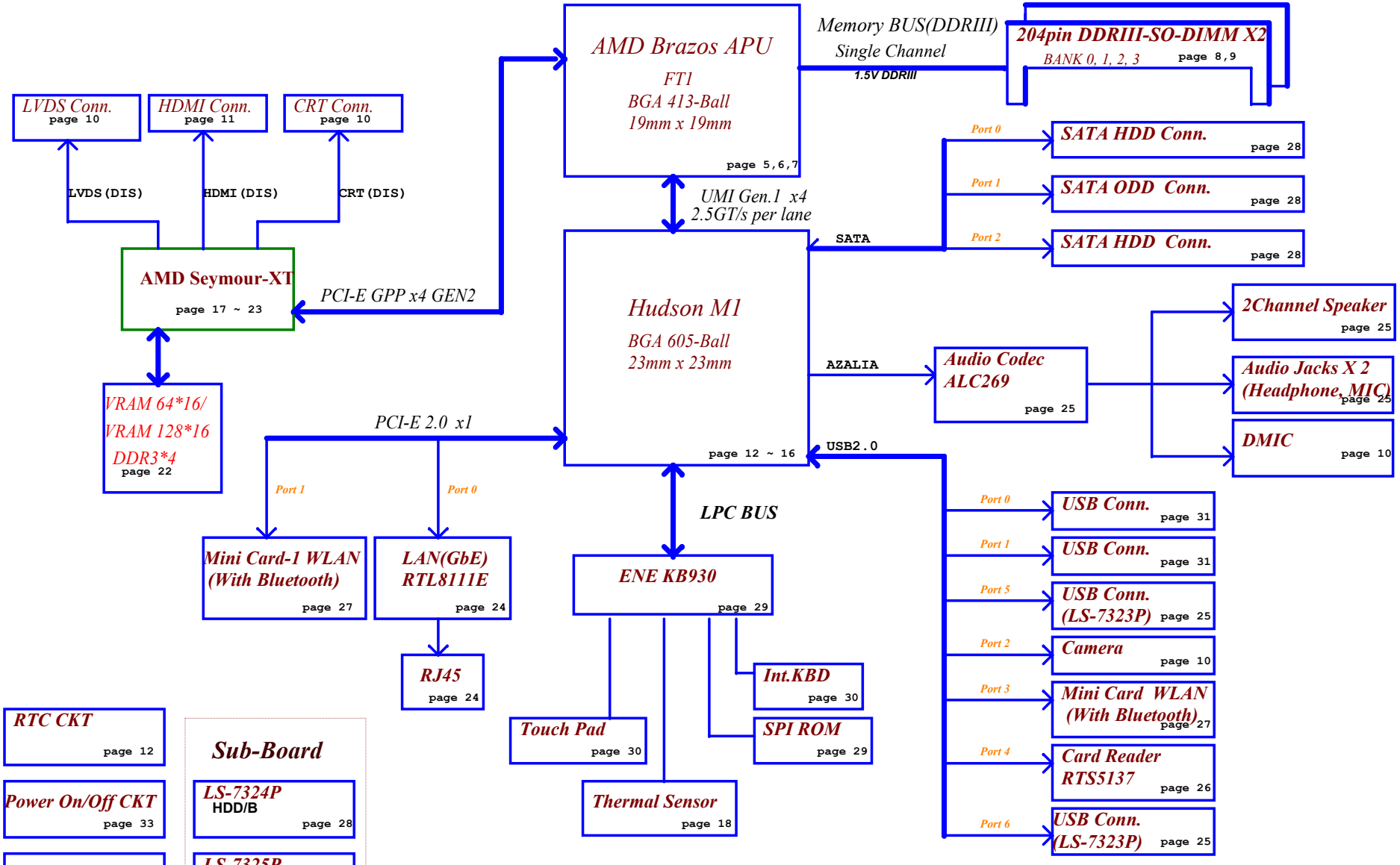

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Compal Electronics, Inc.			
Title	P02-Block Diagrams		
Size B	Document Number LA7323P		Rev 0.22
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SMBUS Control Table

	SOURCE	MIINI1	BATT	APU	FCH	SODIMM	VRAM
EC_SMB_CK1 EC_SMB_DA1	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	V	V	X	V
FCH_SMCLK0 FCH_SMDAT0	PCH	V	X	X	X	V	X
FCH_SMCLK3 FCH_SMDAT3	PCH	X	X	V	X	X	X

SCL0, SDA0 (Primary SMBUS in the S0 domain)
SCL1, SDA1 (Secondary SMBUS supporting ASF)
SCL2, SDA2 (Primary SMBUS in the S5 domain)
SCL3, SDA3 (Primary low-voltage SBMBUS for Processor TSI)
SCL4, SDA4 (Primary SMBUS in the S5 domain)

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	JUSB1
Port1	JUSB2
Port2	Camera
Port3	JMINI(WLAN)
Port4	Card Reader
Port5	JUSB3
Port6	NC
Port7	NC
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

15@ : E240 1.5GHz
16@ :E350 1.6GHz
X76@ : VRAM second source
LS@ : Level Shift
NLS@ :non Level Shift
USB30@ :USB3.0

Symbol Note :

: means Digital Ground

: means Analog Ground

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Power-Up/Down Sequence

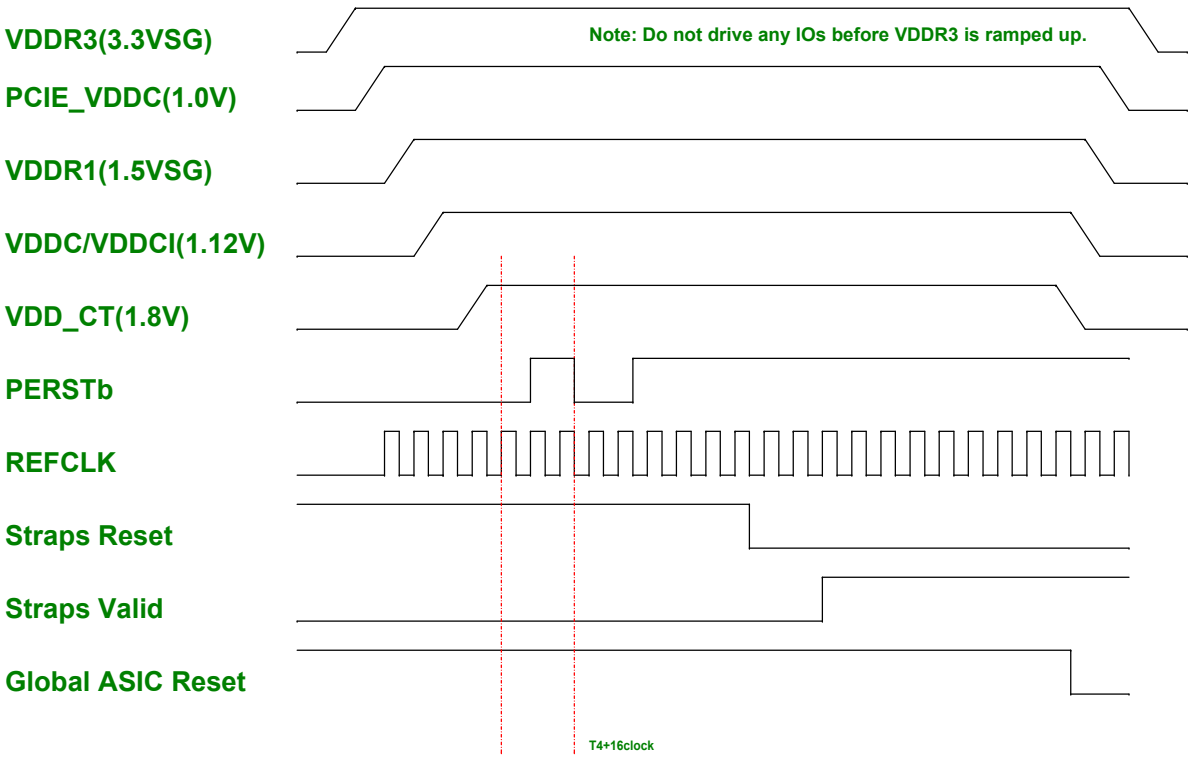
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



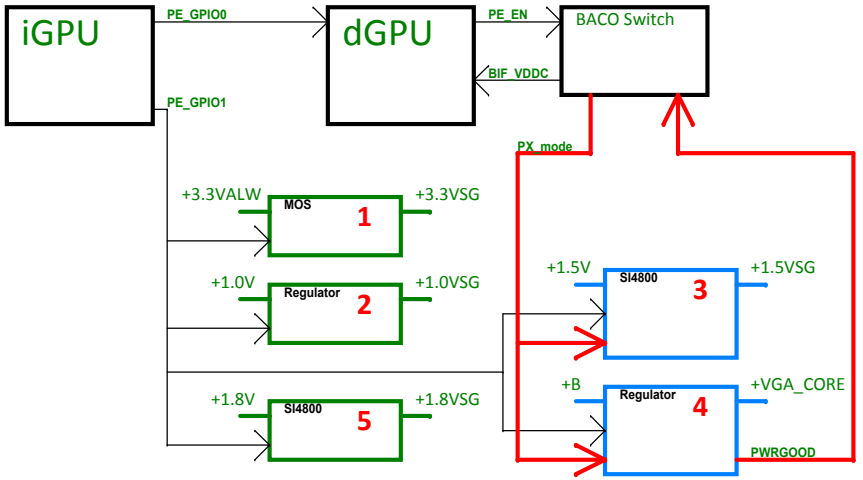
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Compal Electronics, Inc.

Title: P04-dGPU Block Diagram

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U22

ZACATE ZM161032B2238 1.6G BGA 413P

Part Number = SA00004KG70

16@

U22

ONTARIO CMC50AFPB22GT 1G BGA

Part Number = SA00004KD70

C50@

+1.8VS

R399 1 2 1K_0402_5% APU_SVC

R400 1 2 1K_0402_5% APU_SVD

R142 2 1 300_0402_5% APU_RST#

R401 2 1 300_0402_5% APU_PWRGD

R402 1 2 510_0402_1% TEST_25_L

R141 1 2 1K_0402_5% TEST36

C237 1 2 0.01U_0402_25V7K @ APU_RST#

C238 1 2 0.01U_0402_25V7K @ APU_PWRGD

+3VS

R410 1 2 1K_0402_5% APU_PROCHOT#

R411 1 2 1K_0402_5% APU_ALERT#_R

R143 1 2 1K_0402_5% APU_SIC

R414 1 2 1K_0402_5% APU_SID

U22B

DISPLAYPORT 1

A8 TDP1_TXP0

B8 TDP1_TXN0

B9 TDP1_TXP1

A9 TDP1_TXN1

D10 TDP1_TXP2

C10 TDP1_TXN2

A10 TDP1_TXP3

B10 TDP1_TXN3

DISPLAYPORT 0

B5 LTDP0_TXP0

A5 LTDP0_TXN0

D6 LTDP0_TXP1

C6 LTDP0_TXN1

A6 LTDP0_TXP2

B6 LTDP0_TXN2

D8 LTDP0_TXP3

C8 LTDP0_TXN3

CLK

12 APU_CLKP → V2 CLKIN_H

12 APU_CLKN → V1 CLKIN_L

12 APU_DISP_CLKP → D2 DISP_CLKIN_H

12 APU_DISP_CLKN → D1 DISP_CLKIN_L

SER

43 APU_SVC → J1 SVC

43 APU_SVD → J2 SVD

APU_SIC → P3 SIC

APU_SID → P4 SID

CTRL

12 APU_RST# → T3 RESET_L

12 APU_PWRGD → T4 PWROK

29 EC_THERM# → R169 2 0_0402_5%

12 FCH_PROCHOT# → R168 1 @ 2 0_0402_5%

APU_PROCHOT# U1 PROCHOT_L

APU_THERMTRIP# U2 THERMTRIP_L

APU_ALERT#_R T2 ALERT_L

JTAG

APU_TDI N2 TDI

APU_TDO N1 TDO

APU_TCK P1 TCK

APU_TMS P2 TMS

APU_TRST# M4 TRST_L

APU_DBRDY M3 DBRDY

APU_DBREQ# M1 DBREQ_L

T93PAD

T94PAD

Close to APU

43 APU_VDDNB_RUN_FB_H → F4 VDDCR_NB_SENSE

43 APU_VDD0_RUN_FB_H → G1 VDDCR_CPU_SENSE

T77PAD → F3 VDDIO_MEM_S_SENSE

43 APU_VDD0_RUN_FB_L → F1 VSS_SENSE

B4 RSVD_1

W11 RSVD_2

V5 RSVD_3

ZACATE ZM151032B1238 1.5G BGA 413P

15@

DP MISC

H3 DP_ZVSS → R398 1 2 150_0402_1%

G2 DP_BLON

H2 DP_DIGON

H1 DP_VARY_BL

B2 TDP1_AUXP

C2 TDP1_AUXN

C1 TDP1_HPD

A3 LTDP0_AUXP

B3 LTDP0_AUXN

D3 LTDP0_HPD → R406 1 2 100K_0402_5%

VGA DAC

C12 DAC_RED

D13 DAC_REDB

A12 DAC_GREEN

B12 DAC_GREENB

A13 DAC_BLUE

B13 DAC_BLUEB

E1 DAC_HSYNC

E2 DAC_VSYNC

F2 DAC_SCL

D4 DAC_SDA

D12 DAC_ZVSS → R144 1 2 499_0402_1%

TEST

R1 TEST4 → PAD T66

R2 TEST5 → PAD T67

R6 TEST6

T5 TEST14 → PAD T68

E4 TEST15 → R415 1 @ 2 1K_0402_5%

K4 TEST16

L1 TEST17

L2 TEST18 → R416 1 2 1K_0402_5%

M2 TEST19 → R417 1 2 1K_0402_5%

K1 TEST25_H → R418 1 2 510_0402_1%

K2 TEST_25_L

L5 TEST25_L

M5 TEST28_H

M21 TEST28_L

J18 TEST31 → PAD T73

J19 TEST33_H → C516 1 2 0.1U_0402_16V4Z → R420 1 2 51_0402_1%

U15 TEST33_L → C517 1 2 0.1U_0402_16V4Z → R421 1 2 51_0402_1%

T15 TEST33_H

H4 TEST34_L

N5 TEST35 → R422 1 @ 2 1K_0402_5%

R5 TEST36

TEST37 → PAD T76 → R958 1 2 1K_0402_5% +1.8VS

Delete Test point for layout limitation 20100917

K3 TEST38

T1 DMAACTIVE_L → ALLOW_STOP# 12

R423 1 2 1K_0402_5% +1.8VS

C639 1 @ 2 0.1U_0402_16V4Z

+3VS

R424 10K_0402_5% @

R425 1K_0402_5%

Q79 MMBT3904_NL_SOT23-3

APU_THERMTRIP# → H_THERMTRIP# 13

R427 0_0402_5%

If FCH internal pull-up disabled, level-shifter could be deleted.

Need BIOS to disable internal pull-up!!

CPU TSI interface level shift

BSH111, the Vgs is:
min = 0.4V
Typ = 1.0V
Max = 1.3V

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

1.607V for Gate

If use level shift, EC_SMB need pull up (pop R747 & R748)

+3VS

C236 1 @ 2 0.1U_0402_10V7K

R428 @ 31.6K_0402_1%

R160 @ 30K_0402_1%

APU_SID → Q22 BSH111 1N_SOT23-3

R429 1 @ 2 0_0402_5% FCH_SID → FCH_SID 13 T0 FCH

R430 1 2 0_0402_5% EC_SMB_DA2 → EC_SMB_DA2 18,29 TO EC

R431 0_0402_5%

APU_SIC → Q23 BSH111 1N_SOT23-3

R432 1 @ 2 0_0402_5% FCH_SIC → FCH_SIC 13 T0 FCH

R433 1 2 0_0402_5% EC_SMB_CK2 → EC_SMB_CK2 18,29 TO EC

R434 0_0402_5%

AMD Debug

+1.8VS

R842 1K_0402_5%

APU_TRST# → R846 1 2 APU_TRST#_R 0_0402_5%

R847 10K_0402_5%

R176 10K_0402_5%

R177 10K_0402_5%

JHDT1 SAMTE_ASP-136446-07-B CONN@

APU_TCK R843 1K_0402_5%

APU_TMS R840 1K_0402_5%

APU_TDI R798 1K_0402_5%

APU_TDO

APU_PWRGD

APU_RST#

APU_DBRDY

APU_DBREQ# R178 300_0402_5%

J108_PLLTST0 R799 0_0402_5% TEST19

J108_PLLTST1 R863 0_0402_5% TEST18

Please be noted about TEST_18 and TEST_19

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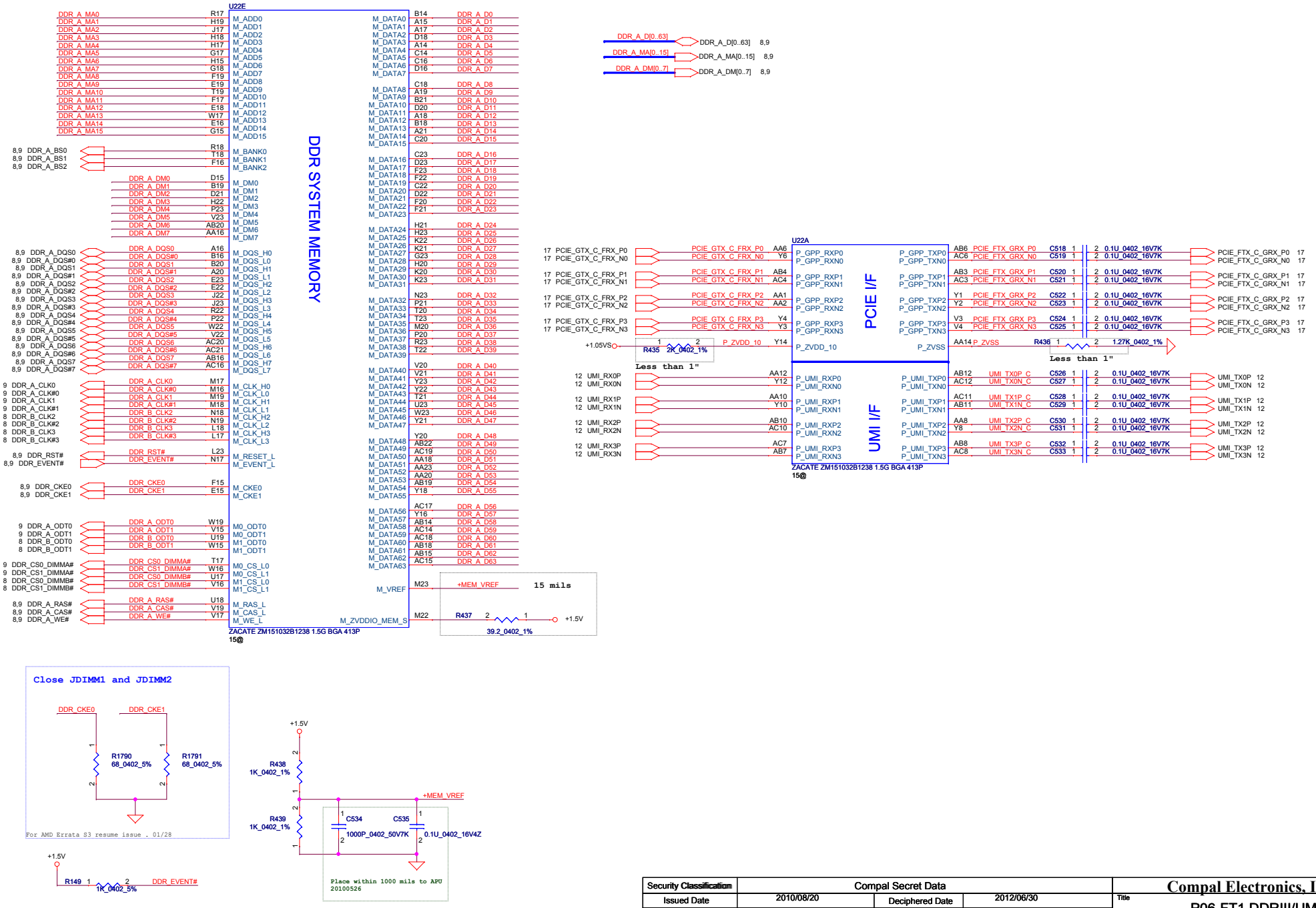
Title: P05-FT1 CTRL/DP/CRT

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 Sheet 5 of 47



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Title: P06-FT1 DDRIII/UMI/PCIE

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Custom	LA7323P	0.22

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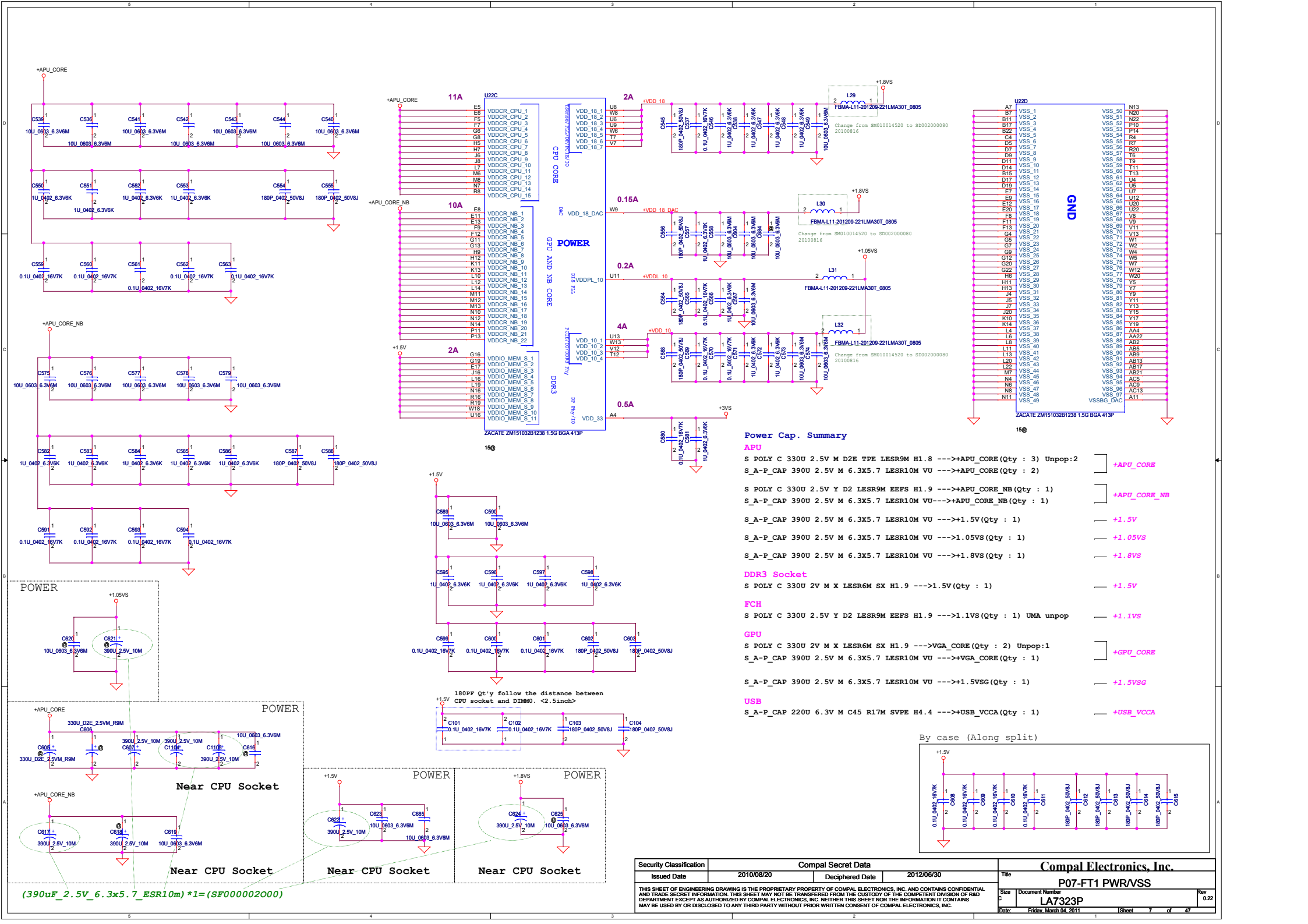

Power Cap. Summary

APU

S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 --->+APU_CORE(Qty : 3) Unpop:2
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+APU_CORE(Qty : 2) — *+APU_CORE*

S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->+APU_CORE_NB(Qty : 1)
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU--->+APU_CORE_NB(Qty : 1) — *+APU_CORE_NB*

S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.5V(Qty : 1) — *+1.5V*

S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->1.05VS(Qty : 1) — *+1.05VS*

S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.8VS(Qty : 1) — *+1.8VS*

DDR3 Socket

S POLY C 330U 2V M X LESR6M SX H1.9 --->1.5V(Qty : 1) — *+1.5V*

FCH

S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 --->1.1VS(Qty : 1) UMA unpop — *+1.1VS*

GPU

S POLY C 330U 2V M X LESR6M SX H1.9 --->VGA_CORE(Qty : 2) Unpop:1
S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+VGA_CORE(Qty : 1) — *+GPU_CORE*

S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU --->+1.5VSG(Qty : 1) — *+1.5VSG*

USB

S_A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 --->+USB_VCCA(Qty : 1) — *+USB_VCCA*

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Issued Date	2010/08/20	Deciphered Date	2012/06/30

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Title: P07-FT1 PWR/VSS

Size	Document Number	Rev
C	LA7323P	0.22

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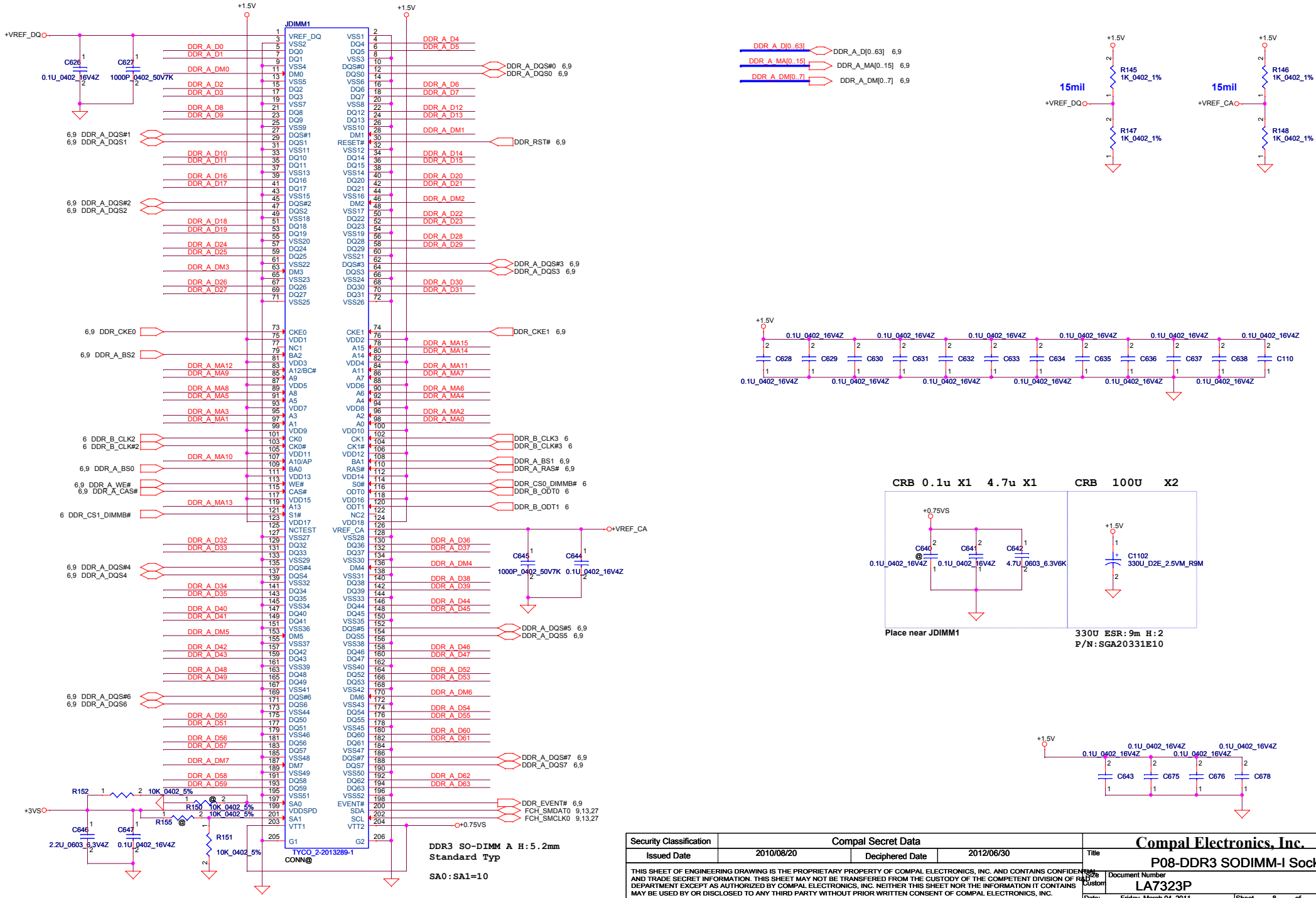


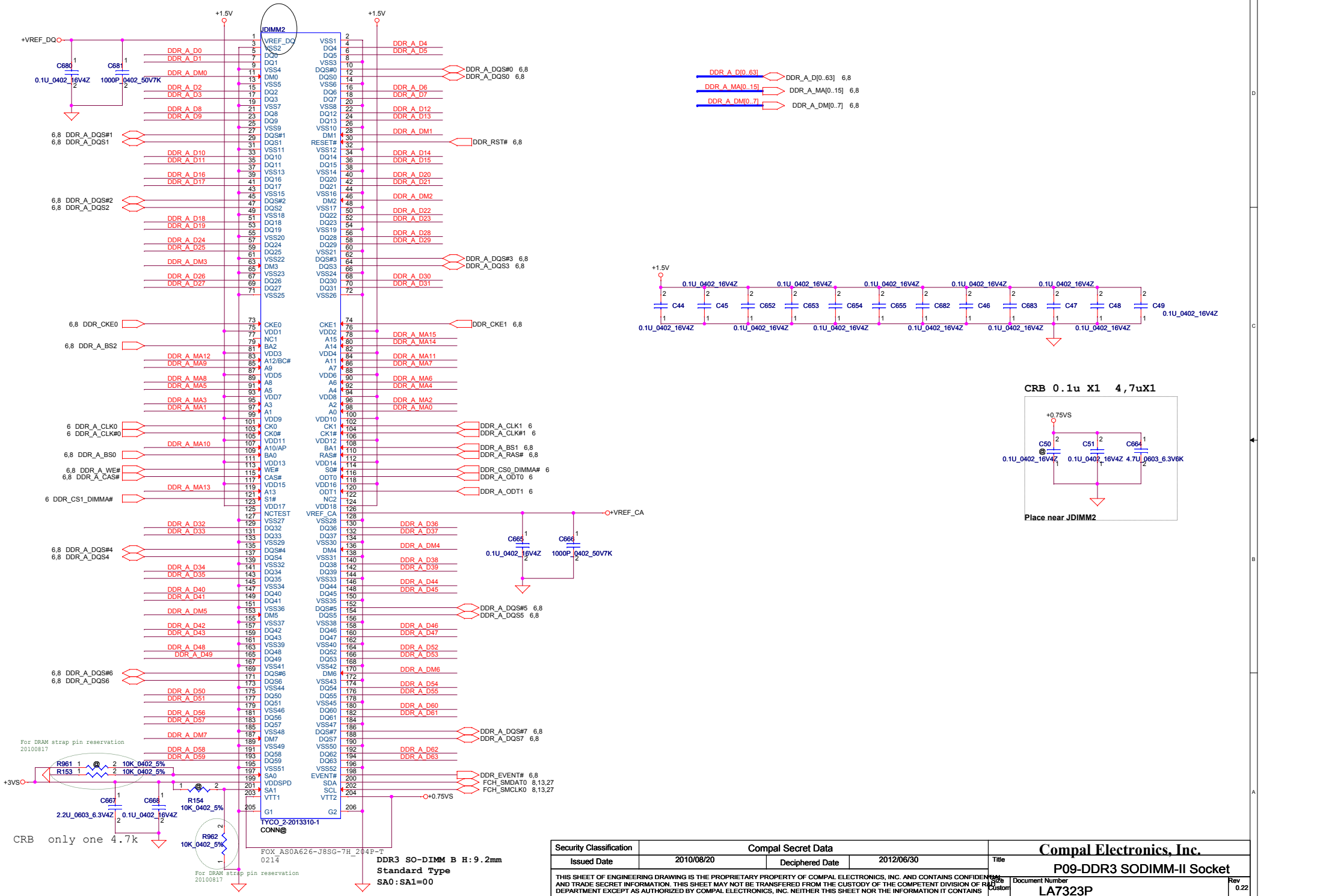
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P08-DDR3 SODIMM-I Socket

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 Sheet 8 of 47



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Compal Electronics, Inc.

Title: P09-DDR3 SODIMM-II Socket

Size	Document Number	Rev
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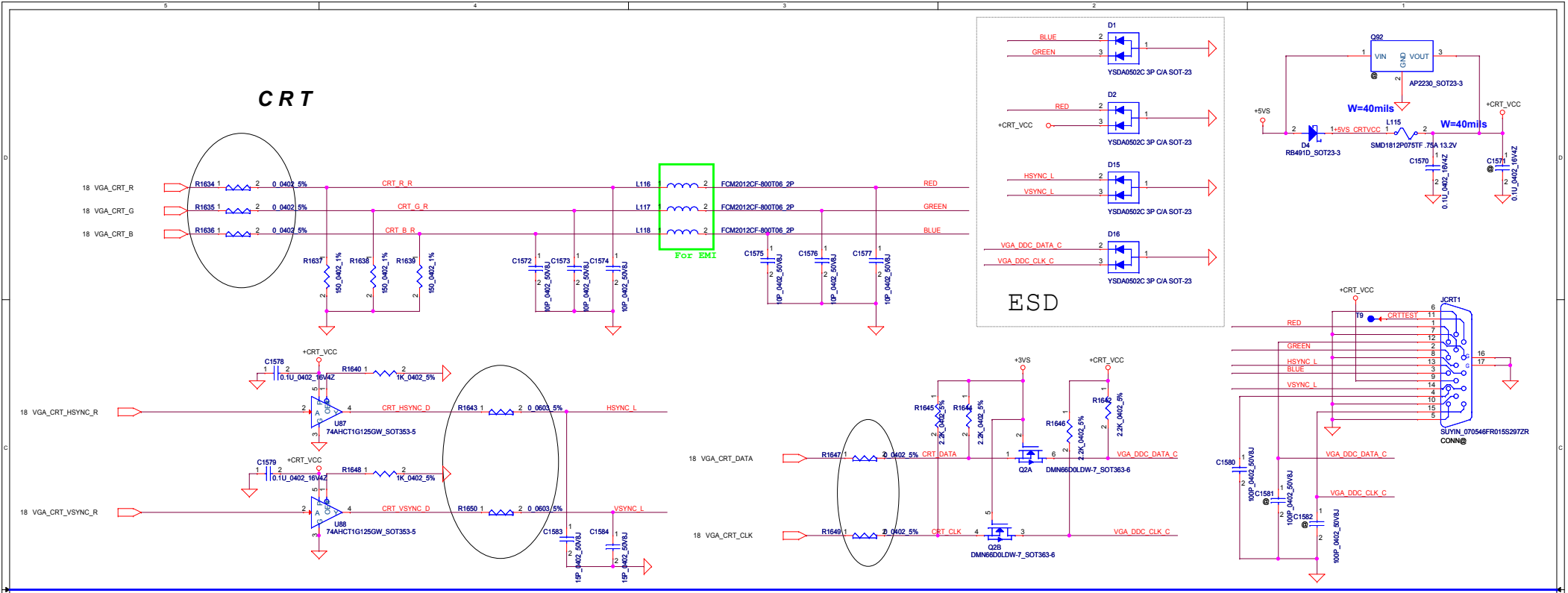
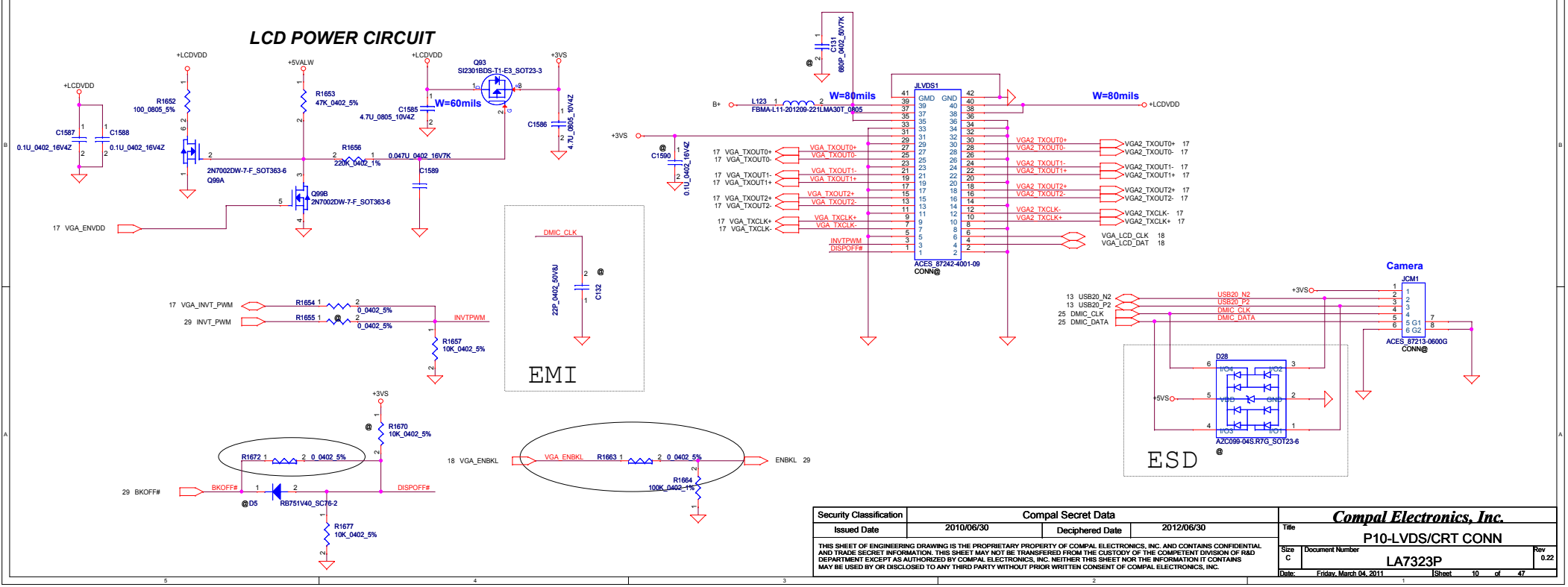


LCD POWER CIRCUIT



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Compal Electronics, Inc.

Title: P10-LVDS/CRT CONN

Size	Document Number	Rev
C	LA7323P	0.22

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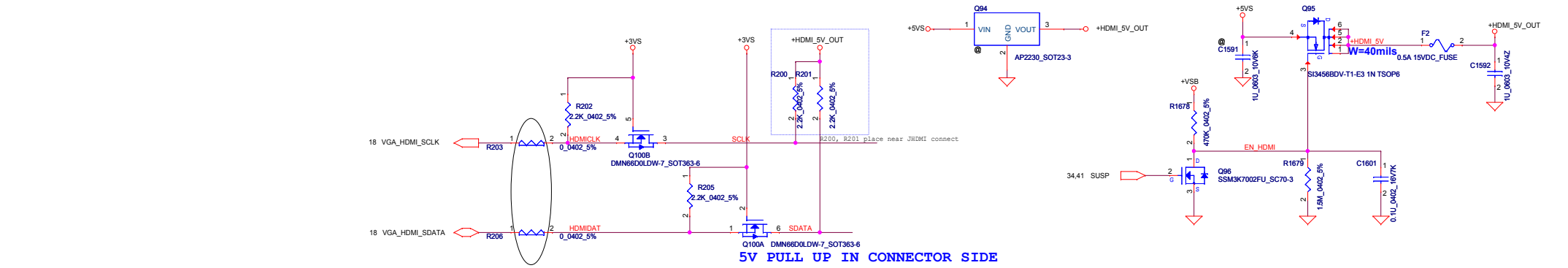

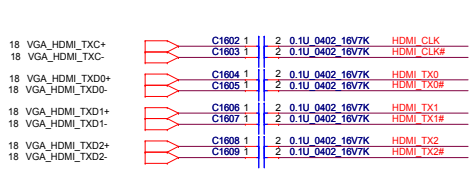

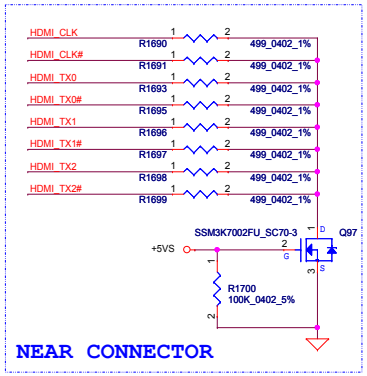

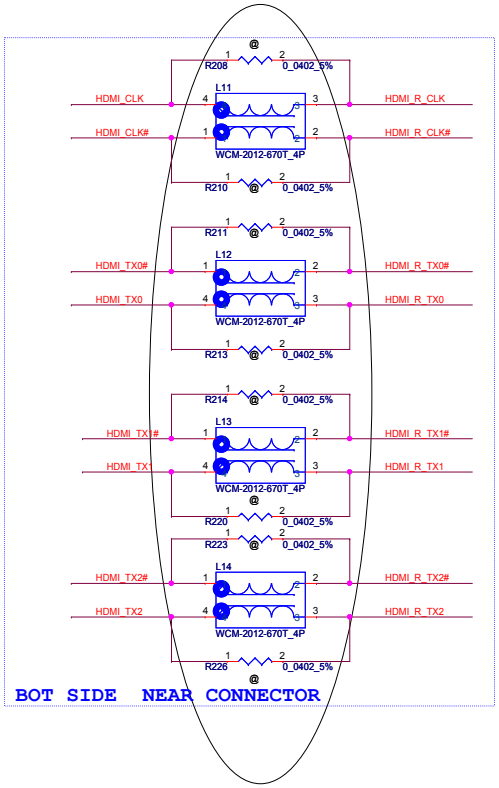

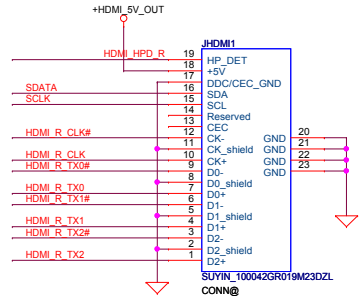

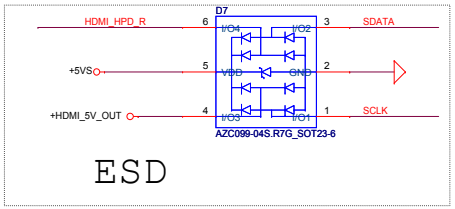

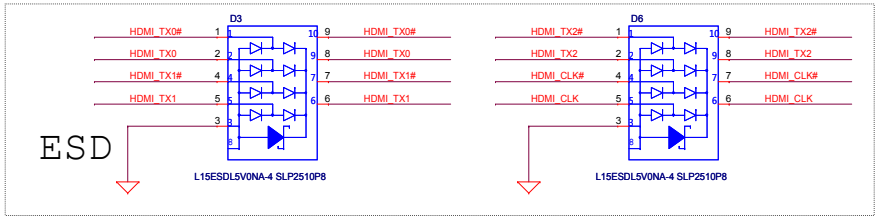

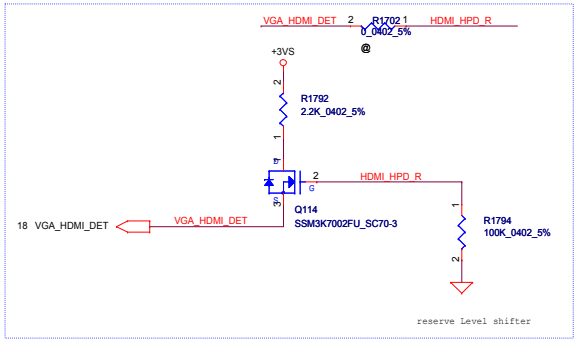

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Compal Electronics, Inc.	
Title	P11-HDMI CONN
Size: Custom	Document Number: LA7323P
Rev	0.22
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For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

U31E

PCIE_RST# P1 / A_RST# L1

29 A_RST#

PCI EXPRESS I/F

6 UMI_RX0P	C53	0.1U_0402_16V7K	UMI_RX0P_C	AD26
6 UMI_RX0N	C54	0.1U_0402_16V7K	UMI_RX0N_C	AD27
6 UMI_RX1P	C55	0.1U_0402_16V7K	UMI_RX1P_C	AC28
6 UMI_RX1N	C56	0.1U_0402_16V7K	UMI_RX1N_C	AC29
6 UMI_RX2P	C57	0.1U_0402_16V7K	UMI_RX2P_C	AB29
6 UMI_RX2N	C58	0.1U_0402_16V7K	UMI_RX2N_C	AB28
6 UMI_RX3P	C59	0.1U_0402_16V7K	UMI_RX3P_C	AB26
6 UMI_RX3N	C60	0.1U_0402_16V7K	UMI_RX3N_C	AB27

UMI_TX0P AE24, UMI_TX0N AE23, UMI_TX1P AD25, UMI_TX1N AD24, UMI_TX2P AC24, UMI_TX2N AC25, UMI_TX3P AB25, UMI_TX3N AB24

UMI_RX0P, UMI_RX0N, UMI_RX1P, UMI_RX1N, UMI_RX2P, UMI_RX2N, UMI_RX3P, UMI_RX3N

R560 2 / R561 2 — 590_0402_1% / 2K_0402_1% — +PCIE_VDDAN — AD29, AD28

PCIE_CALRP, PCIE_CALRN

LAN / WLAN / USB3.0

24 PCIE_FTX_C_DRX_P0	C61	0.1U_0402_16V7K	PCIE_FTX_DRX_P0	AA28
24 PCIE_FTX_C_DRX_N0	C62	0.1U_0402_16V7K	PCIE_FTX_DRX_N0	AA29
27 PCIE_FTX_C_DRX_P1	C717	0.1U_0402_16V7K	PCIE_FTX_DRX_P1	Y29
27 PCIE_FTX_C_DRX_N1	C63	0.1U_0402_16V7K	PCIE_FTX_DRX_N1	Y28
32 PCIE_PTX_C_USBRX_P2	C736	0.1U_0402_16V7K	PCIE_FTX_DRX_P2	Y26
32 PCIE_PTX_C_USBRX_N2	C122	0.1U_0402_16V7K	PCIE_FTX_DRX_N2	Y27

GPP_TX0P W28, GPP_TX0N W29, GPP_TX1P AA22, GPP_TX1N Y21, GPP_TX2P AA25, GPP_TX2N AA24, GPP_TX3P W23, GPP_TX3N V24

24 PCIE_FRX_DTX_P0, 24 PCIE_FRX_DTX_N0, 27 PCIE_FRX_DTX_P1, 27 PCIE_FRX_DTX_N1, 32 PCIE_PRX_C_USBTX_P2, 32 PCIE_PRX_C_USBTX_N2

GPP_RX0P W24, GPP_RX0N W25, GPP_RX1P V25, GPP_RX1N V26, GPP_RX2P T25, GPP_RX2N T26, GPP_RX3P R25, GPP_RX3N R26

CLOCK GENERATOR

close to FCH within 1"

PCIE_RCLKP/NB_LNK_CLKP M23, PCIE_RCLKN/NB_LNK_CLKN P23

5 APU_DISP_CLKP	R564	0_0402_5%	APU_DISP_CLKP_R	U29
5 APU_DISP_CLKN	R565	0_0402_5%	APU_DISP_CLKN_R	U28

NB_DISP_CLKP U29, NB_DISP_CLKN U28

NB_HT_CLKP T26, NB_HT_CLKN T27

5 APU_CLKP	R162	0_0402_5%	APU_CLKP_R	V21
5 APU_CLKN	R163	0_0402_5%	APU_CLKN_R	T21

CPU_HT_CLKP V21, CPU_HT_CLKN T21

17 CLK_PCIE_VGA	R569	0_0402_5%	CLK_PCIE_VGA_R	V23
17 CLK_PCIE_VGA#	R570	0_0402_5%	CLK_PCIE_VGA#_R	T23

SLT_GFX_CLKP V23, SLT_GFX_CLKN T23

LAN

24 CLK_PCIE_LAN	R571	0_0402_5%	CLK_PCIE_LAN_R	L29
24 CLK_PCIE_LAN#	R572	0_0402_5%	CLK_PCIE_LAN#_R	L28

GPP_CLK0P L29, GPP_CLK0N L28

WLAN

27 CLK_PCIE_MINI1	R573	0_0402_5%	CLK_PCIE_MINI1_R	N29
27 CLK_PCIE_MINI1#	R574	0_0402_5%	CLK_PCIE_MINI1#_R	N28

GPP_CLK1P N29, GPP_CLK1N N28

USB3.0

32 CLK_USB30	R595 USB30@	0_0402_5%	CLK_PCIE_USB30_R	M29
32 CLK_USB30#	R585 USB30@	0_0402_5%	CLK_PCIE_USB30#_R	M28

GPP_CLK2P M29, GPP_CLK2N M28

GPP_CLK3P T25, GPP_CLK3N V25

GPP_CLK4P L24, GPP_CLK4N L23

GPP_CLK5P P25, GPP_CLK5N M25

GPP_CLK6P P29, GPP_CLK6N P28

GPP_CLK7P N26, GPP_CLK7N N27

GPP_CLK8P T29, GPP_CLK8N T28

EMI

26 CLK_SD_48M — R170 22_0402_5% — 14M_25M_48M_OSC L25

C66 10P_0402_50V8J — Y3 — R576 1M_0603_5% — C67 12P_0402_50V8J

25MHZ 12PF 5XFA2500012CIF50Q3

25M_CLK_X1 L26 — 25M_X1

25M_CLK_X2 L27 — 25M_X2

21807-A11-HUDSON-M1_FCBGA605

PCI CLKS

PCICLK0 W2 — PAD T96 — PCI_CLK1 16, PCI_CLK2 16, PCI_CLK3 16, PCI_CLK4 16

PCICLK1/GPO36 W1, PCICLK2/GPO37 W3, PCICLK3/GPO38 W4, PCICLK4/14M_OSC/GPO39 Y1

PCIRST_L V2 — PAD T92

PCI I/F

AD0/GPIO0 AA1, AD1/GPIO1 AA4, AD2/GPIO2 AA3, AD3/GPIO3 AB1, AD4/GPIO4 AA5, AD5/GPIO5 AB2, AD6/GPIO6 AB6, AD7/GPIO7 AB5, AD8/GPIO8 AA6, AD9/GPIO9 AC2, AD10/GPIO10 AC3, AD11/GPIO11 AC4, AD12/GPIO12 AC1, AD13/GPIO13 AD1, AD14/GPIO14 AD2, AD15/GPIO15 AC6, AD16/GPIO16 AE2, AD17/GPIO17 AE1, AD18/GPIO18 AF8, AD19/GPIO19 AE3, AD20/GPIO20 AF1, AD21/GPIO21 AG1, AD22/GPIO22 AF2, AD23/GPIO23 AE9, AD24/GPIO24 AD9, AD25/GPIO25 AC11, AD26/GPIO26 AF6, AD27/GPIO27 AF4, AD28/GPIO28 AF3 — VGA_PWRGD_R, AD29/GPIO29 AH2, AD30/GPIO30 AG2, AD31/GPIO31 AH3

PCI_AD23 16, PCI_AD24 16, PCI_AD25 16, PCI_AD26 16, PCI_AD27 16

CBE0_L AA8, CBE1_L AD5, CBE2_L AD8, CBE3_L AA10, FRAME_L AE8, DEVSEL_L AB9, IRDY_L AJ3, TRDY_L AE7, PAR AC5, STOP_L AF5, PERR_L AE6, SERR_L AE4, REQ0_L AE11, REQ1_L/GPIO40 AH5, REQ2_L/CLK_REQ8_L/GPIO41 AH4, REQ3_L/CLK_REQ5_L/GPIO42 AC12

GNT0_L AD12 — PAD T95

GNT1_L/GPO44 AJ5, GNT2_L/GPO45 AH6, GNT3_L/CLK_REQ7_L/GPIO46 AB12

CLKRUN_L AB11 — PAD T97 — R99 1 — 10K_0402_5%

LOCK_L AD7

INTE_L/GPIO32 AJ6, INTF_L/GPIO33 AG6, INTG_L/GPIO34 AG4, INTH_L/GPIO35 AJ4

LPC

R854 0_0402_5% — LPC_CLK1 16
R853 0_0402_5% — LPC_CLK0 16
R575 22_0402_5% — LPC_CLK0_EC 29
R577 22_0402_5% — CLK_PCI_DB 27

LPCCLK0 H24, LPCCLK1 H25

LAD0 J27 — LPC_AD0 27,29
LAD1 J26 — LPC_AD1 27,29
LAD2 H29 — LPC_AD2 27,29
LAD3 H28 — LPC_AD3 27,29
LFRAME_L G28 — LPC_FRAME# 27,29
LDRQ0_L J25
LDRQ1_L/CLK_REQ6_L/GPIO49 AA18
SERIRQ/GPIO48 AB19 — SERIRQ 29

CPU

ALLOW_LDTSTP/DMA_ACTIVE_L G21 — ALLOW_STOP# 5
PROCHOT_L H21 — FCH_PROCHOT# 5
LDT_PG K19 — APU_PWRGD 5
LDT_STP_L G22
LDT_RST_L J24 — APU_RST# 5

RTC

32K_X1 C1 — RTC_32KHI
32K_X2 C2 — RTC_32KHO

RTCCLK D2 — RTC_CLK 16,29
INTRUDER_ALERT_L B2
VDDBT_RTC_G B1

R864 510_0402_5% W=20mils

C1272 0.1U_0402_16V4Z — C1271 1U_0402_6.3V4Z — for Clear CMOS — JOPEN1 @

C1270 0.1U_0402_16V4Z — +RTCVCC

D23 DAN202UT106_SC70-3 — +RTCBATT_R — +CHGRTC

+RTCBATT — R179 1K_0402_5%

+3VALW — C1234 0.1U_0402_16V4Z

A_RST# — R175 33_0402_5% — U28 NC7SZ08P5X_NL_SC70-5 — PLT_RST# 17,24,27,32

C1233 150P_0402_50V8J — R174 8.2K_0402_5%

R582 0_0402_5% — 2PCIE_RST#

Need to check material?

+1.8VS — +3VS — R164 10K_0402_5%

APU_PWRGD — Q90 FDV301N_NL_SOT23-3 — H_PWRGD_L 43

+3VALW — C1199 @ 0.1U_0402_16V4Z

41,42,44 VGA_PWRGD — U33 NC7SZ08P5X_NL_SC70-5 — VGA_PWRGD_R

R830 0_0402_5% — R838 100K_0402_5% — R839 0_0402_5%

RTC BATT Conn.

+RTCBATT — CONN@ — JRTC1 LOTES_AAA-BAT-054-K01

Close to FCH

C64 10P_0402_50V8J — RTC_32KHI — R563 20M_0603_5% — Y4 32.768KHZ_12.5PF_Q13MC1461000100_10PPM — RTC_32KHO — C65 10P_0402_50V8J

FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)

FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)

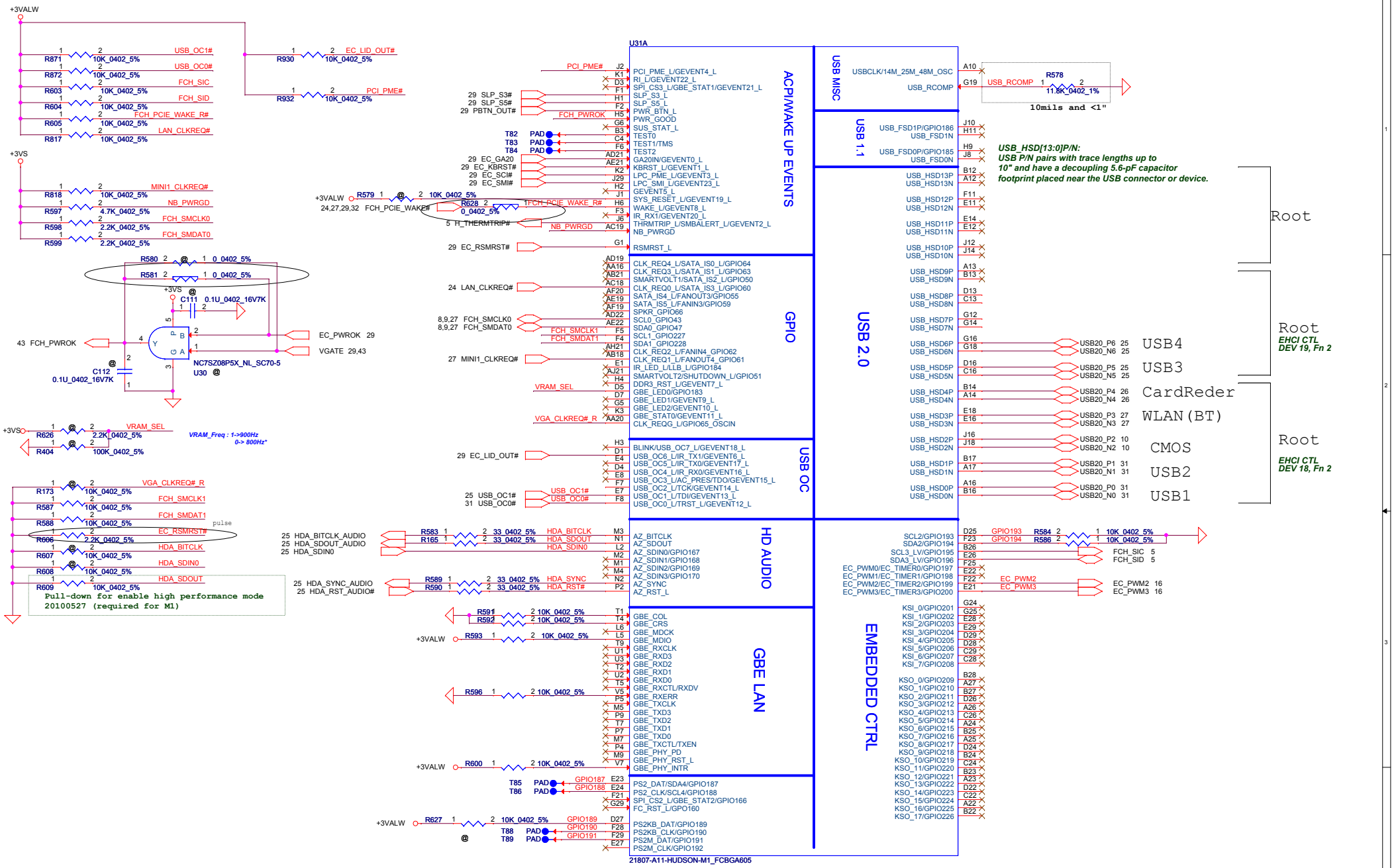
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P12-FCH PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: LA7323P | Rev: 0.22

Date: Friday, March 04, 2011 | Sheet 12 of 47



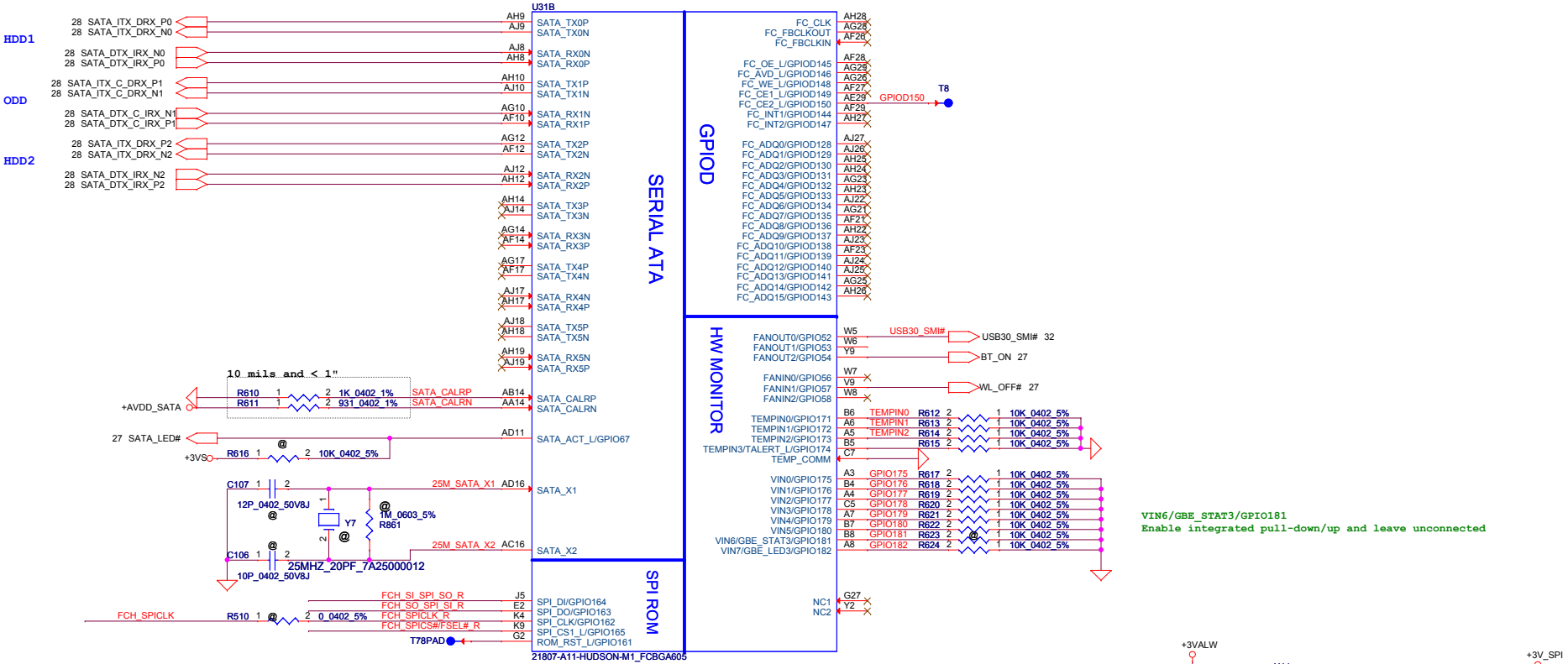
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

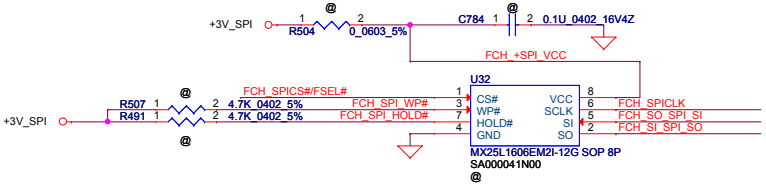
Compal Electronics, Inc.

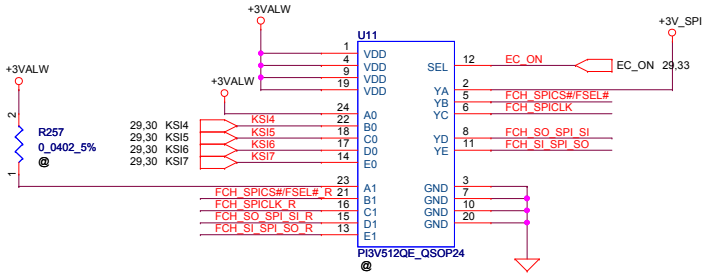
Title: P13-FCH HDA/USB/ACPI

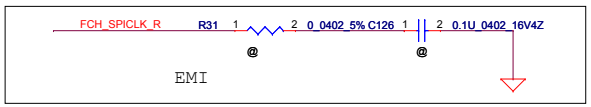
Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 Sheet 13 of 47









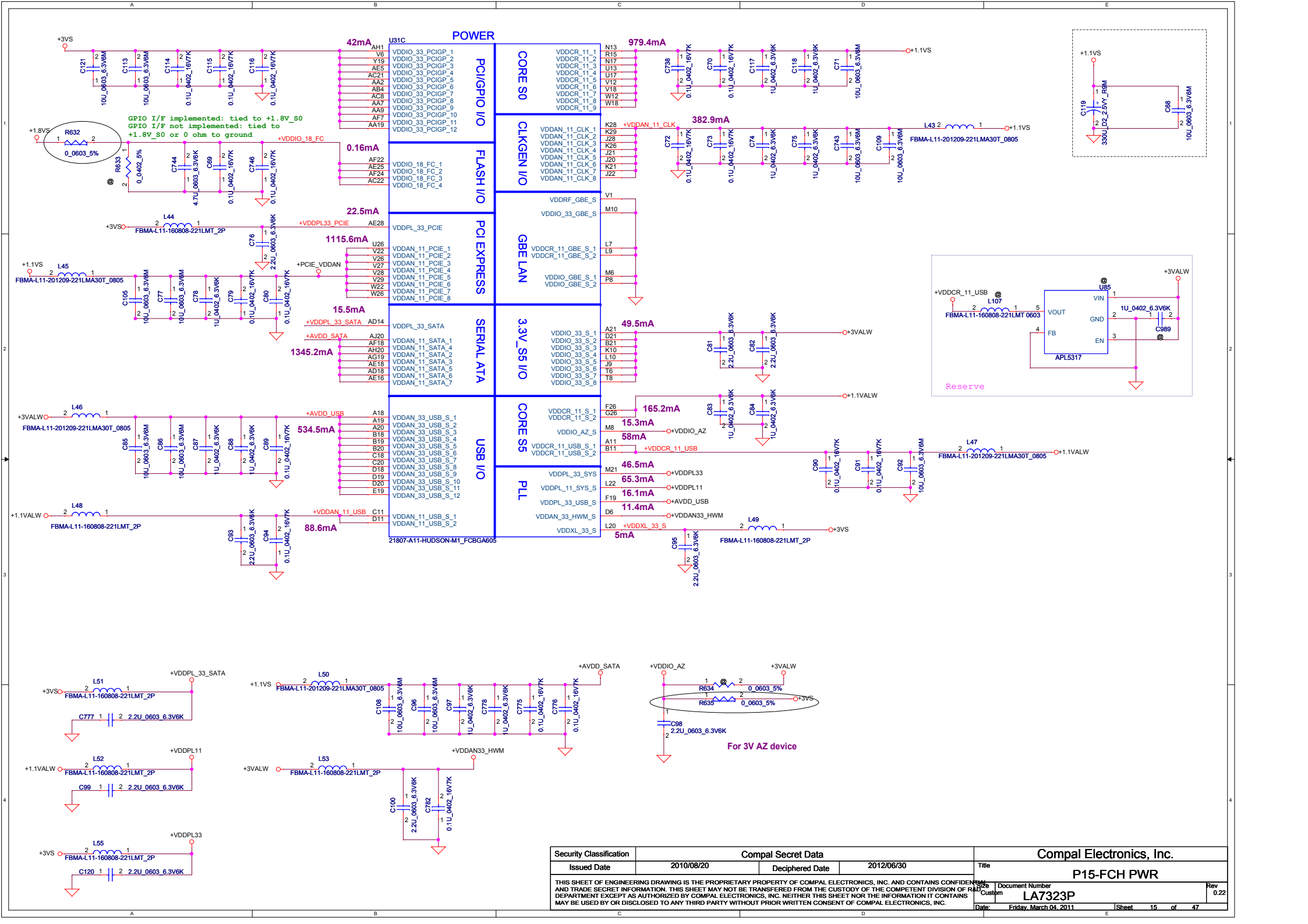
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P14-FCH-SATA/SPI

Size: Custom | Document Number: LA7323P | Rev: 0.22

Date: Friday, March 04, 2011 | Sheet 14 of 47



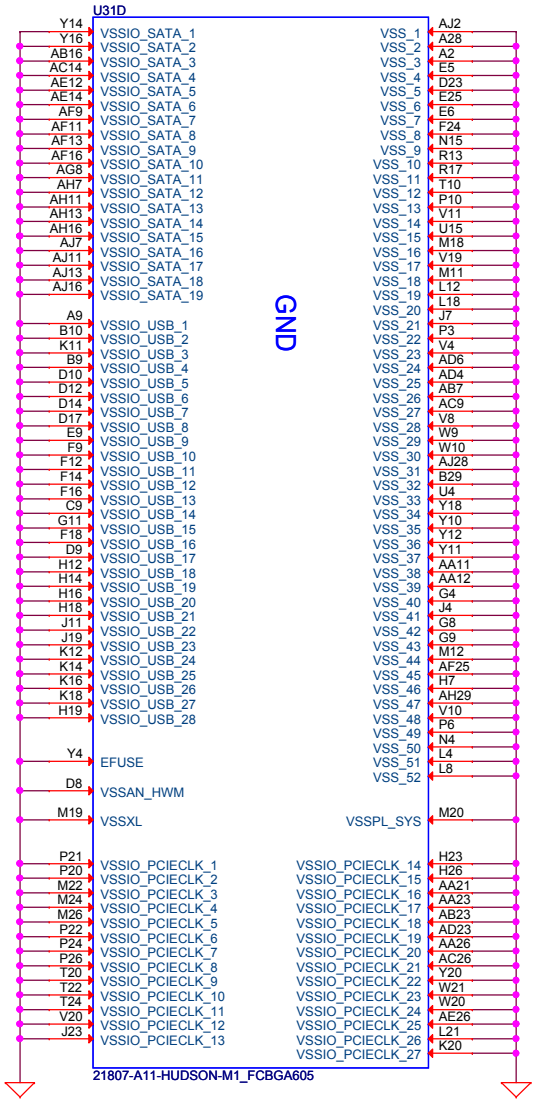
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P15-FCH PWR

Size: Custom | Document Number: LA7323P | Rev: 0.22

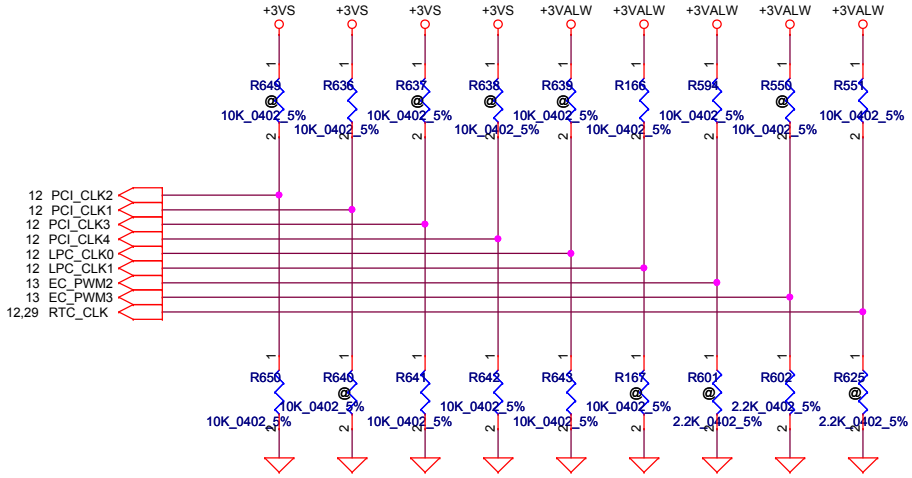
Date: Friday, March 04, 2011 | Sheet 15 of 47



REQUIRED STRAPS

Check Internal PU/PD

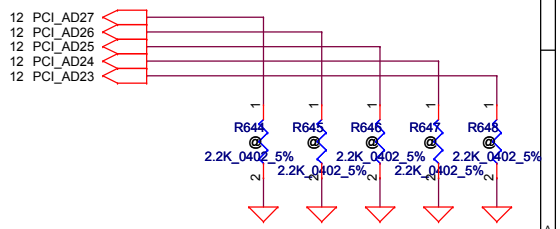
	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H.L) *
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)



DEBUG STRAPS

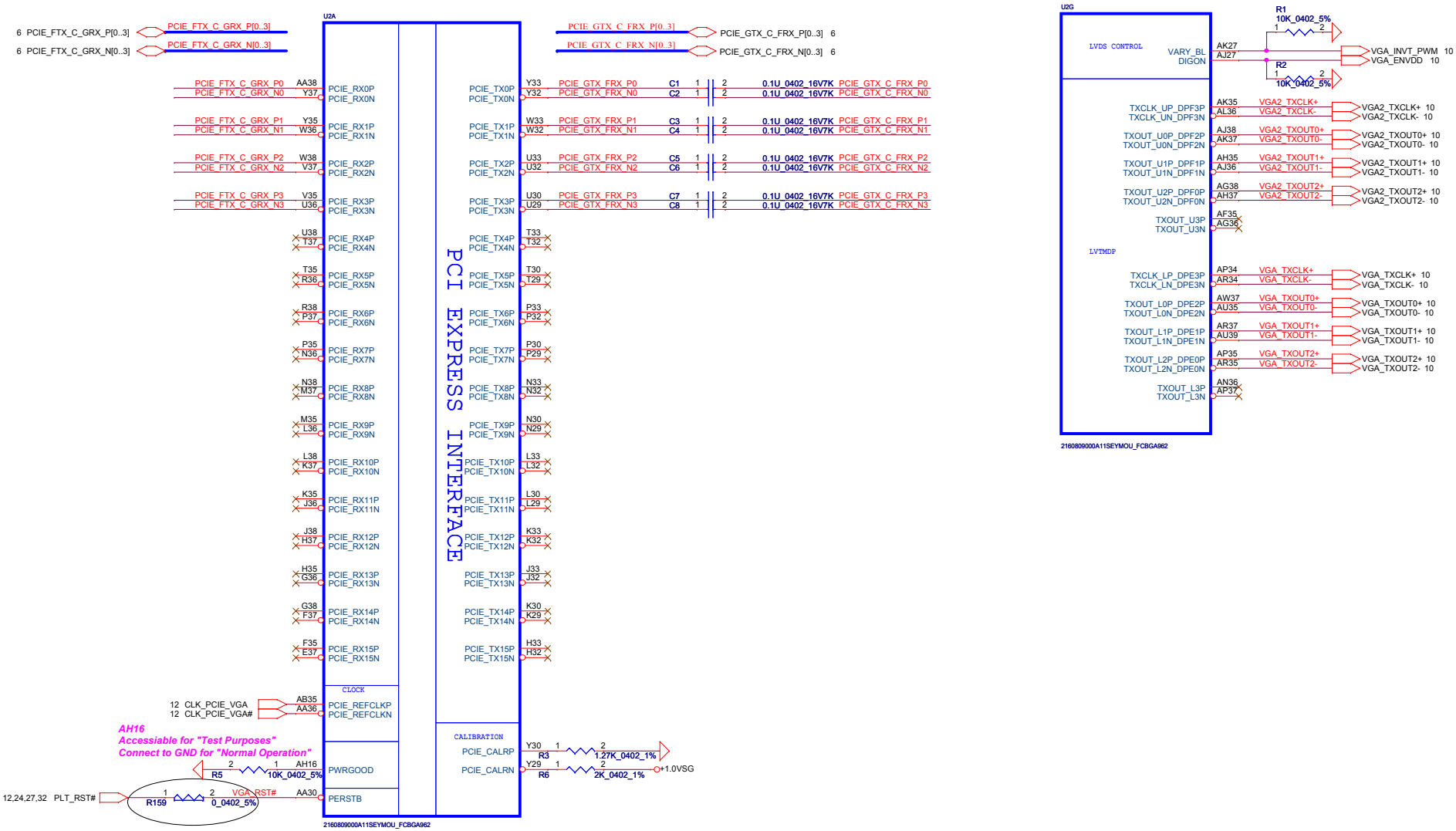
FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/20	Deciphered Date 2012/06/30	Title P16-FCH-VSS/Strap
Size B	Document Number LA7323P		Rev 0.22
Date: Friday, March 04, 2011	Sheet 16 of 47		

GFX PCIE LANE REVERSAL



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P17-Vancouver_ PCIE / LVDS

Size	Document Number	Rev
Custom	LA7323P	0.22

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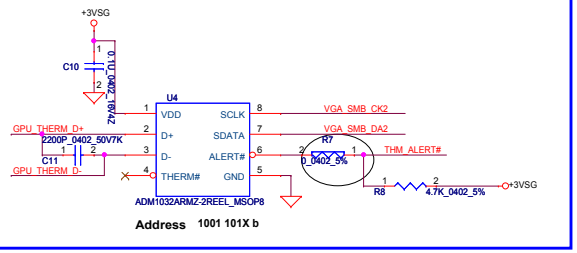
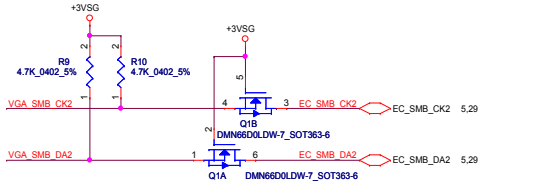
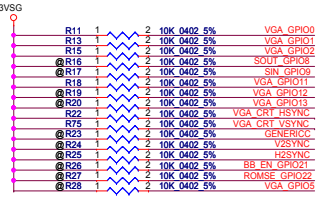
Strap Name		Pin Straps description <all internal PD>	Setting
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	1
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

External VGA Thermal Sensor

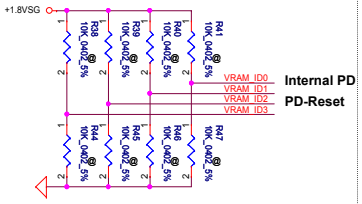


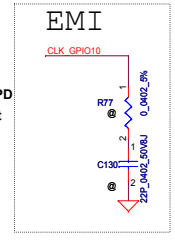


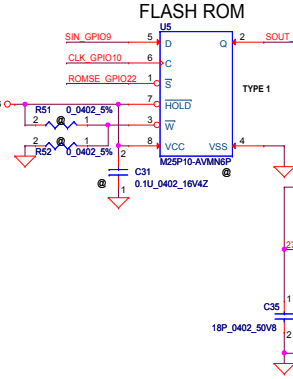


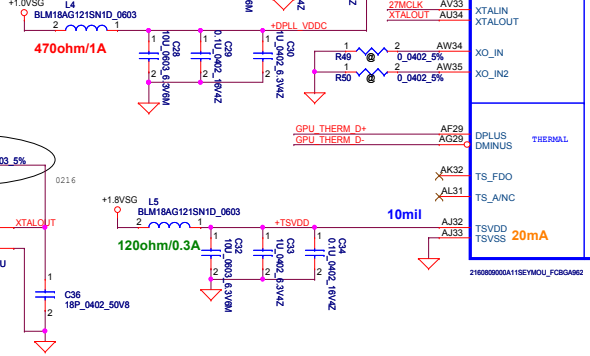
Seymour(XT)

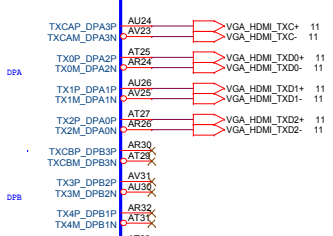
VRAM \ Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung SA00004G830 64M16 K4W1G1646G-BC11	0	0	0	0
Samsung SA00004QA0 128M16 K4W2G1646C-HC11	0	0	0	1
Hynix SA00004IS60 64M16 H5TQ1G63DFR-11C	0	1	0	0
Hynix SA00003YO30 128M16 H5TQ2G63BFR-11C	0	1	0	1

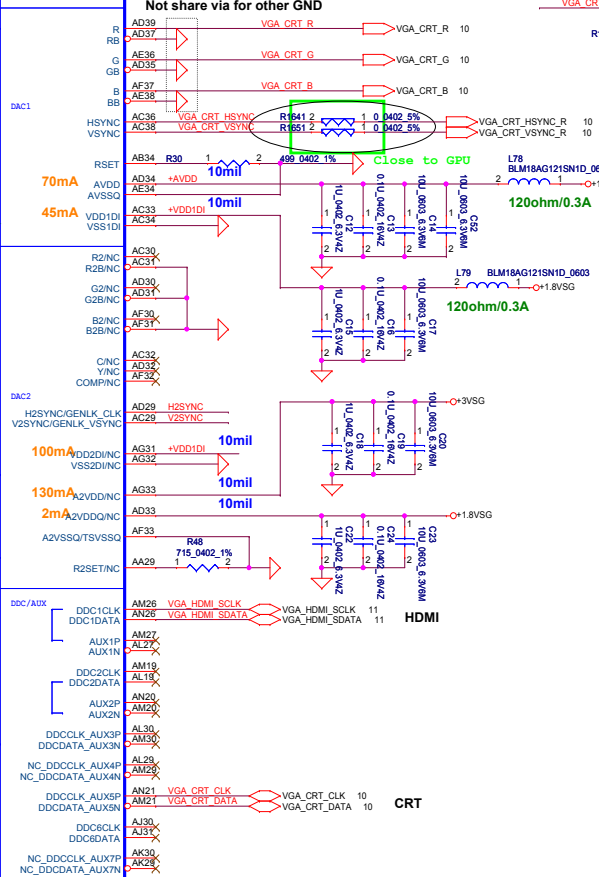


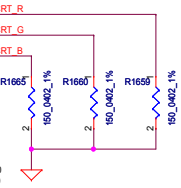












Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

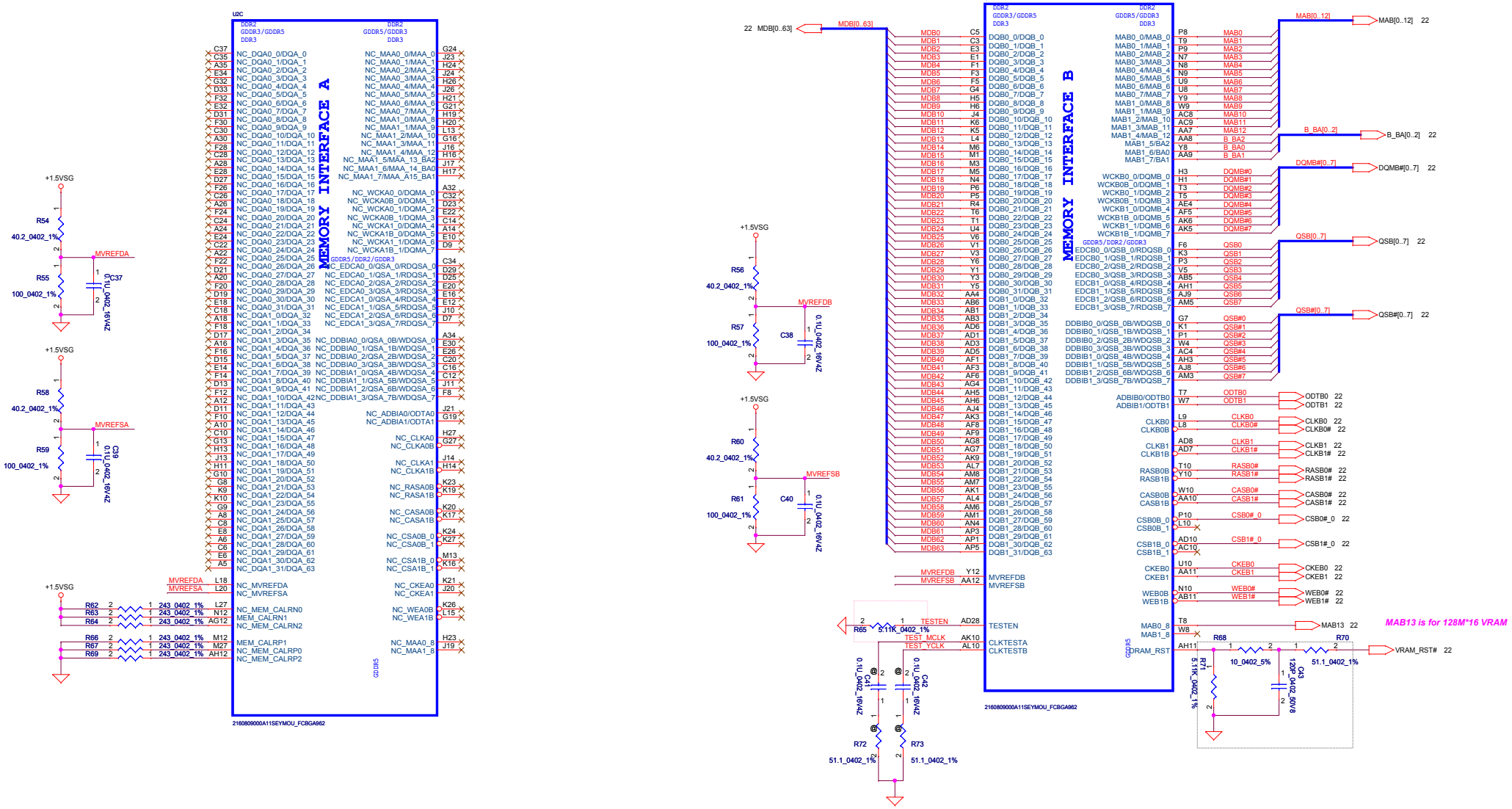
Compal Electronics, Inc.

Title: P18-Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 Sheet 18 of 47

Robson,Seymour only support single channel memory (channel B only)



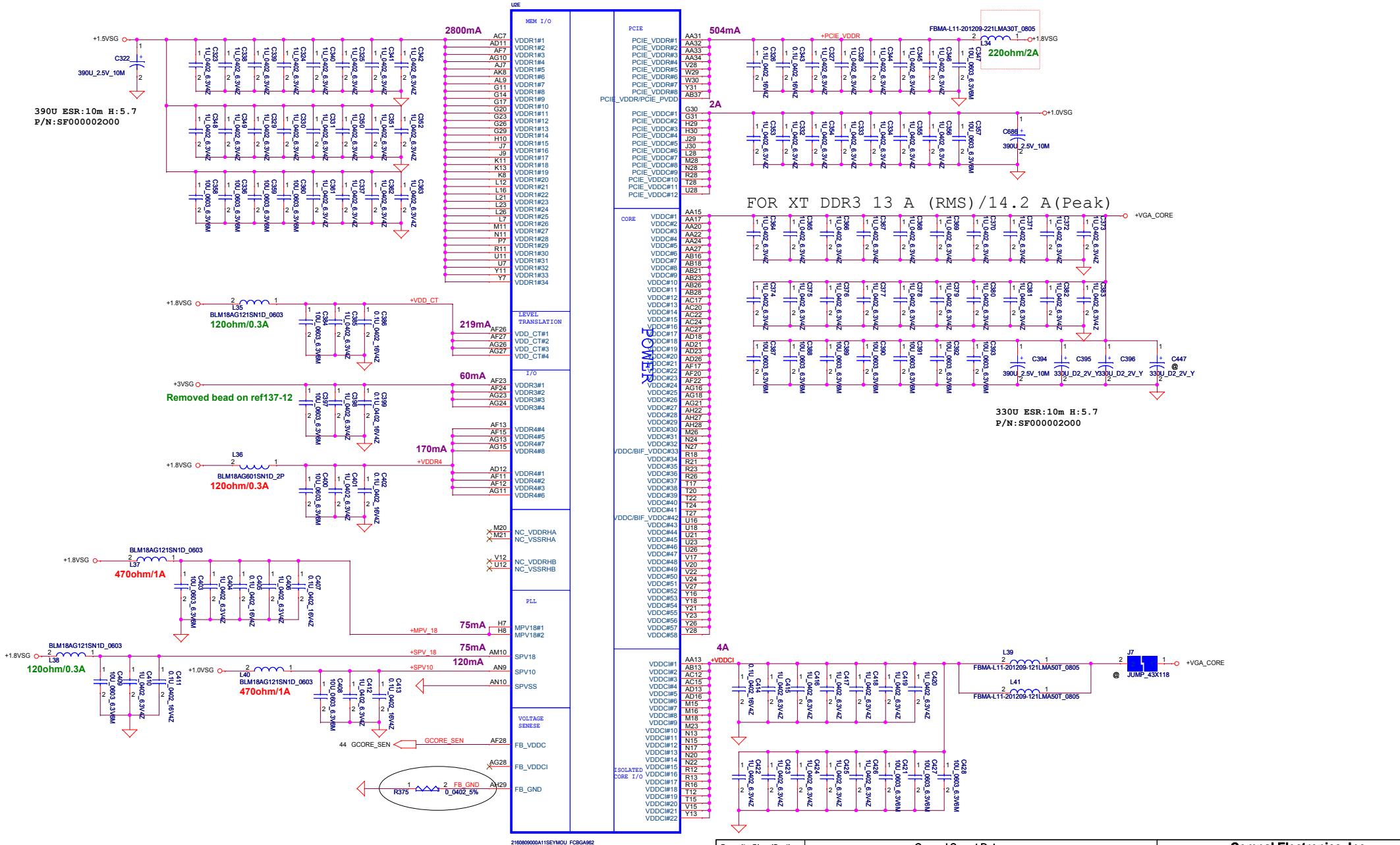
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P19-Vancouver_Memory

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 | Sheet 19 of 47



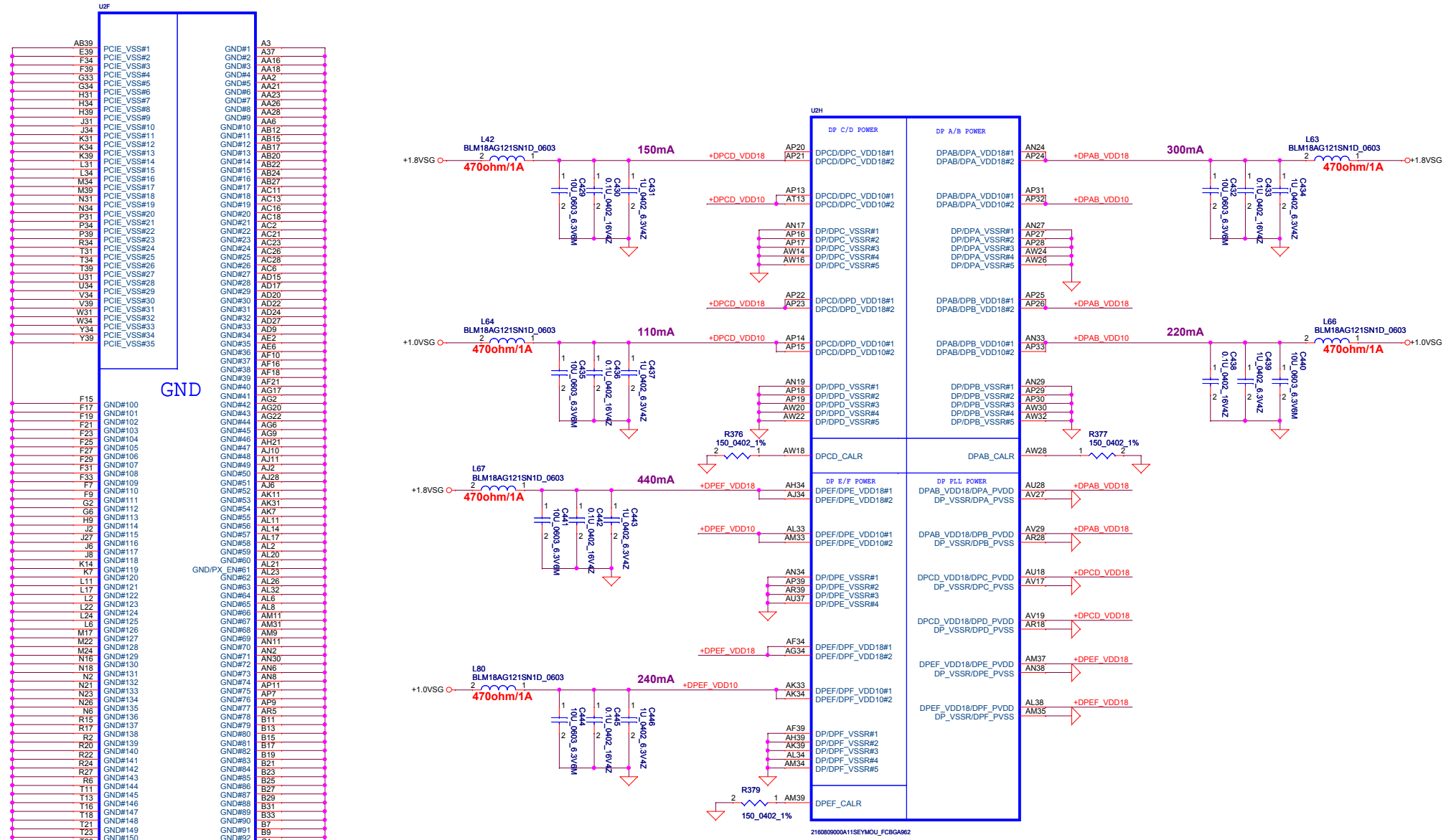
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P20-Vancouver_Power/GND

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 | Sheet 20 of 47



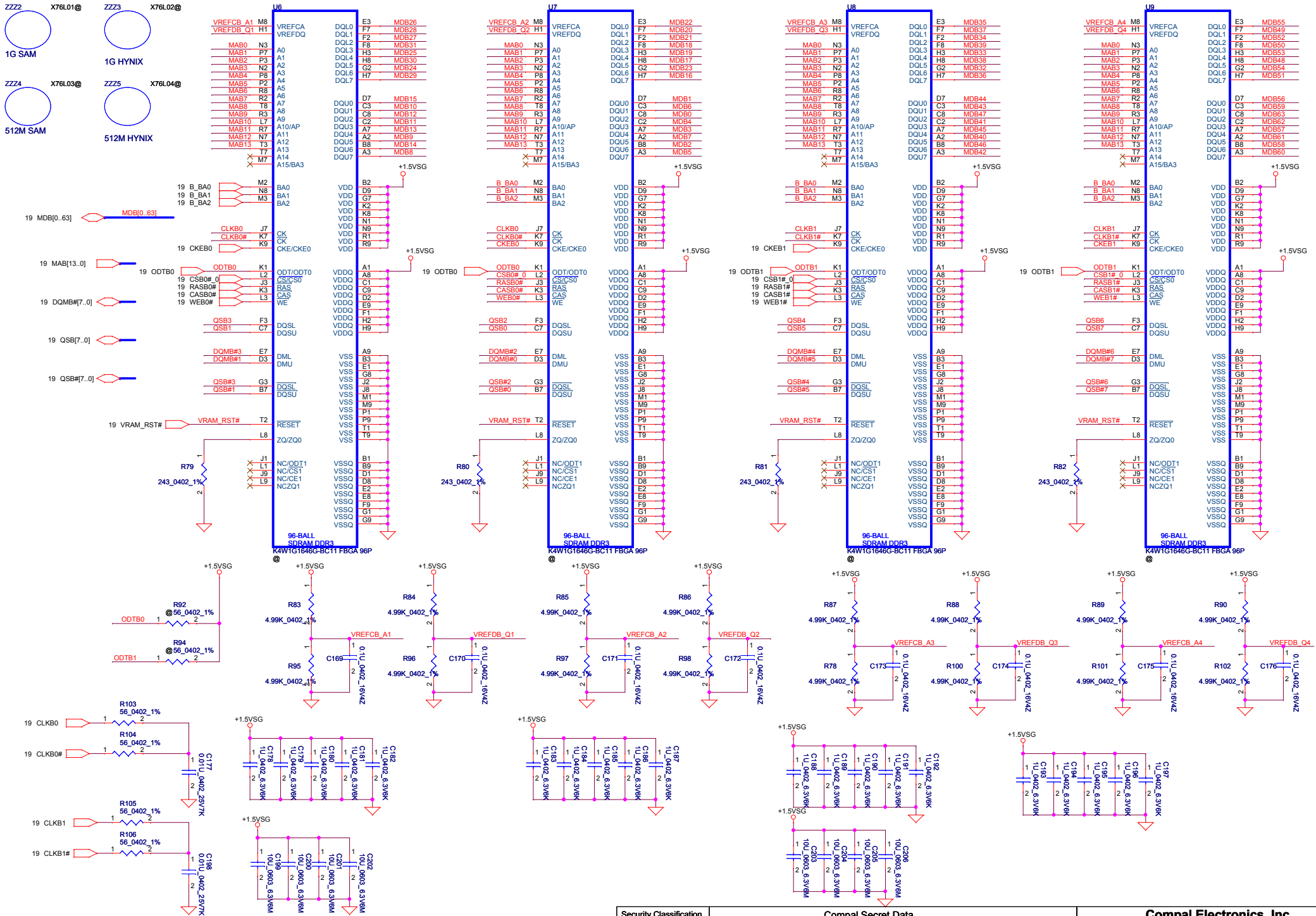
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P21-Vancouver_Power/GND

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 Sheet 21 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

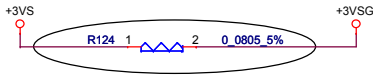
Compal Electronics, Inc.

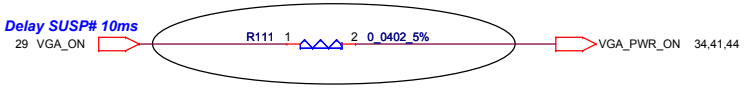
Title: **P22-VRAM_DDR3 / Channel B**

Size	Document Number	Rev
Custom	LA7323P	0.22

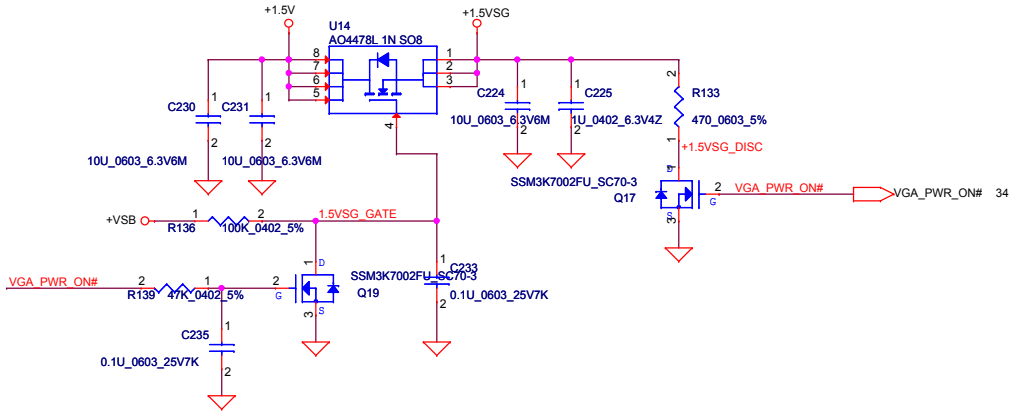
Date: Friday, March 04, 2011 Sheet 22 of 47

+3.3VS TO +3.3VSG



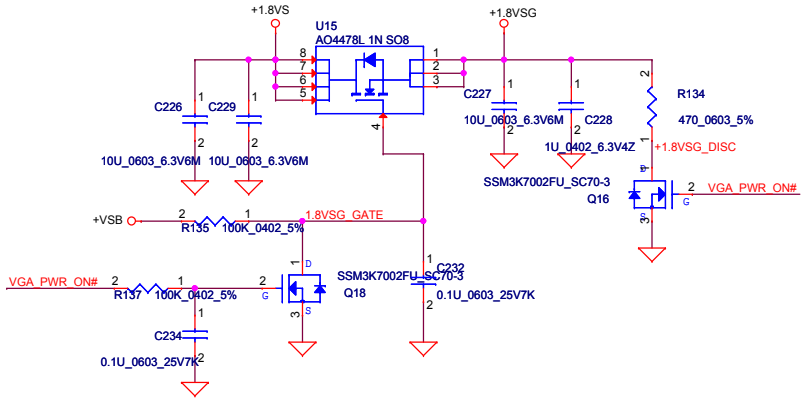


+1.5V TO +1.5VSG



+1.8VS TO +1.8VSG

Change P/N SB00000GV00



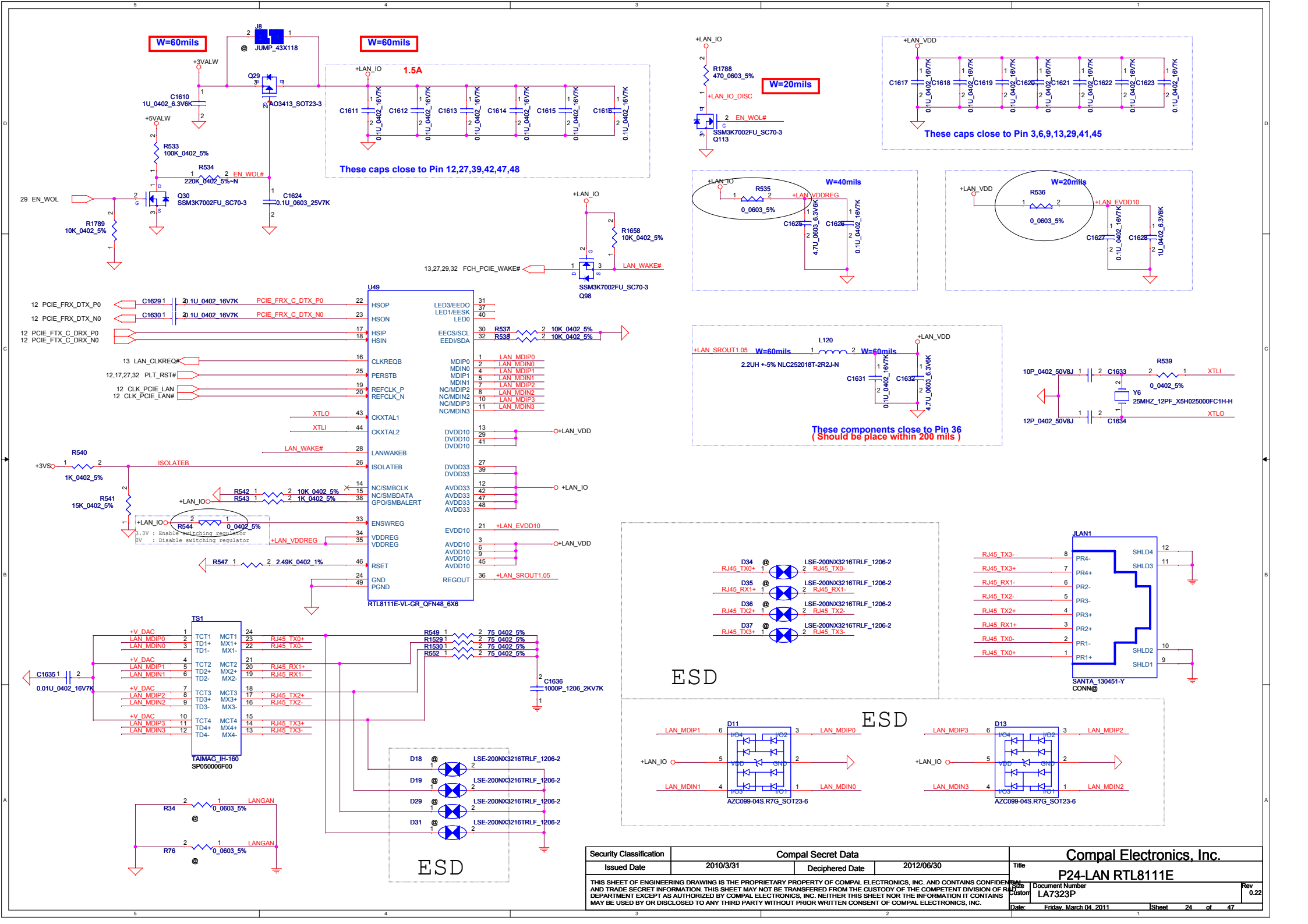
Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P23-VGA DC Interface

Size	Document Number	Rev
Custom	LA7323P	0.22

Date: Friday, March 04, 2011 | Sheet 23 of 47



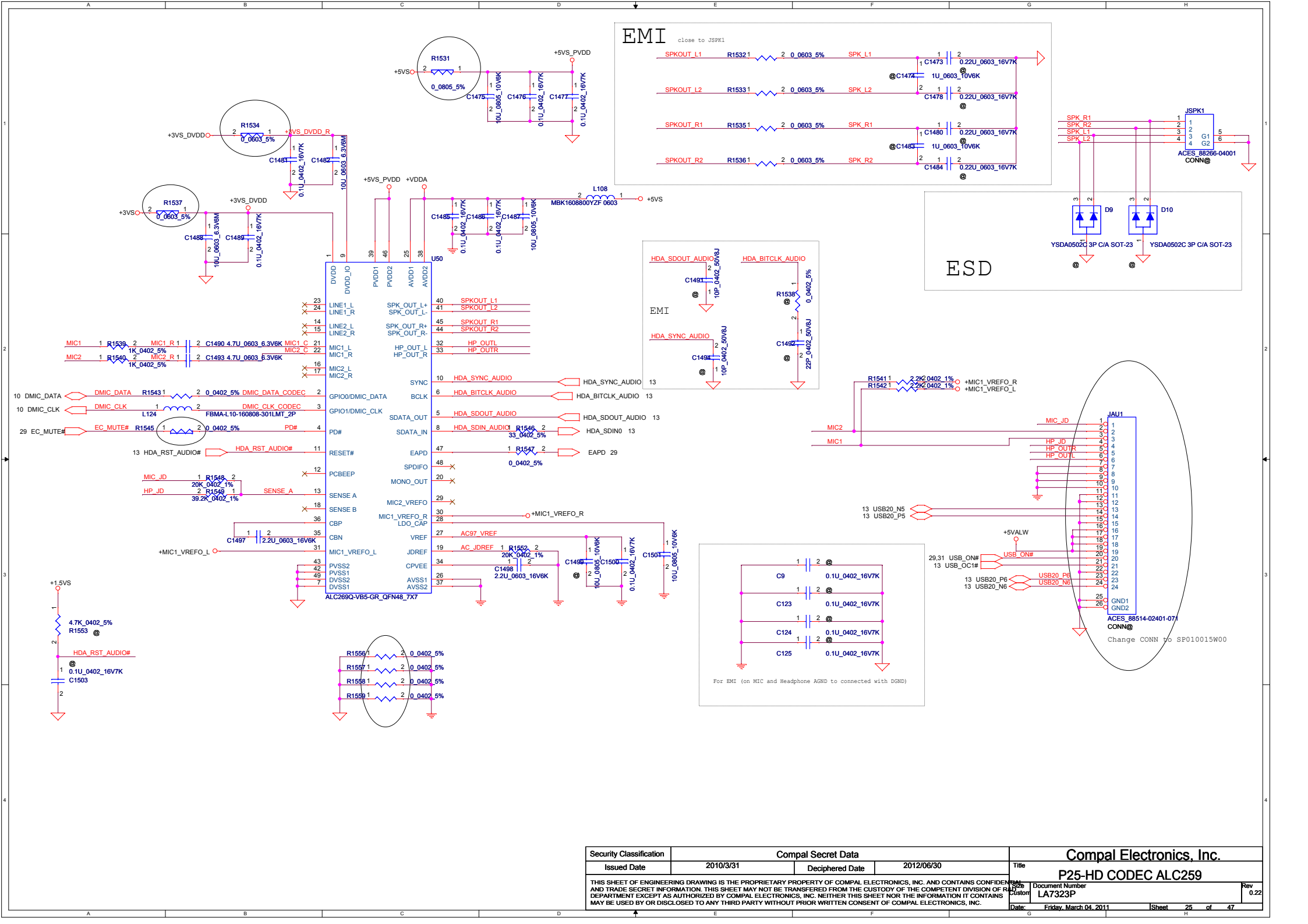
Security Classification	Compal Secret Data		
Issued Date	2010/3/31	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P24-LAN RTL8111E

Size: Custom | Document Number: LA7323P | Rev: 0.22

Date: Friday, March 04, 2011 | Sheet 24 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/3/31	Deciphered Date	2012/06/30

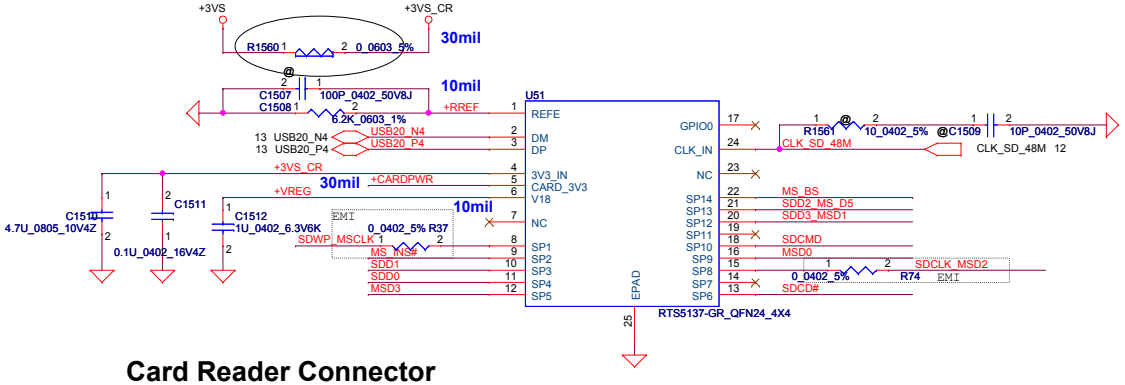
Compal Electronics, Inc.

Title: P25-HD CODEC ALC259

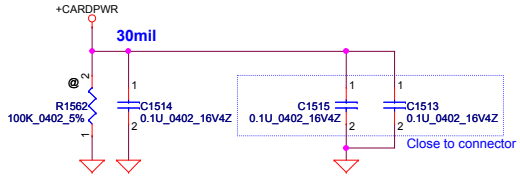
Size: Custom | Document Number: LA7323P | Rev: 0.22

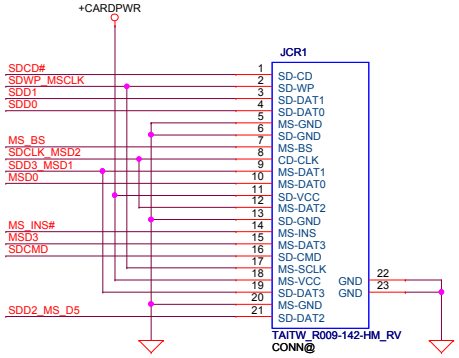
Date: Friday, March 04, 2011 | Sheet 25 of 47

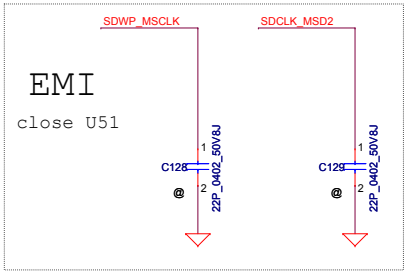
Card Reader RTS5137
(only SD/MMC/MS function)



Card Reader Connector







Security Classification	Compal Secret Data		
Issued Date	2009/10/08	Deciphered Date	2012/06/30

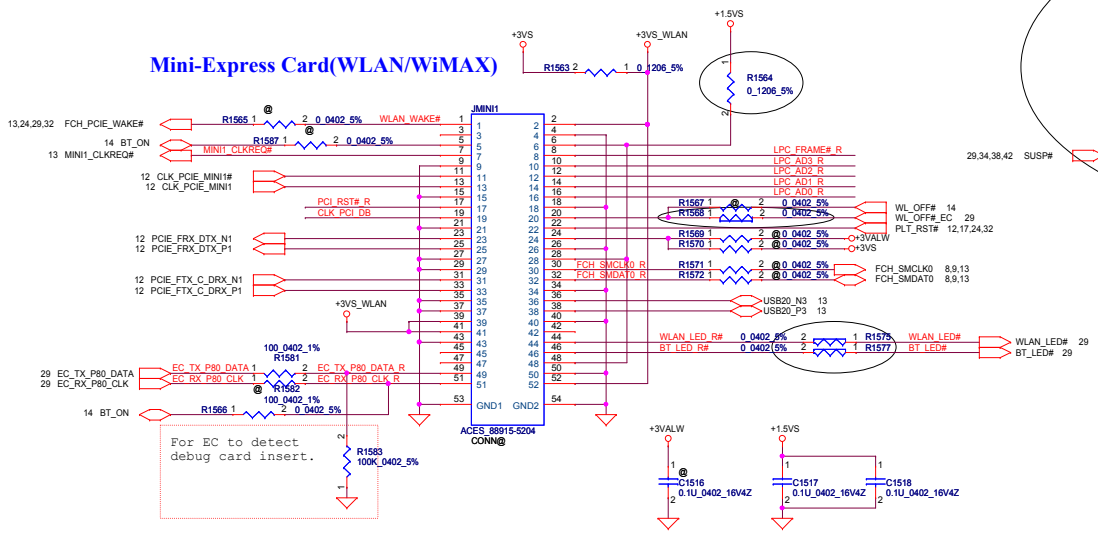
Compal Electronics, Inc.

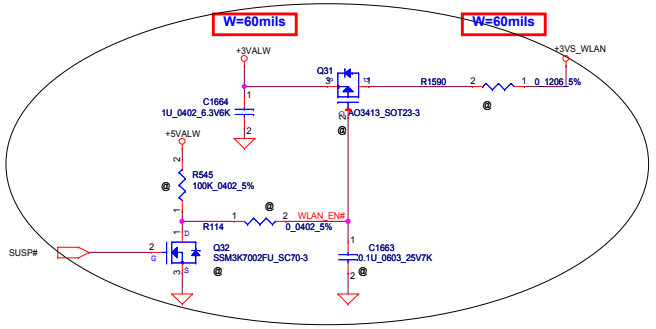
Title: P26-RTS5137 Media Card Controller

Size: Custom | Document Number: LA7323P | Rev: 0.22

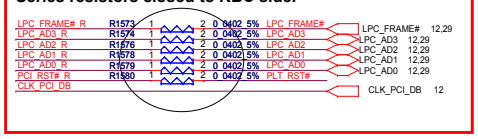
Date: Friday, March 04, 2011 | Sheet 26 of 47

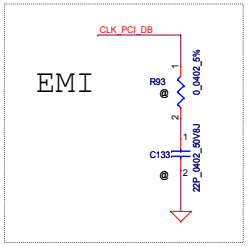
Mini-Express Card for WLAN/WiMAX(Half)

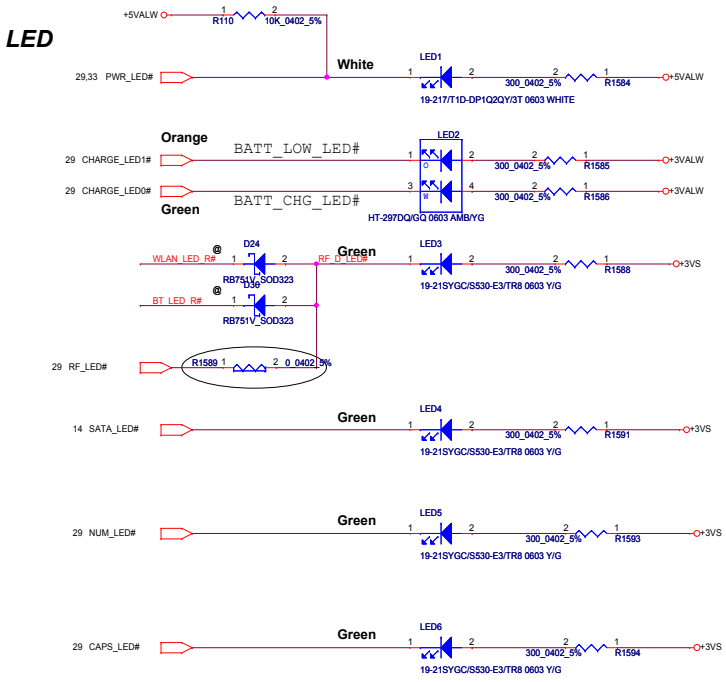


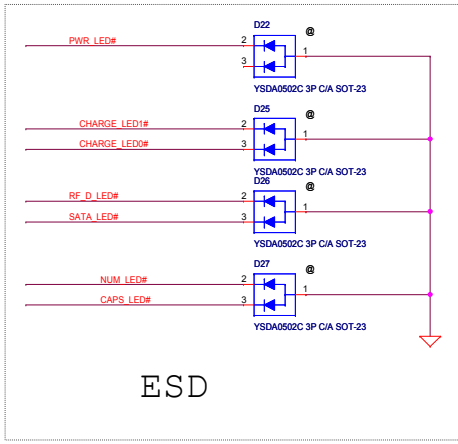


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.







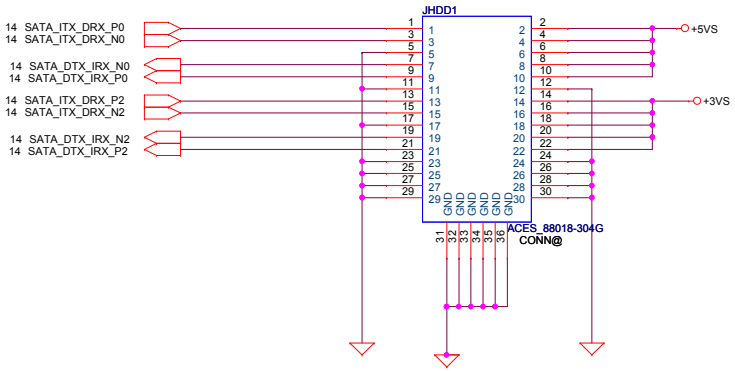


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

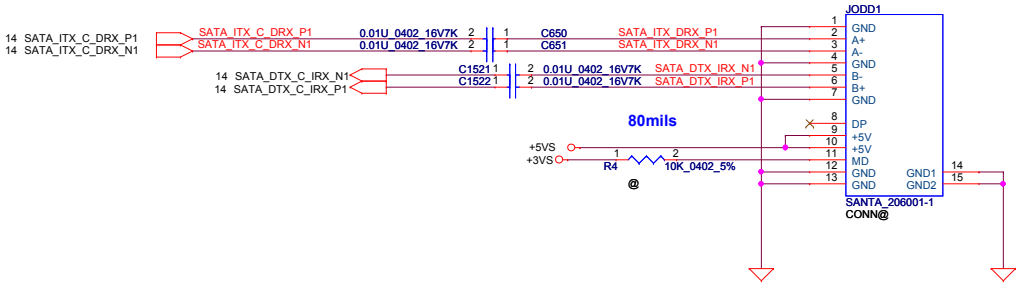
Compal Electronics, Inc.

Title	P27-Mini PCIE/LED	
Size	Document Number: LA7323P	Rev: 0.22
Date: Friday, March 04, 2011	Sheet 27 of 47	

SATA HDD BTB Conn.



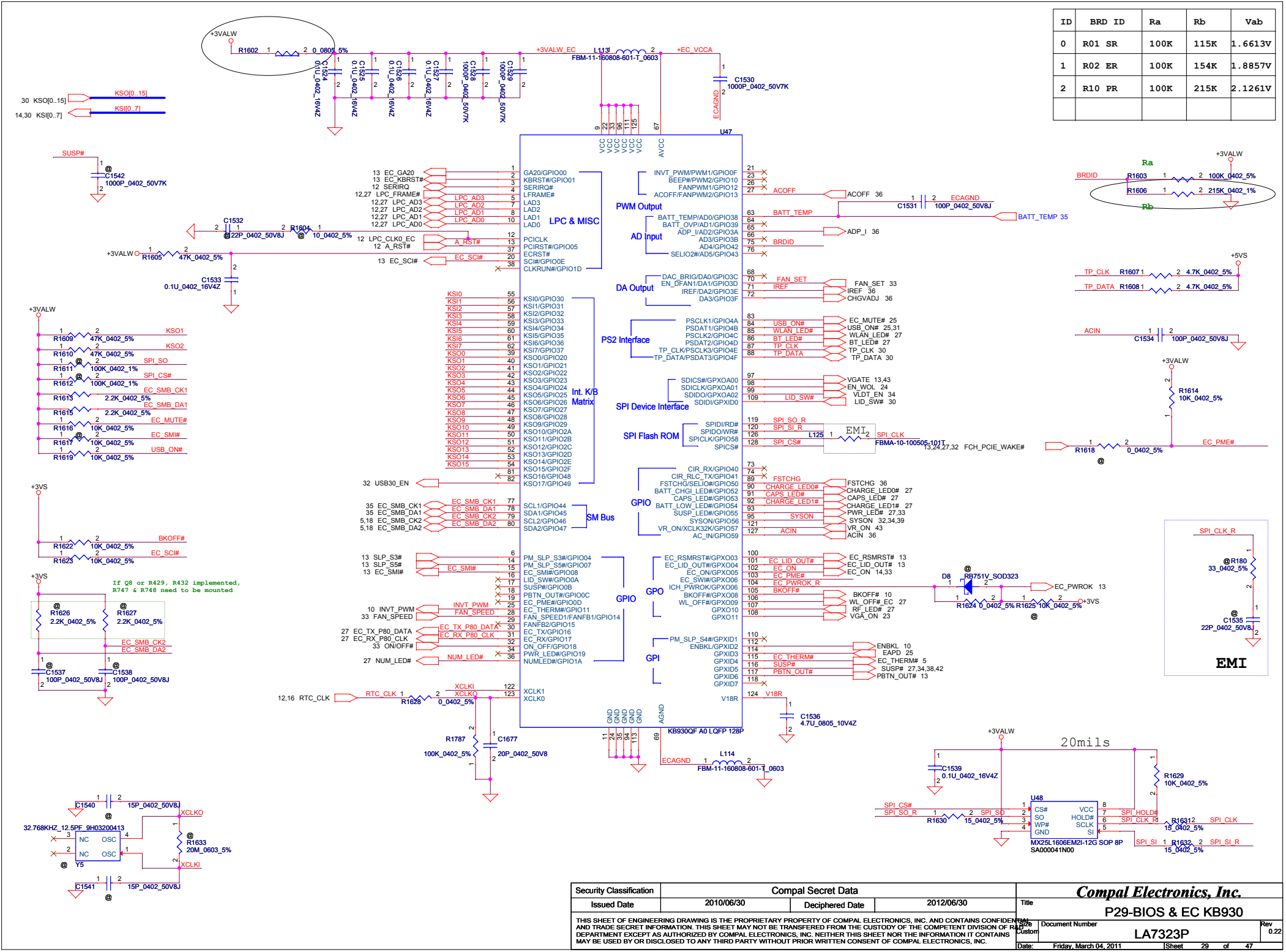
SATA ODD FFC Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.			
Title: P28-HDD & ODD CONN			
Size: B	Document Number: LA7323P		Rev: 0.22
Date: Friday, March 04, 2011		Sheet 28 of 47	

ID	BRD ID	Ra	Rb	Vab
0	R01 SR	100K	115K	1.6613V
1	R02 ER	100K	154K	1.8857V
2	R10 PR	100K	215K	2.1261V



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P29-BIOS & EC KB930

Size	Document Number	Rev
Custom	LA7323P	0.22

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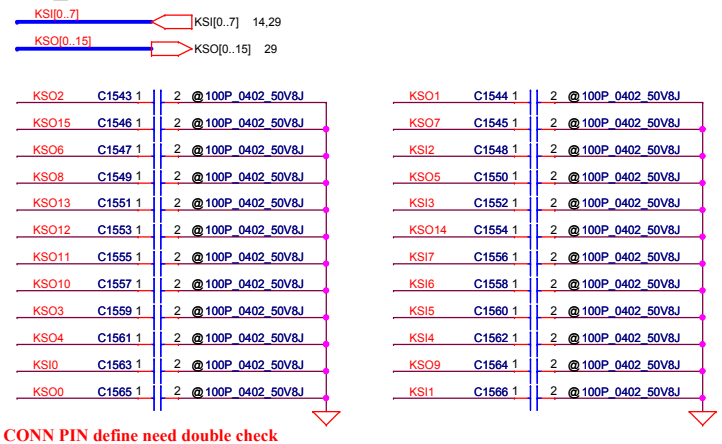
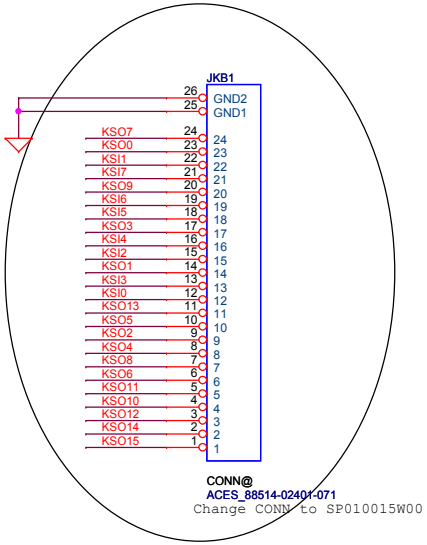
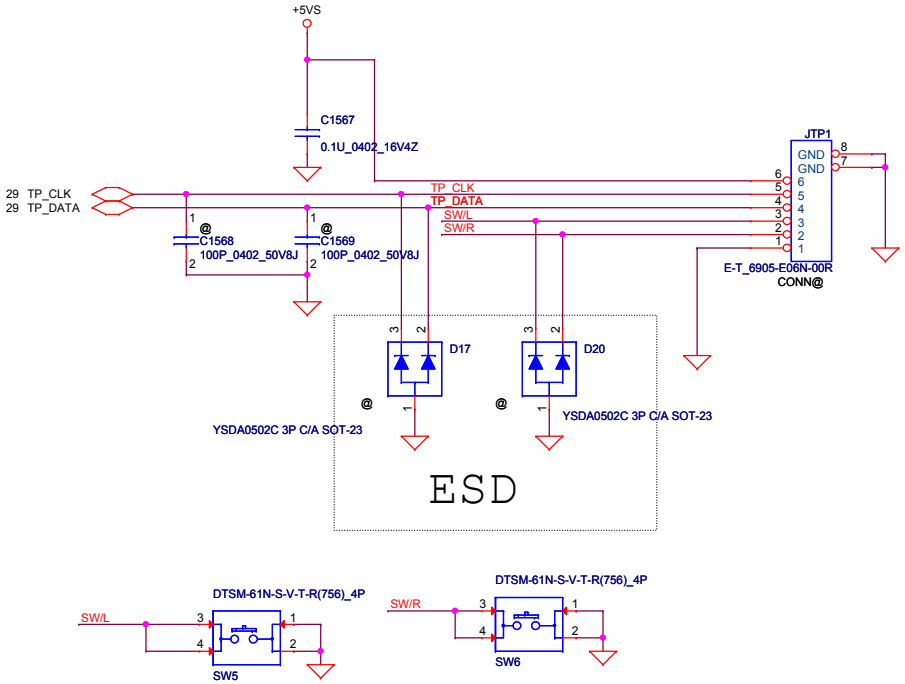
INT_KBD Conn.

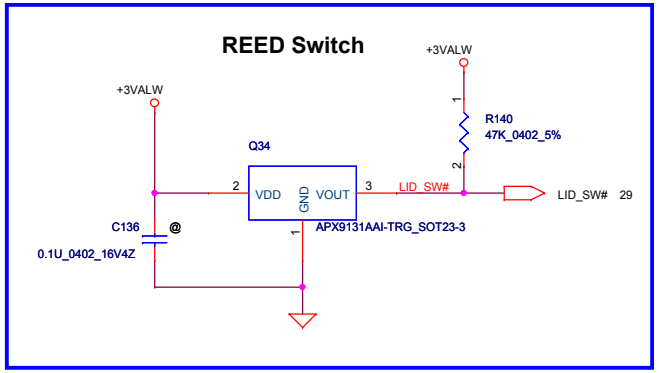


CONN PIN define need double check



To TP/B Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P30-KB /SW/TP/Lid

Size	Document Number	Rev
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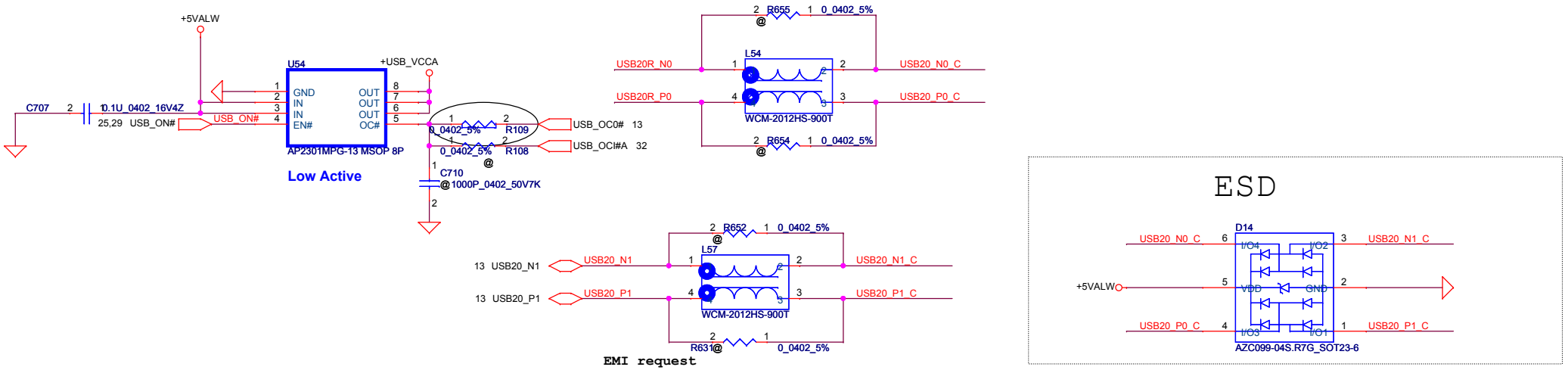

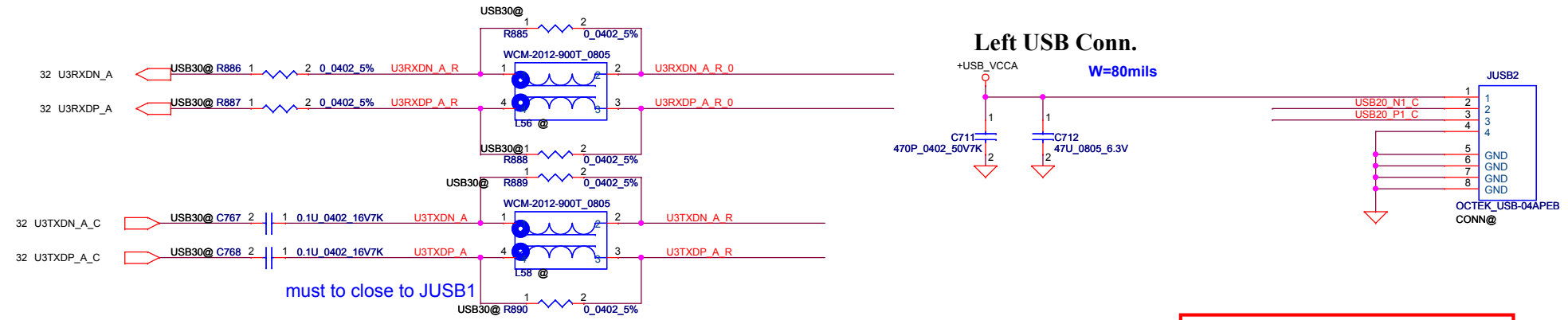

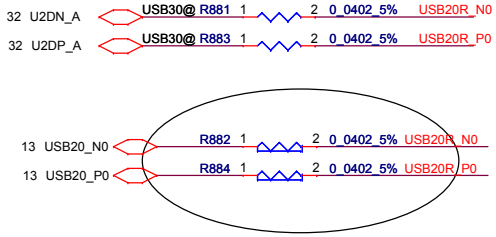

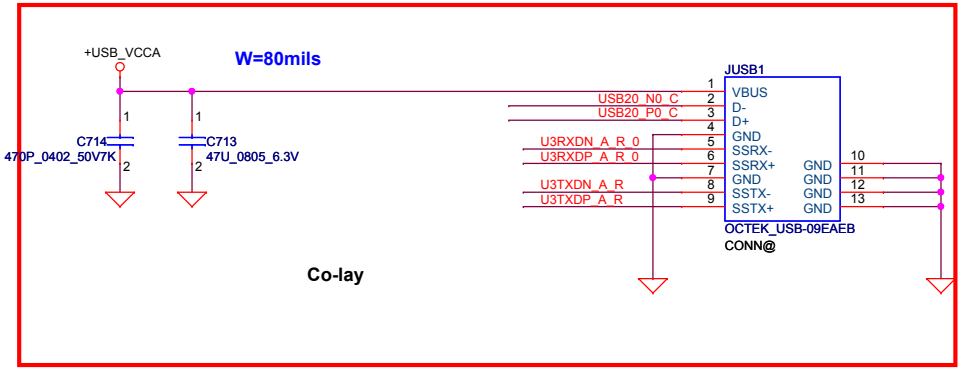

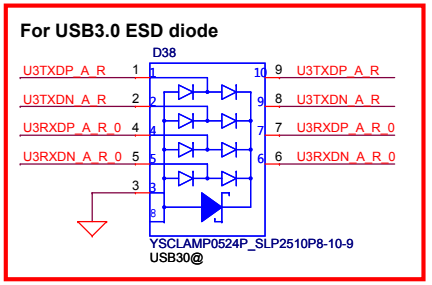

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P31-USB/BT/USBsub

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For WAKE Function

USB_PEPWRDET

	R1719	R1706
S1	Mount	@
S3	@	Mount

USB_PESEL

	R808	R825
Other applaction	Mount	@
Express Card/Mini Card	@	Mount

Power Sequence

ASM1042

+5V
+3V
+1.2V_VTT
PORST#
PE_RST#

T1: 70~80ms
T2: >20ms

ASM1042 (TQFN 64)

Close to ASM1042

+3VALW to +3V Transfer

RT9701-PB_SOT23-5

1208 Add switch

SSM3K7002FU_SC70-3

+3VALW to +1.2V Transfer

APL5930KAI-TRG_SO8

MX25L5121EMC-20G SOP 8P

FBMA-L11-201209-221LMA30T_0805

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P32-USB3.0

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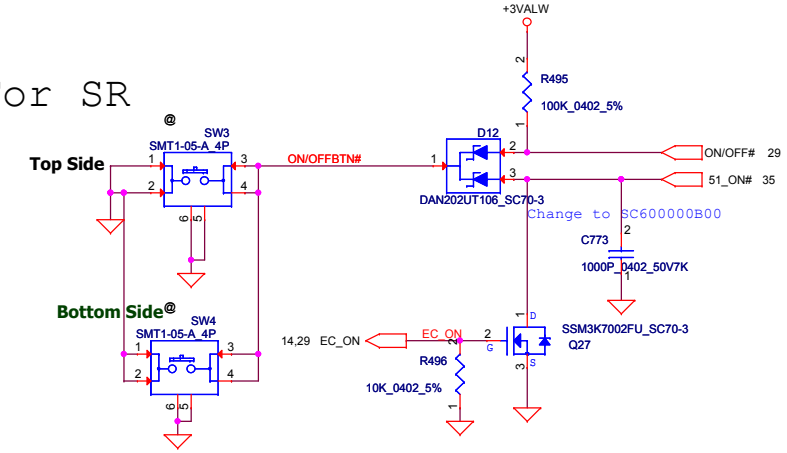
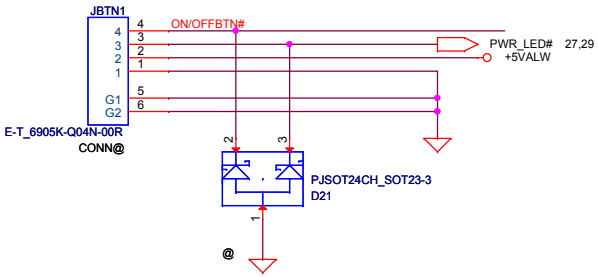
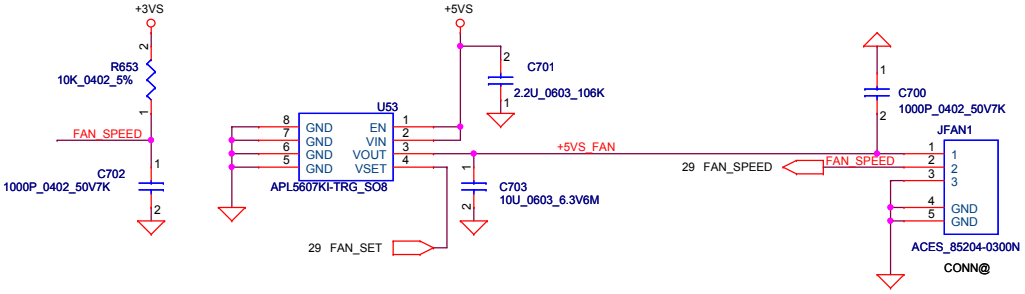
ON/OFF switch **Power Button**

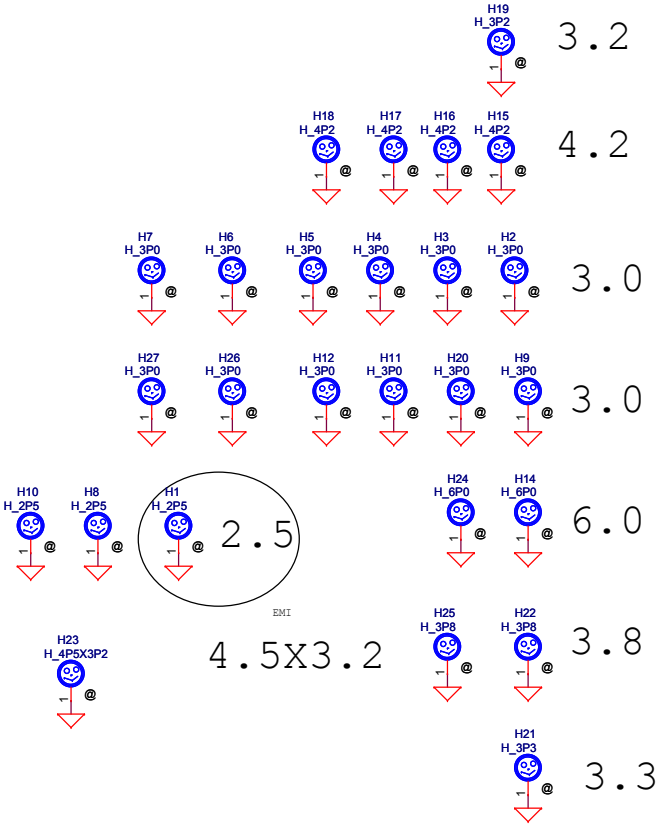
For SR





Fan Control Circuit





FD1 FIDUCIAL_C40M80
FD2 FIDUCIAL_C40M80
FD3 FIDUCIAL_C40M80
FD4 FIDUCIAL_C40M80

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P33-Other IO/USB (right)

Size	Document Number	Rev
Custom	LA7323P	0.22

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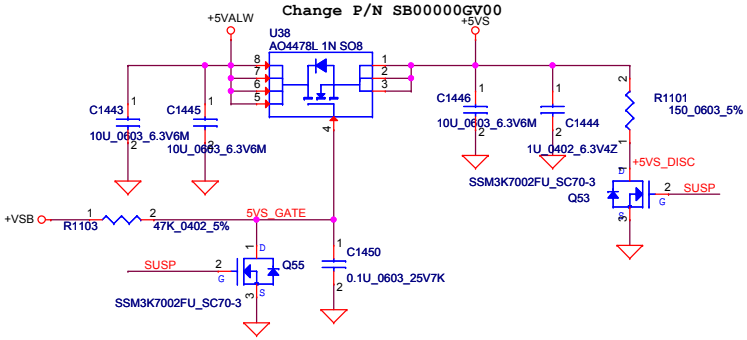
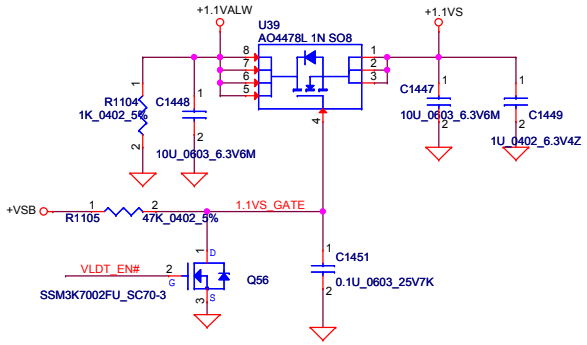
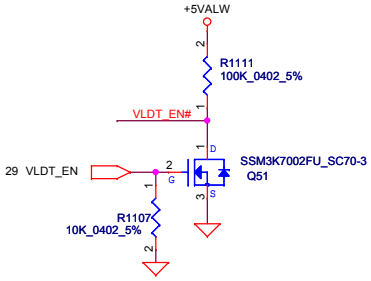
+5VALW TO +5VS

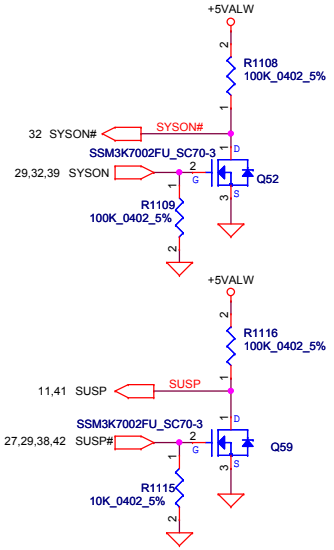
Change P/N SB00000GV00



+1.1VALW TO +1.1VS

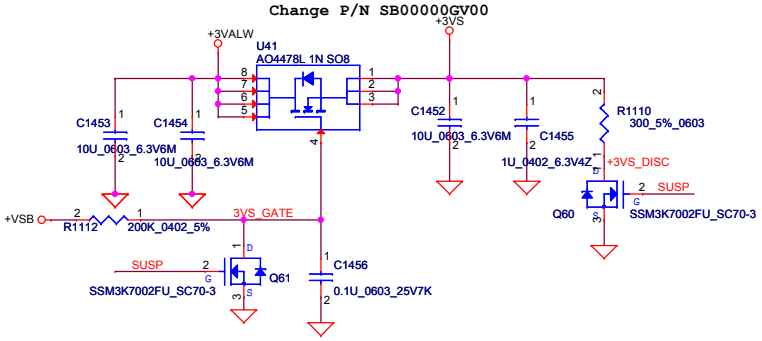




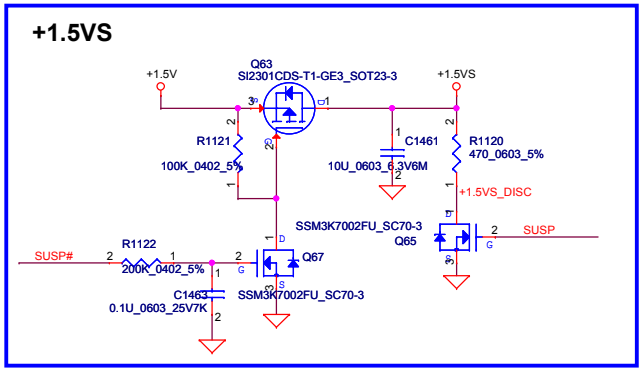


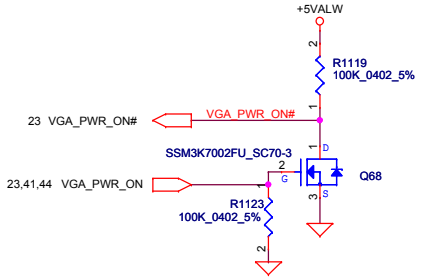
+3VALW TO +3VS

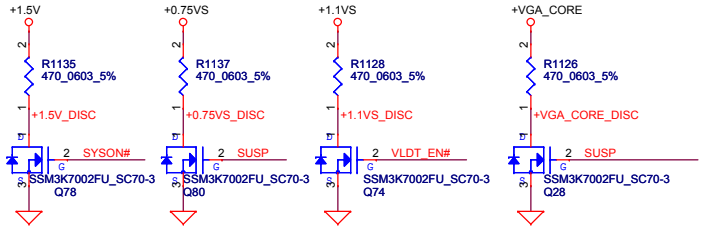
Change P/N SB00000GV00



+1.5VS







Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2012/06/30

Compal Electronics, Inc.

Title: P34-DC Interface

Size: Custom	Document Number: LA7323P	Rev: 0.22
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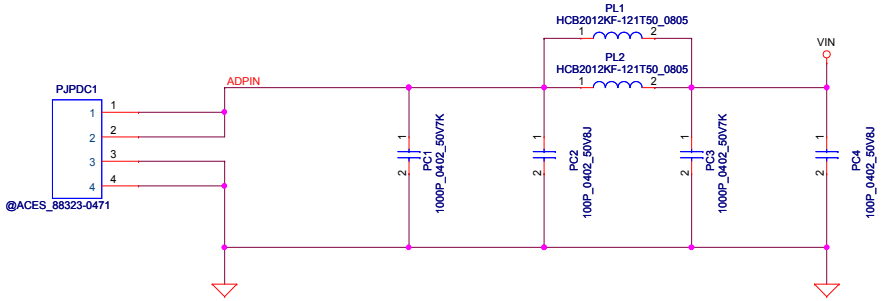
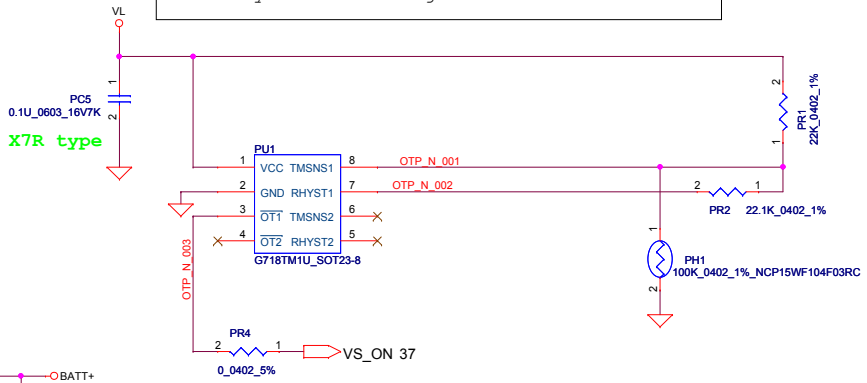
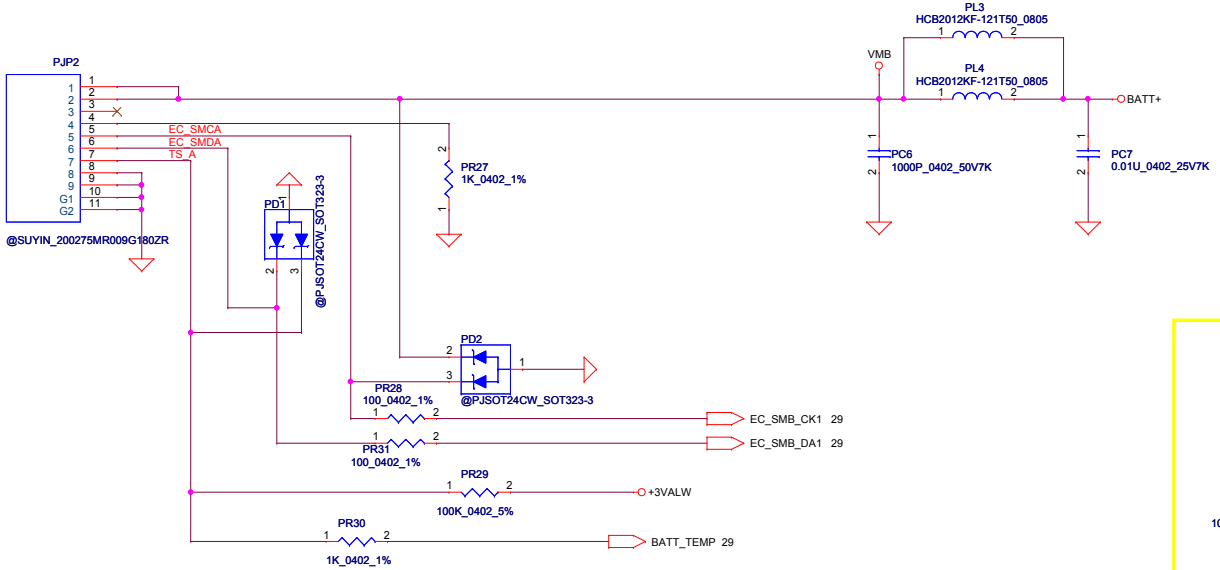
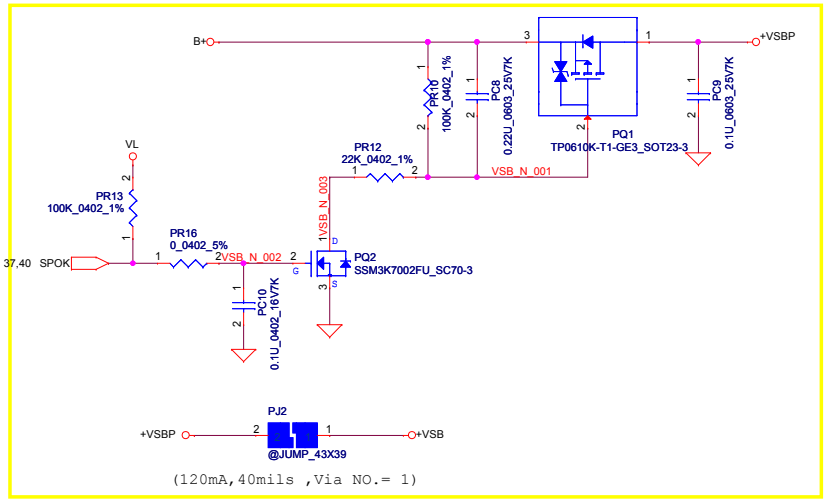
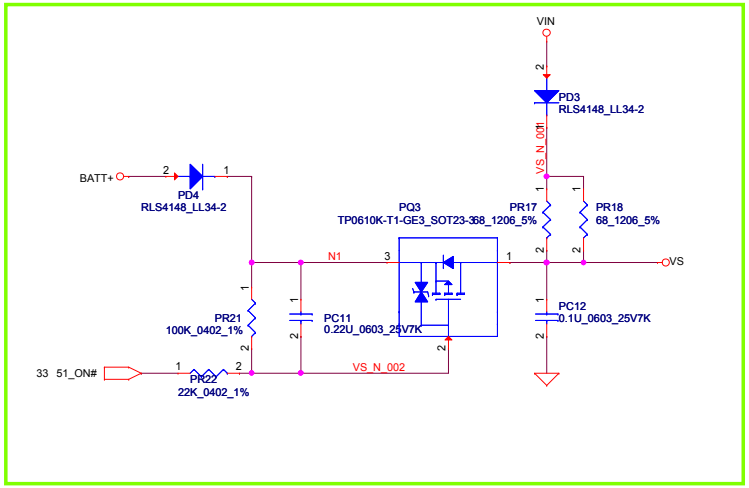
PH1 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 80 +-3 degree C











Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **DCIN / BATT CONN / OTP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.22

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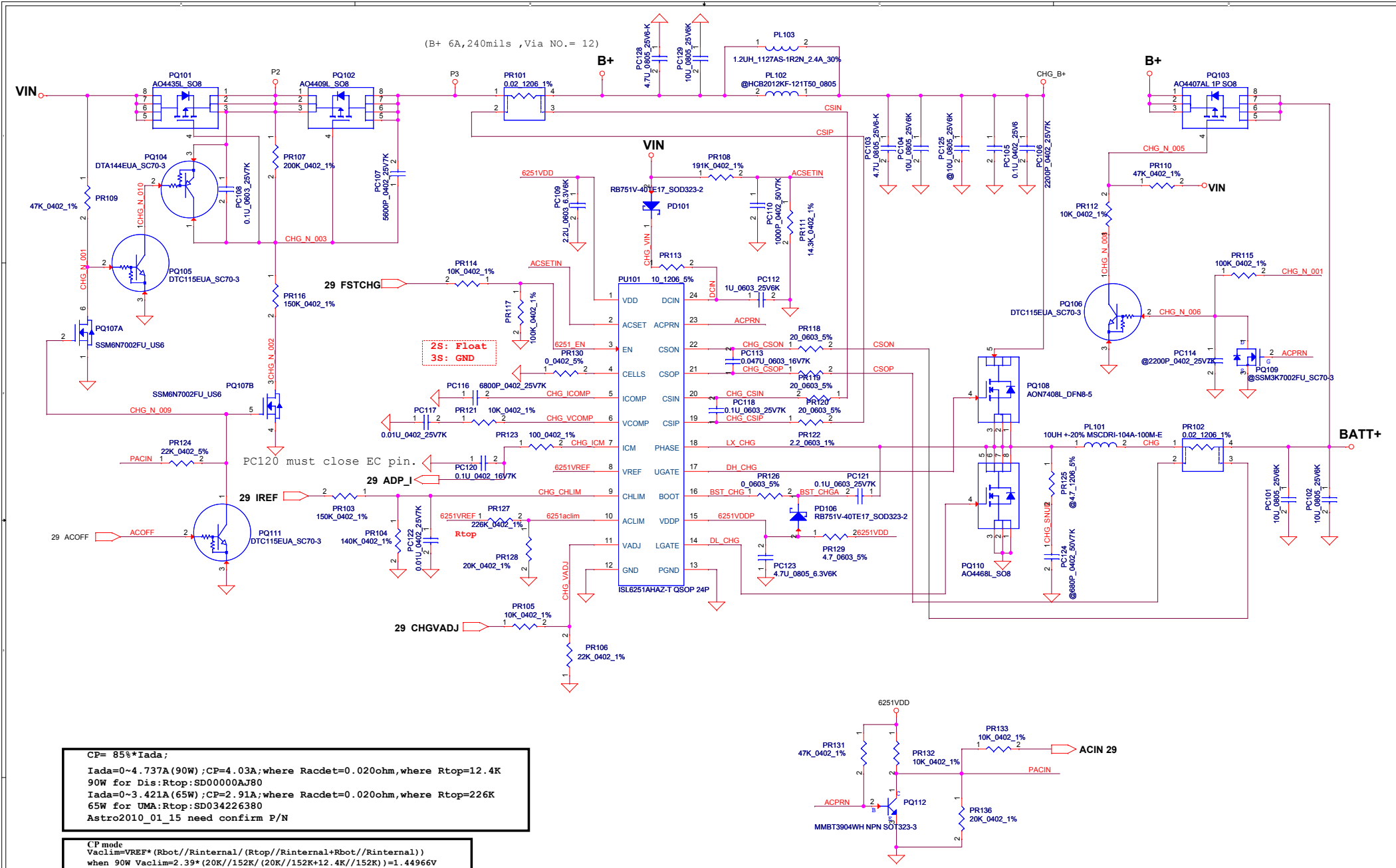

CP= 85%*Iada;

Iada=0~4.737A(90W);CP=4.03A;where Racdet=0.020ohm,where Rtop=12.4K
90W for Dis:Rtop:SD00000AJ80
Iada=0~3.421A(65W);CP=2.91A;where Racdet=0.020ohm,where Rtop=226K
65W for UMA:Rtop:SD034226380
Astro2010_01_15 need confirm P/N

CP mode

Vaclim=VREF*(Rbot//Rinternal/(Rtop//Rinternal+Rbot//Rinternal))
when 90W Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V
when 65W Vaclim=2.39*(20K//152K/(20K//152K+226K//152K))=0.38914V
Iinput=(1/Racdet)*((0.05*Vaclim/VREF+0.05))
when 90W,Iinput=(1/0.02)*(0.05*1.44966/2.39+0.05)=4.02A
when 65W,Iinput=(1/0.02)*(0.05*0.38914/2.39+0.05)=2.92A

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.22

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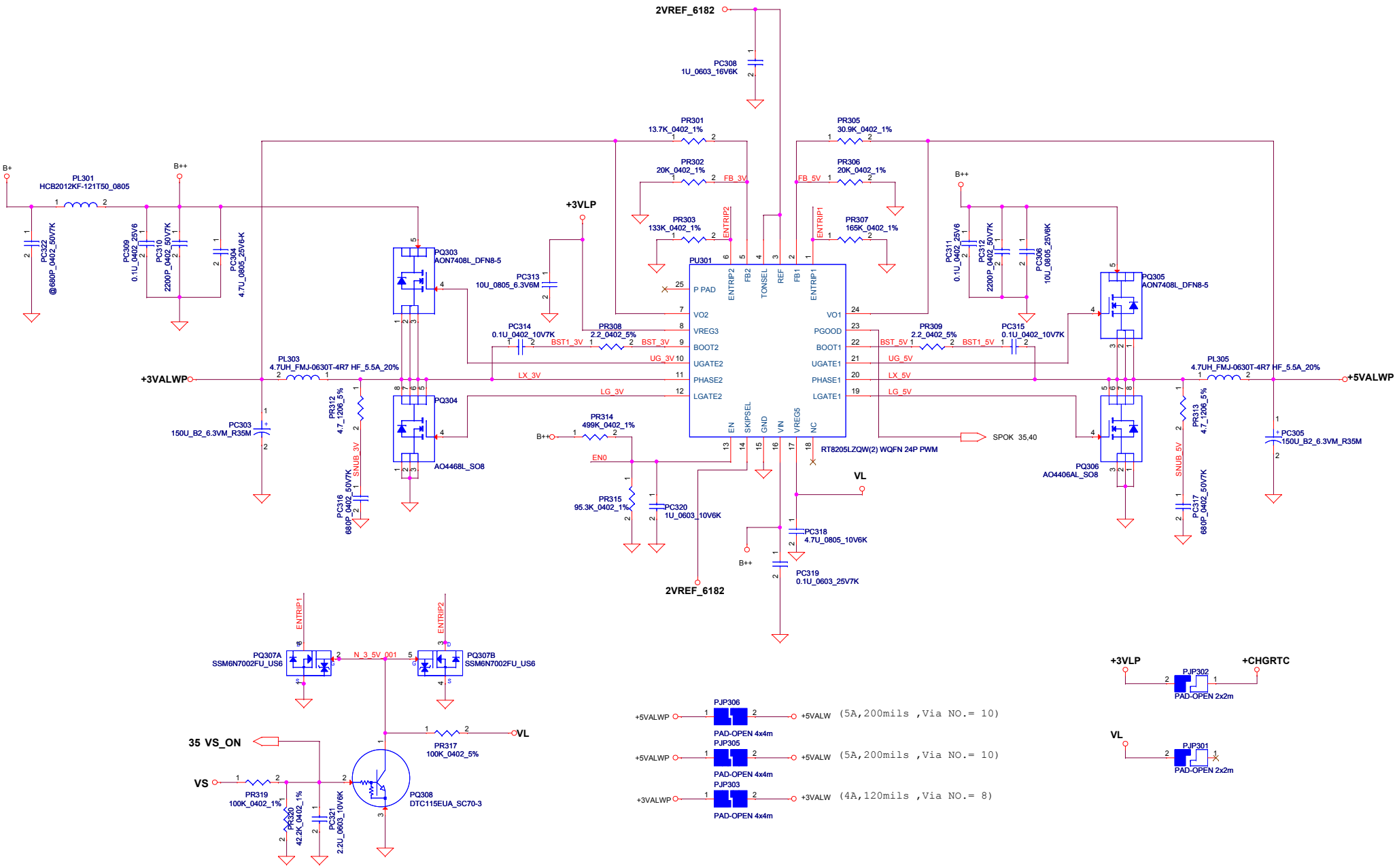


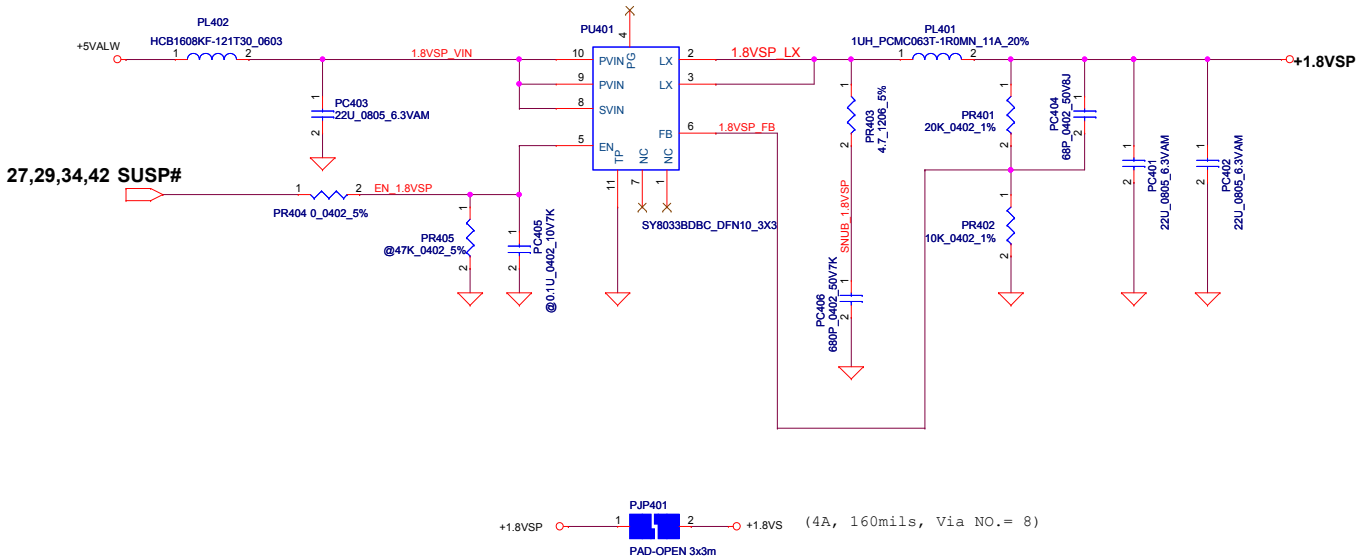
EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 42.2K

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

Compal Electronics, Inc.

Title: **3.3VALWP/5VALWP**

Size: Custom	Document Number: LAXXXX	Rev: 0.22
Date: Friday, March 04, 2011	Sheet 37 of 47	



<Vo=1.8V> VFB=0.6V
Vo=VFB*(1+PR401/PR402)=0.6*(1+20K/10K)=1.8V

(4A, 160mils, Via NO.= 8)

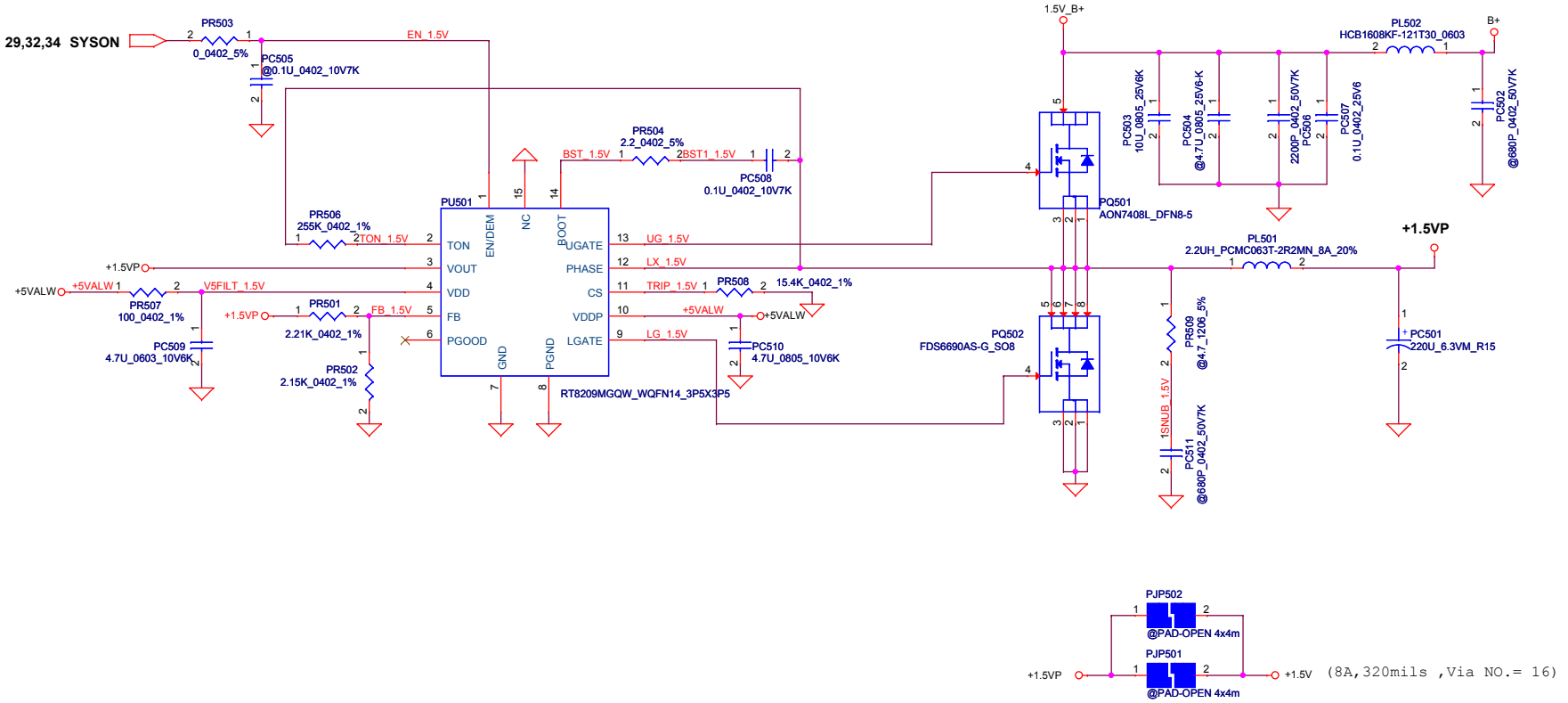
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.22

Date: Friday, March 04, 2011 | Sheet 38 of 47



Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	2008/05/29

Compal Electronics, Inc.

Title: **+1.5VP**

Size	Document Number	Rev
	LAXXXX	0.22

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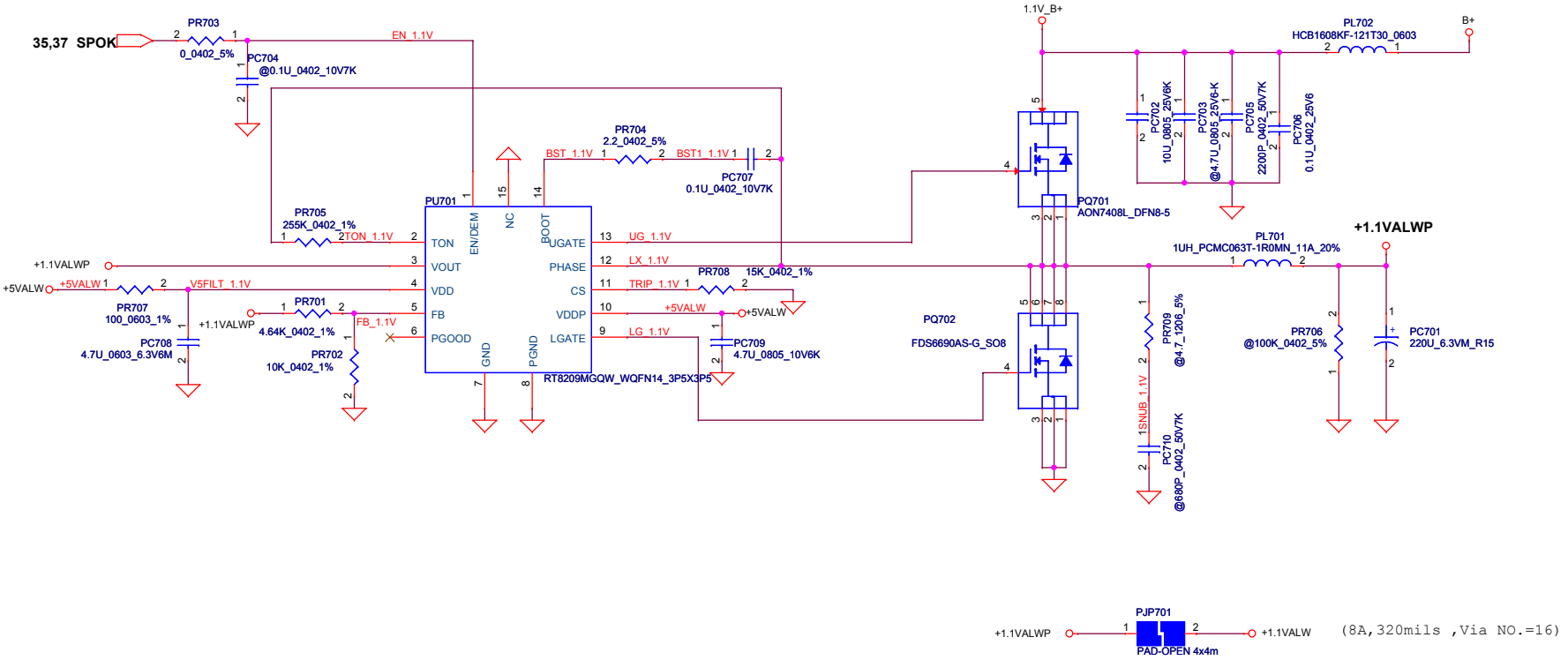

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR+1.1VALWP

Size: Custom | Document Number: LAXXXX | Rev: 0.22

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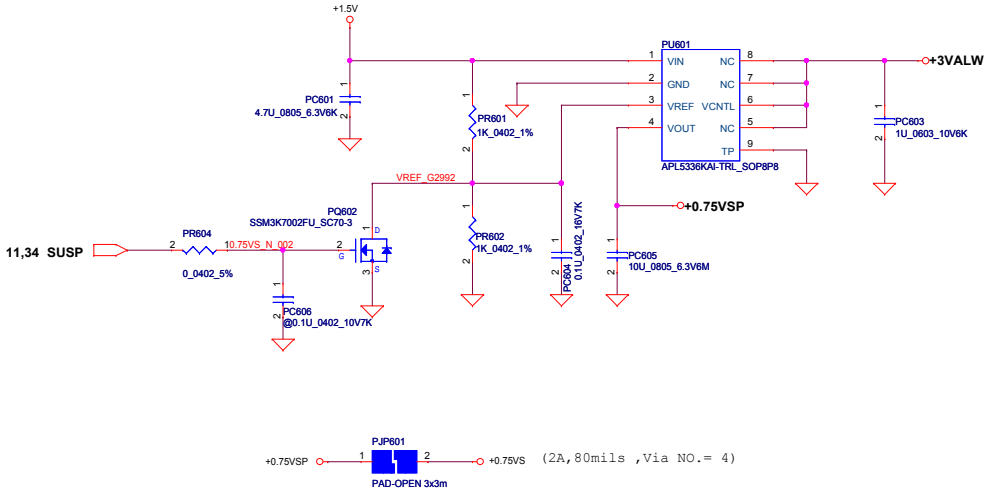
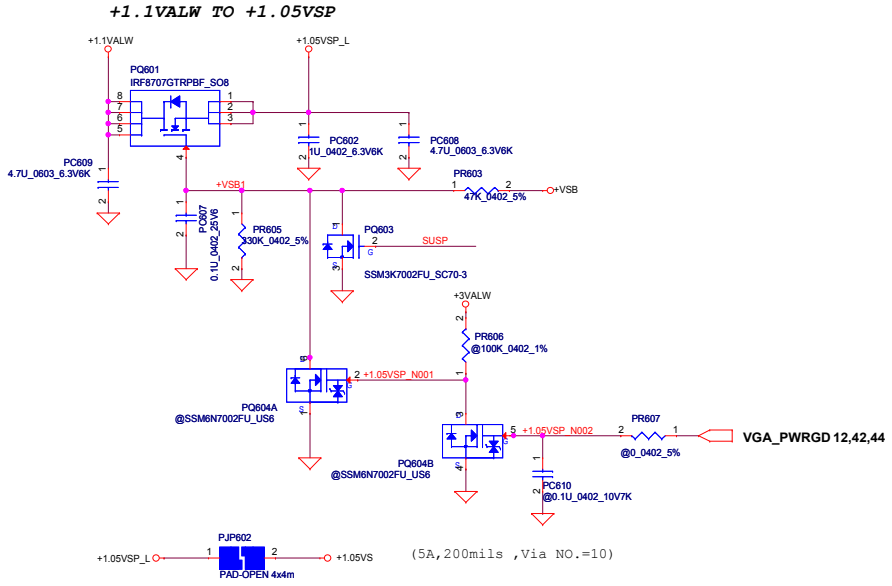
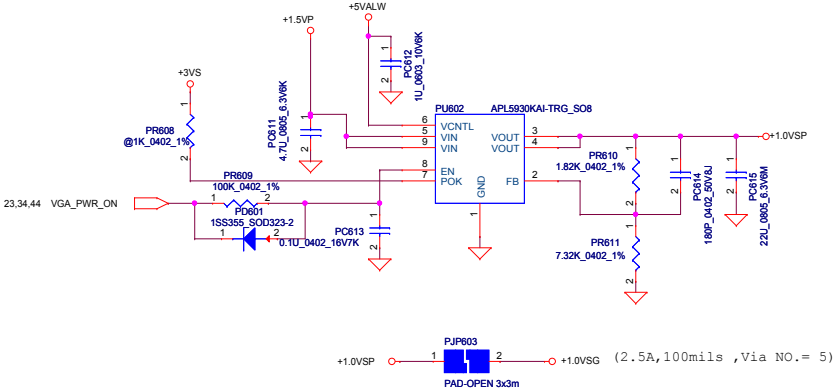




Need to confirm with HW power sequence.



Security Classification	Compal Secret Data		
Issued Date	2006/11/23	Deciphered Date	2007/11/23

Compal Electronics, Inc.

Title: **PWR 0.75VSP +1.05VSP**

Size	Document Number	Rev
	LAXXXX	0.22

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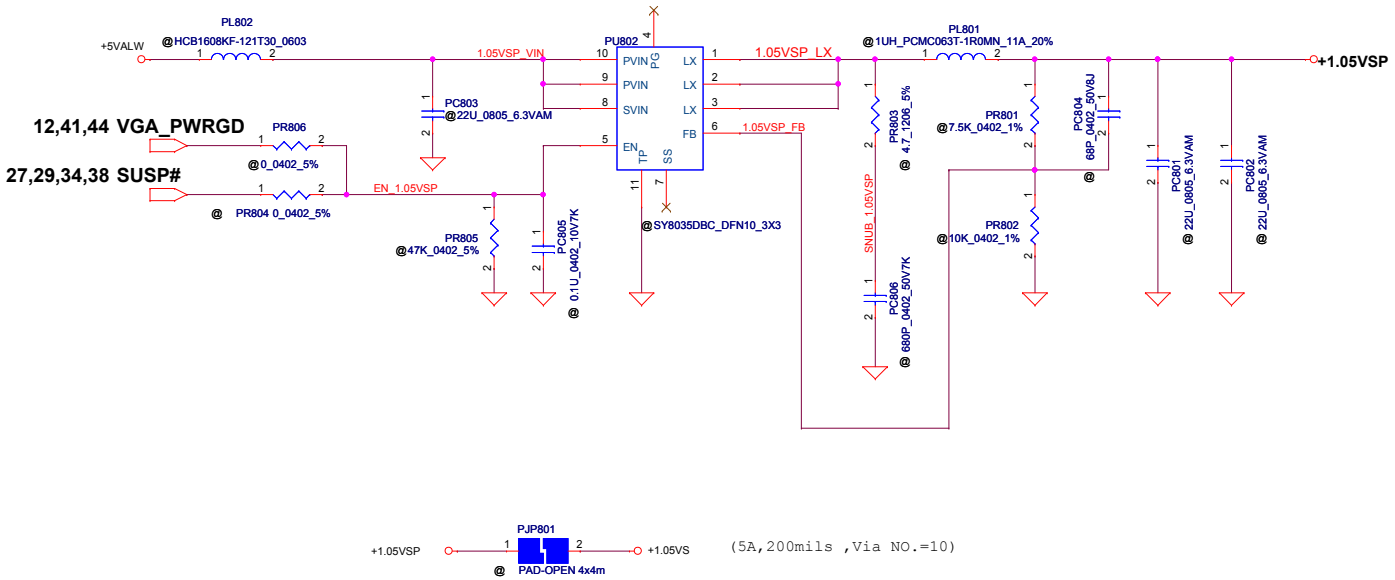


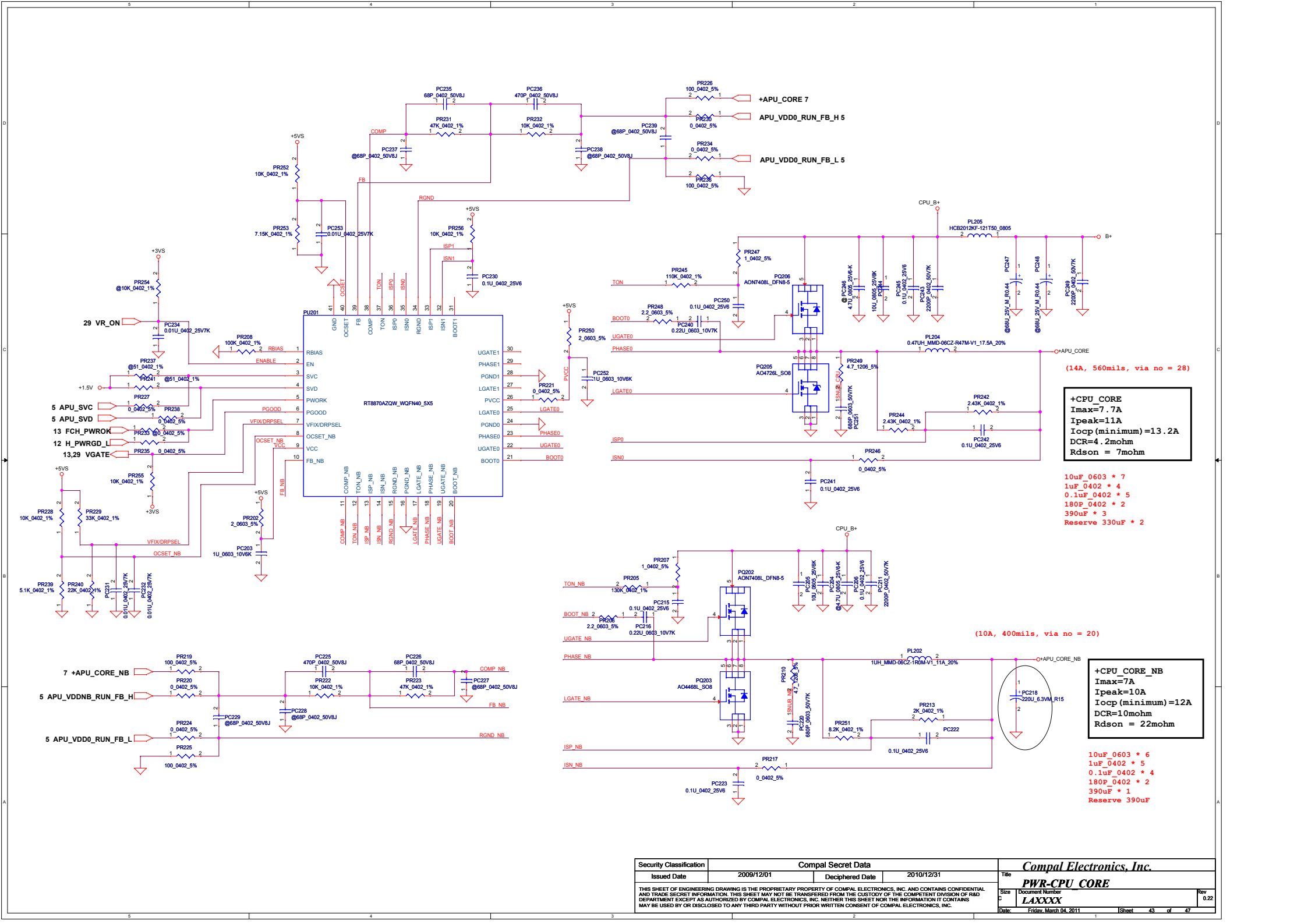
Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

Compal Electronics, Inc.

Title: **+1.8VSP**

Size	Document Number	Rev
	NCL61 LA-6321P M/B	0.22

Date: Friday, March 04, 2011 | Sheet 42 of 47



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR-CPU_CORE			
Size: C	Document Number: LAXXXX		Rev: 0.22
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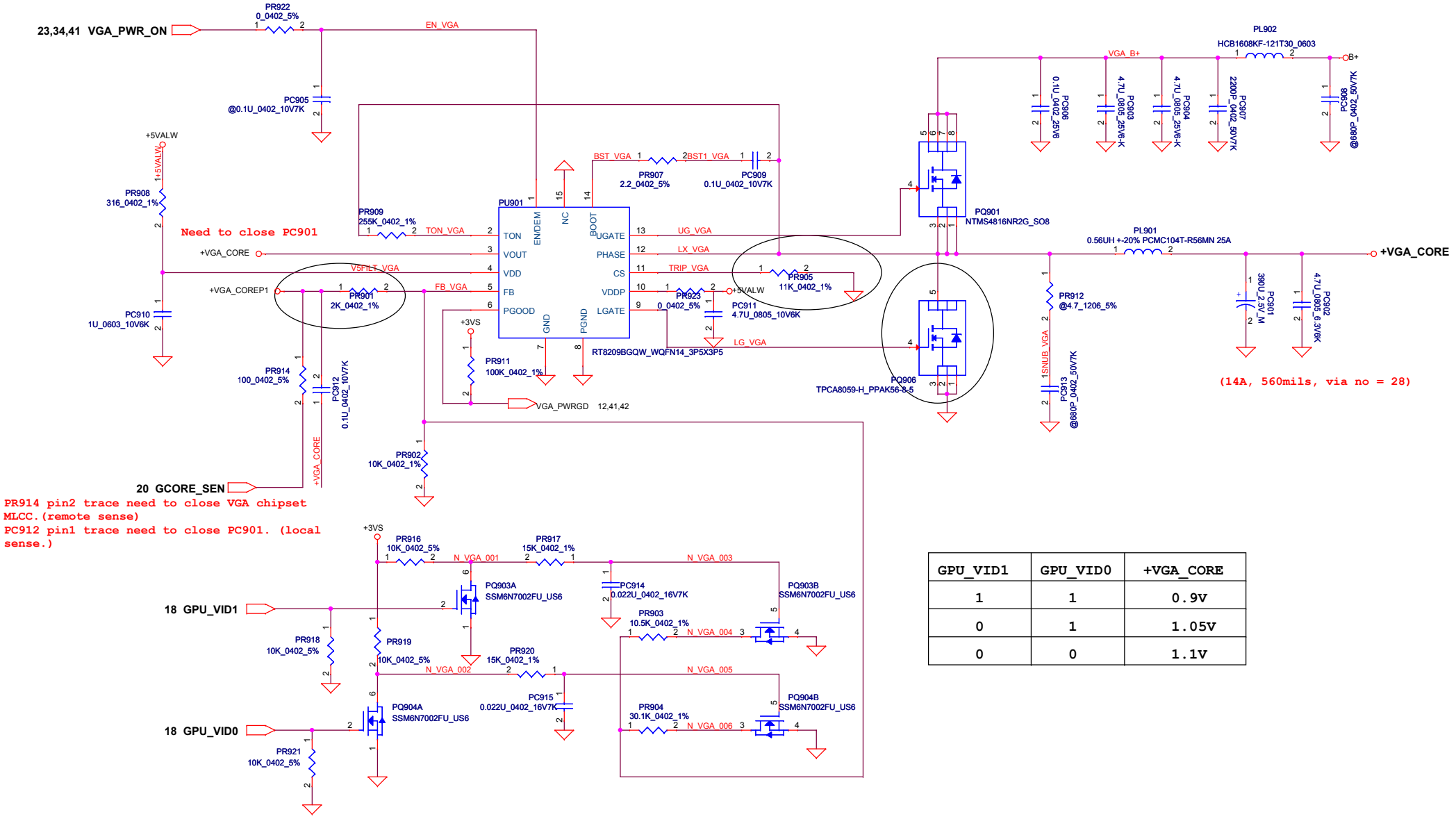

GPU_VID1	GPU_VID0	+VGA_CORE
1	1	0.9V
0	1	1.05V
0	0	1.1V

Security Classification	Compal Secret Data		
Issued Date	2007/05/29	Deciphered Date	200810/11

Compal Electronics, Inc.			
Title: VGA_CORE			
Size	Document Number: LAXXXX		Rev: 0.22
Date: Friday, March 04, 2011		Sheet 44 of 47	

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					

Compal Electronics, Inc.
Title: Changed-List History
Size: Document Number: LA-4902P Rev: 0.22
Date: Friday, March 04, 2011 Sheet 45 of 47

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		DFB request	0.11	PG#10	change JLVDS1 connector to 40 pin and add JCM1 6pin	12/17	ER
2		EC remove ext crystal	0.11	PG#29	Add R1787 and C1677	12/17	ER
3		DFB request for soldering	0.11	PG#30 PG#33	Change JTP1 and JBTN1 footprint	12/17	ER
4		JUSB2 no function	0.11	PG#31	Update JUSB2 symbol	12/17	ER
5		LID issue	0.11	PG#13	R930 change to pop	12/17	ER
6		LID issue	0.11	PG#29	LID_SW# added a pull up 10Kohm. (R35)	12/17	ER
7		Update Broad ID	0.11	PG#29	Change R1606 to 154Kohm	12/17	ER
8		for BIOS crisis	0.12	PG#14	Add U11	12/17	ER
9		DDR3 SPD	0.12	PG#8	Reserve R152 , R155	12/17	ER
10		For discharge spec	0.13	PG#24	Add R1788 and Q113 discharge schematic	12/17	ER
11		For EMI test	0.2	PG#11	Remove Level Shifter schematic	12/17	ER
12		BIOS change to share ROM	0.2	PG#16 PG#29	Pop R594 and R602 , unpop R601 and R550 change U48 meterial	12/17	ER
13		Fix S3 resume black screen	0.21	PG#6	Add R1790 , R1791 68ohm pull down	02/18	PR
14		DFX request	0.21	PG#11	Update JDIMM2 fooprint	02/18	PR
15		Fix S3 resume too long	0.21	PG#18	Add R1795 1M ohm	02/18	PR
16		Fix assembly issue	0.21	PG#29 PG#25	Update JKB1 and JAU1 footprint for ME connector	02/18	PR
17		EMI request	0.22	PG#11	pop L11~L14	02/22	PR
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							

Compal Electronics, Inc.

Title: HW-PIR

Size: Custom | Document Number: LA-7323P | Rev: 0.22

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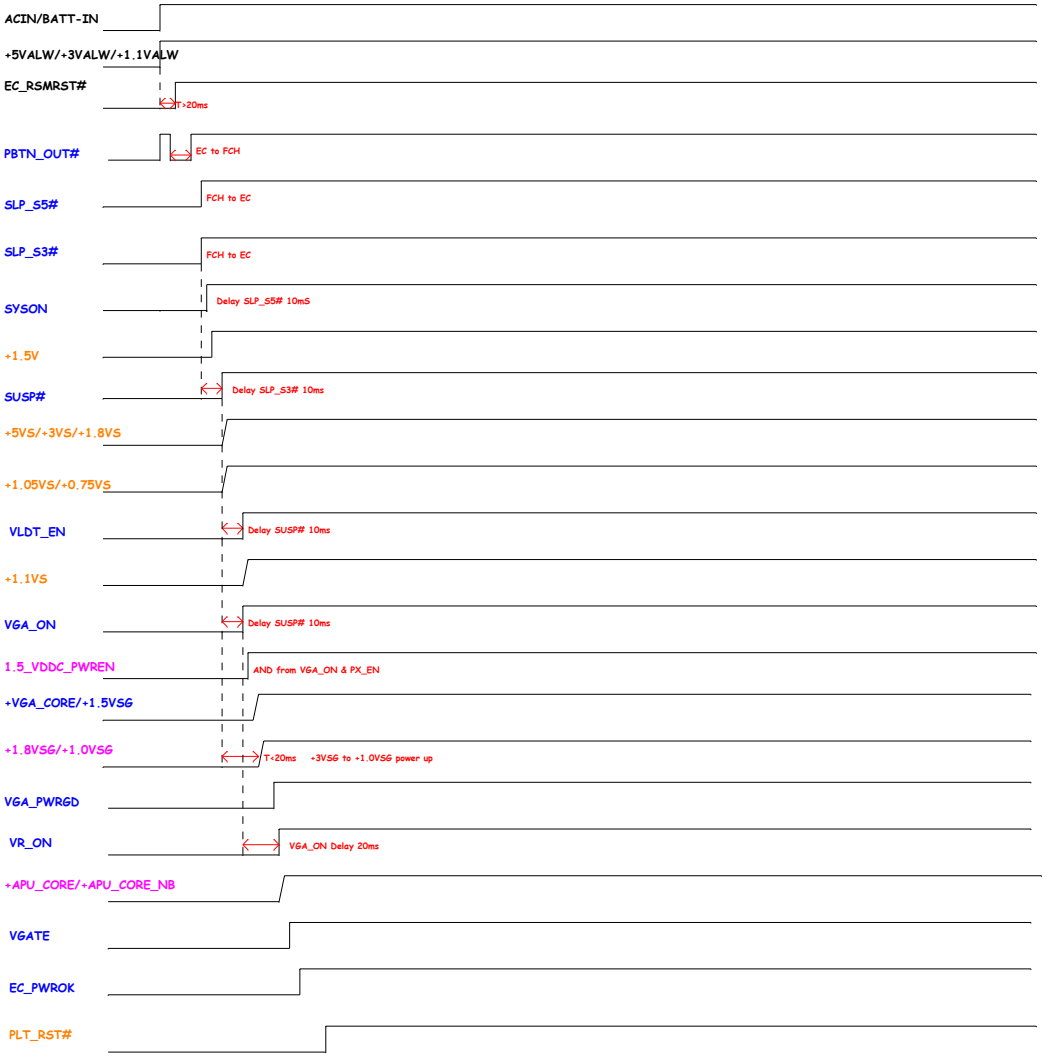
POWER SEQUENCE



Security Classification	Compal Secret Data		
Issued Date	2010/09/30	Deciphered Date	2010/12/31

Title	Power Sequence		
Size	Document Number		Rev
	LA-7323P		0.xx
Date:	Monday, March 07, 2011	Sheet	of