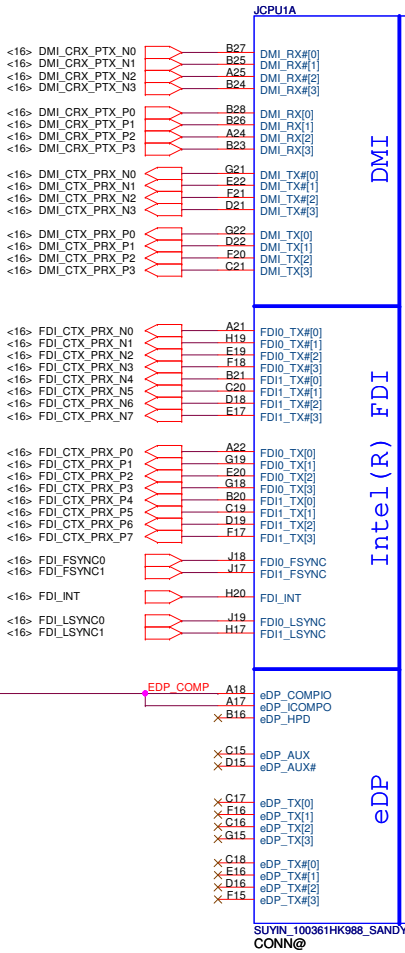
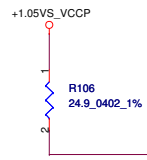
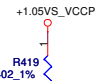
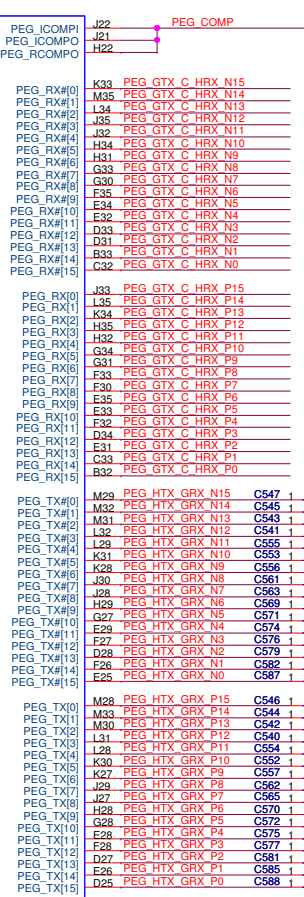


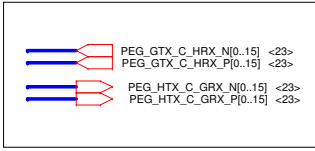
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



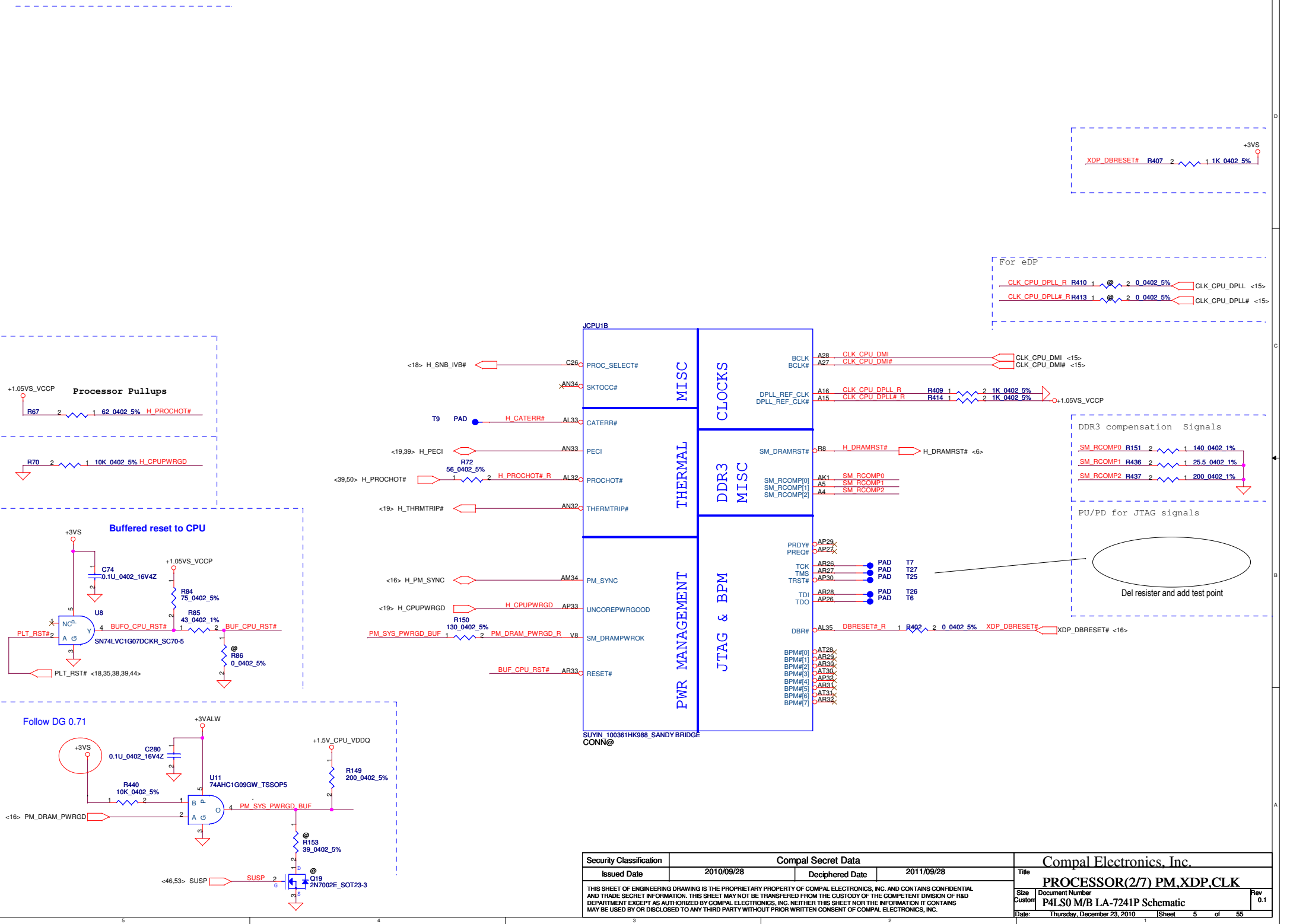
PCI EXPRESS* - GRAPHICS



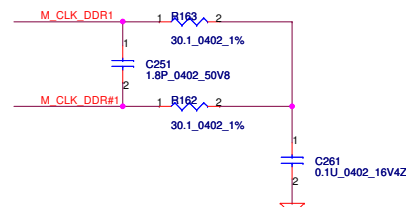
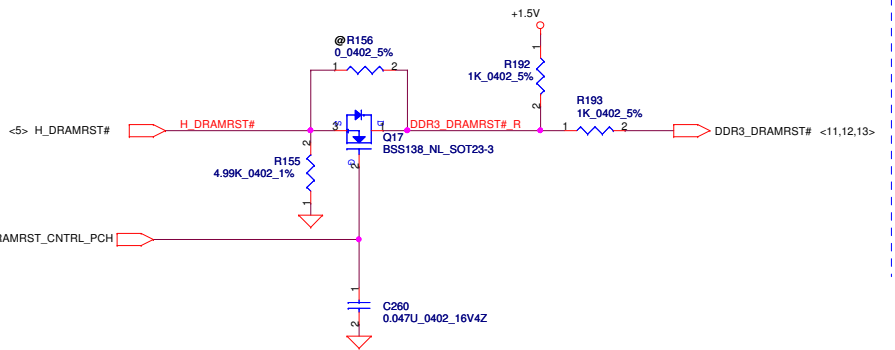
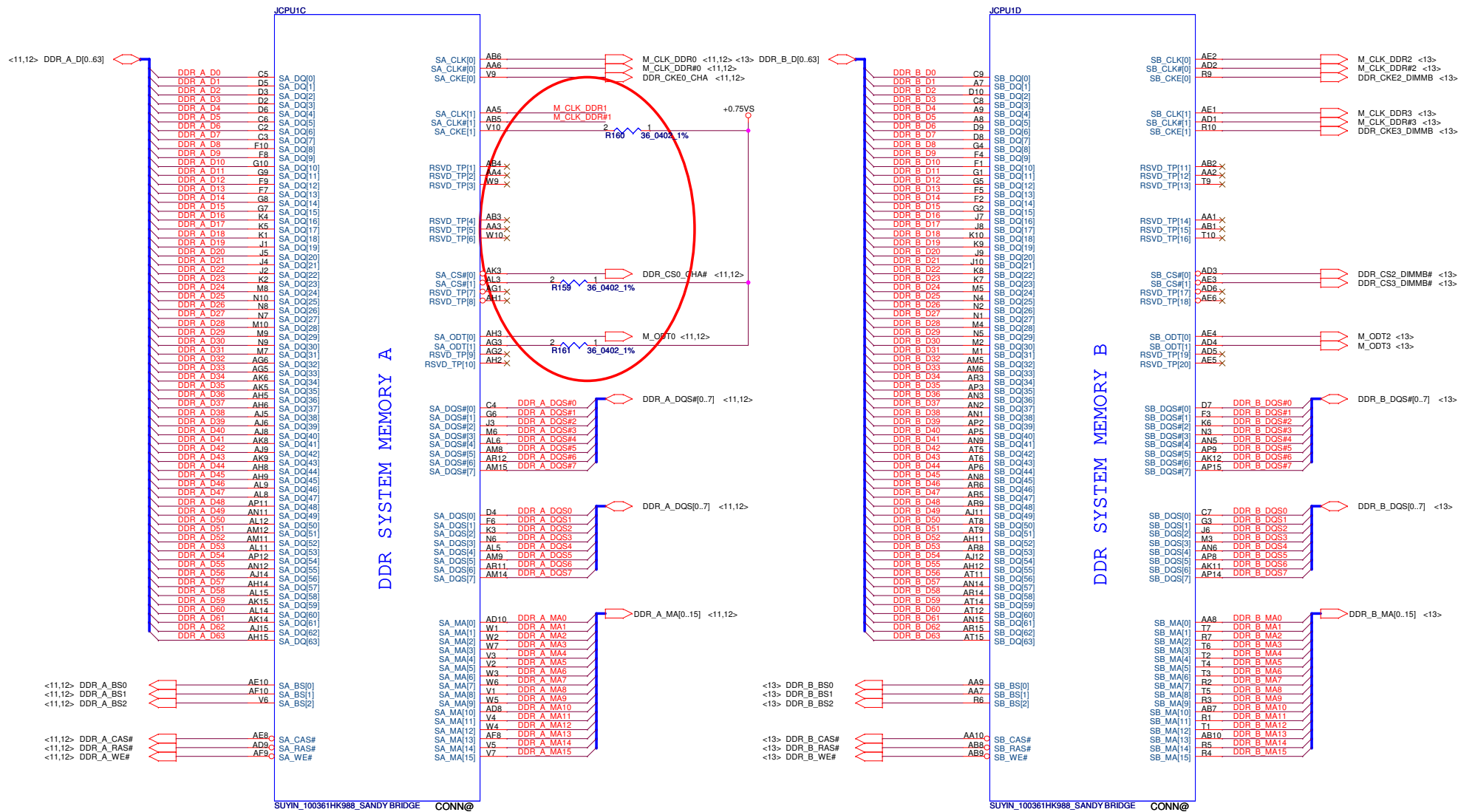
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



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Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title	
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Size		Document Number		Rev	
Custont		P4LS0 M/B LA-7241P Schematic		0.1	
Date:		Thursday, December 23, 2010		Sheet 4 of 55	

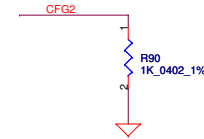


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Issued Date		2010/09/28		Deciphered Date		2011/09/28		Title					
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						Size		Document Number		P4LS0 M/B LA-7241P Schematic		Rev 0.1	
						Custom							
Date:						Thursday, December 23, 2010		Sheet 5 of 55					

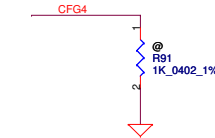


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(3/7) DDRIII
Size	Document Number	Customer	P4L50 M/B LA-7241P Schematic	Rev 0.1
Date:	Thursday, December 23, 2010	Sheet	6	of 55

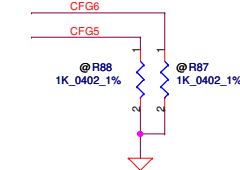
CFG Straps for Processor



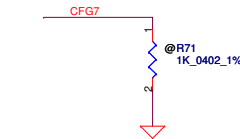
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

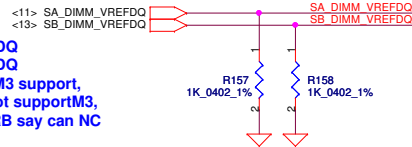


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

AJ31 change to VAXG_VAL_SENSE
AH31 change to VSSAXG_VAL_SENSE
AJ33 change to VCC_VAL_SENSE
AH33 change to VSS_VAL_SENSE

RSVD6 and RSVD7 had changed to
SA_DIMM_VREFDQ and SB_DIMM_VREFDQ

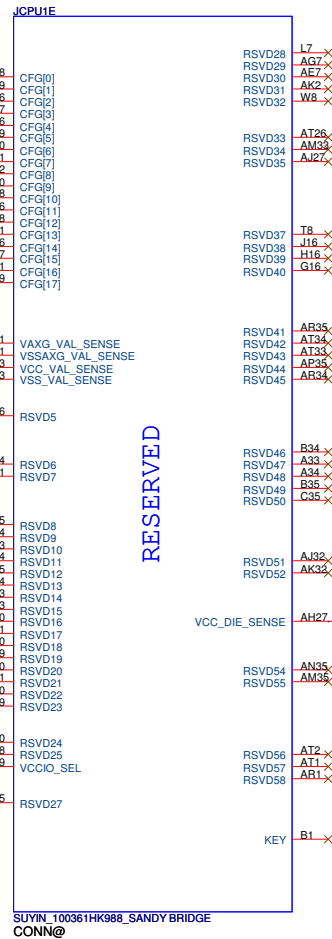
SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandy bridge not support M3,
Check list1.0&CRB say can NC

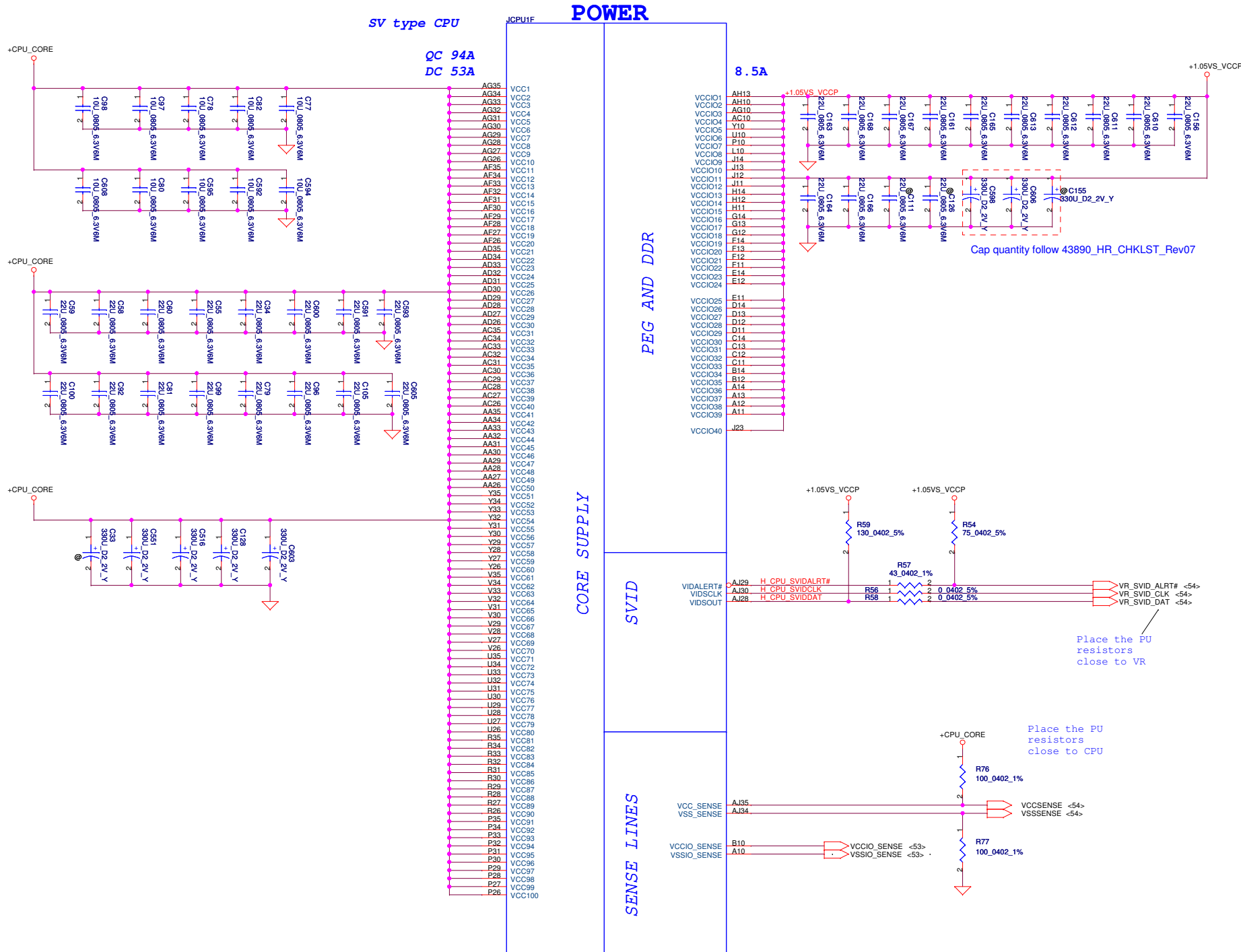


VCCIO_SEL	
A19	* 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

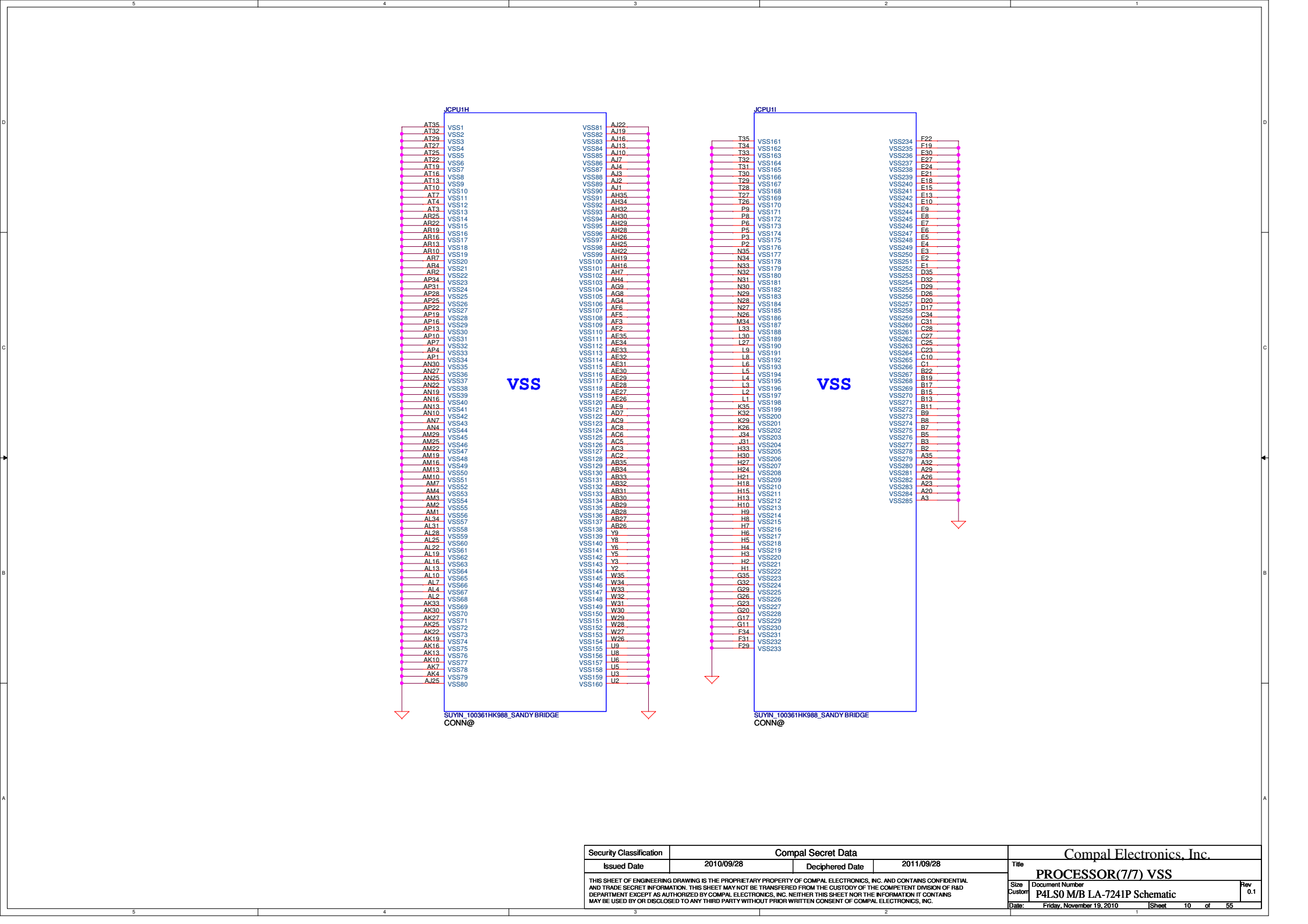
VCCIO_SEL For 2012 CPU support
RSVD26 had changed the name to VCCIO_SEL
Need PH +3VS 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

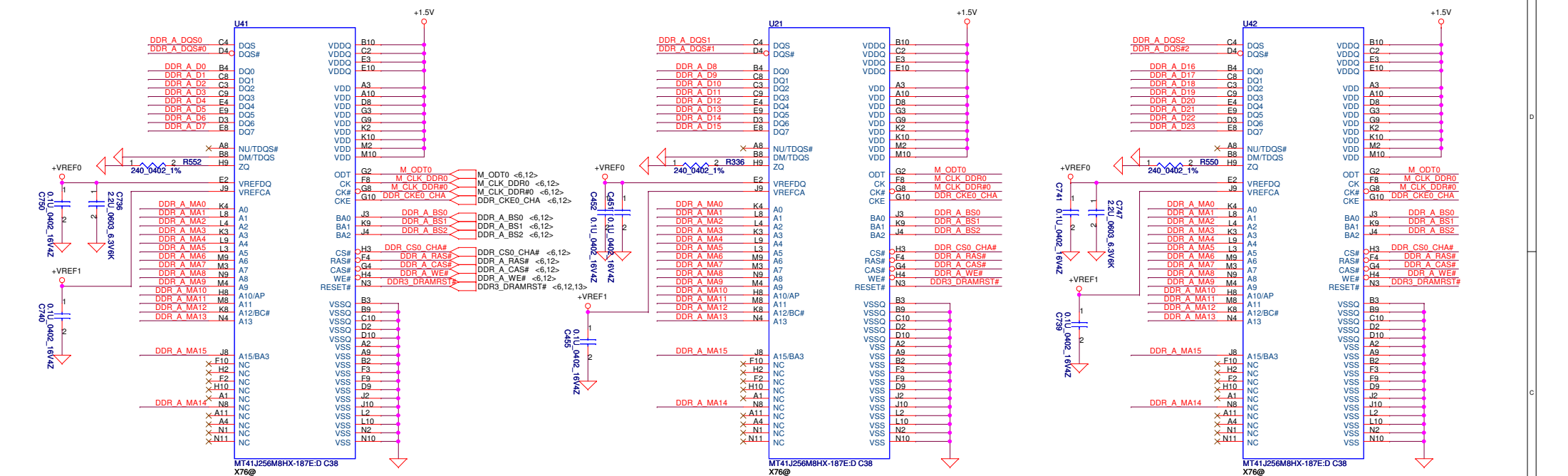
RESERVED



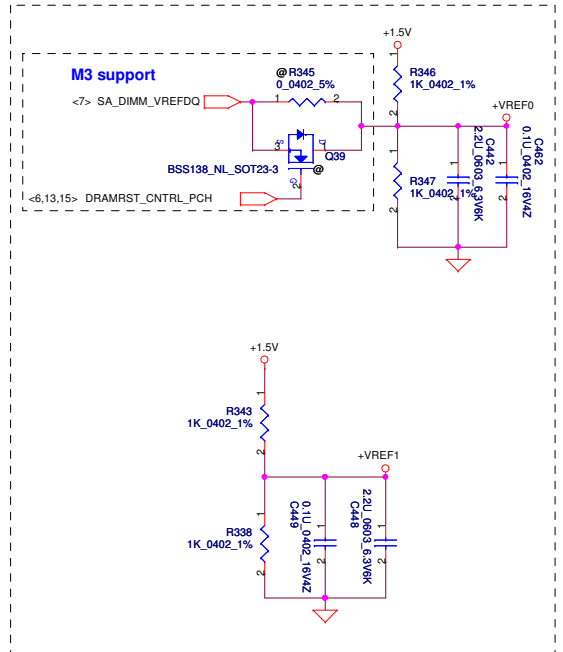
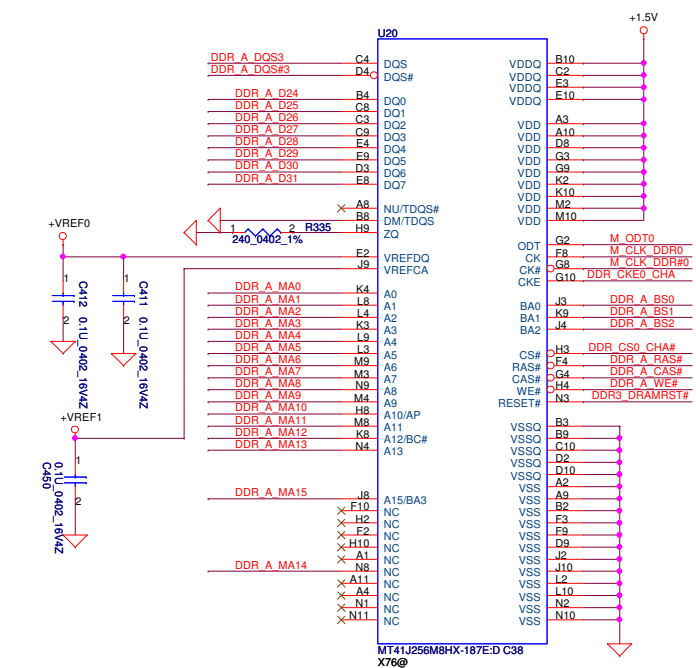


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/09/28				PROCESSOR(5/7) PWR,BYPASS			
Deciphered Date				2011/09/28				P4LS0 M/B LA-7241P Schematic			
Title				Date				Thursday, December 23, 2010			
Size				Document Number				Rev			
Custom				P4LS0 M/B LA-7241P Schematic				0.1			
Sheet				8				of 55			

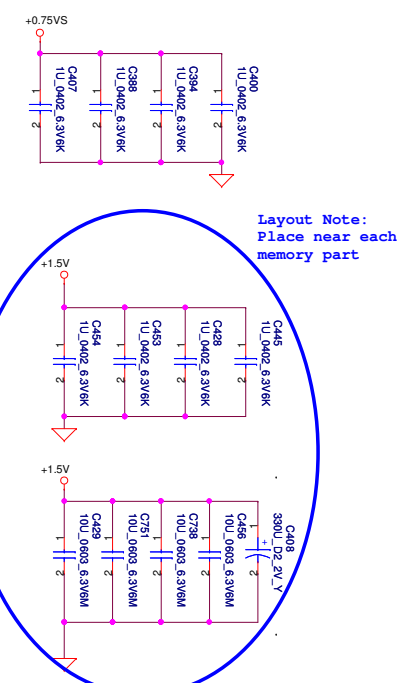
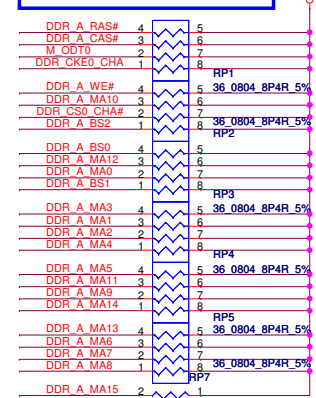




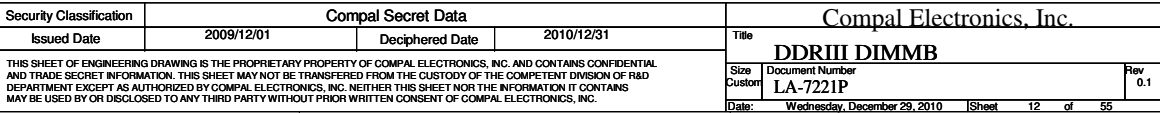
<6,12> DDR_A_MA[0..15] **DDR A MA[0..15]**
<6> DDR_A_DQS#[0..3] **DDR A DQS#0..3]**
<6> DDR_A_DQS[0..3] **DDR A DQS0..3]**
<6> DDR_A_DQ[0..31] **DDR A DQ0..31]**

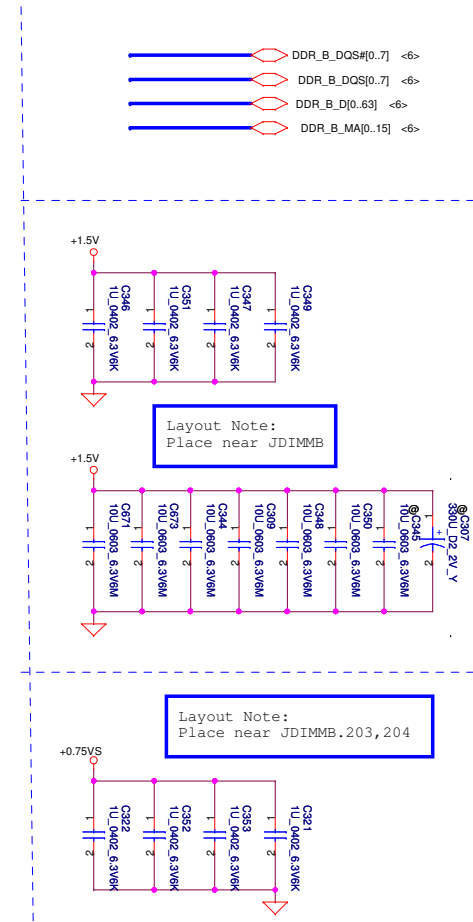


Layout Note:
Place near JDIMM1.203,204



Layout Note:
Place near each memory part





- All VREF traces should have 10 mil trace width

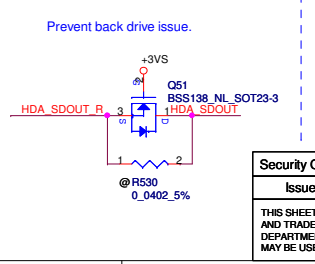
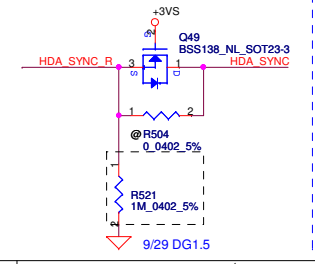
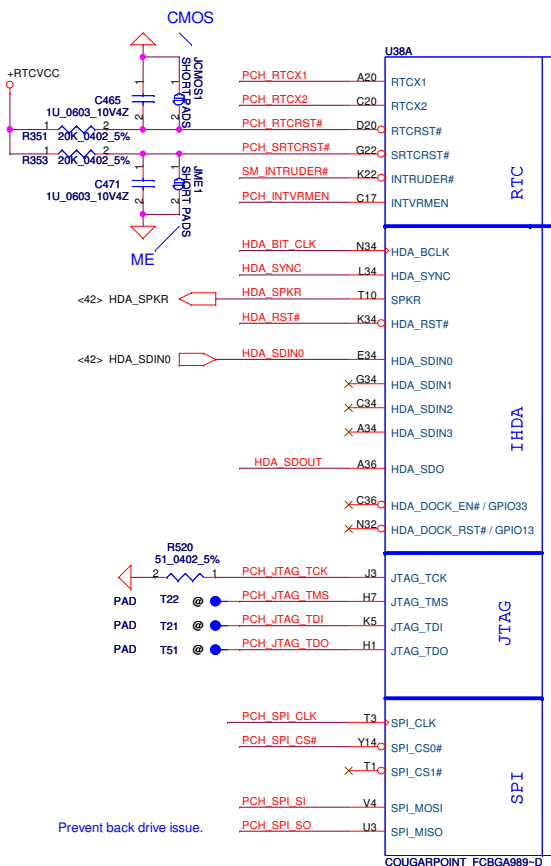
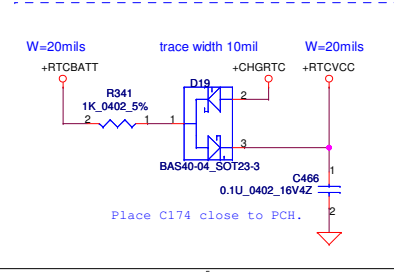
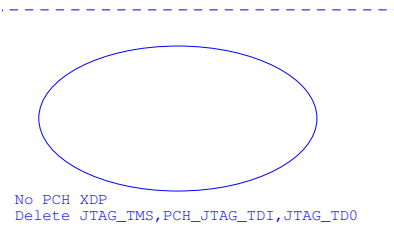
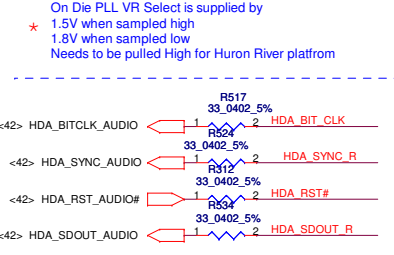
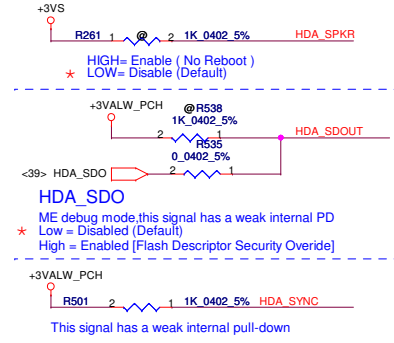
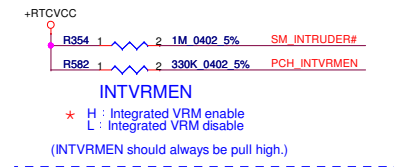
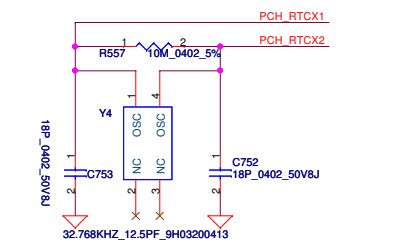
Layout Note:
Place near JDIMMB

Layout Note:
Place near JDIMMB.203,204

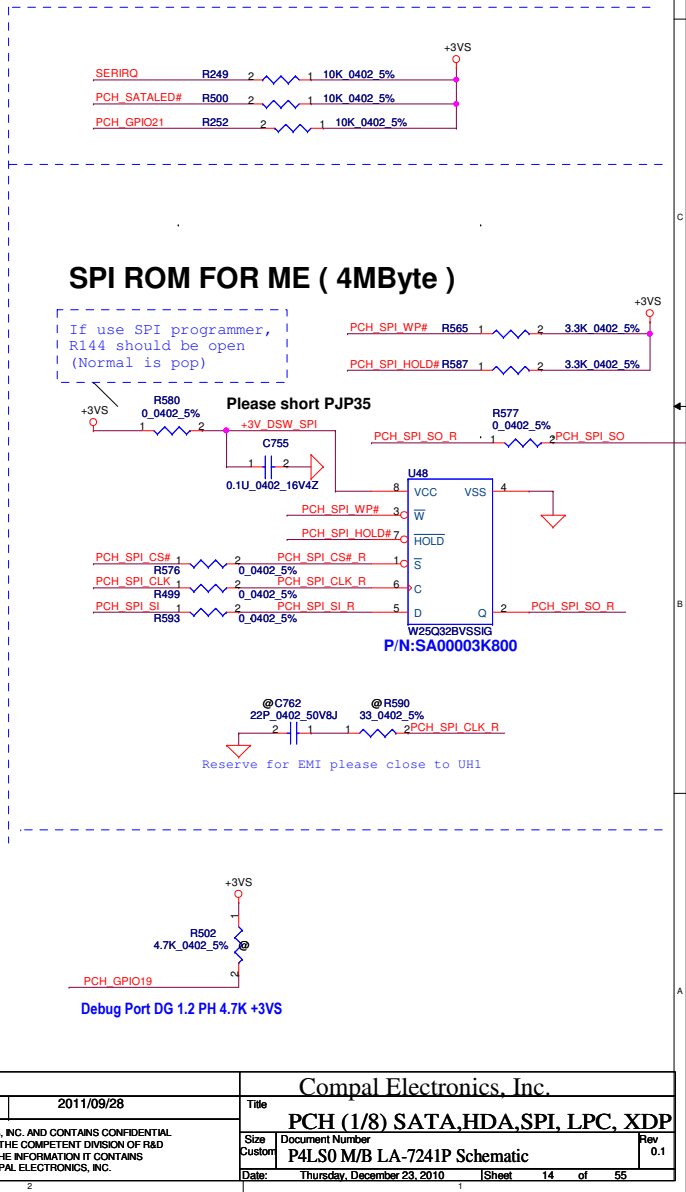
<Address: 01>

DIMM_B Reverse type H:4mm

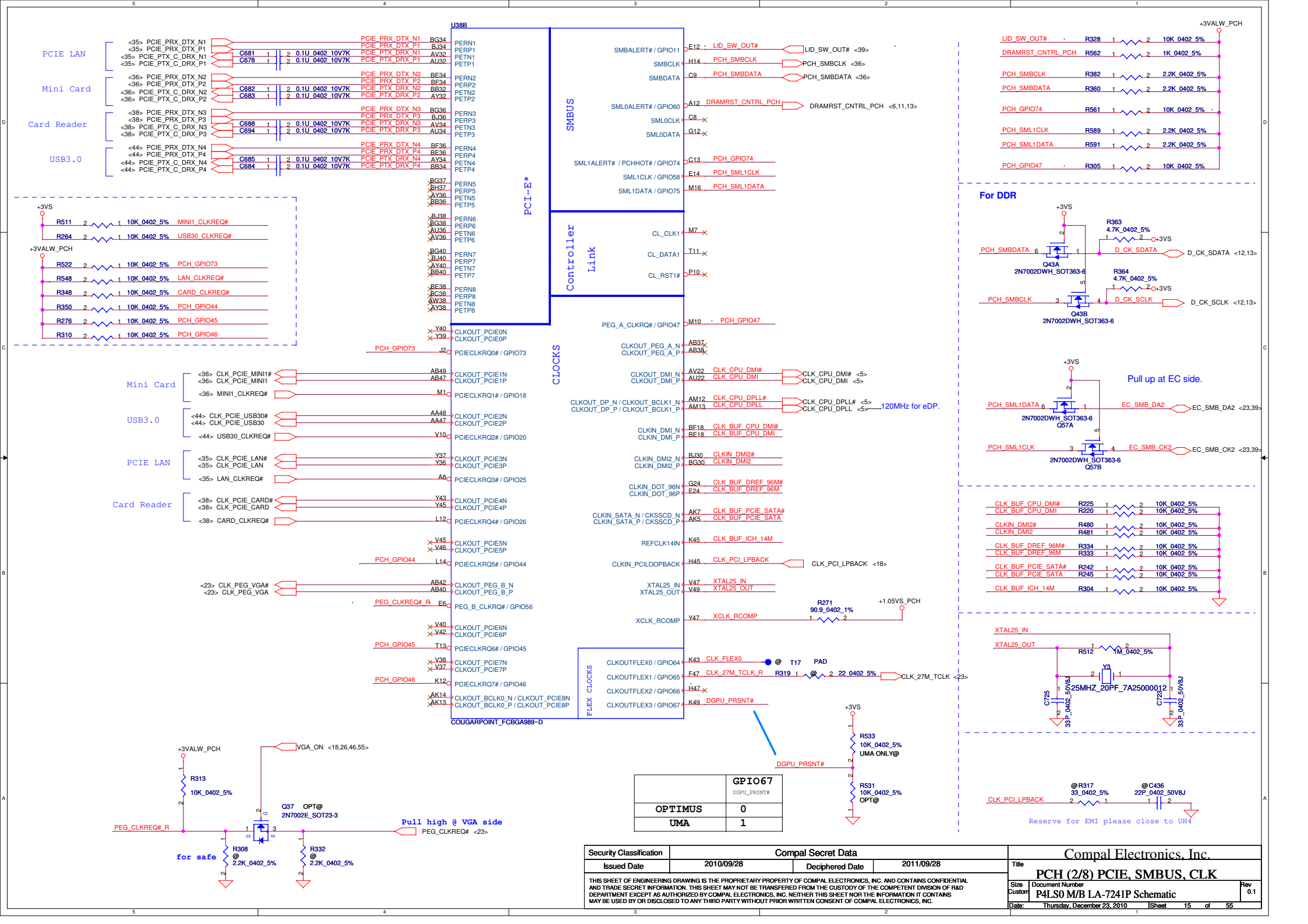
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title	DDRIII DIMMB	
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				Custom	P4L50 M/B LA-7241P Schematic	0.1
				Date:	Thursday, December 23, 2010	Sheet 13 of 55

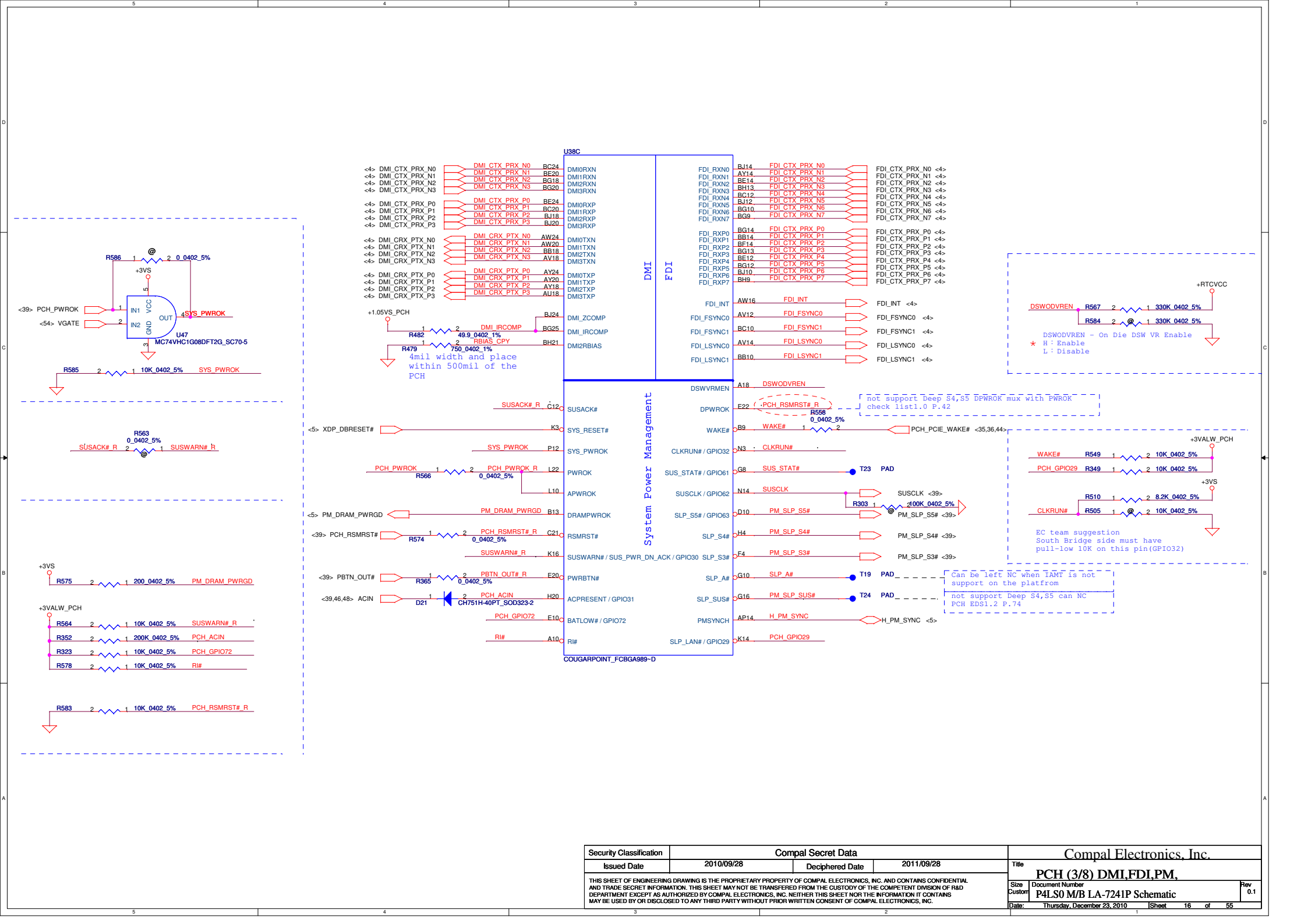


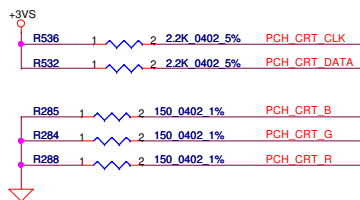
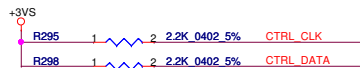
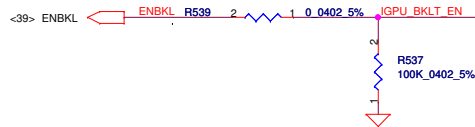
Security Classification		Compal Secret Data	
Issued Date	2010/09/28	Deciphered Date	2011/09/28
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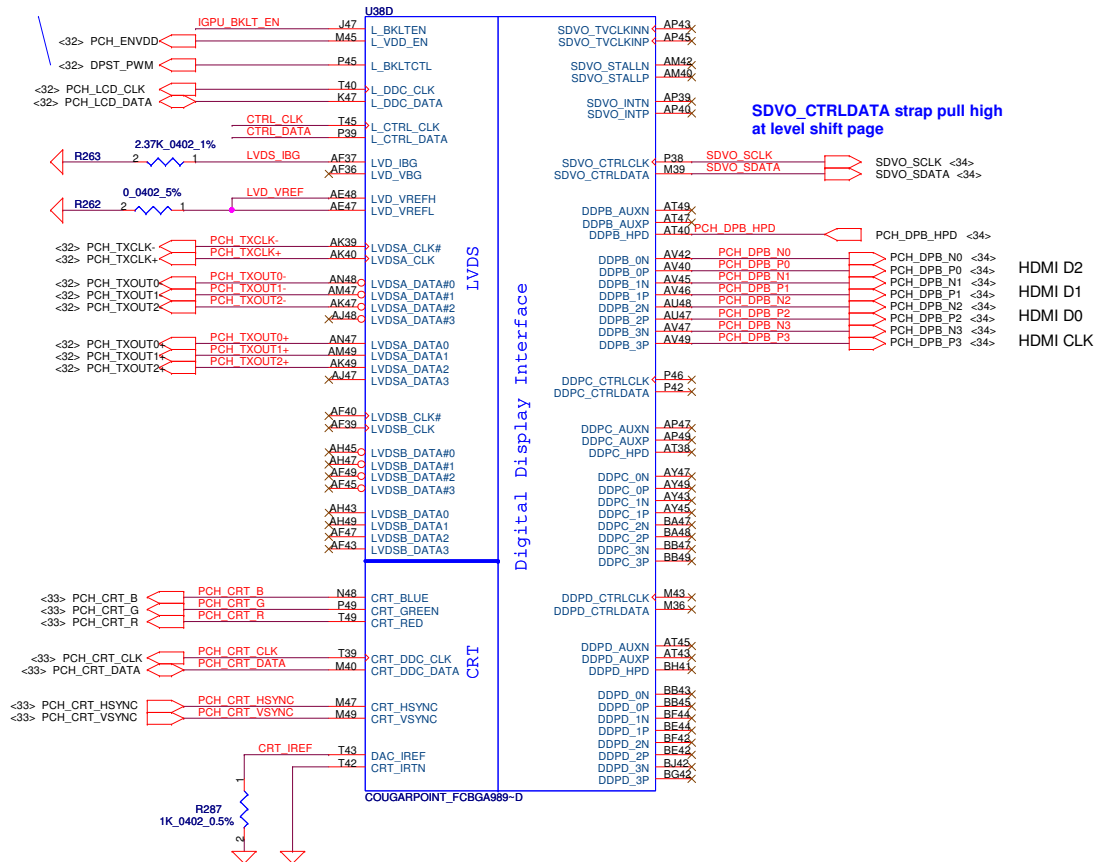
Compal Electronics, Inc.	
PCH (1/8) SATA,HDA,SPI, LPC, XDP	
Title	Document Number
Size	P4LS0 M/B LA-7241P Schematic
Date	Thursday, December 23, 2010
Sheet	14 of 55
Rev	0.1



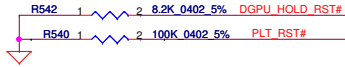
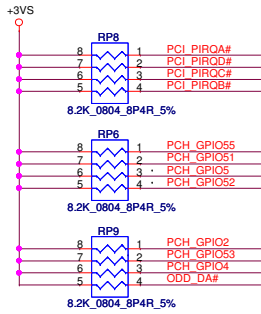




Pull high at LVDS conn side.



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Size		Document Number		Rev	
Custom		P4LS0 M/B LA-7241P Schematic		0.1	
Date:		Thursday, December 23, 2010		Sheet 17 of 55	

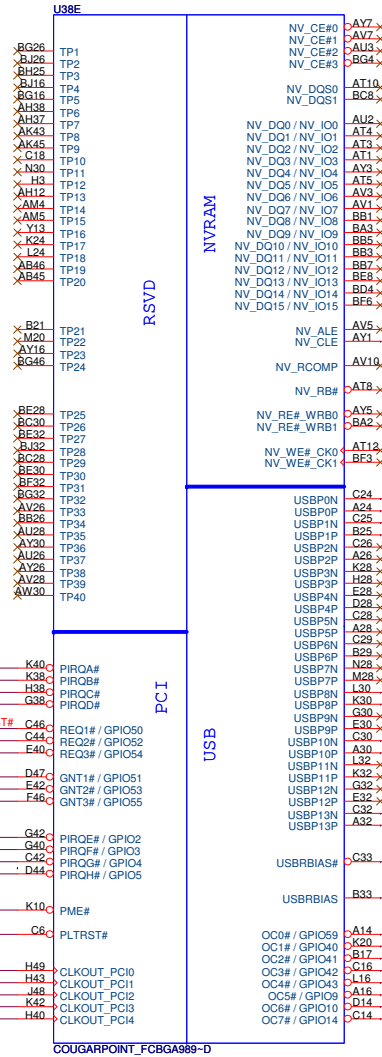
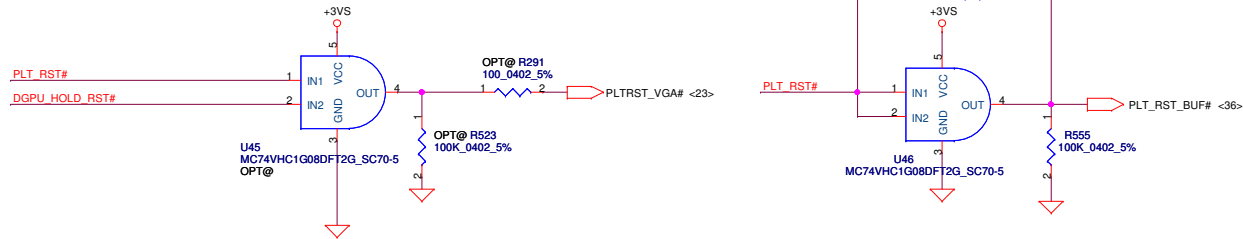


Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	PCI
	1	1	SPI
	0	0	LPC

<15> CLK_PCL_LPBK#
<39> CLK_PCL_LPC

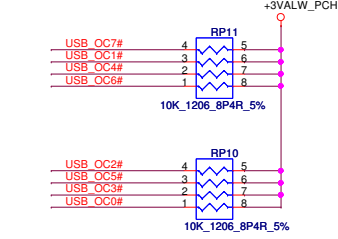
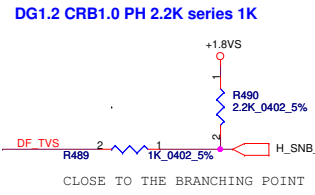
PIRQA# K40
PIRQB# K38
PIRQC# H38
PIRQD# G38
DGPU_HOLD_RST# C46
PCH_GPIO52 C46
VGA_ON E40
PCH_GPIO51 D47
PCH_GPIO53 E42
PCH_GPIO55 F46
<15,26,46,55> VGA_ON
<35> ODD_DA#
PCH_GPIO2 G42
ODD_DA# G40
PCH_GPIO4 C42
PCH_GPIO5 D44
PCH_GPIO55 F46
PME# K10
PLTRST# C6
<5,35,38,39,44> PLT_RST#

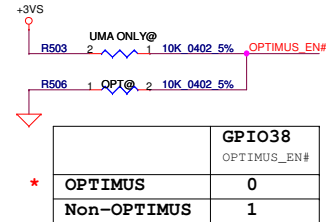
CLK_PCL_LPBK# R316 2 22 0402 5% CLK_PCL0 H49
CLK_PCL_LPC R309 1 22 0402 5% CLK_PCL1 H43
CLK_PCL2 J48
CLK_PCL3 K42
CLK_PCL4 H40
PXD T16 @
PAD T20 @



USB20_N0 <37>
USB20_P0 <37>
USB20_N1 <37>
USB20_P1 <37>
USB20_N8 <36>
USB20_P8 <36>
USB20_N10 <32>
USB20_P10 <32>
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USB20_P13 <37>
USB_OC0# <37>
USB_OC1# <37>
USB_OC2# <37>
USB_OC3# <37>
USB_OC4# <37>
USB_OC5# <37>
USB_OC6# <37>
USB_OC7# <37>

DMI Termination Voltage	
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

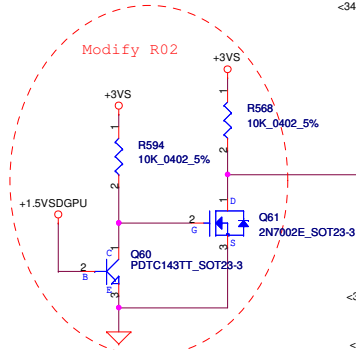
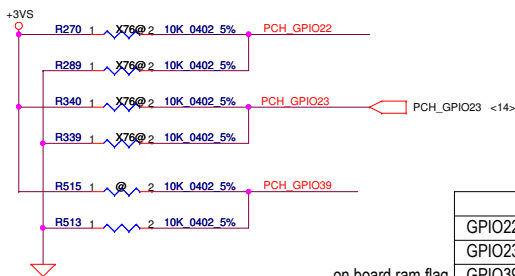
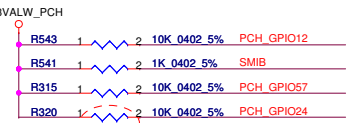
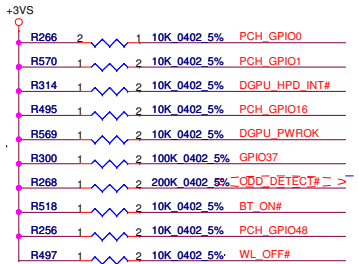
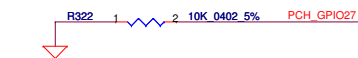
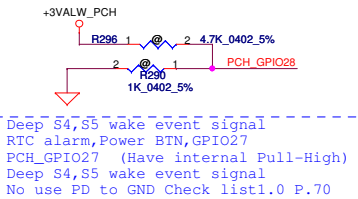




GPIO28

On-Die PLL Voltage Regulator

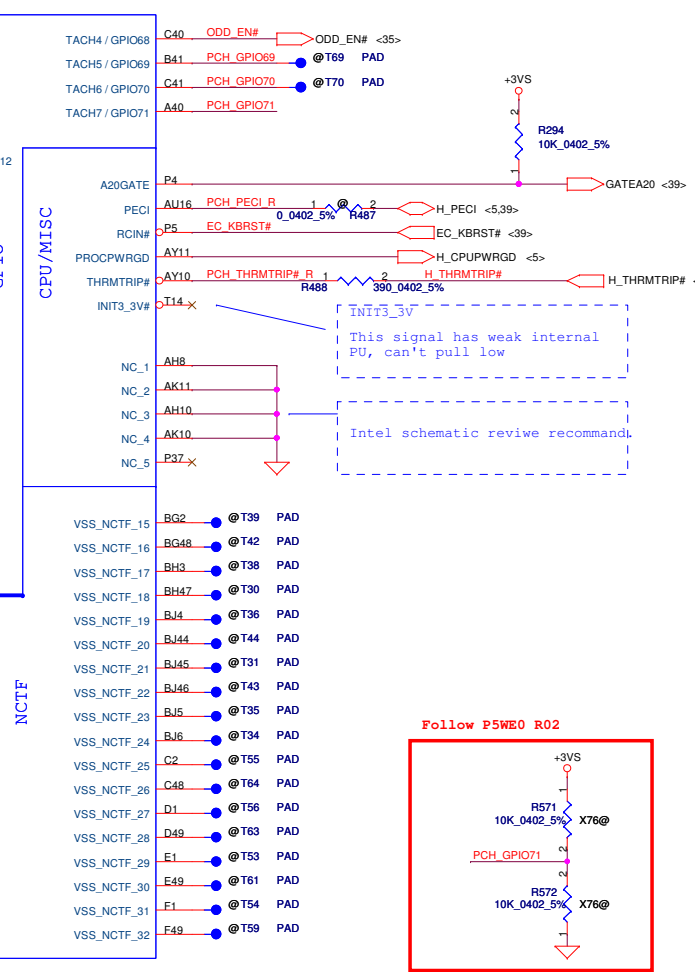
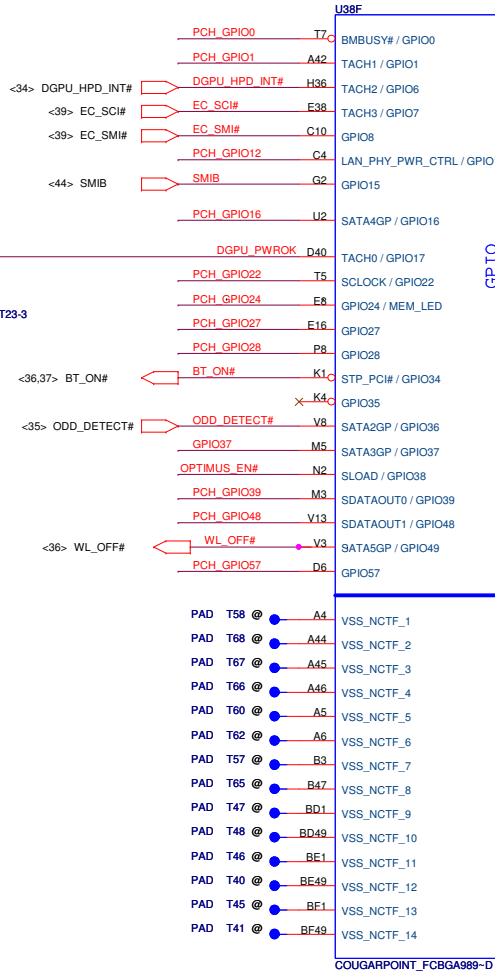
This signal has a weak internal pull up
* H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable



CRB1.0 PH200K to +3VS

CRB1.0 PH10K to +3VALW
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.

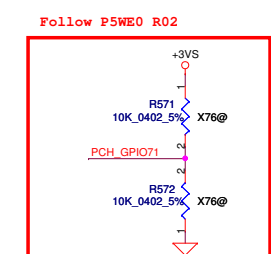
	Samsung 2G	Hynix 2G	Nanya 2G	Micron 2G
GPIO22	0	0	1	1
GPIO23	0	1	0	1
GPIO39	0	0	0	0



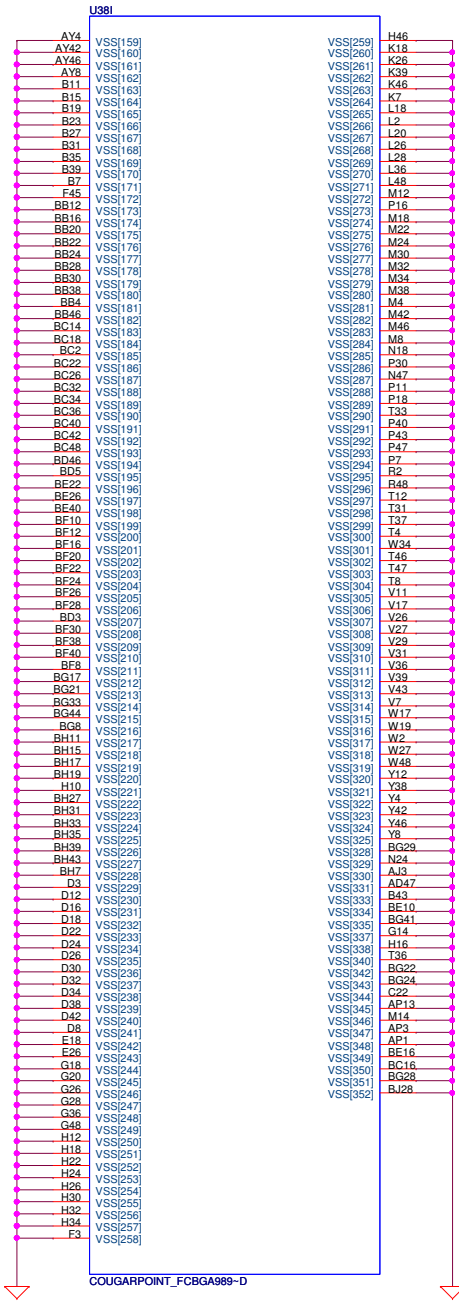
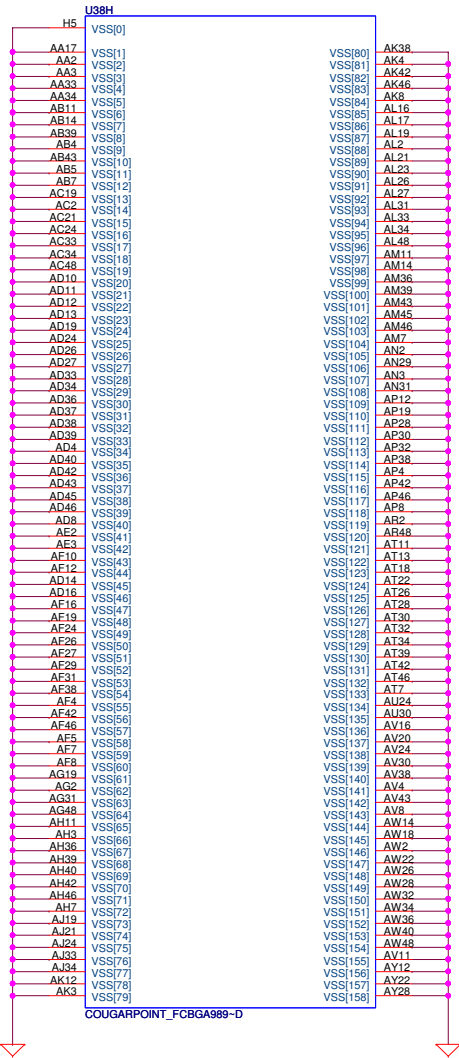
INIT3_3V

This signal has weak internal
PU, can't pull low

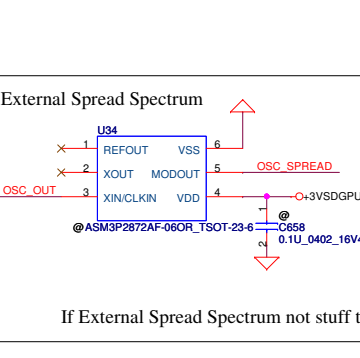
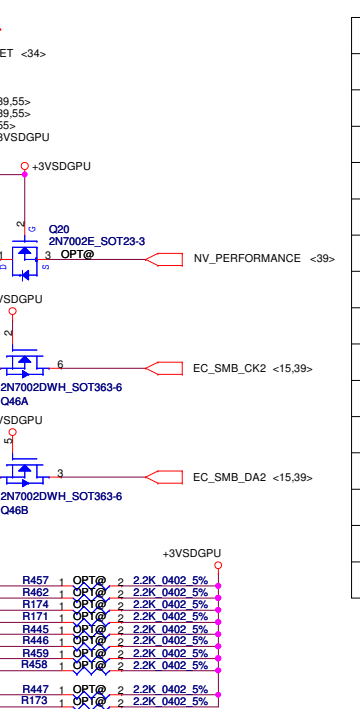
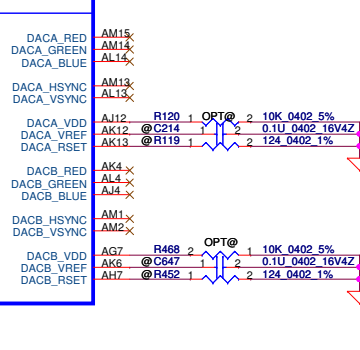
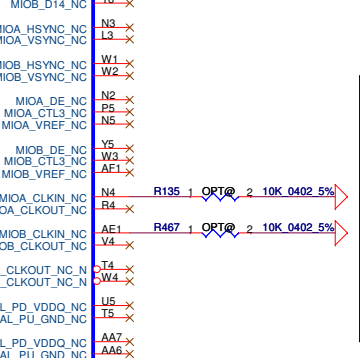
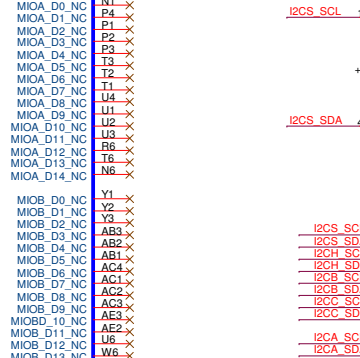
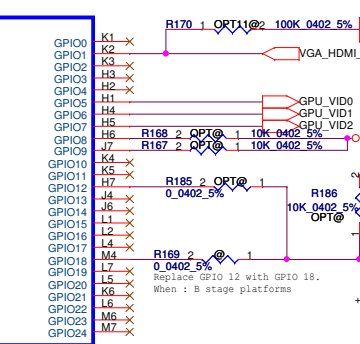
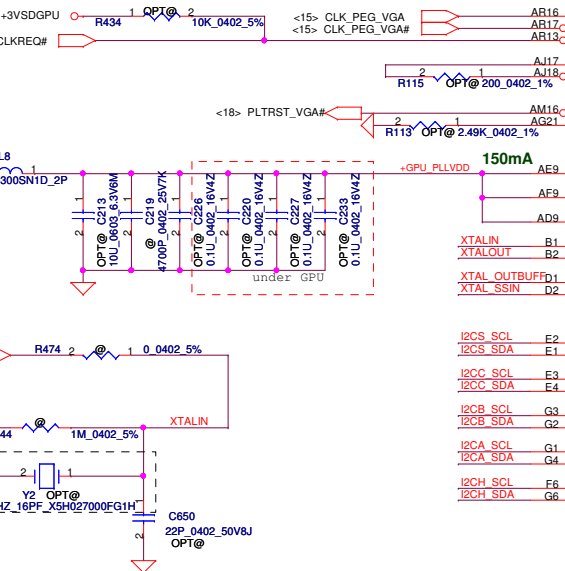
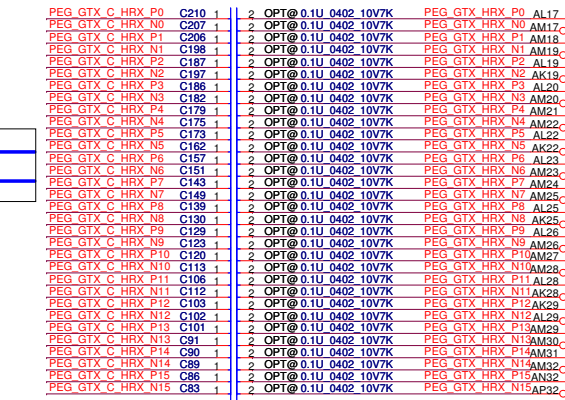
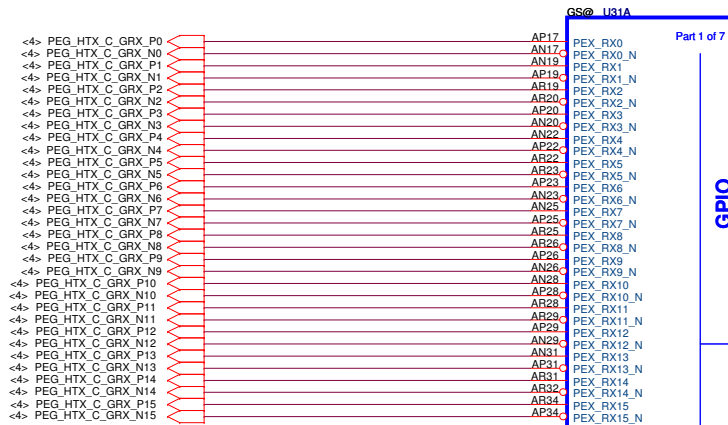
Intel schematic revise recommend



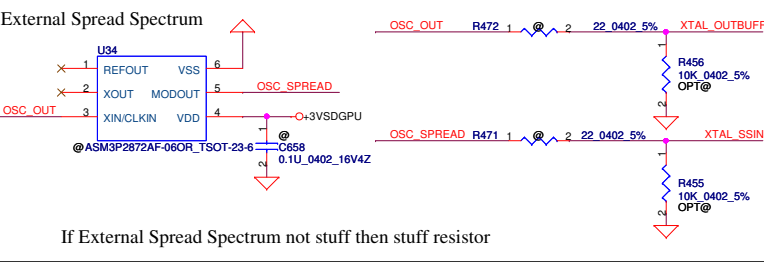
GPIO71	
PCH_GPIO71	
VRAM 800 MHz	0
VRAM 900 MHz	1



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GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	N/A
GPIO2	OUT	H	N/A
GPIO3	OUT	H	N/A
GPIO4	OUT	H	N/A
GPIO5	OUT	N/A	N/A
GPIO6	OUT	N/A	N/A
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

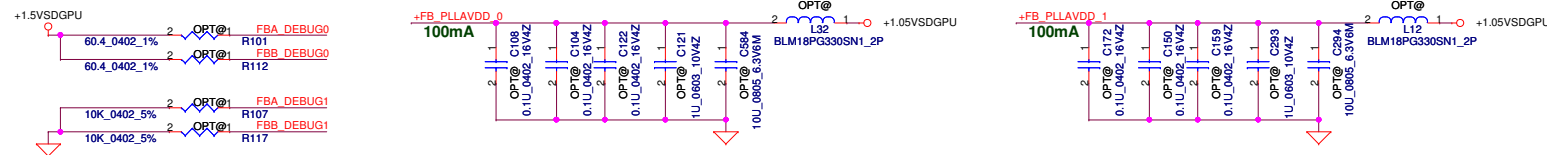
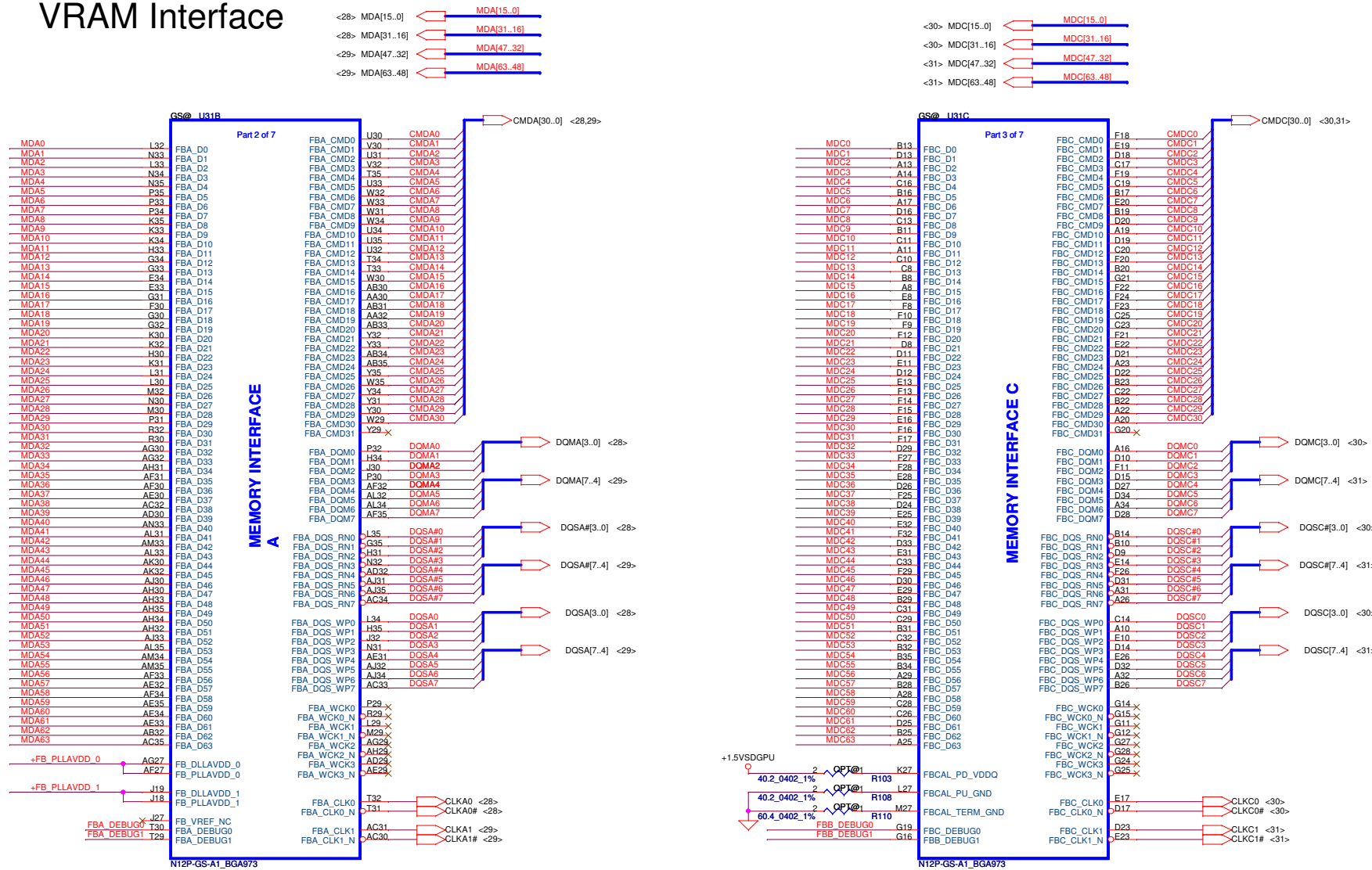


If External Spread Spectrum not stuff then stuff resistor

Option Component

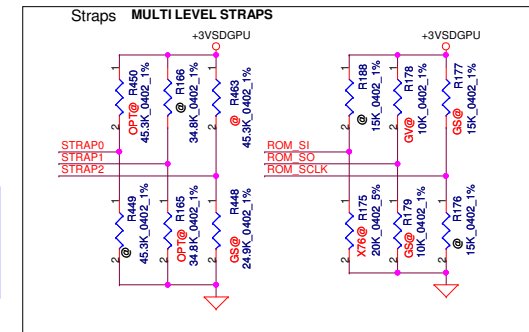
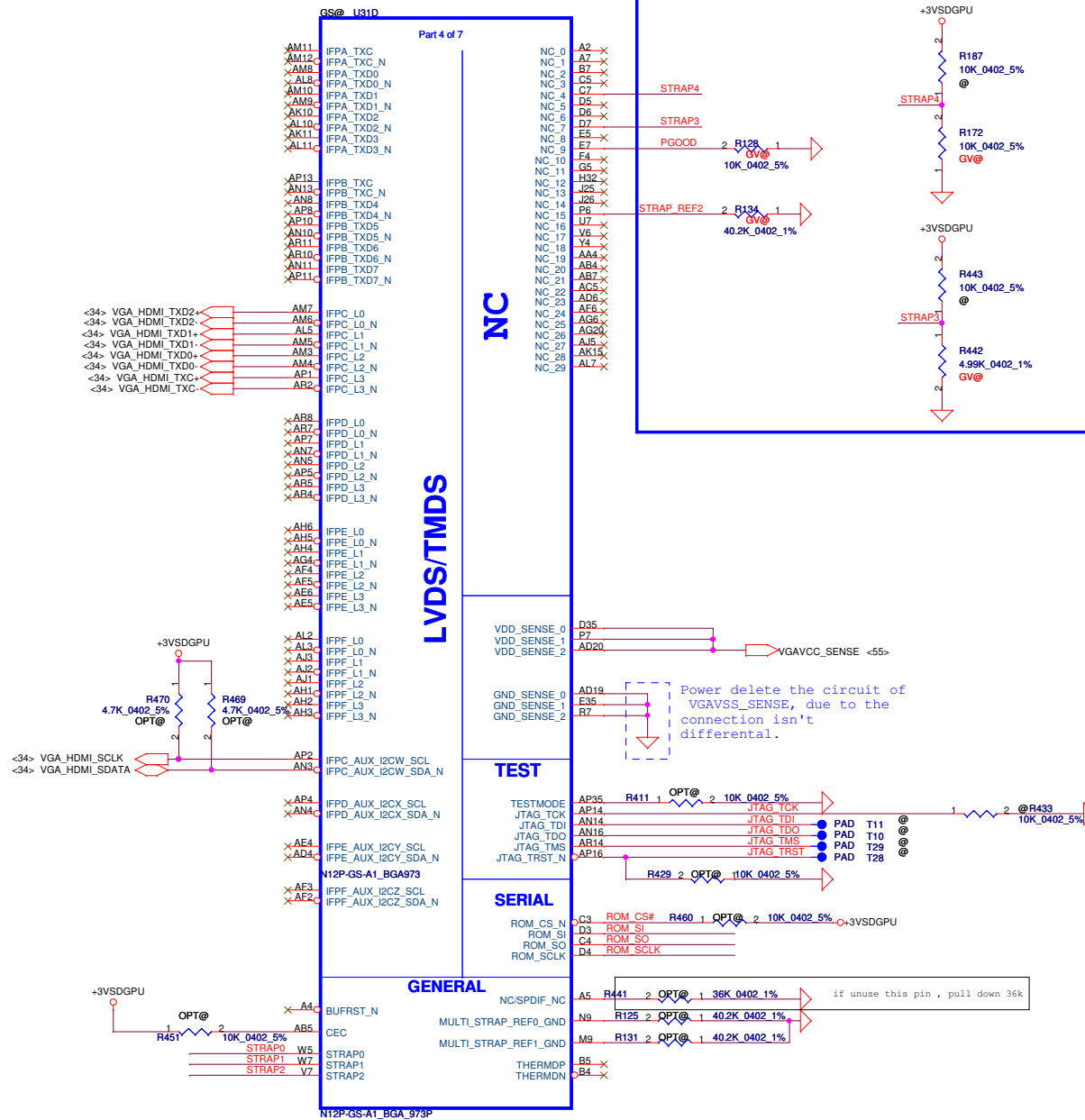


VRAM Interface



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For GB2-128 & GB2b-128 colayout....



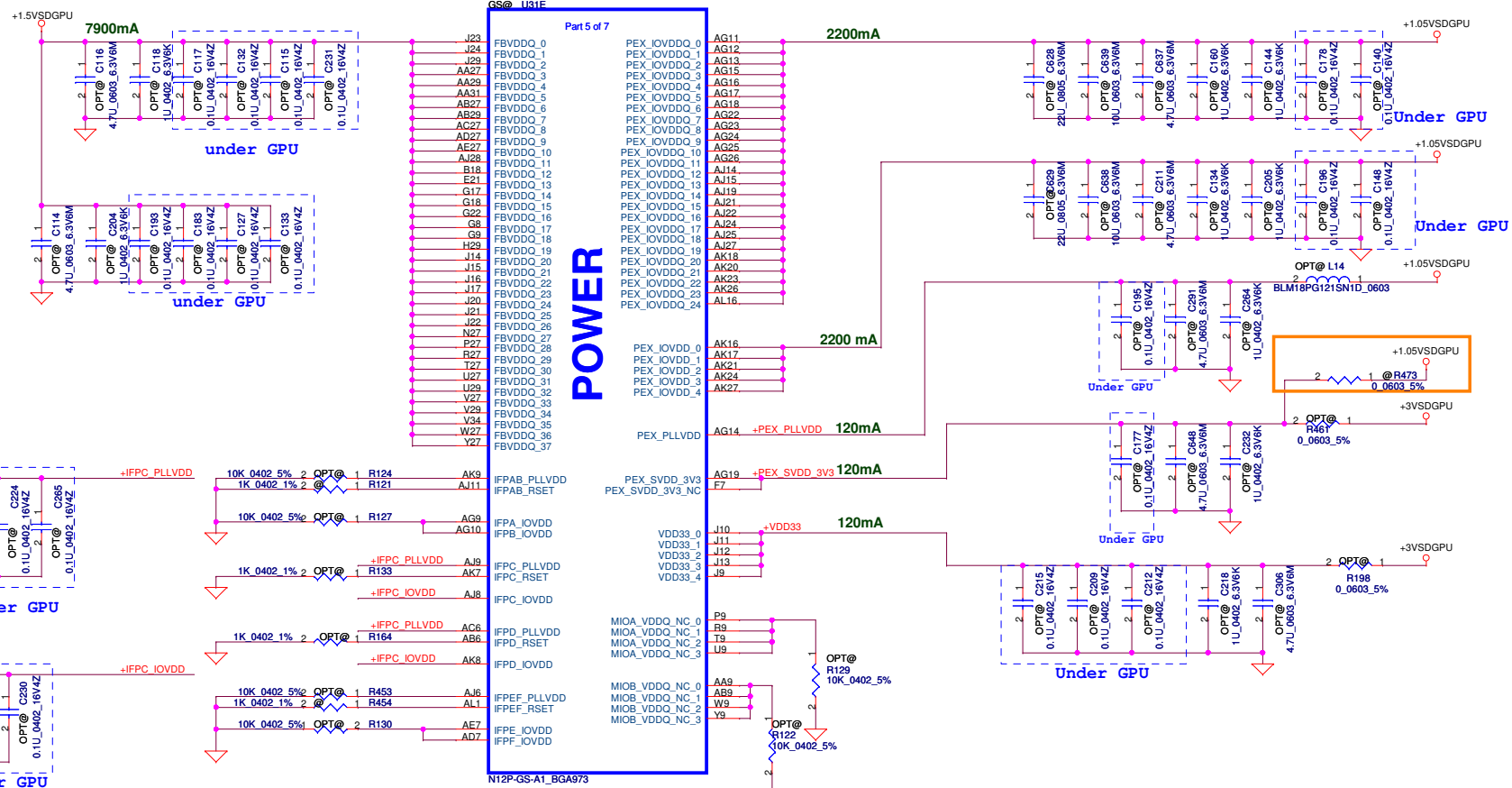
N12P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA0000035700	H 45K	L 35K	L 25K	L 20K	L 10K	H 15K
64MX16 Hynix SA0000032400	H 45K	L 35K	L 25K	L 15K	L 10K	H 15K
128MX16 Samsung SA000047Q20	H 45K	L 35K	L 25K	L 45K	L 10K	H 15K
128MX16 Hynix SA000003VS10	H 45K	L 35K	L 25K	L 35K	L 10K	H 15K

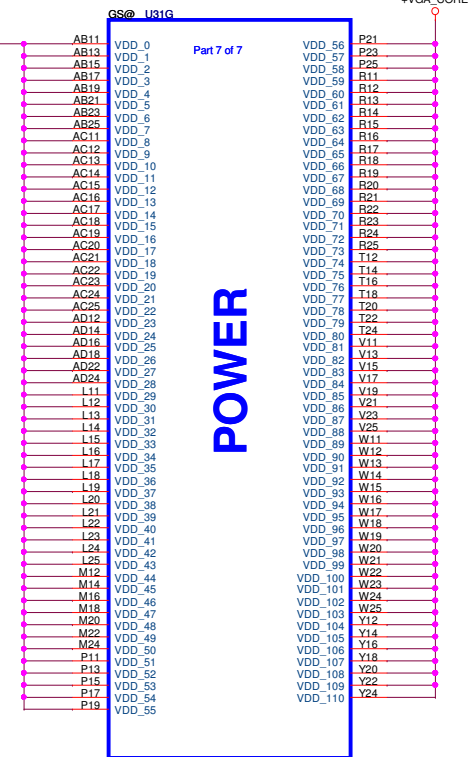
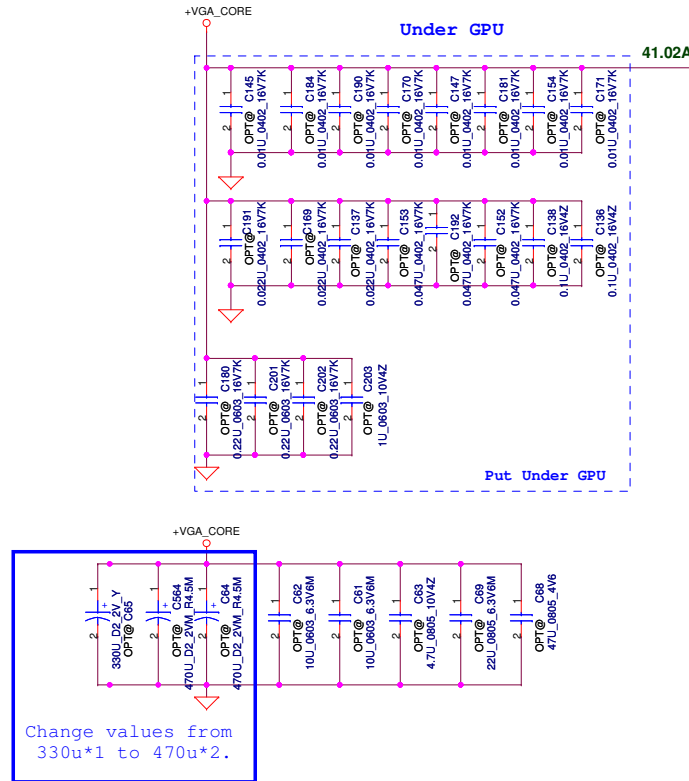
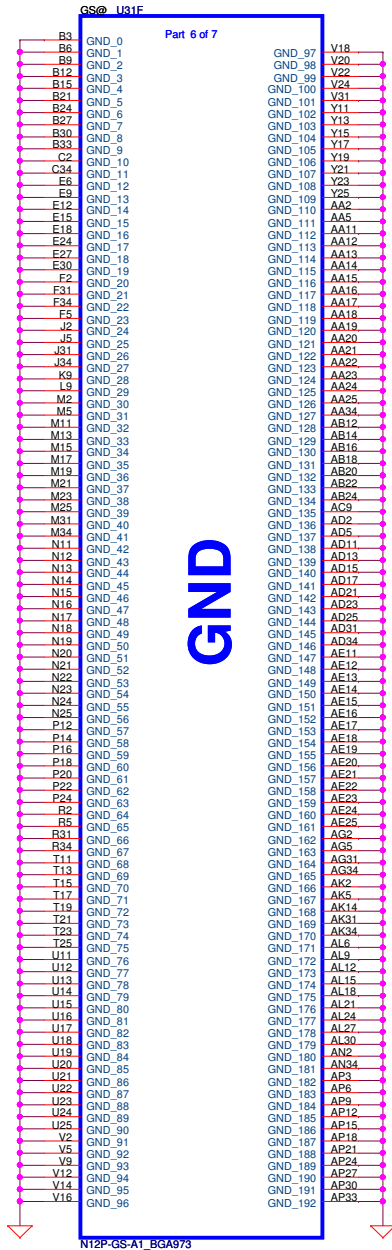
N12P-GV	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 Hynix SA000032400	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
128MX16 Samsung SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K

GPU	DeviceID	ROM_SCLK	STRAP2
N12F-GS	0x0DF4	Pull up 15K	Pull down 25K
N12F-GV	0x0DF7	Pull up 5K	Pull down 5K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix (900MHZ) 128M16 H5TQ2G63BFR-11C SA00003Y020	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64M16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD034200280)
	1GB	0011	PD 20K (SD034200280)
Samsung (900MHZ) 128M16 K4W2G1646C-HC11 SA000047Q20	2GB	0111	PD 45.3K(SD034453280)

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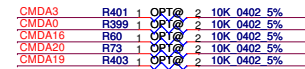
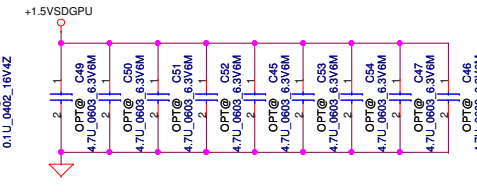
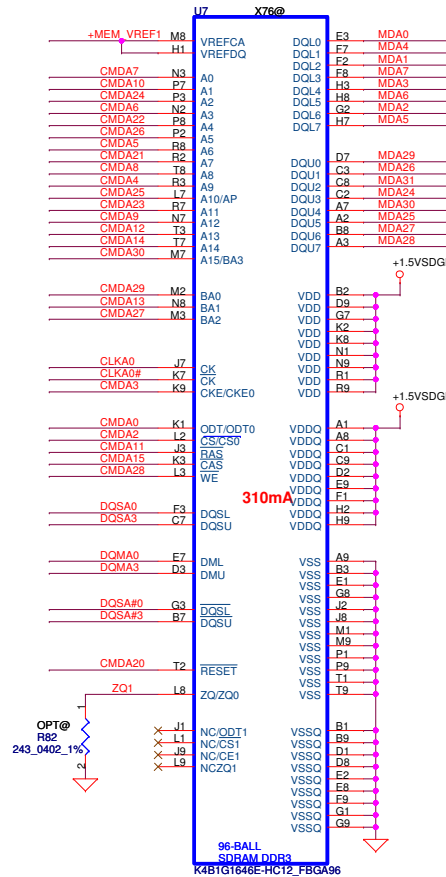
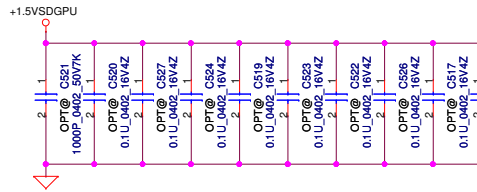
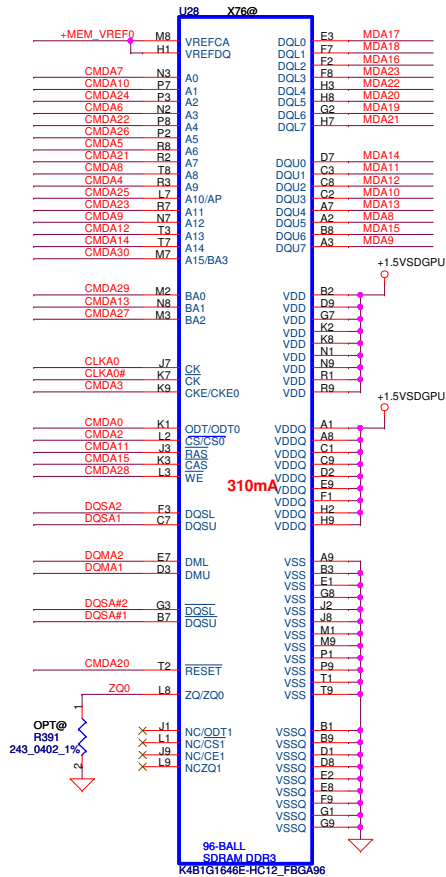
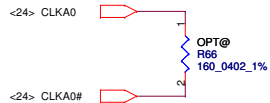
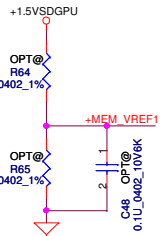
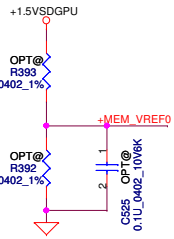
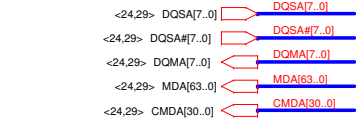




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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11	CS0_H#	
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15	CS1_H#	
CMD19	CMD16	ODT_H	
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		

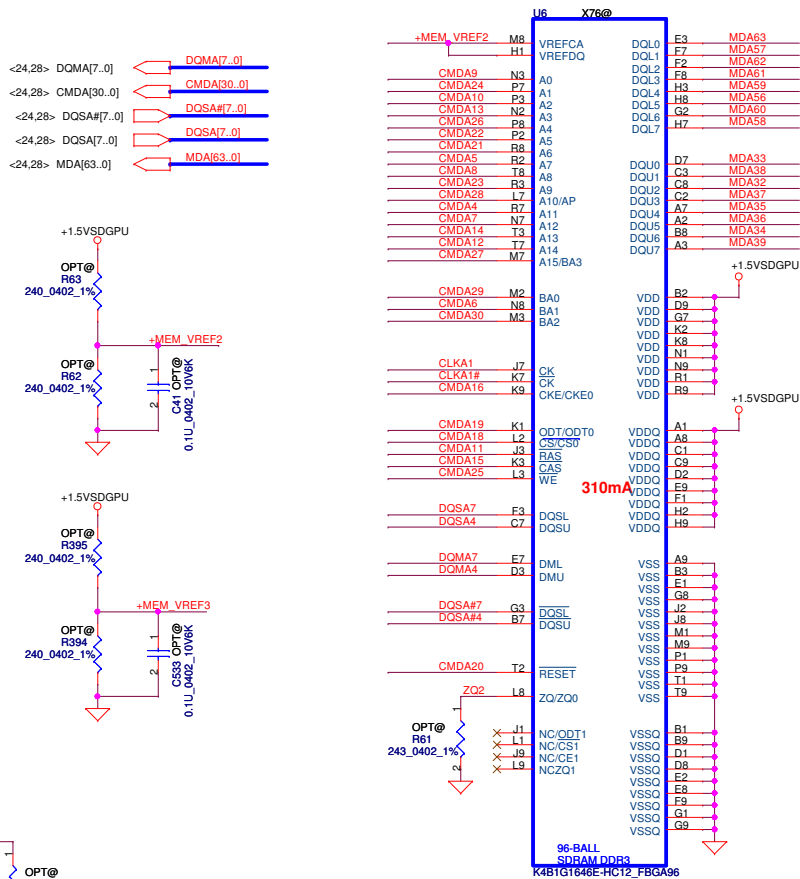
Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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Title		N11P DDR3 6/9	
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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB



Mode B Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		

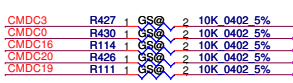
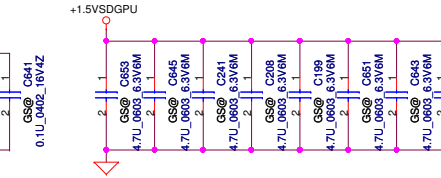
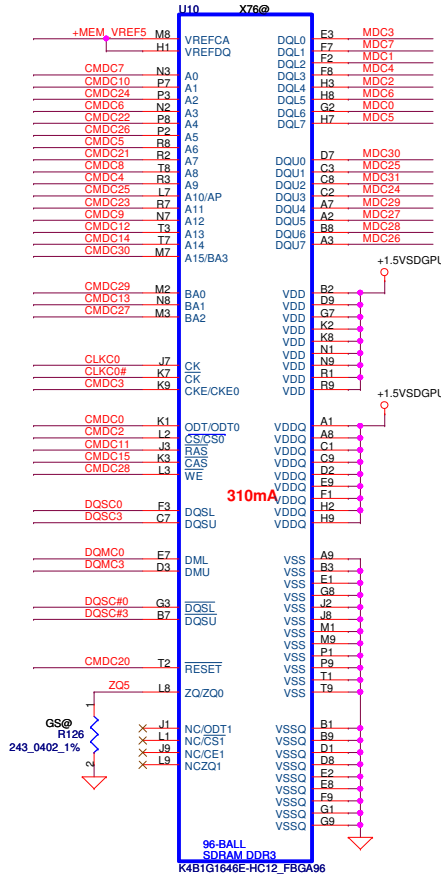
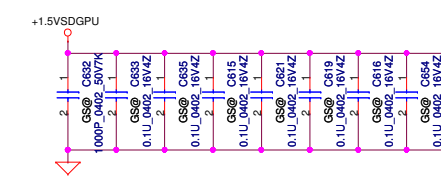
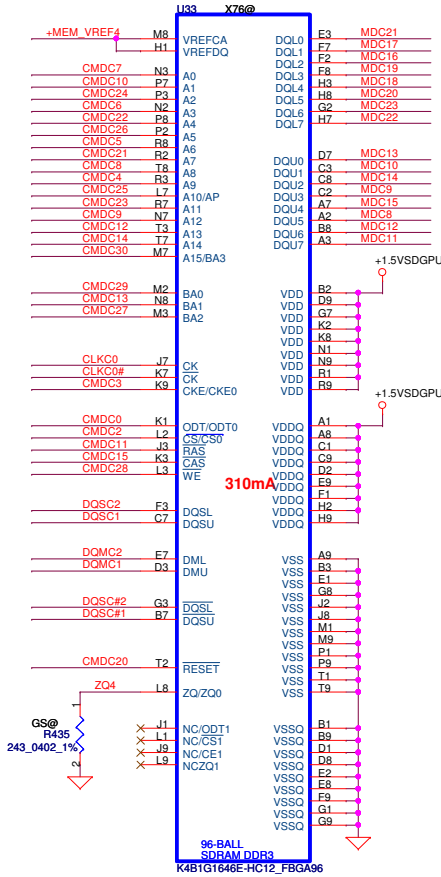
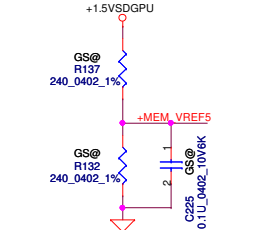
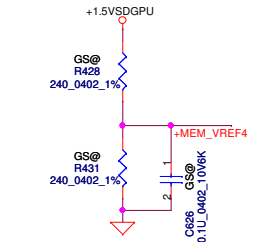
LOW HIGH

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				Size	Rev
				Customer	0.1
				P4LS0 M/B LA-7241P Schematic	
				Date:	Thursday, December 23, 2010
				Sheet	29 of 55

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

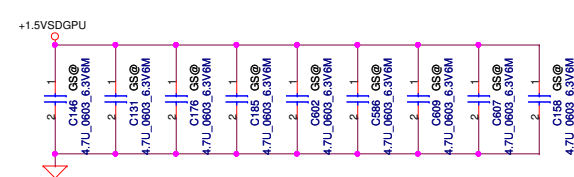
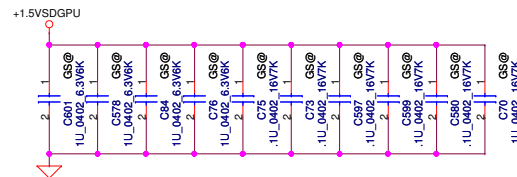
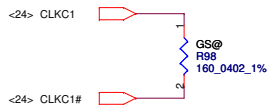
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<24,31> DOMC[7..0] DOMC[7..0]
<24,31> MDC[63..0] MDC[63..0]
<24,31> CMD[30..0] CMD[30..0]



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11	CS0_H#	
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15	CS1_H#	
CMD19	CMD16	ODT_H	
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		

Command Bit	Default Pull-downs
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

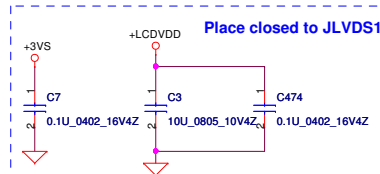
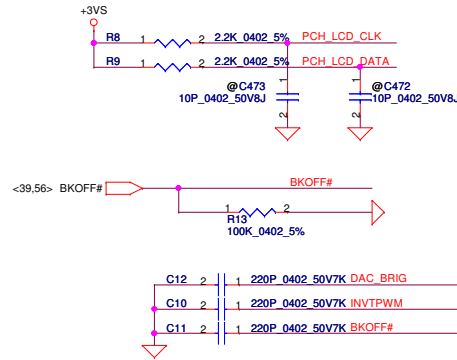
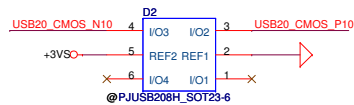
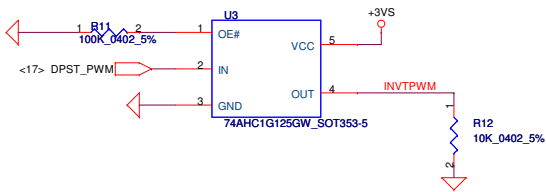
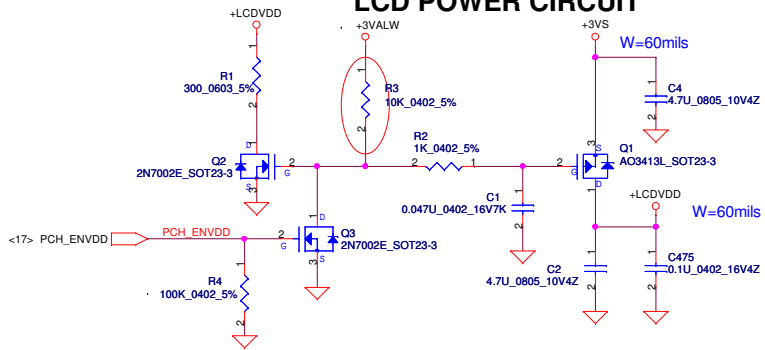
64Mx16 DDR3 *8==>1GB



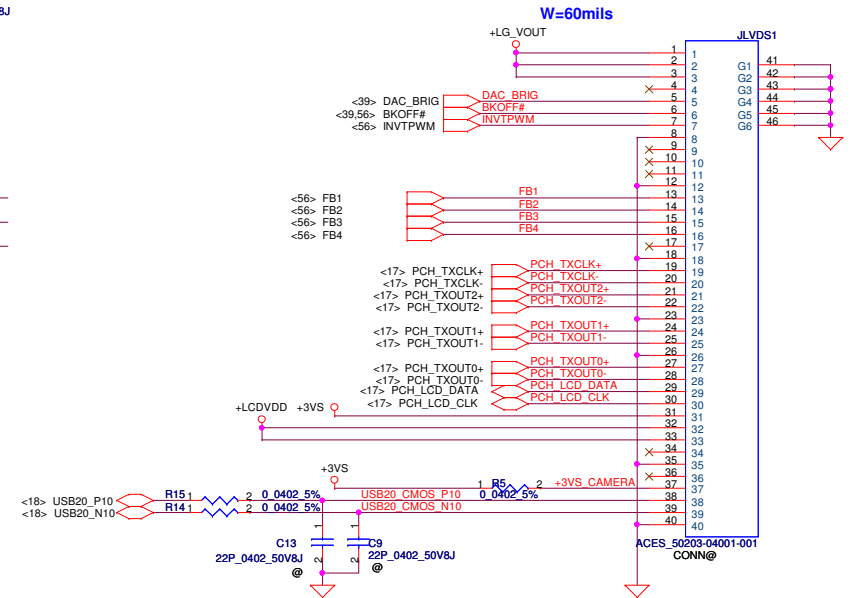
Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		

LOW HIGH

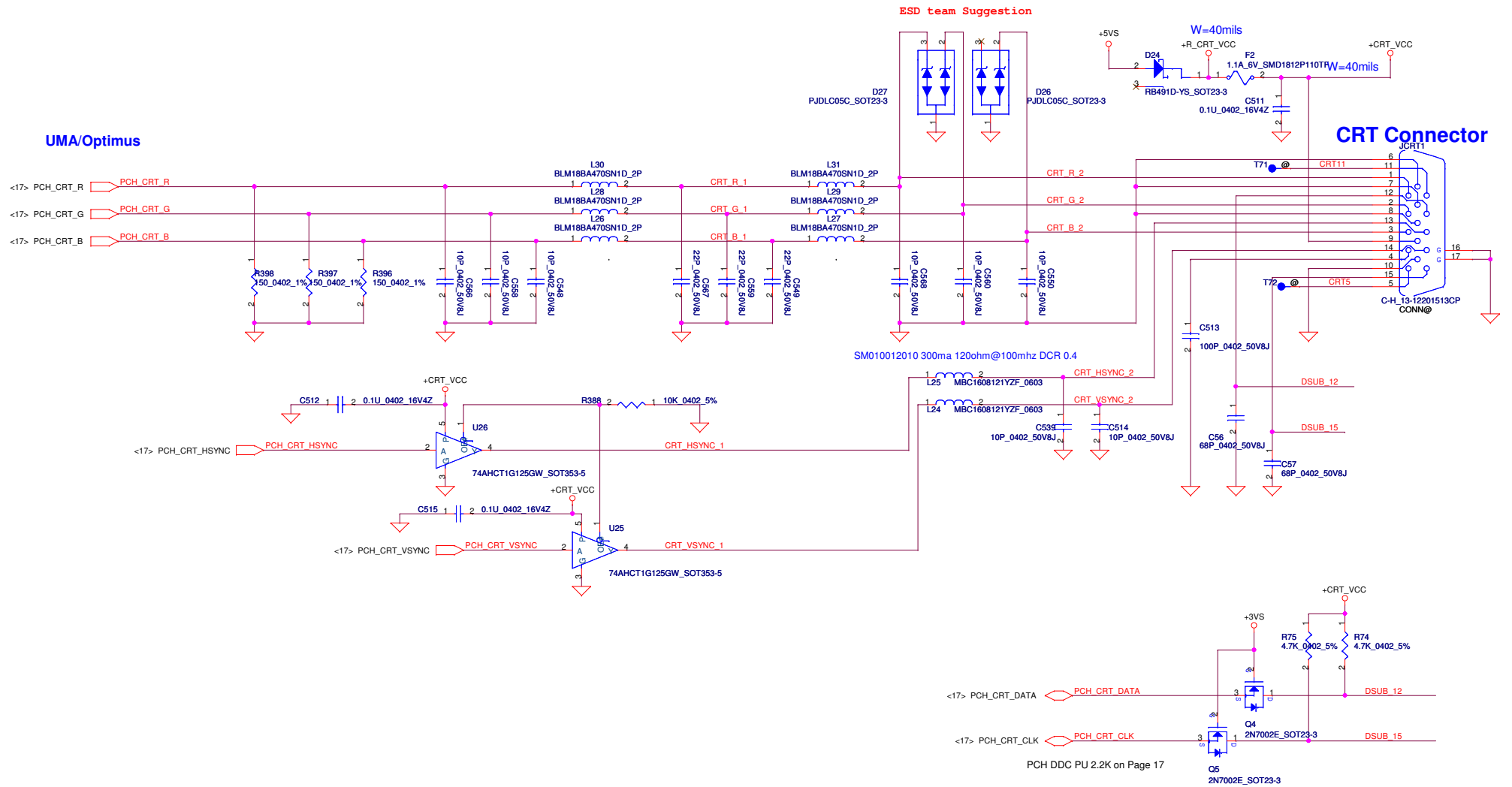
LCD POWER CIRCUIT



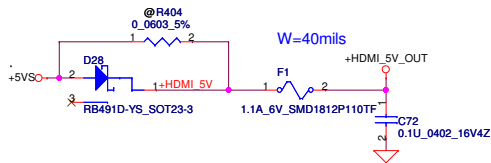
LCD/LED PANEL Conn.



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Size	Document Number	Rev		0.1	
Customer	P4LS0 M/B LA-7241P Schematic				
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Size	Custom	Document Number	P4LS0 M/B LA-7241P Schematic	Rev	0.1
Date:	Thursday, December 23, 2010	Sheet	33	of	55



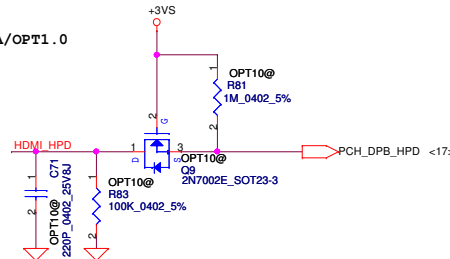
OPT1.0

<17> PCH_DPB_N0	C283 OPT10@2	1 .1U 0402 16V7K	HDMI TX2-
<17> PCH_DPB_P0	C282 OPT10@2	1 .1U 0402 16V7K	HDMI TX2+
<17> PCH_DPB_N1	C288 OPT10@2	1 .1U 0402 16V7K	HDMI TX1-
<17> PCH_DPB_P1	C289 OPT10@2	1 .1U 0402 16V7K	HDMI TX1+
<17> PCH_DPB_N2	C286 OPT10@2	1 .1U 0402 16V7K	HDMI TX0-
<17> PCH_DPB_P2	C287 OPT10@2	1 .1U 0402 16V7K	HDMI TX0+
<17> PCH_DPB_N3	C284 OPT10@2	1 .1U 0402 16V7K	HDMI CLK-
<17> PCH_DPB_P3	C285 OPT10@2	1 .1U 0402 16V7K	HDMI CLK+

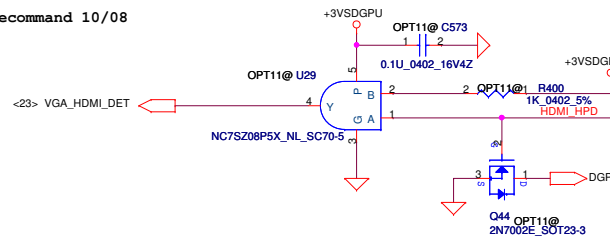
OPT1.1

<25> VGA_HDMI_TXD2-	C267 OPT11@	1 .1U 0402 16V7K	HDMI TX2-
<25> VGA_HDMI_TXD2+	C266 OPT11@	1 .1U 0402 16V7K	HDMI TX2+
<25> VGA_HDMI_TXD1-	C272 OPT11@	1 .1U 0402 16V7K	HDMI TX1-
<25> VGA_HDMI_TXD1+	C273 OPT11@	1 .1U 0402 16V7K	HDMI TX1+
<25> VGA_HDMI_TXD0-	C270 OPT11@	1 .1U 0402 16V7K	HDMI TX0-
<25> VGA_HDMI_TXD0+	C271 OPT11@	1 .1U 0402 16V7K	HDMI TX0+
<25> VGA_HDMI_TXC-	C268 OPT11@	1 .1U 0402 16V7K	HDMI CLK-
<25> VGA_HDMI_TXC+	C269 OPT11@	1 .1U 0402 16V7K	HDMI CLK+

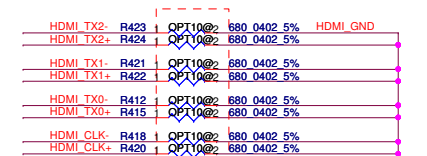
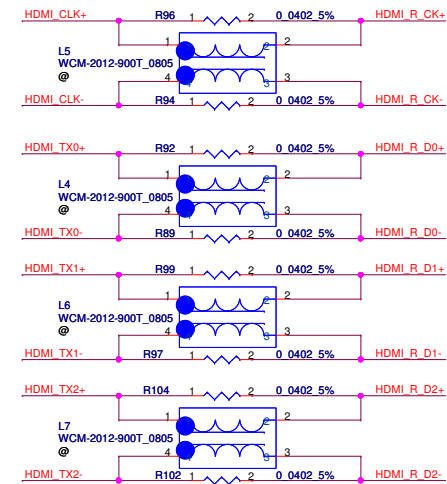
UMA/OPT1.0



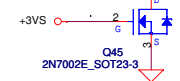
NVIDIA Recommend 10/08 OPT1.1



SM070001310 400ma 90ohm@100mhz DCR 0.3



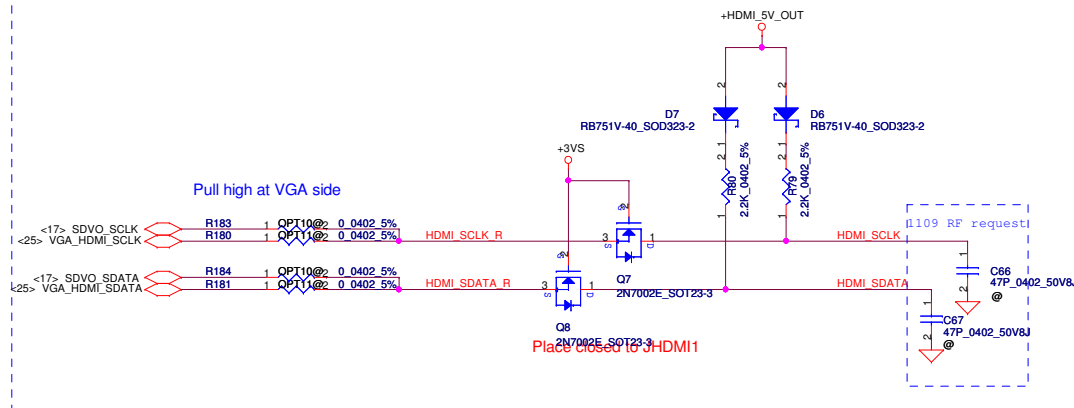
UMA 680_0402_5%
DIS 499_0402_1%



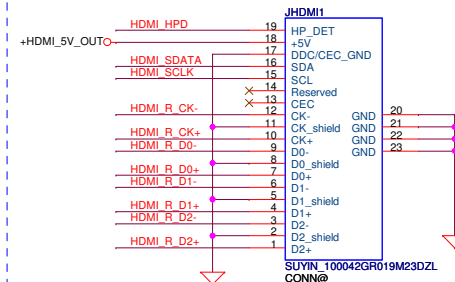
DIS Option Component

R423	2	OPT11@	499_0402_1%
R424	2	OPT11@	499_0402_1%
R421	2	OPT11@	499_0402_1%
R422	2	OPT11@	499_0402_1%
R412	2	OPT11@	499_0402_1%
R415	2	OPT11@	499_0402_1%
R418	2	OPT11@	499_0402_1%
R420	2	OPT11@	499_0402_1%

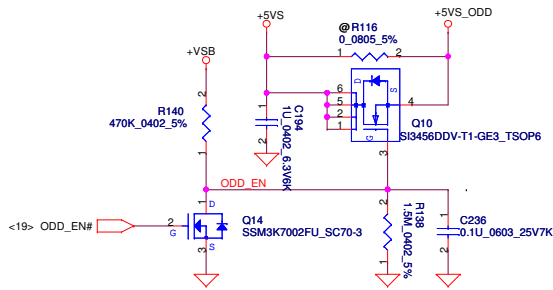
Pull high at VGA side



HDMI connector

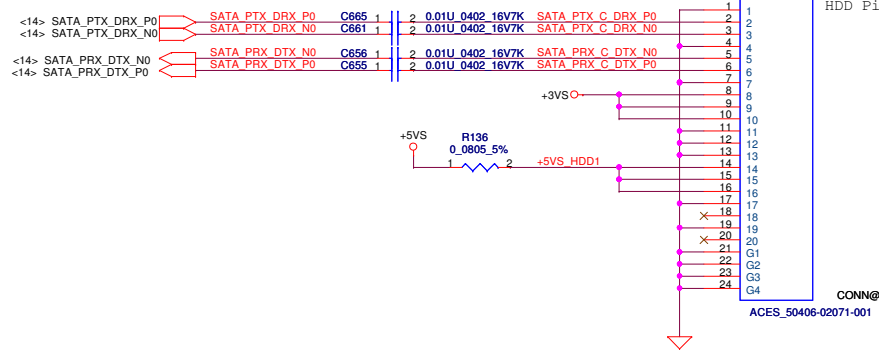


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				Date: Thursday, December 23, 2010	Rev 0.1
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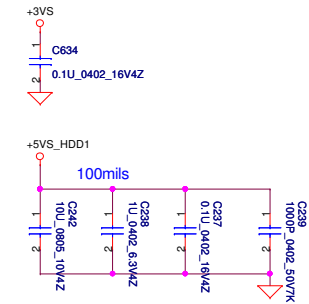


SATA HDD1 Conn.

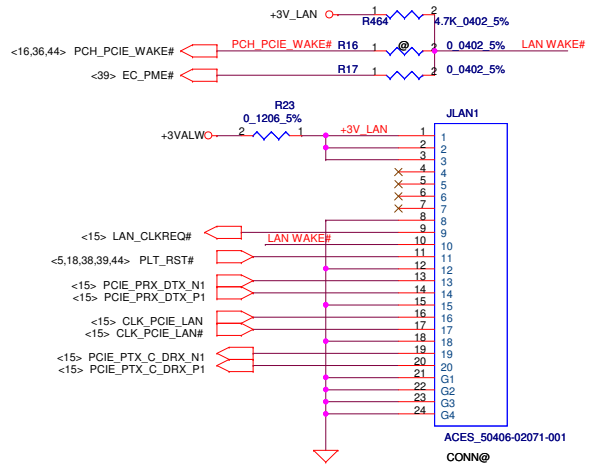
CL 4.0 mm



HDD Pin Definition need check!!!

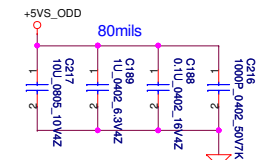
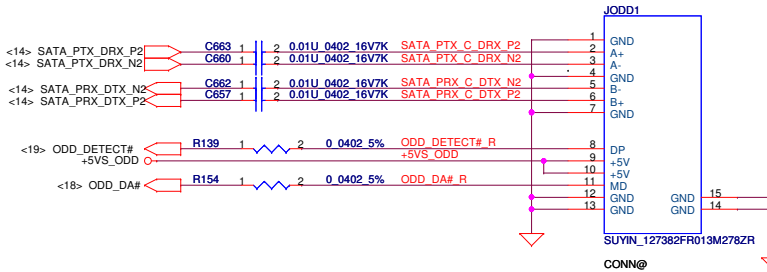


LAN CONN.



M/B side

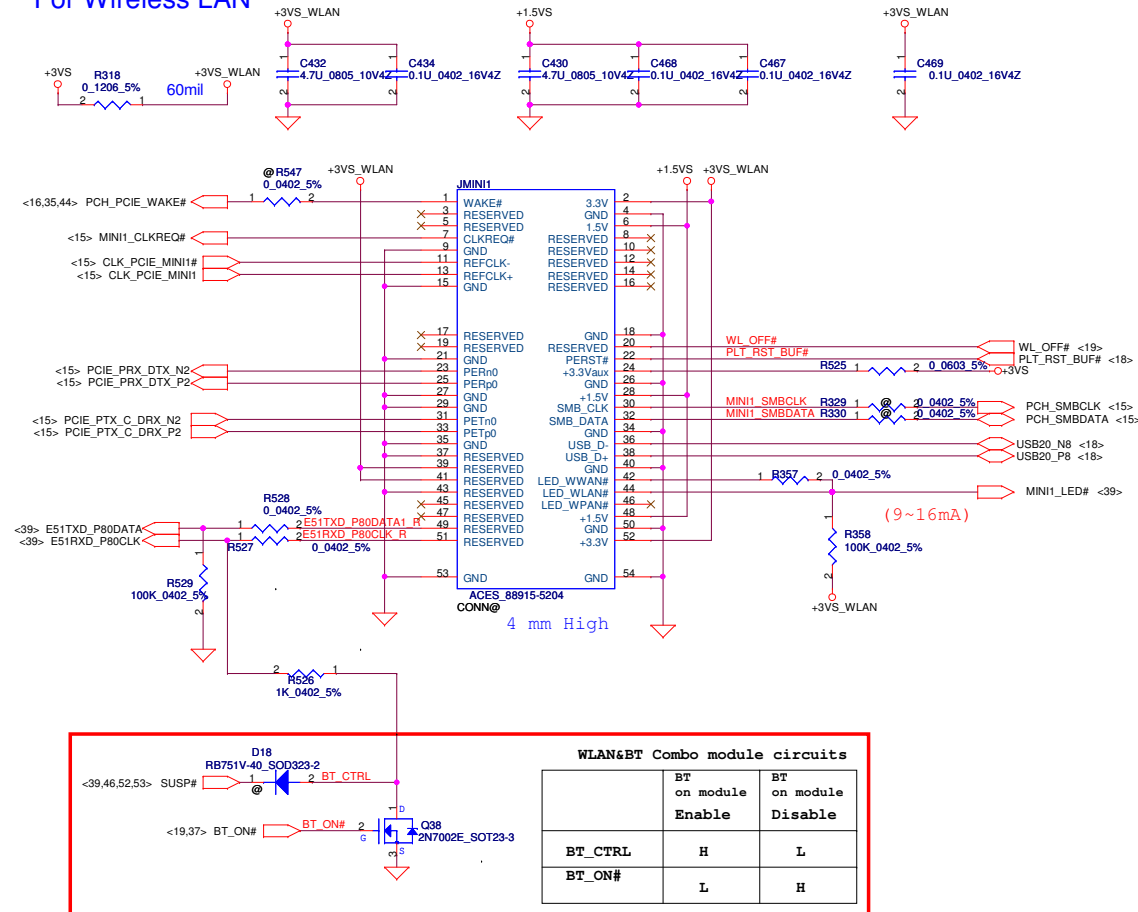
SATA ODD Conn.



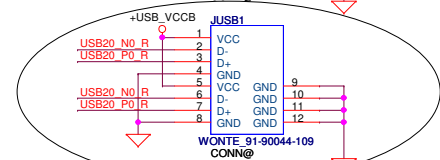
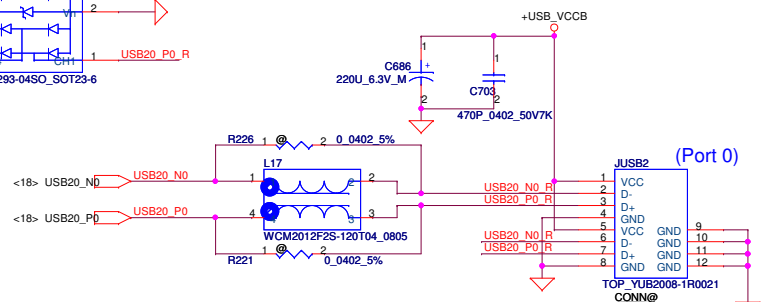
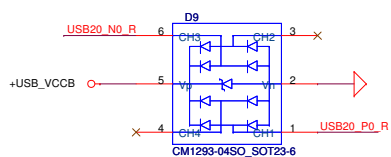
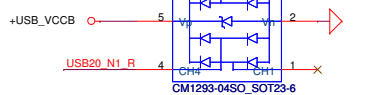
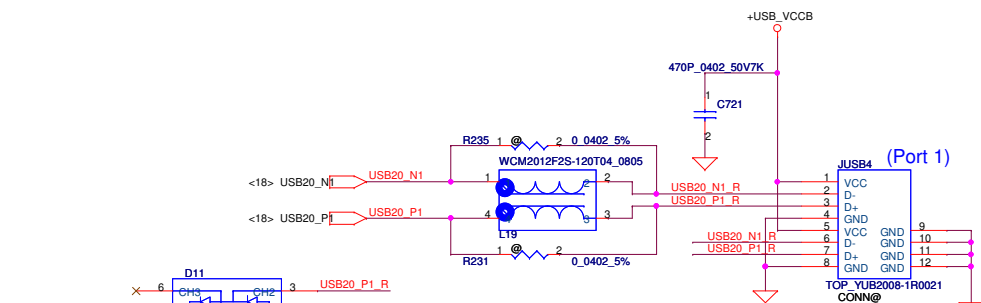
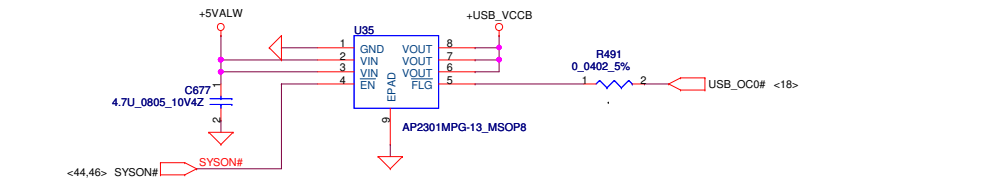
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Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title HDD, ODD & LAN Connector				
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

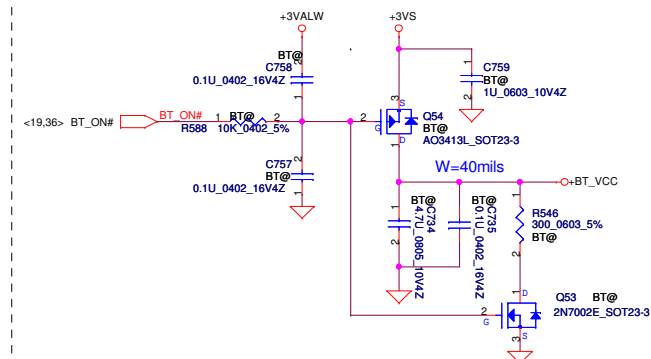
For Wireless LAN



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				MINI CARD (WLAN & TV-Tuner)/USB/BT			
				Size			
Customer		Document Number		P4LS0 M/B LA-7241P Schematic		Rev 0.1	
Date:		Thursday, December 23, 2010		Sheet 36 of 55			

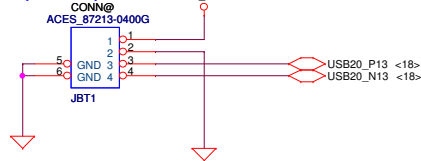


colayout this connector with JUSB1



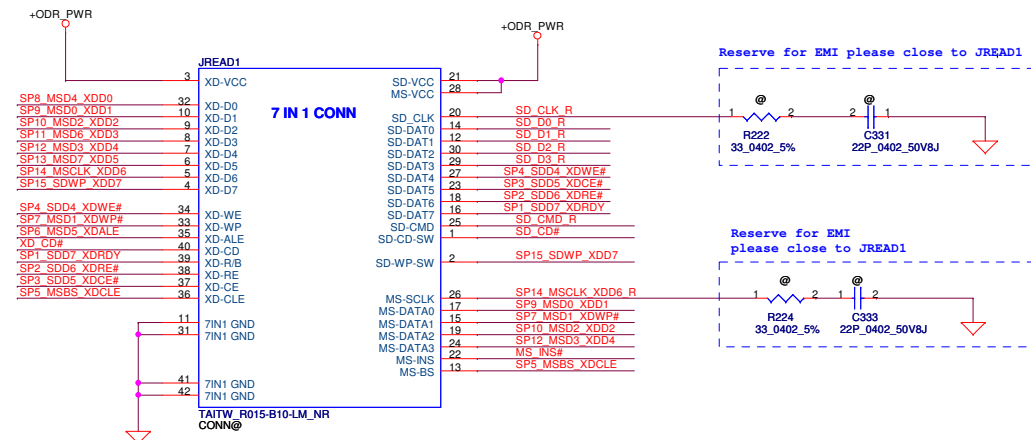
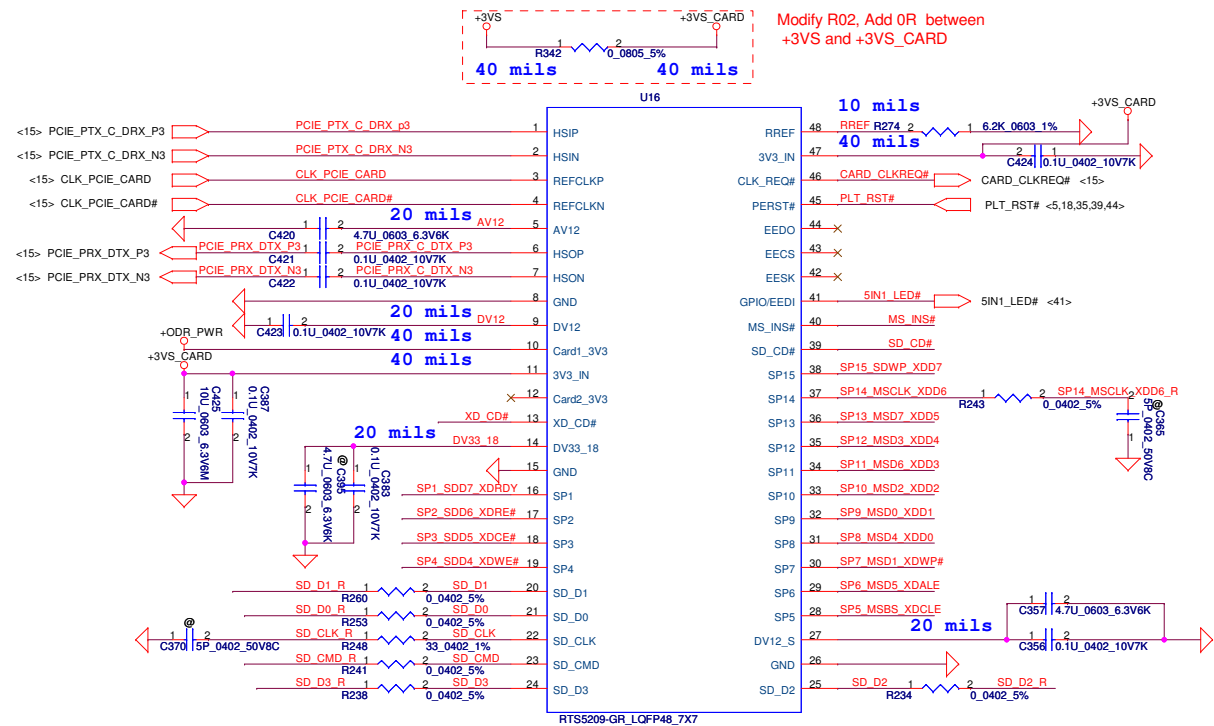
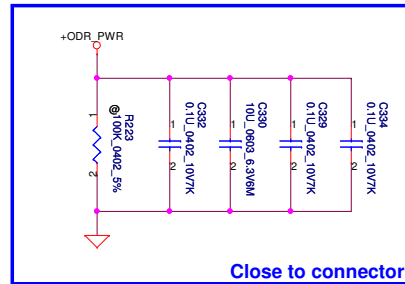
BT Conn.

(Port 13)

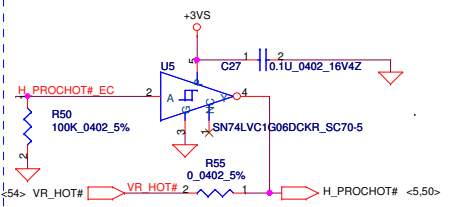
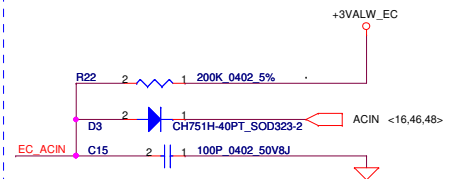
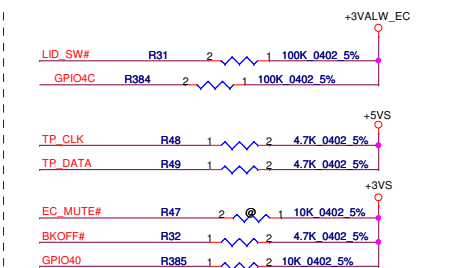
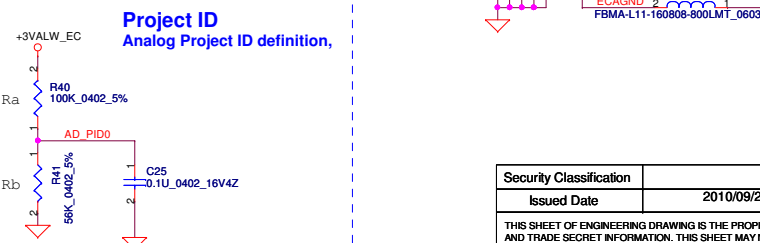
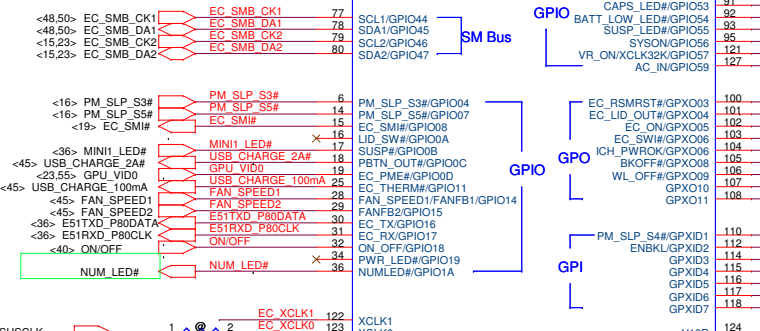
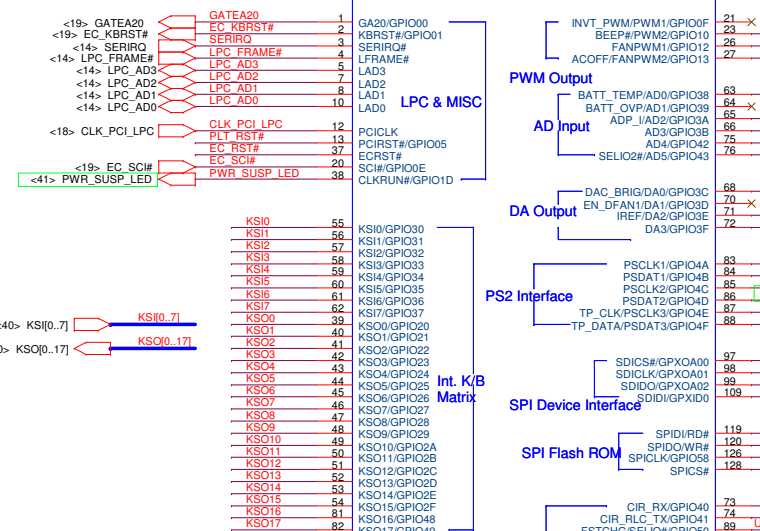
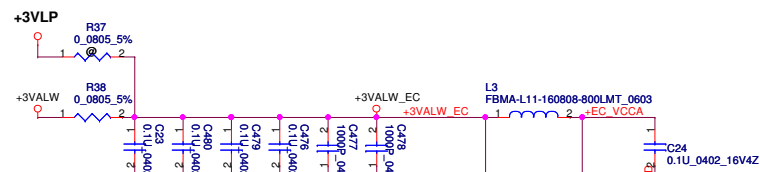
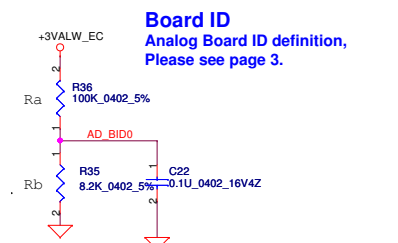


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				MINI CARD (WLAN & TV-Tuner)/USB/BT	
				Size	
				P4LS0 M/B LA-7241P Schematic	
				Rev	
				0.1	
				Date: Thursday, December 23, 2010	
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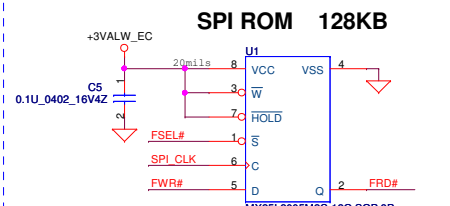
Card Reader



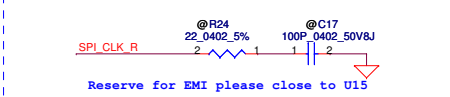
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Issued Date	2010/09/28	Deciphered Date	2011/09/28	Title Card Reader RTS5209			
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				Customer	P4LS0 M/B LA-7241P Schematic	0.1	
				Date:	Thursday, December 23, 2010	Sheet	38 of 55



Latest design guide suggest change UE4 to 74LVC1G06.

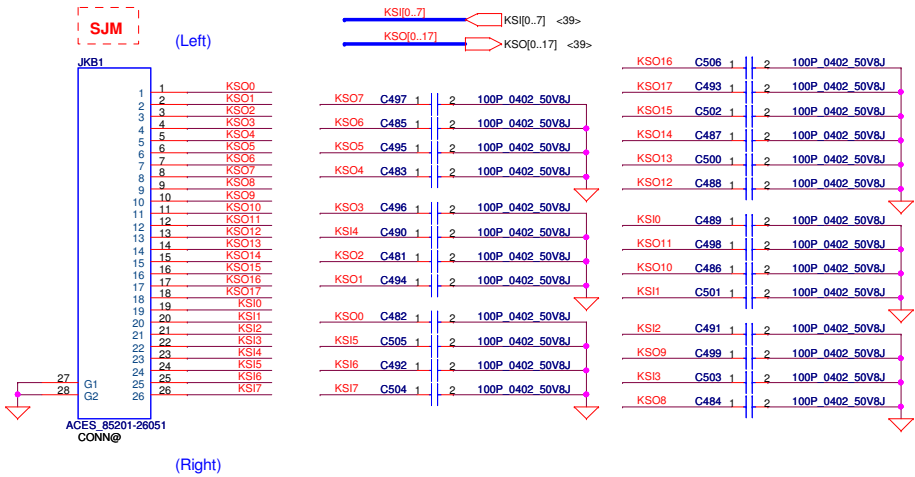


SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)

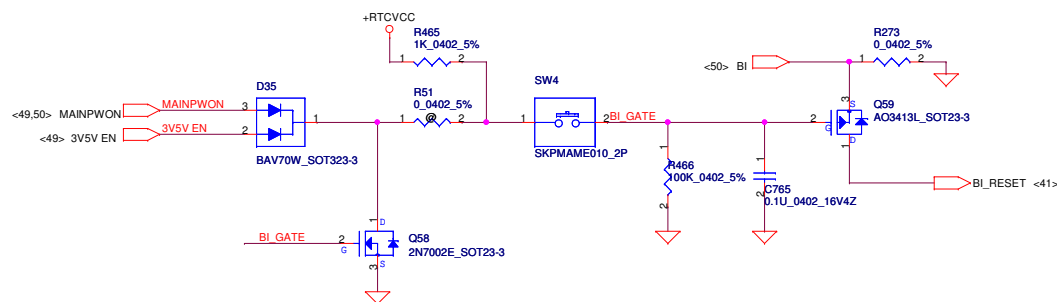


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				Custom	P4LS0 M/B LA-7241P Schematic
				Date:	Thursday, December 23, 2010
				Sheet	39 of 55
				Rev	0.1

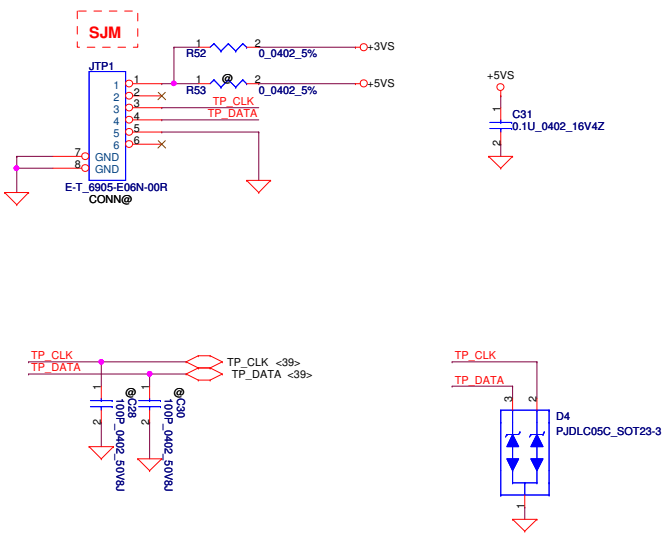
INT_KBD Conn.



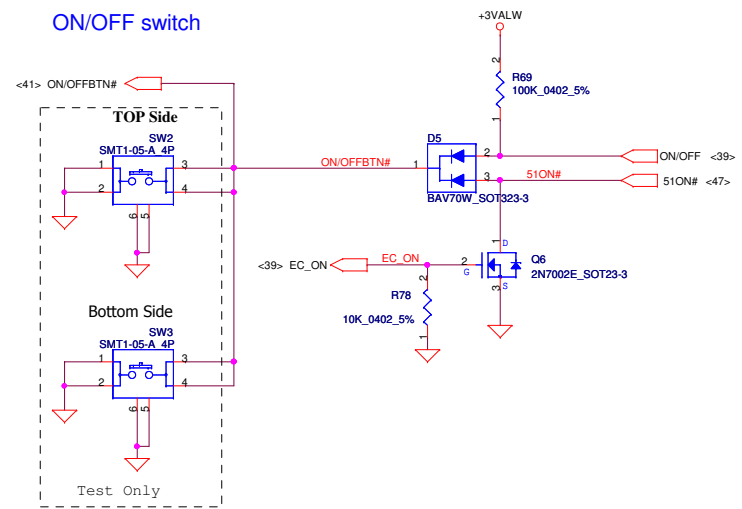
Reset Button



To TP/B Conn.

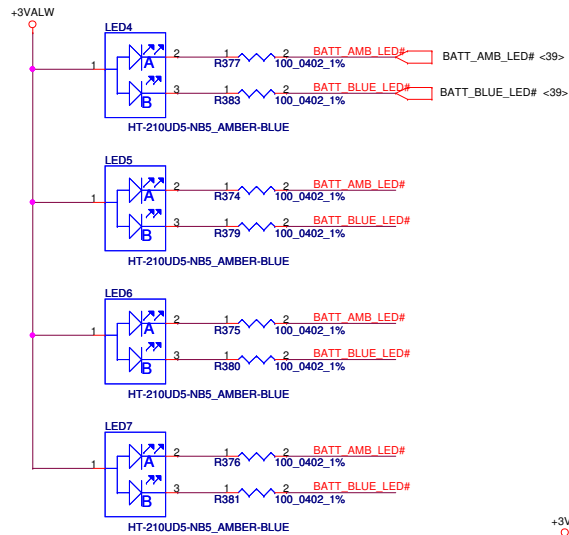


Power Button

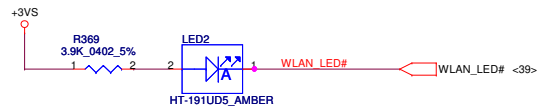


Battery LED

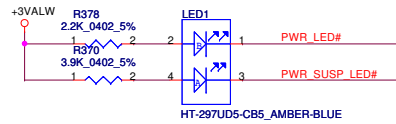
Side View LED with Blue/Amber/Red Color



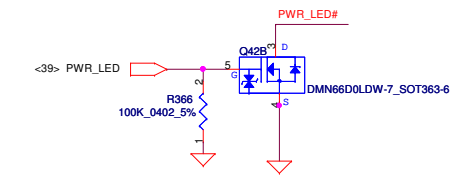
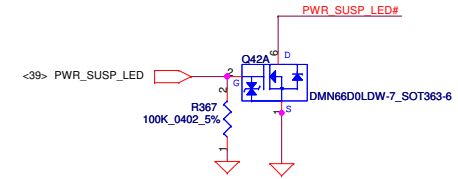
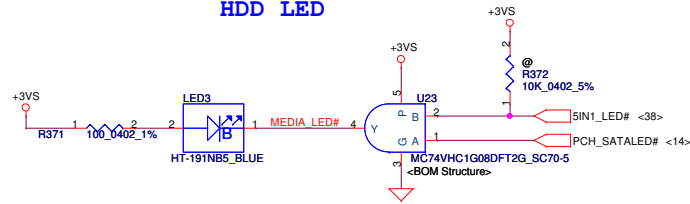
Wireless LED (SJM)



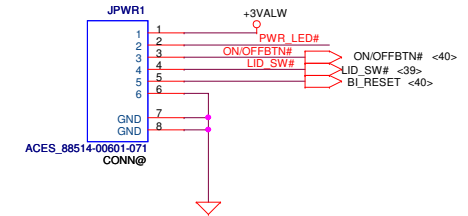
Power LED (SJM)



HDD LED

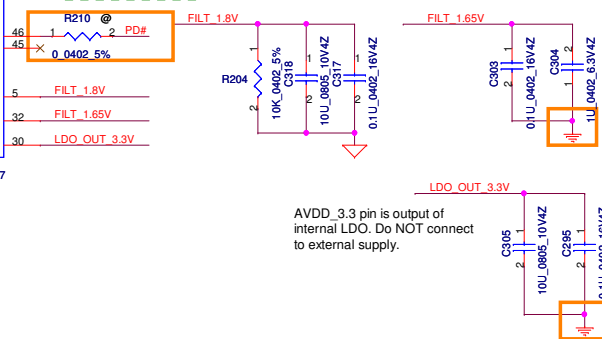
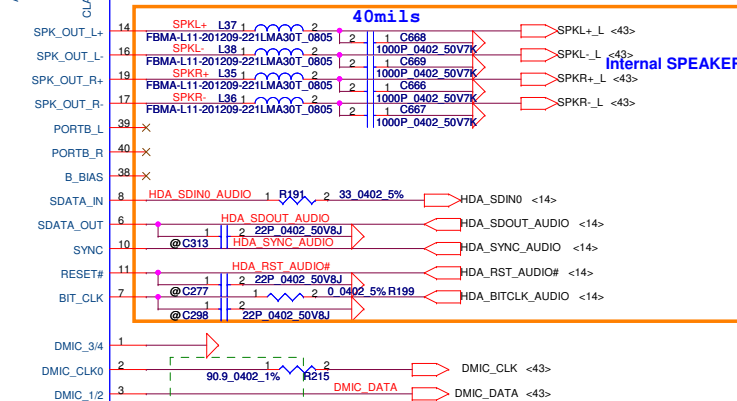
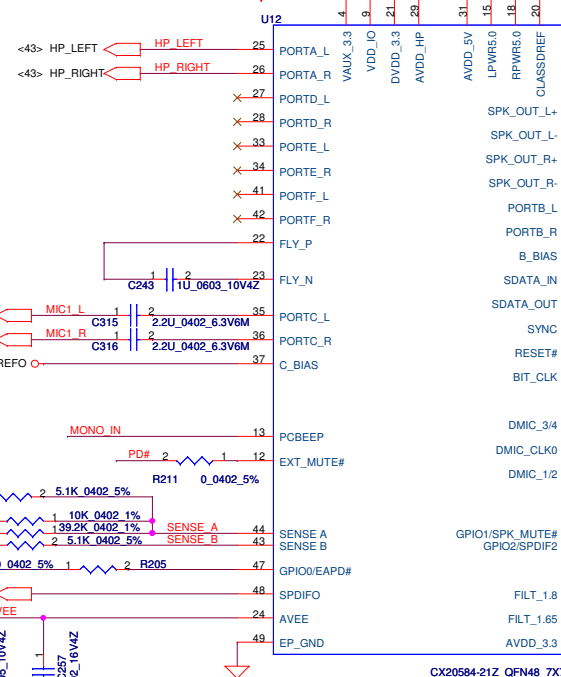
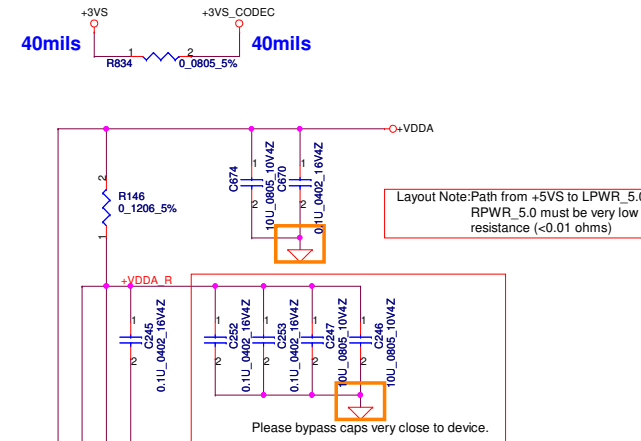
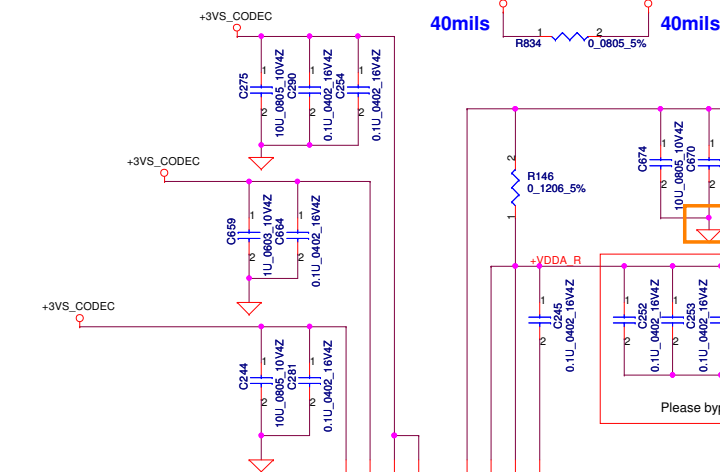
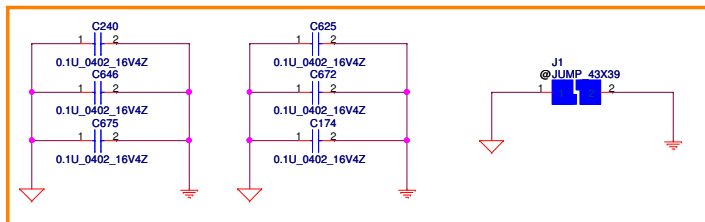
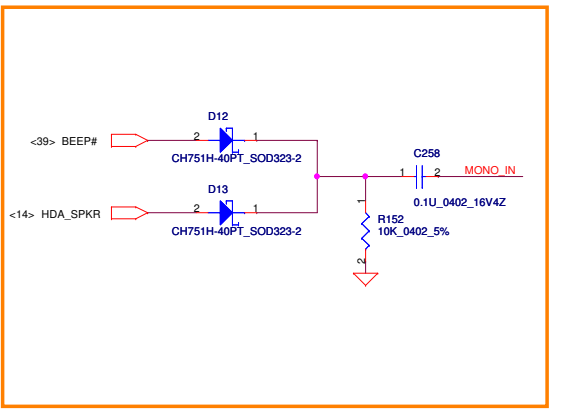
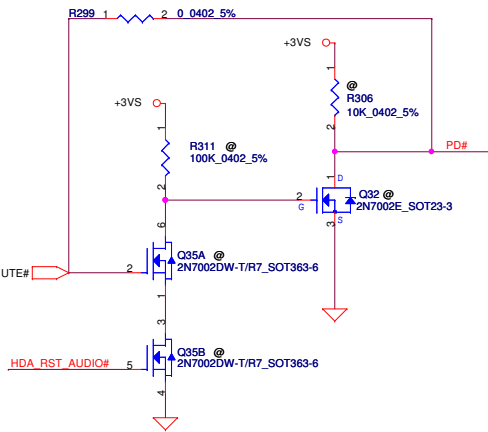
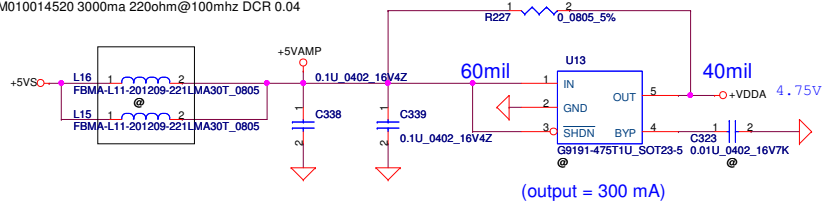


PWR/B



LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth		ACIN
	ON	SUS	Full	Charge	3G	WLAN			
	Blue	Amber	Blue	Amber	Blue	Amber			

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AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

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				Size	Document Number		Rev 0.1
				Custm	P4LS0 M/B LA-7241P Schematic		
Date:		Thursday, December 23, 2010		Sheet	42 of 55		

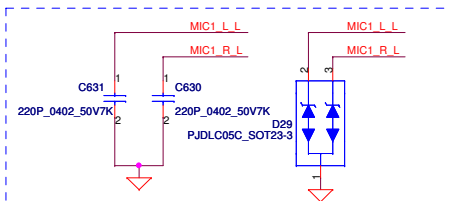
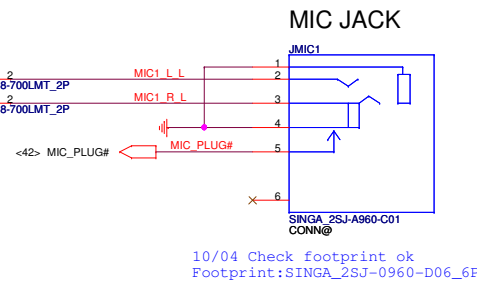
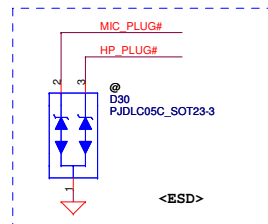
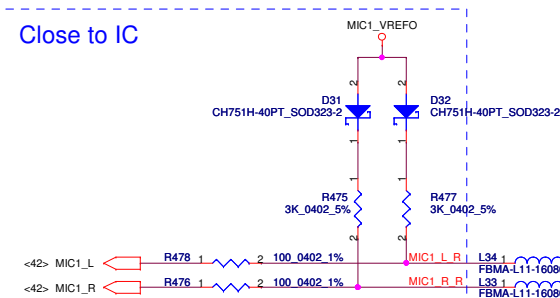
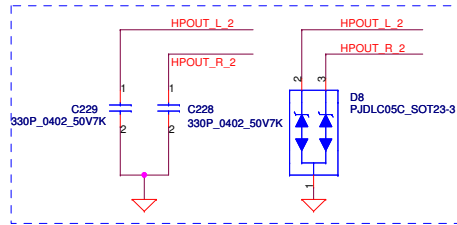
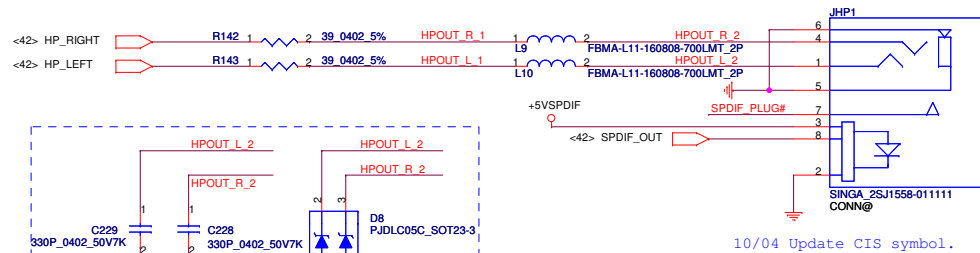


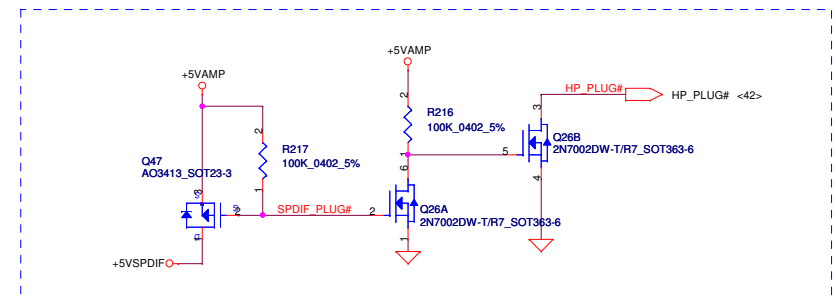
Figure 10: Digital MIC CONN.

The diagram illustrates the connection of a digital microphone to the JSPK1 and JSPK2 ports. It includes a table of pin connections for SPKL+, SPKL-, SPKR+, and SPKR- lines, and two detailed circuit diagrams for the JSPK1 and JSPK2 ports, showing the internal structure of the PJDLC05C_SOT23-3 components and the connection to the ACES_88266-02001 connector.

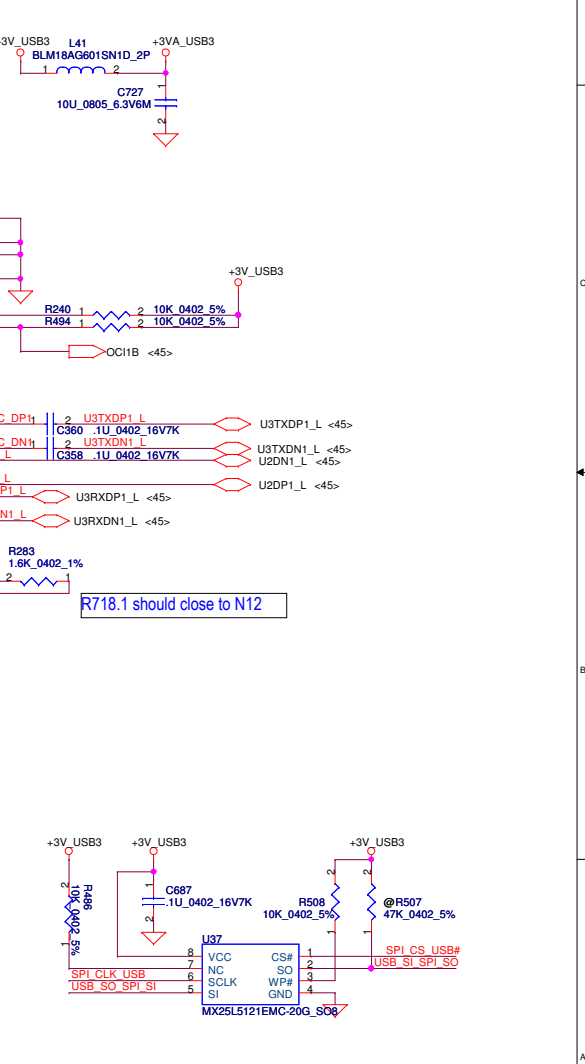
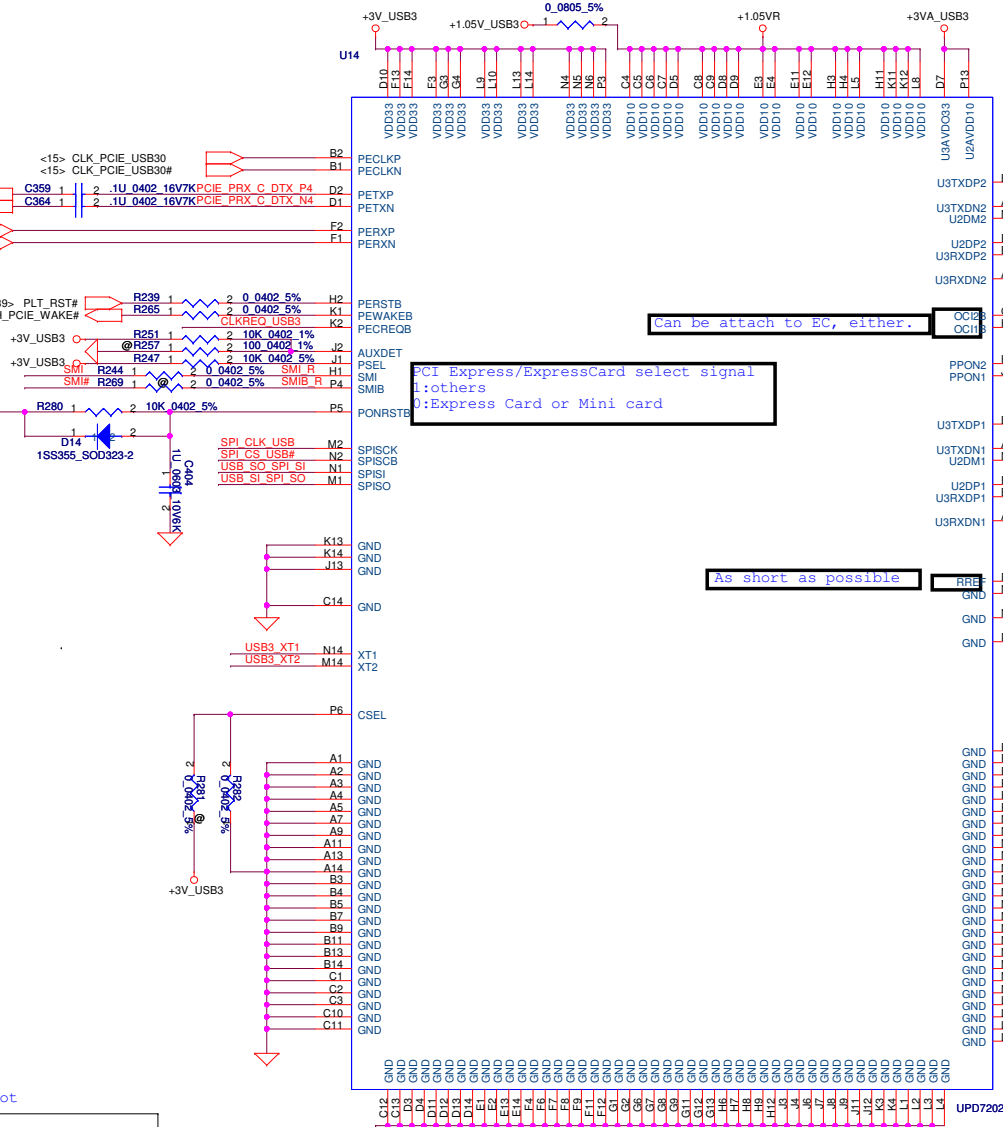
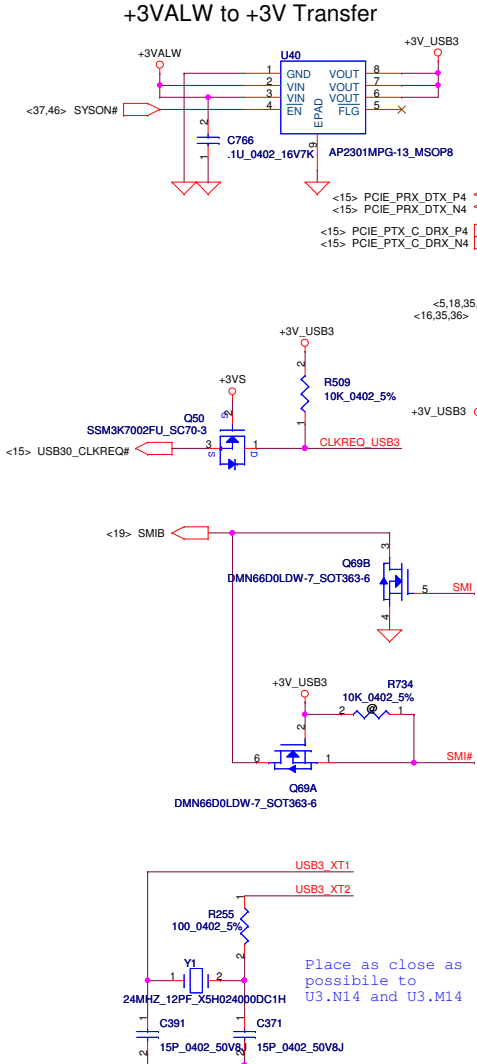
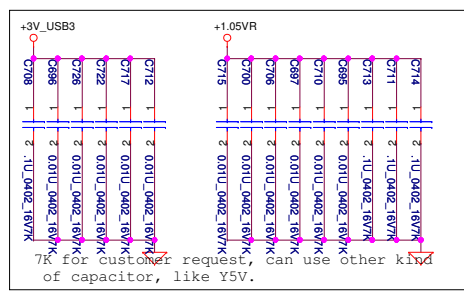
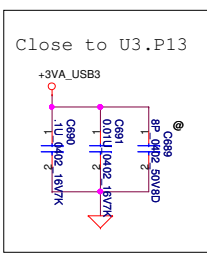
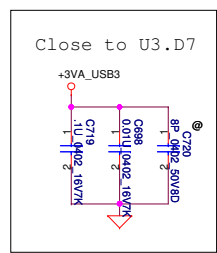
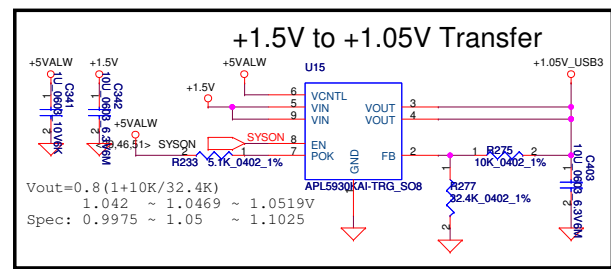
Pin	Signal	Value	Value	Value
<42>	SPKL+ _L	R230	1	2 0.0603 5%
<42>	SPKL+ _L	R236	1	2 0.0603 5%
<42>	SPKR+ _L	R519	1	2 0.0603 5%
<42>	SPKR+ _L	R514	1	2 0.0603 5%

Place D38 near JSPK1

Place D37 near JSPK2

[illegible]

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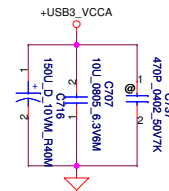
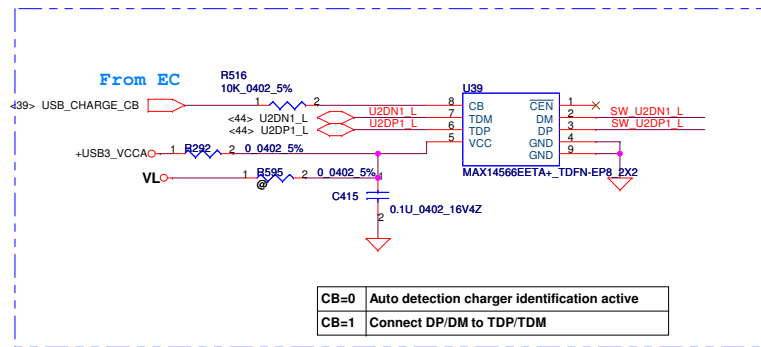
Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

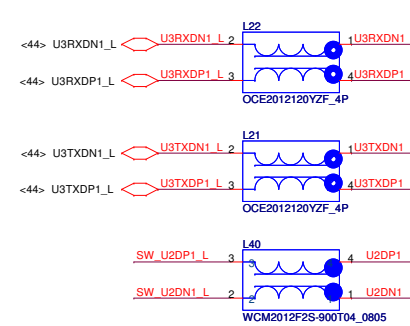
P/N: SA000048H10
(S IC UPD720200AF1-DAP-A_FBG176)

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Size	Document Number	P4L50 M/B LA-7241P Schematic	
Custom		Rev 0.1	
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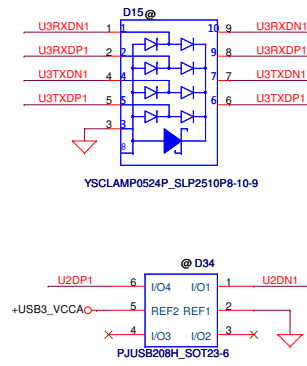
USB Host Charger



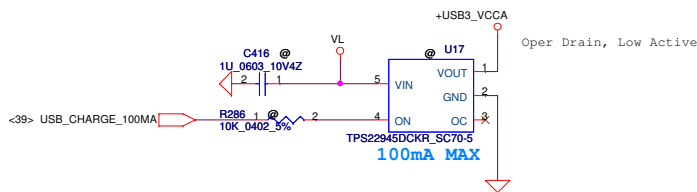
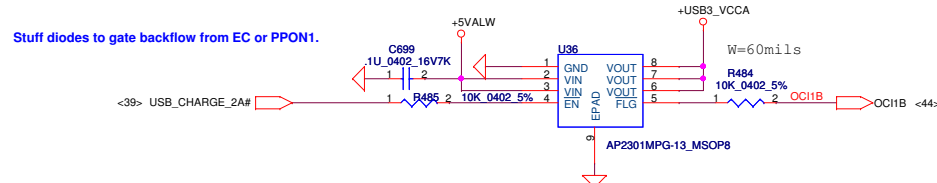
For EMI request



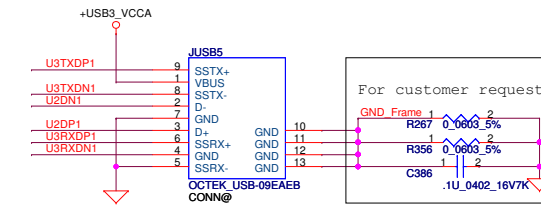
For ESD request



Stuff diodes to gate backflow from EC or PPON1.

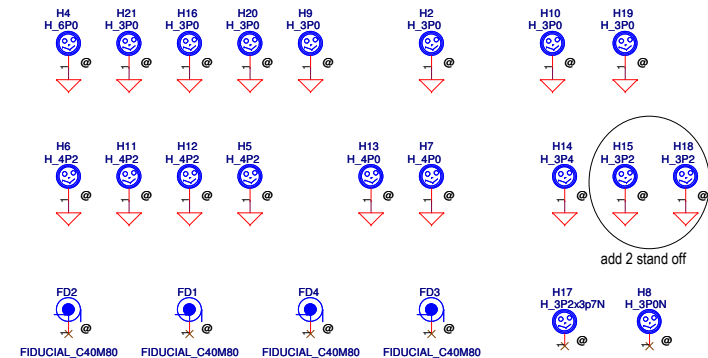
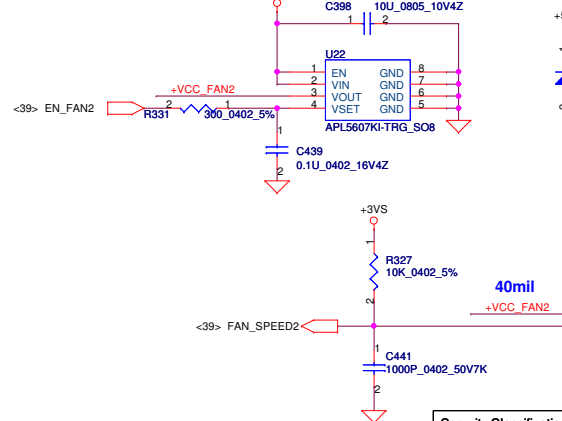
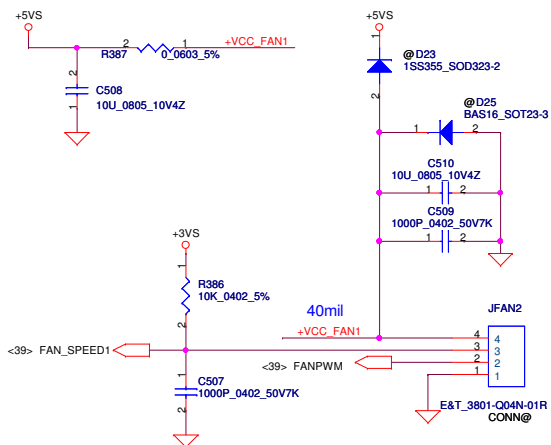


USB3.0 Connector

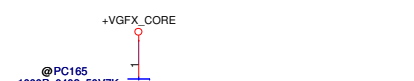
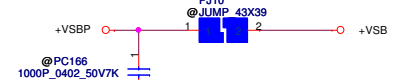
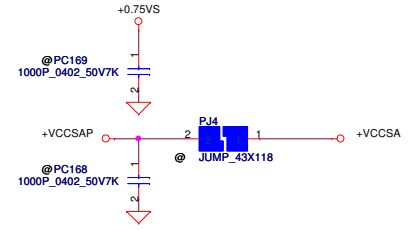
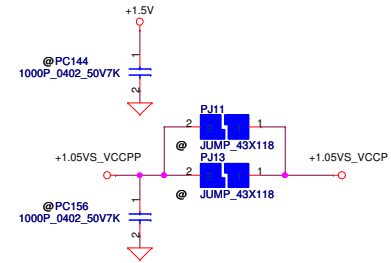
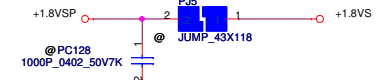
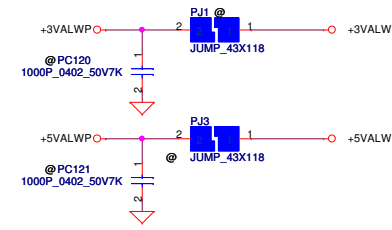
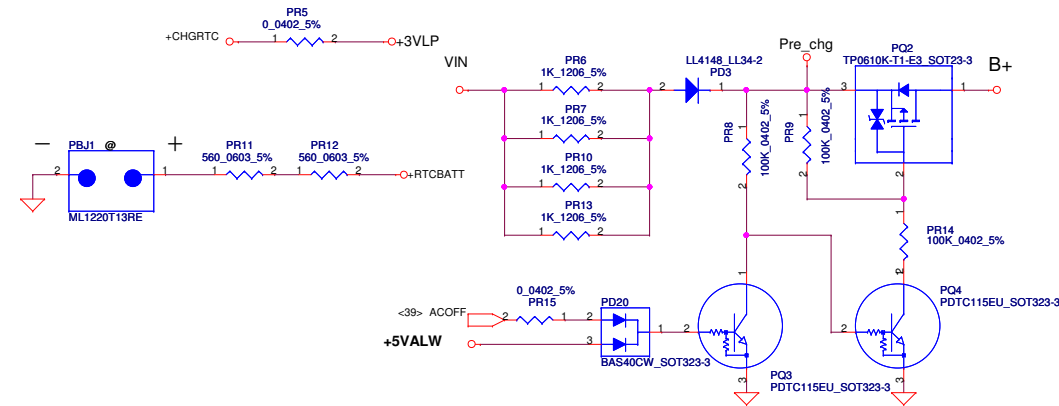
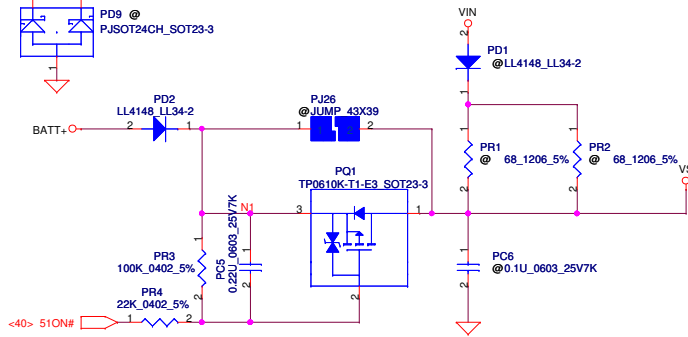
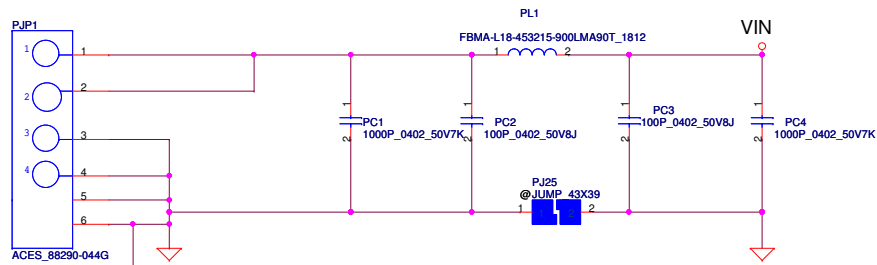


FAN1 Conn

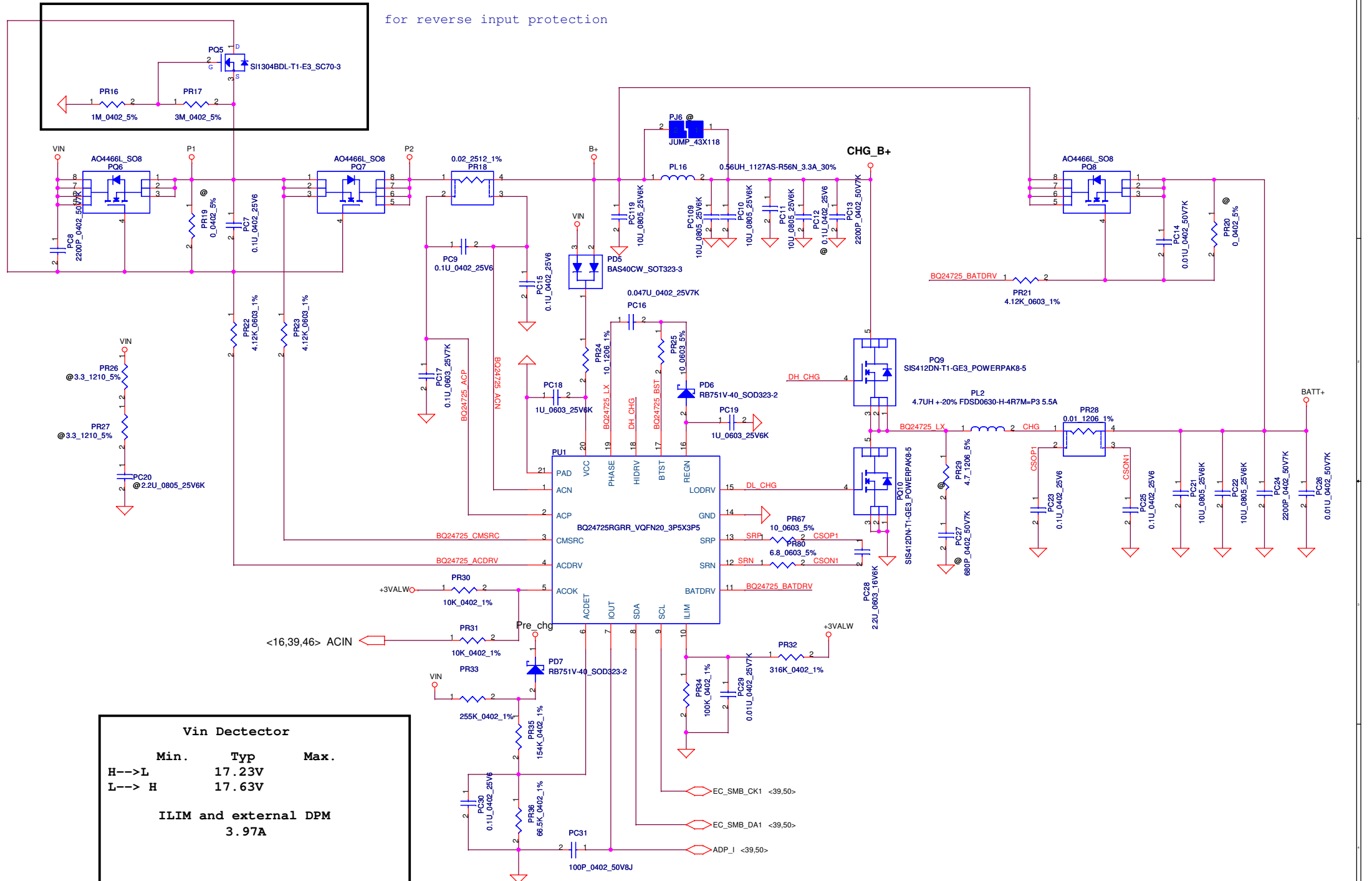
FAN2 Conn



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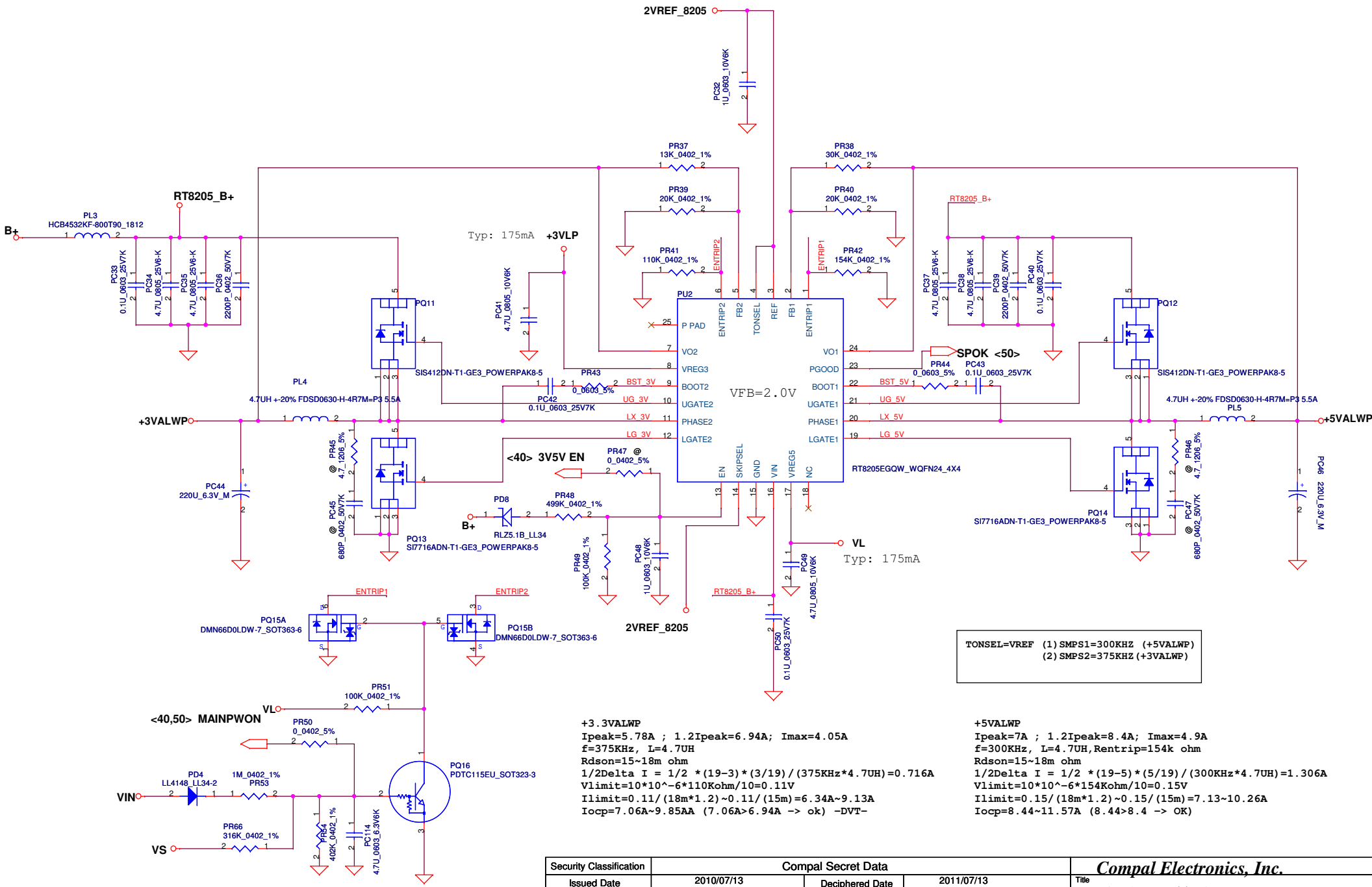
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Deciphered Date				2010/12/31				PWR DCIN / Pre-charge			
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for reverse input protection

Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.97A			

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Typ: 175mA

+3VLP

VFB=2.0V

Typ: 175mA

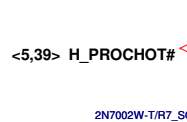
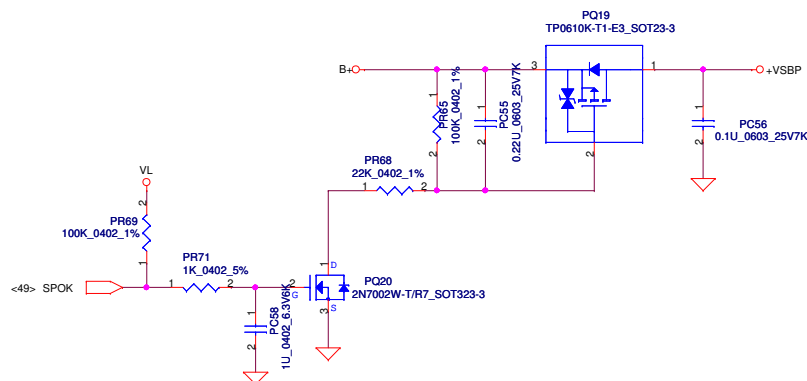
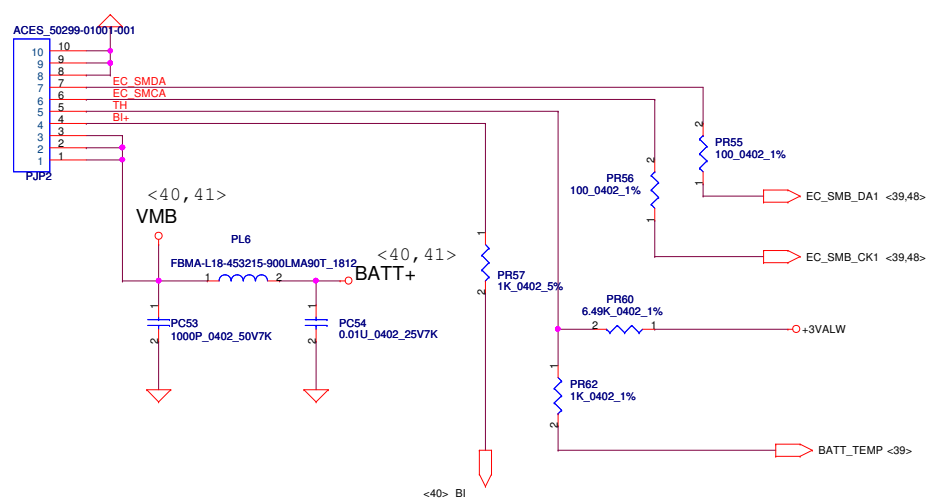
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(2) SMPS2=375KHZ (+3VALWP)

<40,50> MAINPWON

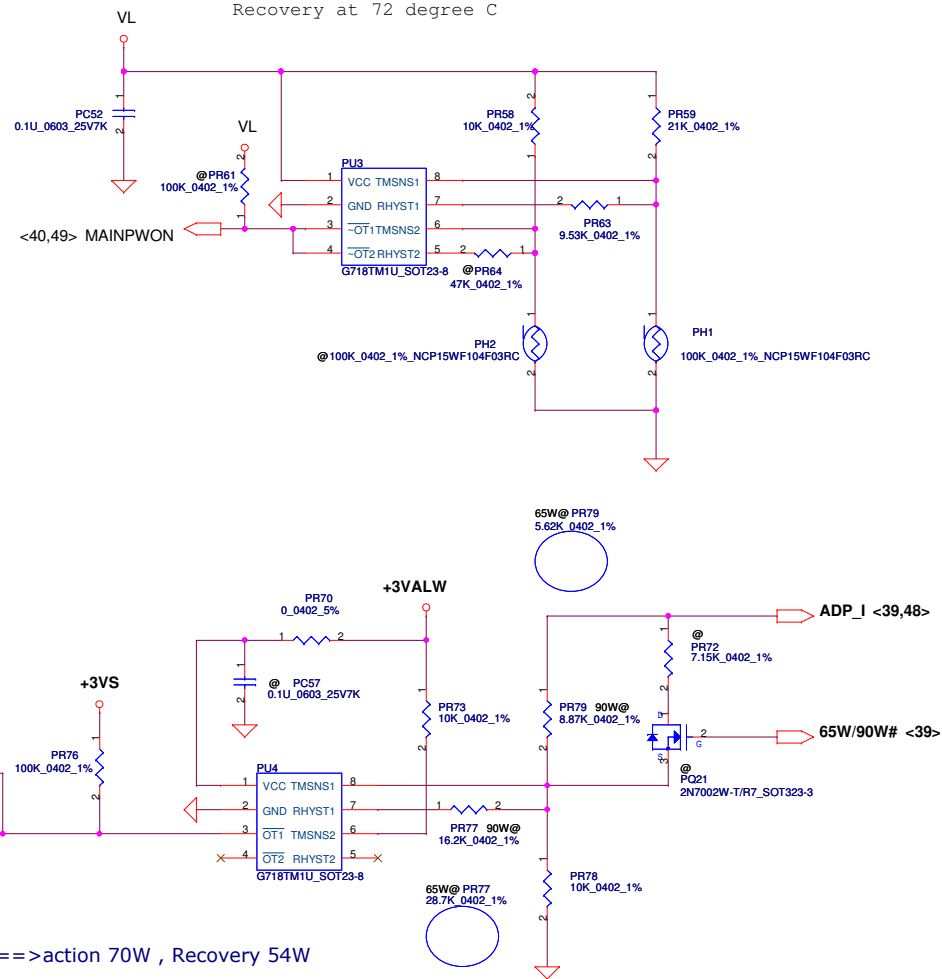
+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 * (19-3) * (3/19) / (375KHz*4.7UH)=0.716A
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH, Rentrrip=154K ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 * (19-5) * (5/19) / (300KHz*4.7UH)=1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)

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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W

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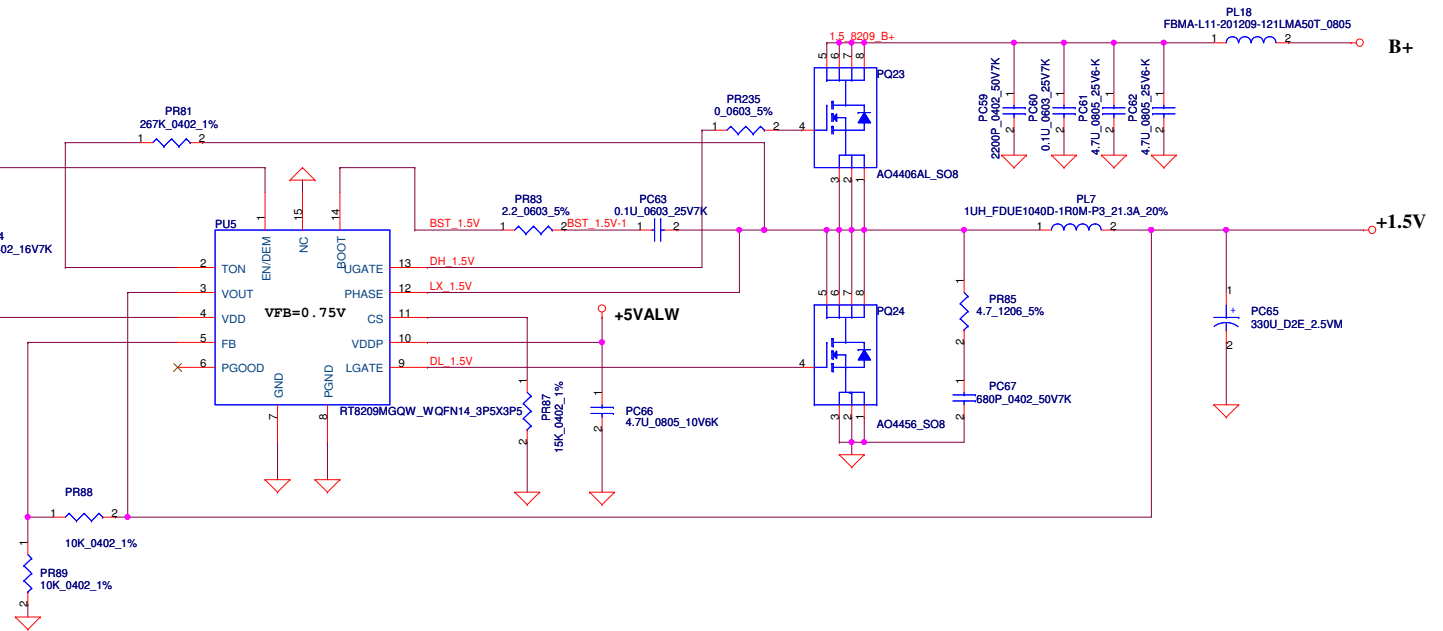
<39,44,46> SYSON

+5VALW

B+

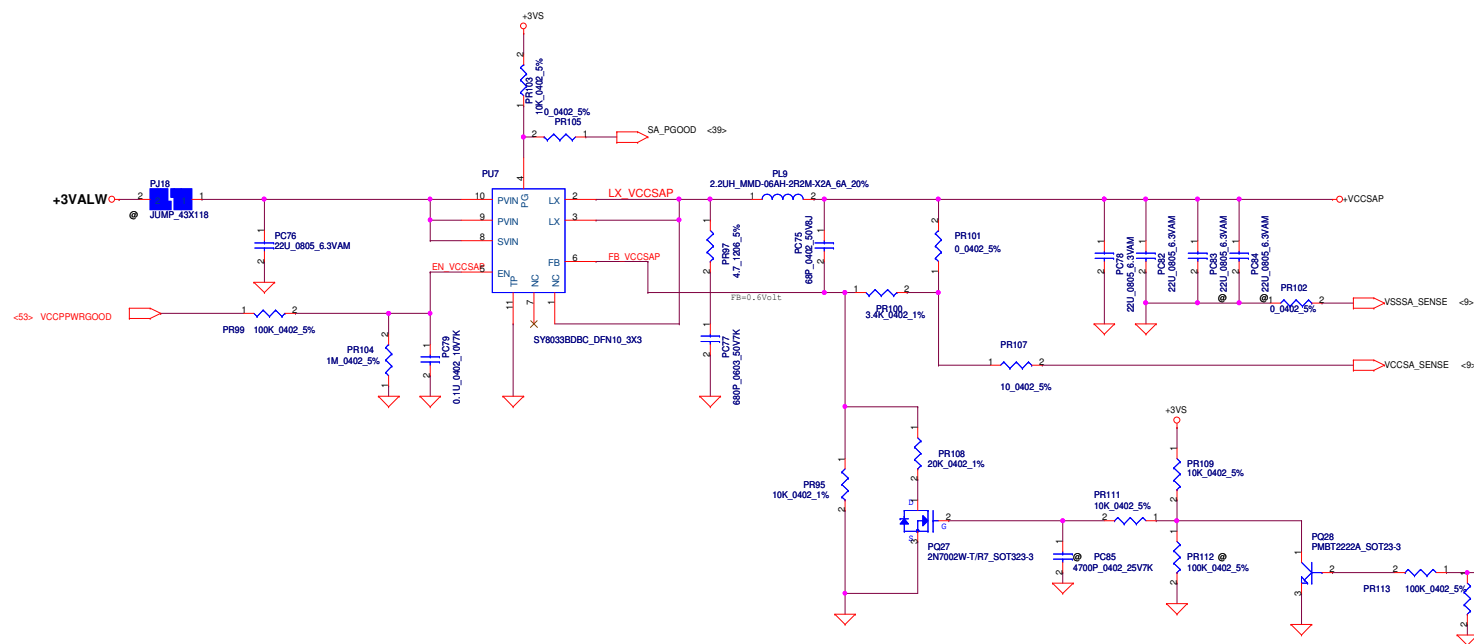
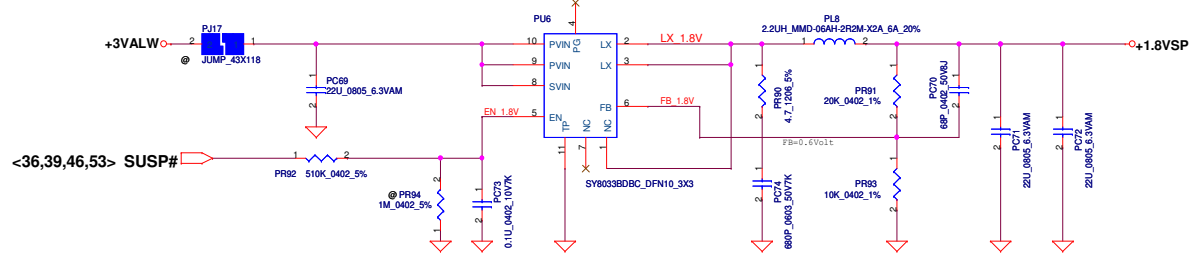
+1.5V

<Vo=1.5V> VFB=0.75V
 $V=0.75 \cdot (1+10K/10K)=1.5V$
 $F_{sw}=298KHz$
 $C_{out} ESR=15m \text{ ohm}$ $R_{dson(max)}=5.6 \text{ mohm}$ $R_{dson(typ)}=4.5 \text{ mohm}$.
 $I_{peak}=19.53A$, $I_{max}=23.44A$, $I_{ocp}=13.67A$
 $\Delta I=((19-1.5) \cdot (1.5/19)) / (L \cdot F_{sw})=4.63A$
 $\Rightarrow 1/2 \Delta I$ $I=2.315A$
choose $R_{cs}=15K$
 $I_{ocpmax}=(15K \cdot 11uA) / (0.0045)+2.315A=35.65A$
 $I_{ocpmin}=(15K \cdot 9uA) / (0.0056 \cdot 1.3)+2.315A=23.06A$
 $I_{ocp}=23.06A \sim 35.65A$



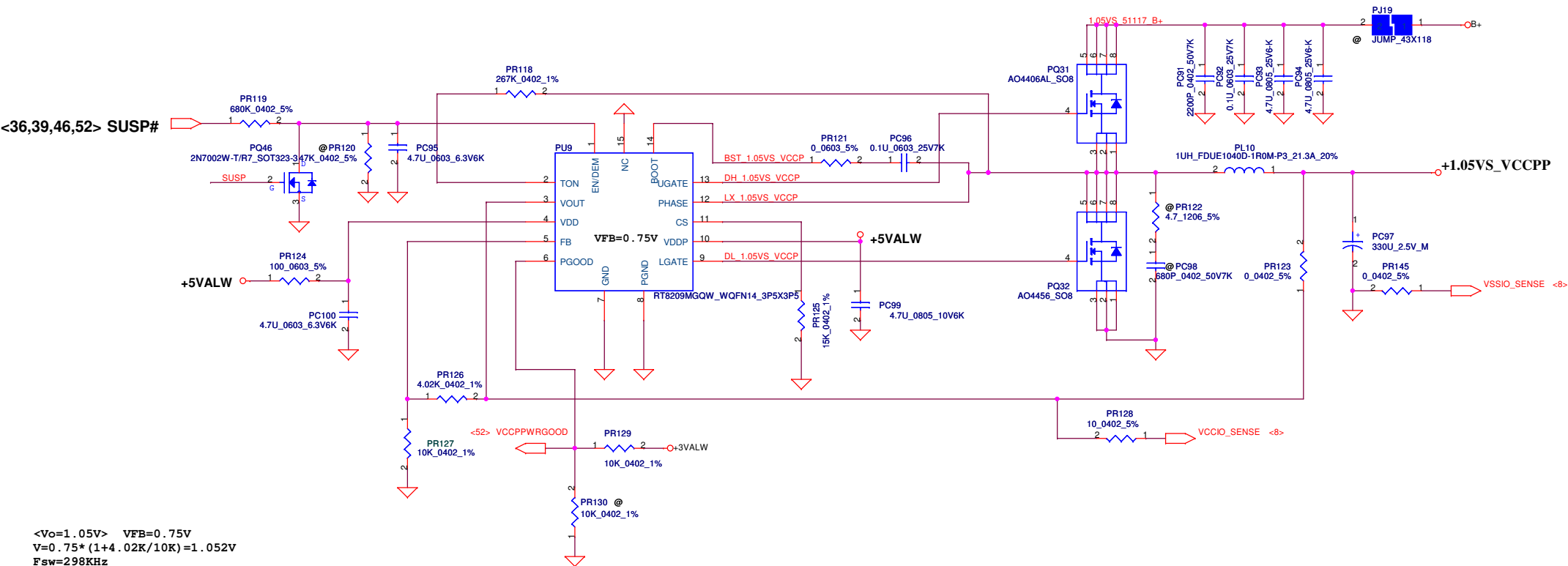
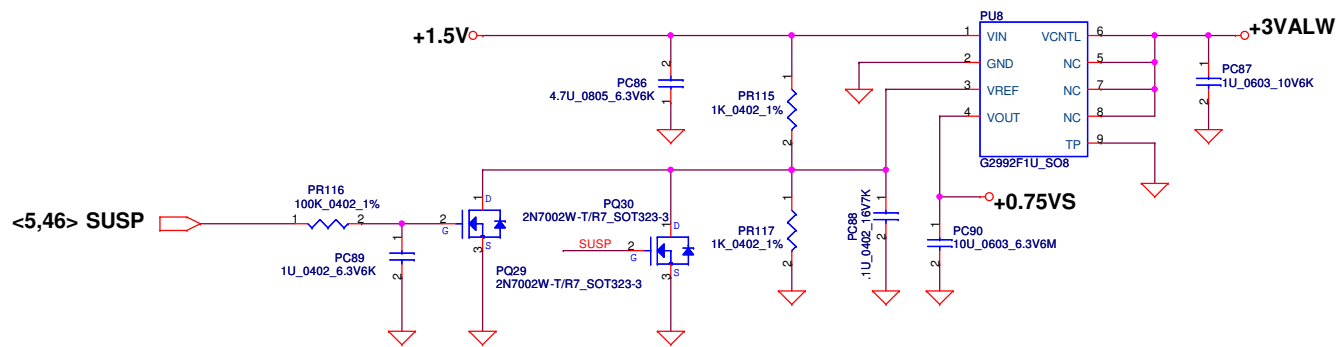
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1.8VSP
 $I_{peak}=3.35A$; $1.2I_{peak}=4.02$; $I_{max}=2.345A$
 $V_{out}=0.6 \cdot (1 + (20K/10K)) = 1.8V$



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
 (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



<Vo=1.05V> VFB=0.75V
 $V=0.75 * (1 + 4.02K/10K) = 1.052V$
 $Fsw=298KHz$

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
 $I_{peak}=12.866A$, $I_{max}=9A$, $I_{ocp}=15.439A$
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Fsw) = 3.33A$
 $\Rightarrow 1/2 \Delta I = 1.665A$
 choose Rcs=15K
 $I_{ocpmax} = ((15K * 11uA) / 0.0045) + 1.665A = 37.62A$
 $I_{ocpmin} = ((15K * 9uA) / (0.0056 * 1.3)) + 1.665A = 23.02A$
 $I_{ocp} = 23.02A \sim 37.62A$

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2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
 2-ph: PR172=169K Vboot=1.1V, Iccmax=54A

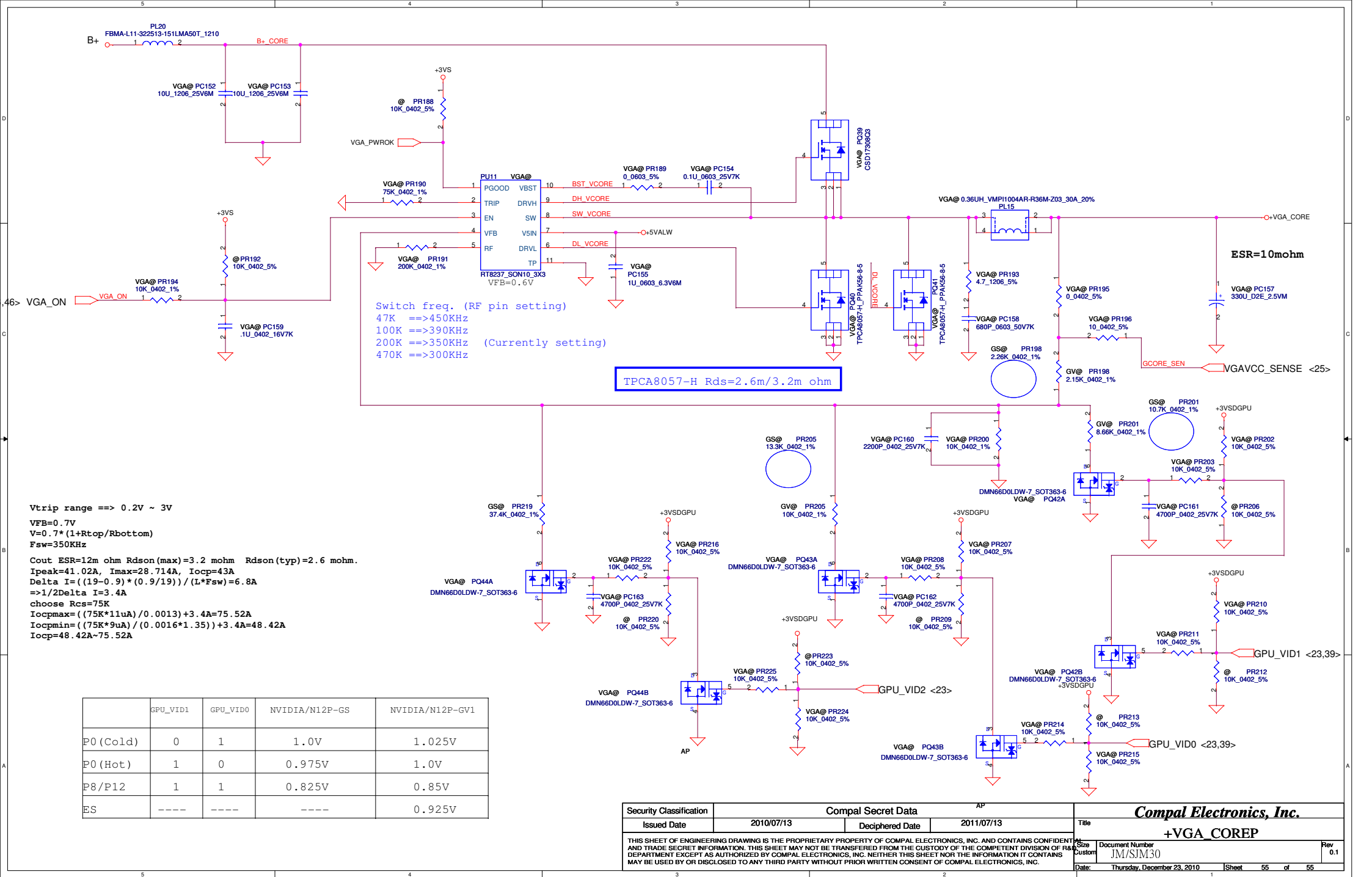
+CPU_CORE
 Iocp=70A, IccMAX=53A
 Load line=1.9mohm
 DCR=1.1mohm

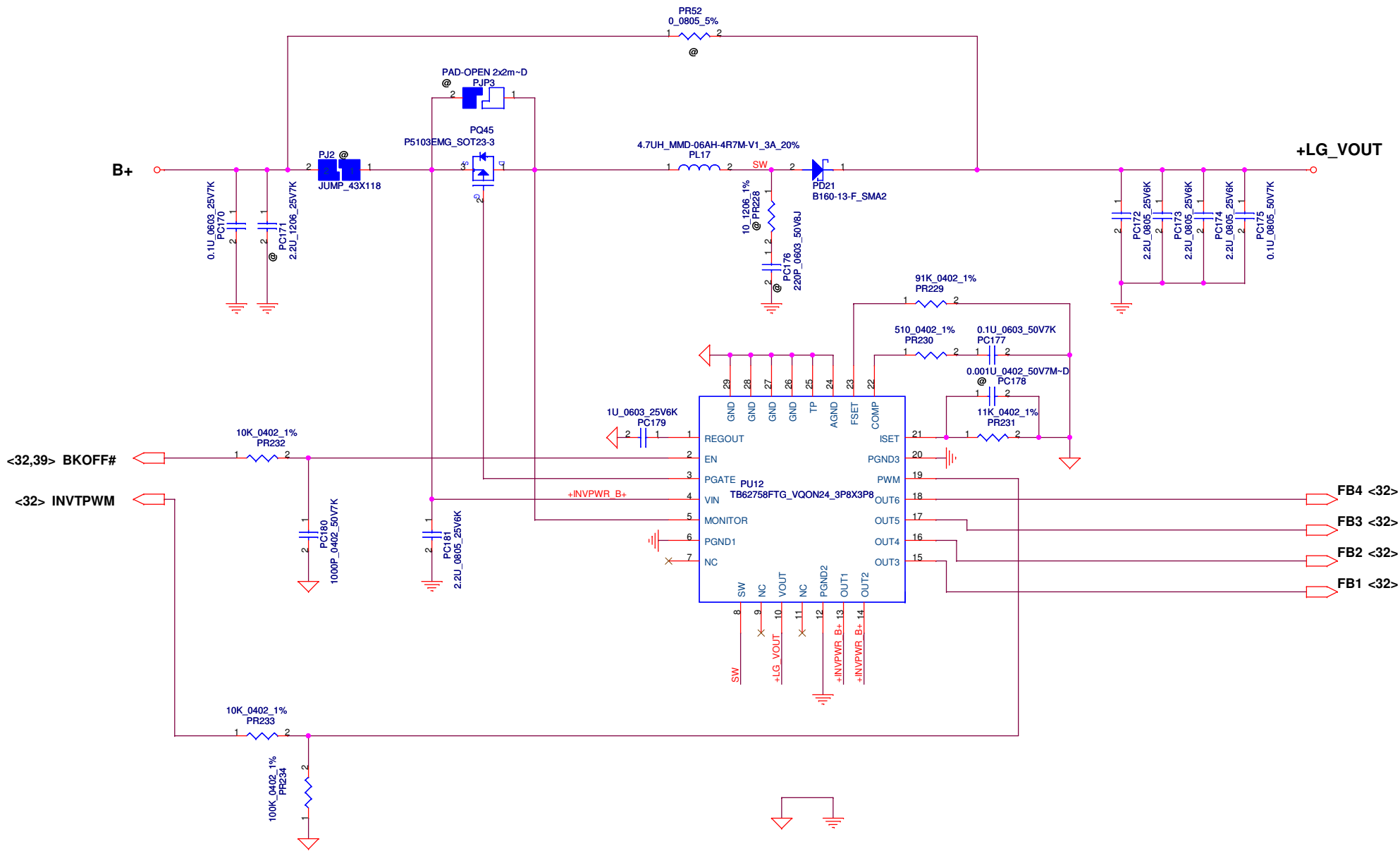
+GFX_CORE
 Iocp=40A, IccMAX=24A
 Load line=3.9mohm
 DCR=1.1mohm

2-ph: PR178=1.47K for -70A OCP

Connect to +5V can disable
 GFX portion

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