PHRAA

Superior 10/10G

LA-7211P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-01-31 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

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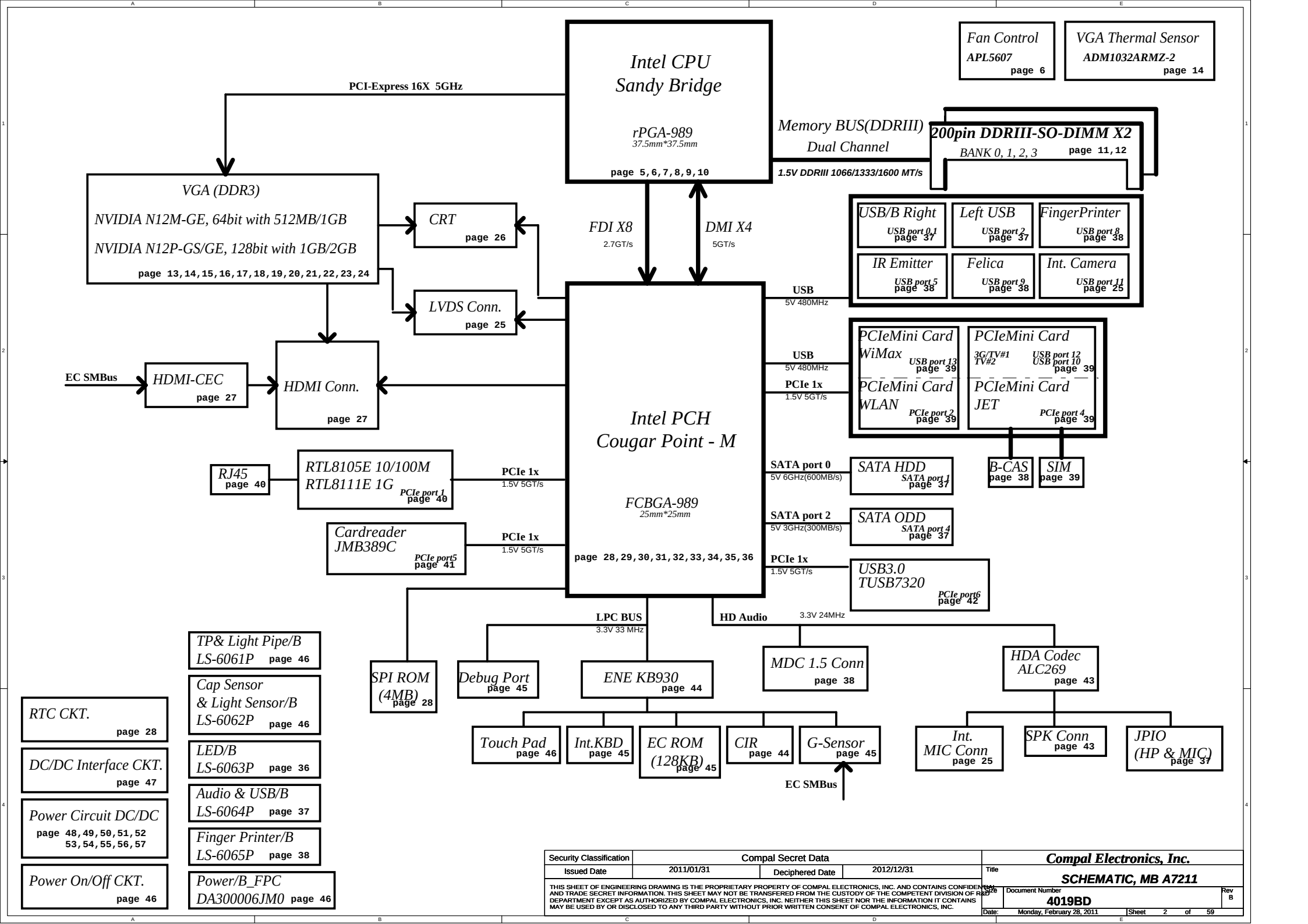
Title: *SCHEMATIC, MB A7211*		
Size: B	Document Number: 4019BD	Rev: B
Date: Monday, February 28, 2011	Sheet 1 of 59	



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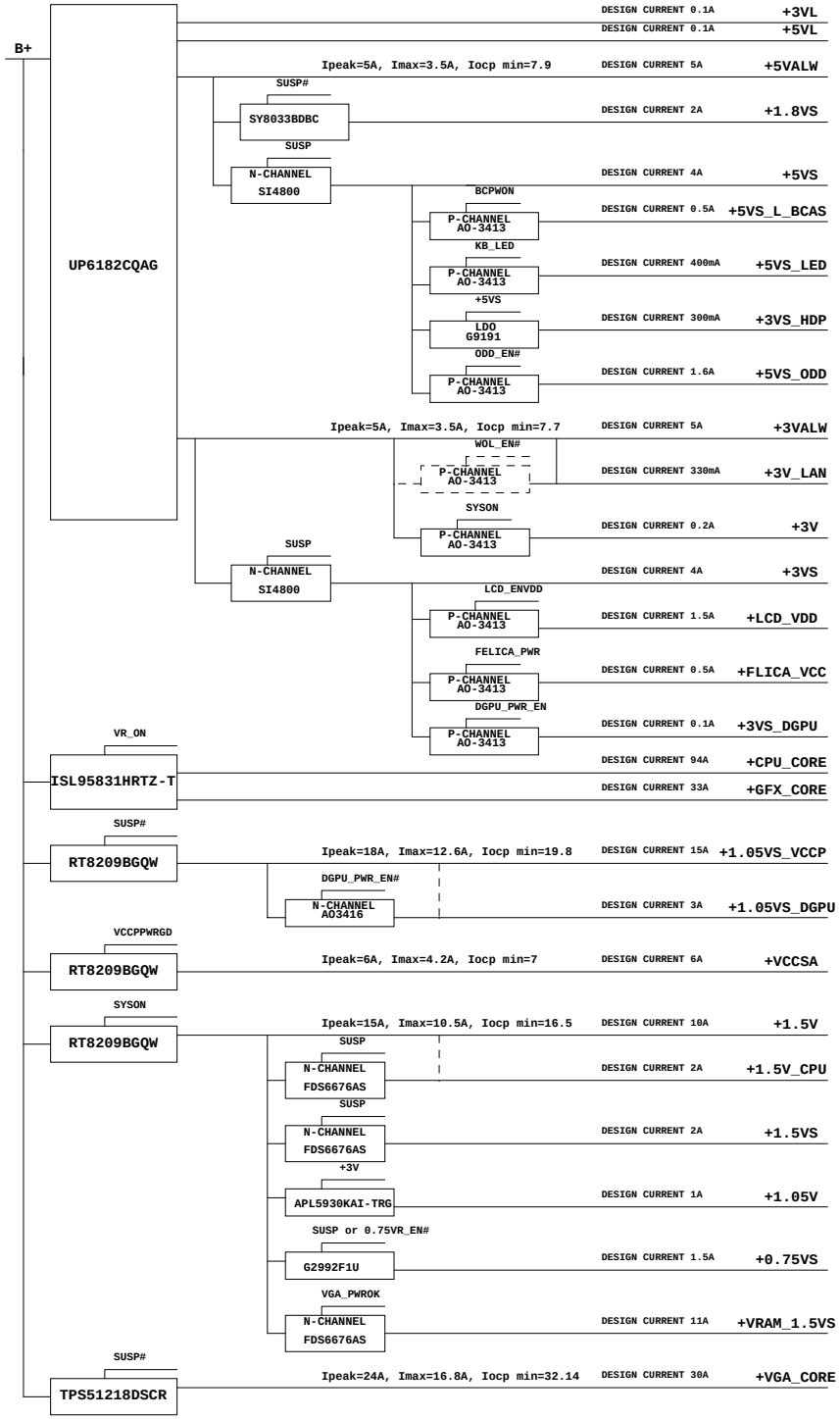
Size: | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 2 of 59



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Title: SCHEMATIC, MB A7211

Size: D | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 3 of 59

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b

Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9A H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b
+3VS	Light Sensor	52 H	0101 0010 b

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/ Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS			Camera & Mic
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel			Camera & Mic
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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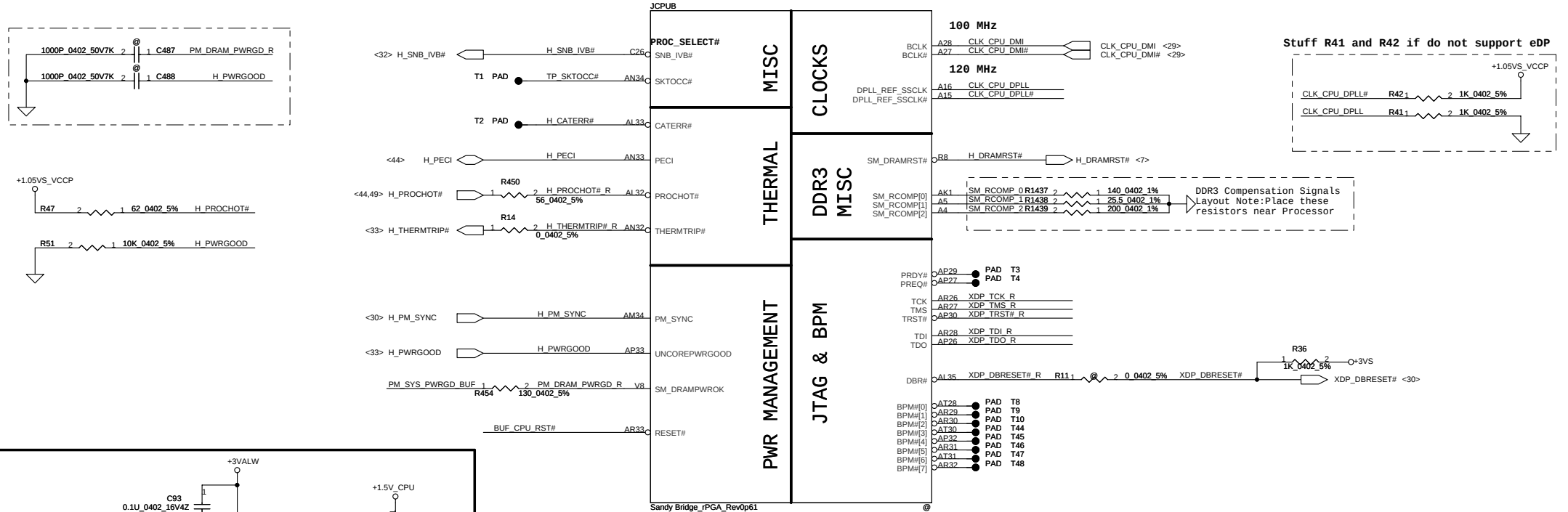
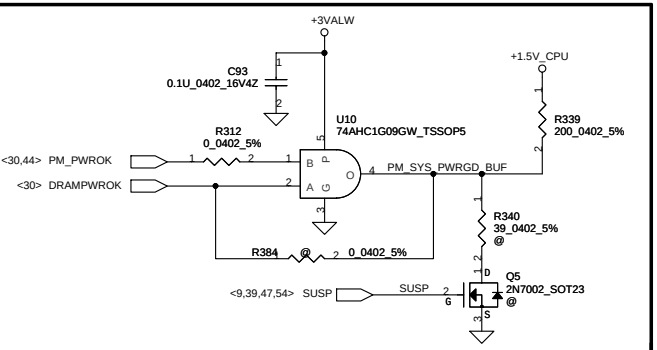
Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 | Sheet 4 of 59

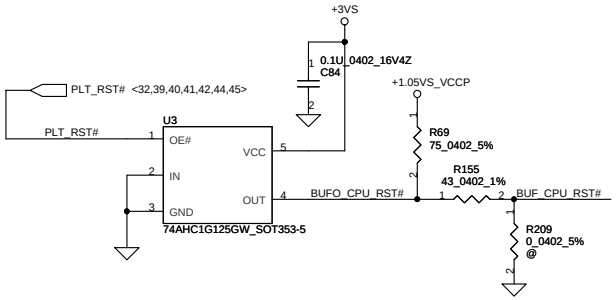


Stuff R41 and R42 if do not support eDP

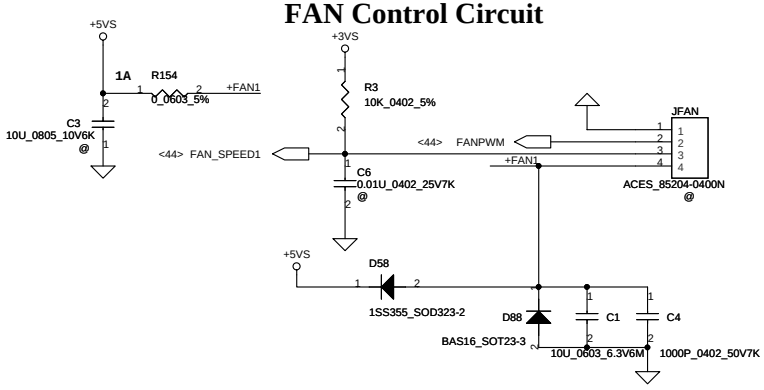
PU/PD for JTAG signals



Buffered Reset to CPU



FAN Control Circuit



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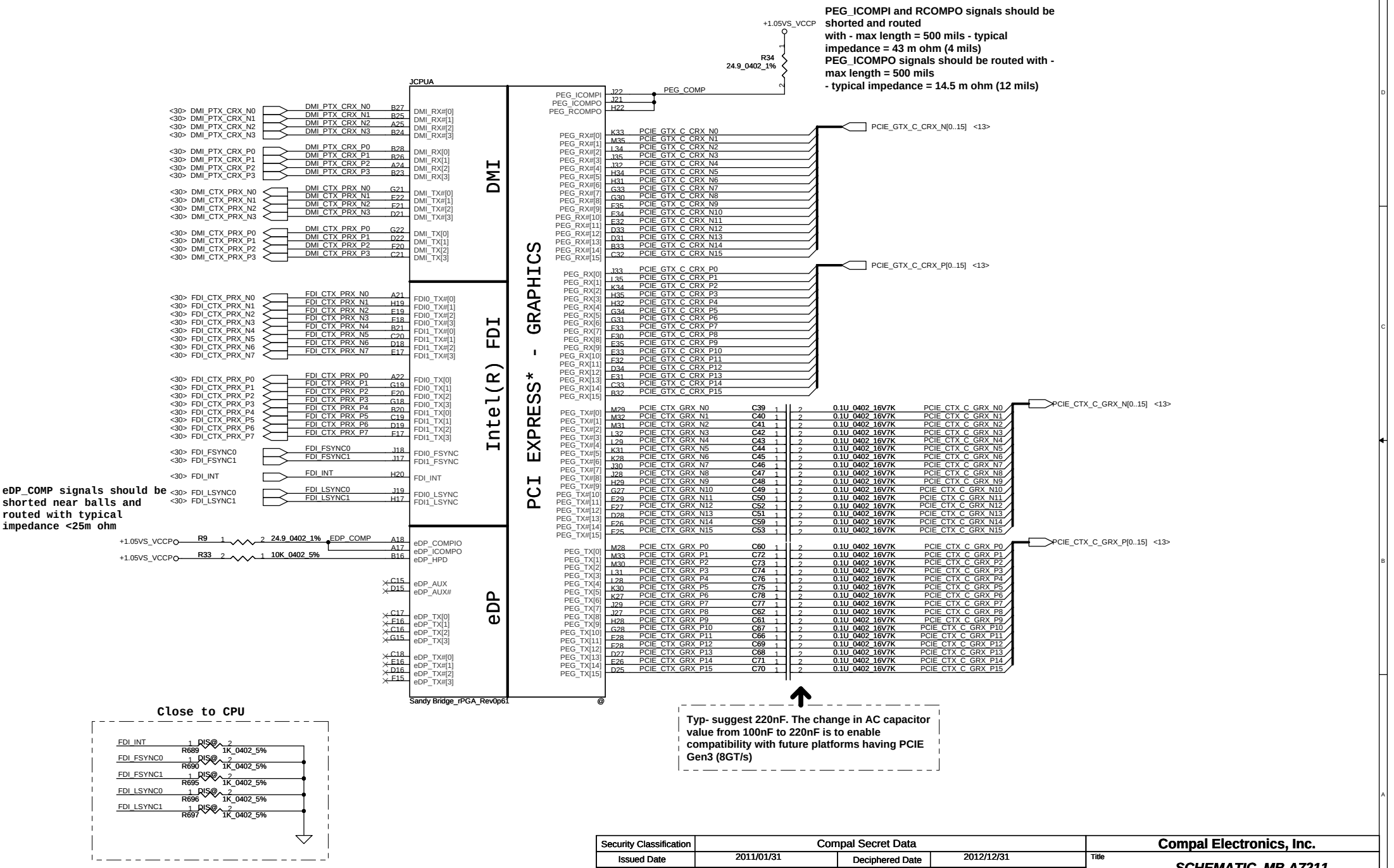
Size: Custom | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 5 of 59



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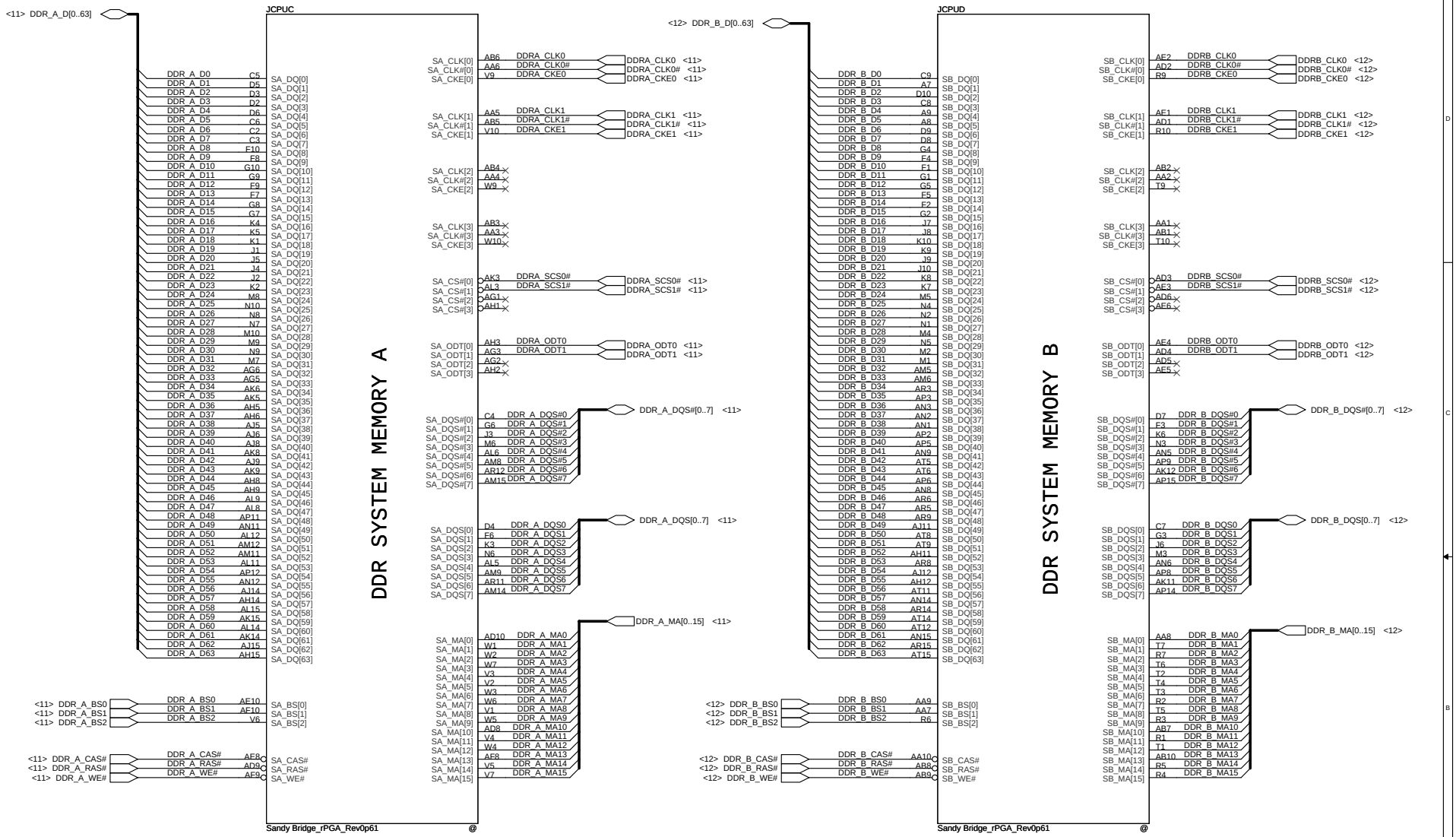
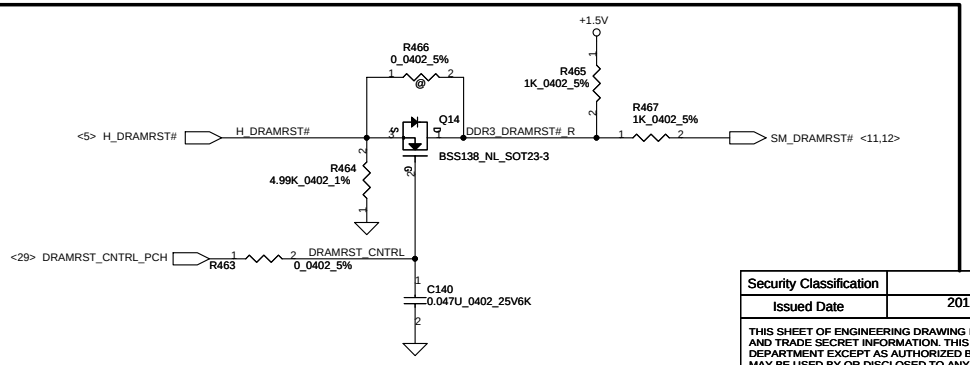
Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 6 of 59





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Size: Custom	Document Number: 4019BD			Rev: B
Date: Monday, February 28, 2011	Sheet 7 of 59			

POWER

JCPUF

94A (Quad Core 45W)
53A (SV 35W)

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+CPU_CORE

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

VSS_SENSE_VCC10

Sandy Bridge_rPGA_Rev0p61

+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

TOP Socket Cavity x 7

+1.05VS_VCCP

22U_0805_6.3V6M: C146 C144 C143 C141 C137 C136 C135 C134 C133 C142

22U_0805_6.3V6M: C147 C145 C163 @ C153 @ C160 @ C152 @ C139 @ C138 @ C132 @

Bottom Socket Cavity x 5

330U_D2_2V_Y

ESR 9mohm

C10 C11 C12 @

330U_D2_2V_Y

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

Bottom Socket Cavity

+CPU_CORE

10U_0805_10V6K: C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 @

Top Socket Edge

+CPU_CORE

22U_0805_6.3V6M: C159 C151 C130 C129 C124 C123 C122 C121 C125 @

Top Socket Cavity

+CPU_CORE

22U_0805_6.3V6M: C158 C150 C128 C127 C120 C118 C119 C117

+1.05VS_VCCP

R70 130_0402_5%

R68 75_0402_5%

VIDALERT#	AJ29	H_CPU_SVIDALRT#			VR_SVID_ALRT# <55>
VIDSCLK	AJ30	H_CPU_SVIDCLK	R67	43_0402_1%	VR_SVID_CLK <55>
VIDSOUT	AJ28	H_CPU_SVIDDAT	R63	0_0402_5%	VR_SVID_DAT <55>
			R66	0_0402_5%	

Pull high resistor on VR side

+CPU_CORE

R64 100_0402_1%

Close to CPU

VCC_SENSE	AJ35	VCCSENSE_R	R65	0_0402_5%	VCCSENSE <55>
VSS_SENSE	AJ34	VSSSENSE_R	R52	0_0402_5%	VSSSENSE <55>
VCCIO_SENSE	B10	VCCIO_SENSE			VCCIO_SENSE <54>
VSSIO_SENSE	A10				

R62 100_0402_1%

R102 0_0402_5%

R105 100_0402_1% @

+1.05VS_VCCP

Close to CPU

Co-Lay with C2, C5, C7, C9

+CPU_CORE

330U_D2_2V_Y

C890 C891 C894

@ @

470U_D2_2VM_R4.5M 470U_D2_2VM_R4.5M

TOP Socket Edge

+CPU_CORE

330U_D2_2V_Y

C2 C5 C7 C9

330U_D2_2V_Y 330U_D2_2V_Y 330U_D2_2V_Y

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Title: SCHEMATIC, MB A7211

Size: Custom | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 8 of 59

POWER

+GFX_CORE Decoupling:
2X 470U (4m ohm), 12X 22U

+GFX_CORE
ESR 17mohm
C873 330U_2.5V_M_R17 @

Bottom Socket Edge
Co-lay for Cost Down Plan

470U_D2_2V_C
C112 OPT@
C113 @ ESR 6mohm 330U_D2_2VM_R6M
R71 0_0402_5% DIS@

Bottom Socket Cavity

22U_0805_6.3V6M: C266 C267 C271 C338 C341 C342 (OPT@)
22U_0805_6.3V6M: C343 C344 C345 C346 C347 C348 (OPT@)
22U_0805_6.3V6M: C349 C350 C351 C391 (@)

Bottom Socket Edge

Top Socket Cavity

Top Socket Edge

JCPUG

33A

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES

VAXG_SENSE
VSSAXG_SENSE

AK35 VCC_AXG_SENSE_R R121 OPT@ 0_0402_5%
AK34 VSS_AXG_SENSE_R R251 OPT@ 0_0402_5%

+GFX_CORE
R74 100_0402_1% OPT@
R75 100_0402_1% OPT@
Close to CPU

VCC_AXG_SENSE <55>
VSS_AXG_SENSE <55>

VREF

SM_VREF

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU
R111 0_0402_5%
R122 1K_0402_0.5%
AL1 +V_SM_VREF_CNT
Q2 @ AP2302GN-HF_SOT23-3
+V_SM_VREF
R252 1K_0402_0.5%
R486 100K_0402_5%
C148 0.1U_0402_16V4Z
RUN_ON_CPU1.5VS3

DDR3 -1.5V RAILS

5A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15

AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

10U_0805_10V6K: C114 C115 C116 C149 C154 C155
ESR 6mohm C180 @ 330U_D2_2VM_R6M

+1.5V_CPU Decoupling:
1X 330U (6m ohm), 6X 10U

+1.5V_CPU
ESR 17mohm C875 330U_2.5V_M_R17

Co-lay for Cost Down Plan

SA RAIL

6A

VCCSA1 VCCSA2 VCCSA3 VCCSA4 VCCSA5 VCCSA6 VCCSA7 VCCSA8

M27 M26 L26 J26 J25 J24 H26 H25

Bottom Socket Cavity

10U_0805_10V6K: C100 C447 C476 C477 (@)
+VCCSA
R253 0_0402_5%
C485 @ 330U_D2_2VM_R6M

Bottom Socket Edge

Co-lay for Cost Down Plan

+VCCSA
ESR 17mohm C877 @ 330U_2.5V_M_R17

+VCCSA Decoupling:
1X 330U (6m ohm), 3X 10U

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge

1.8V RAIL

1.2A

VCCPLL1 VCCPLL2 VCCPLL3

+1.8VS
R76 0_0805_5%
10U_0805_10V6K
+1.8VS_VCCPLL
B6 A6 A2
C185 @ 330U_B2_2.5VM_R15M
C186 C206 1U_0402_6.3V6K
C230 1U_0402_6.3V6K

VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2x1U

MISC

VCCSA_SENSE H23 VCCSA_SENSE
R95 0_0402_5% @
VCCSA_SENSE <53>

VCCSA_VID0
FC_C22 C22 VCCSA_VID0
VCCSA_VID1 C24
VCCSAP_VID1 <53>

R114 10K_0402_5%
R119 @ 10K_0402_5%

Reserve it to follow CRB 1.0.

Sandy Bridge_rPGA_Rev0p61

+1.5V_CPU
C213 C212 C211 C210 0.1U_0402_16V4Z
+1.5V

Vgs=10V,Id=14.5A,Rds=6mohm

+1.5V_CPU +1.5VS
PJ30 @ JUMP_43X118
Q33 FDS6676AS_SO8
+1.5V
R449 470_0805_5%
C179 10U_0805_10V4K
R455 220K_0402_5%
RUN_ON_CPU1.5VS3
+VSB
Q46B 2N7002DW-T/R7_SOT363-6
SUSP
C472 0.1U_0402_25V6
R420 820K_0402_5%
Q46A 2N7002DW-T/R7_SOT363-6
SUSP
SUSP <5,39,47,54>

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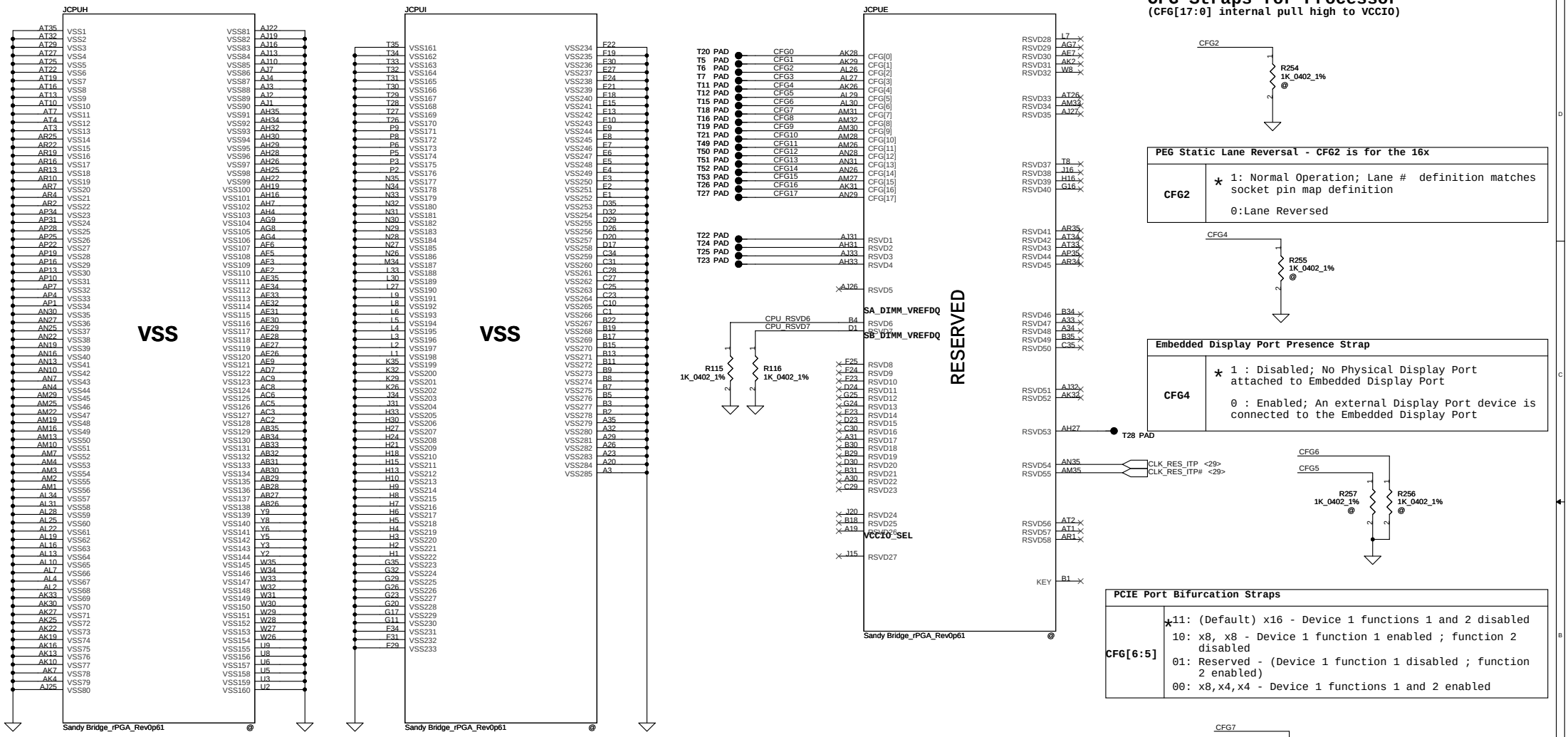

CFG Straps for Processor

(CFG[17:0] internal pull high to VCCIO)

CFG2

R254 1K_0402_1% @

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4

R255 1K_0402_1% @

Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG6

CFG5

R257 1K_0402_1% @

R256 1K_0402_1% @

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7

R258 1K_0402_1% @

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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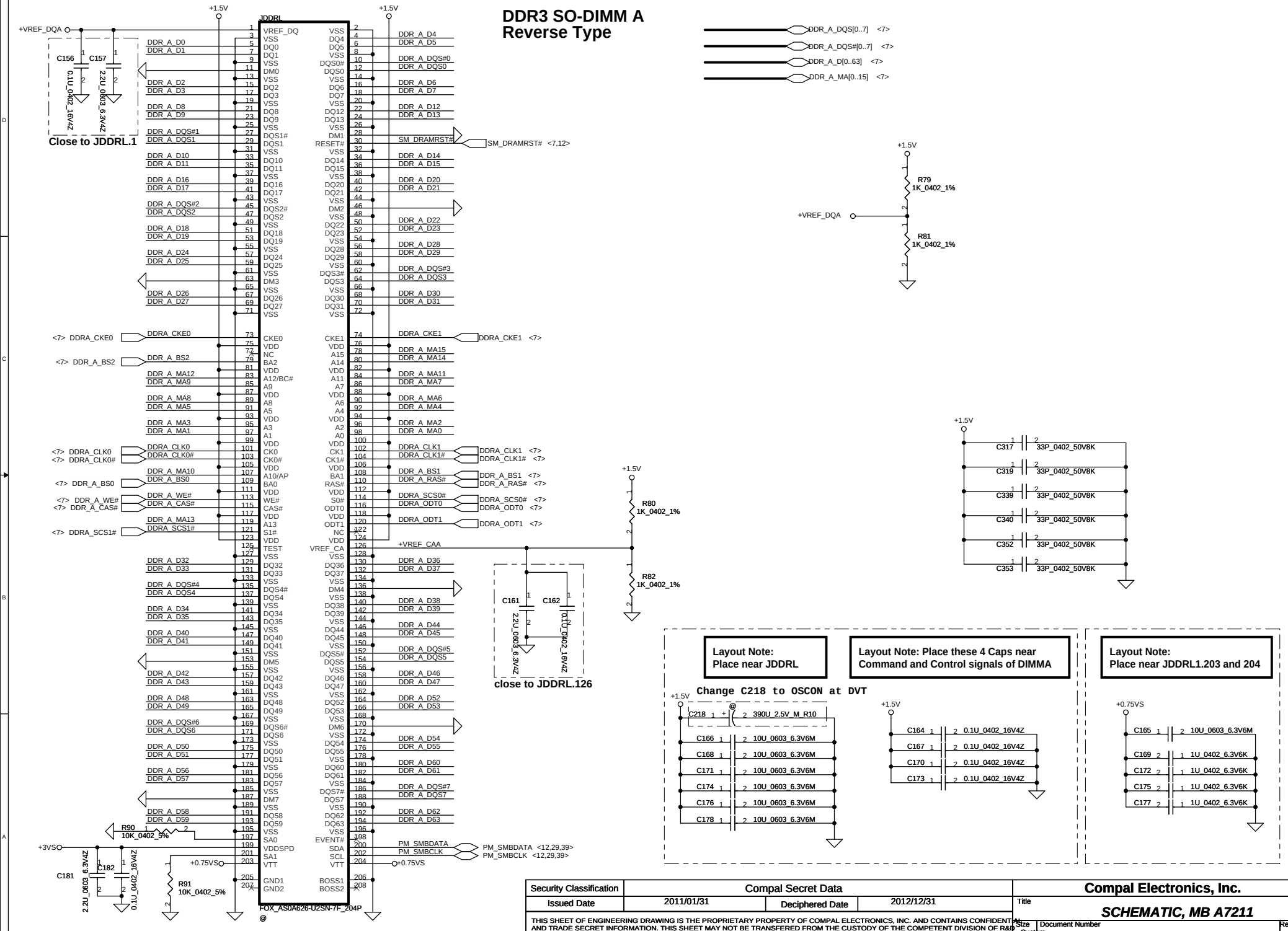
Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 10 of 59

DDR3 SO-DIMM A
Reverse Type



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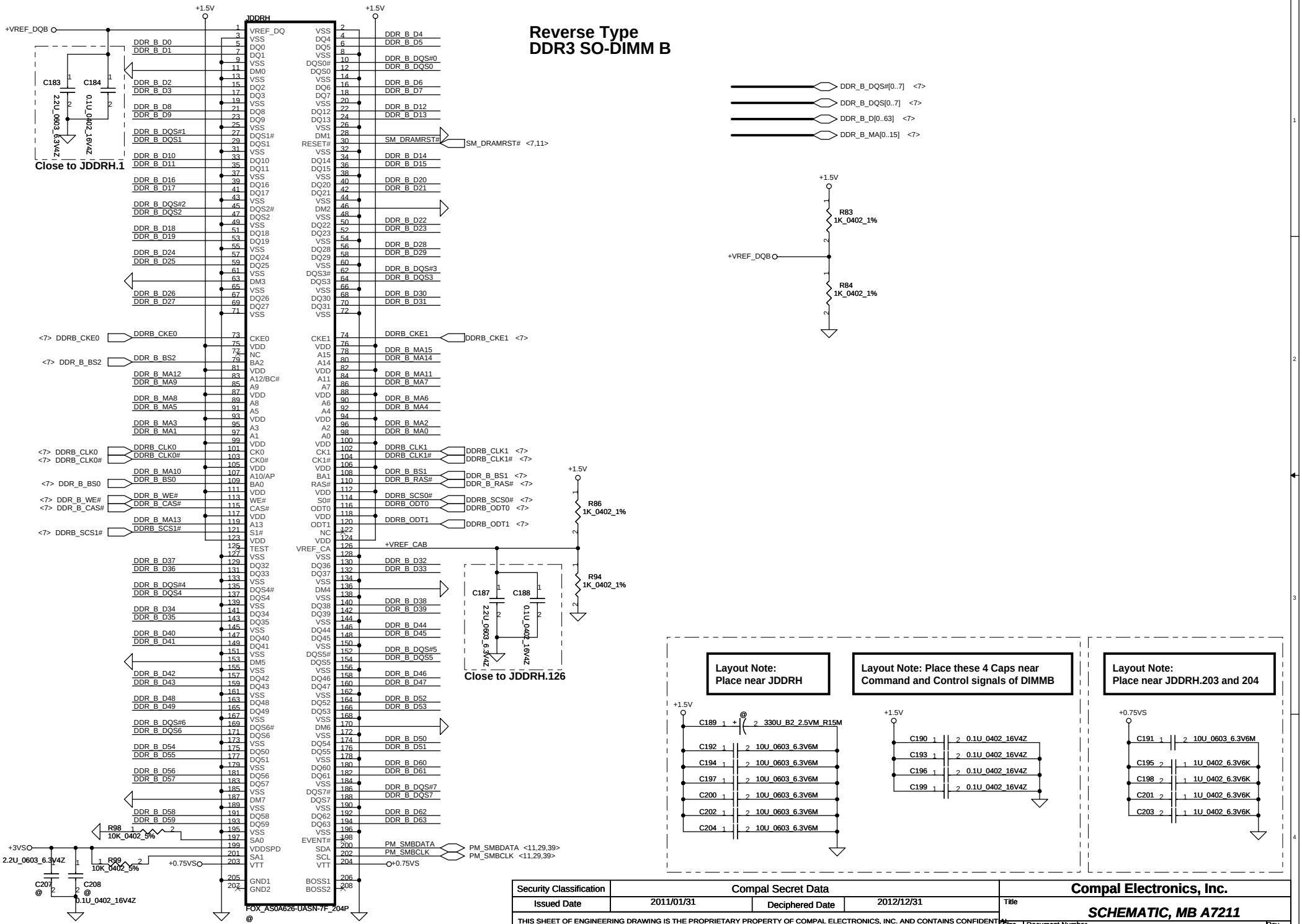
Date: Monday, February 28, 2011 | Sheet 11 of 59

Reverse Type
DDR3 SO-DIMM B



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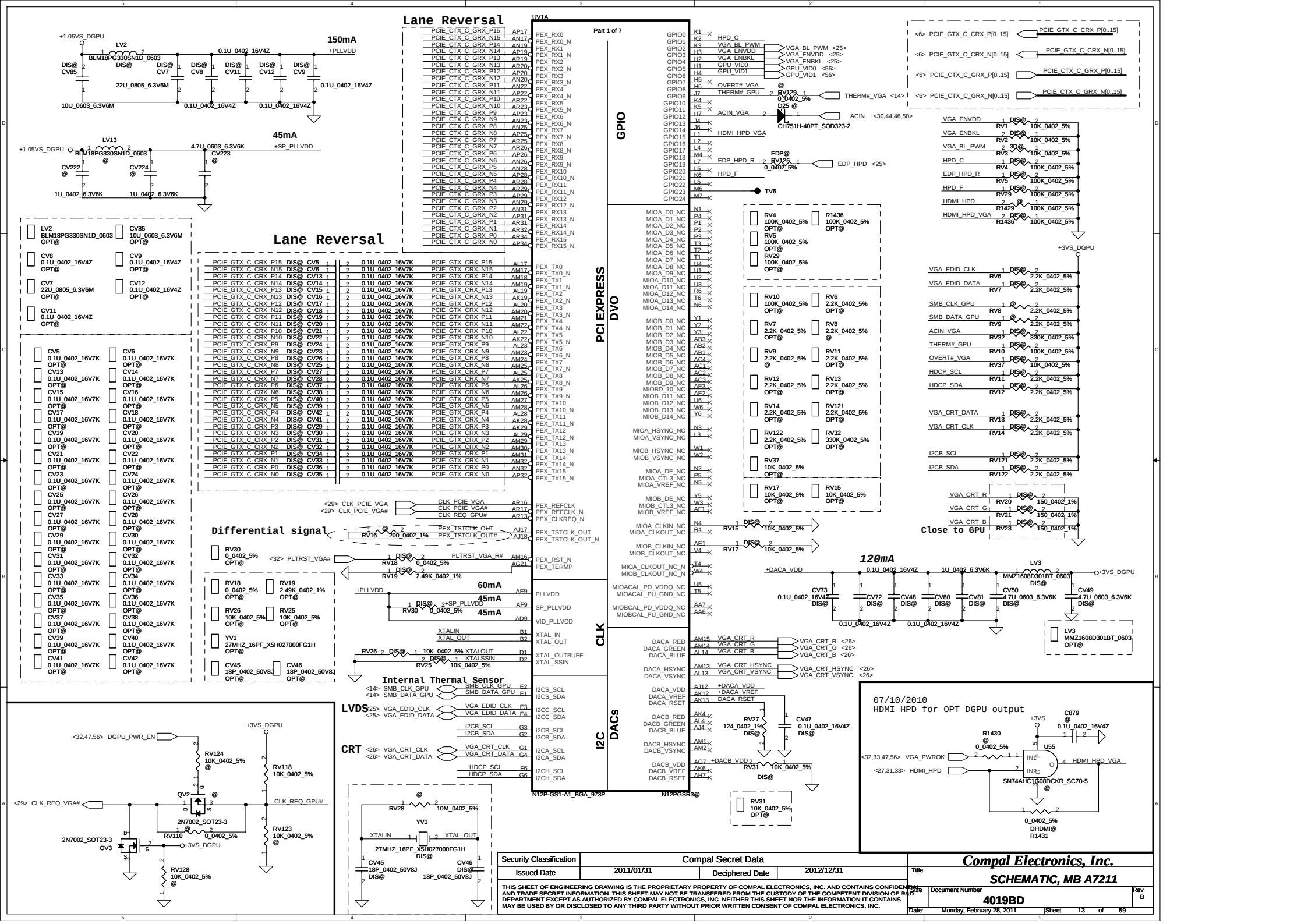

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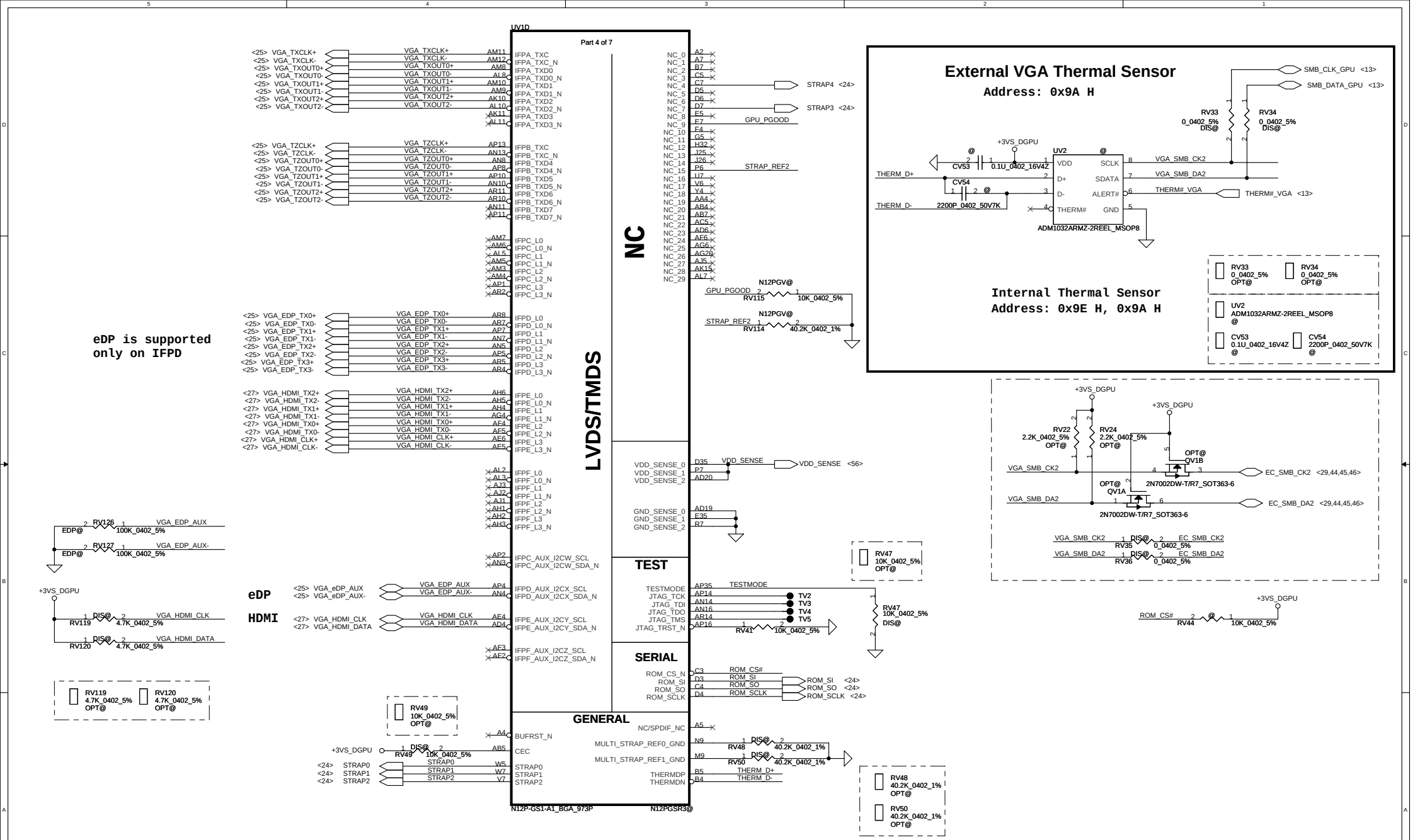

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Size	Document Number	Rev
	4019BD	B

Date: Monday, February 28, 2011 | Sheet 14 of 59

For PHQAA EVT Phase only

Mode	VID1	VID0	+VGA_CORE
P0(Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

N12M-GE Performance Mode

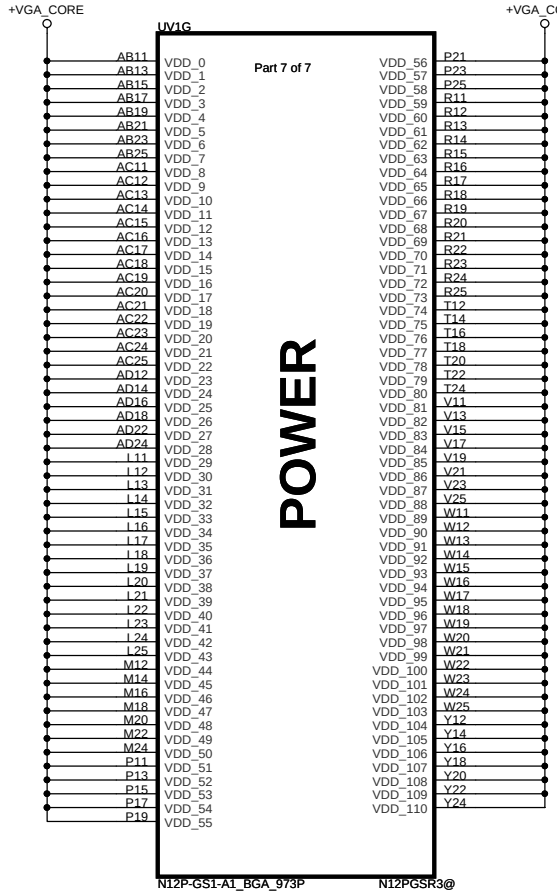
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GS Performance Mode

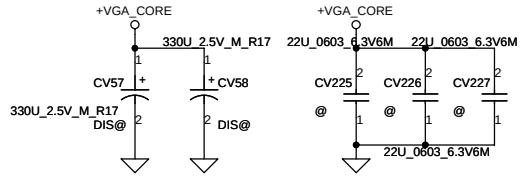
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

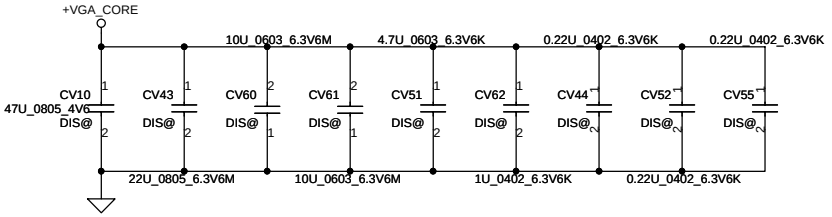
N12P-GE Performance Mode

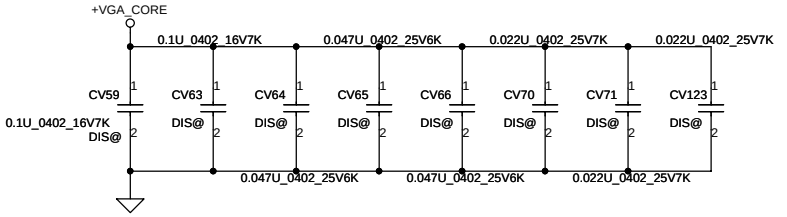
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

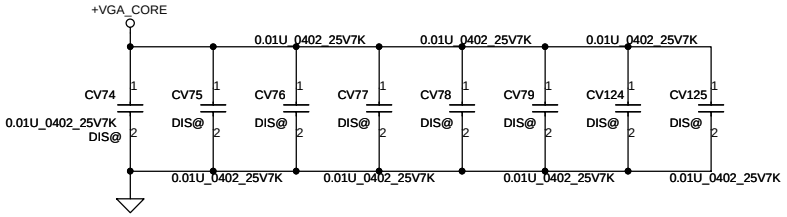


32A for N11E-GE1-LP
28A for N11P-GE1
16A for N11M-GE1 & N11M-OP1
14A for N11M-GE2









CV225	22U_0603_6.3V6M	@	
CV226	22U_0603_6.3V6M	@	
CV227	22U_0603_6.3V6M	@	
CV57	330U_2.5V_M_R17	OPT@	
CV58	330U_2.5V_M_R17	OPT@	
CV10	47U_0805_4V6	OPT@	
CV43	22U_0805_6.3V6M	OPT@	
CV60	10U_0603_6.3V6M	OPT@	
CV61	10U_0603_6.3V6M	OPT@	
CV51	4.7U_0603_6.3V6K	OPT@	
CV62	1U_0402_6.3V6K	OPT@	
CV44	0.22U_0402_6.3V6K	OPT@	
CV52	0.22U_0402_6.3V6K	OPT@	
CV55	0.22U_0402_6.3V6K	OPT@	
CV59	0.1U_0402_16V7K	OPT@	
CV63	0.1U_0402_16V7K	OPT@	
CV64	0.047U_0402_25V6K	OPT@	
CV65	0.047U_0402_25V6K	OPT@	
CV66	0.047U_0402_25V6K	OPT@	
CV70	0.022U_0402_25V7K	OPT@	
CV71	0.022U_0402_25V7K	OPT@	
CV123	0.022U_0402_25V7K	OPT@	
CV74	0.01U_0402_25V7K	OPT@	
CV75	0.01U_0402_25V7K	OPT@	
CV76	0.01U_0402_25V7K	OPT@	
CV77	0.01U_0402_25V7K	OPT@	
CV78	0.01U_0402_25V7K	OPT@	
CV79	0.01U_0402_25V7K	OPT@	
CV124	0.01U_0402_25V7K	OPT@	
CV125	0.01U_0402_25V7K	OPT@	

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

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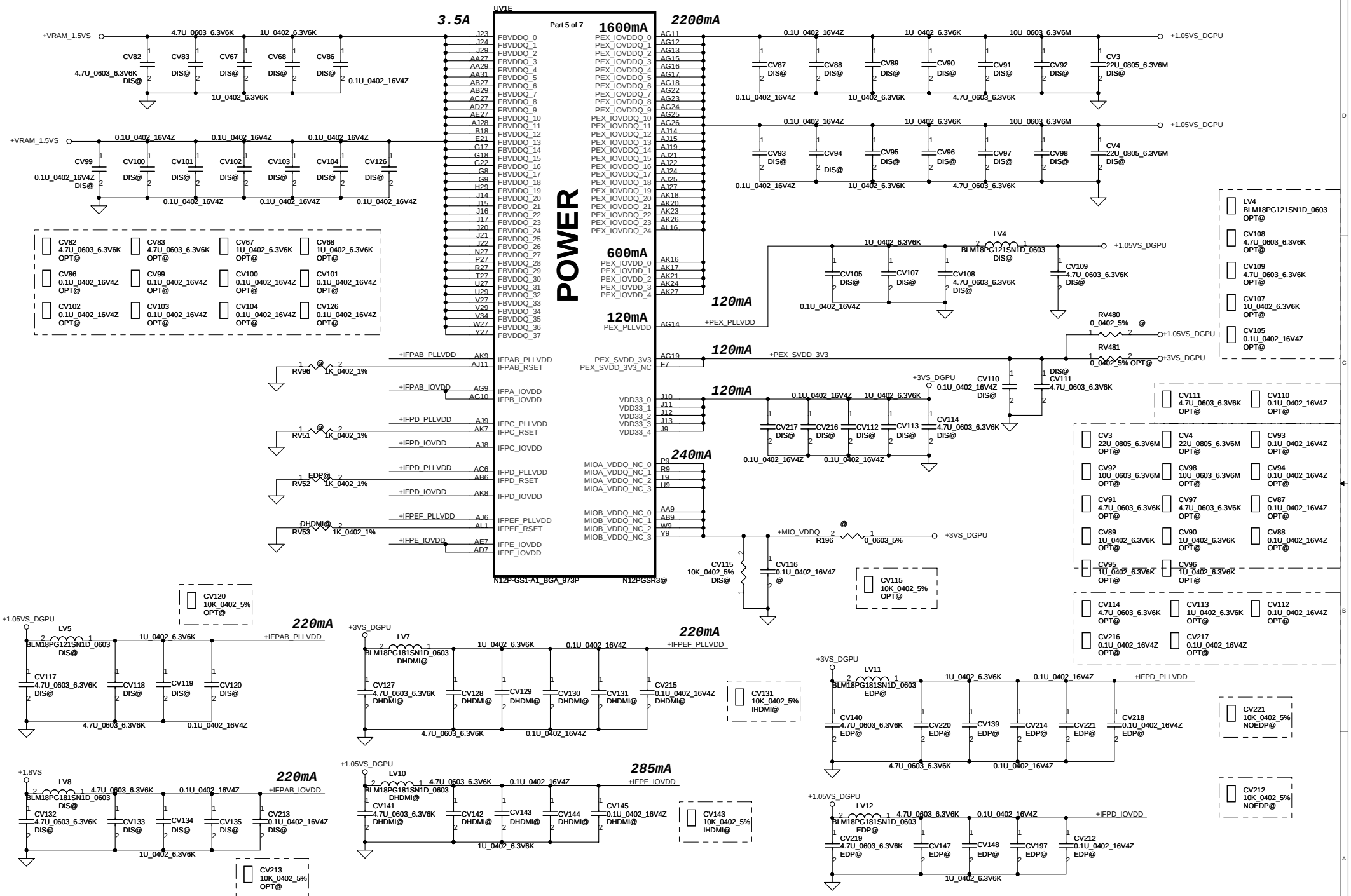
Title: **SCHEMATIC, MB A7211**

Size | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 15 of 59



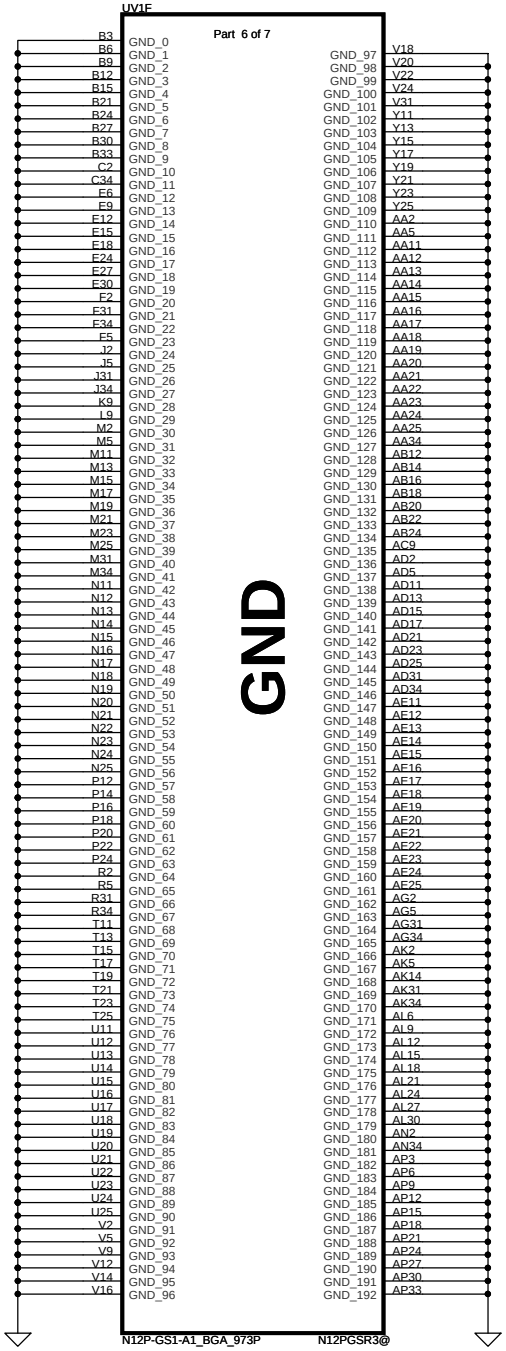
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size	Document Number	Rev
	4019BD	B

Date: Monday, February 28, 2011 | Sheet 16 of 59



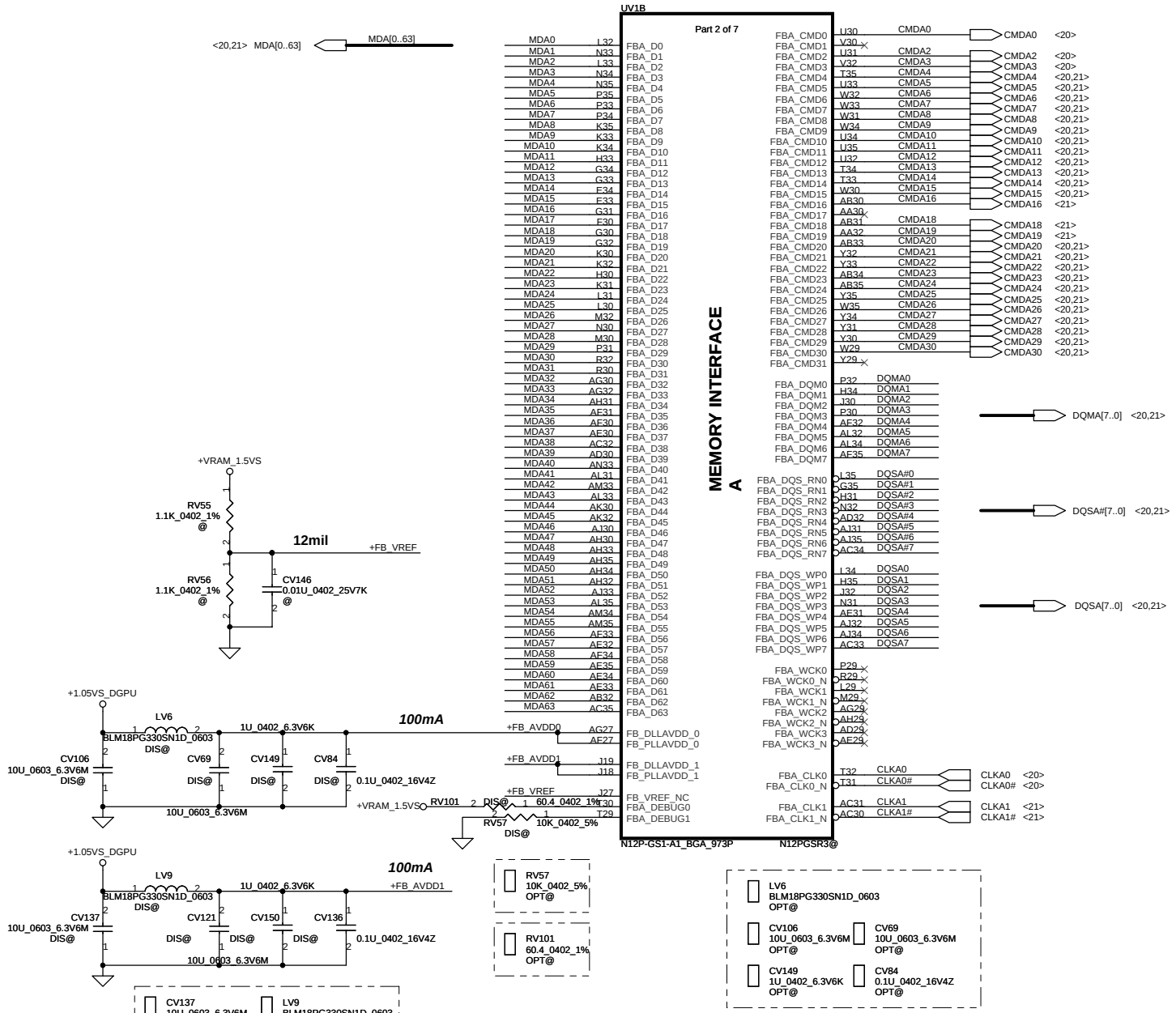
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size | Document Number: **4019BD** | Rev: **B**

Date: Monday, February 28, 2011 | Sheet 17 of 59



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

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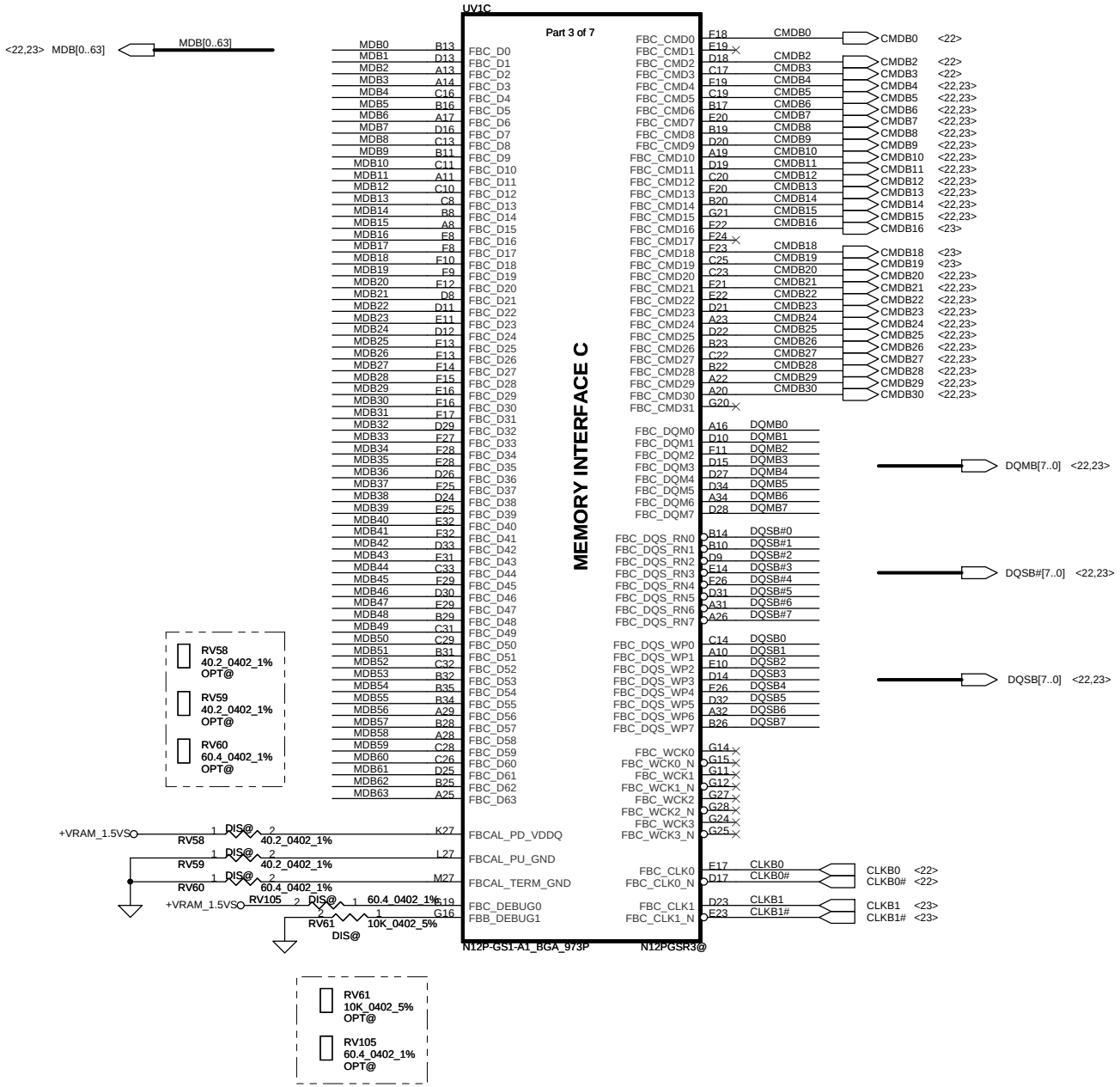
Title: SCHEMATIC, MB A7211

Size | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 18 of 59



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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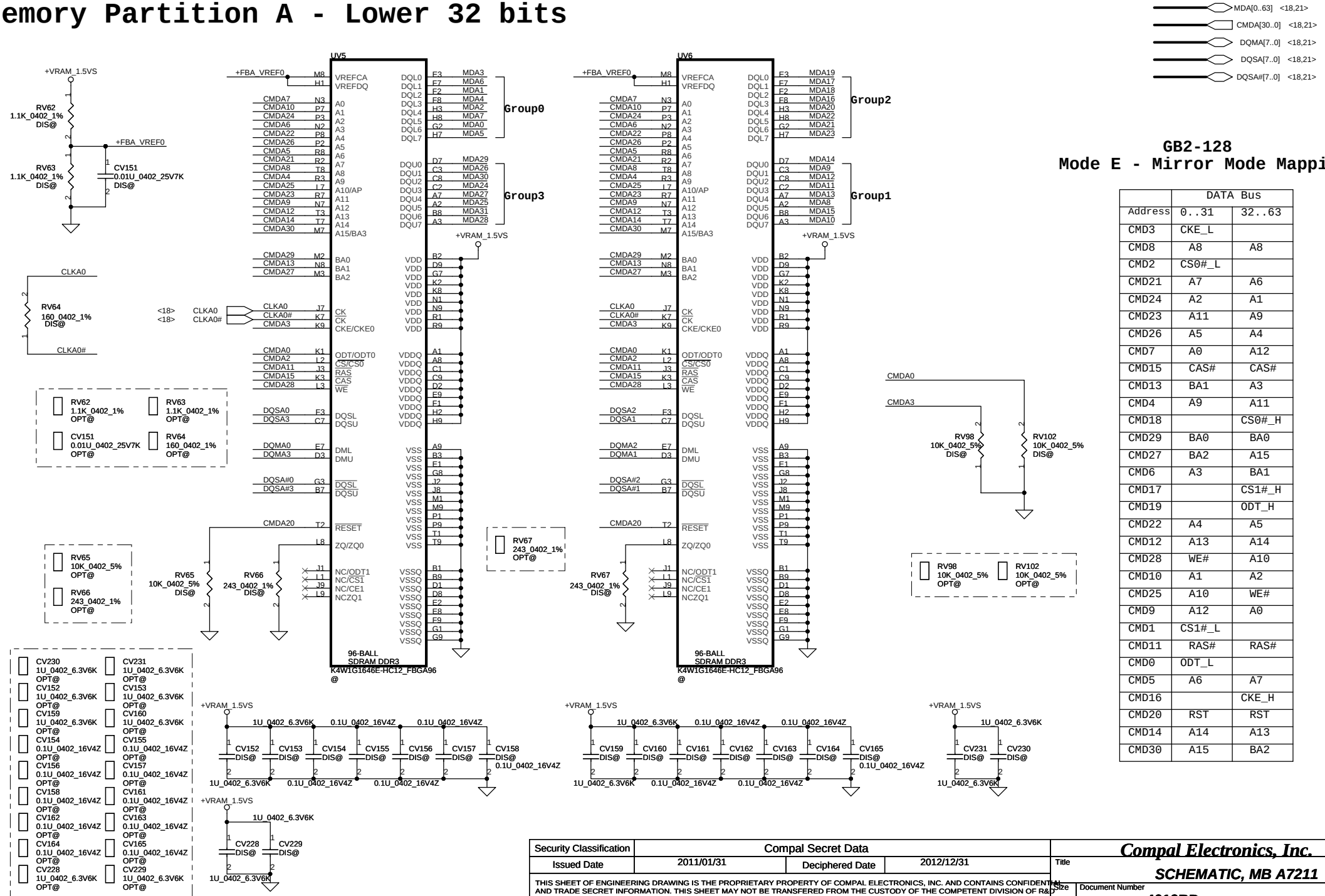
Title: SCHEMATIC, MB A7211

Size | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 19 of 59

Memory Partition A - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

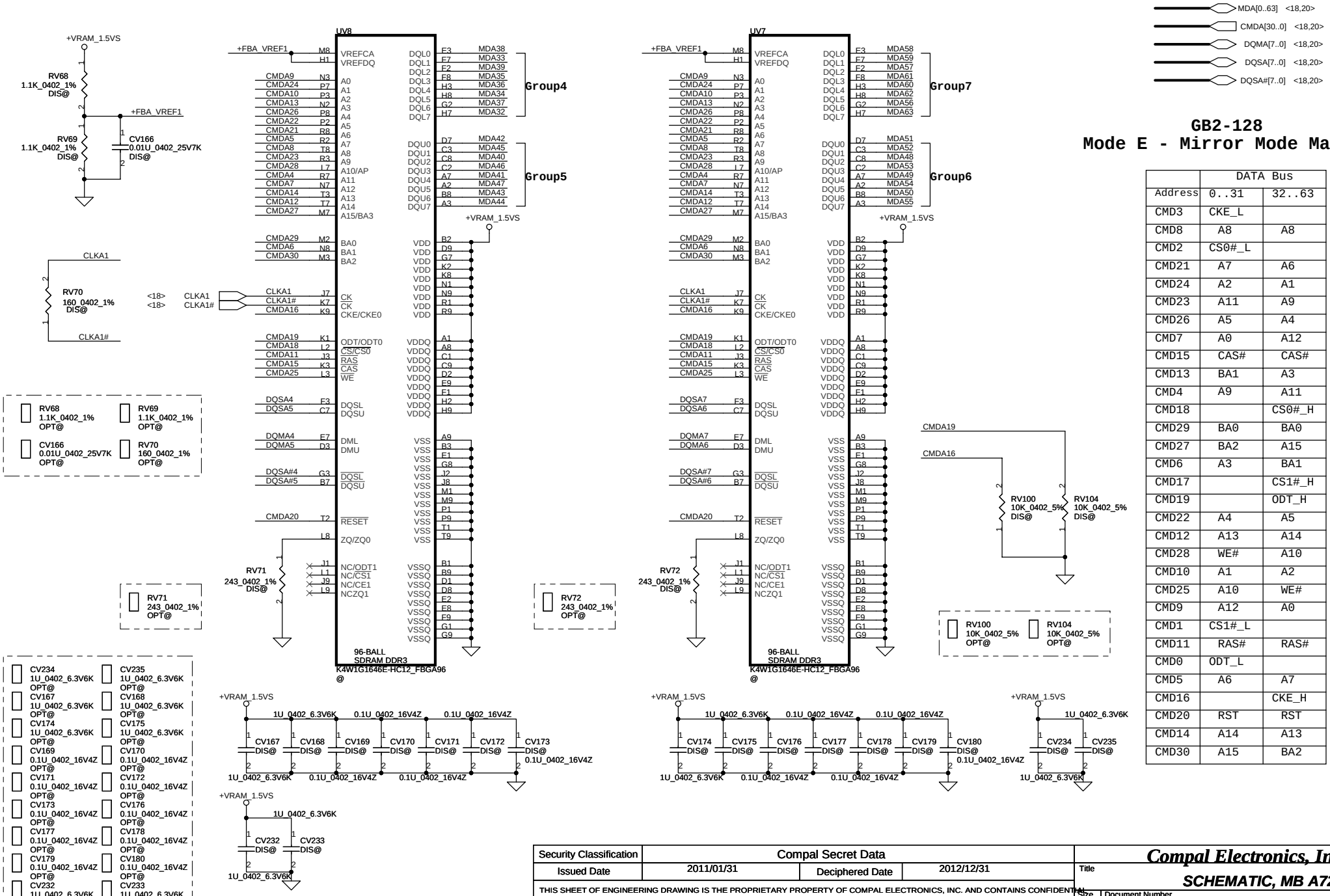
Compal Electronics, Inc.

Title: SCHEMATIC, MB A7211

Size | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 20 of 59

Memory Partition A - Upper 32 bits



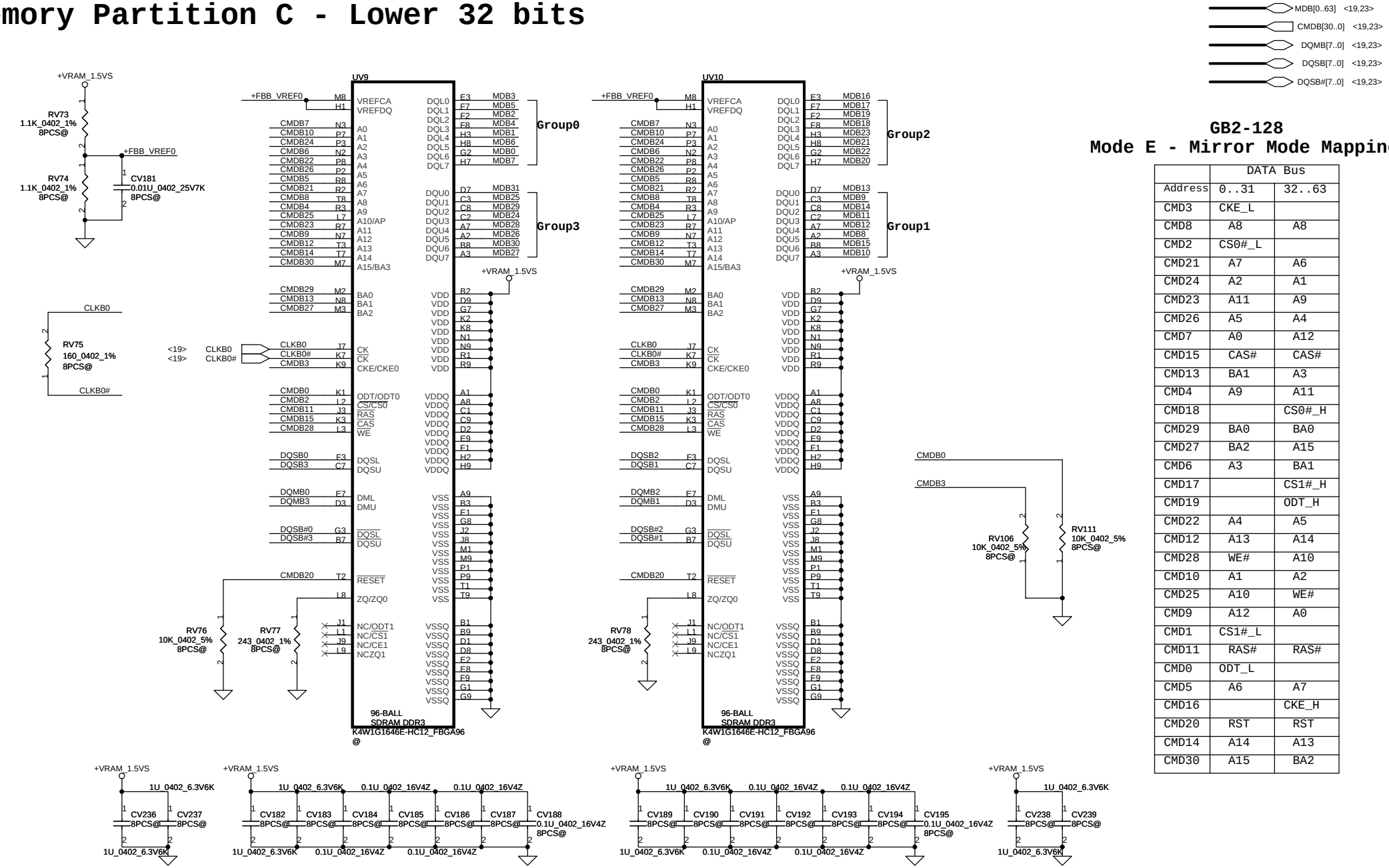
GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: SCHEMATIC, MB A7211
Size: | Document Number: 4019BD | Rev: B
Date: Monday, February 28, 2011 | Sheet 21 of 59

Memory Partition C - Lower 32 bits



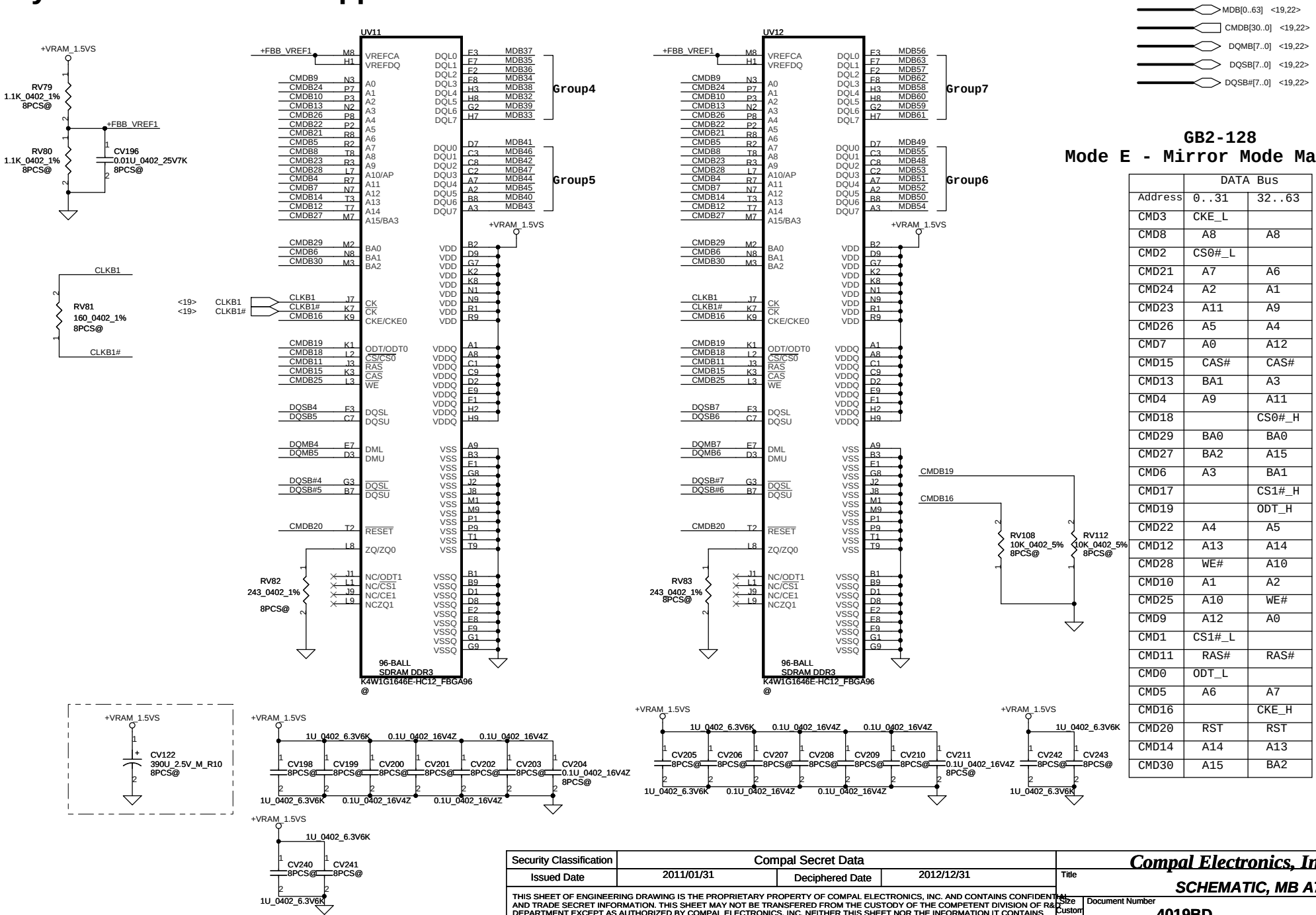
GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: SCHEMATIC, MB A7211
Size: Custom
Document Number: 4019BD
Rev: B
Date: Monday, February 28, 2011
Sheet 22 of 59

Memory Partition C - Upper 32 bits

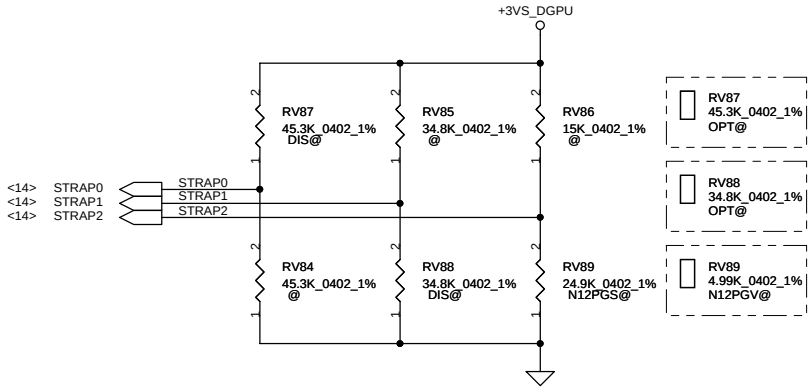


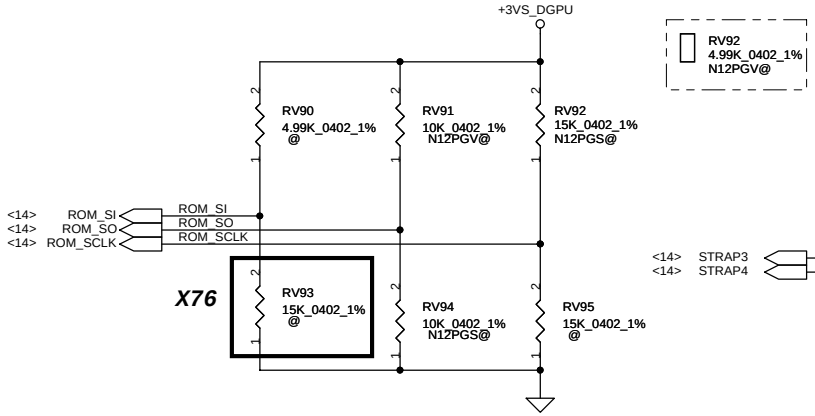
GB2-128
Mode E - Mirror Mode Mapping

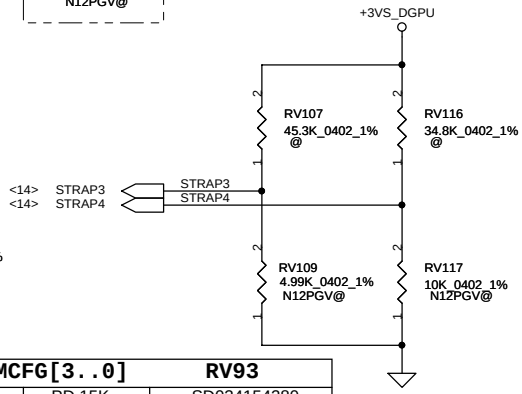
	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.
Title: SCHEMATIC, MB A7211
Size: Custom
Document Number: 4019BD
Rev: B
Date: Monday, February 28, 2011
Sheet 23 of 59







Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV93
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C	512MB	0010	PD 15K	SD034154280
		SA000041S20	1GB	0010	PD 15K	SD034154280
		Samsung K4W1G1646E-HC11	512MB	0011	PD 20K	SD034200280
		SA000041T00	1GB	0011	PD 20K	SD034200280
	128M16 900MHz	Hynix H5TQ2G63BFR-11C	1GB	0110	PD 34.8K	SD034348280
		SA00003YO00	2GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC11	1GB	0111	PD 45.3K	SD034453280
		SA000047Q00	2GB	0111	PD 45.3K	SD034453280
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C				
		SA0000324C0	512MB	0010	PD 15K	SD034154280
		Samsung K4W1G1646G-BC12				
		SA00004HS00	512MB	0011	PD 20K	SD034200280
	128M16 800MHz	Hynix H5TQ2G63BFR-12C				
		SA00003VS00	1GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC12	1GB	0111	PD 45.3K	SD034453280

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATIC, MB A7211

Size: Custom | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 24 of 59

OPTIMUS

<31> LCD_TXOUT0+ — R262 OPT@ 0_0402_5% — LVDS_TXOUT0+
<31> LCD_TXOUT0- — R263 OPT@ 0_0402_5% — LVDS_TXOUT0-
<31> LCD_TXOUT1+ — R265 OPT@ 0_0402_5% — LVDS_TXOUT1+
<31> LCD_TXOUT1- — R264 OPT@ 0_0402_5% — LVDS_TXOUT1-
<31> LCD_TXOUT2+ — R298 OPT@ 0_0402_5% — LVDS_TXOUT2+
<31> LCD_TXOUT2- — R277 OPT@ 0_0402_5% — LVDS_TXOUT2-
<31> LCD_TXCLK+ — R297 OPT@ 0_0402_5% — LVDS_TXCLK+
<31> LCD_TXCLK- — R296 OPT@ 0_0402_5% — LVDS_TXCLK-
<31> LCD_EDID_CLK — R300 OPT@ 0_0402_5% — LVDS_EDID_CLK
<31> LCD_EDID_DATA — R299 OPT@ 0_0402_5% — LVDS_EDID_DATA

<31> LCD_TZOUT0+ — R270 OPT@ 0_0402_5% — LVDS_TZOUT0+
<31> LCD_TZOUT0- — R267 OPT@ 0_0402_5% — LVDS_TZOUT0-
<31> LCD_TZOUT1+ — R269 OPT@ 0_0402_5% — LVDS_TZOUT1+
<31> LCD_TZOUT1- — R268 OPT@ 0_0402_5% — LVDS_TZOUT1-
<31> LCD_TZOUT2+ — R337 OPT@ 0_0402_5% — LVDS_TZOUT2+
<31> LCD_TZOUT2- — R283 OPT@ 0_0402_5% — LVDS_TZOUT2-
<31> LCD_TZCLK+ — R333 OPT@ 0_0402_5% — LVDS_TZCLK+
<31> LCD_TZCLK- — R329 OPT@ 0_0402_5% — LVDS_TZCLK-

<31> UMA_ENVDD — R350 OPT@ 0_0402_5% — LCD_ENVDD
<31> UMA_ENBKL — R357 OPT@ 0_0402_5% — EC_ENBKL — EC_ENBKL <44>

Close to LVDS Connector

DISCRETE

<14> VGA_TXOUT0+ — R331 DISL/DS@ 0_0402_5% — LVDS_TXOUT0+
<14> VGA_TXOUT0- — R309 DISL/DS@ 0_0402_5% — LVDS_TXOUT0-
<14> VGA_TXOUT1+ — R317 DISL/DS@ 0_0402_5% — LVDS_TXOUT1+
<14> VGA_TXOUT1- — R315 DISL/DS@ 0_0402_5% — LVDS_TXOUT1-
<14> VGA_TXOUT2+ — R308 DISL/DS@ 0_0402_5% — LVDS_TXOUT2+
<14> VGA_TXOUT2- — R302 DISL/DS@ 0_0402_5% — LVDS_TXOUT2-
<14> VGA_TXCLK+ — R305 DISL/DS@ 0_0402_5% — LVDS_TXCLK+
<14> VGA_TXCLK- — R304 DISL/DS@ 0_0402_5% — LVDS_TXCLK-
<13> VGA_EDID_CLK — R314 DISL/DS@ 0_0402_5% — LVDS_EDID_CLK
<13> VGA_EDID_DATA — R310 DISL/DS@ 0_0402_5% — LVDS_EDID_DATA

<13> VGA_ENVDD — R356 DIS@ 0_0402_5% — LCD_ENVDD
<13> VGA_ENBKL — R358 DIS@ 0_0402_5% — EC_ENBKL

Close to LVDS Connector

+3VS — R1434 EDP@ 100K_0402_5% — LVDS_EDID_DATA
+3VS — R1435 EDP@ 100K_0402_5% — LVDS_EDID_CLK

DISCRETE for Dual Chanel Panel

<14> VGA_TZOUT0+ — R500 DISL/DS@ 0_0402_5% — LVDS_TZOUT0+
<14> VGA_TZOUT0- — R501 DISL/DS@ 0_0402_5% — LVDS_TZOUT0-
<14> VGA_TZOUT1+ — R502 DISL/DS@ 0_0402_5% — LVDS_TZOUT1+
<14> VGA_TZOUT1- — R503 DISL/DS@ 0_0402_5% — LVDS_TZOUT1-
<14> VGA_TZOUT2+ — R504 DISL/DS@ 0_0402_5% — LVDS_TZOUT2+
<14> VGA_TZOUT2- — R505 DISL/DS@ 0_0402_5% — LVDS_TZOUT2-
<14> VGA_TZCLK+ — R507 DISL/DS@ 0_0402_5% — LVDS_TZCLK+
<14> VGA_TZCLK- — R508 DISL/DS@ 0_0402_5% — LVDS_TZCLK-

Close to LVDS1 Connector

DISCRETE for Full-HD and 3D eDP Panel

<14> VGA_EDP_TX0+ — C880 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT0+
<14> VGA_EDP_TX0- — C881 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT0-
<14> VGA_EDP_TX1+ — C882 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT1+
<14> VGA_EDP_TX1- — C883 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT1-
<14> VGA_EDP_TX2+ — C884 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT2+
<14> VGA_EDP_TX2- — C885 EDP@ 0.1U_0402_16V7K — LVDS_TXOUT2-
<14> VGA_EDP_TX3+ — C886 EDP@ 0.1U_0402_16V7K — LVDS_TXCLK+
<14> VGA_EDP_TX3- — C887 EDP@ 0.1U_0402_16V7K — LVDS_TXCLK-

<14> VGA_EDP_AUX — C888 EDP@ 0.1U_0402_16V7K — LVDS_EDID_CLK
<14> VGA_EDP_AUX — C889 EDP@ 0.1U_0402_16V7K — LVDS_EDID_DATA

Close to LVDS Connector

LCD/PANEL BD. Conn.

+3VS — R388 CAM@ 0_0603_5% — +3VS_LVDS_CAM — C225 CAM@ 0.1U_0402_16V4Z
W=20mils

JLVDS

USB20_P11_R	3	4	LVDS_TXCLK+
USB20_N11_R	5	6	LVDS_TXCLK-
LVDS_TXOUT0+	9	10	LVDS_TZCLK+
LVDS_TXOUT0-	11	12	LVDS_TZCLK-
LVDS_TXOUT1+	13	14	LVDS_EDID_CLK
LVDS_TXOUT1-	15	16	LVDS_EDID_DATA
LVDS_TXOUT2+	17	18	INT_MIC_CLK
LVDS_TXOUT2-	19	20	INT_MIC_DATA
	21	22	LCD_ENVDD
LVDS_TZOUT0+	23	24	LED_PWM — R387 @ 0_0402_5% — INVT_PWM <44>
LVDS_TZOUT0-	25	26	+3VS_LVDSDDC
LVDS_TZOUT1+	27	28	
LVDS_TZOUT1-	29	30	
LVDS_TZOUT2+	31	32	
LVDS_TZOUT2-	33	34	
BKOFF#_R	35	36	
	37	38	
	39	40	
	41	42	
	GMD	GND	

ACES_87242-4001-09 @

+LCD_INV — +LCD_INV

D84 — AZ5125-02S.R7G_SOT23-3

INT_MIC_CLK <43>
INT_MIC_DATA <43>

3A

C226 0.1U_0402_16V4Z — C227 4.7U_0805_10V4Z — +LCD_VDD

INT_MIC_CLK — For EMI — C13 CAM@ 220P_0402_50V7K

+3VS_LVDSDDC — R1440 NOEDP@ 0_0603_5% — +3VS
R143 EDP@ 0_0402_5% — EDP_HPD <13>

For EMI — C231 @ 680P_0402_50V7K — C232 0.1U_0402_16V4Z

RB751V40_SC76-2 D18
BKOFF#_R — R103 @ 33_0402_5% — BKOFF# <44>
R113 10K_0402_5%

Reserve for EMI request

R78 CAM@ 0_0402_5%
L55 @
<32> USB20_N11 — USB20_N11_R
<32> USB20_P11 — USB20_P11_R
WCM-2012-900T_0805
R96 CAM@ 0_0402_5%

+LCD_INV — L2 FBMA-L11-201209-221LMA30T_0805 — B+
C234 68P_0402_50V8J — C235 0.1U_0402_25V6

R107 150_0603_5% EDP@ — R109 47K_0402_5% EDP@ — C233 0.1U_0402_16V4Z EDP@
C229 0.01U_0402_25V7K EDP@ — Q1 2N7002DW-T/R7_SOT363-6 EDP@

+LCD_VDD — R107 150_0603_5% OPT@ — +3VS — R108 100K_0402_5% OPT@ — +5VS — R120 100K_0402_5% EDP@

Q1A 2N7002DW-T/R7_SOT363-6 OPT@
Q1B 2N7002DW-T/R7_SOT363-6 OPT@
LCD_ENVDD — R112 100K_0402_5% OPT@

C228 OPT@ 0.1U_0402_16V7K — W=80mils — Q17 OPT@ AO3413_SOT23
R109 47K_0402_5% OPT@ — >LCDPWR_GATE
C229 0.01U_0402_25V7K OPT@
+LCD_VDD — W=80mils — C233 0.1U_0402_16V4Z OPT@

C292 EDP@ 0.1U_0402_16V7K — W=80mils — Q23 EDP@ AO3413_SOT23
LCDPWR_GATE
+LCD_VDD — W=80mils

R107 150_0603_5% NO3D@ — R108 100K_0402_5% NO3D@ — R109 47K_0402_5% NO3D@ — C228 0.1U_0402_16V7K NO3D@
Q1 2N7002DW-T/R7_SOT363-6 NO3D@ — C229 0.01U_0402_25V7K NO3D@ — C233 0.1U_0402_16V4Z NO3D@
Q17 AO3413_SOT23 NO3D@

<31> PCH_PWM — R332 OPT@ 0_0402_5% — R347 @ 0_0402_5% — LED_PWM
<13> VGA_BL_PWM — R349 3D@ 0_0402_5% — D17 — RB751V40_SC76-2 — R131 47K_0402_5%

B+ — For EMI
C236 @ 0.1U_0402_25V6 — C268 @ 0.1U_0402_25V6 — C489 @ 0.1U_0402_25V6 — C490 @ 0.1U_0402_25V6

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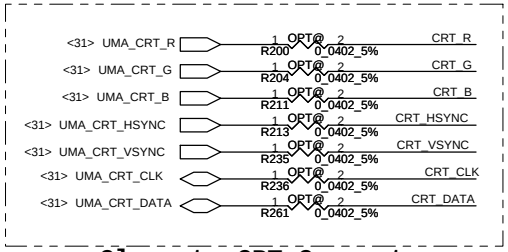
Title: **SCHEMATIC, MB A7211**

Size: Custom | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 25 of 59

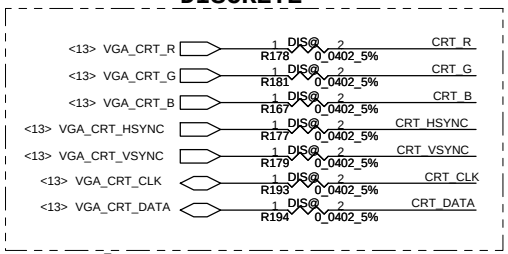
CRT CONNECTOR

OPTIMUS

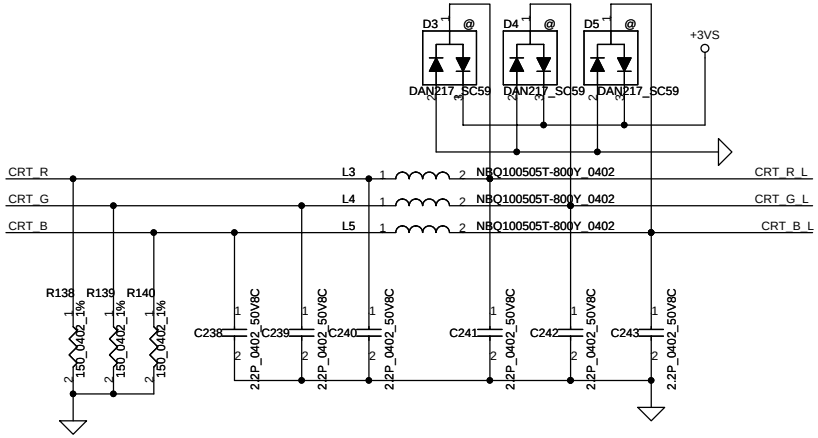


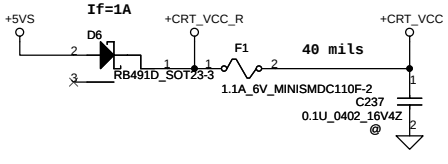
Close to CRT Connector

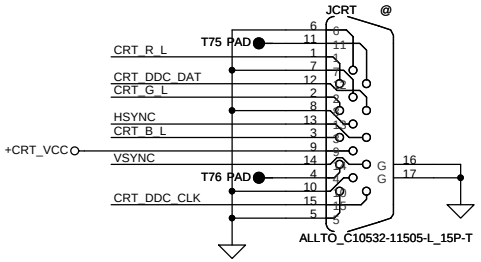
DISCRETE

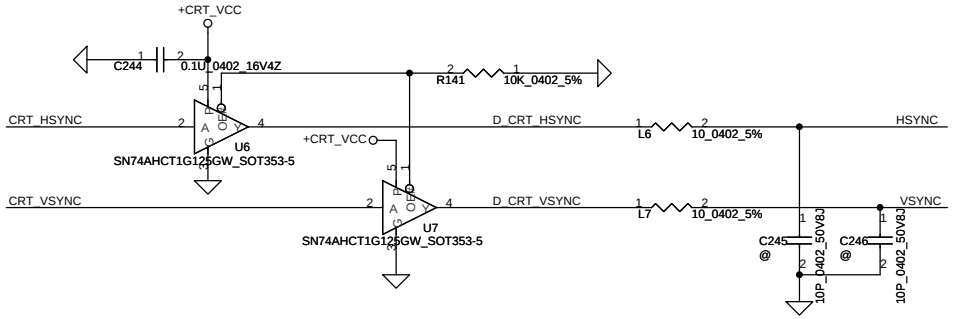


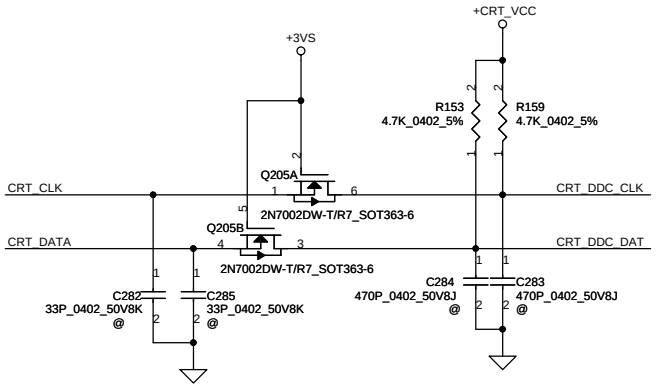
Close to CRT Connector











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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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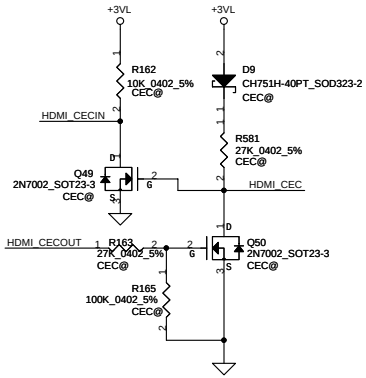
Title: ***SCHEMATIC, MB A7211***

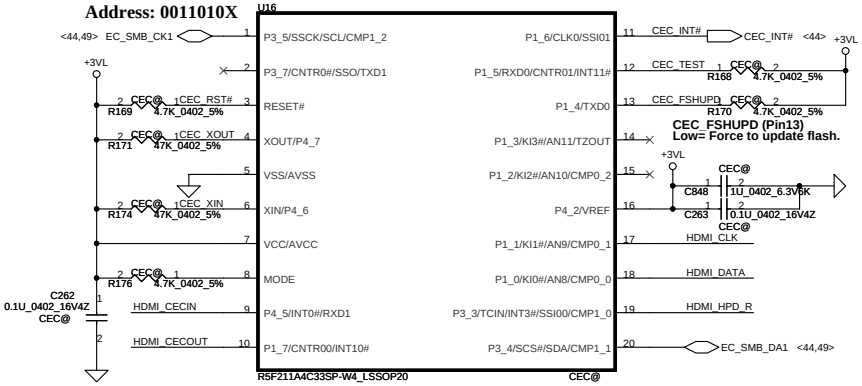
Size | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 26 of 59

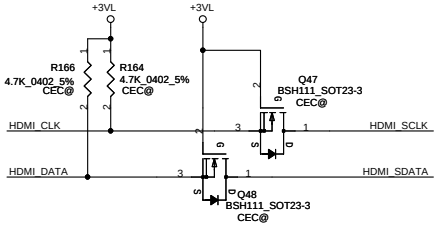
HDMI CEC Controller



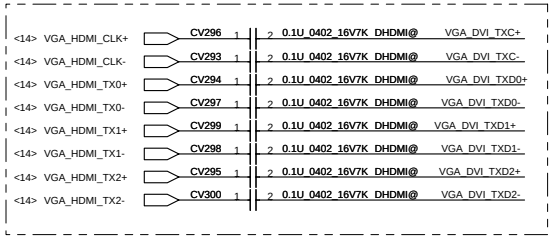
Address: 0011010X



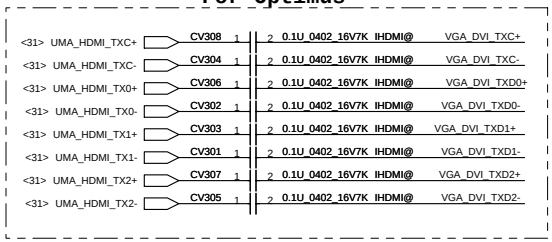
CEC_FSHUPD (Pin13)
Low= Force to update flash.

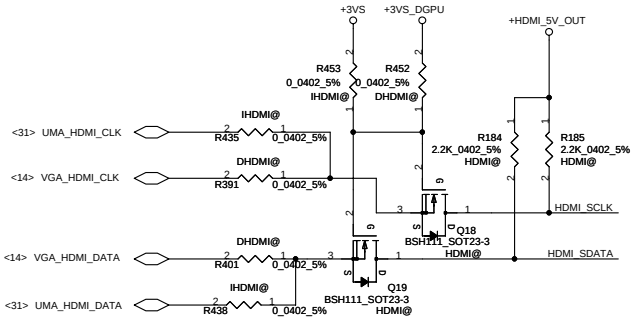


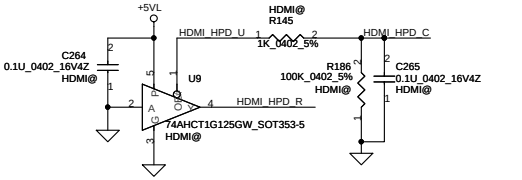
For DISCRETE

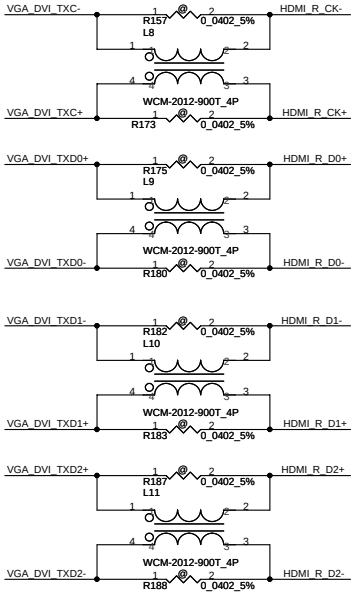


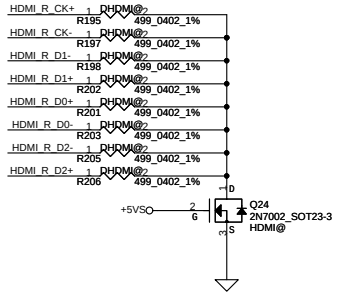
For Optimus

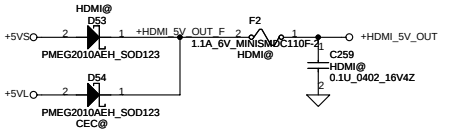


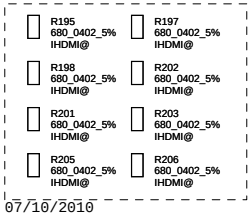






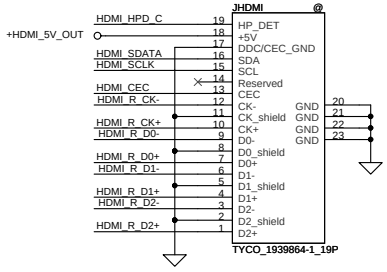






07/10/2010
Intel DG P.132

HDMI Connector



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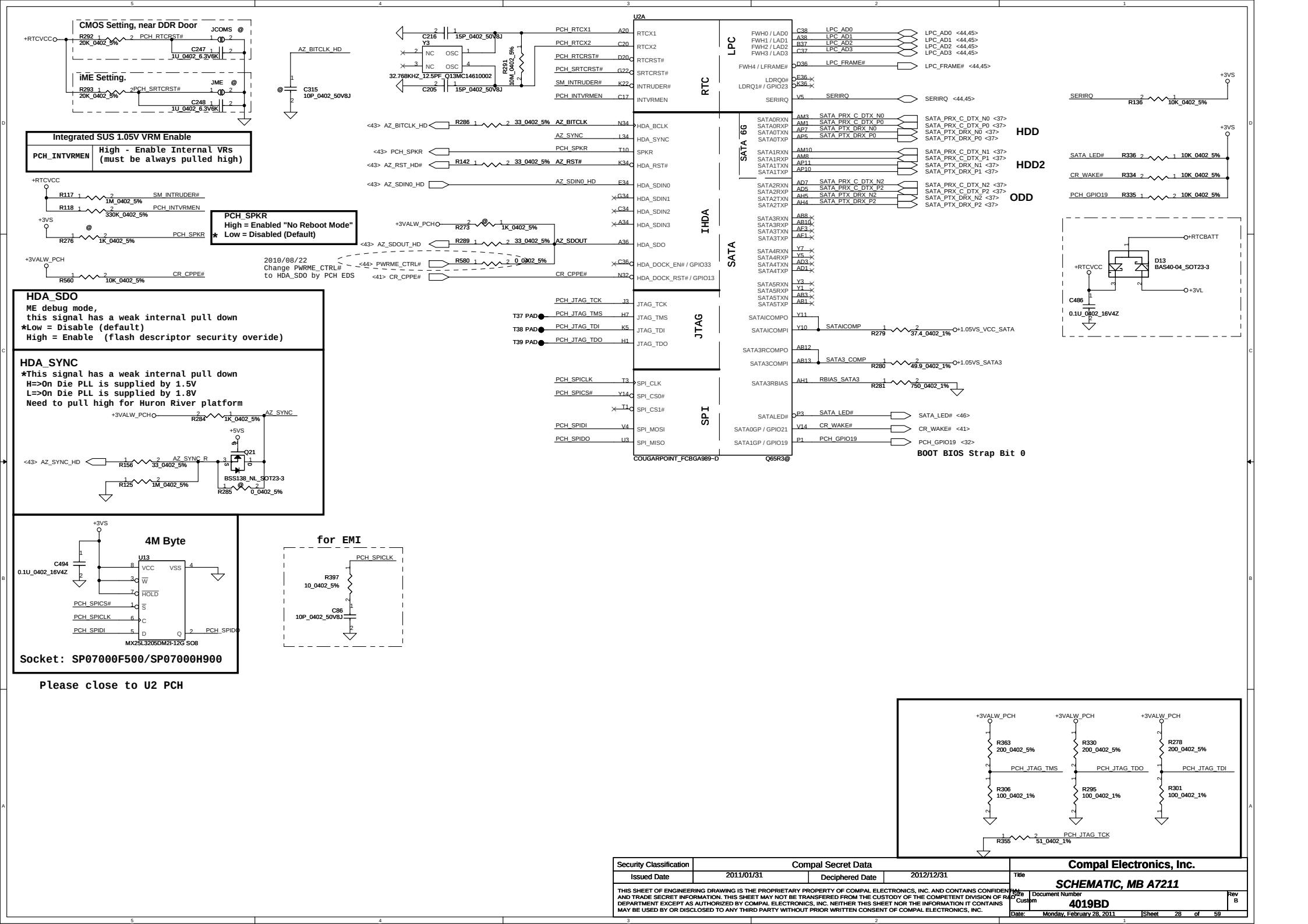
Title	SCHEMATIC, MB A7211
Size	Document Number: 4019BD — Rev: B
Date: Monday, February 28, 2011	Sheet 27 of 59



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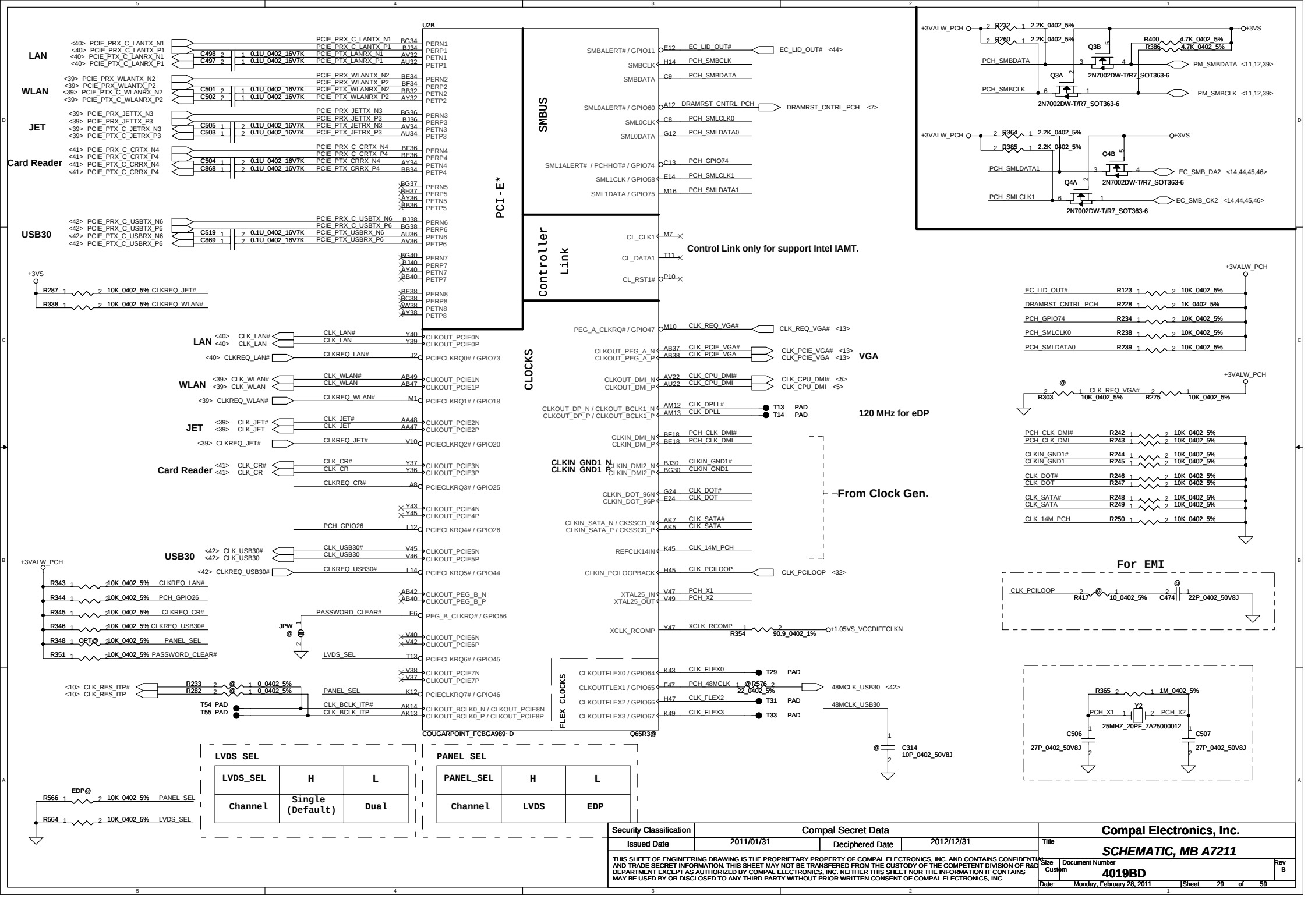
Title: ***SCHEMATIC, MB A7211***

Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 28 of 59



LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL	H	L
Channel	LVDS	EDP

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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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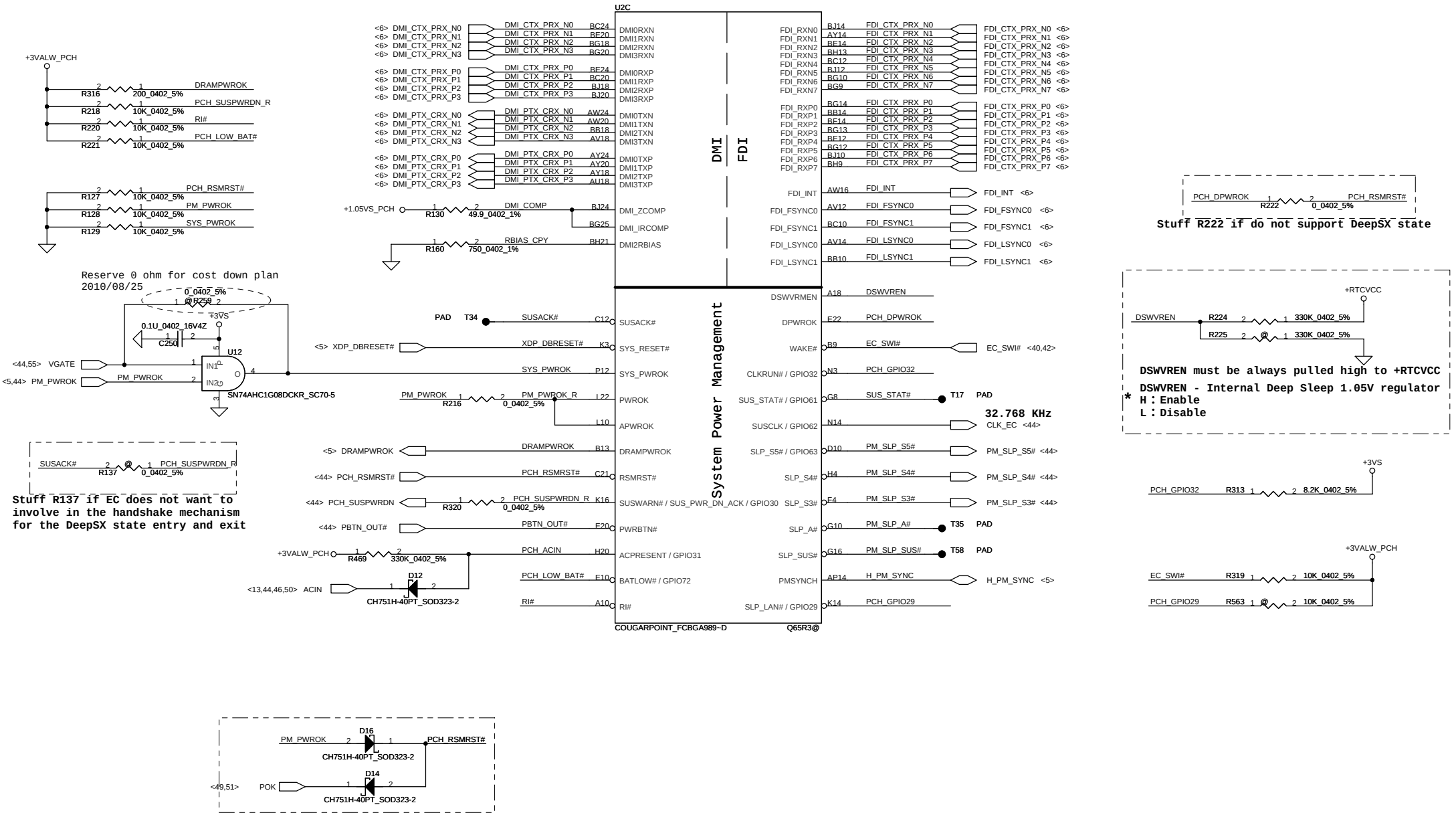
Title: SCHEMATIC, MB A7211

Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 29 of 59



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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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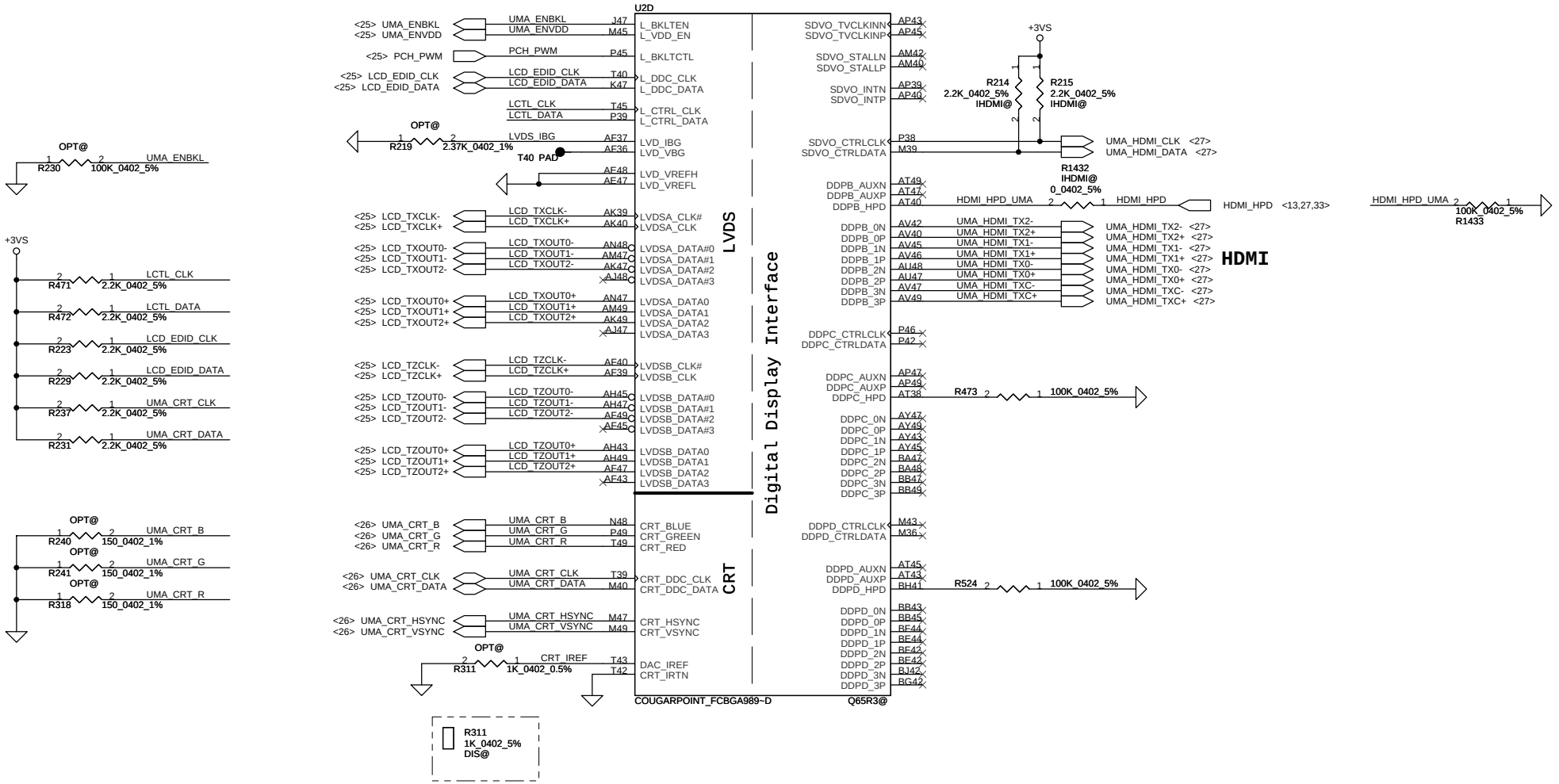
Title: *SCHEMATIC, MB A7211*

Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 30 of 59



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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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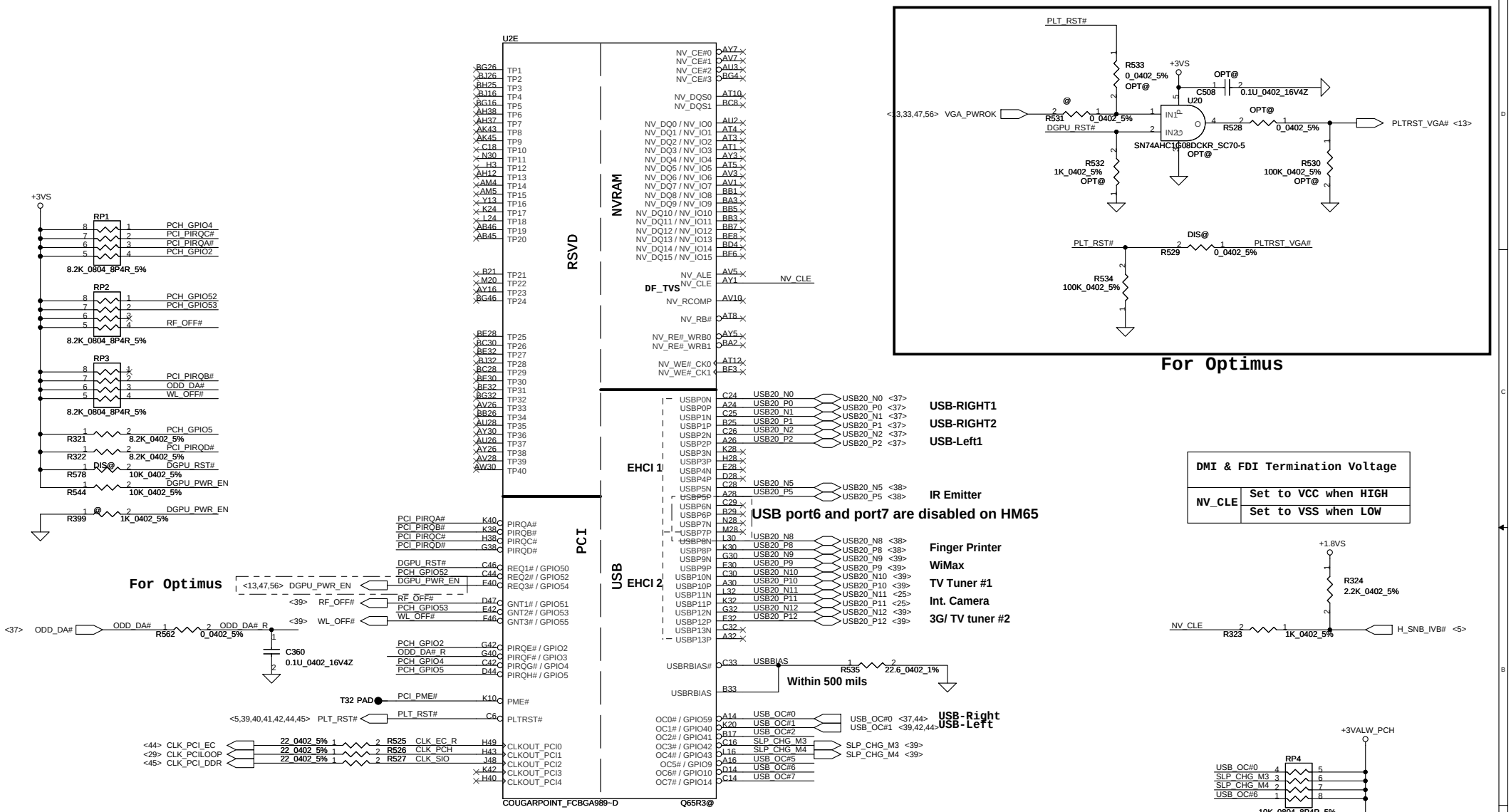
Title: ***SCHEMATIC, MB A7211***

Size	Document Number	Rev
Custom	**4019BD**	B

Date: Monday, February 28, 2011 | Sheet 31 of 59



Boot BIOS Strap

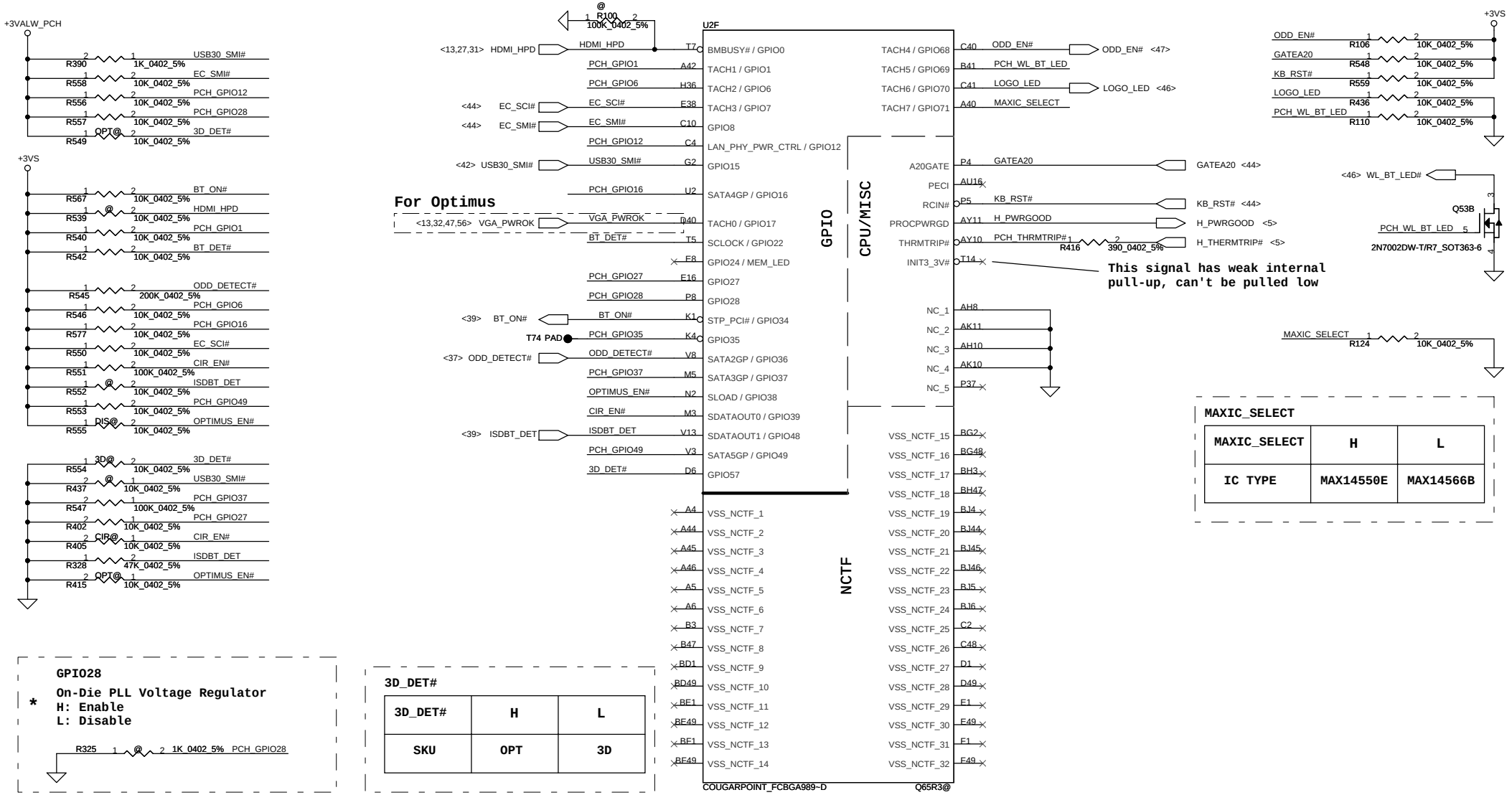
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

A16 Swap Override Strap

WL_OFF#	*	Low= A16 swap override Enable High= A16 swap override Disable

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	SCHEMATIC, MB A7211
Size: Custom	Document Number: 4019BD
Rev	B
Date: Monday, February 28, 2011	Sheet 32 of 59



MAXIC_SELECT

MAXIC_SELECT	H	L
IC TYPE	MAX14550E	MAX14566B

GPIO28

* On-Die PLL Voltage Regulator
H: Enable
L: Disable

R325 1 @ 2 1K_0402_5% PCH_GPIO28

3D_DET#

3D_DET#	H	L
SKU	OPT	3D

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable

R326 1 @ 2 1K_0402_5% EC_SMI#

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

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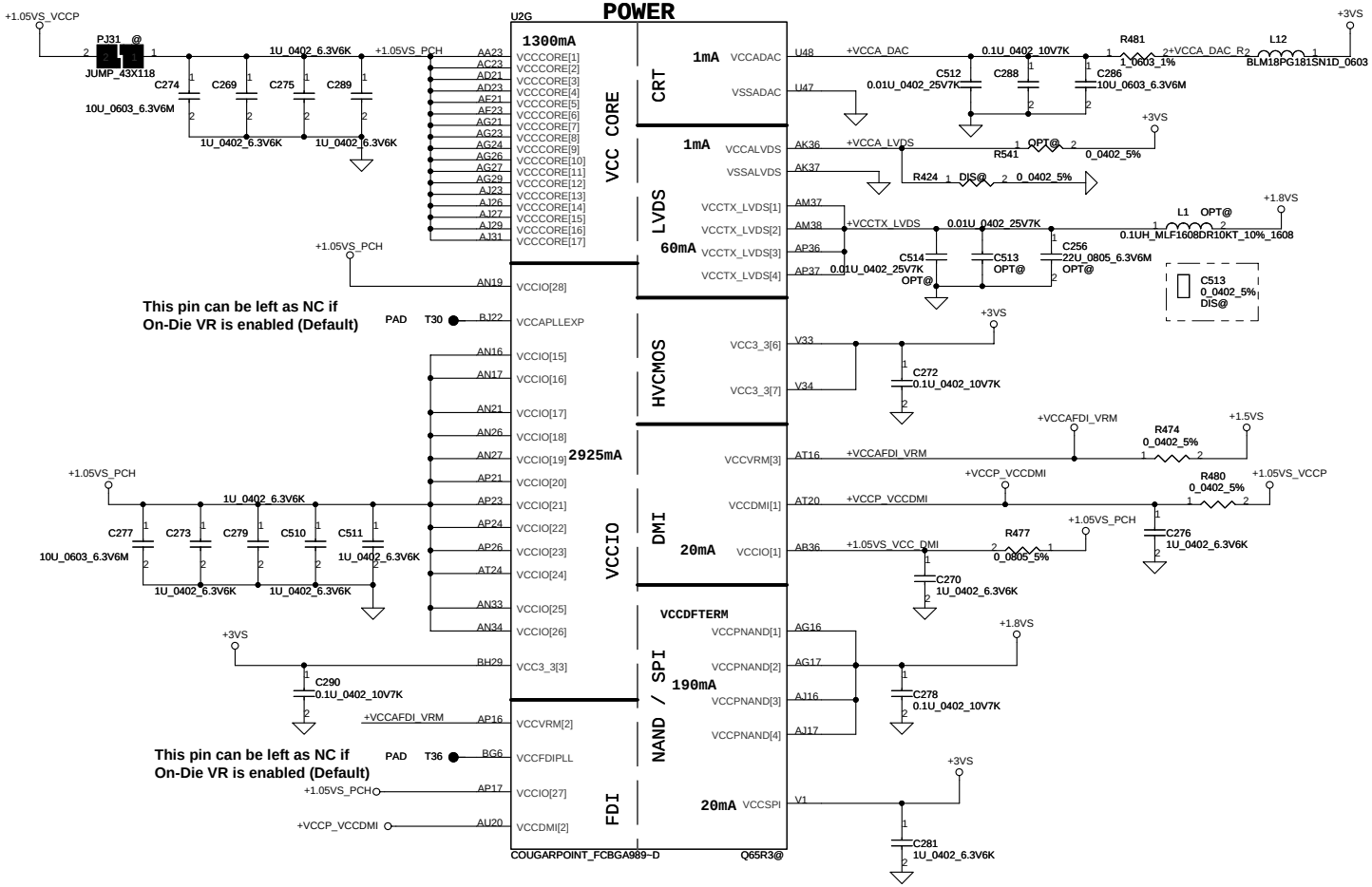
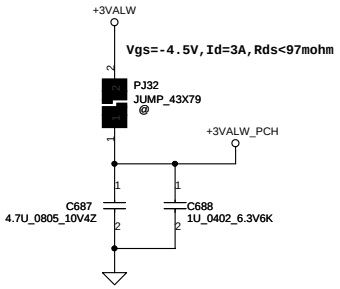
Title: SCHEMATIC, MB A7211			
Size: B	Document Number: 4019BD		Rev: B
Date: Monday, February 28, 2011	Sheet 33 of 59		



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSusHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06



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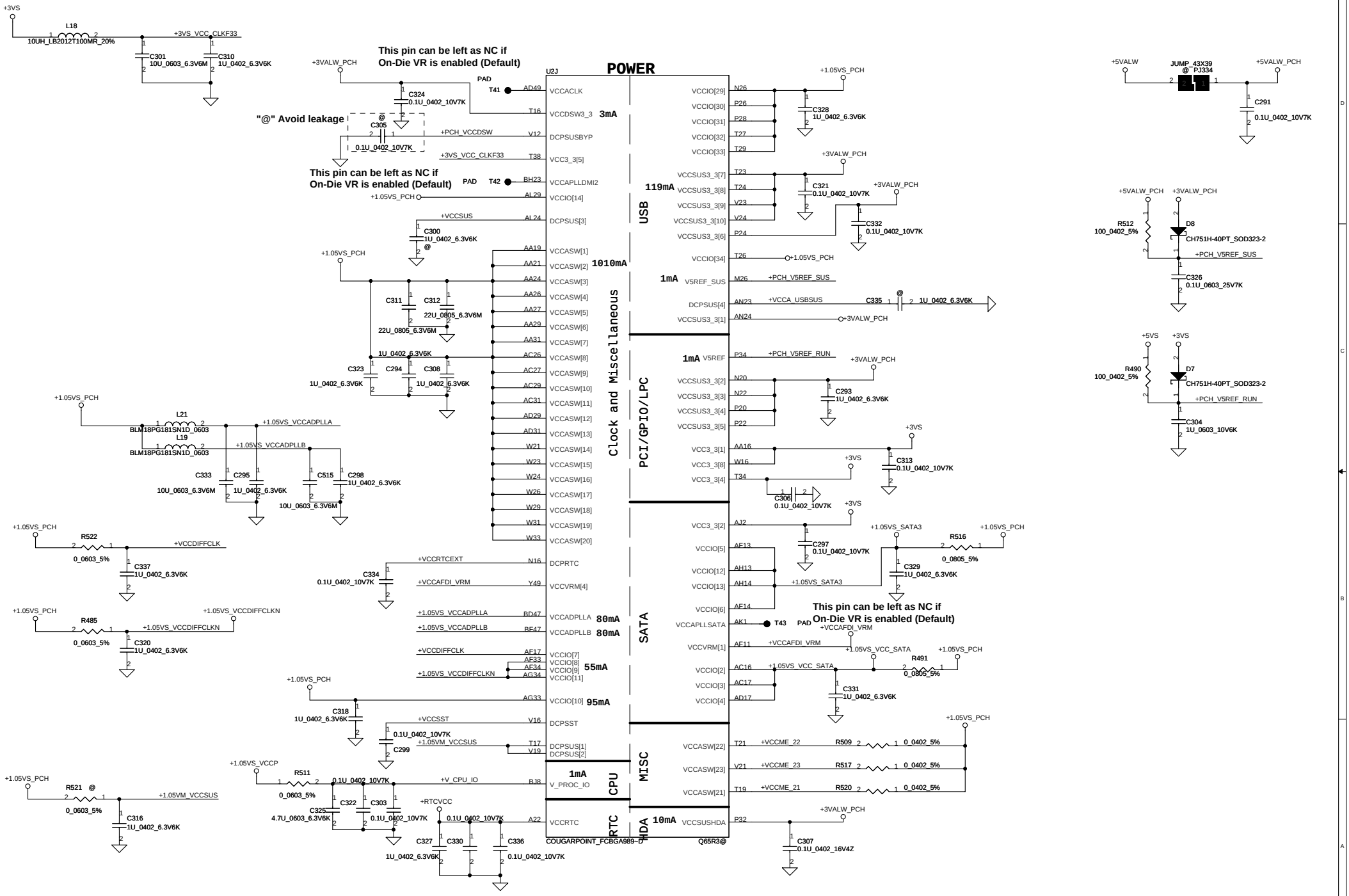
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title: SCHEMATIC, MB A7211
Size: Custom	Document Number: 4019BD			Rev: B
Date: Monday, February 28, 2011	Sheet 34 of 59			



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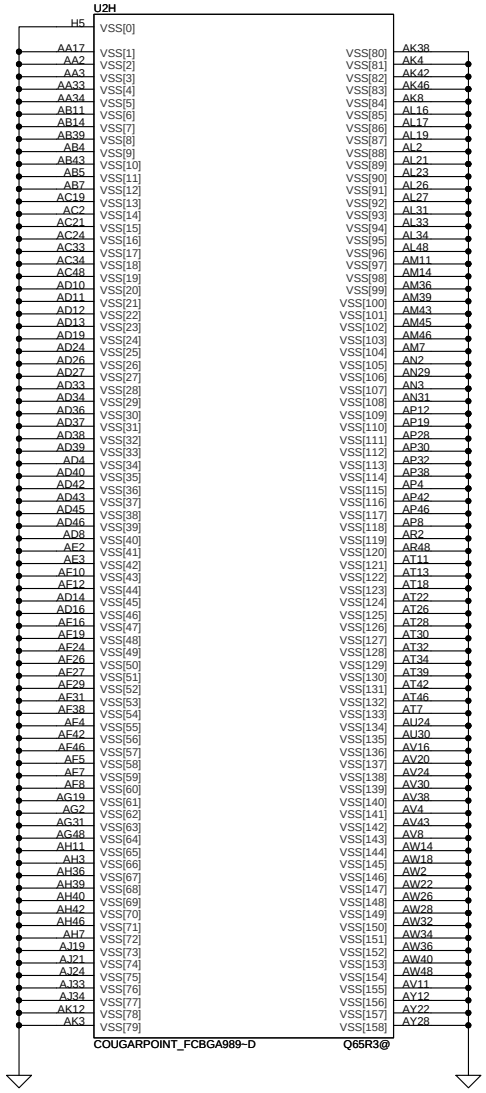
Issued Date	2011/01/31	Deciphered Date	2012/12/31

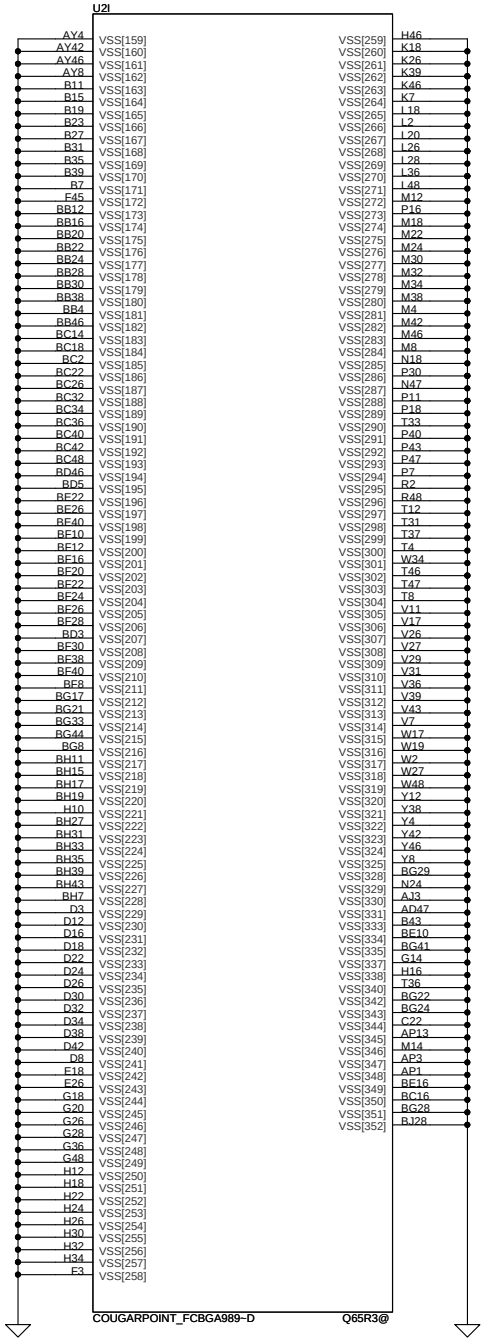
Compal Electronics, Inc.

Title: ***SCHEMATIC, MB A7211***

Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 | Sheet 35 of 59





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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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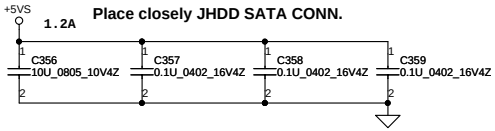
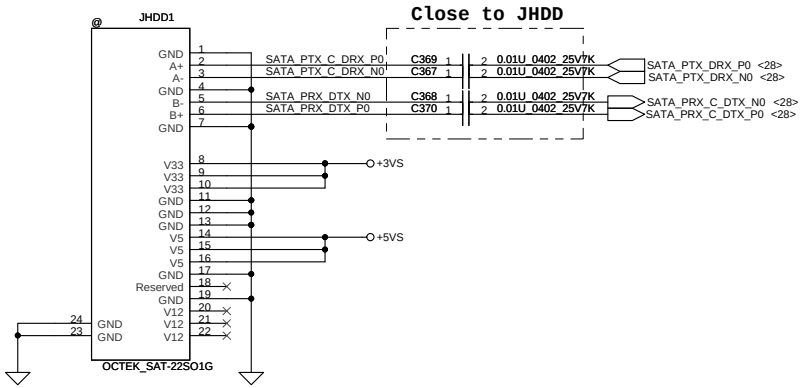
Title: ***SCHEMATIC, MB A7211***

Size	Document Number	Rev
Custom	**4019BD**	B

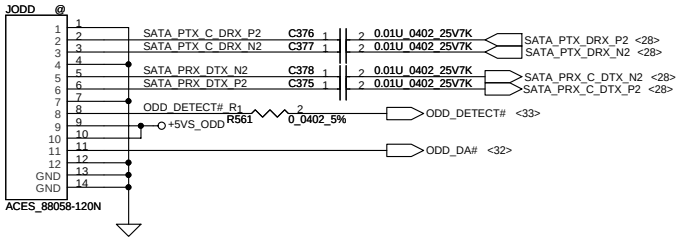
Date: Monday, February 28, 2011 Sheet 36 of 59

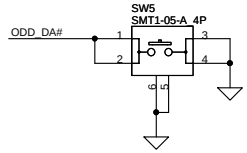
SATA HDD Conn.



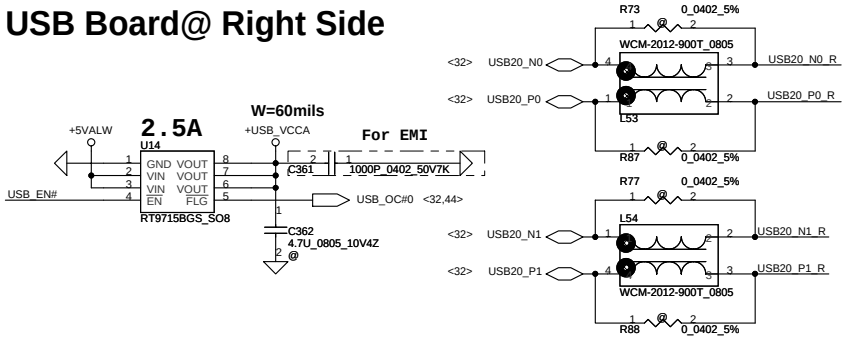


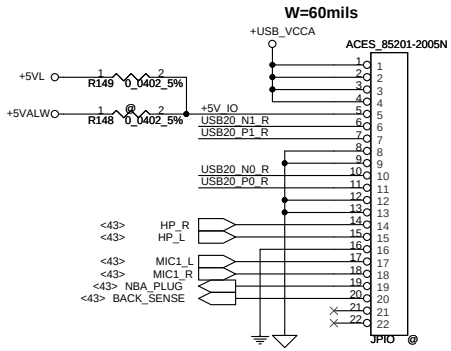
SATA ODD Conn



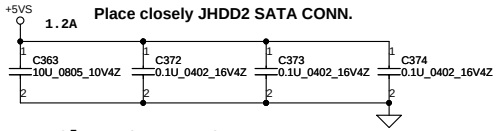


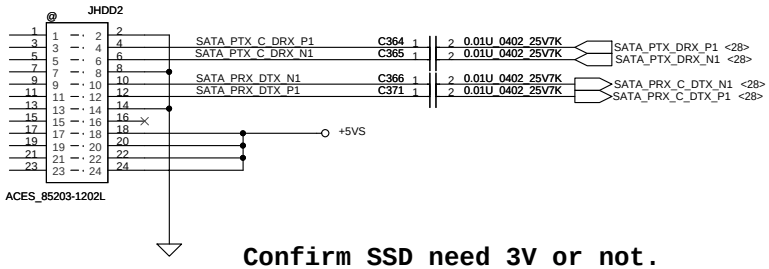
USB Board@ Right Side





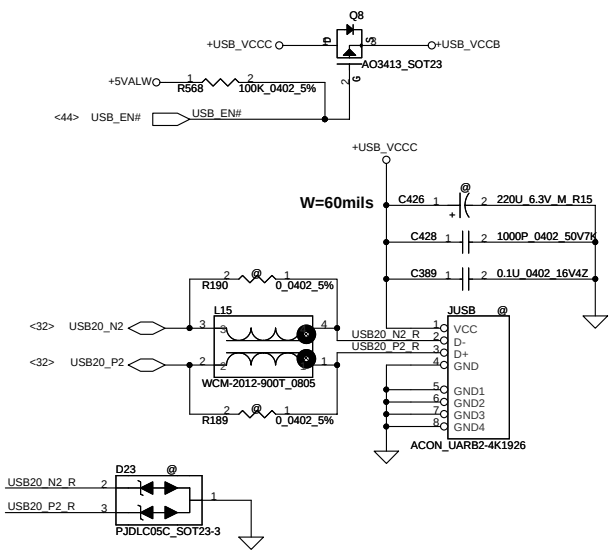
SATA 2nd HDD Conn.

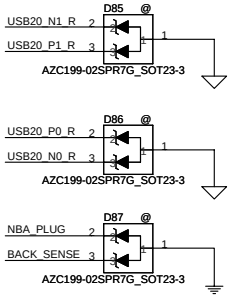




Confirm SSD need 3V or not.

USB Board@ Left Side





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Issued Date	2011/01/31	Deciphered Date	2012/12/31

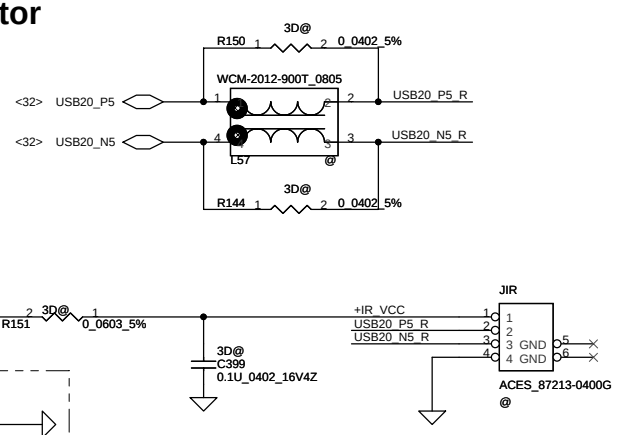
Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

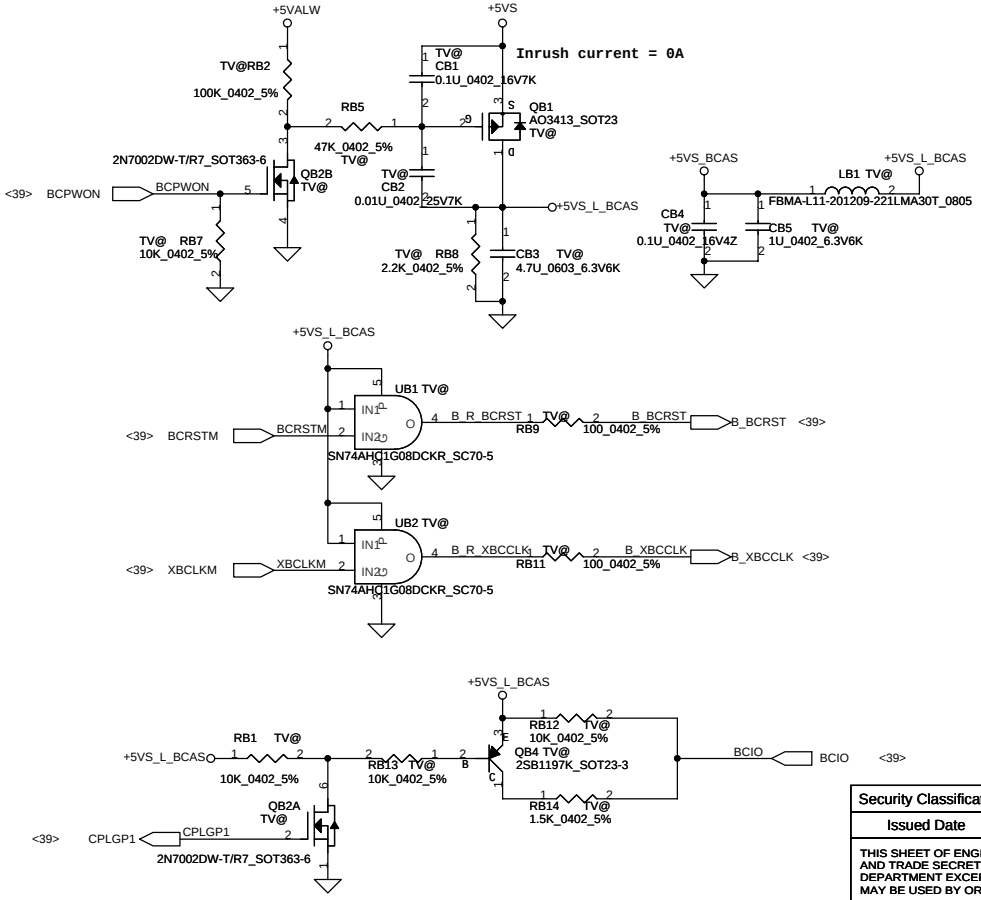
Size	Document Number	Rev
	4019BD	B

Date: Monday, February 28, 2011 Sheet 37 of 59

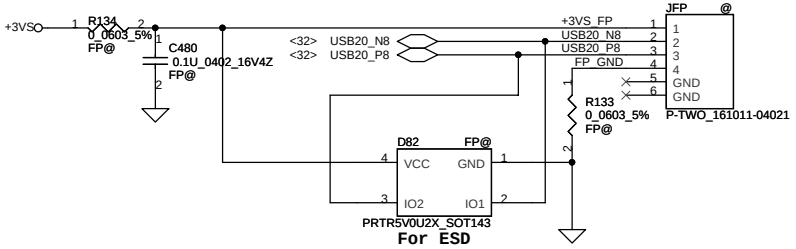
IR Emitter Connector



B-CAS Circuit



Finger printer



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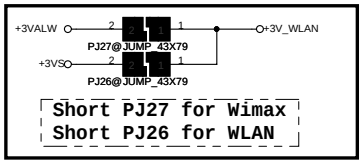
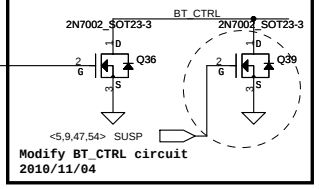
Compal Electronics, Inc.			
Title: SCHEMATIC, MB A7211			
Size	Document Number: 4019BD		Rev: B
Date: Monday, February 28, 2011	Sheet 38 of 59		

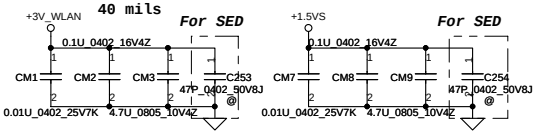
Slot 1 Half PCIe Mini Card-WLAN/ WiMax

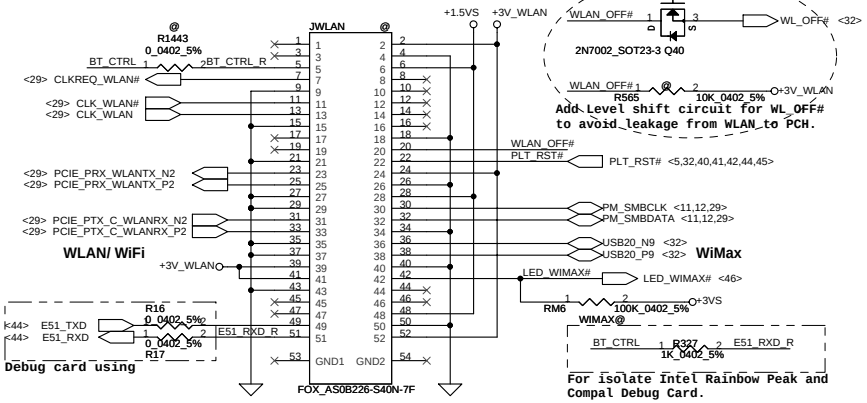


WLAN&BT Combo module circuits

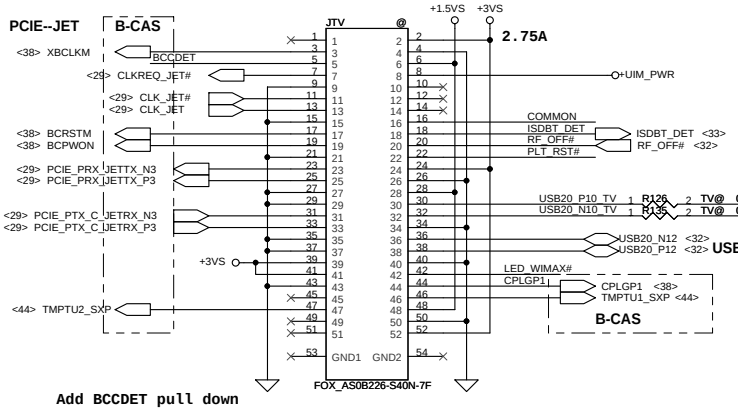
	BT on module Enable	BT on module Disable
BT_CRTL	H	L
BT_ON#	L	H



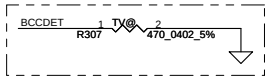


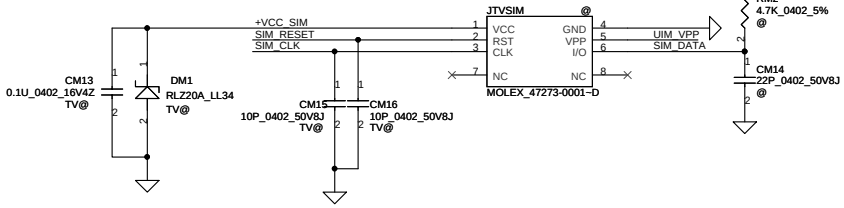


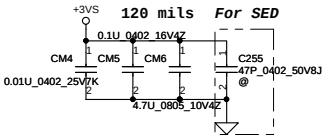
Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET

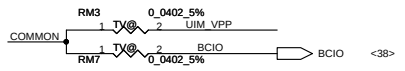


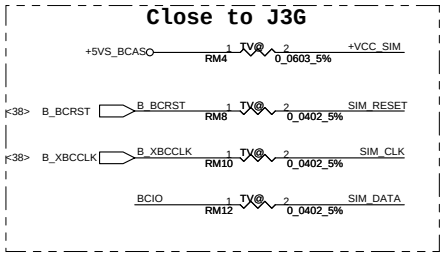
Add BCCDET pull down







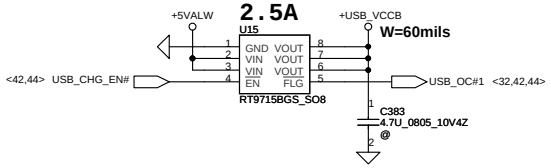


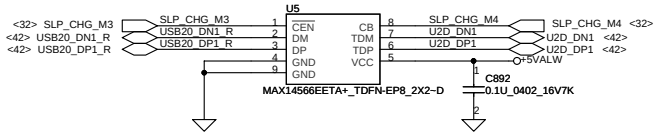


USB Sleep & Charge
Auto-Mode
Mode3/Mode4

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM





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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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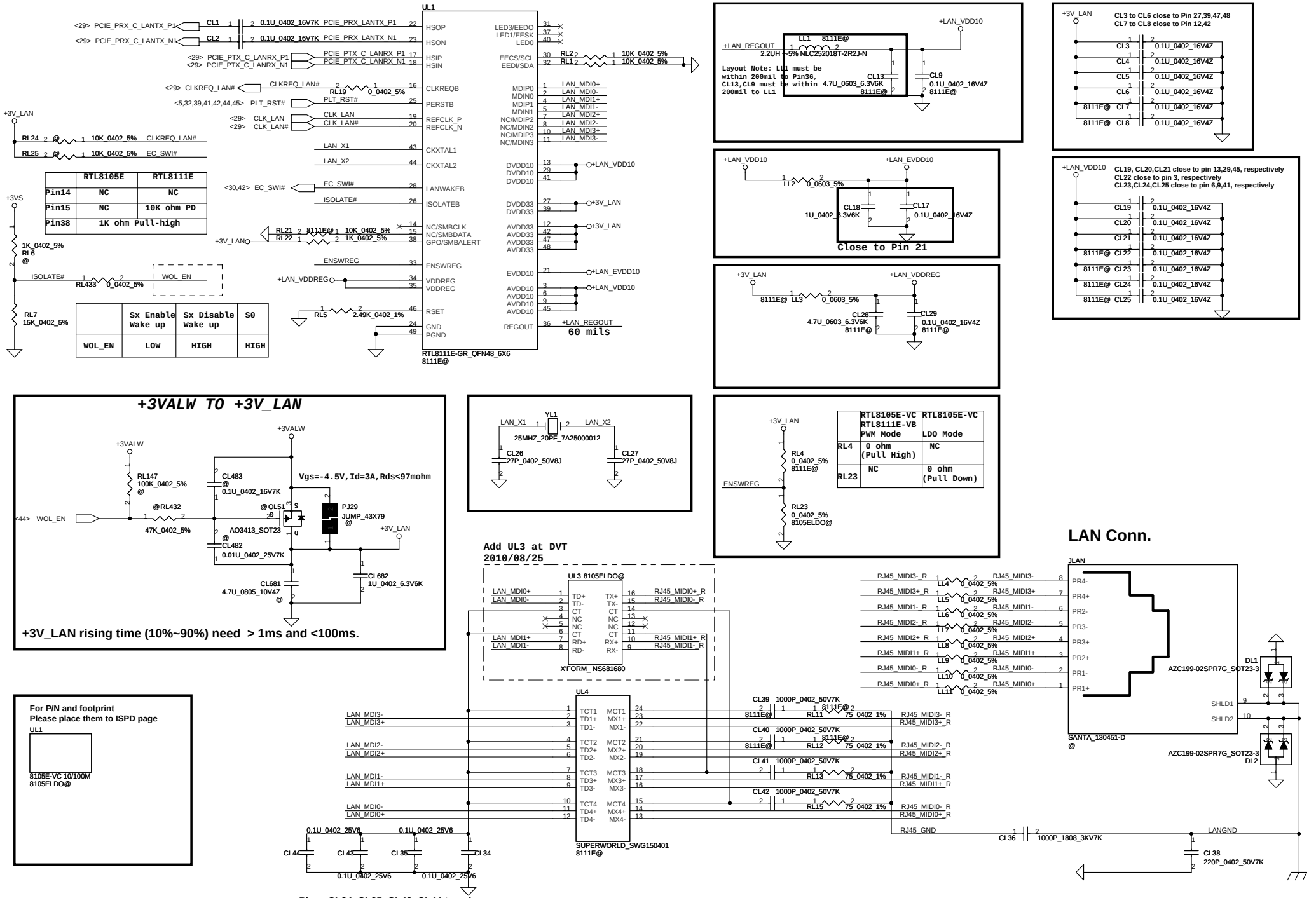
Title: **SCHEMATIC, MB A7211**

Size: | Document Number: **4019BD** | Rev: **B**

Date: Monday, February 28, 2011 | Sheet 39 of 59



+3VALW TO +3V_LAN

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

	RTL8105E-VC RTL8111E-VB PWM Mode	RTL8105E-VC LDO Mode
RL4	0 ohm (Pull High)	NC
RL23	NC	0 ohm (Pull Down)

For P/N and footprint
Please place them to ISPD page
UL1
8105E-VC 10/100M
8105ELDO@

Add UL3 at DVT
2010/08/25

LAN Conn.

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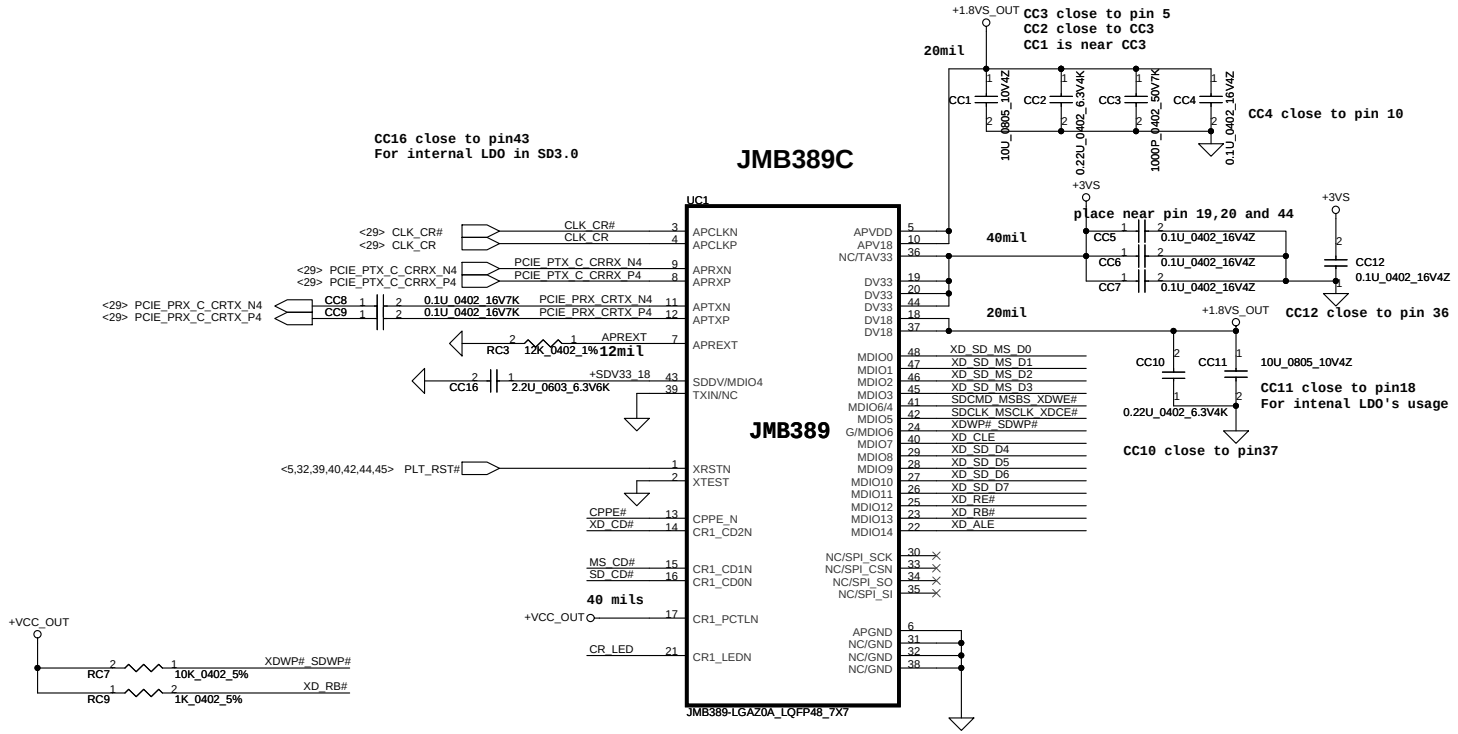
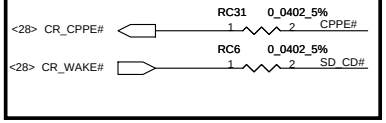
Title: SCHEMATIC, MB A7211

Size: Custom | Document Number: 4019BD | Rev: B

Date: Monday, February 28, 2011 | Sheet 40 of 59

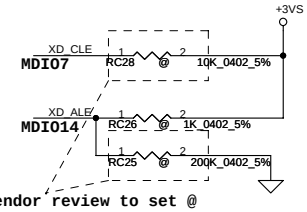


D3E mode

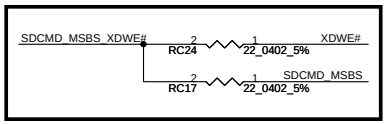


Power On Strapping setting

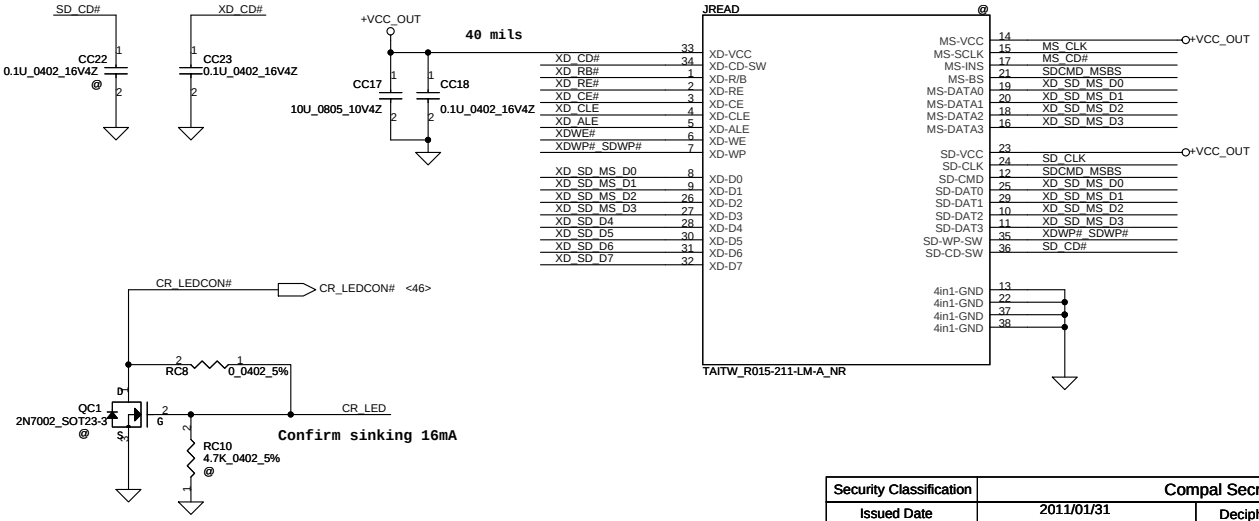
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★

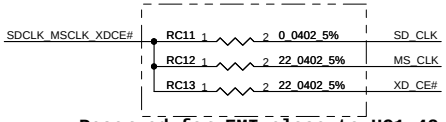


Add RC24 and RC17 close to UC1 for xD issue

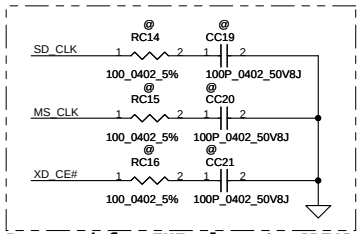


5 in 1 Card Reader





Reserved for EMI,close to UC1.42
Change RC11 from 22ohm to 0ohm
in order fix SDXC performance low.



Reserved for EMI,close to JREAD

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Issued Date	2011/01/31	Deciphered Date	2012/12/31

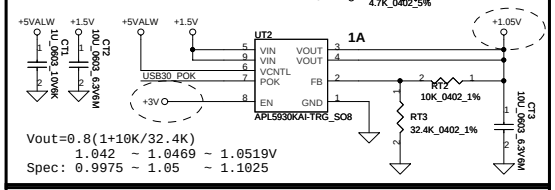
Compal Electronics, Inc.

Title: SCHEMATIC, MB A7211

Size: Custom | Document Number: 4019BD | Rev: B

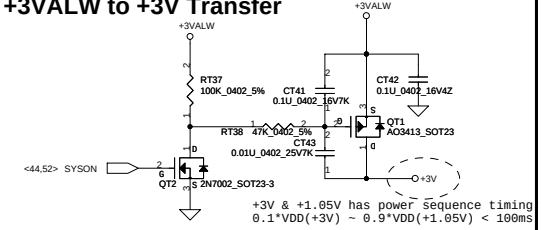
Date: Monday, February 28, 2011 | Sheet 41 of 59

+1.5V to +1.05V Transfer



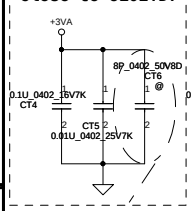
Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

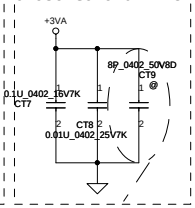


+3V & +1.05V has power sequence timing
0.1*VDD(+3V) ~ 0.9*VDD(+1.05V) < 100ms

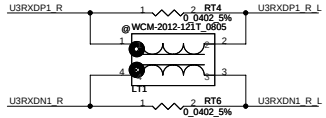
Close to U102.D7

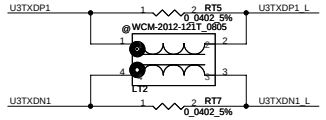


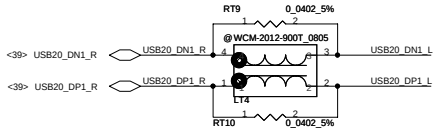
Close to U102.P13

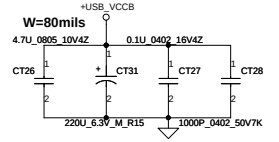


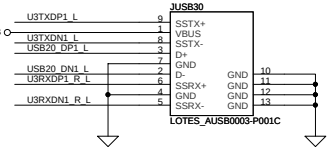
Follow Vendor recommend.

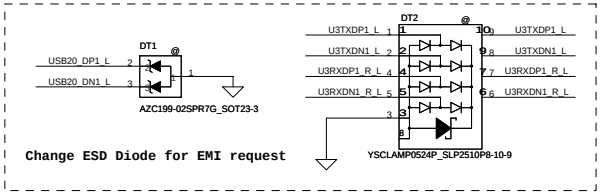


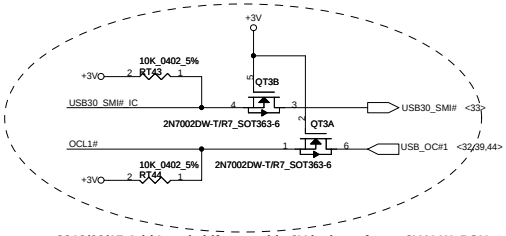












2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

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Issued Date	2011/01/31	Deciphered Date	2012/12/31

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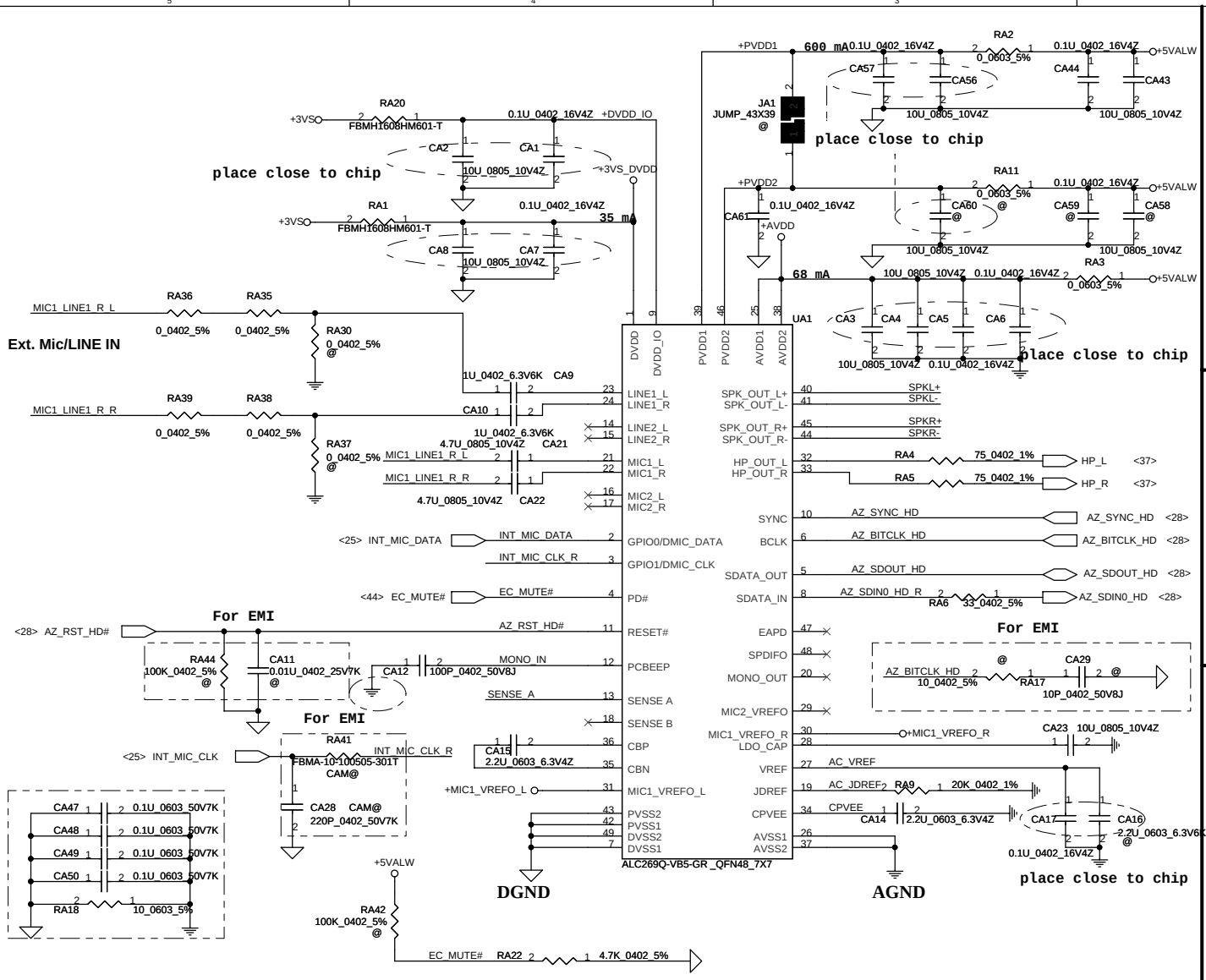
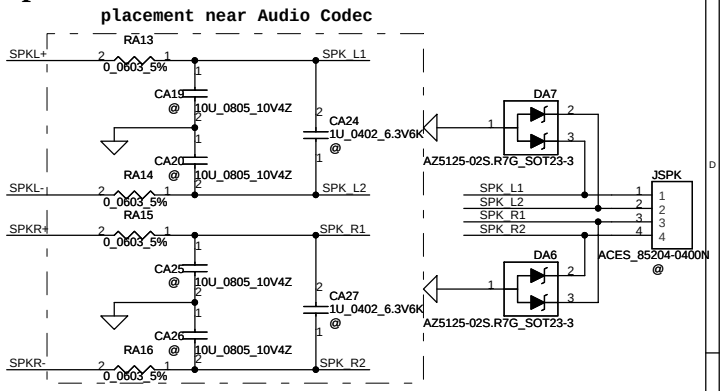
Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 42 of 59

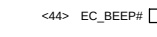


Speaker Connector

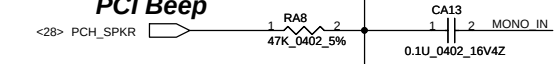
placement near Audio Codec



EC Beep

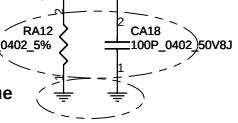


PCI Beep



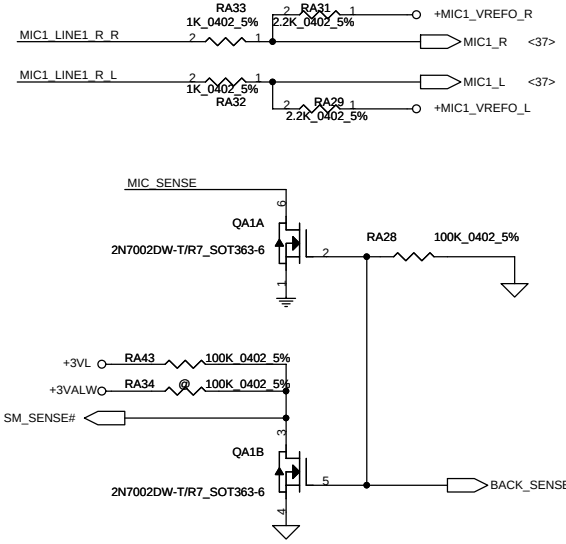
Beep sound

Change value for Beep by A51 demand. 2010/08/31



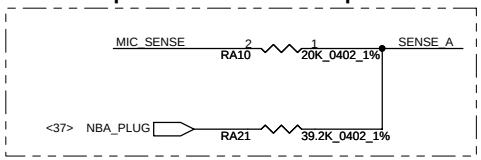
Change to AGND for high frequency noise issue

Ext.MIC/LINE IN JACK



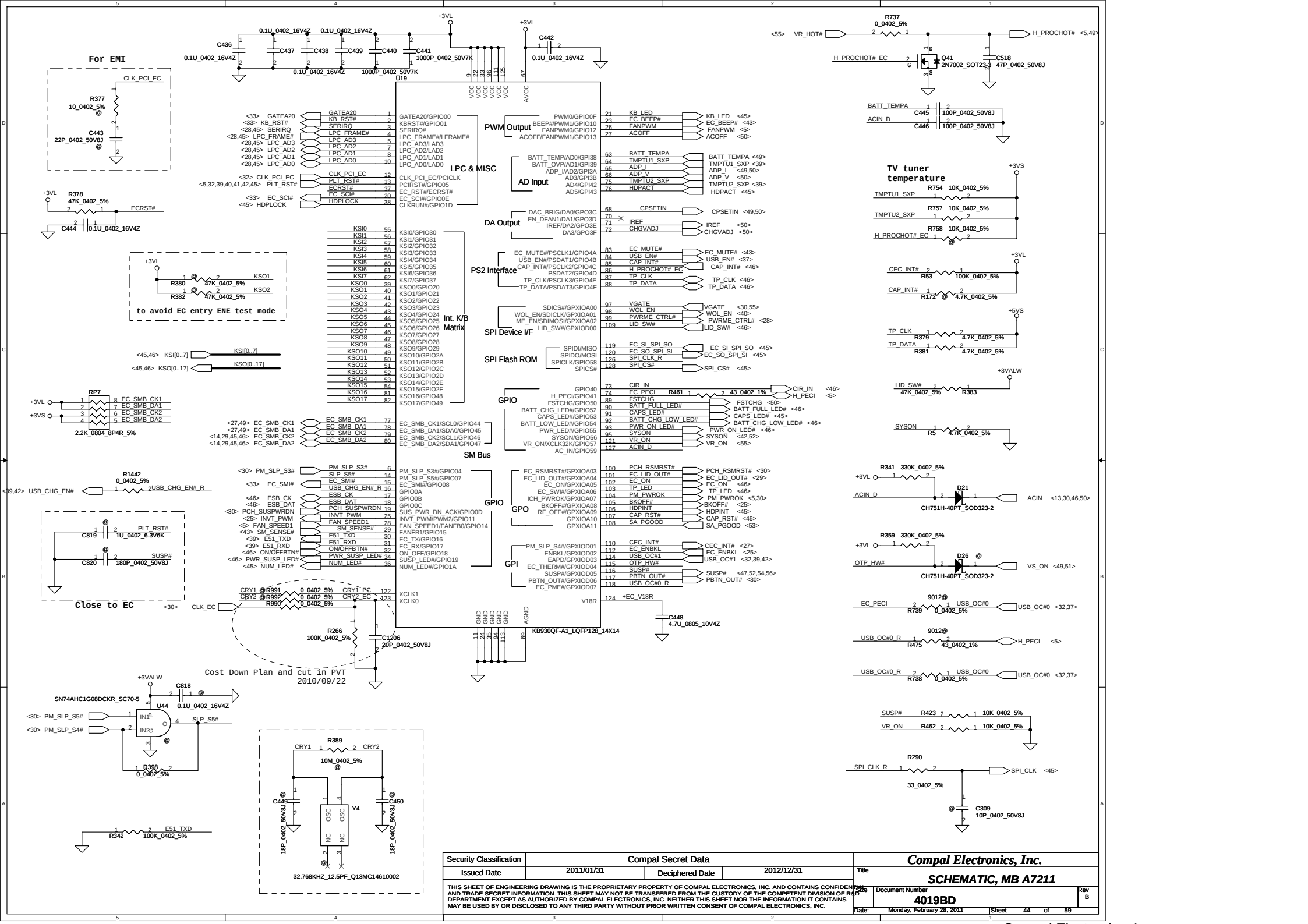
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

place close to chip



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	SCHEMATIC, MB A7211
Size	Document Number: 4019BD
Rev	B
Date:	Monday, February 28, 2011
Sheet	43 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

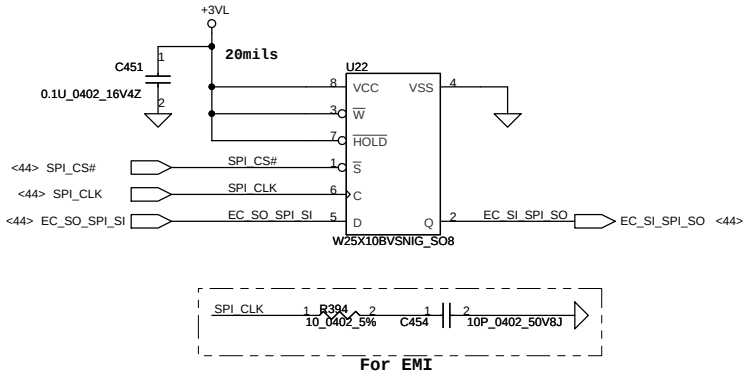
Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size	Document Number	Rev
	4019BD	B

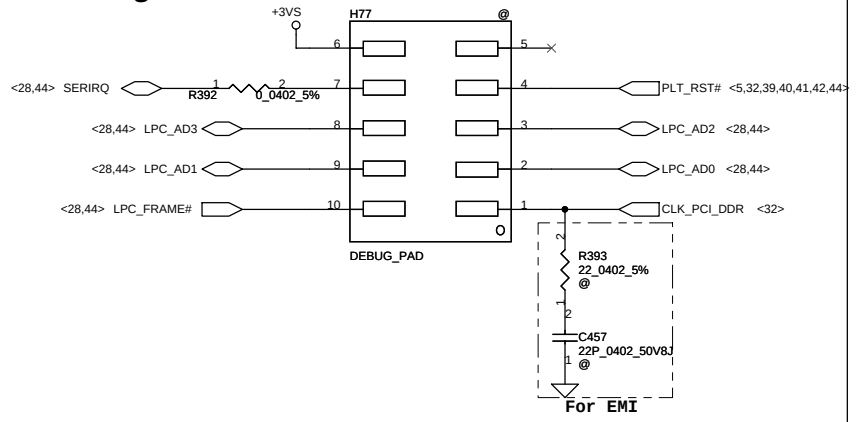
Date: Monday, February 28, 2011 Sheet 44 of 59

SPI Flash (256KB)

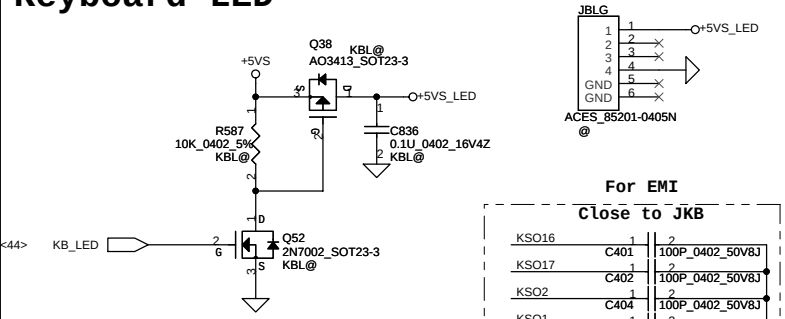


LPC Debug Port

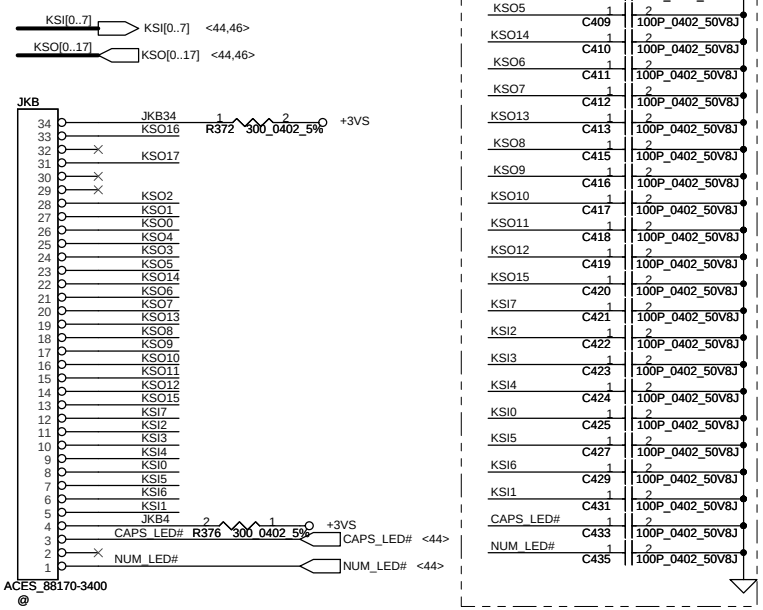
Place the PAD under DDR DIMM.



Keyboard LED

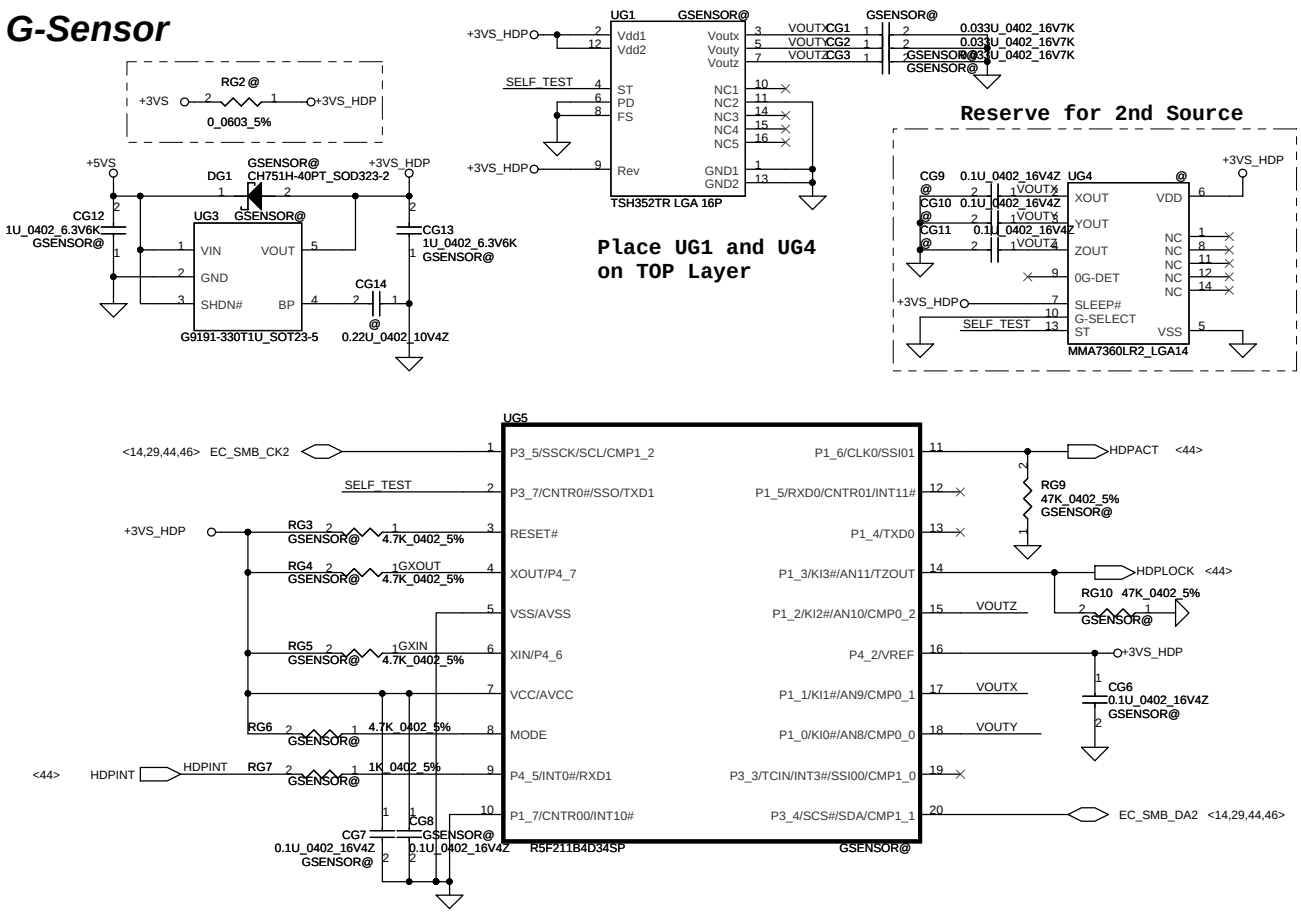


KEYBOARD CONN.



For EMI
Close to JKB

G-Sensor



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

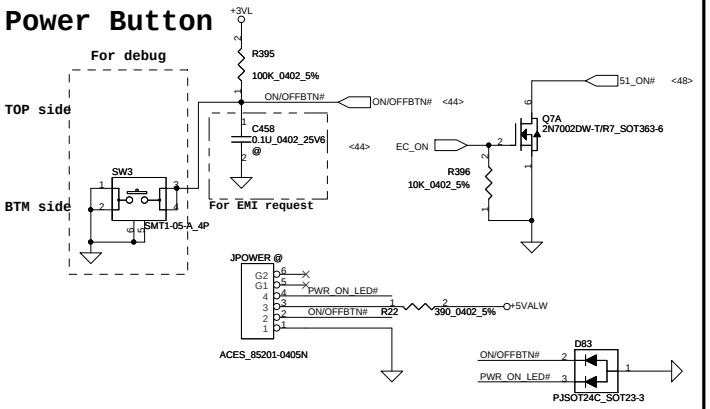
Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

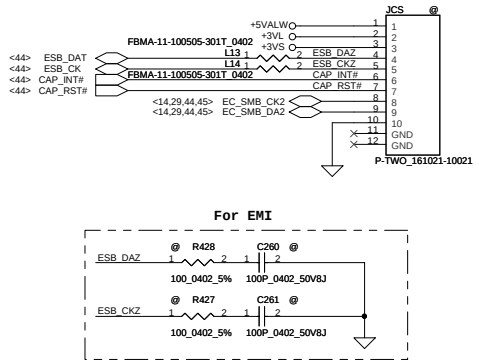
Size	Document Number	Rev
	4019BD	B

Date: Monday, February 28, 2011 Sheet 45 of 59

Power Button

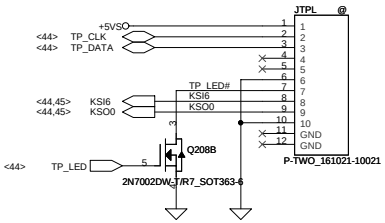


Caps Sensor/Light Sensor Conn.

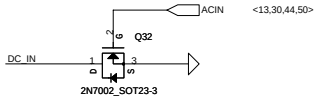


For EMI

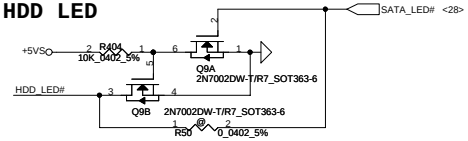
Touchpad & Light Pipe Connector



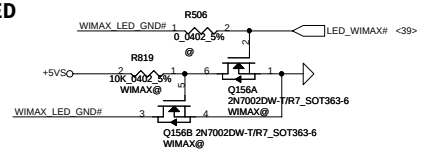
DC-IN LED



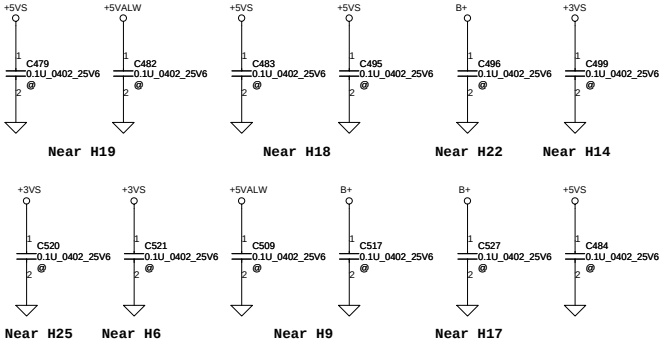
HDD LED



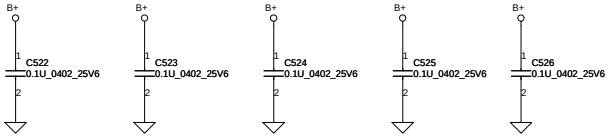
WiMAX LED



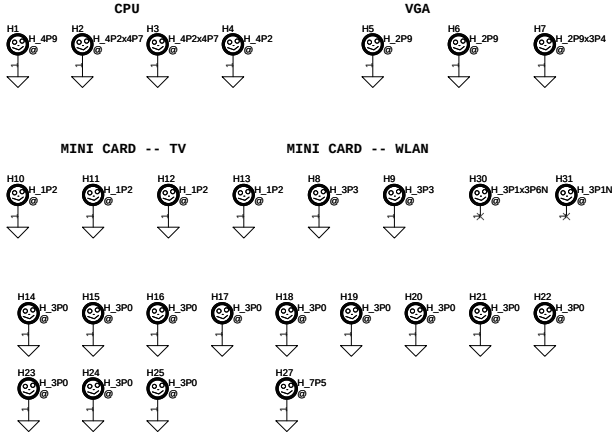
ESD solution



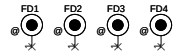
EMI solution



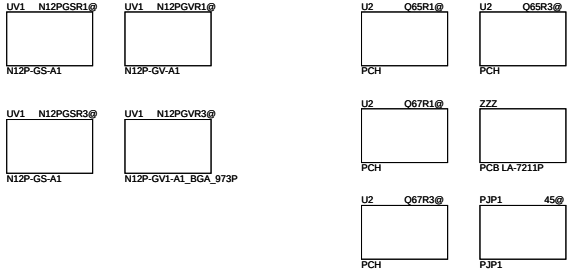
Screw Hole



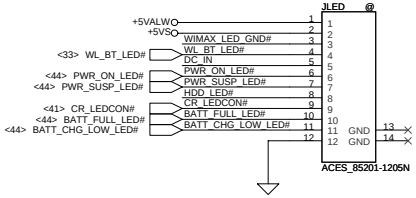
PCB Fedical Mark PAD



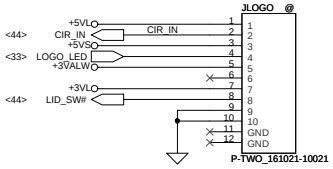
ISPD



LED/B Connector



LOGO/B Connector



Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

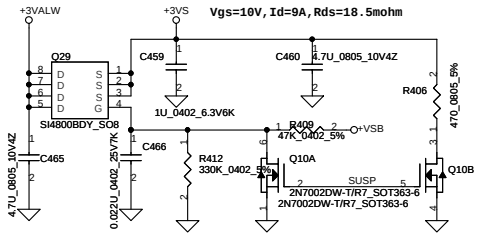
Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

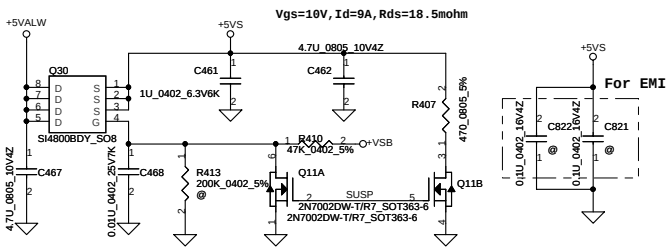
Size | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 46 of 59

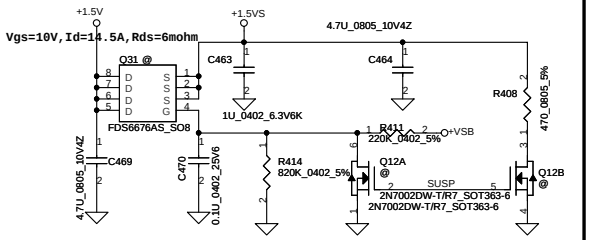
+3VALW TO +3VS

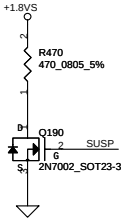


+5VALW TO +5VS

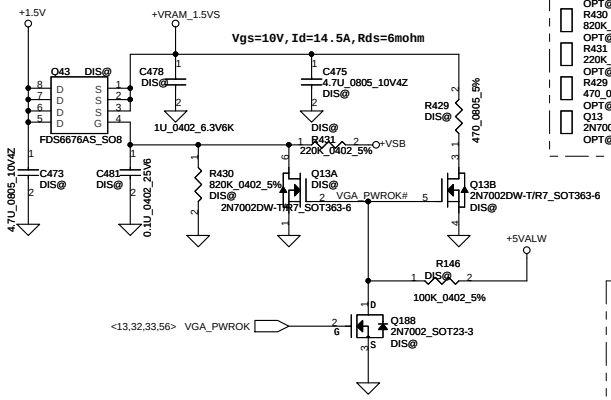


+1.5V to +1.5VS



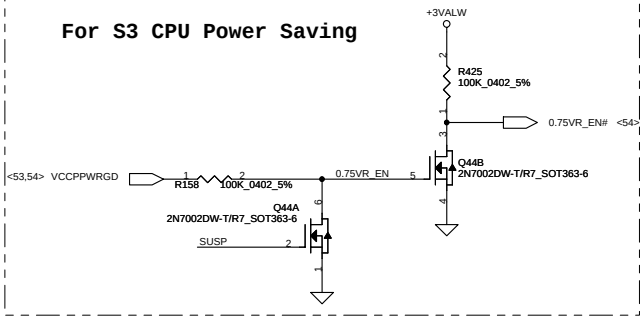


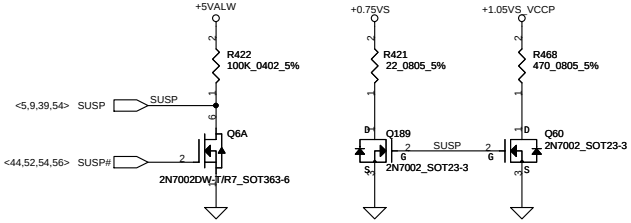
+1.5V to +VRAM_1.5VS



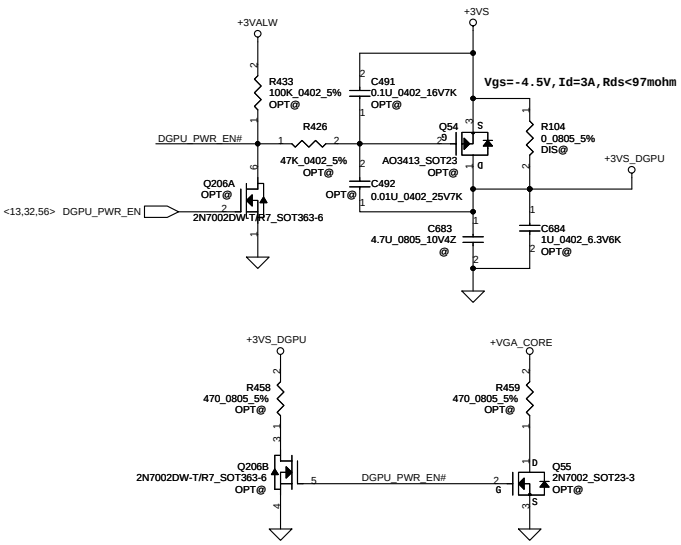
Q43 FDS6676AS_SO8 OPT@		C473 4.7U_0805_10V4Z OPT@	
C481 0.1U_0402_25V6 OPT@		C478 1U_0402_6.3V6K OPT@	
R430 820K_0402_5% OPT@		C475 4.7U_0805_10V4Z OPT@	
R431 220K_0402_5% OPT@		R146 100K_0402_5% OPT@	
R429 470_0805_5% OPT@		Q188 2N7002_SOT23-3 OPT@	
Q13 2N7002DW-T/R7_SOT363-6 OPT@			

For S3 CPU Power Saving

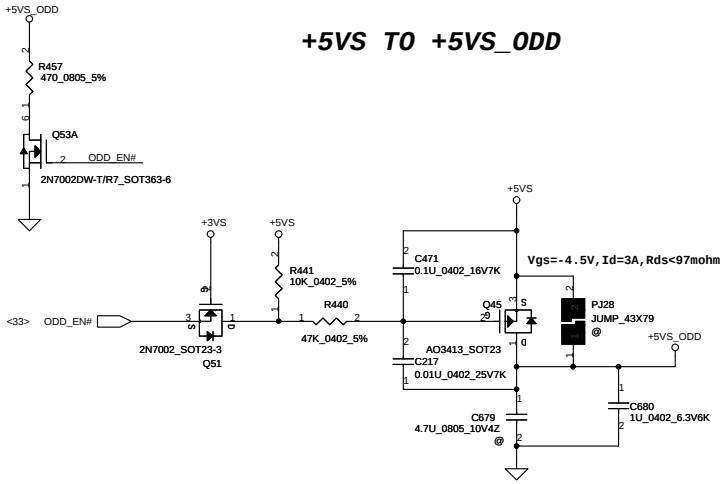




+3VS to +3VS_DGPU

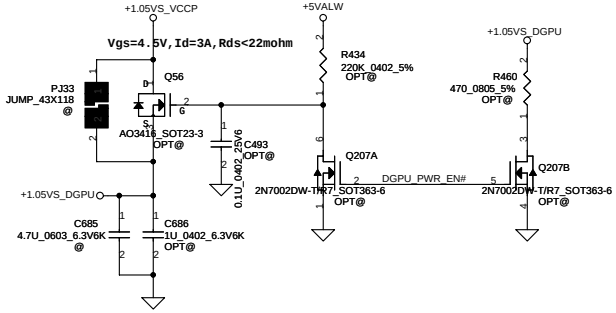


+5VS TO +5VS_ODD



+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs



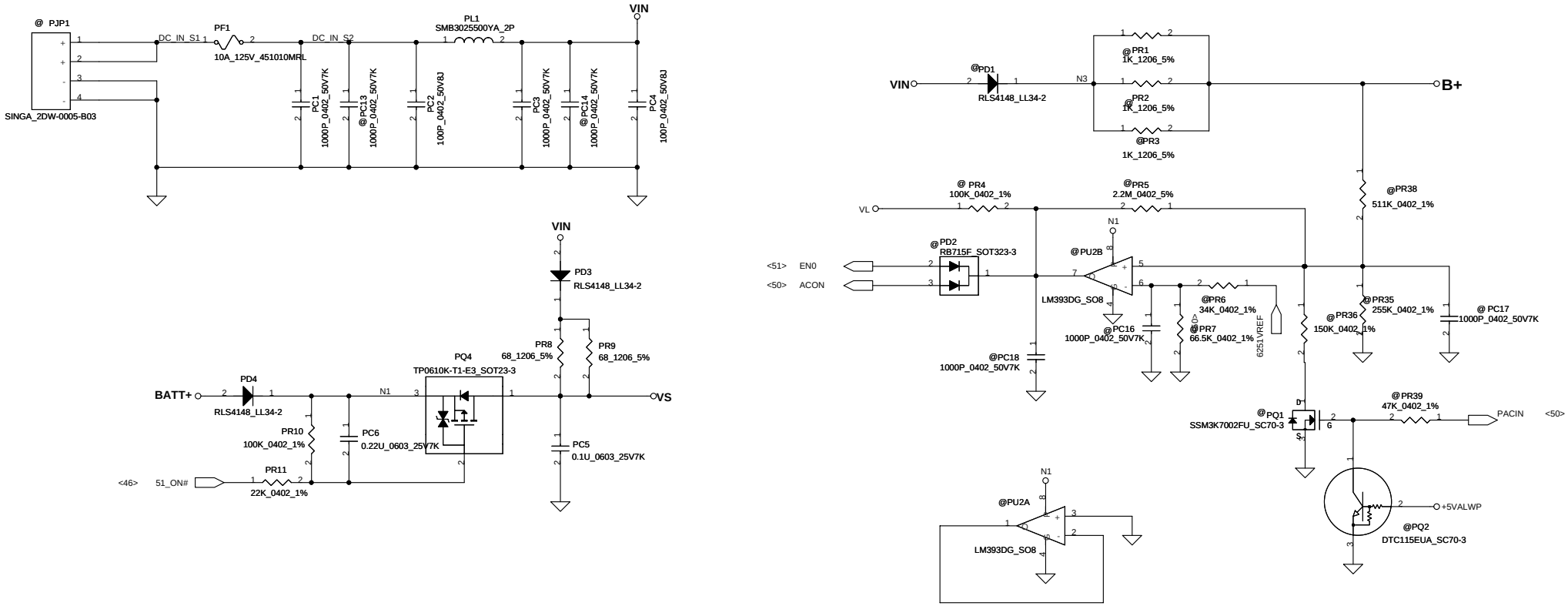
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: SCHEMATIC, MB A7211

Size	Document Number	Rev
	4019BD	B

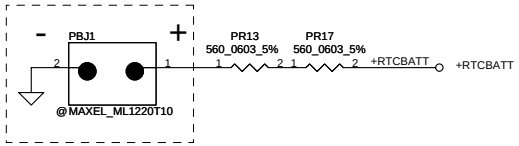
Date: Monday, February 28, 2011 Sheet 47 of 59



ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

RTC Battery



SP093MX0000

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

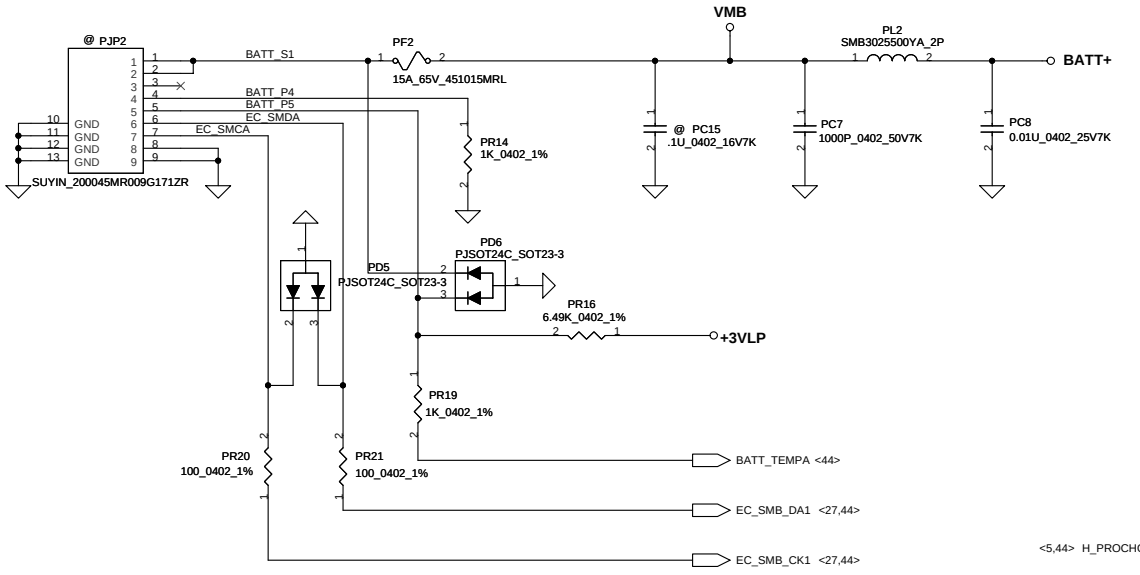
Compal Electronics, Inc.

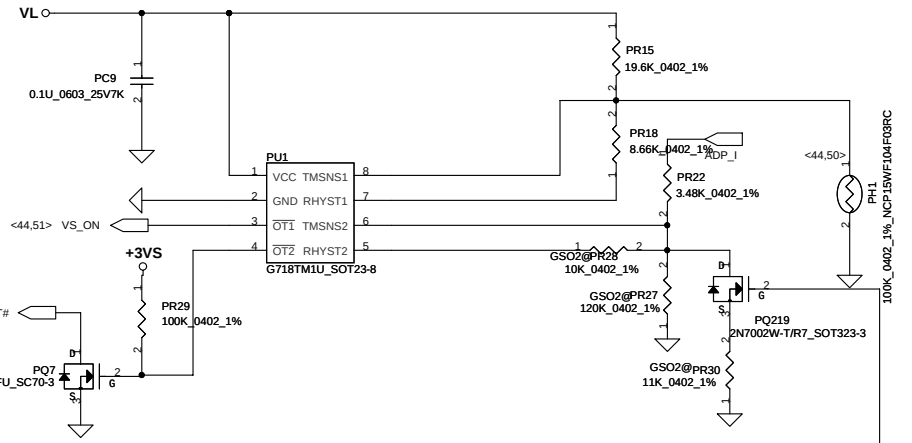
Title: ***SCHEMATIC, MB A7211***

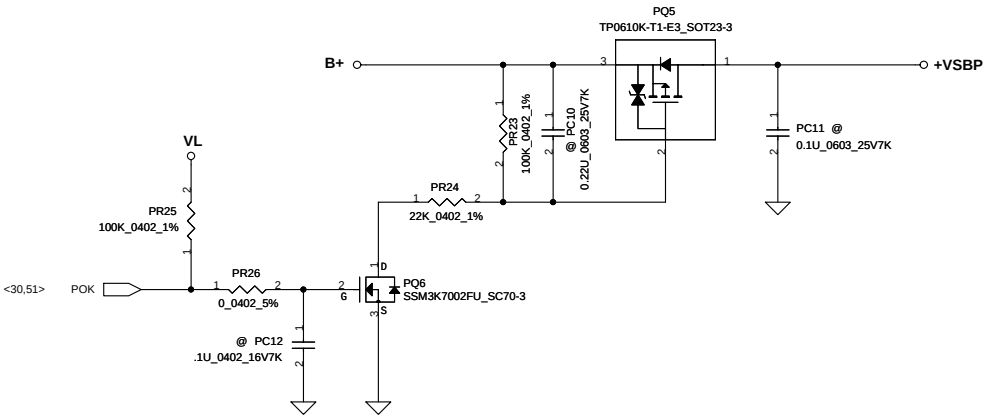
Size | Document Number: **4019BD** | Rev: B

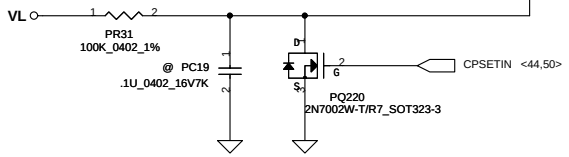
Date: Monday, February 28, 2011 | Sheet 48 of 59

PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C









GS2@ PR30 Value = 11K_0402_1%
GVO9@ PR30 Value = 14.7K_0402_1%
GS2@ PR28 Value = 10K_0402_1%
GVO9@ PR28 Value = 20K_0402_1%
GS2@ PR27 Value = 120K_0402_1%
GVO9@ PR27 Value = 15.8K_0402_1%

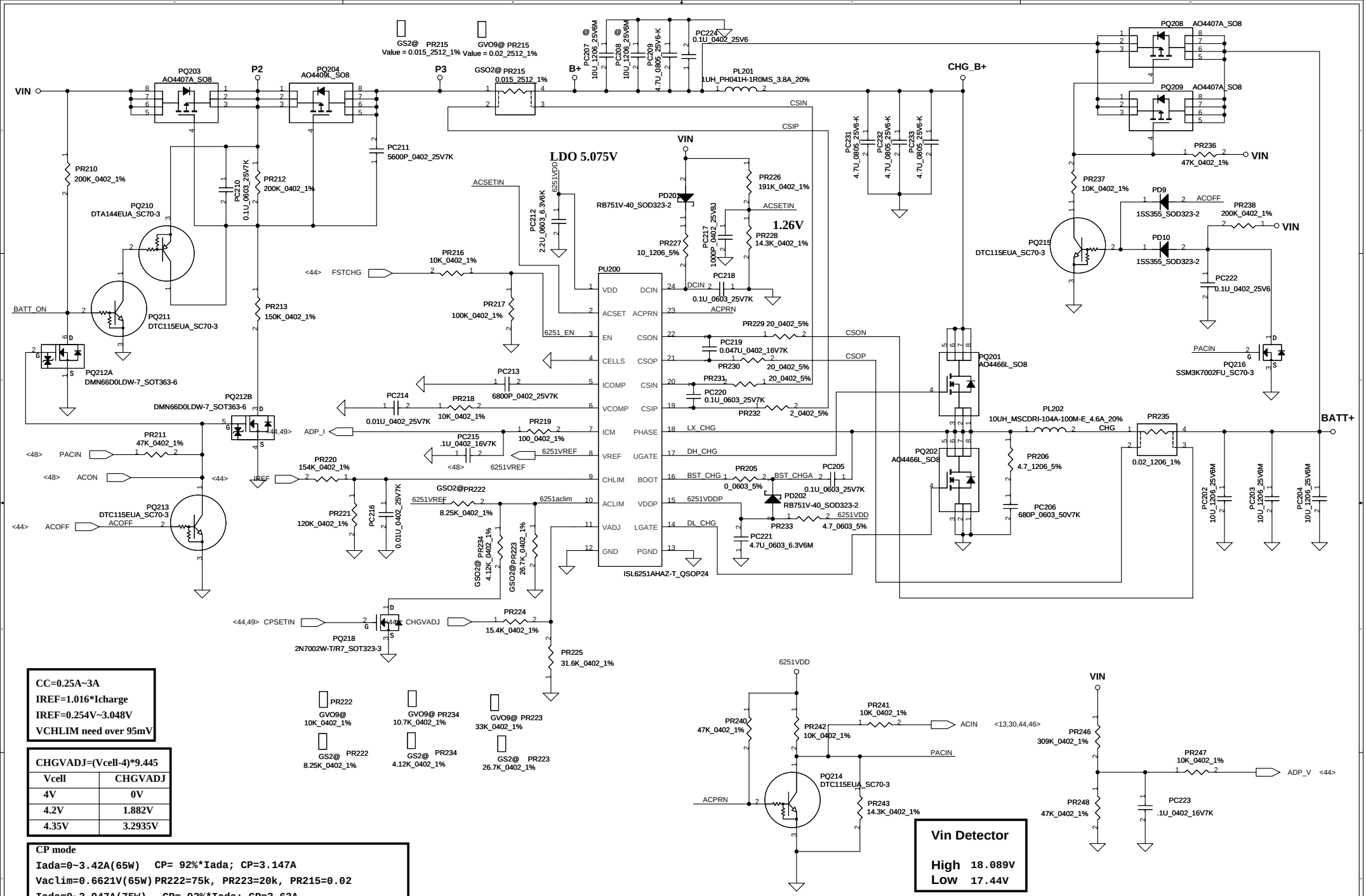
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: ***SCHEMATIC, MB A7211***

Size: | Document Number: **4019BD** | Rev: **B**

Date: Monday, February 28, 2011 | Sheet 49 of 59



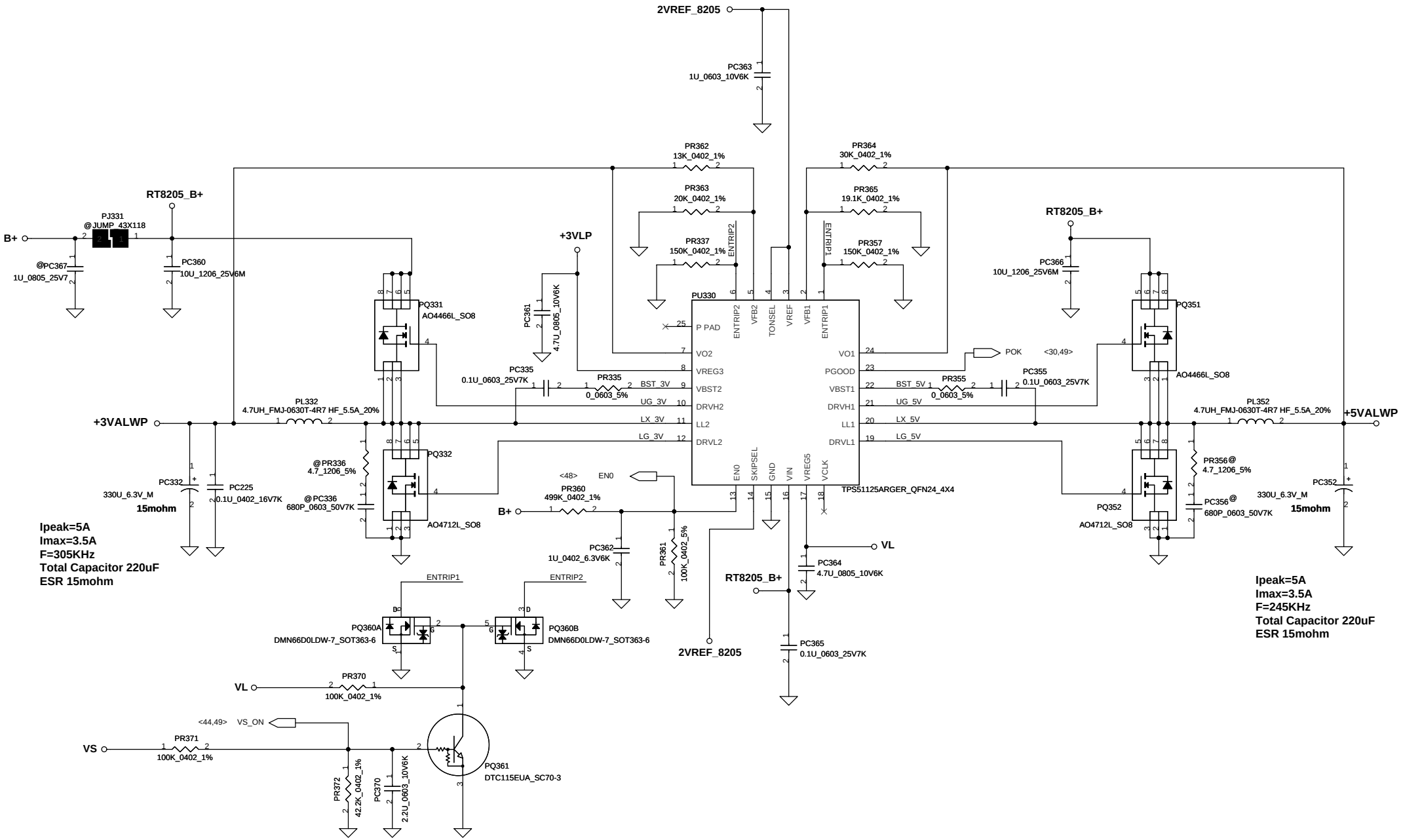
Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size	Document Number	Rev
Custom	4019BD	B

Date: Monday, February 28, 2011 Sheet 50 of 59



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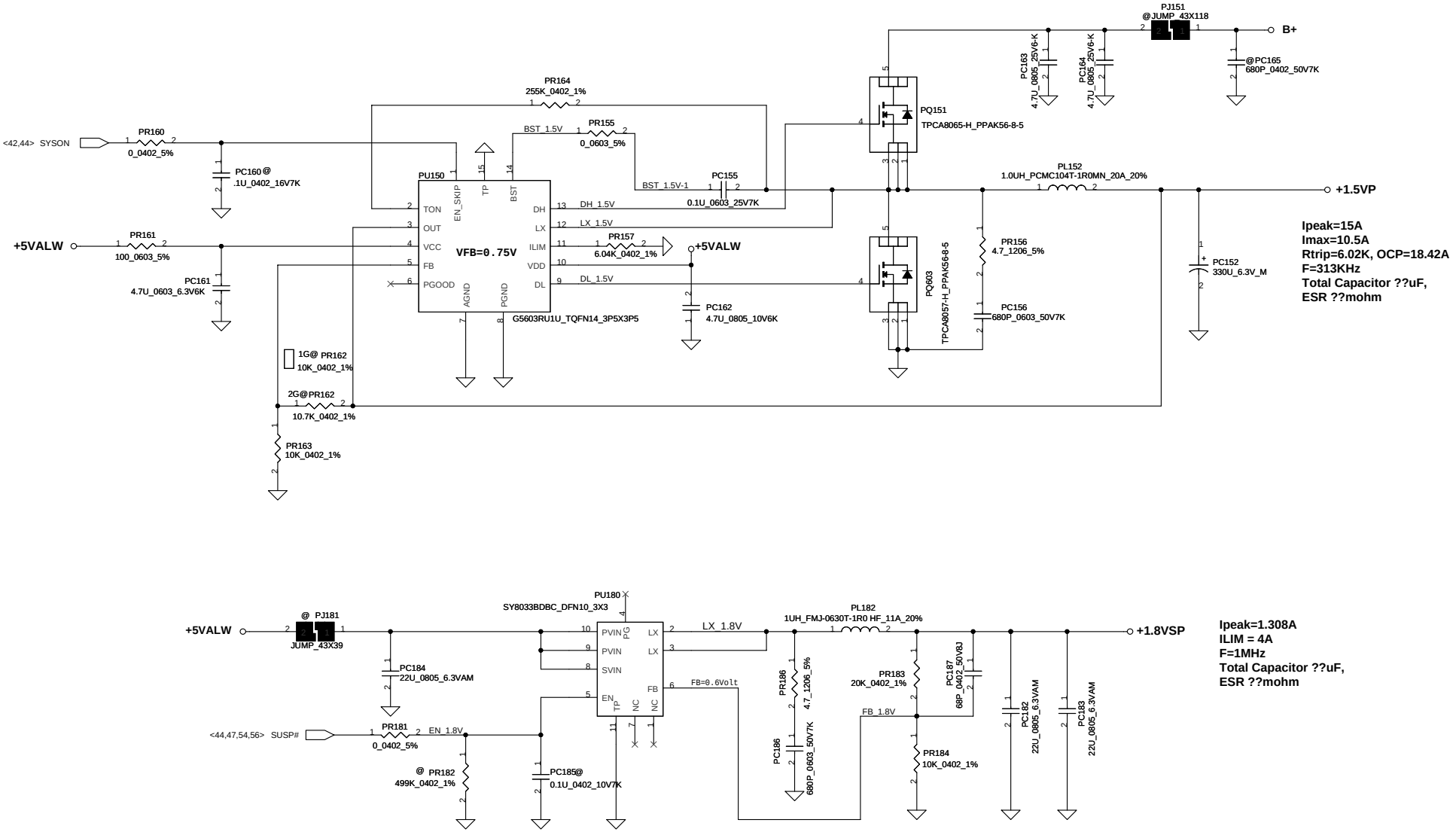
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 51 of 59



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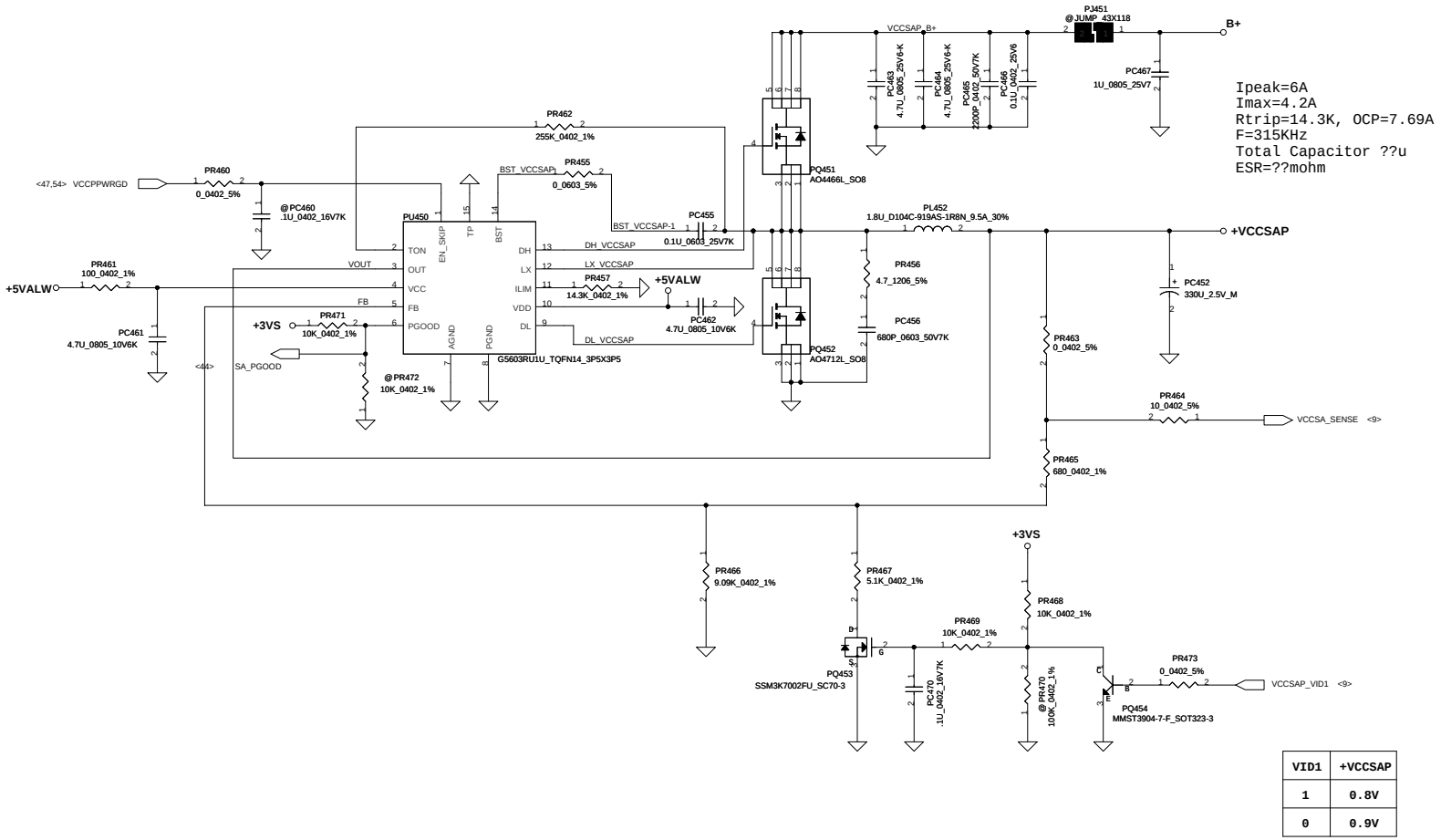
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: ***SCHEMATIC, MB A7211***

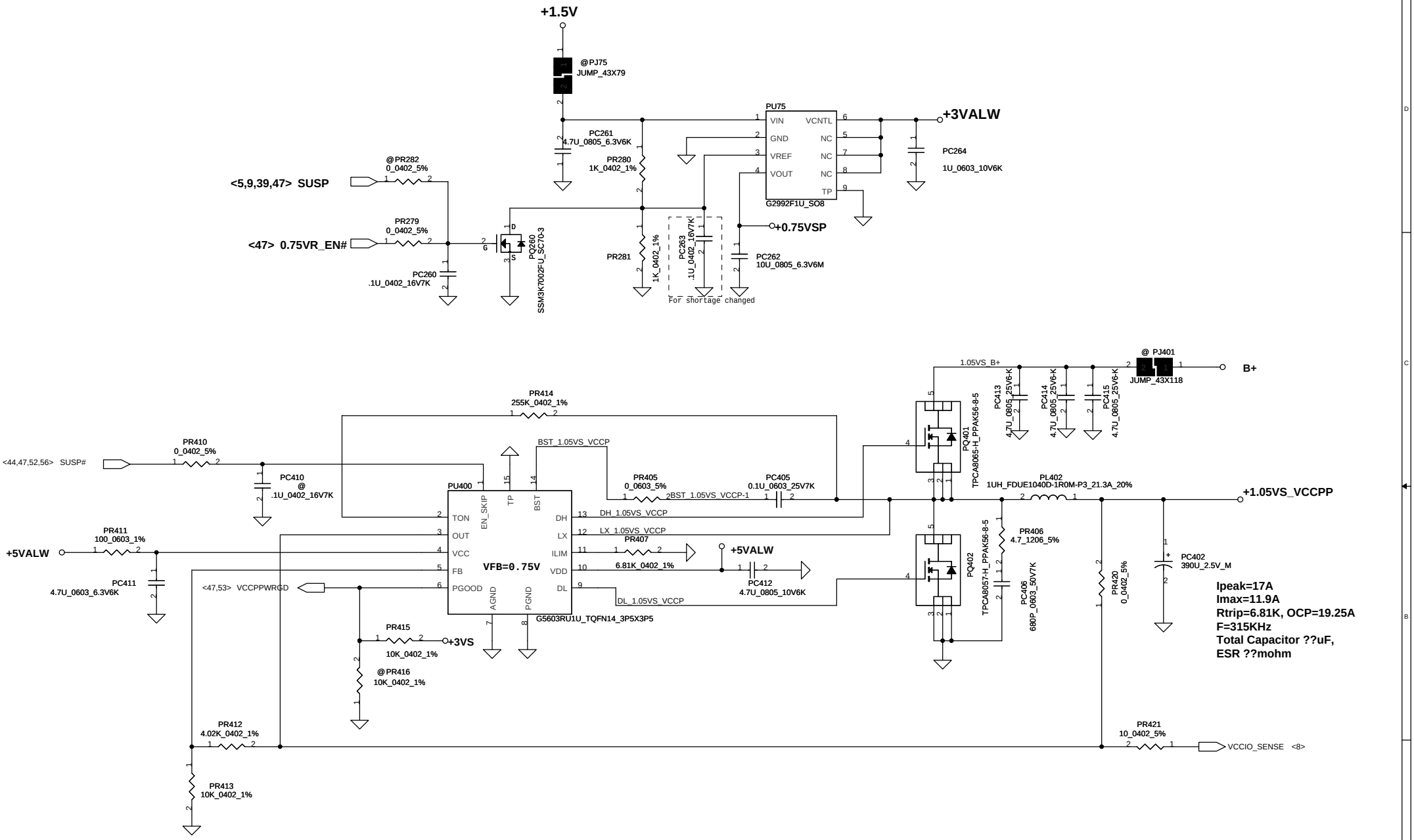
Size: Custom | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 52 of 59



VID1	+VCCSAP
1	0.8V
0	0.9V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/01/31	Deciphered Date	2012/12/31
Title	SCHEMATIC, MB A7211		
Size C	Document Number 4019BD		Rev B
Date: Monday, February 28, 2011	Sheet 53 of 59		


+1.5V
@PJ75
JUMP_43X79
PU75
VIN
GND
VREF
VOUT
VCNTL
NC
TP
G2992F1U_SO8
+3VALW
PC261
4.7U_0805_6.3V6K
PR280
1K_0402_1%
PC264
1U_0603_10V6K
@PR282
0_0402_5%
<5,9,39,47> SUSP
PR279
0_0402_5%
<47> 0.75VR_EN#
PQ260
SSM3K7002FU_SC70-3
PC260
.1U_0402_16V7K
PR281
1K_0402_1%
PC263
.1U_0402_16V7K
For shortage changed
PC262
10U_0805_6.3V6M
+0.75VSP
@ PJ401
JUMP_43X118
1.05VS_B+
B+
PC413
4.7U_0805_25V6-K
PC414
4.7U_0805_25V6-K
PC415
4.7U_0805_25V6-K
PQ401
TPCA8065-H_PPAK56-8-5
PR414
255K_0402_1%
PR410
0_0402_5%
<44,47,52,56> SUSP#
PC410
@
.1U_0402_16V7K
BST_1.05VS_VCCP
PU400
TON
OUT
VCC
FB
PGOOD
EN_SKIP
TP
BST
DH
LX
ILIM
VDD
DL
AGND
PGND
VFB=0.75V
G5603RU1U_TQFN14_3P5X3P5
DH_1.05VS_VCCP
LX_1.05VS_VCCP
DL_1.05VS_VCCP
PR405
0_0603_5%
2BST_1.05VS_VCCP-1
PC405
0.1U_0603_25V7K
PL402
1UH_FDUE1040D-1R0M-P3_21.3A_20%
+1.05VS_VCCPP
PR411
100_0603_1%
+5VALW
PC411
4.7U_0603_6.3V6K
<47,53> VCCPPWRGD
PR407
6.81K_0402_1%
+5VALW
PC412
4.7U_0805_10V6K
PQ402
TPCA8057-H_PPAK56-8-5
PR406
4.7_1206_5%
PC406
680P_0603_50V7K
PR420
0_0402_5%
PC402
390U_2.5V_M
Ipeak=17A
Imax=11.9A
Rtrip=6.81K, OCP=19.25A
F=315KHz
Total Capacitor ??uF,
ESR ??mohm
PR415
10K_0402_1%
+3VS
@PR416
10K_0402_1%
PR412
4.02K_0402_1%
PR413
10K_0402_1%
PR421
10_0402_5%
VCCIO_SENSE <8>
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2011/01/31
Deciphered Date
2012/12/31
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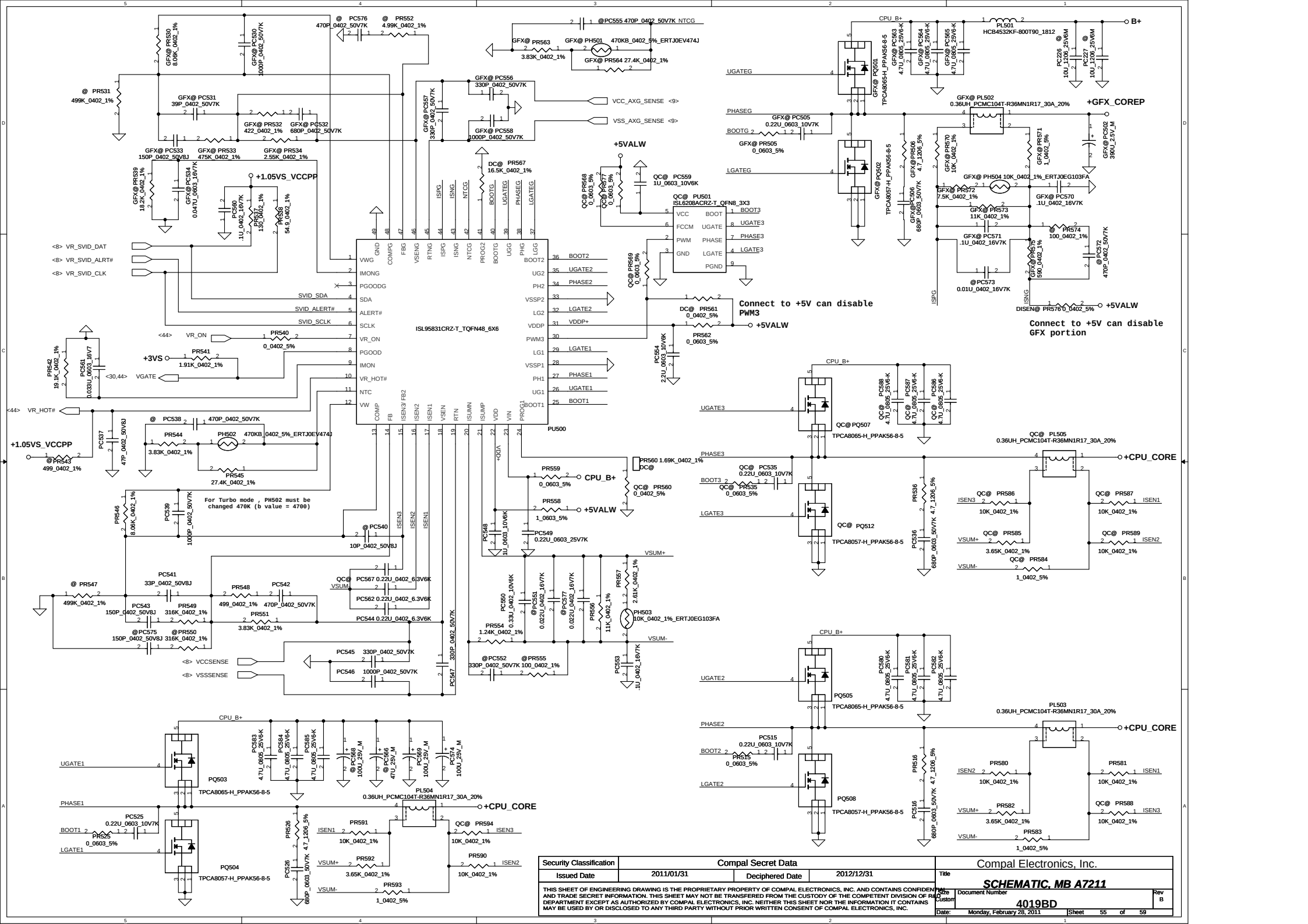
Monday, February 28, 2011
Sheet
54
of
59


ISL95831CRZ-T_TQFN48_6X6
PU500
ISL6208ACRZ-T_QFN8_3X3
QC@ PU501
Connect to +5V can disable PWM3
Connect to +5V can disable GFX portion
For Turbo mode , PH502 must be changed 470K (b value = 4700)
+GFX_COREP
+CPU_CORE
+1.05VS_VCCPP
+3VS
+5VALW
CPU_B+
B+
PL501 HCB4532KF-800T90_1812
PQ501 TPCA8065-H_PPAK56-8-5
PQ502 TPCA8057-H_PPAK56-8-5
PQ503 TPCA8065-H_PPAK56-8-5
PQ504 TPCA8057-H_PPAK56-8-5
PQ505 TPCA8065-H_PPAK56-8-5
PQ507 TPCA8065-H_PPAK56-8-5
PQ508 TPCA8057-H_PPAK56-8-5
PQ512 TPCA8057-H_PPAK56-8-5
PL502 0.36UH_PCMC104T-R36MN1R17_30A_20%
PL503 0.36UH_PCMC104T-R36MN1R17_30A_20%
PL504 0.36UH_PCMC104T-R36MN1R17_30A_20%
PH501 470KB_0402_5%_ERTJ0EV474J
PH502 470KB_0402_5%_ERTJ0EV474J
PH503 10K_0402_1%_ERTJ0EG103FA
PH504 10K_0402_1%_ERTJ0EG103FA
Security Classification
Compal Secret Data
Issued Date
2011/01/31
Deciphered Date
2012/12/31
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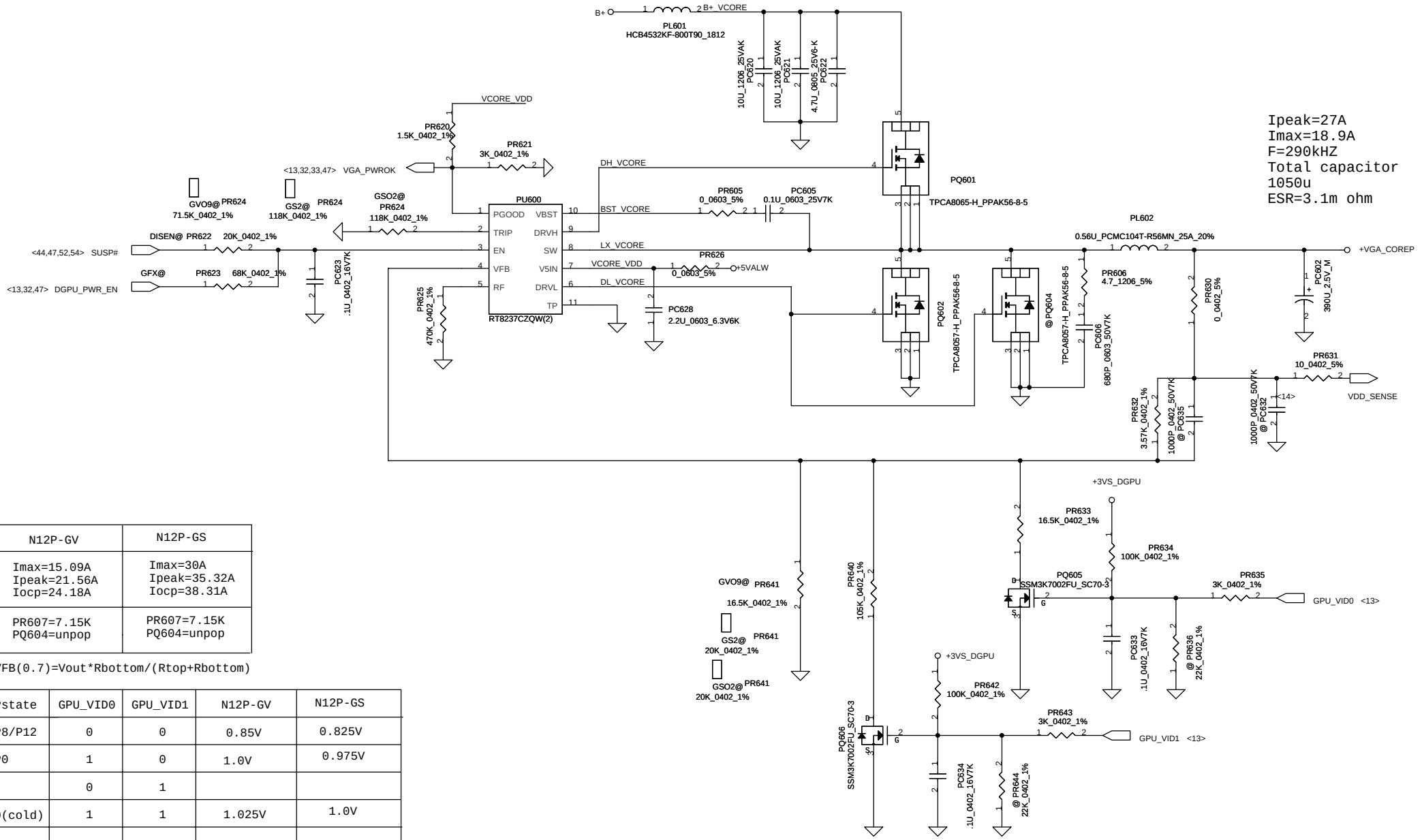
Title
SCHEMATIC, MB A7211
Size
Custom
Document Number
4019BD
Rev
B
Date:
Monday, February 28, 2011
Sheet
55
of
59



Ipeak=27A
Imax=18.9A
F=290kHZ
Total capacitor
1050u
ESR=3.1m ohm

N12P-GV	N12P-GS
Imax=15.09A Ipeak=21.56A Iocp=24.18A	Imax=30A Ipeak=35.32A Iocp=38.31A
PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop

VFB(0.7)=Vout*Rbottom/(Rtop+Rbottom)

Pstate	GPU_VID0	GPU_VID1	N12P-GV	N12P-GS
P8/P12	0	0	0.85V	0.825V
P0	1	0	1.0V	0.975V
	0	1		
P0(cold)	1	1	1.025V	1.0V
			PR632=3.57K PR641=16.5K PR633=16.5K PR640=105K	PR632=3.57K PR641=20K PR633=16.5K PR640=105K

Security Classification	Compal Secret Data		
Issued Date	2011/01/31	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **SCHEMATIC, MB A7211**

Size: Custom | Document Number: **4019BD** | Rev: **B**

Date: Monday, February 28, 2011 | Sheet 56 of 59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	
	2010/10/23	P49	Change PR29 to 100K,Delete PQ7	Circuit modify
	2010/10/23	P50	Change PQ204 to AO4409L,PR210 to 200K ohm,PR211 to 47k ohm	Circuit modify
			Change PQ212 to SB00000EO00,delete PQ218 ,add PR206,PC206	
			Change PR222 to 53.6K ohm,PR223 to 20k ohm for L01	
	2010/10/23	P51	Change PQ360 to SB00000EO00	Circuit modify
	2010/10/23	P52	Change PR157 to 6.04K ohm,PQ151 to TPCA8065,PQ603 TPCA8057	Circuit modify
			Change PL152 to 1UH,add PR156,PC156	
	2010/10/23	P53	Change PC452 to 220U_4.3mm height,add PR456,PC456	Circuit modify
	2010/10/23	P54	Change PQ401 to TPCA8065,PQ402 TPCA8057,add PR406,PC406	Circuit modify
	2010/10/23	P55	Add 3rd phase function,PC569,PC574,delete PC568,PC566	Circuit modify
			Change All high side to TPCA8065,all low side to TPCA8057	
			Add GFX function for L01,L03,add all sunnber	
	2010/10/23	P56	Add VGA_CORE function	Circuit modify
	2010/11/29	P48	Disable Pre charge function	Circuit modify
	2010/11/29	P49	Change PR22 to 3.48KΩ,PR28 to 30.9KΩ,PR27,PR31 to 100KΩ PR20 to 17.8KΩ, add PQ7	Circuit modify
	2010/11/29	P50	Change PR219 to 100KΩ,PL201 to 1UH,add PC204,PQ218	Circuit modify
			Change PR222 to 6.34KΩ,PR234 to 3.24KΩ,PR223 to 20KΩ	N12P-GS SKU
			Change PR222 to 53.6KΩ,PR234 to 5.49KΩ,PR223 to 20KΩ	N12P-GV SKU
			Add PC209,PC224	EMI request
	2010/11/29	P51	Add pc225	EMI request
	2010/11/29	P54	Change PR407 to 6.81KΩ	Circuit modify
	2010/11/29	P55	Add pc560	Circuit modify
	2010/11/29	P56	Change PR624 to 95.3KΩ,PR632 to 3.57KΩ,PR640 to 105KΩ PR633 to 16.5KΩ,PR641 to 20KΩ	N12P-GS SKU
			Change PR624 to 71.5KΩ,PR632 to 3.57KΩ,PR640 to 105KΩ PR633,PR641 to 16.5KΩ	N12P-GV SKU
	2010/12/29	P49	Change PR27 to 15.8KΩ,PR28 to 20KΩ,PR30 to 14.7KΩ	N12P-GV SKU
			Change PR27 to 120KΩ,PR28 to 10KΩ,PR30 to 11KΩ	N12P-GS SKU
	2010/12/29	P50	Change PR219 to 100Ω	Circuit modify
			Change PR222 to 10KΩ,PR223 to 33KΩ,PR234 to 10.7KΩ,PR215 to 20mΩ	N12P-GV SKU
			Change PR222 to 8.25KΩ,PR223 to 26.7KΩ,PR234 to 4.12KΩ	N12P-GS SKU
	2010/12/29	P55	Change PC549 to 0.22U_0603_25V	Circuit modify
	2010/12/29	P56	Change PU600 to RT8237C	Circuit modify
			Change PR624 to 118K	OCP modify
	2011/02/09	P49	Change PQ219,PQ220 to SB000009610	Circuit modify
	2011/02/09	P50	Change PC209 to 4.7U_0805,PQ218 to SB000009610	Circuit modify
			Add PR246,PR247,PR248,PC223	Add ADP_V
	2011/02/09	P52	Add PR186,PC186	Circuit modify
	2011/02/09	P53	Change PC452 to 330U_4.2H	Circuit modify
	2011/02/10	P55	Change PC537 to 47P_0403	Circuit modify

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Title: ***SCHEMATIC, MB A7211***

Size | Document Number: **4019BD** | Rev: B

Date: Monday, February 28, 2011 | Sheet 57 of 59

HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2010/10/26

Item	Date	Page	Component	Solution	Request
Base LA-6831 0929 schematic to modify					
Delete 14550@					
Delete 3G@					
Delete Felica@					
Delete UMA@					
Update ODD schematic for sub board					
Add logo board schematic					
Remove CIR and LID schematic to sub board					
Update TP Button for sub board					
Change JHDD1, JHDD2, JUSB, JLVDS, JFP, JFAN, JODD, JIR footprint for ME					
Change FAN schematic to PWM					
Modify Screw Hole for PHRAA ME					
1)	10/04	44	R290, C309	Reserve RC filter on SPI_CLK	For EMI request
2)	10/04	29	C314	Reserve Reserve 10P Cap on 48MCLK_USB30	For EMI request
3)	10/04	28	C315	Reserve 10P Cap on AZ_BITCLK_HD	For EMI request
4)	10/04	11	C317, C319, C339, C340, C352, C353	Reserve 6PCS 33P cap on +1.5V	For EMI request
5)	10/04	40		LAN_R_GND change to GND	For EMI request
6)	10/04	25	D84	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
7)	10/04	38	D82	Change ESD diode (D82) BOM to SC300000100	For ESD request
8)	10/04	37	D85, D86, D87	Reserve ESD diode and close to the connector	For ESD request
9)	10/04	43	DA6, DA7	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
10)	10/04	46	D83	Change ESD diode (D83) BOM to SCA00000E00	For ESD request
11)	10/04	32	C516	Reserve C516 on PLT_RST#	For ESD request
12)	10/05	38	JFP	Change footprint to P-TWO_161011-04021	For ME request
13)	10/06	27	L8,L9,L10,L11	Change Common mode choke to SM070000K00	For EMI request
14)	10/06	42	DT2	Change to SC600001600	For ESD request
15)	10/06	42	DT4	Add DT4	For ESD request
16)	10/06	25	R267,R268,R269 R270,R283,R333 R337,R329	Co-lay with optimus support 2-CH panel	For SPEC design ready
17)	10/09	25		Change JLVDS PIN define	For HW4 common design
18)	10/12	25		Change JLVDS PIN define	For layout request
19)	10/12	34	L22,C509	Change to test point T30	On-die VR default support
20)	10/12	34	R483,C280	Change to test point T36	On-die VR default support
21)	10/12	35	R498	Change to test point T41	On-die VR default support
22)	10/12	35	L20,C302	Change to test point T42	On-die VR default support
23)	10/12	35	L17,C296	Change to test point T43	On-die VR default support
24)	10/12	34	R541,R474,R480 R509,R517,R520	Change size to 0402	For layout request
25)	10/12	46		Change LID +3VALW to +3VL	
26)	10/12	06		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
27)	10/12	13		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
28)	10/12	09	R122,R252	Change from 100 ohm to 1k ohm	For HW4 schematic review
29)	10/12	09		Add +1.5VS to PJ30 and	For HW4 schematic review
30)	10/12	09		Change +1.5V from PJ30 to Q33	For HW4 schematic review
31)	10/12	29	R564	Change to @	For HW4 schematic review
32)	10/12	33	R124	Delete	For HW4 schematic review
33)	10/12	33	R444	Change BOM structure to mount	For HW4 schematic review
34)	10/12	05		Delete XDP function and change to test point	For layout space
35)	10/12	28		Delete PCH SPI schematic	For layout space
36)	10/12	37		Swap JPIO PIN define	
37)	10/12	42		Swap LT4	For layout request
38)	10/12	05		Update FAN control schematic	For HW4 schematic review
39)	10/12	40	CL43, CL44	Add CL43, CL44	For EMI request
40)	10/12	40	CL683,CL684	Delete CL683,CL684	For layout space
41)	10/12	42	JUSB30	Change to LOTES_AUSB0003-P001C	For ME request
42)	10/14	37	JHDD2	Change to ACES_88058-120N	
43)	10/14	46	H26,H28,H29	Delete	For ME last drawing
44)	10/14	46	H1~H7	Update screw hole	For ME last drawing
45)	10/14	38	L57	Swap L57	For layout request
46)	10/18	37	D86	Swap D86	For layout request
47)	10/18	25	D84	Change D84 BOM structure to install	For ESD request
48)	10/18	43	DA6,DA7	Change DA6,DA7 BOM structure to install	For ESD request
49)	10/18	46	C479,C482,C483 C484,C495,C496 C499,C500,C509 C517,C520	Reserve 0.1u Cap	For ESD request

Compal Electronics, Inc.			
Title: SCHEMATIC, MB A7211			
Size: Custom	Document Number: 4019BD		Rev: B
Date: Monday, February 28, 2011	Sheet 58 of 59		

HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0
GERBER-OUT DATE: 2011/01/31

NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
50)	10/20	29	R228	Change R228 from10k to 1k ohm	For Intel spec demand
51)	10/20	41	CC23	Mount CC23	For vendor demand
52)	10/20	44	R172	Change to @ due to the pull high will be in Cap sensor board	
53)	10/20	47	C493	Change C493 from 0.01uF to 0.1uF	To avoid inrush current.
54)	10/25	37	JHDD2	Swap JHDD2	For sub board
55)	10/25	14	RV114,RV115		For NV schematic
56)	10/25	16	RV480,RV481		
57)	10/25	24	RV107,RV109 RV116,RV117		
58)	10/26	38	QB4	Change QB4 from SB211970110 to SB00000R300	For sourcer demand
59)	10/26	39	U5	Change U5 from SA000045Z00 to SA00004GV00	For design change
60)	11/12	28	+3V_SPI	Change +3V_SPI to +3VS	For EVT issue
61)	11/12	44	R290	Mount R290	For EVT issue(88)
62)	11/12	11	C317,C319,C339 C340,C352,C353	Mount this part for DDR +1.5V return path	
63)	11/12	46	C522~C526	Mount this part	For EMI request
64)	11/12	39	D24	Remove D24	For SUSP# leakage
65)	11/12	20	CV228,CV229 CV230,CV231	Add VRAM +VRAM_1.5VS power rail	For NV demand
66)	11/12	21	CV232,CV233 CV234,CV235	Add VRAM +VRAM_1.5VS power rail	For NV demand
67)	11/12	22	CV236,CV237 CV238,CV239	Add VRAM +VRAM_1.5VS power rail	For NV demand
68)	11/12	44		Change EC GPXIOD04 from SLP_CHG# to OTP_HW	For PWR demand
69)	11/12	44	D26, R359	Add for OTP_HW function	For PWR demand
70)	11/12	44	R1428, R439	Remove for SLP_CHG#	For PWR demand
71)	11/12	26	T75,T76	Add test point at JCRT pin4, pin11	For CIC demand
72)	11/12	39	Q39,Q40	Add Q39,Q40	For avoid SUSP# leakage
73)	11/21	46	JPOWER	Reverse JPOWER pin define	
74)	11/21	37	JHDD2	Reverse (vertical and horizontal) JHDD2 pin define	
75)	11/21	46	H8,H9	Change H8&H9 to 3P3	
76)	11/25	42	LT1,LT2	Change to SM070001U00	For EMI request
77)	11/25	40	CL37,CL38	Remove CL37 and change CL38 from 4.7U to 220P	For EMI request
78)	11/25	40	LL4~LL11	Reserve LL4~LL11	For EMI request
79)	11/25	44	R383	Delete R383	For HW4 LID SW common design
80)	11/25	25,43	C13,CA28	Add C13 and CA28	For EMI request
81)	11/25	38		Seap JIR PIN define	For common with PHQAA
82)	11/25	46	C484,C495,C527	Reserve 0.1u Cap	For ESD request
83)	11/25	40	CL484~CL487	Add CL484~CL487 to 0.1 cap	For EMI request
84)	12/28	42	UT1	Change P/N to SA000048H00	
85)	12/28	25	R131	Add R131 for Sumsong panel issue	For panel issue
86)	12/28	44	R383	Add R383	For HW4 LID SW common design
87)	12/28	35	C333,C515	Change C333, C515 to 10uF	For HW4 cost down plan
88)	12/28	37	C426	Change C426 BOM structure to @	For HW4 cost down plan
89)	12/28	44	R398,U44,C818	Add R398 and change U44,C818 BOM structure to @	For HW4 cost down plan
90)	12/29	35	L19,L21	Change L19,L21 to SM010028480	For HW4 cost down plan
91)	12/29	37	C375~C378	Add C375~C378 on ODD fuction	
92)	12/29	37	C360	Add C360	For ESD request
93)	12/29	44	R475,R738,R739	Add R475,R738,R739	For 9012 co-lay
94)	01/19			Change D9,D55,DG1,D7,D8,D12,D14,D16,D21,D26, D25 to SCS00000Z00	
95)	01/19	05	D88	Change D88 to SC100001M00	
96)	01/19			Change U2 P/N to SA00004EE80	
97)	01/19	25	R387	Change R387 BOM structure t0 @	For 3D panel brightness issue
98)	01/19	08	C890,C894	Delete C890, C894	For power request
99)	01/19	08	C890	Change C891 to SGA20331E10	For power request
100)	01/19	08	C2,C7	Add C2,C7	For power request
101)	01/19	09		Change C873 to C112	For low ESR to pass transient
102)	01/19	25	R131	Change R131 to 47k	For 3D panel brightness issue
103)	01/19	32	R399	Change R399 BOM structure to @	For optimus device loss issue
104)	01/19	32	R544	Change R544 BOM structure to OPT@	For optimus device loss issue
105)	01/19	47	R434	Change R434 from 47K to 220K	For optimus device loss issue
106)	02/10	09	R877	Change R877 to @	For VCCSA voltage margin check ok
107)	02/10	32	R360	Add R360 to 0.1u	For ESD request
108)	02/10	46	U2	Change U2 P/N to SA00004EET0(R3 P/N) and SA00004EES0(R1 P/N)	
109)	02/10	46	UV1	Change UV1 P/N to SA000047U00(R3 P/N) and SA000047U20(R1 P/N)	
110)	02/10	46	PCB	Change PCB P/N to DAZ0I700100	

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Title: SCHEMATIC, MB A7211		
Size: Custom	Document Number: 4019BD	Rev: B
Date: Monday, February 28, 2011	Sheet 59 of 59	