

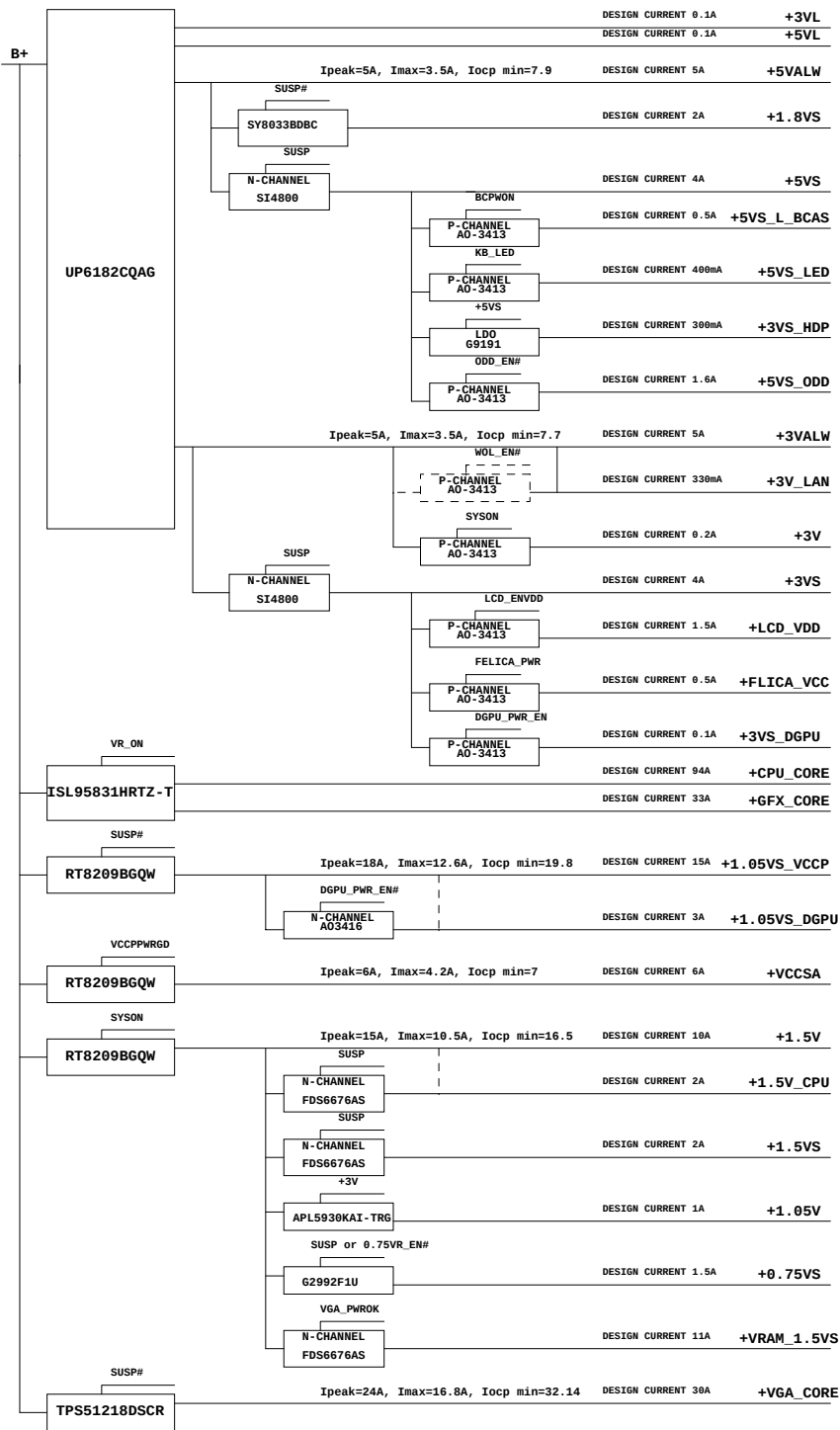
PHRAA

Superior 10/10G

LA-7211P REV 1.0 Schematic

**Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-01-31 Rev 1.0**

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				Document Number	
Date: Monday, February 28, 2011				Sheet 1 of 59	Rev B



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				4019BD	
				Date	Monday, February 28, 2011
				Sheet	3 of 69

Voltage Rails

(0 MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	0	0	0	0	0	0
S1	0	0	0	0	0	0
S3	0	0	0	0	0	X
S5 S4/AC	0	0	0	0	X	X
S5 S4/ Battery only	0	0	0	X	X	X
S5 S4/AC & Battery don't exist	0	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	NVIDIA GPU	9A H	1001 1010 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

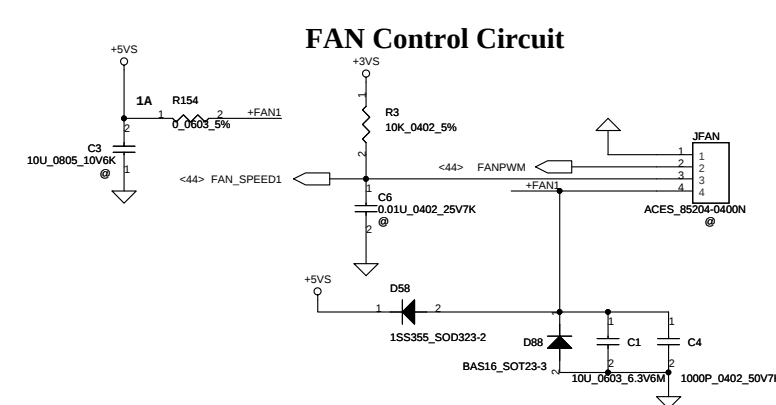
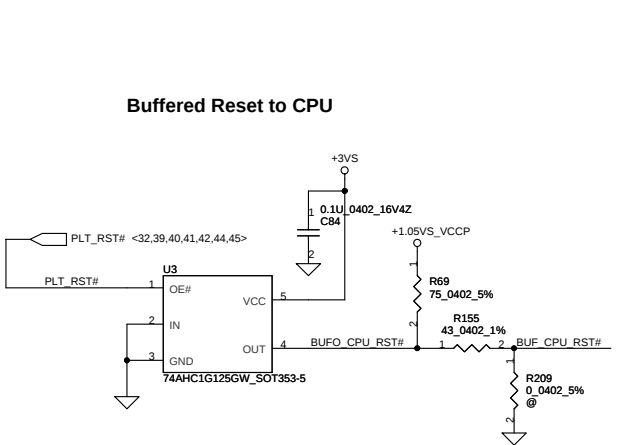
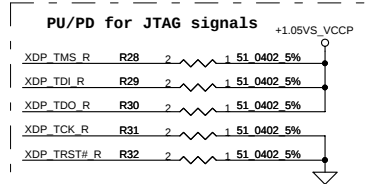
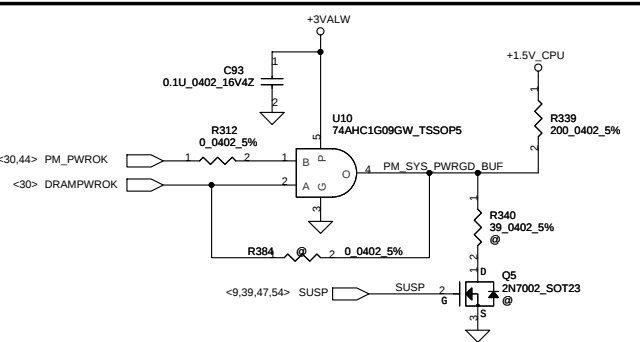
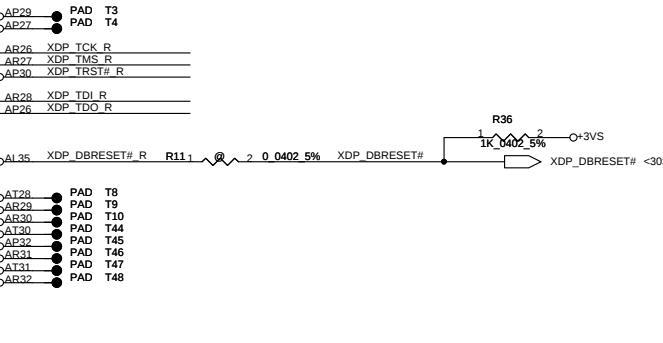
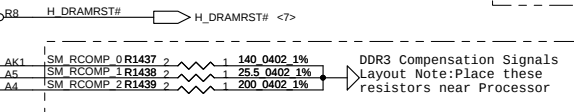
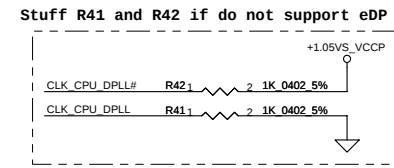
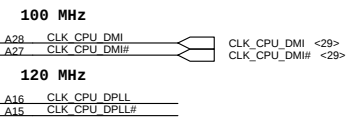
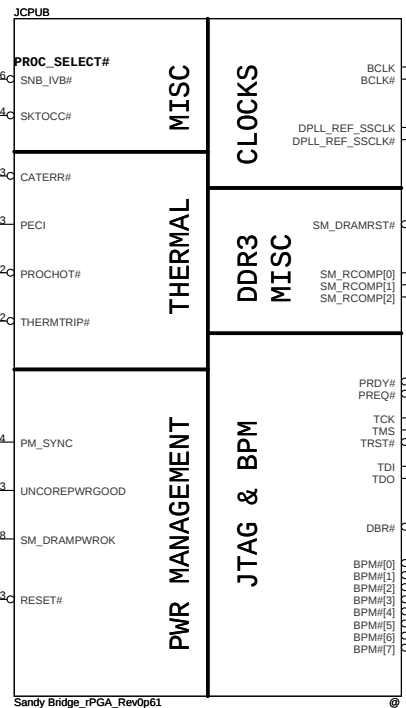
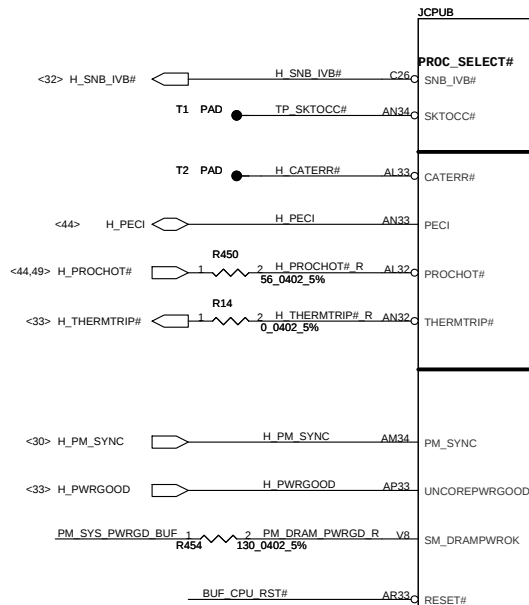
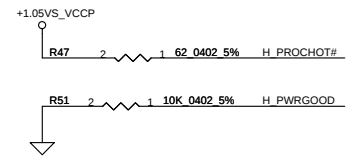
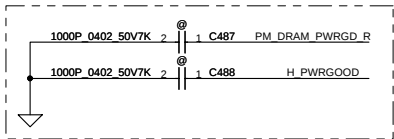
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

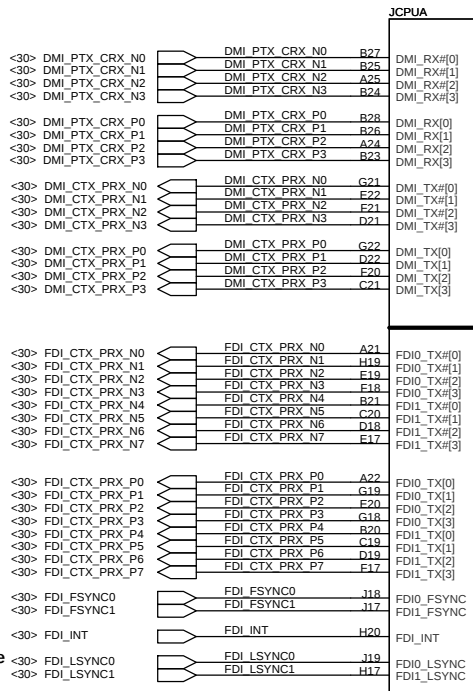
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

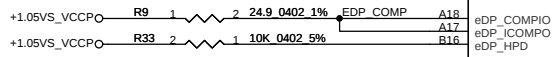
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						Document Number		Rev B	
						4019BD			
						Date: Monday, February 28, 2011		Sheet 4 of 59	



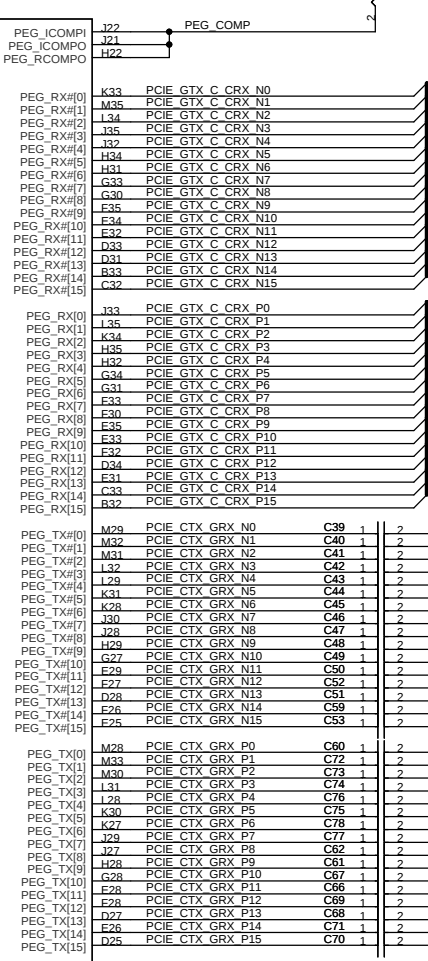
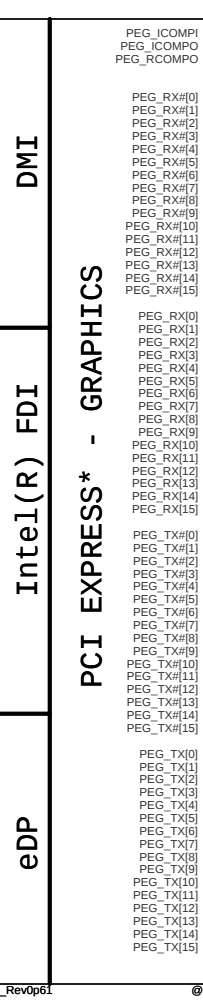
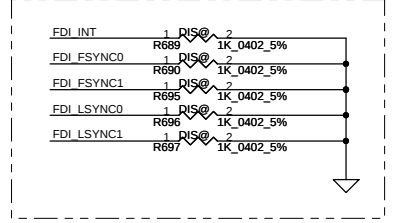
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				4019BD	
				Date: Monday, February 28, 2011	Sheet 5 of 59



eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm



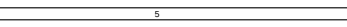
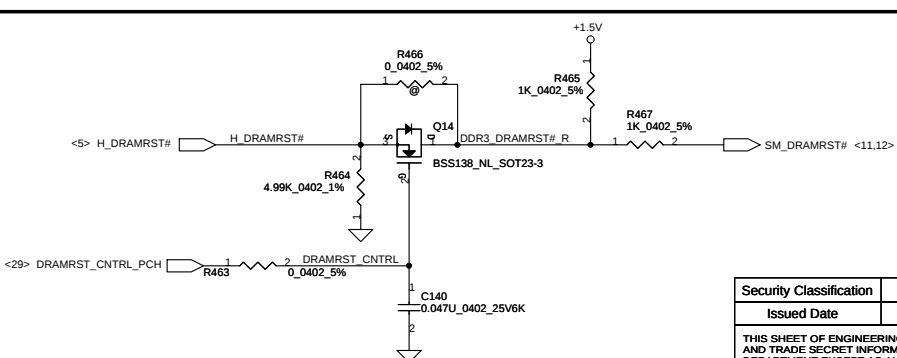
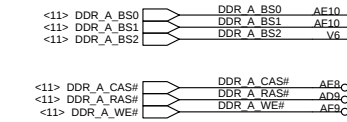
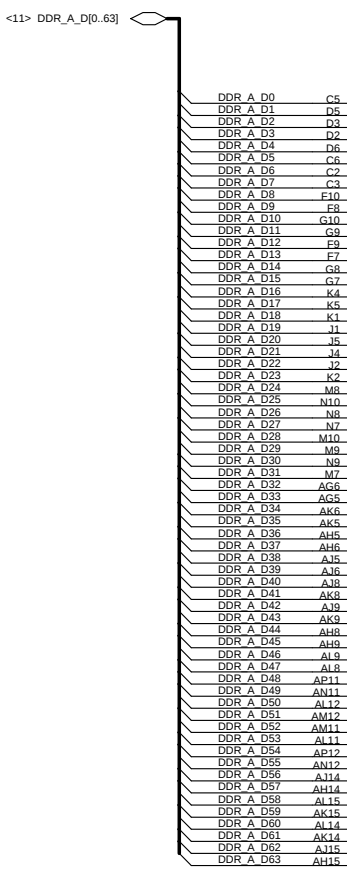
Close to CPU



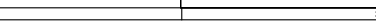
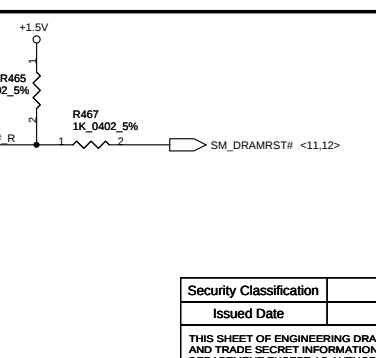
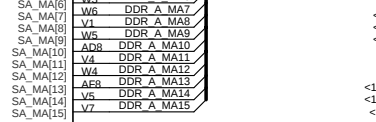
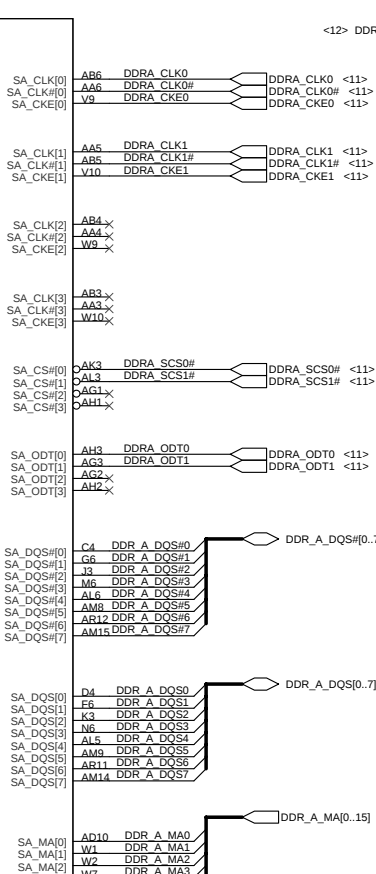
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

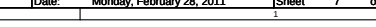
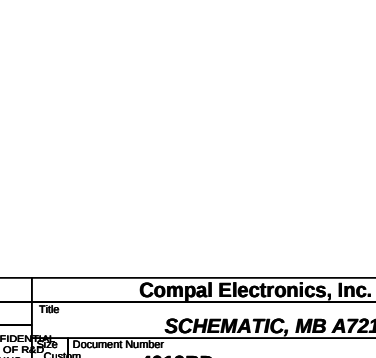
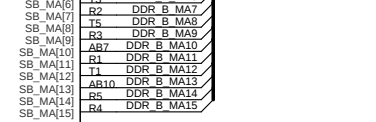
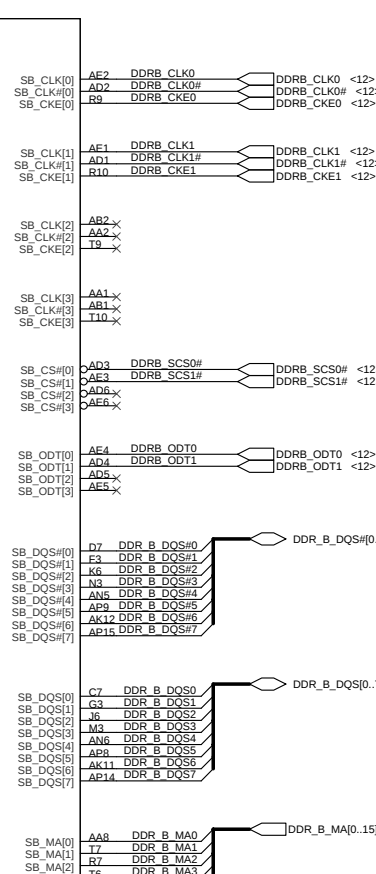
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				Date: Monday, February 28, 2011	Sheet 6 of 59



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B



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Compal Electronics, Inc.		Title	
Document Number		Rev	
4019BD		B	
Date		Sheet	
Monday, February 28, 2011		7 of 59	

POWER

94A (Quad Core 45W)
53A (SV 35W)

8.5A

PEG AND DDR

SVID

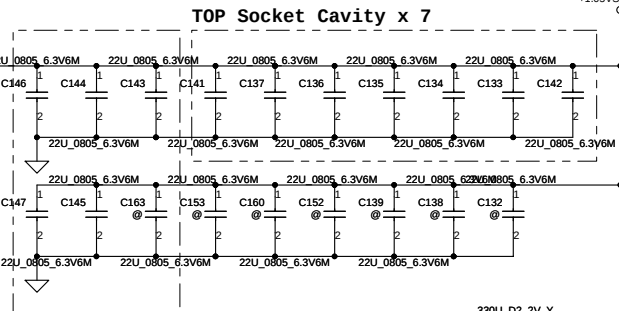
SENSE LINES

VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
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VCC30
VCC31
VCC32
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VCC98
VCC99
VCC100

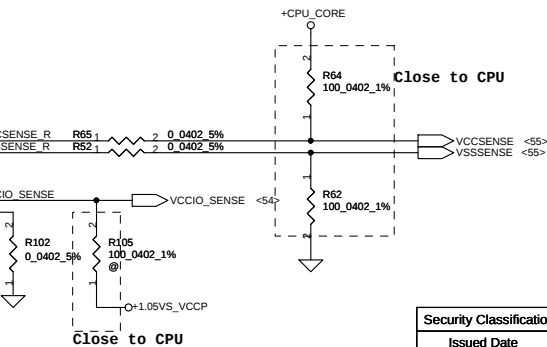
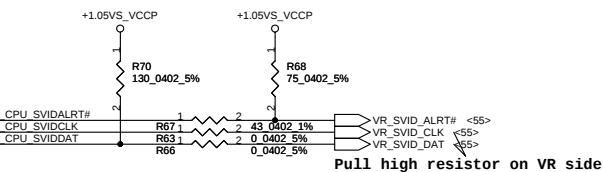
VIDALERT#
VIDSClk
VIDSOUT

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE



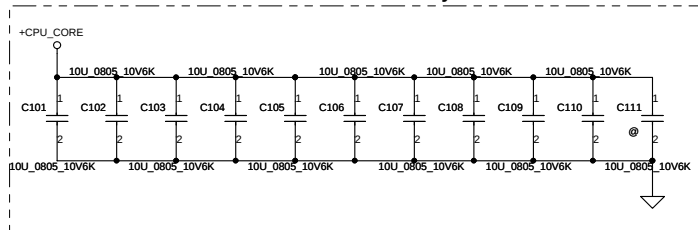
Bottom Socket Cavity x 5



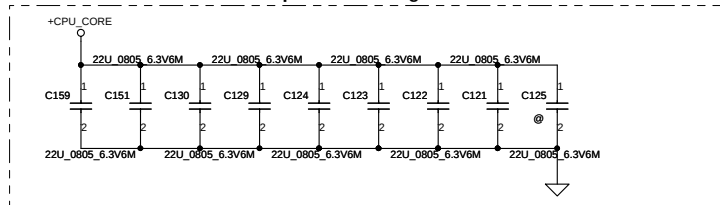
+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U

+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U

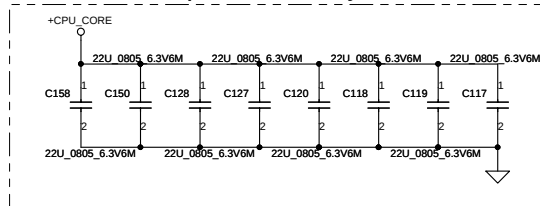
Bottom Socket Cavity



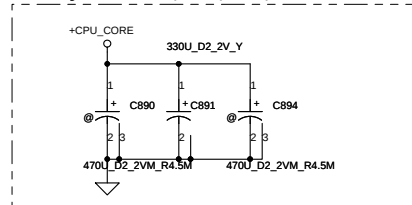
Top Socket Edge



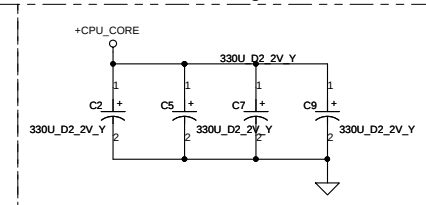
Top Socket Cavity



Co-Lay with C2, C5, C7, C9



TOP Socket Edge



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				Custom	4019BD	B
				Date:	Monday, February 28, 2011	Sheet 8 of 59

ESR 17mohm

1

C873 +

330U_2.5V_M_R17

SENSE
/ TNES

DDR3 -1.5V RATS

A RATIO

MTSC

GRAPHICS

1.2A
VCCPLL1
VCCPLL2
VCCPLL3

Sandy Bridge rPGA Rev0p6

+1.5

Test Down Plan

ESR 17mohm

+VCCSA

1

+

@

2

C877

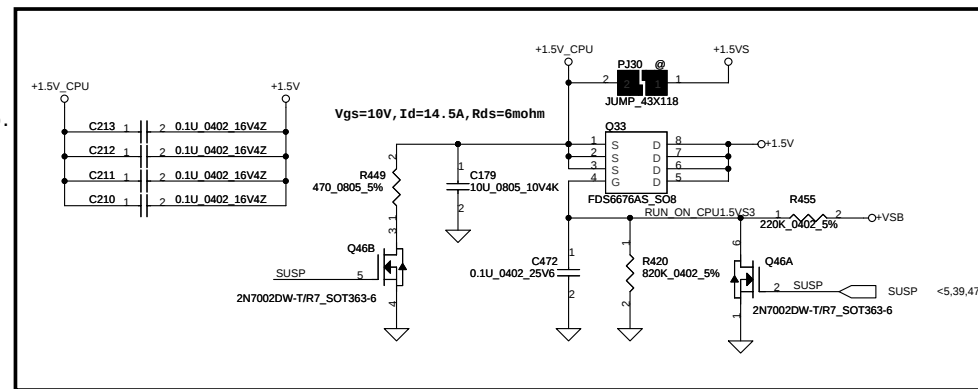
330U_2.5V_M_R17

```
graph TD
    VCCSA[+VCCSA] --- 1[1]
    1 --- P1[+]
    P1 --- AT[@]
    AT --- 2[2]
    2 --- C877[C877]
    C877 --- R17[330U_2.5V_M_R17]
    R17 --- GND[Ground]
```

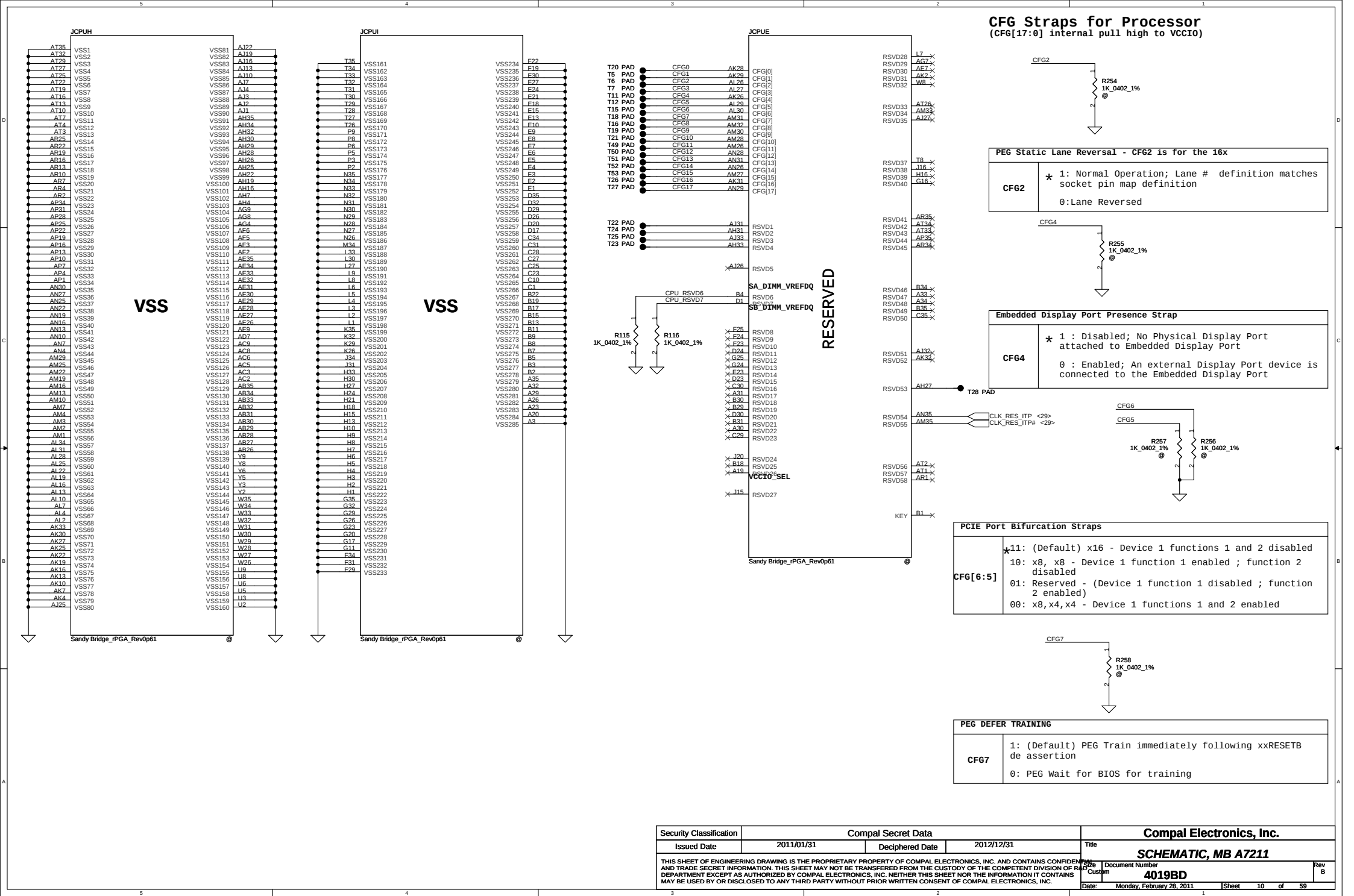
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

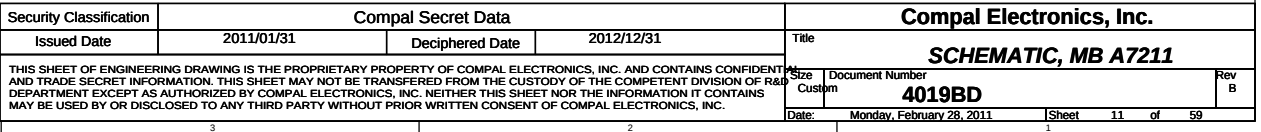
For Sandy Bridge

Reserve it to
follow CRB 1.0

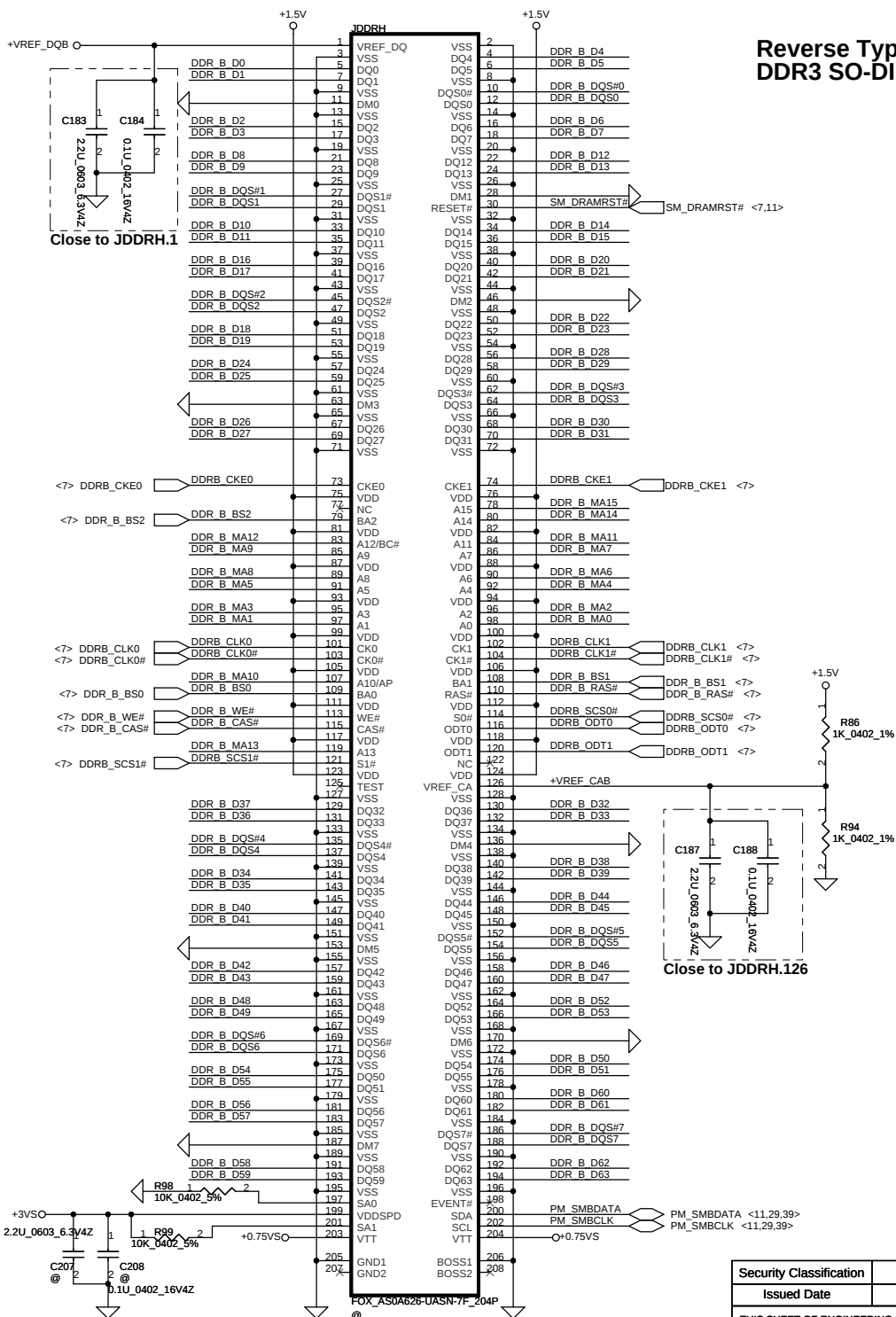


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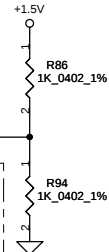
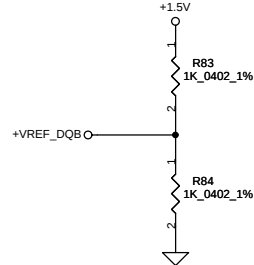




Reverse Type DDR3 SO-DIMM B



DDR_B_DQS#[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_D#[0..63] <7>
DDR_B_MA#[0..15] <7>

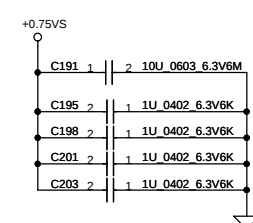
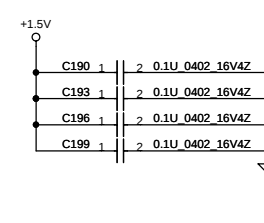
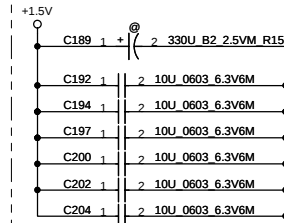


Close to JDDR.H.126

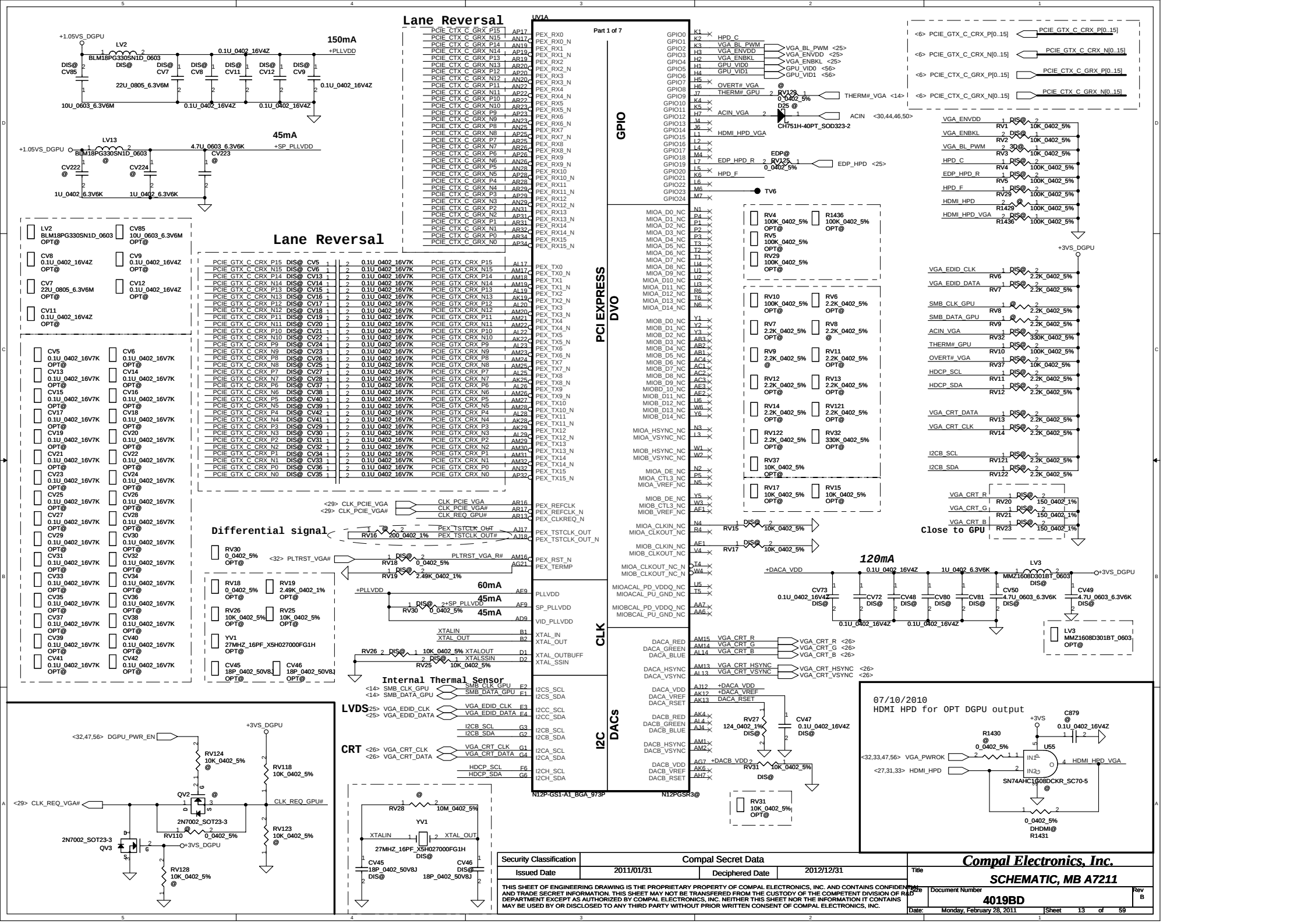
Layout Note:
Place near JDDR.H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMM B

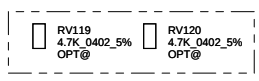
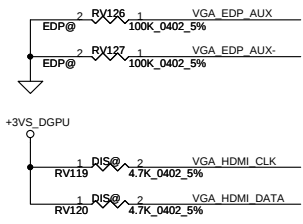
Layout Note:
Place near JDDR.H.203 and 204



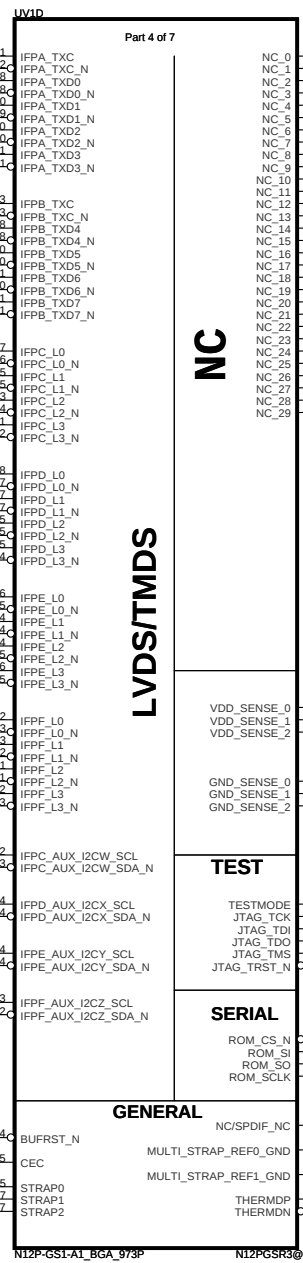
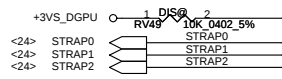
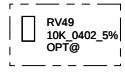
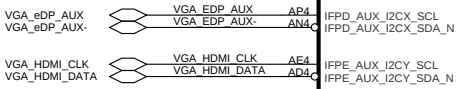
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	
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				4019BD	
				Date: Monday, February 28, 2011	Sheet 12 of 59



EDP is supported
only on IFPD



EDP
HDMI



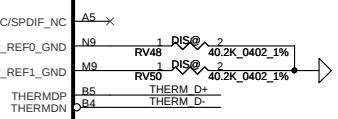
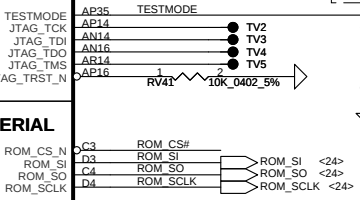
NC

LVDS/TMDS

TEST

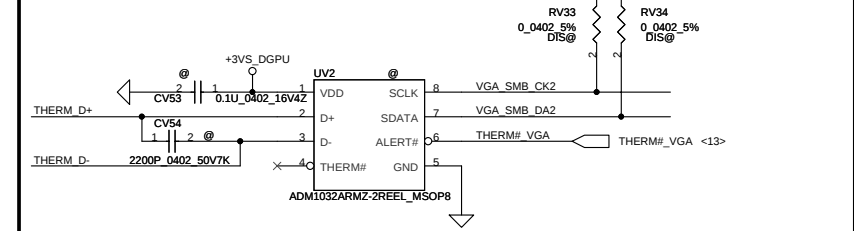
SERIAL

GENERAL



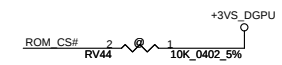
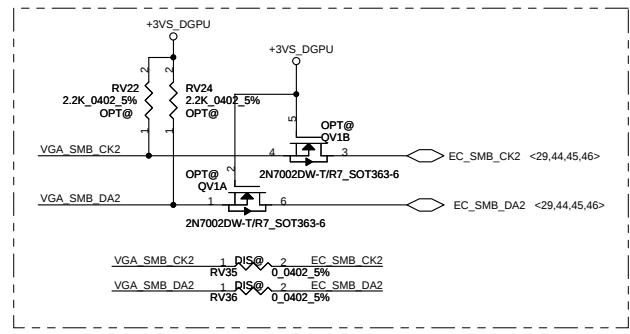
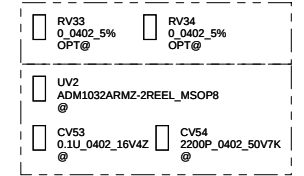
External VGA Thermal Sensor

Address: 0x9A H



Internal Thermal Sensor

Address: 0x9E H, 0x9A H



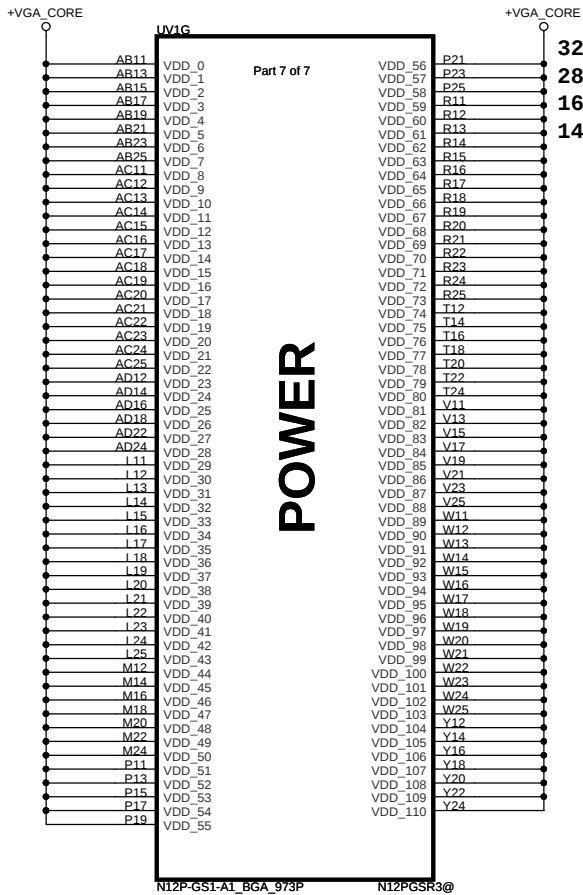
Security Classification		Compal Secret Data		Title	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Document Number	Rev B
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Date: Monday, February 28, 2011		Sheet 14 of 59			

For PHQAA EVT Phase only			
Mode	VID1	VID0	+VGA_CORE
P0(Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

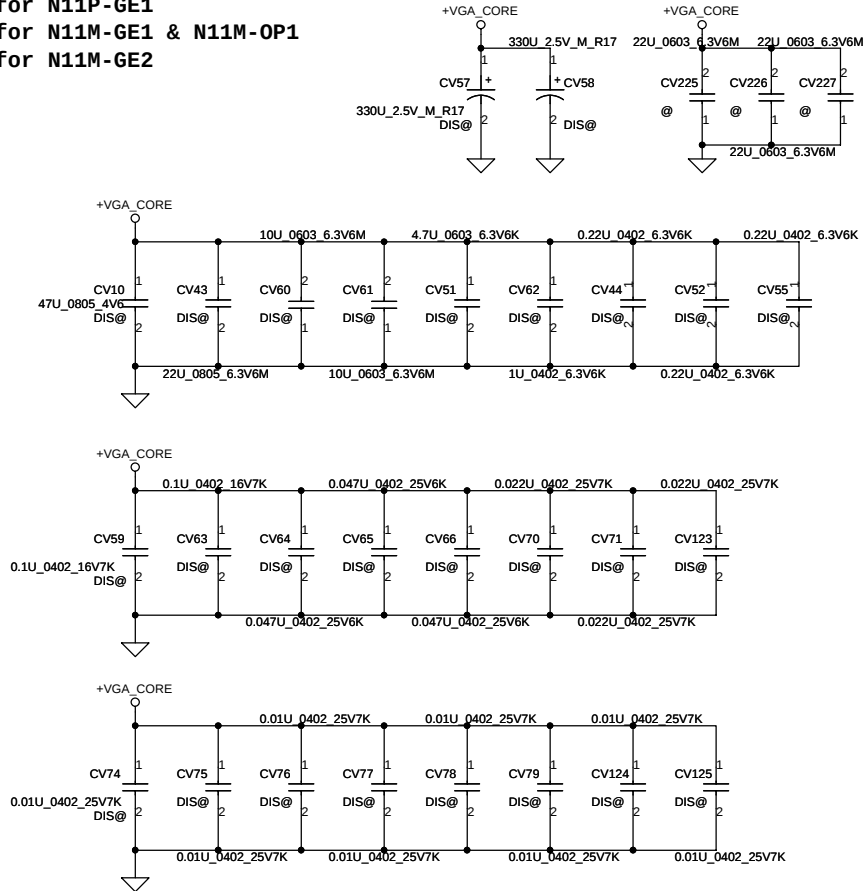
N12M-GE Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GS Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GE Performance Mode			
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

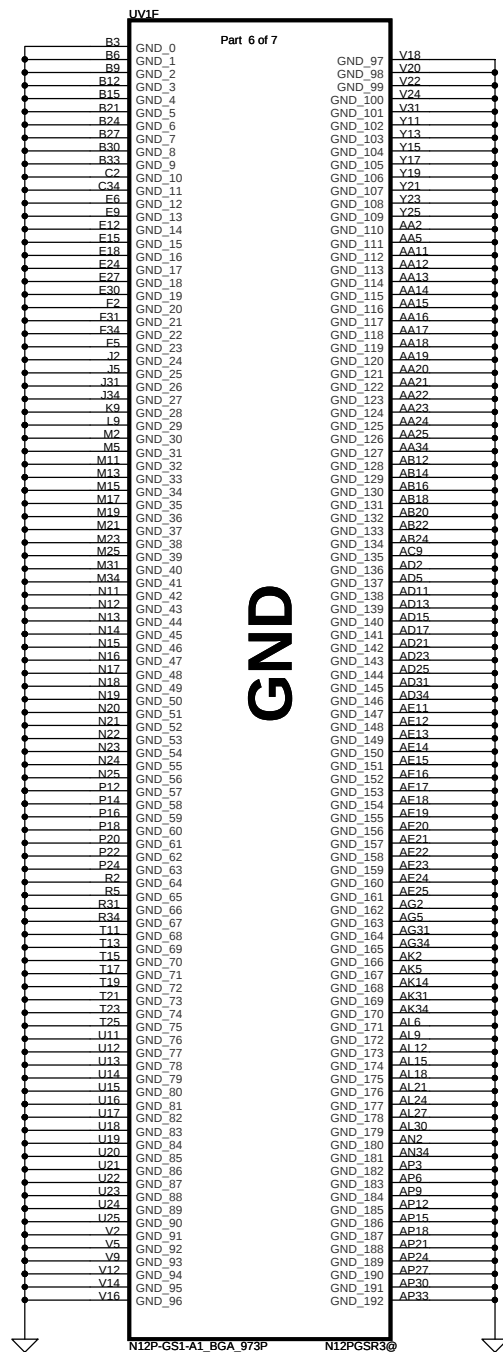


32A for N11E-GE1-LP
28A for N11P-GE1
16A for N11M-GE1 & N11M-OP1
14A for N11M-GE2



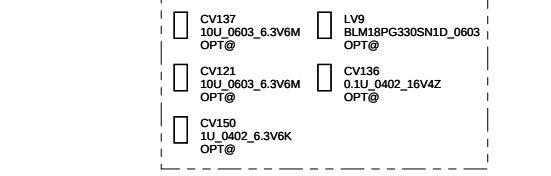
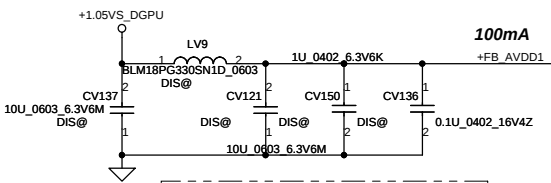
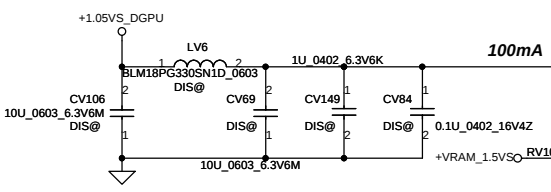
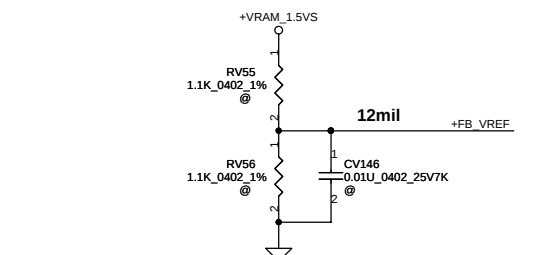
CV225 22U_0603_6.3V6M @	CV226 22U_0603_6.3V6M @	CV227 22U_0603_6.3V6M @
CV57 330U_2.5V_M_R17 OPT@	CV58 330U_2.5V_M_R17 OPT@	CV43 22U_0805_6.3V6M OPT@
CV10 47U_0805_4V6 OPT@	CV60 10U_0603_6.3V6M OPT@	CV61 10U_0603_6.3V6M OPT@
CV51 4.7U_0603_6.3V6K OPT@	CV62 1U_0402_6.3V6K OPT@	CV52 0.22U_0402_6.3V6K OPT@
CV44 0.22U_0402_6.3V6K OPT@	CV55 0.22U_0402_6.3V6K OPT@	CV59 0.1U_0402_16V7K OPT@
CV63 0.1U_0402_16V7K OPT@	CV64 0.047U_0402_25V6K OPT@	CV66 0.047U_0402_25V6K OPT@
CV70 0.022U_0402_25V7K OPT@	CV71 0.022U_0402_25V7K OPT@	CV123 0.022U_0402_25V7K OPT@
CV75 0.01U_0402_25V7K OPT@	CV76 0.01U_0402_25V7K OPT@	CV77 0.01U_0402_25V7K OPT@
CV79 0.01U_0402_25V7K OPT@	CV124 0.01U_0402_25V7K OPT@	CV125 0.01U_0402_25V7K OPT@

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									4019BD	B	
								Date:	Monday, February 28, 2011	Sheet	15 of 59



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					4019BD
				Date:	Monday, February 28, 2011
				Sheet	17 of 59

<20,21> MDA[0..63] ← MDA[0..63]



MDA0	L32	FBA_D0
MDA1	N33	FBA_D1
MDA2	L33	FBA_D2
MDA3	N34	FBA_D3
MDA4	N35	FBA_D4
MDA5	P35	FBA_D5
MDA6	P33	FBA_D6
MDA7	P34	FBA_D7
MDA8	K35	FBA_D8
MDA9	K34	FBA_D9
MDA10	H33	FBA_D10
MDA11	H34	FBA_D11
MDA12	G34	FBA_D12
MDA13	G33	FBA_D13
MDA14	F34	FBA_D14
MDA15	F33	FBA_D15
MDA16	G31	FBA_D16
MDA17	F30	FBA_D17
MDA18	G30	FBA_D18
MDA19	G32	FBA_D19
MDA20	K30	FBA_D20
MDA21	K32	FBA_D21
MDA22	H30	FBA_D22
MDA23	K31	FBA_D23
MDA24	L31	FBA_D24
MDA25	L30	FBA_D25
MDA26	M32	FBA_D26
MDA27	M30	FBA_D27
MDA28	M31	FBA_D28
MDA29	P31	FBA_D29
MDA30	R32	FBA_D30
MDA31	R30	FBA_D31
MDA32	AG30	FBA_D32
MDA33	AG32	FBA_D33
MDA34	AE31	FBA_D34
MDA35	AE31	FBA_D35
MDA36	AE30	FBA_D36
MDA37	AE30	FBA_D37
MDA38	AC32	FBA_D38
MDA39	AD30	FBA_D39
MDA40	AN33	FBA_D40
MDA41	AL31	FBA_D41
MDA42	AM33	FBA_D42
MDA43	AL33	FBA_D43
MDA44	AK30	FBA_D44
MDA45	AK32	FBA_D45
MDA46	AI30	FBA_D46
MDA47	AH30	FBA_D47
MDA48	AH33	FBA_D48
MDA49	AH35	FBA_D49
MDA50	AI34	FBA_D50
MDA51	AH32	FBA_D51
MDA52	AI33	FBA_D52
MDA53	AI35	FBA_D53
MDA54	AM34	FBA_D54
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MDA56	AE33	FBA_D56
MDA57	AE32	FBA_D57
MDA58	AE34	FBA_D58
MDA59	AE35	FBA_D59
MDA60	AE34	FBA_D60
MDA61	AE33	FBA_D61
MDA62	AB32	FBA_D62
MDA63	AC35	FBA_D63

Part 2 of 7

MEMORY INTERFACE

FBA_CMD0	U30	CMDA0	CMDA0	<20>
FBA_CMD1	U30	CMDA1	CMDA1	<20>
FBA_CMD2	U31	CMDA2	CMDA2	<20>
FBA_CMD3	V32	CMDA3	CMDA3	<20>
FBA_CMD4	T35	CMDA4	CMDA4	<20,21>
FBA_CMD5	W32	CMDA5	CMDA5	<20,21>
FBA_CMD6	W33	CMDA6	CMDA6	<20,21>
FBA_CMD7	W31	CMDA7	CMDA7	<20,21>
FBA_CMD8	W34	CMDA8	CMDA8	<20,21>
FBA_CMD9	U34	CMDA9	CMDA9	<20,21>
FBA_CMD10	U35	CMDA10	CMDA10	<20,21>
FBA_CMD11	U32	CMDA11	CMDA11	<20,21>
FBA_CMD12	T34	CMDA12	CMDA12	<20,21>
FBA_CMD13	T33	CMDA13	CMDA13	<20,21>
FBA_CMD14	W30	CMDA14	CMDA14	<20,21>
FBA_CMD15	AB30	CMDA15	CMDA15	<20,21>
FBA_CMD16	AB30	CMDA16	CMDA16	<21>
FBA_CMD17	AB31	CMDA17	CMDA17	<21>
FBA_CMD18	AB32	CMDA18	CMDA18	<21>
FBA_CMD19	AB33	CMDA19	CMDA19	<21>
FBA_CMD20	Y32	CMDA20	CMDA20	<20,21>
FBA_CMD21	Y33	CMDA21	CMDA21	<20,21>
FBA_CMD22	AB34	CMDA22	CMDA22	<20,21>
FBA_CMD23	AB35	CMDA23	CMDA23	<20,21>
FBA_CMD24	Y35	CMDA24	CMDA24	<20,21>
FBA_CMD25	W35	CMDA25	CMDA25	<20,21>
FBA_CMD26	Y34	CMDA26	CMDA26	<20,21>
FBA_CMD27	Y31	CMDA27	CMDA27	<20,21>
FBA_CMD28	Y30	CMDA28	CMDA28	<20,21>
FBA_CMD29	W29	CMDA29	CMDA29	<20,21>
FBA_CMD30	Y29	CMDA30	CMDA30	<20,21>
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FBA_DQM1	L34	DQMA1	DQMA1	<20,21>
FBA_DQM2	L30	DQMA2	DQMA2	<20,21>
FBA_DQM3	P30	DQMA3	DQMA3	<20,21>
FBA_DQM4	AE32	DQMA4	DQMA4	<20,21>
FBA_DQM5	AI32	DQMA5	DQMA5	<20,21>
FBA_DQM6	AI34	DQMA6	DQMA6	<20,21>
FBA_DQM7	AE35	DQMA7	DQMA7	<20,21>
FBA_DQS_RN0	L35	DQSA#0	DQSA#0	<20,21>
FBA_DQS_RN1	G35	DQSA#1	DQSA#1	<20,21>
FBA_DQS_RN2	H31	DQSA#2	DQSA#2	<20,21>
FBA_DQS_RN3	N32	DQSA#3	DQSA#3	<20,21>
FBA_DQS_RN4	AD32	DQSA#4	DQSA#4	<20,21>
FBA_DQS_RN5	AI31	DQSA#5	DQSA#5	<20,21>
FBA_DQS_RN6	AI35	DQSA#6	DQSA#6	<20,21>
FBA_DQS_RN7	AC34	DQSA#7	DQSA#7	<20,21>
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FBA_DQS_WP2	J32	DQSA2	DQSA2	<20,21>
FBA_DQS_WP3	N31	DQSA3	DQSA3	<20,21>
FBA_DQS_WP4	AE31	DQSA4	DQSA4	<20,21>
FBA_DQS_WP5	AI32	DQSA5	DQSA5	<20,21>
FBA_DQS_WP6	AI34	DQSA6	DQSA6	<20,21>
FBA_DQS_WP7	AC33	DQSA7	DQSA7	<20,21>
FBA_WCK0	P29	WCK0	WCK0	<20,21>
FBA_WCK0_N	P29	WCK0_N	WCK0_N	<20,21>
FBA_WCK1	L29	WCK1	WCK1	<20,21>
FBA_WCK1_N	L29	WCK1_N	WCK1_N	<20,21>
FBA_WCK2	AD29	WCK2	WCK2	<20,21>
FBA_WCK2_N	AD29	WCK2_N	WCK2_N	<20,21>
FBA_WCK3	AE29	WCK3	WCK3	<20,21>
FBA_WCK3_N	AE29	WCK3_N	WCK3_N	<20,21>
FBA_CLK0	T32	CLKA0	CLKA0	<20>
FBA_CLK0_N	T31	CLKA0#	CLKA0#	<20>
FBA_CLK1	AC31	CLKA1	CLKA1	<21>
FBA_CLK1_N	AC30	CLKA1#	CLKA1#	<21>

GB2-128 Mode E - Mirror Mode Mapping

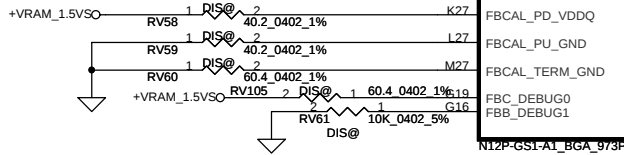
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	A8
CMD8	A8	A8
CMD2	CS0#_L	A6
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

<22,23> MDB[0..63]

RV58
40.2_0402_1%
OPT@

RV59
40.2_0402_1%
OPT@

RV60
60.4_0402_1%
OPT@



RV61
10K_0402_5%
OPT@

RV105
60.4_0402_1%
OPT@

UVIC

Part 3 of 7

MEMORY INTERFACE C

MDB0 B13 FBC_D0
MDB1 D13 FBC_D1
MDB2 A14 FBC_D2
MDB3 C16 FBC_D3
MDB4 C16 FBC_D4
MDB5 B16 FBC_D5
MDB6 A17 FBC_D6
MDB7 D16 FBC_D7
MDB8 C13 FBC_D8
MDB9 B11 FBC_D9
MDB10 A11 FBC_D10
MDB11 A11 FBC_D11
MDB12 C10 FBC_D12
MDB13 C8 FBC_D13
MDB14 B8 FBC_D14
MDB15 A8 FBC_D15
MDB16 F8 FBC_D16
MDB17 F8 FBC_D17
MDB18 F10 FBC_D18
MDB19 E9 FBC_D19
MDB20 F12 FBC_D20
MDB21 D8 FBC_D21
MDB22 D11 FBC_D22
MDB23 F11 FBC_D23
MDB24 D12 FBC_D24
MDB25 E13 FBC_D25
MDB26 B13 FBC_D26
MDB27 F14 FBC_D27
MDB28 F15 FBC_D28
MDB29 F16 FBC_D29
MDB30 F16 FBC_D30
MDB31 F17 FBC_D31
MDB32 D29 FBC_D32
MDB33 F27 FBC_D33
MDB34 F28 FBC_D34
MDB35 E28 FBC_D35
MDB36 D26 FBC_D36
MDB37 E25 FBC_D37
MDB38 D24 FBC_D38
MDB39 E25 FBC_D39
MDB40 E32 FBC_D40
MDB41 F32 FBC_D41
MDB42 D33 FBC_D42
MDB43 F31 FBC_D43
MDB44 C33 FBC_D44
MDB45 F29 FBC_D45
MDB46 D30 FBC_D46
MDB47 F29 FBC_D47
MDB48 B29 FBC_D48
MDB49 C31 FBC_D49
MDB50 C29 FBC_D50
MDB51 B31 FBC_D51
MDB52 C32 FBC_D52
MDB53 B32 FBC_D53
MDB54 B35 FBC_D54
MDB55 B34 FBC_D55
MDB56 A29 FBC_D56
MDB57 B28 FBC_D57
MDB58 A28 FBC_D58
MDB59 C28 FBC_D59
MDB60 C26 FBC_D60
MDB61 D25 FBC_D61
MDB62 B25 FBC_D62
MDB63 A25 FBC_D63

FBC_CMD0 F18 CMDB0 > CMDB0 <22>
FBC_CMD1 F19 CMDB2 > CMDB2 <22>
FBC_CMD2 D18 CMDB3 > CMDB3 <22>
FBC_CMD3 C17 CMDB4 > CMDB4 <22,23>
FBC_CMD4 C19 CMDB5 > CMDB5 <22,23>
FBC_CMD5 B17 CMDB6 > CMDB6 <22,23>
FBC_CMD6 E20 CMDB7 > CMDB7 <22,23>
FBC_CMD7 B19 CMDB8 > CMDB8 <22,23>
FBC_CMD8 D20 CMDB9 > CMDB9 <22,23>
FBC_CMD9 A19 CMDB10 > CMDB10 <22,23>
FBC_CMD10 C20 CMDB11 > CMDB11 <22,23>
FBC_CMD11 F20 CMDB12 > CMDB12 <22,23>
FBC_CMD12 B20 CMDB13 > CMDB13 <22,23>
FBC_CMD13 G21 CMDB14 > CMDB14 <22,23>
FBC_CMD14 E22 CMDB15 > CMDB15 <22,23>
FBC_CMD15 F24 CMDB16 > CMDB16 <23>
FBC_CMD16 E23 CMDB18 > CMDB18 <23>
FBC_CMD17 C25 CMDB19 > CMDB19 <23>
FBC_CMD18 F21 CMDB20 > CMDB20 <22,23>
FBC_CMD19 E22 CMDB21 > CMDB21 <22,23>
FBC_CMD20 D21 CMDB22 > CMDB22 <22,23>
FBC_CMD21 A23 CMDB23 > CMDB23 <22,23>
FBC_CMD22 D22 CMDB24 > CMDB24 <22,23>
FBC_CMD23 B23 CMDB25 > CMDB25 <22,23>
FBC_CMD24 C22 CMDB26 > CMDB26 <22,23>
FBC_CMD25 B22 CMDB27 > CMDB27 <22,23>
FBC_CMD26 A22 CMDB28 > CMDB28 <22,23>
FBC_CMD27 A20 CMDB29 > CMDB29 <22,23>
FBC_CMD28 G20 CMDB30 > CMDB30 <22,23>
FBC_CMD29 D10 DQMB0
FBC_CMD30 F11 DQMB1
FBC_CMD31 D15 DQMB2
FBC_CMD32 D15 DQMB3
FBC_CMD33 D27 DQMB4
FBC_CMD34 D34 DQMB5
FBC_CMD35 A34 DQMB6
FBC_CMD36 D28 DQMB7

FBC_CMD37 B14 DQSB#0
FBC_CMD38 D10 DQSB#1
FBC_CMD39 D11 DQSB#2
FBC_CMD40 E14 DQSB#3
FBC_CMD41 E26 DQSB#4
FBC_CMD42 D31 DQSB#5
FBC_CMD43 A31 DQSB#6
FBC_CMD44 A26 DQSB#7

FBC_CMD45 C14 DQSB0
FBC_CMD46 A10 DQSB1
FBC_CMD47 E10 DQSB2
FBC_CMD48 D14 DQSB3
FBC_CMD49 E26 DQSB4
FBC_CMD50 D32 DQSB5
FBC_CMD51 A32 DQSB6
FBC_CMD52 B26 DQSB7

FBC_CMD53 G14
FBC_CMD54 G15
FBC_CMD55 G11
FBC_CMD56 G12
FBC_CMD57 G27
FBC_CMD58 G28
FBC_CMD59 G24
FBC_CMD60 G25

FBC_CMD61 FBC_WCK0
FBC_CMD62 FBC_WCK1
FBC_CMD63 FBC_WCK1_N
FBC_CMD64 FBC_WCK2
FBC_CMD65 FBC_WCK2_N
FBC_CMD66 FBC_WCK3
FBC_CMD67 FBC_WCK3_N

FBC_CMD68 FBC_CLK0
FBC_CMD69 FBC_CLK0_N
FBC_CMD70 FBC_CLK1
FBC_CMD71 FBC_CLK1_N

DQMB[7..0] <22,23>

DQSB[7..0] <22,23>

DQSB[7..0] <22,23>

CLKB0 <22>

CLKB0# <22>

CLKB1 <23>

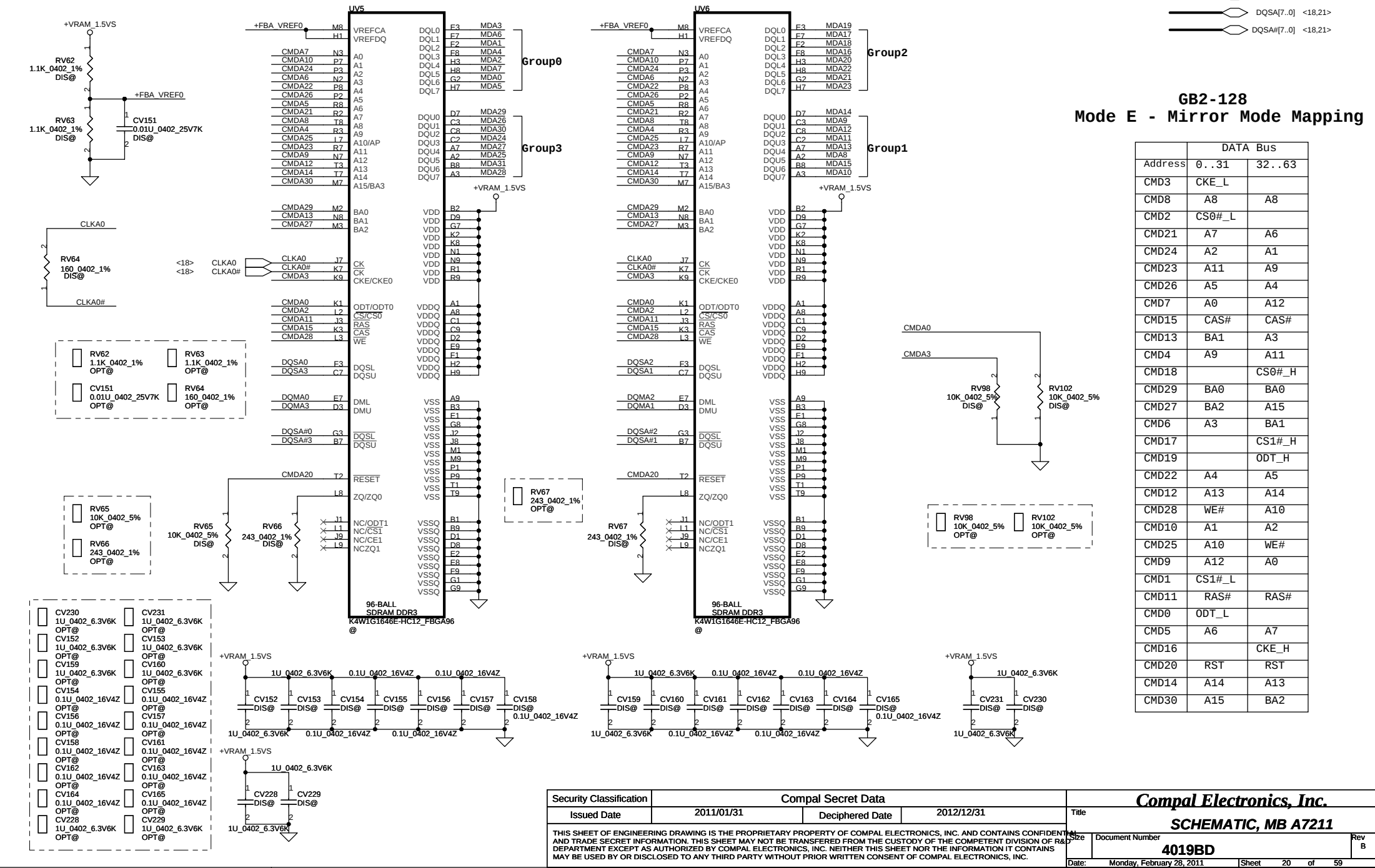
CLKB1# <23>

GB2-128 Mode E - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

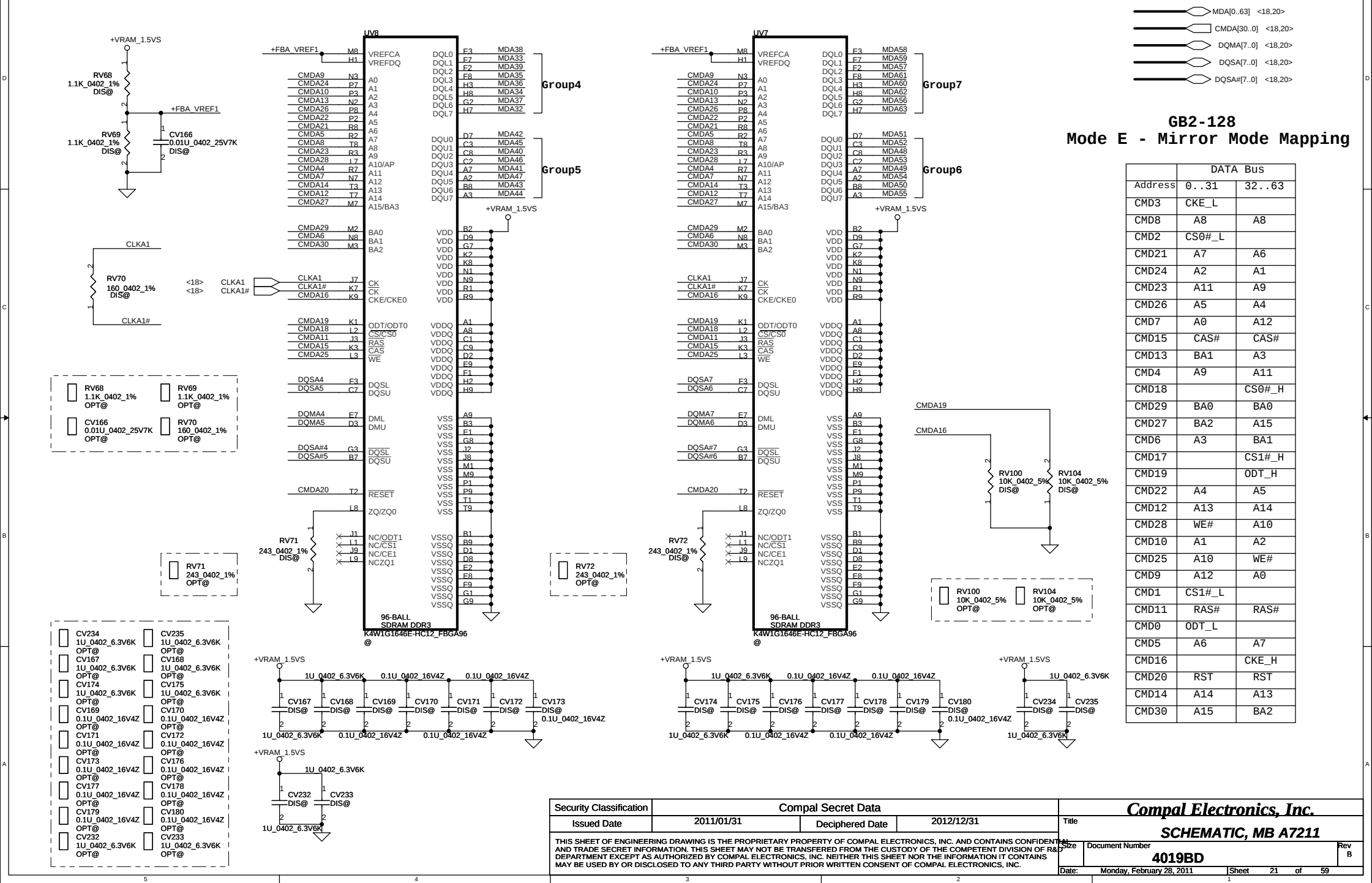
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/01/31	Deciphered Date	2012/12/31	Title	SCHEMATIC, MB A7211
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	4019BD
				Date:	Monday, February 28, 2011
				Sheet	19 of 59

Memory Partition A - Lower 32 bits

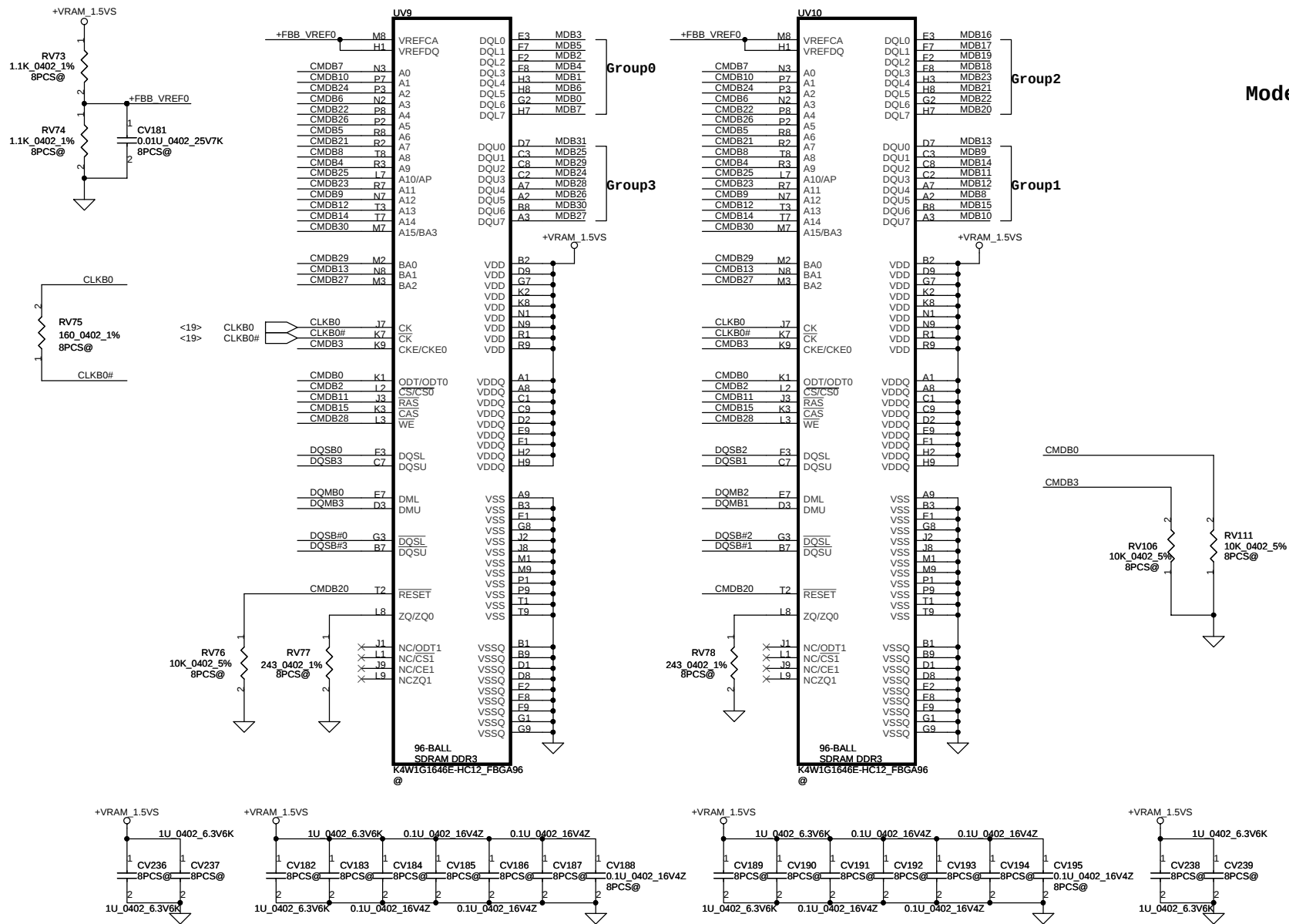


DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
CMD11	RAS#
CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15
	BA2

Memory Partition A - Upper 32 bits



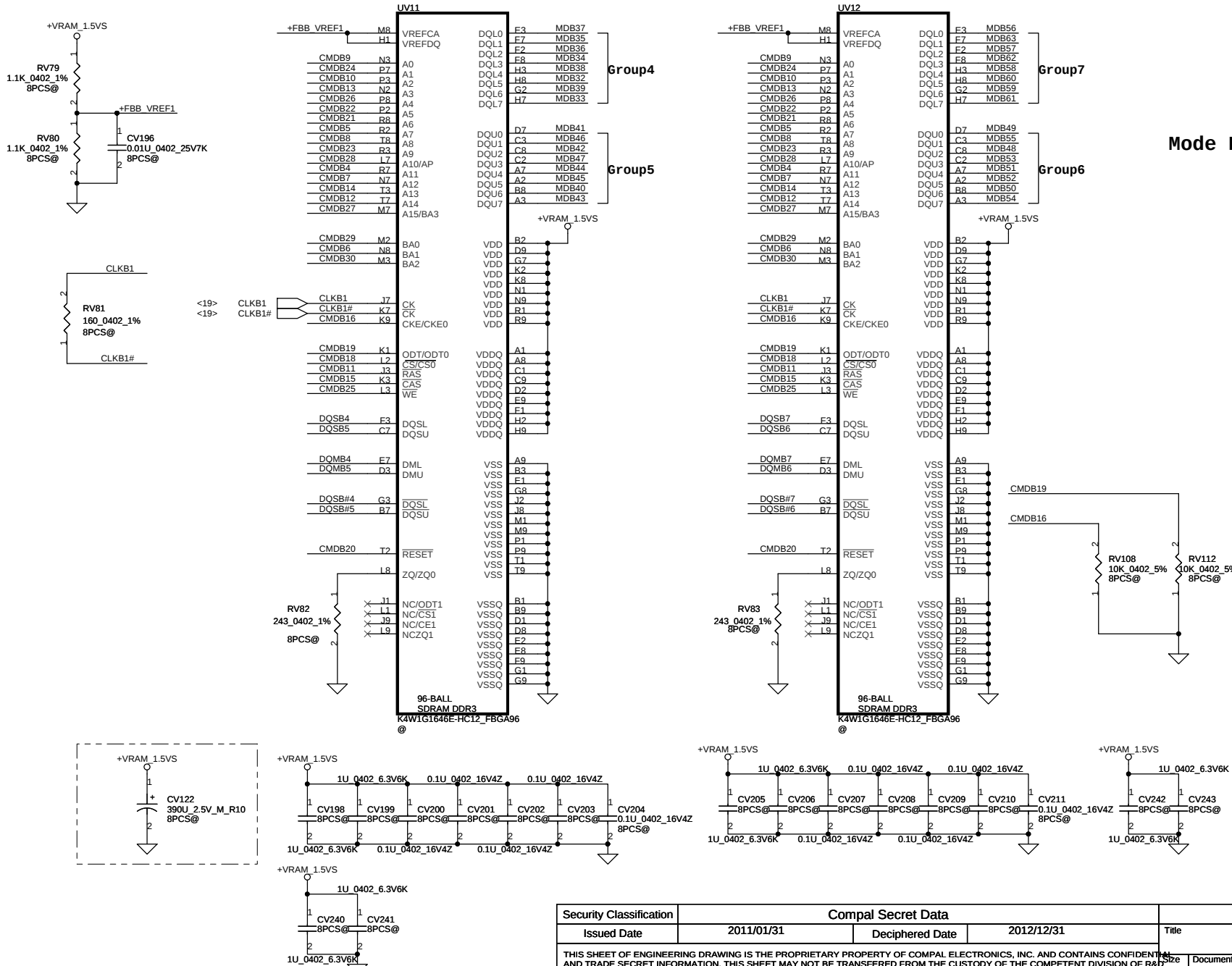
Memory Partition C - Lower 32 bits



GB2-128
Mode E - Mirror Mode Mapping

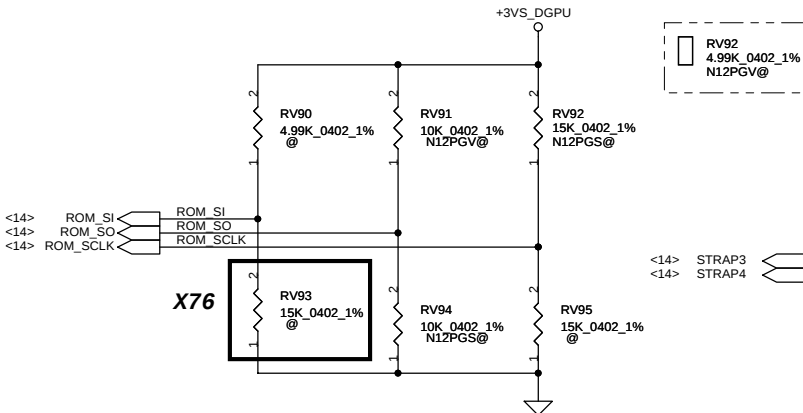
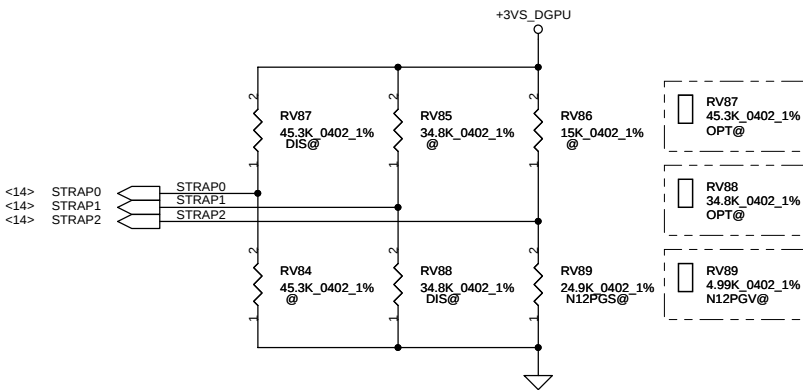
DATA Bus		
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits



GB2-128
Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

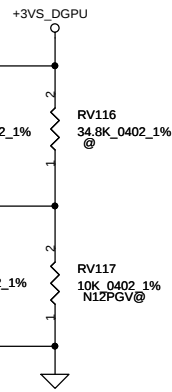


Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_S0	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

GPU	DDR3 Type	VRAM		RAMCFG[3..0]		RV93
N12P-GS	64M16 900MHZ	Hynix H5TQ1G63DFR-11C	512MB	0010	PD 15K	SD034154280
		SA000041S20	1GB	0010	PD 15K	SD034154280
		Samsung K4W1G1646E-HC11	512MB	0011	PD 20K	SD034200280
		SA000041T00	1GB	0011	PD 20K	SD034200280
	128M16 900MHZ	Hynix H5TQ2G63BFR-11C	1GB	0110	PD 34.8K	SD034348280
		SA00003YO00	2GB	0110	PD 34.8K	SD034348280
		Samsung K4W2G1646C-HC11	1GB	0111	PD 45.3K	SD034453280
		SA000047Q00	2GB	0111	PD 45.3K	SD034453280
N12P-GV	64M16 800MHZ	Hynix H5TQ1G63DFR-12C	512MB	0010	PD 15K	SD034154280
		SA0000324C0				
		Samsung K4W1G1646G-BC12	512MB	0011	PD 20K	SD034200280
		SA00004HS00				
	128M16 800MHZ	Hynix H5TQ2G63BFR-12C	1GB	0110	PD 34.8K	SD034348280
		SA00003VS00				
	Samsung K4W2G1646C-HC12	1GB	0111	PD 45.3K	SD034453280	



SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

OPTIMUS

Close to LVDS Connector

DISCRETE

W=20mils

Pin 1 USB20 P11 R

Pin 2 USB20 N11 R

Pin 3 LVDS_TXOUT0+

Pin 4 LVDS_TXOUT0-

Pin 5 LVDS_TXOUT1+

Pin 6 LVDS_TXOUT1-

Pin 7 LVDS_TXOUT2+

Pin 8 LVDS_TXOUT2-

Pin 9 LVDS_TXCLK+

Pin 10 LVDS_TXCLK-

Pin 11 LVDS_EDID_CLK

Pin 12 LVDS_EDID_DATA

Pin 13 LVDS_TXOUT0+

Pin 14 LVDS_TXOUT0-

Pin 15 LVDS_TXOUT1+

Pin 16 LVDS_TXOUT1-

Pin 17 LVDS_TXOUT2+

Pin 18 LVDS_TXOUT2-

Pin 19 LVDS_TXCLK+

Pin 20 LVDS_TXCLK-

Pin 21 LVDS_EDID_CLK

Pin 22 LVDS_EDID_DATA

Pin 23 LVDS_TXOUT0+

Pin 24 LVDS_TXOUT0-

Pin 25 LVDS_TXOUT1+

Pin 26 LVDS_TXOUT1-

Pin 27 LVDS_TXOUT2+

Pin 28 LVDS_TXOUT2-

Pin 29 LVDS_TXCLK+

Pin 30 LVDS_TXCLK-

Pin 31 LVDS_EDID_CLK

Pin 32 LVDS_EDID_DATA

Pin 33 LVDS_TXOUT0+

Pin 34 LVDS_TXOUT0-

Pin 35 LVDS_TXOUT1+

Pin 36 LVDS_TXOUT1-

Pin 37 LVDS_TXOUT2+

Pin 38 LVDS_TXOUT2-

Pin 39 LVDS_TXCLK+

Pin 40 LVDS_TXCLK-

Pin 41 LVDS_EDID_CLK

Pin 42 LVDS_EDID_DATA

Pin 43 LVDS_TXOUT0+

Pin 44 LVDS_TXOUT0-

Pin 45 LVDS_TXOUT1+

Pin 46 LVDS_TXOUT1-

Pin 47 LVDS_TXOUT2+

Pin 48 LVDS_TXOUT2-

Pin 49 LVDS_TXCLK+

Pin 50 LVDS_TXCLK-

Pin 51 LVDS_EDID_CLK

Pin 52 LVDS_EDID_DATA

Pin 53 LVDS_TXOUT0+

Pin 54 LVDS_TXOUT0-

Pin 55 LVDS_TXOUT1+

Pin 56 LVDS_TXOUT1-

Pin 57 LVDS_TXOUT2+

Pin 58 LVDS_TXOUT2-

Pin 59 LVDS_TXCLK+

Pin 60 LVDS_TXCLK-

Pin 61 LVDS_EDID_CLK

Pin 62 LVDS_EDID_DATA

Pin 63 LVDS_TXOUT0+

Pin 64 LVDS_TXOUT0-

Pin 65 LVDS_TXOUT1+

Pin 66 LVDS_TXOUT1-

Pin 67 LVDS_TXOUT2+

Pin 68 LVDS_TXOUT2-

Pin 69 LVDS_TXCLK+

Pin 70 LVDS_TXCLK-

Pin 71 LVDS_EDID_CLK

Pin 72 LVDS_EDID_DATA

Pin 73 LVDS_TXOUT0+

Pin 74 LVDS_TXOUT0-

Pin 75 LVDS_TXOUT1+

Pin 76 LVDS_TXOUT1-

Pin 77 LVDS_TXOUT2+

Pin 78 LVDS_TXOUT2-

Pin 79 LVDS_TXCLK+

Pin 80 LVDS_TXCLK-

Pin 81 LVDS_EDID_CLK

Pin 82 LVDS_EDID_DATA

Pin 83 LVDS_TXOUT0+

Pin 84 LVDS_TXOUT0-

Pin 85 LVDS_TXOUT1+

Pin 86 LVDS_TXOUT1-

Pin 87 LVDS_TXOUT2+

Pin 88 LVDS_TXOUT2-

Pin 89 LVDS_TXCLK+

Pin 90 LVDS_TXCLK-

Pin 91 LVDS_EDID_CLK

Pin 92 LVDS_EDID_DATA

Pin 93 LVDS_TXOUT0+

Pin 94 LVDS_TXOUT0-

Pin 95 LVDS_TXOUT1+

Pin 96 LVDS_TXOUT1-

Pin 97 LVDS_TXOUT2+

Pin 98 LVDS_TXOUT2-

Pin 99 LVDS_TXCLK+

Pin 100 LVDS_TXCLK-

Pin 101 LVDS_EDID_CLK

Pin 102 LVDS_EDID_DATA

Pin 103 LVDS_TXOUT0+

Pin 104 LVDS_TXOUT0-

Pin 105 LVDS_TXOUT1+

Pin 106 LVDS_TXOUT1-

Pin 107 LVDS_TXOUT2+

Pin 108 LVDS_TXOUT2-

Pin 109 LVDS_TXCLK+

Pin 110 LVDS_TXCLK-

Pin 111 LVDS_EDID_CLK

Pin 112 LVDS_EDID_DATA

Pin 113 LVDS_TXOUT0+

Pin 114 LVDS_TXOUT0-

Pin 115 LVDS_TXOUT1+

Pin 116 LVDS_TXOUT1-

Pin 117 LVDS_TXOUT2+

Pin 118 LVDS_TXOUT2-

Pin 119 LVDS_TXCLK+

Pin 120 LVDS_TXCLK-

Pin 121 LVDS_EDID_CLK

Pin 122 LVDS_EDID_DATA

Pin 123 LVDS_TXOUT0+

Pin 124 LVDS_TXOUT0-

Pin 125 LVDS_TXOUT1+

Pin 126 LVDS_TXOUT1-

Pin 127 LVDS_TXOUT2+

Pin 128 LVDS_TXOUT2-

Pin 129 LVDS_TXCLK+

Pin 130 LVDS_TXCLK-

Pin 131 LVDS_EDID_CLK

Pin 132 LVDS_EDID_DATA

Pin 133 LVDS_TXOUT0+

Pin 134 LVDS_TXOUT0-

Pin 135 LVDS_TXOUT1+

Pin 136 LVDS_TXOUT1-

Pin 137 LVDS_TXOUT2+

Pin 138 LVDS_TXOUT2-

Pin 139 LVDS_TXCLK+

Pin 140 LVDS_TXCLK-

Pin 141 LVDS_EDID_CLK

Pin 142 LVDS_EDID_DATA

Pin 143 LVDS_TXOUT0+

Pin 144 LVDS_TXOUT0-

Pin 145 LVDS_TXOUT1+

Pin 146 LVDS_TXOUT1-

Pin 147 LVDS_TXOUT2+

Pin 148 LVDS_TXOUT2-

Pin 149 LVDS_TXCLK+

Pin 150 LVDS_TXCLK-

Pin 151 LVDS_EDID_CLK

Pin 152 LVDS_EDID_DATA

Pin 153 LVDS_TXOUT0+

Pin 154 LVDS_TXOUT0-

Pin 155 LVDS_TXOUT1+

Pin 156 LVDS_TXOUT1-

Pin 157 LVDS_TXOUT2+

Pin 158 LVDS_TXOUT2-

Pin 159 LVDS_TXCLK+

Pin 160 LVDS_TXCLK-

Pin 161 LVDS_EDID_CLK

Pin 162 LVDS_EDID_DATA

Pin 163 LVDS_TXOUT0+

Pin 164 LVDS_TXOUT0-

Pin 165 LVDS_TXOUT1+

Pin 166 LVDS_TXOUT1-

Pin 167 LVDS_TXOUT2+

Pin 168 LVDS_TXOUT2-

Pin 169 LVDS_TXCLK+

Pin 170 LVDS_TXCLK-

Pin 171 LVDS_EDID_CLK

Pin 172 LVDS_EDID_DATA

Pin 173 LVDS_TXOUT0+

Pin 174 LVDS_TXOUT0-

Pin 175 LVDS_TXOUT1+

Pin 176 LVDS_TXOUT1-

Pin 177 LVDS_TXOUT2+

Pin 178 LVDS_TXOUT2-

Pin 179 LVDS_TXCLK+

Pin 180 LVDS_TXCLK-

Pin 181 LVDS_EDID_CLK

Pin 182 LVDS_EDID_DATA

Pin 183 LVDS_TXOUT0+

Pin 184 LVDS_TXOUT0-

Pin 185 LVDS_TXOUT1+

Pin 186 LVDS_TXOUT1-

Pin 187 LVDS_TXOUT2+

Pin 188 LVDS_TXOUT2-

Pin 189 LVDS_TXCLK+

Pin 190 LVDS_TXCLK-

Pin 191 LVDS_EDID_CLK

Pin 192 LVDS_EDID_DATA

Pin 193 LVDS_TXOUT0+

Pin 194 LVDS_TXOUT0-

Close to LVDS Connector

DISCRETE for Dual Chancel Panel

Signal	Pin	Signal	Pin
<14> VGA_TZOUT0+	R500	LVDS_TZOUT0+	1
<14> VGA_TZOUT0-	R501	LVDS_TZOUT0-	2
<14> VGA_TZOUT1+	R502	LVDS_TZOUT1+	3
<14> VGA_TZOUT1-	R503	LVDS_TZOUT1-	4
<14> VGA_TZOUT2+	R504	LVDS_TZOUT2+	5
<14> VGA_TZOUT2-	R505	LVDS_TZOUT2-	6
<14> VGA_TZCLK+	R507	LVDS_TZCLK+	7
<14> VGA_TZCLK-	R508	LVDS_TZCLK-	8

Reserve f

<32> USB20_N11

<32> USB20_P11

R78
L55
WCM-20
R96

Pin	Module Pin	Signal
<14>	R500	VGA_TZOUT0+
<14>	R501	VGA_TZOUT0-
<14>	R502	VGA_TZOUT1+
<14>	R503	VGA_TZOUT1-
<14>	R504	VGA_TZOUT2+
<14>	R505	VGA_TZOUT2-
<14>	R507	VGA_TZCLK+
<14>	R508	VGA_TZCLK-

Figure 10 shows the USB20 pin connections. The left side is a table mapping module pins to signals. The right side is a schematic diagram of the USB20 module with pins R500 through R508 connected to the module's pins. The module pins are labeled: R500, R501, R502, R503, R504, R505, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569, R570, R571, R572, R573, R574, R575, R576, R577, R578, R579, R580, R581, R582, R583, R584, R585, R586, R587, R588, R589, R590, R591, R592, R593, R594, R595, R596, R597, R598, R599, R600, R601, R602, R603, R604, R605, R606, R607, R608, R609, R610, R611, R612, R613, R614, R615, R616, R617, R618, R619, R620, R621, R622, R623, R624, R625, R626, R627, R628, R629, R630, R631, R632, R633, R634, R635, R636, R637, R638, R639, R640, R641, R642, R643, R644, R645, R646, R647, R648, R649, R650, R651, R652, R653, R654, R655, R656, R657, R658, R659, R660, R661, R662, R663, R664, R665, R666, R667, R668, R669, R670, R671, R672, R673, R674, R675, R676, R677, R678, R679, R680, R681, R682, R683, R684, R685, R686, R687, R688, R689, R690, R691, R692, R693, R694, R695, R696, R697, R698, R699, R700, R701, R702, R703, R704, R705, R706, R707, R708, R709, R710, R711, R712, R713, R714, R715, R716, R717, R718, R719, R720, R721, R722, R723, R724, R725, R726, R727, R728, R729, R730, R731, R732, R733, R734, R735, R736, R737, R738, R739, R740, R741, R742, R743, R744, R745, R746, R747, R748, R749, R750, R751, R752, R753, R754, R755, R756, R757, R758, R759, R760, R761, R762, R763, R764, R765, R766, R767, R768, R769, R770, R771, R772, R773, R774, R775, R776, R777, R778, R779, R780, R781, R782, R783, R784, R785, R786, R787, R788, R789, R790, R791, R792, R793, R794, R795, R796, R797, R798, R799, R800, R801, R802, R803, R804, R805, R806, R807, R808, R809, R810, R811, R812, R813, R814, R815, R816, R817, R818, R819, R820, R821, R822, R823, R824, R825, R826, R827, R828, R829, R830, R831, R832, R833, R834, R835, R836, R837, R838, R839, R840, R841, R842, R843, R844, R845, R846, R847, R848, R849, R850, R851, R852, R853, R854, R855, R856, R857, R858, R859, R860, R861, R862, R863, R864, R865, R866, R867, R868, R869, R870, R871, R872, R873, R874, R875, R876, R877, R878, R879, R880, R881, R882, R883, R884, R885, R886, R887, R888, R889, R890, R891, R892, R893, R894, R895, R896, R897, R898, R899, R900, R901, R902, R903, R904, R905, R906, R907, R908, R909, R910, R911, R912, R913, R914, R915, R916, R917, R918, R919, R920, R921, R922, R923, R924, R925, R926, R927, R928, R929, R930, R931, R932, R933, R934, R935, R936, R937, R938, R939, R940, R941, R942, R943, R944, R945, R946, R947, R948, R949, R950, R951, R952, R953, R954, R955, R956, R957, R958, R959, R960, R961, R962, R963, R964, R965, R966, R967, R968, R969, R970, R971, R972, R973, R974, R975, R976, R977, R978, R979, R980, R981, R982, R983, R984, R985, R986, R987, R988, R989, R990, R991, R992, R993, R994, R995, R996, R997, R998, R999, R1000, R1001, R1002, R1003, R1004, R1005, R1006, R1007, R1008, R1009, R1010, R1011, R1012, R1013, R1014, R1015, R1016, R1017, R1018, R1019, R1020, R1021, R1022, R1023, R1024, R1025, R1026, R1027, R1028, R1029, R1030, R1031, R1032, R1033, R1034, R1035, R1036, R1037, R1038, R1039, R1040, R1041, R1042, R1043, R1044, R1045, R1046, R1047, R1048, R1049, R1050, R1051, R1052, R1053, R1054, R1055, R1056, R1057, R1058, R1059, R1060, R1061, R1062, R1063, R1064, R1065, R1066, R1067, R1068, R1069, R1070, R1071, R1072, R1073, R1074, R1075, R1076, R1077, R1078, R1079, R1080, R1081, R1082, R1083, R1084, R1085, R1086, R1087, R1088, R1089, R1090, R1091, R1092, R1093, R1094, R1095, R1096, R1097, R1098, R1099, R1100, R1101, R1102, R1103, R1104, R1105, R1106, R1107, R1108, R1109, R1110, R1111, R1112, R1113, R1114, R1115, R1116, R1117, R1118, R1119, R1120, R1121, R1122, R1123, R1124, R1125, R1126, R1127, R1128, R1129, R1130, R1131, R1132, R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1143, R1144, R1145, R1146, R1147, R1148, R1149, R1150, R1151, R1152, R1153, R1154, R1155, R1156, R1157, R1158, R1159, R1160, R1161, R1162, R1163, R1164, R1165, R1166, R1167, R1168, R1169, R1170, R1171, R1172, R1173, R1174, R1175, R1176, R1177, R1178, R1179, R1180, R1181, R

Close to LVDS1 Connector

DISCRETE for Full-HD and 3D eDP Panel

The diagram illustrates the connection of LVDS1 signals to a discrete component. The top section shows TX signals (TX0+, TX0-, TX1+, TX1-, TX2+, TX2-, TX3+, TX3-) connected to components C880-C887, which then connect to R332, R347, R349, D17, and R8751N. The bottom section shows AUX signals (AUX+, AUX-) connected to components C888-C889, which then connect to R332, R347, R349, D17, and R8751N. A bottom-right inset shows a security warning.

Signal	Component	Value	Pin	Signal	Component	Value	Pin
<14> VGA_EDP_TX0+	C880	0.1U 0402 16V7K	1	<31> PCH_PWM	R332	0.0402 5%	1
<14> VGA_EDP_TX0-	C881	0.1U 0402 16V7K	1				
<14> VGA_EDP_TX1+	C882	0.1U 0402 16V7K	1				
<14> VGA_EDP_TX1-	C883	0.1U 0402 16V7K	1	<13> VGA_BL_PWM	R349	0.0402 5%	1
<14> VGA_EDP_TX2+	C884	0.1U 0402 16V7K	1				
<14> VGA_EDP_TX2-	C885	0.1U 0402 16V7K	1				
<14> VGA_EDP_TX3+	C886	0.1U 0402 16V7K	1				
<14> VGA_EDP_TX3-	C887	0.1U 0402 16V7K	1				
<14> VGA_EDP_AUX+	C888	0.1U 0402 16V7K	1				
<14> VGA_EDP_AUX-	C889	0.1U 0402 16V7K	1				

Security

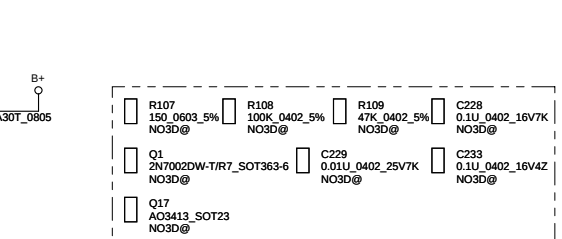
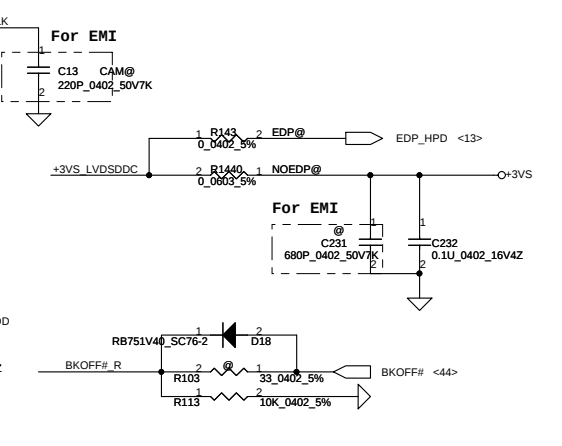
Issue

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The schematic diagram illustrates the electrical connections for the ACES_87242-4001-09 camera module. The module is a 42-pin device with a width of 20 mils. It is powered by a +3VSD supply and a +3VSDCAM supply. The camera outputs video signals (LVDS TXCLK+, LVDS TXCLK-, LVDS TZCLK+, LVDS TZCLK-) and control signals (LVDS EDID_CLK, LVDS EDID_DATA, INT_MIC_CLK, INT_MIC_DATA, LCD_ENVDD, LED_PWM, +3VSD LVSDSDC). The camera is connected to a system via a USB20 P11 R connector, a USB20 N11 R connector, a D64 connector, and a 3A connector. The system is labeled 'ACES_87242-4001-09'.

The schematic diagram illustrates the USB interface circuit. On the left, two USB signals are shown: <32> USB20_N11 and <32> USB20_P11. These signals pass through capacitors C234 and C235 (both 0.1µF, 0402_25V6) and are connected to the FBMA-L11-201209-221LMA component. The circuit also includes a +LCD_INV signal source, a capacitor C236 (0.1µF, 0402_25V6), and a resistor R2 (47K, 0402_5%). The output of the circuit is labeled LED_PWM.



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				Custom	4019BD	
				Date:	Monday, February 28, 2011	Sheet 25 of 59

OPTIMUS

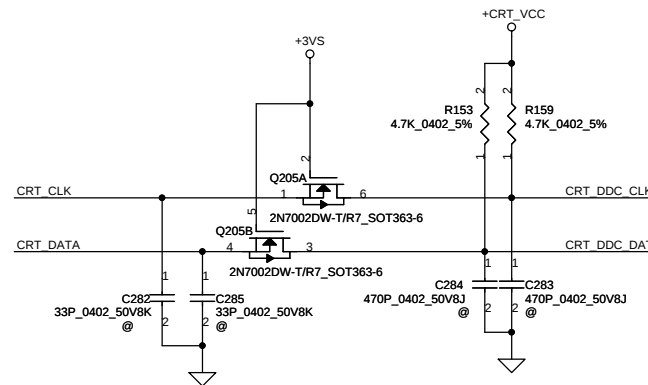
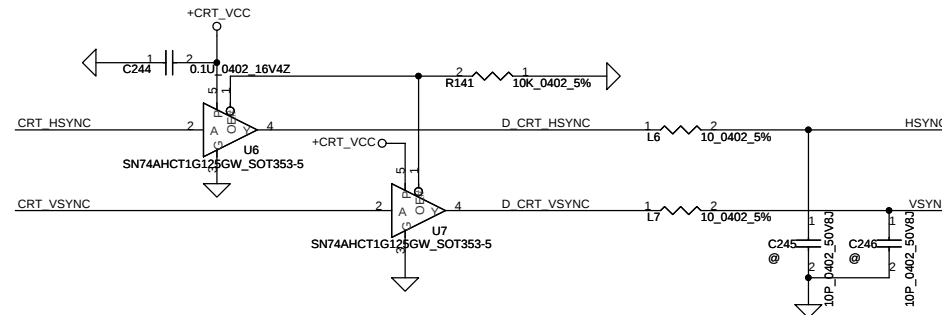
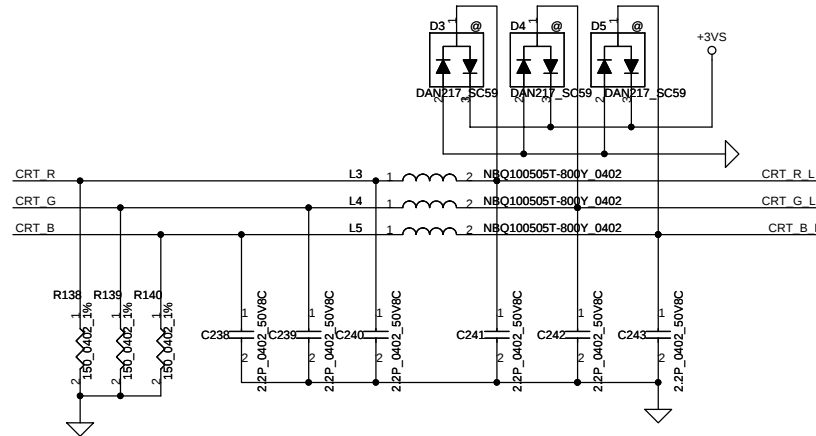
<31> UMA_CRT_R	1 OPT0 2	CRT_R
<31> UMA_CRT_G	1 OPT0 2	CRT_G
<31> UMA_CRT_B	1 OPT0 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT0 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT0 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT0 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT0 2	CRT_DATA

Close to CRT Connector

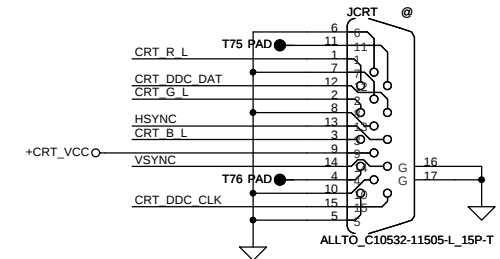
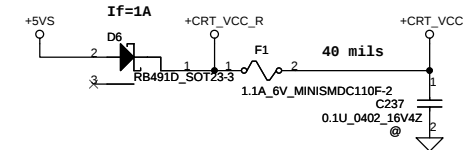
DISCRETE

<13> VGA_CRT_R	1 DIS0 2	CRT_R
<13> VGA_CRT_G	1 DIS0 2	CRT_G
<13> VGA_CRT_B	1 DIS0 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS0 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS0 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS0 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS0 2	CRT_DATA

Close to CRT Connector

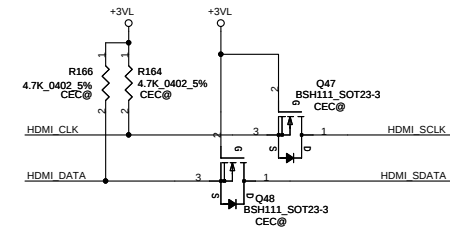
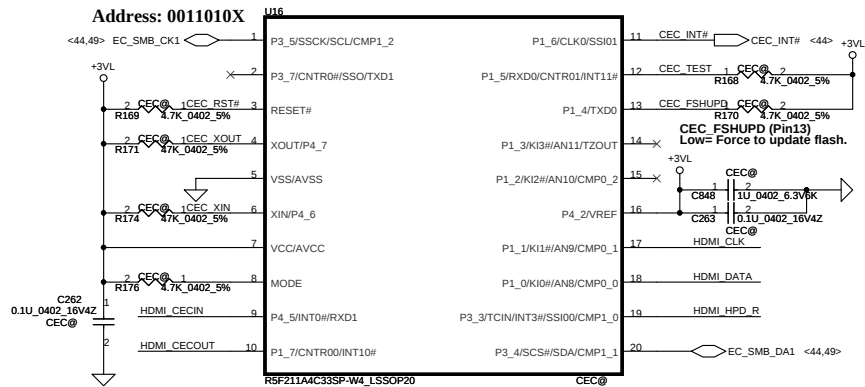
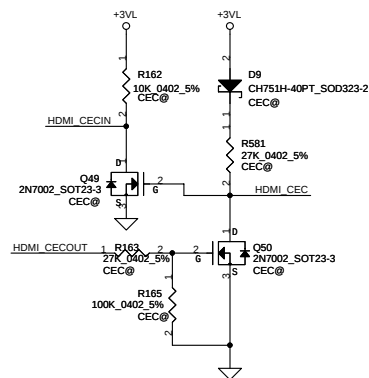


CRT CONNECTOR



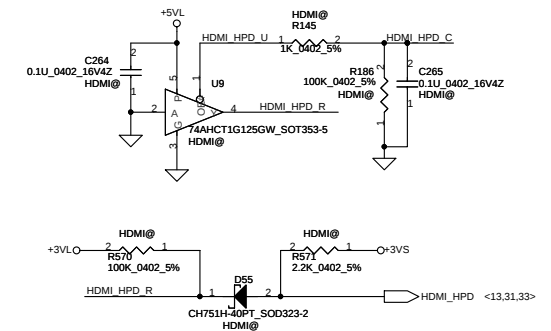
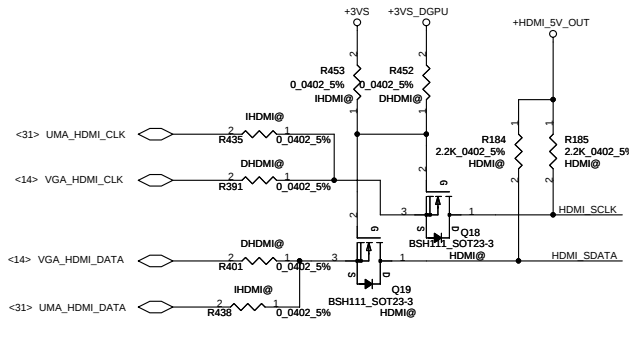
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				Date	Monday, February 28, 2011
				Sheet	26 of 59

HDMI CEC Controller



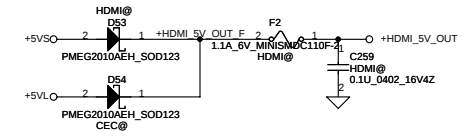
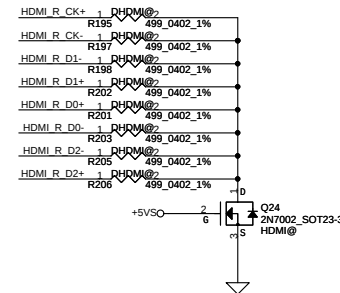
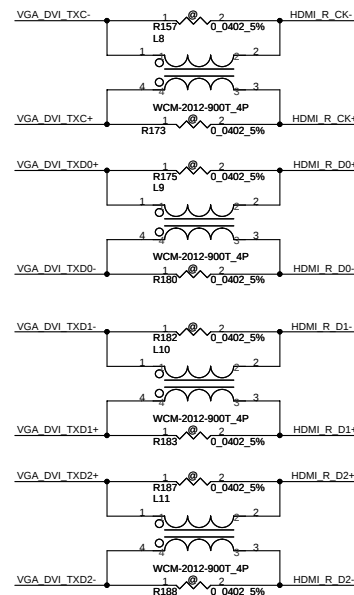
For DISCRETE

<14>	VGA_HDMI_CLK+	CV296	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXC+
<14>	VGA_HDMI_CLK-	CV293	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXC-
<14>	VGA_HDMI_TX0+	CV294	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD0
<14>	VGA_HDMI_TX0-	CV297	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD0-
<14>	VGA_HDMI_TX1+	CV299	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD1+
<14>	VGA_HDMI_TX1-	CV298	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD1-
<14>	VGA_HDMI_TX2+	CV295	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD2+
<14>	VGA_HDMI_TX2-	CV300	1	2	0.1U	0402	16V7K	DHDMI@	VGA DVI TXD2-

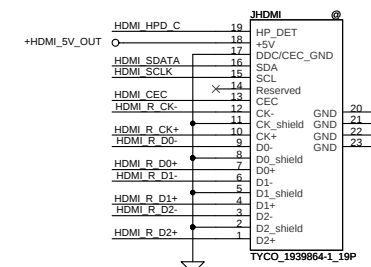


For Optimus

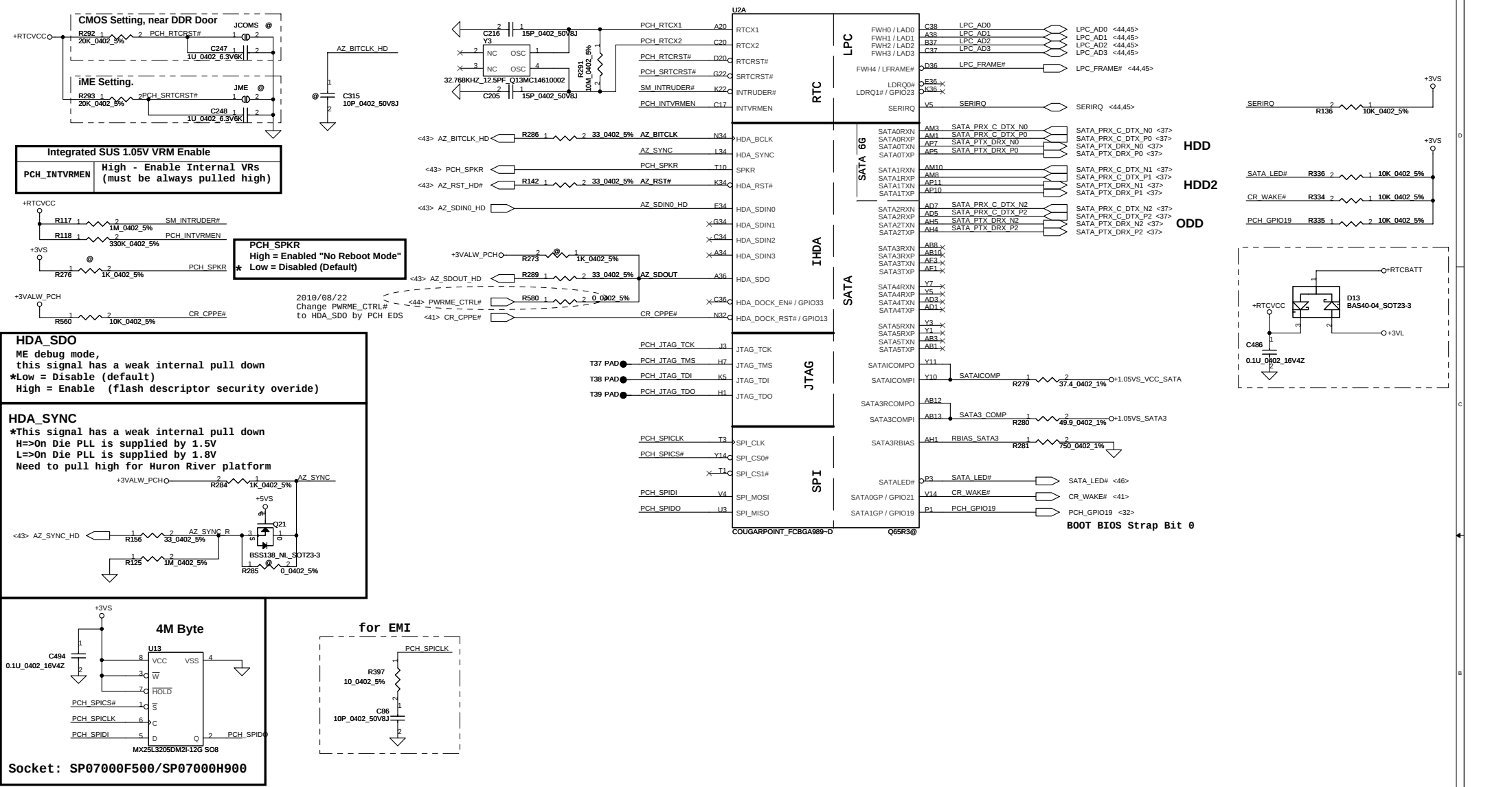
<31> UMA_HDMI_TXC+	CV308	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXC+
<31> UMA_HDMI_TXC-	CV304	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXC-
<31> UMA_HDMI_TX0+	CV306	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TX0+
<31> UMA_HDMI_TX0-	CV302	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TX0-
<31> UMA_HDMI_TX1+	CV303	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXD1+
<31> UMA_HDMI_TX1-	CV301	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXD1-
<31> UMA_HDMI_TX2+	CV307	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXD2+
<31> UMA_HDMI_TX2-	CV305	1	2	0 1U 0402 16V7K IHDMI@	VGA DVI TXD2-

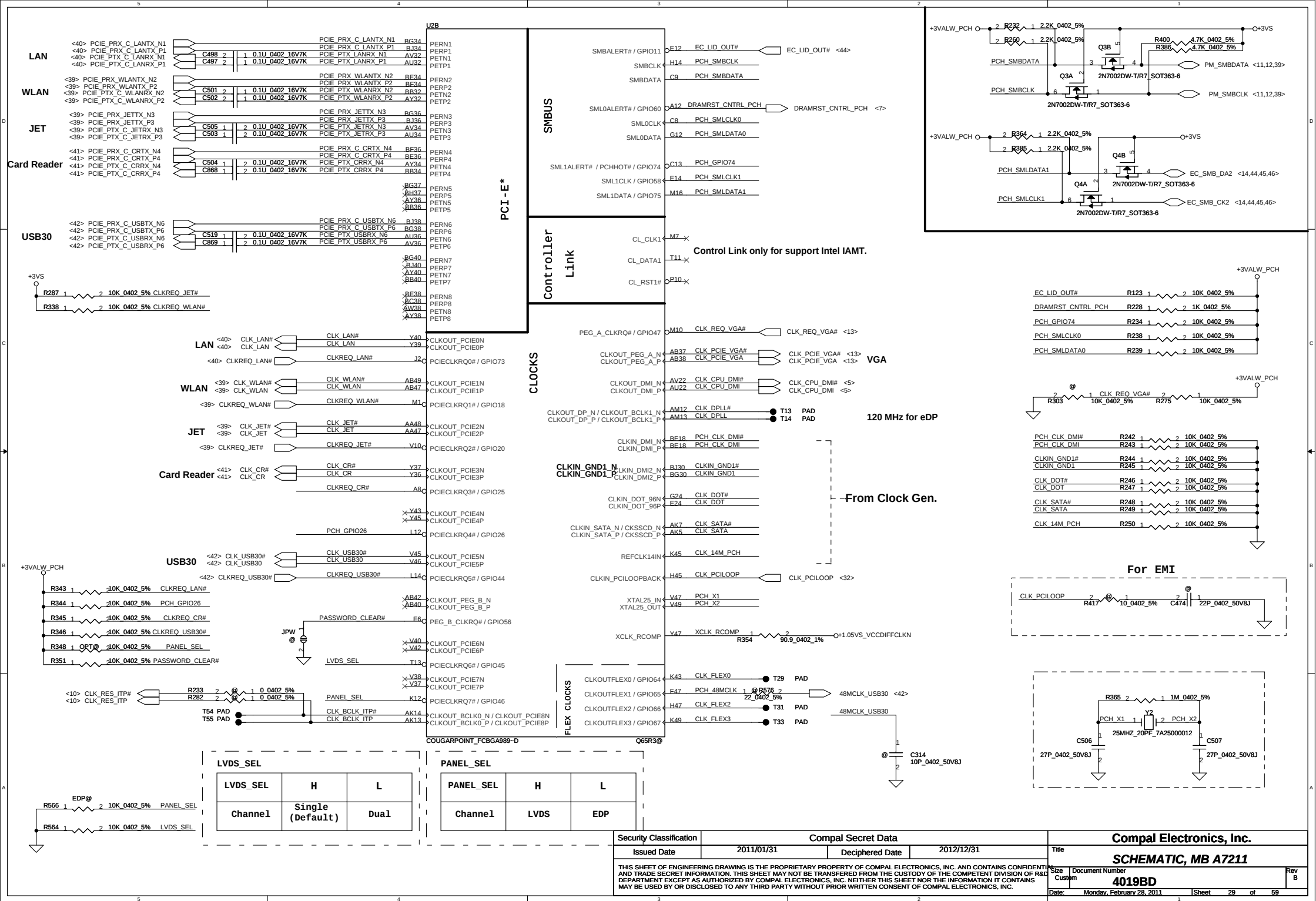


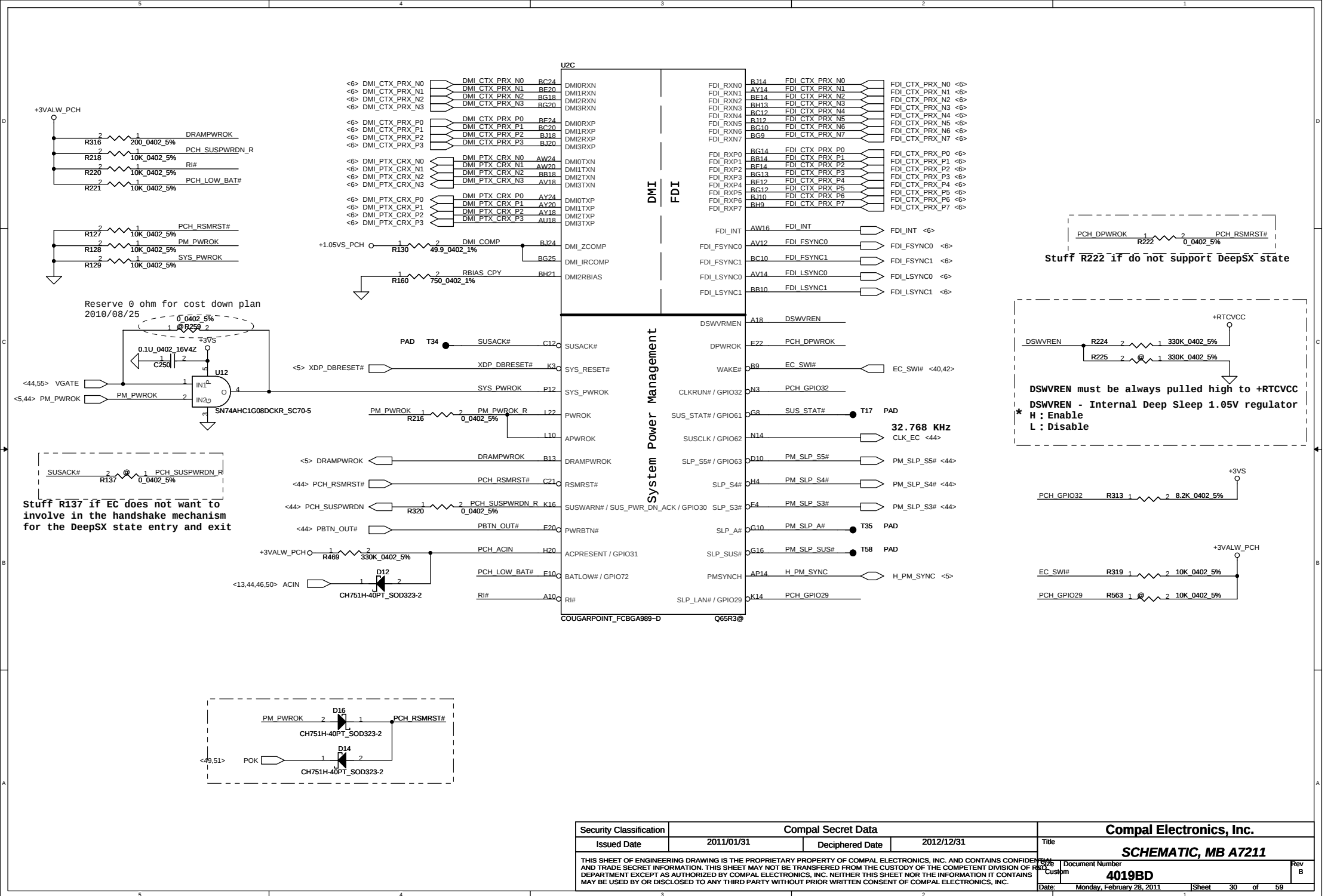
HDMI Connector

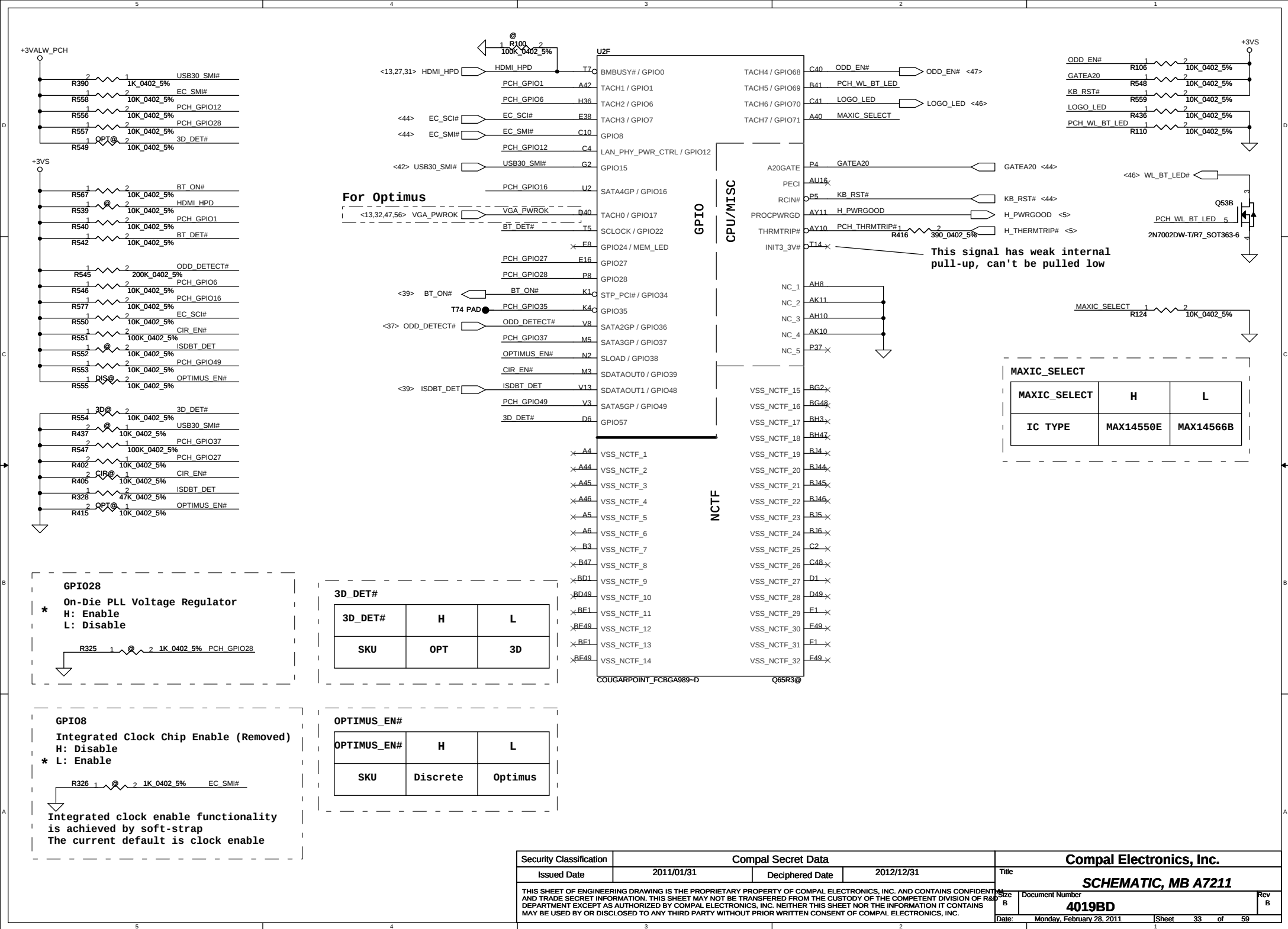


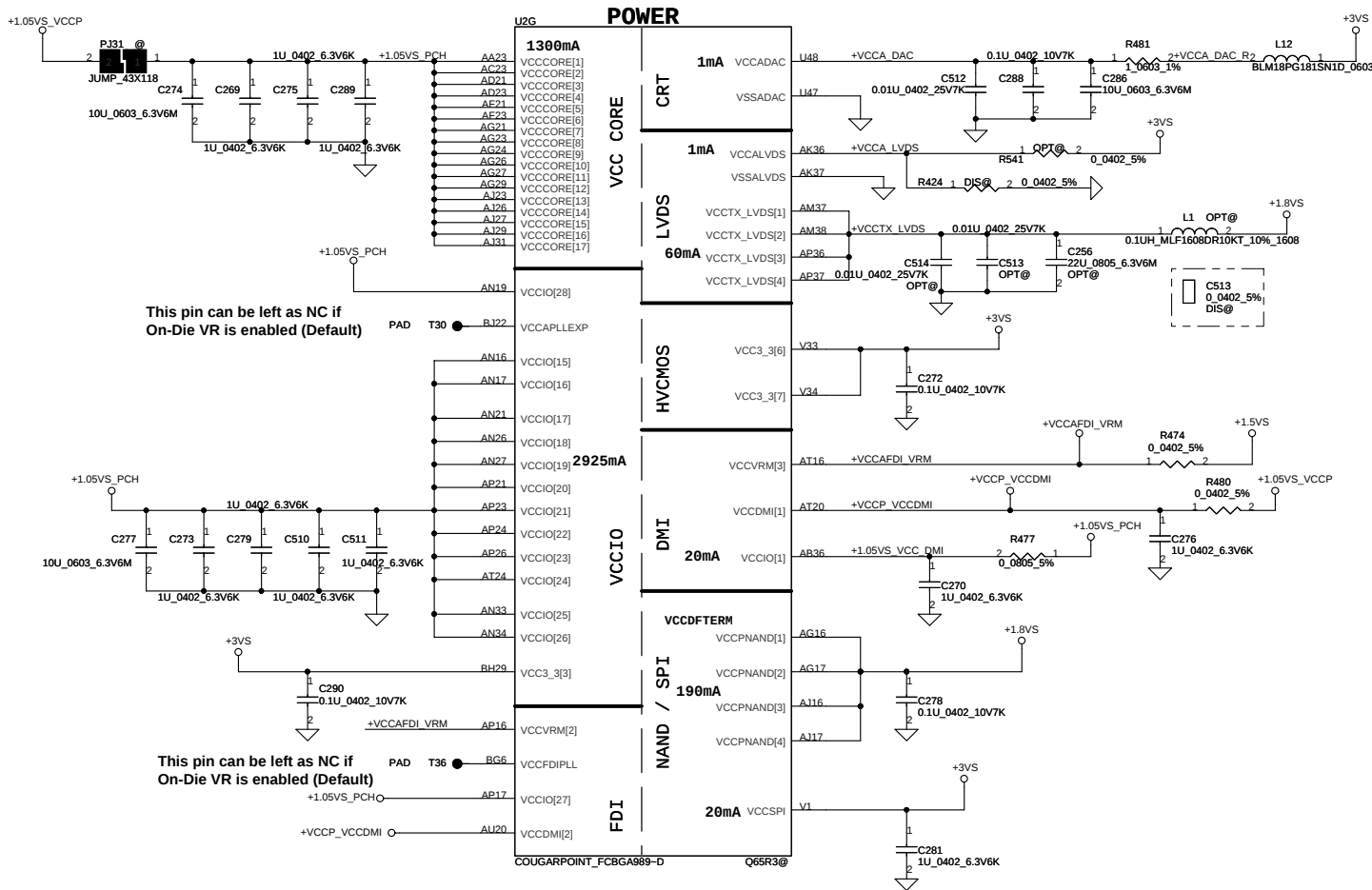
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				4019BD		
Date: Monday, February 28, 2011				Sheet	27	of 59



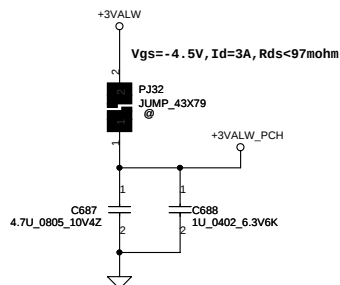




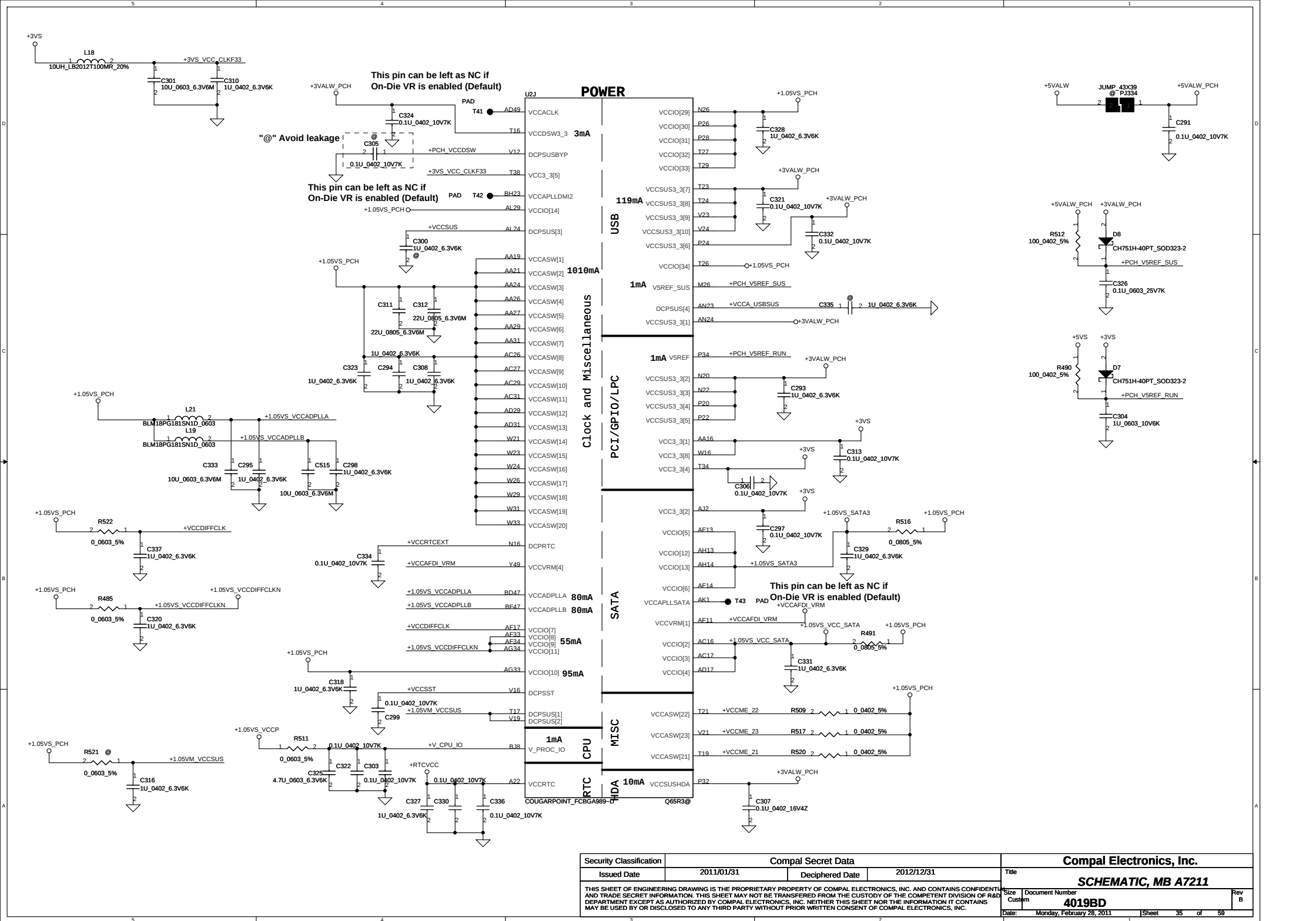


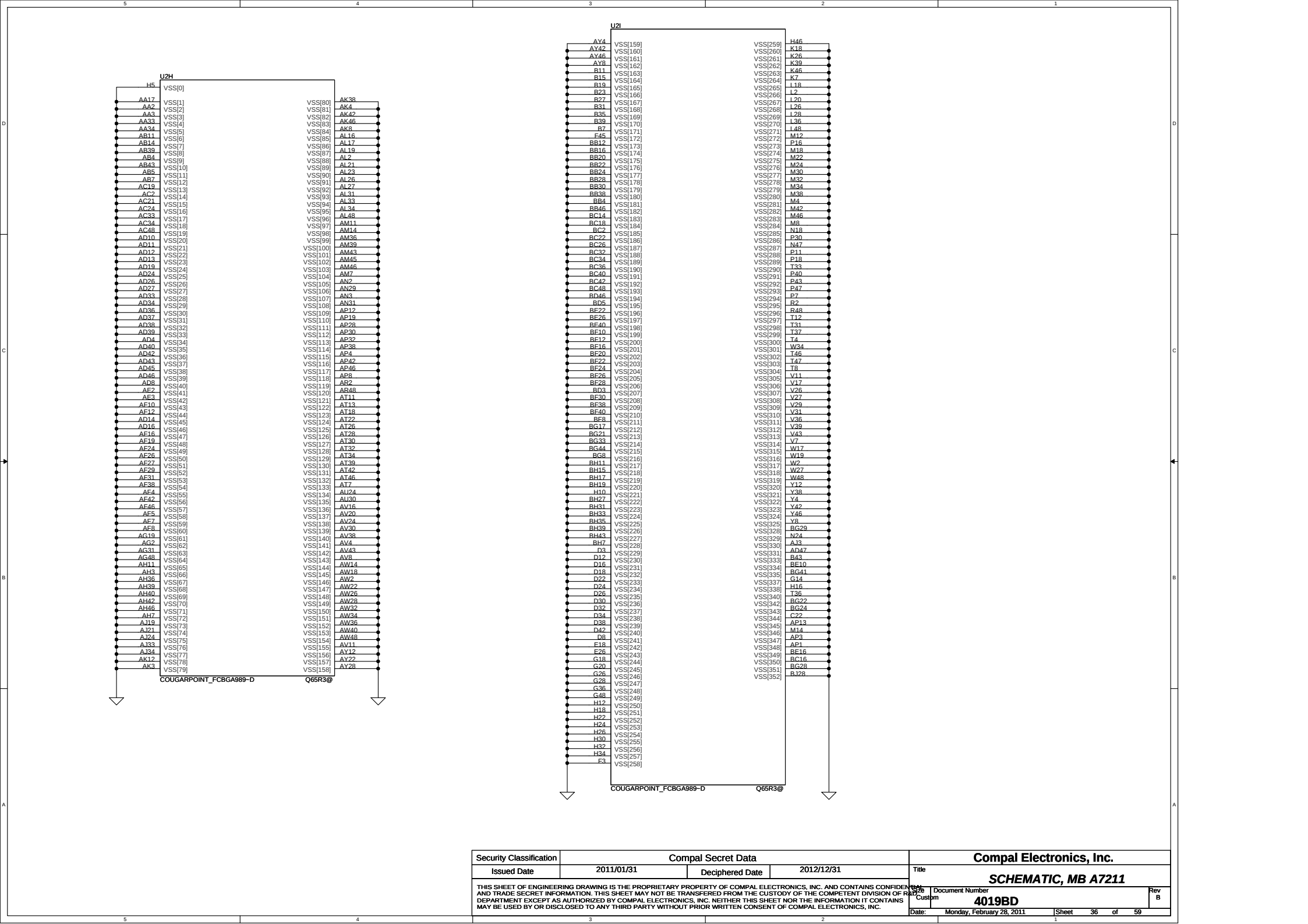


PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCDAC	3.3	0.001
VCCADPLL	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

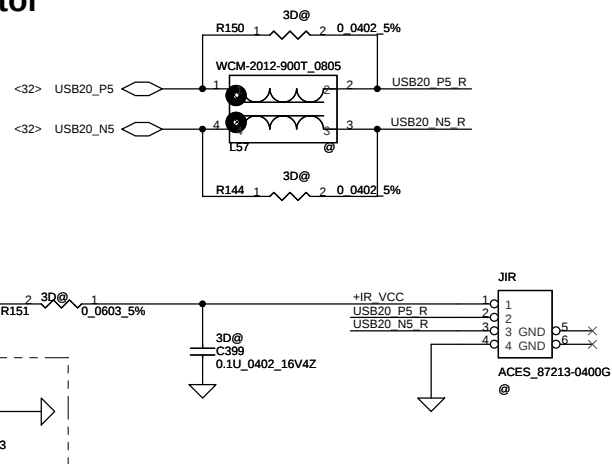


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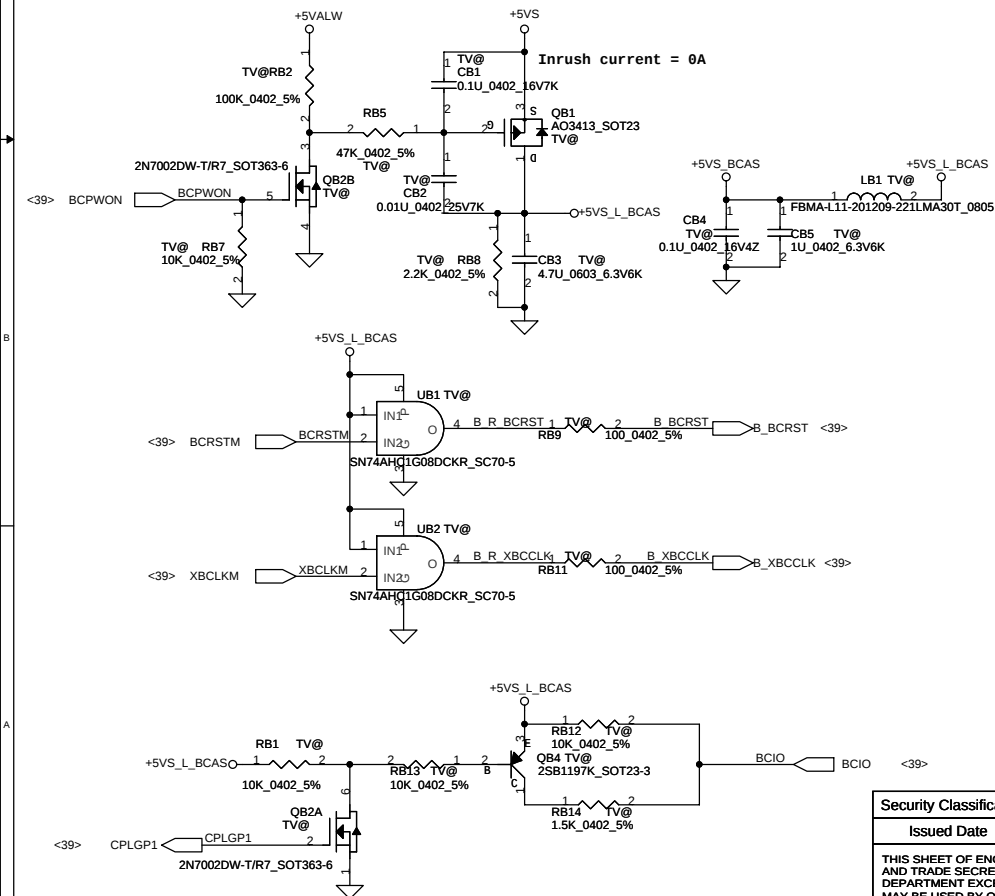




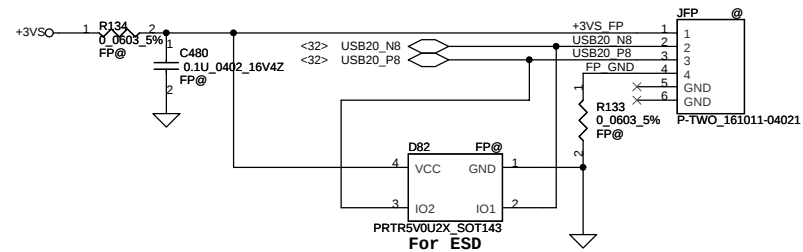
IR Emitter Connector



B-CAS Circuit



Finger printer

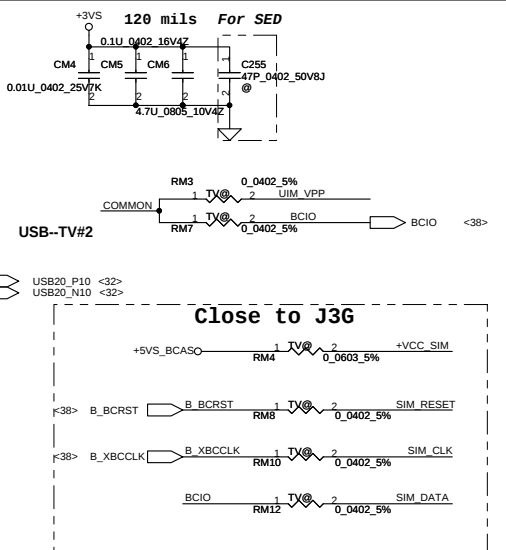
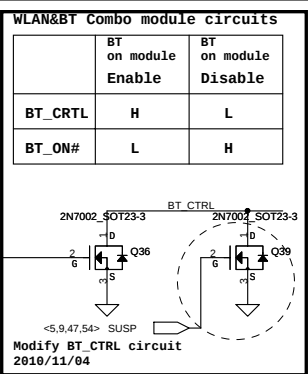


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					4019BD		
				Date:	Monday, February 28, 2011	Sheet 38 of 59	

The diagram illustrates the hardware configuration of the Intel Rainbow Peak and Compal debug card. It features a central microcontroller (U1) connected to various peripheral components. Key components include:

- Power Management:** 3V_WLAN and 3V_WLON pins are connected to the microcontroller. A 3V_WLON pin is also connected to a 3V_WLON pin.
- Capacitors:** CM1, CM2, CM3, CM4, CM5, CM6, CM7, CM8, CM9, CM10, CM11, CM12, CM13, CM14, CM15, CM16, CM17, CM18, CM19, CM20, CM21, CM22, CM23, CM24, CM25, CM26, CM27, CM28, CM29, CM30, CM31, CM32, CM33, CM34, CM35, CM36, CM37, CM38, CM39, CM40, CM41, CM42, CM43, CM44, CM45, CM46, CM47, CM48, CM49, CM50, CM51, CM52, CM53, CM54, CM55, CM56, CM57, CM58, CM59, CM60, CM61, CM62, CM63, CM64, CM65, CM66, CM67, CM68, CM69, CM70, CM71, CM72, CM73, CM74, CM75, CM76, CM77, CM78, CM79, CM80, CM81, CM82, CM83, CM84, CM85, CM86, CM87, CM88, CM89, CM90, CM91, CM92, CM93, CM94, CM95, CM96, CM97, CM98, CM99, CM100.
- Resistors:** R1433, R1434, R1435, R1436, R1437, R1438, R1439, R1440, R1441, R1442, R1443, R1444, R1445, R1446, R1447, R1448, R1449, R1450, R1451, R1452, R1453, R1454, R1455, R1456, R1457, R1458, R1459, R1460, R1461, R1462, R1463, R1464, R1465, R1466, R1467, R1468, R1469, R1470, R1471, R1472, R1473, R1474, R1475, R1476, R1477, R1478, R1479, R1480, R1481, R1482, R1483, R1484, R1485, R1486, R1487, R1488, R1489, R1490, R1491, R1492, R1493, R1494, R1495, R1496, R1497, R1498, R1499, R1500.
- Integrated Circuits:** U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100.

The diagram also includes a table for BT_CTRL and BT_ON# signals, and a section for the WLAN/WiFi interface. The schematic is labeled "FOX_AS08226-S40N-7F" and "Debug card using".



2.5A

W=60mils

RT9715BGS_S08

Pin 1: GND

Pin 2: VIN (+5VALW)

Pin 3: VOUT (+USB_VCCB)

Pin 4: EN (USB_CHG_EN#)

Pin 5: FLG (USB_OC1#)

Pin 6: VOUT (+USB_VCCB)

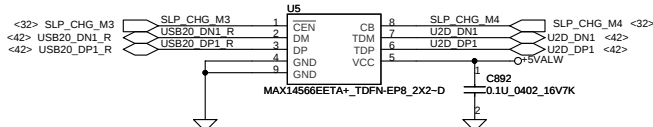
Pin 7: VOUT (+USB_VCCB)

Pin 8: VOUT (+USB_VCCB)

C983: 4.7uF 0805_10V4Z

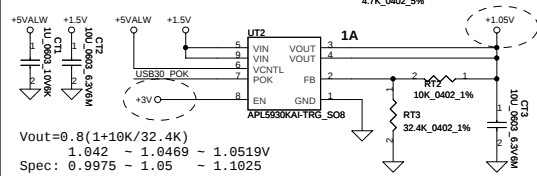
MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

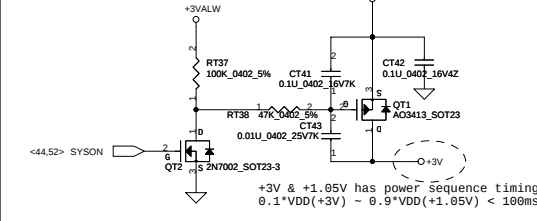


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				4019BD		
				Date:	Monday, February 28, 2011	Sheet 30 of 50

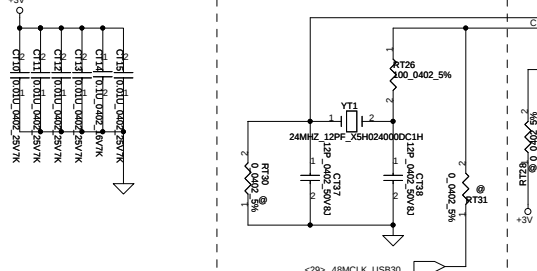
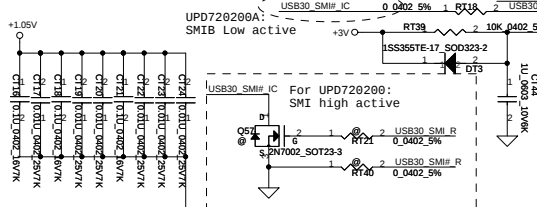
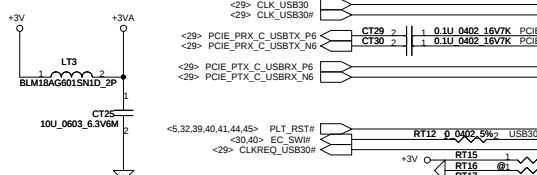
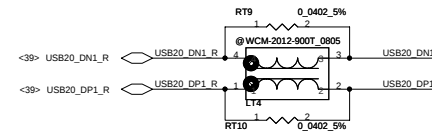
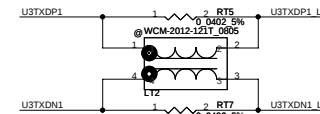
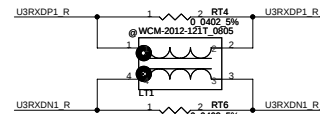
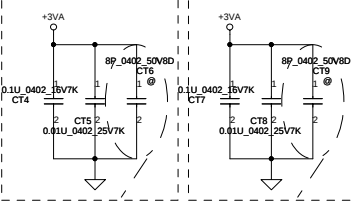
+1.5V to +1.05V Transfer



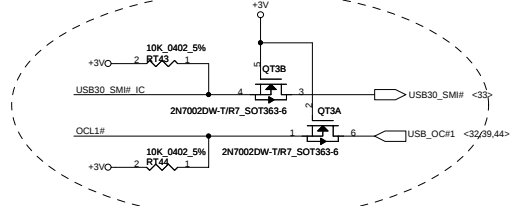
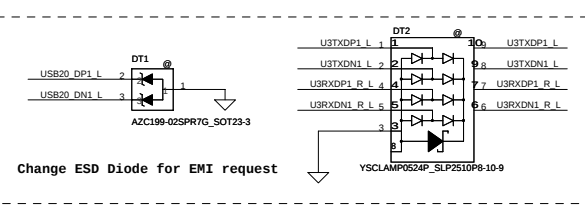
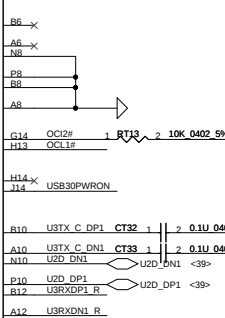
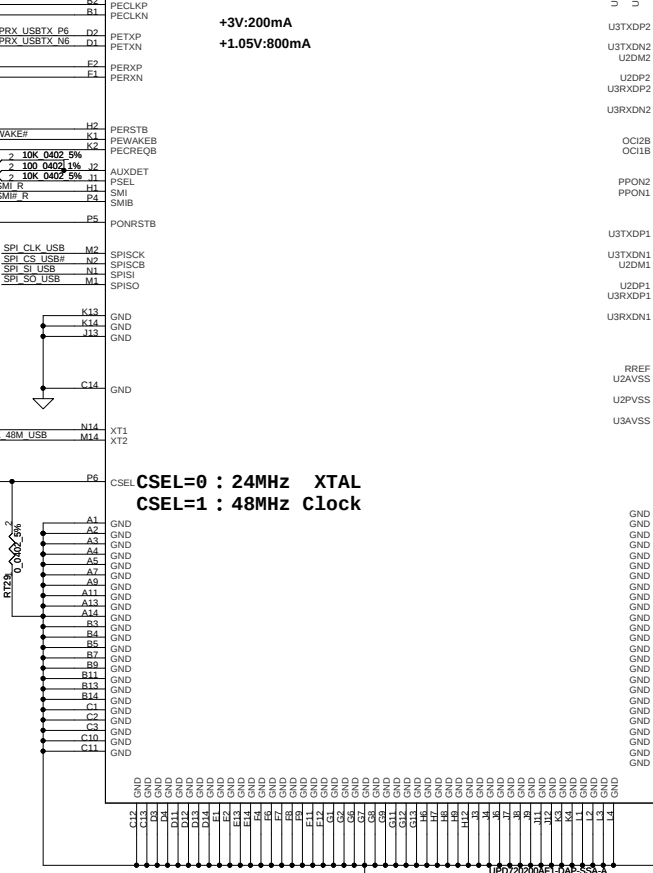
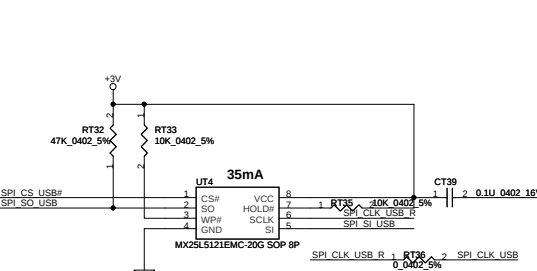
+3VALW to +3V Transfer



Close to U102.D7 Close to U102.P13

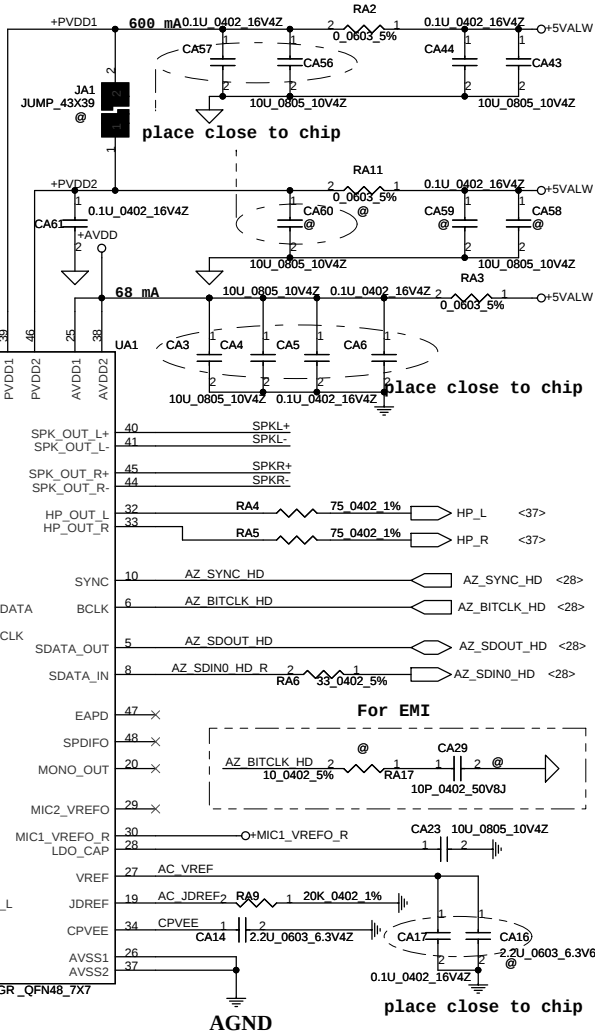
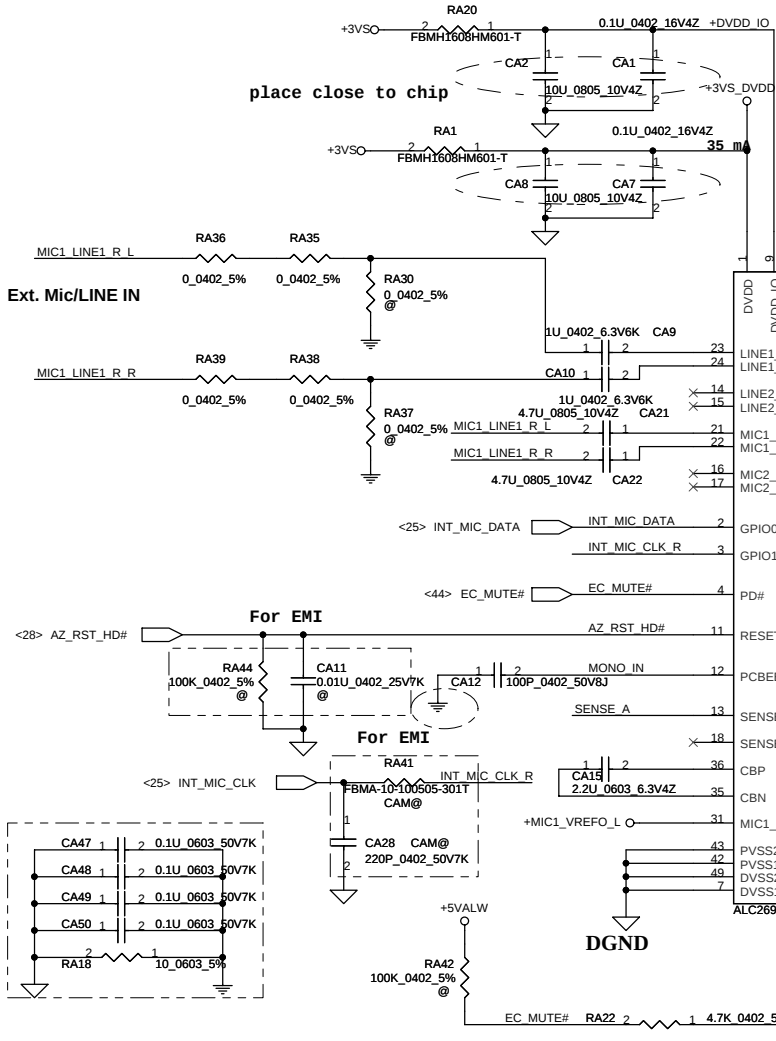


Place as close as possible to U102.N14 and U102.M14

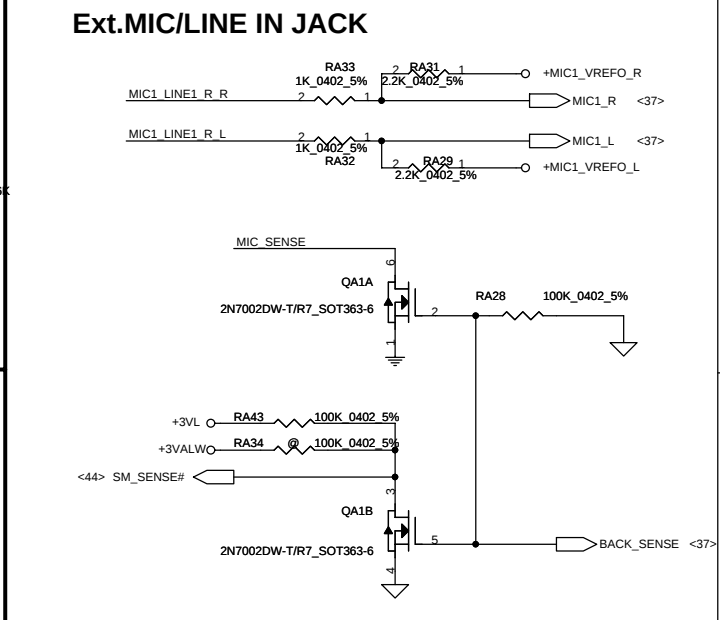
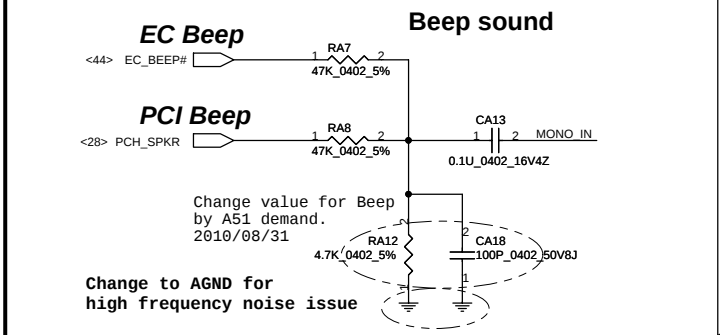
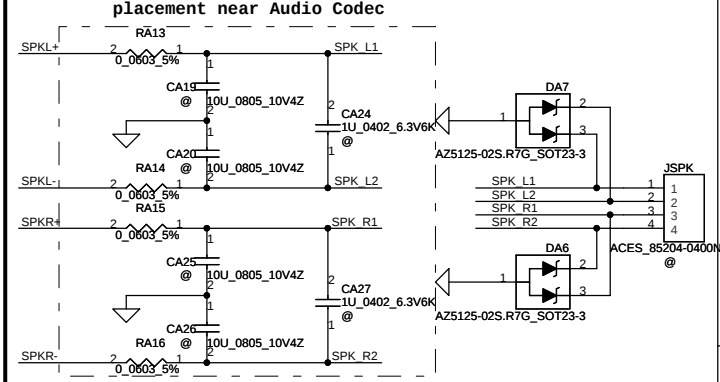


2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

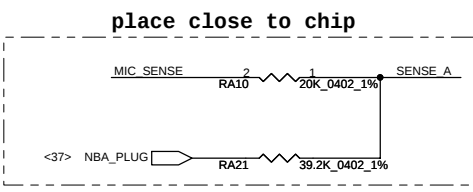
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Date	Monday, February 28, 2011	Sheet	42	of	59	Rev B



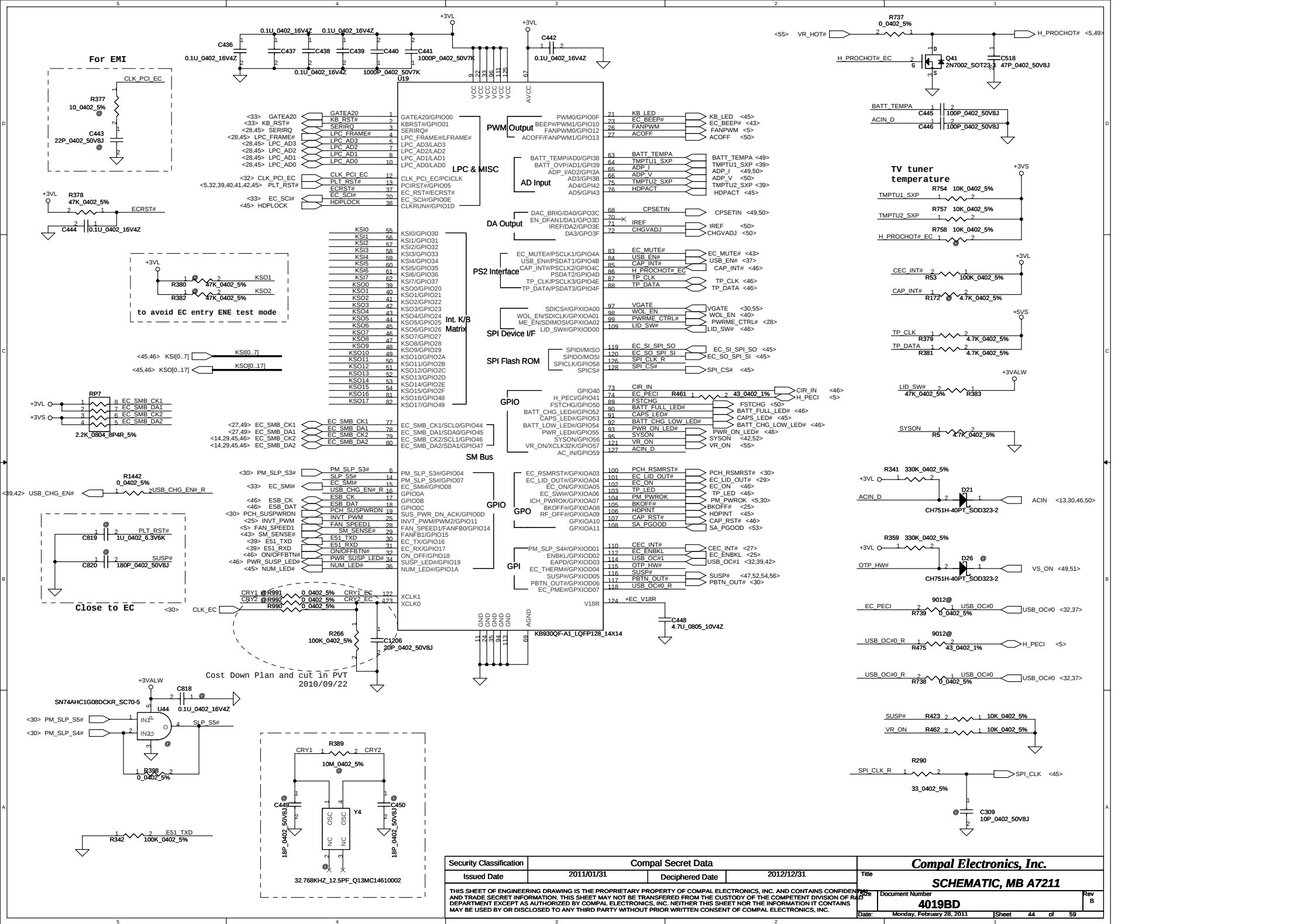
Speaker Connector



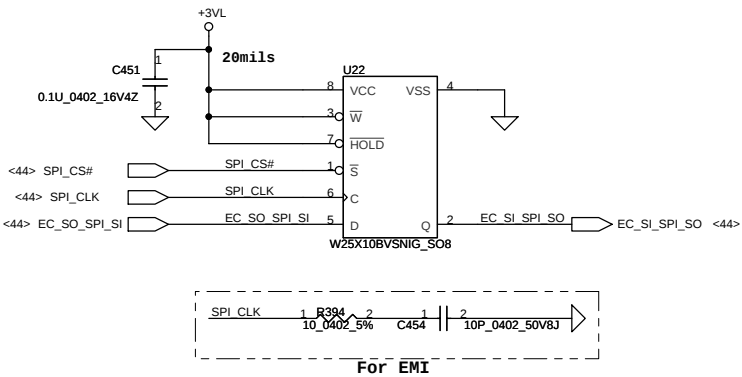
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



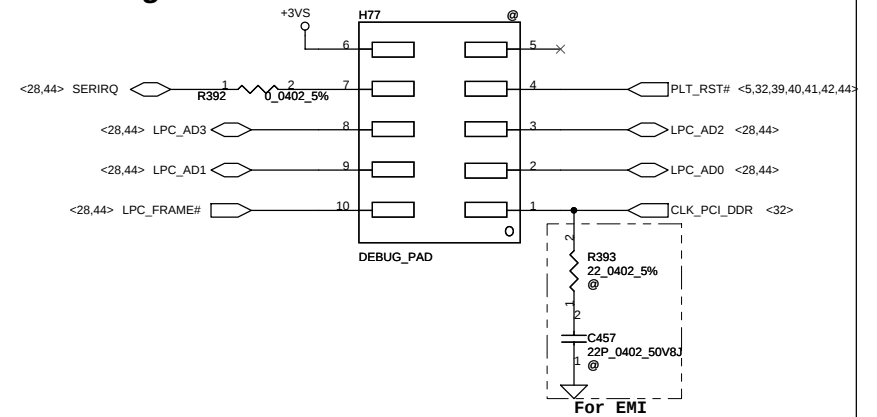
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				Date	Monday, February 28, 2011
				Sheet	43 of 59



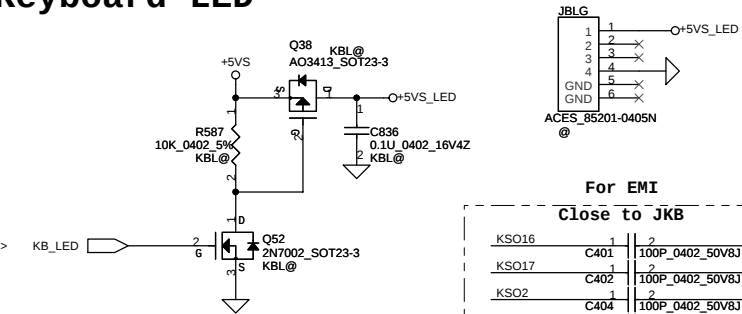
SPI Flash (256KB)



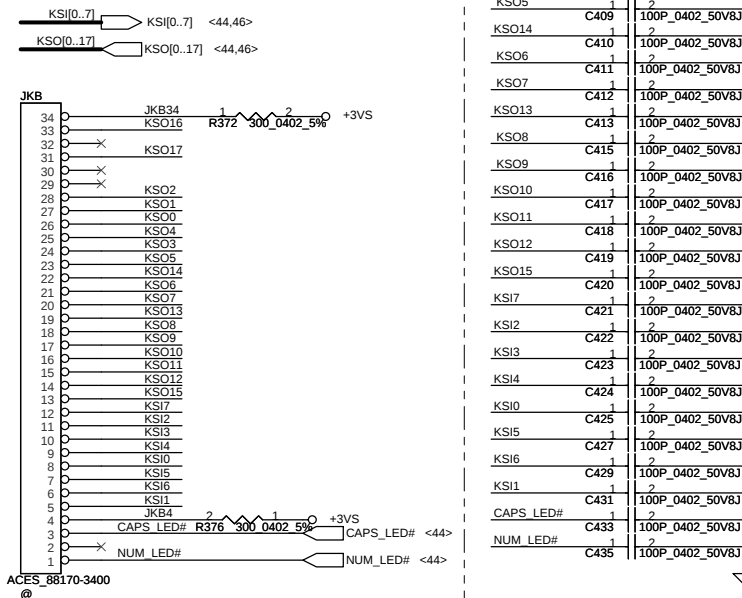
LPC Debug Port



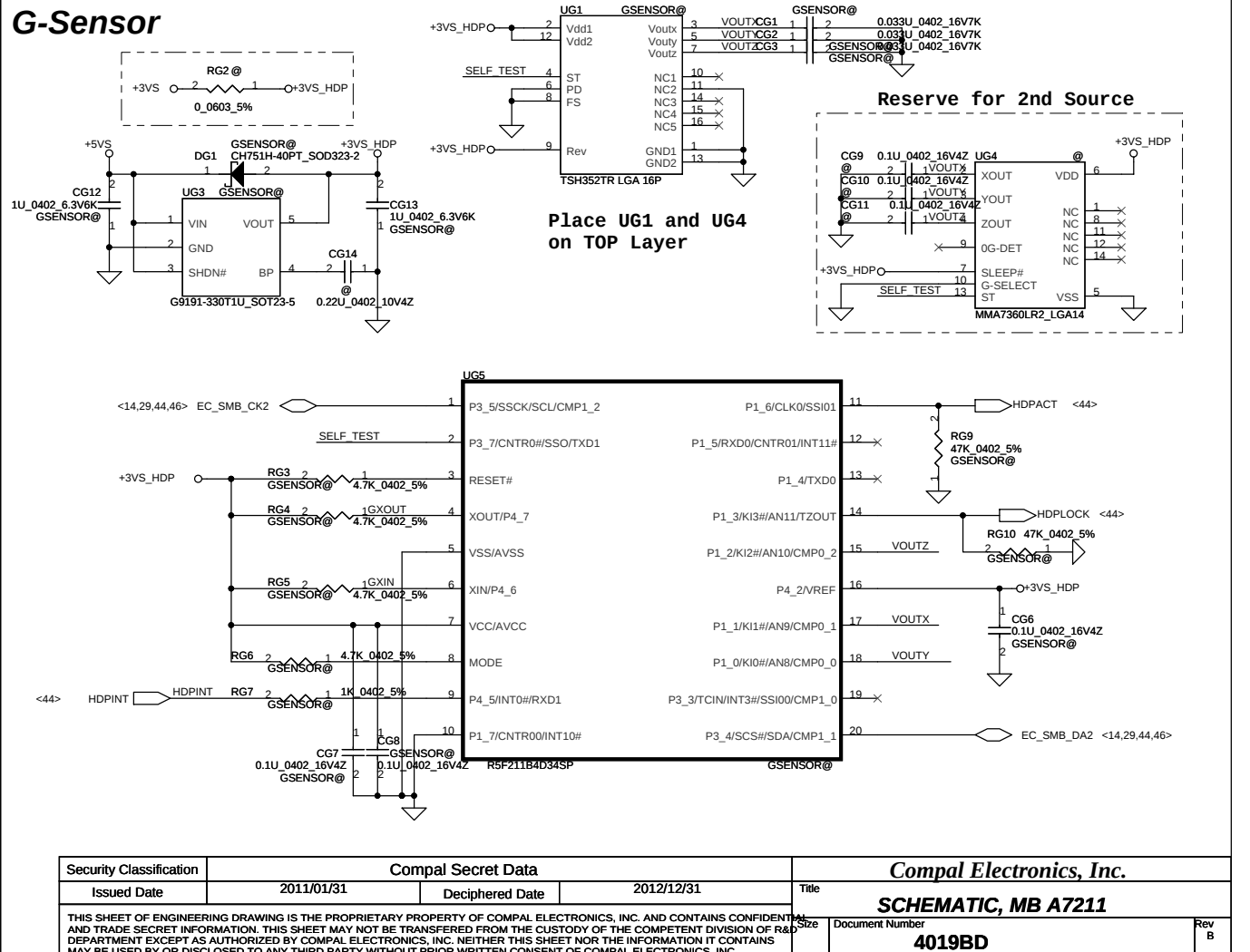
Keyboard LED



KEYBOARD CONN.

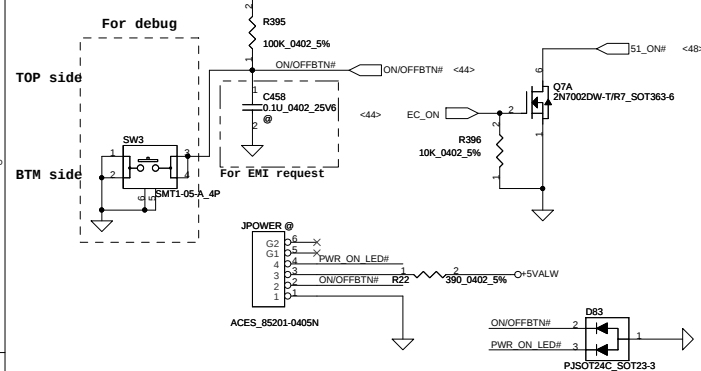


G-Sensor

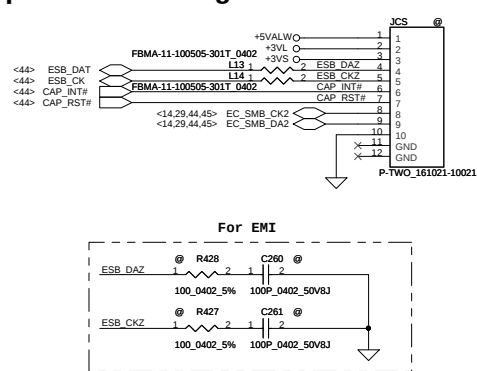


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				Document Number
				4019BD
				Rev B
				Date: Monday, February 28, 2011
				Sheet 45 of 59

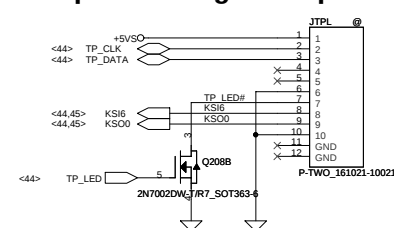
Power Button



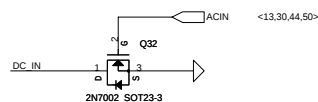
Caps Sensor/Light Sensor Conn.



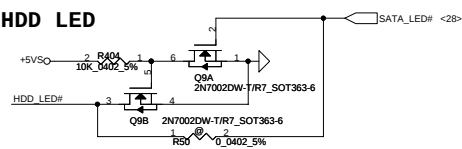
Touchpad & Light Pipe Connector



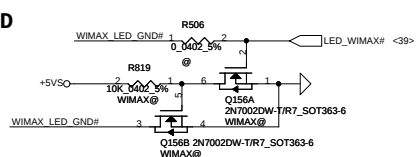
DC-IN LED



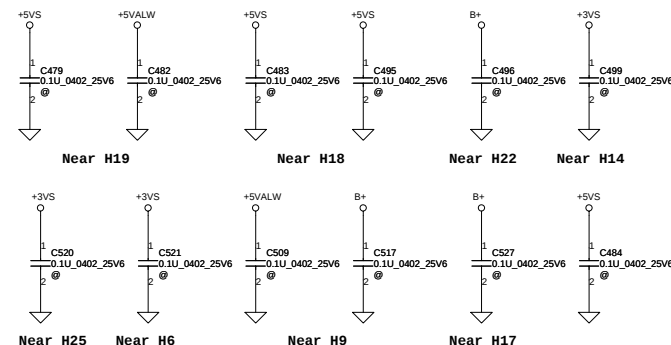
HDD LED



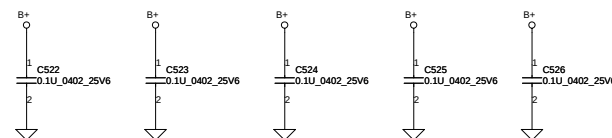
WiMAX LED



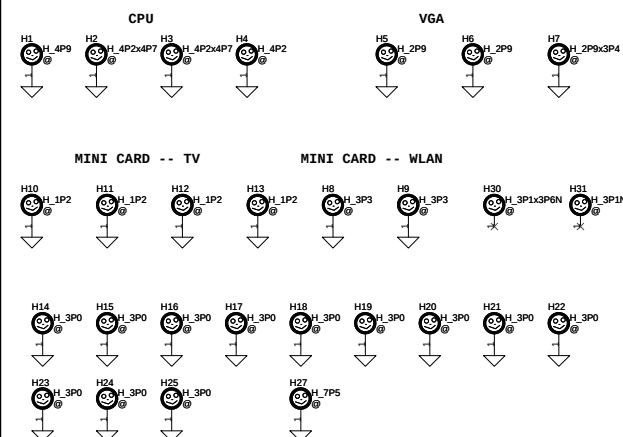
ESD solution



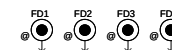
EMI solution



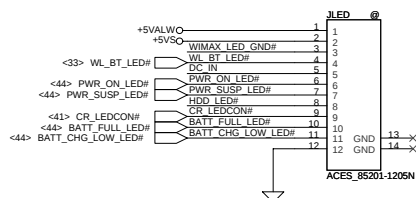
Screw Hole



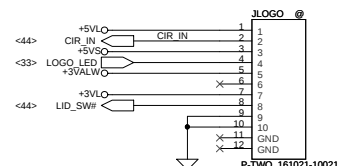
PCB Fedical Mark PAD



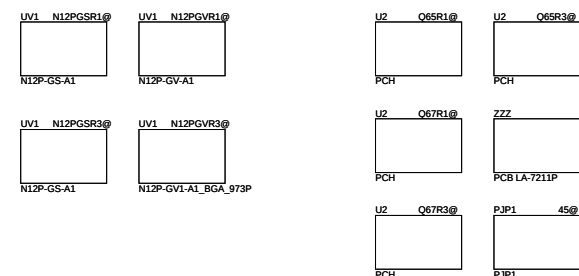
LED/B Connector



LOGO/B Connector

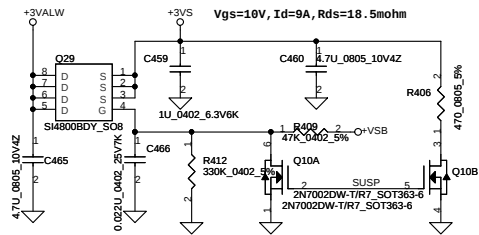


ISPD

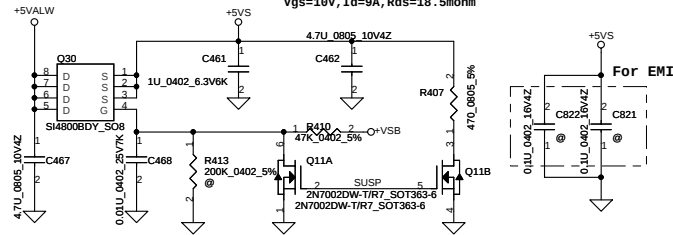


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				4019BD		
				Date:	Monday, February 28, 2011	Sheet 46 of 59

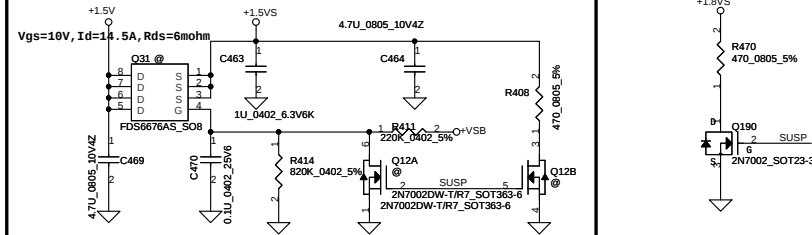
+3VALW TO +3VS



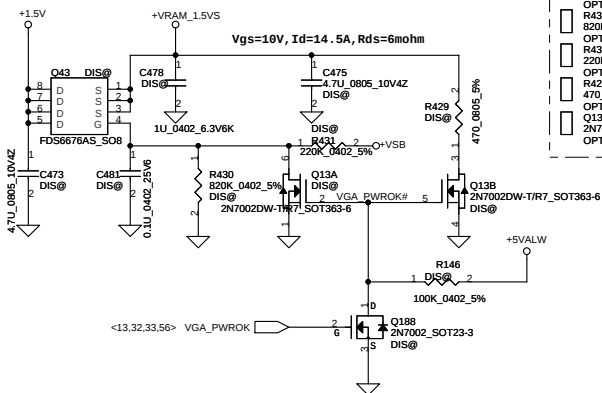
+5VALW TO +5VS



+1.5V to +1.5VS

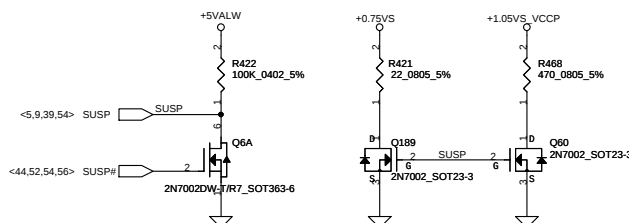
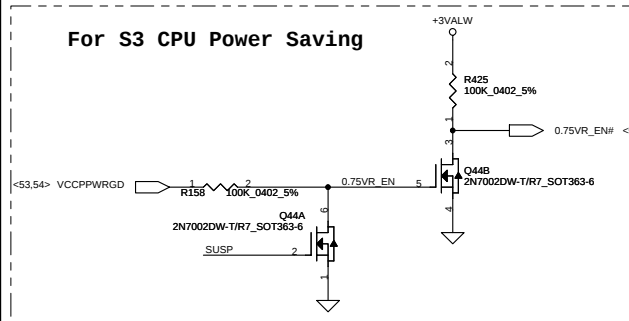


+1.5V to +VRAM_1.5VS

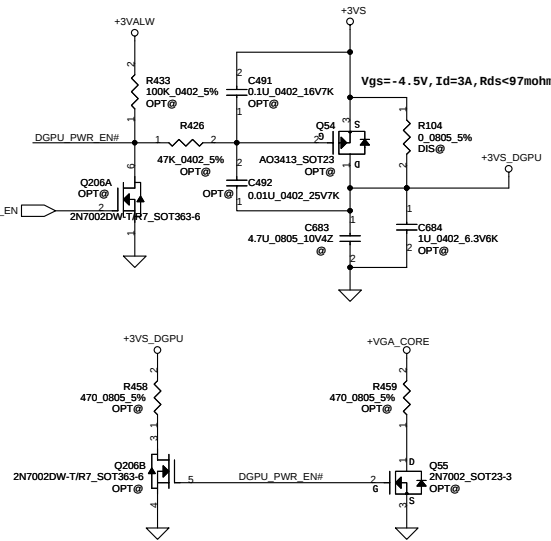


Q43 FD56676AS_S08 OPT@	C473 4.7U_0805_10V4Z OPT@
C481 0.1U_0402_25V6 OPT@	C478 1U_0402_6.3V6K OPT@
R430 820K_0402_5% OPT@	C475 4.7U_0805_10V4Z OPT@
R431 220K_0402_5% OPT@	R146 100K_0402_5% OPT@
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Q13 2N7002DW-T/R7_SOT363-6 OPT@	

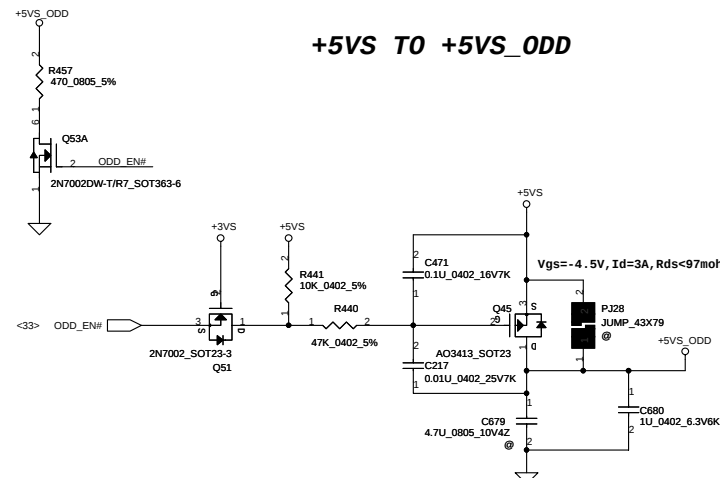
For S3 CPU Power Saving



+3VS to +3VS_DGPU

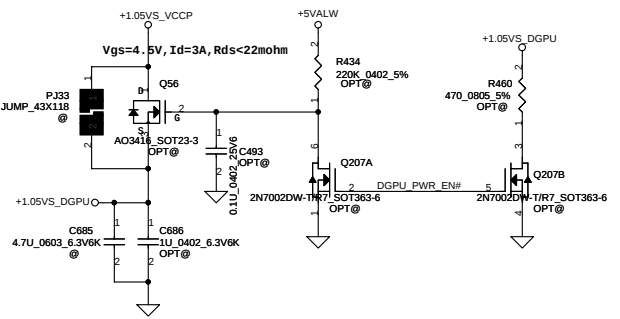


+5VS TO +5VS_ODD

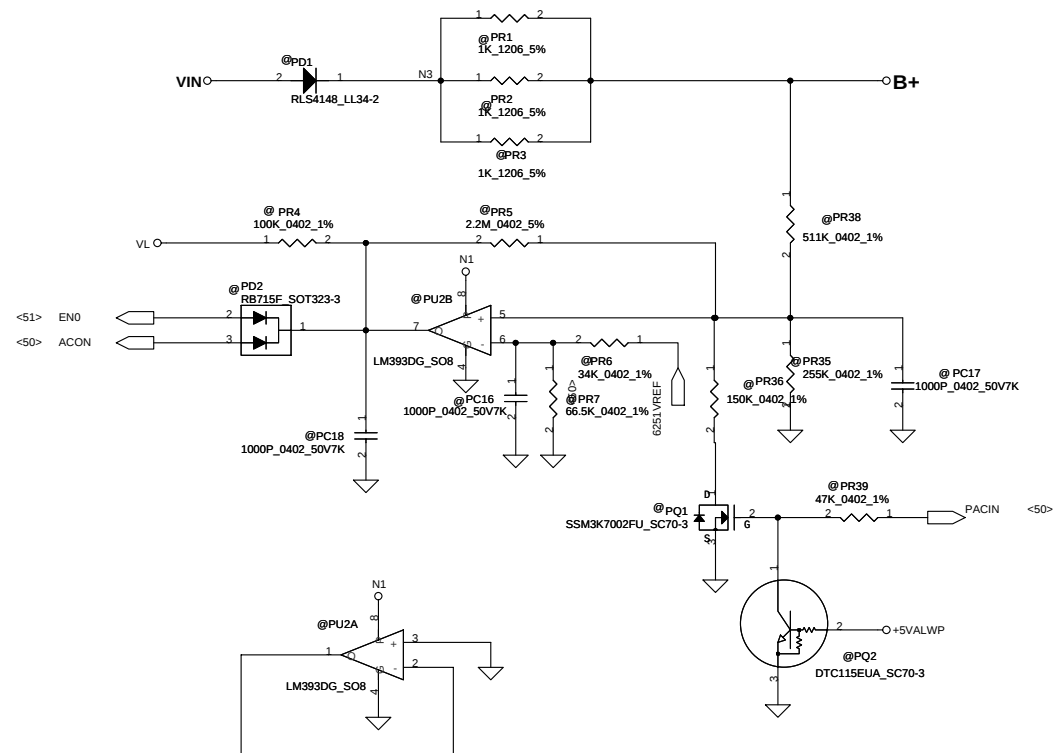
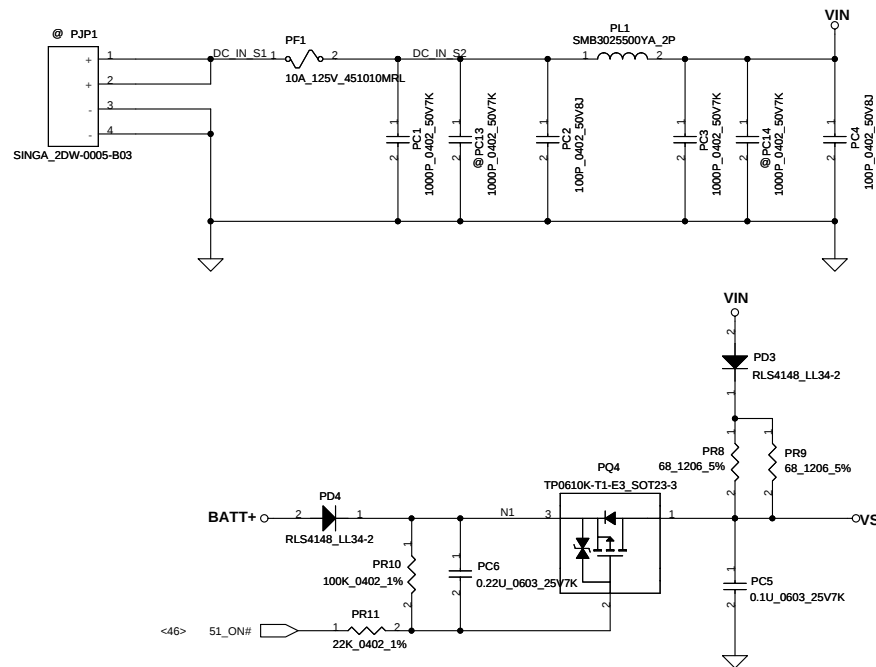


+1.05VS_VCCP to +1.05VS_DGPU

Short PJ33 for Discrete SKUs

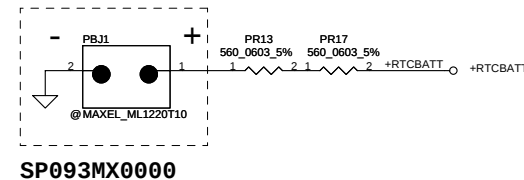


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				4019BD
				Rev B
				Date: Monday, February 28, 2011
				Sheet 47 of 59

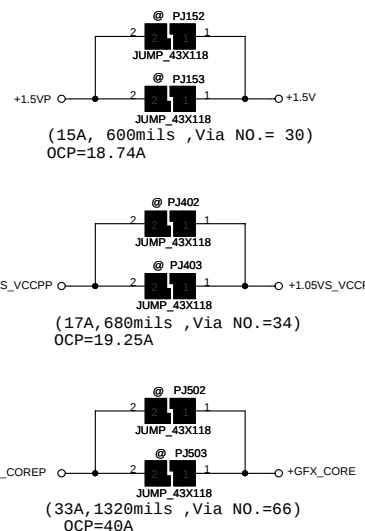
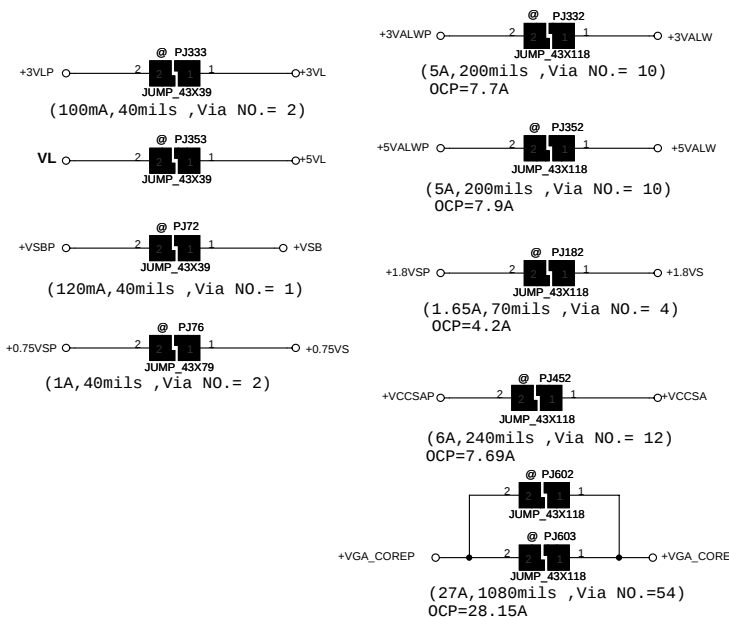


ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

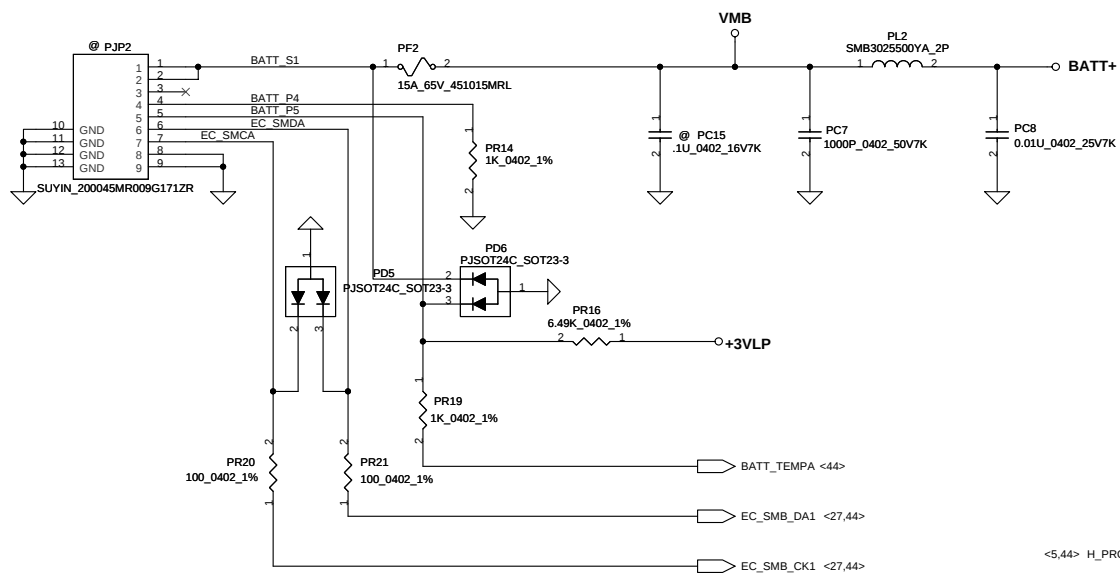
RTC Battery



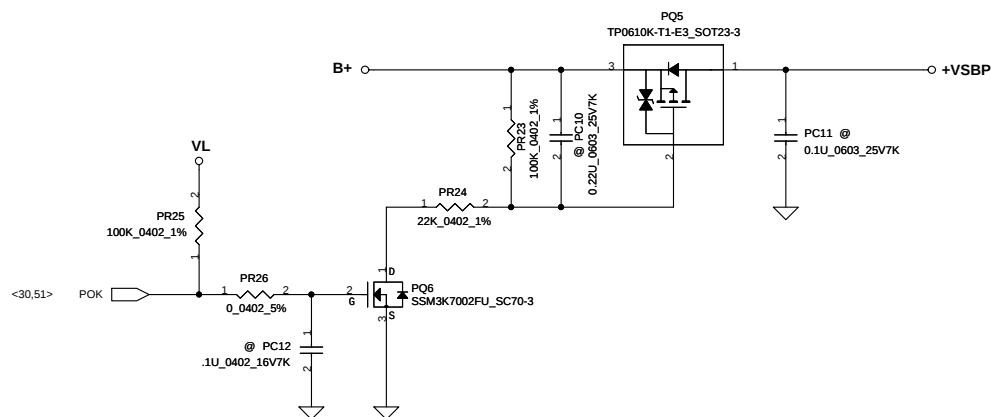
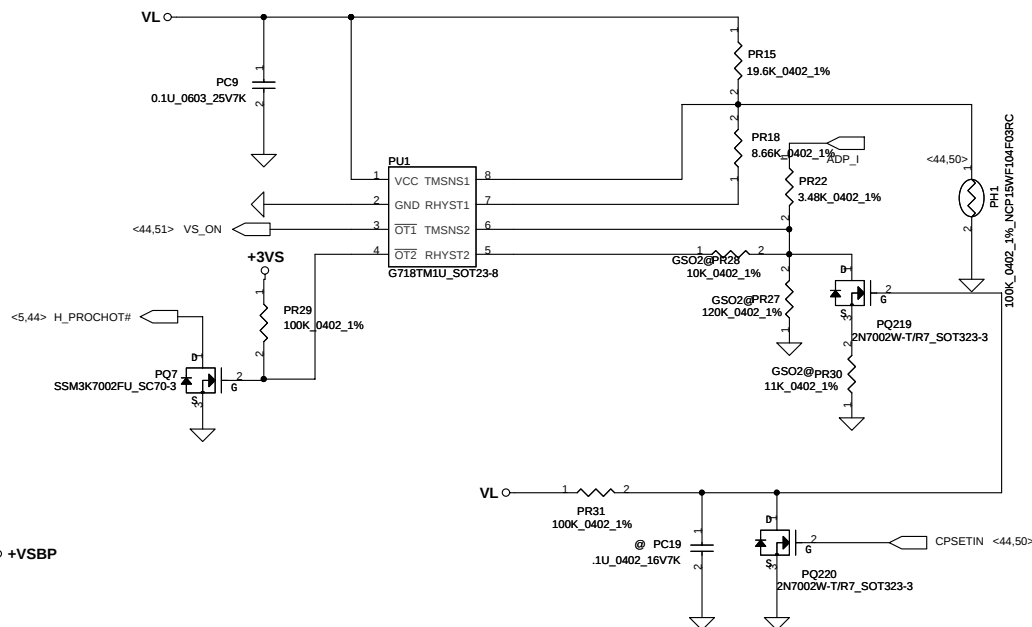
SP093MX0000



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						4019BD			
						Document Number		Rev B	
						Date: Monday, February 28, 2011		Sheet 48 of 59	

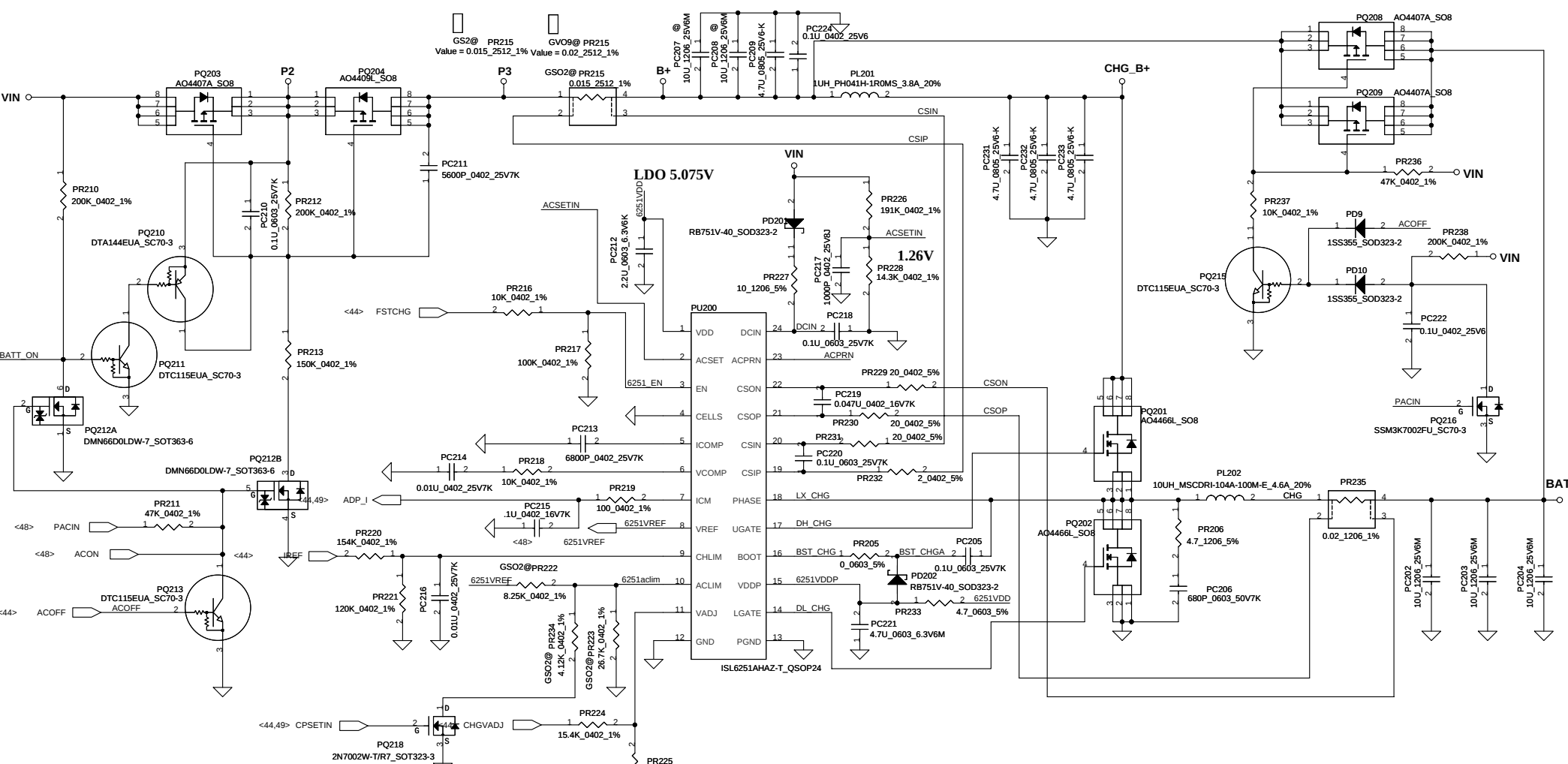


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



GS2@ PR30 Value = 11K_0402_1% GVO9@ PR30 Value = 14.7K_0402_1%
GS2@ PR28 Value = 10K_0402_1% GVO9@ PR28 Value = 20K_0402_1%
GS2@ PR27 Value = 120K_0402_1% GVO9@ PR27 Value = 15.8K_0402_1%

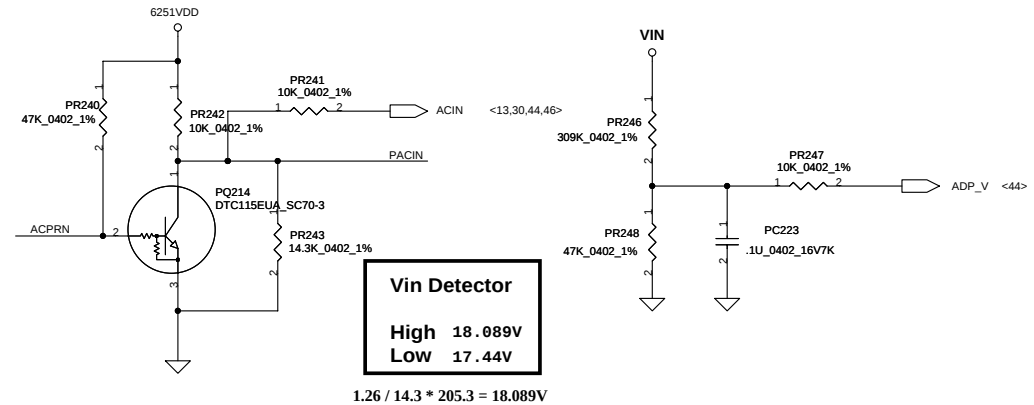
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				Date: Monday, February 28, 2011	Sheet 49 of 59

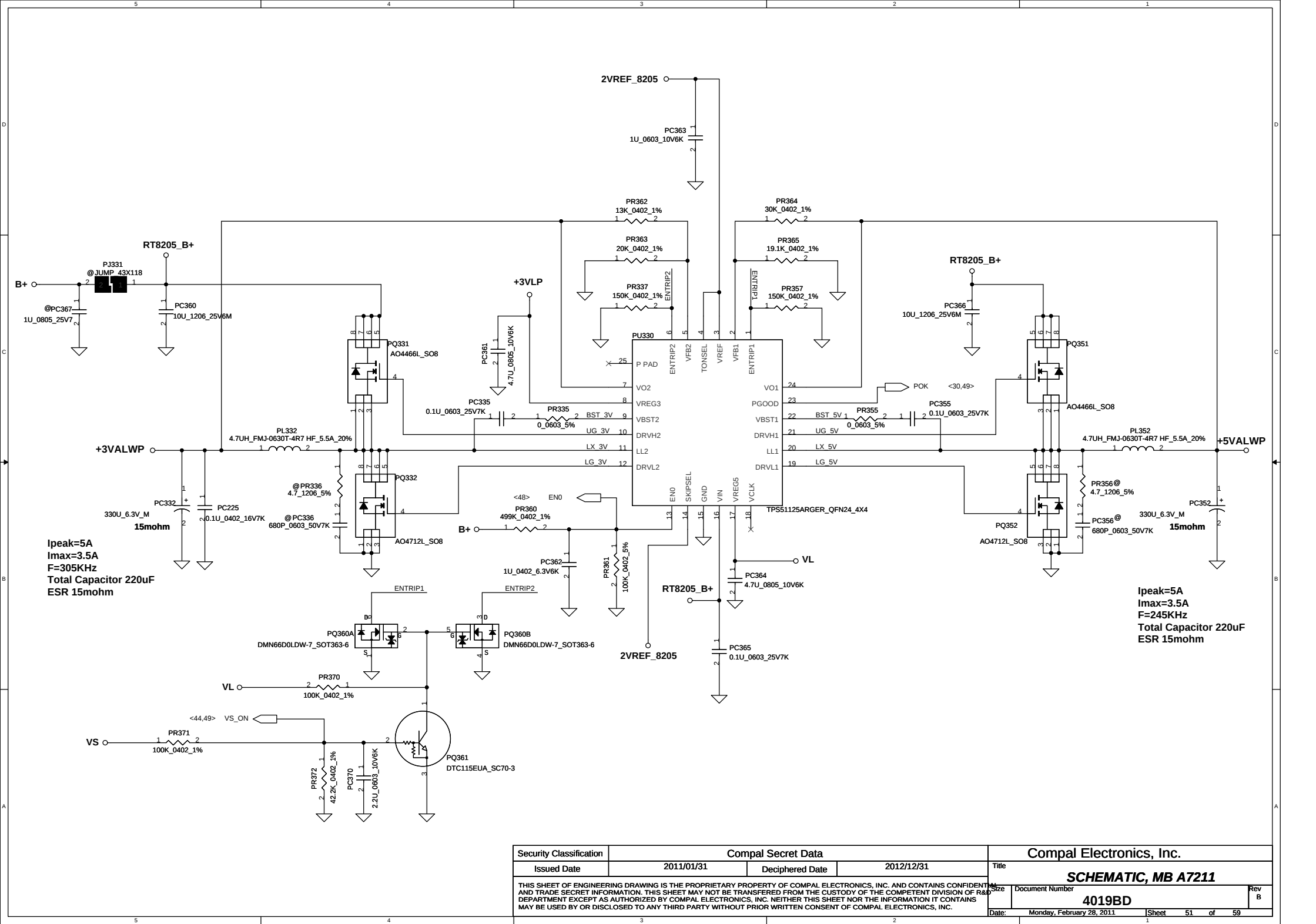


CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

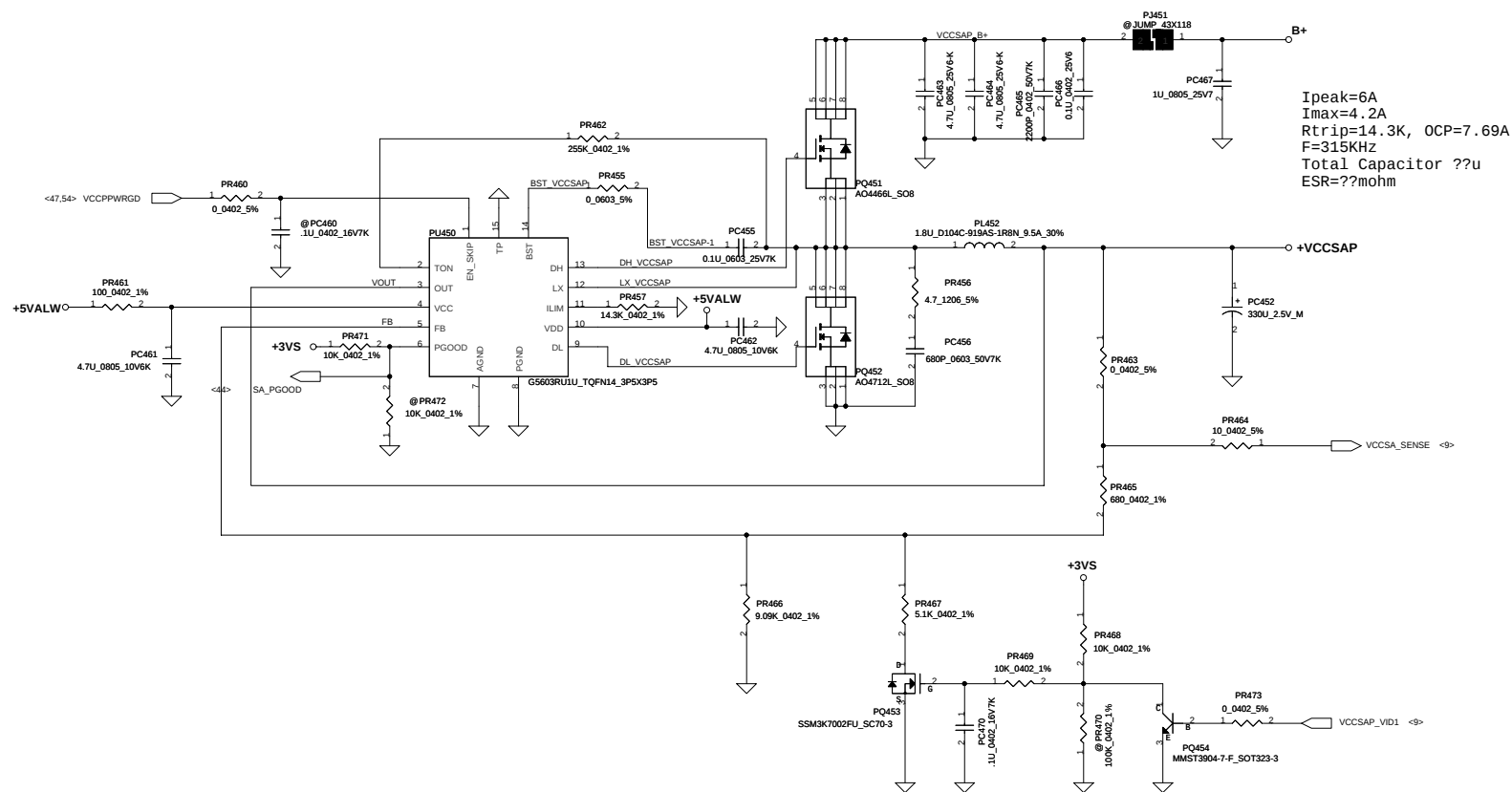
CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode	
Iada=0~3.42A(65W)	CP= 92%*Iada; CP=3.147A
VacLim=0.6621V(65W)	PR222=75k, PR223=20k, PR215=0.02
Iada=0~3.947A(75W)	CP= 92%*Iada; CP=3.63A
VacLim=1.1V(75W)	PR222=24k, PR223=20k, PR215=0.02
Iada=0~4.737A(90W)	CP= 92%*Iada; CP=4.36A
VacLim=0.737V(90W)	PR222=53.6k, PR223=20k, PR215=0.015
Iada=0~6.316A(120W)	CP= 92%*Iada; CP=5.81A
VacLim=1.777V(120W)	PR222=8.25k, PR223=26.7k, PR215=0.015



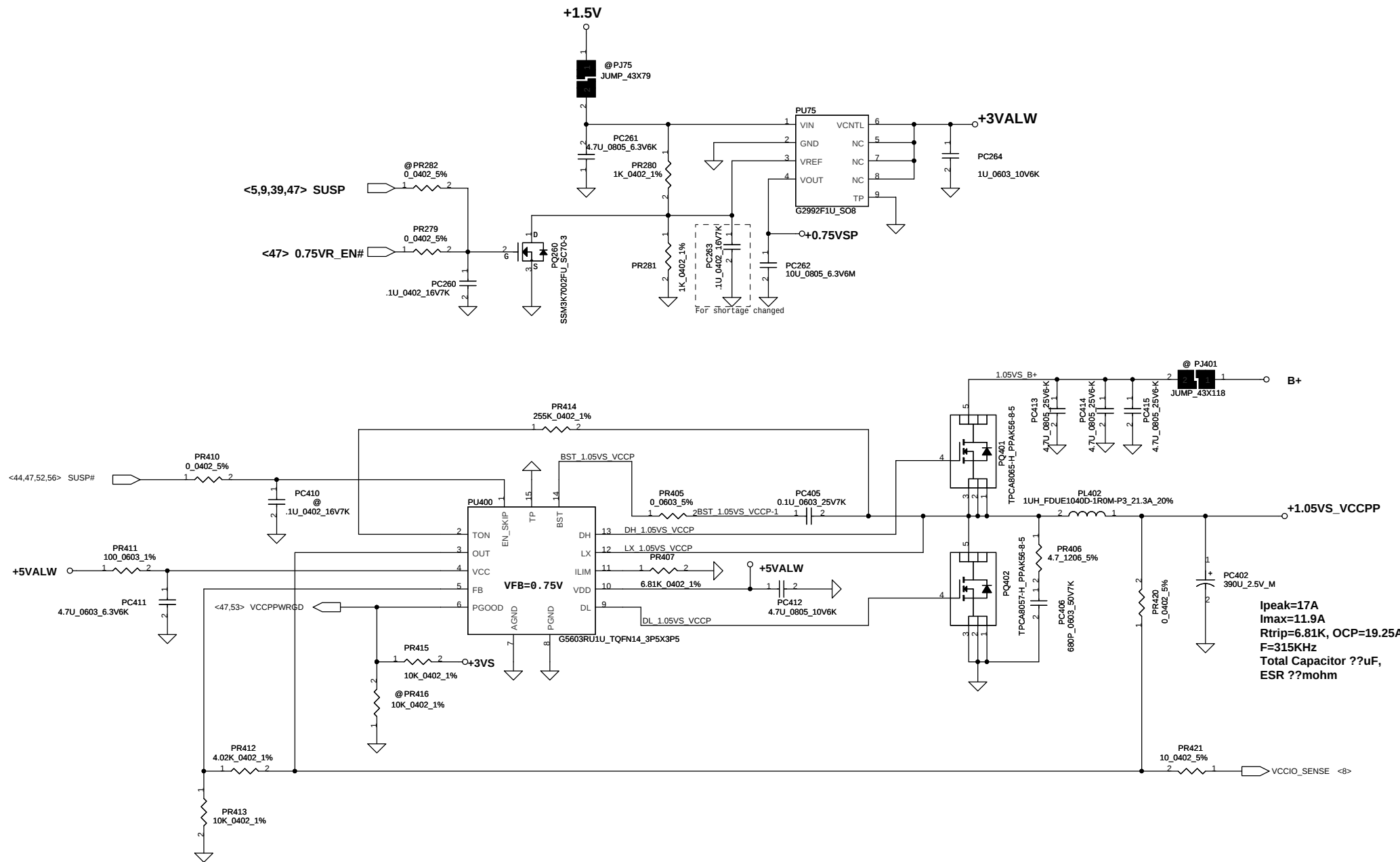


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				Document Number	Rev B
				Date	Monday, February 28, 2011
				Sheet	51 of 59

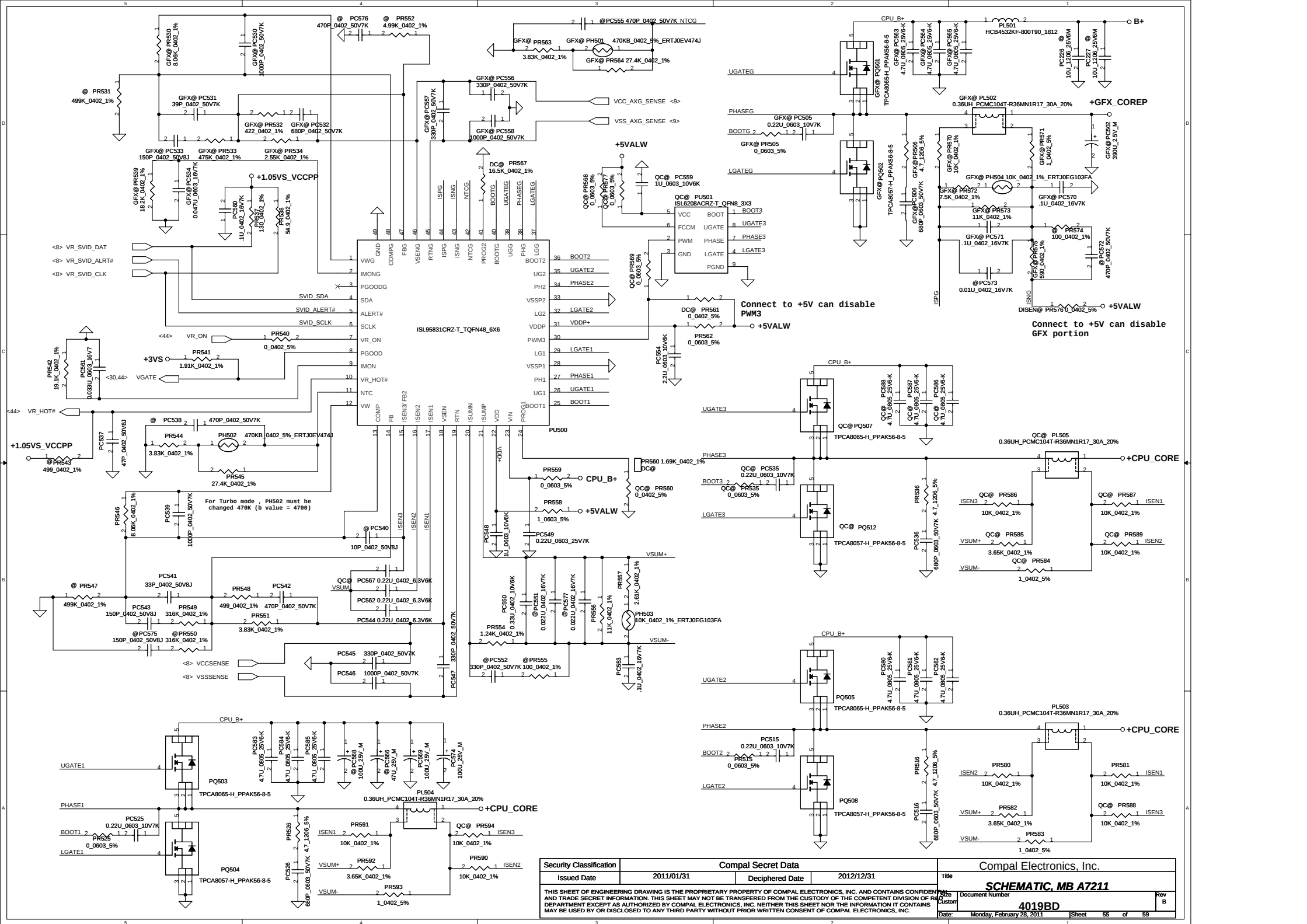


Ipeak=6A
Imax=4.2A
Rtrip=14.3K, OCP=7.69A
F=315KHz
Total Capacitor ??u
ESR=??mohm

VID1	+VCCSAP
1	0.8V
0	0.9V



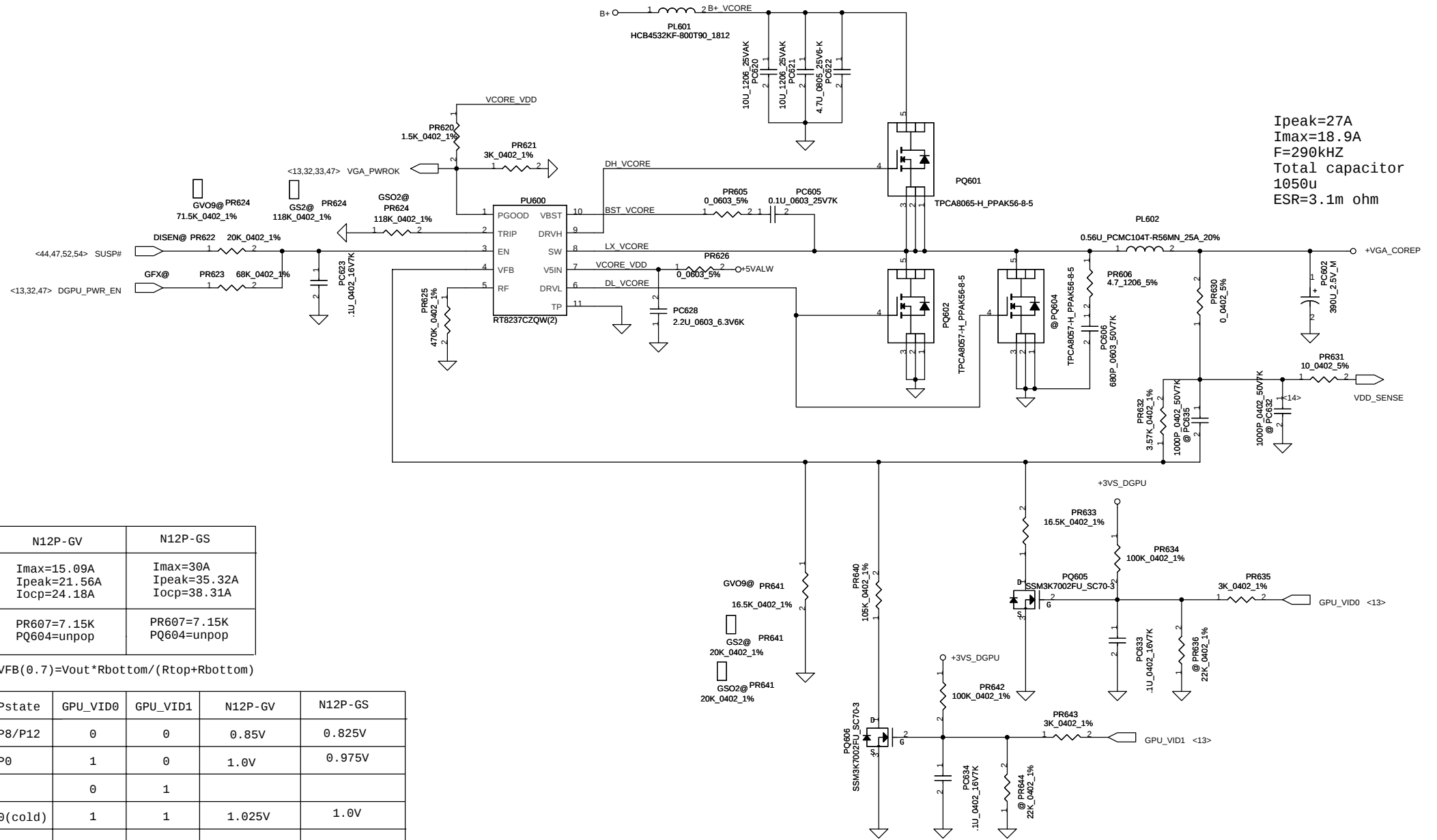
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				Document Number	4019BD
				Date	Monday, February 28, 2011
				Sheet	54 of 59
				Rev	B



N12P-GV	N12P-GS
I _{max} =15.09A I _{peak} =21.56A I _{ocp} =24.18A	I _{max} =30A I _{peak} =35.32A I _{ocp} =38.31A
PR607=7.15K PQ604=unpop	PR607=7.15K PQ604=unpop

$$VFB(0.7) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$$

Pstate	GPU_VID0	GPU_VID1	N12P-GV	N12P-GS
P8/P12	0	0	0.85V	0.825V
P0	1	0	1.0V	0.975V
	0	1		
P0(cold)	1	1	1.025V	1.0V
			PR632=3.57K PR641=16.5K PR633=16.5K PR640=105K	PR632=3.57K PR641=20K PR633=16.5K PR640=105K



I_{peak}=27A
I_{max}=18.9A
F=290kHz
Total capacitor
1050u
ESR=3.1m ohm

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										SCHEMATIC, MB A7211	
										4019BD	
										Date: Monday, February 28, 2011	
										Sheet 56 of 59	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	
	2010/10/23	P49	Change PR29 to 100K,Delete PQ7	Circuit modify
	2010/10/23	P50	Change PQ204 to A04409L,PR210 to 200K ohm,PR211 to 47k ohm	Circuit modify
			Change PQ212 to SB00000E000,delete PQ218 ,add PR206,PC206	
			Change PR222 to 53.6K ohm,PR223 to 20k ohm for L01	
	2010/10/23	P51	Change PQ360 to SB00000E000	Circuit modify
	2010/10/23	P52	Change PR157 to 6.04K ohm,PQ151 to TPCA8065,PQ603 TPCA8057	Circuit modify
			Change PL152 to 1UH,add PR156,PC156	
	2010/10/23	P53	Change PC452 to 220U_4.3mm height,add PR456,PC456	Circuit modify
	2010/10/23	P54	Change PQ401 to TPCA8065,PQ402 TPCA8057,add PR406,PC406	Circuit modify
	2010/10/23	P55	Add 3rd phase function,PC569,PC574,delete PC568,PC566	Circuit modify
			Change All high side to TPCA8065,all low side to TPCA8057	
			Add GFX function for L01,L03,add all sunnber	
	2010/10/23	P56	Add VGA_CORE function	Circuit modify
	2010/11/29	P48	Disable Pre charge function	Circuit modify
	2010/11/29	P49	Change PR22 to 3.48K Ω ,PR28 to 30.9K Ω ,PR27,PR31 to 100K Ω	Circuit modify
			PR20 to 17.8K Ω , add PQ7	
	2010/11/29	P50	Change PR219 to 100K Ω ,PL201 to 1UH,add PC204,PQ218	Circuit modify
			Change PR222 to 6.34K Ω ,PR234 to 3.24K Ω ,PR223 to 20K Ω	N12P-GS SKU
			Change PR222 to 53.6K Ω ,PR234 to 5.49K Ω ,PR223 to 20K Ω	N12P-GV SKU
			Add PC209,PC224	EMI request
	2010/11/29	P51	Add pc225	EMI request
	2010/11/29	P54	Change PR407 to 6.81K Ω	Circuit modify
	2010/11/29	P55	Add pc560	Circuit modify
	2010/11/29	P56	Change PR624 to 95.3K Ω ,PR632 to 3.57K Ω ,PR640 to 105K Ω	N12P-GS SKU
			PR633 to 16.5K Ω ,PR641 to 20K Ω	
			Change PR624 to 71.5K Ω ,PR632 to 3.57K Ω ,PR640 to 105K Ω	N12P-GV SKU
			PR633,PR641 to 16.5K Ω	
	2010/12/29	P49	Change PR27 to 15.8K Ω ,PR28 to 20K Ω ,PR30 to 14.7K Ω	N12P-GV SKU
			Change PR27 to 120K Ω ,PR28 to 10K Ω ,PR30 to 11K Ω	N12P-GS SKU
	2010/12/29	P50	Change PR219 to 100 Ω	Circuit modify
			Change PR222 to 10K Ω ,PR223 to 33K Ω ,PR234 to 10.7K Ω ,PR215 to 20m Ω	N12P-GV SKU
			Change PR222 to 8.25K Ω ,PR223 to 26.7K Ω ,PR234 to 4.12K Ω	N12P-GS SKU
	2010/12/29	P55	Change PC549 to 0.22U_0603_25V	Circuit modify
	2010/12/29	P56	Change PU600 to RT8237C	Circuit modify
			Change PR624 to 118K	OCP modify
	2011/02/09	P49	Change PQ219,PQ220 to SB000009610	Circuit modify
	2011/02/09	P50	Change PC209 to 4.7U_0805,PQ218 to SB000009610	Circuit modify
			Add PR246,PR247,PR248,PC223	Add ADP_V
	2011/02/09	P52	Add PR186,PC186	Circuit modify
	2011/02/09	P53	Change PC452 to 330U_4.2H	Circuit modify
	2011/02/10	P55	Change PC537 to 47P_0403	Circuit modify

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					4019BD	B
				Date:	Monday, February 28, 2011	Sheet 57 of 59

HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/10/26

Item	Date	Page	Component	Solution	Request

Base LA-6831 0929 schematic to modify					
Delete 14550@					
Delete 3G@					
Delete Felica@					
Delete UMA@					
Update ODD schematic for sub board					
Add logo board schematic					
Remove CIR and LID schematic to sub board					
Update TP Button for sub board					
Change JHDD1, JHDD2, JUSB, JLVDS, JFP, JFAN, JODD, JIR footprint for ME					
Change FAN schematic to PWM					
Modify Screw Hole for PHRAA ME					

Item	Date	Page	Component	Solution	Request

1)	10/04	44	R290, C309	Reserve RC filter on SPI_CLK	For EMI request
2)	10/04	29	C314	Reserve Reserve 10P Cap on 48MCLK_USB30	For EMI request
3)	10/04	28	C315	Reserve 10P Cap on AZ_BITCLK_HD	For EMI request
4)	10/04	11	C317, C319, C339, C340, C352, C353	Reserve 6PCS 33P cap on +1.5V	For EMI request
5)	10/04	40		LAN_R_GND change to GND	For EMI request
6)	10/04	25	D84	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
7)	10/04	38	D82	Change ESD diode (D82) BOM to SC300000100	For ESD request
8)	10/04	37	D85, D86, D87	Reserve ESD diode and close to the connector	For ESD request
9)	10/04	43	DA6, DA7	Change P/N and add ESD diode(D84) BOM to SCA00001A00	For ESD request
10)	10/04	46	D83	Change ESD diode (D83) BOM to SCA00000E00	For ESD request
11)	10/04	32	C516	Reserve C516 on PLT_RST#	For ESD request
12)	10/05	38	JFP	Change footprint to P-TWO_161011-04021	For ME request
13)	10/06	27	L8,L9,L10,L11	Change Common mode choke to SM070000K00	For EMI request
14)	10/06	42	DT2	Change to SC600001600	For ESD request
15)	10/06	42	DT4	Add DT4	For ESD request
16)	10/06	25	R267,R268,R269 R270,R283,R333 R337,R329	Co-lay with optimus support 2-CH panel	For SPEC design ready
17)	10/09	25		Change JLVDS PIN define	For HW4 common design
18)	10/12	25		Change JLVDS PIN define	For layout request
19)	10/12	34	L22,C509	Change to test point T30	On-die VR default support
20)	10/12	34	R483,C280	Change to test point T36	On-die VR default support
21)	10/12	35	R498	Change to test point T41	On-die VR default support
22)	10/12	35	L20,C302	Change to test point T42	On-die VR default support
23)	10/12	35	L17,C296	Change to test point T43	On-die VR default support
24)	10/12	34	R541,R474,R480 R509,R517,R520	Change size to 0402	For layout request
25)	10/12	46		Change LID +3VALW to +3VL	
26)	10/12	06		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
27)	10/12	13		Change PEG AC coupling caps from 0.22uF to 0.1uF(SE076104K80)	For NVDIA suggest
28)	10/12	09	R122,R252	Change from 100 ohm to 1k ohm	For HW4 schematic review
29)	10/12	09		Add +1.5VS to PJ30 and	For HW4 schematic review
30)	10/12	09		Change +1.5V from PJ30 to Q33	For HW4 schematic review
31)	10/12	29	R564	Change to @	For HW4 schematic review
32)	10/12	33	R124	Delete	For HW4 schematic review
33)	10/12	33	R444	Change BOM structure to mount	For HW4 schematic review
34)	10/12	05		Delete XDP function and change to test point	For layout space
35)	10/12	28		Delete PCH SPI schematic	For layout space
36)	10/12	37		Swap JPIO PIN define	
37)	10/12	42		Swap LT4	For layout request
38)	10/12	05		Update FAN control schematic	For HW4 schematic review
39)	10/12	40	CL43, CL44	Add CL43, CL44	For EMI request
40)	10/12	40	CL683,CL684	Delete CL683,CL684	For layout space
41)	10/12	42	JUSB30	Change to LOTES_AUSB0003-P001C	For ME request
42)	10/14	37	JHDD2	Change to ACES_88058-120N	
43)	10/14	46	H26,H28,H29	Delete	For ME last drawing
44)	10/14	46	H1-H7	Update screw hole	For ME last drawing
45)	10/14	38	L57	Swap L57	For layout request
46)	10/18	37	D86	Swap D86	For layout request
47)	10/18	25	D84	Change D84 BOM structure to install	For ESD request
48)	10/18	43	DA6,DA7	Change DA6,DA7 BOM structure to install	For ESD request
49)	10/18	46	C479,C482,C483 C484,C495,C496 C499,C500,C509 C517,C520	Reserve 0.1u Cap	For ESD request

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Date:	Monday, February 28, 2011	Sheet	58	of	59

HW PIR (Product Improve Record)

PHRAA LA-7211P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0

GERBER-OUT DATE: 2011/01/31

NO DATE PAGE MODIFICATION LIST

PURPOSE

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50)	10/20	29	R228	Change R228 from10k to 1k ohm	For Intel spec demand
51)	10/20	41	CC23	Mount CC23	For vendor demand
52)	10/20	44	R172	Change to @ due to the pull high will be in Cap sensor board	
53)	10/20	47	C493	Change C493 from 0.01uF to 0.1uF	To avoid inrush current.
54)	10/25	37	JHDD2	Swap JHDD2	For sub board
55)	10/25	14	RV114, RV115		For NV schematic
56)	10/25	16	RV480, RV481		
57)	10/25	24	RV107, RV109		
			RV116, RV117		
58)	10/26	38	QB4	Change QB4 from SB211970110 to SB00000R300	For sourcer demand
59)	10/26	39	U5	Change U5 from SA000045Z00 to SA00004GV00	For design change
60)	11/12	28	+3V_SPI	Change +3V_SPI to +3VS	For EVT issue
61)	11/12	44	R290	Mount R290	For EVT issue(88)
62)	11/12	11	C317, C319, C339	Mount this part for DDR +1.5V return path	
			C340, C352, C353		
63)	11/12	46	C522-C526	Mount this part	For EMI request
64)	11/12	39	D24	Remove D24	For SUSP# leakage
65)	11/12	28	CV228, CV229	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV230, CV231		
66)	11/12	21	CV232, CV233	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV234, CV235		
67)	11/12	22	CV236, CV237	Add VRAM +VRAM_1.5VS power rail	For NV demand
			CV238, CV239		
68)	11/12	44		Change EC GPXI0D04 from SLP_CHG# to OTP_HW	For PWR demand
69)	11/12	44	D26, R359	Add for OTP_HW function	For PWR demand
70)	11/12	44	R1428, R439	Remove for SLP_CHG#	For PWR demand
71)	11/12	26	T75, T76	Add test point at JCRT pin4, pin11	For CIC demand
72)	11/12	39	Q39, Q40	Add Q39, Q40	For avoid SUSP# leakage
73)	11/21	46	JPOWER	Reverse JPOWER pin define	
74)	11/21	37	JHDD2	Reverse (vertical and horizontal) JHDD2 pin define	
75)	11/21	46	H8, H9	Change H8&H9 to 3P3	
76)	11/25	42	LT1, LT2	Change to SM070001U00	For EMI request
77)	11/25	40	CL37, CL38	Remove CL37 and change CL38 from 4.7U to 220P	For EMI request
78)	11/25	40	LL4-LL11	Reserve LL4-LL11	For EMI request
79)	11/25	44	R383	Delete R383	For HW4 LID SW common design
80)	11/25	25, 43	C13, CA28	Add C13 and CA28	For EMI request
81)	11/25	38		Seap JIR PIN define	For common with PHQAA
82)	11/25	46	C484, C495, C527	Reserve 0.1u Cap	For ESD request
83)	11/25	40	CL484-CL487	Add CL484-CL487 to 0.1 cap	For EMI request
84)	12/28	42	UT1	Change P/N to SA000048H00	
85)	12/28	25	R131	Add R131 for Sumsong panel issue	For panel issue
86)	12/28	44	R383	Add R383	For HW4 LID SW common design
87)	12/28	35	C333, C515	Change C333, C515 to 10uF	For HW4 cost down plan
88)	12/28	37	C426	Change C426 BOM structure to @	For HW4 cost down plan
89)	12/28	44	R398, U44, C818	Add R398 and change U44, C818 BOM structure to @	For HW4 cost down plan
90)	12/29	35	L19, L21	Change L19, L21 to SM010028400	For HW4 cost down plan
91)	12/29	37	C375-C378	Add C375-C378 on ODD fuction	
92)	12/29	37	C360	Add C360	For ESD request
93)	12/29	44	R475, R738, R739	Add R475, R738, R739	For 0012 co-lay
94)	01/19			Change D9, D55, D61, D7, D8, D12, D14, D16, D21, D26, D25 to SCS00000Z00	
95)	01/19	05	D88	Change D88 to SC100001M00	
96)	01/19			Change U2 P/N to SA000004EE00	
97)	01/19	25	R307	Change R307 BOM structure to @	For 3D panel brightness issue
98)	01/19	08	C890, C894	Delete C890, C894	For power request
99)	01/19	08	C890	Change C891 to SGA20331E10	For power request
100)	01/19	08	C2, C7	Add C2, C7	For power request
101)	01/19	09		Change C873 to C112	For low ESR to pass transient
102)	01/19	25	R131	Change R131 to 47K	For 3D panel brightness issue
103)	01/19	32	R399	Change R399 BOM structure to @	For optimus device loss issue
104)	01/19	32	R544	Change R544 BOM structure to OPT@	For optimus device loss issue
105)	01/19	47	R434	Change R434 from 47K to 220K	For optimus device loss issue
106)	02/10	09	R877	Change R877 to @	For VCCSA voltage margin check ok
107)	02/10	32	R360	Add R360 to 0.1u	For ESD request
108)	02/10	46	U2	Change U2 P/N to SA00004EET0(R3 P/N) and SA00004EES0(R1 P/N)	
109)	02/10	46	UV1	Change UV1 P/N to SA000047U00(R3 P/N) and SA000047U20(R1 P/N)	
110)	02/10	46	PCB	Change PCB P/N to DAZ01700100	