

Compal Confidential

JE51/HM51/SJV51_BZ

P5WE7/P5WH7/P5WS7 Schematics Document

AMD Brazos

Brazos with Ontario / Hudson M1 / Robson XT

DIS only / UMA only / PX Muxless / PX Muxless with BACO

2010-11-29

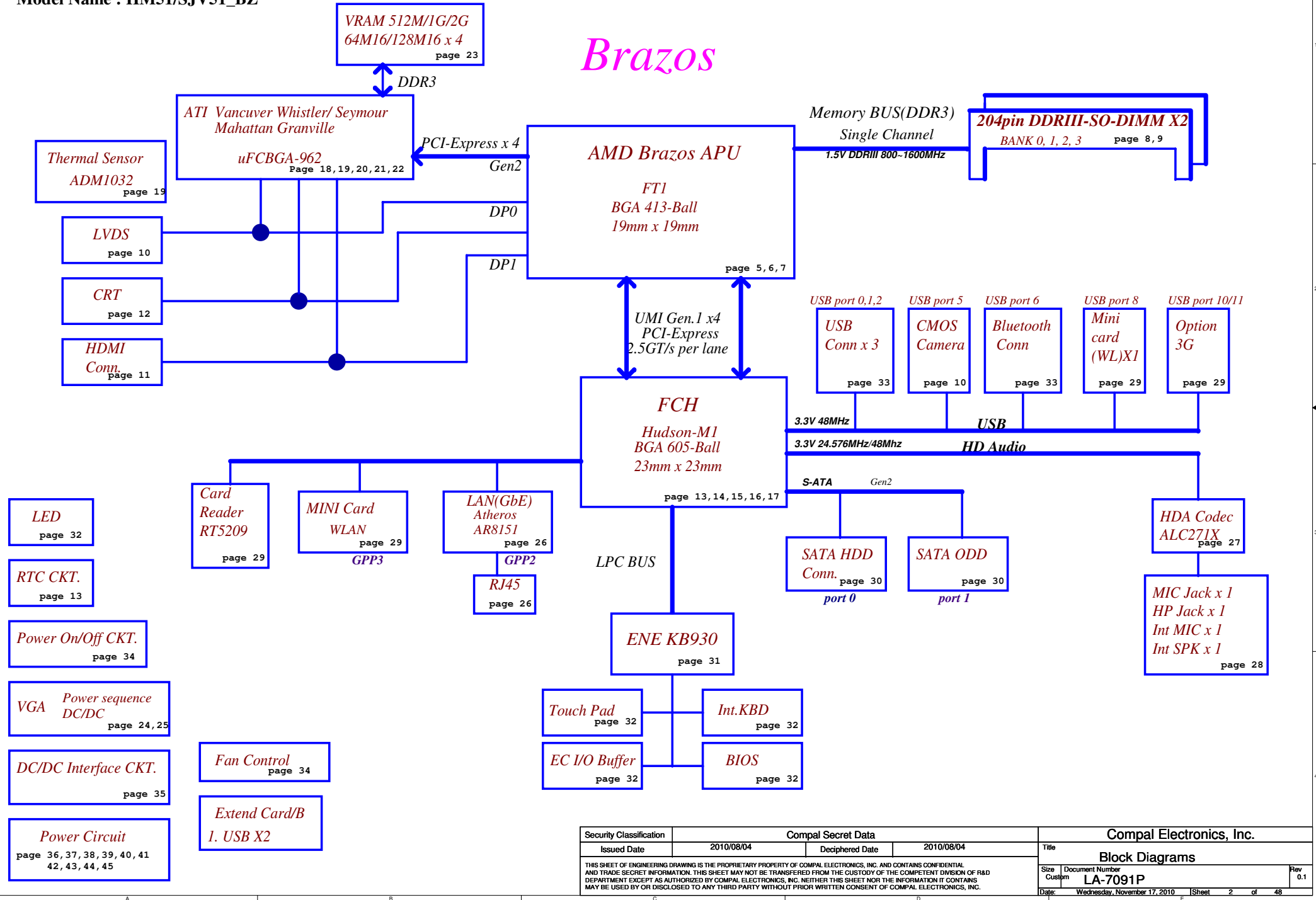
LA-7091P REV: 0.2



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Model Name : HM51/SJV51_BZ



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	NA	EMC1403-2(GPU)	1001-101xb	9EH

SM Bus Controller 0 (FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
--------	---------	-----

APU SIC/SID (FCH_SMB3)
H_THERMTRIP# (FCH_ALERT#)

SM Bus Controller 1 (FCH_SMB0)

Device	Address	HEX
--------	---------	-----

DDR DIMM1 (FCH_SMB0) 1001-000xb 90
DDR DIMM2 (FCH_SMB0) 1001-001xb 92
WLAN (FCH_SMB0)

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
	Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	EVT
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Display from APU	UMA@
Display from VGA	DISO@
Use VGA	VGA@
Muxless w/BACO	BACO@
Muxless wo/BACO	WOBACO@
Muxless	PX@
w/Vancouver Series	VAN@
w/Manhattan Series	MAN@
Bluetooth	BT@
AR8151	8151@

*UMA only : UMA@ BT@ 8151@
*DIS only : VGA@ DISO@ WOBACO@ VAN@ BT@ 8151@
*Muxless w/BACO : UMA@ VGA@ PX@ BACO@ VAN@ BT@ 8151@
Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ VAN@ BT@ 8151@

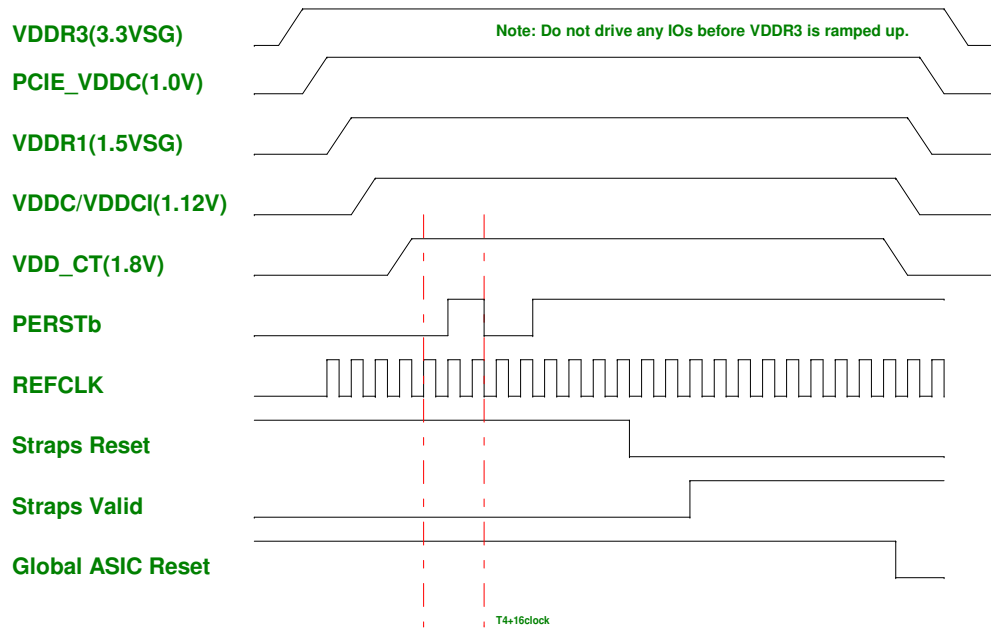
For Robson:

DIS only : VGA@ DISO@ WOBACO@ MAN@ BT@ 8151@
Muxless w/BACO : UMA@ VGA@ PX@ BACO@ MAN@ BT@ 8151@
Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ MAN@ BT@ 8151@

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Power-Up/Down Sequence

1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
2. VDDR3 should ramp-up before or simultaneously with VDDC.
3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.
4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.
5. VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



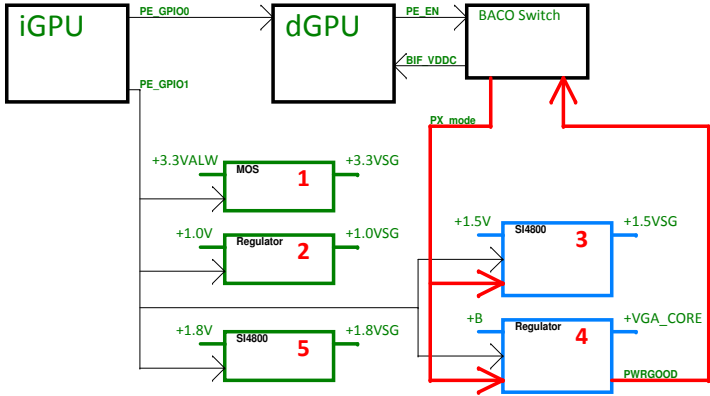
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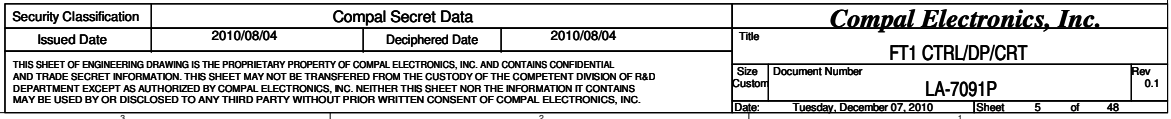
PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

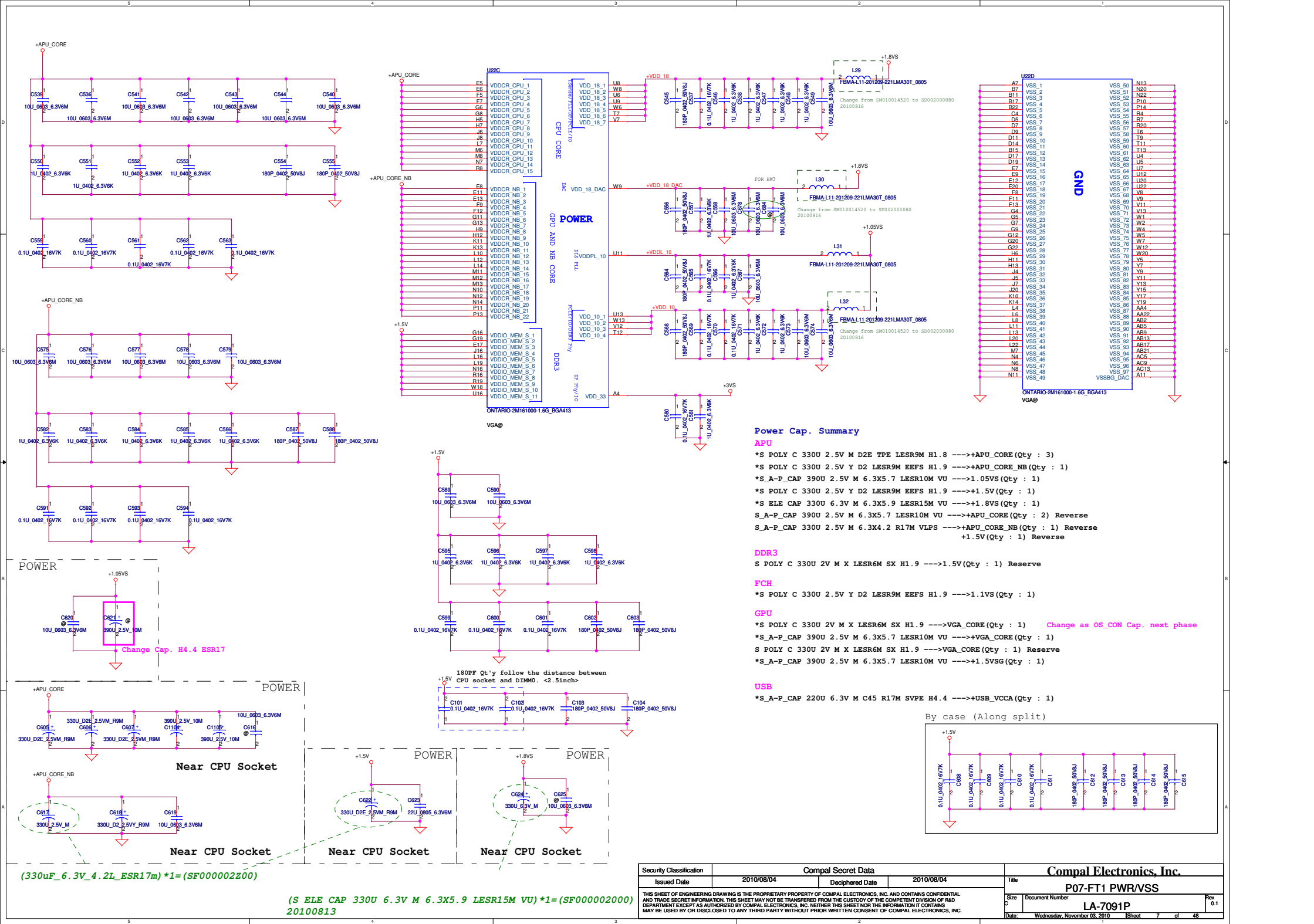
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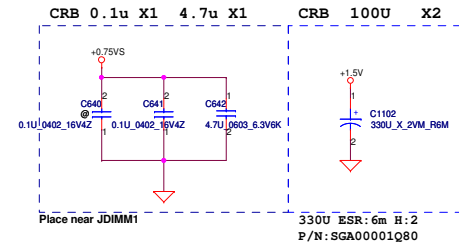
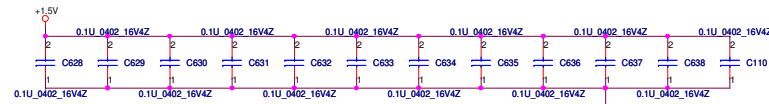
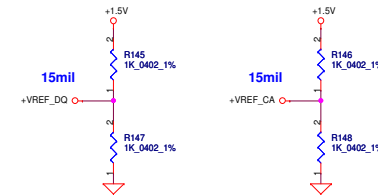
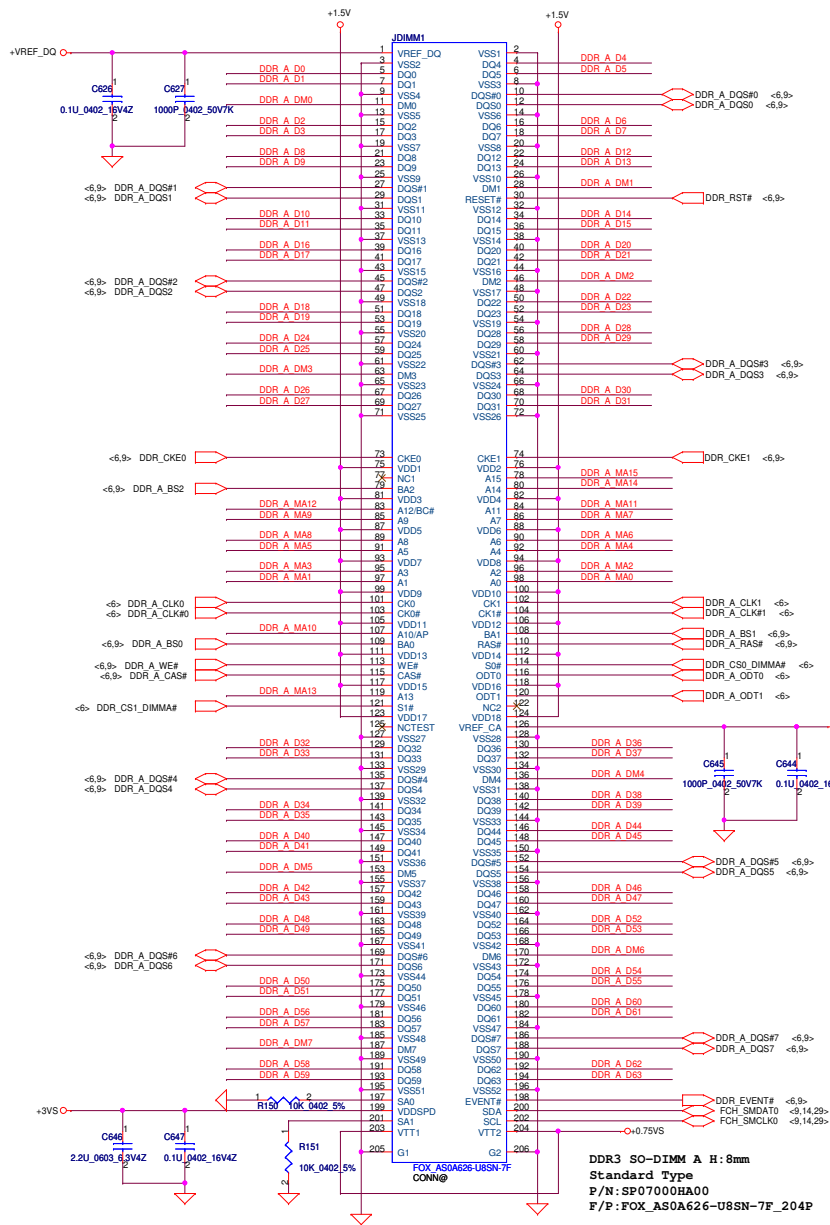
PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON (always High)

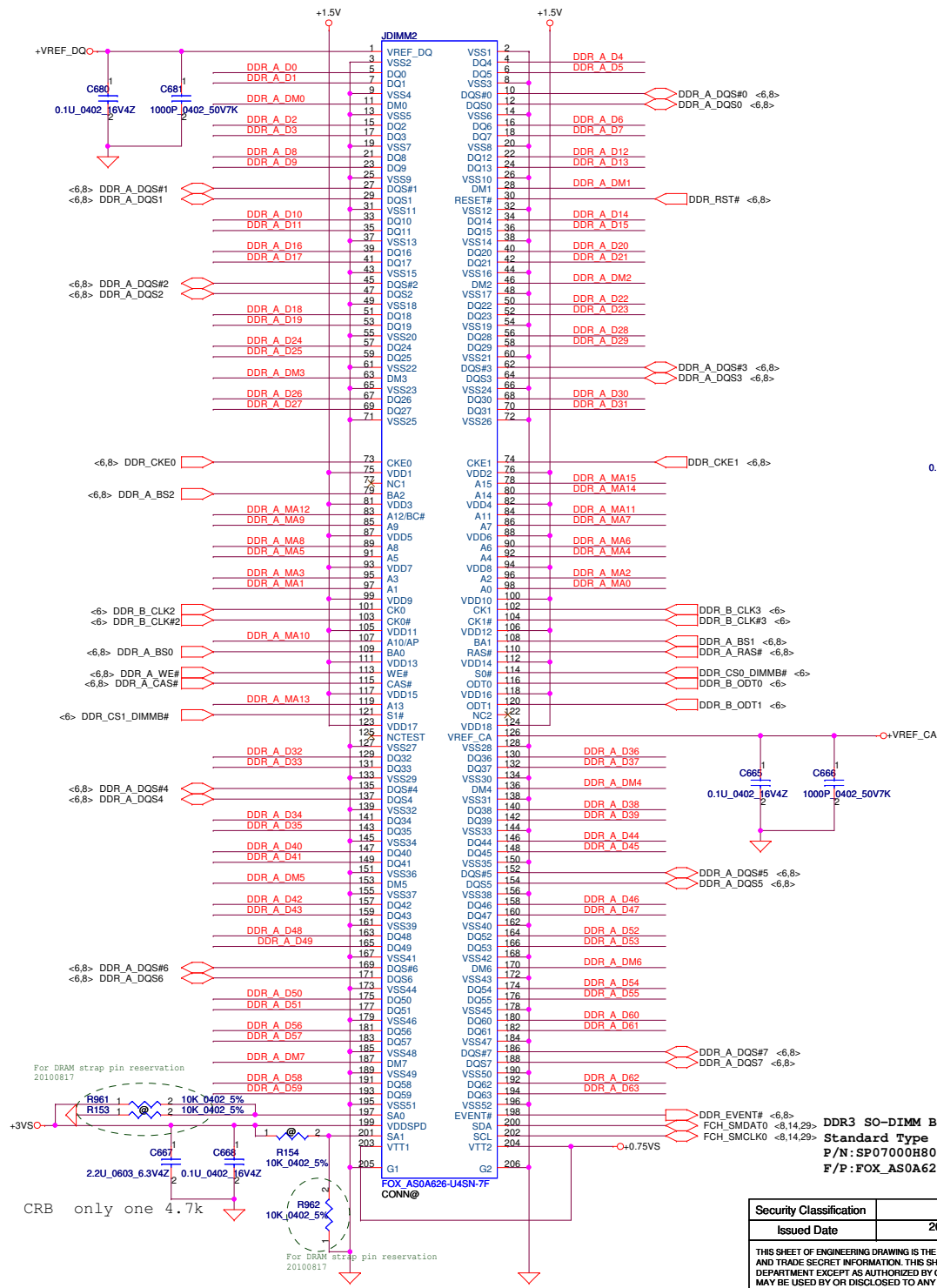
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, AZVDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



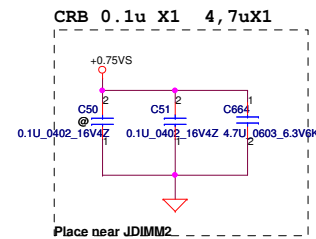
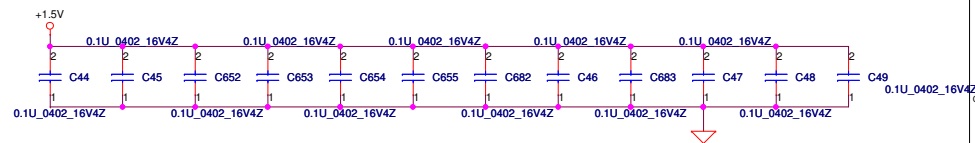








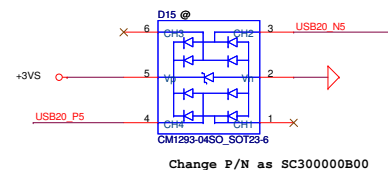
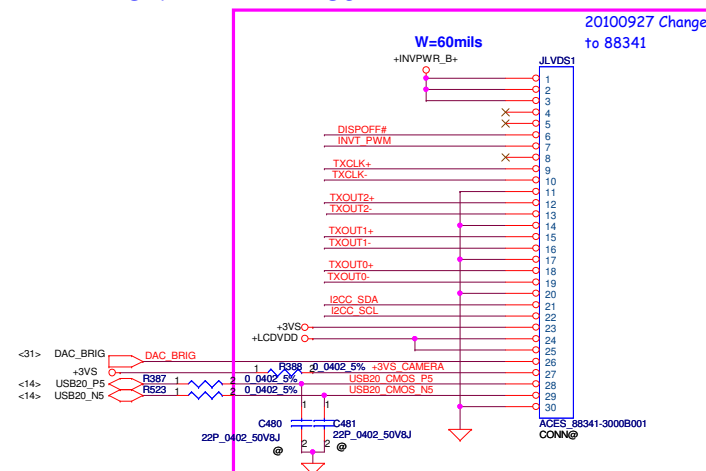
DDR A D0[.63] <6.8>
 DDR A MA0[.15] <6.8>
 DDR A DM0[.7] <6.8>



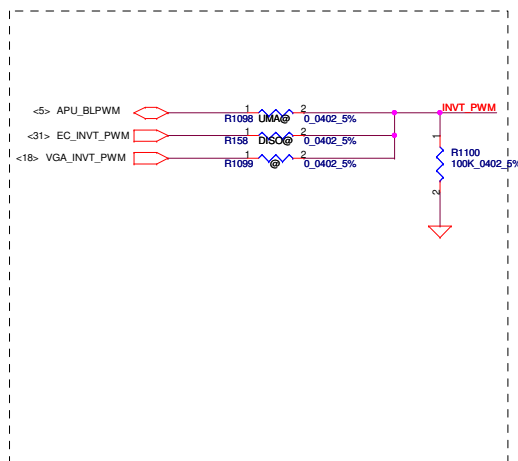
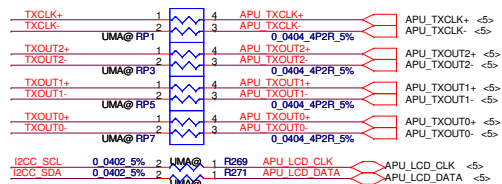
DDR3 SO-DIMM B H:4mm
 Standard Type
 P/N: SP07000H800
 F/P: FOX_AS0A626-U4SN-7F_204P

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LCD/LED PANEL Conn.

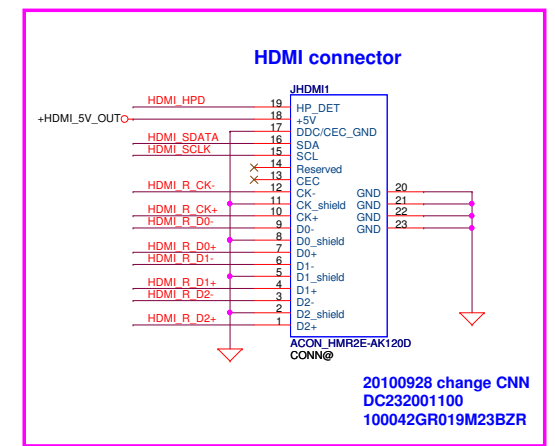
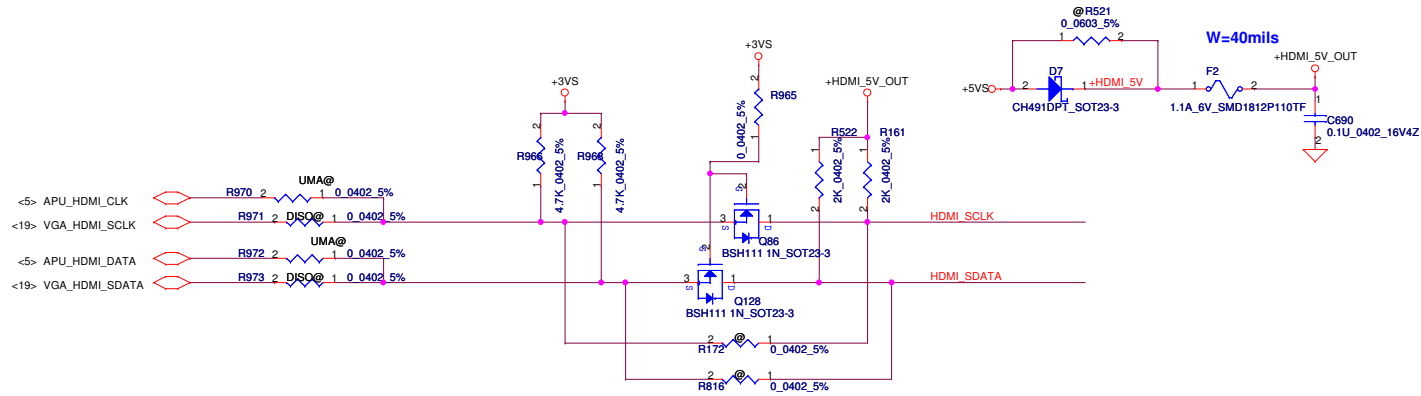


UMA ONLY



- 1.Add DISO@ and VGA path connect circuit
- 2.Remove reserve DMIC circuit

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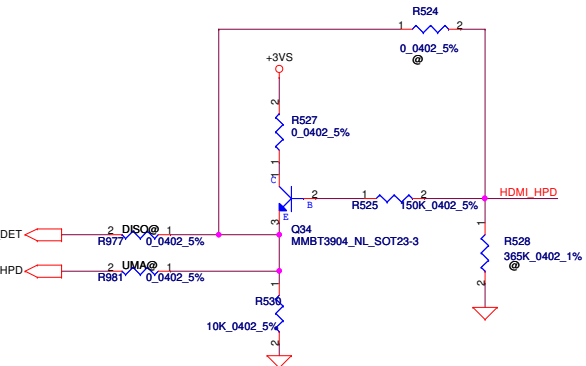
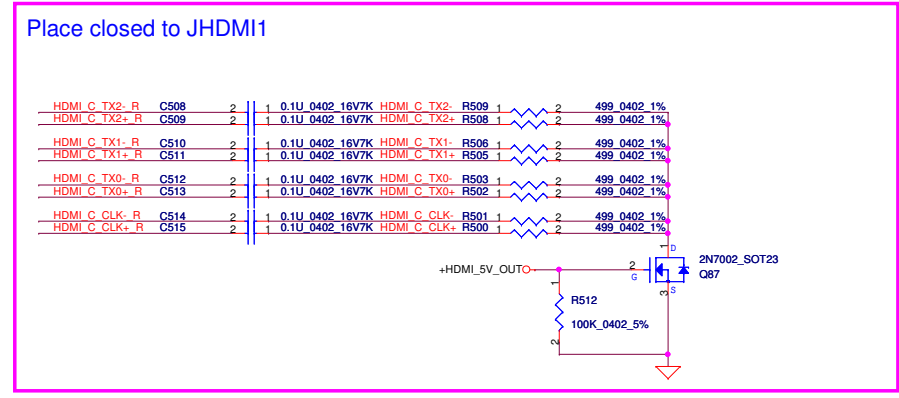
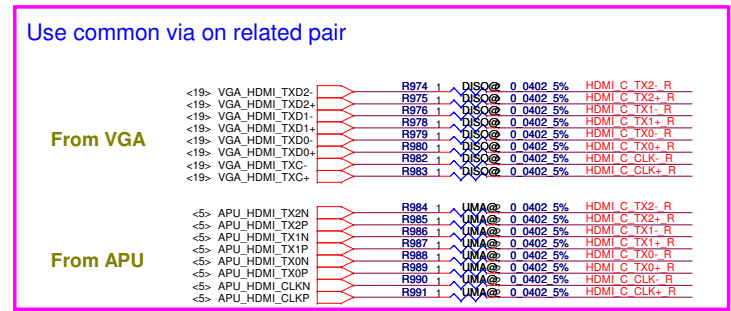
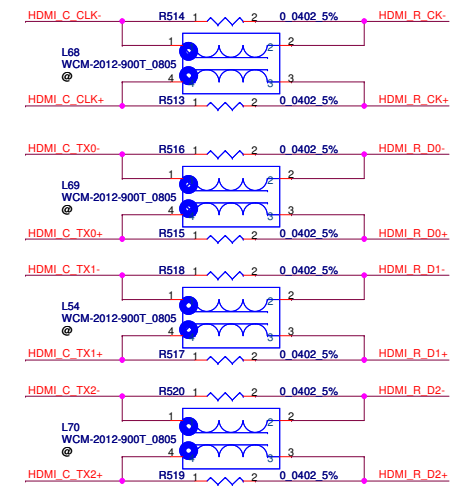


20100928 change CNN
DC232001100
100042GR019M23BZR

HDMI Function Change list For R01
1.Add DISO@ and VGA path connect circuit
2.Level Shift implement
3.Add termination resistance option

Place closed to JHDMI1

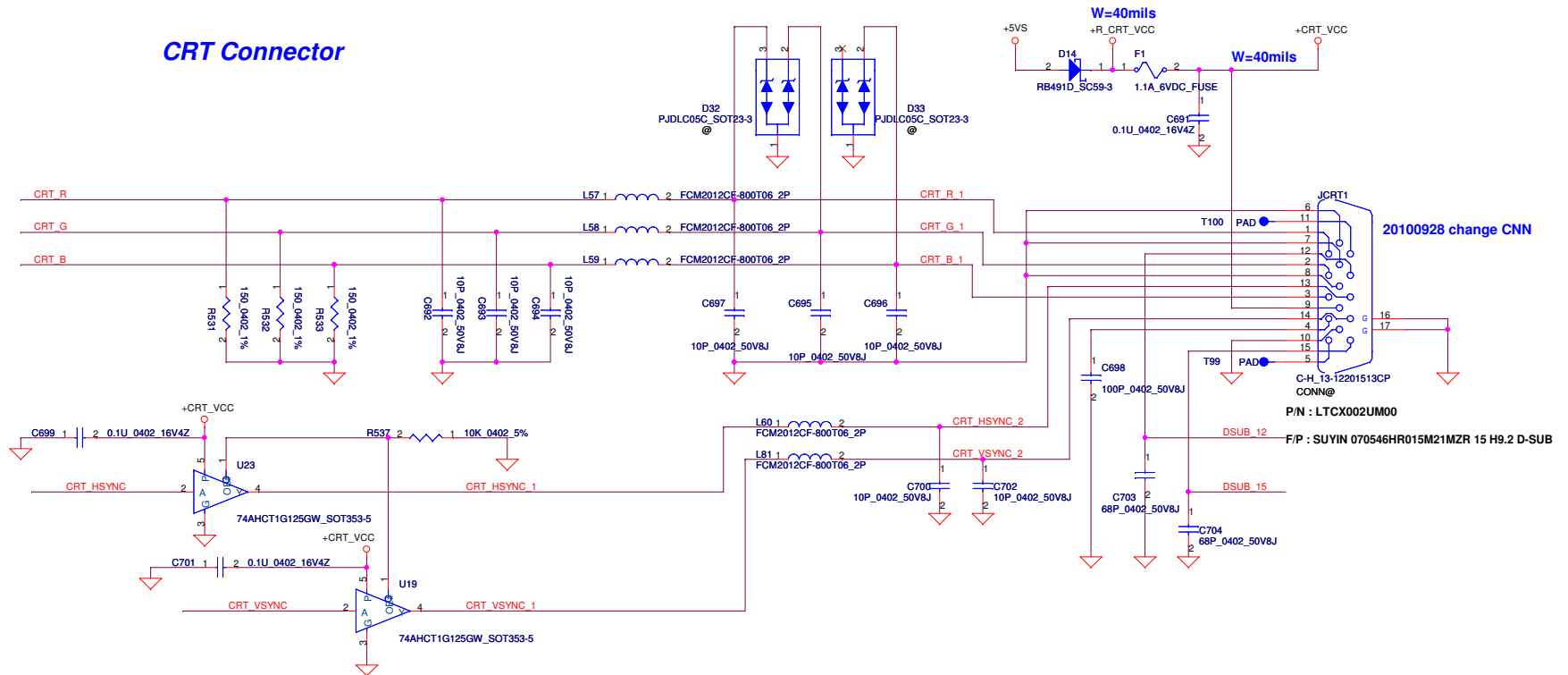
SM070001310 400ma 90ohm@100mhz DCR 0.3



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								HDMI Connector			
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CRT Connector



CRTI Function Change list For R01

1. Add DISO@ and VGA path connect circuit
2. Level Shift implement

Use common via on related pair

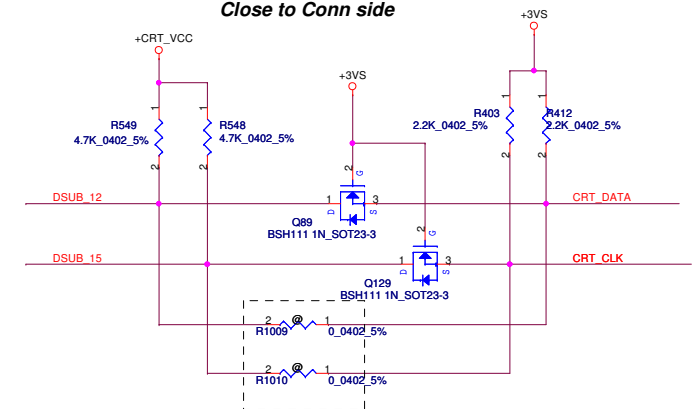
From APU

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<5> APU_CRT_B	APU_CRT_B	R997	2	UMA@	1	0.0402 5%	CRT_B
<5> APU_CRT_HSYNC	APU_CRT_HSYNC	R998	2	UMA@	1	0.0402 5%	CRT_HSYNC
<5> APU_CRT_VSYNC	APU_CRT_VSYNC	R999	2	UMA@	1	0.0402 5%	CRT_VSYNC
<5> APU_CRT_DDC_SDA	APU_CRT_DDC_SDA	R1000	2	UMA@	1	0.0402 5%	CRT_DATA
<5> APU_CRT_DDC_SCL	APU_CRT_DDC_SCL	R1001	2	UMA@	1	0.0402 5%	CRT_CLK

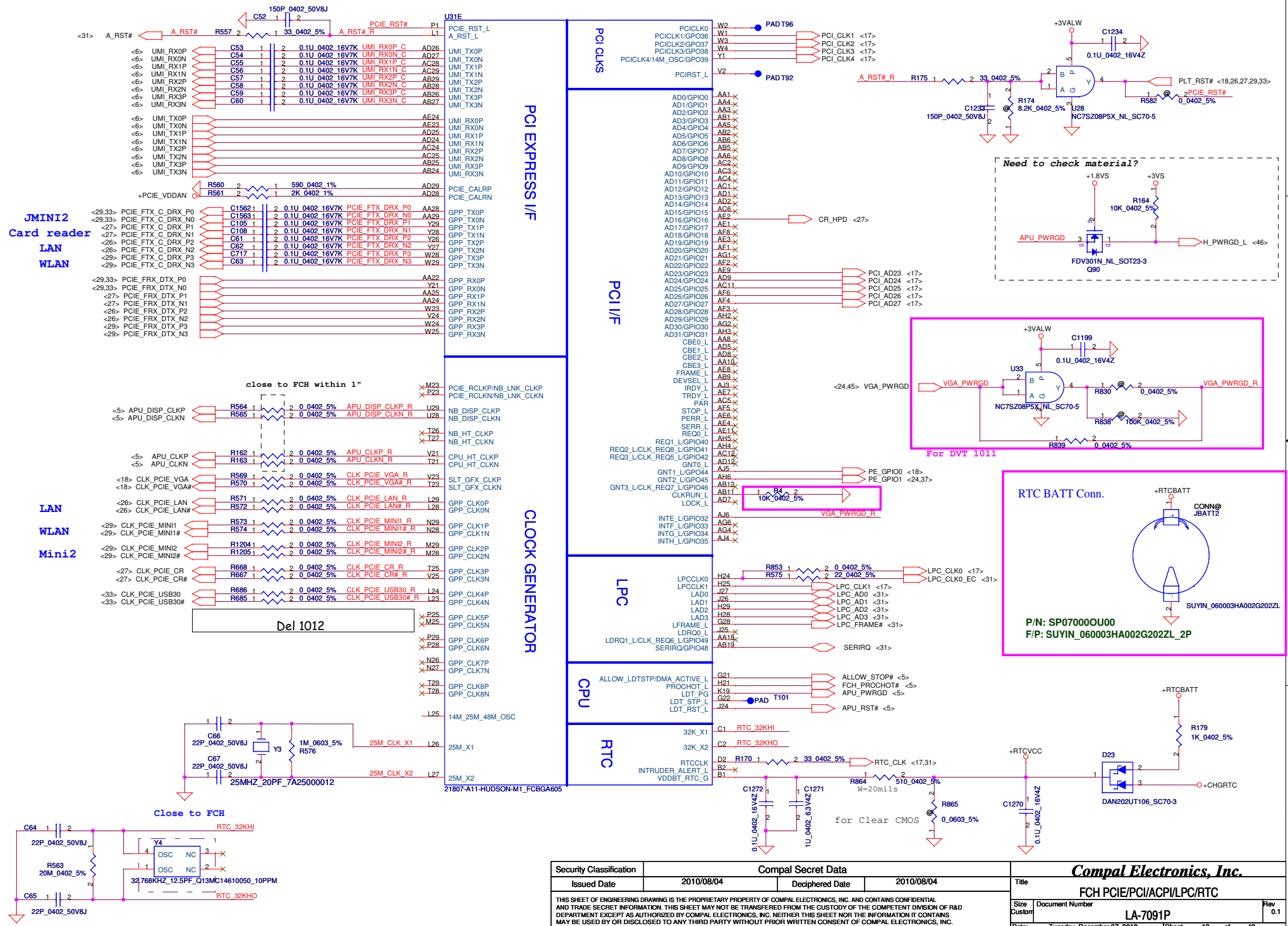
From VGA

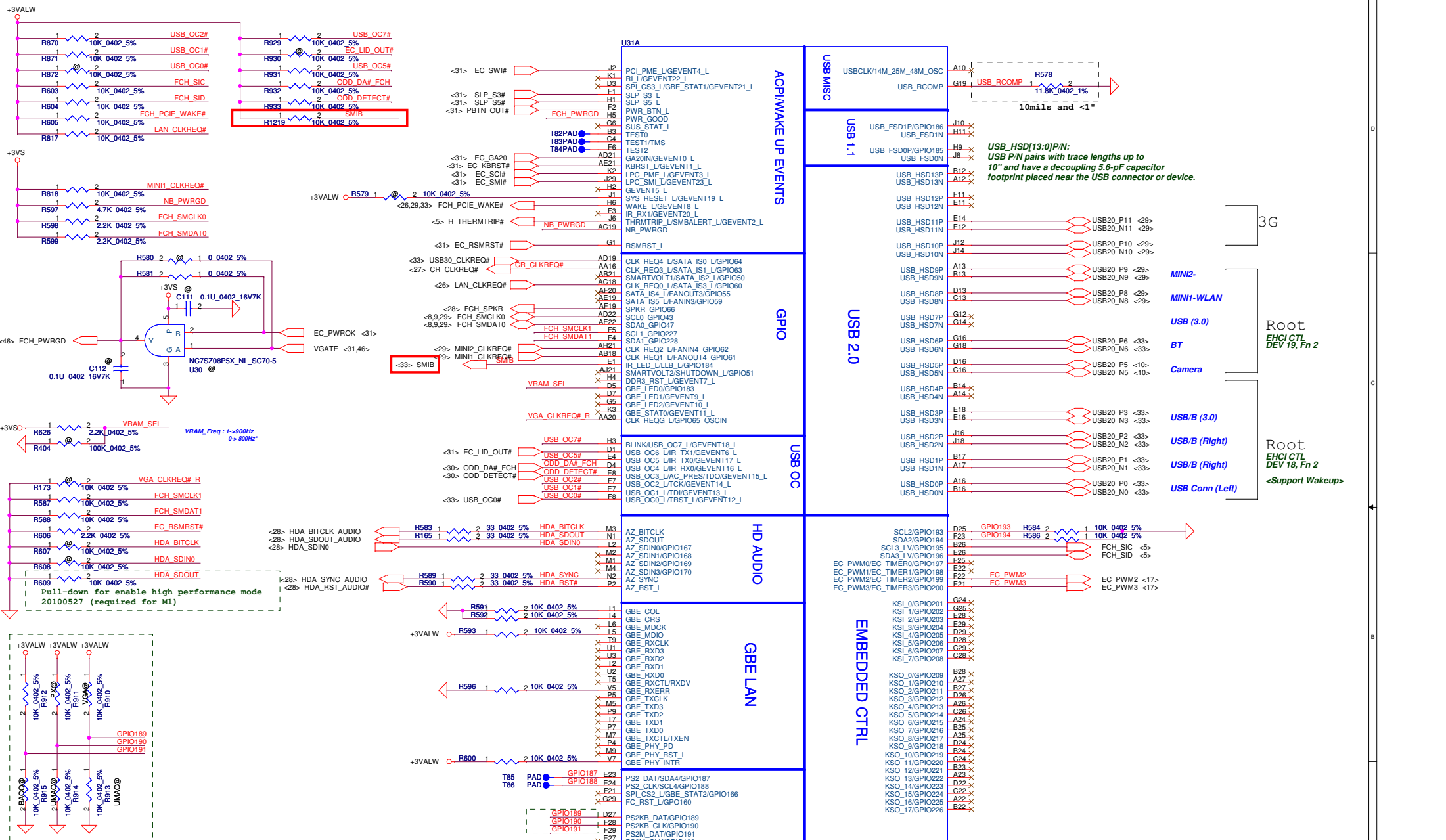
<19> VGA_CRT_R	VGA_CRT_R	R1002	2	DISO@	1	0.0402 5%	CRT_R
<19> VGA_CRT_G	VGA_CRT_G	R1003	2	DISO@	1	0.0402 5%	CRT_G
<19> VGA_CRT_B	VGA_CRT_B	R1004	2	DISO@	1	0.0402 5%	CRT_B
<19> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R1005	2	DISO@	1	0.0402 5%	CRT_HSYNC
<19> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R1006	2	DISO@	1	0.0402 5%	CRT_VSYNC
<19> VGA_CRT_DATA	VGA_CRT_DATA	R1007	2	DISO@	1	0.0402 5%	CRT_DATA
<19> VGA_CRT_CLK	VGA_CRT_CLK	R1008	2	DISO@	1	0.0402 5%	CRT_CLK

Close to Conn side

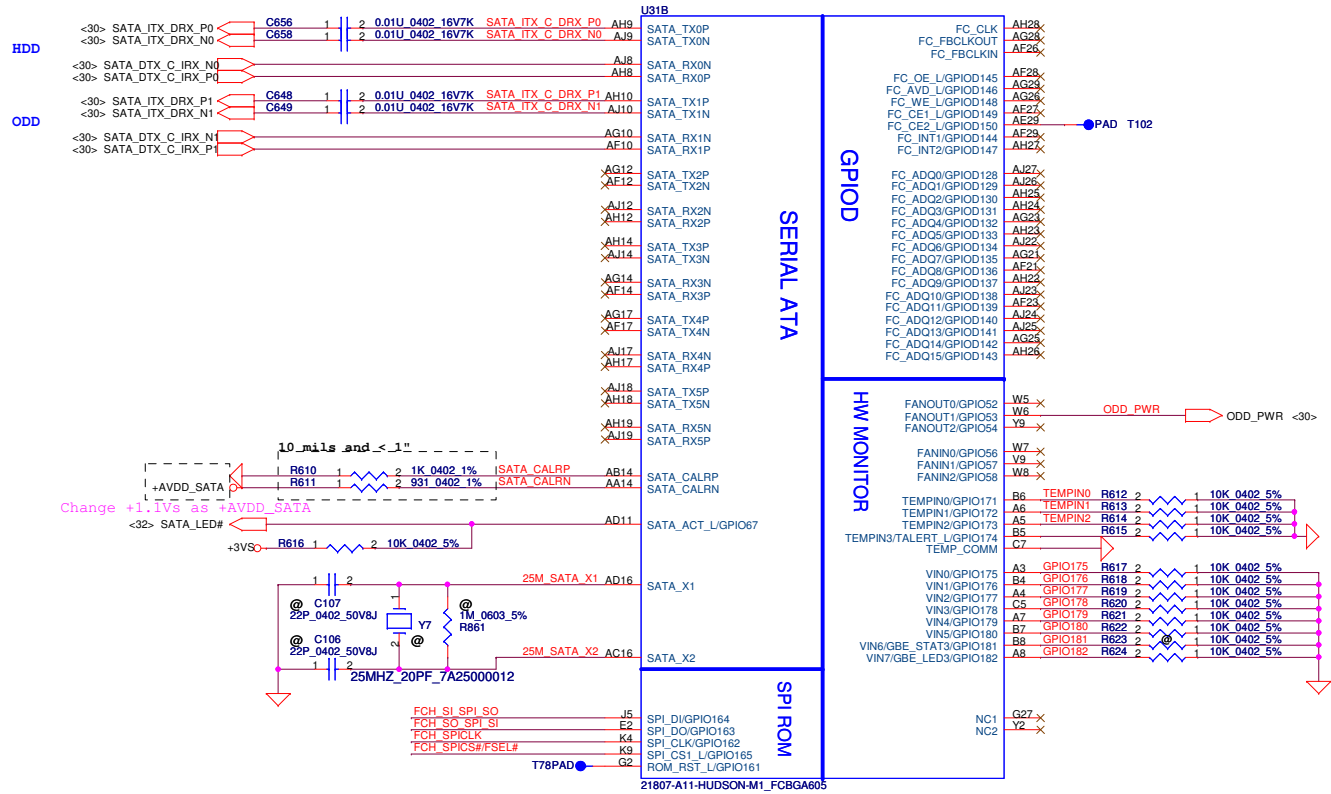


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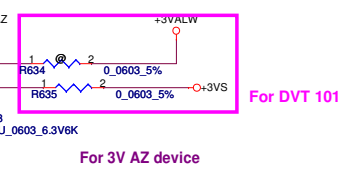
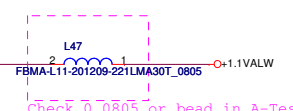
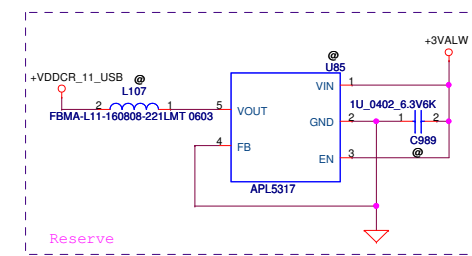
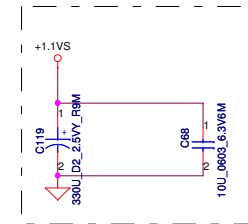
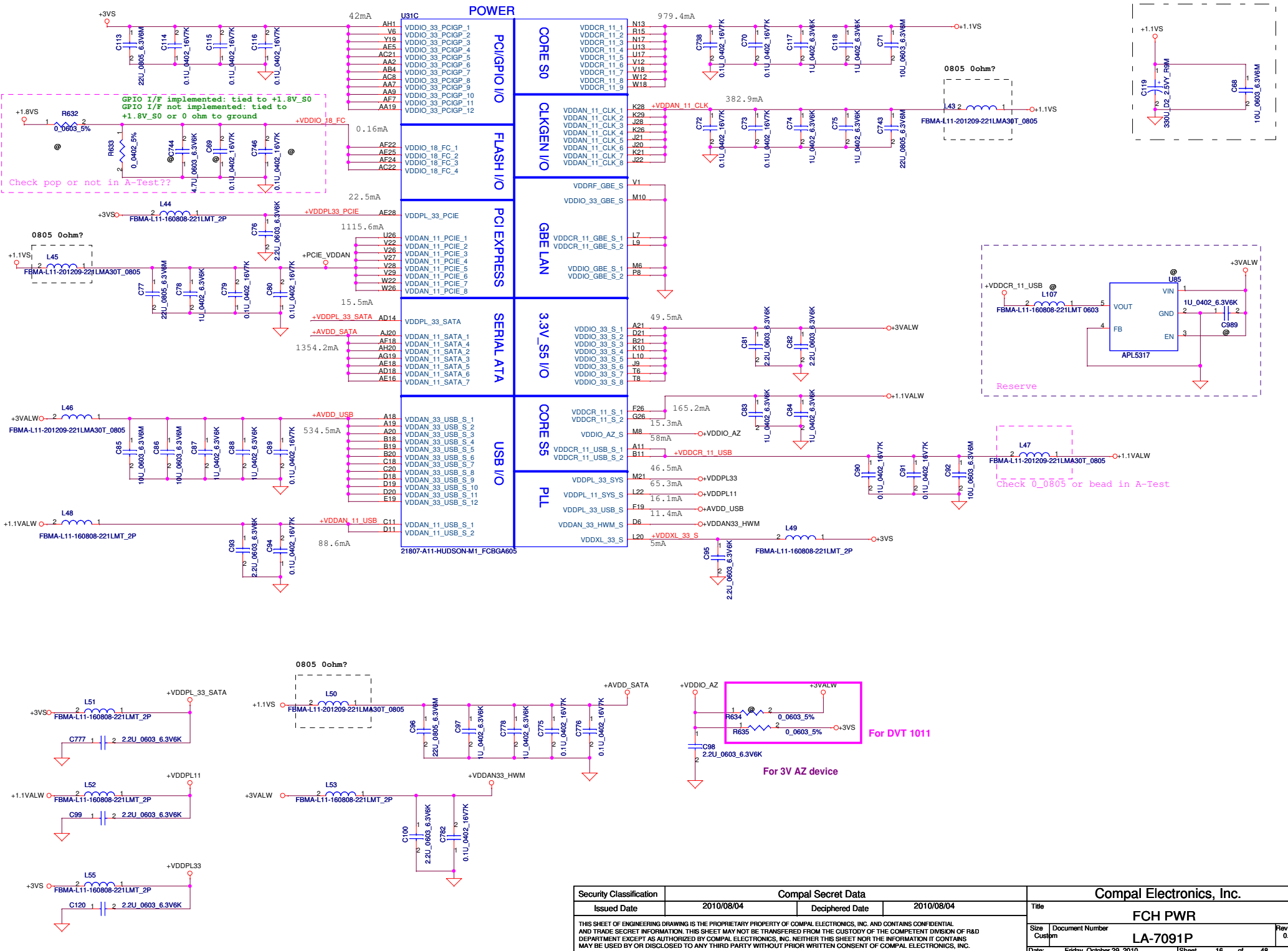


BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	1	UMA
	1	0	1	DIS
	1	1	1	PX3
	1	1	0	PX4



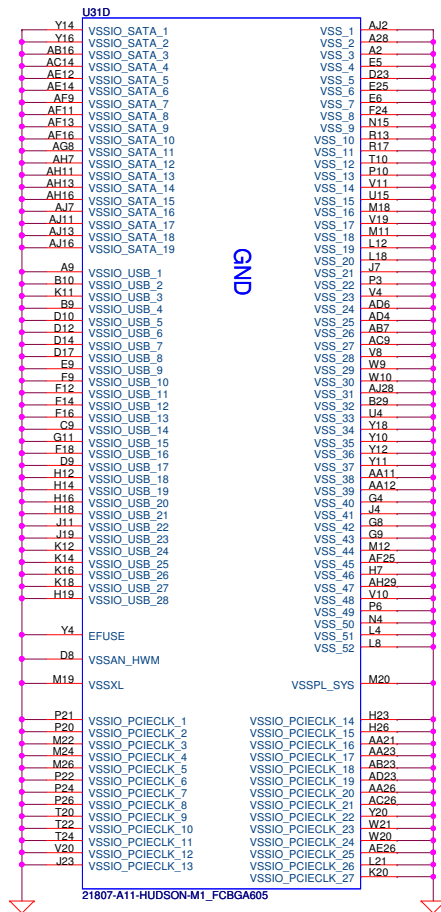
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Deciphered Date				2010/08/04				FCH-SATA/SPI			
Size				Document Number				Rev			
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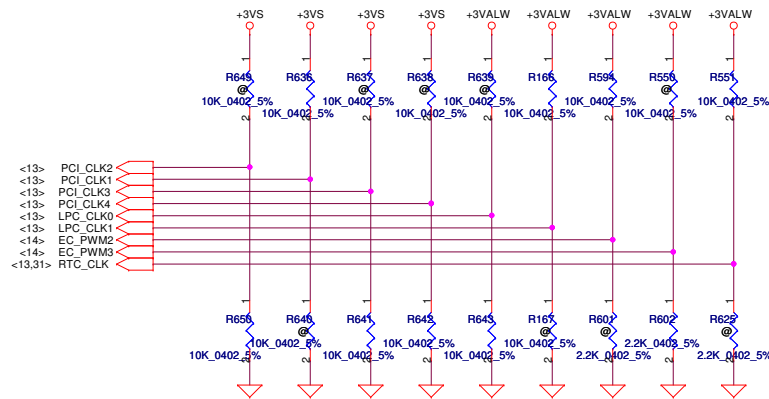
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REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2	EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	Internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H,L) DEFAULT	
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	Internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)	



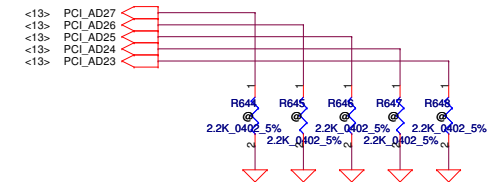
DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

check default



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				Size	Document Number	Rev
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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN (GENLK_VSYNC)	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver will ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on
Whistler and Seymour

NC on Park,
Robson and Seymour

NC on Park and Robson

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Robson and Seymour

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Robson and Seymour

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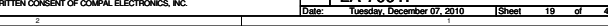
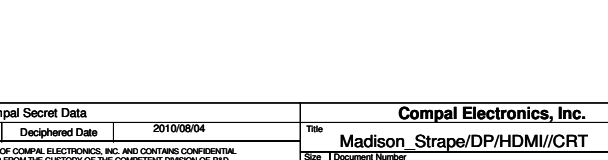
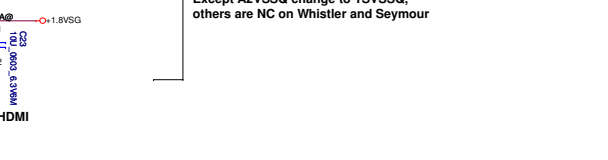
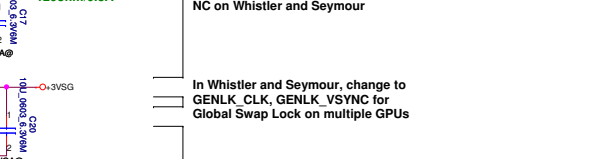
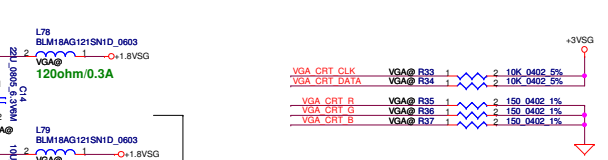
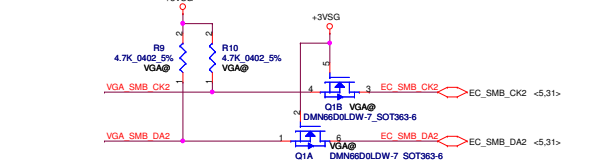
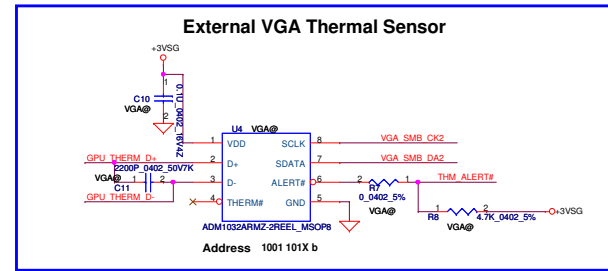
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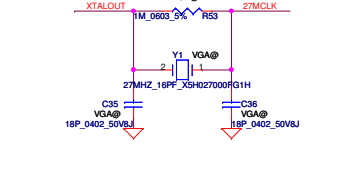
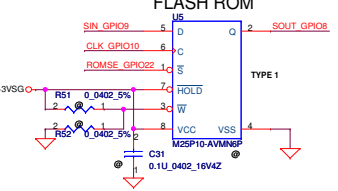
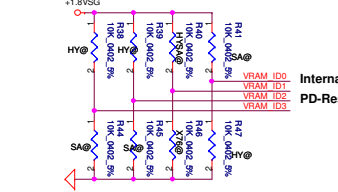
NC on Park,
Robson and Seymour

NC on Park,
Robson and Seymour



Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM	<vendor>			
Hynix (512M)	1	1	1	0
Samsung (512M)	0	0	1	1

Check option2 need to
be added or not?



AL31 Manhattan/Vancouver is NC, Boardway is
ADC input(0-1V) use measure regulator current or temperature

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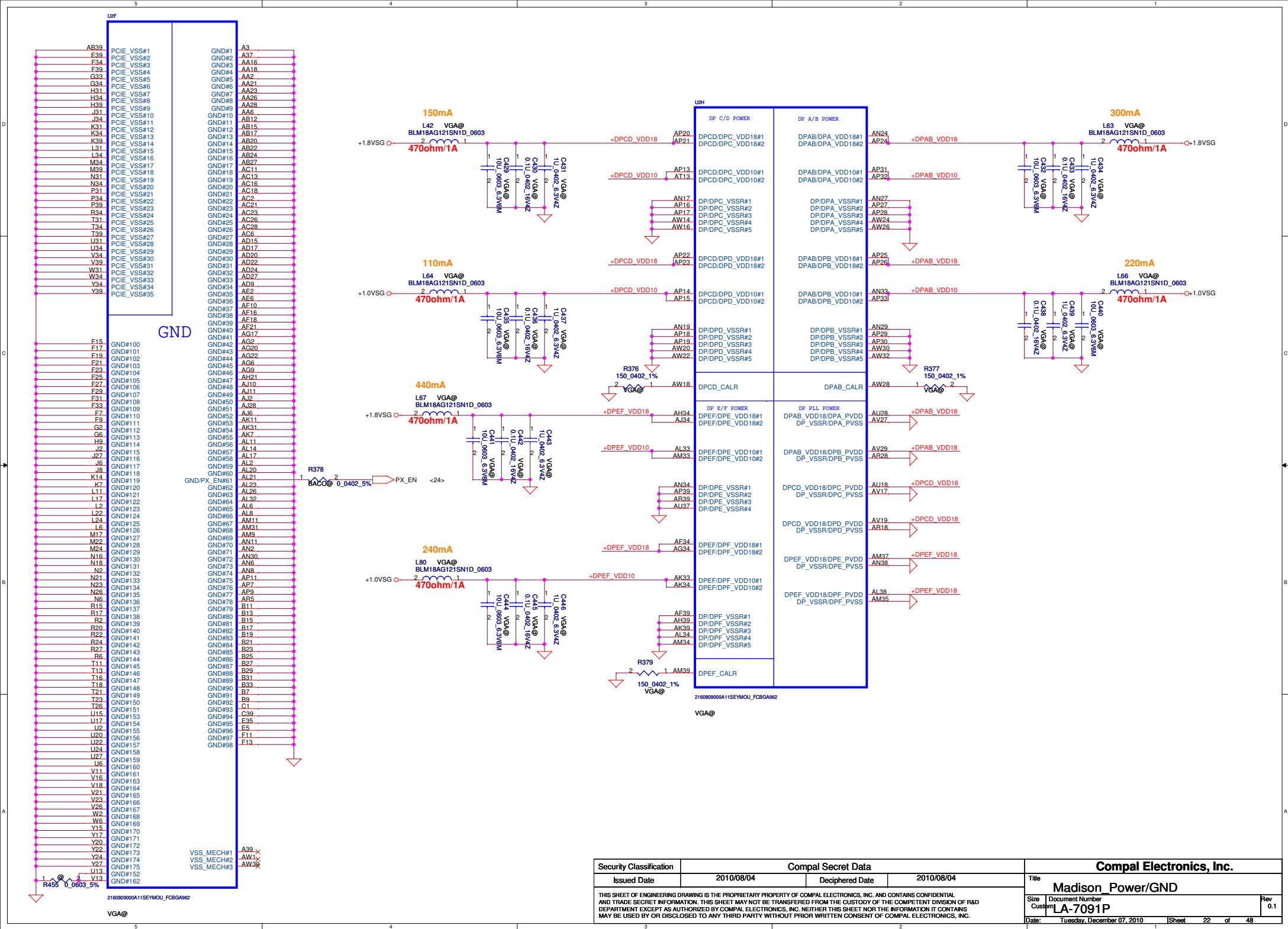
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ADC input(0-1V) use measure regulator current or temperature

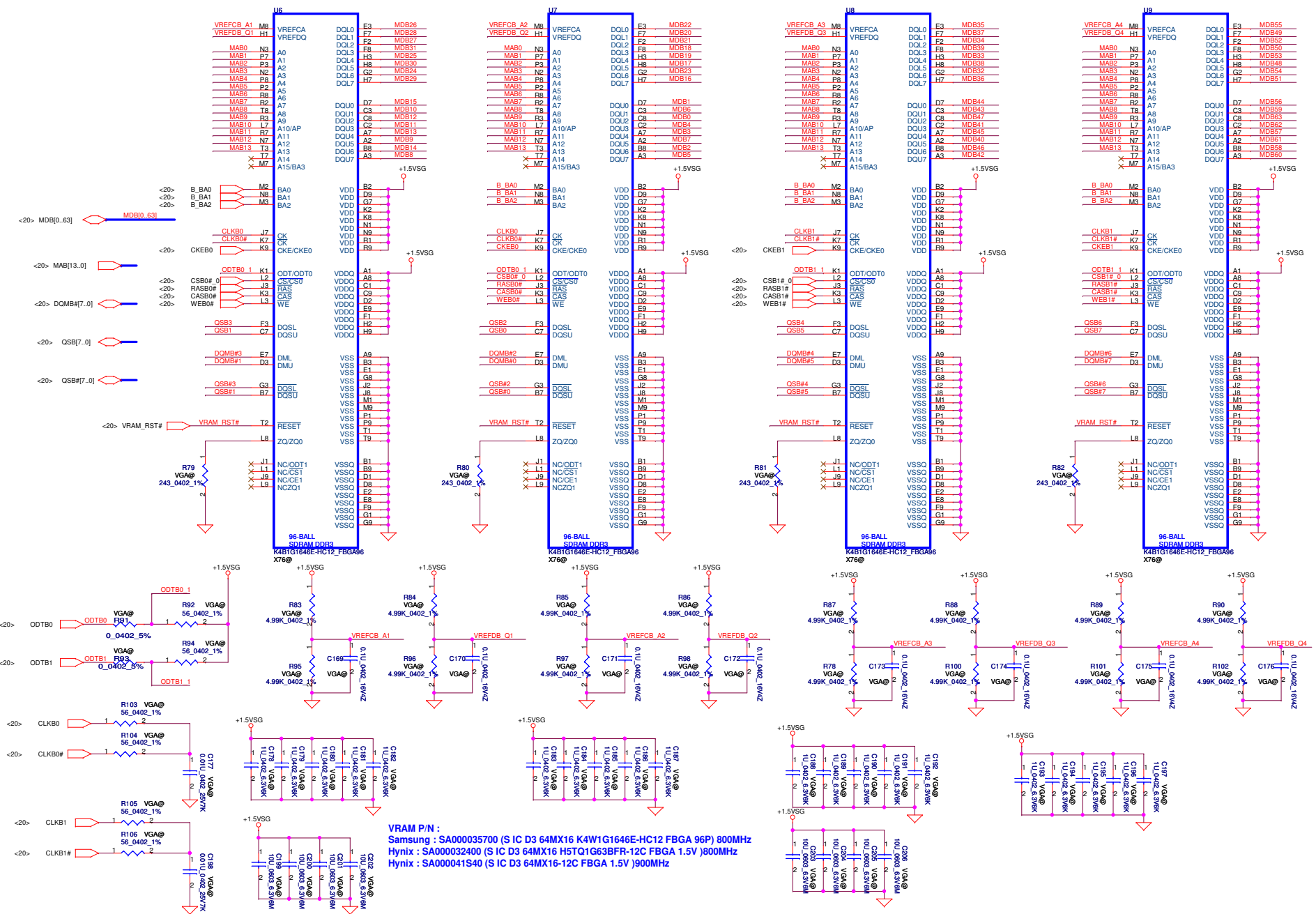
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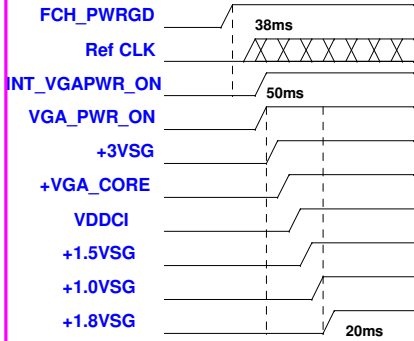
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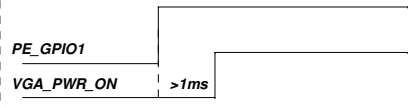


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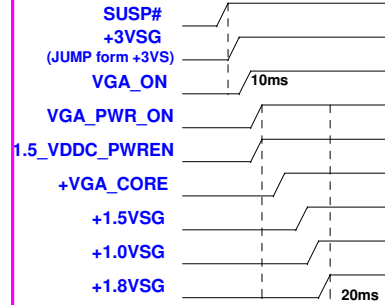
Power Sequence of Granville



For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON



Power Sequence of Whistler and Seymour



VGA Muxless and Dis only Status Mapping table

	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

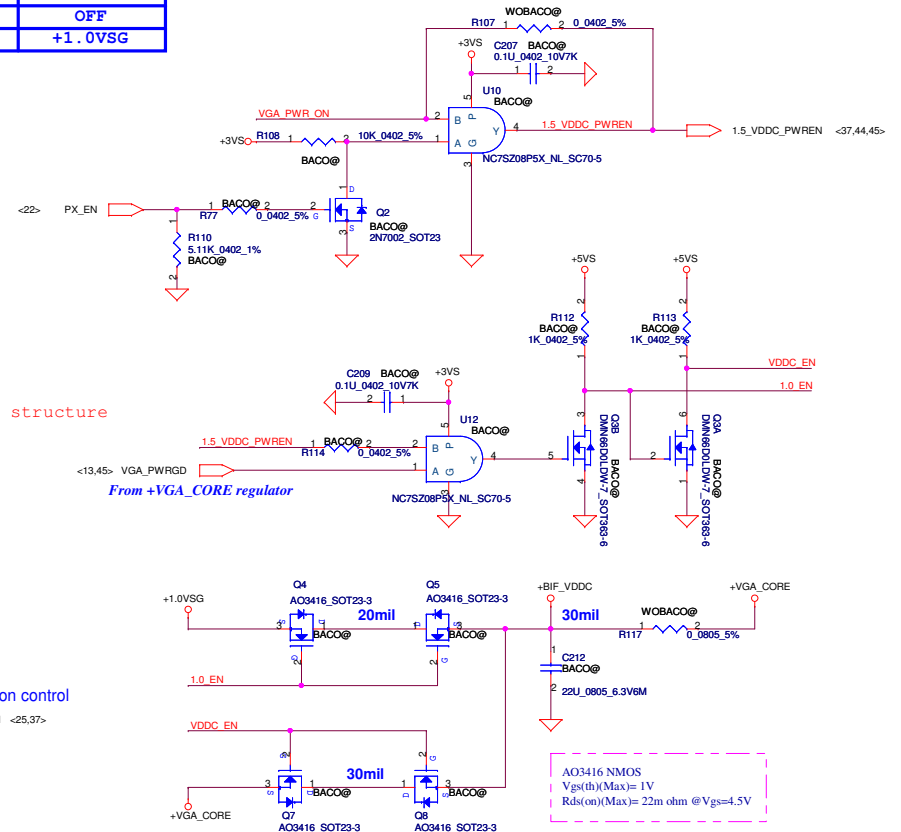
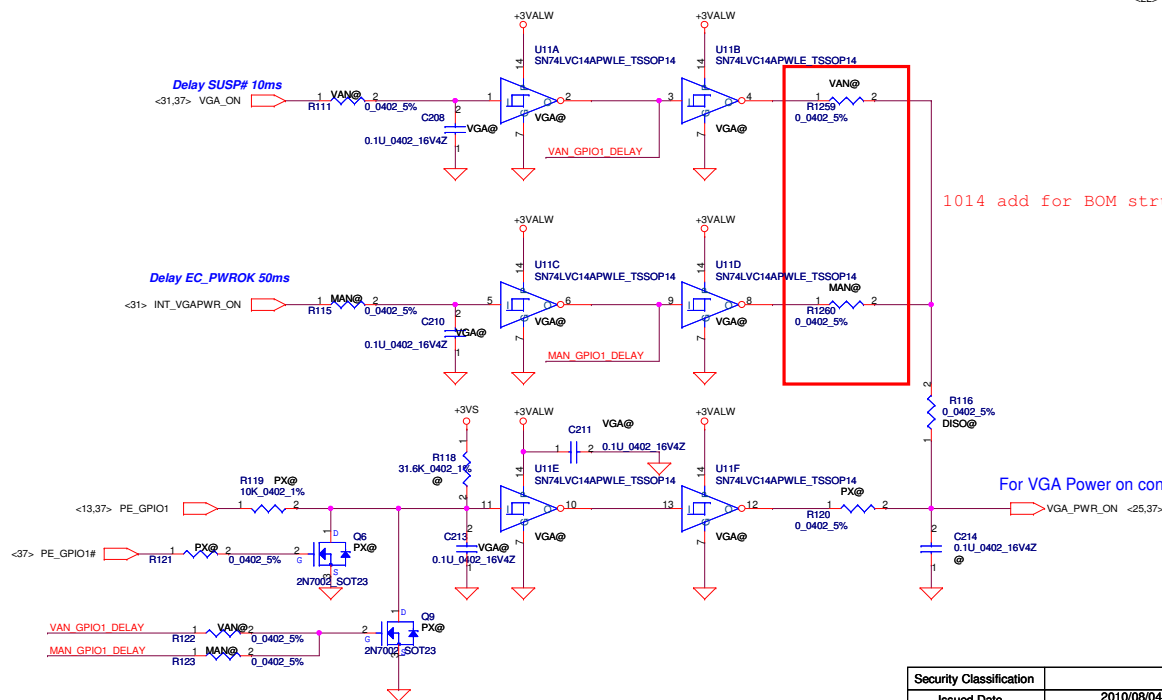
VGA Muxless with BACO Status Mapping table

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table

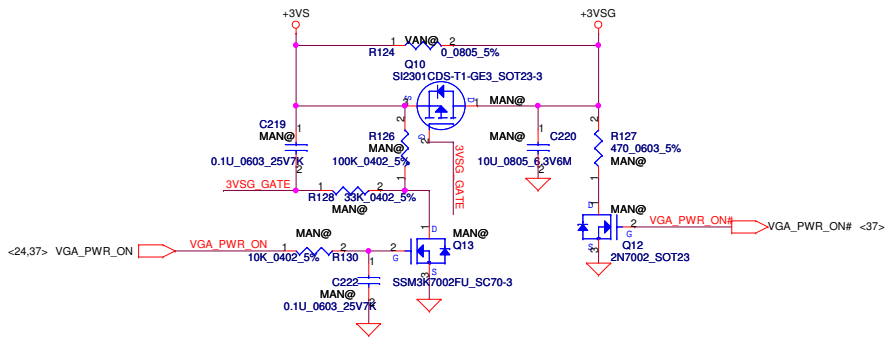
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

VGA Power ON Circuit

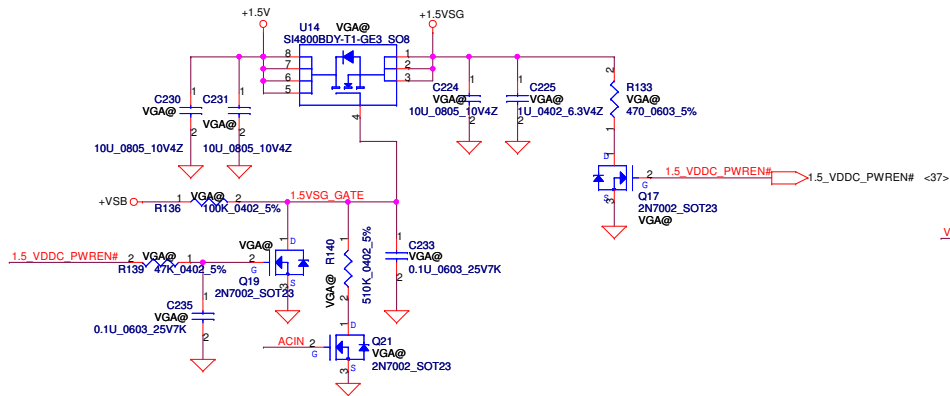


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Deciphered Date				2010/08/04				VGA power sequence and BACO			
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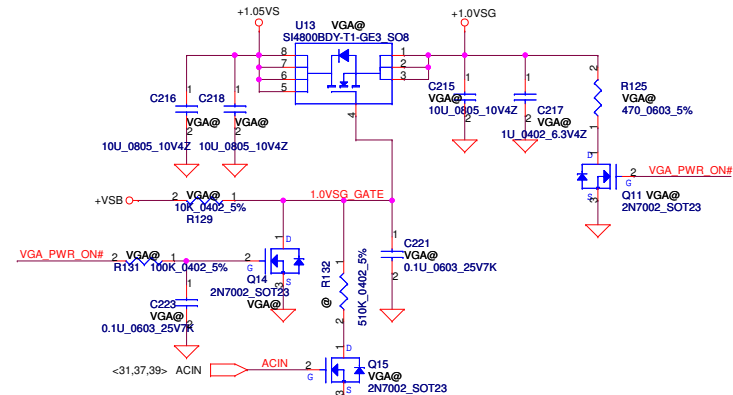
+3.3VS TO +3.3VSG



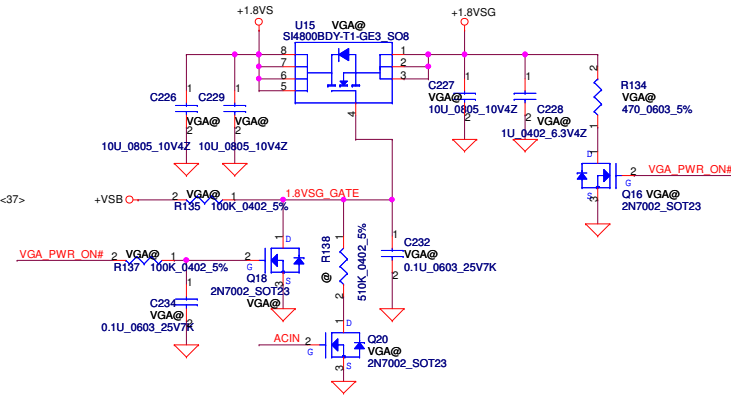
+1.5V TO +1.5VSG



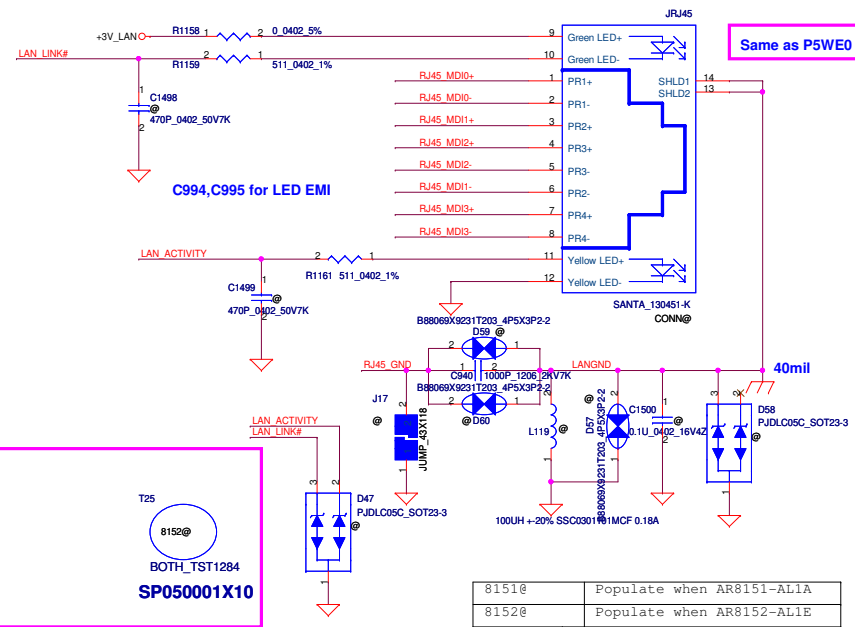
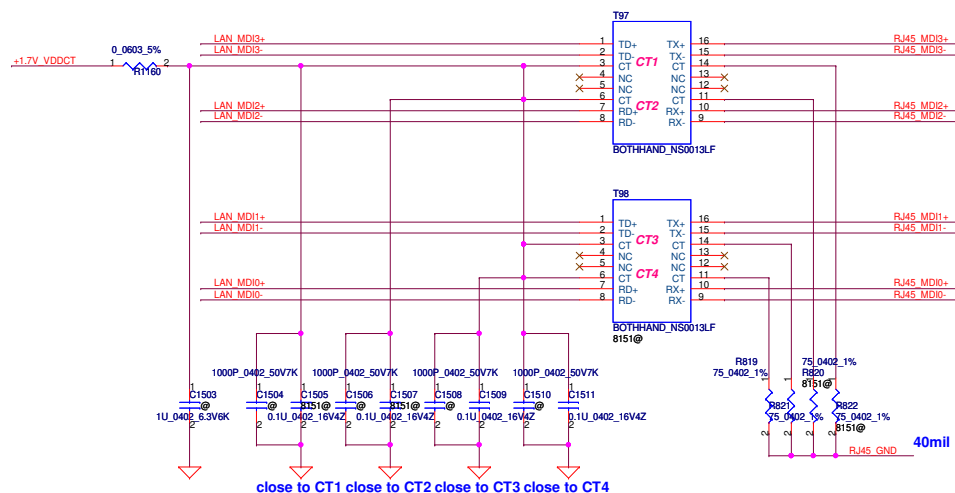
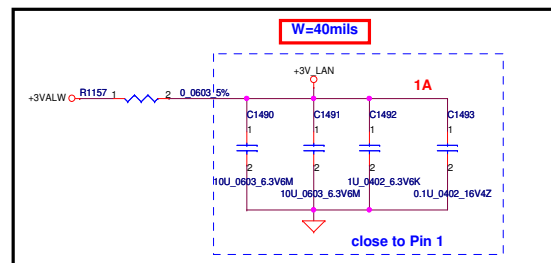
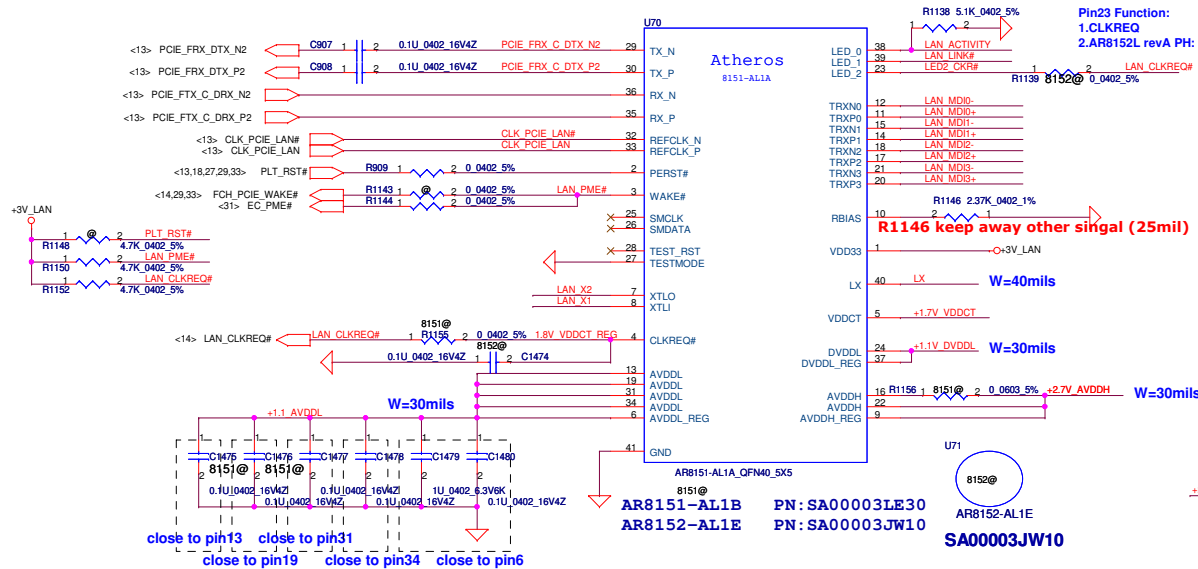
1.05VS TO +1.0VSG



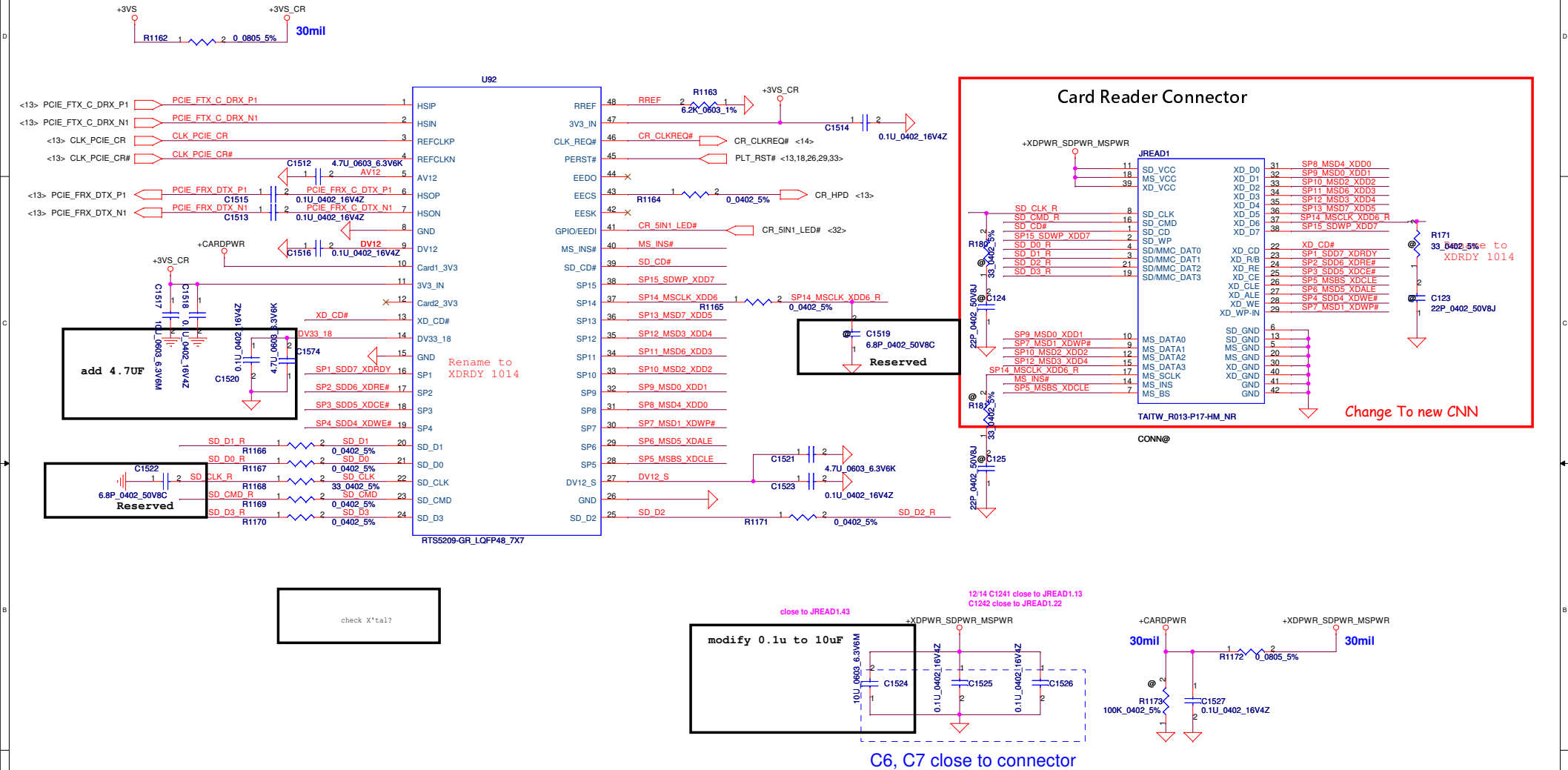
+1.8VS TO +1.8VSG



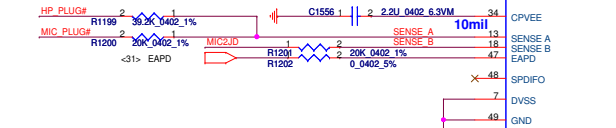
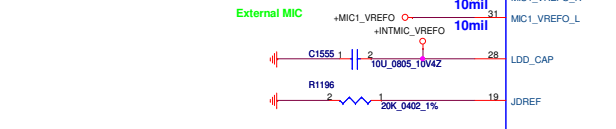
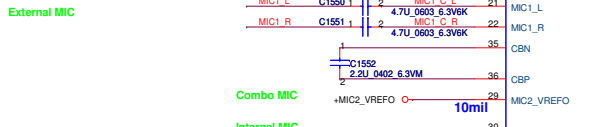
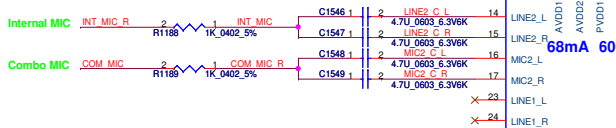
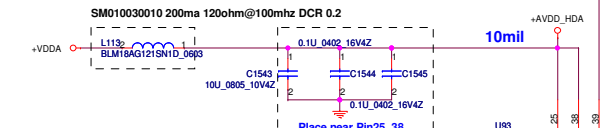
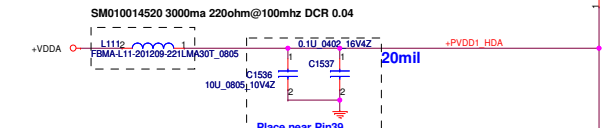
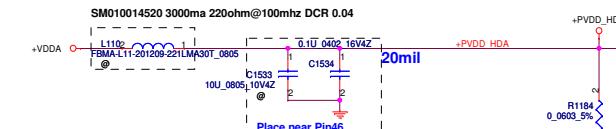
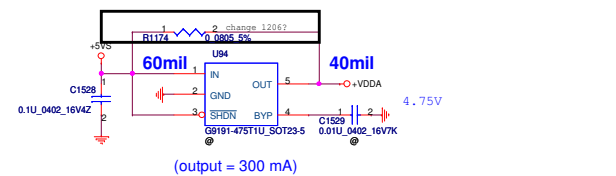
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RTS5209-GR



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				Date: Tuesday, December 07, 2010	Sheet 27 of 48



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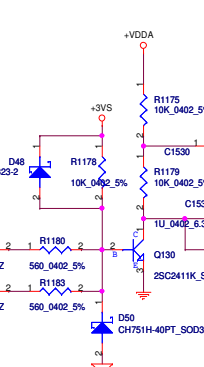
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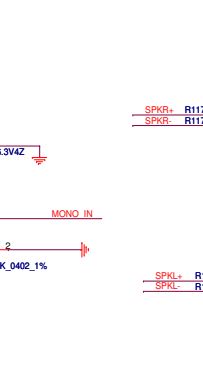
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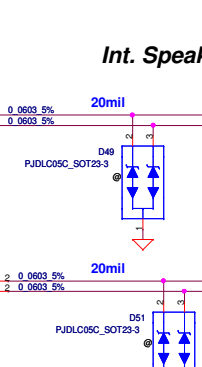
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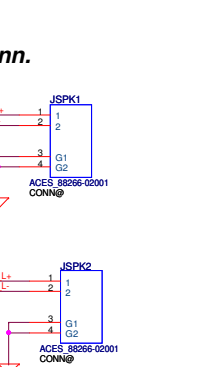
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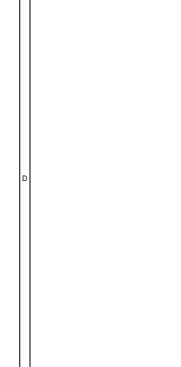
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Int. Speaker Conn.

Int. Speaker Conn.

Int. Speaker Conn.

Int. Speaker Conn.

Int. Speaker Conn.

Int. Speaker Conn.

Int. Speaker Conn.

Singatron 2SJ2326

DC021007151

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

Headphone Out

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

MIC JACK

Int. MIC

Int. MIC

Int. MIC

Int. MIC

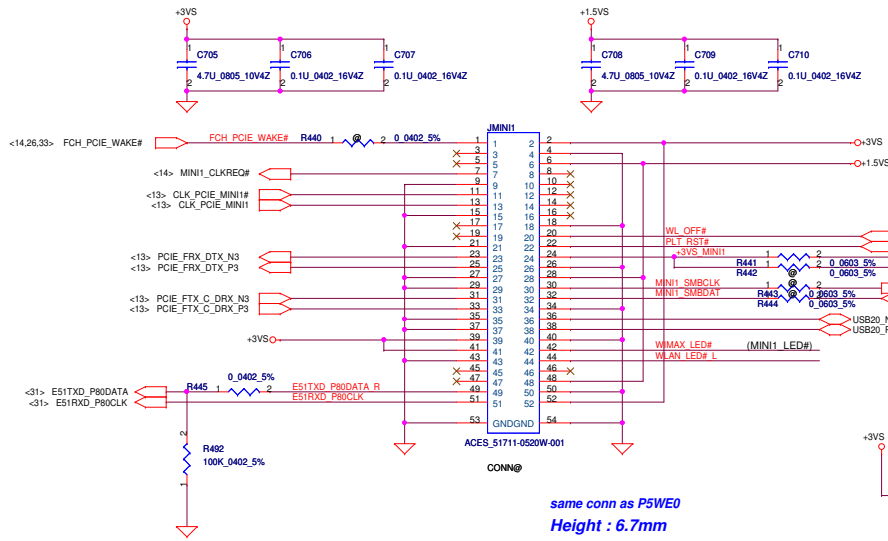
Int. MIC

Int. MIC

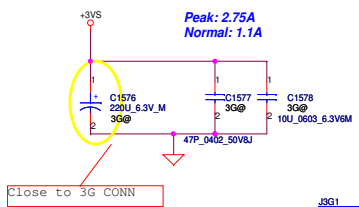
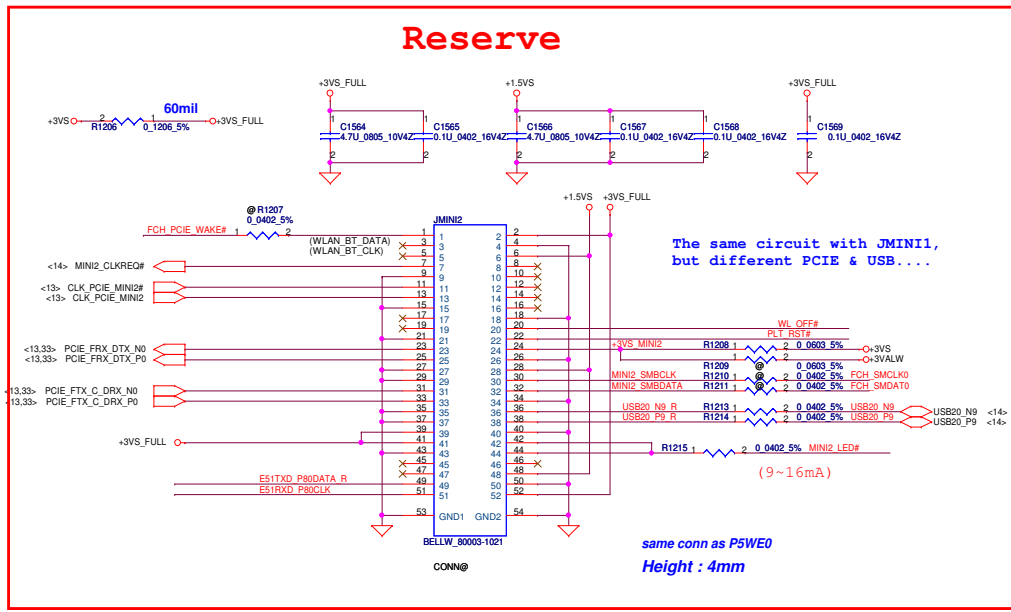
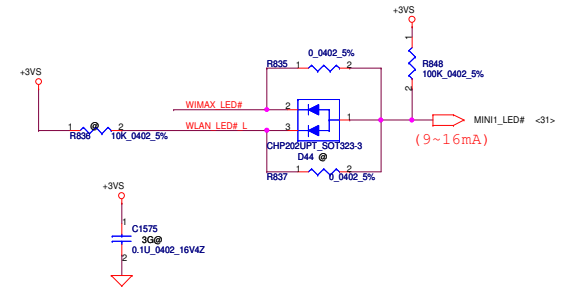
Int. MIC

Security Classification	Compal Secret Data	2010/08/04	2010/08/04	2010/08/04
Issued Date	2010/08/04	Deciphered Date	2010/08/04	2010/08/04
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Size	C	Document Number	LA-7091P	Rev 0.1
Date:	Tuesday, December 07, 2010	Sheet	28	of 48

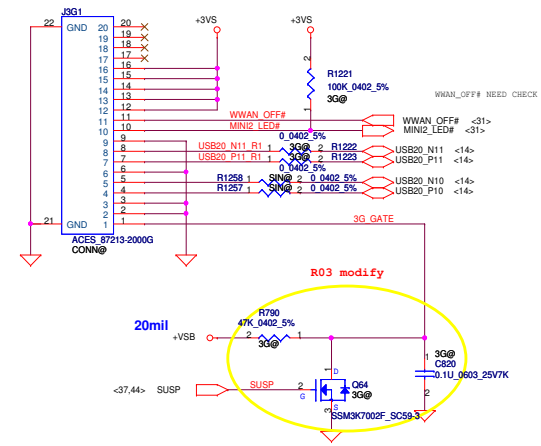
Mini-Express Card for WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

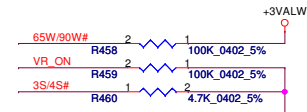
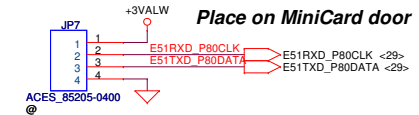


For 3G / GPS
To 3G Module Connect

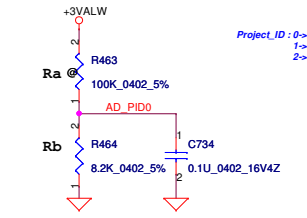


For EC Tools

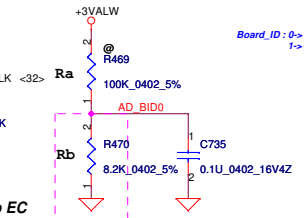
Place on MiniCard door



Analog Project ID definition



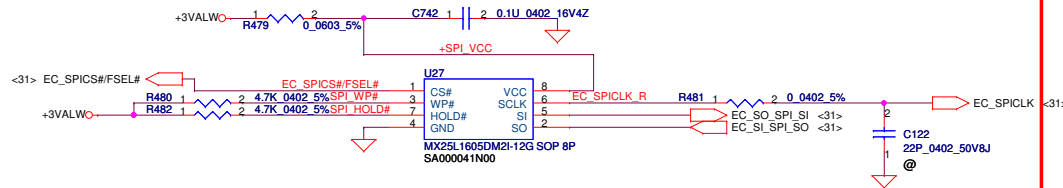
Analog Board ID definition



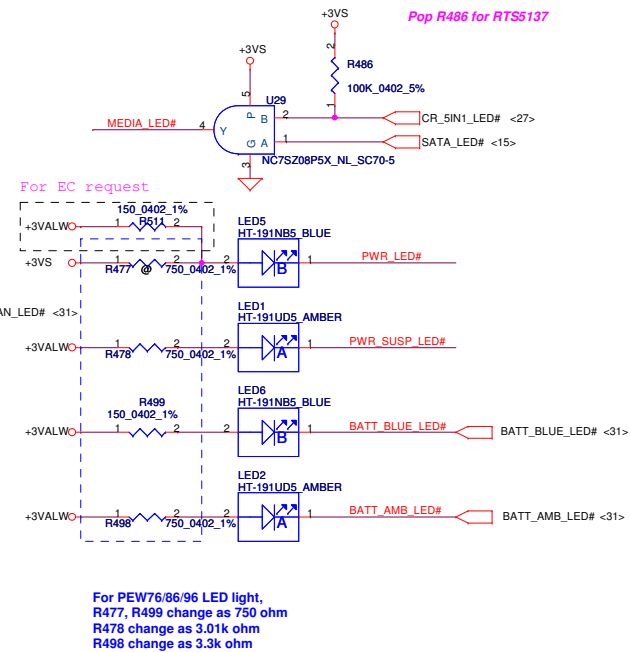
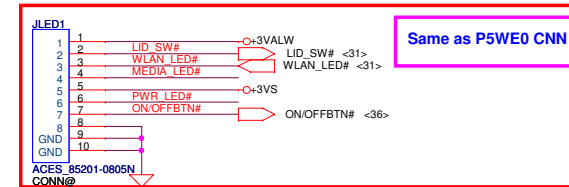
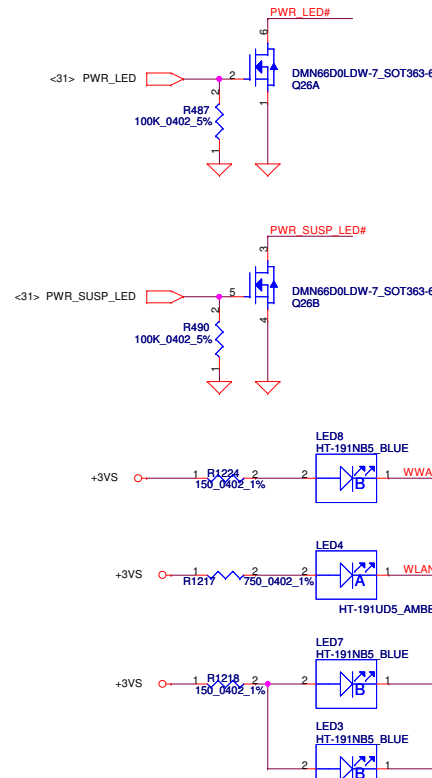
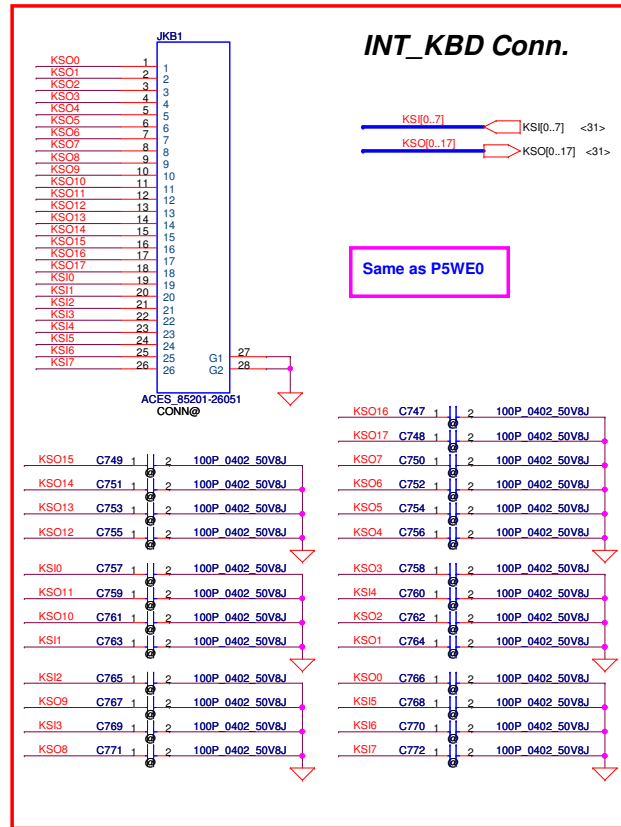
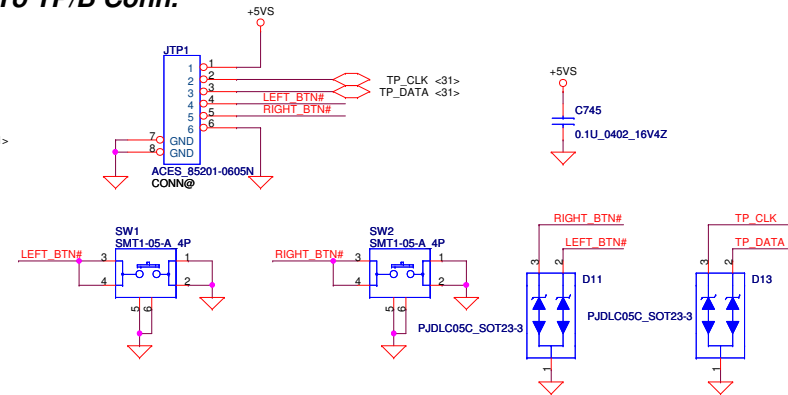
Reserve for EMI, close to EC

Delay SUSP# 10ms

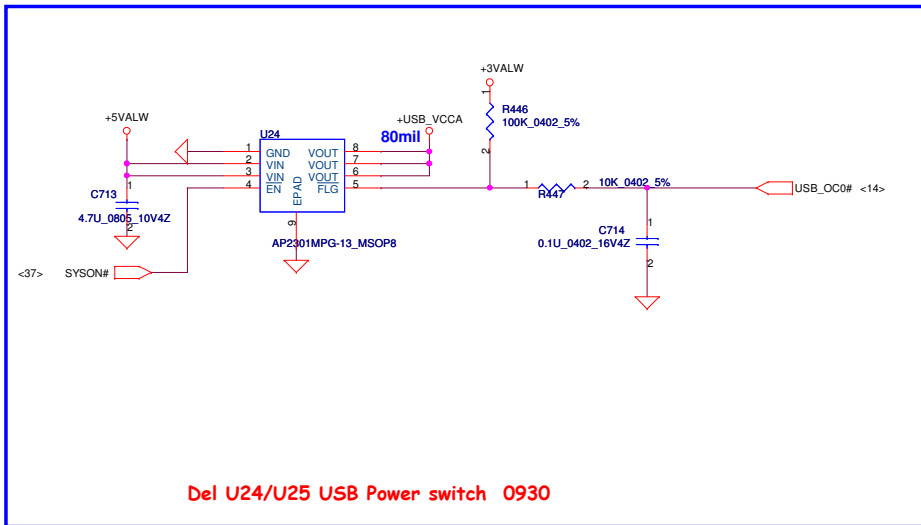
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2010/08/04				2010/08/04				EC ENE KB930			
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				Custom				LA-7091P			
				Date				Tuesday, December 07, 2010			
				Sheet				31 of 48			



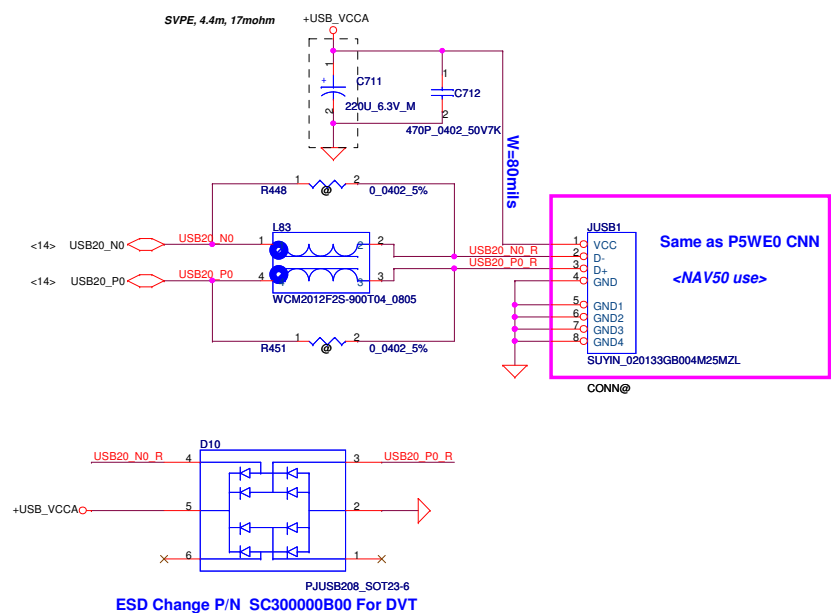
To TP/B Conn.



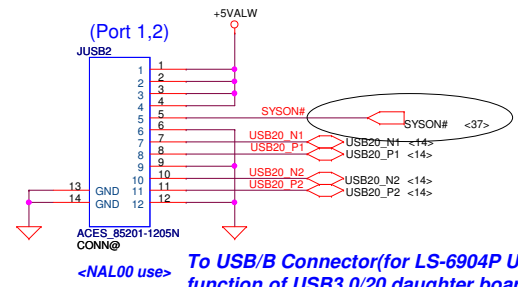
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Issued Date	2010/08/04	Deciphered Date	2010/08/04	KB/TP/LED/SPI ROM/PWRb
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Date: Tuesday, December 07, 2010				Rev 0.1



Del U24/U25 USB Power switch 0930

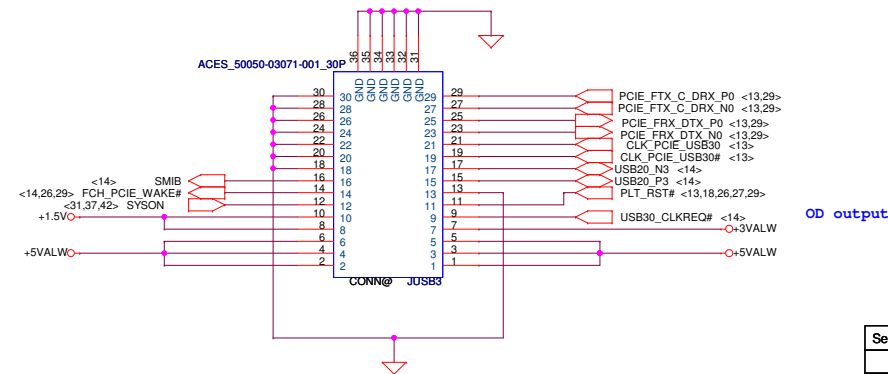


ESD Change P/N SC300000B00 For DVT

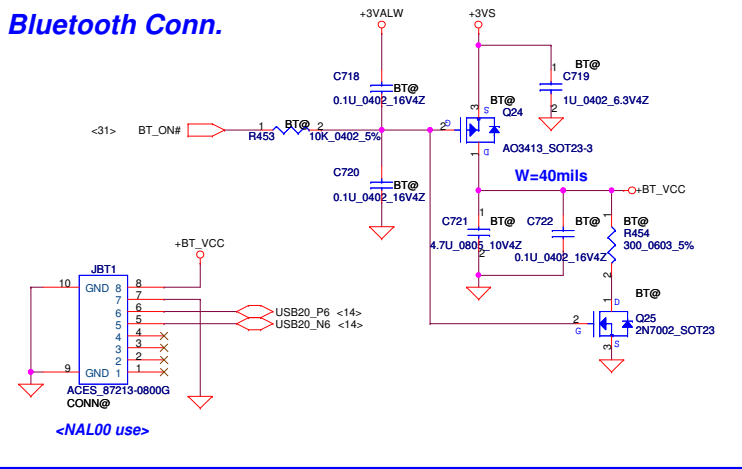


To USB/B Connector(for LS-6904P USB2.0 function of USB3.0/20 daughter board)

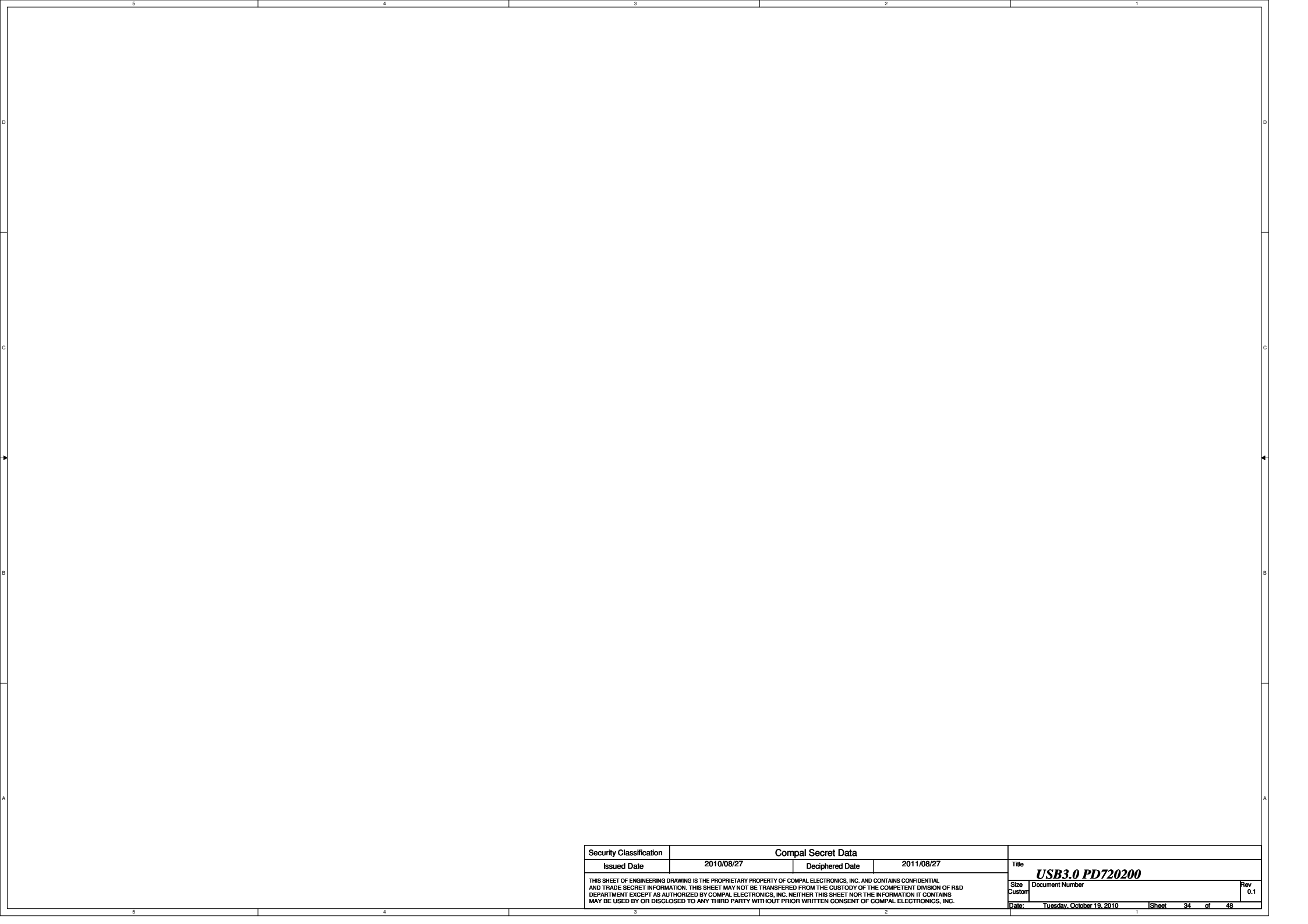
USB3.0 Conn.



Bluetooth Conn.

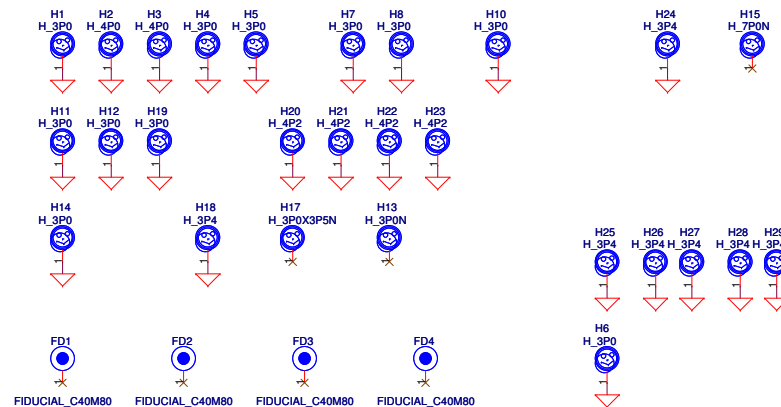
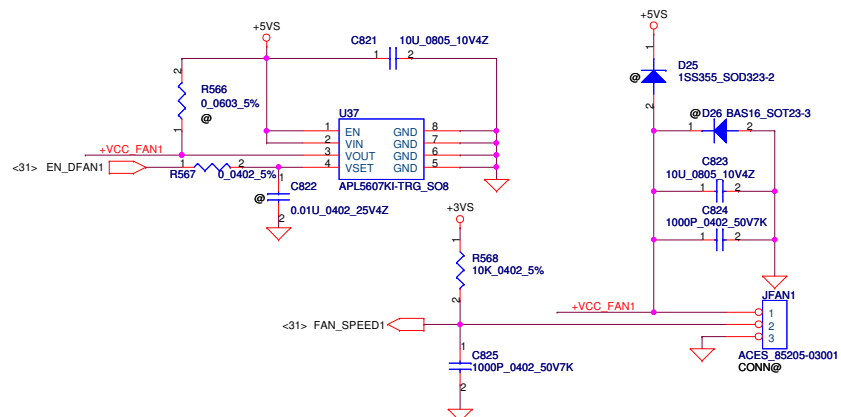
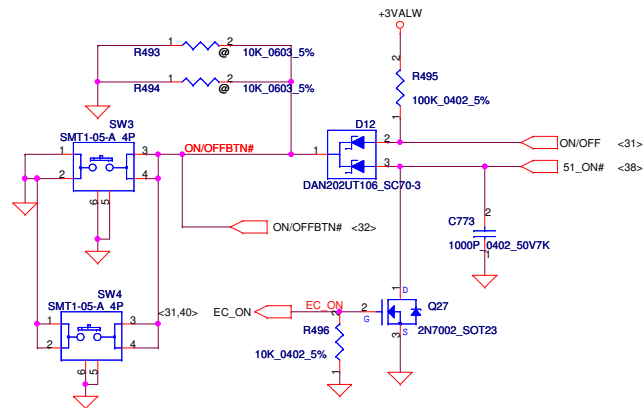


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Issued Date	2010/08/04	Deciphered Date	2010/08/04	Title		
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				Size	Document Number	Rev
				Custom	LA-7091P	0.1
				Date:	Tuesday, December 07, 2010	Sheet 33 of 48



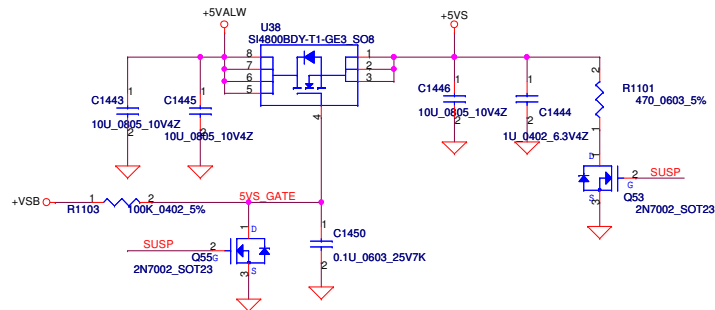
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Issued Date	2010/08/27	Deciphered Date	2011/08/27	USB3.0 PD720200	
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				Custom	
				Date: Tuesday, October 19, 2010	

5	4	3	2	1																								
D				D																								
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B				B																								
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<table><tr><td colspan="2">Security Classification</td><td colspan="2">Compal Secret Data</td><td colspan="2">Title</td></tr><tr><td>Issued Date</td><td>2010/08/27</td><td>Deciphered Date</td><td>2011/08/27</td><td colspan="2">USB3.0 PD720200</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size Custom</td><td>Rev 0.1</td></tr><tr><td colspan="4">Date: Tuesday, October 19, 2010</td><td>Sheet 35 of 48</td><td></td></tr></table>					Security Classification		Compal Secret Data		Title		Issued Date	2010/08/27	Deciphered Date	2011/08/27	USB3.0 PD720200		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 0.1	Date: Tuesday, October 19, 2010				Sheet 35 of 48	
Security Classification		Compal Secret Data		Title																								
Issued Date	2010/08/27	Deciphered Date	2011/08/27	USB3.0 PD720200																								
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Date: Tuesday, October 19, 2010				Sheet 35 of 48																								
5	4	3	2	1																								

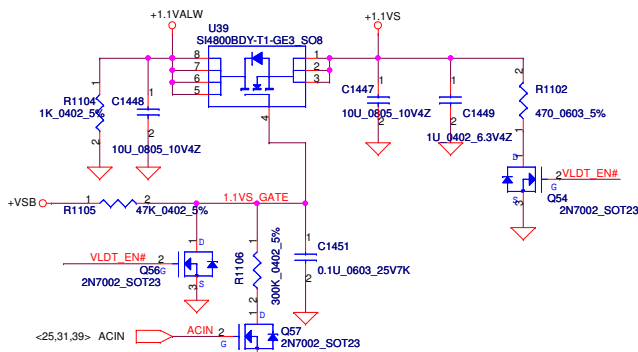


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Issued Date		2010/08/04	Deciphered Date	2010/08/04		Title
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				Size	Document Number	Rev
				Custom	LA-7091P	0.1
				Date: Tuesday, December 07, 2010		
				Sheet 36 of 48		

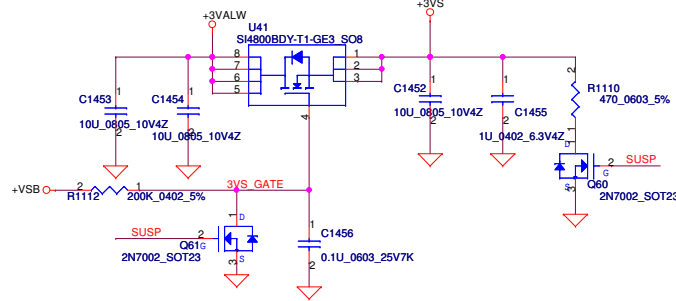
+5VALW TO +5VS



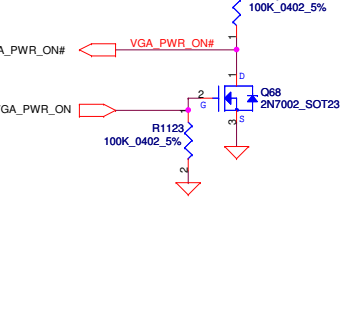
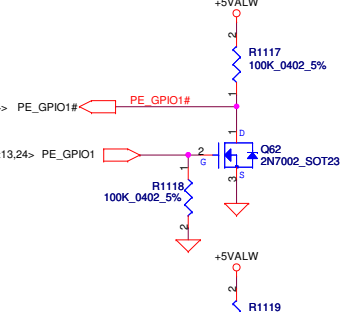
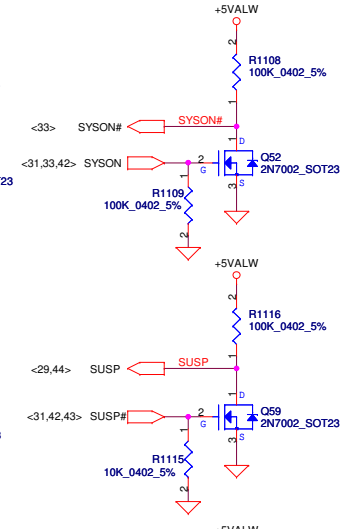
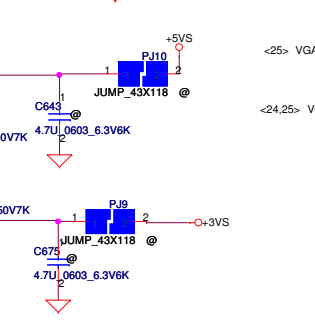
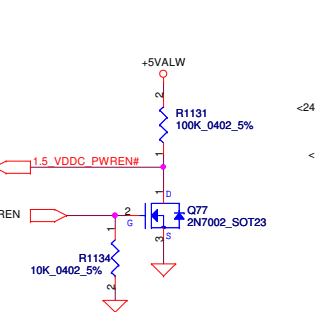
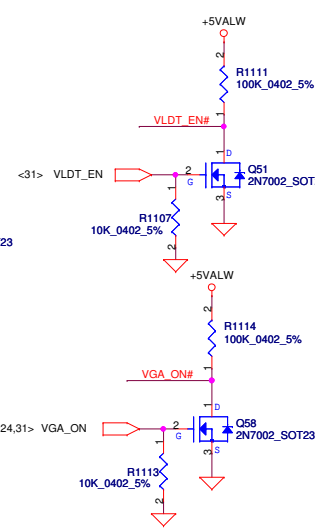
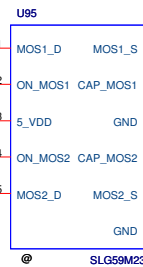
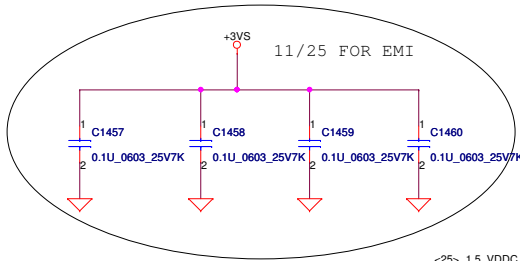
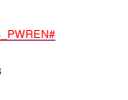
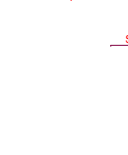
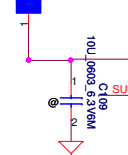
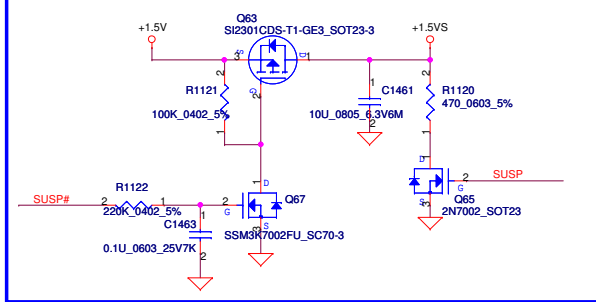
+1.1VALW TO +1.1VS



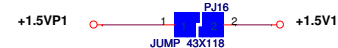
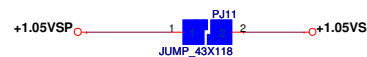
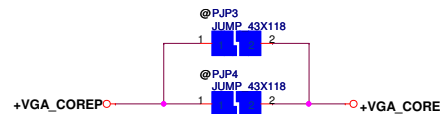
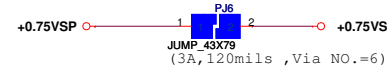
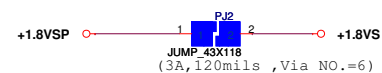
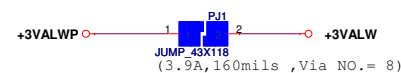
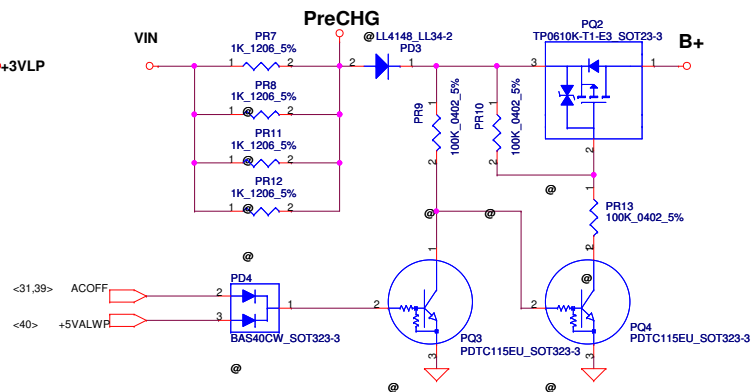
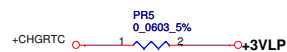
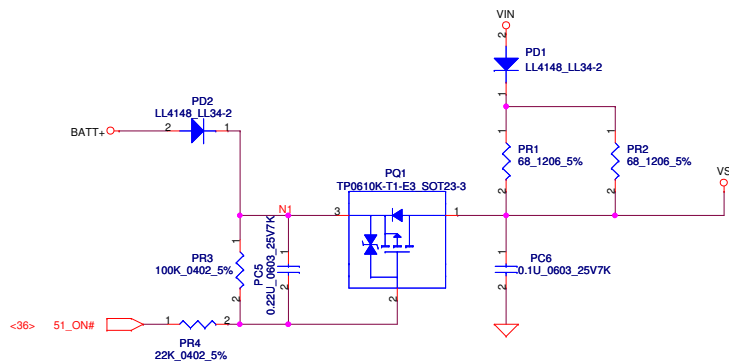
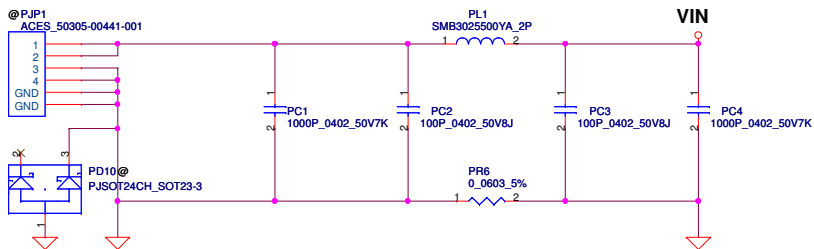
+3VALW TO +3VS



+1.5VS



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Size	Custom	Document Number	LA-7091P	Rev	
Date	Tuesday, December 07, 2010	Sheet	37	of 48	



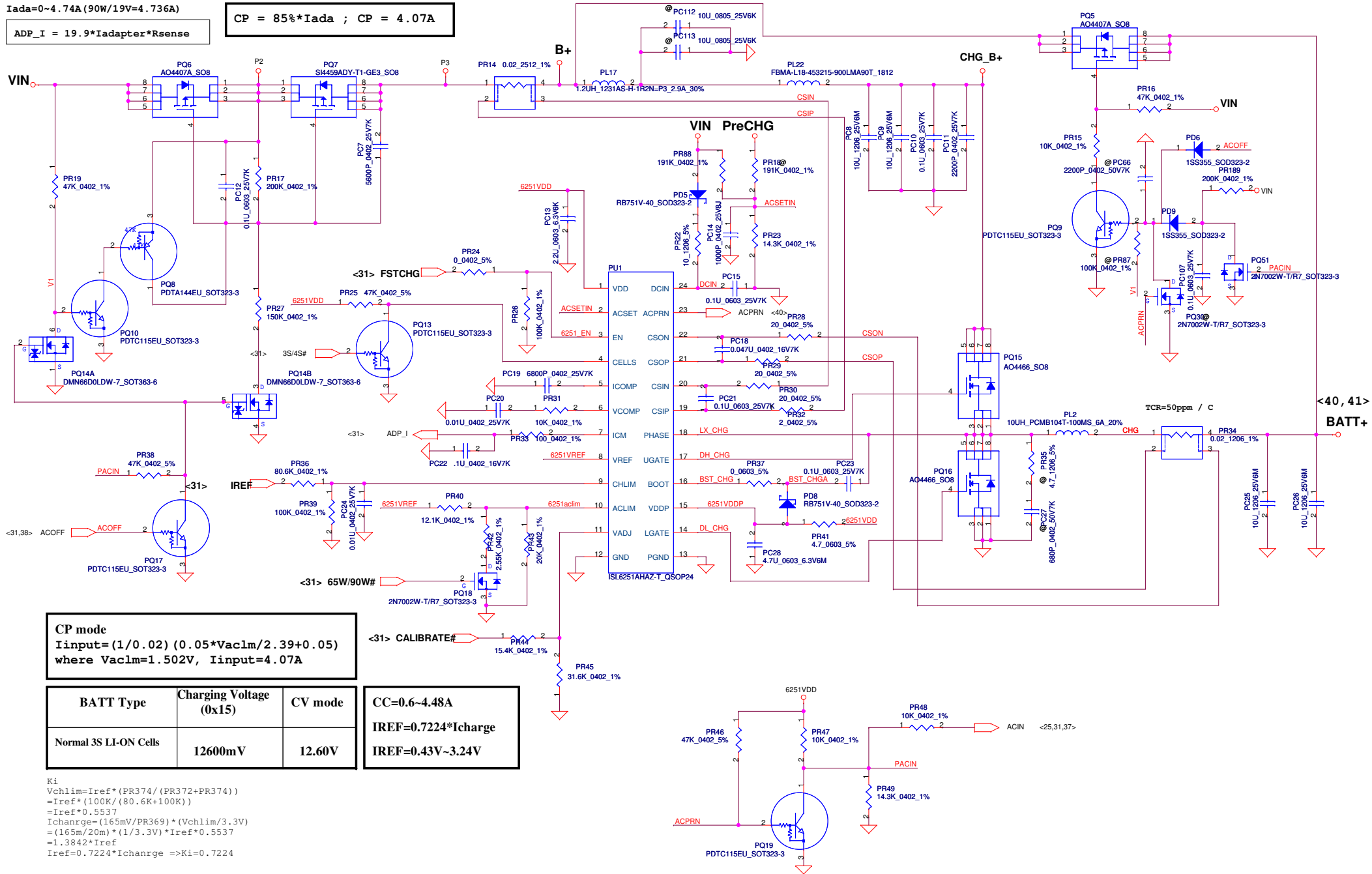
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Issued Date				2010/07/13		Deciphered Date		2011/07/13		Title	
										PWR DCIN / Pre-charge	
										P5WE0 M/B LA-6901P Schematic	
										Rev 0.1	
										Date: Tuesday, December 07, 2010	
										Sheet 38 of 47	

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I_{ada}=0~4.74A (90W/19V=4.736A)

CP = 85%*I_{ada} ; CP = 4.07A

ADP_I = 19.9*I_{adapter}*R_{sense}



CP mode

I_{input}=(1/0.02) (0.05*V_{ac1m}/2.39+0.05)
where V_{ac1m}=1.502V, I_{input}=4.07A

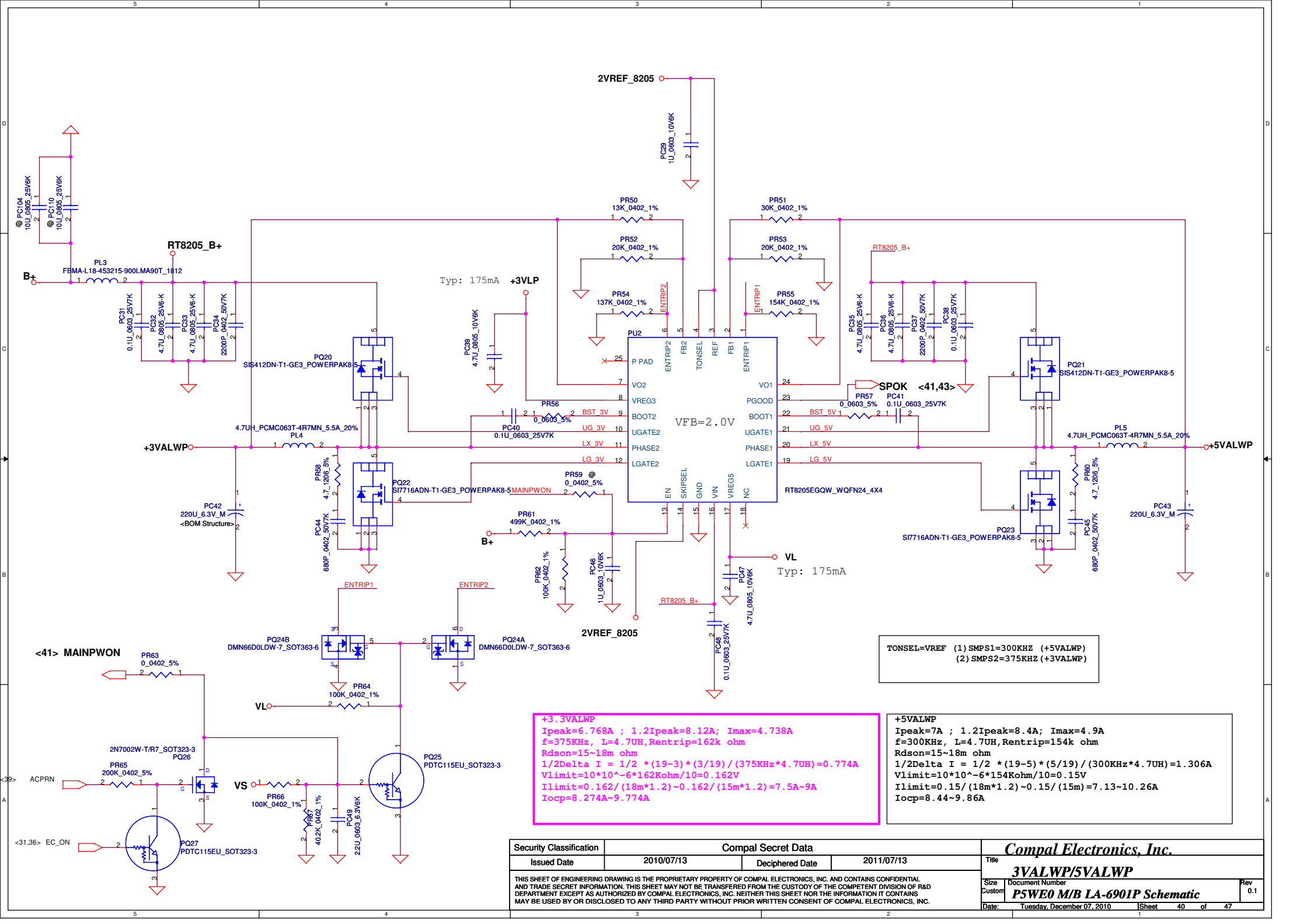
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
I_{REF}=0.7224*I_{charge}
I_{REF}=0.43V~3.24V

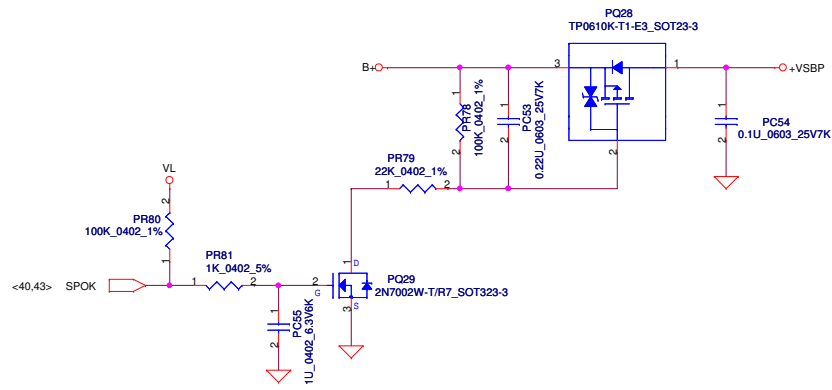
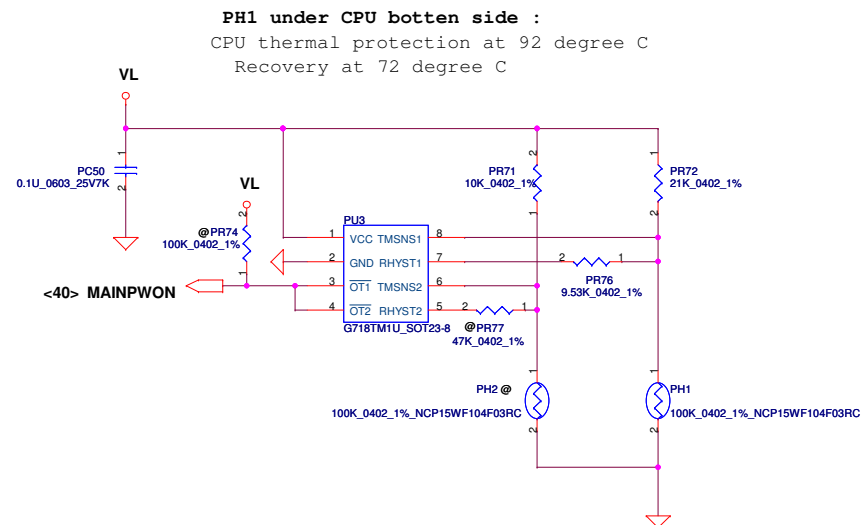
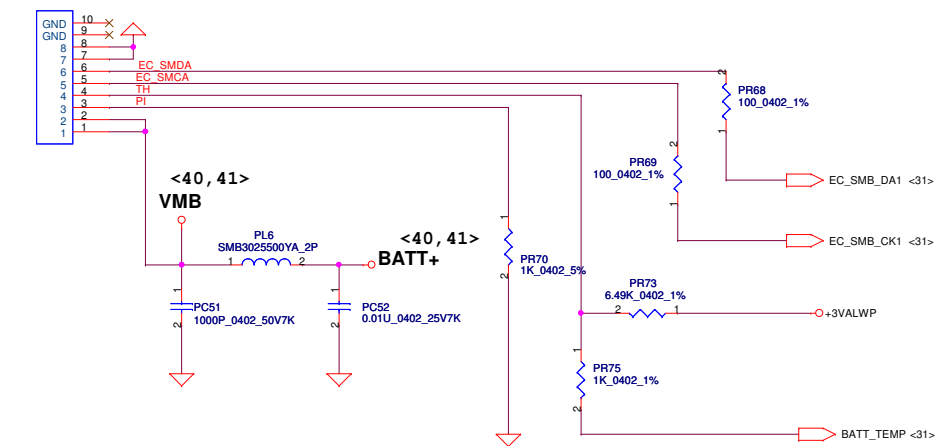
K_i
V_{chlim}=I_{ref}*(PR374/(PR372+PR374))
=I_{ref}*(100K/(80.6K+100K))
=I_{ref}*0.5537
I_{charge}=(165mV/PR369)*(V_{chlim}/3.3V)
=(165m/20m)*(1/3.3V)*I_{ref}*0.5537
=1.3842*I_{ref}
I_{ref}=0.7224*I_{charge} =>K_i=0.7224

K_v
R_{internal} ic=514K Rec=3K R₁=PR379=15.4K R₂=PR381=31.6K
R=514K//31.6K/(15.4K+3K)=11.372K
r=514K//514K//31.6K=28.14K
V_{cell}=0.175*V_{adj}+3.99V
4.2V=0.175*V_{adj}+3.99V =>V_{adj}=1.2V
V_{adj}=V_{ref}*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(V_{cell}+A*0.175))*K_v=(4.2-(4.2+A*0.175))*K_v
A=V_{ref}*(R/(R+514K))=0.052
K_v=9.451

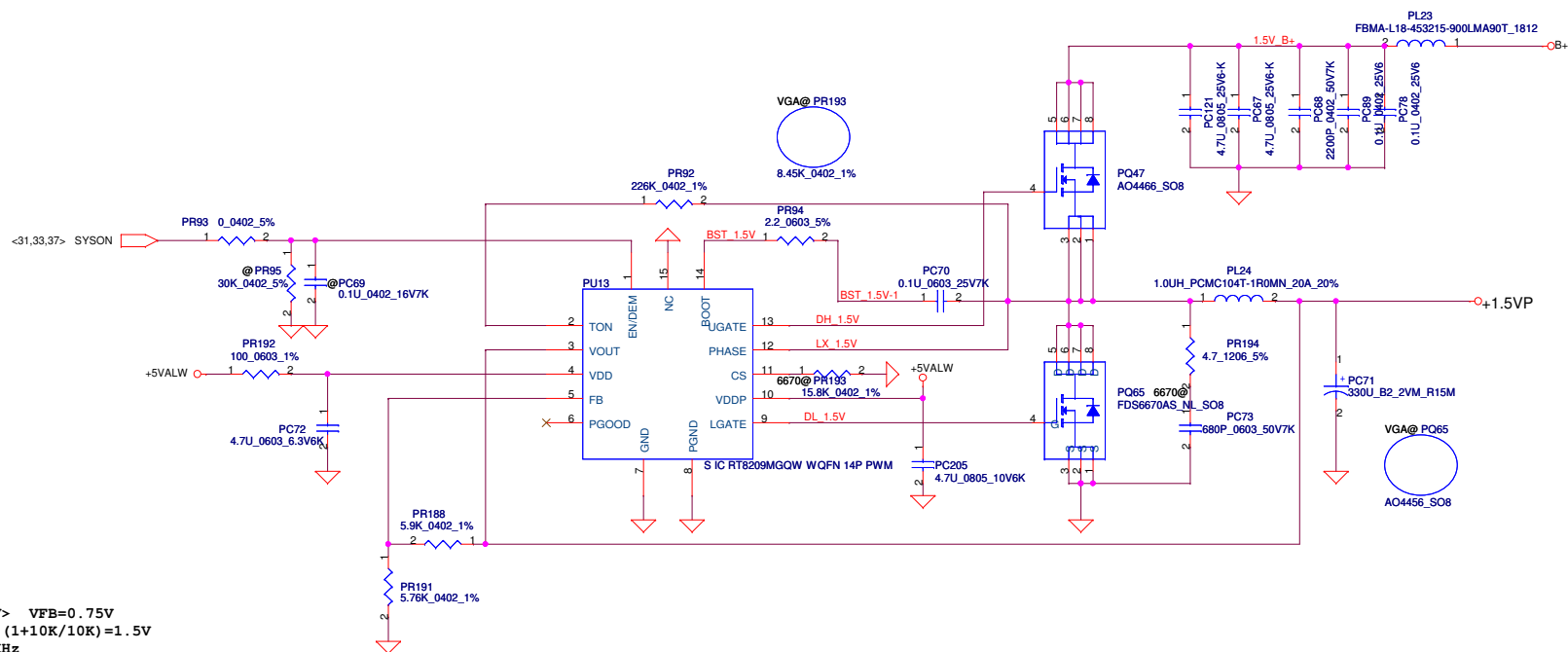
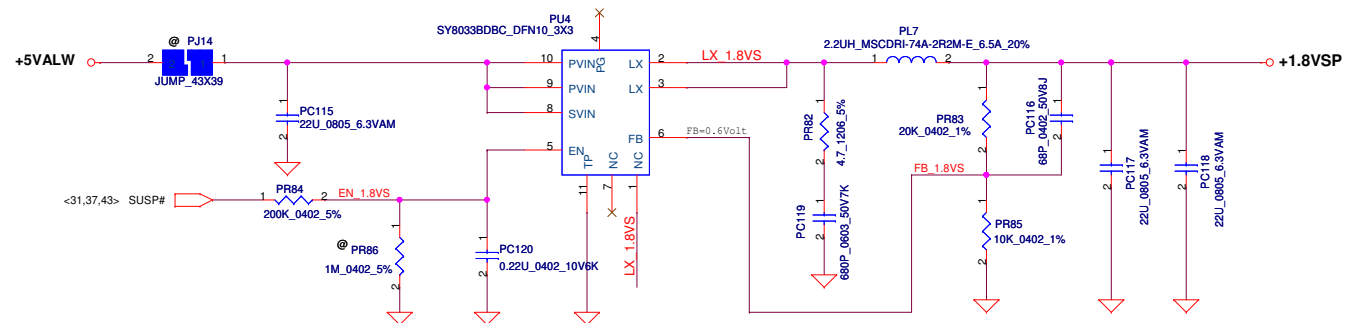
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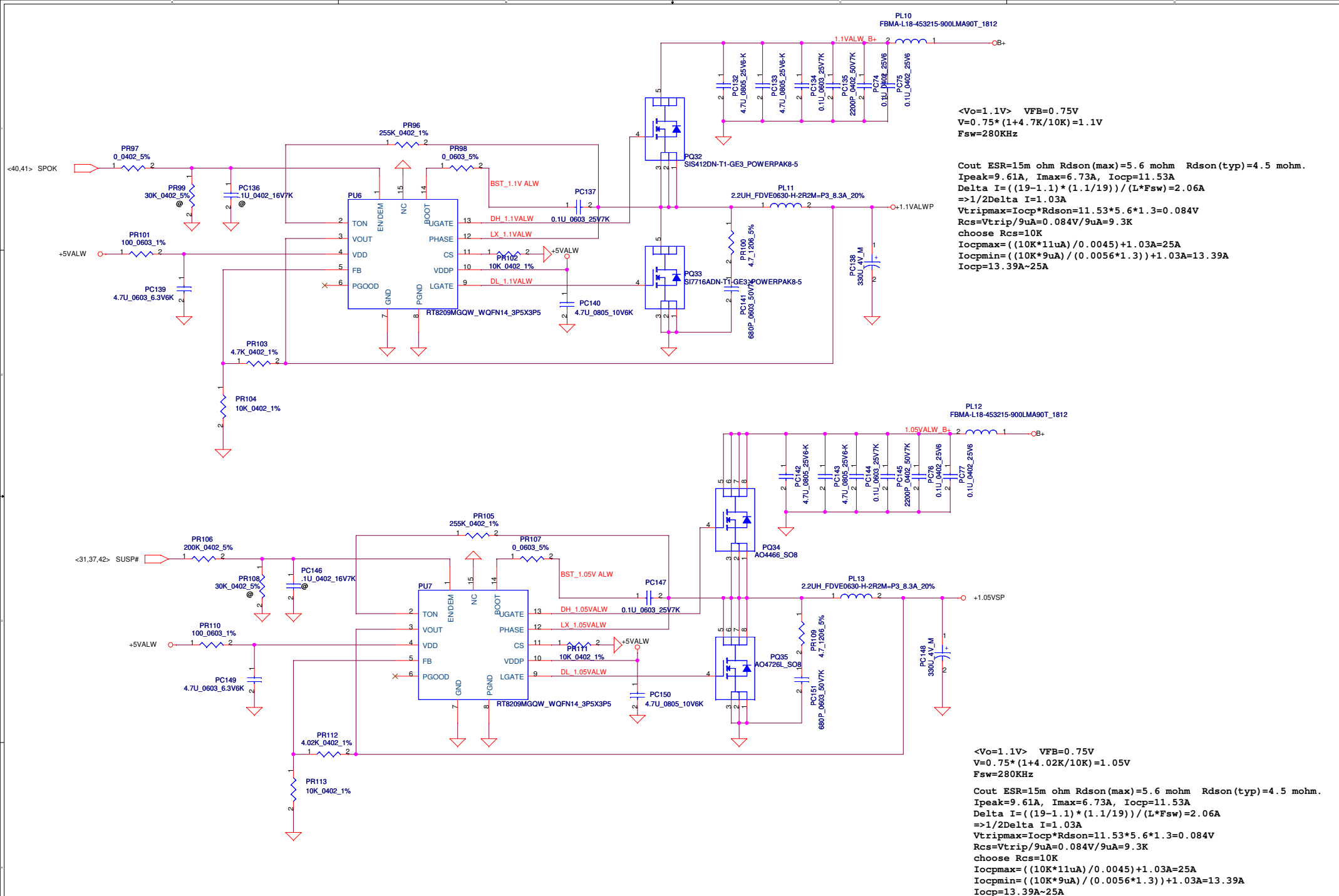


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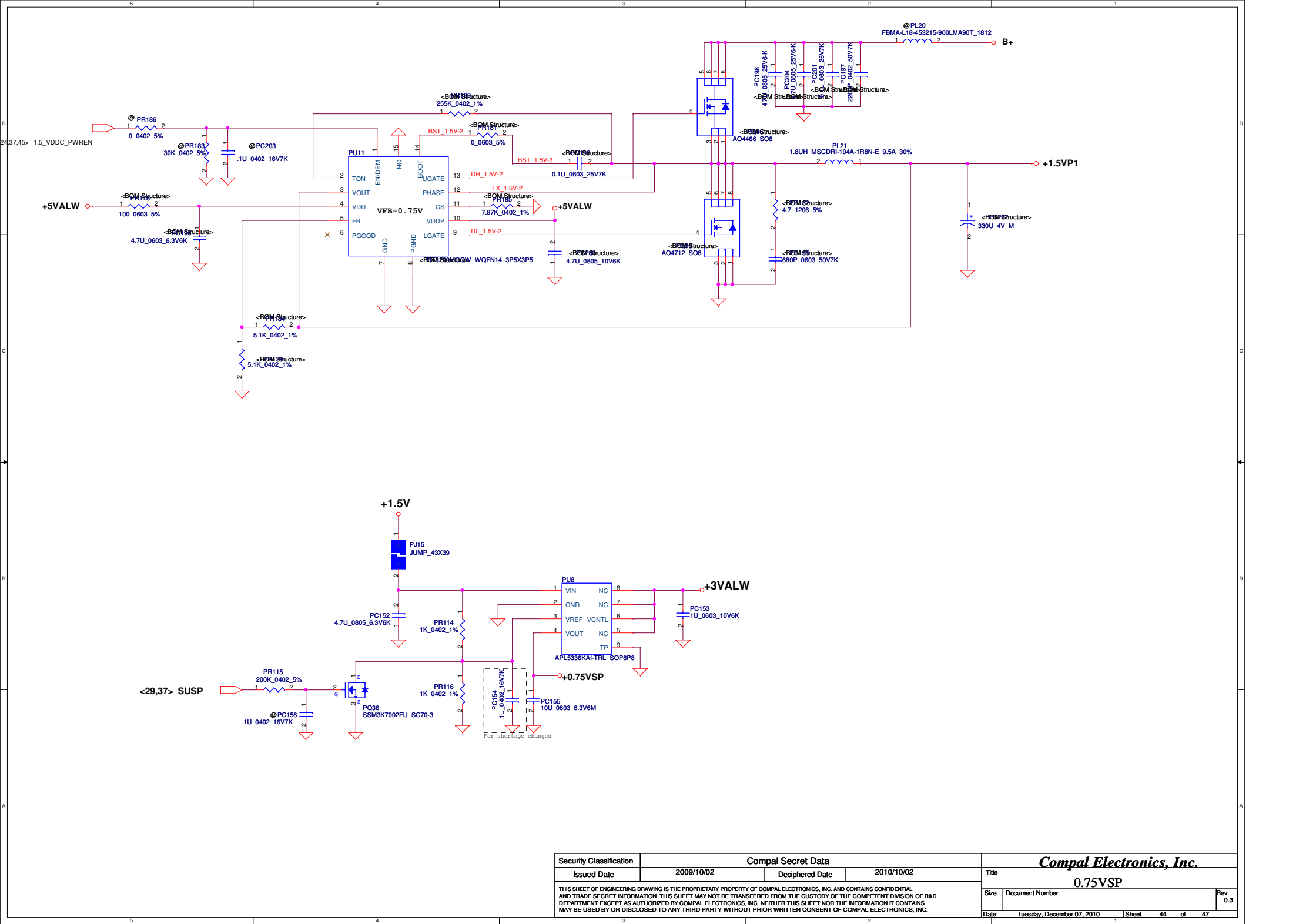


$V_o = 1.5V$ $V_{FB} = 0.75V$
 $V_o = 0.75 * (1 + 10K / 10K) = 1.5V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 17 \text{ mohm}$ $R_{dson}(\text{max}) = 5.6 \text{ mohm}$ $R_{dson}(\text{typ}) = 4.5 \text{ mohm}$
 $I_{peak} = 14.4A$ $I_{max} = 10.08A$ $I_{ocp} = 17.28A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * F_{sw}) = 3.9A$
 $\Rightarrow 1/2 \Delta I = 1.95A$
 $V_{tripmax} = I_{ocp} * R_{dson} = 16.2 * 5.6 * 1.3 = 0.118V$
 $R_{cs} = V_{trip} / 9uA = 0.118V / 9uA = 13.1K$
 choose $R_{cs} = 13K$
 $I_{ocpmax} = ((13K * 11uA) / 0.0045) + 1.95A = 32A$
 $I_{ocpmin} = ((13K * 9uA) / (0.0056 * 1.3)) + 1.95A = 18A$
 $I_{ocp} = 18A \sim 32A$

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