

Compal Confidential

Cougar 2.0

Schematics Document

Intel Cedar Trail Processor/ Tiger point

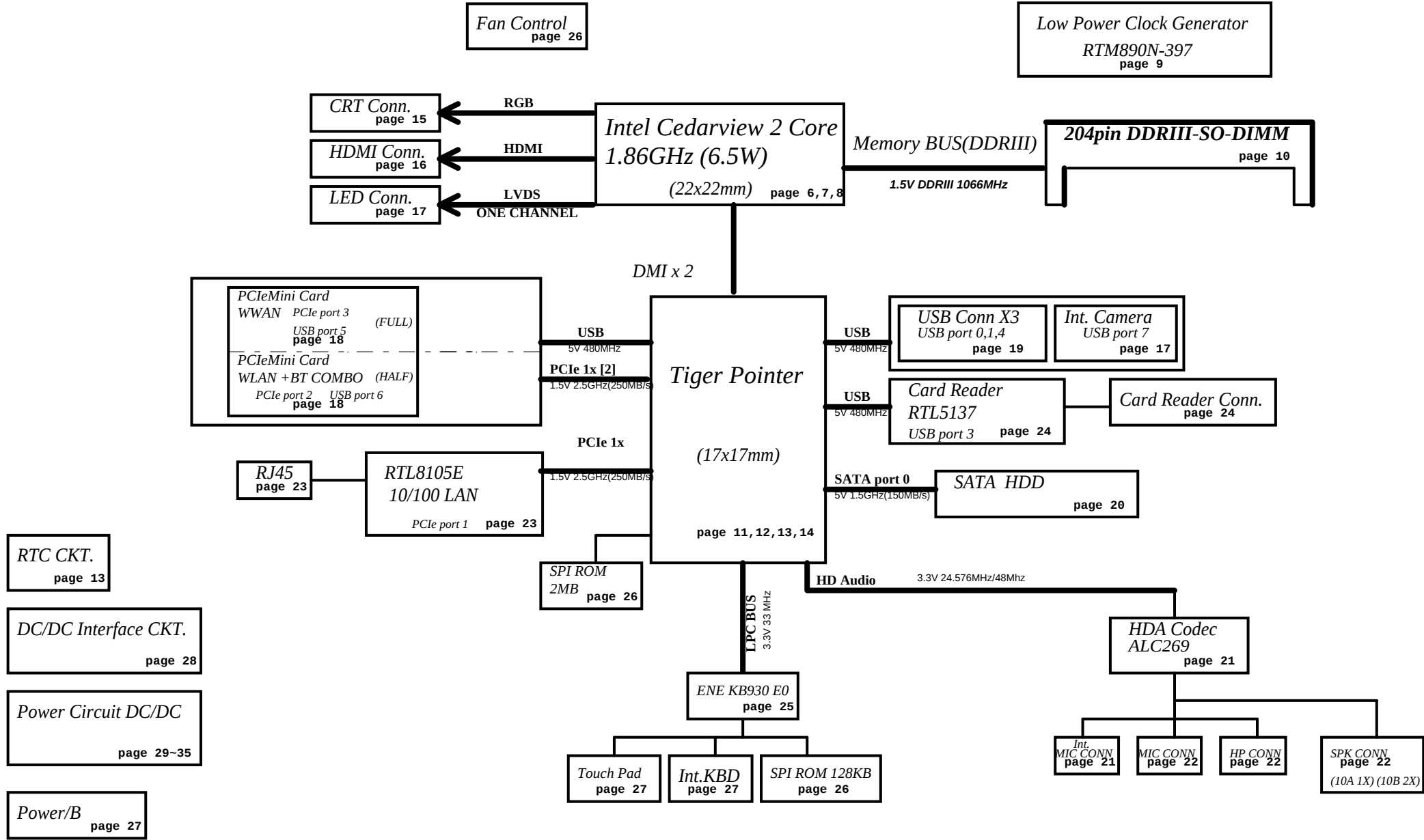
2011-11-07

LA-6859P REV:1.0

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Model Name : Cougar 2.0
Project Code : QBU00



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+GFX_CORE	GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	OFF	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+3VS_PRIME	3.3V power rail for CPU and PCH	ON	OFF	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT			Display		Clock gen	
description							
explain	Wi-Fi	WWAN	3G	CRT	HDMI	Tpye	
BTO	WLAN@	WWAN@	3G@	CRT@	HDMI@	low@	normal@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

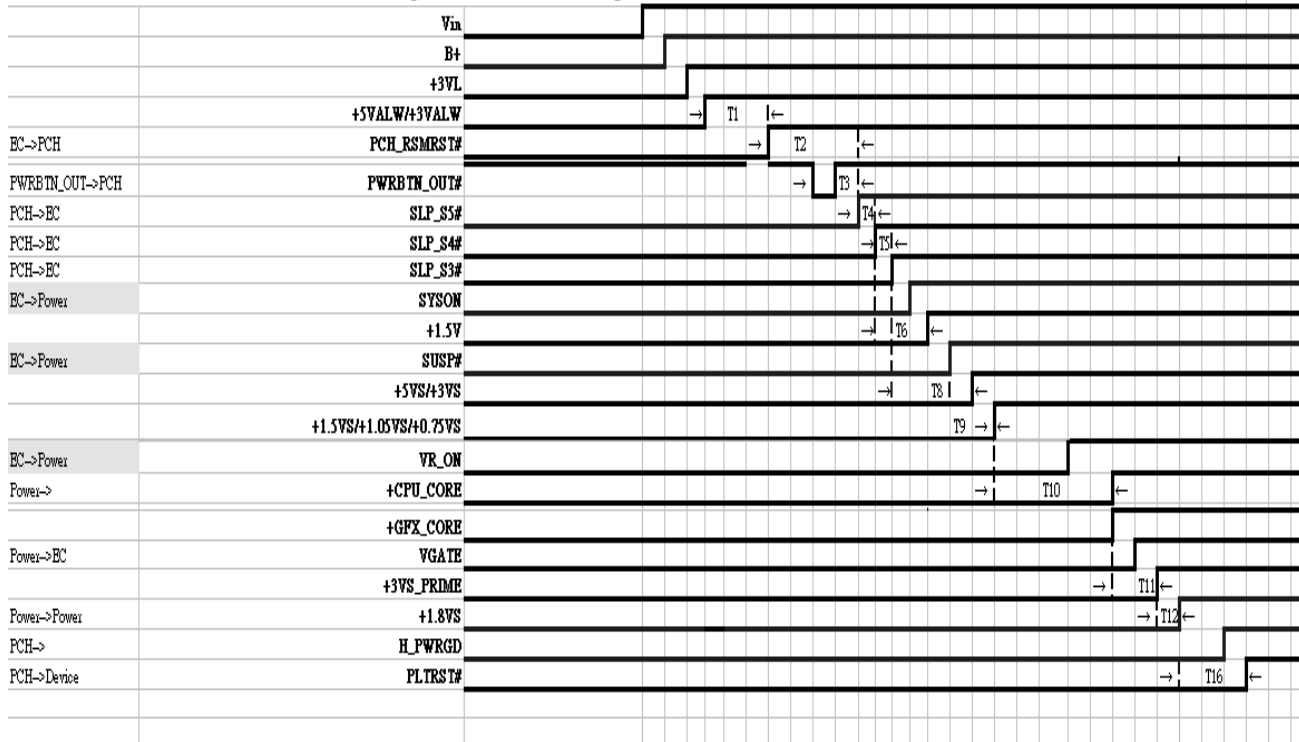
EC SM Bus2 address

NM10 SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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QBU00 Power ON sequence



Power-on Sequence

Time	Description	Expected
T1	+5V/3VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	>0ms
T4	SLP_S5# inactive to SLP_S4# inactive	28.992us ~ 64.088us
T5	SLP_S4# inactive to SLP_S3# inactive	28.992us ~ 64.088us
T6	SLP_S4# inactive to +1.5V active	>0ms
T8	SLP_S3# inactive to +5VS inactive	>0ms
T9	+1.5VS active to +1.05VS active	>0ms
T10	+1.05VS active to +CPU_CORE	>0ms
T11	+CPU_CORE active to +3.3V_PRIME	>0ms
T12	+3.3V_PRIME active to +1.8VS	3.3-1.8<700mV
T16	H_PWRGD inactive to PLTRST# inactive	34<RTCCLK<41

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Cougar Power Map

B+

DESIGN CURRENT 250mA

Ipeak=6.97A, Imax=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

TPS51125ARGER

** The SW just is reserved.
The power passes by jump or
0-ohm resistor.

WOL_EN#

** P-CHANNEL
A03413

DESIGN CURRENT 300mA

+3V_LAN

Ipeak=3.98A, Imax=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL
SI7326DN

DESIGN CURRENT 2286mA

+5VS

VGATE

APL5930KA

DESIGN CURRENT 151mA

+1.8VS

SUSP

N-CHANNEL
SI7326DN

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL
A03413

DESIGN CURRENT 2000mA

+LCD_VDD

VGATE#

N-CHANNEL
SI7326DN

DESIGN CURRENT 294mA

+3VS_PRIME

SUSP#

SY8033BDBC

Ipeak=1.308A, Imax=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR_ON

RT8165BGQW

Imax=3.5A

DESIGN CURRENT 4500mA

+CPU_COREP

DESIGN CURRENT 2000mA

+GFX_COREP

SYSON

G5603RU1U

Ipeak=19.6A, Imax=13.72A

DESIGN CURRENT 2270mA

+1.5VP +-5%

SUSP#

SI7326DN

DESIGN CURRENT 2112mA

+1.5VSP

SUSP

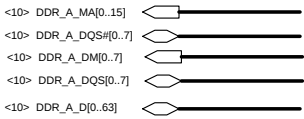
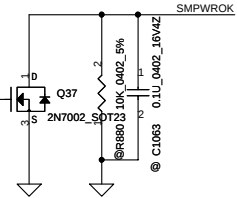
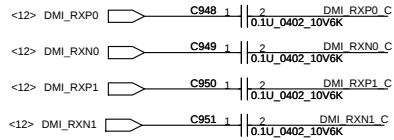
G2992F1U

DESIGN CURRENT 500mA

+0.75VSP

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+1.5V pull up must be placed within 500 mils from Cedarview



N2800@
U1
QB0Y B2 1.86G

U1B N2600@

CEDARVIEW

REV = 1.10

Q80Z B2 1.6G

1 OF 6

?

Y30 DDR A D0

Y29 DDR A D1

AC30 DDR A D2

AC31 DDR A D3

W31 DDR A D4

W28 DDR A D5

AB28 DDR A D6

AB30 DDR A D7

AA24 DDR A D8

AA22 DDR A D9

AE27 DDR A D10

AE26 DDR A D11

AA25 DDR A D12

AA25 DDR A D13

AA22 DDR A D14

AD22 DDR A D15

AD29 DDR A D16

AE29 DDR A D17

AJ30 DDR A D18

AK29 DDR A D19

AD28 DDR A D20

AD30 DDR A D21

AG30 DDR A D22

AJ29 DDR A D23

AE24 DDR A D24

AG24 DDR A D25

AD22 DDR A D26

AC21 DDR A D27

AG27 DDR A D28

AG25 DDR A D29

AG21 DDR A D30

AE21 DDR A D31

AD13 DDR A D32

AD11 DDR A D33

AG8 DDR A D34

AG7 DDR A D35

AG13 DDR A D36

AE13 DDR A D37

AD10 DDR A D38

AE8 DDR A D39

AE8 DDR A D40

AD2 DDR A D41

AD2 DDR A D42

AD3 DDR A D43

AD4 DDR A D44

AE4 DDR A D45

AE2 DDR A D46

AD4 DDR A D47

AD7 DDR A D48

AD6 DDR A D49

AA6 DDR A D50

AB5 DDR A D51

AE8 DDR A D52

AE5 DDR A D53

AB9 DDR A D54

AA8 DDR A D55

AB2 DDR A D56

AB4 DDR A D57

W4 DDR A D58

V3 DDR A D59

AC2 DDR A D60

AB3 DDR A D61

Y2 DDR A D62

W1 DDR A D63

AA30 DDR A DQ50

AB24 DDR A DQ51

AE30 DDR A DQ52

AE22 DDR A DQ53

AG10 DDR A DQ54

AE4 DDR A DQ55

AB6 DDR A DQ56

Y3 DDR A DQ57

AA31 DDR A DQ58

AB25 DDR A DQ59

AE29 DDR A DQ60

AE22 DDR A DQ61

AE10 DDR A DQ62

AE3 DDR A DQ63

AB7 DDR A DQ64

AA2 DDR A DQ65

DDR3_DQ50

DDR3_DQ51

DDR3_DQ52

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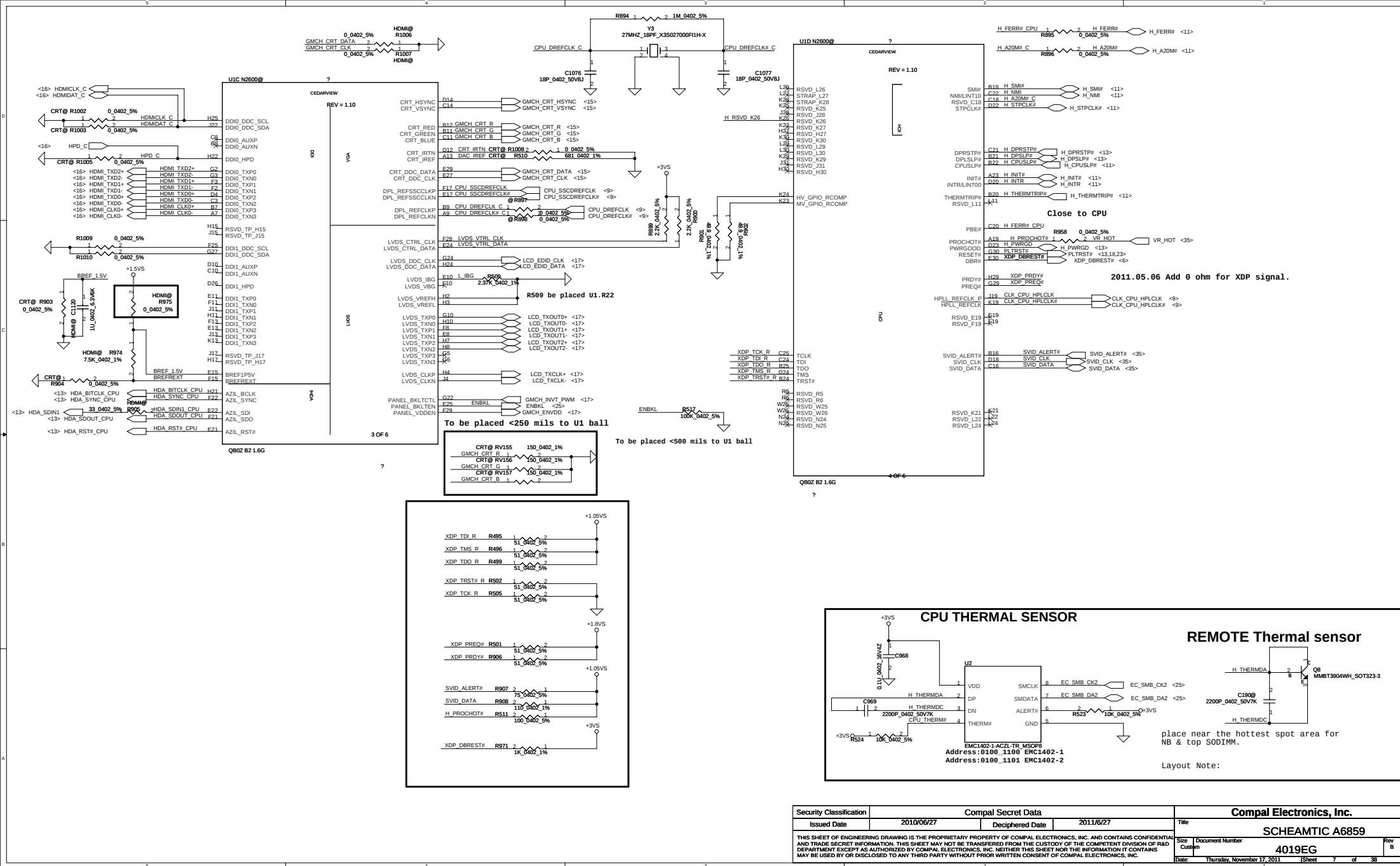
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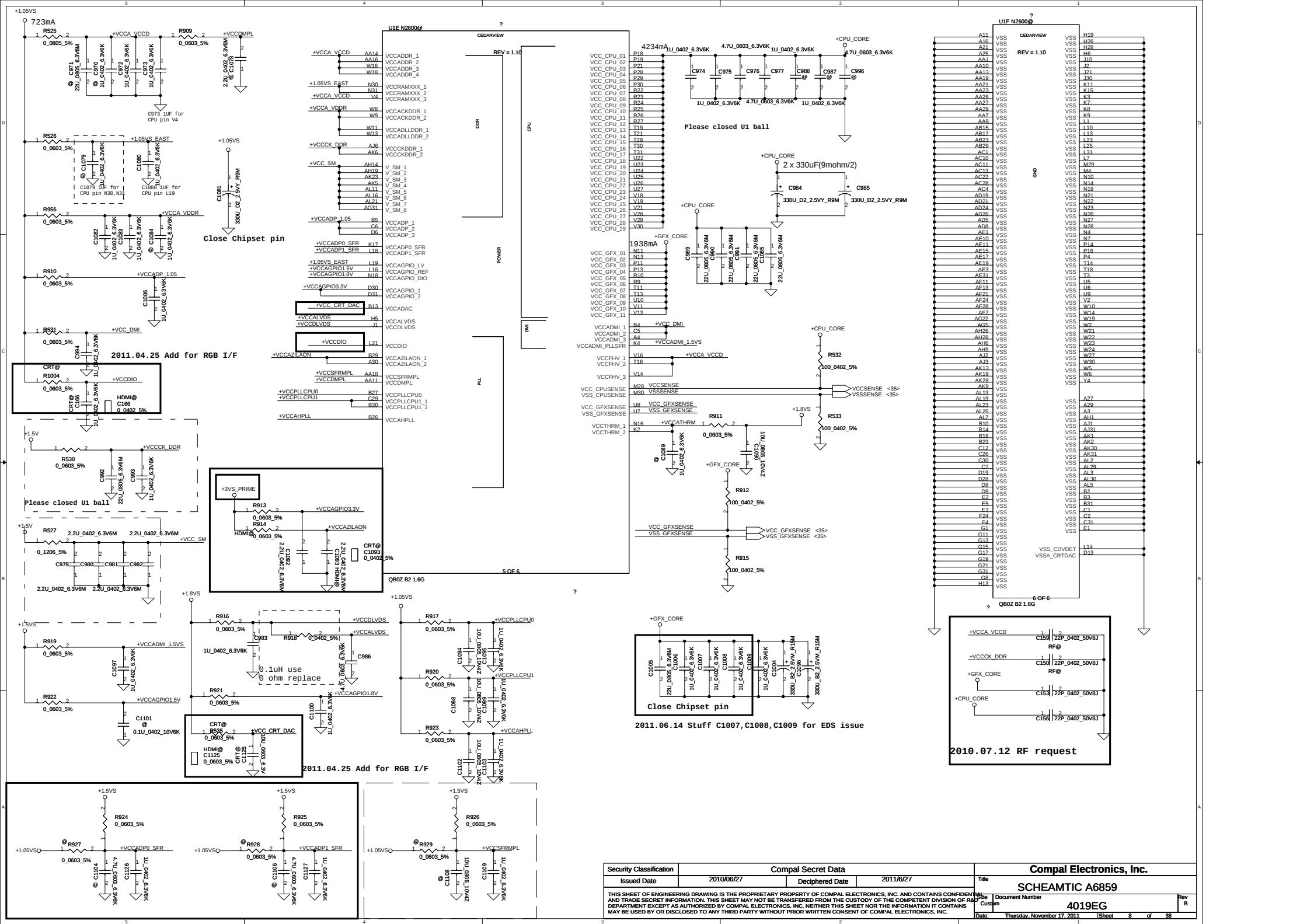
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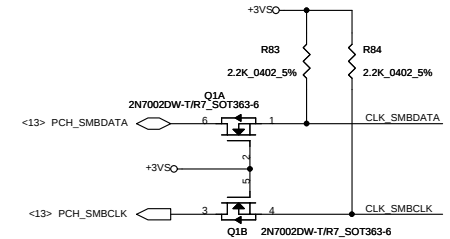
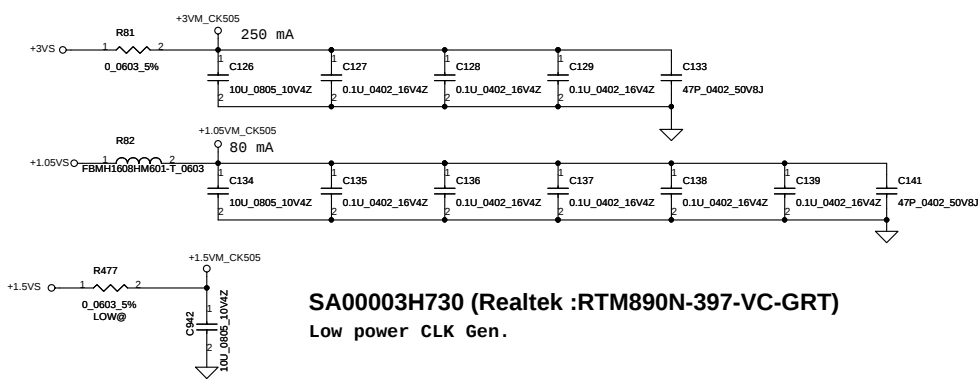


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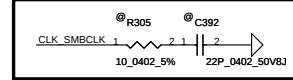


FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff

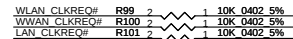


2011.04.29 Reserve R305,C392 for RF



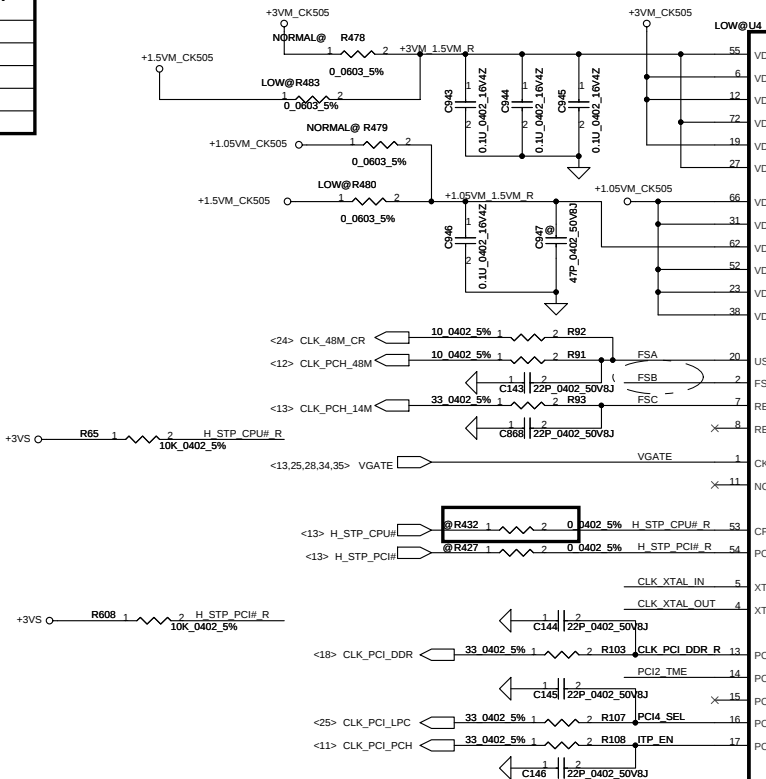
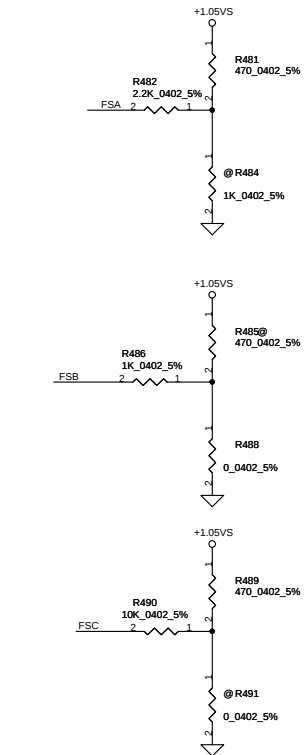
SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	
SRC3	CPU_EXP
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

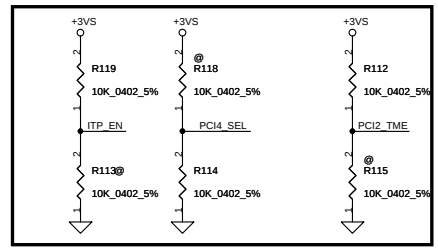


REQ PORT LIST

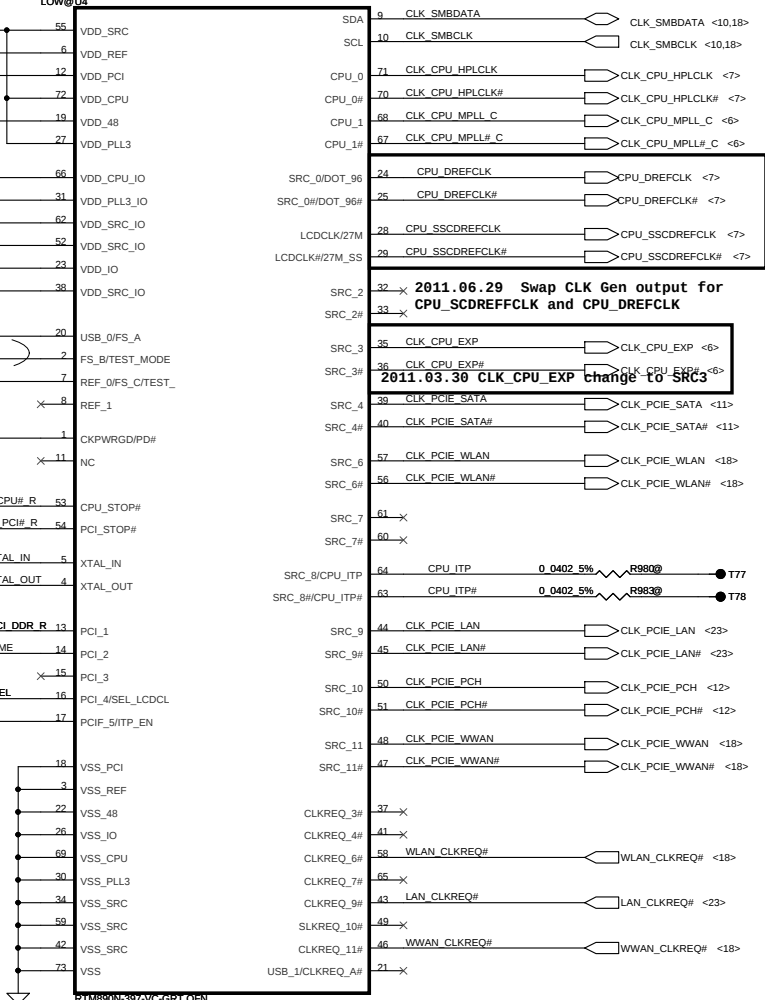
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	



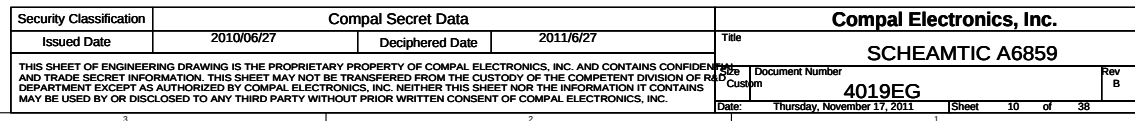
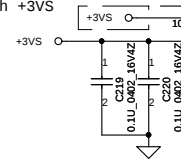
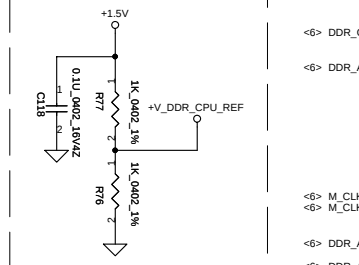
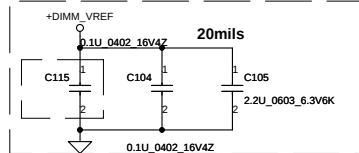
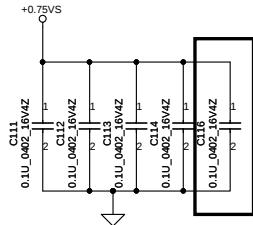
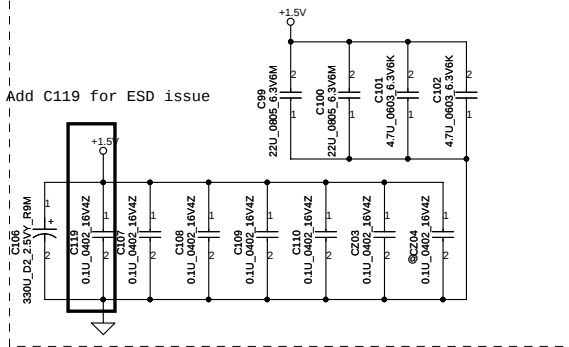
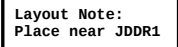
For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS
For PCI2_TME:0=Overclocking of CPU and SRC allowed (ICS only) 1=Overclocking of CPU and SRC NOT allowed

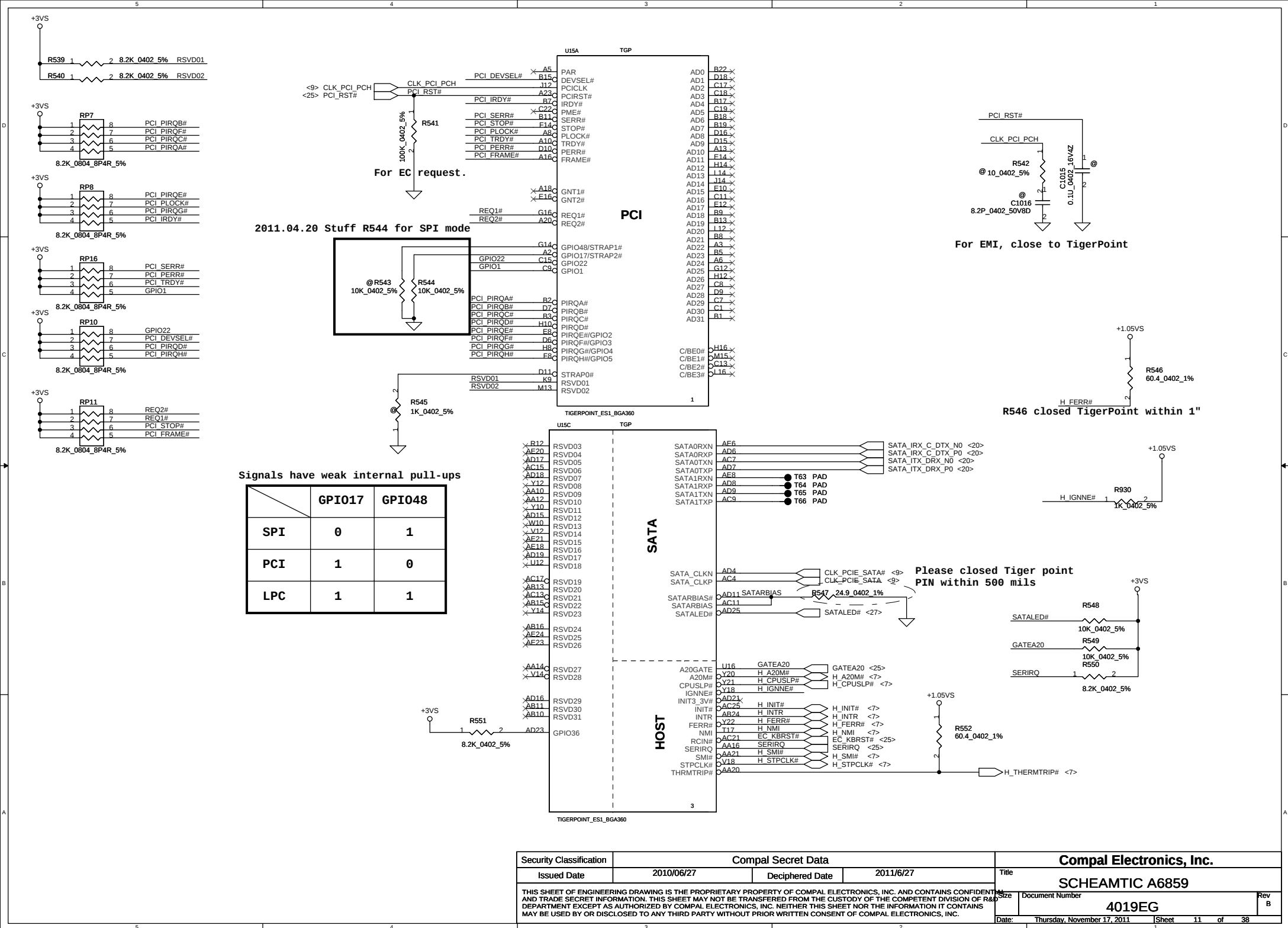


Routing the trace at least 10mil



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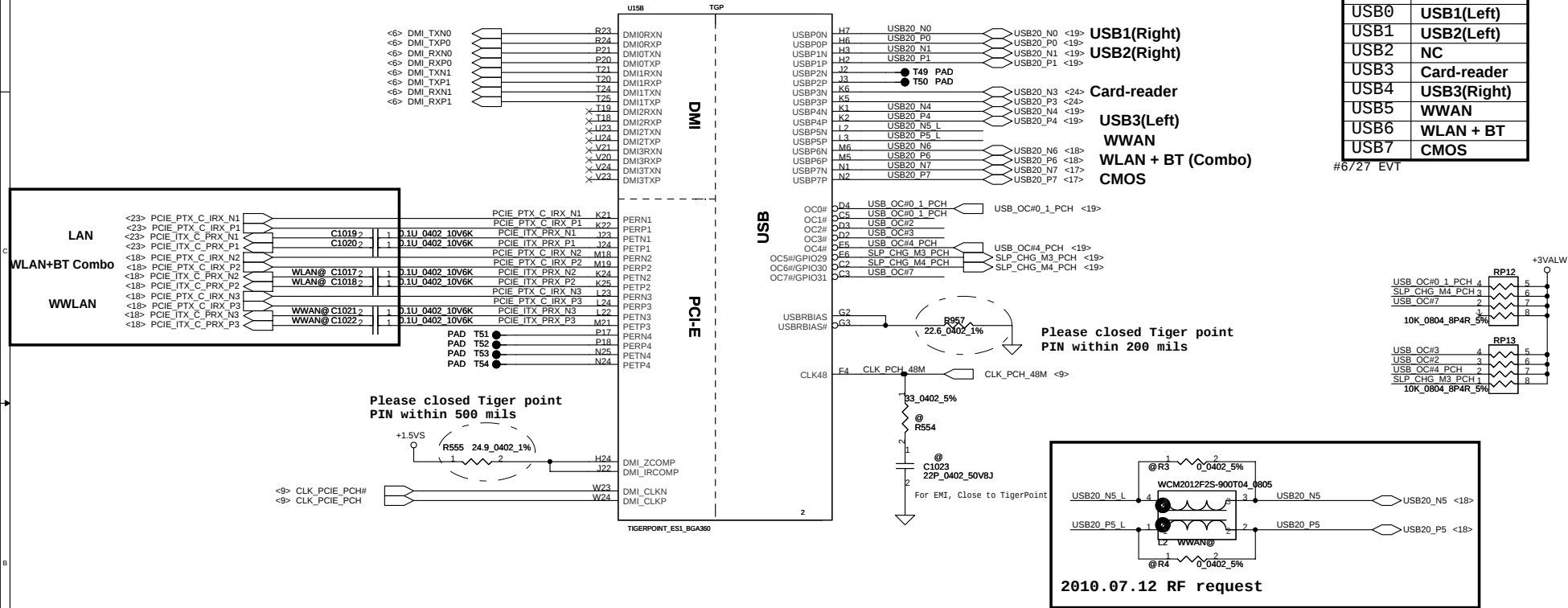


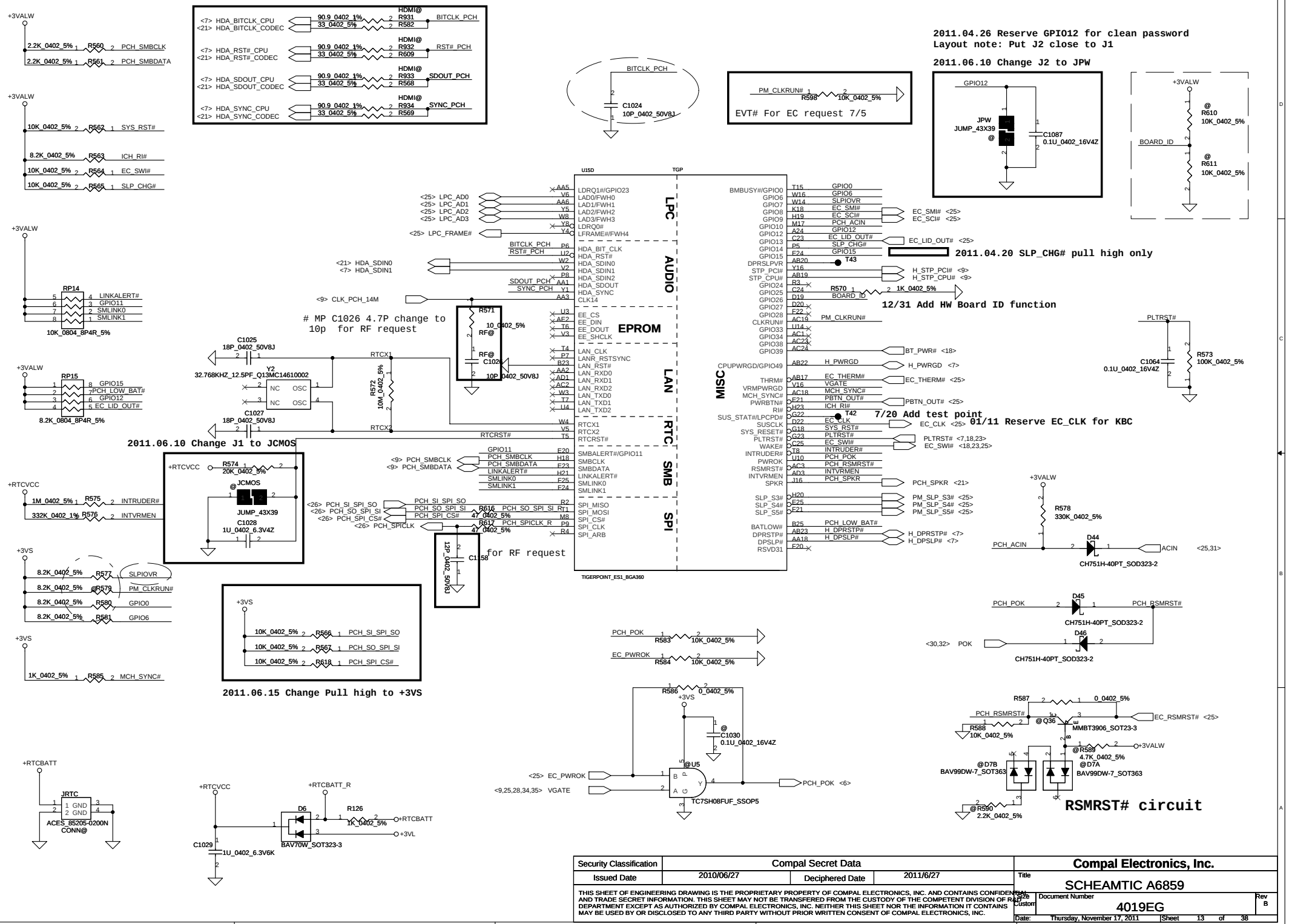


USB PORT LIST

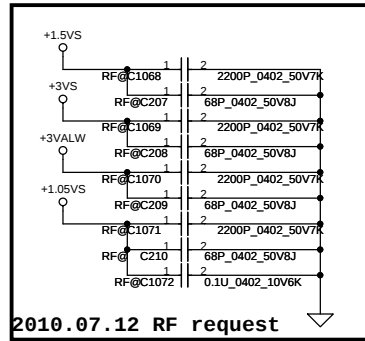
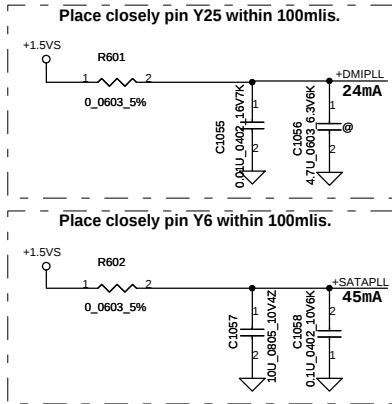
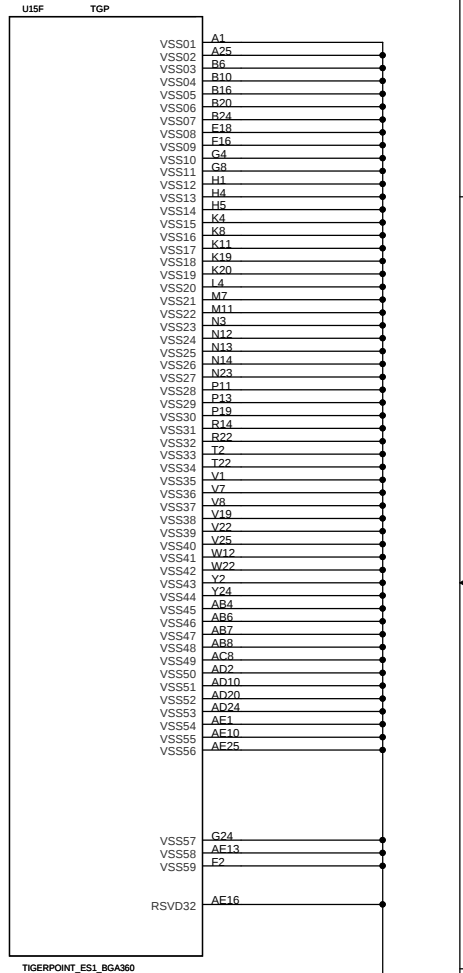
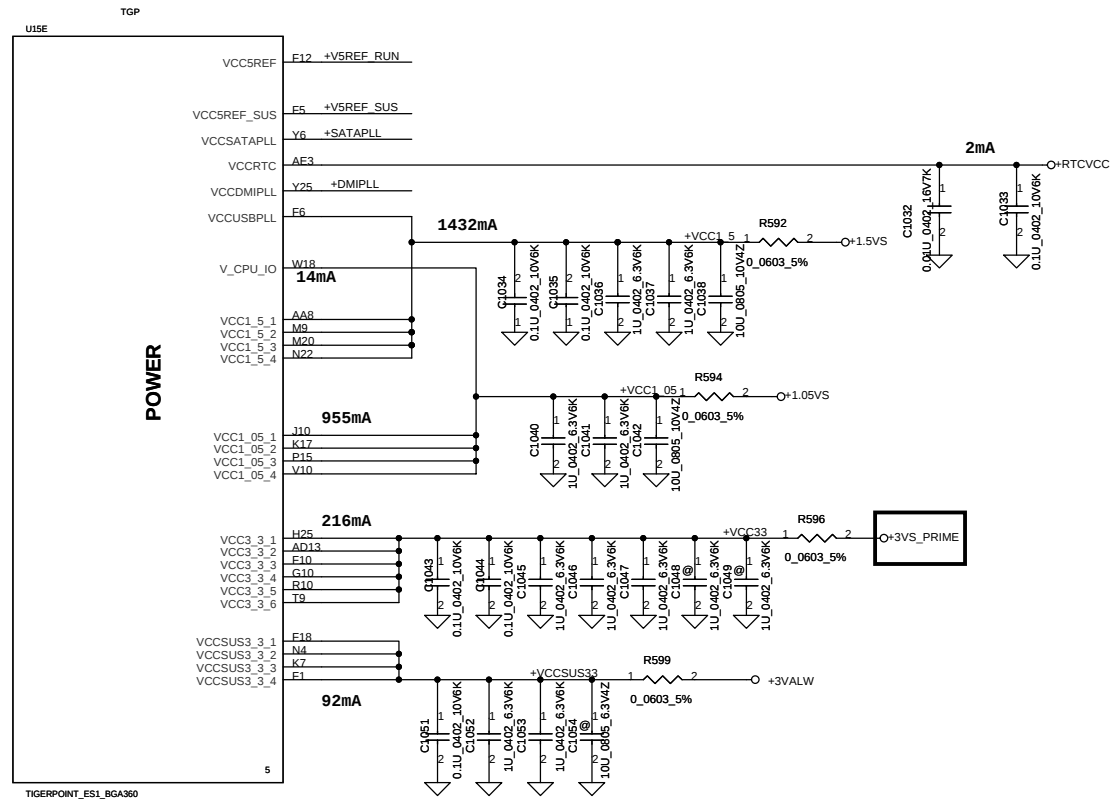
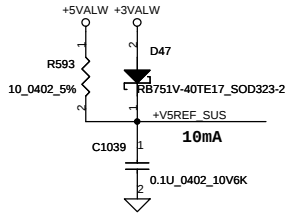
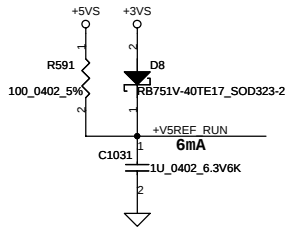
PORT	#EVT	DEVICE
USB0		USB1(Left)
USB1		USB2(Left)
USB2		NC
USB3		Card-reader
USB4		USB3(Right)
USB5		WWAN
USB6		WLAN + BT
USB7		CMOS

#6/27 EVT



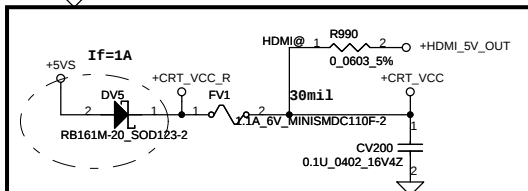


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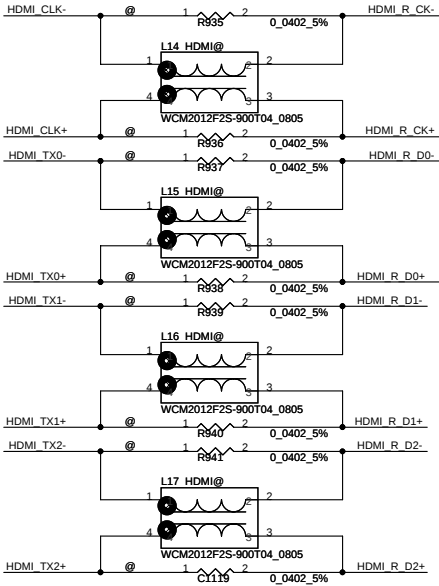
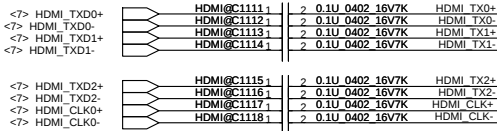
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				Date	Thursday, November 17, 2011
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A	B	C	D	E
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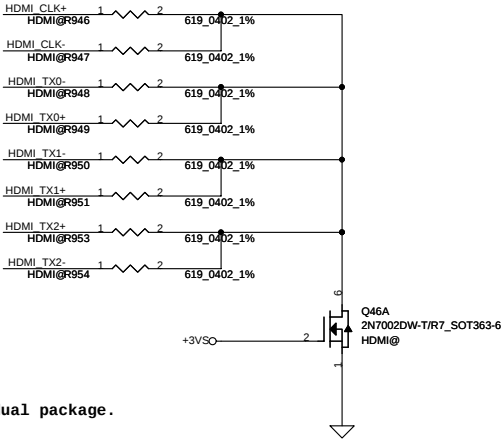
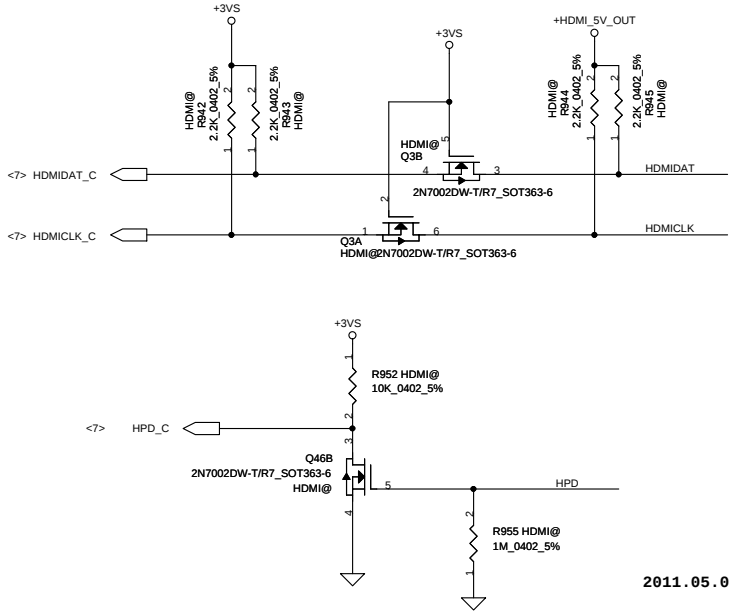
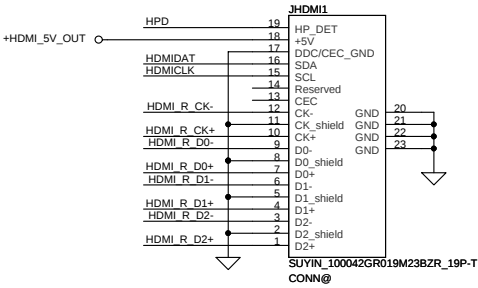


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HDMI CONNECTOR



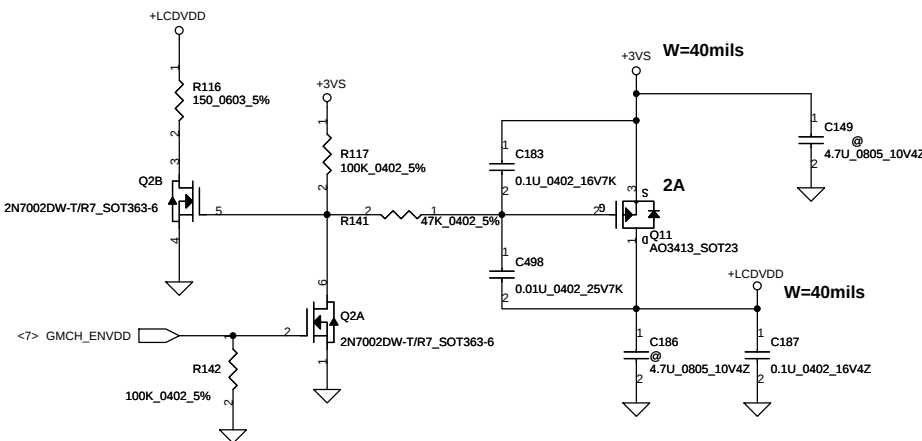
< HDMI Connector >



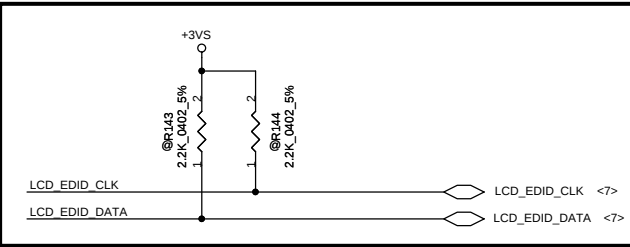
2011.05.04 Change Q42,Q43 to dual package.

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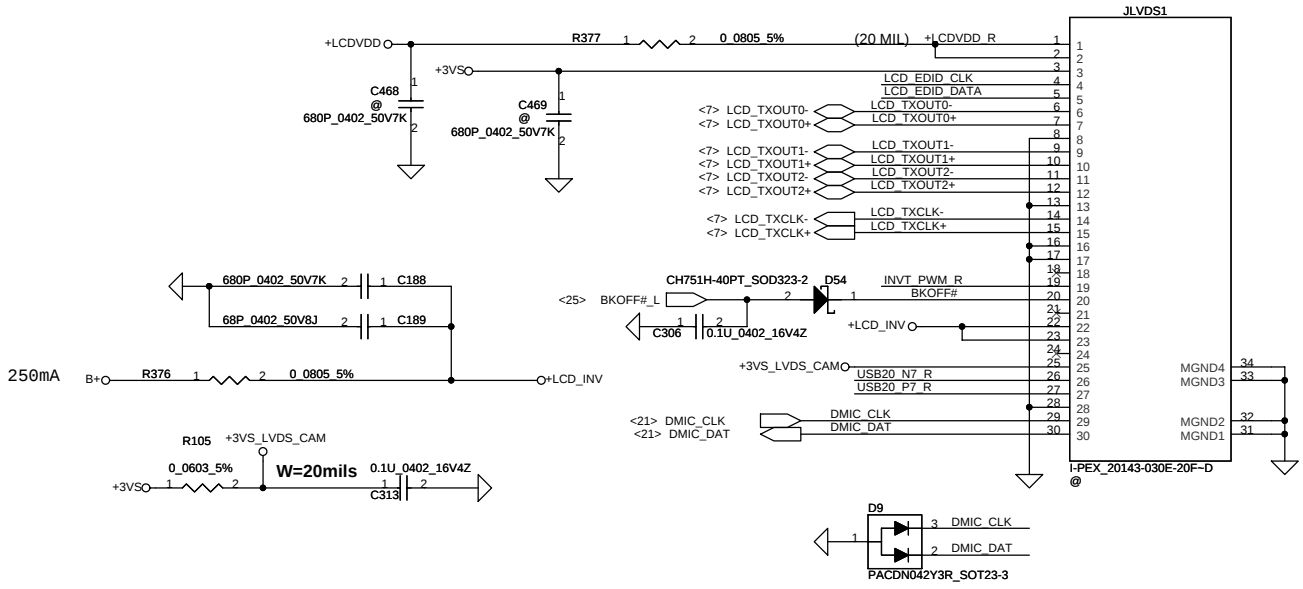
LCD POWER CIRCUIT



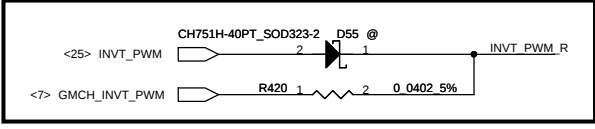
2011.05.22 Remove EDID pull up resistors for Intel issue



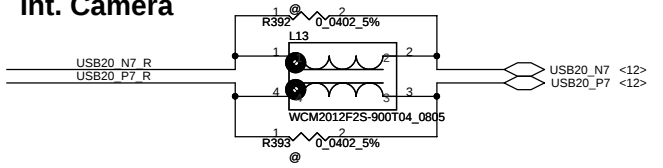
LED/PANEL BD. Conn.



2011.05.20 LCD brightness will controlled by CPU(DPST)

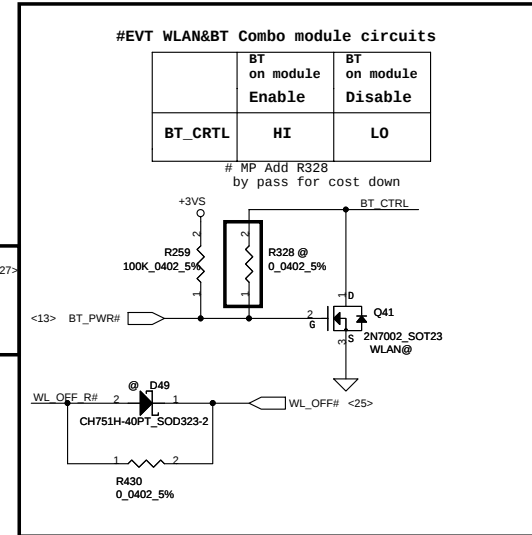


Int. Camera

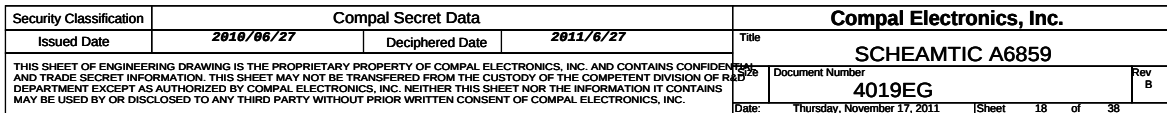


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```
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@
```

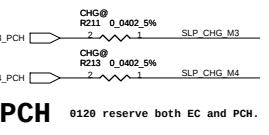
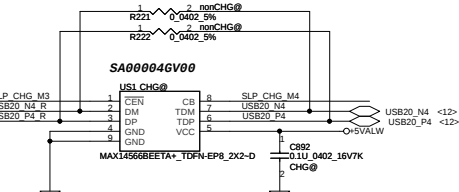


3G current need to 2750mA 3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@

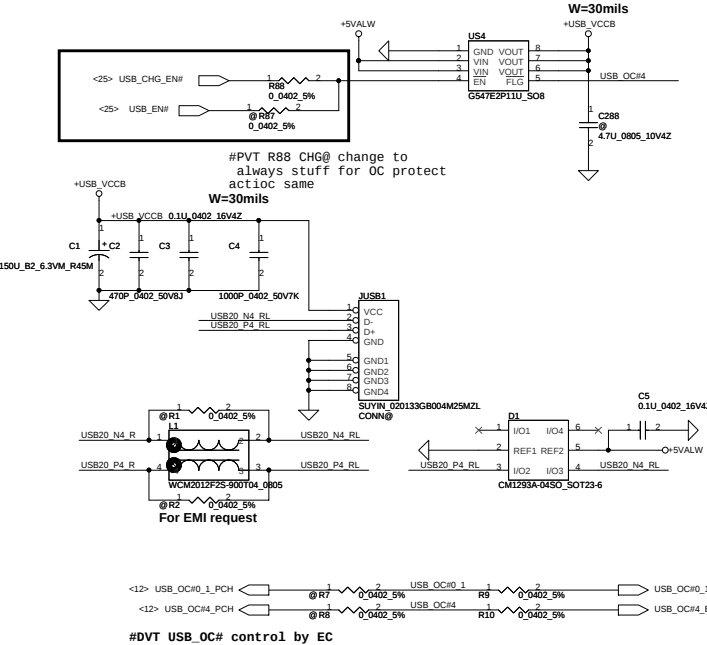
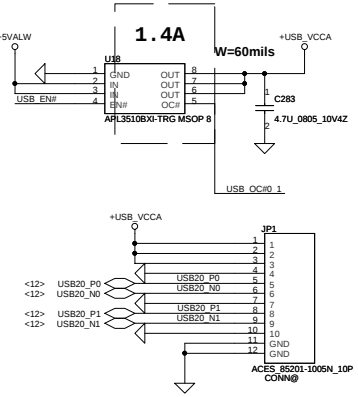


USB Sleep & Charge
Auto-Mode
Mode3

MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

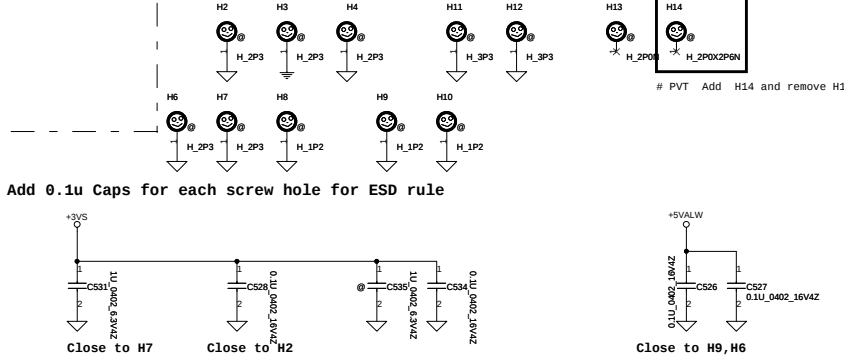


USB CONN

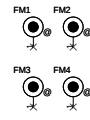


For EMI request
2/3 DVT: Change D38, D37 from PRT85V0U2X_S0T143-4 to CM1293A-04S0_S0T23-6

For EMI request

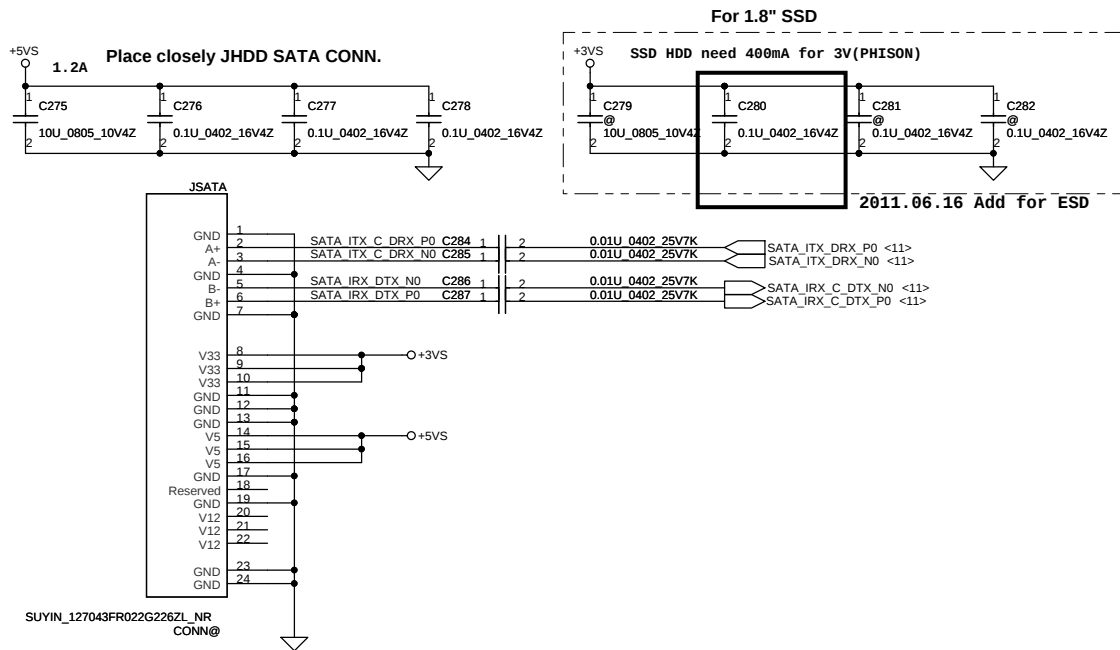


FIDUCIAL_C40M80



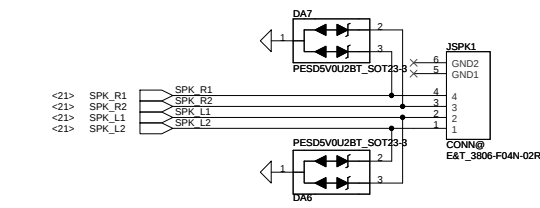
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SATA Conn.

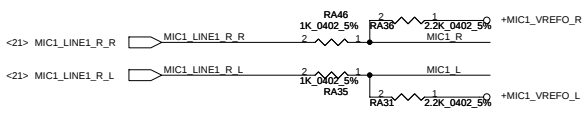


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4019EG		SCHEAMTIC A6859			

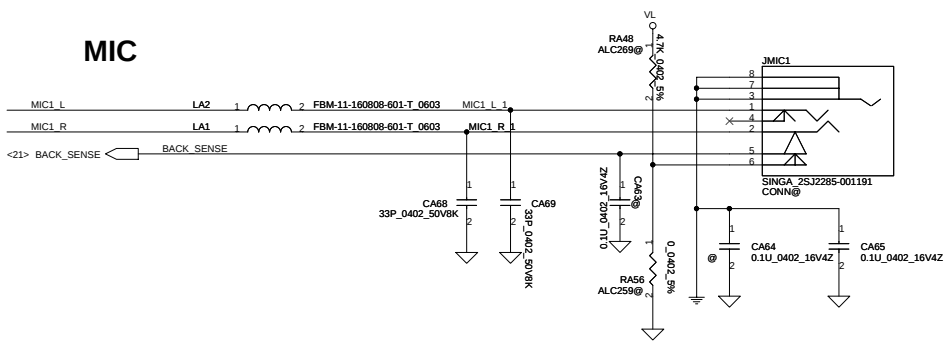
SPEAKER



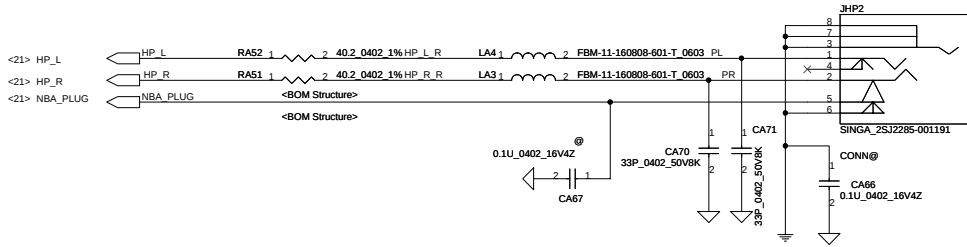
Ext.MIC/LINE IN JACK



MIC

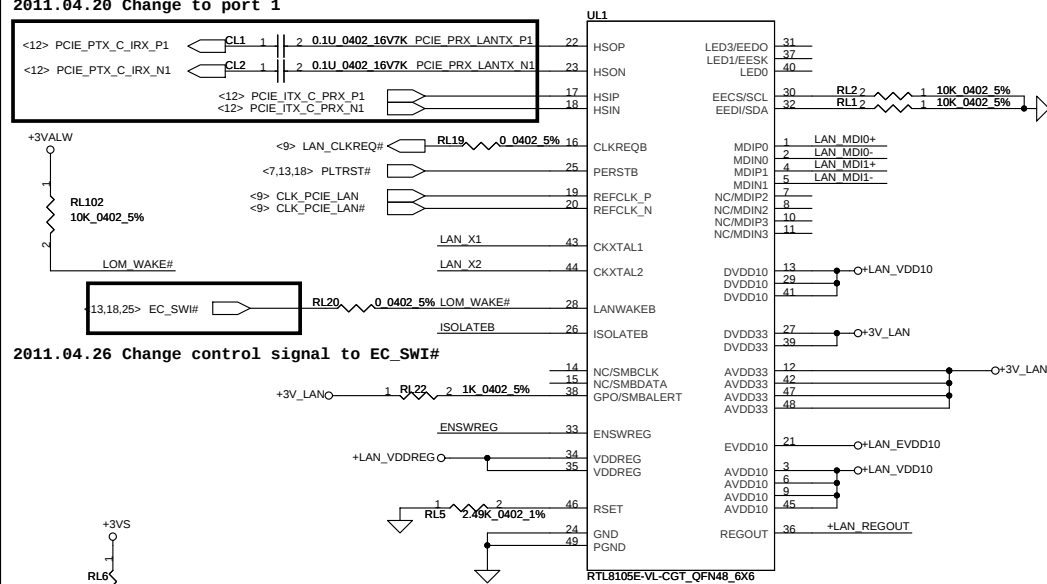


Head phone

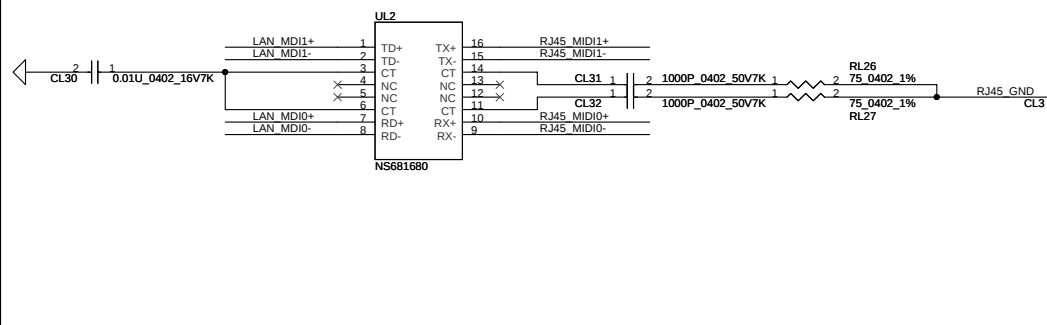
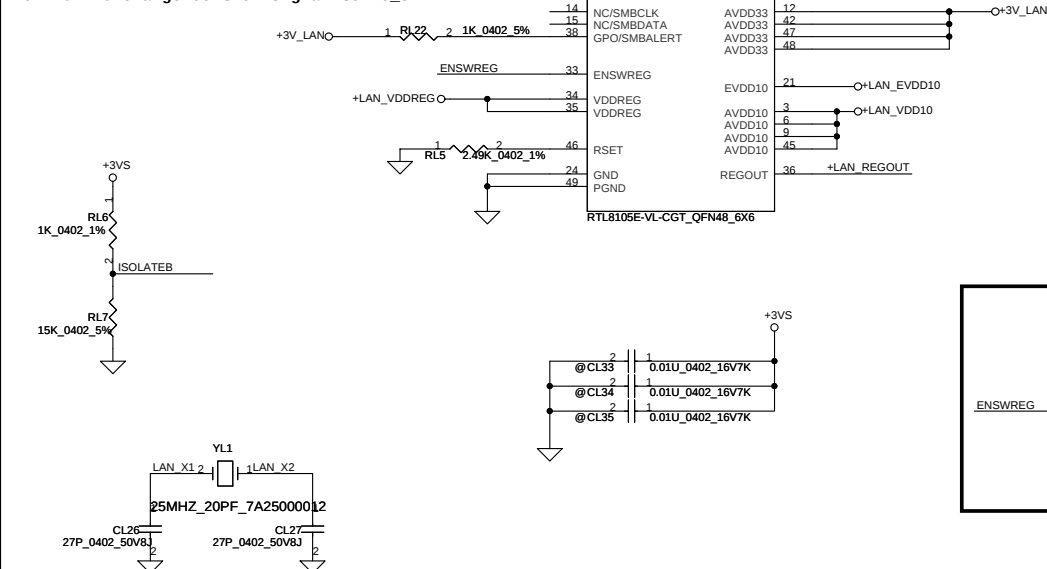


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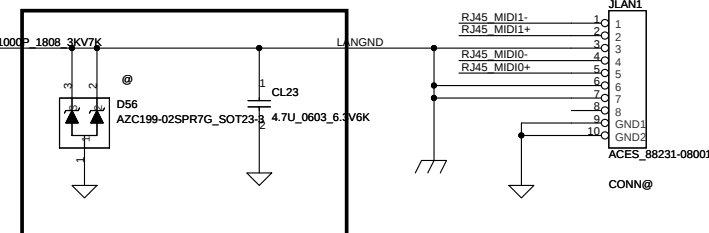
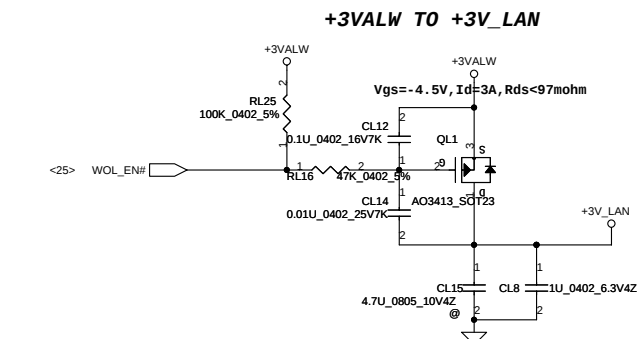
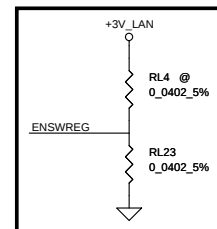
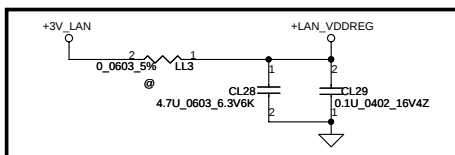
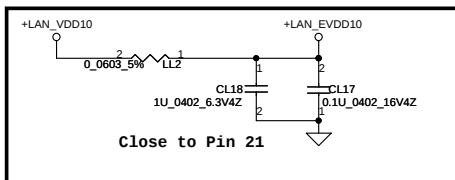
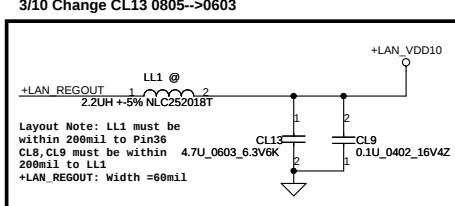
2011.04.20 Change to port 1



2011.04.26 Change control signal to EC_SWI#



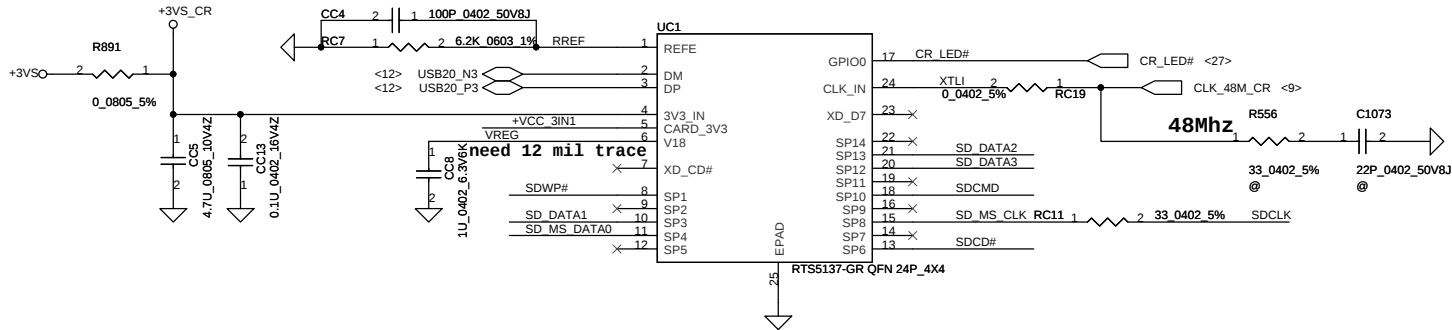
3/10 Change CL13 0805-->0603



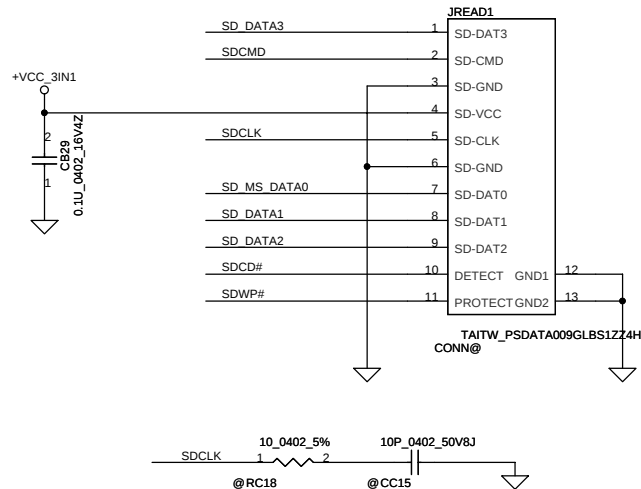
2011/04/18 Add D56 for ESD request

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	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CEF	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

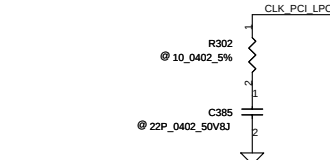


2 in 1 Card Reader



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<18> LPC_FRAME#_R LPC_FRAME#_R 1 2 LPC_FRAME#
 0.0402_5% DEBUG@ R310
 <18> LPC_AD3_R LPC_AD3_R 1 2 LPC_AD3
 0.0402_5% DEBUG@ R311
 <18> LPC_AD2_R LPC_AD2_R 1 2 LPC_AD2
 0.0402_5% DEBUG@ R315
 <18> LPC_AD1_R LPC_AD1_R 1 2 LPC_AD1
 0.0402_5% DEBUG@ R316
 <18> LPC_AD0_R LPC_AD0_R 1 2 LPC_AD0
 0.0402_5% DEBUG@ R317

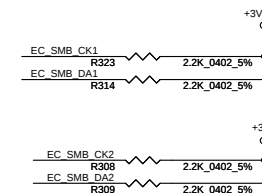


2011.04.26 Reserve GPIO to control LED



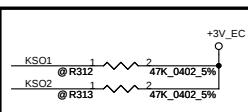
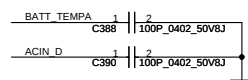
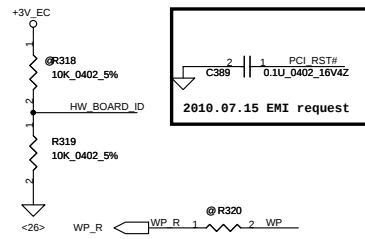
<26> KSI[0..15] KSI[0..15]
 <26> KSI[0..7] KSI[0..7]

confirm battery team change +5VALW to +3VALW

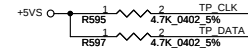
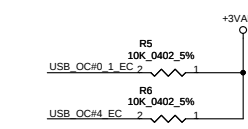
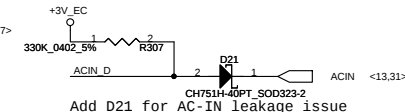
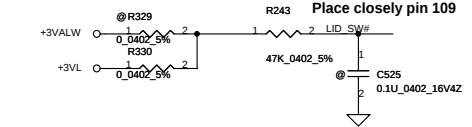
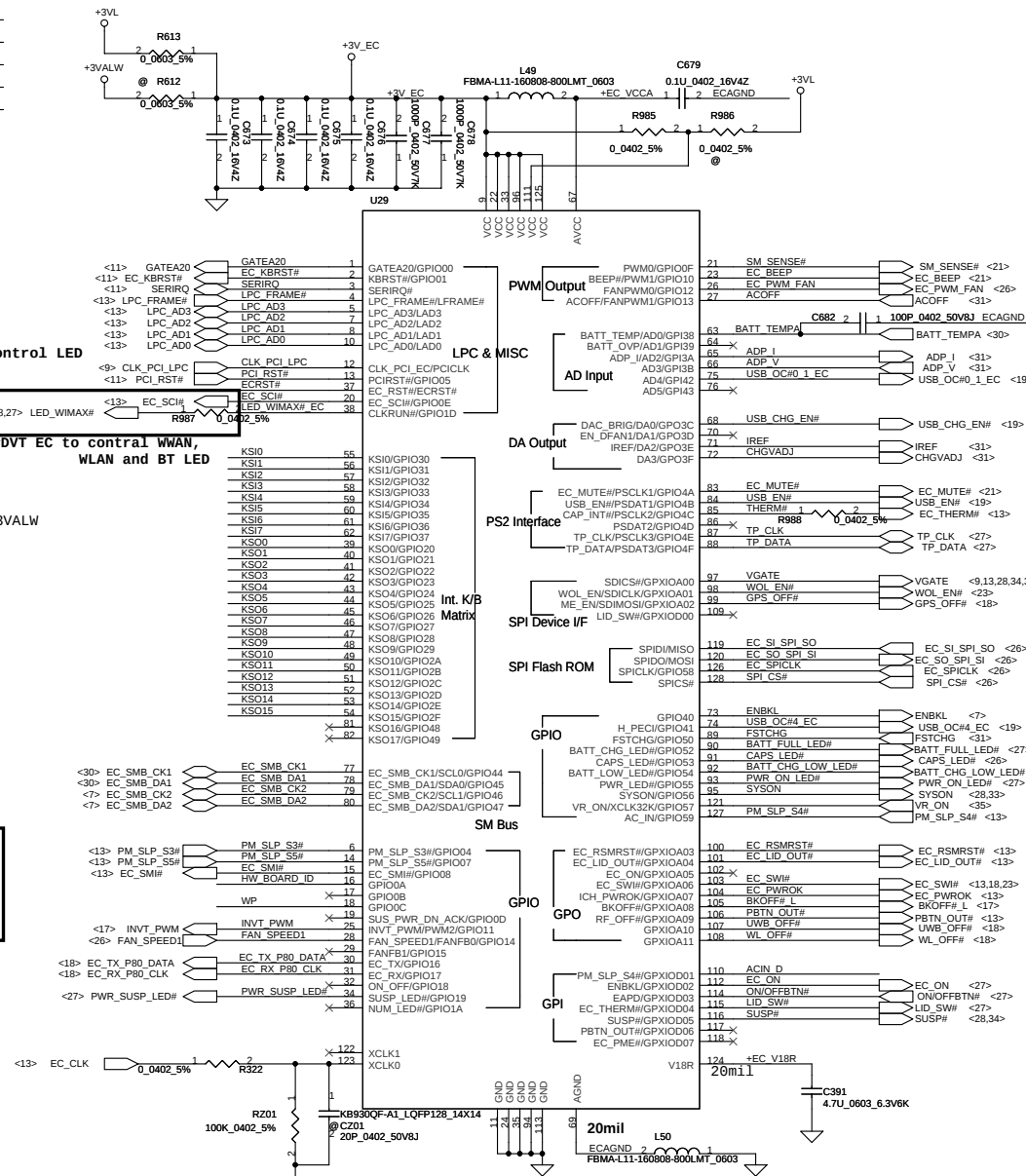


For EC recommend 10/17

01/06 Add HW board ID in EC pin16

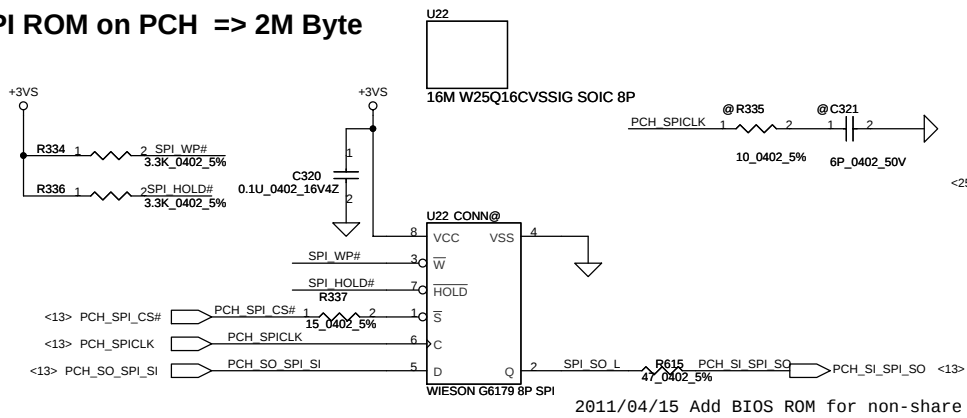


2011.08.29 Un-stuff R312,R313, KB930 dosen't need pull high



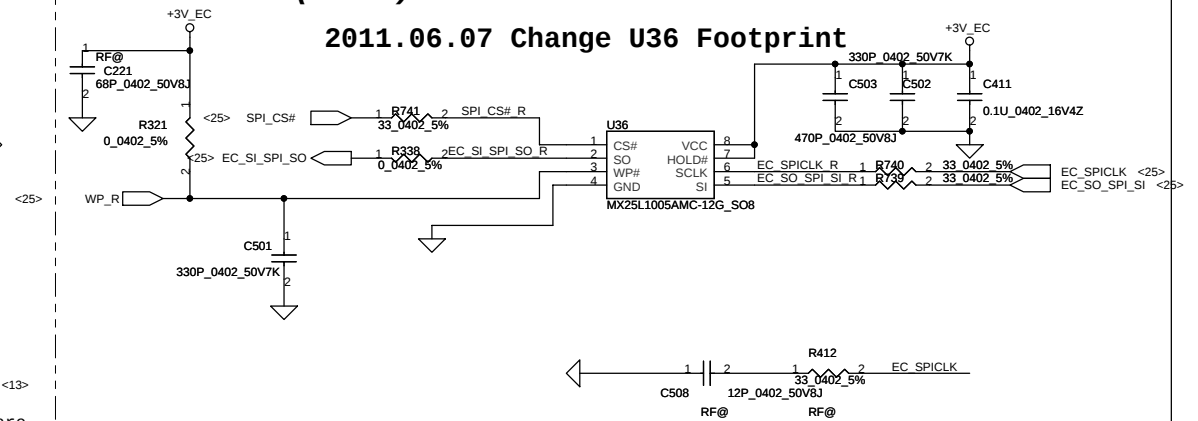
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SPI ROM on PCH => 2M Byte

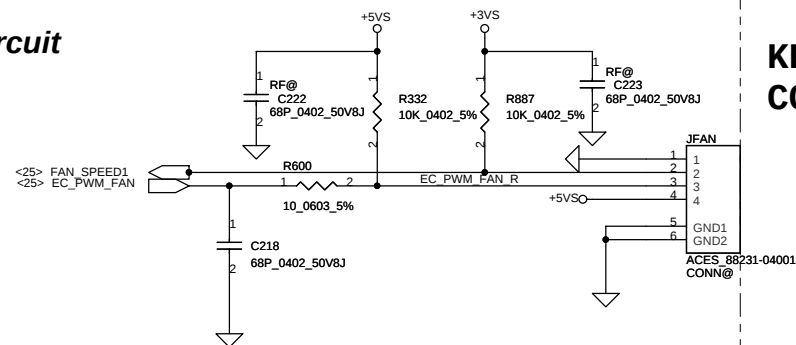


SPI Flash (1Mb*1)

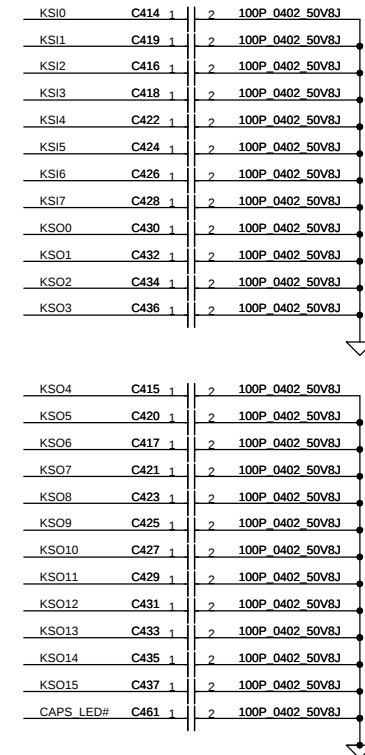
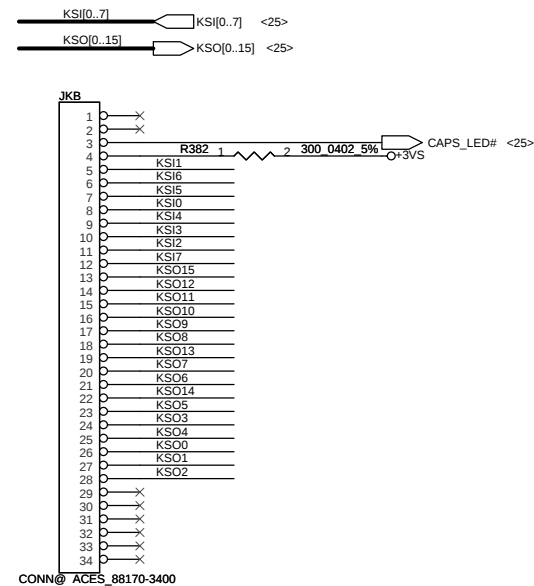
2011.06.07 Change U36 Footprint



FAN Control Circuit

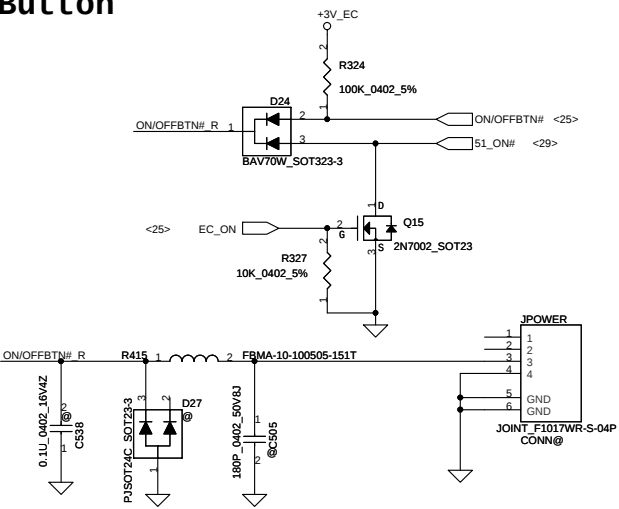


**KEYBOARD
CONN.**

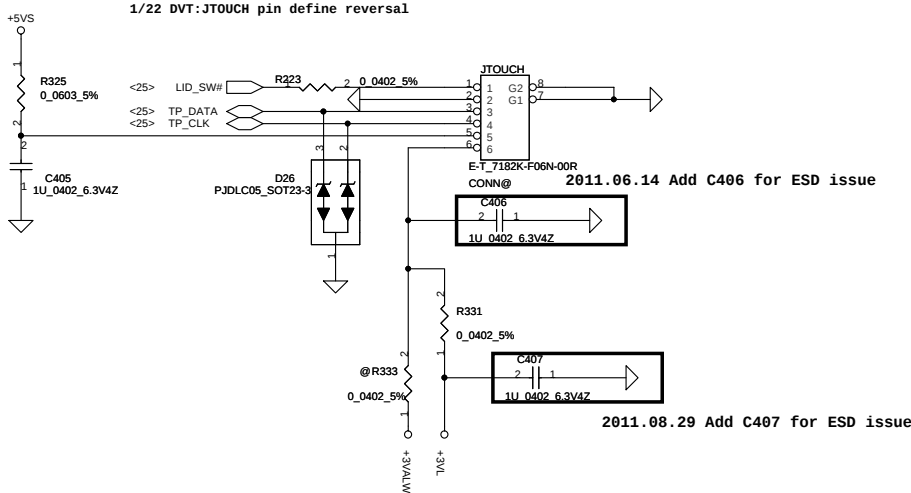


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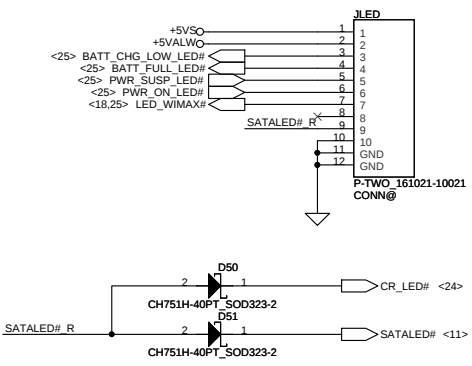
Power Button



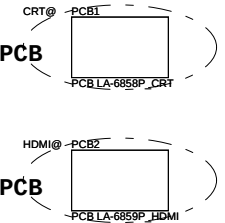
Touch/B Connector



LED Conn



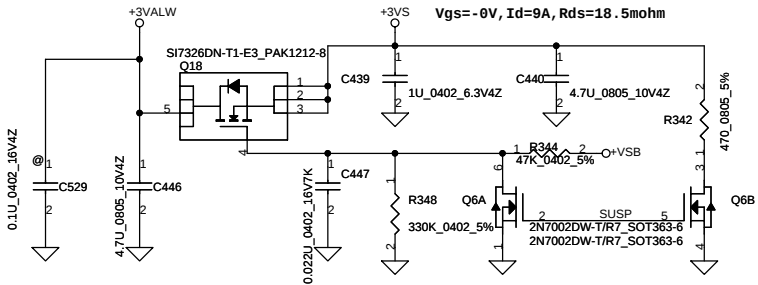
ISPD



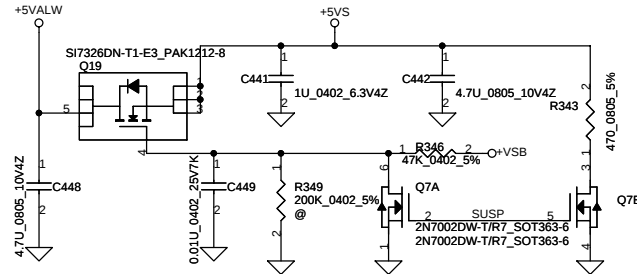
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+3VALW TO +3VS

Vgs=-0V, Id=9A, Rds=18.5mohm

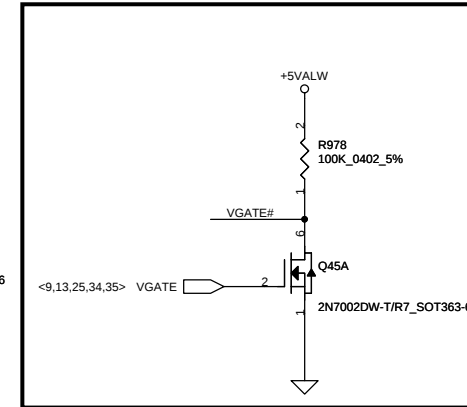
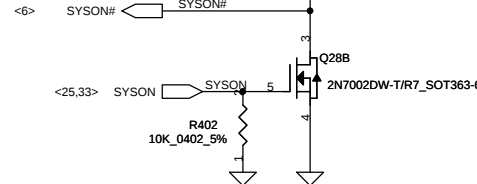
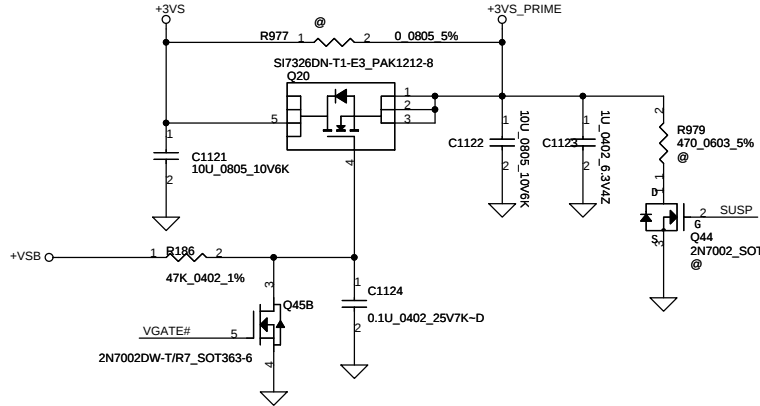


+5VALW TO +5VS

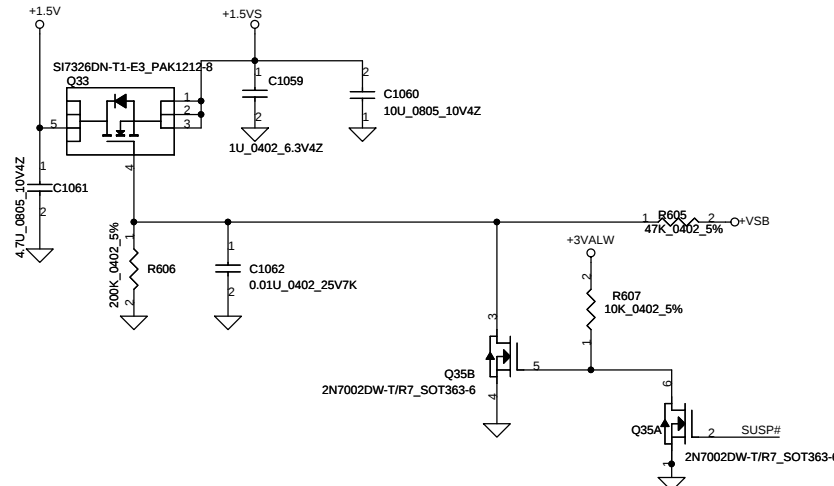


4/2 MP:For EMI ESD solution

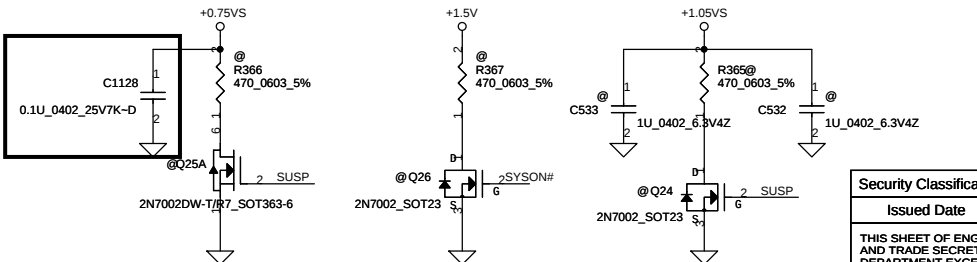
+3VS TO +3VS_PRIME



+1.5V TO +1.5VS

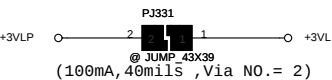
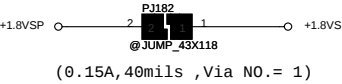
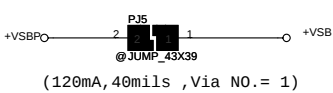
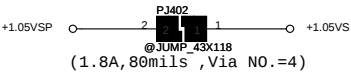
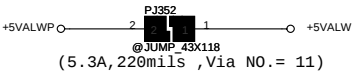
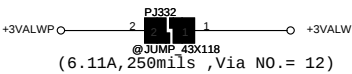
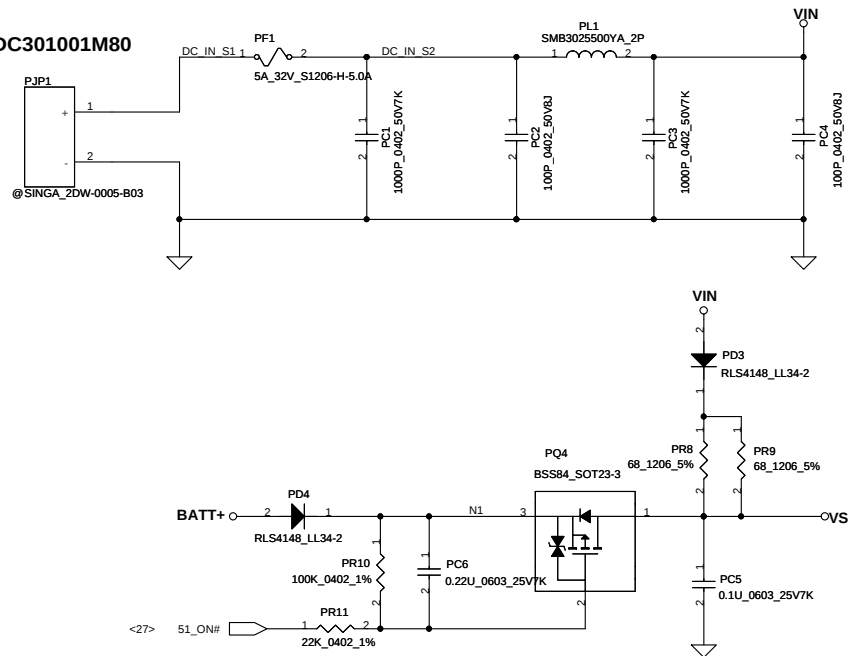


2011.06.14 Add C1128 for ESD issue

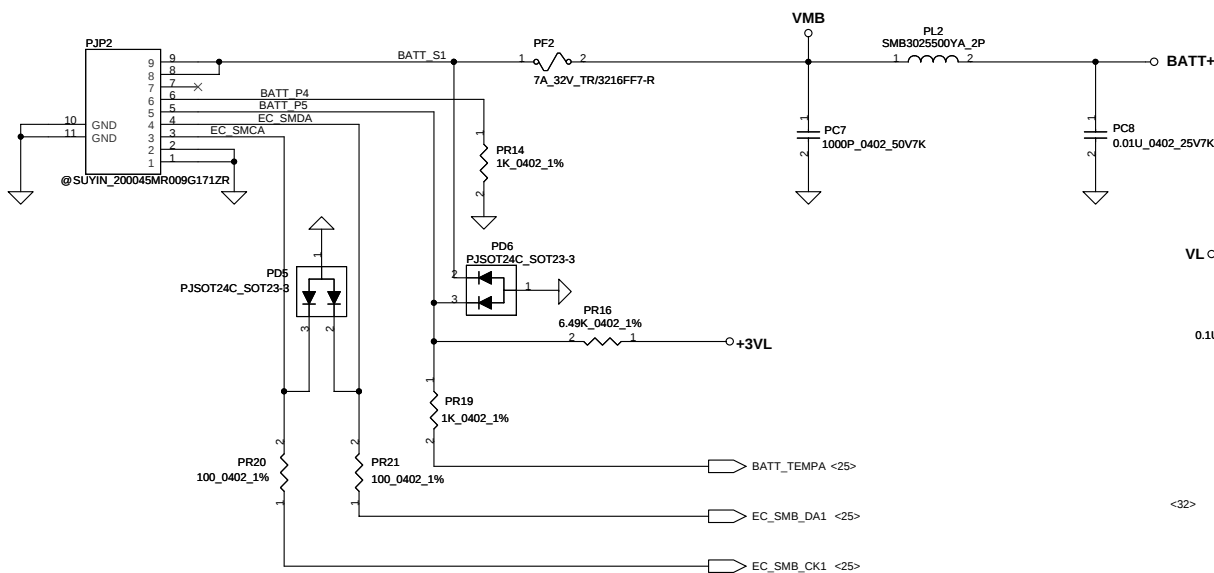


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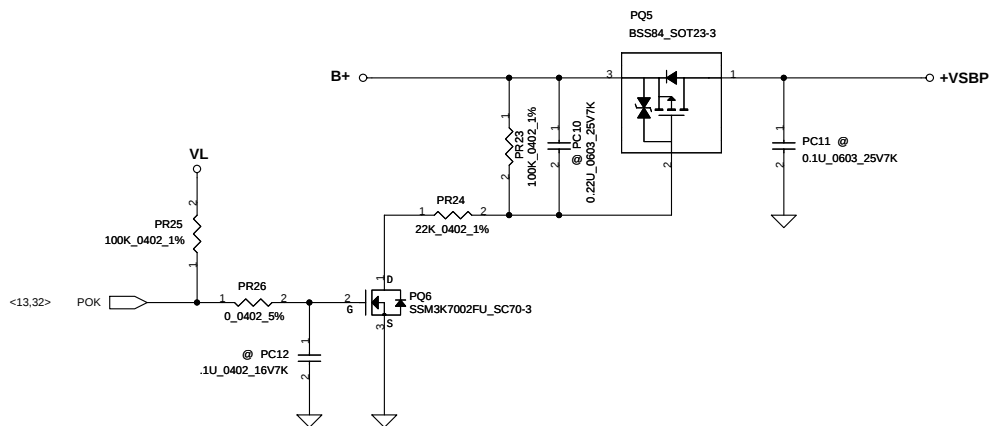
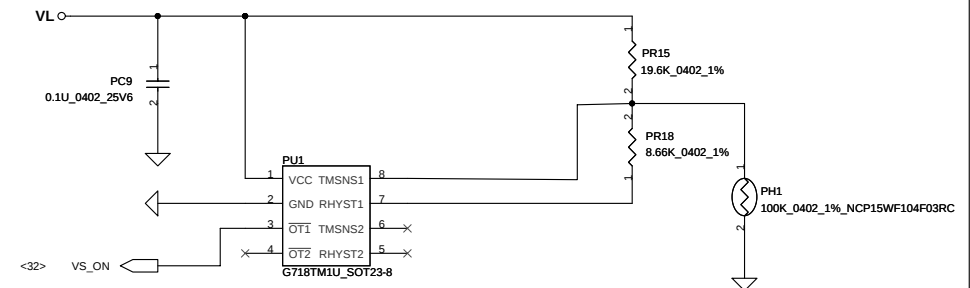
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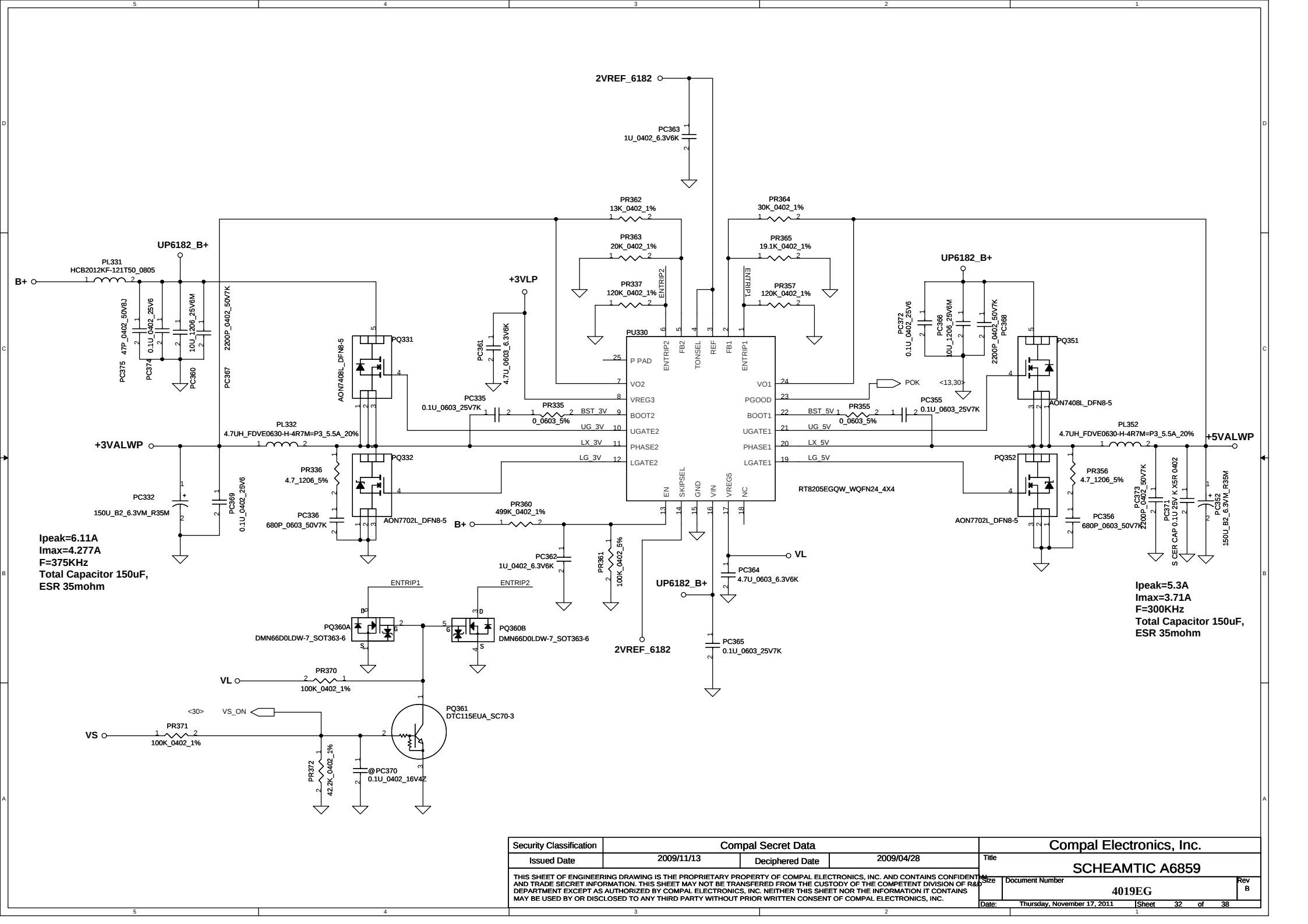
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PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C



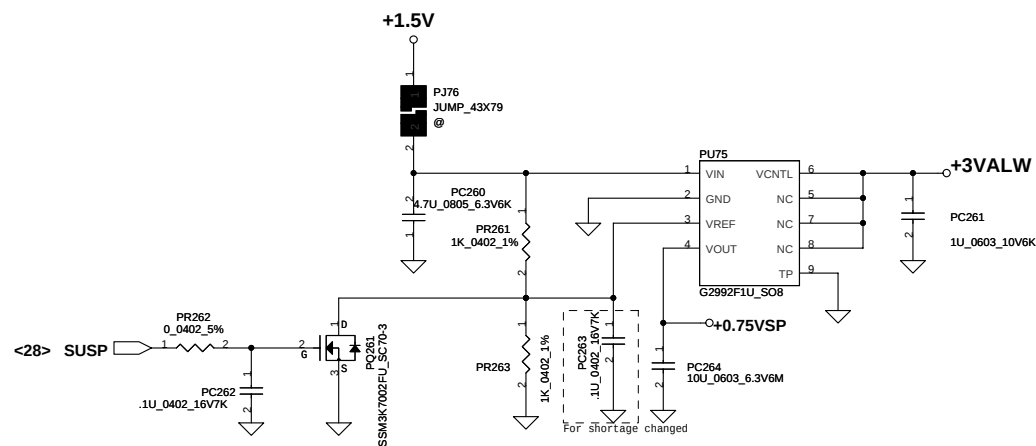
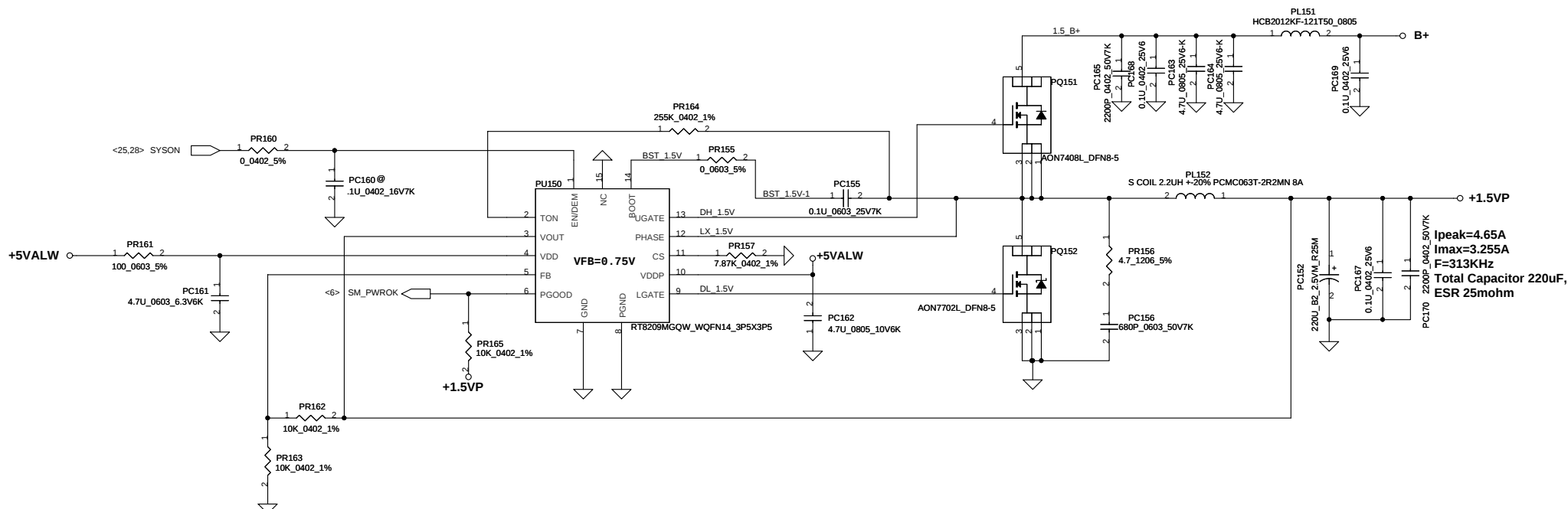
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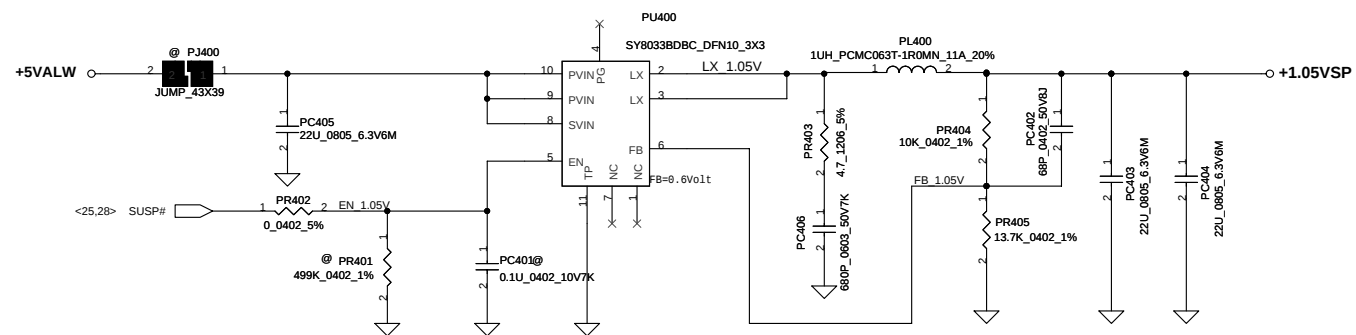
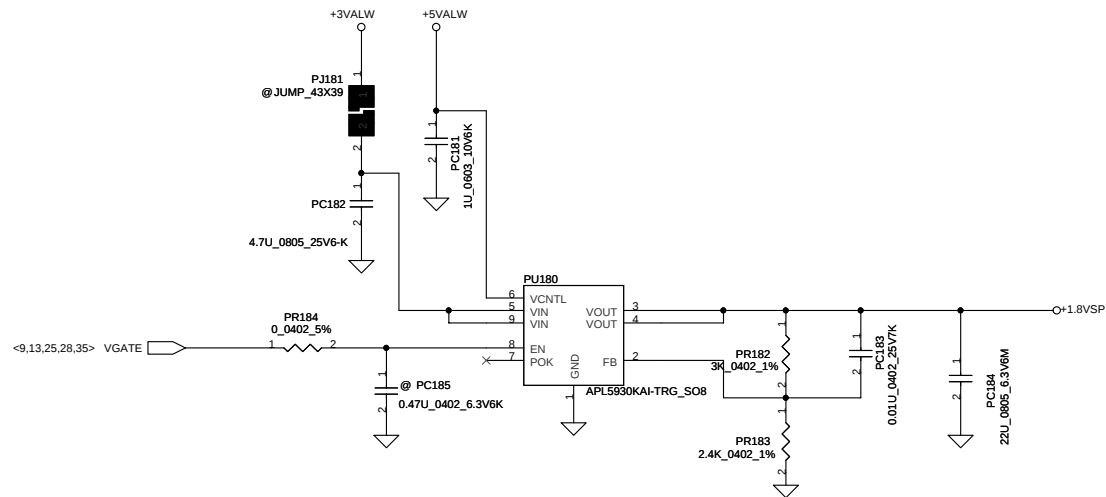
Ipeak=6.11A
Imax=4.277A
F=375KHz
Total Capacitor 150uF,
ESR 35mohm

Ipeak=5.3A
Imax=3.71A
F=300KHz
Total Capacitor 150uF,
ESR 35mohm

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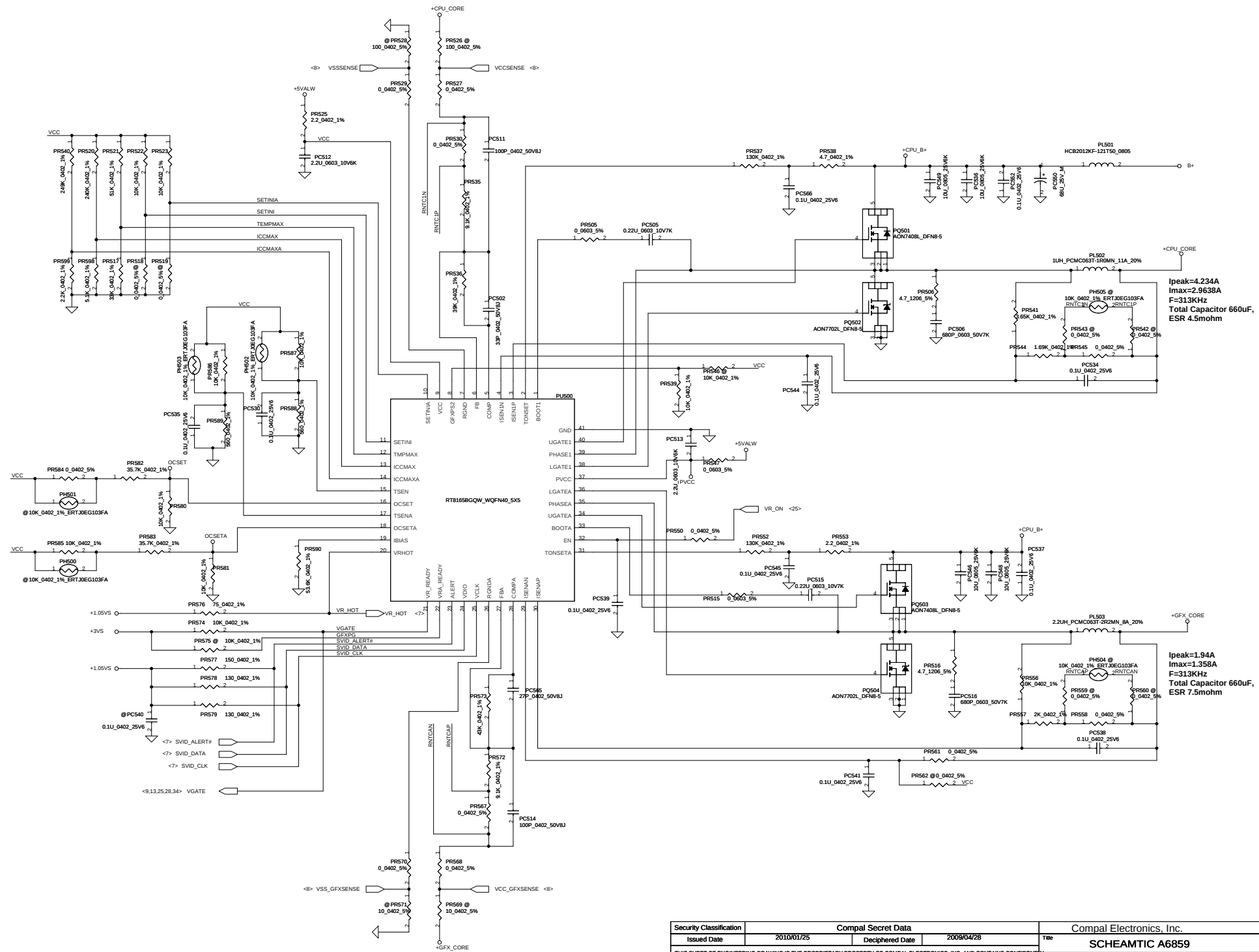
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$I_{peak} = 1.8A$
 $I_{LIM} = 1.26A$
 $F = 1MHz$
 Total Capacitor 330uF, 9mohm

Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,
 SY8035 is for 5A loading , let LX shape can bigger!!

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PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	04/ 26	06	Delete C948,C949,C950,C951	ES2 CPU only support 2 pairs DMI
02.	04/ 26	06	Add DDR_A_MA15 signal in CPU side	Cedar Trail platform supports MA0-MA15 total sixteen address signals
03.	04/ 26	07	Reserve 0 ohm for DDC_SCL / SDA , HPD, BREF1P5V, BREFREXT connect to GND.	Follow Intel V1.0 check list to disable HDMI
04.	04/ 26	07	Add CRT DAC,SYNC signals and add RV155,RV156,RV157 150 ohm pull down resistor for CRT DAC signal.	Follow Intel V1.0 check list to enable RGB I/F
05.	04/ 26	08	Reserve 0 ohm for VCCADP / VCCADP_SFR connect to GND	Follow Intel V1.0 check list to disable HDMI
06.	04/ 26	08	Add R1004,C166 for +VCCDIO / R535,C1125 for +VCC_CRT_DAC	Follow Intel V1.0 check list to enable RGB I/F
07.	04/ 26	10	Add MA15 signal for SODIMM connector	Cedar Trail platform supports MA0-MA15 total sixteen address signals
08.	04/ 26	11	Stuff R544	System will change to non-share ROM design, PCH STRAP2/1 will be 01
09.	04/ 26	12	Change PCIe port arrangement	Follow BIOS team's request to re-arrang PCIe port for power saving.
10.	04/ 26	13	Use BOM option for R931,R932,R933,R934	Follow Intel V1.0 check list to disable HDMI
11.	04/ 26	13	Add J2 and C1087 for PCH GPIO12	BIOS will use GPIO12 for clean password function.
12.	04/ 26	13	Add R566,R567,R618 10K pull high resistors for PCH SPI I/F	System will change to non-share ROM design
13.	04/ 26	15	Add CRT circuit	Follow Intel PDG and V1.0 check list to implement CRT circuit
14.	04/ 26	19	Change USB charger(US1) solution to MAX14566B	Follow A51 common design
15.	04/ 26	19	Reserve US2 bus switch	Support BIOS team's new debug card.
16.	04/ 26	19	Change US4 USB power switch to 2A	Support USB charge V1.1 SPEC--->support 1.8A
17.	04/ 26	23	Change LOM_WAKE# control signal to EC_SWI#	LOM WAKE# will connect to PCH directly and change net name to "EC_SWI#"
18.	04/ 26	25	Change KBC to KB930/KB9012	Follow EC team KB930/KB9012 common design
19.	04/ 26	26	Add U22 -->2MB SPI ROM	System will change to non-share ROM design
20.	04/ 28	18	Reserve 0 ohm and test points in JGPS pin1/3/5/44/46/51	Cougar 2.0 will support new 3G/LTE module
21.	04/ 29	25	Delete C211,C212,C216,C217	RF team has no necessity
22.	04/ 29	07	Delete 220p caps for sideband signals.	EMC team has no necessity
23.	04/ 29	09	Delete C940,C941	RF team has no necessity
24.	04/ 29	09	Delete C1067,C1066	RF team has no necessity
25.	04/ 29	09	Reserve R305,C392 for SMBus_CLK	Reserve R-C for RF team's requirement
26.	04/ 29	17	Delete C227,C228,C290,C230,C231,C232,C1074,C1075	RF team has no necessity
27.	04/ 29	18	Delete C307,C298,C297	RF team has no necessity
28.	05/ 03	07	Add R984 0 ohm resistor for XDP pin17	Reserve 0 ohm for XDP when XDP connector no use.
29.	05/ 04	16	Change Q42,Q43 to dual package	Save layout space and cost
30.	05/ 06	07	Add R989 (0 ohm) for XDP signal	Reserve 0 ohm for XDP when XDP connector no use.
31.	05/ 10	15	Delete D53,F1,C1110	Share 5V with CRT circuit.
32.	05/ 10	07	Change XDP un-define net name	Follow naming rule

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01.	06/ 07	07	Remove XDP connector	XDP debug port is no necessary in PVT
02.	06/ 07	08	Keep +VCCADP_1.05, +VCCADP_SFR power rail even disable DDI interface	Intel correct their DDI disable guideline
03.	06/ 07	26	Change U36 Symbol and footprint	Fix DFB issue
04.	06/ 10	13	Change J1 to JCMOS, J2 to JPW	Follow A51 jumper naming rule
05.	06/ 10	19	Remove US2 USB bus switch	PVT won't reserve USB debug port
06.	06/ 14	08	Stuff 1u (C1007,C1008,C1009) on GFX_CORE	To solve ESD issue
07.	06/ 14	28	Add 0.1u (C1128) on +0.75VS power rail	To solve ESD issue
08.	06/ 14	10	Add 0.1u (C116) on +0.75VS power rail	To solve ESD issue
09.	06/ 14	10	Add 0.1u (C119) on +1.5V power rail	To solve ESD issue
10.	06/ 14	10	Add 0.1u (C406) on +1.5V power rail	To solve ESD issue
11.	06/ 14	27	Add 1u (C406) on touch pad power rail	To solve ESD issue
12.	06/ 15	13	Change PCH SPI I/F pull high to +3VS	To solve S3/S5 +3VS power plan leakage issue
13.	06/ 16	20	Stuff 0.1u (C280) on +3VS power rail	To solve ESD issue
14.	06/ 18	07	Add R1009, R1010 for DDI1_DDC_SCL/SDA	Follow Intel DDI disable guideline

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PIR (Product Improve Record)

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3

NO DATE PAGE MODIFICATION LIST				PURPOSE
01. 06/ 29 09 Swap CLK Gen output for CPU_SCDREFFCLK and CPU_DREFCLK				Intel recommend CPU_SSCDREFFCLK use SSC CLK

QBU00 LA-6858P SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0

NO DATE PAGE MODIFICATION LIST				PURPOSE
01. 08/ 29 07 Change R975 from 10ohm to 0 ohm				Follow Intel CRB design.
02. 08/ 29 25 Un-stuff R312,R313				KS01,KS02 of KB930 don't need to pull high.
03. 08/ 29 27 Add 1u(C406) on touch pad power rail.				To solve ESD issue

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2011/06/14		32	PR336, PR356 to 1206 4.7ohm; PC336, PC356 to 0603 680pF	For EMI Solution
2011/06/14		35	PR526, PR528, PR569, PR571 to @ PR506, PR516 to 1206 4.7ohm; PC506, PC516 to 0603 680pF	For EMI Solution
2011/06/14		33	PU150 change to RT8209MGQW	
2011/06/14		33	PR157 change to S RES 1/16W 7.87K +-1% 0402	For OCP Solution
2011/06/14		35	PC550 to @	Reserve PC550 location and change it to 5.3mm cap (SF000003Z00) for ME solution
2011/06/21		35	PC536 to 42.2K	Change PR536 to 42.2Kohm to meet Cedar Trail loadline spec
2011/06/27		35	PH505, PR542, PR543, PH504, PR559, PR560 to @ PR545, PR558, PR530, PR567 to 0ohm PR541 to 3.62K, PR544 to 1.69K, PR556 to 10K PR557 to 2K, PR536 to 39K	For Cedar Trail loadline spec
2011/06/27		35	PR582, PR583 to 35.7K	For CPU & GFX OCP Solution
2011/06/27		35	PL503 to 2.2uH	Base on GFX_Core ripple & dynamic test result
2011/06/27		35	PR584 to 0_0402_5%	For AP Code material
2011/11/1		29	PF1 change to SART 5A_32V_S1206-H-5.0A	For burn out issue
2011/11/1		30	PF2 change to Cooper 7A_32V_TR/3216FF-R	For burn out issue
2011/11/1		32	PU330 change to RT8205EGQW	For burn out issue
2011/11/1		35	PC550 change to Lelon 68uF 5.3H	For acoustic issue

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