

Compal Confidential

Cougar

Schematics Document

Intel Cedar Trail Processor/ Tiger point

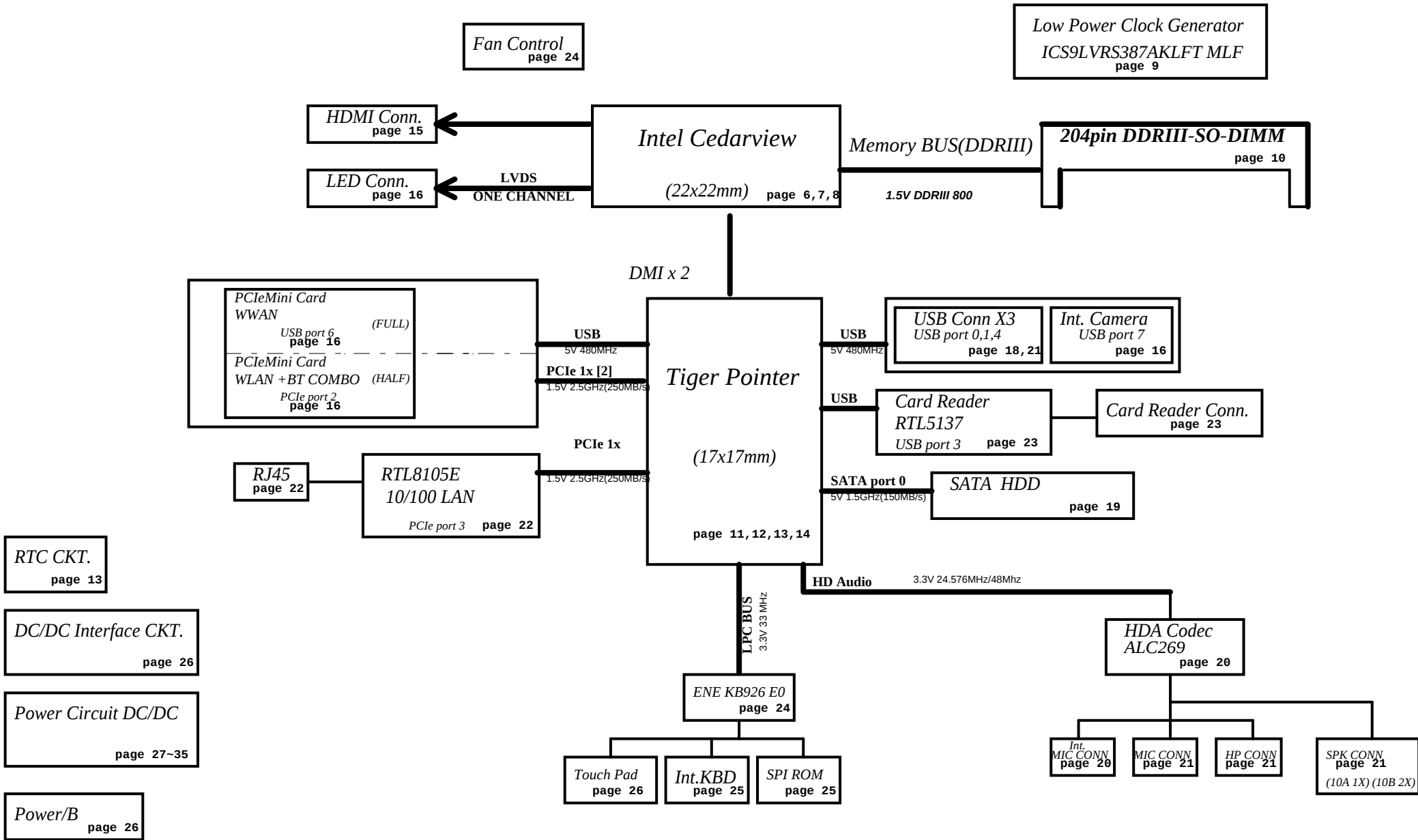
2010-11-05

REV : 0 . 1

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				Rev	A

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Model Name : PBU00
File Name : P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE T00TH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE T00TH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

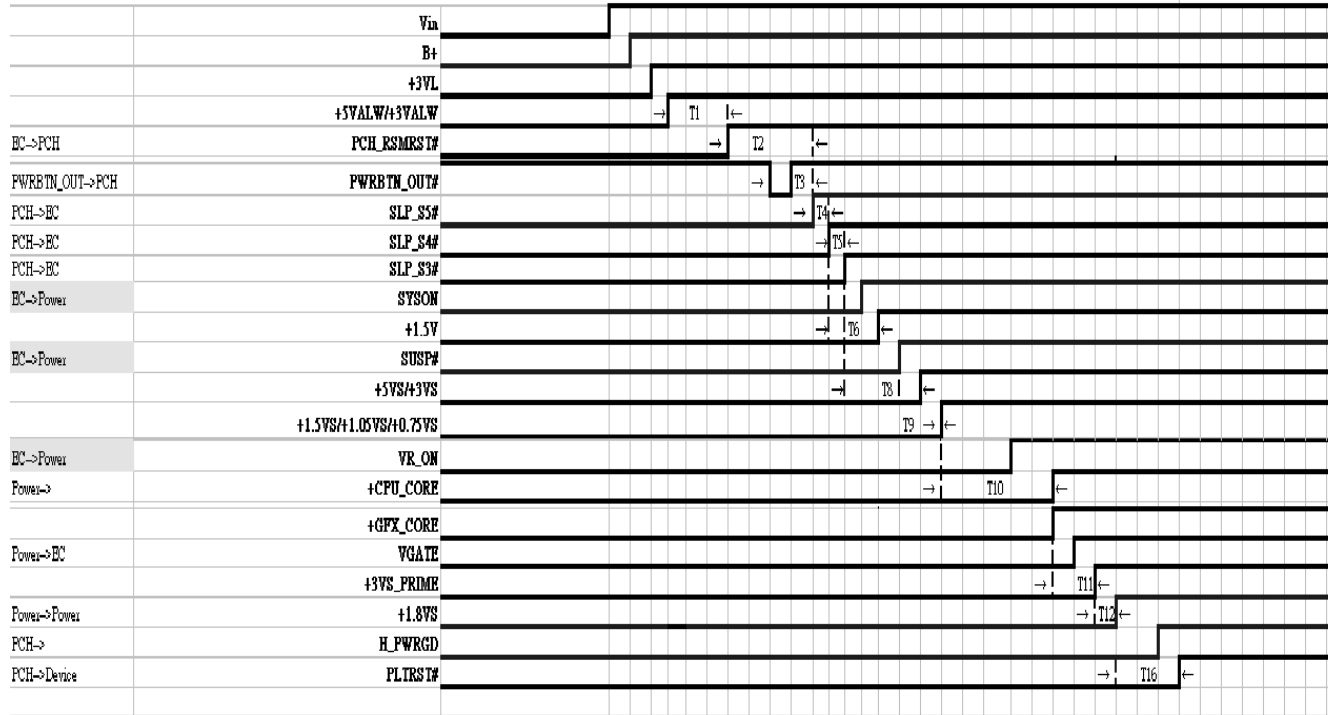
EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

PBU00 Power ON sequence

2010/7/2



Power-on Sequence

Time	Description	Expected
T1	+5VALW to PCH_RSMRST# inactive	>0ms
T2	PCH_RSMRST# inactive to SLP_S5# inactive	<110ms
T3	PWRBTN_OUT# inactive to SLP_S5# inactive	"
T4	SLP_S5# inactive to SLP_S4# inactive	28.992ms ~ 64.088ms
T5	SLP_S4# inactive to SLP_S3# inactive	28.992ms ~ 64.088ms
T6	SLP_S3# inactive to +1.5V active	"
T7	SLP_S3# inactive to +5VS inactive	"
T8	+1.5V active to +1.05V active	"
T9	+1.05V active to +CPU_CORE	"
T10	+CPU_CORE active to +3.3V_PRIME	"
T11	+3.3V_PRIME active to +1.8V	3.3-1.8<700mV
T12	H_PWRGD inactive to PLTRST# inactive	34<RTCCCLK[4]

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Cougar Power Map

B+

DESIGN CURRENT 250mA

Ipeak=6.97A, I_{max}=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

UP6182CQAG

** The SW just is reserved.
The power passes by jump or
0-ohm resistor.

WOL_EN#

** P-CHANNEL
A03413

DESIGN CURRENT 300mA

+3V_LAN

Ipeak=3.98A, I_{max}=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL
SI4800BDY

DESIGN CURRENT 2286mA

+5VS

VGATE

APL5930KA

DESIGN CURRENT 151mA

+1.8VS

SUSP

N-CHANNEL
SI4800BDY

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL
A03413

DESIGN CURRENT 2000mA

+LCD_VDD

VGATE#

N-CHANNEL
SI4800BDY

DESIGN CURRENT 294mA

+3VS_PRIME

SUSP#

SY8033BDBC

Ipeak=1.308A, I_{max}=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR_ON

RT8165BGQW

I_{max}=3.5A

DESIGN CURRENT 4500mA

+CPU_COREP

DESIGN CURRENT 2000mA

+GFX_COREP

SYSON

G5603RU1U

Ipeak=19.6A, I_{max}=13.72A

DESIGN CURRENT 2270mA

+1.5VP +-5%

SUSP#

IRF8113PBF

DESIGN CURRENT 2112mA

+1.5VSP

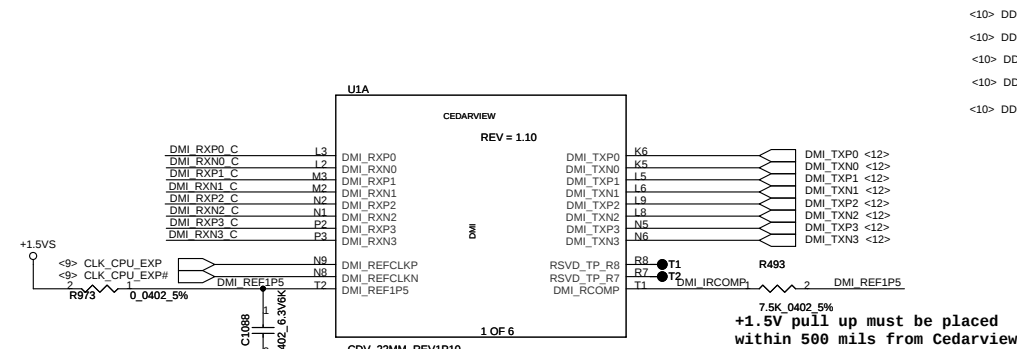
SUSP

UP7711U8

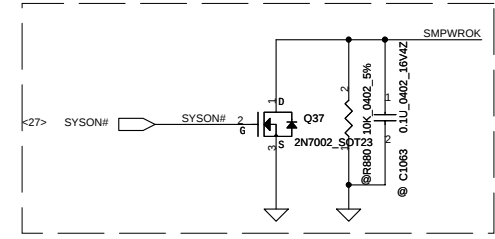
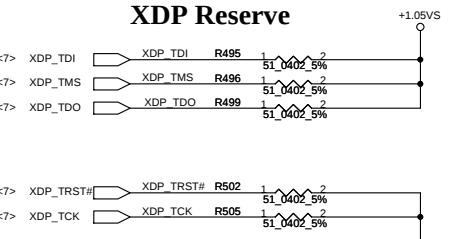
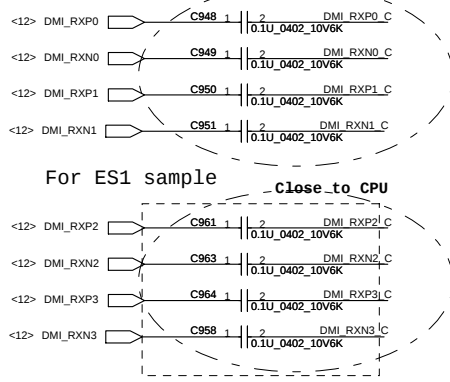
DESIGN CURRENT 500mA

+0.75VSP

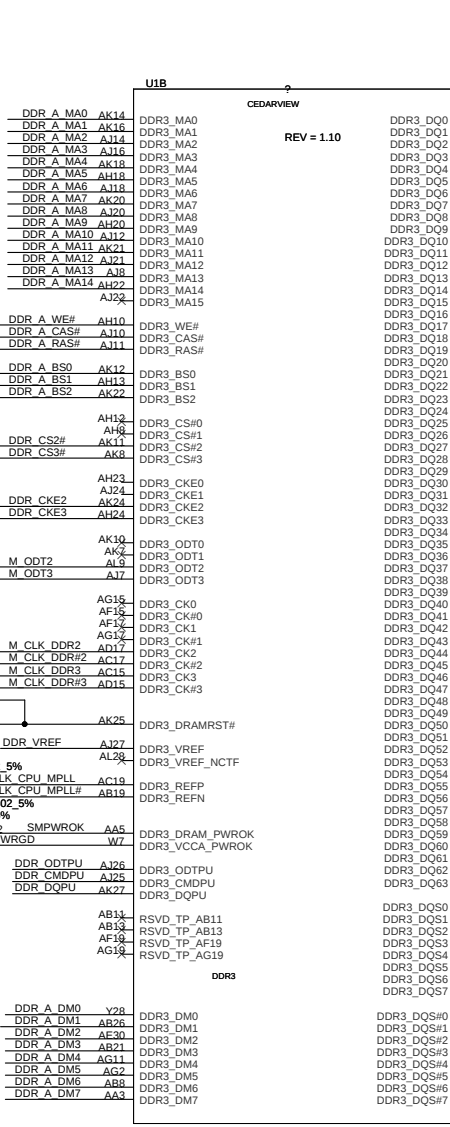
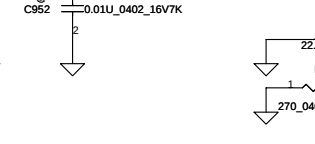
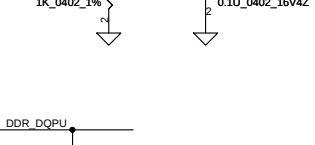
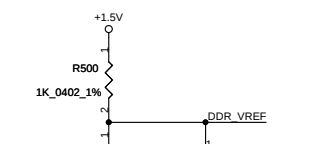
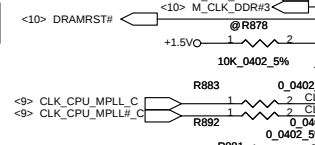
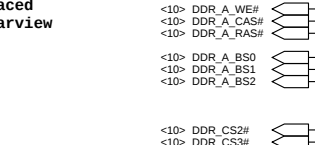
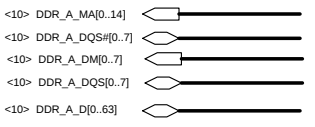
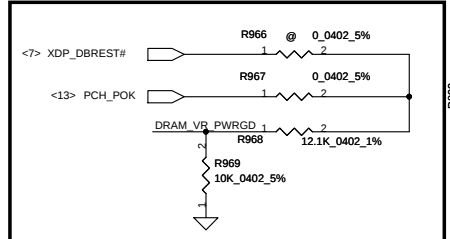
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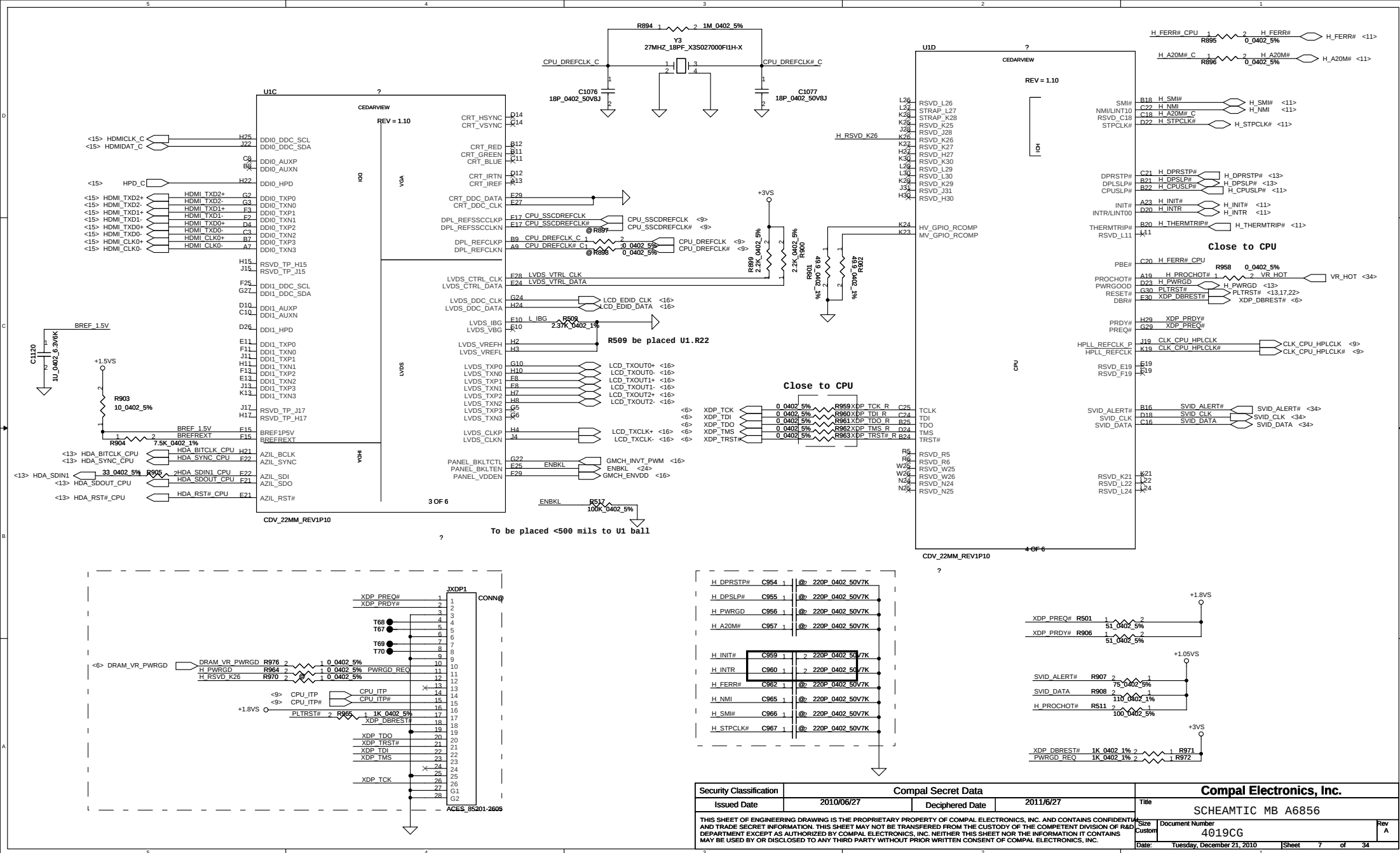
+1.5V pull up must be placed within 500 mils from Cedarview



Reserve PM_SLP_S4# to turn on DRAM_PWROK

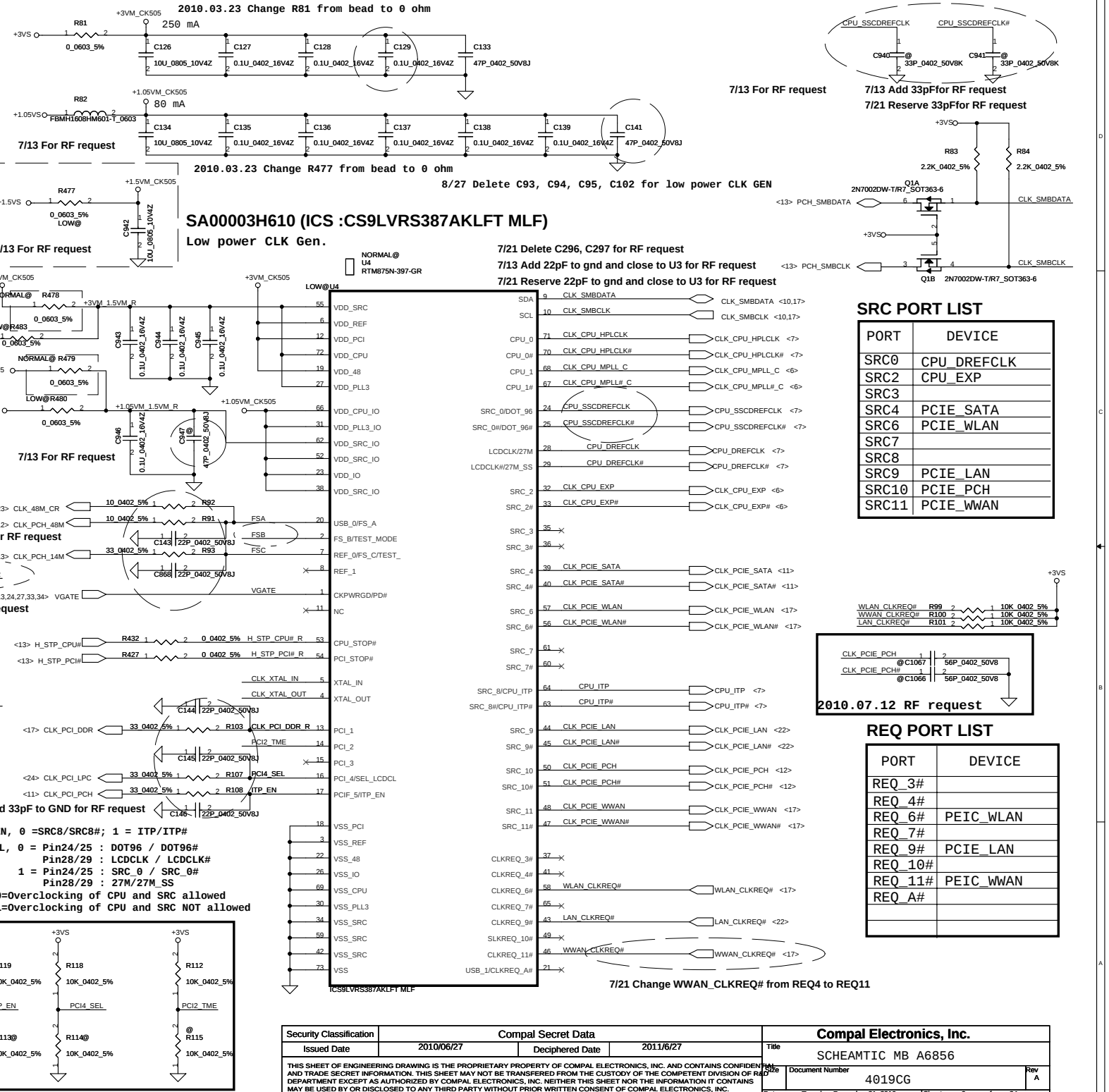
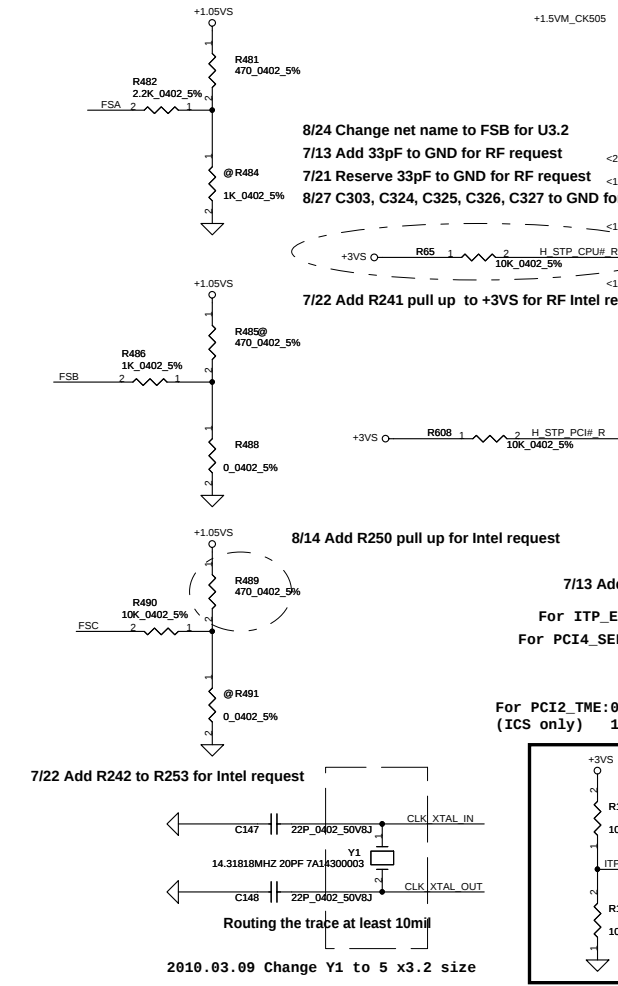


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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHZ	MHZ	MHZ	MHZ	MHZ	MHZ
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff



SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	CPU_EXP
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

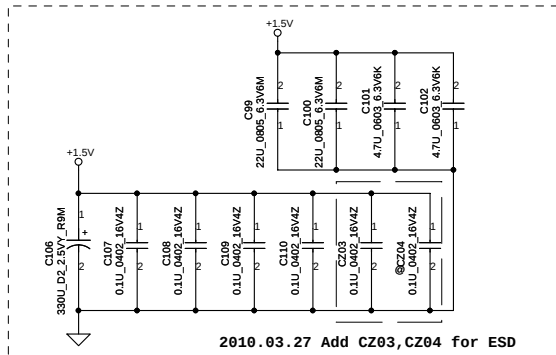
REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

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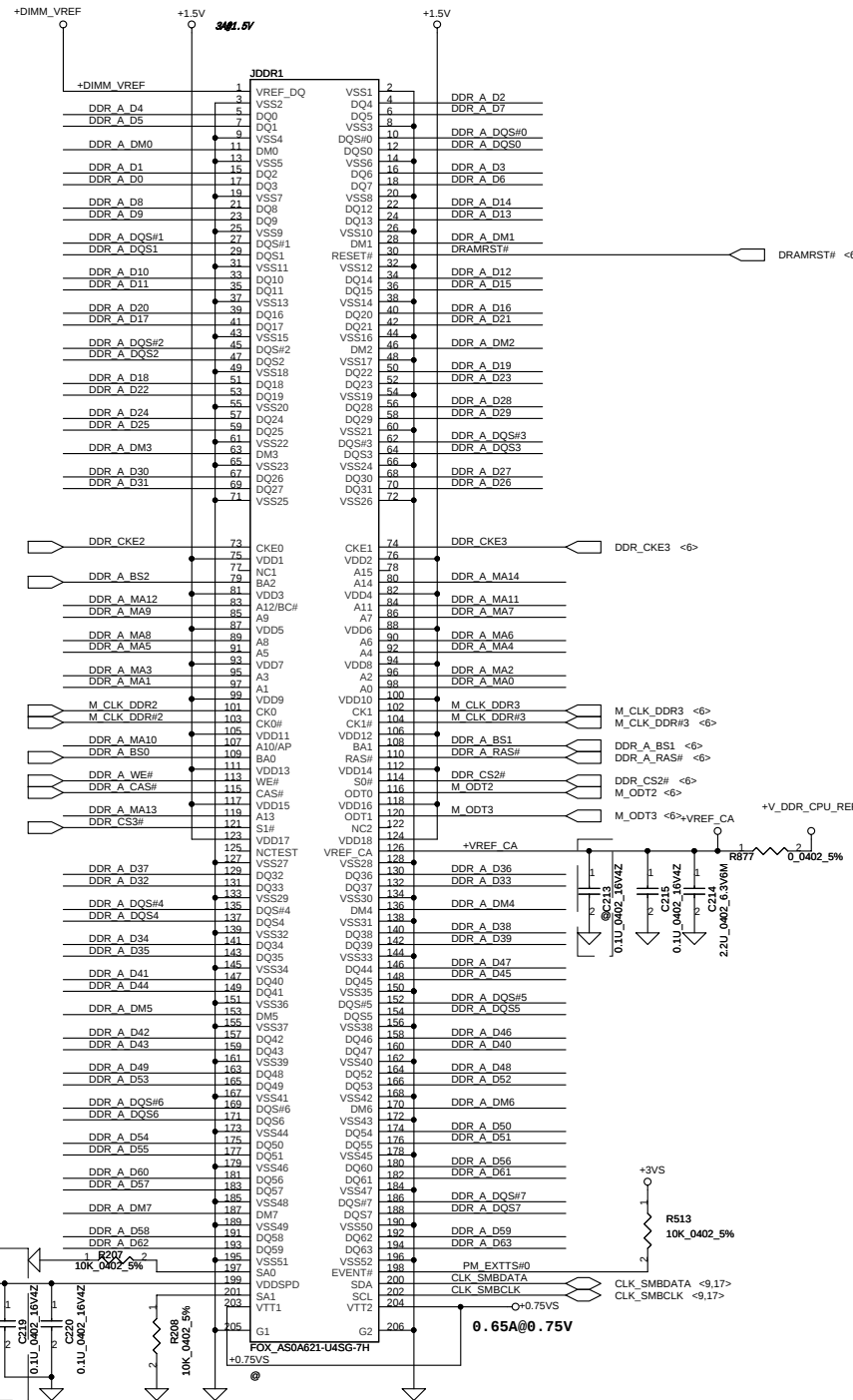
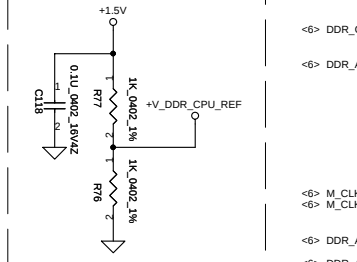
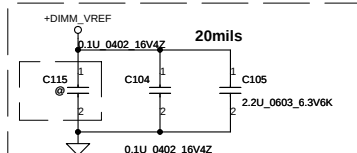
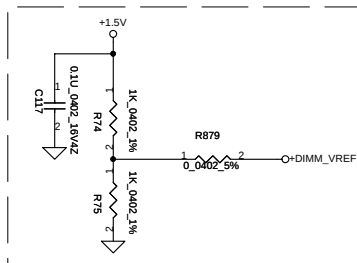
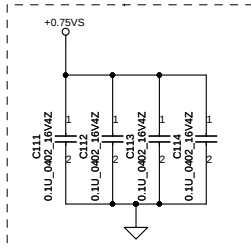
<6> DDR_A_DQS#[0..7]
 <6> DDR_A_D[0..63]
 <6> DDR_A_DM[0..7]
 <6> DDR_A_DQS[0..7]
 <6> DDR_A_MA[0..14]

Layout Note:
Place near JDDR1

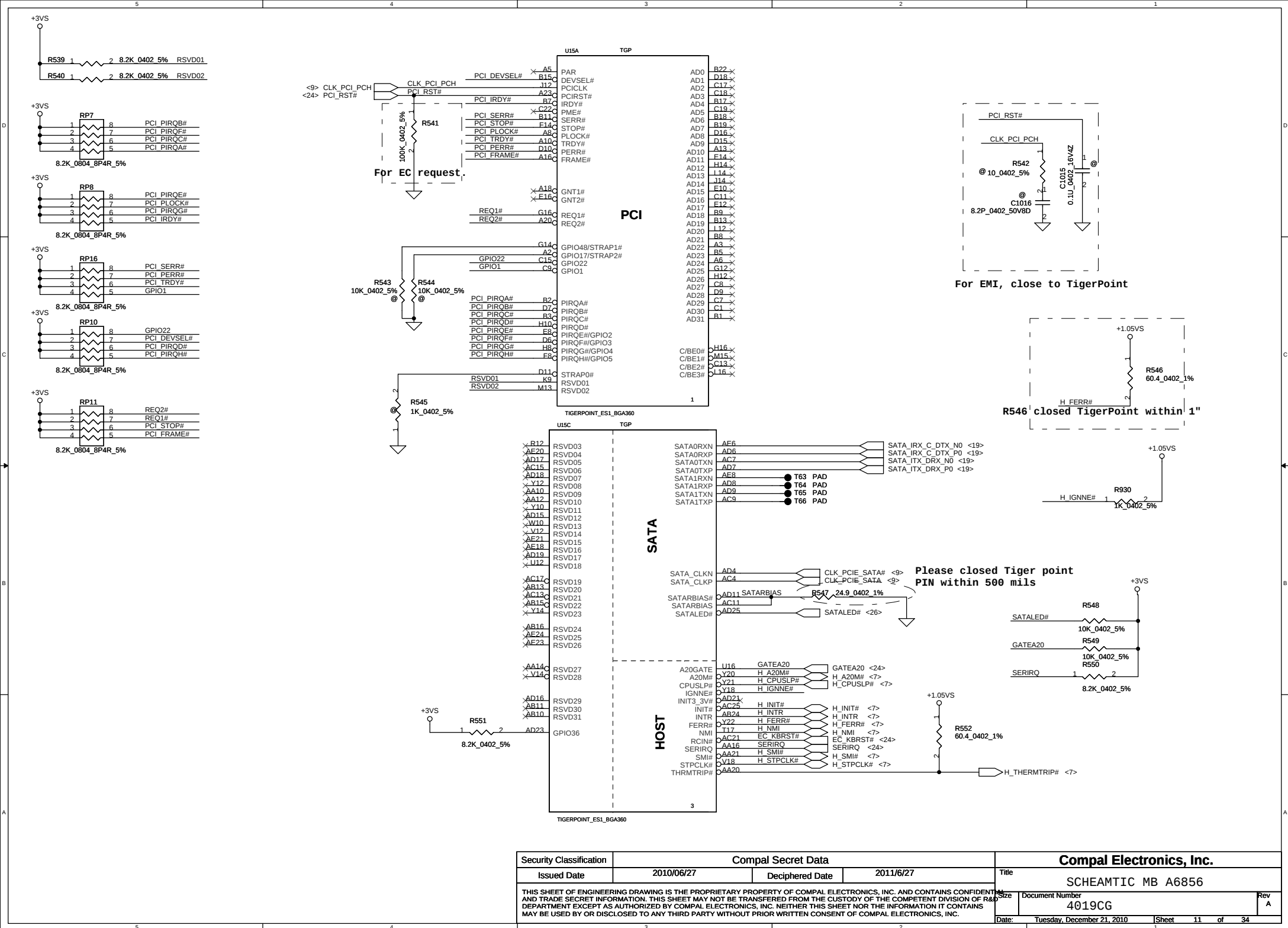


2010.03.27 Add CZ03,CZ04 for ESD

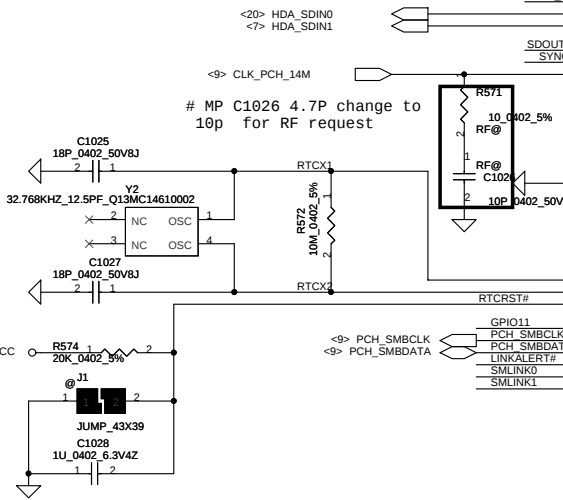
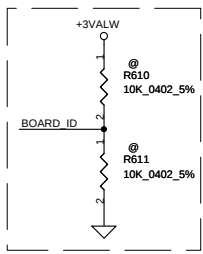
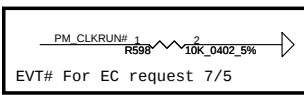
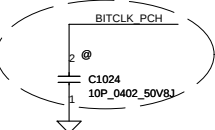
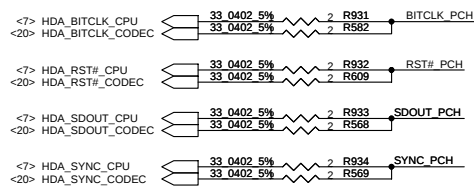
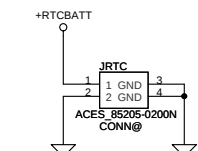
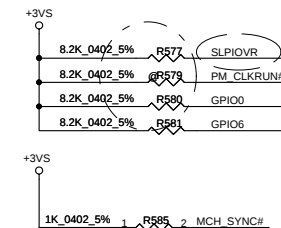
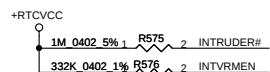
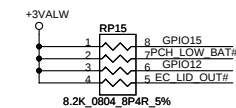
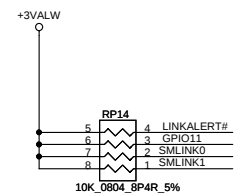
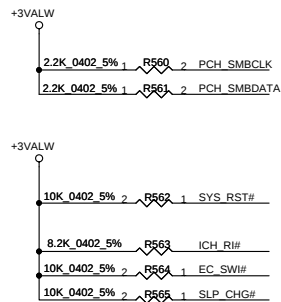
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.75VS



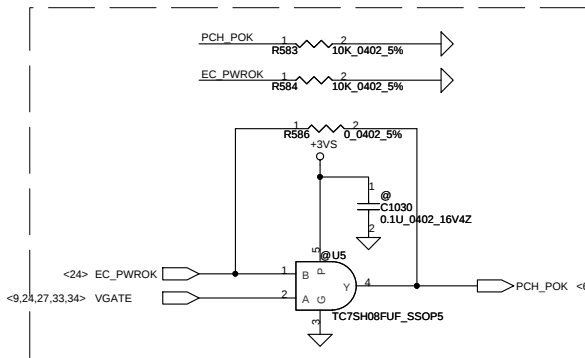
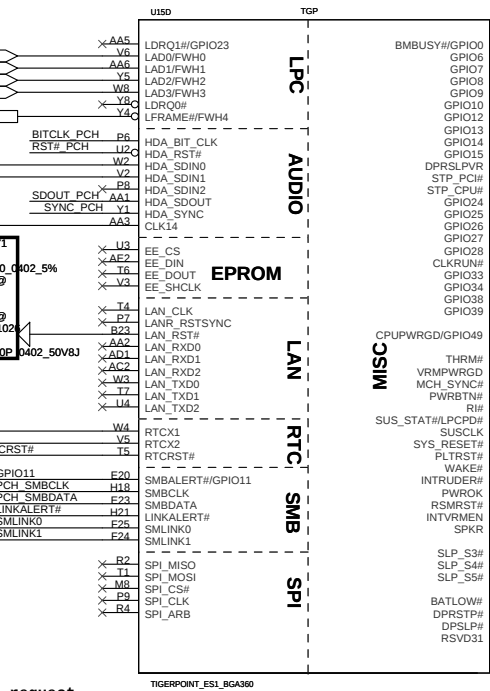
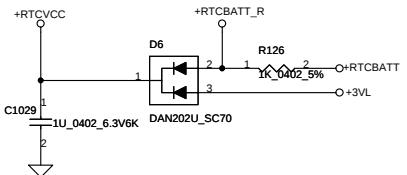
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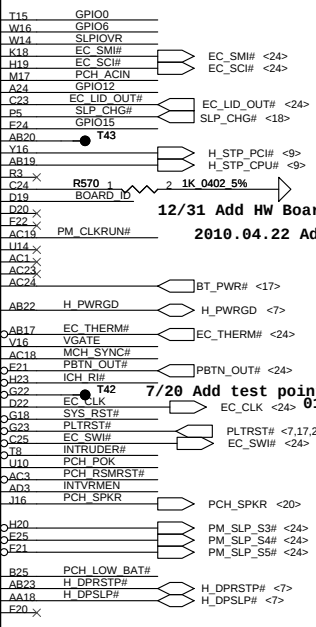
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7/20 Add SLPIOV# pull up 8.2k to +3vs
9/23 Change RP17 to R256, R257, R258 for layout request



2010.03.22 Un-stuff U5 and C1030



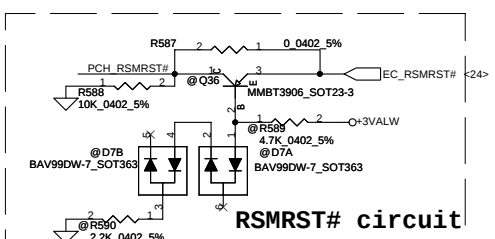
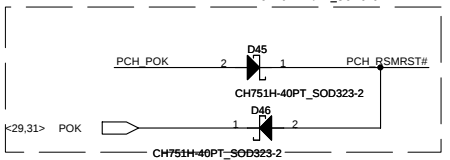
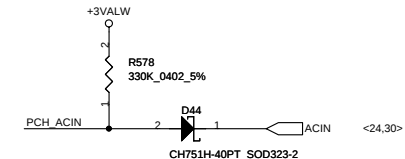
12/31 Add HW Board ID function

2010.04.22 Add C1064 for ESD solution

7/20 Add test point

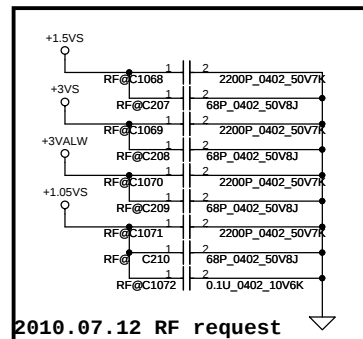
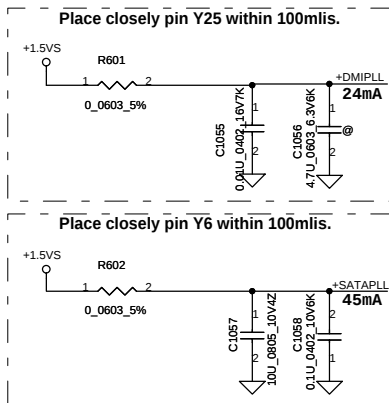
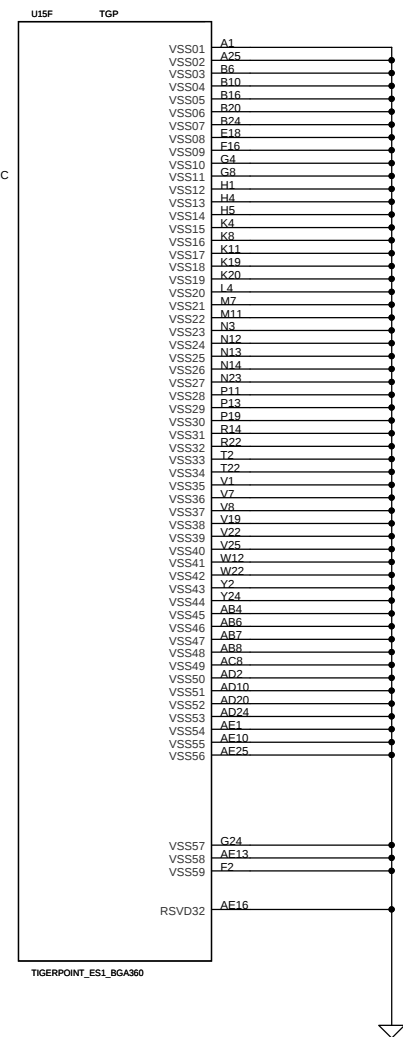
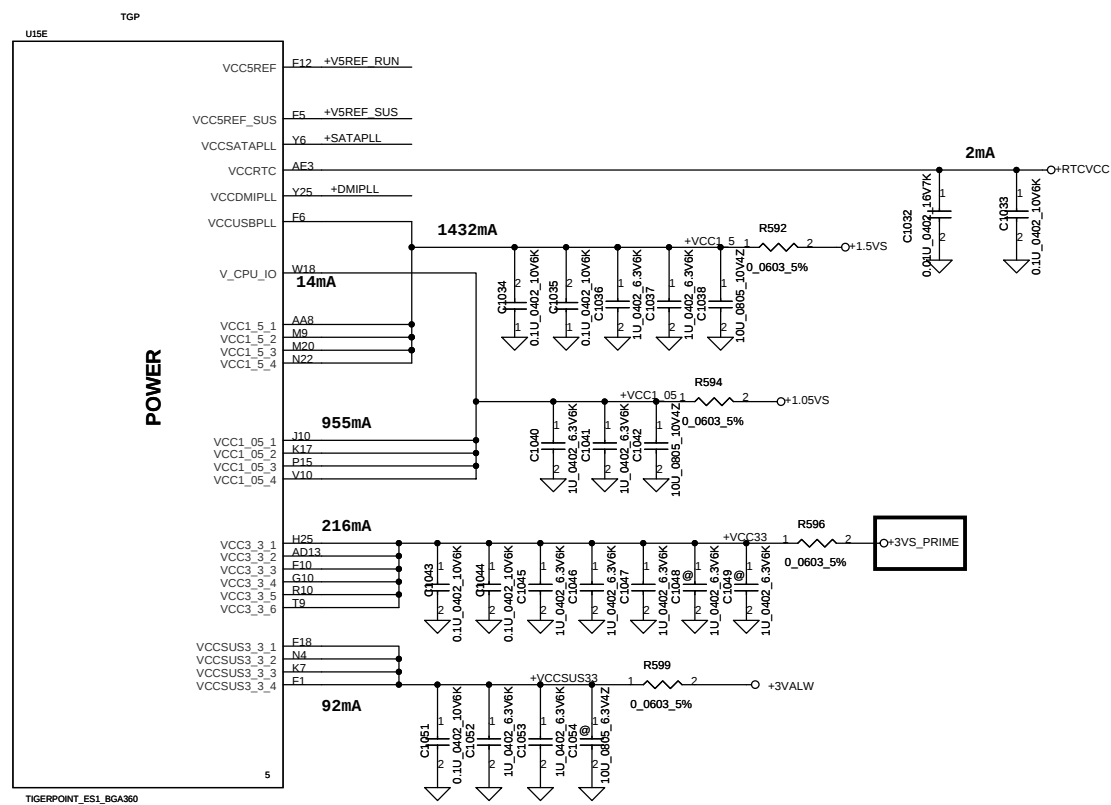
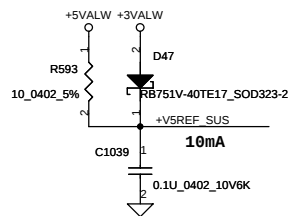
01/11 Reserve EC_CLK for KBC

8/24 Add R254 pull down for EC request



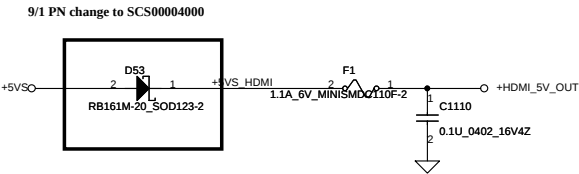
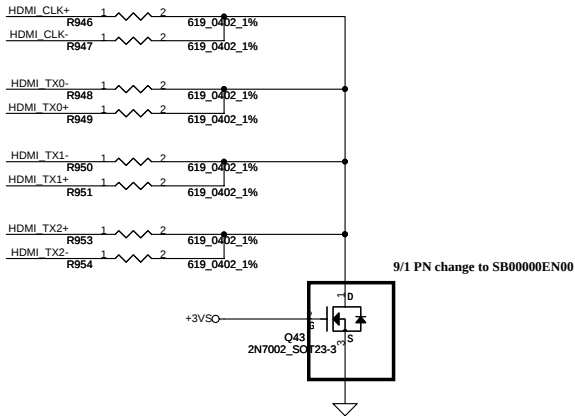
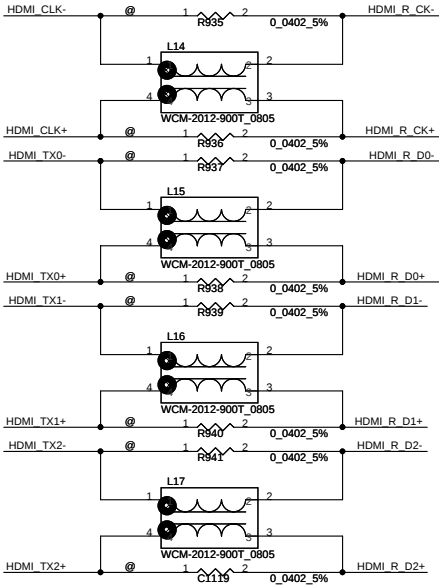
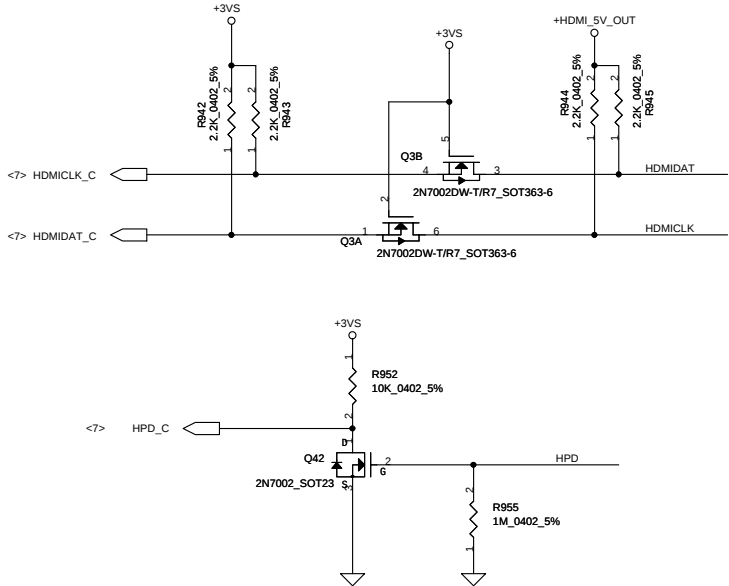
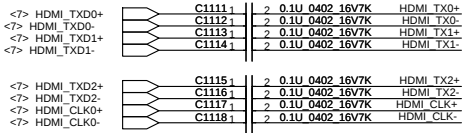
2010.03.22 Un-stuff RSMRST# circuit and use 0 ohm bypass

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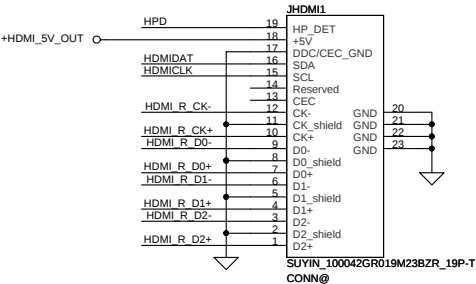


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HDMI CONNECTOR



< HDMI Connector >

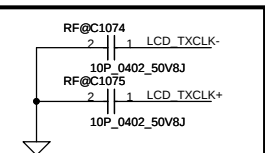
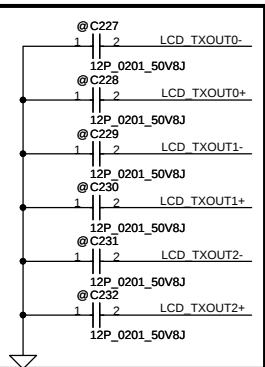


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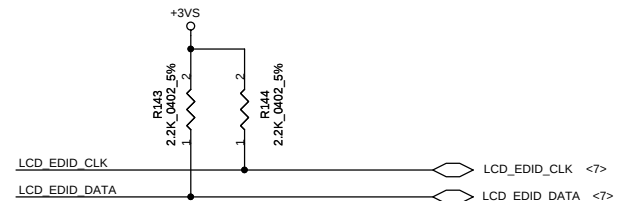
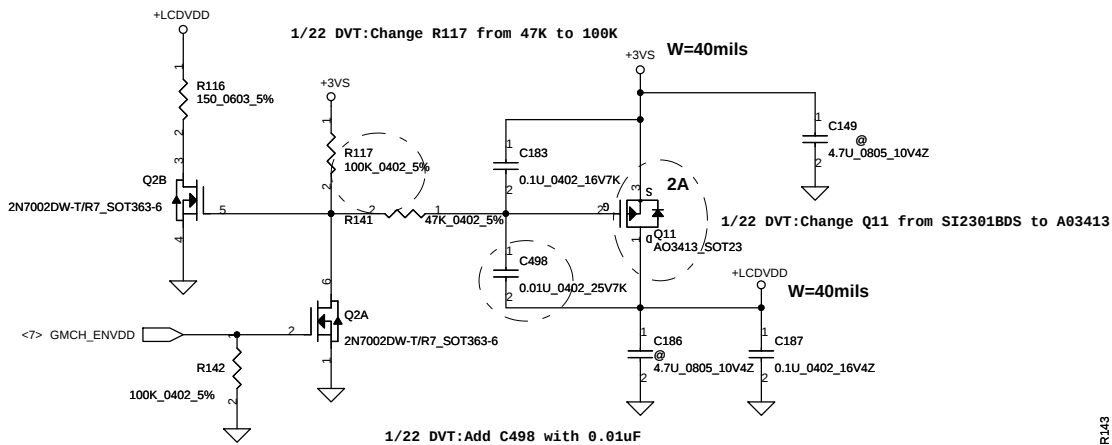
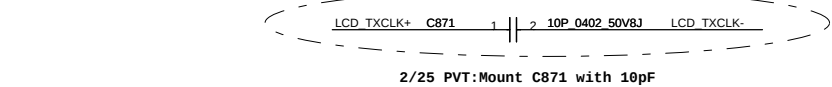
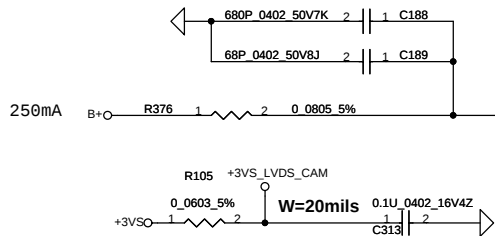
LCD POWER CIRCUIT

LED/PANEL BD. Conn.

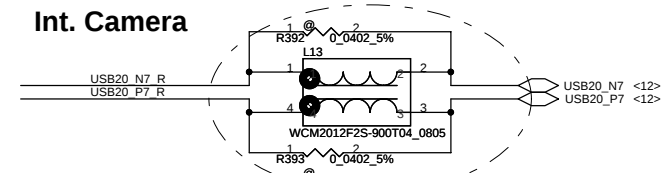
MP Add C227~C232 for RF request



PVT Add C1074, C1075 10p and stuff for RF



Int. Camera

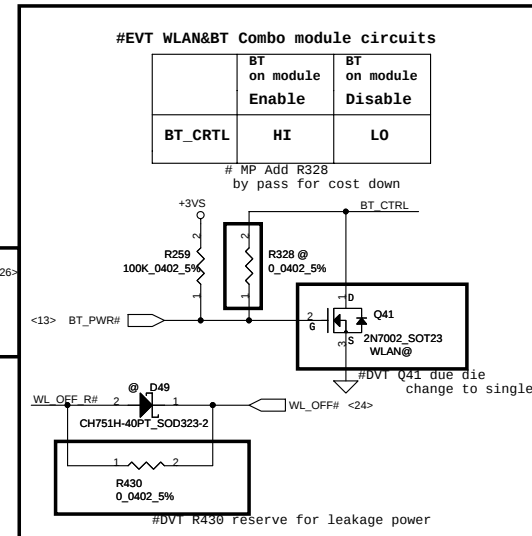
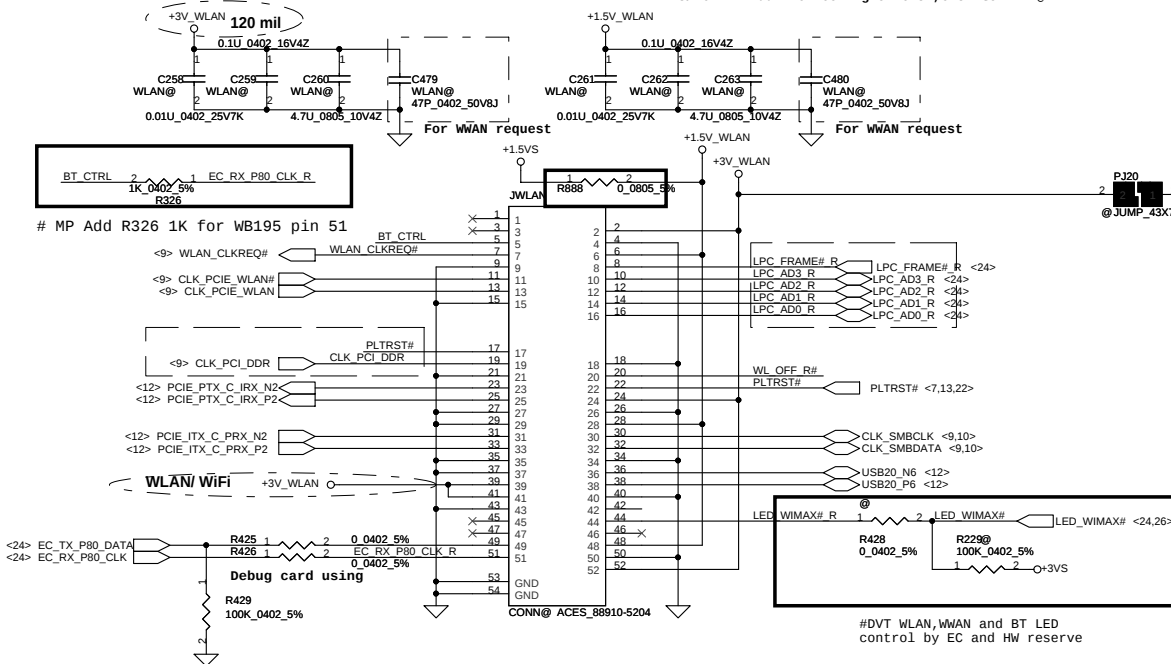


For EMI request

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Mini-Express Card for WLAN/WiMax

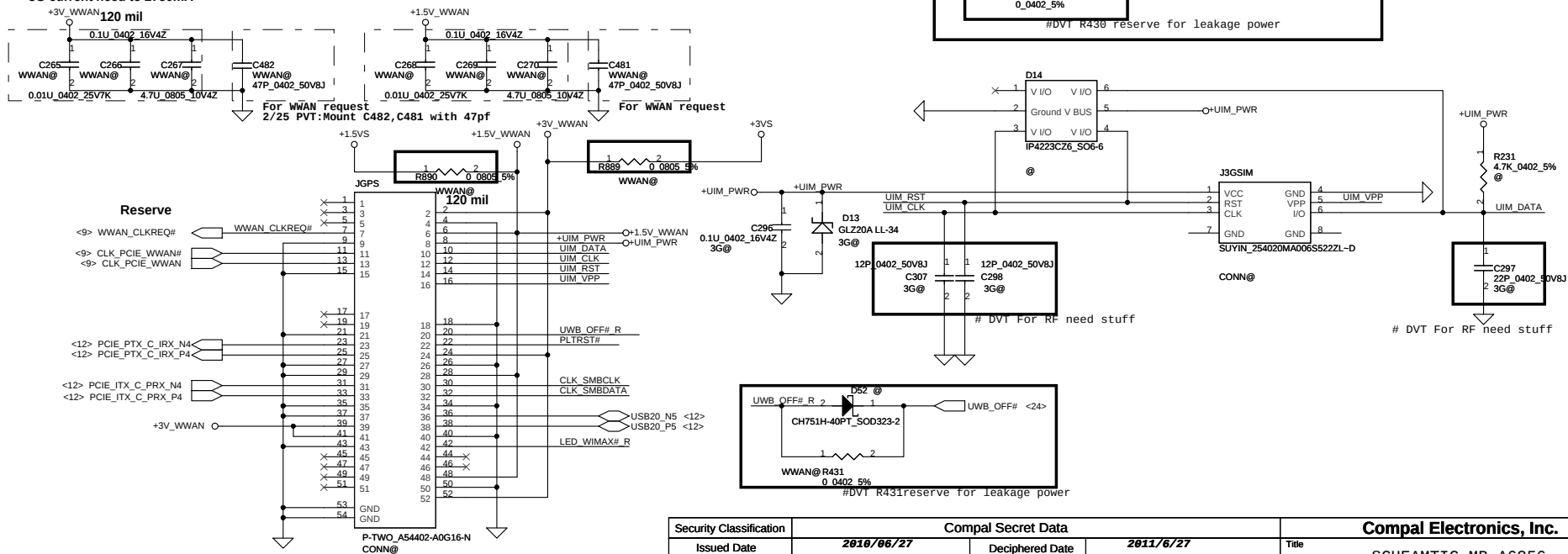
```
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@
```



Mini-Express Card for 3G/GPS

3G current need to 2750mA

3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@

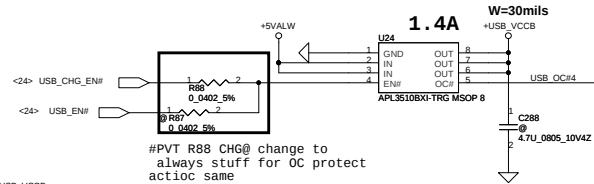
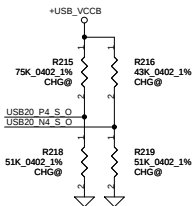
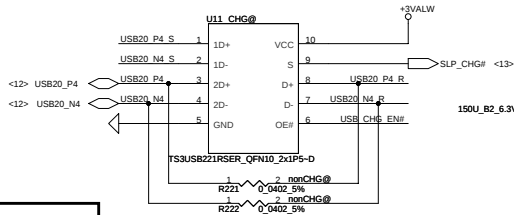
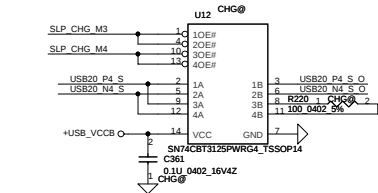
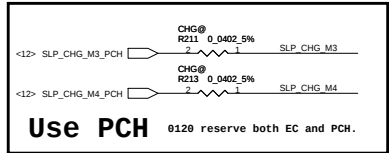


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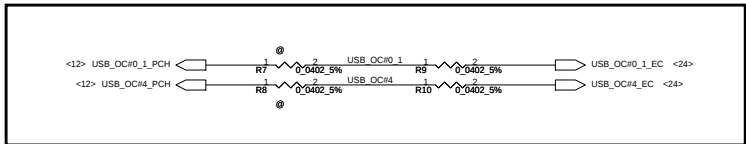
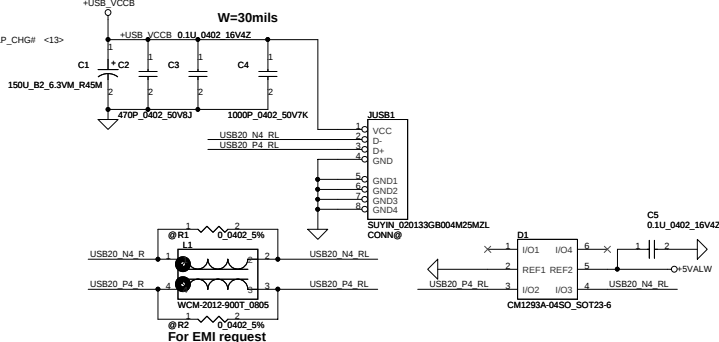
USB CONN- -Left

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



#PVT R88 CHG@ change to always stuff for OC protect actioc same

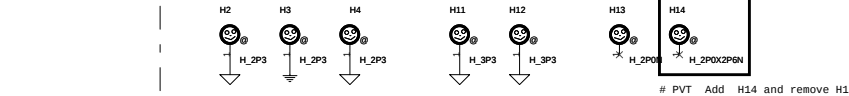
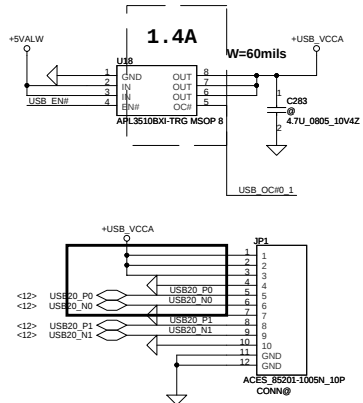


#DVT USB_OC# control by EC

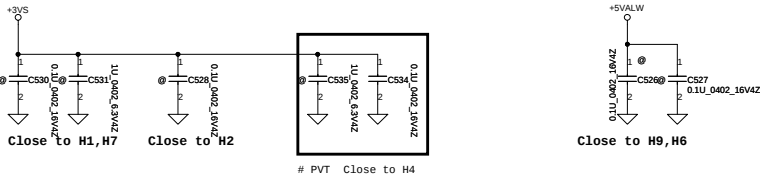
For EMI request
BVT: Change D38, D37 from PRT85V0U2X_SOT143-4 to CM1293A-04S0_SOT23-6

For EMI request

USB CONN

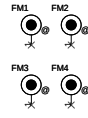


Add 0.1u Caps for each screw hole for ESD rule



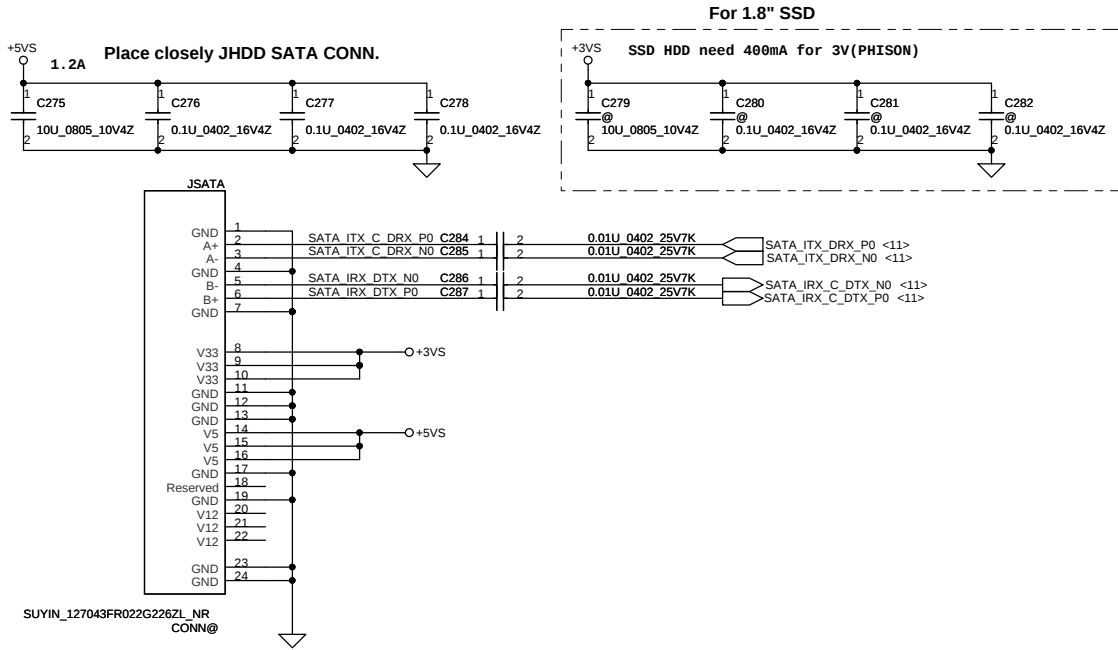
2010.07.20 Add for ESD solution

FIDUCIAL_C40M80



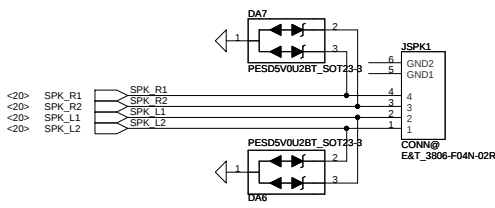
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SATA Conn.

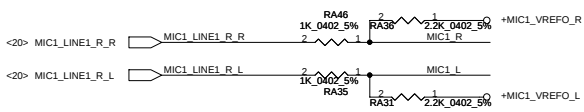


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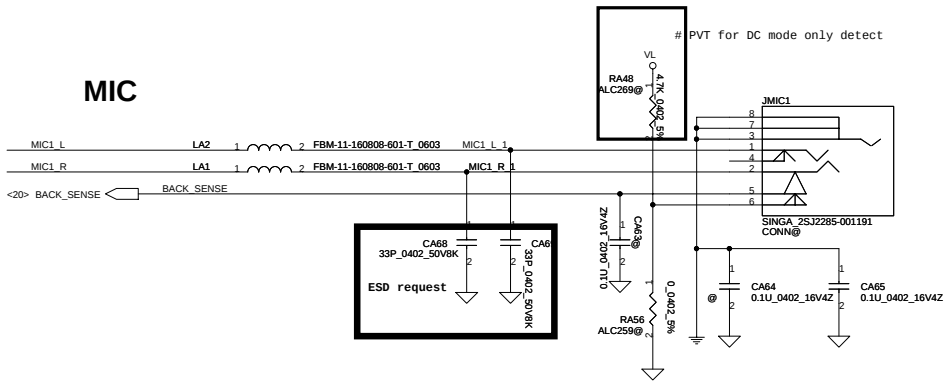
SPEAKER



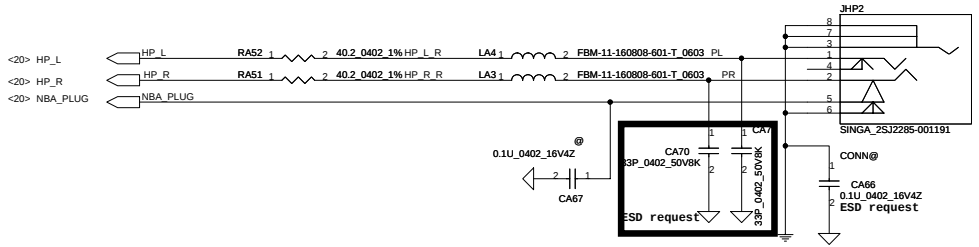
Ext.MIC/LINE IN JACK



MIC

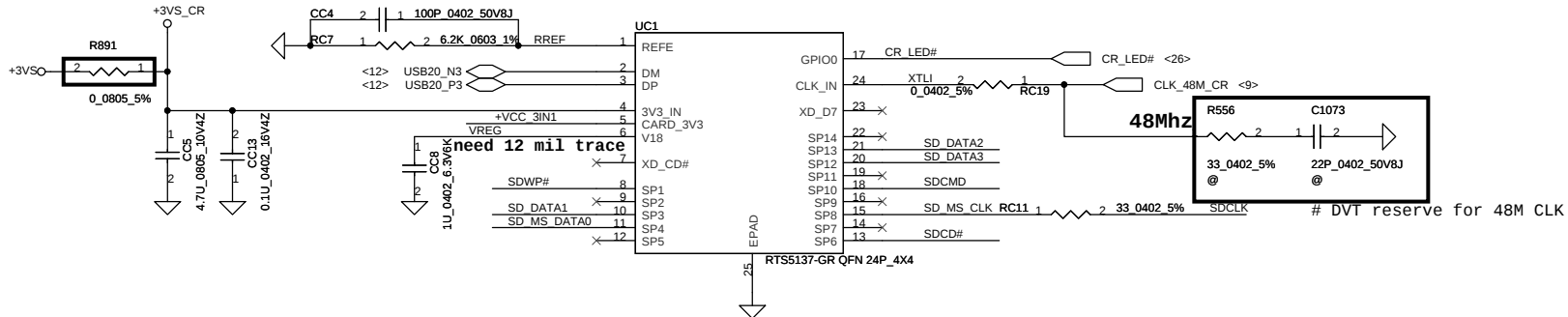


Head phone

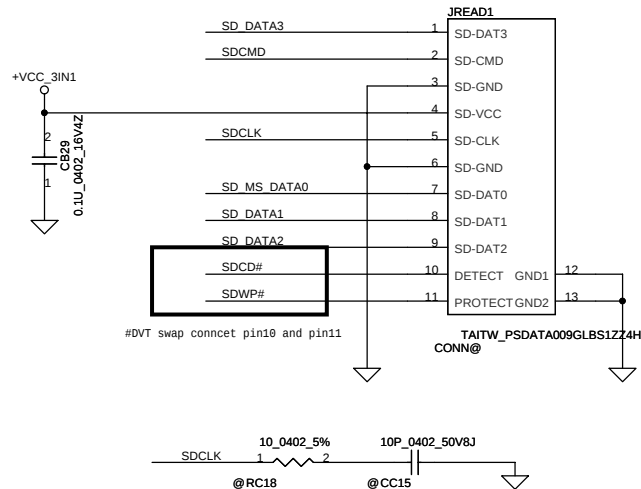


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	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CEF	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		

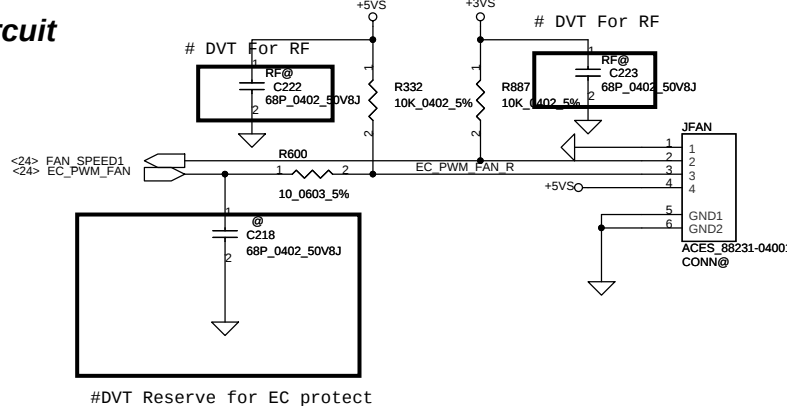


2 in 1 Card Reader

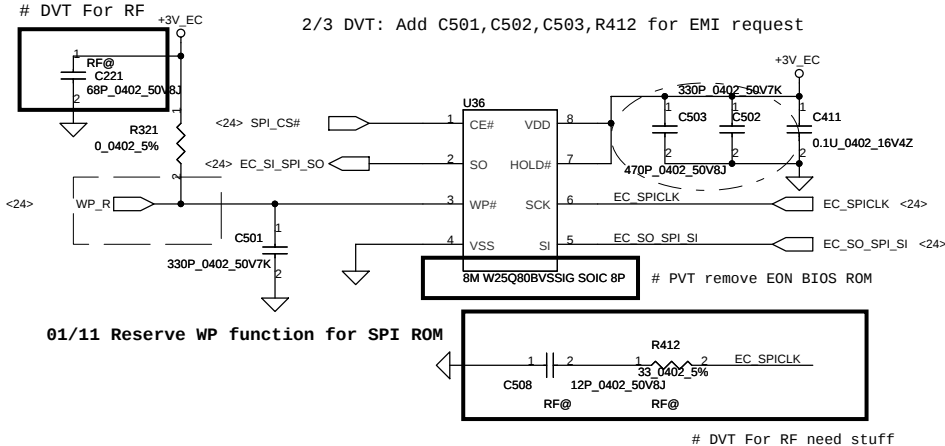


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FAN Control Circuit

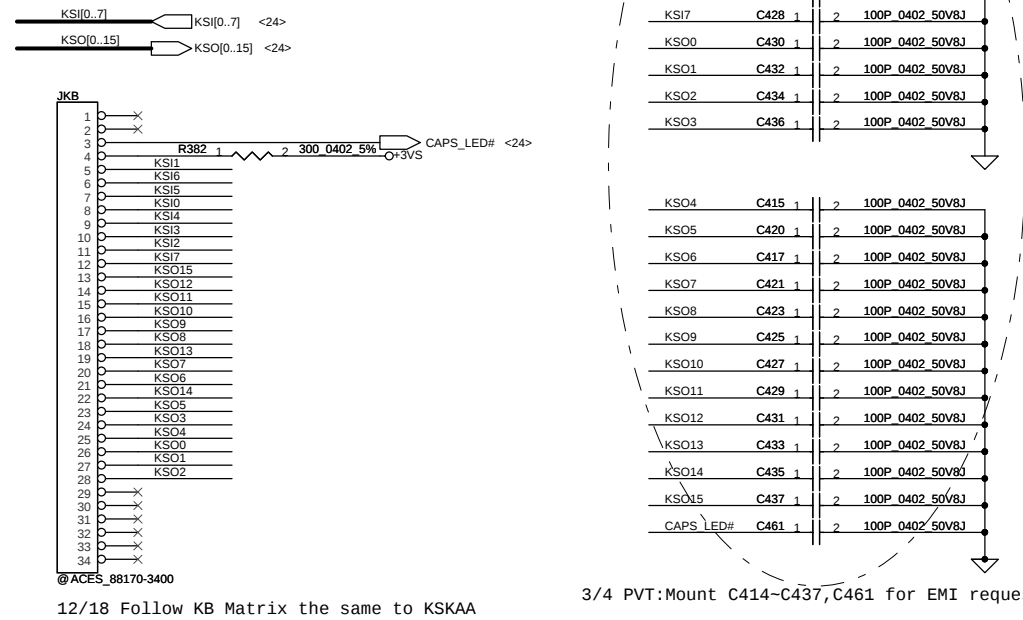


SPI Flash (8Mb*1)



LPC Debug Port

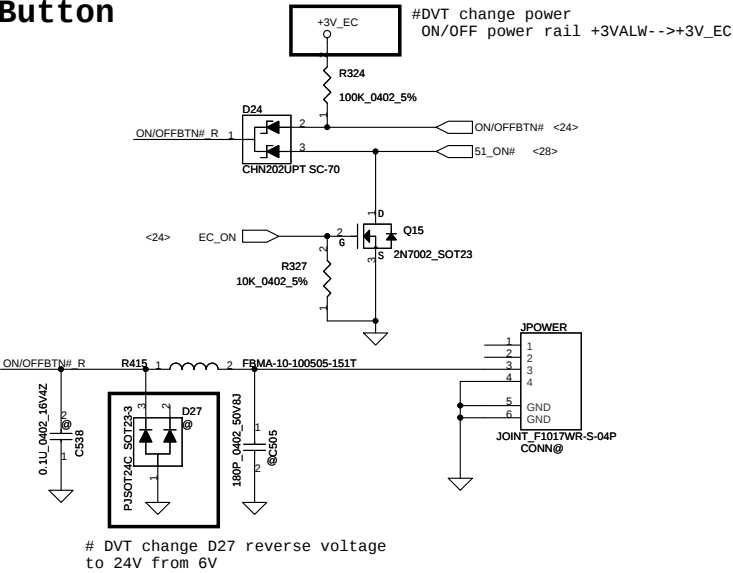
KEYBOARD CONN.



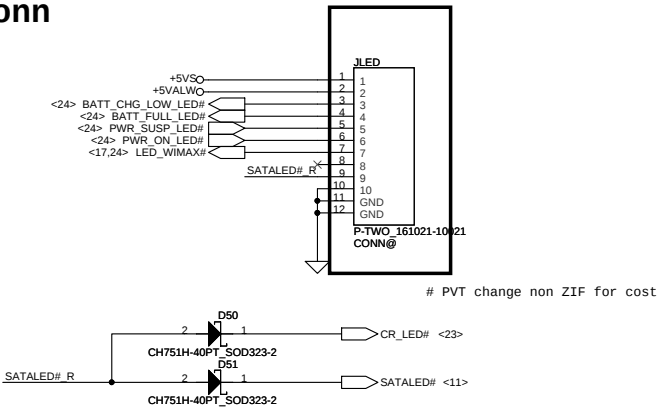
3/4 PVT:Mount C414-C437,C461 for EMI request

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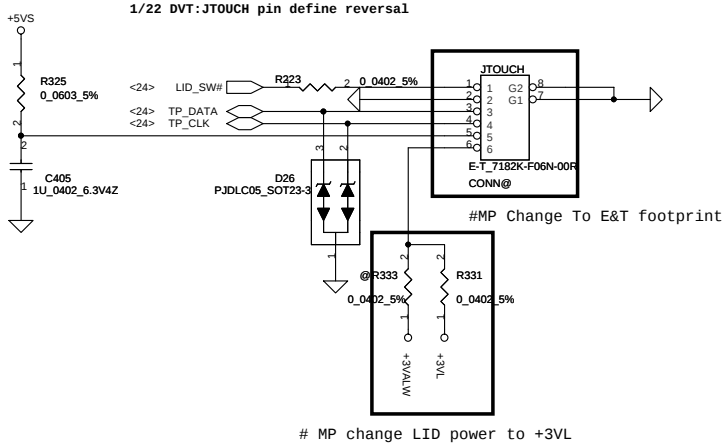
Power Button



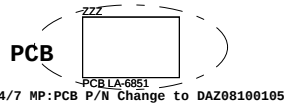
LED Conn



Touch/B Connector



ISPD

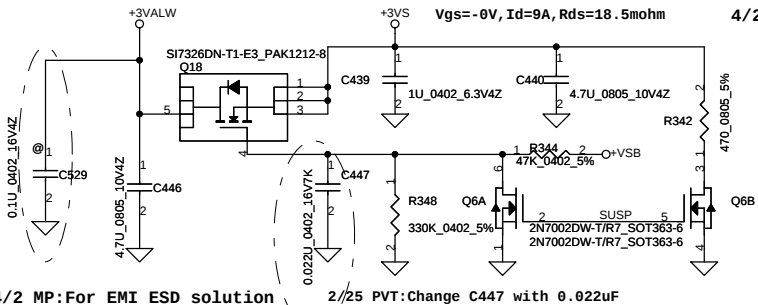


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+3VALW TO +3VS

Vgs=-0V, Id=9A, Rds=18.5mohm

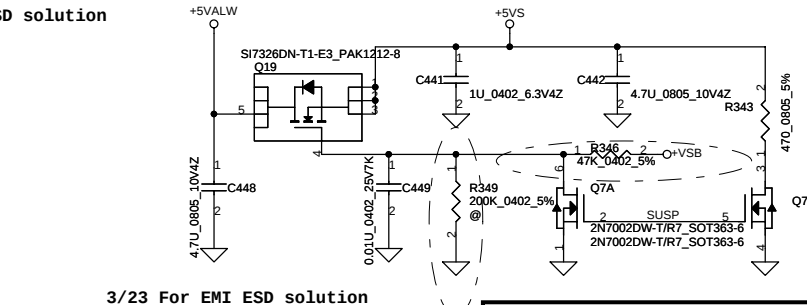
4/2 MP:For EMI ESD solution



+5VALW TO +5VS

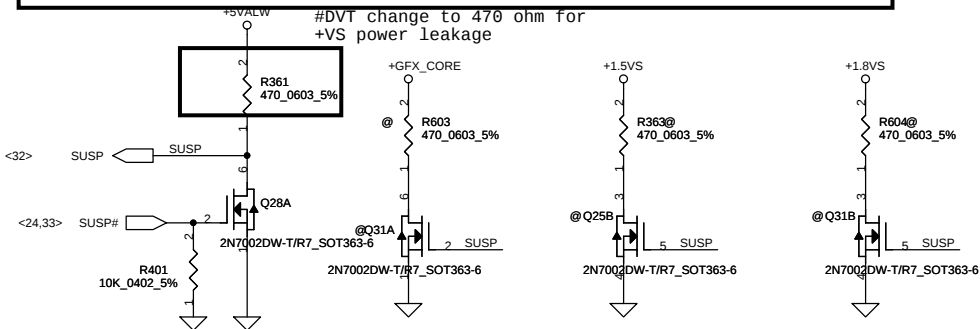
4/2 MP:For EMI ESD solution

3/23 For EMI ESD solution



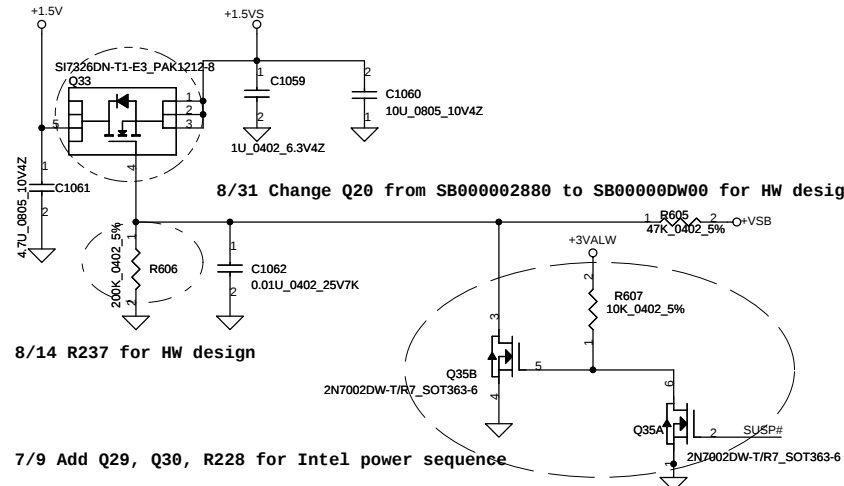
+3VS TO +3VS_PRIME

#DVT change to 470 ohm for +VS power leakage



+1.5V TO +1.5VS

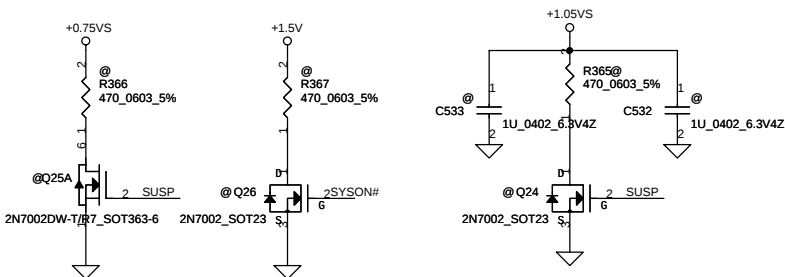
8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design



8/14 R237 for HW design

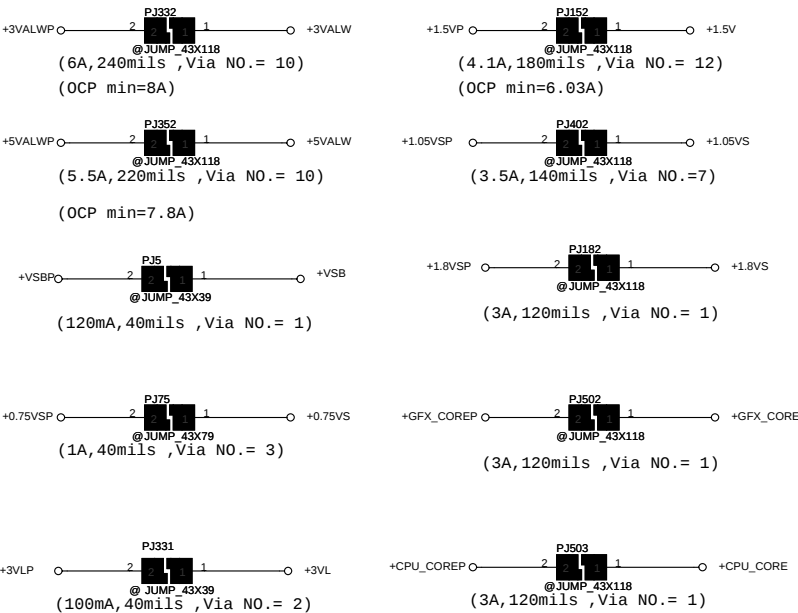
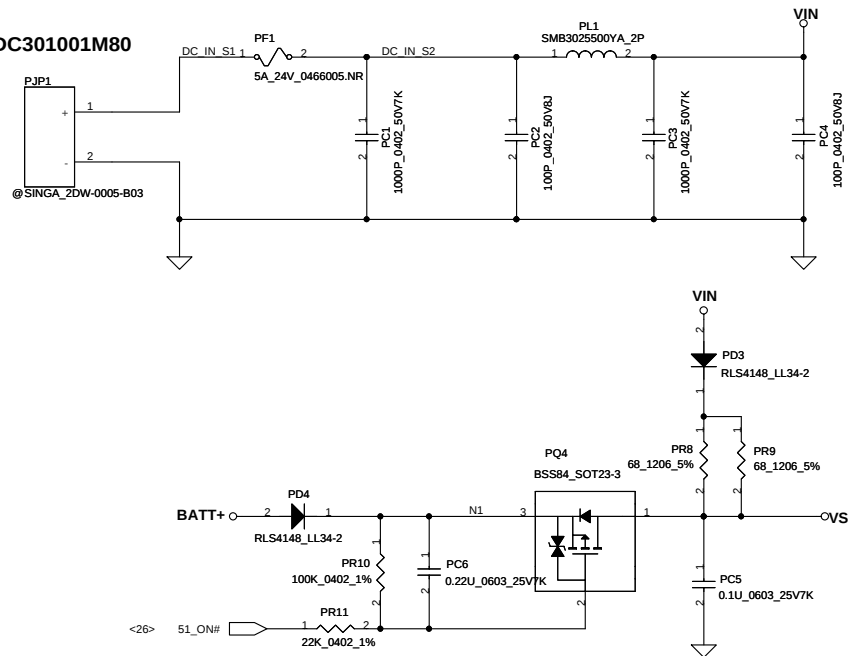
7/9 Add Q29, Q30, R228 for Intel power sequence

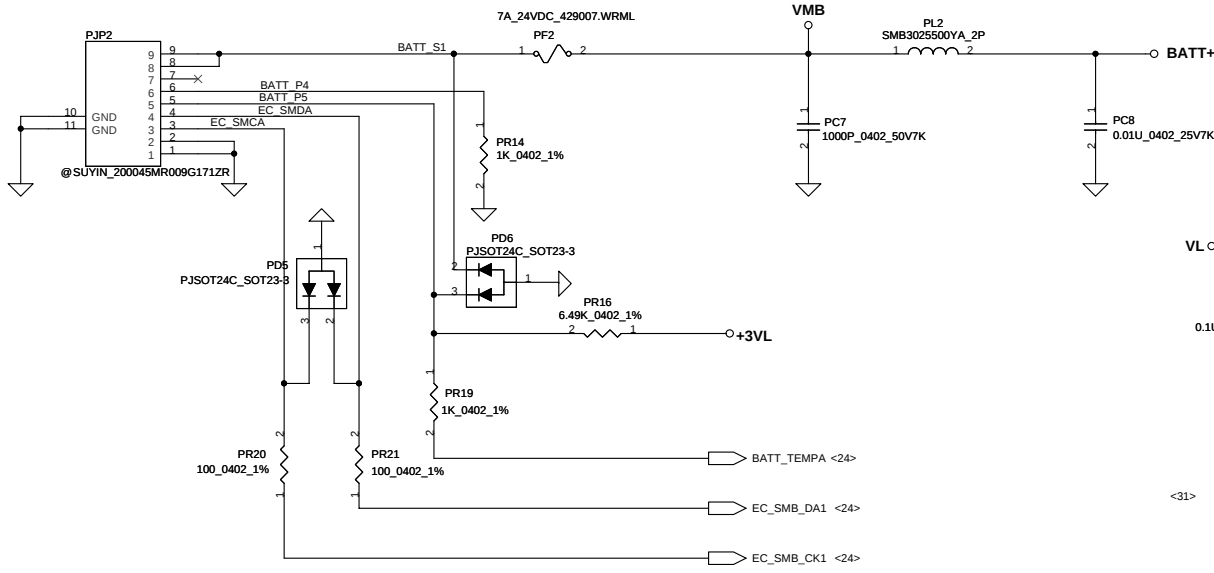
2/6 DVT: Reserve +1.5VS,+1.05VS,+0.75VS,+1.8VS discharge circuit



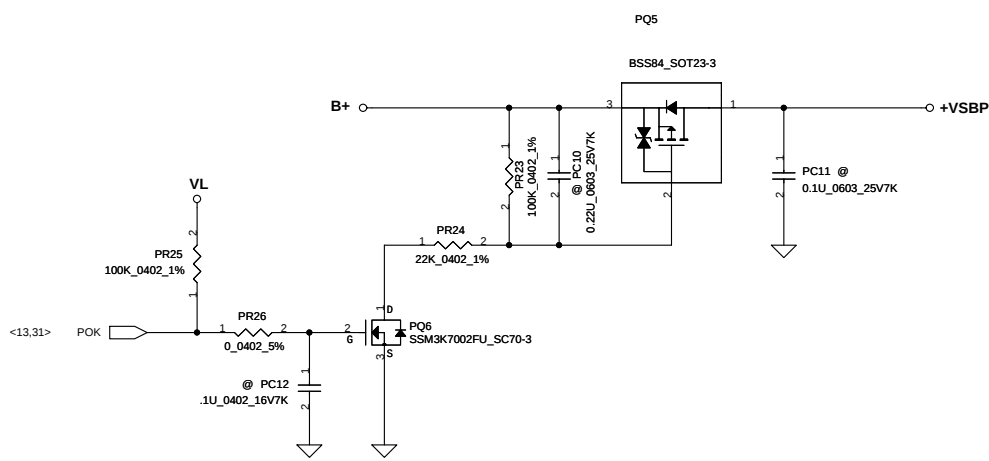
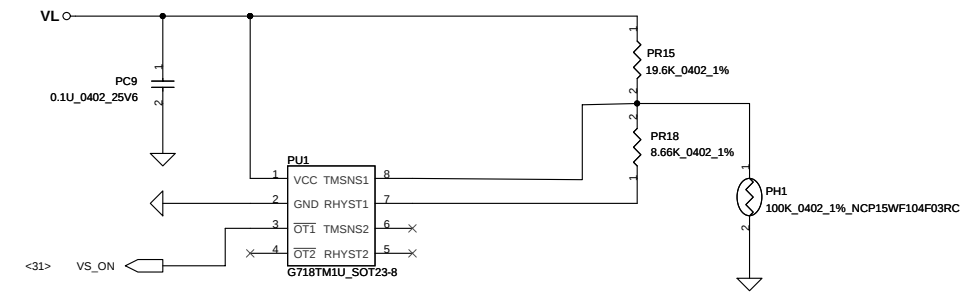
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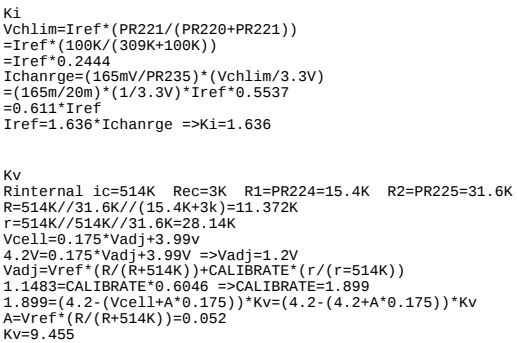
DC301001M80



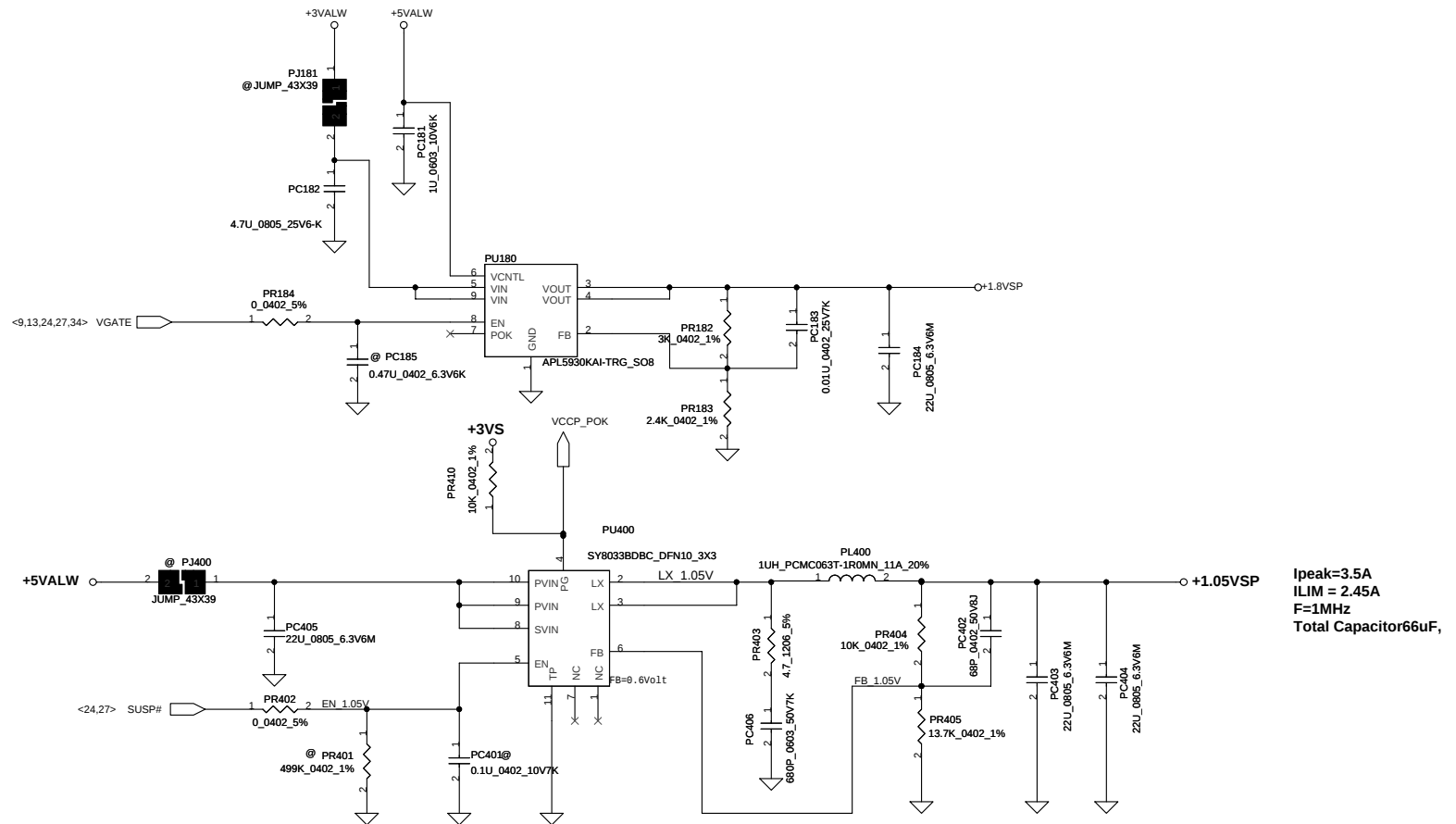


PH1 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C

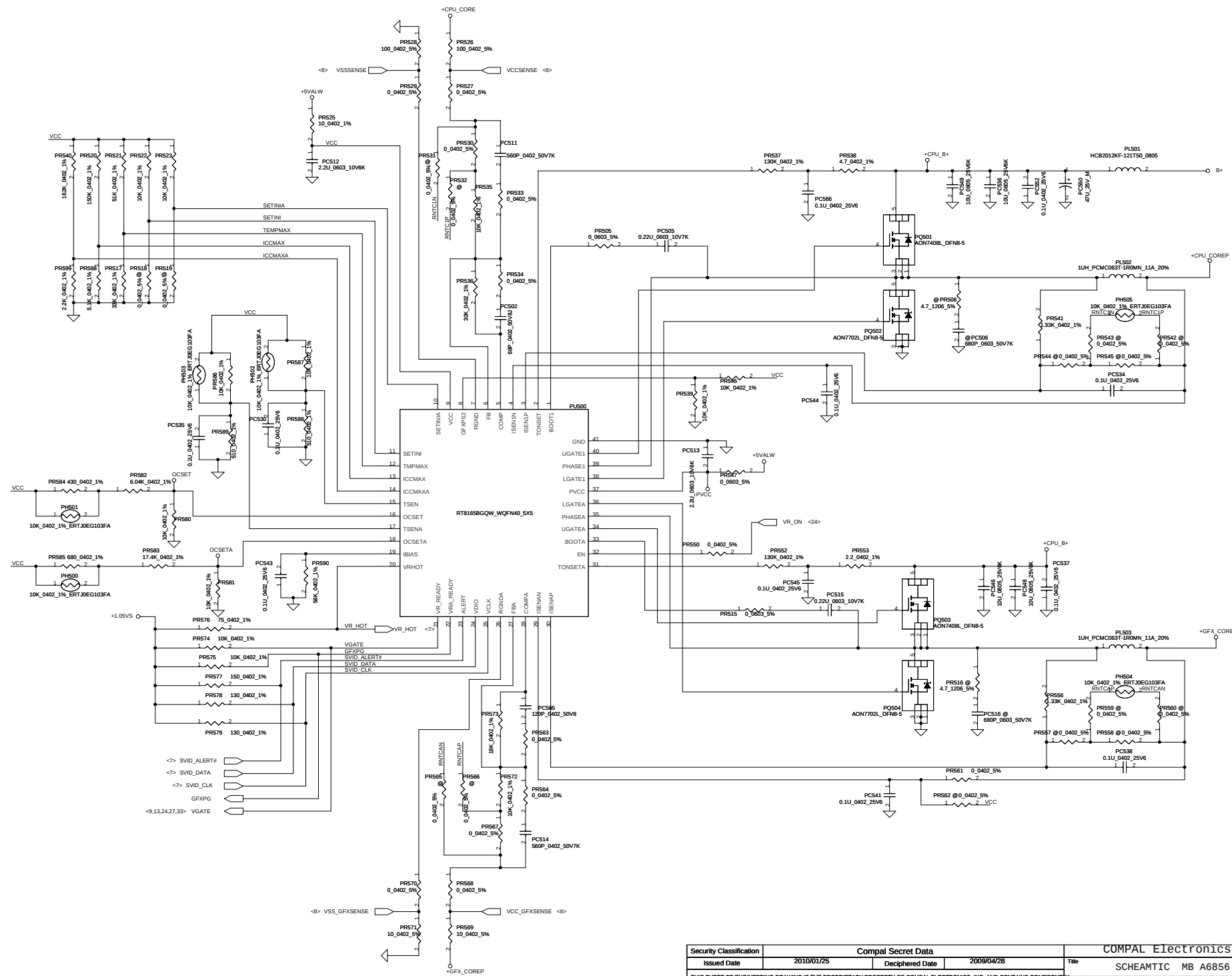




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