Compal Confidential

Cougar

LA-6851P Schematics Document

Intel Pine View Processor/ Tiger point

2010-10-10

REV: 1.0

Toshiba Satellite NB500 NB505

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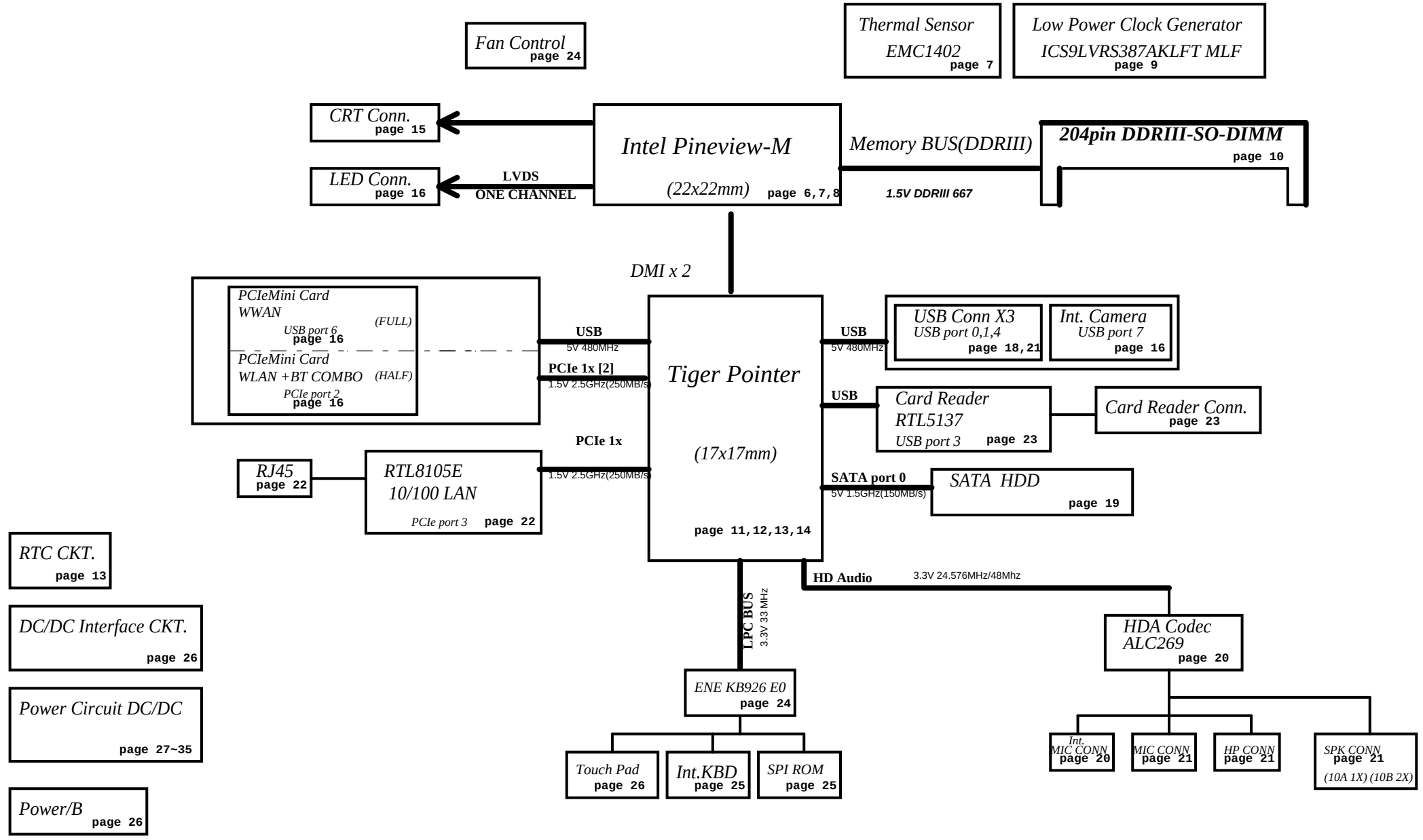
Model Name : PBU00
File Name : LA-6851P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
EMC1402	1001 010X b

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

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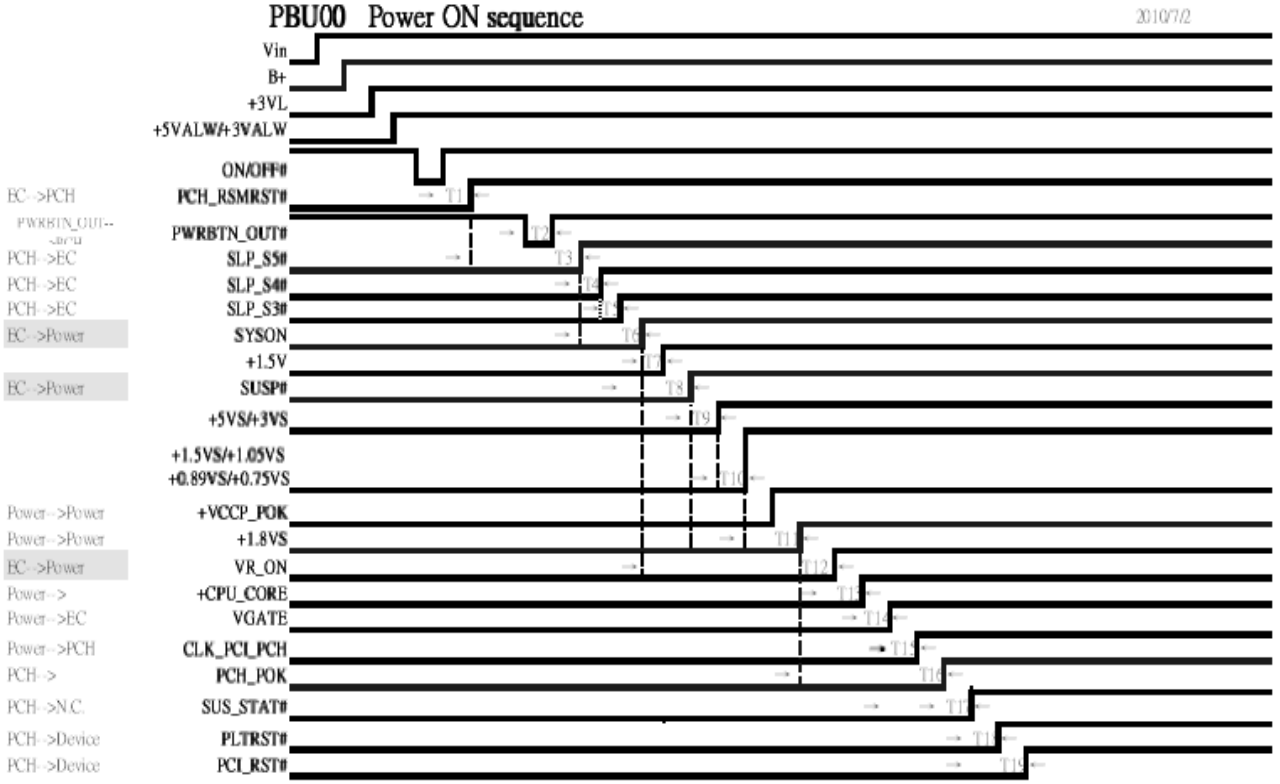

Power-on Sequence

Time	Description	Expected
T1	Power Button active to PCH_RSMRST# inactive	> 105ms
T2	Power Button active to PBTN_OUT# inactive	< T1
T3	PCH_RSMRST# inactive to PM_SLP_S5# inactive	< 110ms
T4	PM_SLP_S5# inactive to PM_SLP_S4# inactive	28.992us ~ 64.088us
T5	PM_SLP_S4# inactive to PM_SLP_S3# inactive	28.992us ~ 64.088us
T6	PM_SLP_S5# inactive to SYSON active	>10ms
T7	SYSON active to +1.5V active	>0
T8	PM_SLP_S3# inactive to SUSP# inactive	>10ms
T9	SUSP# inactive to +5VS active	>0
T9	SUSP# inactive to +3VS active	>0
T10	SUSP# inactive to +1.5VS active	> 0
T10	SUSP# inactive to +0.89VS active	> 0
T10	SUSP# inactive to +1.05VS active	> 0
T10	SUSP# inactive to +0.75VS active	>0
T11	+1.05VS inactive to +1.8VS active	>0
T12	SUSP# inactive to VR_ON active	>10ms
T13	VR_ON active to +CPU_CORE active	>0
T14	+CPU_CORE active to VGATE	<10ms
T15	VGATE active to CLK_PCI_ICH stable	< 1.8ms
T16	+1.5VS power active to ICH_PWROK active	>99ms
T17	ICH_PWROK active to SUS_STAT# inactive	0.928ms ~ 1.218ms
T18	SUS_STAT# inactive to PLT_RST# inactive	57.984us ~ 96.132us
T23	SUS_STAT# inactive to PCI_RST# inactive	57.984us ~ 96.132us

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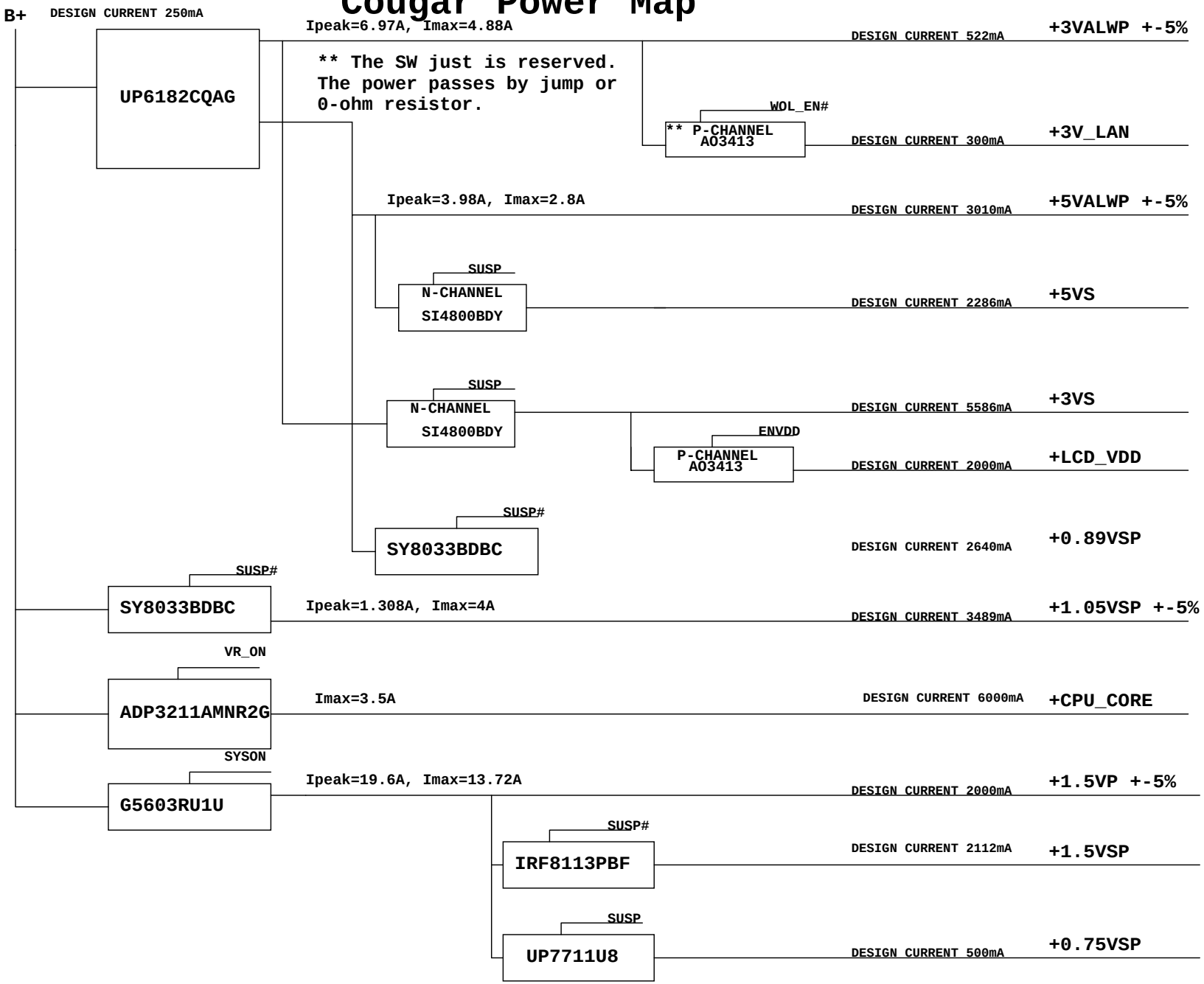
Cougar Power Map



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N455@
U1
U80610006237AA SLBX9 A0 1.66G

N475@
U1
AU80610006240AA SLBX5

PINEVIEW_M

U1A

REV = 1.1

DMI

PINEVIEW-M_FCBGA8559

1 OF 6

N550@

Close to CPU

Pull-down must be placed within 500 mils from Pineview-M

Reserve PM_SLP_S4# to turn on DRAM_PWROK

MP Remove XDP resistor for ESD

2010.07.12 RF request

PINEVIEW_M

U1B

REV = 1.1

DDR_A

2 OF 6

PINEVIEW-M_FCBGA8559

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PINEVIEW_M

U1C

XDP_RSVD_00 XDP_RSVD_01 XDP_RSVD_02 XDP_RSVD_03 XDP_RSVD_04 XDP_RSVD_05 XDP_RSVD_06 XDP_RSVD_07 XDP_RSVD_08 XDP_RSVD_09 XDP_RSVD_10 XDP_RSVD_11 XDP_RSVD_12 XDP_RSVD_13 XDP_RSVD_14 XDP_RSVD_15 XDP_RSVD_16 XDP_RSVD_17

RSVD

RSVD_TP

VGA

CRT_HSYNC CRT_VSYNC CRT_RED CRT_GREEN CRT_BLUE CRT_IRTN CRT_DDC_DATA CRT_DDC_CLK DAC_IREF

REFCLKINP REFCLKINN REFSSCLKINP REFSSCLKINN

PM_EXTTS#_1/DPRSLPVR PM_EXTTS#_0 PWROK RSTIN#

HPL_CLKINN HPL_CLKINP

MISC

3 OF 6

PINEVIEW-M_FCBGA8559

GMCH_CRT_HSYNC <15>
GMCH_CRT_VSYNC <15>
GMCH_CRT_R <15>
GMCH_CRT_G <15>
GMCH_CRT_B <15>
GMCH_CRT_DATA <15>
GMCH_CRT_CLK <15>

R510 be placed <500 mils to U1.P28

R509 be placed U1.R22

R510 665_0402_1%

CPU_DREFCLK <9>
CPU_DREFCLK# <9>
CPU_SSCDREFCLK <9>
CPU_SSCDREFCLK# <9>

0_0402_5%
R512

PM_DPRSLPVR <13>
PM_EXTTS#0 <10>
PCH_POK <13>
PLTRST# <13,17,22>

CLK_CPU_HPLCLK# <9>
CLK_CPU_HPLCLK <9>

To be placed <250 mils to U1 ball

GMCH_CRT_R R514 150_0402_1%
GMCH_CRT_G R515 150_0402_1%
GMCH_CRT_B R516 150_0402_1%
ENBKL R517 100K_0402_5%

To be placed <500 mils to U1 ball

RF@C205 LCD_EDID_CLK 12P_0402_50V8J
RF@C206 LCD_EDID_DATA 12P_0402_50V8J

2010.07.12 RF request

PVT C205, C206 change to 12p and stuff for RF

XDP_RSVD_9 R518 1K_0402_5%

U1D

PINEVIEW_M

LA_CLKN LA_CLKP LA_DATAN_0 LA_DATAP_0 LA_DATAN_1 LA_DATAP_1 LA_DATAN_2 LA_DATAP_2

LIBG LVBG LVREFH LVREFL LBKLT_EN LBKLT_CTL LCTLA_CLK LCTLB_DATA LDDC_CLK LDDC_DATA LVDD_EN

LVDS

<16> LCD_TXCLK- <16> LCD_TXCLK+ <16> LCD_TXOUT0- <16> LCD_TXOUT0+ <16> LCD_TXOUT1- <16> LCD_TXOUT1+ <16> LCD_TXOUT2- <16> LCD_TXOUT2+

R509 2.37K_0402_1% L_IBG

<24> ENBKL <16> GMCH_INVT_PWM ENBKL

<16> LCD_EDID_CLK <16> LCD_EDID_DATA <16> GMCH_ENVDD

+3VS R513 10K_0402_5%

Close to Processor pin

PM_EXTTS#0

BPM_1_0# BPM_1_1# BPM_1_2# BPM_1_3#

BPM_2_0#/RSVD BPM_2_1#/RSVD BPM_2_2#/RSVD BPM_2_3#/RSVD

CPU

Close to CPU

Close to CPU

RSVD TDI TDO TCK TMS TRST#

<6> XDP_TDI <6> XDP_TDO <6> XDP_TCK <6> XDP_TMS <6> XDP_TRST#

H_THERMDA H_THERMDC THRMDA_1 THRMDC_1

THRMDA_2/RSVD THRMDC_2/RSVD

4 OF 6

PINEVIEW-M_FCBGA8559

SMI# A20M# FERR# LINT0 LINT1 IGNNE# STPCLK#

DPRSTP# DPSLP# INIT# PRDY# PREQ#

THERMTRIP#

PROCHOT# CPUPWRGOOD

GTLREF VSS

RSVD RSVD

BCLKN BCLKP

BSEL_0 BSEL_1 BSEL_2

VID_0 VID_1 VID_2 VID_3 VID_4 VID_5 VID_6

RSVD RSVD RSVD RSVD

RSVD_TP RSVD_TP EXTBGREF

H_SMI# <11>
H_A20M# <11>
H_FERR# <11>
H_INTR <11>
H_NMI <11>
H_IGNNE# <11>
H_STPCLK# <11>

H_DPRSTP# <13>
H_DPSLP# <13>
H_INIT# <11>
XDP_PREQ# <6>

Close to CPU

H_THERMTRIP# <11>

Close to CPU +1.05VS

68_0402_5% R511

H_PROCHOT#
H_PWRGD <13>

H_GTLREF

CLK_CPU_BCLK# <9>
CLK_CPU_BCLK <9>

CPU_BSEL0 <9>
CPU_BSEL1 <9>
CPU_BSEL2 <9>

CPU_VID0 <35>
CPU_VID1 <35>
CPU_VID2 <35>
CPU_VID3 <35>
CPU_VID4 <35>
CPU_VID5 <35>
CPU_VID6 <35>

T39 T40

H_EXTBGREF

CPU THERMAL SENSOR

+3VS C961 0.1U_0402_16V4Z

U2

VDD DP DN THERM# SMCLK SMDATA ALERT# GND

H_THERMDA H_THERMDC C968 2200P_0402_50V7K CPU_THERM#

EC_SMB_CK2 EC_SMB_DA2 @R523 10K_0402_5%

+3VS R524 10K_0402_5%

EMC1402-1-ACZL-TR_MSOP8

Address:0100_1100 EMC1402-1
Address:0100_1101 EMC1402-2

H_DPRSTP# C954 H_DPSLP# C955 H_PWRGD C956 H_A20M# C957 H_IGNNE# C958 H_INIT# C959 H_INTR C960 H_FERR# C962 H_NMI C965 H_SMI# C966 H_STPCLK# C967

@ 220P_0402_50V7K

PVT C959, C960 stuff for ESD

ESD request

placed within 0.5" of processor pin.

+1.05VS R519 1K_0402_1% H_GTLREF C963 220P_0402_50V7K R521 2K_0402_1%

placed within 0.5" of processor pin and 5 mils spacing

+1.05VS R520 976_0402_1% H_EXTBGREF C964 1U_0402_6.3V6K R522 3.3K_0402_1%

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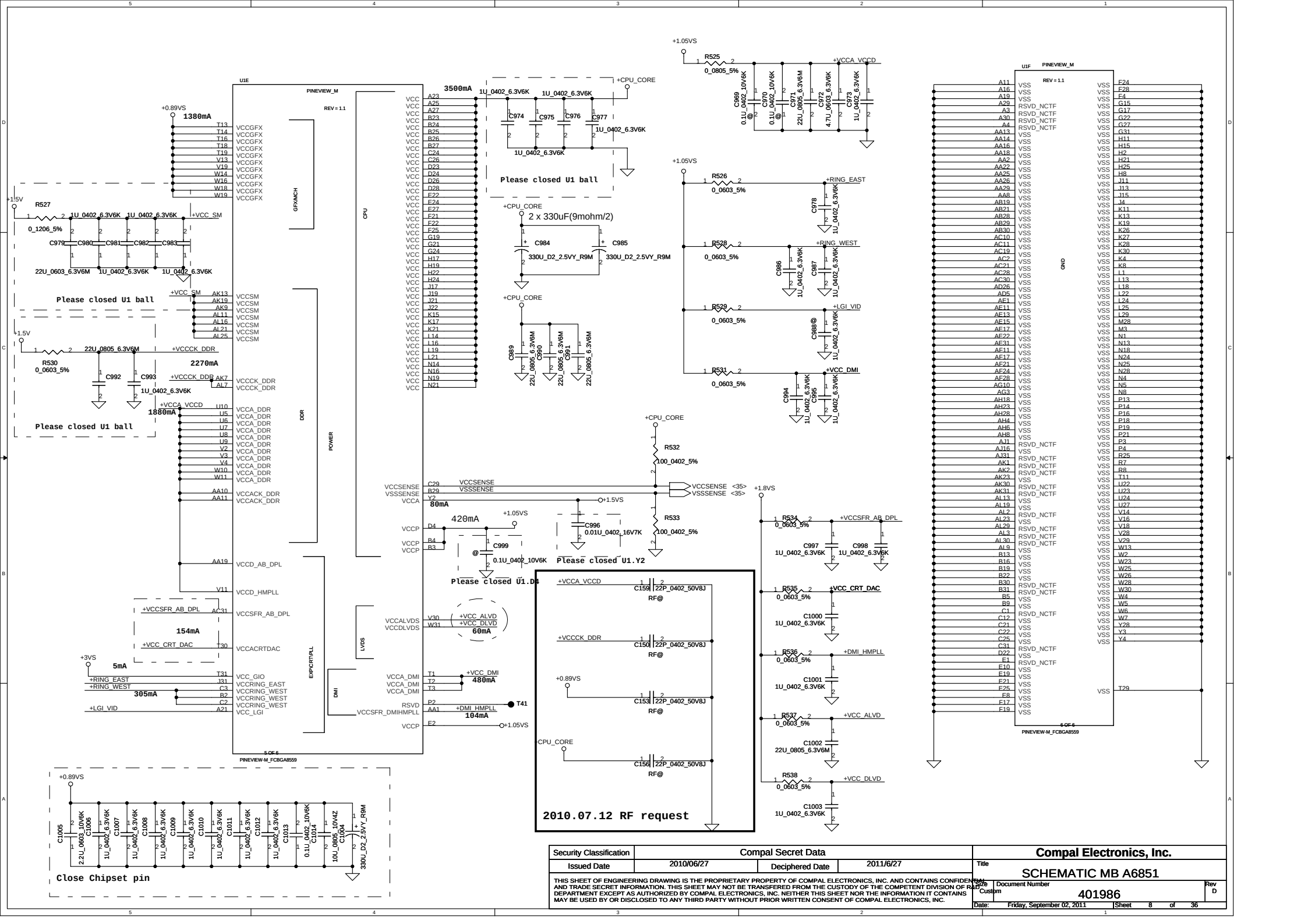

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff

2010.03.23 Change R81 from bead to 0 ohm

2010.03.23 Change R477 from bead to 0 ohm

8/27 Delete C93, C94, C95, C102 for low power CLK GEN

7/13 For RF request

7/13 Add 33pFfor RF request

7/21 Reserve 33pFfor RF request

SA00003H610 (ICS :CS9LVRS387AKLFT MLF)

Low power CLK Gen.

7/21 Delete C296, C297 for RF request

7/13 Add 22pF to gnd and close to U3 for RF request

7/21 Reserve 22pF to gnd and close to U3 for RF request

8/24 Change net name to FSB for U3.2

7/13 Add 33pF to GND for RF request

7/21 Reserve 33pF to GND for RF request

8/27 C303, C324, C325, C326, C327 to GND for RF request

7/22 Add R241 pull up to +3VS for RF Intel request

8/14 Add R250 pull up for Intel request

7/22 Add R242 to R253 for Intel request

Routing the trace at least 10mil

2010.03.09 Change Y1 to 5 x3.2 size

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#

For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

2010.07.12 RF request

7/21 Change WWAN_CLKREQ# from REQ4 to REQ11

SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	CPU_EXP
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

REQ PORT LIST

PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

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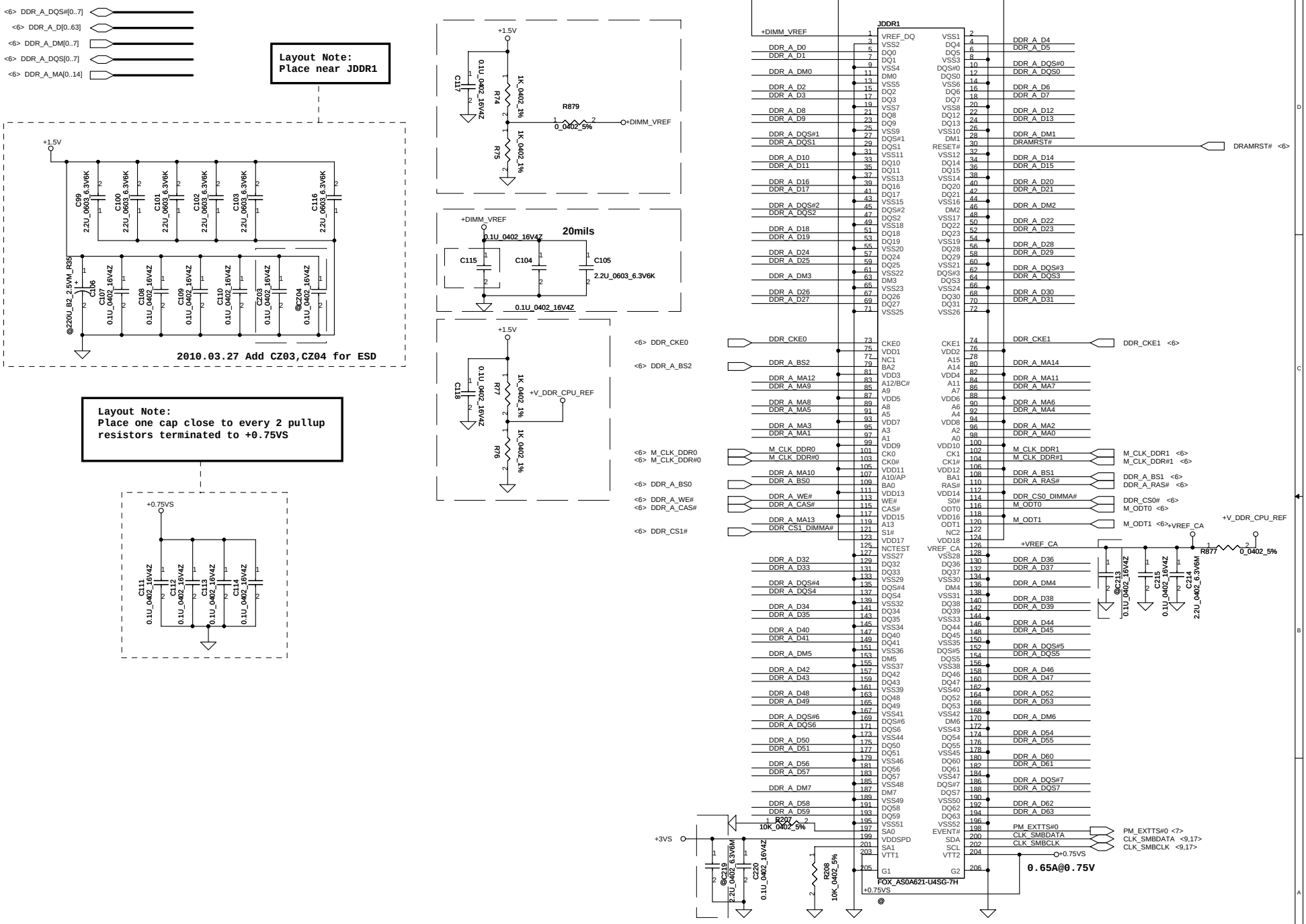

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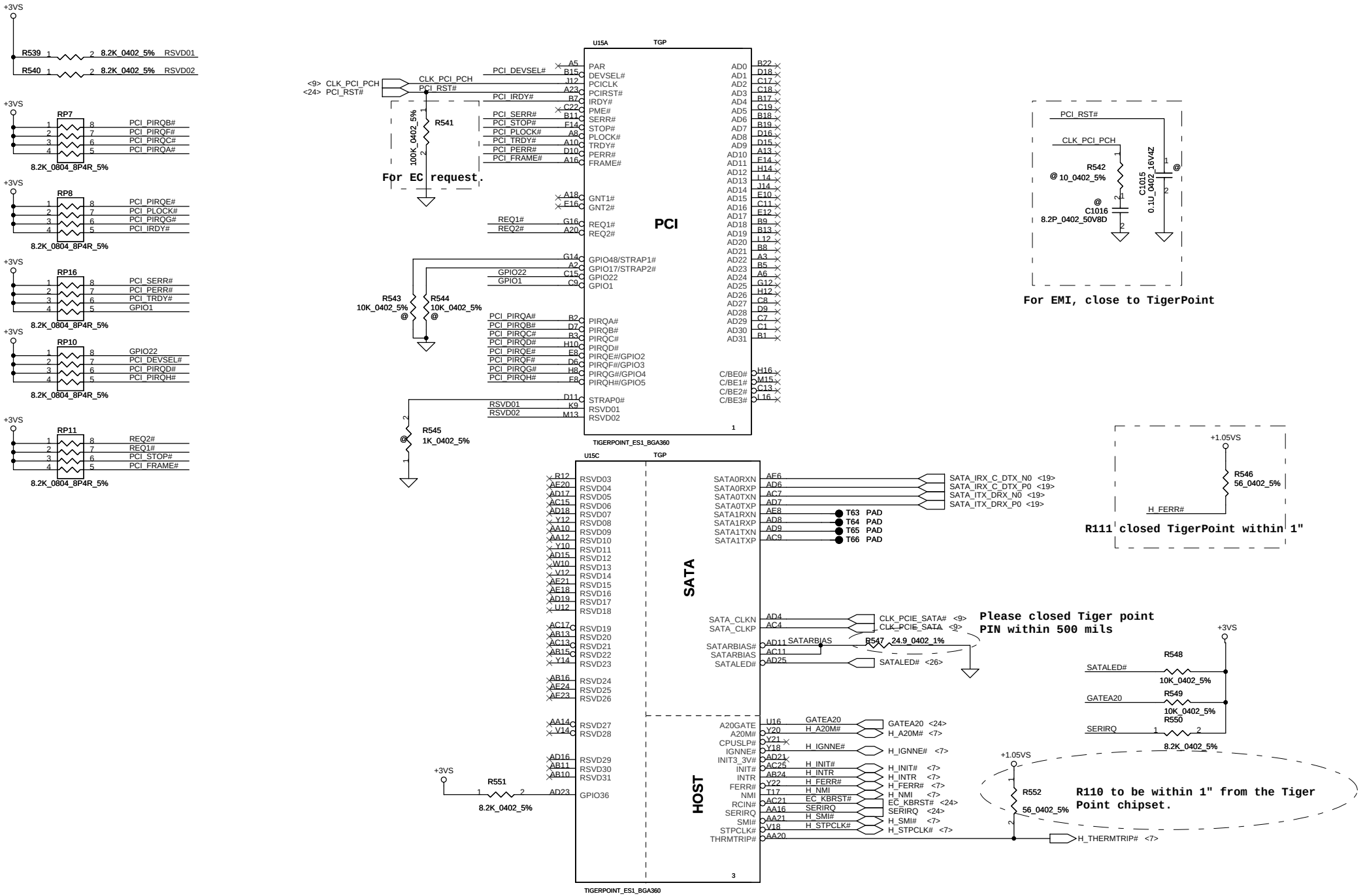

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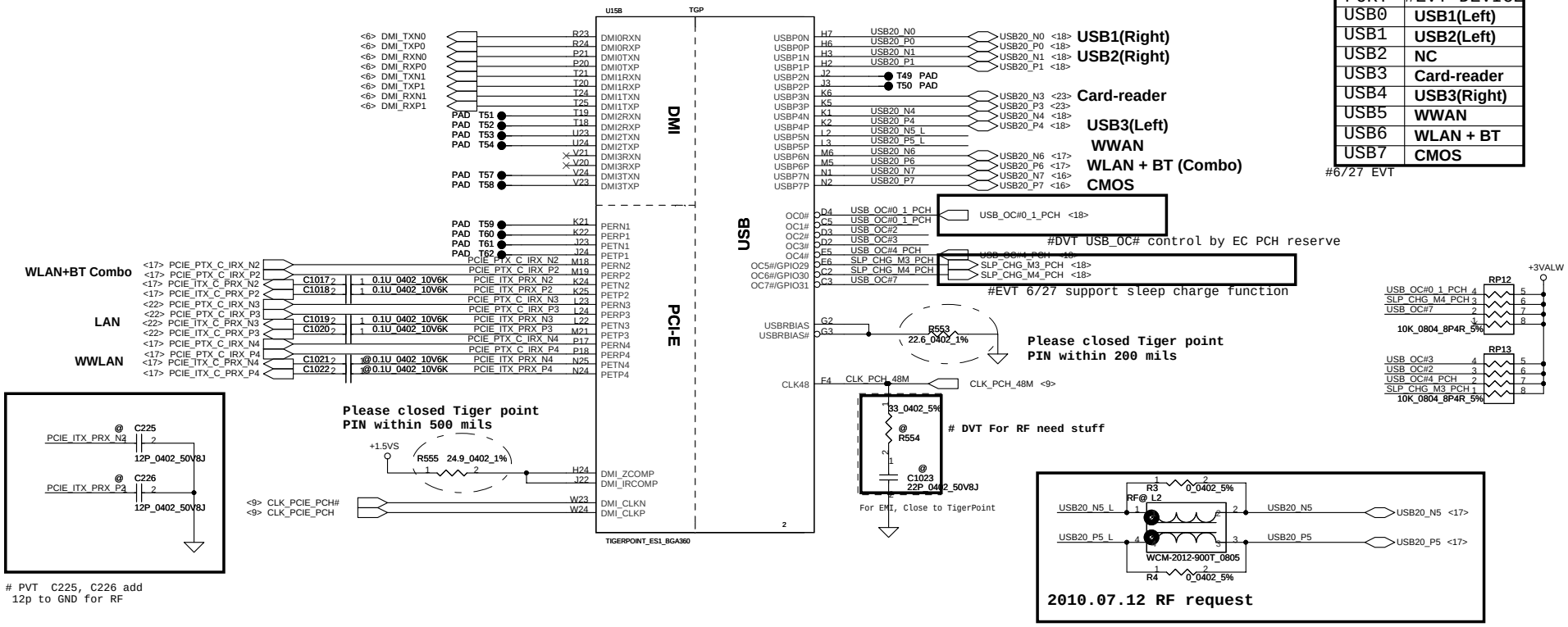
USB PORT LIST

PORT	#EVT DEVICE
USB0	USB1(Left)
USB1	USB2(Left)
USB2	NC
USB3	Card-reader
USB4	USB3(Right)
USB5	WWAN
USB6	WLAN + BT
USB7	CMOS

#6/27 EVT



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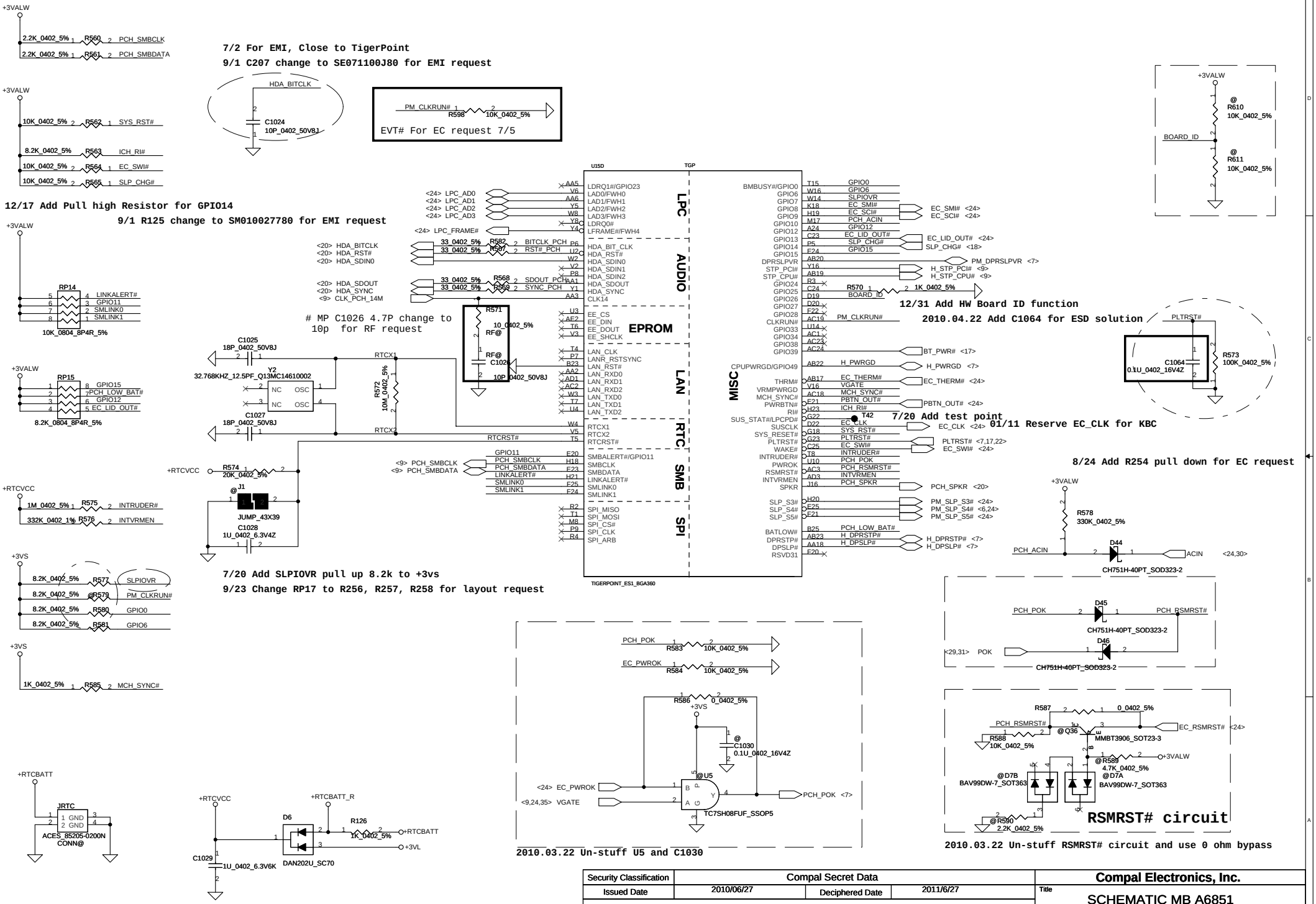

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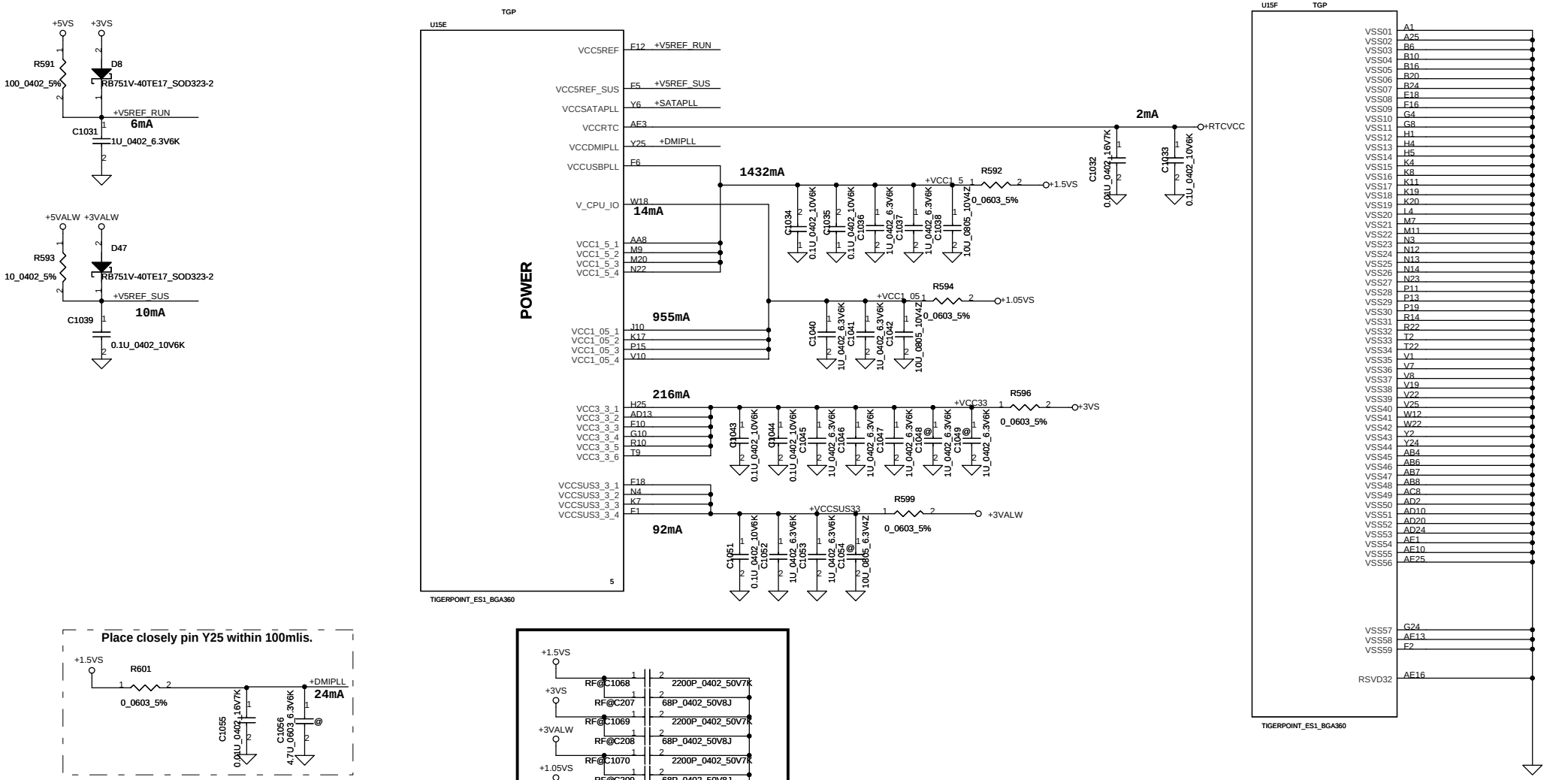

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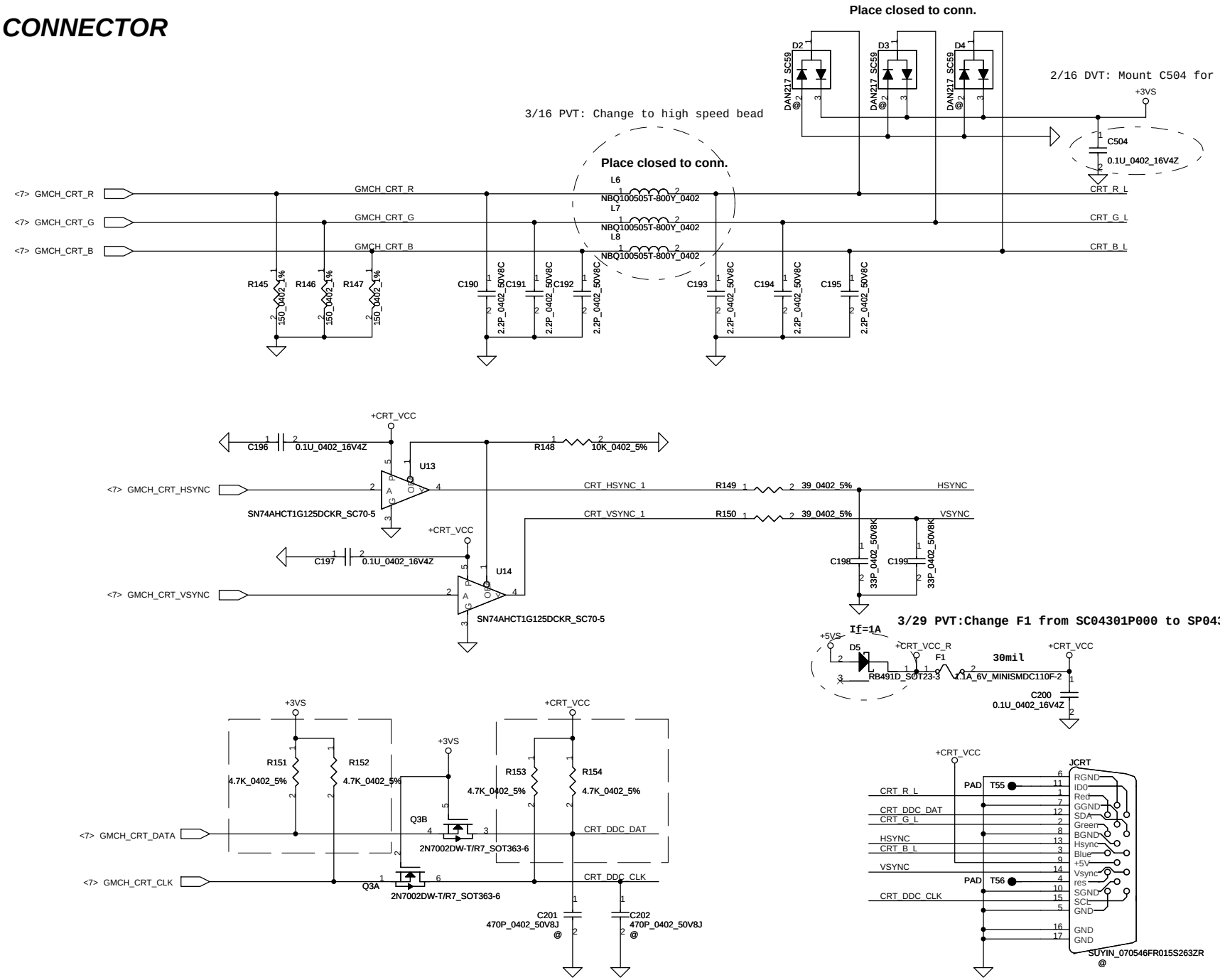
CRT CONNECTOR



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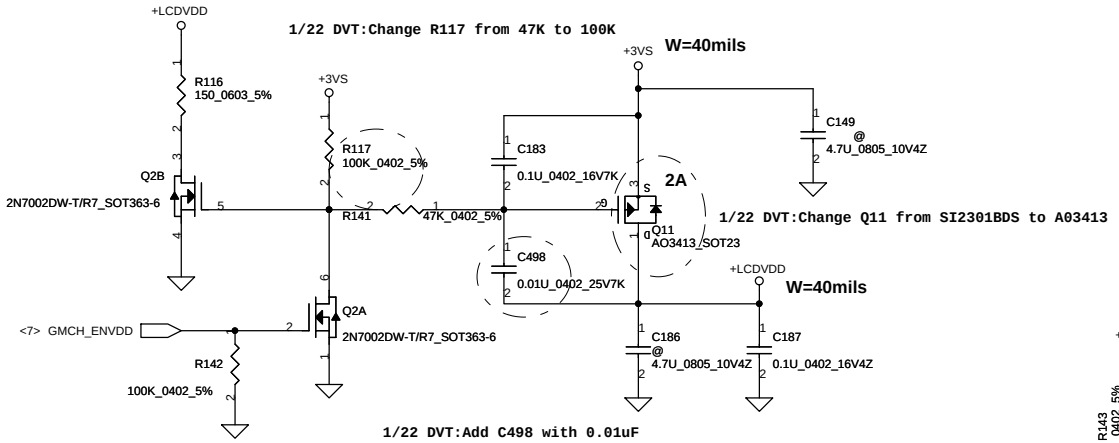
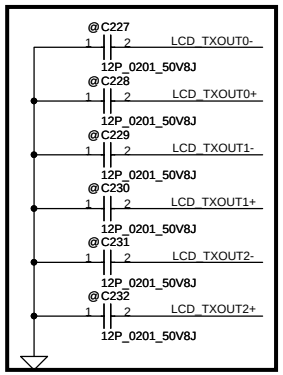
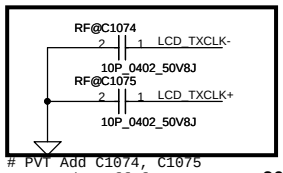
LCD POWER CIRCUIT

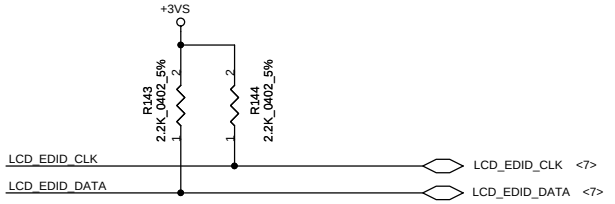


MP Add C227~C232 for RF request

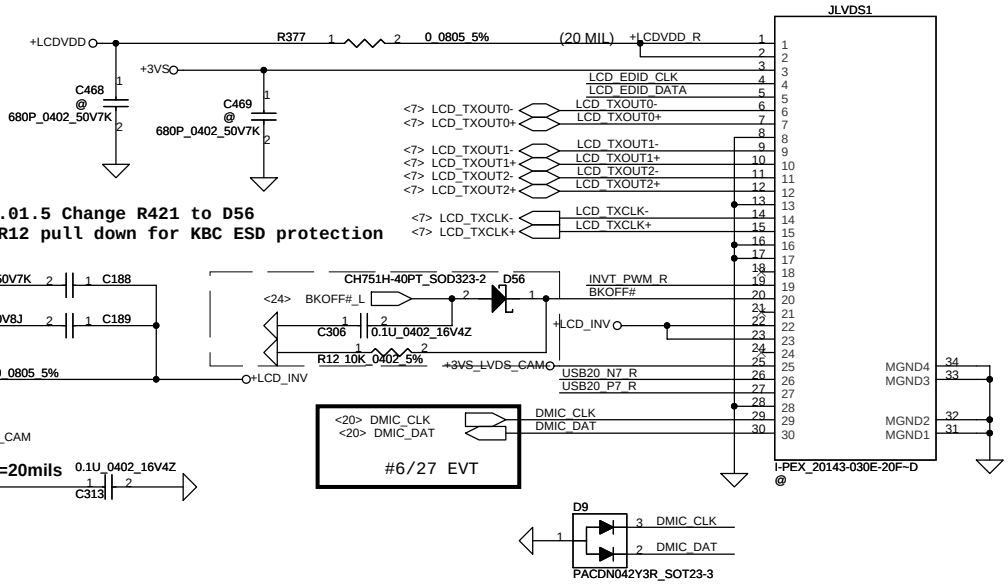


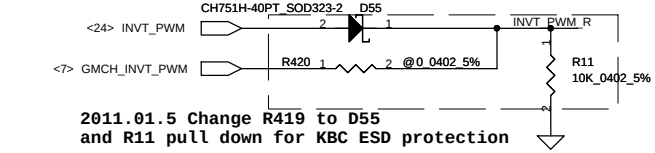


PVT Add C1074, C1075
10p and stuff for RF

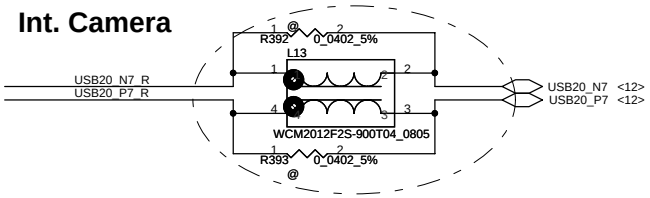


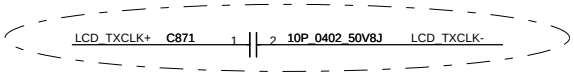
LED/PANEL BD. Conn.





Int. Camera





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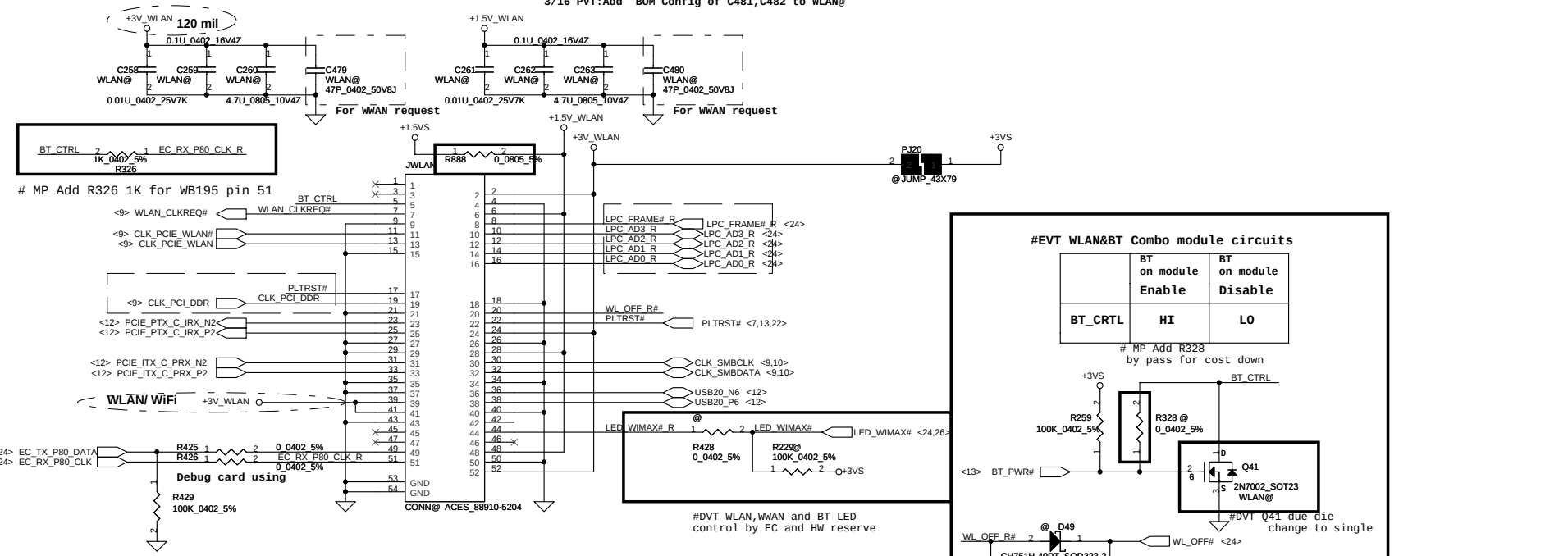
Mini-Express Card for WLAN/WiMax

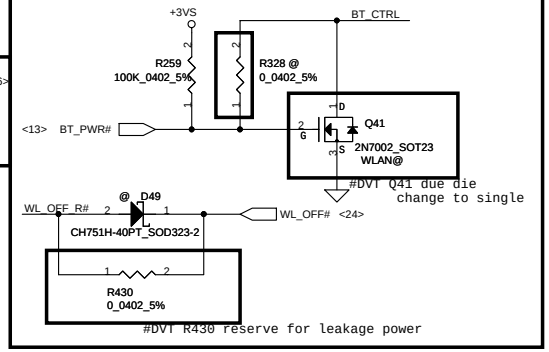
2/25 PVT:Mount C479,C480 with 47pf
3/16 PVT:Add BOM Config of C481,C482 to WLAN@



#EVT WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO

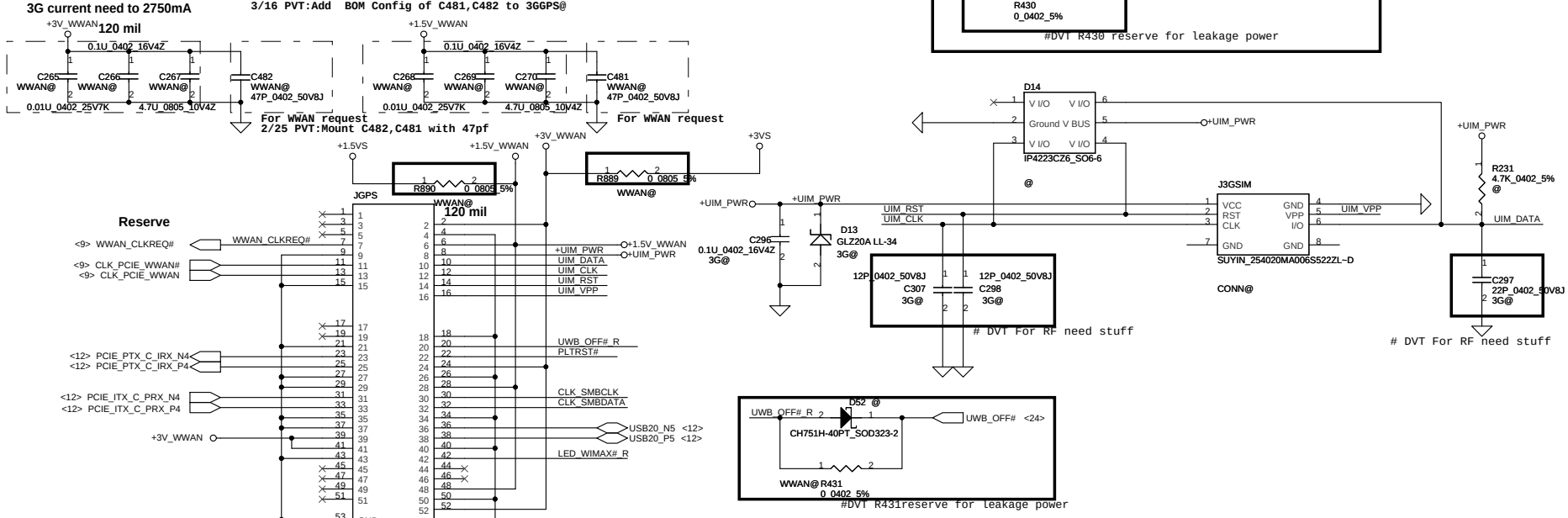
MP Add R328
by pass for cost down



Mini-Express Card for 3G/GPS

3G current need to 2750mA

3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@



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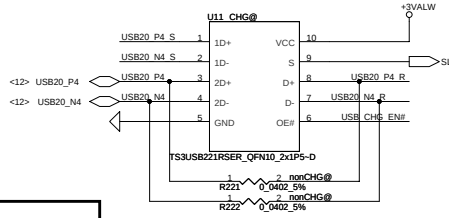
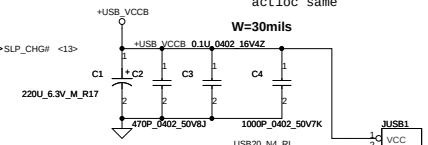
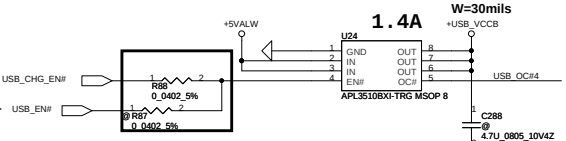
USB CONN- -Left

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

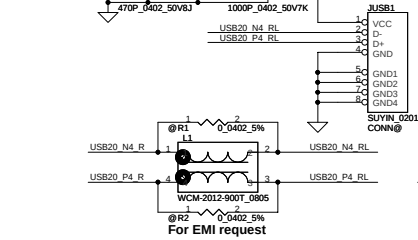
SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



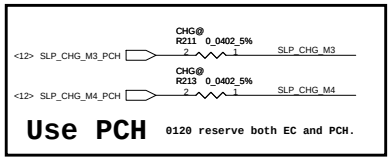


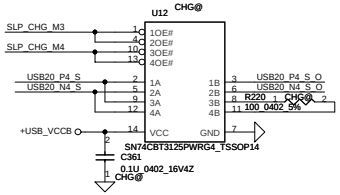


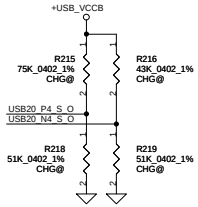
#PVT R88 CHG@ change to
always stuff for OC protect
actioc same

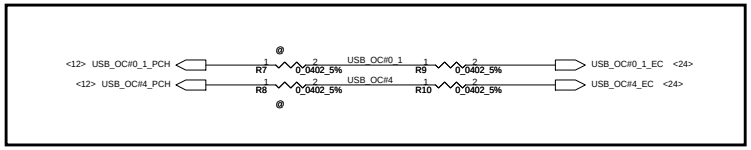


For EMI request









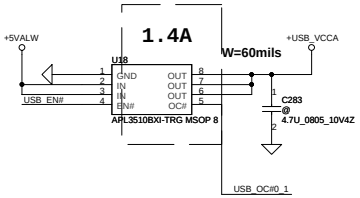
#DVT USB_OC# control by EC

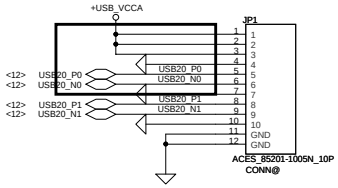
For EMI request

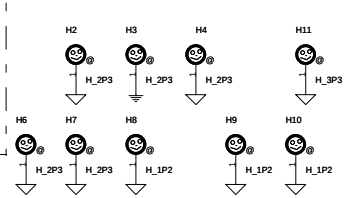
2/3 DVT: Change D38,D37 from PRTR5V0U2X_SOT143-4 to CM1293A-04SO_SOT23-6

For EMI request

USB CONN

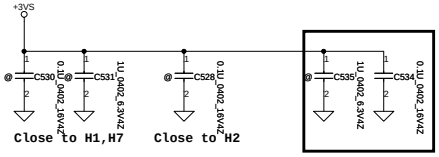






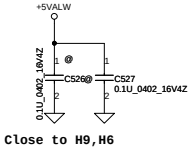
PVT Add H14 and remove H1

Add 0.1u Caps for each screw hole for ESD rule



Close to H1,H7 Close to H2

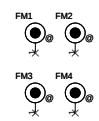
PVT Close to H4



Close to H9,H6

2010.07.20 Add for ESD solution

FIDUCIAL_C40M80



Close to H5

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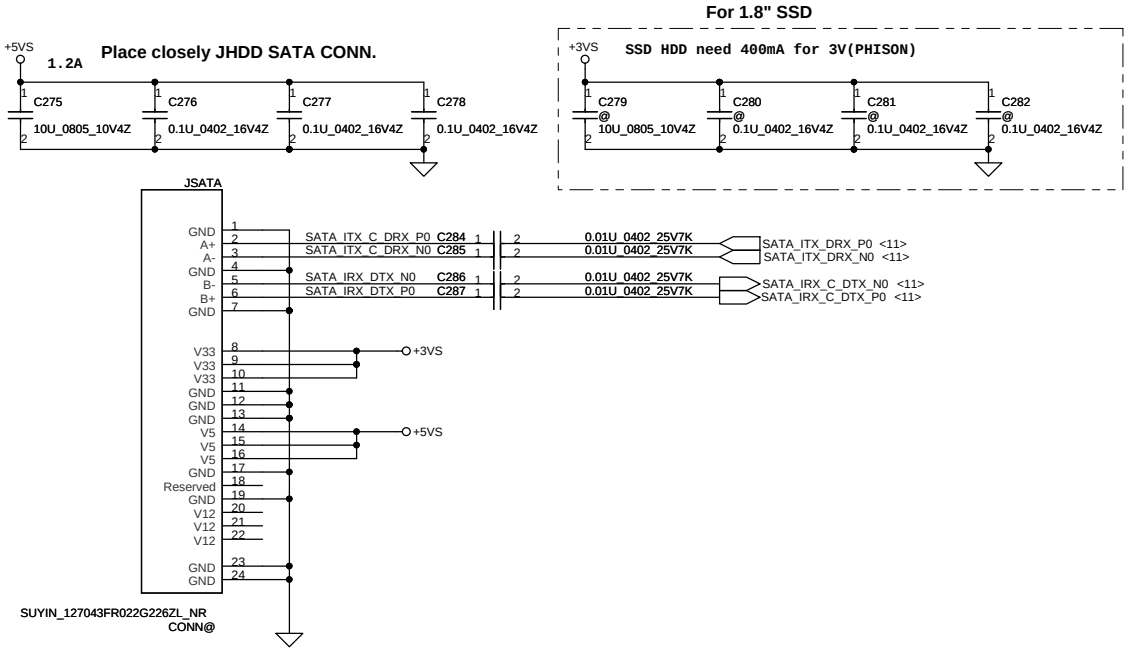
SATA Conn.



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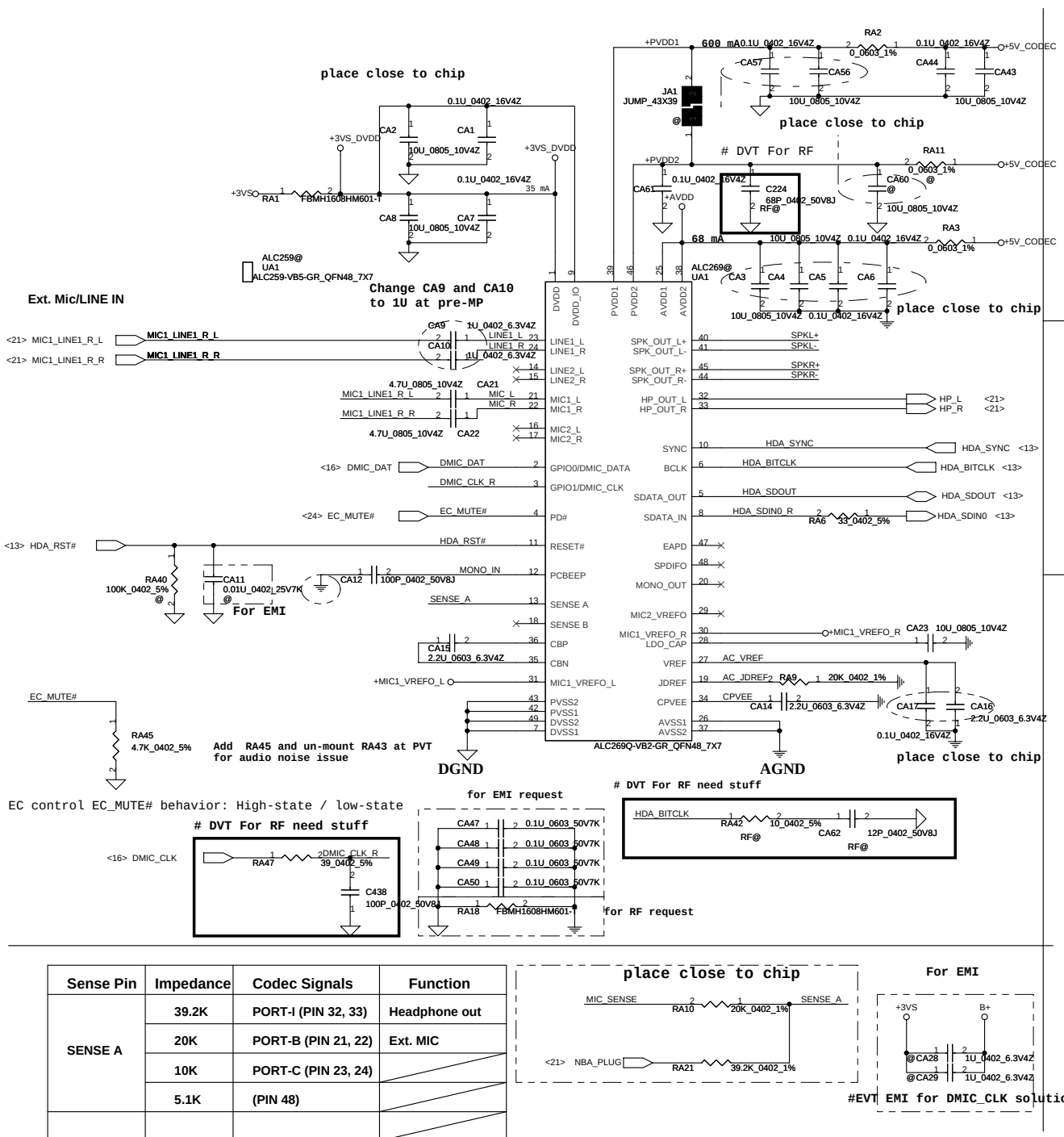

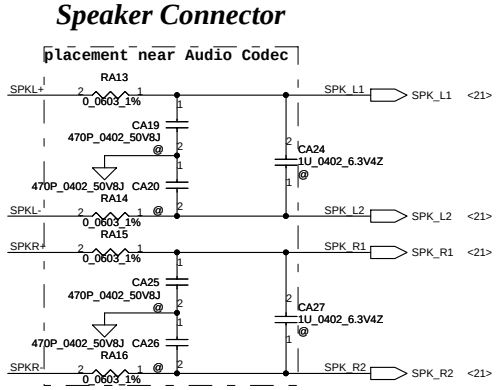

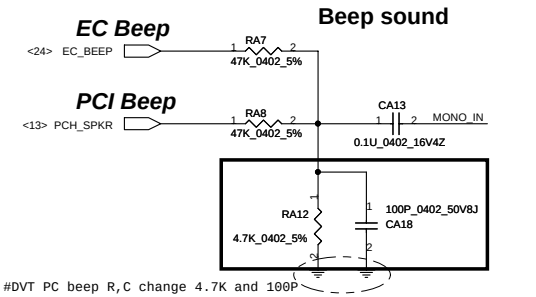

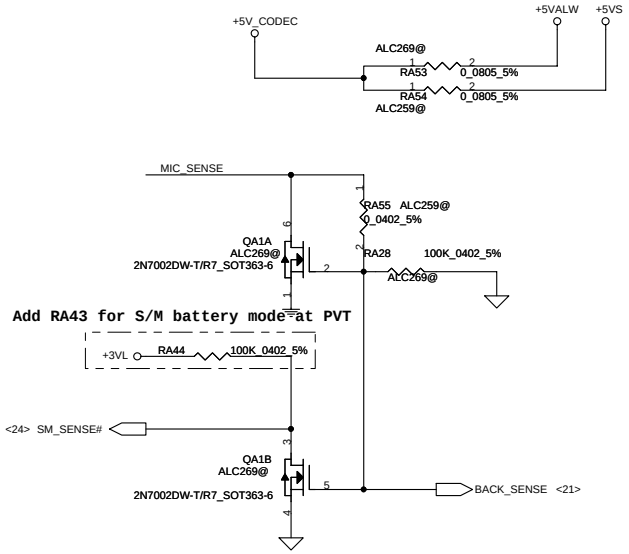

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

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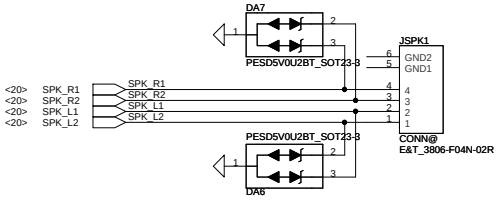
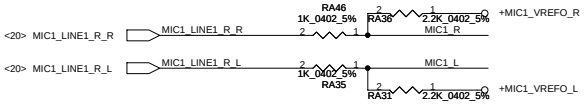
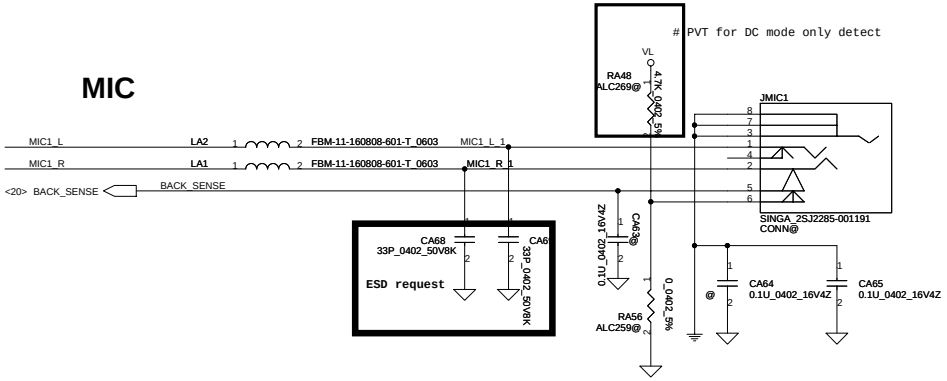
SPEAKER



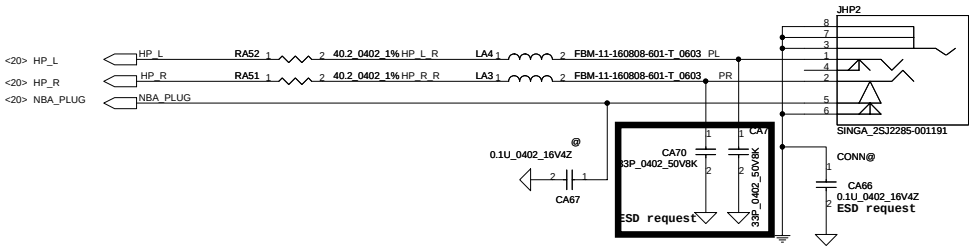
Ext.MIC/LINE IN JACK



MIC



Head phone



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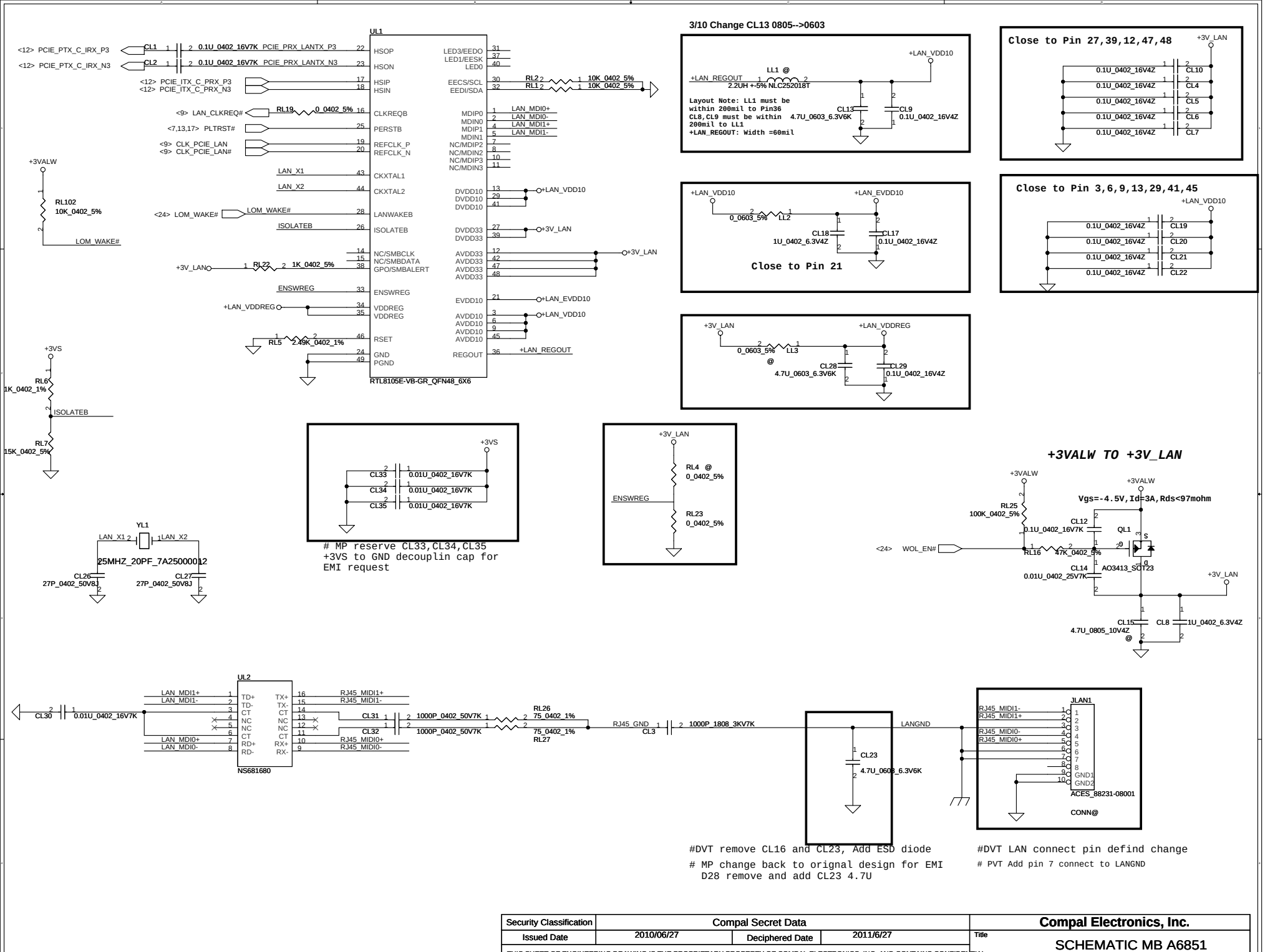

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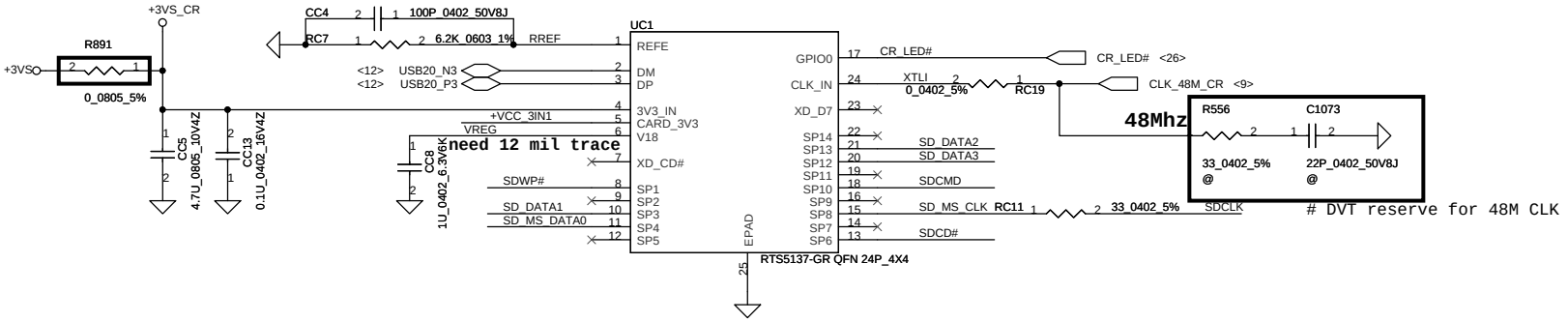
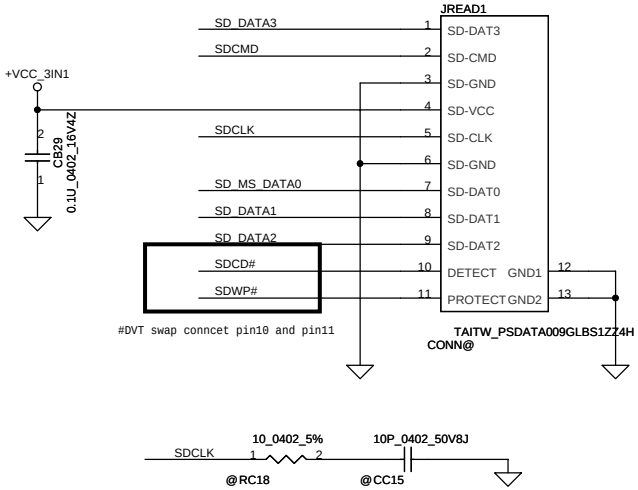
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



2 in 1 Card Reader



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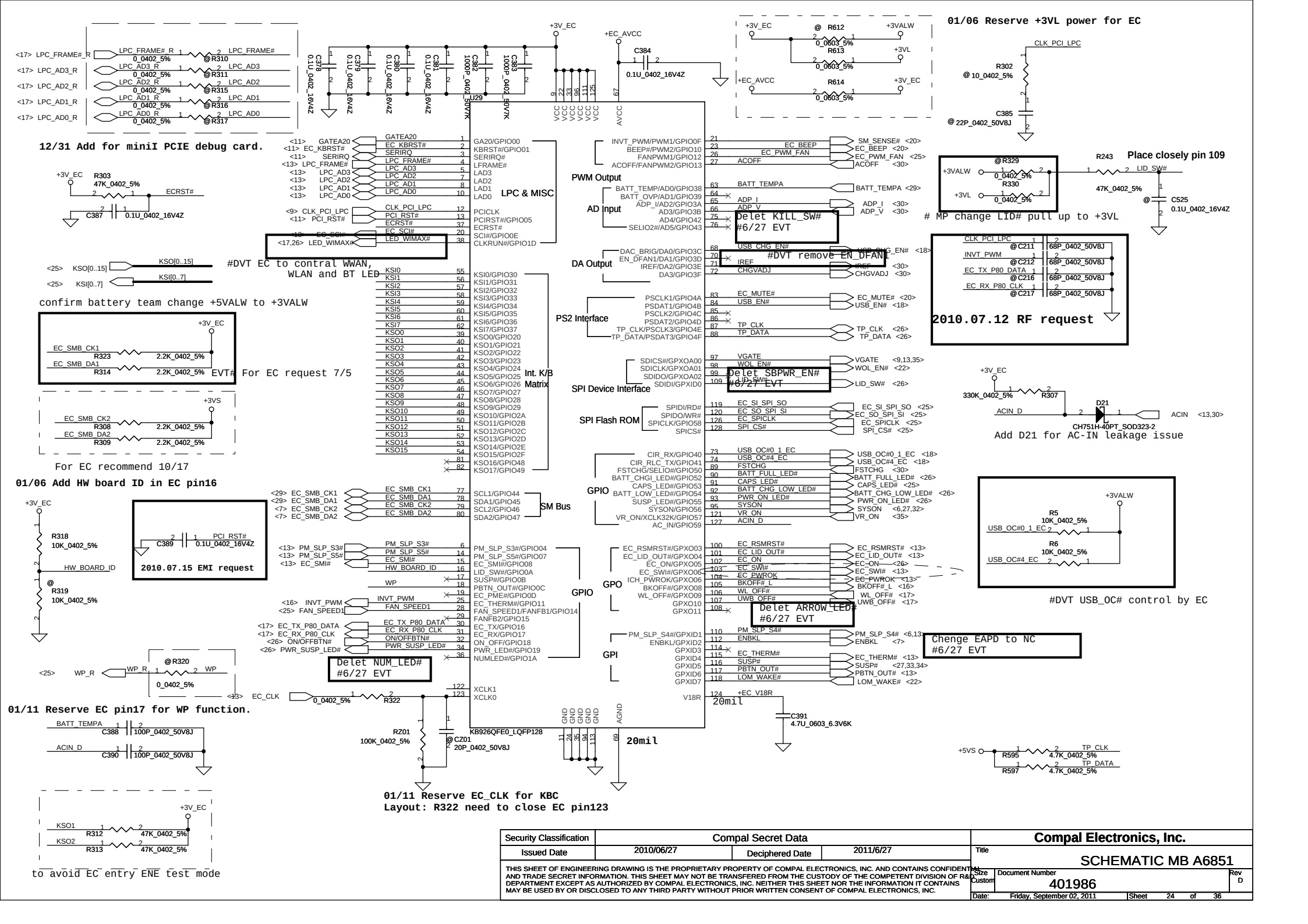

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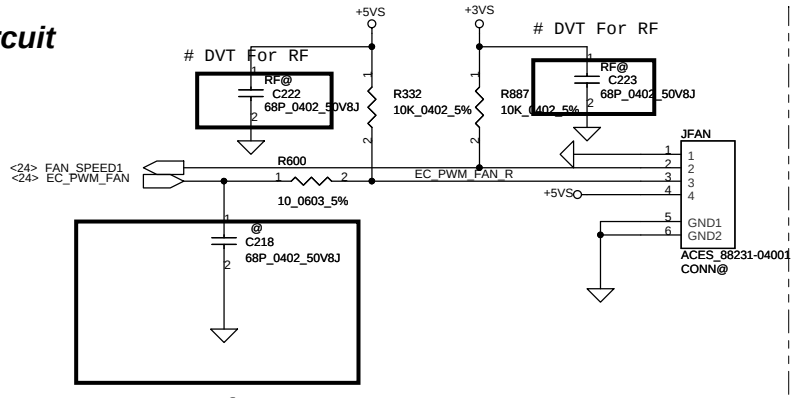
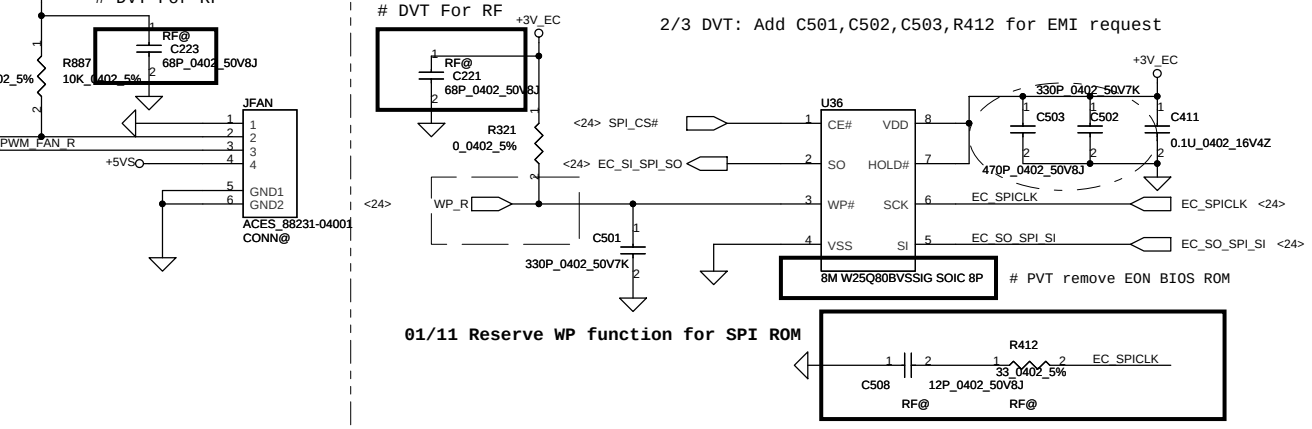
FAN Control Circuit



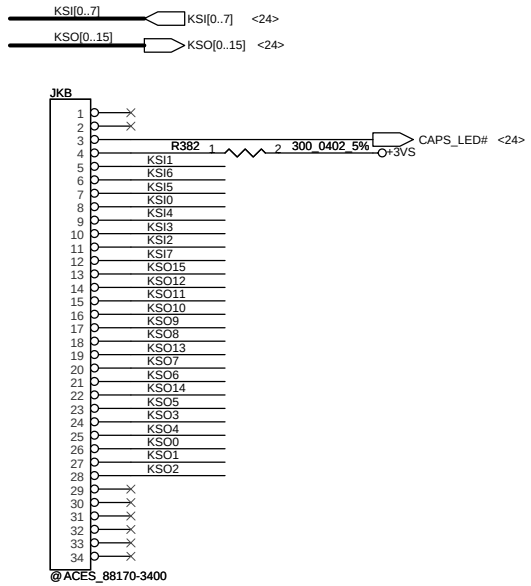
#DVT Reserve for EC protect

SPI Flash (8Mb*1)

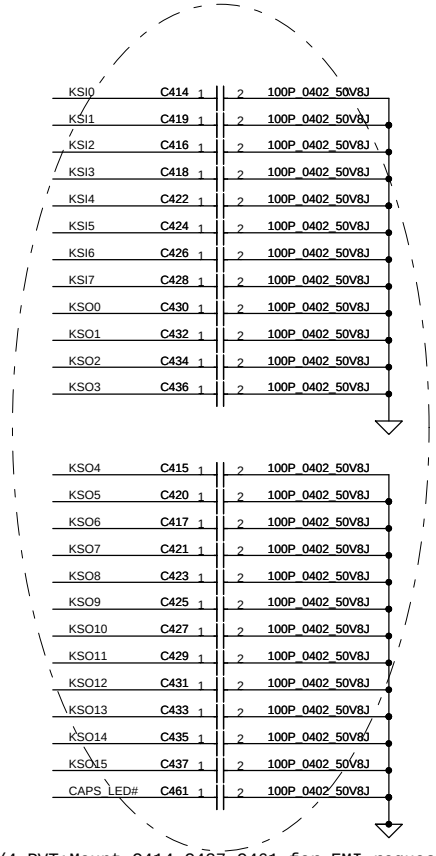


LPC Debug Port

KEYBOARD CONN.



12/18 Follow KB Matrix the same to KSKAA



3/4 PVT:Mount C414~C437,C461 for EMI request

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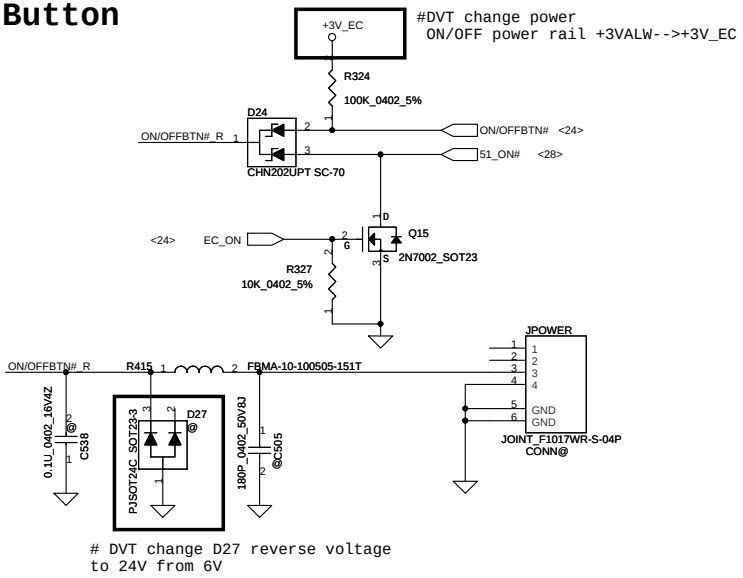
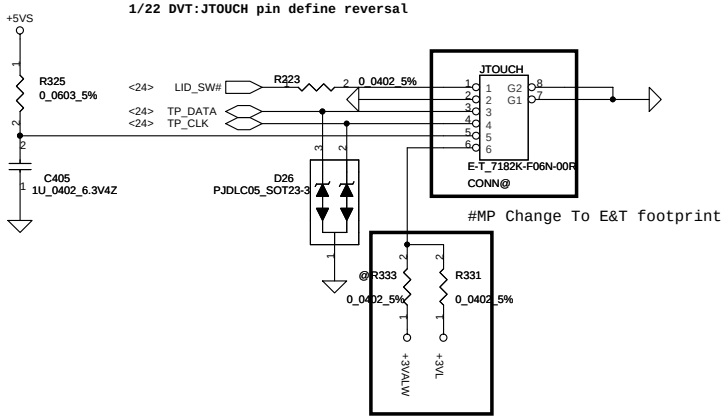
Power Button



DVT change D27 reverse voltage to 24V from 6V

Touch/B Connector

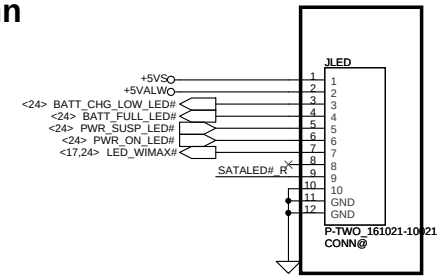
1/22 DVT:JTOUCH pin define reversal



#MP Change To E&T footprint

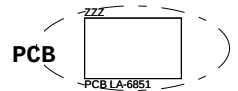
MP change LID power to +3VL

LED Conn



PVT change non ZIF for cost

ISPD



4/7 MP:PCB P/N Change to DAZ08100105

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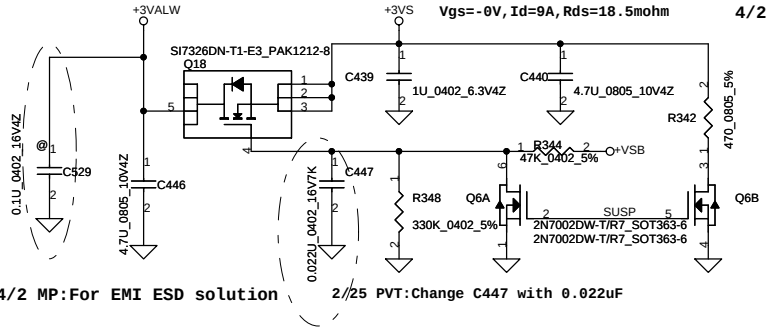
+3VALW TO +3VS



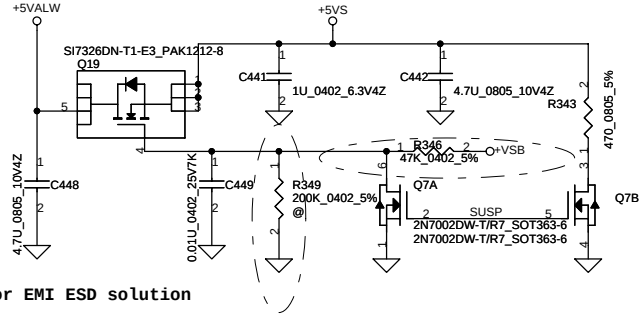
4/2 MP:For EMI ESD solution

4/2 MP:For EMI ESD solution

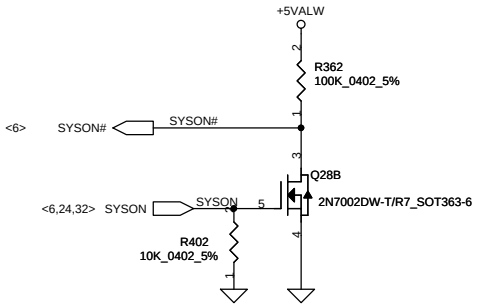
2/25 PVT:Change C447 with 0.022uF

+5VALW TO +5VS

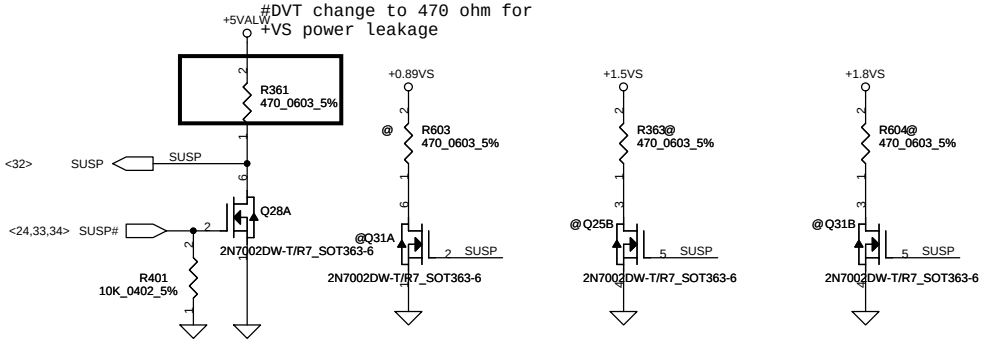
4/2 MP:For EMI ESD solution



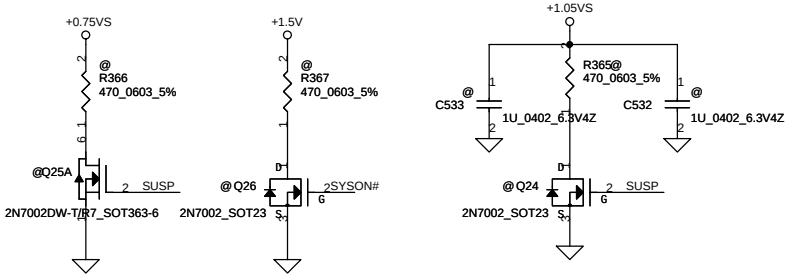
3/23 For EMI ESD solution



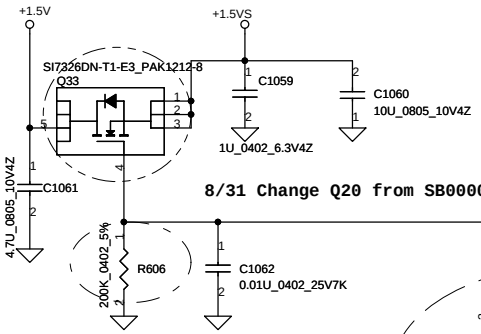
#DVT change to 470 ohm for +VS power leakage



2/6 DVT: Reserve +1.5VS,+1.05VS,+0.75VS,+1.8VS discharge circuit



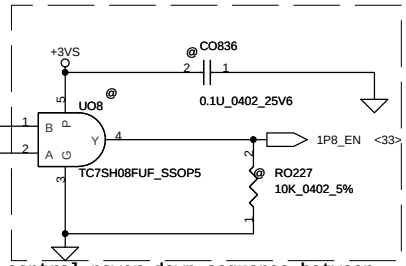
+1.5V TO +1.5VS



8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

8/14 R237 for HW design

7/9 Add Q29, Q30, R228 for Intel power sequence



reserve UO8 to control power down sequence between 1.8vs and 1.05vs,01/08,2010

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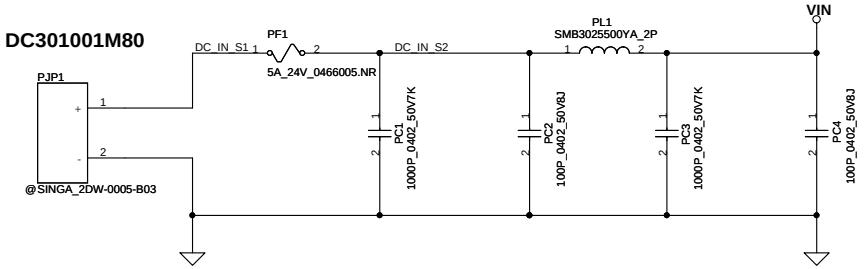
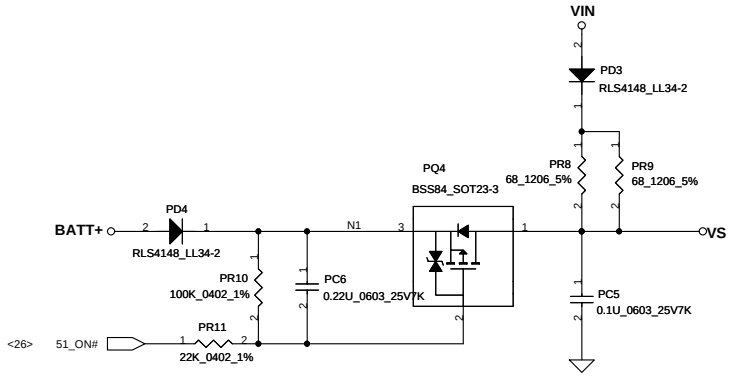
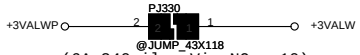
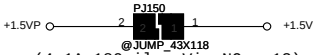






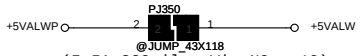
(6A,240mils ,Via NO.= 10)

(OCP min=8A)



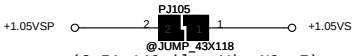
(4.1A,180mils ,Via NO.= 12)

(OCP min=6.03A)

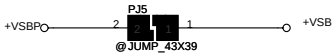


(5.5A,220mils ,Via NO.= 10)

(OCP min=7.8A)

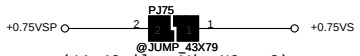


(3.5A,140mils ,Via NO.=7)



(120mA,40mils ,Via NO.= 1)

(3A,120mils ,Via NO.= 1)



(1A,40mils ,Via NO.= 3)

(2.6A,120mils ,Via NO.=6)

(100mA,40mils ,Via NO.= 2)

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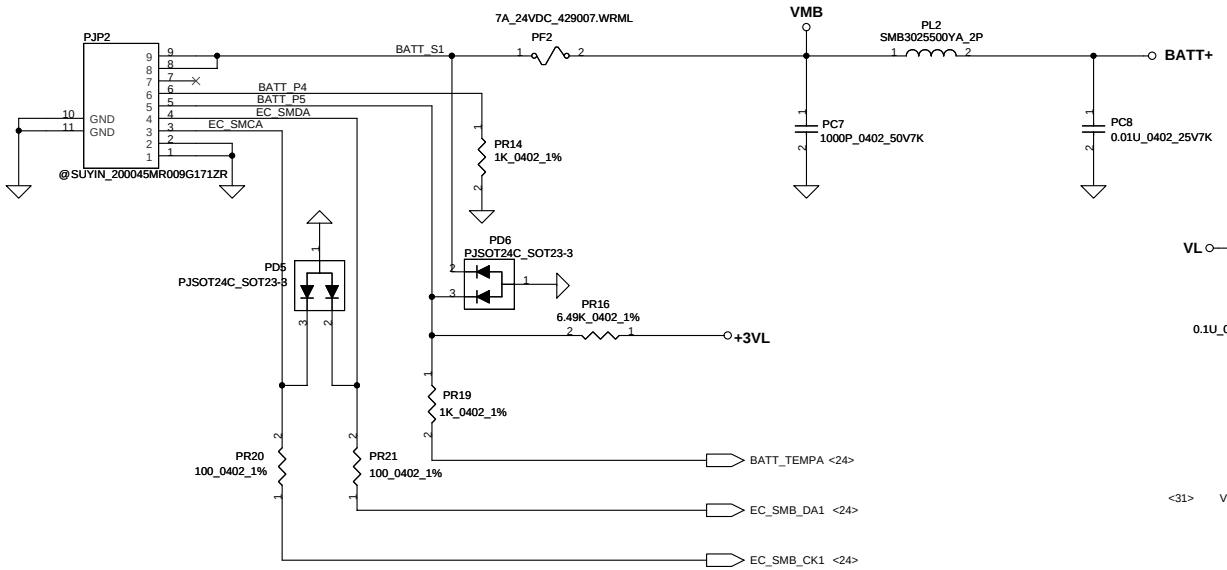
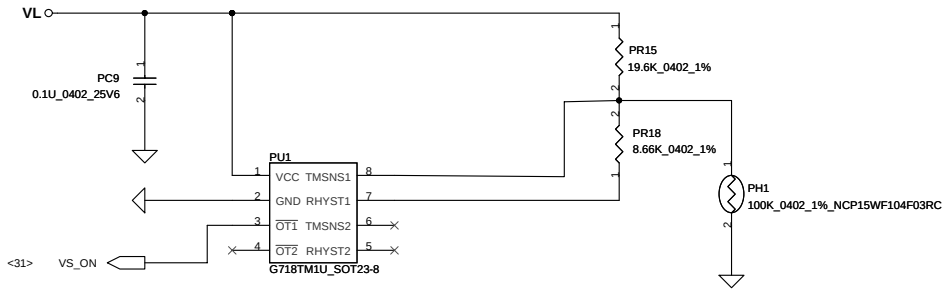
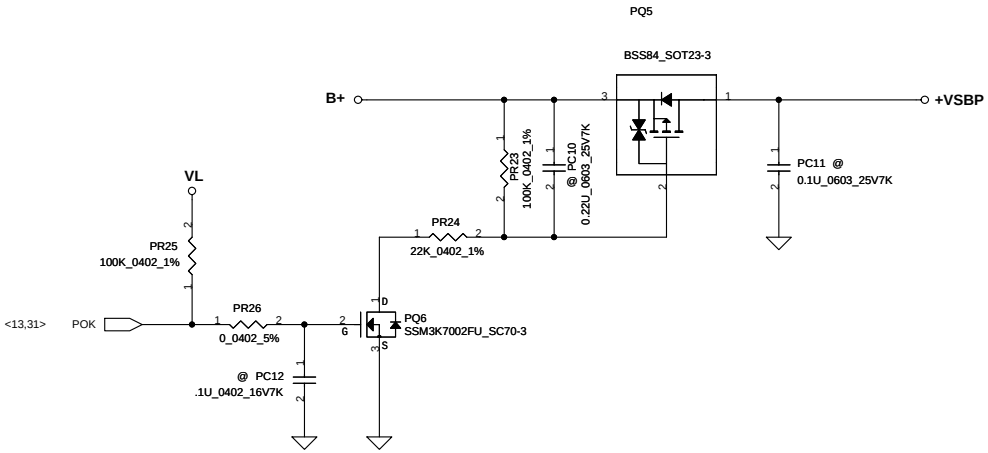


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2009/04/28

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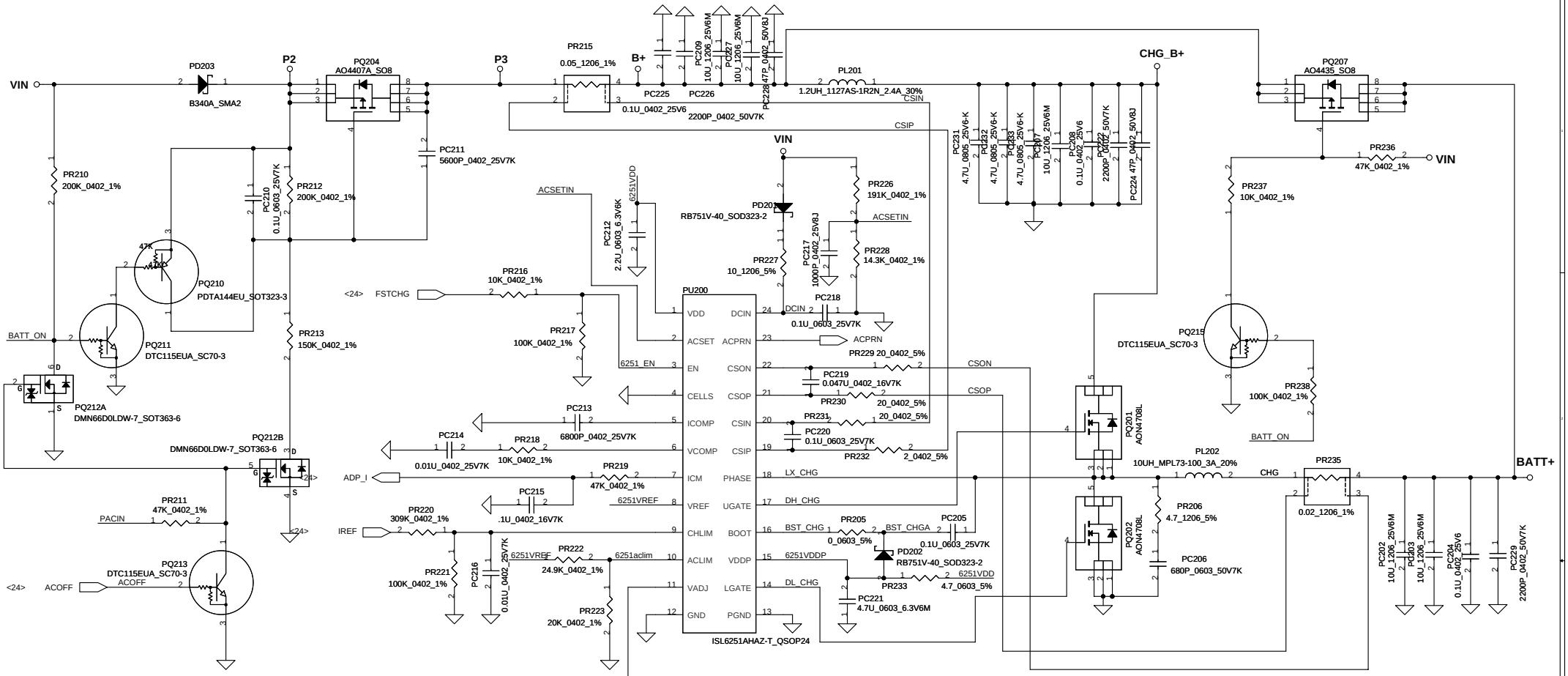

CP mode

Iada=0~1.579A(30W) CP= 92%*Iada; CP=1.45A

Vaclim=1.08132V(30W) PR70=53.6k PR216=0.05

CC=0.25A~2A
IREF=1.636*Icharge
IREF=0.409V~3.272V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.455

Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.309V

Ki
Vchlim=Iref*(PR221/(PR220+PR221))
=Iref*(100K/(309K+100K))
=Iref*0.2444
Ichanrge=(165mV/PR235)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=0.611*Iref
Iref=1.636*Ichanrge =>Ki=1.636

Kv
Rinternal ic=514K Rec=3K R1=PR224=15.4K R2=PR225=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.455

Vin Detector

High 18.089V
Low 17.44V

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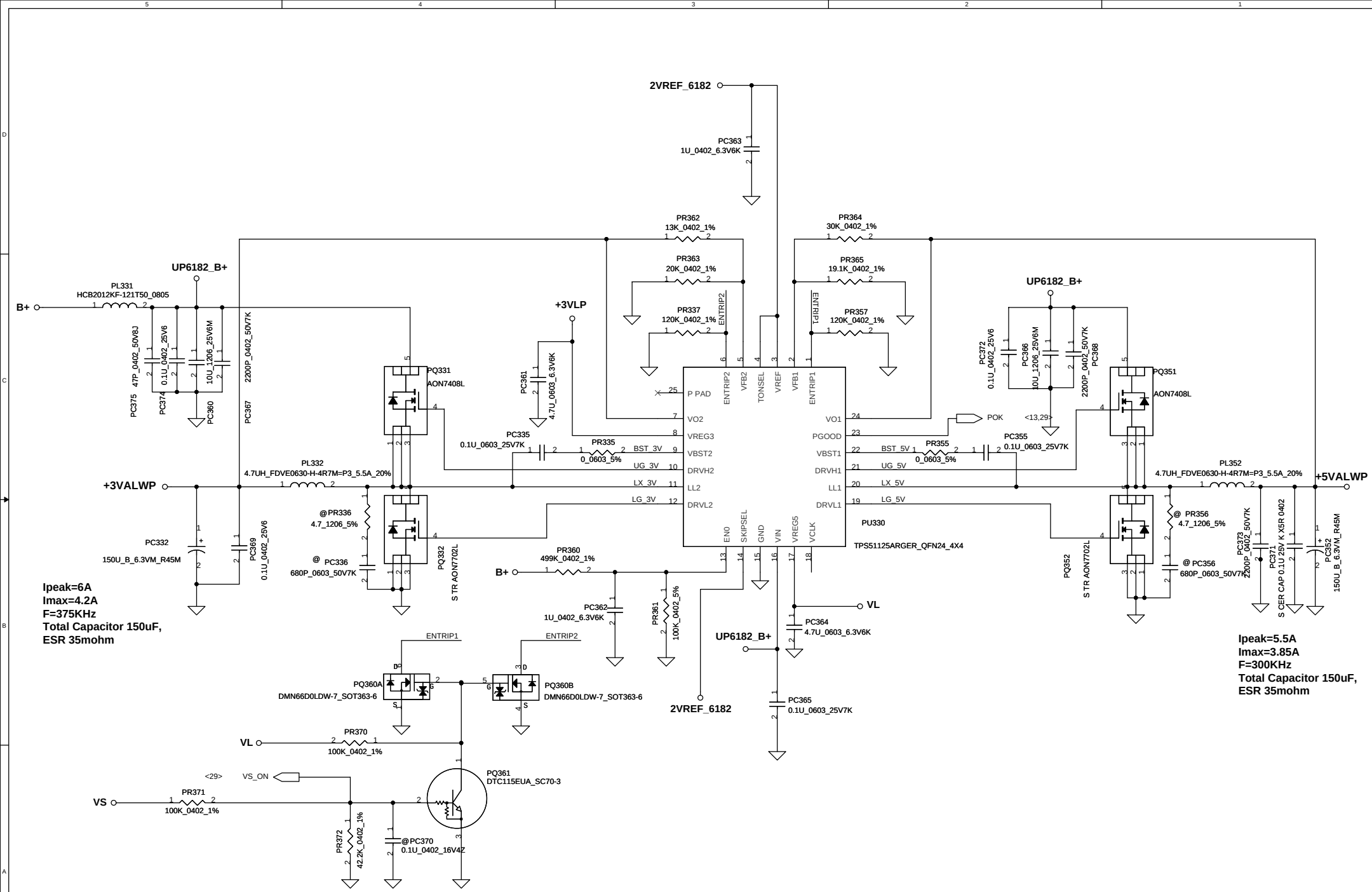

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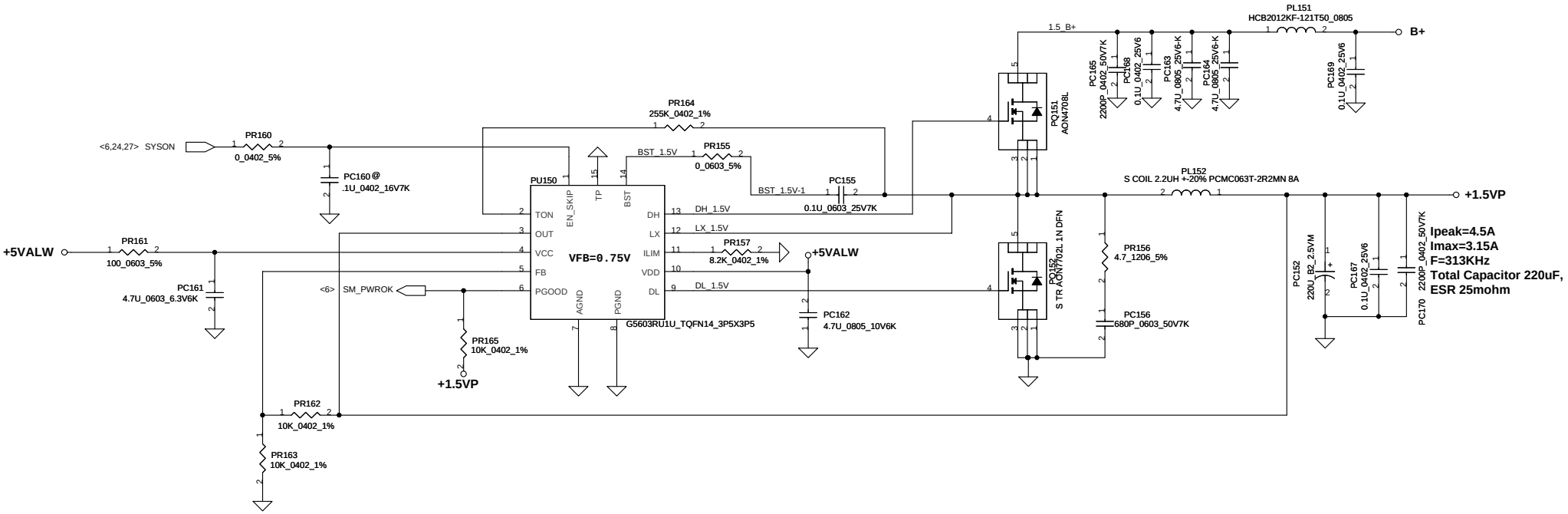

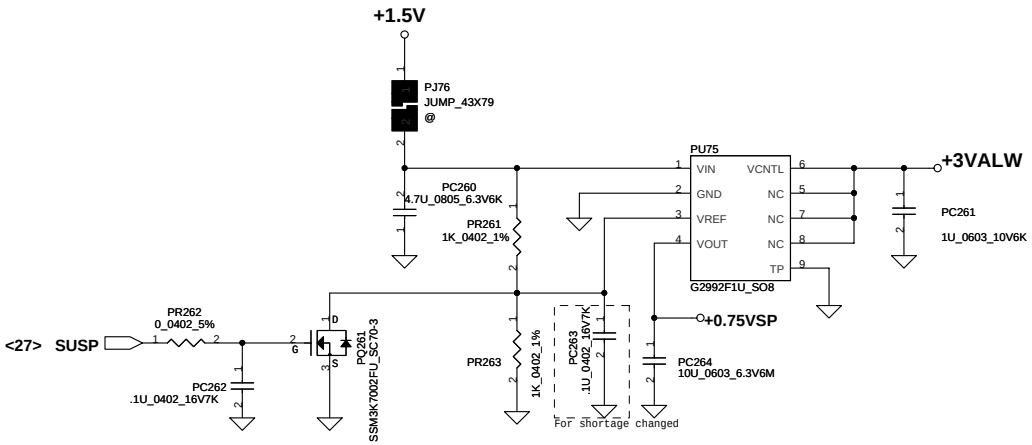

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

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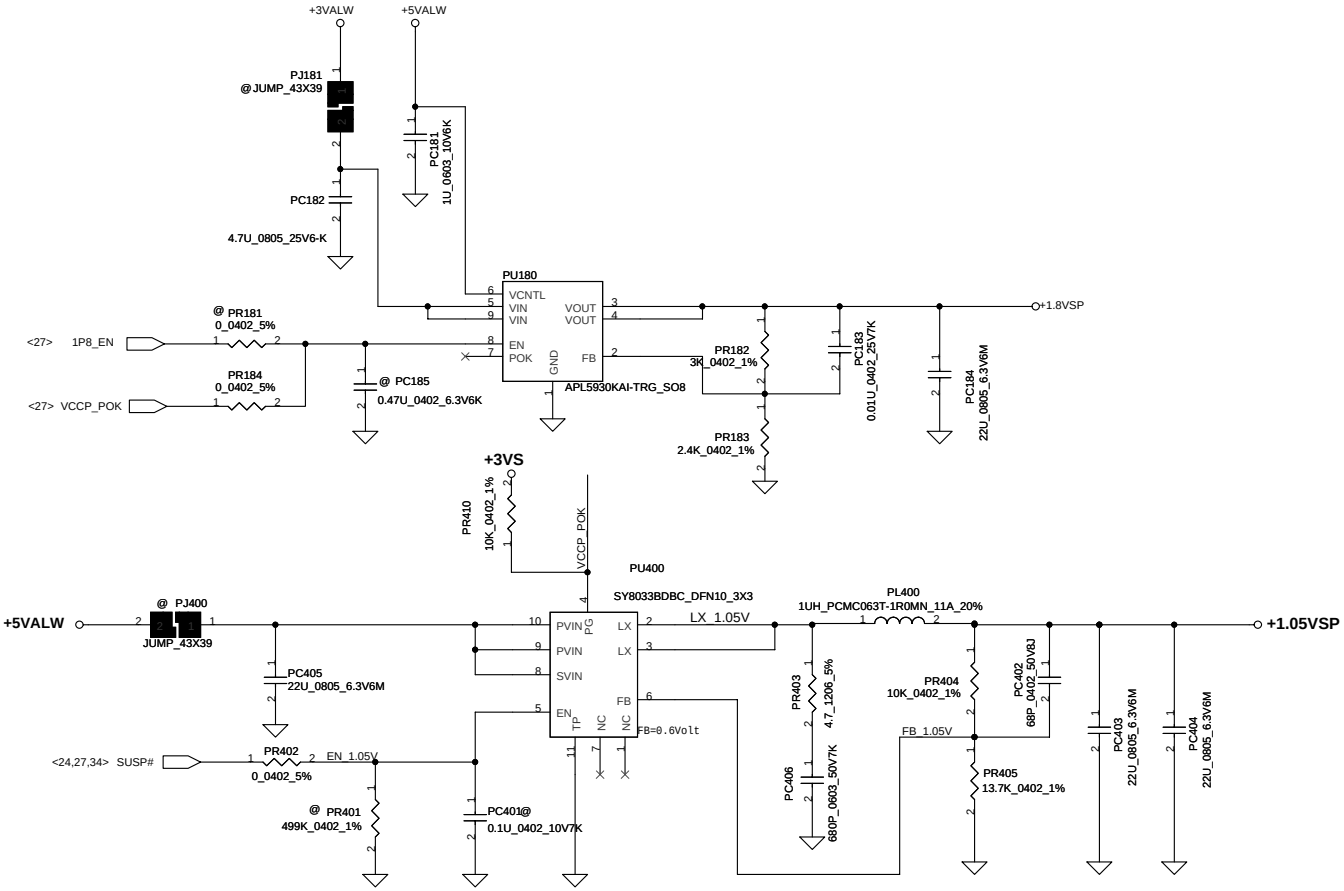

Ipeak=3.5A
ILIM = 2.45A
F=1MHz
Total Capacitor66uF,

Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,
SY8035 is for 5A loading , let LX shape can bigger!!

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Issued Date	2010/01/25	Deciphered Date	2009/04/28

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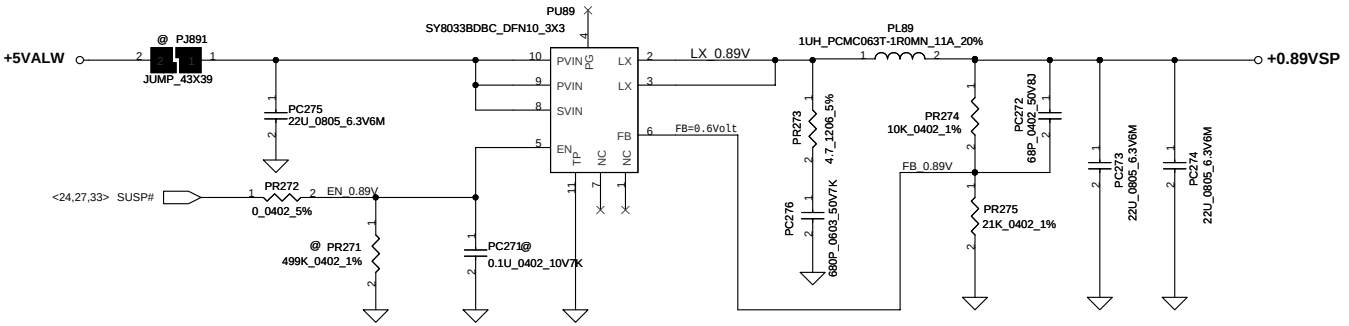

Ipeak=3A
ILIM = 2.1A
F=1MHz
Total Capacitor 330uF,
ESR 9mohm

Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,
SY8035 is for 5A loading , let LX shape can bigger!!

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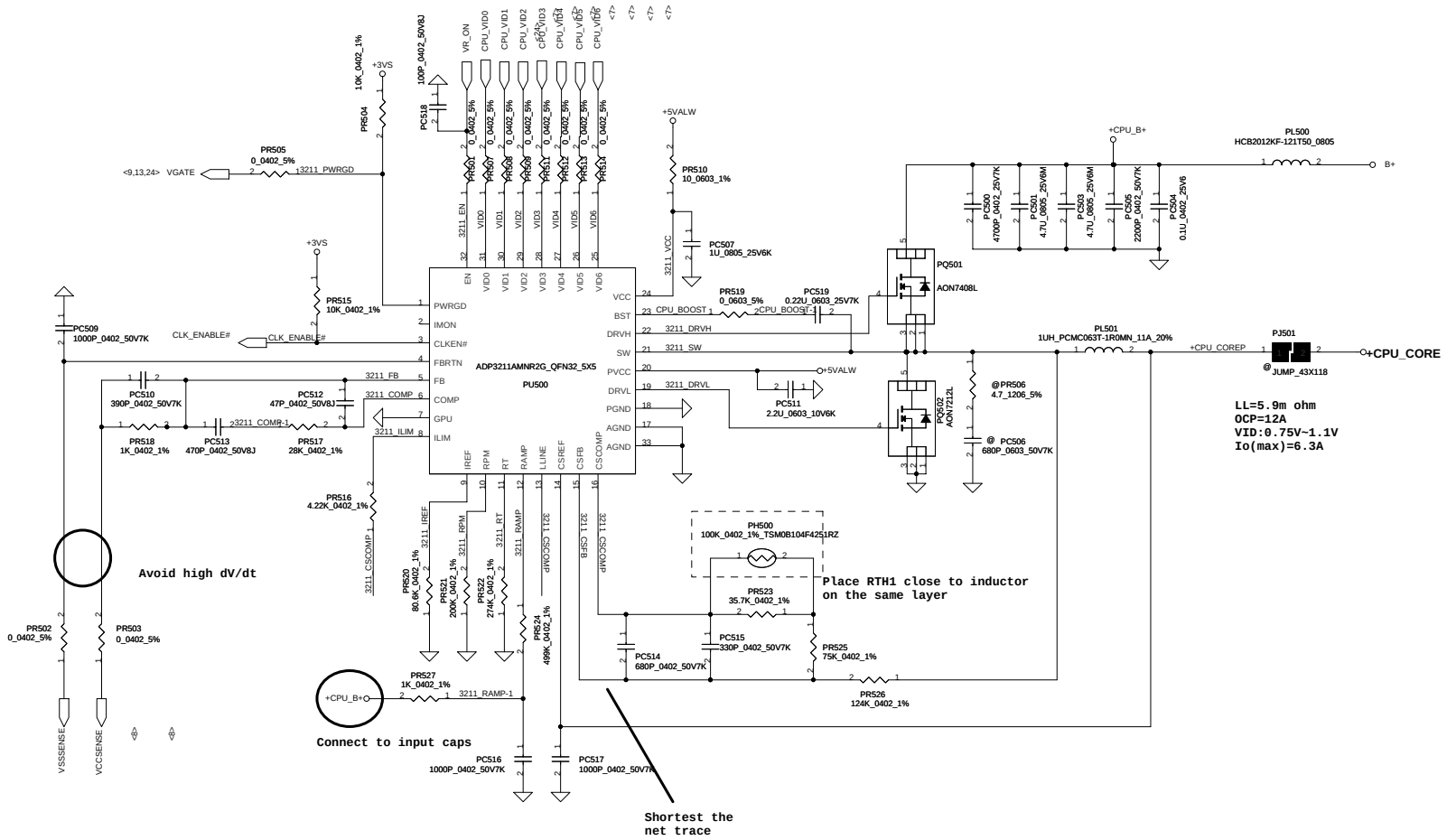

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2010/8/23(DVT)	P32 +1.5VP/+0.75VSP	Change PU75 UP7711(SA00003XI00) -->G2992(SA00000VE80)	UPI had patent issue
	2010/8/23(DVT)	P30 Charger	Change PU200 G5209(SA00003TK00)-->ISL6251(SA00001EP80)	G5209 had leakage issue
	2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Change PU330 UP6182(SA000043H00) -->TI51125A(SA000020C80)	UPI had patent issue
	2010/8/23(DVT)	P30 Charger	add PR247(SD034100280) PC223(SE076104K80) PR246(SD034309380) PR248(SD034470280)	Support SA ECO unit
	2010/8/23(DVT)	P35 CPU_CORE	Change PR526 174K (SD034174380) -->124K(SD034124380)	debug CPU load issue
	2010/8/23(DVT)	All snuber	Change PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000008L80) -->PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000000I10)	Chose the same material s
	2010/8/23(DVT)	P30 Charger	Install PC222 PC224 0.1u (SE00000G880)	EMI commond
	2010/8/23(DVT)	P30 Charger	Install PC227,PC209,PC207,PC208,PC204 10u (SE142106M80)	EMI commond
	2010/8/23(DVT)	P35 CPU_CORE	Change PL500(SM01000BY00)-->(SM01000C000)	Chose the same material s
	2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC371,PC369 0.1u (SE00000G880)	RF commond
	2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC367 2200P(SE074222K80)	RF commond
	2010/8/23(DVT)	P32 +1.5VP	Install PC165 2200P(SE074222K80)	RF commond
	2010/8/23(DVT)	P32 +1.5VP	Install PC169,PC168,PC167 0.1u(SE00000G880)	RF commond
	2010/8/23(DVT)	P35 CPU_CORE	add PC518 (SE071101J80)	debug CPU VR-ON issue
	2010/9/21(PVT)	P30 Charger	Install PC225 PC208PC204 (0.1u) , PC226 PC222 PC229(2200P) Add PC208 add PC228 PC224 (47P),install snubber PR206,PC206	RF commond
	2010/9/21(PVT)	P31 +5VALWP/+3VALWP	Add PC372 PC374(0.1u) , PC375(47P) PC371 (2200P)	RF commond
	2010/9/21(PVT)	P32 +1.5VP	Add PC170(2200P) install snubber PR156 PC156	RF commond
	2010/10/8(pre-MP)	P30 Charger	Change PL210 to 1.2u (SH00000B100)	EMI commond
	2010/10/08(Pre-MP)	P31 +5VALWP/+3VALWP	Change PC332 & PC352 to ESR 45 m ohm	cost down plane
	2010/10/08(Pre-MP)	P32 +1.5VP	Change PC152 to ESR 35 m ohm	cost down plane

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