

PWWAA

Marseille LC

L-A6841P REV 0.1 Schematic

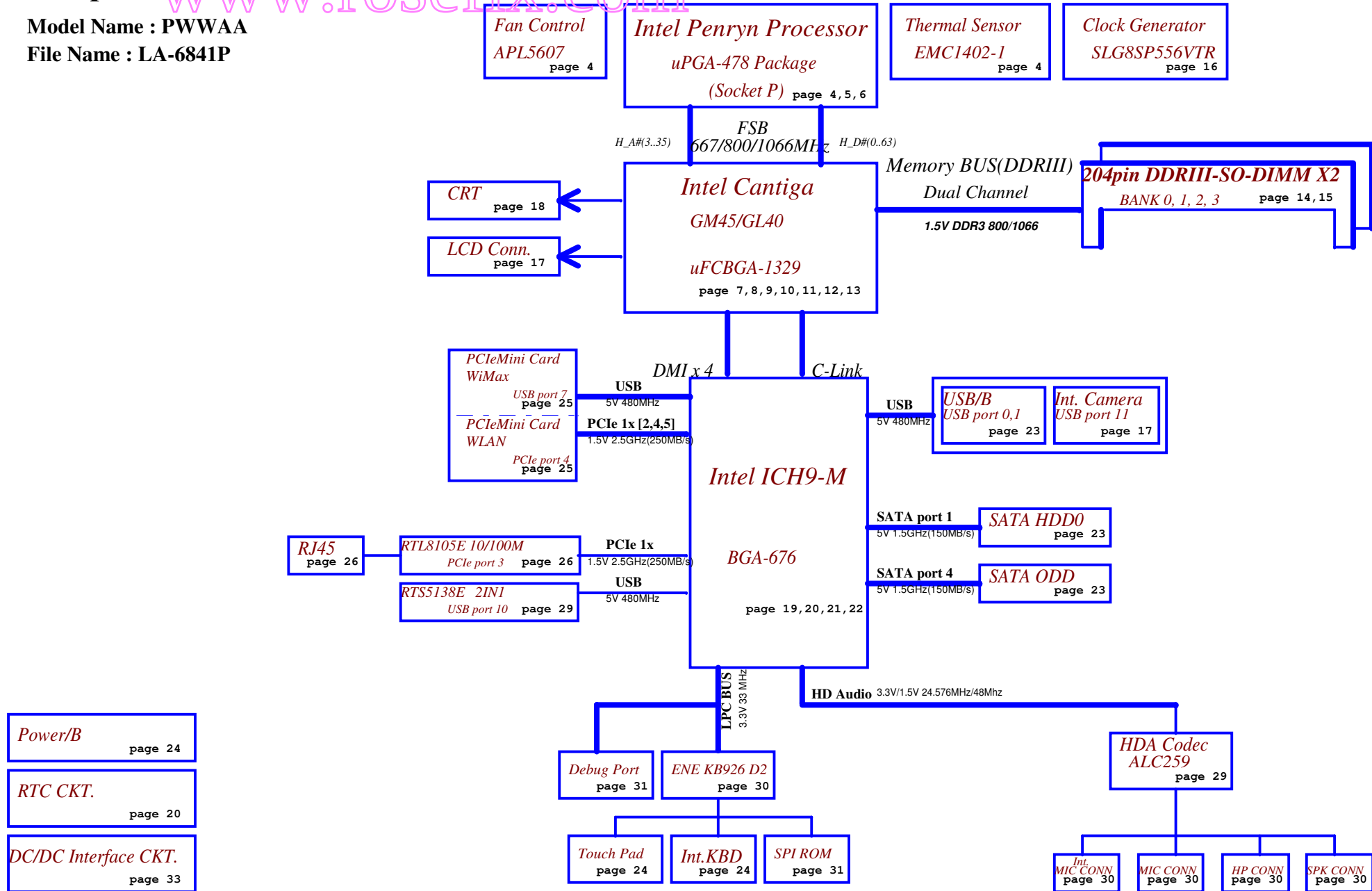
Intel Penryn/ Cantiga/ ICH9M
2010-07-22 Rev. 0.1

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Compal Confidential

Model Name : PWWAA

File Name : LA-6841P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5 power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8V power rail	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for SB	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	Card Reader	Camera	WLAN	Energy Star
description		(X)	Always	Always
explain		Camera	WLAN	Energy Star
BTO		CAM@	WLAN@	

External PCI Devices

DEVICE	PCI DEVICE ID	IDSEL#	REQ/GNT#	PIRQ
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EC SM Bus1 address

EC SM Bus2 address

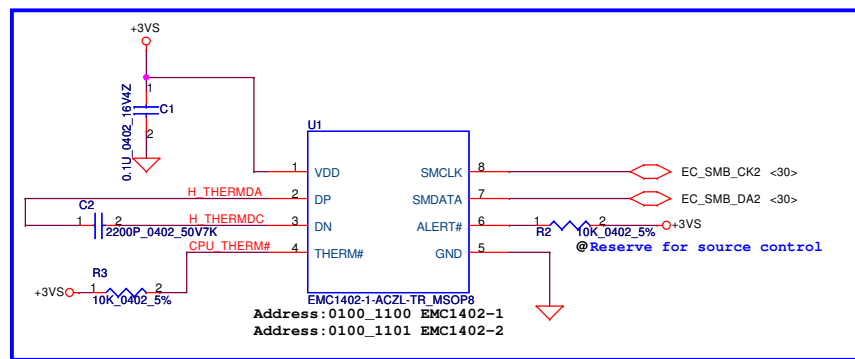
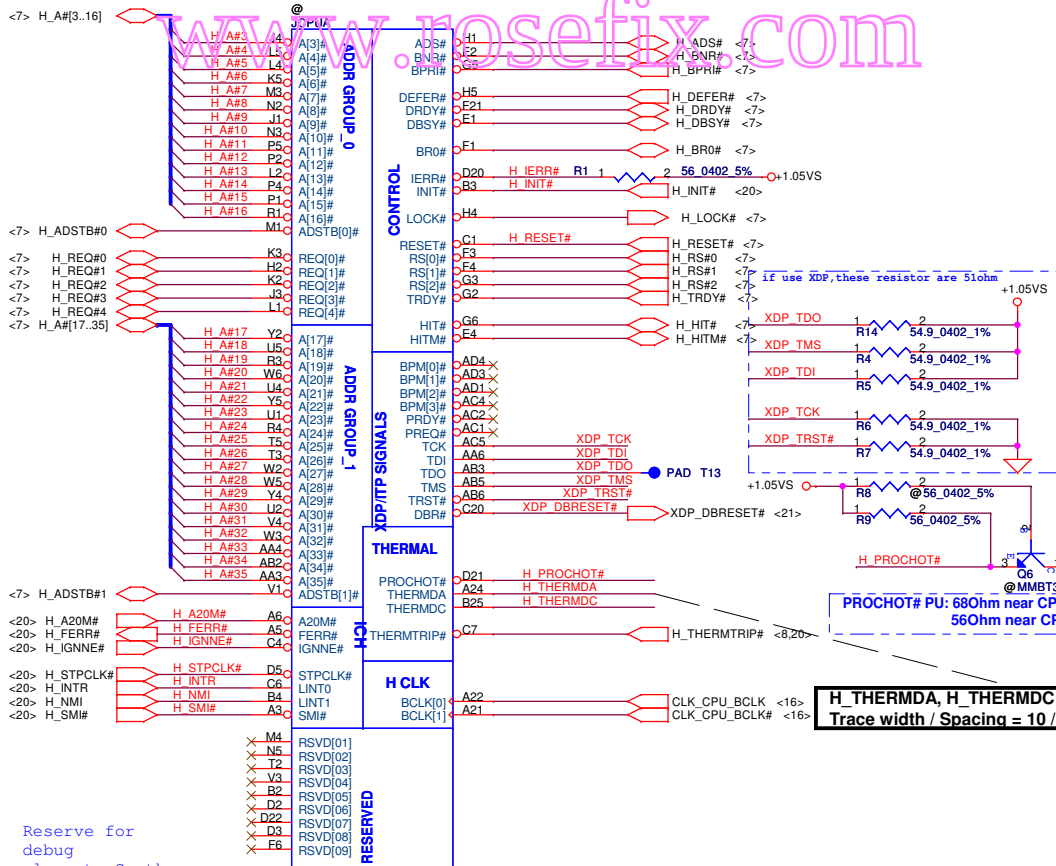
Power	Device	Address	Power	Device	Address
+3VL	EC KB926 D2		+3VS	EC KB926 D2	
+3VL	Smart Battery	0001 011X b	+3VS	CPU THM Sen	1001 101Xb
				SMSC SMC1402	

ICH9M SM Bus address

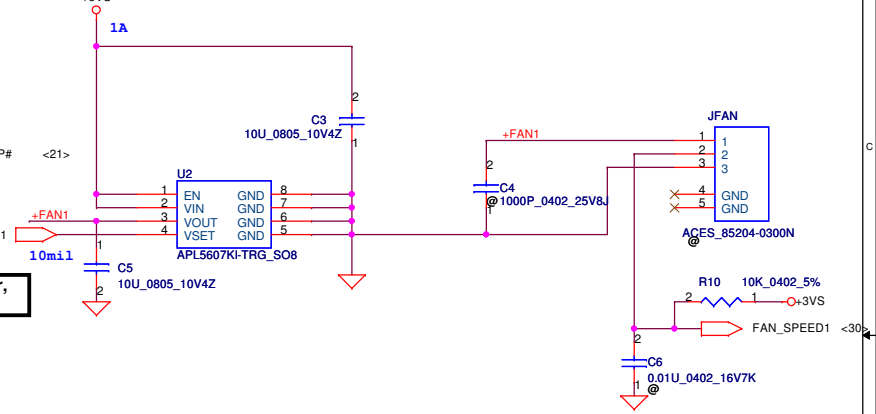
Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb

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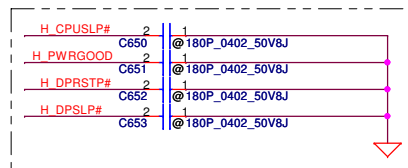


FAN Control Circuit



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

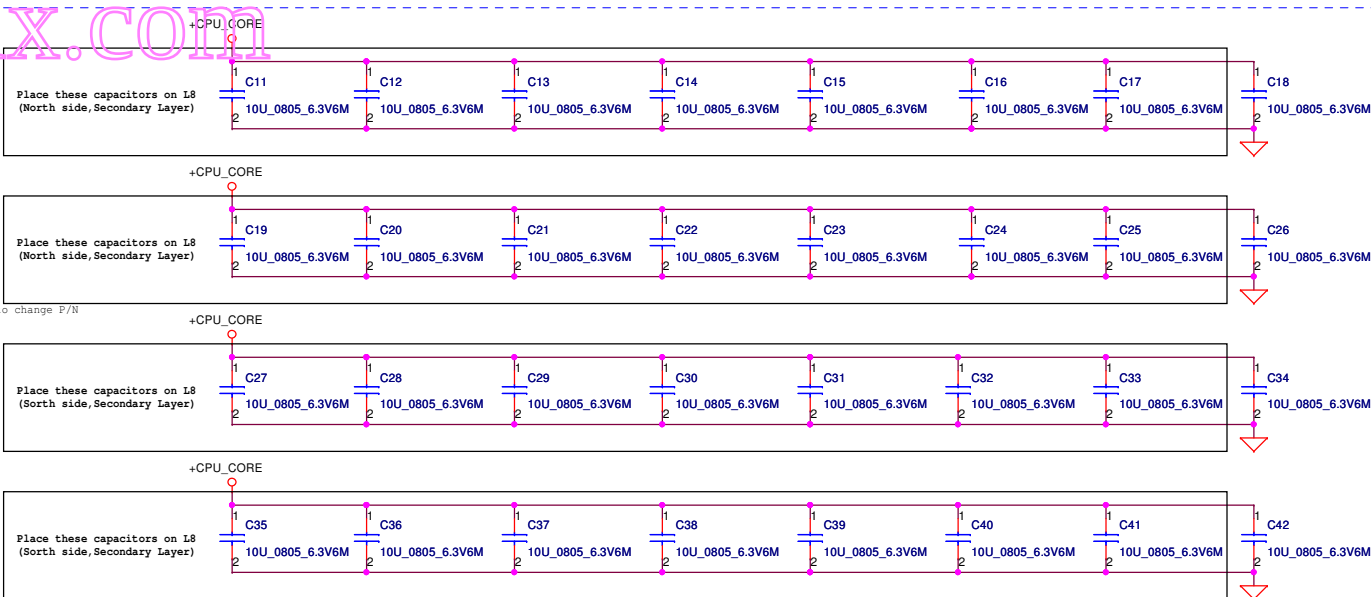
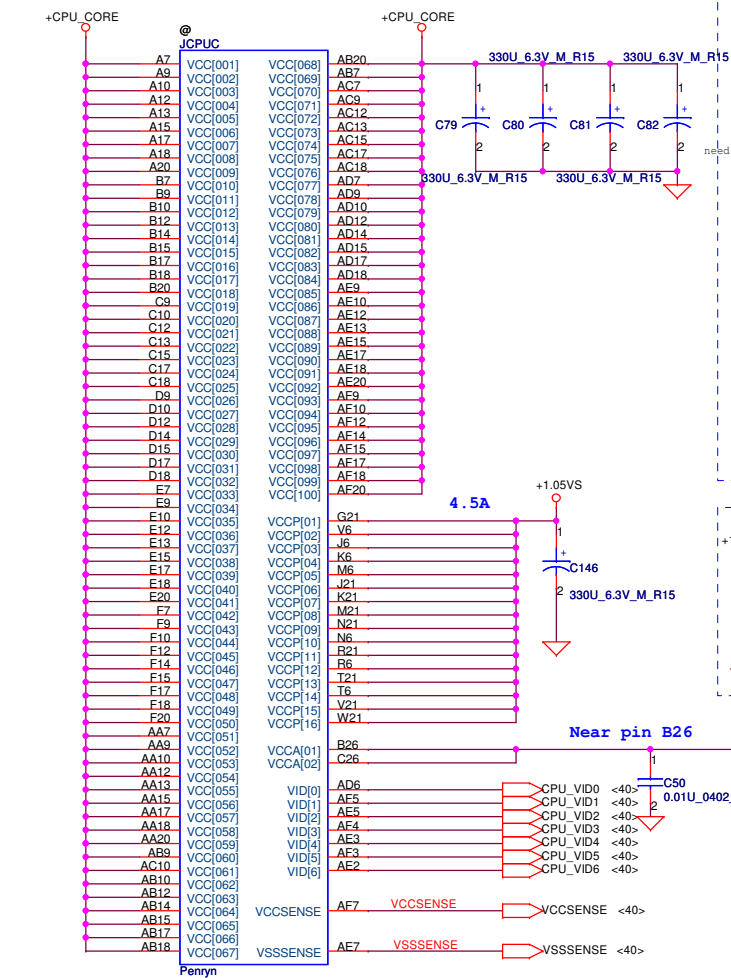
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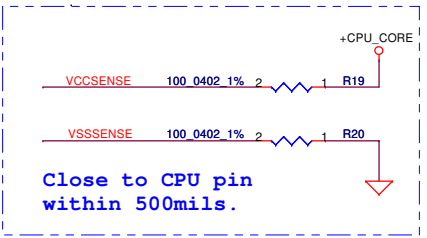
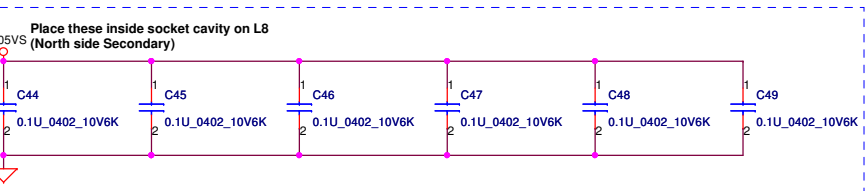
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Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

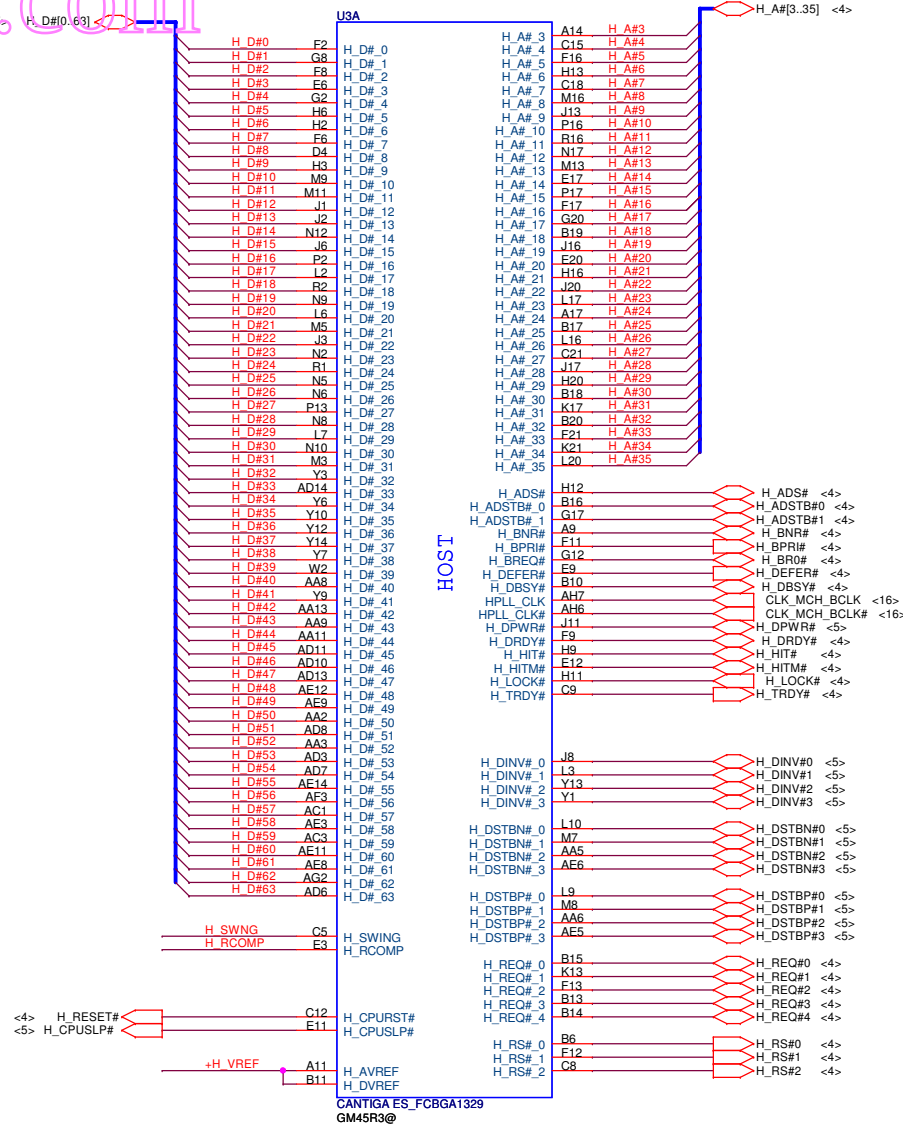
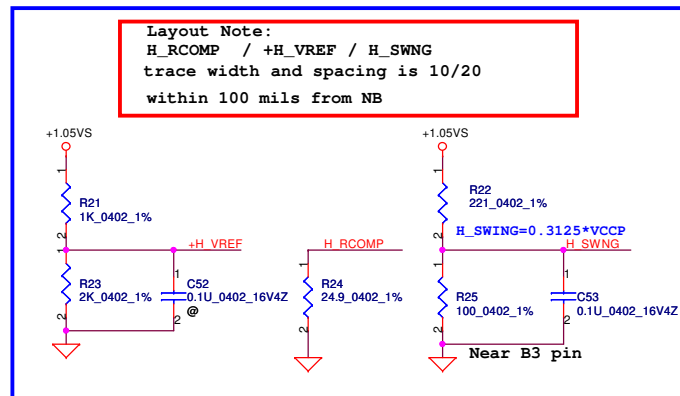


Mid Frequency Decoupling



Length match within 25 mils.
The trace width/space/other is 14/7/25.

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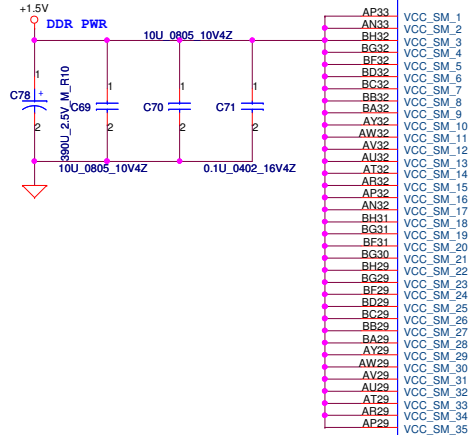


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DDR2, 657mA, 2680mA
DDR2, 870mA, 3000mA

+1.05VS
Int. Graphic

Extnal Graphic: 1210.34mA
Integrated Graphic: 1930.4mA
Intel Management Engine Link:508.12mA



BA36 VCC_SM_36/NC
BB24 VCC_SM_37/NC
BD16 VCC_SM_38/NC
BB21 VCC_SM_39/NC
AW16 VCC_SM_40/NC
AW13 VCC_SM_41/NC
AT13 VCC_SM_42/NC

8700mA

Y26 VCC_AXG_1
AE25 VCC_AXG_2
AB25 VCC_AXG_3
AA25 VCC_AXG_4
AE24 VCC_AXG_5
AC24 VCC_AXG_6
AA24 VCC_AXG_7
Y24 VCC_AXG_8
AE23 VCC_AXG_9
AB23 VCC_AXG_10
AA23 VCC_AXG_11
AJ21 VCC_AXG_12
AG21 VCC_AXG_13
AE21 VCC_AXG_14
AC21 VCC_AXG_15
AA21 VCC_AXG_16
Y21 VCC_AXG_17
AH20 VCC_AXG_18
AF20 VCC_AXG_19
AE20 VCC_AXG_20
AC20 VCC_AXG_21
AB20 VCC_AXG_22
AA20 VCC_AXG_23
TI17 VCC_AXG_24
TI16 VCC_AXG_25
AM15 VCC_AXG_26
AL15 VCC_AXG_27
AE15 VCC_AXG_28
AH15 VCC_AXG_29
AG15 VCC_AXG_30
AF15 VCC_AXG_31
AB15 VCC_AXG_32
AA15 VCC_AXG_33
Y15 VCC_AXG_34
V15 VCC_AXG_35
U15 VCC_AXG_36
AN14 VCC_AXG_37
AM14 VCC_AXG_38
U14 VCC_AXG_39
TI14 VCC_AXG_40
VCC_AXG_41
VCC_AXG_42

PAD T3 AJ14 VCC_AXG_SENSE
PAD T4 AH14 VSS_AXG_SENSE

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GM45R3@

VCC_AXG_NCTF_1 W28
VCC_AXG_NCTF_2 W28
VCC_AXG_NCTF_3 W26
VCC_AXG_NCTF_4 W26
VCC_AXG_NCTF_5 W25
VCC_AXG_NCTF_6 W25
VCC_AXG_NCTF_7 W24
VCC_AXG_NCTF_8 W23
VCC_AXG_NCTF_9 W23
VCC_AXG_NCTF_10 W23
VCC_AXG_NCTF_11 AL21
VCC_AXG_NCTF_12 AK21
VCC_AXG_NCTF_13 W21
VCC_AXG_NCTF_14 W21
VCC_AXG_NCTF_15 U21
VCC_AXG_NCTF_16 AM20
VCC_AXG_NCTF_17 AK20
VCC_AXG_NCTF_18 W20
VCC_AXG_NCTF_19 U20
VCC_AXG_NCTF_20 AM19
VCC_AXG_NCTF_21 AL19
VCC_AXG_NCTF_22 AH19
VCC_AXG_NCTF_23 AG19
VCC_AXG_NCTF_24 AF19
VCC_AXG_NCTF_25 AE19
VCC_AXG_NCTF_26 AB19
VCC_AXG_NCTF_27 AA19
VCC_AXG_NCTF_28 Y19
VCC_AXG_NCTF_29 W19
VCC_AXG_NCTF_30 V19
VCC_AXG_NCTF_31 U19
VCC_AXG_NCTF_32 AM17
VCC_AXG_NCTF_33 AK17
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WS_C3A

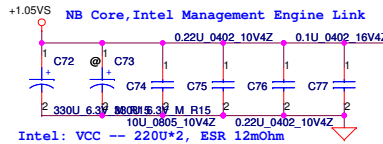
VCC GFX NCTF

POWER

VCC GFX

VCC SM LF

VCC_SM_LF1 AV44 VCCSM_LF1
VCC_SM_LF2 BA37 VCCSM_LF2
VCC_SM_LF3 AA40 VCCSM_LF3
VCC_SM_LF4 AV21 VCCSM_LF4
VCC_SM_LF5 AY5 VCCSM_LF5
VCC_SM_LF6 AM10 VCCSM_LF6
VCC_SM_LF7 BB13 VCCSM_LF7



AG34 VCC_1
AC34 VCC_2
AA34 VCC_3
Y34 VCC_4
V34 VCC_5
U34 VCC_6
AK33 VCC_7
AM33 VCC_8
AK33 VCC_9
AG33 VCC_10
AF33 VCC_11
VCC_12

AE33 VCC_13
AC33 VCC_14
AA33 VCC_15
Y33 VCC_16
W33 VCC_17
V33 VCC_18
U33 VCC_19
AH28 VCC_20
AF28 VCC_21
AC28 VCC_22
AA28 VCC_23
AJ28 VCC_24
AG26 VCC_25
AE26 VCC_26
AC26 VCC_27
AH25 VCC_28
AG25 VCC_29
AF25 VCC_30
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AJ23 VCC_32
AH23 VCC_33
AF23 VCC_34
T32 VCC_35

VCC CORE

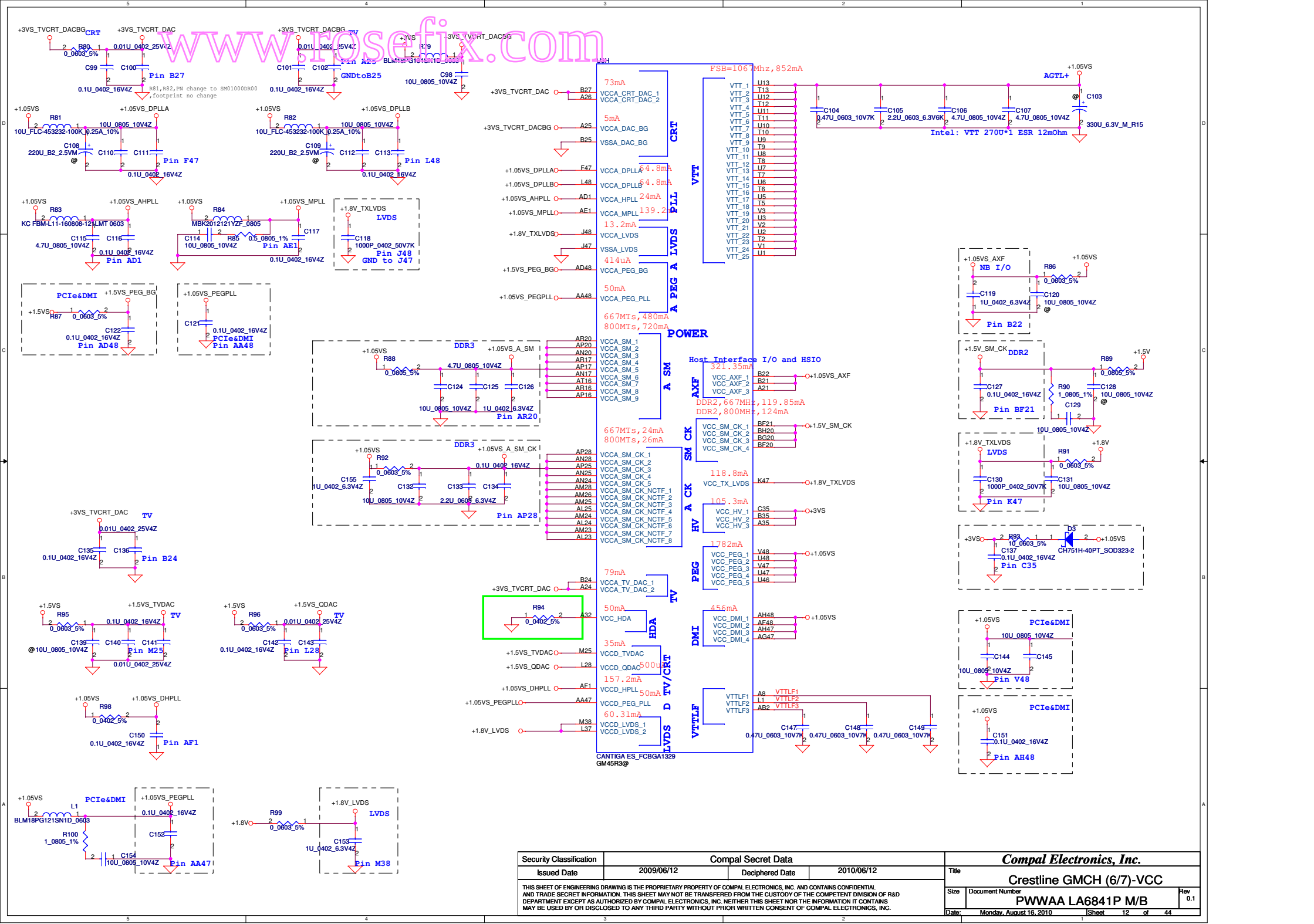
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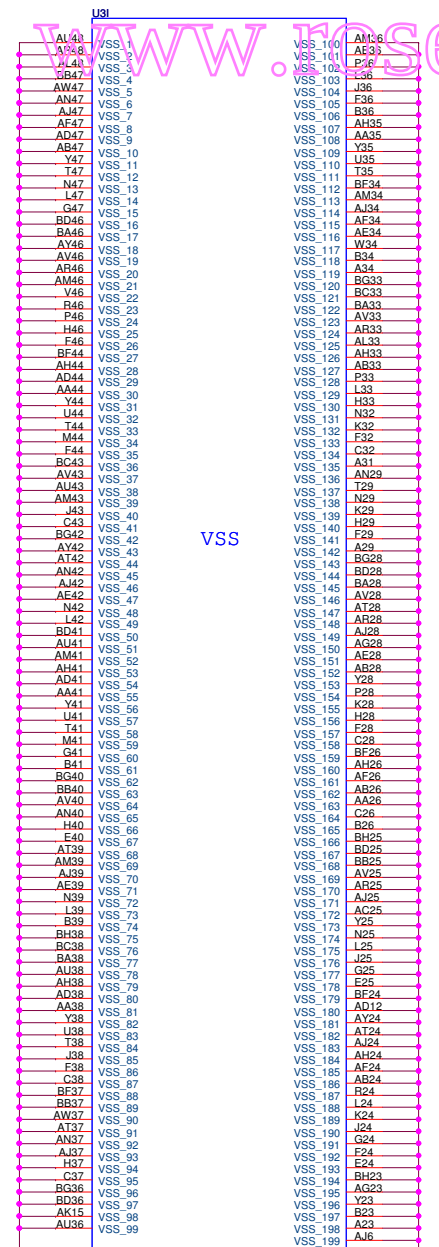
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VCC_NCTF_6 AE32
VCC_NCTF_7 AC32
VCC_NCTF_8 AA32
VCC_NCTF_9 Y32
VCC_NCTF_10 W32
VCC_NCTF_11 U32
VCC_NCTF_12 AM30
VCC_NCTF_13 AL30
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VCC_NCTF_26 AH29
VCC_NCTF_27 AE29
VCC_NCTF_28 AC29
VCC_NCTF_29 AA29
VCC_NCTF_30 Y29
VCC_NCTF_31 W29
VCC_NCTF_32 U29
VCC_NCTF_33 AM28
VCC_NCTF_34 AL28
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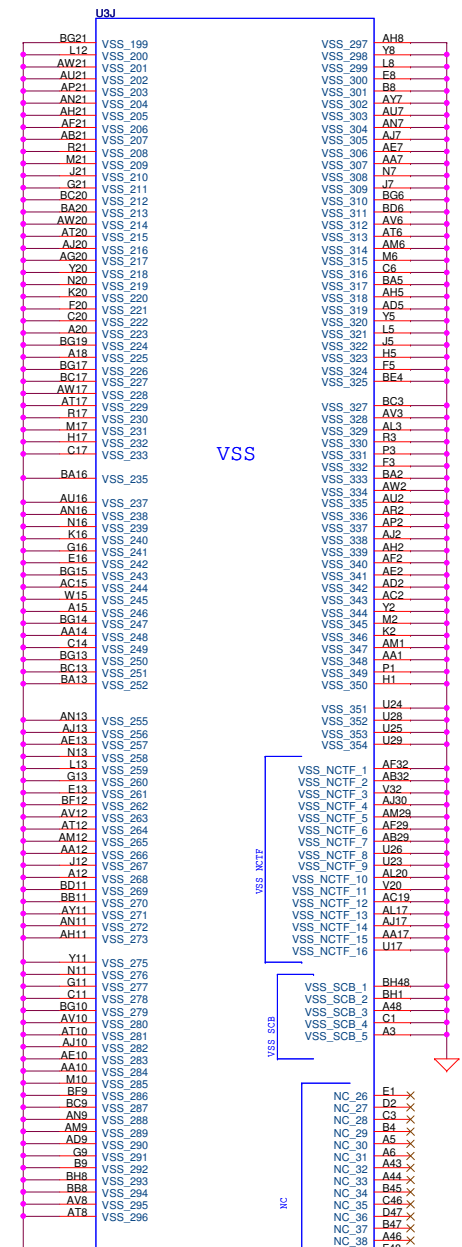
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GM45R3@

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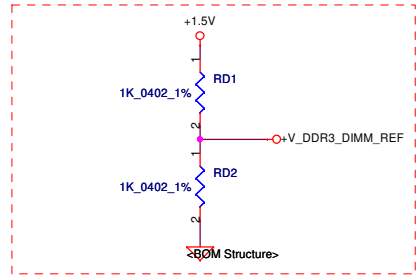
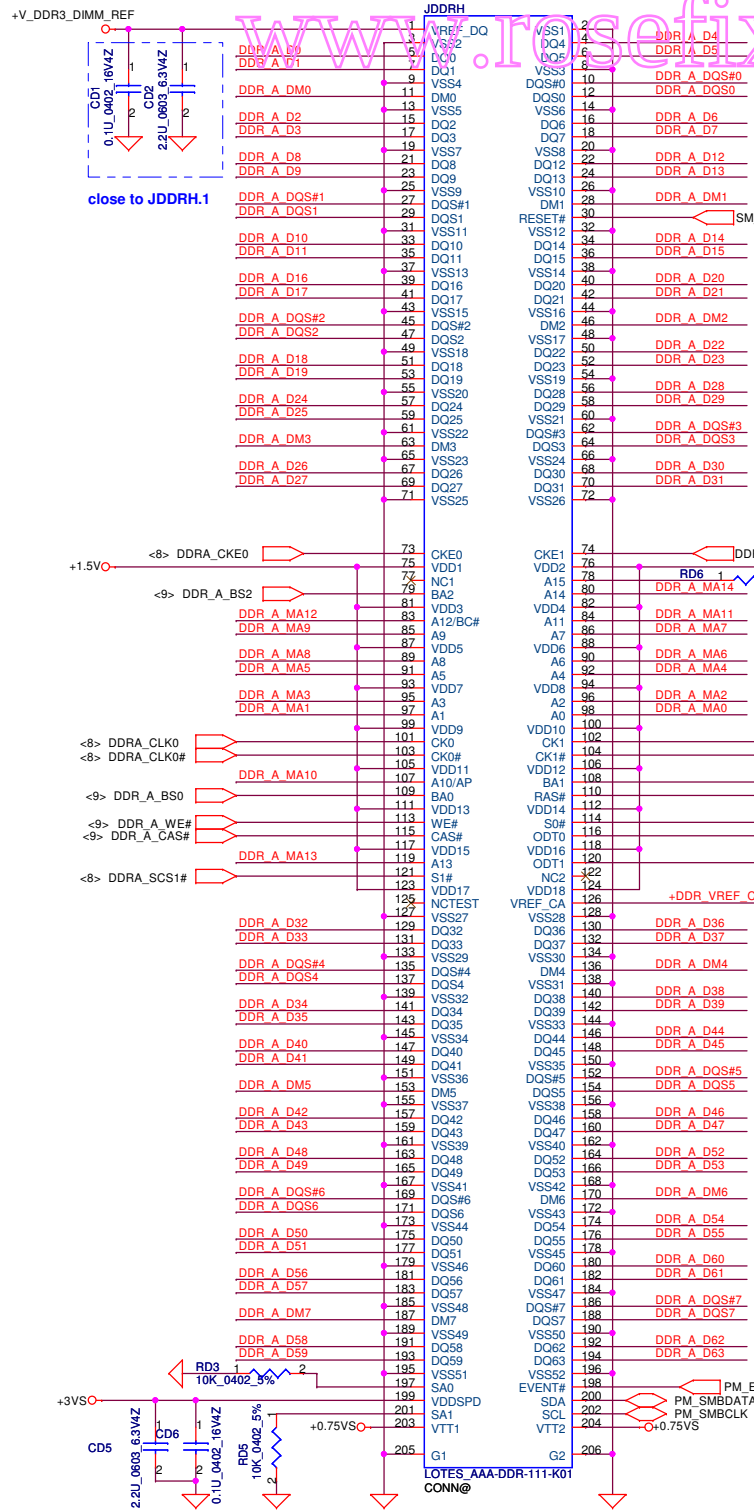


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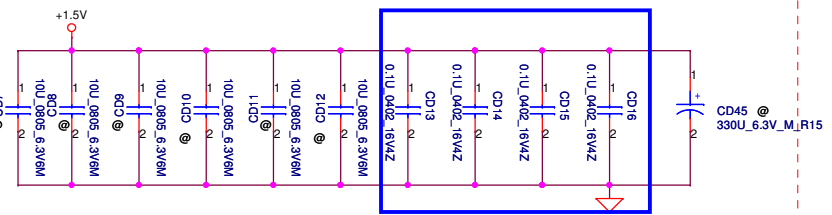
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DDR3 SO-DIMM A REVERSE TYPE

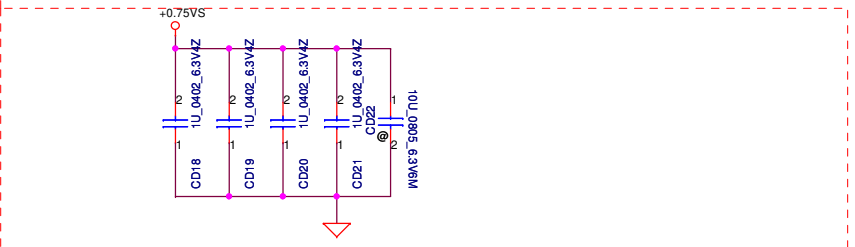


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Place near JDDRH

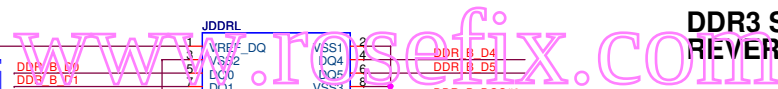
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



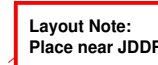
Layout Note:
Place near JDDRH.203 & JDDRH.204



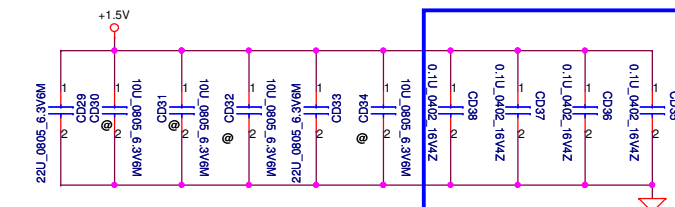
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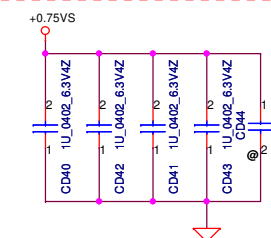
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Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



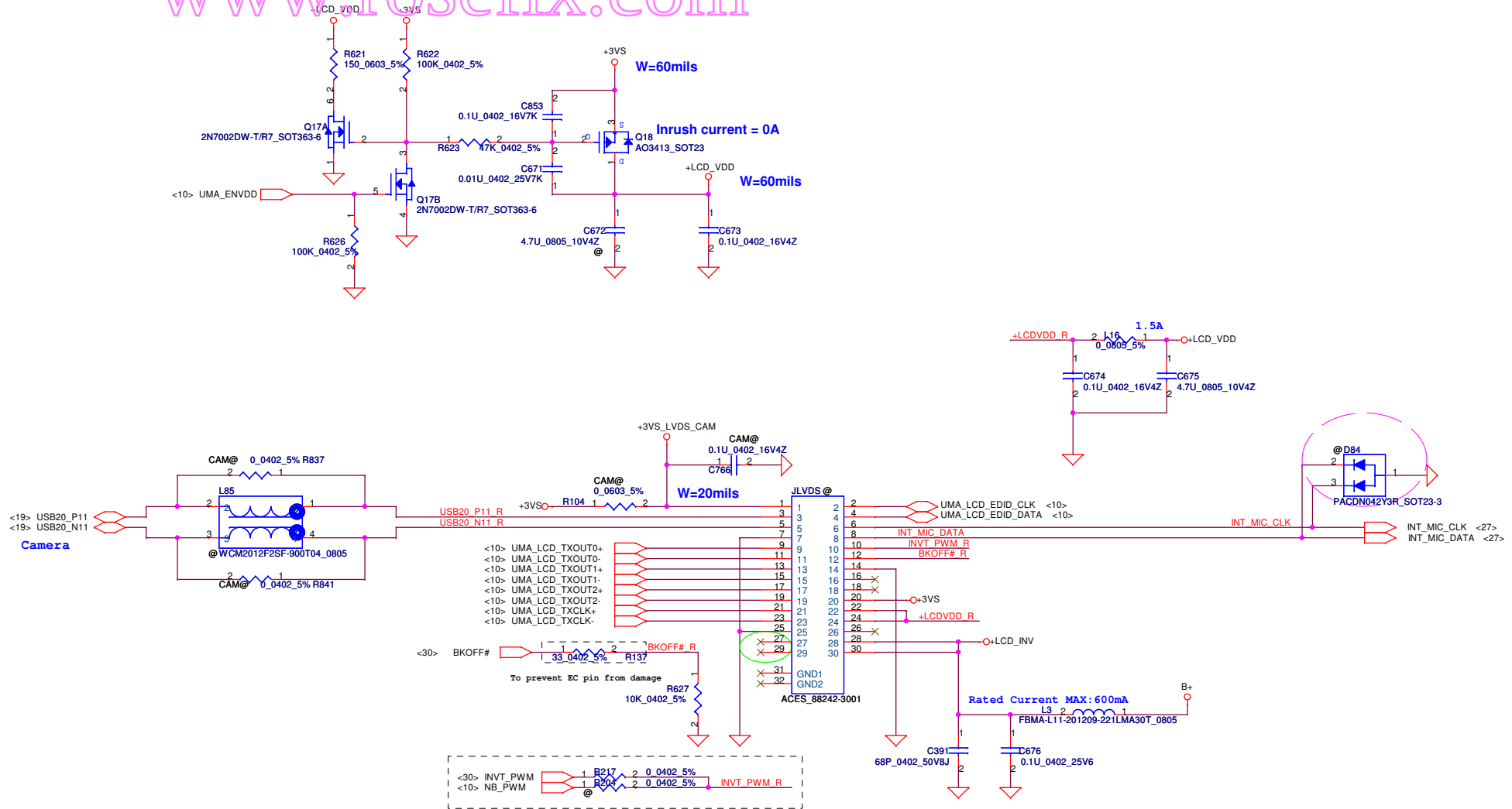
Layout Note:
Place near JDDR.L.203 & JDDR.L.204



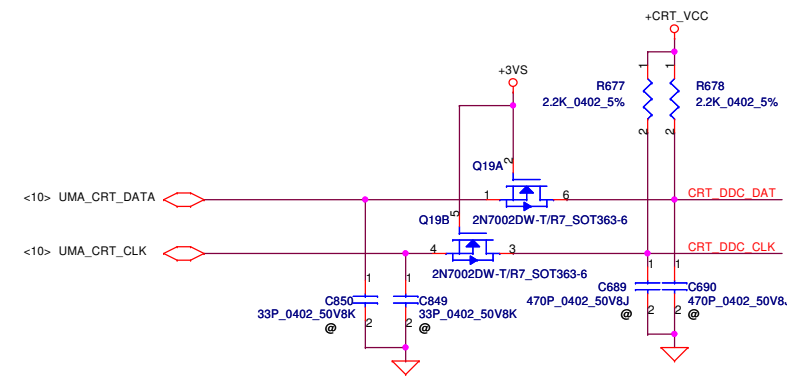
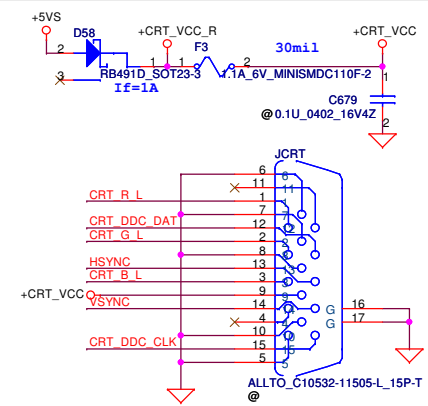
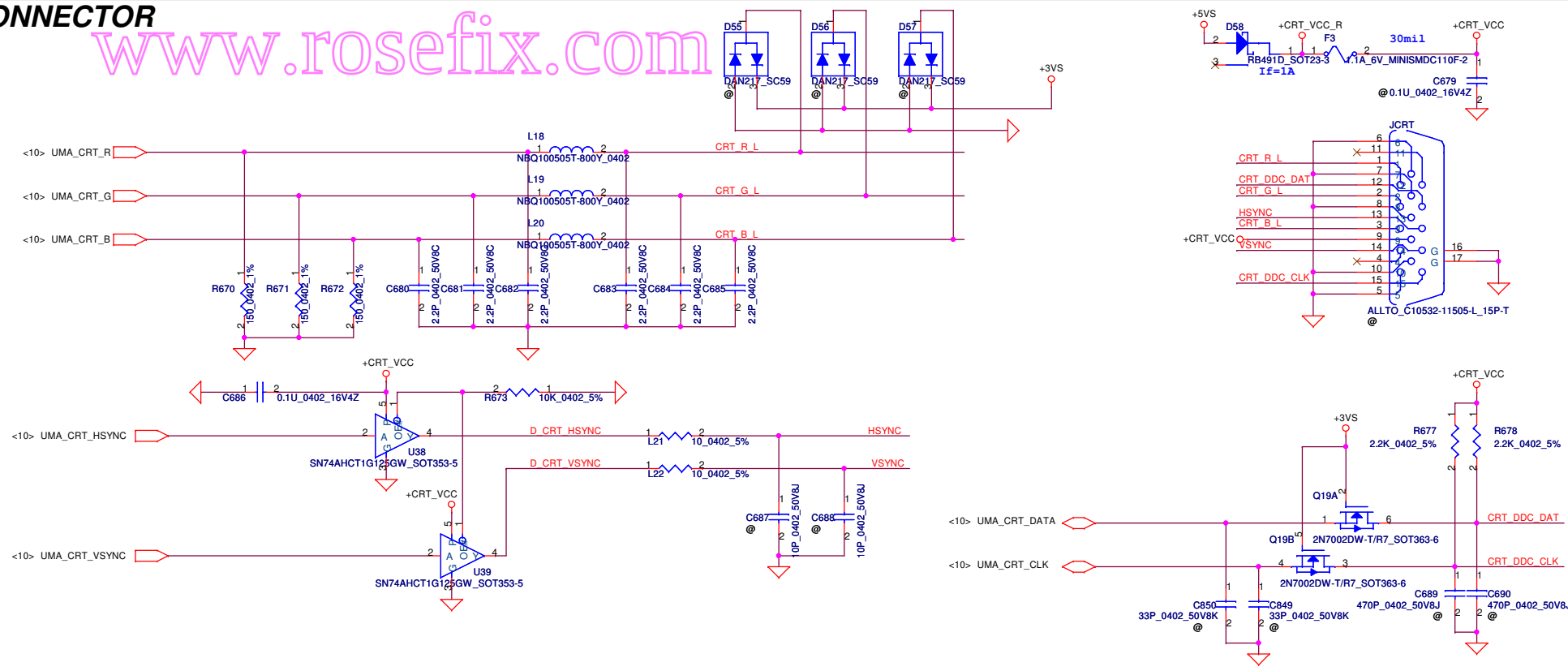
Compal Electronics, Inc.			
Title		DDRII-SODIMM0	
Size	Document Number	PWWAA LA6841P M/B	Rev 0.1
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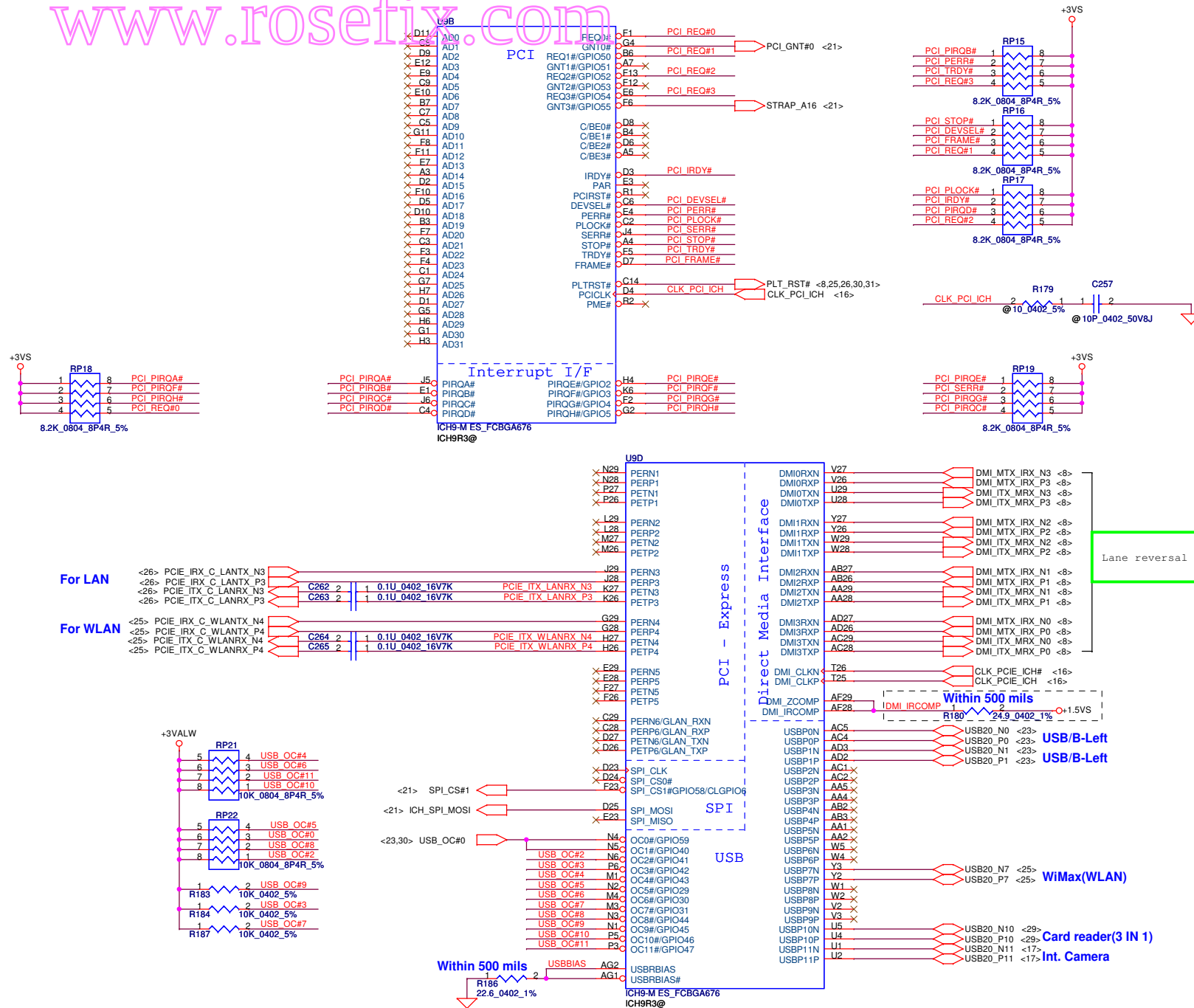
LCD/PANEL BD Conn.



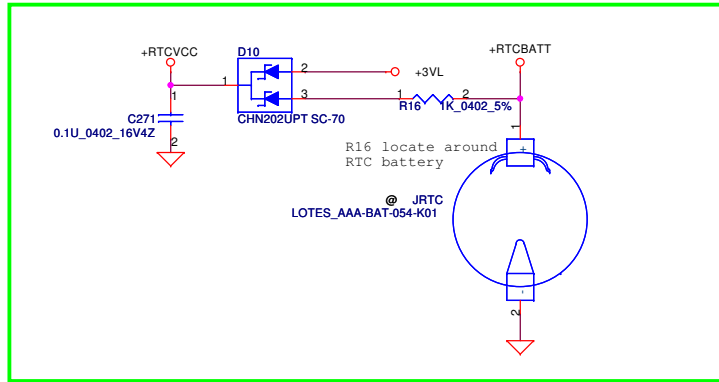
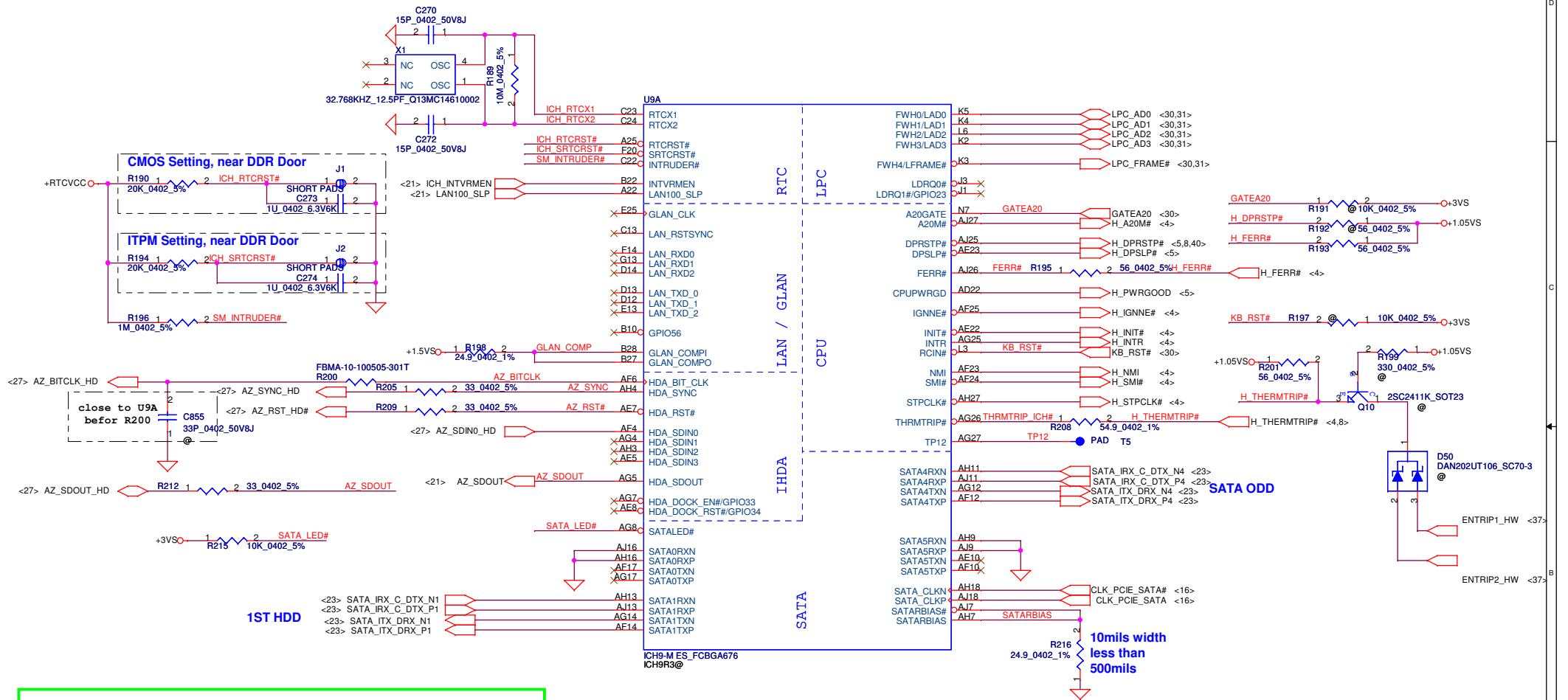
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Issued Date	2009/06/12	Deciphered Date	2010/06/12	Title	
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Date:	Monday, August 16, 2010	Sheet	17	of	44



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Size		Document Number		Rev	
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PWWAA LA6841P M/B		0.1			

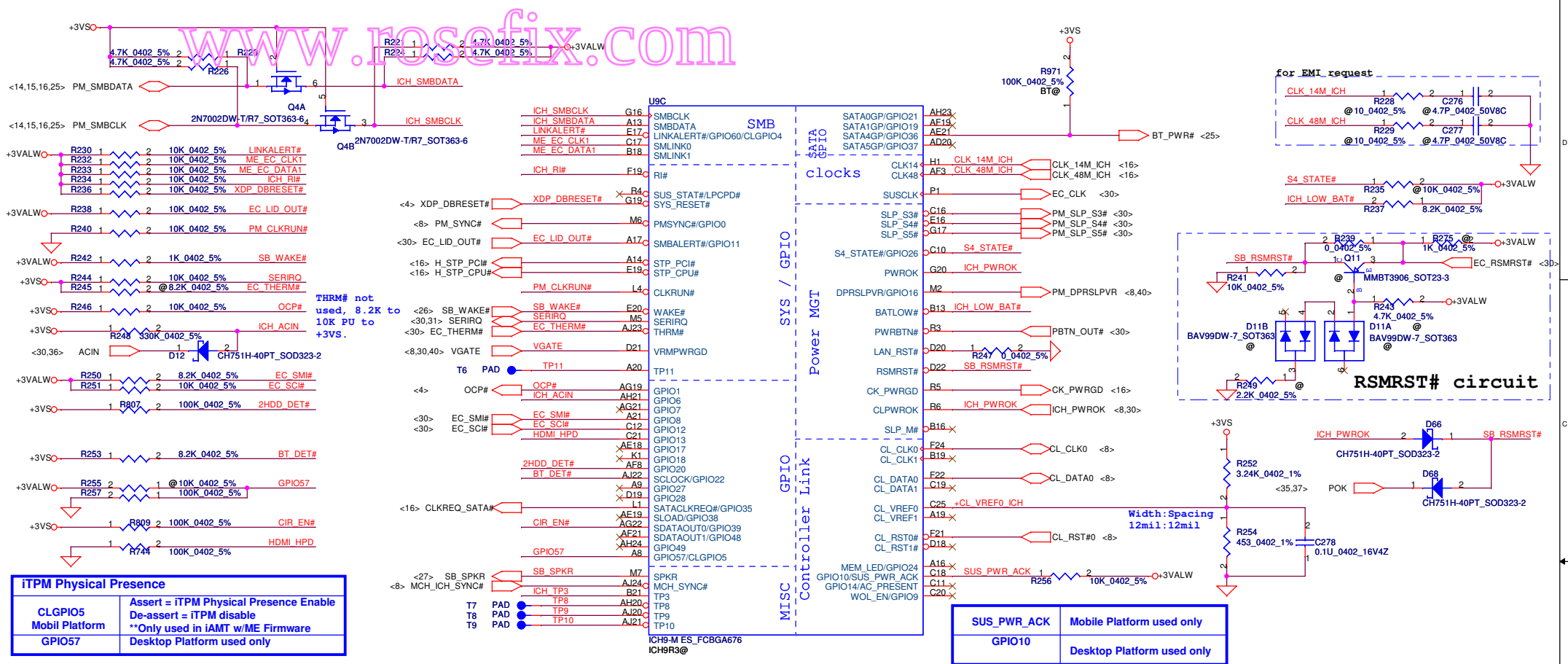


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Size	Document Number	PWWAA LA6841P M/B		Rev	0.1
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Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/06/12		Deciphered Date		Title			
								ICH9M(2/4)-LAN, IDELPC, RTC			
								Size			
								Document Number			
								PWWAA LA6841P M/B			
								Date			
								Monday, August 16, 2010			
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								Rev			
								0.1			

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ICH9M Strap Pin

+3VSO R258 @ 1K_0402_5% ICH_SPI_MOSI <19>

+3VSO R261 @ 1K_0402_5% SB_SPKR

R263 @ 1K_0402_5% PCI_GNT#0 <19>
R265 @ 1K_0402_5% SPI_CS#1 <19>

R267 @ 1K_0402_5% STRAP_A16 <19>

Internal TPM Strap (Internal pull-down)

SPI_MOSI	Low= Disable
High= iTPM enable by MCH strap*	

No Reboot Strap (Internal pull-up)

SB_SPKR	Low= "Default"
High= "No Reboot"	

Boot BIOS Strap (Internal pull-up)

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable
High= Default* (Internal pull-up)	

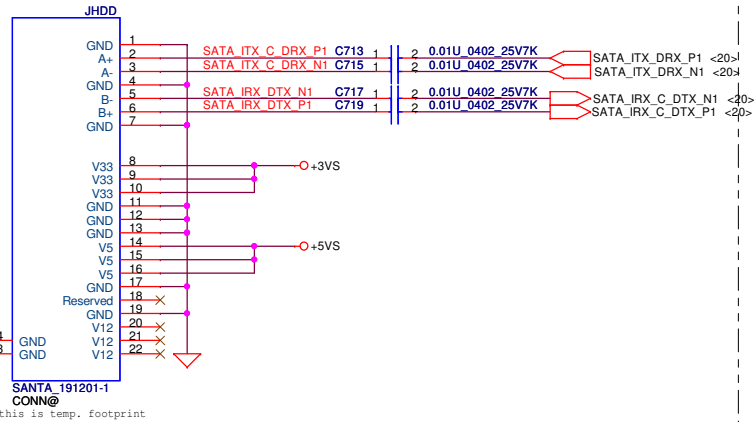
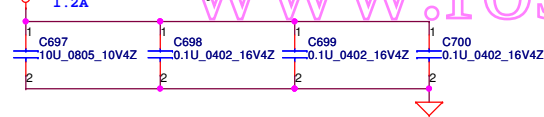
+RTCVCCO R259 330K_0402_5% ICH_INTVRMEN <20>
R260 @ 0_0402_5% LAN100_SLP <20>

+3VSO R266 @ 1K_0402_5% AZ_SDOUT <20>
R268 @ 1K_0402_5% ICH_TP3

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Size		Document Number		PWWAA LA6841P M/B	
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				Rev 0.1	

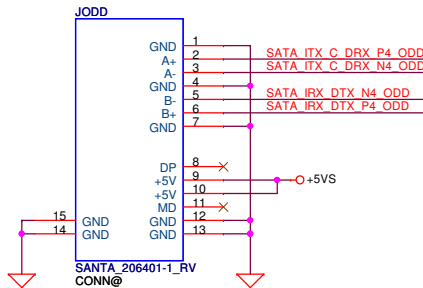
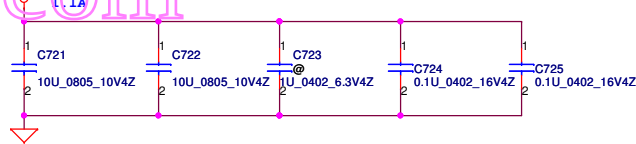
SATA HDD Conn.

Place closely JHDD SATA CONN.

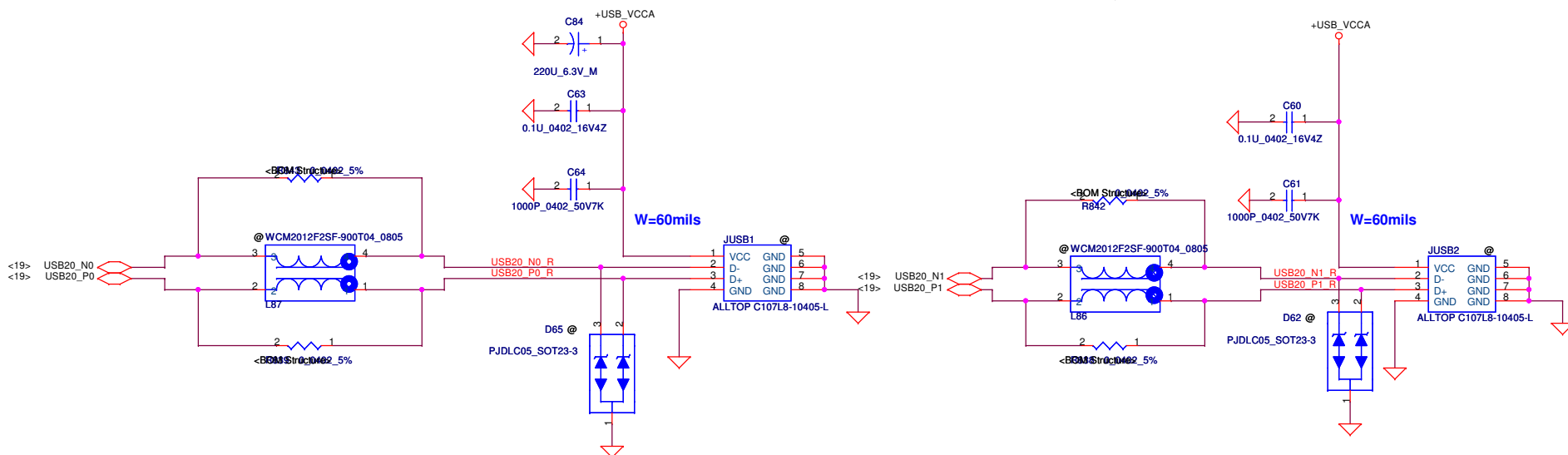


SATA ODD Conn

Place components close to ODD CONN.

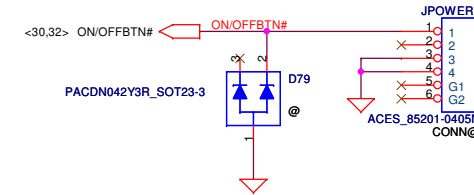


USB Conn

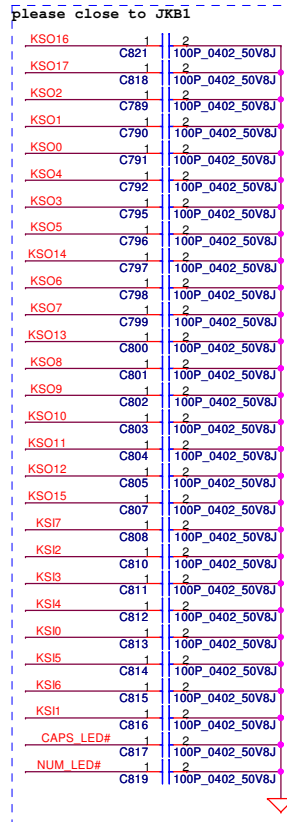
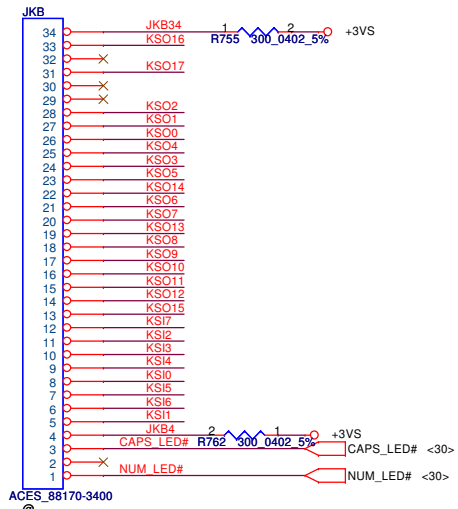


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POWER/B Connector Check footprint and pin define

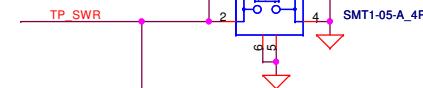


KEYBOARD CONN

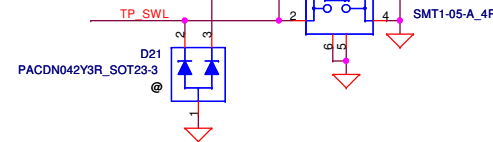


Touch/B Connector

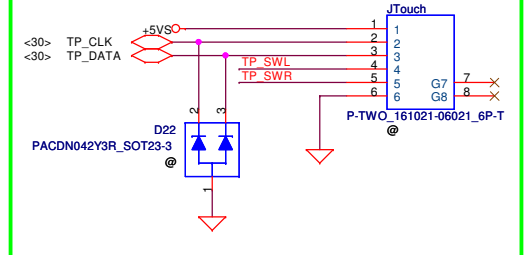
Right Switch



Left Switch

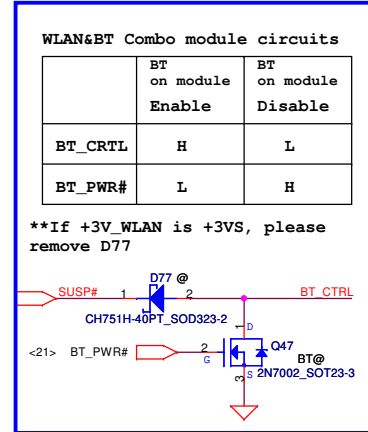
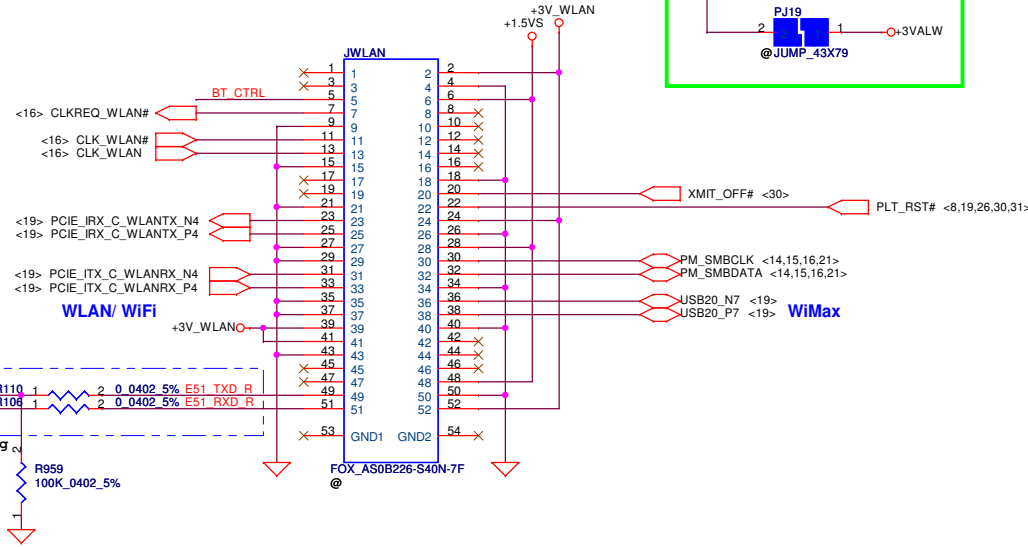
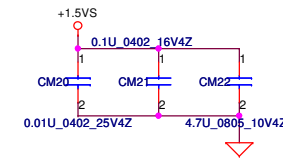
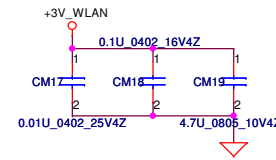
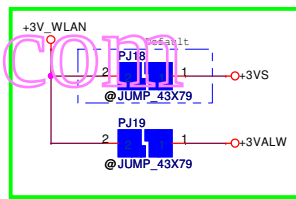


Check signal to TP module through FFC

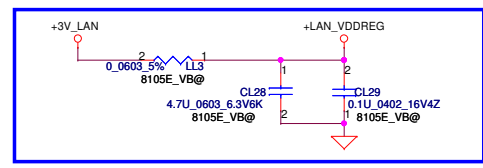
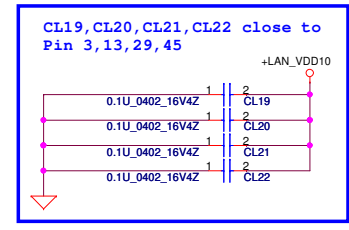
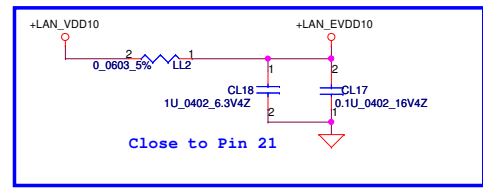
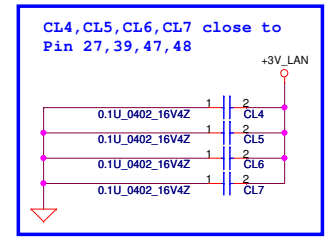
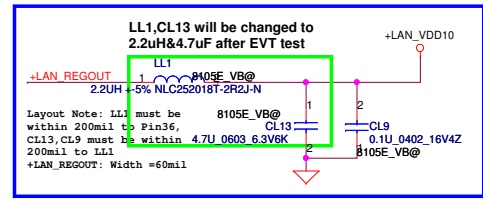
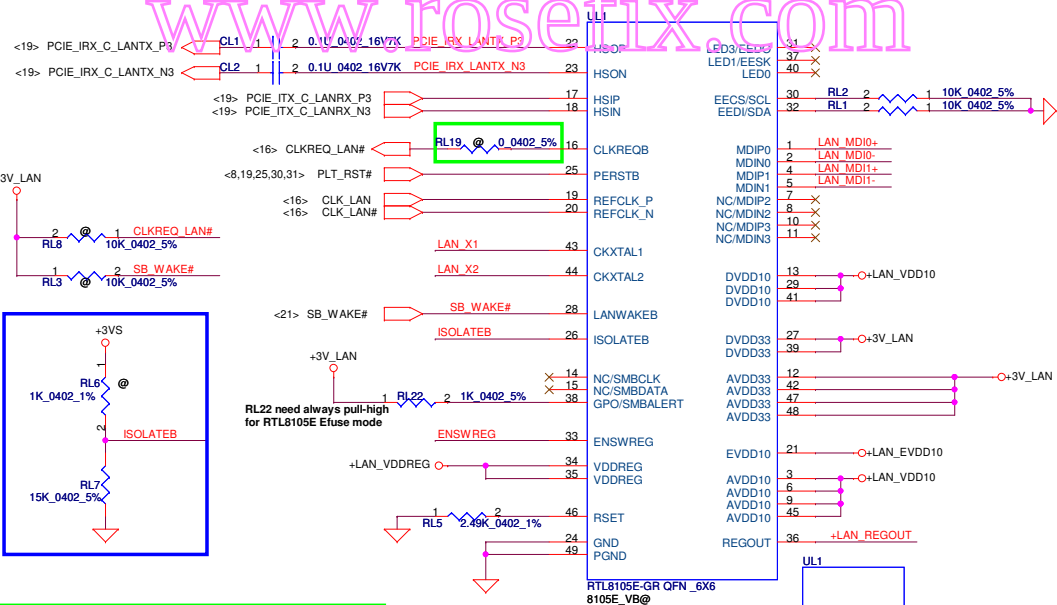


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PCle Mini Card-WLAN/WiMax

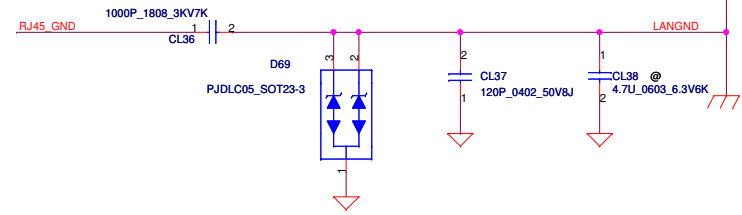
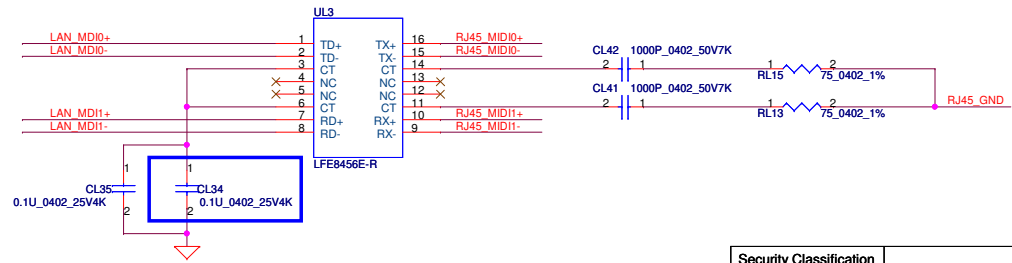
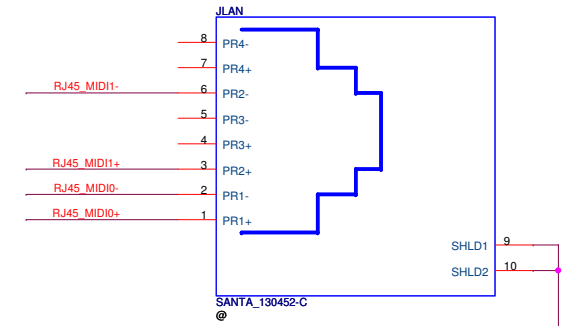


Add BT_CTRL for WLAN & BT Combo module at DVT

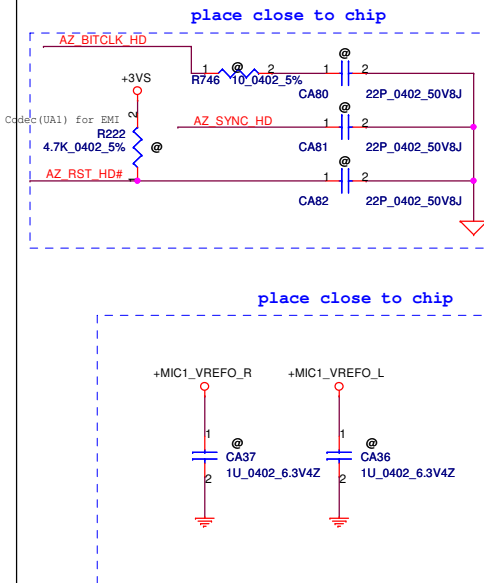


Need to change to non-LED type

LAN Conn.



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						Size		Document Number		Rev	
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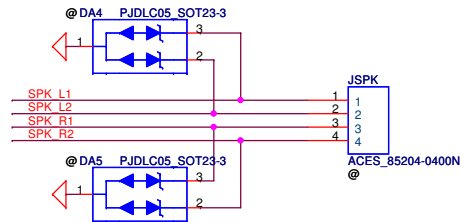
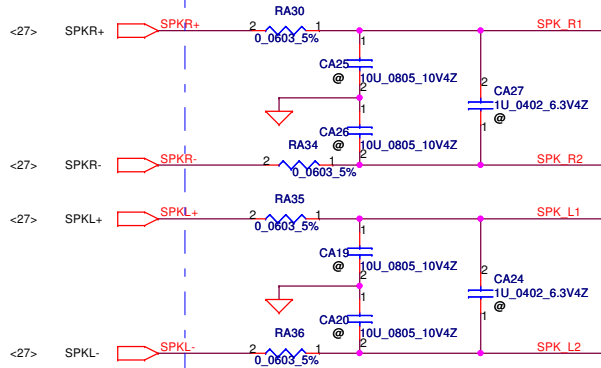
place close to chip

<28> MIC_SENSE  RA10  20K_0402_1  SENSE_A

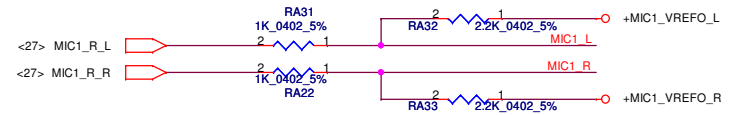
<28> NBA_PLUG  RA21  39.2K_0402_1  SENSE_A

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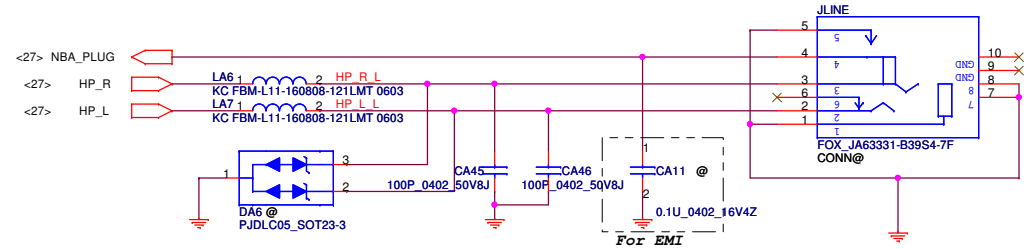
placement near Audio Codec UA1



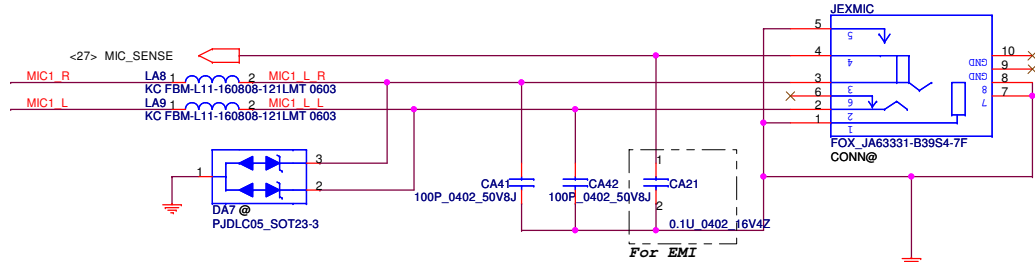
Ext. Mic



HeadPhone/LINE Out JACK

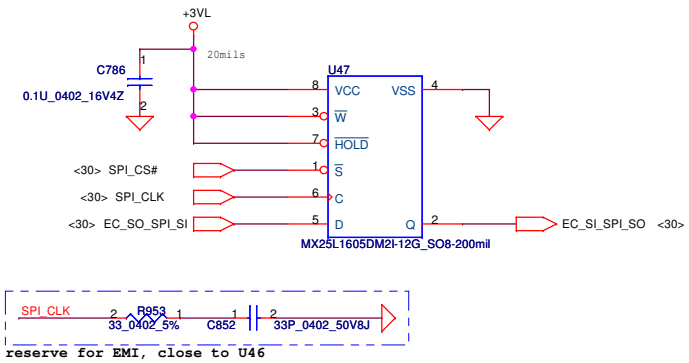


Ext.MIC/LINE IN JACK

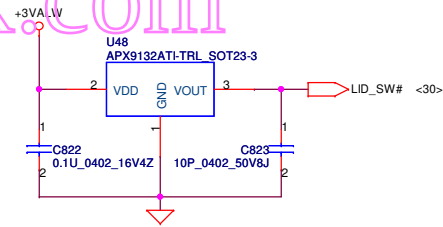


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SPI Flash (16M*1)

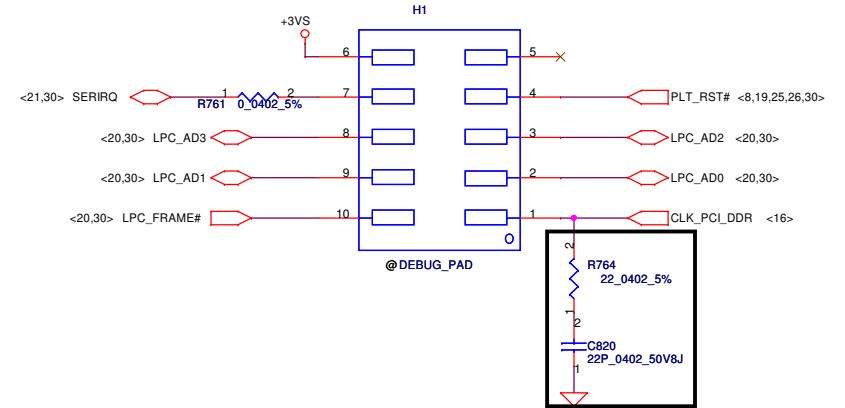


Lid SW

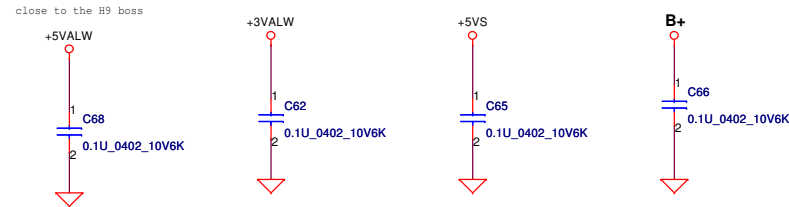


LPC Debug Port

Please place the PAD under DDR DIMM.



for EMI



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Power Button

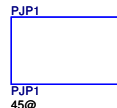
www.rosefix.com

ISPD

PCB



DC-IN



NB_GL40_R3

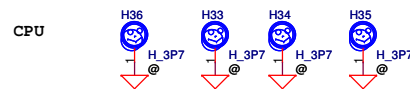
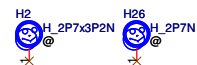
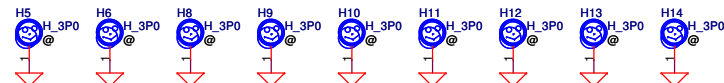
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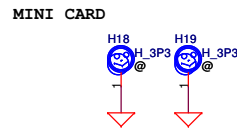
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SB_R1

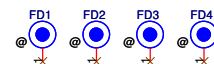
Screw Hole



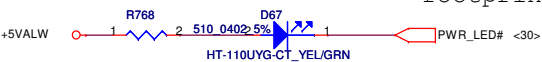
SB



PCB Fedcal Mark PAD

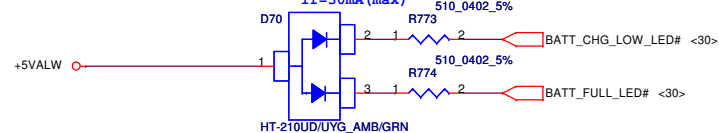


DC-IN LED Vf=2.0V (typ), 2.4V (max) If=30mA (max) footprint is SC510UYG000



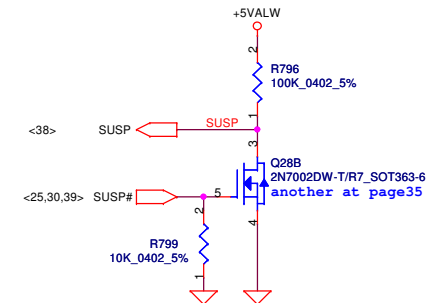
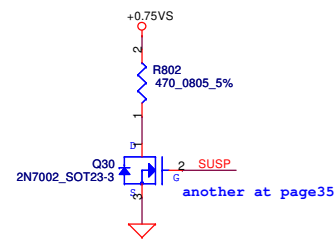
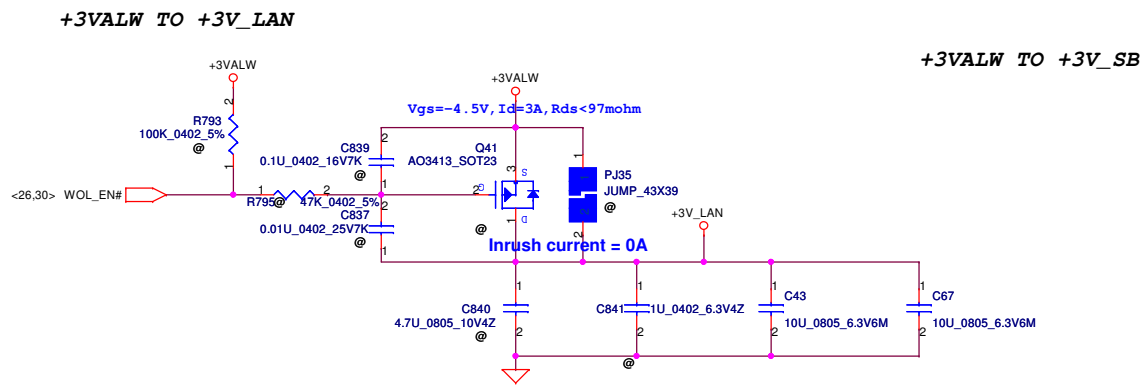
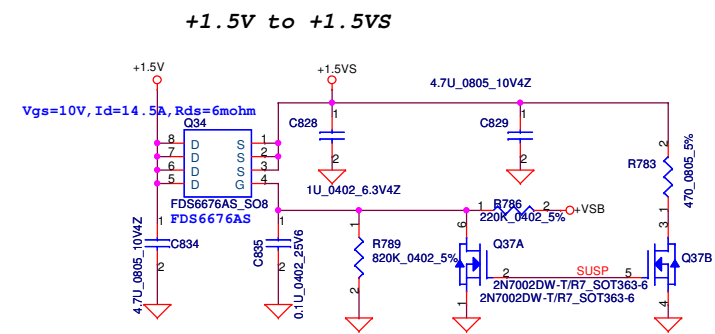
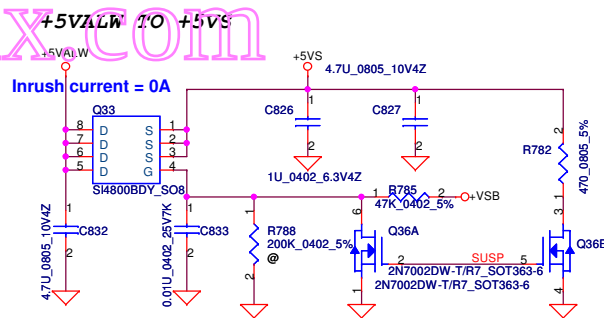
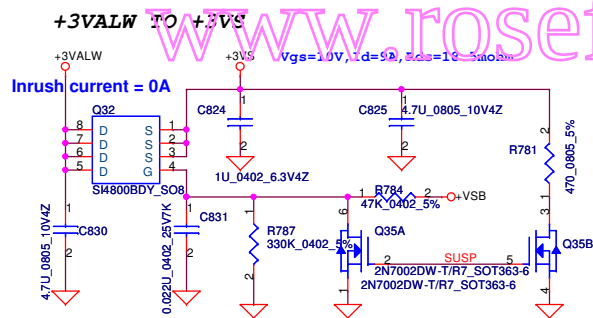
BATT CHARGE/FULL LED

Vf=1.9V (typ), 2.4V (max) for amber
Vf=2.0V (typ), 2.4V (max) for green
If=30mA (max)



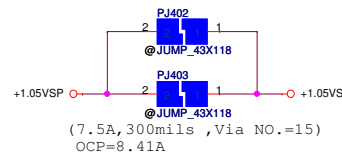
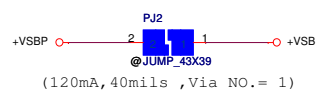
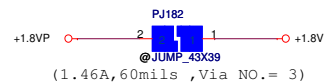
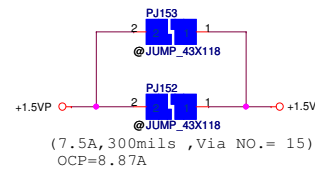
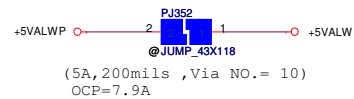
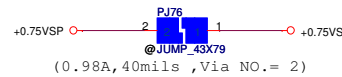
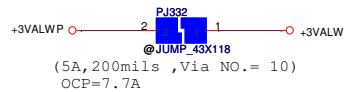
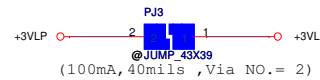
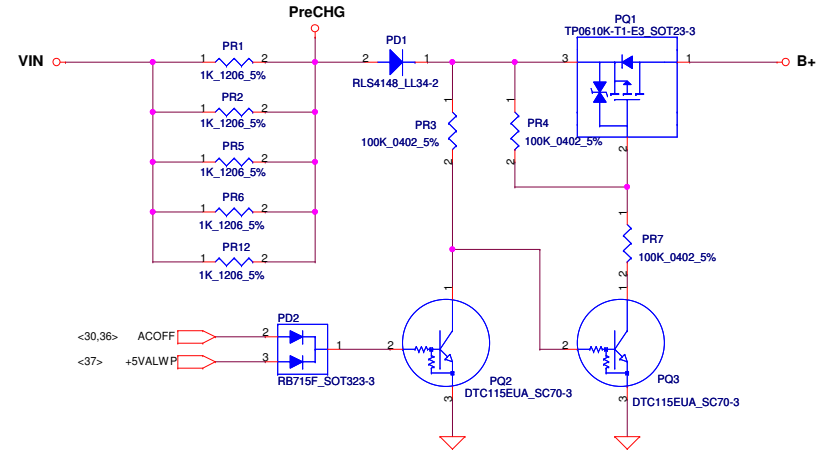
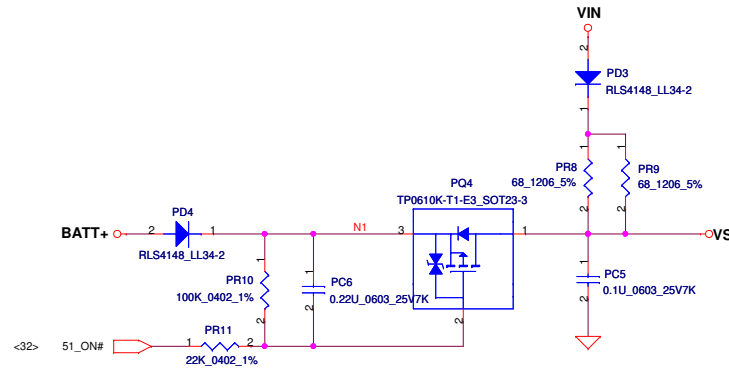
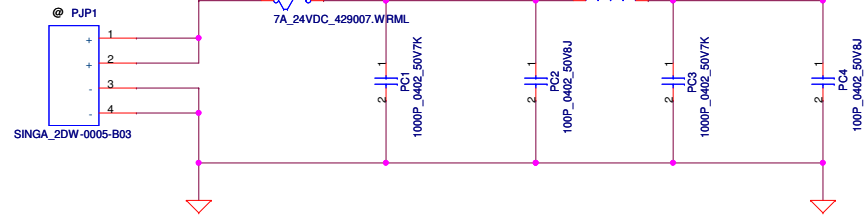
footprint is SC510UDG000

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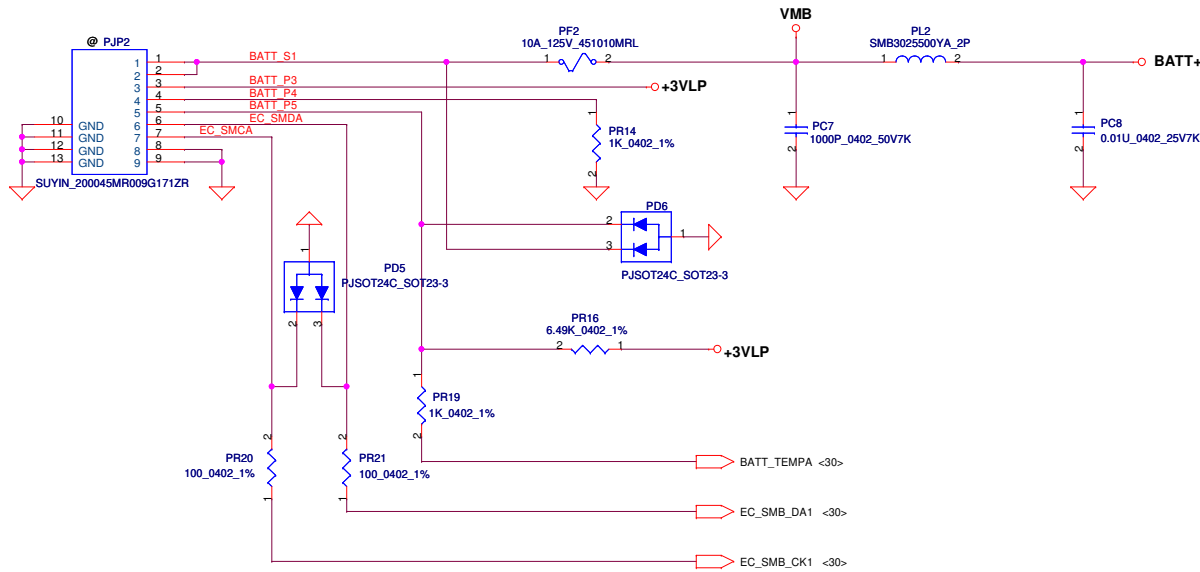
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Size	Document Number	PSWAA LA6511P M/B		Rev	0.1
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DC301001M80

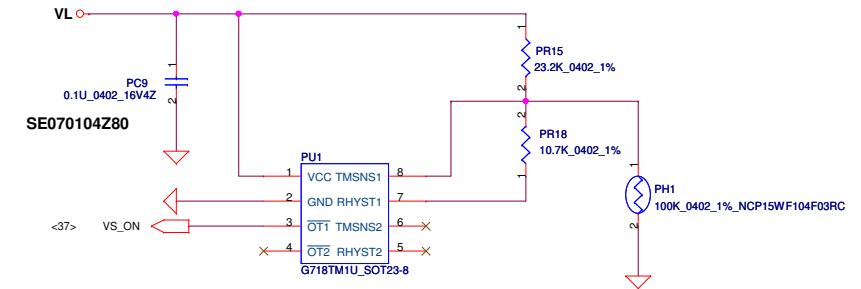


ACIN

	Precharge detector		
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V



PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 56 degree C



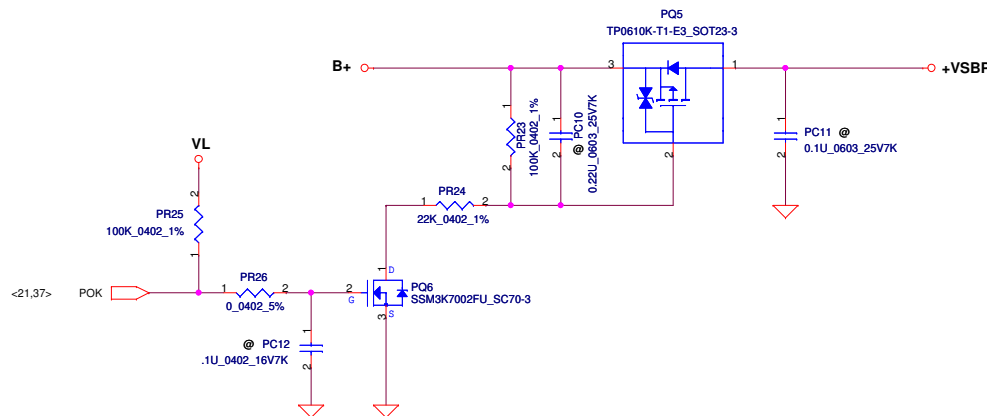
$$R_{set} = 3 * R_{tmh}$$

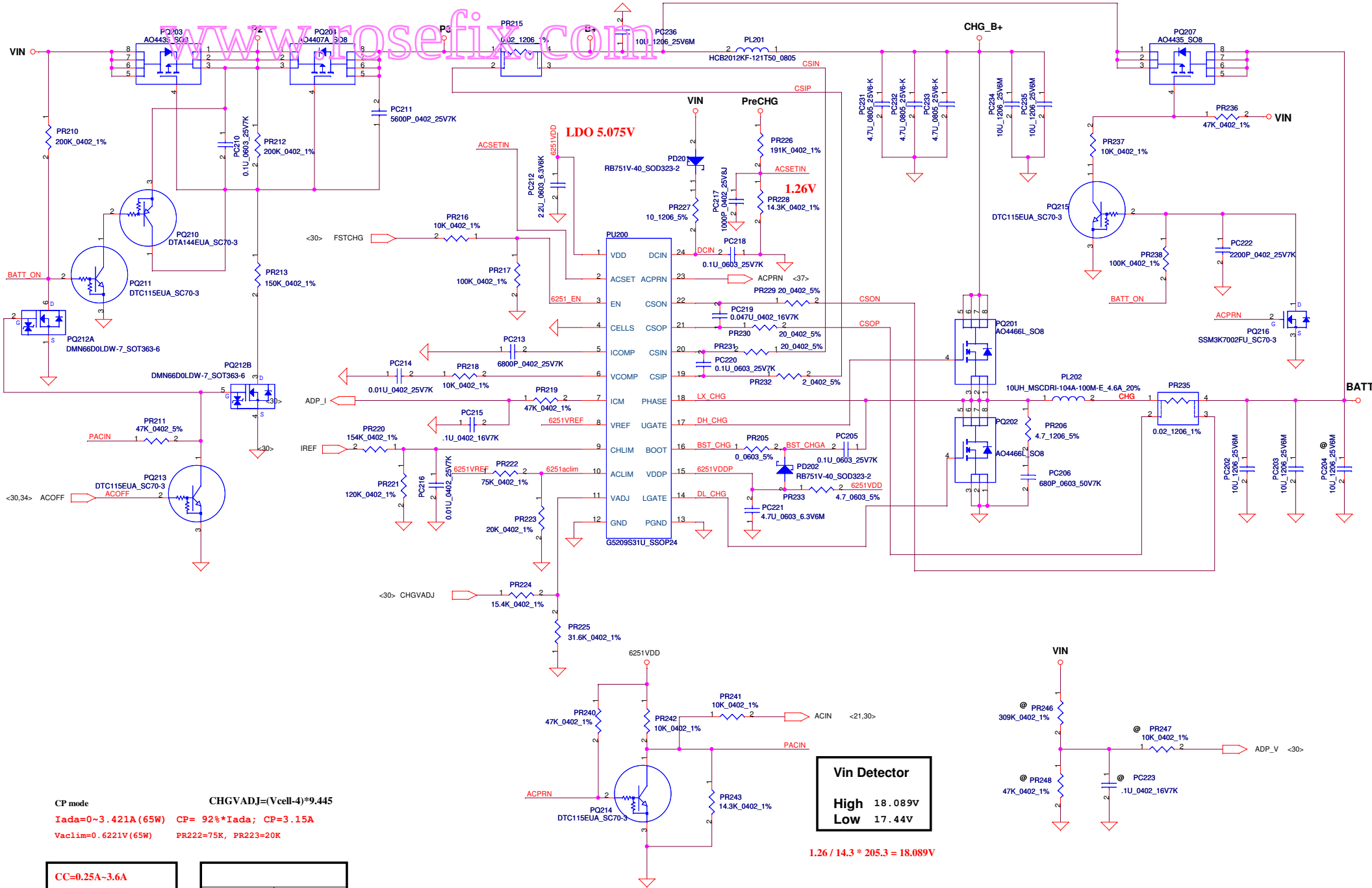
$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.79K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.79K = 23.37K \Rightarrow 23.2K$$

$$R_{hyst} = (23.2K * 26.1K) / (3 * 26.1K - 23.2K) = 10.99K \Rightarrow 10.7K$$





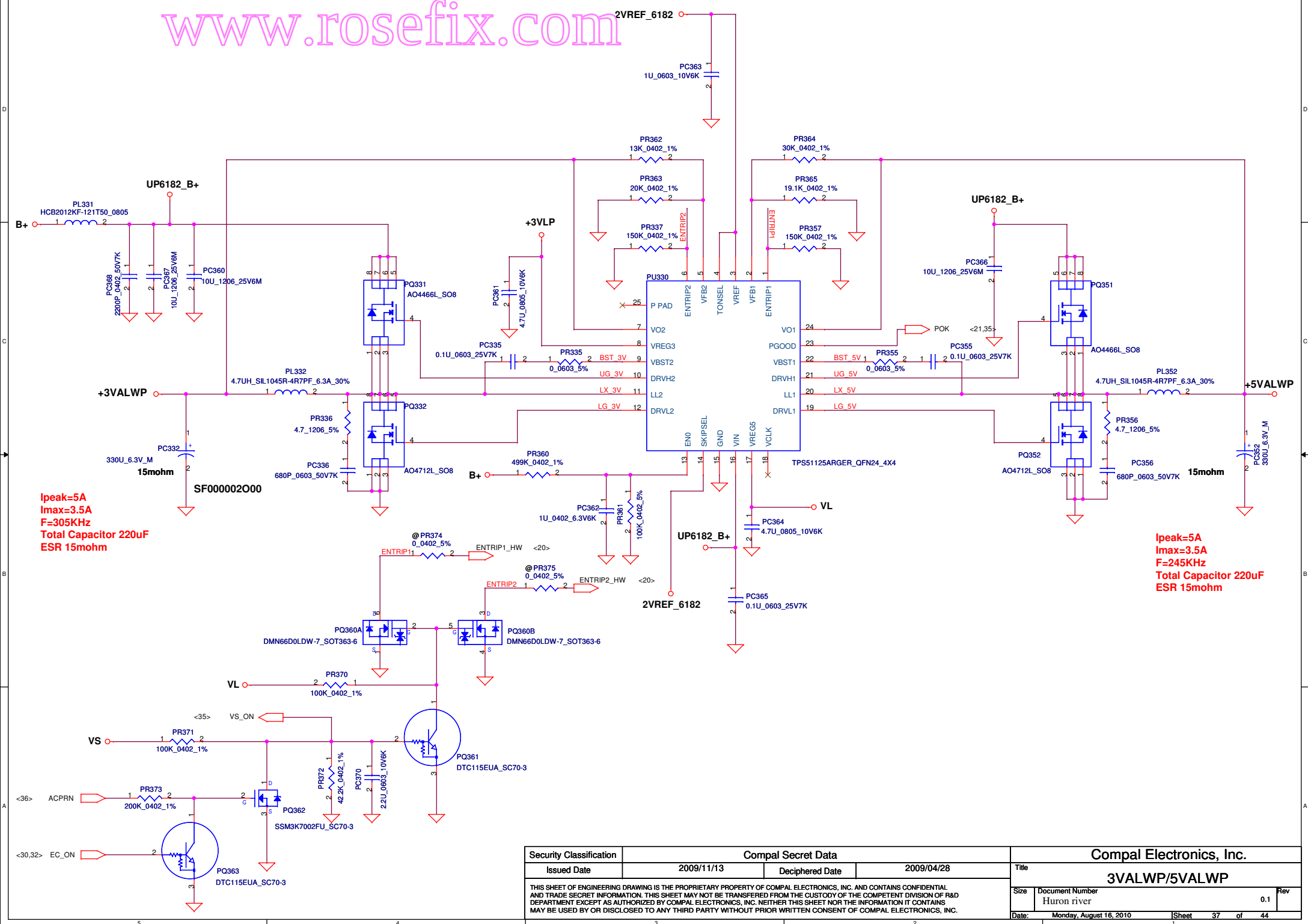
CP mode CHGVADJ=(Vcell-4)*9.445
 I_{ada}=0~3.421A (65W) CP= 92%*I_{ada}; CP=3.15A
 V_{ac1im}=0.6221V (65W) PR222=75K, PR223=20K

CC=0.25A-3.6A
 IREF=0.9133*I_{charge}
 IREF=0.228V-3.29V
 VCHLIM need over 95mV

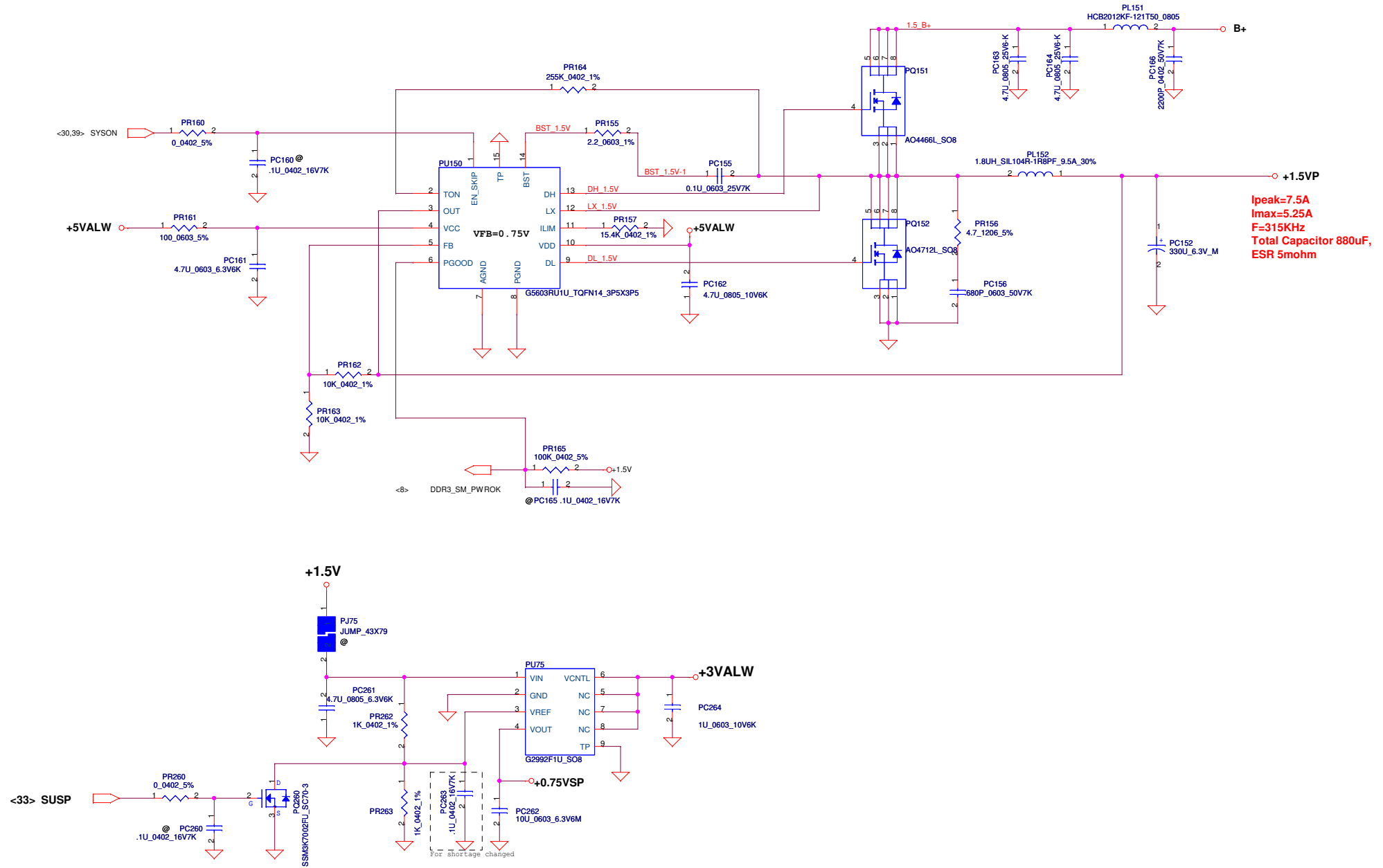
Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

Vin Detector
 High 18.089V
 Low 17.44V

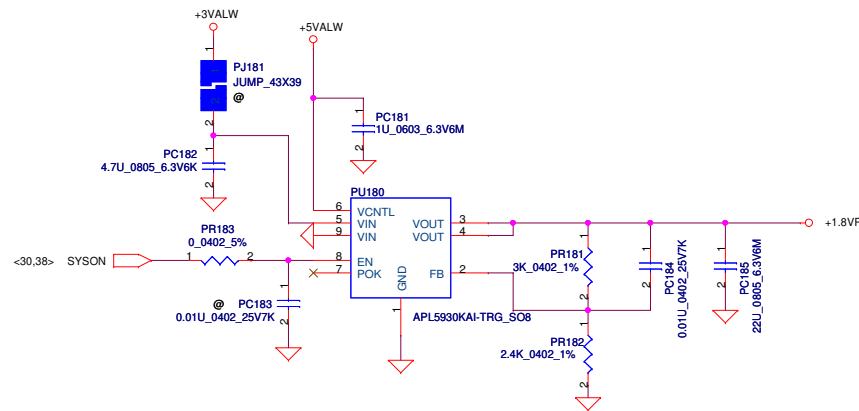
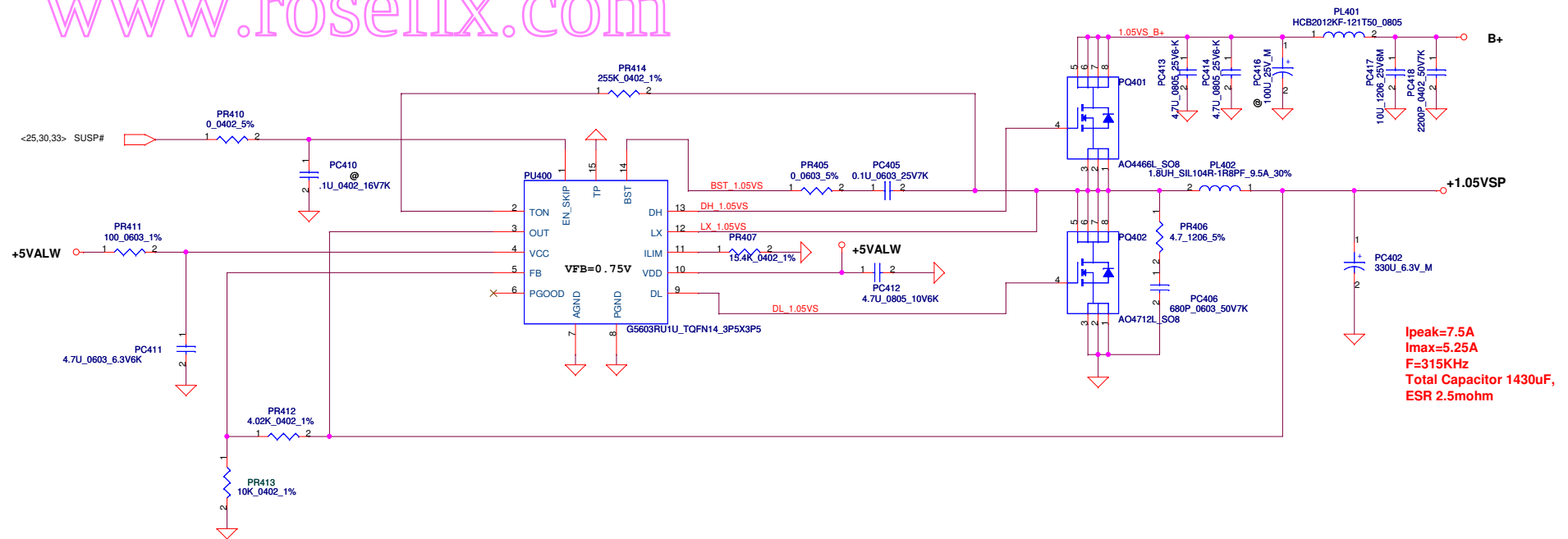
$1.26 / 14.3 * 205.3 = 18.089V$

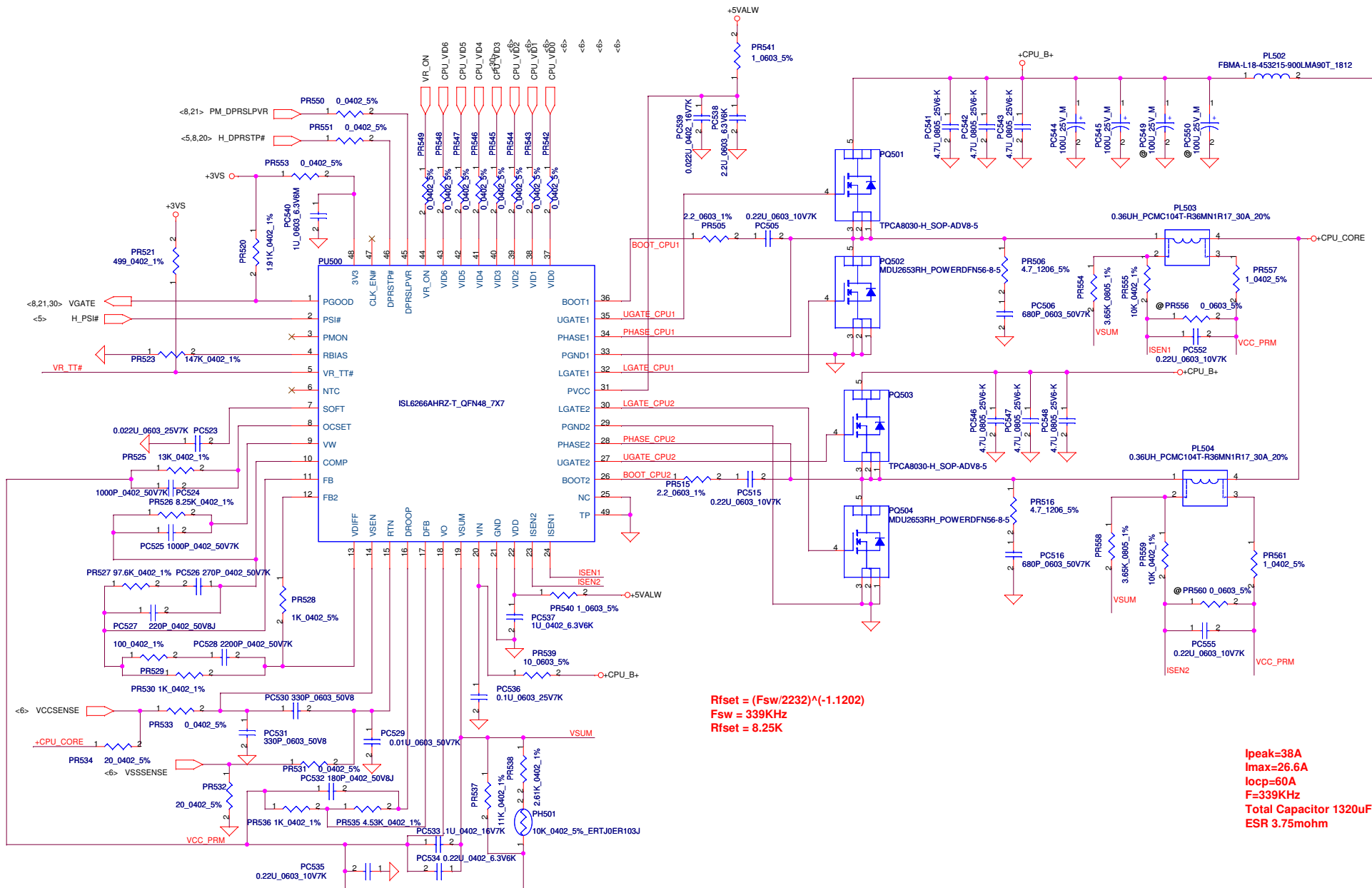


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				Size	Rev
				Document Number	0.1
				KSWAA	
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Rfset = (Fsw/2232)^(-1.1202)
Fsw = 339KHz
Rfset = 8.25K

Ipeak=38A
Imax=26.6A
Iocp=60A
F=339KHz
Total Capacitor 1320uF,
ESR 3.75mohm

PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 0.2 EVT
NO DATE PAGE MODIFICATION LIST

				PURPOSE
1.	07/23	32	Change R768,R773 from 120 ohm to 510 ohm	for changed 5mA LED
2.	07/23	32	Chage LED power rail from +3valw to +5valw	for changed 5mA LED
3.	07/23	23	del. L86,L87 EMI component	for EMI request
4.	07/23	31	Add 1PCS(C62) 0.1uF_0402 on +3Valw-->GND	for EMI request
5.	07/23	31	Add 1PCS(C65) 0.1uF_0402 on +5Vs-->GND	for EMI request
6.	07/23	31	Add 0.1uF_0402(C66) on B+-->GND close to H8	for EMI request
7.	07/23	28	JLINE and JEXMIC change from DC2300006300 to DC230004L00	for SMT DFx request
8.	07/27	30	change R742 from +3VALW to +3VL	for LED no function issue
9.	07/27	8	add test pad ON U3.E36,U3.AK34	for ATE request
10.	07/27	33	change part number of Q30 (SB770020010)	for Reduce BOM part type
11.	07/27	32	Change D67(power on LED) from SC510UYG000 to SC500009D00	for changed 5mA LED
12.	07/27	32	Change D70(DC in LED) from SC510UDG000 to SC500009800	for changed 5mA LED
13.	07/29	14	un-mount CD7,CD8,CD9,CD10,CD11,CD12,CD30,CD31,CD32,CD34,and mount(22uF) CD29,CD33	for design change
14.	07/29	11	For +1.5V ,C78 from 330uF to 390u (SF000002000)	for design change
15.	07/29	12	Change R82 and R81 from inductor to Bead	for design change
16.	07/29	15	+0.75VS filter un-mount CD22 and CD44	for design change
17.	08/03	25	un-mount D77	for If +3V_WLAN is +3VS, please un-mount D77

PIR (Product Improve Record)

www.rosefix.com

REVISION CHANGE: 0.2 TO 0.3 Pre-MP

NO	DATE	PAGE	MODIFICATION LIST
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- | | | | |
|----|-------|----|---------------------------|
| 1. | 08/09 | 29 | Change net V1_8 to +v1_8 |
| 2. | 08/09 | 32 | add R774 |
| 3. | 08/12 | 32 | un-mount SW5 and SW6 |
| 4. | 08/12 | 20 | add R16 (for RTC battery) |
| 5. | 08/13 | 26 | add D69 and un-mount CL38 |
| 6. | 08/13 | 26 | CL37 from 0.1uF to 120pF |
| 7. | 08/13 | 26 | add CL35 |
| 8. | 08/13 | 27 | add CA51 |
| 9. | 08/13 | 33 | add C67 and C43 |

PURPOSE

- for power trace
for LED control
for Pre-MP do need power SW
for design change
for EMI request
for EMI request
for EMI request
for EMI request
for EMI request

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PIR (Product Improve Record)

REVISION CHANGE: 0.1 TO 1.0

NO DATE PAGE MODIFICATION LIST

PURPOSE

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Page#

Item Title

Solution Description

PVT : modification from EVT		
P35	mount ESD diode	mount PD5, PD6
P36	EMI request	add PC236 10uF
P37	EMI request	add PC367 10uF, PC368 2200pF
P37	change 3/5V IC main source	change PU330 to UP6182
P38	EMI request	add PC166 2200pF
P39	EMI request	add PC417 10uF, PC418 2200pF
P40	adjust loadline	change PR535 to 3.09K
P34	unify source	change PD1 to SC11N414880
P36	unify source	change PQ216 to SB0000009610
P37	unify source	change PQ362 to SB0000009610
P40	unify source	change PL502 to SM010020720
P40	turn on speed too quick	change PQ502, PQ504 to MDU2653RH
P37	change cap to 330uF with same price	change PC332, PC352 to SF0000002000
P38	change cap to 330uF with same price	change PC152 to SF0000002000
P39	change cap to 330uF with same price	change PC402 to SF0000002000
P36	EMI request to mount snubber circuit, ISN caps	add PR206, PC206; PC234, PC235
P37	EMI request to mount snubber circuit	add PR336, PC336; PR356, PC356
P38	EMI request to mount snubber circuit & boost resistor	add PR156, PC156; change PR155 to 2.2ohm
P39	EMI request to mount snubber circuit	add PR406, PC406
P40	EMI request to mount snubber circuit	add PR506, PC506; PR516, PC516
PreMP : modification from PVT		
P34	increase precharge design margin	add PR12 1K
P35	change OTP setting	change PR15 to 23.2K, PR18 to 10.7K
P35	change source	chagne PC9 to SE070104280
P37	change 3/5V IC main source	change PU330 to TP851125A
P38	change 0.75V IC main source	change PU75 to G2992
P40	adjust loadline	change PR535 to 4.53K
P40	adjust transient stability	change PR527 to 220pF