

Compal Confidential

PBL10 Project

LA-6731P REV1.0 Schematic

Intel Sandy Bridge/Cougar Point(UMA)

2010-12-06 Rev 1.0

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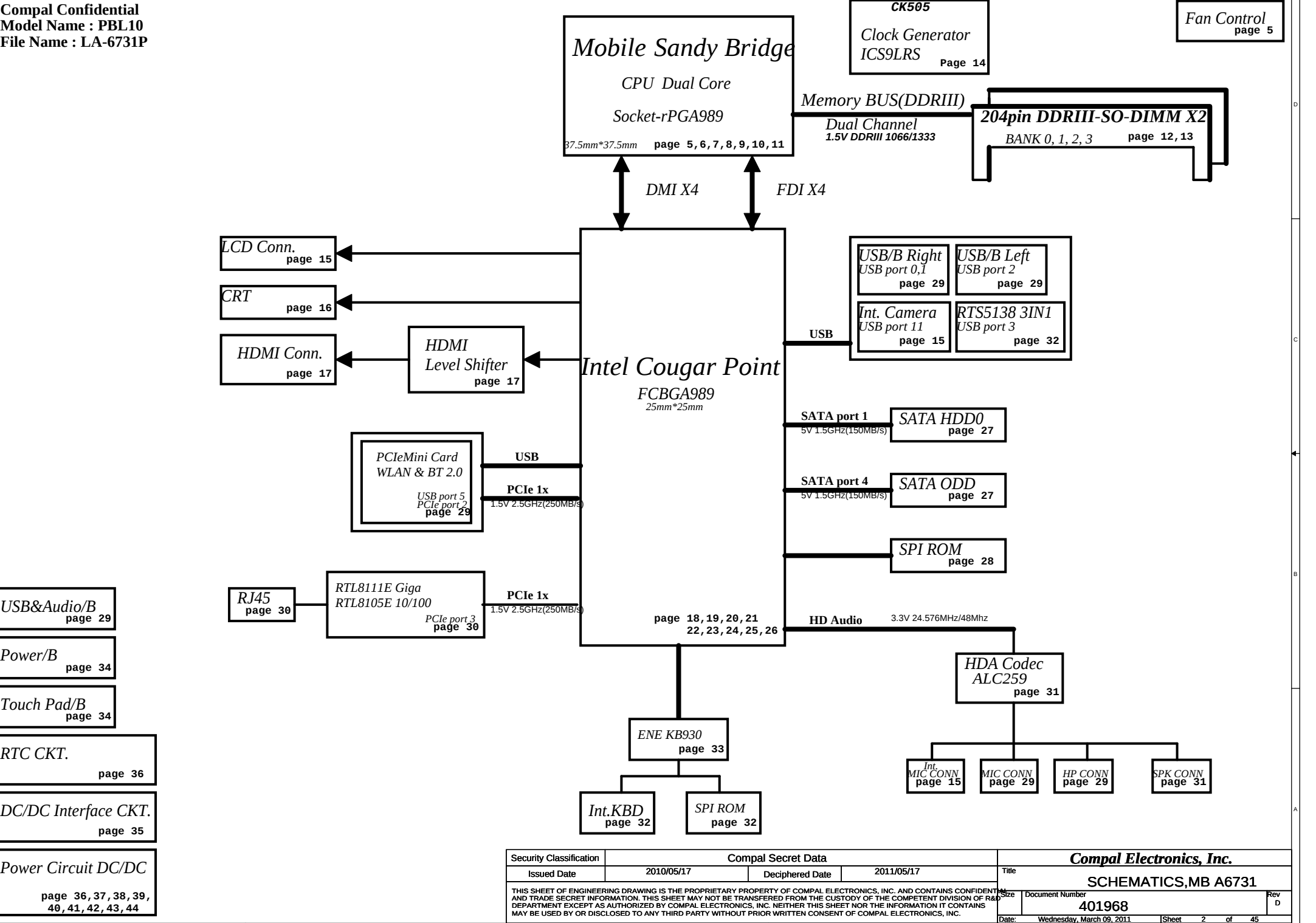
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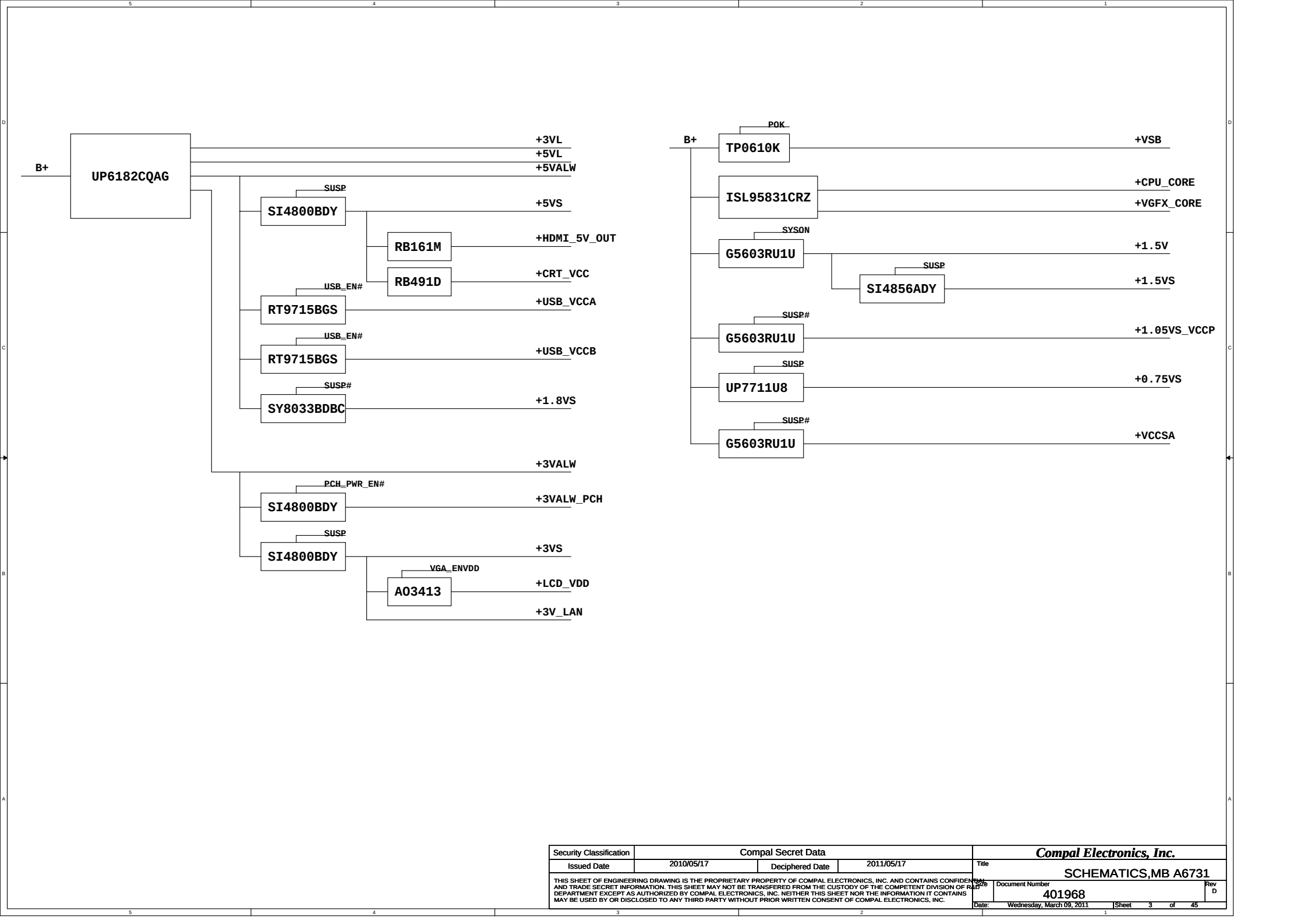
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page 36

DC/DC Interface CKT.
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SIGNAL							
	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

EC SM Bus2 address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM configu table

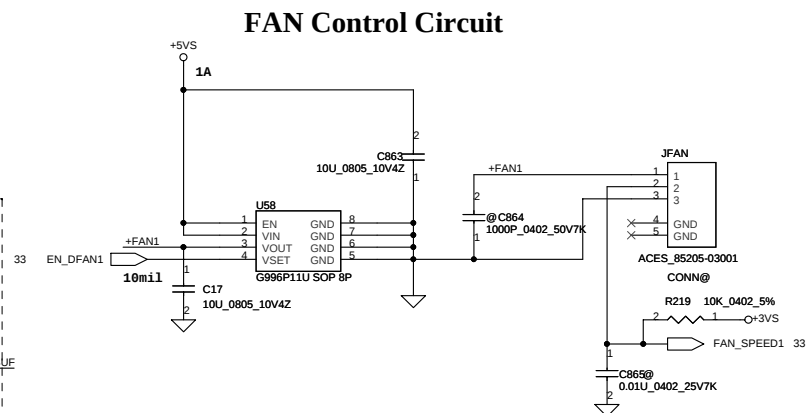
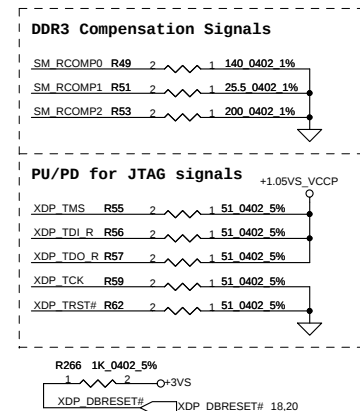
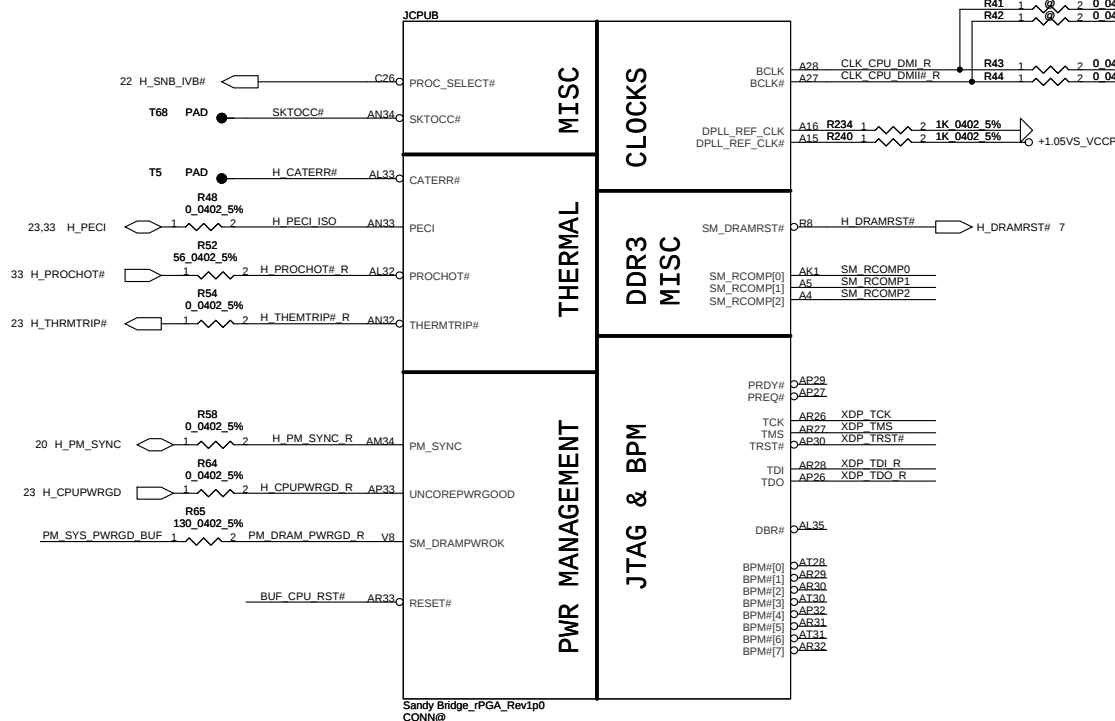
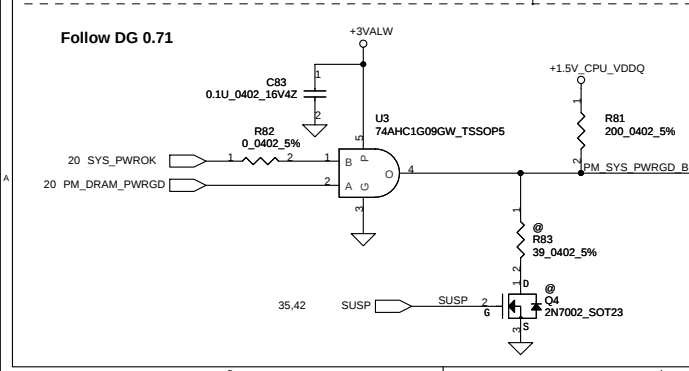
	SKU	Bom config	Description
1	46196830L01	DA6@/HDMI@/8105E@/PCH@	PBL10 UMA DUAL 10-100
2	46196830L02	DA6@/HDMI@/8111E@/PCH@	PBL10 UMA DUAL GIGA LAN
3			
4			
5			
6			
7			
8			

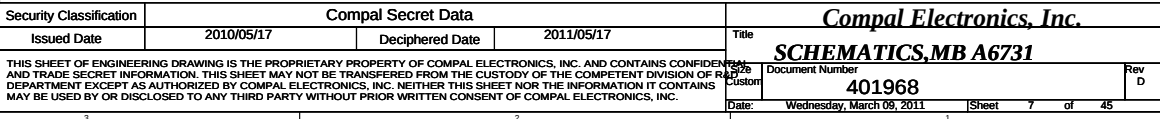
Bom configu(HDMI@/8105E@/8111E@/DA6@/DAZ@/45@)

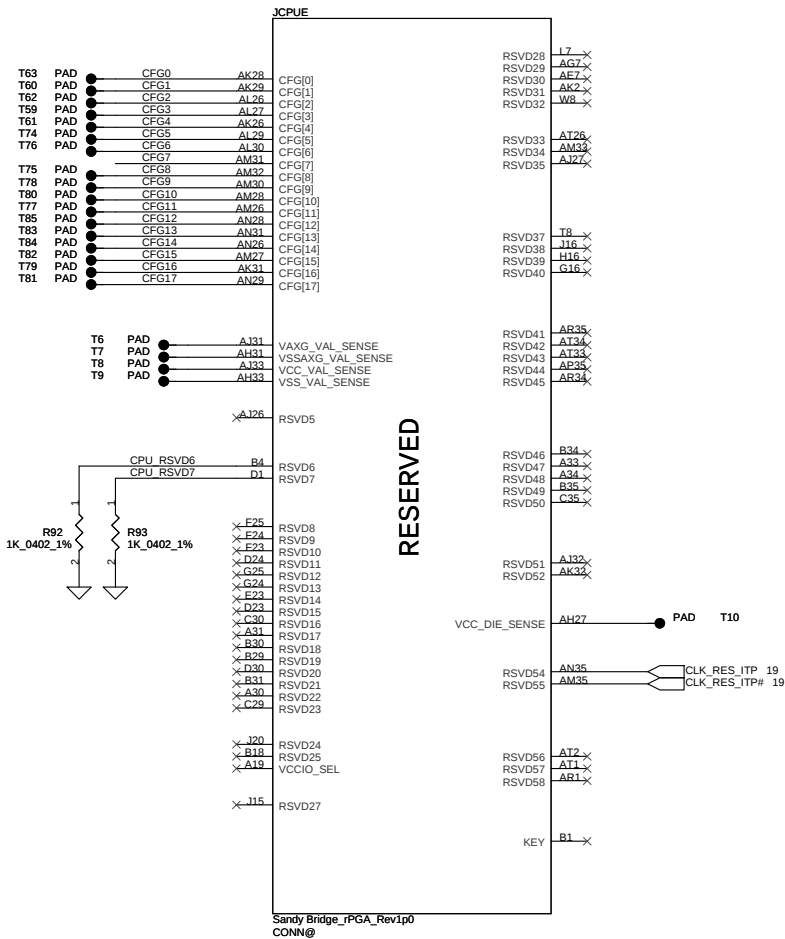
PCH And PCBA table

PCH	U4 BD82HM65 SLH9D B2 FCBGA 989P PCH PCH@				
PCB	ZZZ DAZ@ PCB LA-6731P REV10	ZZZ DA6@ PCB LA-6731P REV10	ZZZ DA4@ PCB LS-6732P REV10	ZZZ DA2@ PCB LS-6731P REV10	

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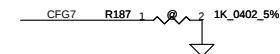
CFG Straps for Processor

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

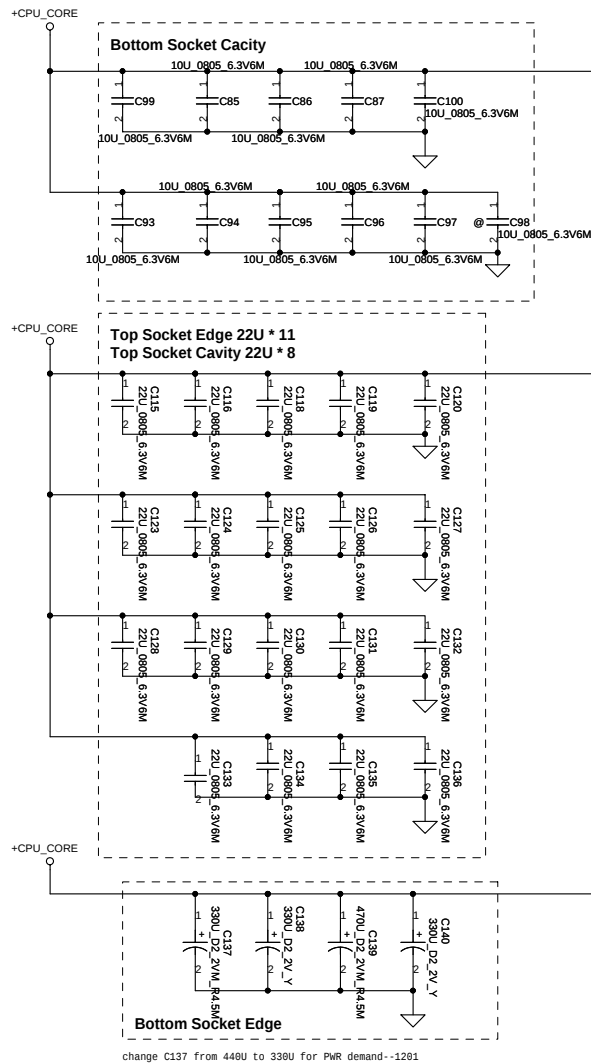
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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POWER



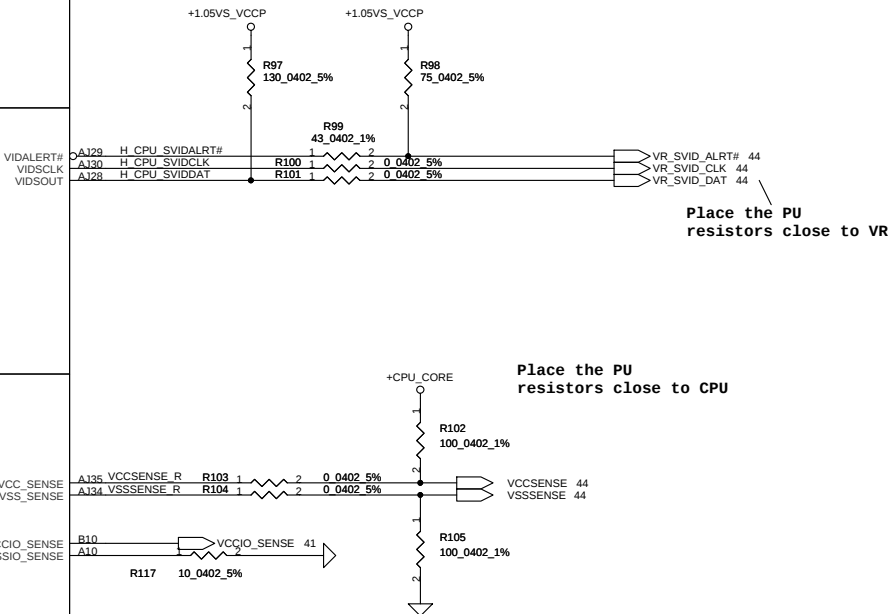
94A	
AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
Y25	VCC61
Y24	VCC62
Y23	VCC63
Y22	VCC64
Y21	VCC65
Y20	VCC66
Y19	VCC67
Y18	VCC68
Y17	VCC69
Y16	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
U25	VCC81
U24	VCC82
U23	VCC83
U22	VCC84
U21	VCC85
U20	VCC86
U19	VCC87
U18	VCC88
U17	VCC89
U16	VCC90
U15	VCC91
U14	VCC92
U13	VCC93
U12	VCC94
U11	VCC95
U10	VCC96
U9	VCC97
U8	VCC98
U7	VCC99
U6	VCC100

CORE SUPPLY

SVID

SENSE LINES

PEG AND DDR

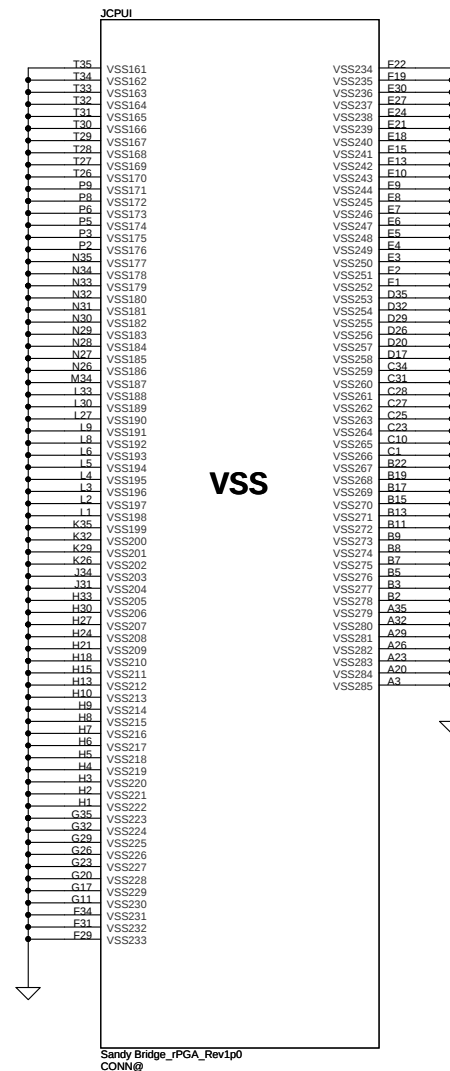
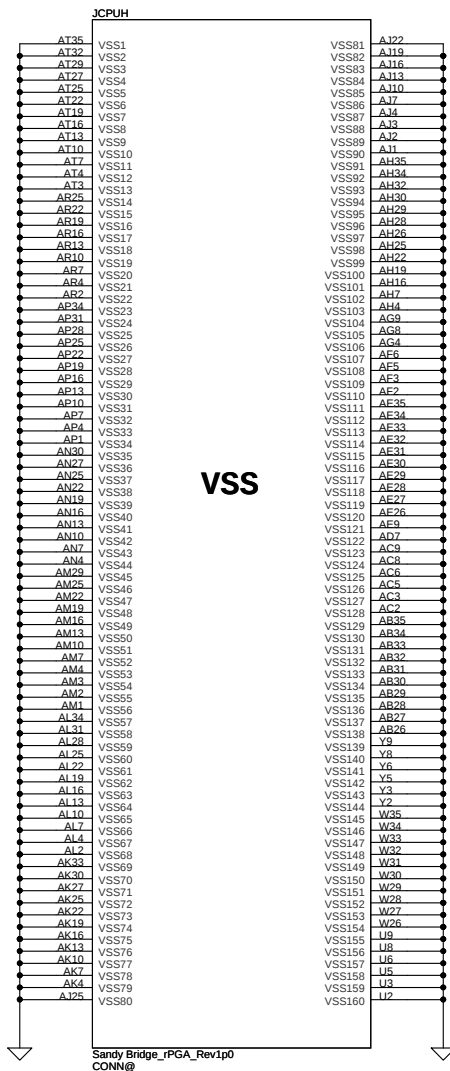


Sandy Bridge_rPGA_Rev1p0
CONV@

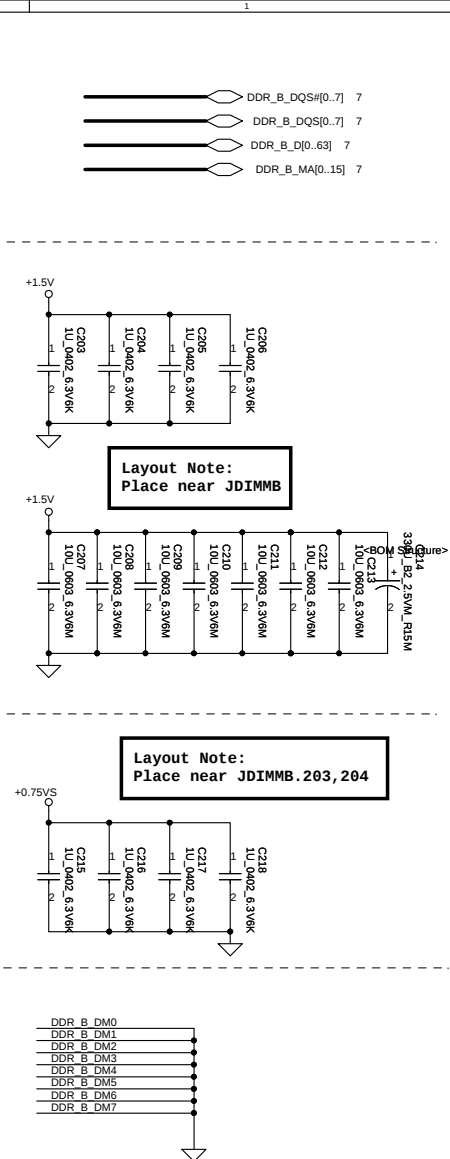
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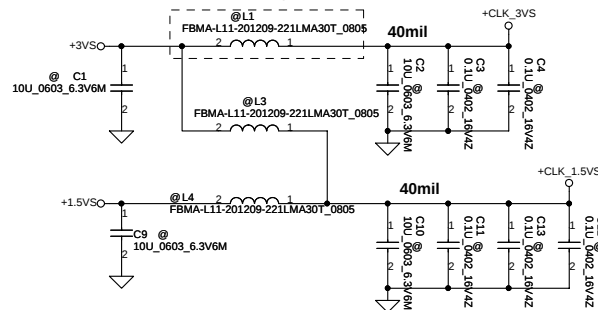


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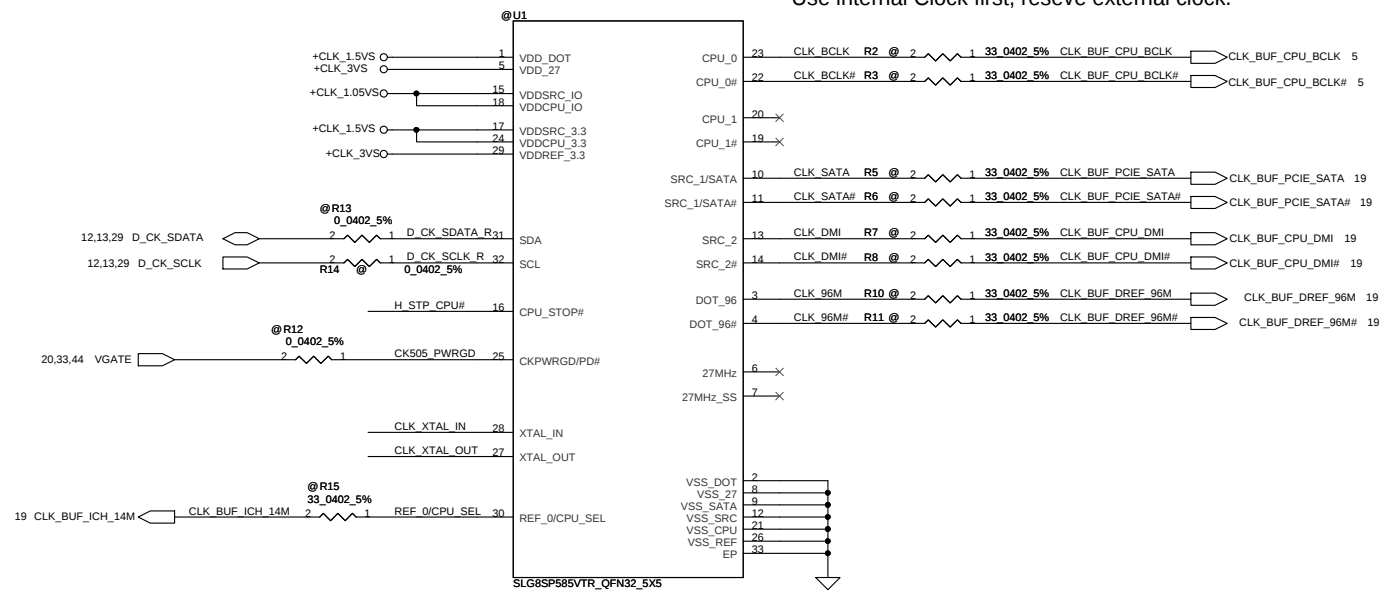


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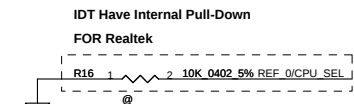
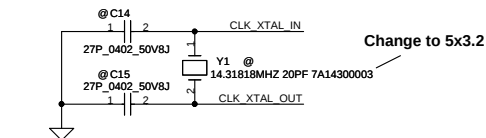
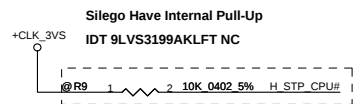
SM010014520 3000ma 220ohm@100mhz DCR 0.04



Use internal Clock first, reseve external clock.

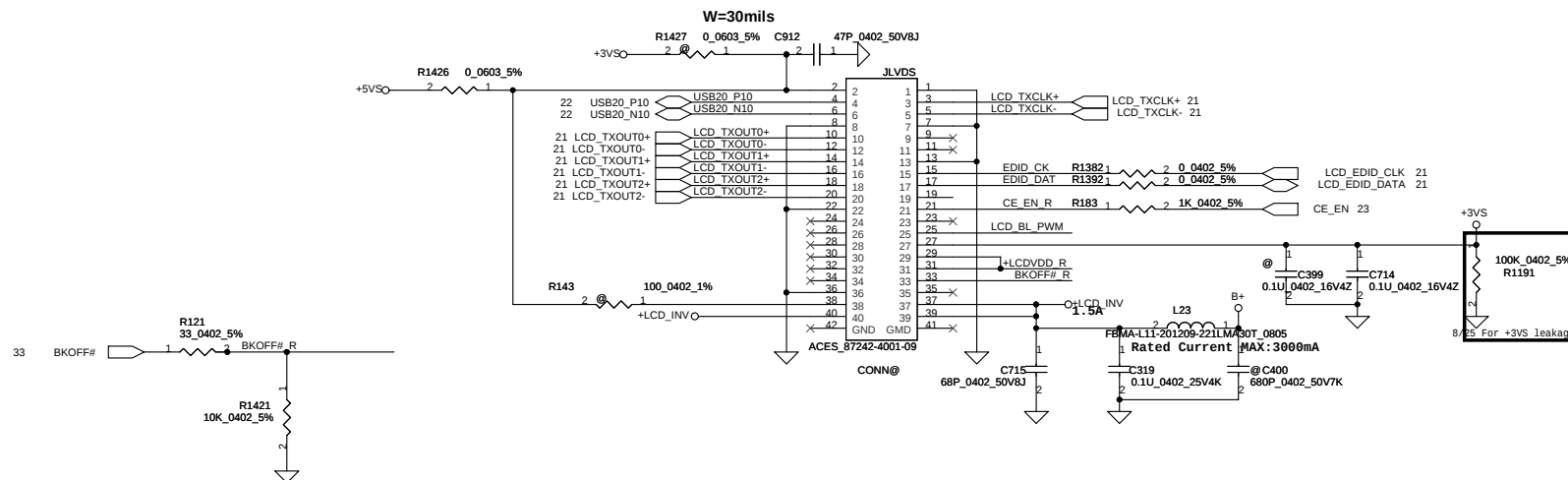
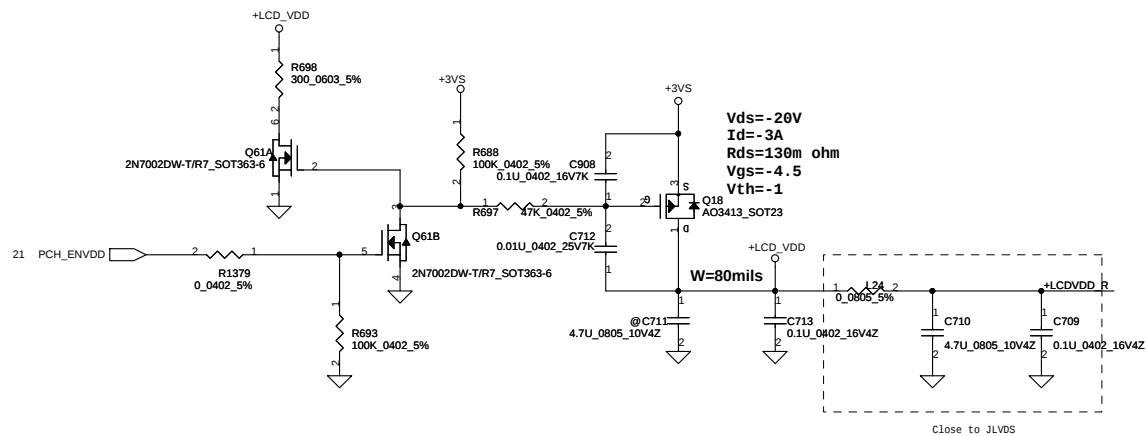


Standard
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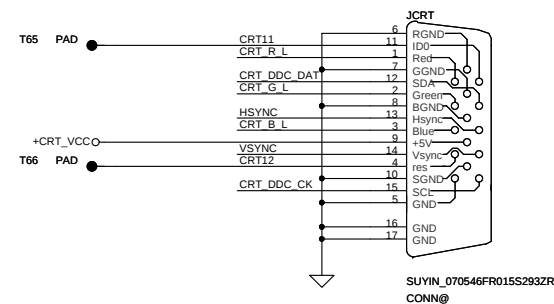
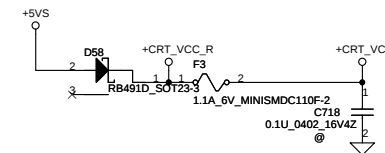
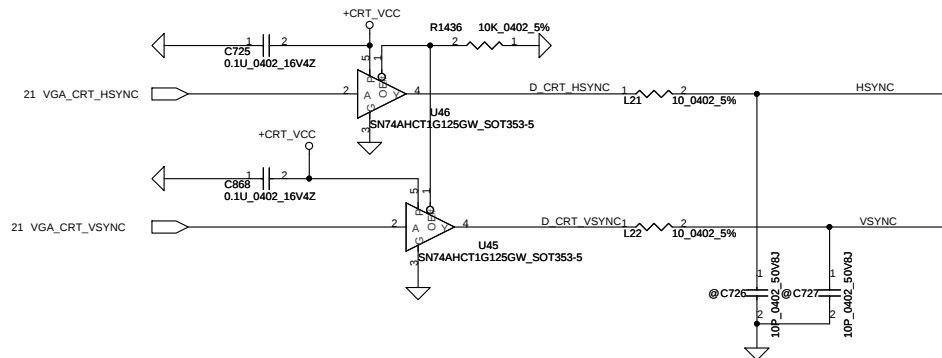
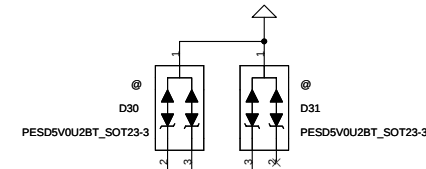
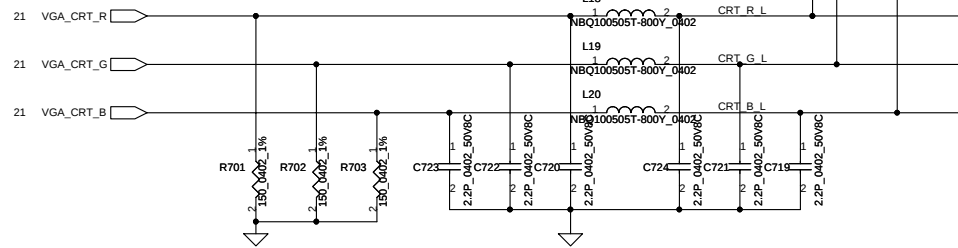
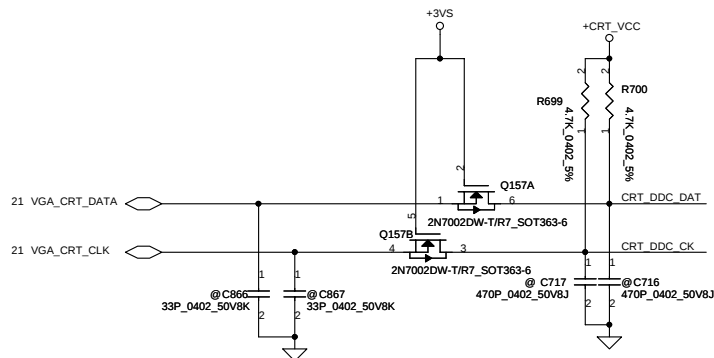


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

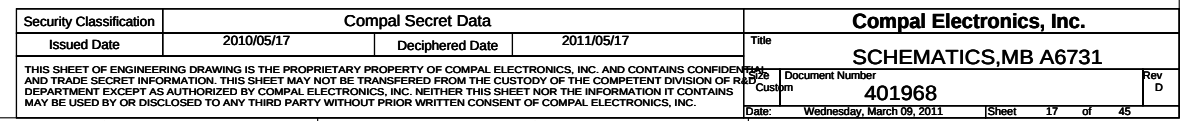
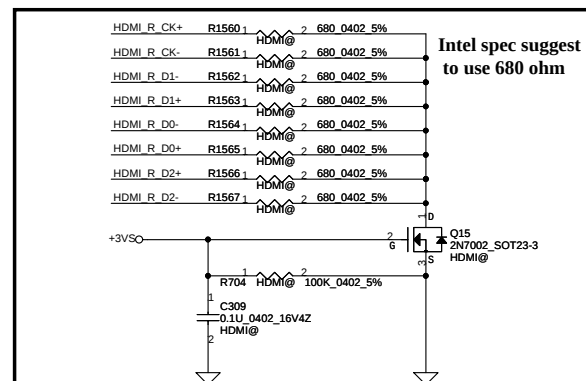
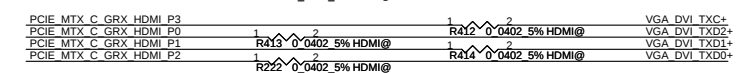
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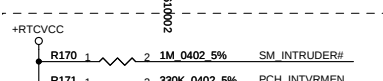
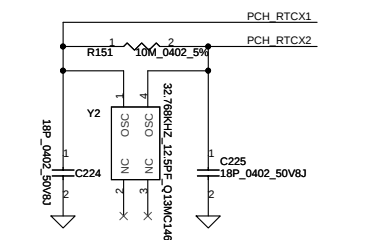


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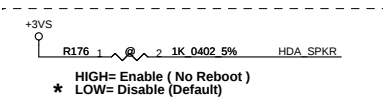


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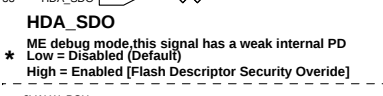




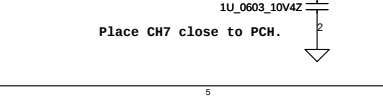
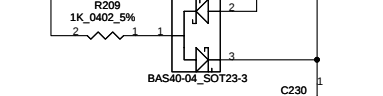
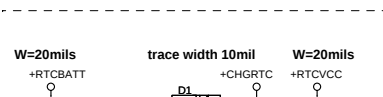
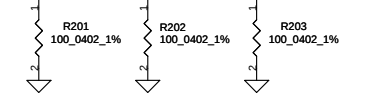
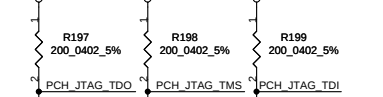
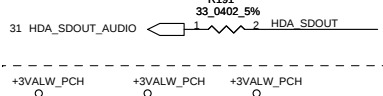
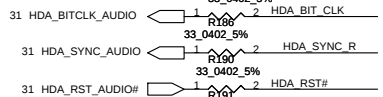
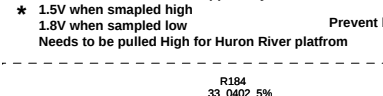
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

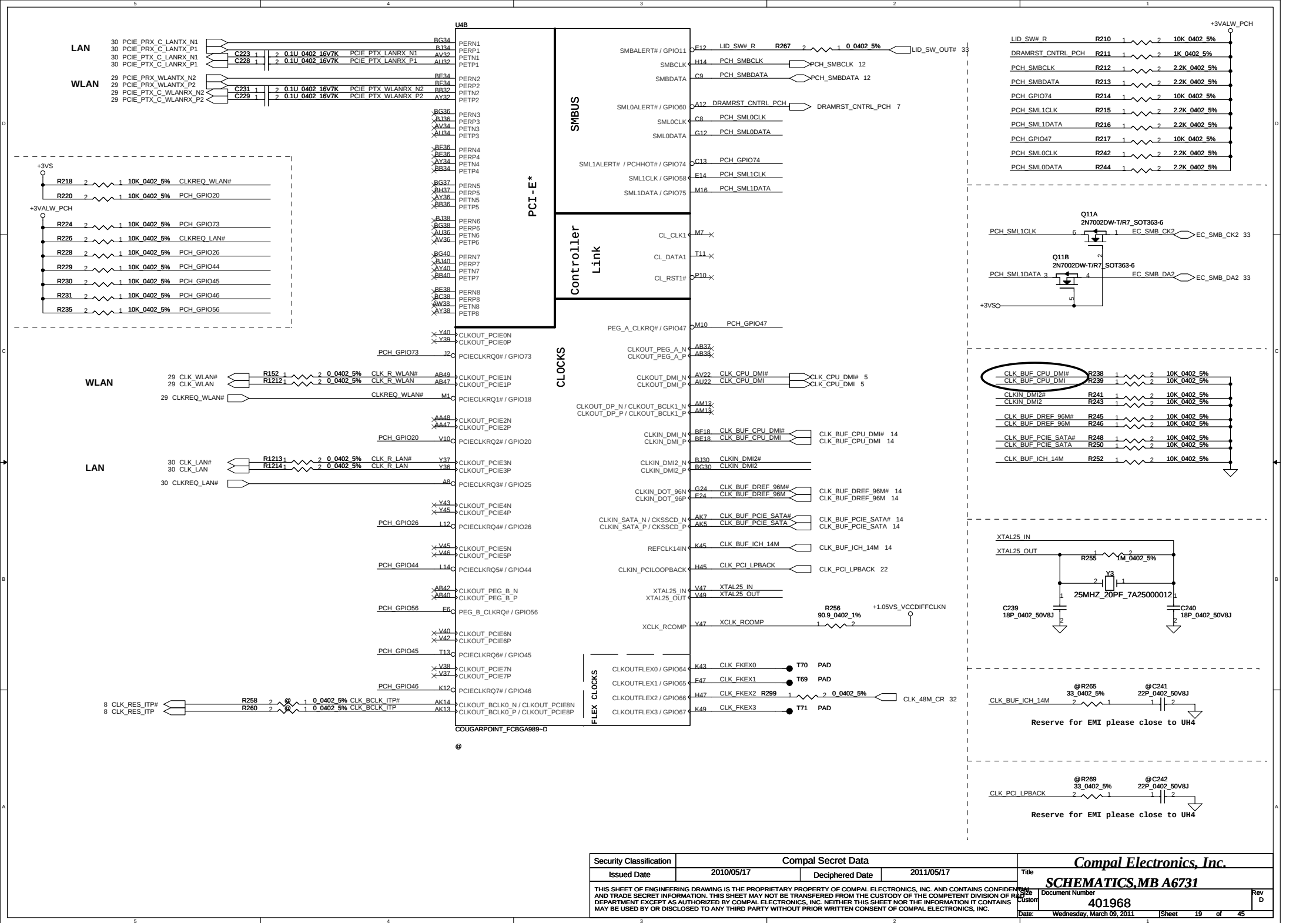


HDA_SDO
ME debug mode, this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]

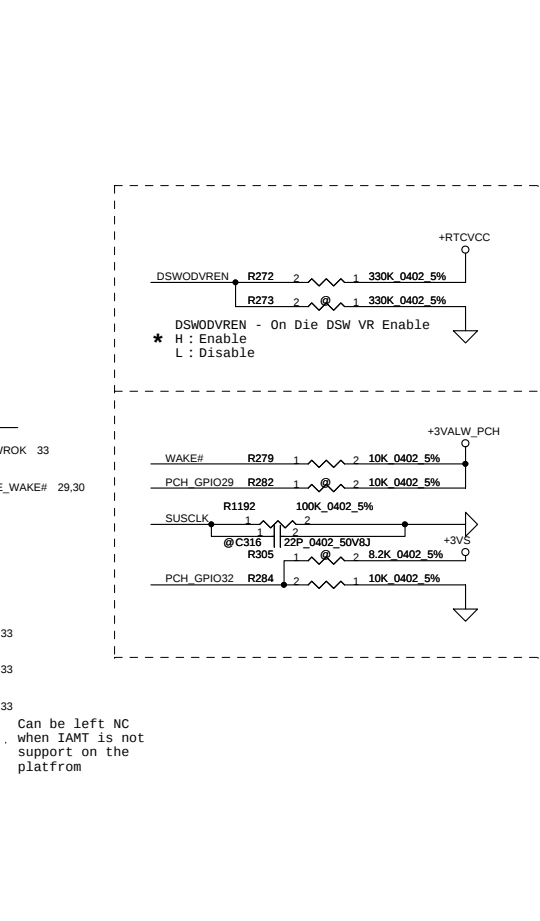
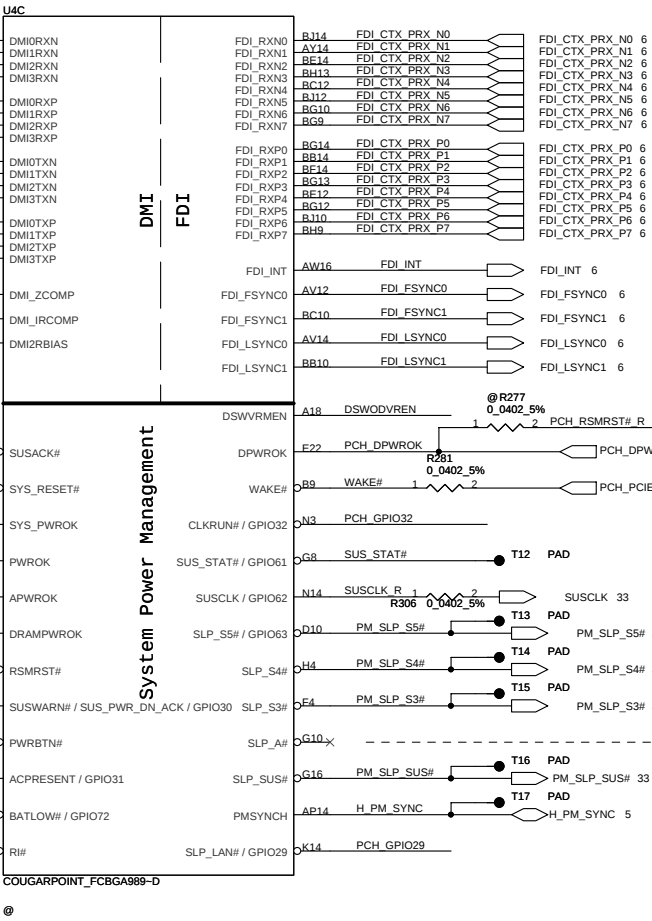
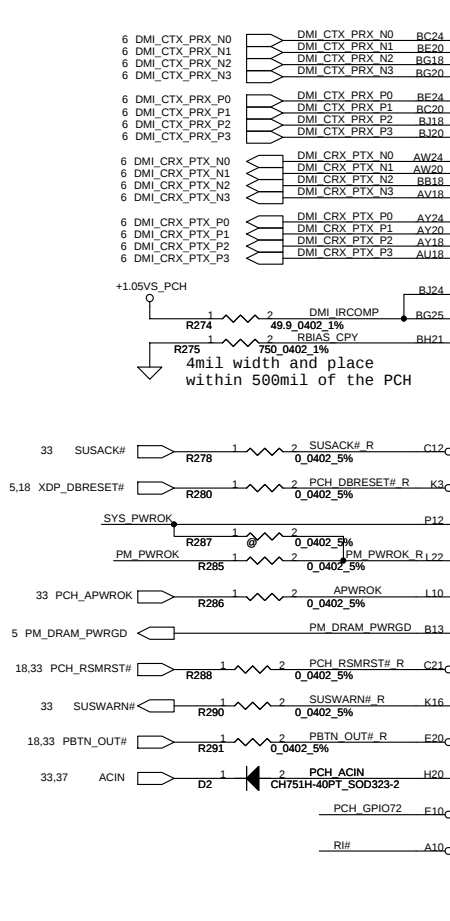
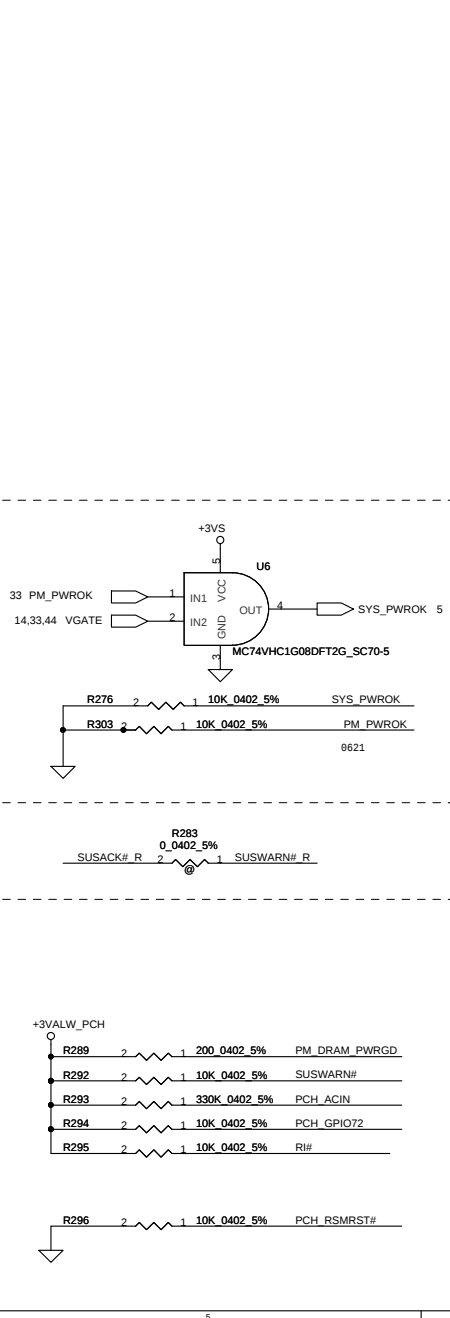


HDA_SYNC
On Die PLL VR Select is supplied by
* 1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platform

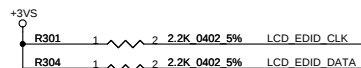
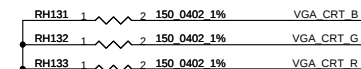
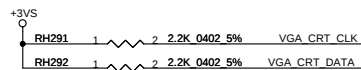
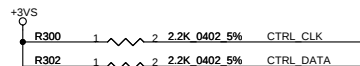
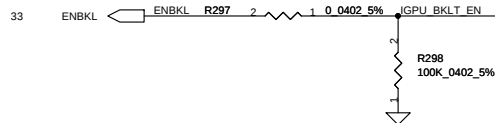




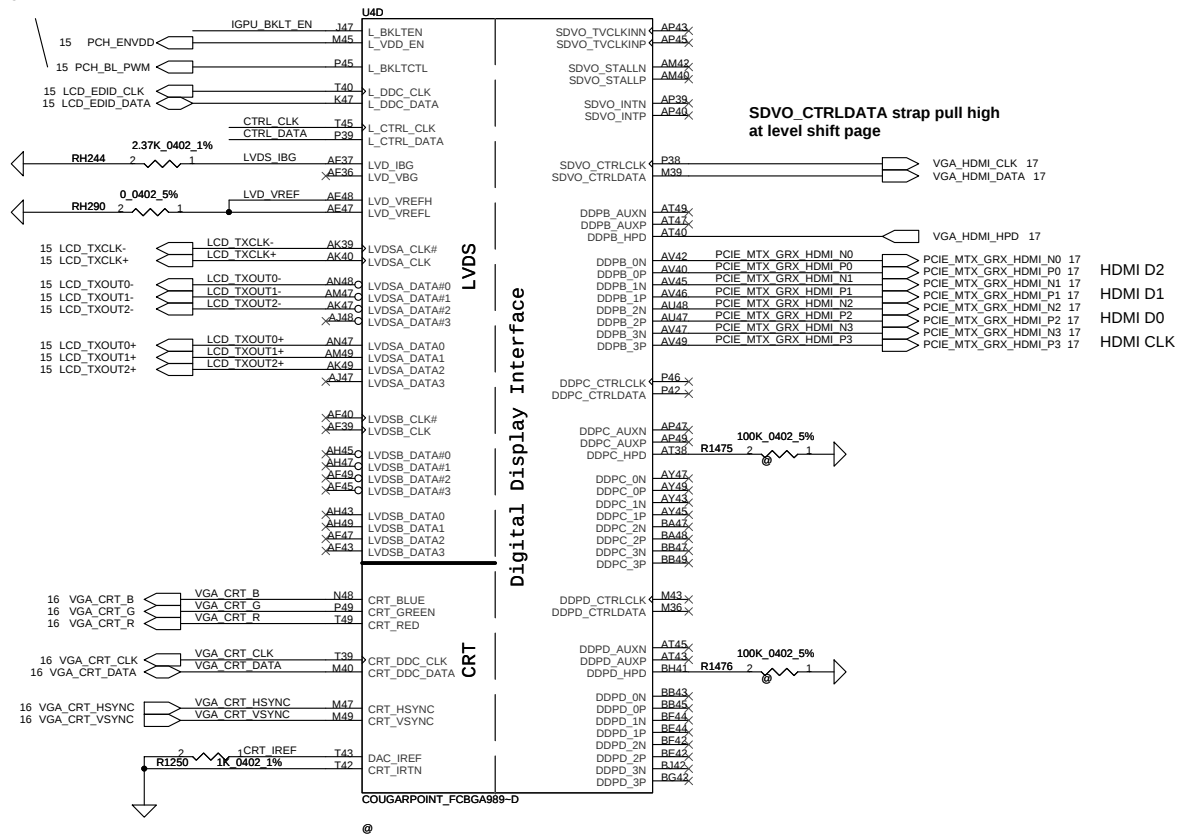
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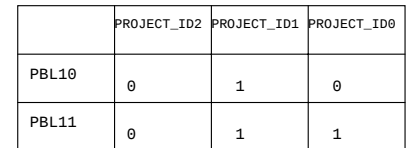
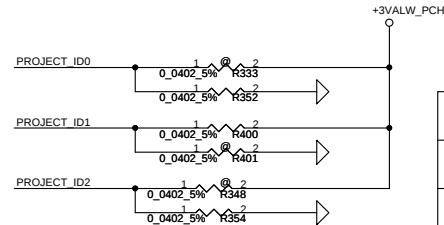
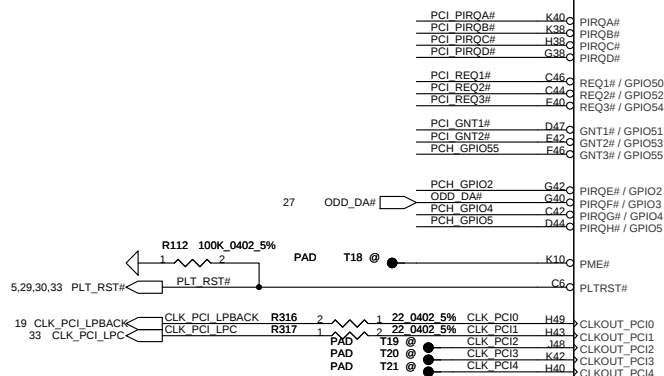
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				Date	Wednesday, March 09, 2011
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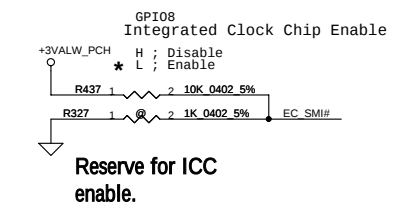
Pull high at LVDS conn side.



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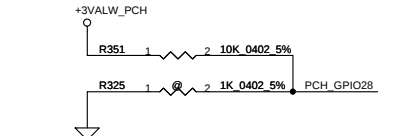
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3 1 2				Date:	Wednesday, March 09, 2011	Sheet 22 of 45



GPIO28
On-Die PLL Voltage Regulator

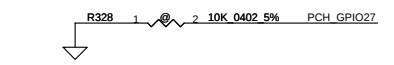
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

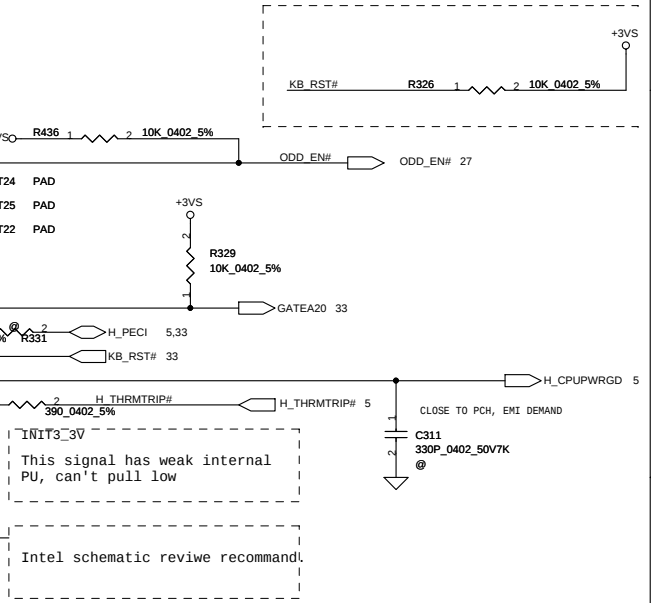
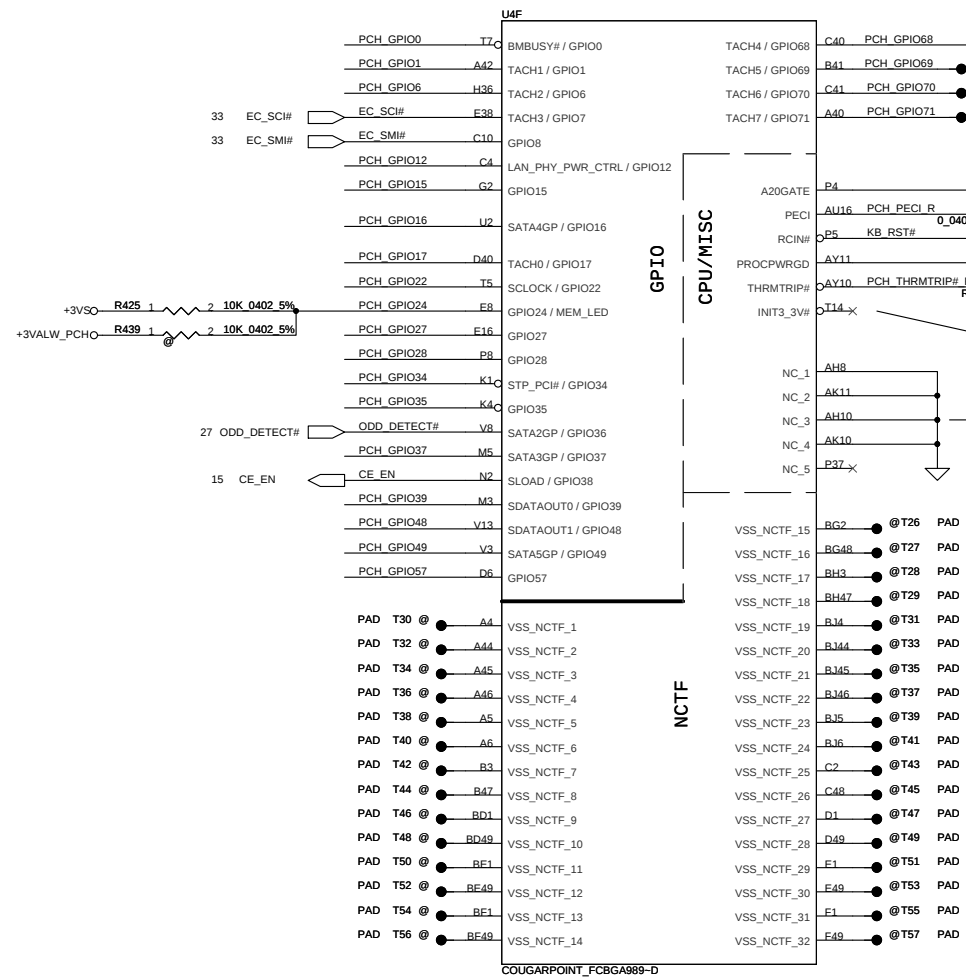
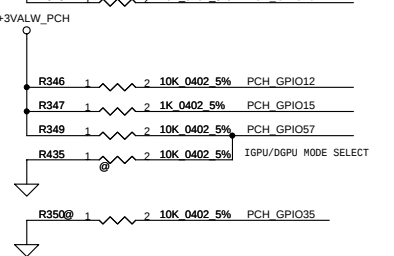
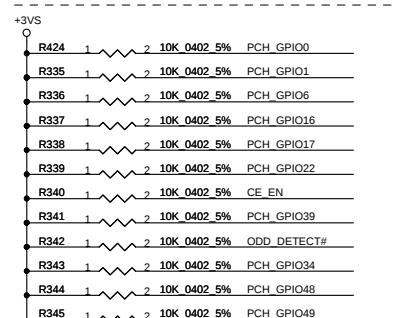
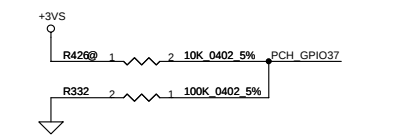


PCH_GPIO27 (Have internal Pull-High)

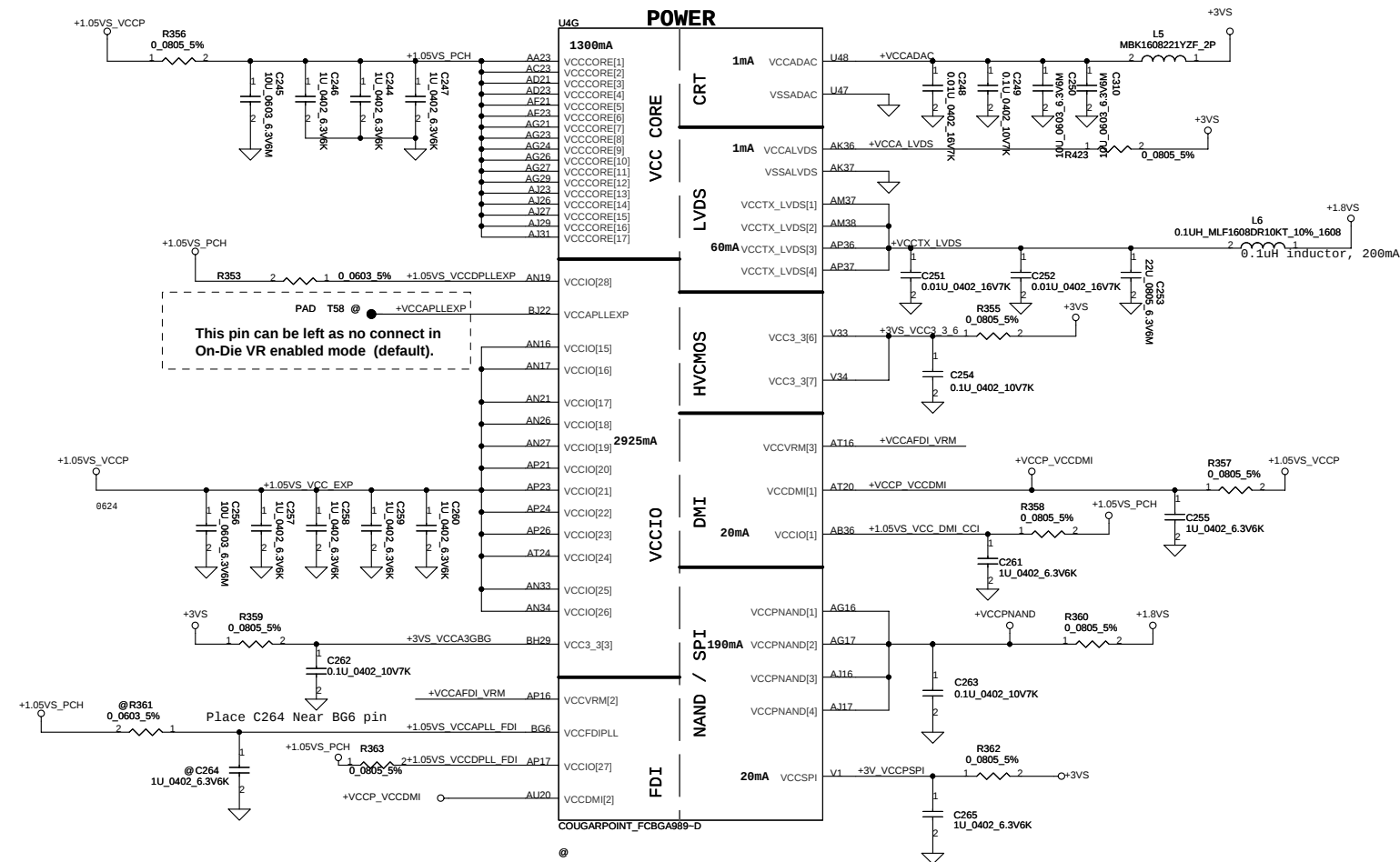
*High: VCCVRM VR Enable
Low: VCCVRM VR Disable



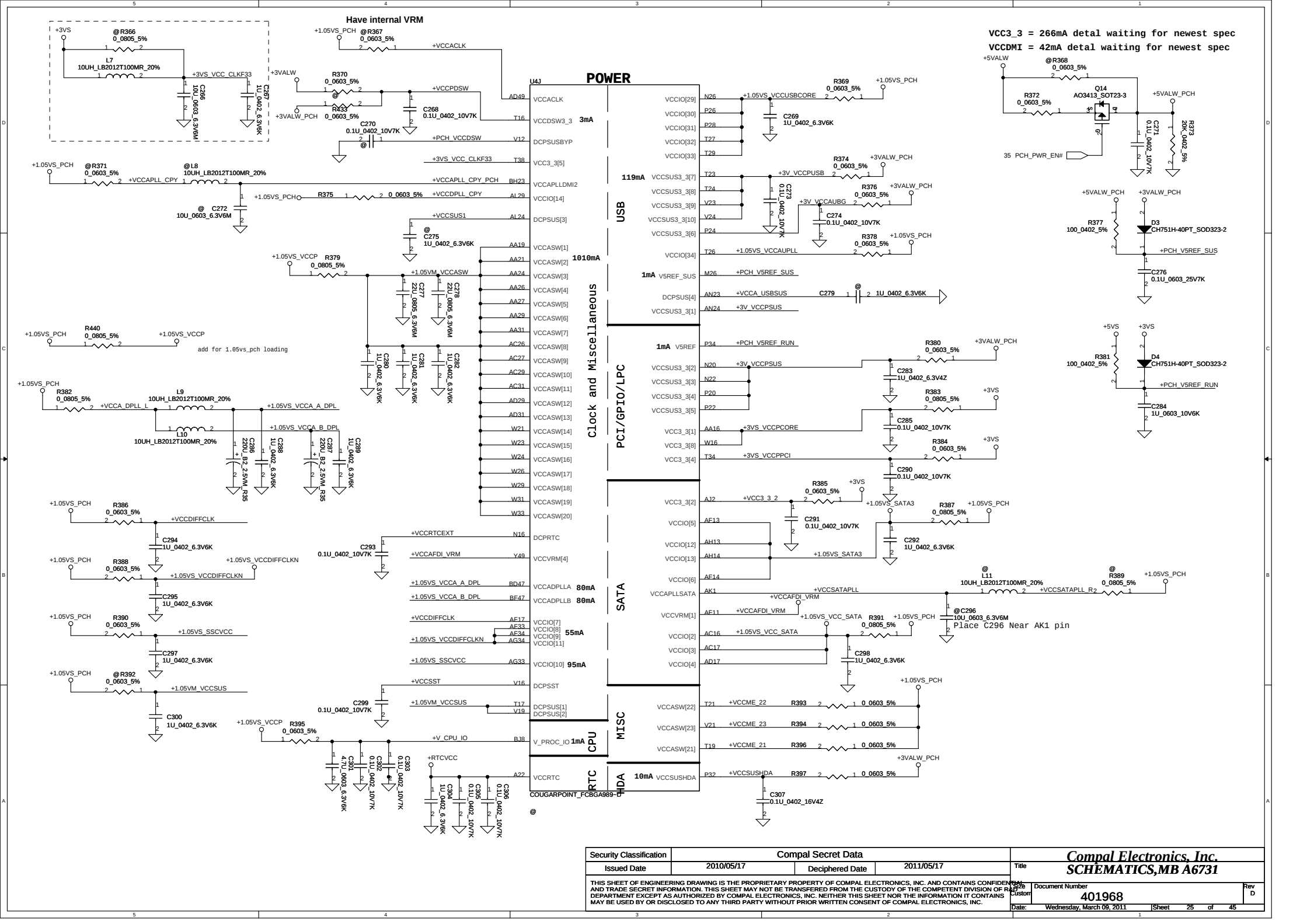
PCH_GPIO37

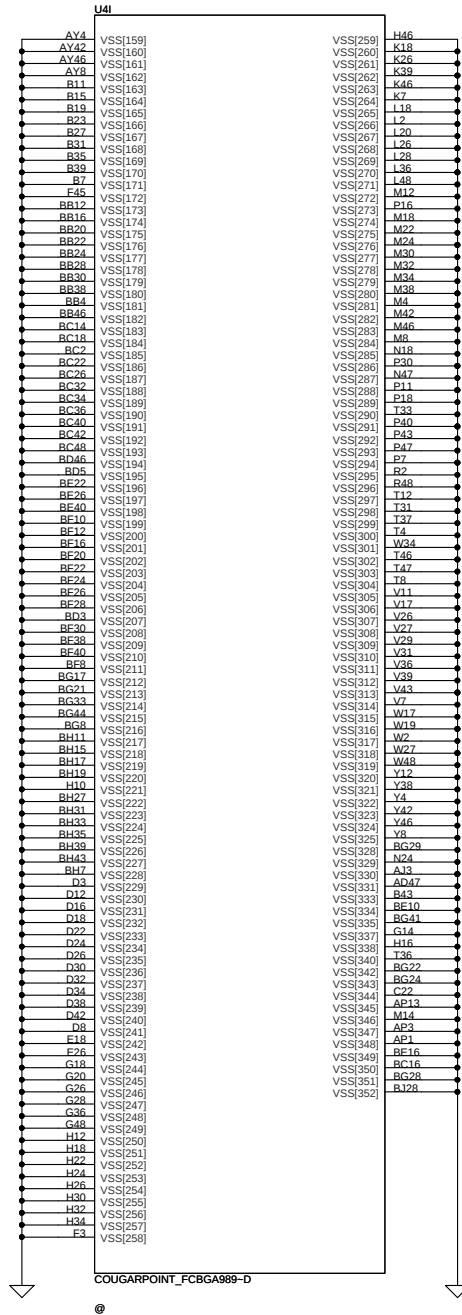
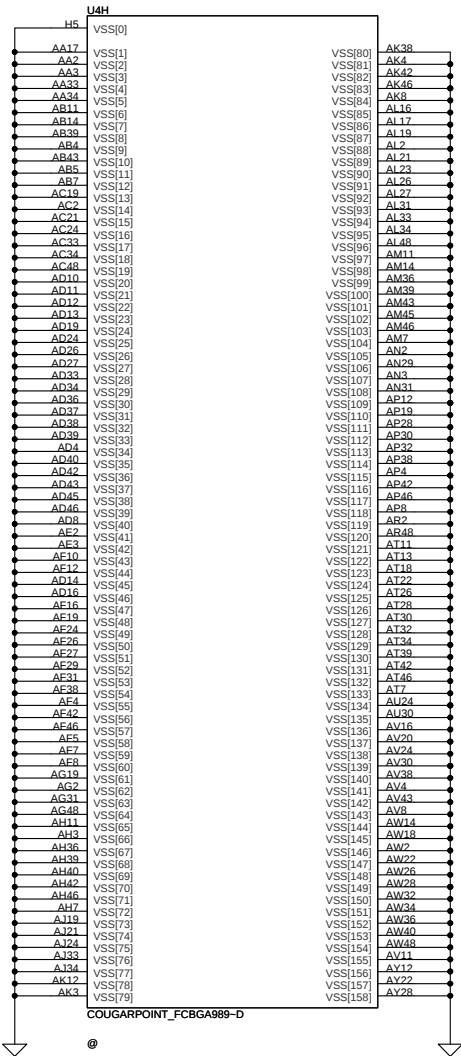


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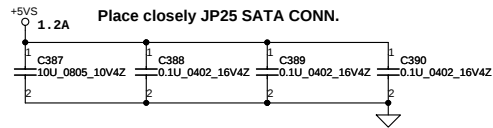
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROG_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



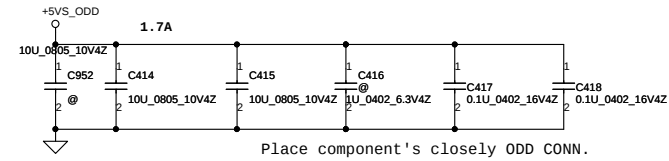


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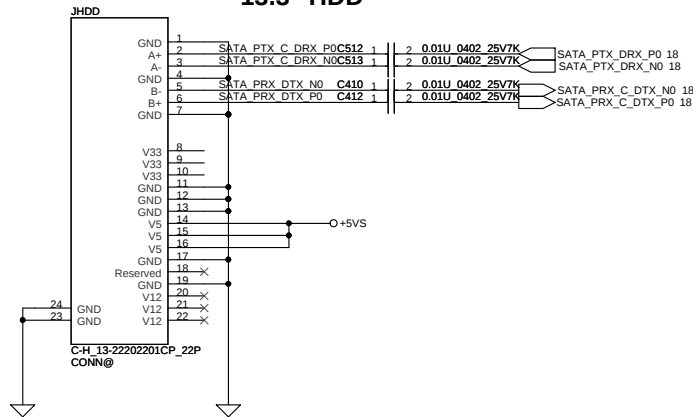
SATA HDD1 Conn.



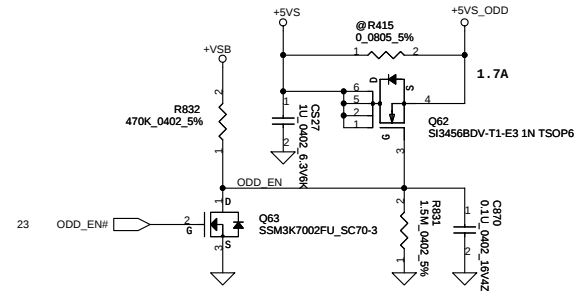
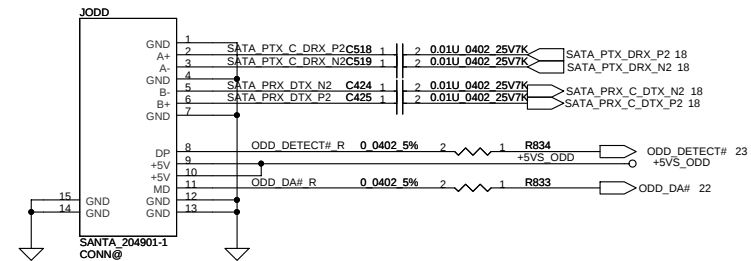
SATA ODD Conn



13.3" HDD

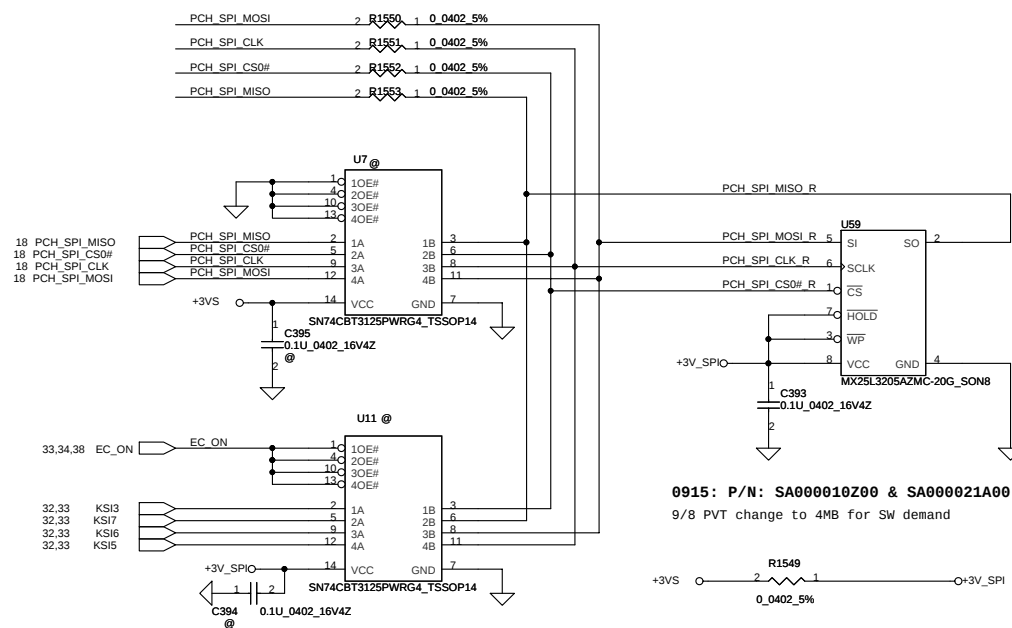
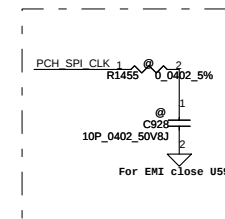
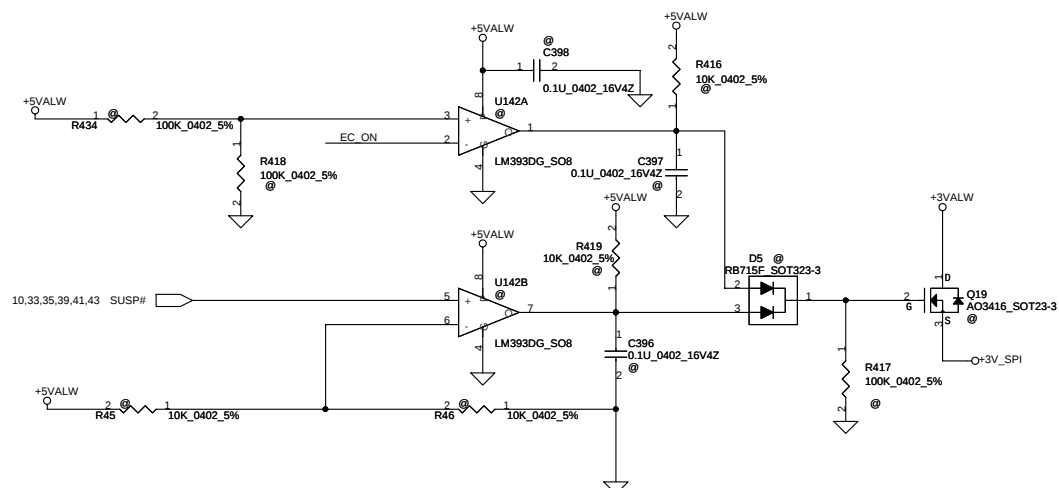


13.3" ODD



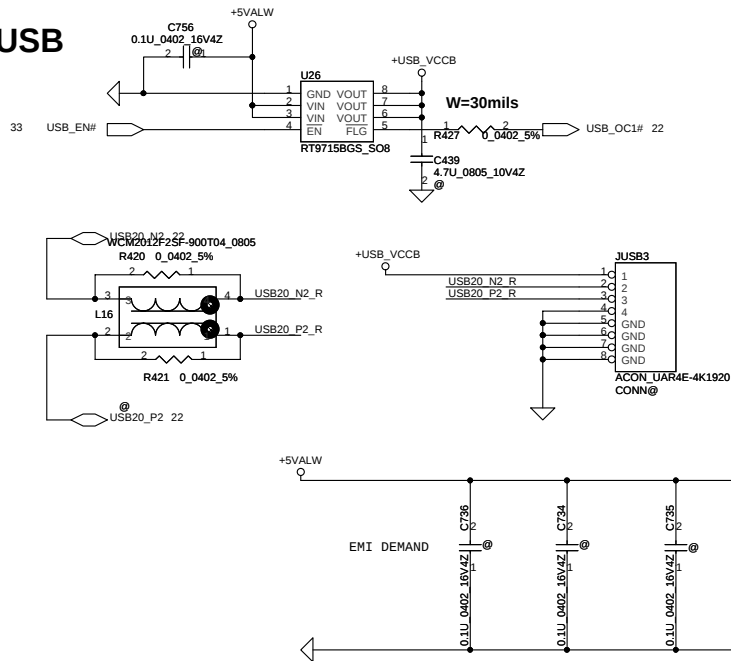
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**SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte**

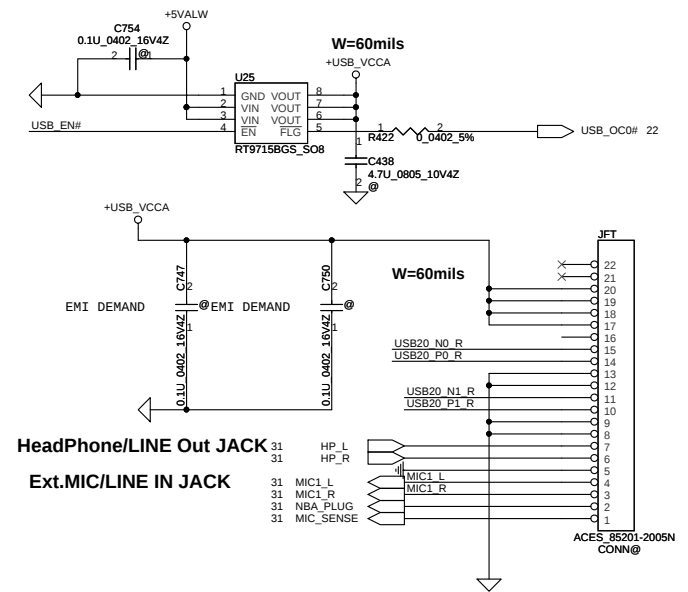
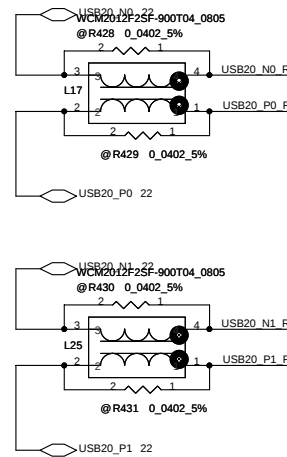


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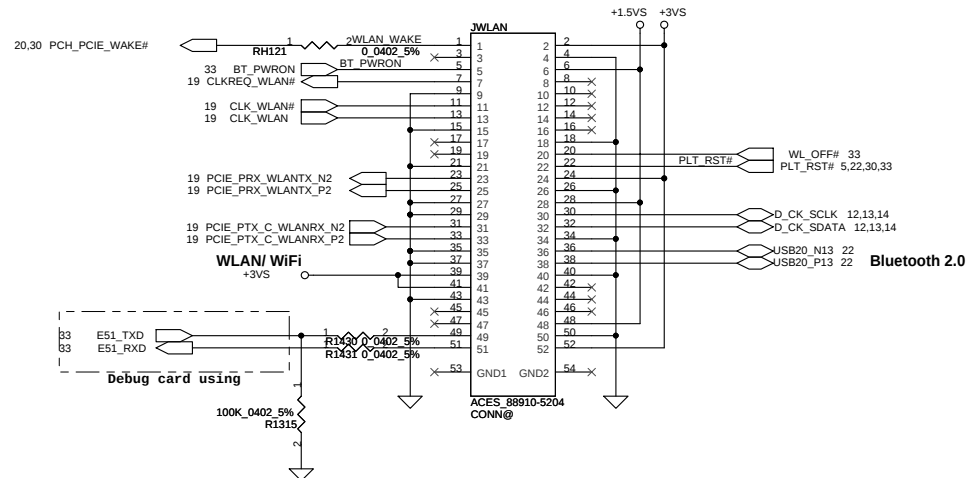
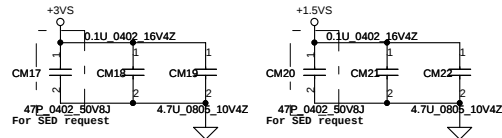
Left USB



Function Board

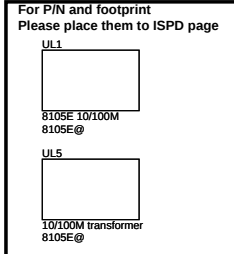
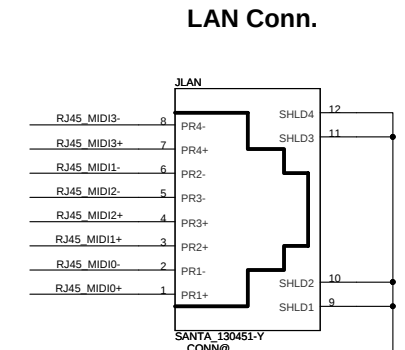
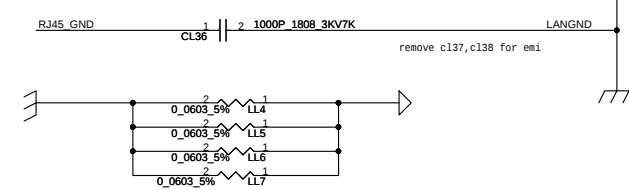
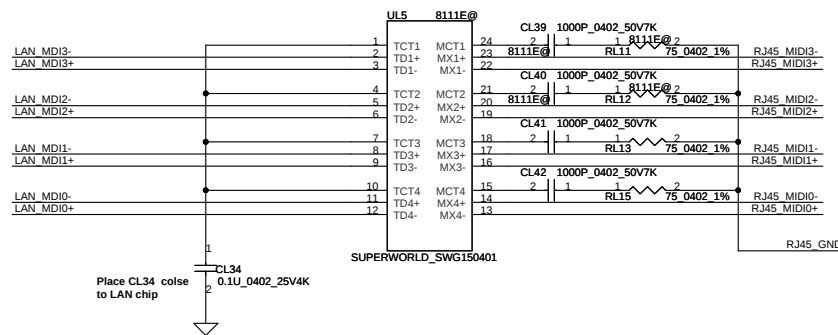
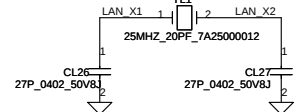
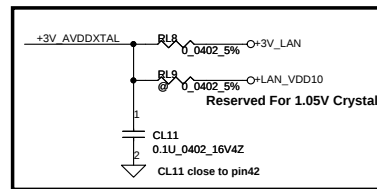
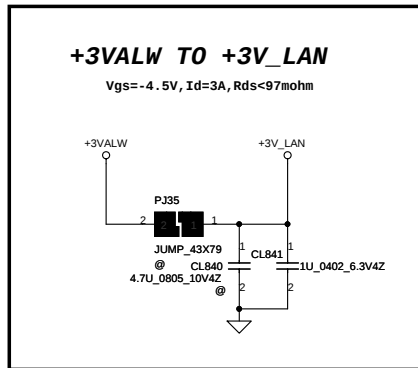
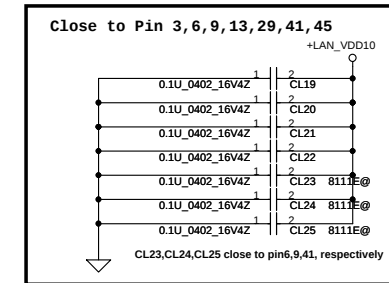
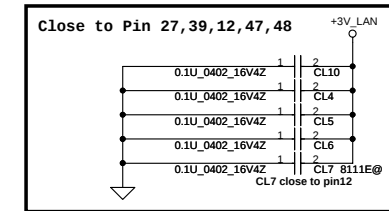
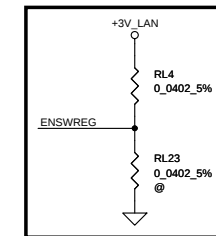
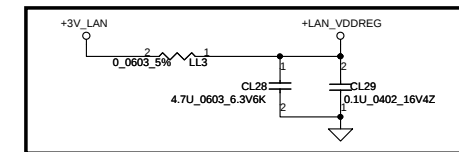
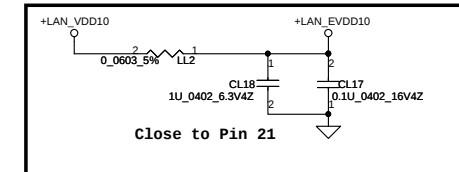
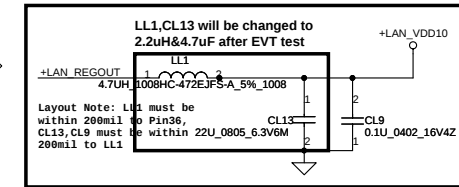
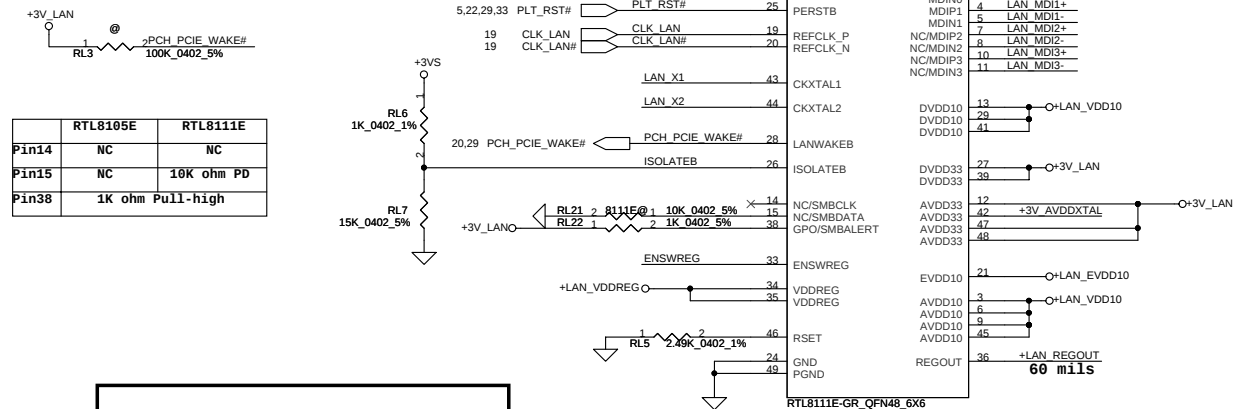


Slot 1 Half PCIe Mini Card-WLAN & BT2.0

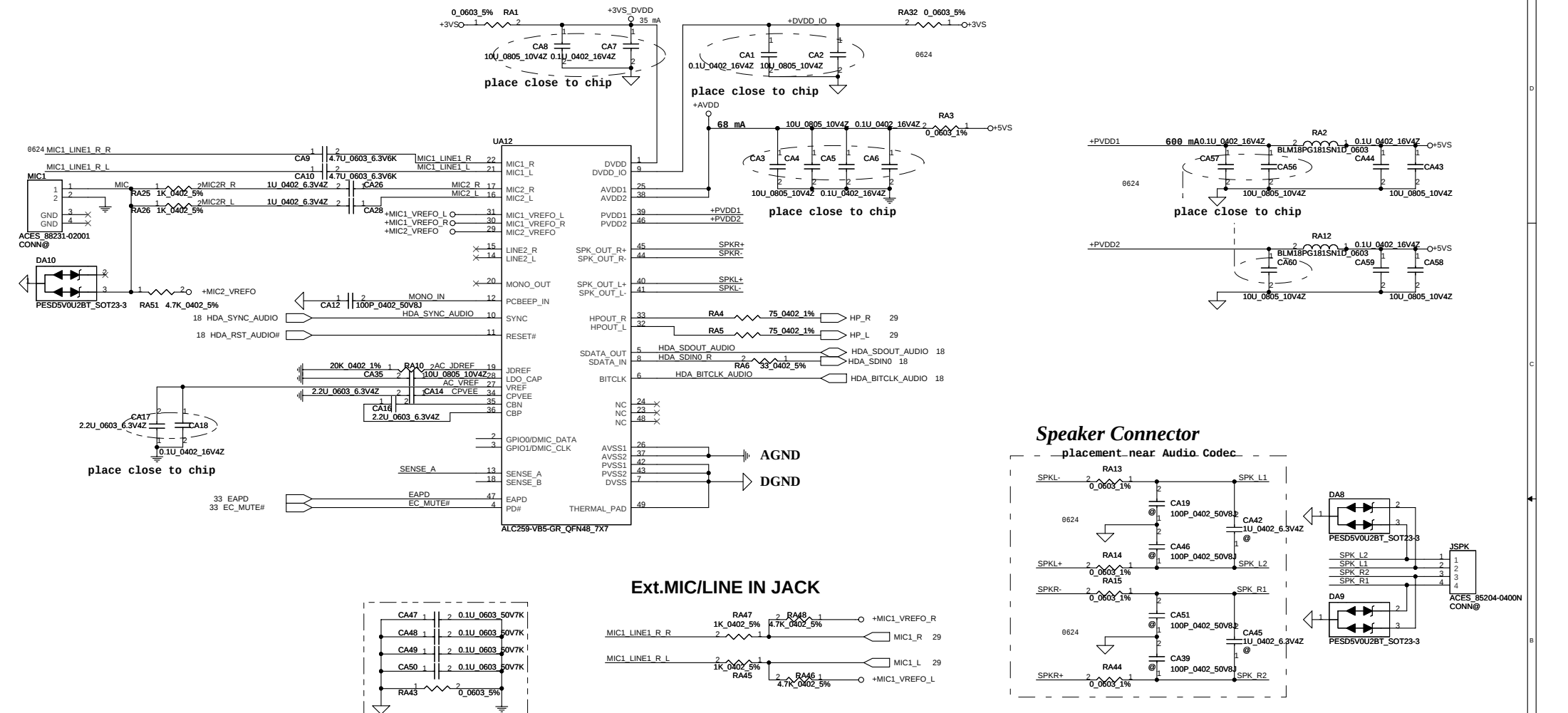


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				Revision				401968			
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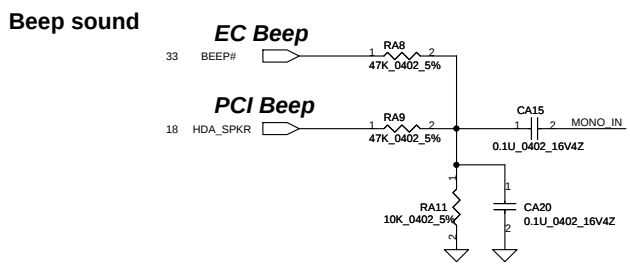
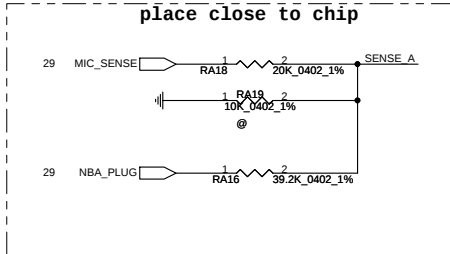
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



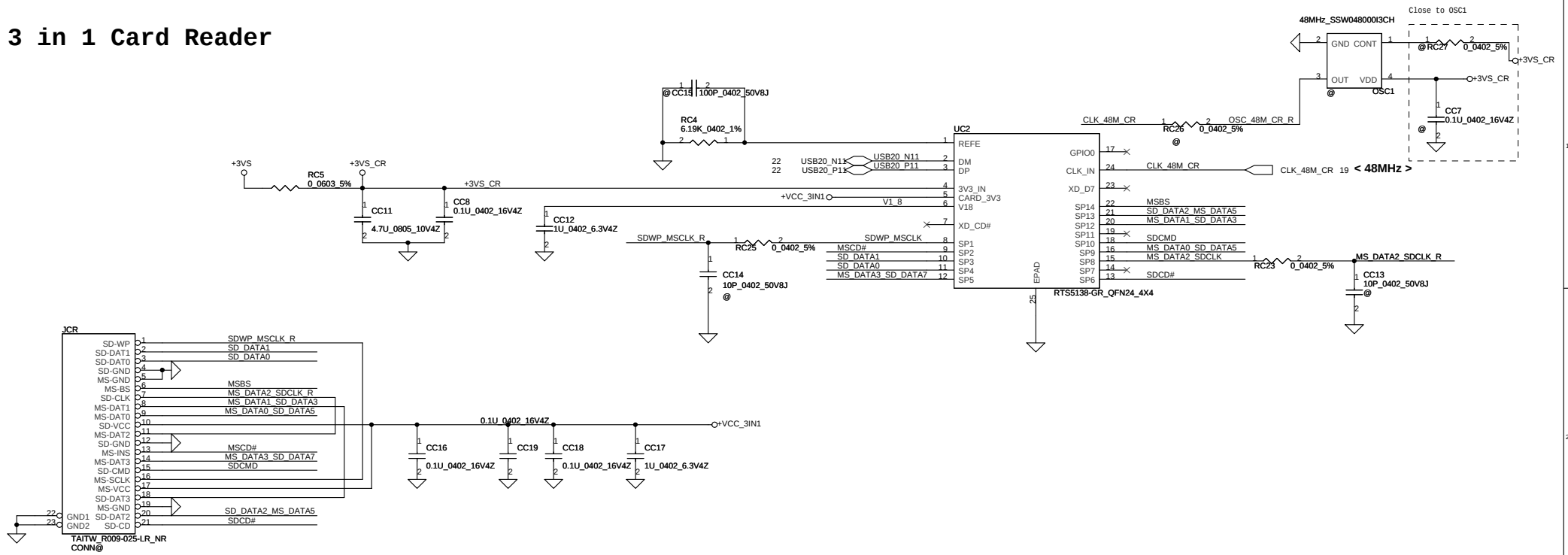
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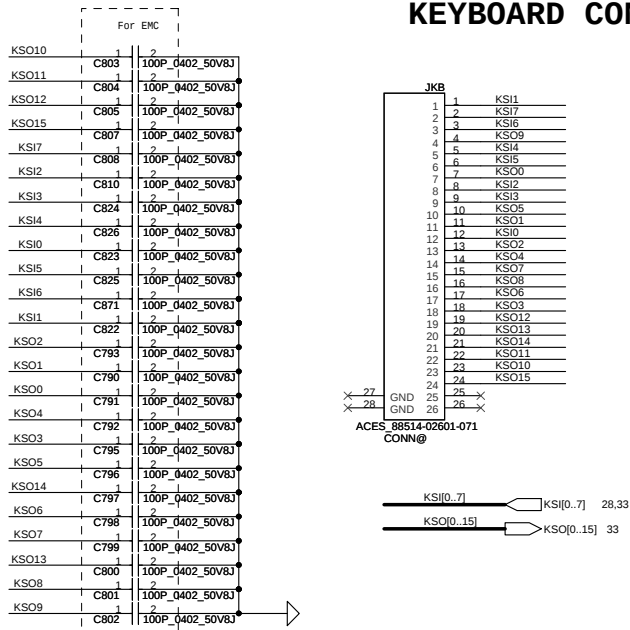
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



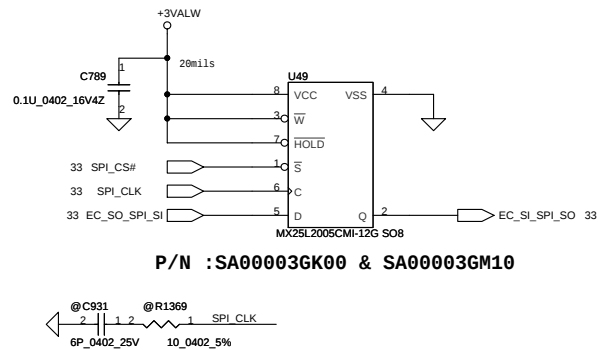
3 in 1 Card Reader



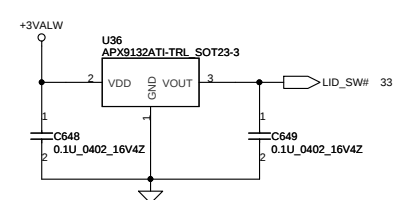
KEYBOARD CONN.



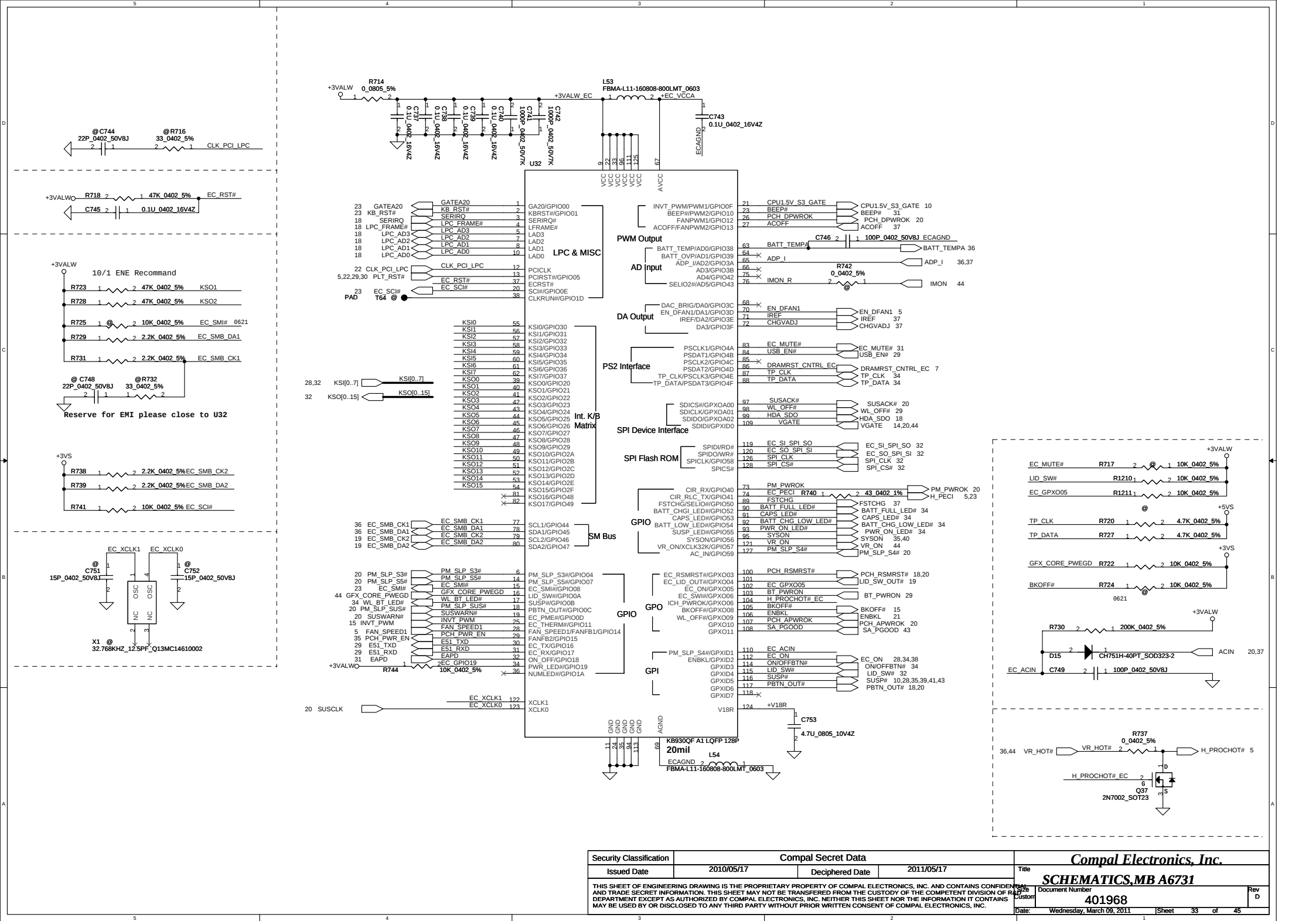
SPI Flash (1MByte*1)



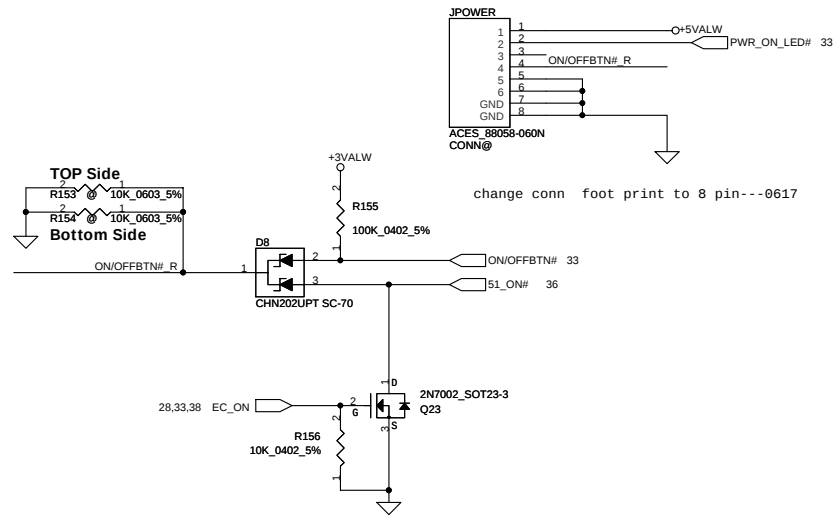
Lid SW



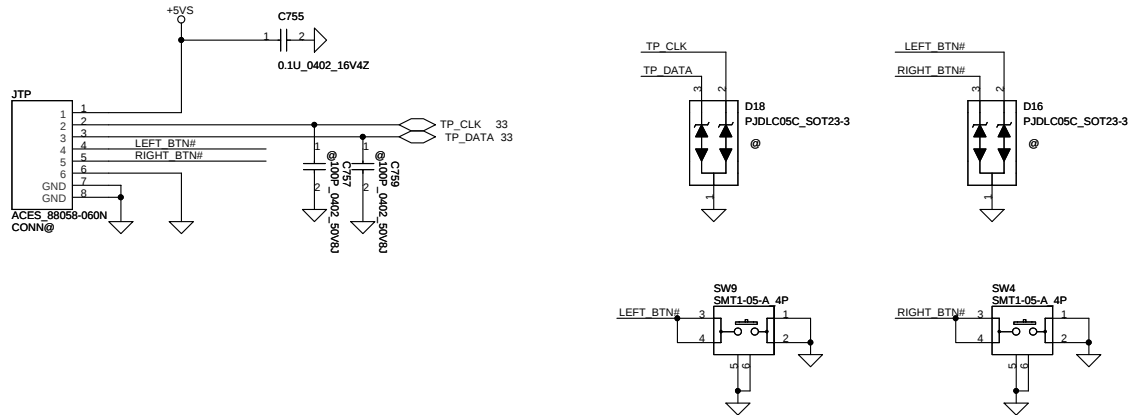
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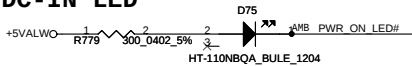
Power Button/ PWR/B



Touch/B Connector



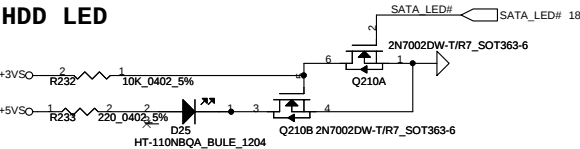
DC-IN LED



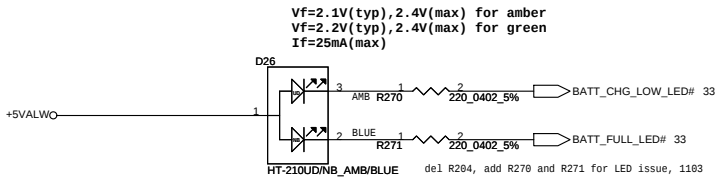
WL&BT LED



HDD LED



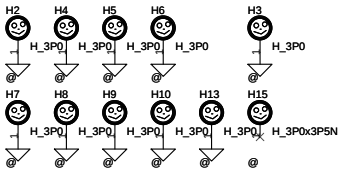
BATT CHARGE/FULL LED



CAP LOCK LED



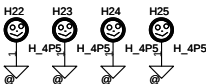
Screw Hole



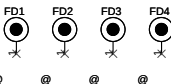
JWLAN



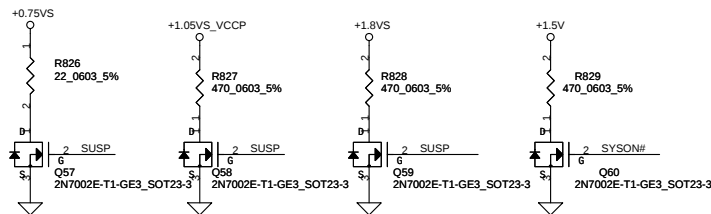
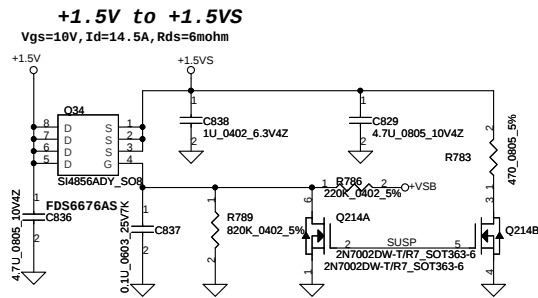
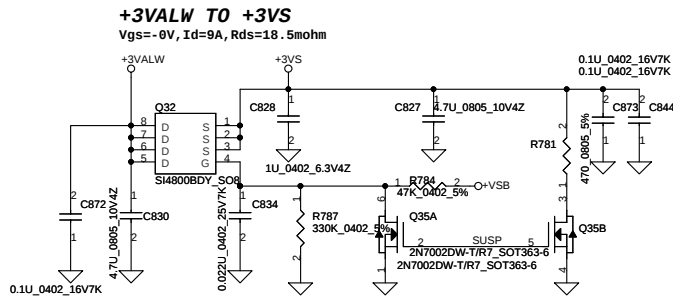
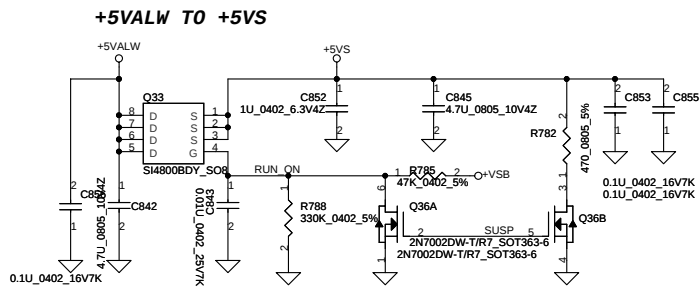
CPU



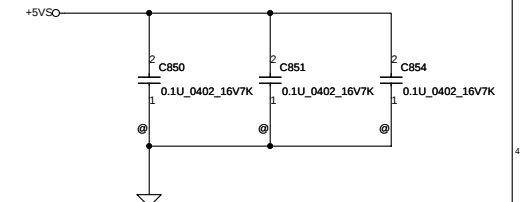
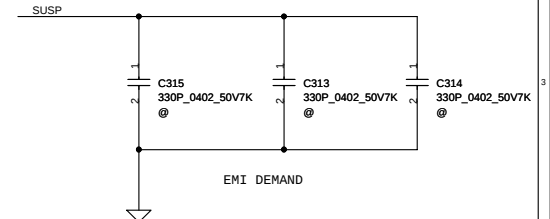
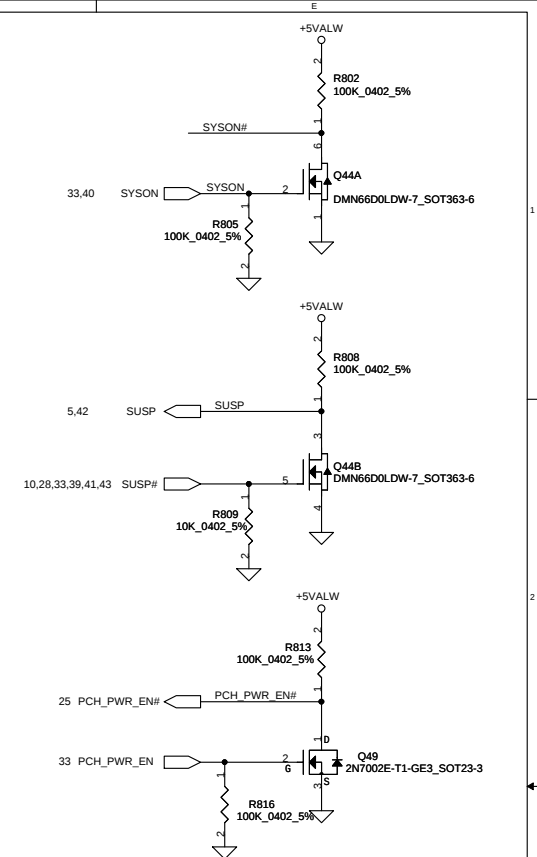
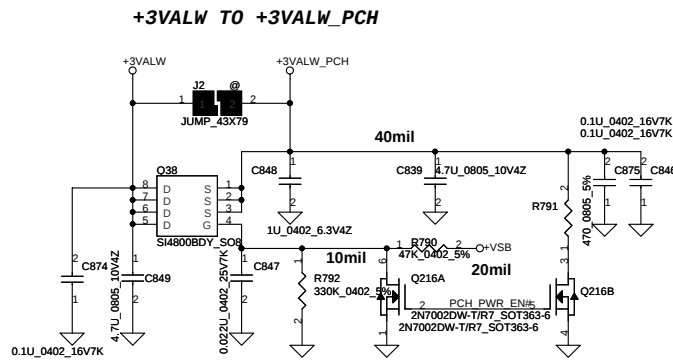
PCB Fedical Mark PAD



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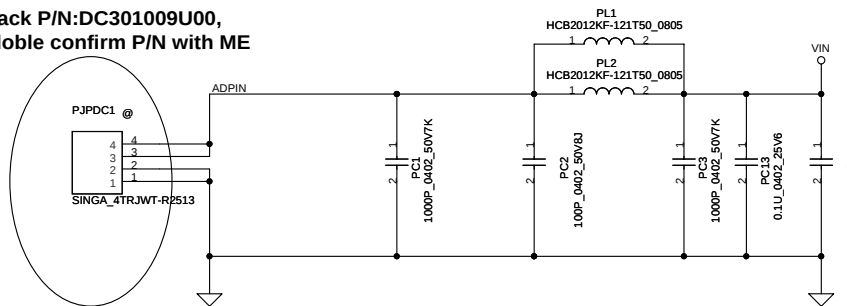


2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

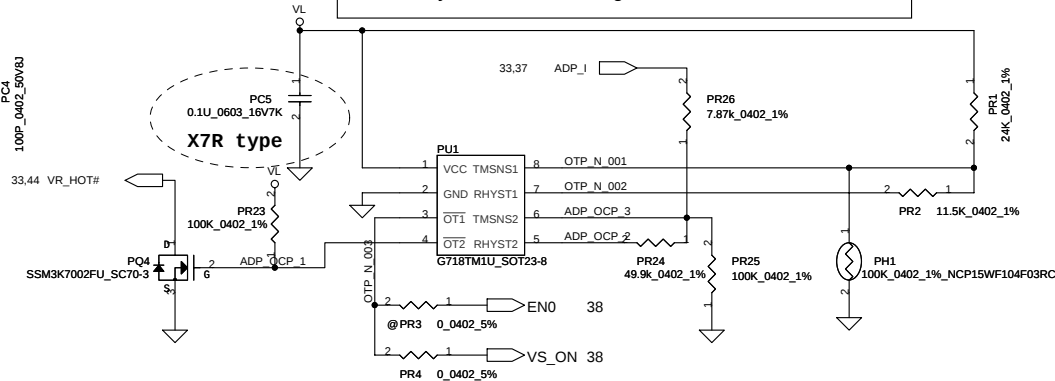


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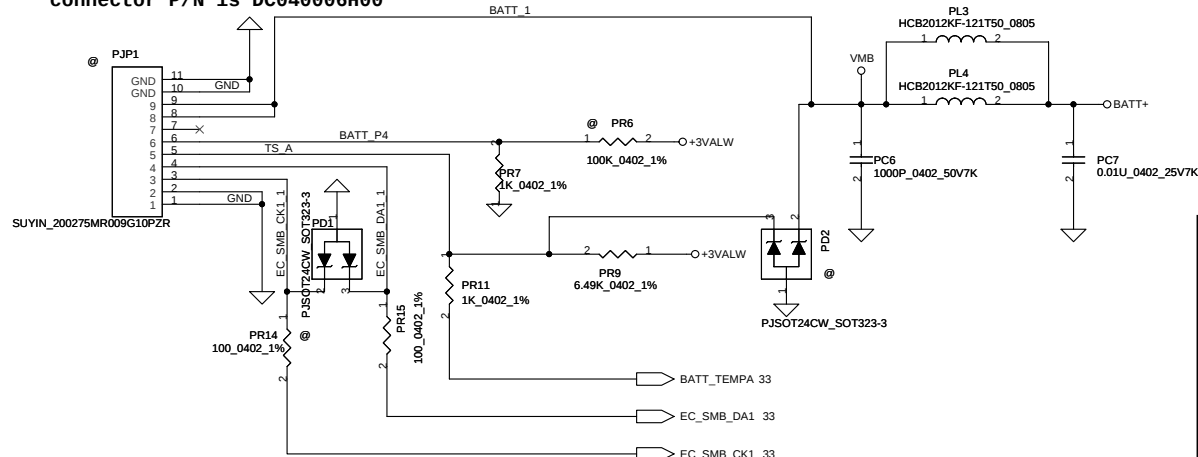
DCIN jack P/N:DC301009U00,
need doble confirm P/N with ME



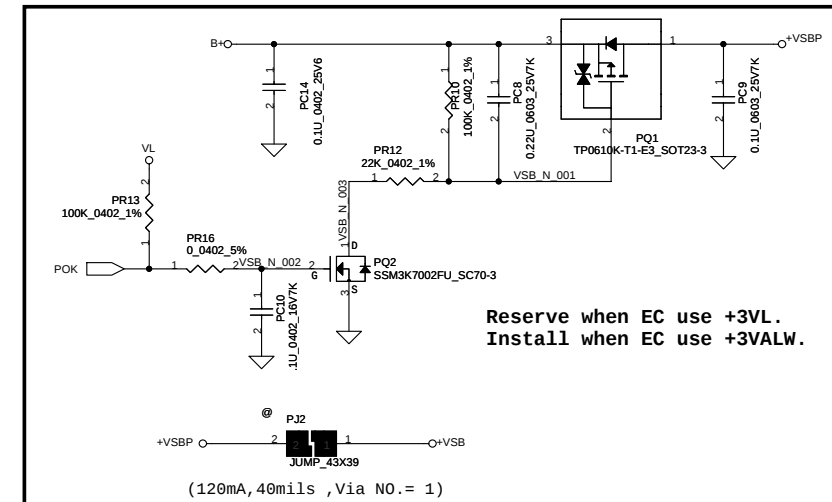
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



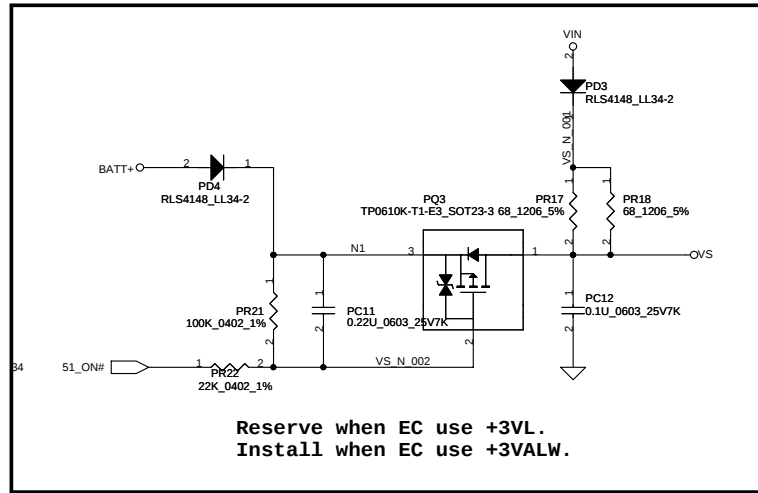
need confirm: ME give us battery
connector P/N is DC040006H00



If EC use 3VL and can not detect VGATE,
must connect EN0

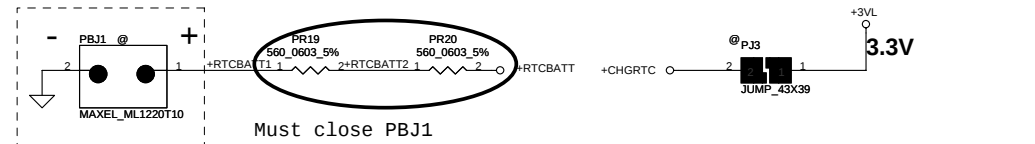


Reserve when EC use +3VL.
Install when EC use +3VALW.



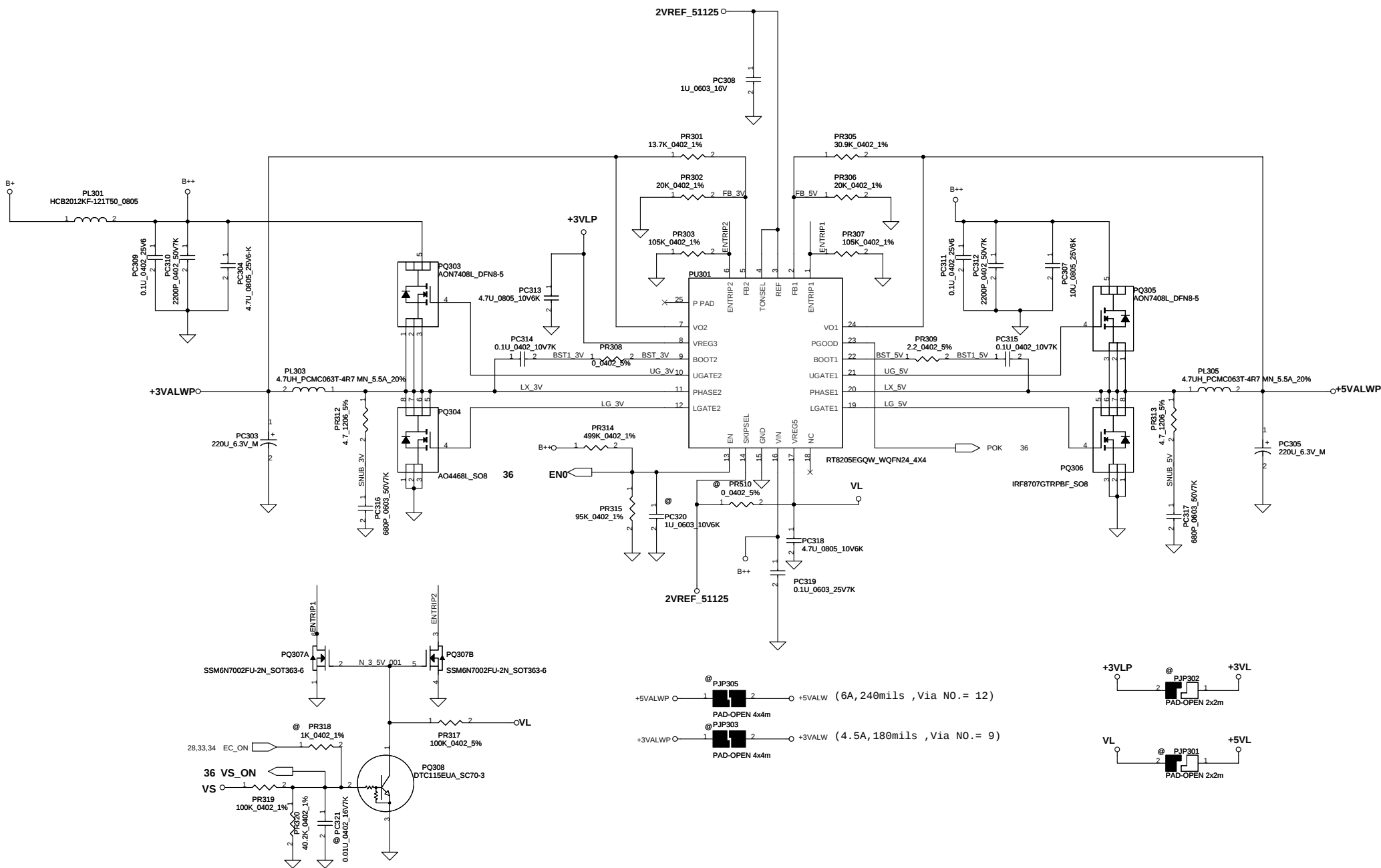
Reserve when EC use +3VL.
Install when EC use +3VALW.

RTC Battery



SP093MX0000

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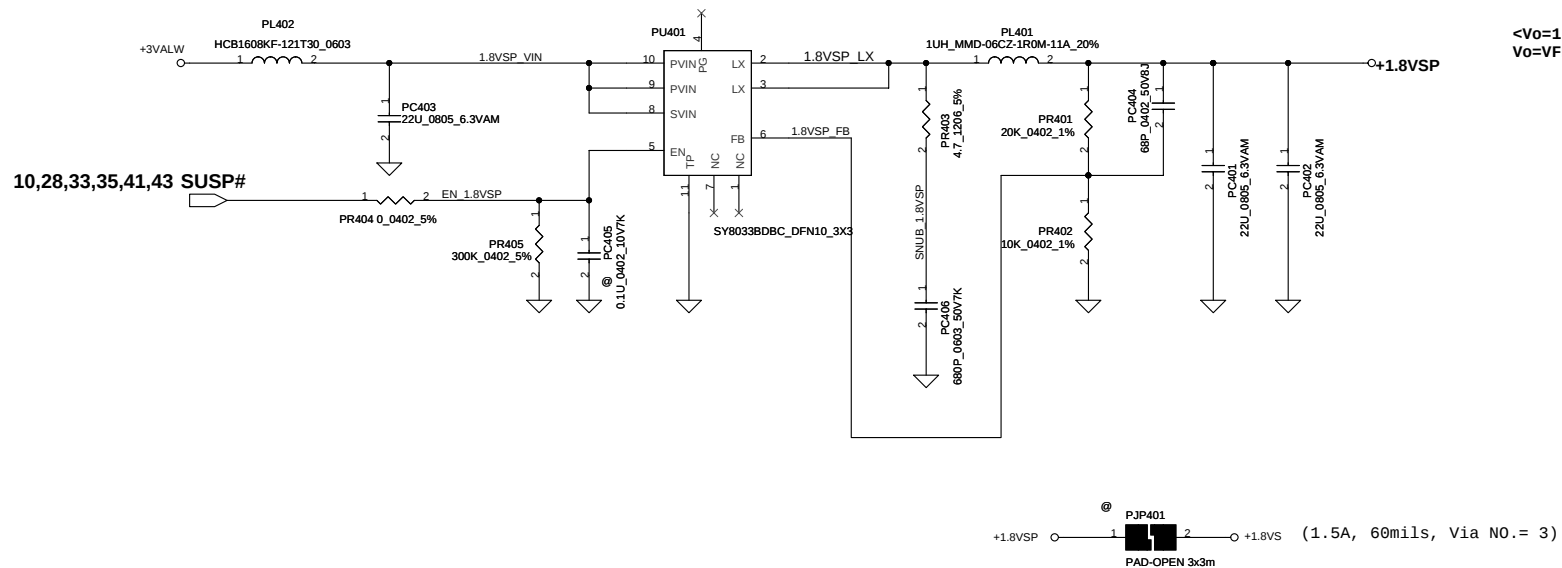


EC:+3VL, reserve PR319, install PR318, PR320 100K
 EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

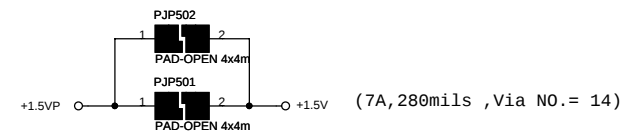
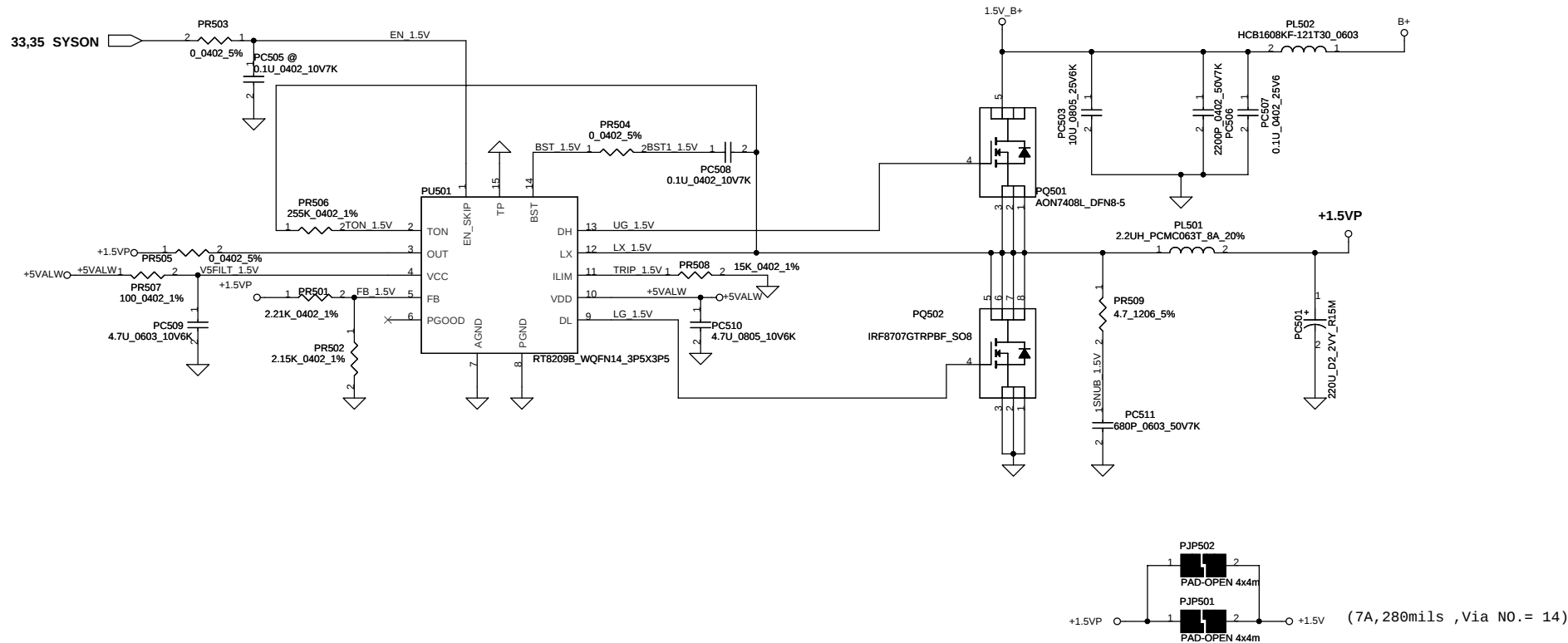
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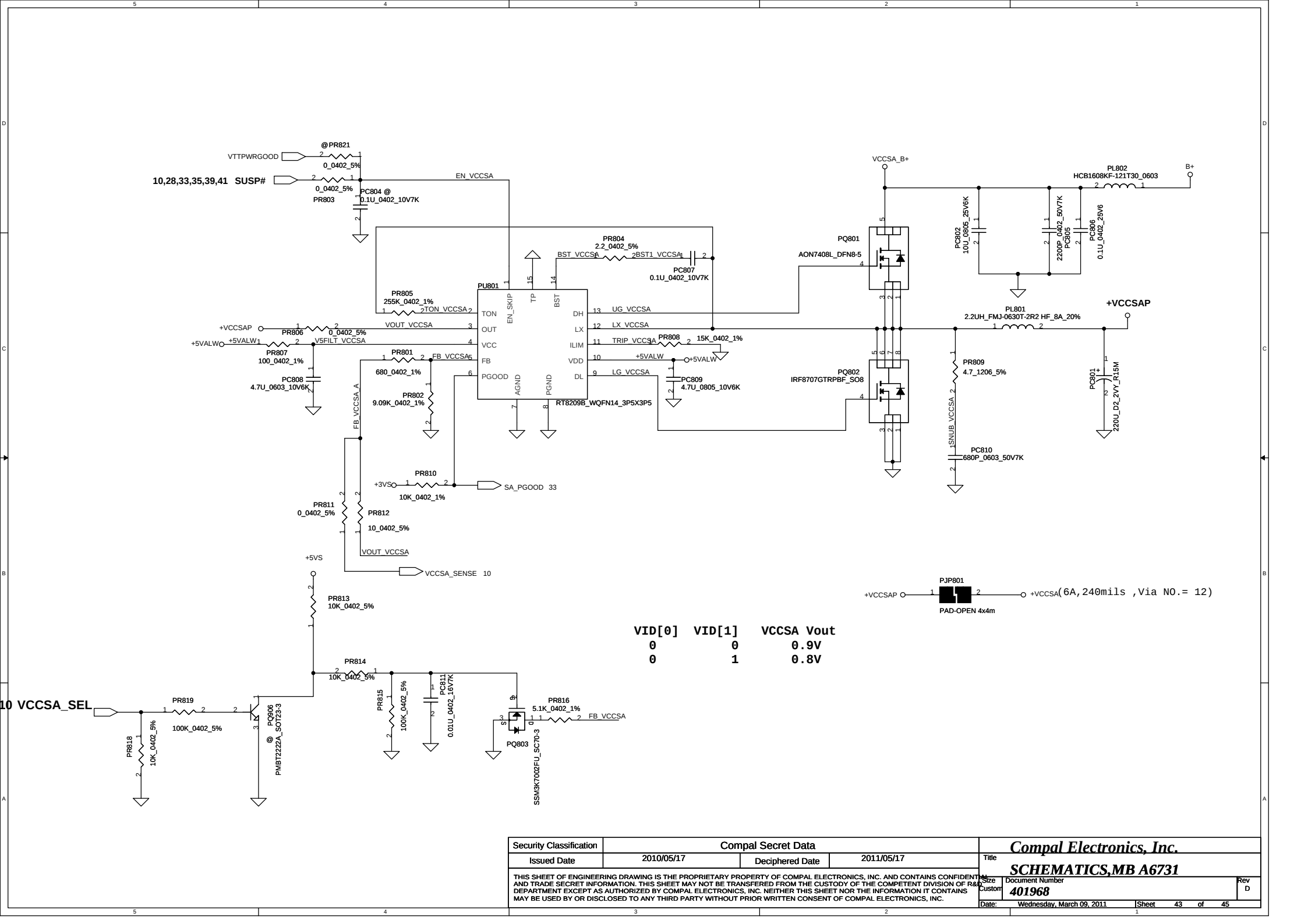
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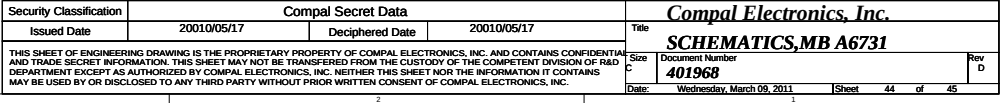


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VID[0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V

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PIR (Product Improve Record)

Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/13	25	Reserve R433	Reserve +3VLW power for VCCPDSW
2	08/13	31	DEL RA17, RA19-->RA19@, change RA16 to 39.2K	Audio MIC sense from B to A
3	08/13	17	Add R432,unpop R572,R1530,U47,C869 for HDMI HPD	HDMI HPD design change
4	08/23	31	change CA9 CA10 to 4.7u(0603)	Audio test Issue
6	08/23	28	Change U142A compare circuit Change U142B compare circuit Change new Bus switch for 3V system Change KB930 programming strap pin	change degug schematic to follow PBL21
7	08/23	34	change LED(D74,D75,D25,D26) to follow ID and ME define	EMI demand
8	09/03	35	Change ODD_EN# from GPIO24 to GPIO68 GPIO24 PU +3VS 10K	GPIO Common design
9	09/03	41	Reserve C729,C730,C731,C732 to +3VS	EMI demand
10	09/03		Reserve C330,C311 on H_PWRGD	EMI demand
11	09/03		Reserve C314,C315,C315 on SUSP	EMI demand
12	09/03		Reserve C850,C851, C854 on 5VS	EMI demand

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	09/28	31	change MIC1 from onboard MIC to Conn	change onboard MIC.
2	10/22	18	swap HP_R and HP_L	error
3	10/28	20	Del R734, Add R1192 for SUSCLK PD	EC Request, Common Design
4	10/28	10	R114,R115 change to 1K fro SM_VREF	Follow Intel DG
5	10/28	8	R92,R93 change to mount for RSVD6,7	Follow Intel DG
6	10/28	18	Del T72, Add R193 for PCH_GPIO19,Del R182	Follow Intel DG
7	10/28	22	change R314 to 1K for NV_CLE	Follow Intel DG
8	10/28	24	change VCC_SPI to +3VS	Common DG
9	10/28	18	add R438(1M) for HAD_SNC_R PD	Follow Intel DG
10	10/28	5	add C234,C235,C236,C238,C243 for EMI demand	EMI demand
11	10/29	33	add R744,R1211	EC GPIO Common design for USB30_OC# and P_USB#

Revision Change: 0.3 to 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/06	34	Charge LED:del R204, add R270,R271	to fit the SPEC
2	12/06	10	change C137 from 470U to 330U for PWR demand	CPU_CORE CAP COST
3	12/06	20	add C316 for EC demand	EC Request, Common Design
4	12/06	05	XDP:del XDP for ESD demand	ESD DEMAND
5	12/06	31	MIC:add DA10 A-GND	EMI DEMAND
6	12/06	23	PCH_GPIO24:add R439 for 3VALW_PCH PU(reserve)	Follow Intel DG