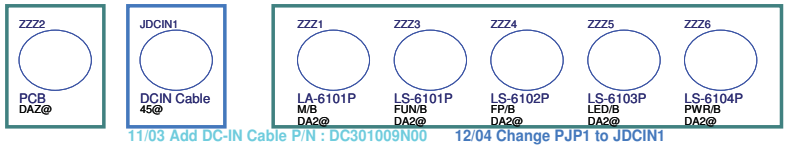

11/03 Add DC-IN Cable P/N : DC301009N00 12/04 Change PJP1 to JDCIN1

11/18 Change PCB P/N from DA60000G300 to DA60000G200

02/26 Change LA-6101P P/N from DA60000G200 to DA60000G210

02/26 Add DAZ P/N and other small board P/N

02/26 Change DAZ P/N from DAZ0D9001001 to DAZ0D900101

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NAU00 LA-6101P Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

SV M/B

2010-03-09

Rev : 1.0

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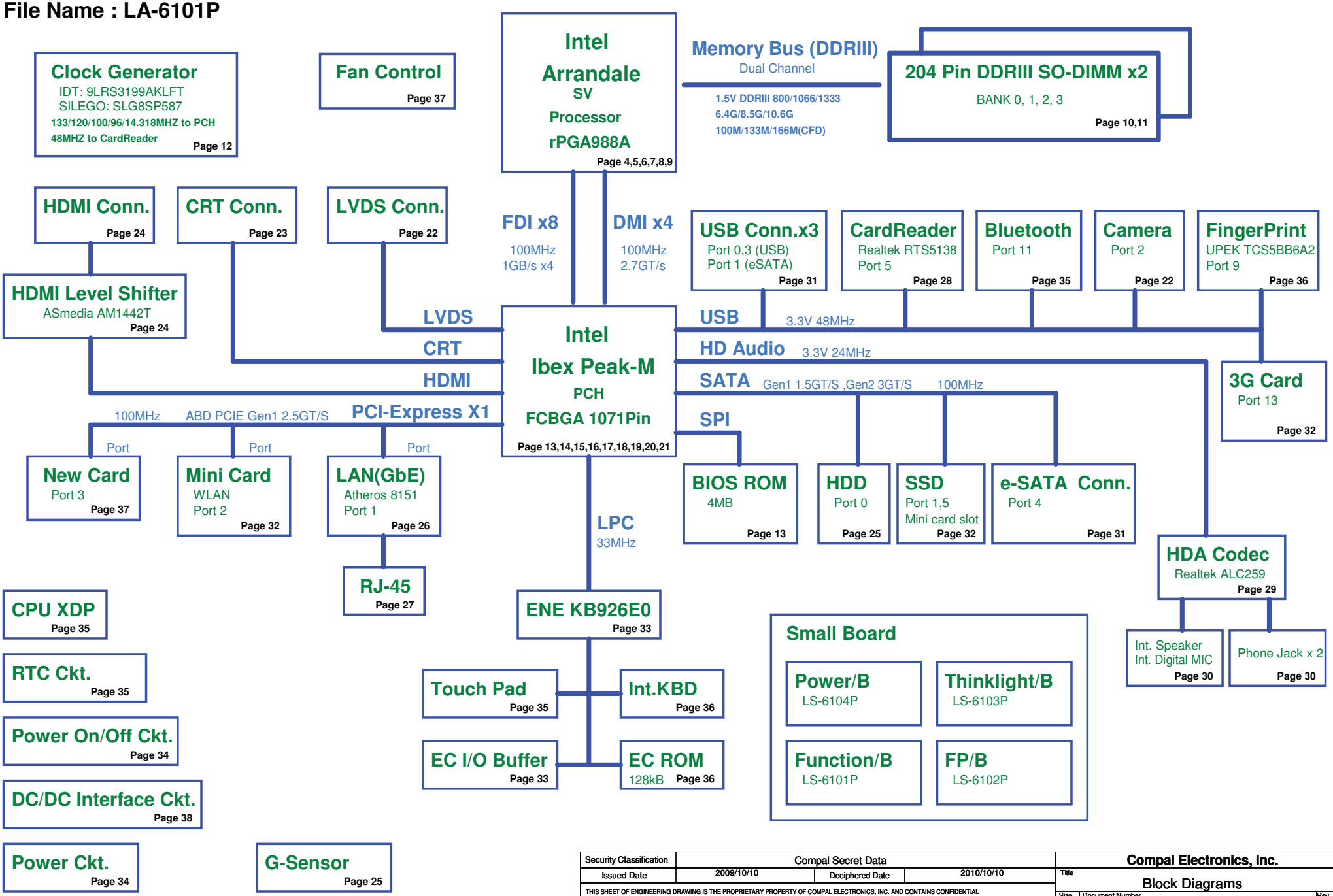
Title: Cover Page

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 1 of 48

Compal Confidential

Model Name : NAU00
File Name : LA-6101P



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title	Block Diagrams	
Size: B	Document Number: NAU00 M/B LA-6101P Schematics	Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

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Title: Notes List

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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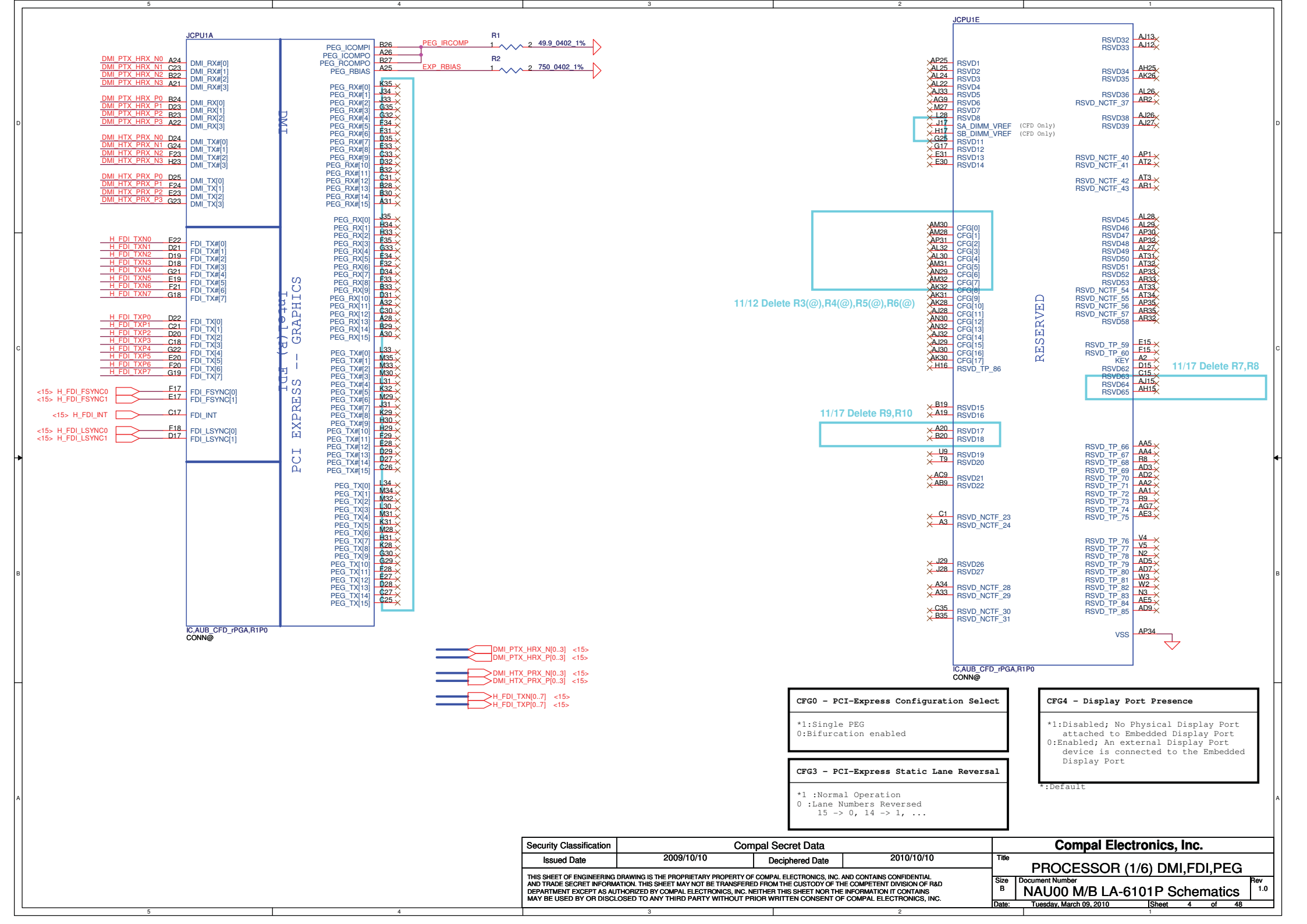

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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JCPU1B

MISC CLOCKS

MISC THERMAL

DDR3 MISC

JTAG & BPM

PWR MANAGEMENT

H_COMP3 AT23 COMP3
H_COMP2 AT24 COMP2
H_COMP1 G16 COMP1
H_COMP0 AT26 COMP0
T1 PAD @ SKTOCC# R AH24 SKTOCC#
H_CATERR# AK14 CATERR#
<18> H_PECI R19 1 2 0_0402_5% H_PECI_R AT15 PECI
<33,47> H_PROCHOT# H_PROCHOT# AN26 PROCHOT#
<18> H_THERMTRIP# R29 1 2 0_0402_5% H_THERMTRIP#_R AK15 THERMTRIP#

H_CPURST# AP26 RESET_OBS#
<15> H_PM_SYNC R32 1 2 0_0402_5% H_PM_SYNC_R AL15 PM_SYNC
R34 1 2 0_0402_5% H_CPUPWRGD_1 AN14 VCCPWRGOOD_1
<18> H_CPUPWRGD R37 1 2 0_0402_5% H_CPUPWRGD_0 AN27 VCCPWRGOOD_0
<15> PM_DRAM_PWRGD R40 1 2 0_0402_5% PM_DRAM_PWRGD_R AK13 SM_DRAMPWROK
<45> VCCP_POK R620 1 2 1K_0402_1% VCCP_POK_R AM15 VTTPWRGOOD
R621 1 2 560_0402_5%
AM26 TAPPWRGOOD
<17,33> PLT_RST# R42 1 2 1.5K_0402_1% PLT_RST#_R AL14 RSTIN#
R43 750_0402_1%

2009/2/4
#414044 DG
Update Rev1.11

IC,AUB_CFD_rPGA,R1P0
CONN@

10/30 Add R620,R621 (Follow NIWE2)
10/21 Delete R41
Delete Net : H_PWRGD_XDP,H_PWRGD_XDP_R

BCLK A16 CLK_CPU_BCLK
BCLK# B16 CLK_CPU_BCLK#
CLK_CPU_BCLK <18>
CLK_CPU_BCLK# <18>

11/12 Delete R11,R12,R15,R16 (Layout Spacing)

BCLK_ITP AR30 CLK_CPU_ITP_R
BCLK_ITP# AT30 CLK_CPU_ITP#_R
PAD T17 @
PAD T18 @

10/21 Delete R13,R14, Add T17,T18

PEG_CLK E16 CLK_CPU_DMI
PEG_CLK# D16 CLK_CPU_DMI#
CLK_CPU_DMI <14>
CLK_CPU_DMI# <14>

DPLL_REF_SSCLK A18 CLK_CPU_DP_R
DPLL_REF_SSCLK# A17 CLK_CPU_DP#_R
R572 1 2 0_0402_5%
R573 1 2 0_0402_5%

10/30 Delete Net : CLK_CPU_DP#,CLK_CPU_DP#
Delete R17,R18

SM_DRAMRST# F6 SM_DRAMRST# <10>

11/05 Delete R21(@)

SM_RCOMP[0] AL1 SM_RCOMP_0
SM_RCOMP[1] AM1 SM_RCOMP_1
SM_RCOMP[2] AN1 SM_RCOMP_2

+1.1VS_VTT
R25 1 2 10K_0402_5%
R27 1 2 10K_0402_5%
R28 1 2 0_0402_5%

PM_EXT_TS#[0] AN15 PM_EXTTS#0
PM_EXT_TS#[1] AP15 PM_EXTTS#1_R
PM_EXTTS#0_1 <10,11>

PRDY# AT28 XDP_PRDY#
PREQ# AP27 XDP_PREQ#

TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#

TDI AT29 XDP_TDI
TDO AR27 XDP_TDO
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M

DBR# AN25 XDP_DBR#_R
R36 1 @ 2 0_0402_5%
XDP_DBRESET#
XDP_DBRESET# <15>

11/25 Change R36 from mount to @ (Follow NIWE2)

XDP_DBR#_R C500 1 2 @0.1U_0402_16V4Z

ESD Recommend

BPM#[0] AJ22
BPM#[1] AK22
BPM#[2] AK24
BPM#[3] AJ24
BPM#[4] AJ25
BPM#[5] AH22
BPM#[6] AK23
BPM#[7] AH23

10/21 Delete Net : XDP_OBS[7:0]

2009/2/4
Delete dampling resistor for power noise and Layout space issue

+1.1VS_VTT
XDP_PRDY# R20 1 @ 2 51_0402_5%
XDP_TMS R22 1 @ 2 51_0402_5%
XDP_TDI R23 1 @ 2 51_0402_5%
XDP_PREQ# R24 1 @ 2 51_0402_5%
XDP_TCLK R26 1 @ 2 51_0402_5%

XDP_TRST# R30 1 2 51_0402_5%

XDP_TDO_M
R35 0_0402_5%
XDP_TDI_M

10/28 Delete R31,R33(@),R38(@),R39
Delete Net : XDP_TDI_R,XDP_TDO_R

Processor CLK

Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

+3VALW
+1.5V_1
VCCP_POK VCCP_POK <45>
U1 NC7SZ08P5X_NL_SC70-5
R44 @ 1.1K_0402_1%
R45 1.5K_0402_1%
PM_DRAM_PWRGD_R
R53 @ 3K_0402_1%
R54 750_0402_1%

Note: When implement S3 power reduction not to pop,R53,R44 pop U1,R45,R54

11/23 Change R44,R53 from mount to @
Change U1,R45,R54 from @ to mount

+1.1VS_VTT
H_CATERR# R46 1 2 49.9_0402_1%
H_PROCHOT# R47 1 2 68_0402_5%
H_CPURST# R48 1 @ 2 68_0402_5%

H_COMP0 R49 1 2 49.9_0402_1%
H_COMP1 R50 1 2 49.9_0402_1%
H_COMP2 R51 1 2 20_0402_1%
H_COMP3 R55 1 2 20_0402_1%

SM_RCOMP_0 R58 1 2 100_0402_1%
SM_RCOMP_1 R60 1 2 24.9_0402_1%
SM_RCOMP_2 R61 1 2 130_0402_1%

11/16 Reserve C530,C531,C532 for avoiding switching noise
11/23 Change C530,C531,C532 from @ to mount

VCCP_POK C530 1 2 100P_0402_50V8J
PM_DRAM_PWRGD_R C531 1 2 100P_0402_50V8J
H_CPUPWRGD C532 1 2 100P_0402_50V8J

10/21 Delete JP1,R52,R56,R57,R59,C1
Delete Net : H_CPUPWRGD,H_PWRGOOD_R,
PBTN_OUT#_XDP,CLK_CPU_XDP,CLK_CPU_XDP#

XDP_DBRESET# 1 @ 2 R62 1K_0402_5% +3VS
XDP_TDO 1 2 R63 51_0402_5% +1.1VS_VTT
Leakage Issue

10/22 Change R62 from mount to @
10/30 Change R62 from @ to mount (Follow NCQD0)
11/25 Change R62 from mount to @ (Follow NIWE2)

+5VALW
R574 10K_0402_5%
S3_0.75V_EN S3_0.75V_EN <44>
VCCP_POK
Q37 SSM3K7002FU_SC70-3

12/04 Change Q37 from SB000008J00 to SB000009610 (Layout Spacing)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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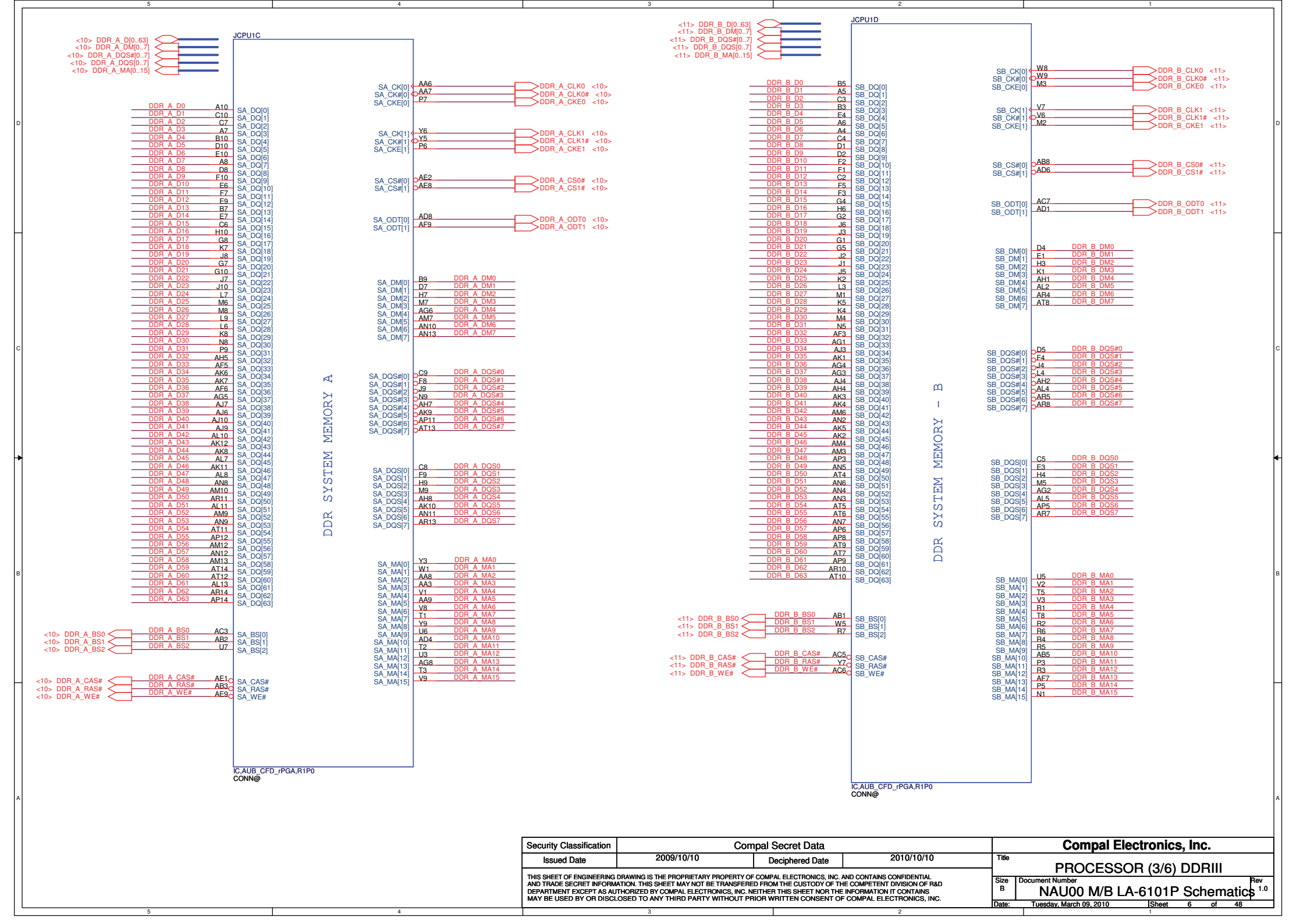

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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JCPU1F

WW15 MOW
Peak 21A
Continuous 18A

48A

+CPU_CORE

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0
CONN@

1.1V RAIL POWER

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.1VS_VTT

10U_0805_6.3V6M

C2 C3 C4 C5 C6 C7 C8

330U_D2_2.5VY_R9M

C18 C19 C20

330U_D2_2.5VY_R9M 330U_D2E_2VM_R6M

11/25 Change C18,C19,C20 from SGA00002380 (6mohm) to SGA00002680 (9mohm)
11/25 Change C19 from mount to @
11/30 Change C20 from SGA00002680 (9mohm) to SGA00002U00 (6mohm)
11/09 Change R64,R66 from mount to @ (PWR Recommend)
11/09 Change R65,R67 from @ to mount (PWR Recommend)

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

22U_0805_6.3V6M

C28 C29

CPU CORE SUPPLY

POWER

CPU VIDS

PSI# AN33 PSI# <47>

VID[0] AK35 H_VID0 <47>
VID[1] AK33 H_VID1 <47>
VID[2] AK34 H_VID2 <47>
VID[3] AL35 H_VID3 <47>
VID[4] AL33 H_VID4 <47>
VID[5] AM35 H_VID5 <47>
VID[6] AM34 H_VID6 <47>

PROC_DPRSLPVR PROC_DPRSLPVR <47>

VTT_SELECT G15 VTT_SELECT VTT_SELECT <45>

VTT_SELECT = Low, 1.1V
VTT_SELECT = High, 1.05V

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

SENSE LINES

ISENSE AN35 IMVP_IMON <47>

VCC_SENSE AJ34 VCCSENSE_CPU R83 0_0402_5%
VSS_SENSE AJ35 VSSSENSE_CPU R84 0_0402_5%

R82 100_0402_1% +CPU_CORE
VCCSENSE <47>
VSSSENSE <47>
R85 100_0402_1%

VTT_SENSE B15 VTT_SENSE <45>
VSS_SENSE_VTT A15 VSS_SENSE_VTT
R86 @ 0_0402_5%

11/25 Change R86 from mount to @ (Follow NIWE2)

Note:CRB has the VTT_SENSE connected through a "no-stuff" 0- series resistor and VSS_SENSE_VTT floating.Connect VSS_SENSE_VTT to GND or can be left floating.

+CPU_CORE
10U_0805_6.3V6M
C9 C10 C11 C12 C13 C14 C15 C16 C17
(Place these capacitors between inductor and socket on Bottom)

+CPU_CORE
10U_0805_6.3V6M
C21 C22 C23 C24 C25 C26 C27
(Place these capacitors under CPU socket, top layer)

CSC (Current Sense Configuration)
11/09 H_VID[6:0] => 0100100

H_VID0 R64 R65 1K_0402_1%
H_VID1 R66 R67 1K_0402_1%
H_VID2 R68 R69 1K_0402_1%
H_VID3 R70 R71 1K_0402_1%
H_VID4 R72 R73 1K_0402_1%
H_VID5 R74 R75 1K_0402_1%
H_VID6 R76 R77 1K_0402_1%
PROC_DPRSLPVR R78 R79 1K_0402_1%
PSI# R80 R81 1K_0402_1%

11/17 Reserve C534,C535 for avoiding switching noise
11/17 Change C534,C535 from @ to mount

VTT_SELECT C534 100P_0402_50V8J
VTT_SENSE C535 100P_0402_50V8J
Please place C534,C535 close to PU701

+CPU_CORE
22U_0805_6.3V6M
C34 C30 C35 C31 C32 C33
(Place these capacitors on CPU cavity, Bottom Layer)

+CPU_CORE
22U_0805_6.3V6M
C36 C37 C38 C39 C40 C41
(Place these capacitors on CPU cavity, Bottom Layer)

11/09 Change C42~C47 from SGA00002U00 to SGA00001Q80 (PWR Recommend)
11/11 Correct C42~C47 footprint

+CPU_CORE
4 x 330uF(6m ohm@100kHz) SGA00001Q80
C42 C44 C45 C46 C47 C43
330U_X_2VM_R6M
TOP side (under inductor)

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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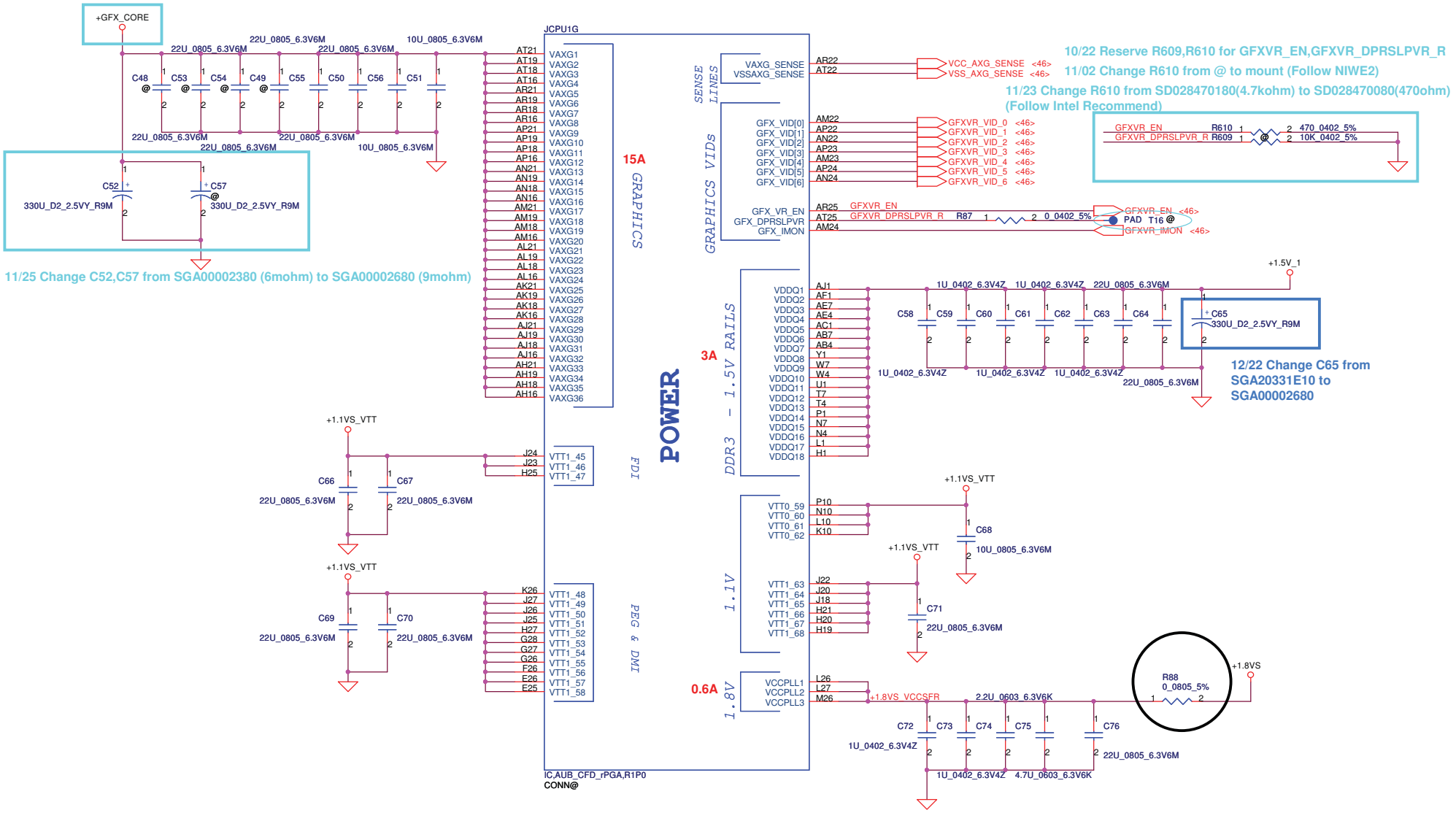

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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JCPU1H

VSS

IC,AUB_CFD_rPGA,R1P0
CONN@

JCPU1I

VSS

IC,AUB_CFD_rPGA,R1P0
CONN@

11/17 Delete T2,T3,T4,T5

NCTF

Screw cap.

Please place C520~C529 close to H1,H10,H2,H20,H3,H4,H6,H7,H8,H9

11/17 Change the power of C520,C528 from +3VS to B+

12/15 Change C520(@),C528(@) from SE070104Z80 to SE042104K80

11/10 Add C520~C529(@) (ESD Recommend)

11/13 Change C522 power from +3VS to +3VALW

11/17 Delete C521(@),C523(@)

12/15 Add C536~C540 (EMI Recommend)

12/15 Change C539,C540 from SE070104Z80 to SE042104K80

12/15 Add C541~C543 (EMI Recommend)

01/15 Add C544~C549 (EMI Recommend)

01/16 Add C550 (EMI Recommend)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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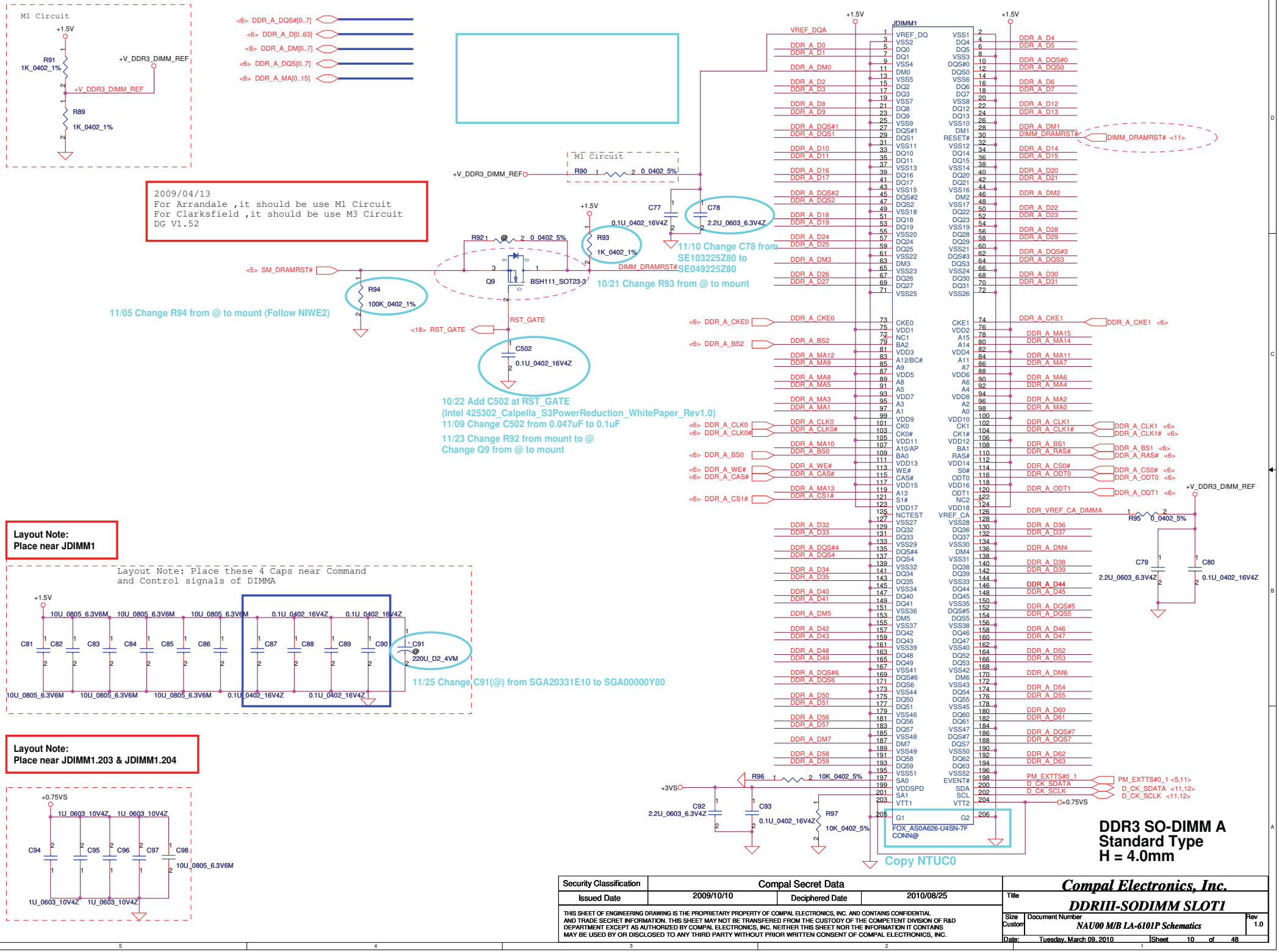
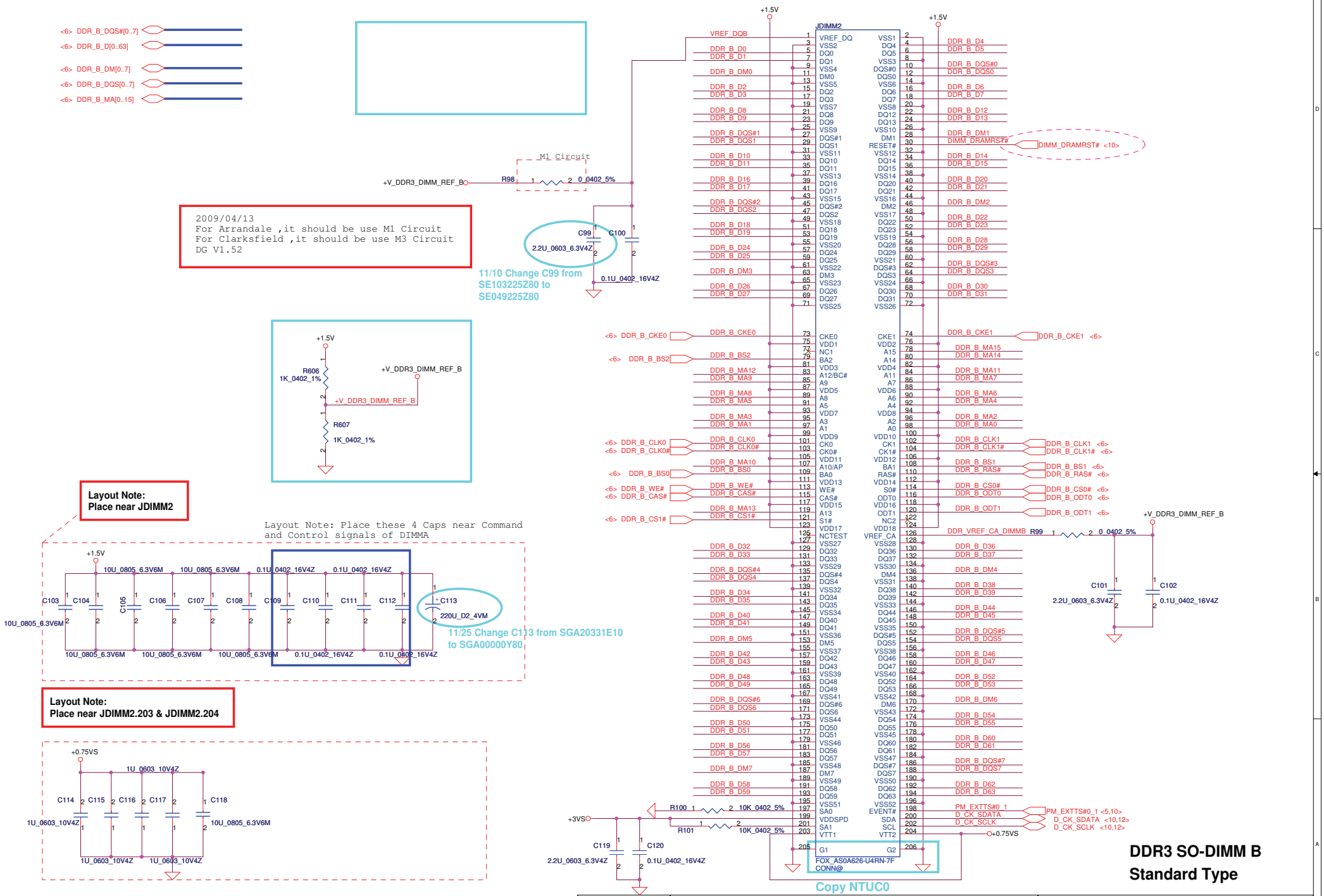


Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: DDRIII-SODIMM SLOT1			
Size: Custom	Document Number: NAU00 M/B LA-6101P Schematics		Rev: 1.0
Date: Tuesday, March 09, 2010	Sheet 10 of 48		



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/08/25

Compal Electronics, Inc.	
Title	DDRIII-SODIMM SLOT2
Size	Document Number: NAU00 M/B LA-6101P Schematics
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Layout note:
Place C122 close to L2
Place C123 close to U2.15
Place C124 close to U2.18

+1.1VS_VTT
L2 1 2 0_0603_5%
+CLK_VDDSRC
0.1U_0402_16V4Z
C122 10U_0805_10V4Z
C123
C124
0.1U_0402_16V4Z

11/06 Change +1.05VS to +1.1VS_VTT

11/03 Delete C121(@)
11/03 Change L2 from SM01000AX00 to 0ohm (Follow NIWE2)

Layout note:
Place C130 close to L1
Place C131 close to U2.5
Place C132 close to U2.29

+3VS
L1 1 2 0_0603_5%
+CLK_VDD
0.1U_0402_16V4Z
C130 10U_0805_10V4Z
C131
C132
0.1U_0402_16V4Z

11/03 Delete C129(@)
11/03 Change L1 from SM01000AX00 to 0ohm (Follow NIWE2)

Layout note:
Place C507 close to R103

+1.5VS
R103 1 2 0_0402_5%

11/03 Delete L3,C126,C125(@)
10/23 Delete C127, C128, C501 on +CLK_1.5VDD

+CLK_VDD
R102 @ 0_0402_5%
+VDD_3V3_1V5
C507 10U_0805_10V4Z
C133
C134
C135 0.1U_0402_16V4Z
0.1U_0402_16V4Z 0.1U_0402_16V4Z

Layout note:
Place C133 close to U2.1
Place C134 close to U2.17
Place C135 close to U2.24

10/23 Add C1000 on +VDD_3V3_1V5
Change C133, C134, C135 from +CLK_VDD to +VDD_3V3_1V5
11/03 Change C507 from @ to mount

Type	R102	R103
Standard	Mount	@
Low Power	@	Mount

10/23 Change U2 Pin1,17,24
Net Name to +VDD_3V3_1V5

Clock Generator

11/03 Delete RP1,RP2,RP3,RP4

<14> CLK_BUF_DREF_96M
<14> CLK_BUF_DREF_96M#
CLK_BUF_DREF_96M
CLK_BUF_DREF_96M#

10/21 Change R542 from 0ohm to 33ohm (Vendor Recommend)

<28> CLK_48M
C510 1 2 @15P_0402_50V8J
R542 1 2 33_0402_5%
48M

<14> CLK_BUF_PCIE_SATA
<14> CLK_BUF_PCIE_SATA#
CLK_BUF_PCIE_SATA
CLK_BUF_PCIE_SATA#

<14> CLK_BUF_CPU_DMI
<14> CLK_BUF_CPU_DMI#
CLK_BUF_CPU_DMI
CLK_BUF_CPU_DMI#

11/04 Reserve C510(@) for CLK_48M (RF Recommend)

+CLK_VDDSRC
+CLK_VDD
+VDD_3V3_1V5
+CLK_VDD
H_STP_CPU#

U2

1	VDD_USB_48	SCL	32
2	VSS_48M	SDA	31
3	DOT_96	REF_0/CPU_SEL	30
4	DOT_96#	VDD_REF	29
5	VDD_27	XTAL_IN	28
6	27MHZ	XTAL_OUT	27
7	27MHZ_SS	VSS_REF	26
8	USB_48	CKPWRGD/PD#	25
9	VSS_27M	VDD_CPU	24
10	SATA	CPU_0	23
11	SATA#	CPU_0#	22
12	VSS_SRC	VSS_CPU	21
13	SRC_1	CPU_1	20
14	SRC_1#	CPU_1#	19
15	VDD_SRC_IO	VDD_CPU_IO	18
16	CPU_STOP#	VDD_SRC	17
33	TGND		

SLG8SP587VTR_QFN32_5X5
SA00003HR00
11/03 Change U2 from SA00003MF00 to SA00002XY00
11/23 Change U2 from SA00002XY00 to SA00003HR00

D_CK_SCLK
D_CK_SDATA
REF_0/CPU_SEL
R104 1 2 33_0402_5%
D_CK_SCLK <10,11>
D_CK_SDATA <10,11>
CLK_BUF_ICH_14M <14>

CLK_XTAL_IN
CLK_XTAL_OUT
CK505_PWRGD

C509 10P_0402_50V8J

11/04 Reserve C509(@) for CLK_BUF_ICH_14M (RF Recommend)
01/15 Add C509 (10pF)

CLK_BUF_CPU_BCLK
CLK_BUF_CPU_BCLK#
CLK_BUF_CPU_BCLK <14>
CLK_BUF_CPU_BCLK# <14>

10/23 Change R107 from mount to @
11/03 Change R107 from @ to mount

+3VS
R107 1 2 10K_0402_5% H_STP_CPU#

IDT& Realtek Have Internal Pull-Down

R109 1 2 10K_0402_5% REF_0/CPU_SEL

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

+3VS
Q11 SSM3K7002FU_SC70-3
R108 4.7K_0402_5%
<14,32,37> PCH_SMBDATA
D_CK_SDATA

9/10 Change symbol of Q31/Q32 to SC70-3

Q12 SSM3K7002FU_SC70-3
R110 4.7K_0402_5%
<14,32,37> PCH_SMBCLK
D_CK_SCLK

Realtek Have Internal Pull-Down

R105 10K_0402_5%
R106 0_0402_5%
CK505_PWRGD
VGATE <15,47>
Q10 SSM3K7002FU_SC70-3
CLK_EN# <47>

9/10 Change symbol of Q29 to SC70-3

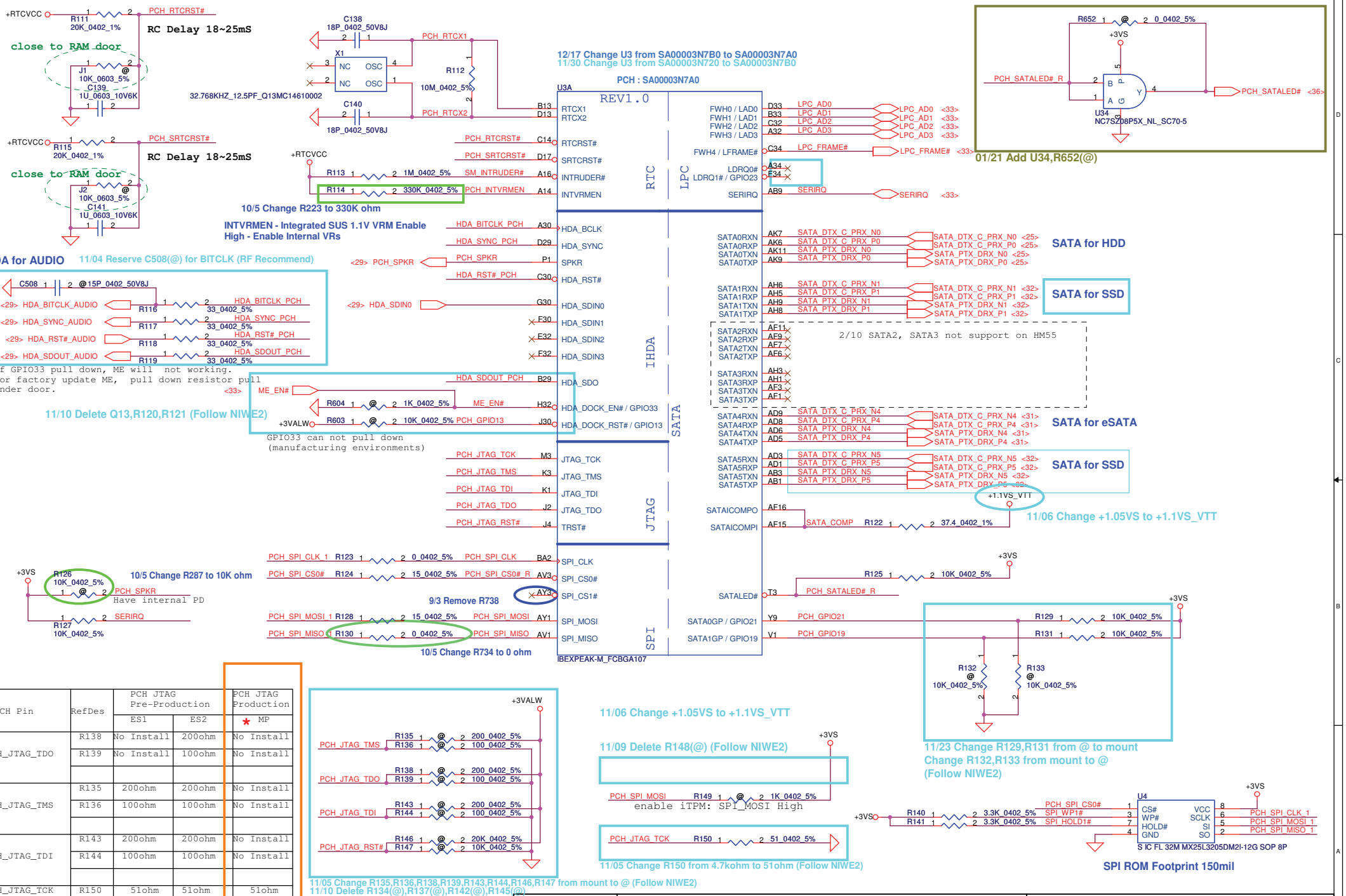
CLK_XTAL_IN
CLK_XTAL_OUT
Y1 14.318MHZ_16PF_7A14300083
C136 22P_0402_50V8J
C137 22P_0402_50V8J

9/23 Change C495 to 22pF

update PCB footprint

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.
Title: Clock Generator (CK505)
Size: Custom
Document Number: NAU00 M/B LA-6101P Schematics
Rev: 1.0
Date: Tuesday, March 09, 2010
Sheet 12 of 48



PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R138	No Install	200ohm	No Install
	R139	No Install	100ohm	No Install
PCH_JTAG_TMS	R135	200ohm	200ohm	No Install
	R136	100ohm	100ohm	No Install
PCH_JTAG_TDI	R143	200ohm	200ohm	No Install
	R144	100ohm	100ohm	No Install
PCH_JTAG_TCK	R150	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R146	20Kohm	20Kohm	No Install
	R147	10Kohm	10Kohm	No Install

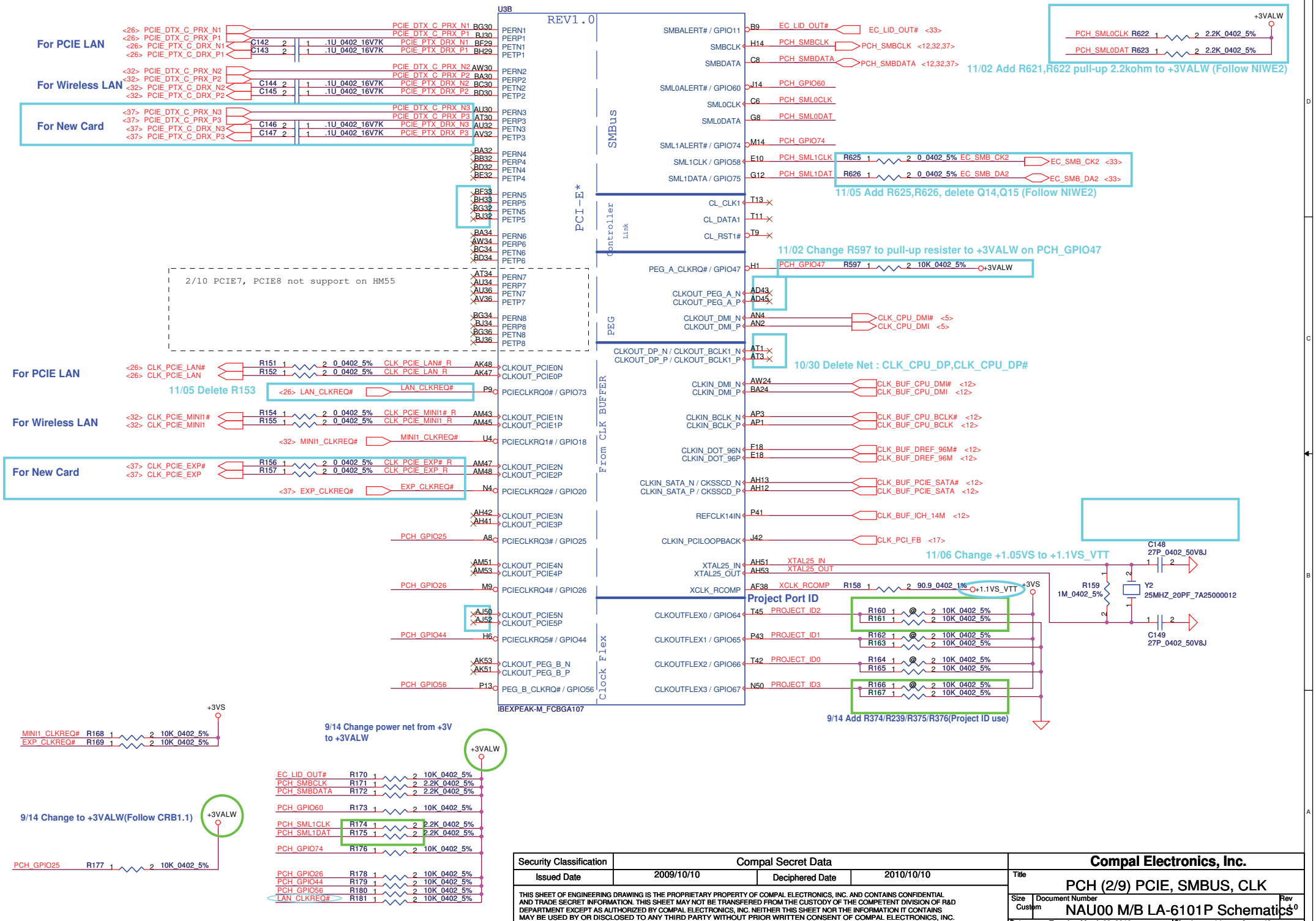
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 | Sheet 13 of 48

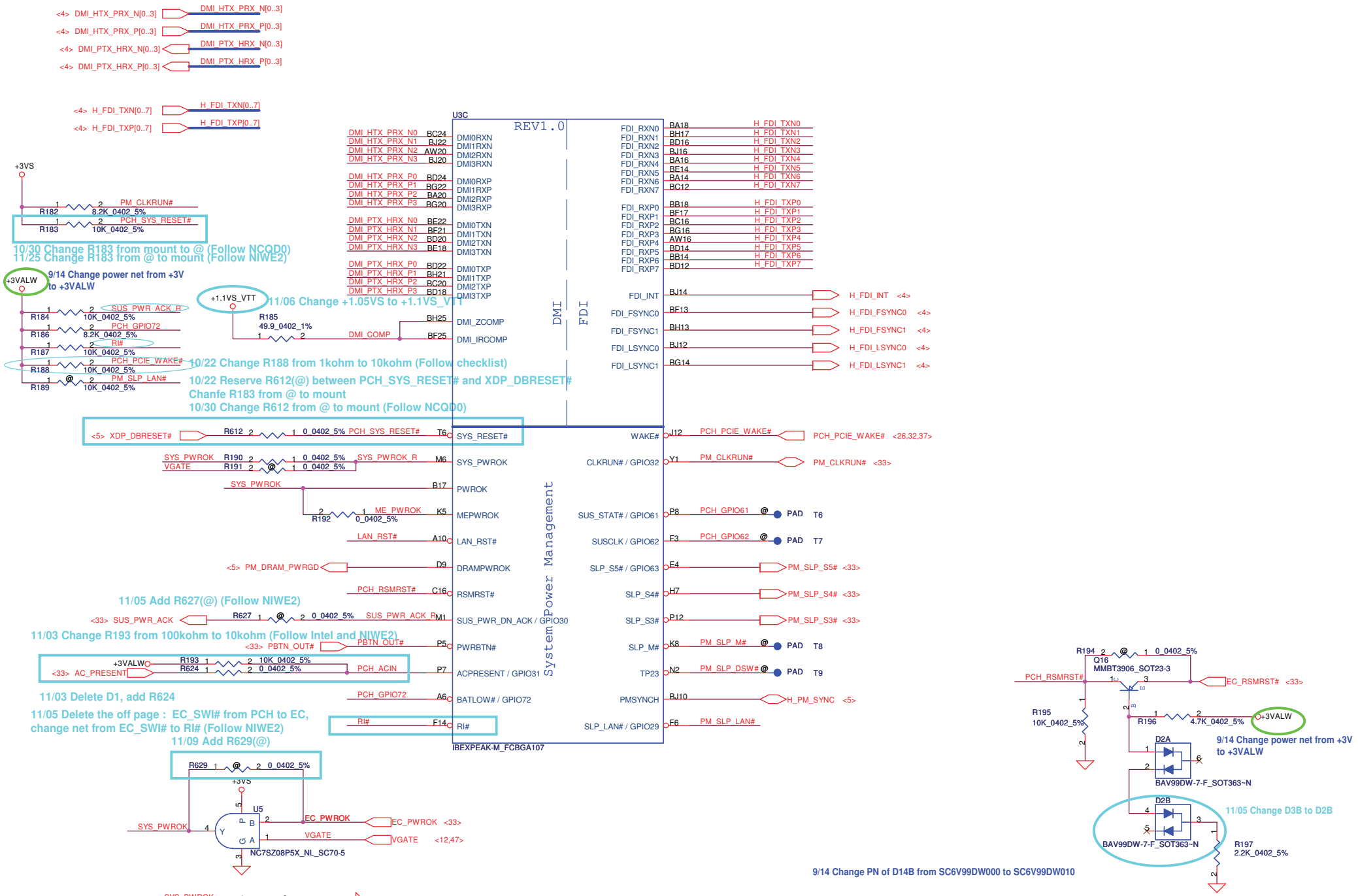


Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0
Date: Tuesday, March 09, 2010	Sheet 14 of 48	



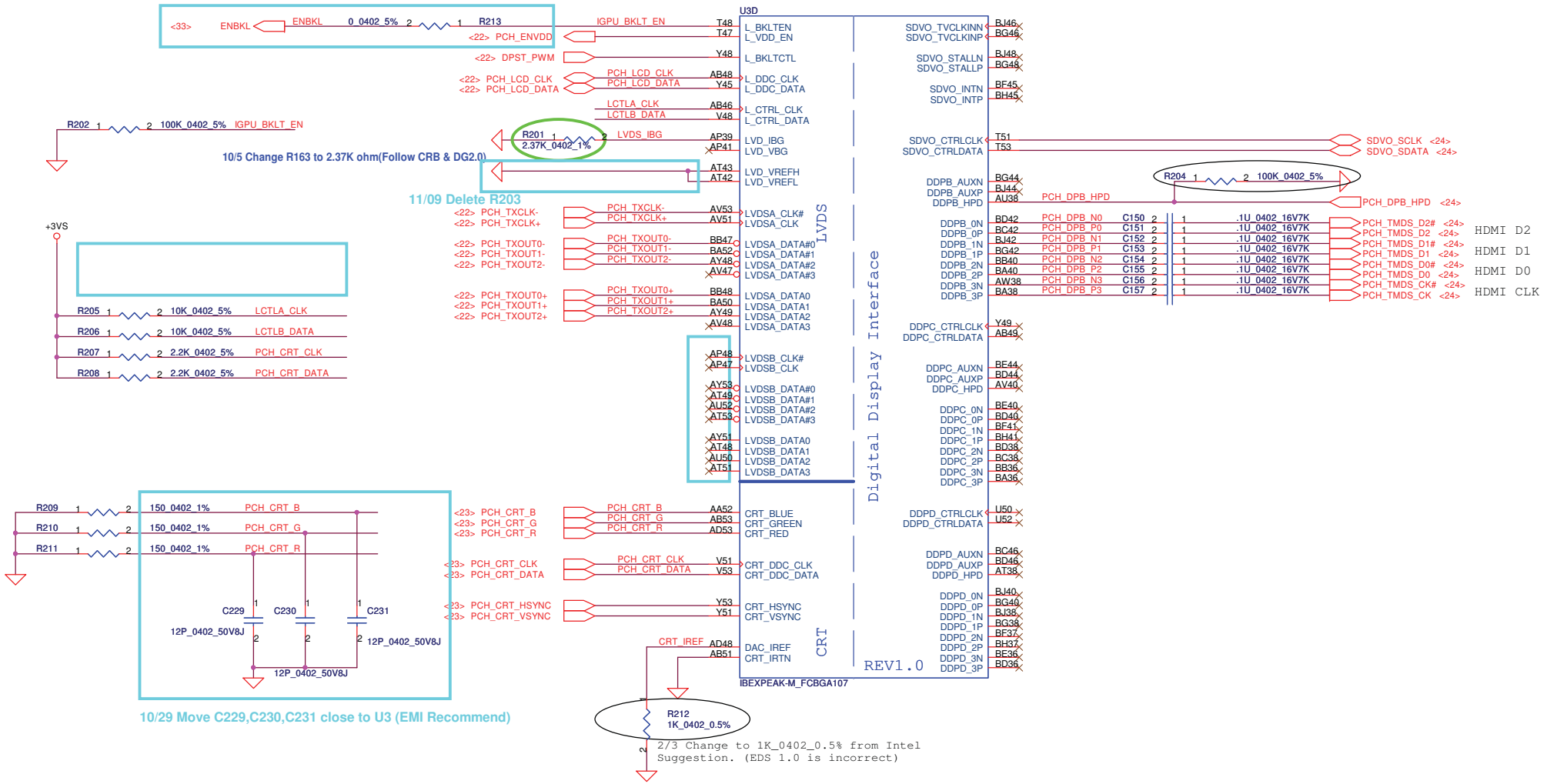
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 15 of 48



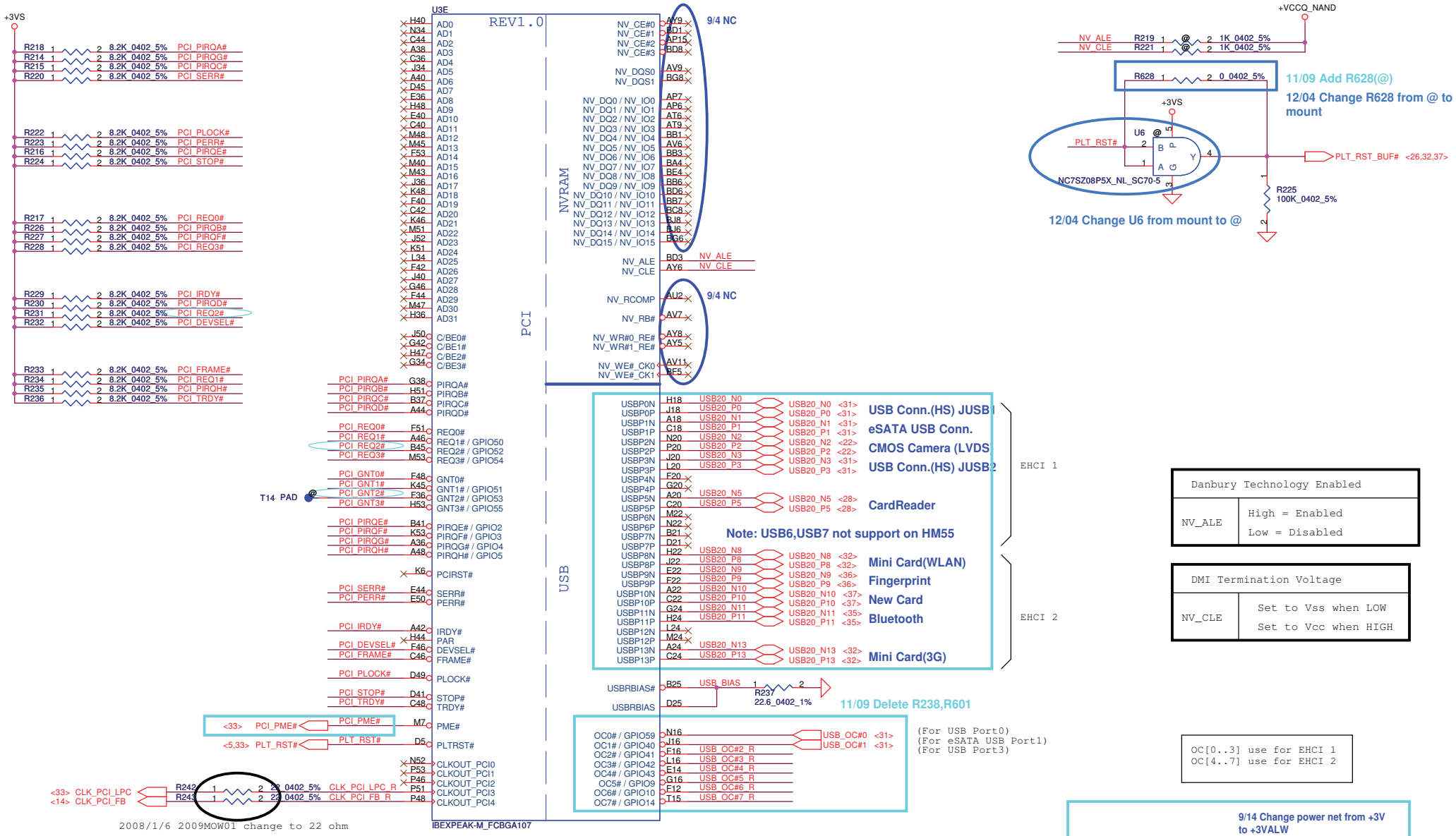
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 16 of 48



Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

*

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

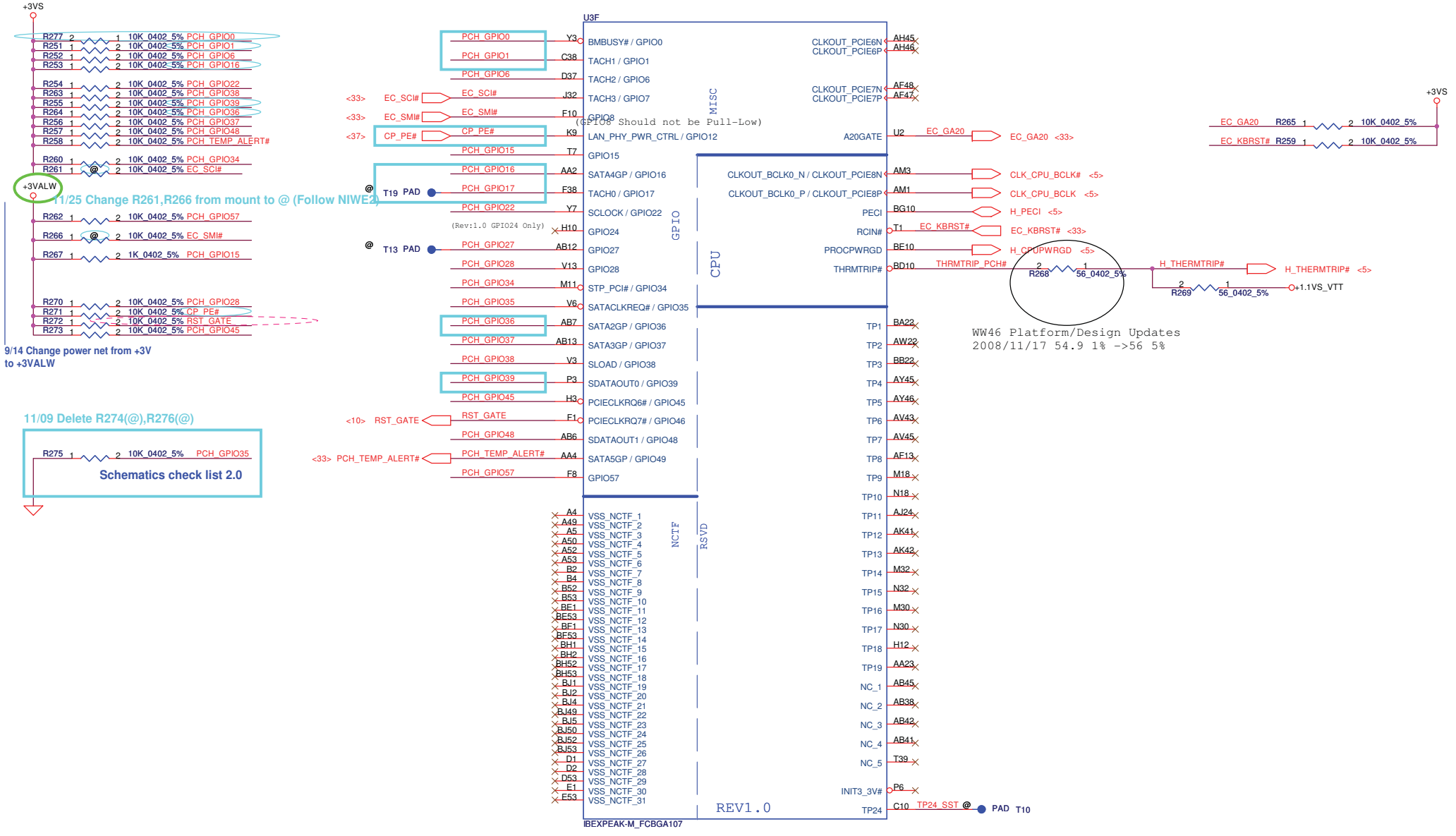
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 17 of 48



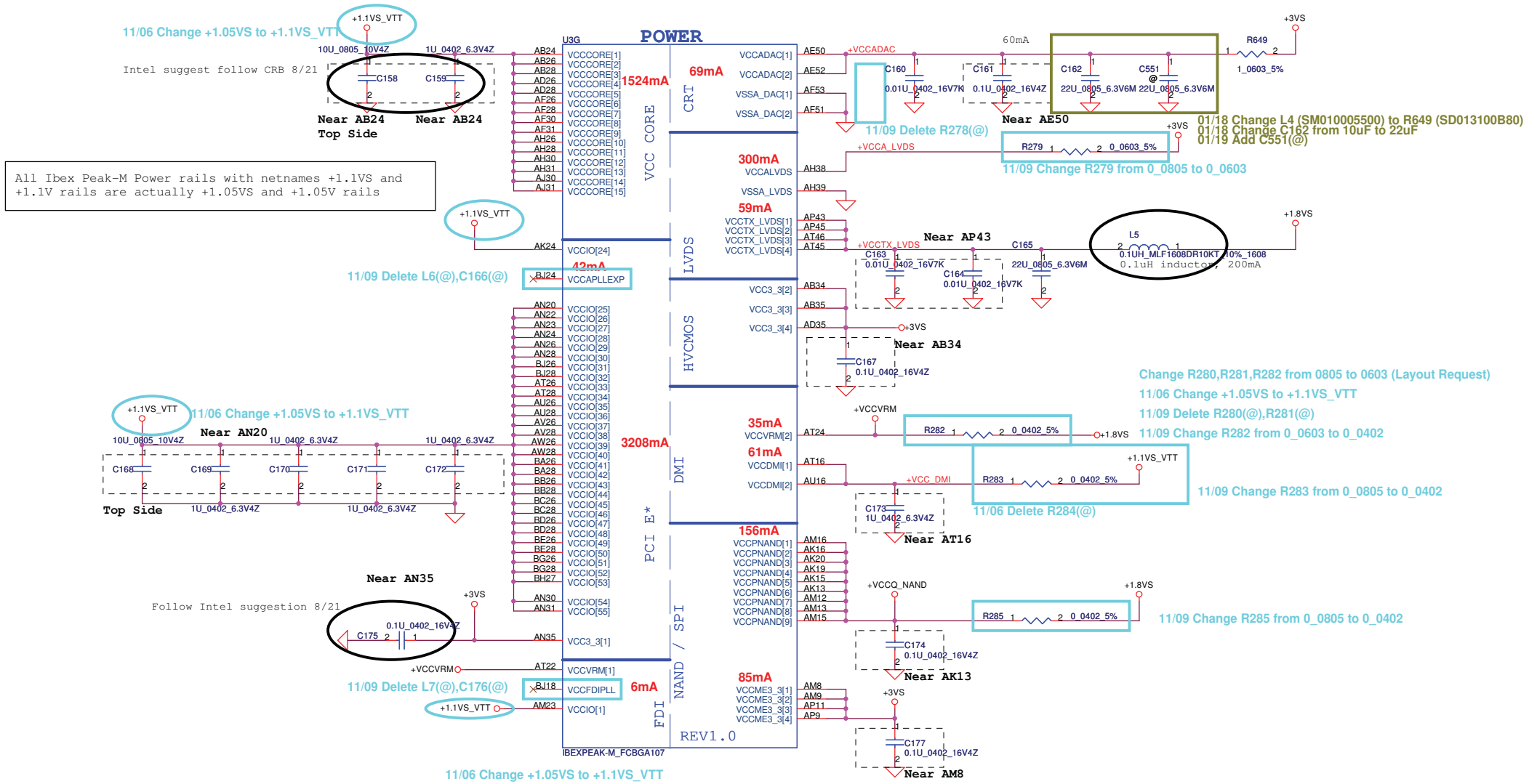
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 18 of 48



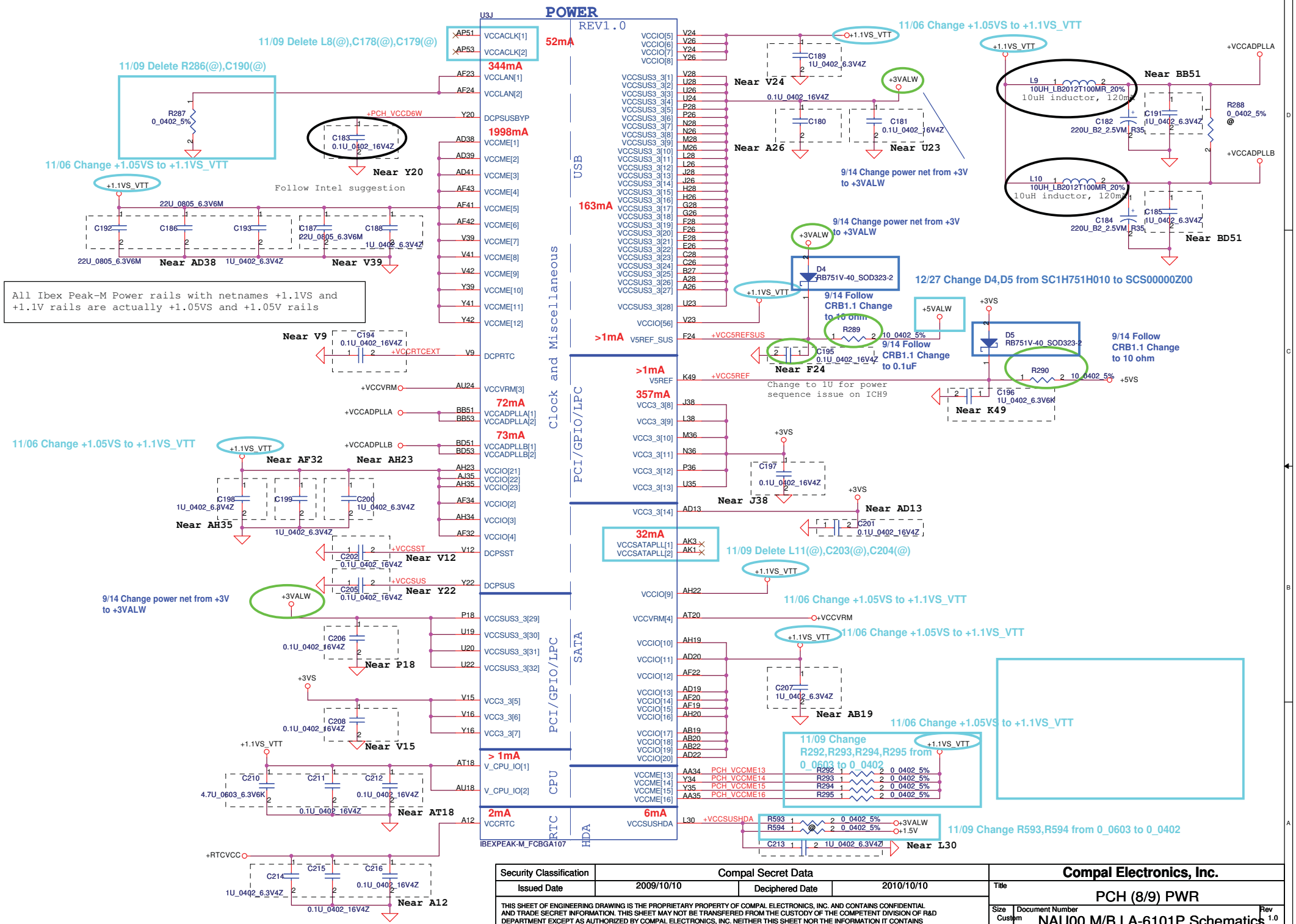
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 19 of 48



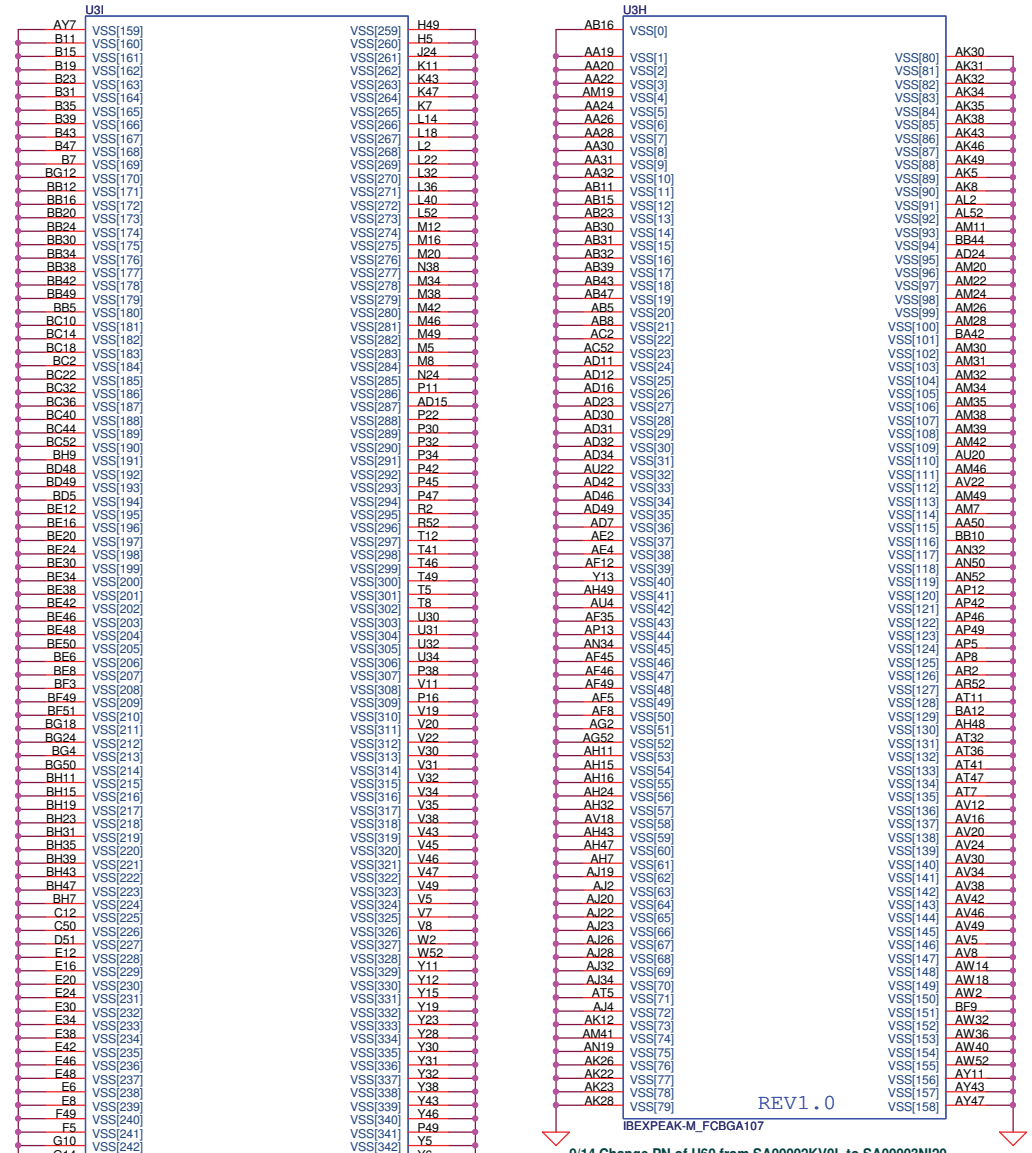
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Friday, February 26, 2010 | Sheet 20 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

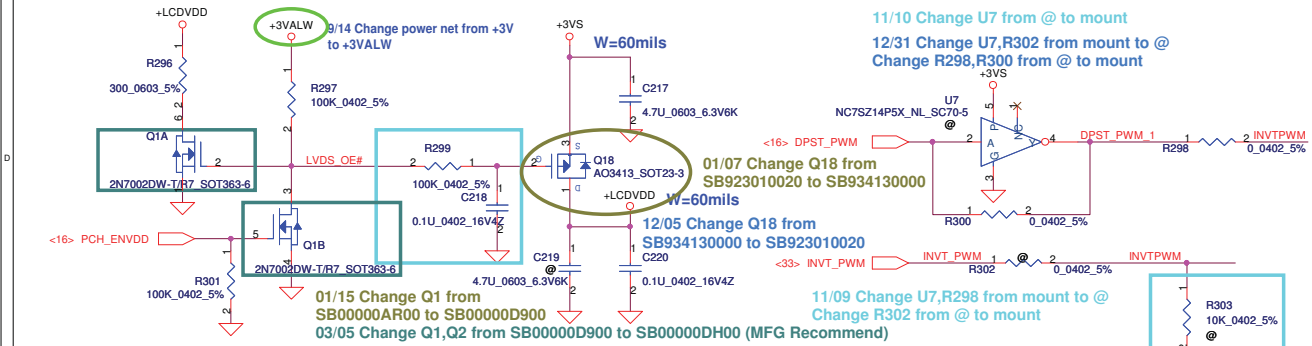
Compal Electronics, Inc.

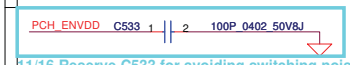
Title: PCH (9/9) VSS & PCH XDP Port

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Friday, February 26, 2010 Sheet 21 of 48

LCD POWER CIRCUIT

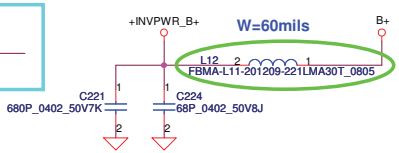


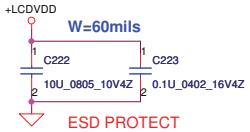


11/09 Change C218 from 0.047uf to 0.1uF
Change R299 from 1kohm to 100kohm
Change C219 from mount to @
(Follow KHLBX)

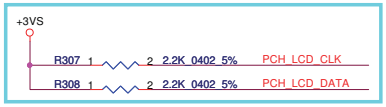
11/09 Delete R304(@) 11/10 Delete R305

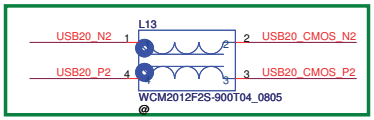
9/1 Del D5/R22(BKOFF# not need to pull high)

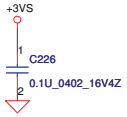


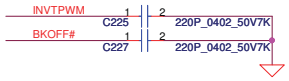


ESD PROTECT
CLOSE TO JLVDS1

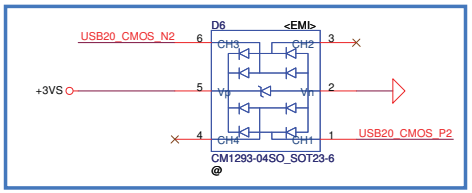


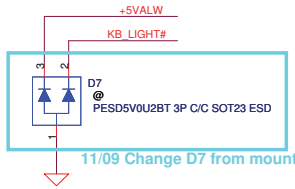






9/14 Add By Vivian(EMI suggest)

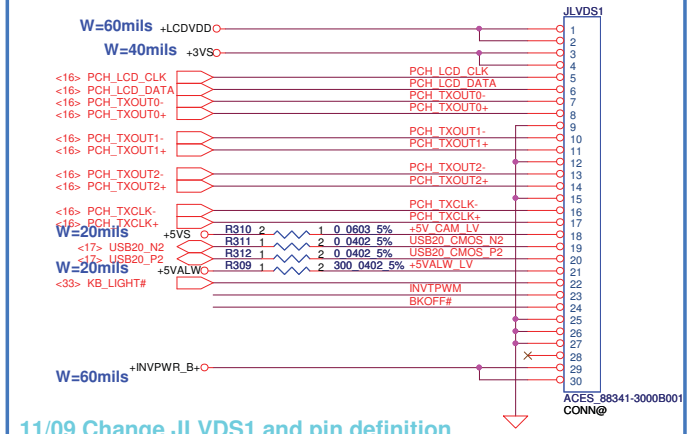




11/09 Change D7 from mount to @

LCD/PANEL BD. Conn.

Copy NAV50 Conn.



11/09 Change JLVDS1 and pin definition
12/04 Change JLVDS1 and pin definition

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 22 of 48

CRT Connector

10/29 Delete L14,L15,L16 (For layout spacing)

W=40mils

+5VS → D11 RB491D_SC59-3 → +R_CRT_VCC → F1 1.1A_6V_SMD1812P110TF → W=40mils → +CRT_VCC

C228 0.1U_0402_16V4Z

<16> PCH_CRT_R
<16> PCH_CRT_G
<16> PCH_CRT_B

10/29 Delete D8,D9,D10 (For layout spacing)

PCH_CRT_R → L18 FCM2012CF-800T06_2P → CRT_R_2
PCH_CRT_G → L19 FCM2012CF-800T06_2P → CRT_G_2
PCH_CRT_B → L22 FCM2012CF-800T06_2P → CRT_B_2

R313 150_0402_1%
R314 150_0402_1%
R315 150_0402_1%
150_0402_1%

C232 22P_0402_50V8J
C233 22P_0402_50V8J
C234 22P_0402_50V8J

C235 15P_0402_50V8J
C236 15P_0402_50V8J
C237 15P_0402_50V8J
Change to 12pf for DIS

Copy KAV60

JCRT1
SUYIN_070546FR015S290ZR
CONN@

C238 100P_0402_50V8J

DSUB_12
DSUB_15

C242 68P_0402_50V8J
C243 68P_0402_50V8J

0909 Change JCRT1 symbol from KAVAA

+CRT_VCC

C239 0.1U_0402_16V4Z

R317 10K_0402_5%

<16> PCH_CRT_HSYNC → U8 TC7SET125FUF SC70 5P BUFFER → CRT_HSYNC_R → R540 39_0402_5% → CRT_HSYNC_1

L23 BLM18AG121SN1D_2P → CRT_HSYNC_2
L24 BLM18AG121SN1D_2P → CRT_VSYNC_2

C240 10P_0402_50V8J
C241 10P_0402_50V8J

11/11 Correct L23,L24 footprint

+CRT_VCC

C244 0.1U_0402_16V4Z

<16> PCH_CRT_VSYNC → U9 TC7SET125FUF SC70 5P BUFFER → CRT_VSYNC_R → R541 39_0402_5% → CRT_VSYNC_1

11/03 Change U8,U9 from SA411250130 to SA00000RZ00

11/10 Add C518,C519 (EMI Recommend)

+3VS

C518 680P_0402_50V7K
C519 680P_0402_50V7K

PCH DDC PU 2.2K
on Page 17

+CRT_VCC

R538 2.2K_0402_5%
R539 2.2K_0402_5%

+3VS

Q2A
Q2B
2N7002DW-T/R7_SOT363-6

<16> PCH_CRT_DATA → PCH_CRT_DATA → DSUB_12
<16> PCH_CRT_CLK → PCH_CRT_CLK → DSUB_15

01/15 Change Q2 from
SB00000AR00 to SB00000D900
03/05 Change Q1,Q2 from SB00000D900 to SB00000DH00 (MFG Recommend)

9/10 Change from 2N7002E-T1-E3_SOT23-3
to 2N7002DW-T/R7_SOT363-6
Michael

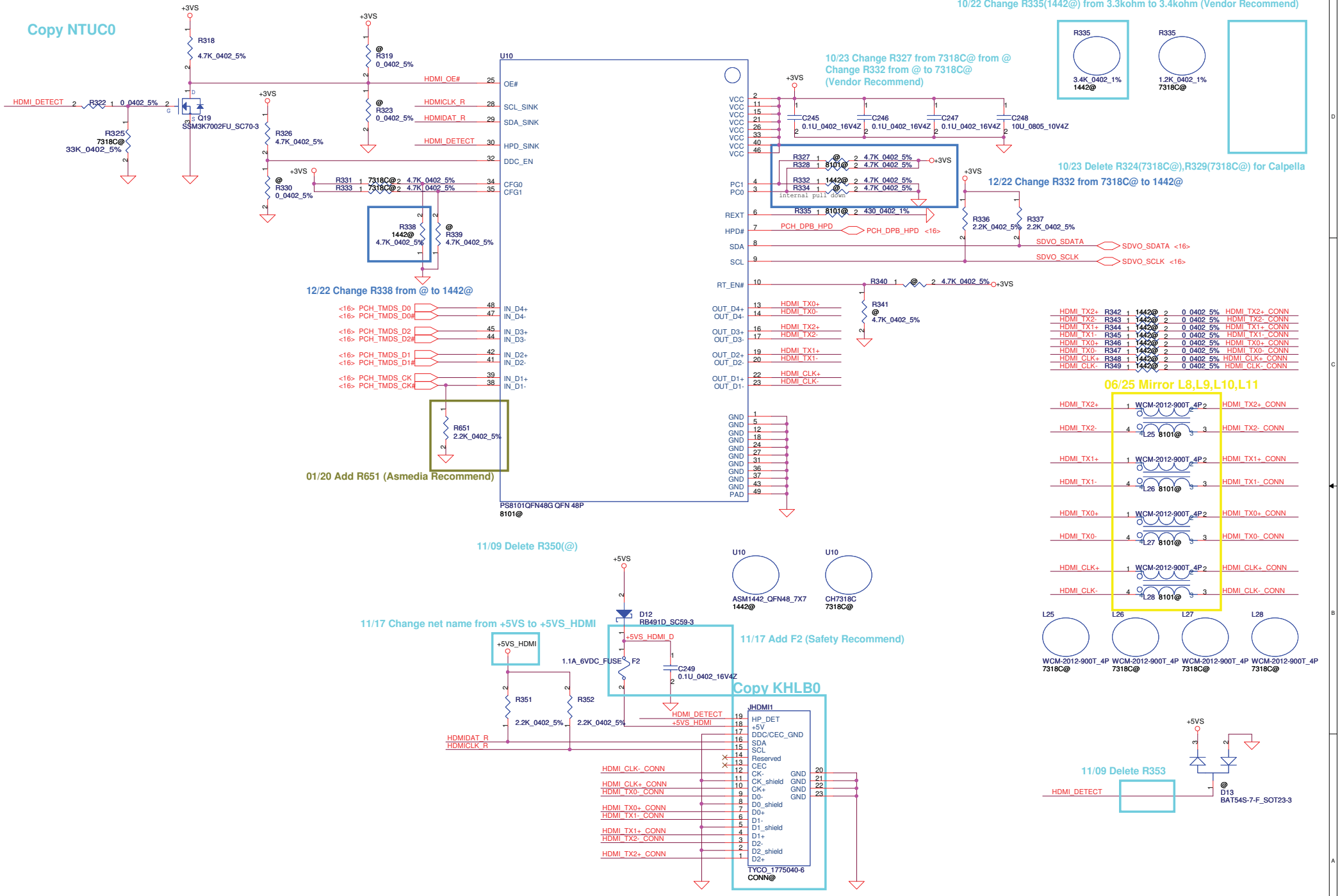
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 23 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/03/20

Compal Electronics, Inc.

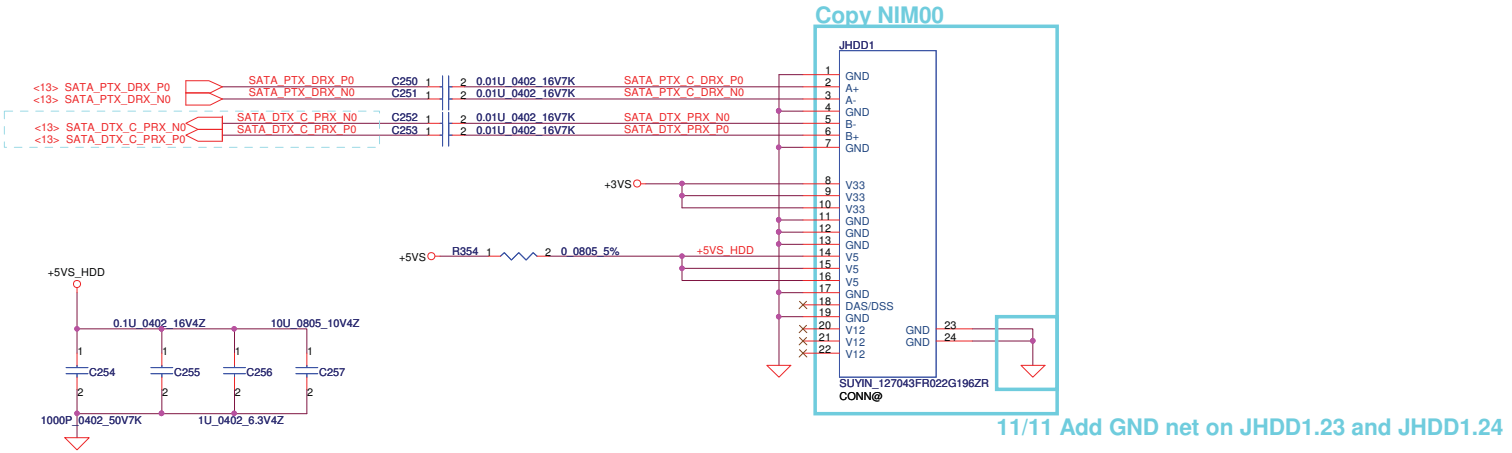
Title: **HDMI Level Shifter & Conn.**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 24 of 48

HDD

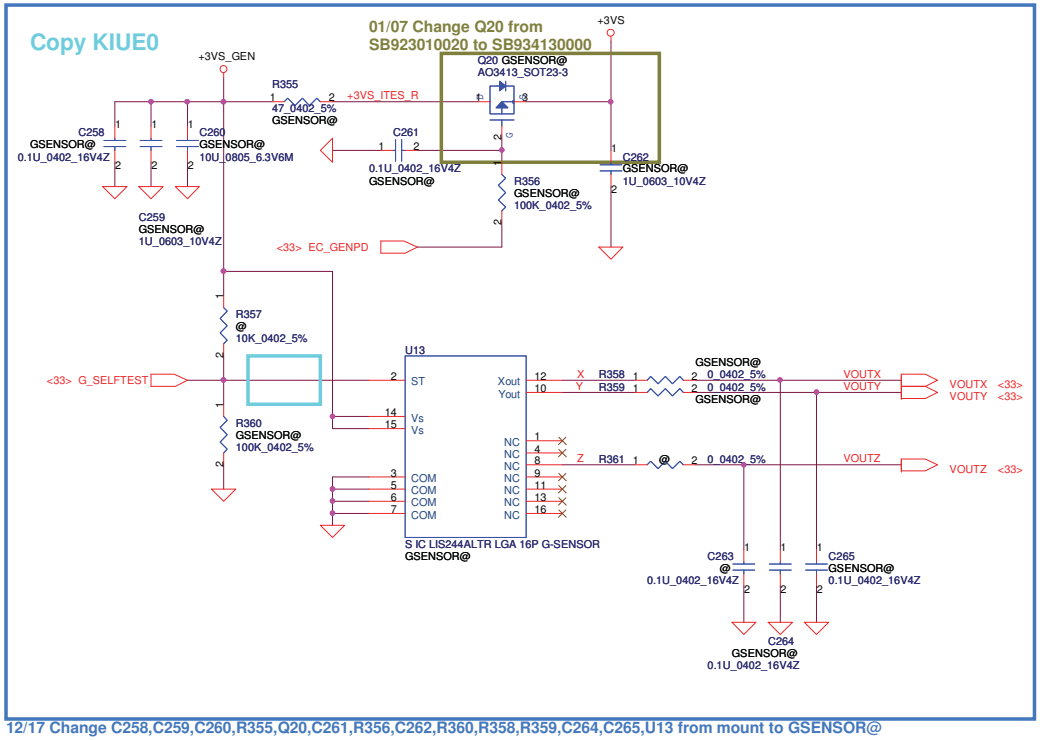
SATA HDD Conn.



11/11 Add GND net on JHDD1.23 and JHDD1.24

G-Sensor

11/11 Correct Q20 footprint



12/17 Change C258,C259,C260,R355,Q20,C261,R356,C262,R360,R358,R359,C264,C265,U13 from mount to GSENSOR@

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: **HDD Conn/G-Sensor**

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 25 of 48

LAN Power Circuit & Refer NTUC0

+3V_LAN

60mil

+3VALW R362 1 @ 2 0_0603_5%

1U_0402_6.3V4Z C269 — C270 — C271 — 1000P_0402_50V7K C272 — C493 10U_0805_10V4Z

10U_0805_10V4Z — 0.1U_0402_16V4Z

Q21 AO3413_SOT23-3

01/07 Change Q21 from SB923010020 to SB934130000

Place Close to Pin 1
Refer CRB

R363 1 2 10K_0402_5% EN_WOL# <33>

C273 0.1U_0402_16V4Z

01/15 Change R362 from mount to @
Change Q21,R363,C273 from @ to mount

+1.7_VDDCT — +1.7_LX

C266 10U_0805_10V4Z — C267 0.1U_0402_16V4Z — C288 1000P_0402_50V7K

+1.7_VDDCT — L33 4.7UH_SIA4012-4R7M_20% — +1.7_LX

Layout note : C266,C267,C268&L33 Close to Pin40

Note:
Place Close to LAN chip
L33 DCR< 0.15 ohm
Rate current of L33 > 1A

10/22 Remove R364

10/100_LINK_LED — R365 0_0402_5% — 1000_LINK_LED — LAN_LINK# <27>

LED2_CKR# — D14 CHP202UPT_SOT323-3

U14 Atheros 8151-AL1A AR8151-AL1A_QFN40_5X5

<14> PCIE_DTX_C_PRX_N1 — C274 .1U_0402_16V7K — PCIE_DTX_PRX_N1 — 29 TX_N
<14> PCIE_DTX_C_PRX_P1 — C275 .1U_0402_16V7K — PCIE_DTX_PRX_P1 — 30 TX_P
<14> PCIE_PTX_C_DRX_N1 — 36 RX_N
<14> PCIE_PTX_C_DRX_P1 — 35 RX_P
<14> CLK_PCIE_LAN# — R369 0_0402_5% — CLK_PCIE_LAN#_C — 32 REFCLK_N
<14> CLK_PCIE_LAN — R370 0_0402_5% — CLK_PCIE_LAN_C — 33 REFCLK_P
<17,32,37> PLT_RST_BUF# — PLT_RST_BUF# — 2 PERST#
<15,32,37> PCH_PCIE_WAKE# — R543 0_0402_5% — PCH_PCIE_WAKE#_R — 3 WAKE#
<33> PCH_PCIE_WAKE#_R
25 SMCLK
26 SMDATA

10/22 Change off-page direction of PCH_PCIE_WAKE# and PCH_PCIE_WAKE#_R

+3V_LAN — R374 2 @ 1 4.7K_0402_5% — LAN_TEST_RST — 28 TEST_RST
27 TESTMODE

11/02 Change R374 from mount to @

LAN_XTALO — 7 XTLO
LAN_XTALI — 8 XTLI

<14> LAN_CLKREQ# — LAN_CLKREQ# — 4 CLKREQ#

13 AVDDL
19 AVDDL
31 AVDDL
34 AVDDL
6 AVDDL_REG
41 GND

+1.1_AVDDL — C282 C283 C284 C285 C286 1U_0402_6.3V4Z C287 — 0.1U_0402_16V4Z

Layout note : C286&C287 Close to Pin6
C282 Close to Pin13
C283 Close to Pin19
C284 Close to Pin31
C285 Close to Pin34

R366 5.1K_0402_5% — no overclocking PD 5.1K

LED_0 38 — LAN_ACTIVITY# — LAN_ACTIVITY# <27>
LED_1 39 — 10/100_LINK_LED
LED_2 23 — LED2_CKR#

TRXN0 12 — MIDI0- — MIDI0- <27>
TRXP0 11 — MIDI0+ — MIDI0+ <27>
TRXN1 15 — MIDI1- — MIDI1- <27>
TRXP1 14 — MIDI1+ — MIDI1+ <27>
TRXN2 18 — MIDI2- — MIDI2- <27>
TRXP2 17 — MIDI2+ — MIDI2+ <27>
TRXN3 21 — MIDI3- — MIDI3- <27>
TRXP3 20 — MIDI3+ — MIDI3+ <27>

RBIAS 10 — LAN_RBIAS — R372 2.37K_0402_1%

VDD33 1 — +3V_LAN — +3V_LAN
+1.7_LX

LX 40 — +1.7_LX
+1.7_VDDCT

VDDCT 5 — +1.7_VDDCT — C279 0.1U_0402_16V4Z

DVDDL 24 — +1.1_DVDDL — C278 0.1U_0402_16V4Z
DVDDL_REG 37 — C280 1U_0402_6.3V4Z
C281 0.1U_0402_16V4Z
Near Pin37

AVDDH 16
AVDDH 22
AVDDH_REG 9 — +2.7_AVDDH — C288 1U_0402_6.3V4Z — C289 C290 C291 0.1U_0402_16V4Z

Layout note : C288&C289 Close to Pin9
C290 Close to Pin16
C291 Close to Pin22

+3V_LAN — R371 2 @ 1 4.7K_0402_5% — LAN_CLKREQ#

10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)

Place Close to LAN chip

MIDI0+	R378 49.9_0402_1%	C292	1000P_0402_50V7K
MIDI0-	R379 49.9_0402_1%	C293	0.1U_0402_16V4Z
MIDI1+	R380 49.9_0402_1%	C294	1000P_0402_50V7K
MIDI1-	R381 49.9_0402_1%	C295	0.1U_0402_16V4Z
MIDI2+	R382 49.9_0402_1%	C296	1000P_0402_50V7K
MIDI2-	R383 49.9_0402_1%	C297	0.1U_0402_16V4Z
MIDI3+	R384 49.9_0402_1%	C298	1000P_0402_50V7K
MIDI3-	R385 49.9_0402_1%	C299	0.1U_0402_16V4Z

LAN_XTALI — LAN_XTALO — Y3 25MHZ_20PF_7A25000012 — C276 27P_0402_50V8J — C277 27P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LAN AR8151

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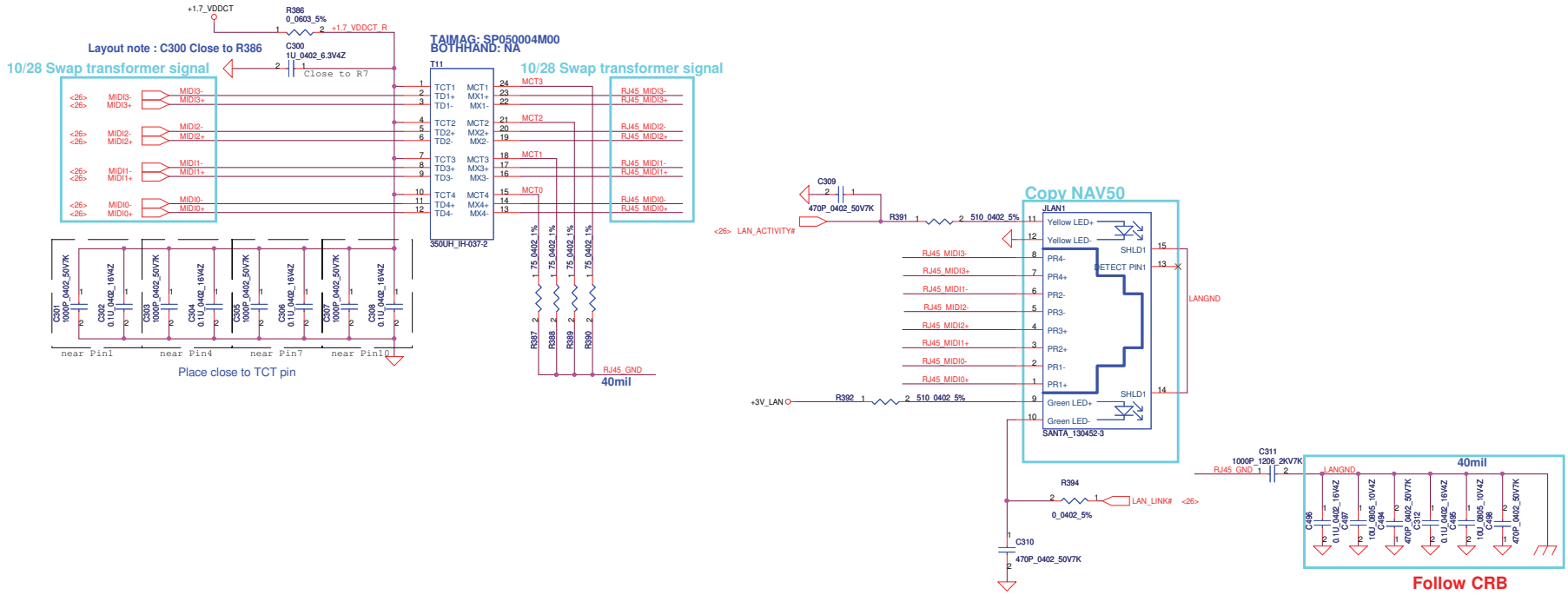
Copy NIMUA



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 27 of 48

CR_REFE must far away from
48MHz clock trace.
Place CR1,RR2 close to U15 Pin1

11/04 Change CR1 from SE071101J1M to SE071101J80

11/09 Delete RR1(@)

CR1 100P_0402_50V8J

RR2 6.19K_0402_1%

Pin1 and pin6 of U15 trace width = 20mil

+3VS RR3 0_0603_5%

40mil

40mil

+3VS_CR

<17> USB20_N5
<17> USB20_P5

+VCC_3IN1

40mil

CR2 0.1U_0402_16V4Z

CR3 10U_0805_10V6K

Place CR2,CR3 close to U15 Pin4

CR4 0.1U_0402_16V4Z

CR5 1U_0402_6.3V6K

Place CR4,CR5 close to U15 Pin5,6

+V18_CR : 20mil

XD_RDY_SD_WP_MS_CLK_R RR5 0_0402_5%

U15

CR_REFE → REFE
DM
DP
3V3_IN
CARD_3V3
V18
XD_CD#
SP1
SP2
SP3
SP4
SP5
GPIO0
CLK_IN
XD_D7
SP14 XD_D6_MS_BS
SP13 XD_D5_SD_D2_MS_D5
SP12 XD_D4_SD_D3_MS_D1
SP11 XD_D3_SD_D4_MS_D4
SP10 XD_D2_SD_CMD
SP9 XD_D1_SD_D5_MS_D0
SP8 XD_D0_SD_CLK_MS_D2
SP7 XD_WP_SD_D6_MS_D6
SP6 XD_WE#_SD_CD#
EPAD
RTS5138-GR_QFN24_4X4

+VCC_3IN1
+V18_CR
XD_CD#
XD_RDY_SD_WP_MS_CLK
XD_RE#_MS_INS#
XD_CE#_SD_D1
XD_CLE_SD_D0_MS_D7
XD_ALE_SD_D7_MS_D3

11/09 Delete RR4

CLK_48M → CLK_48M <12>

XD_D7

RR6 0_0402_5%

XD_D0_SD_CLK_MS_D2_R

Ground pad must have 4 via

no more than 2 via on all signal trace

Pin8 and Pin15 Keep trace routing lengths as short as possible,
Avoid via and layer changes

Close to U15 pin24

CLK_48M
RR7 22_0402_5%
CR6 10P_0402_50V8J

12/22 Mount RR7,CR6

7 in 1 Card Reader

Copy NCQF0

20mil +VCC_3IN1

20mil +VCC_3IN1

JCR1

XD-VCC
XD10-D0
XD11-D1
XD12-D2
XD13-D3
XD14-D4
XD15-D5
XD16-D6
XD17-D7
XD07-WE
XD08-WP
XD06-ALE
XD01-CD
XD02-R/B
XD03-RE
XD04-CE
XD05-CLE
XD GND
XD GND
SD CD/WP GND
SD CD/WP GND
SD4-VDD
MS9-VCC
SD5-CLK
SD7-DAT0
SD8-DAT1
SD9-DAT2
SD1-DAT3
SD2-CMD
SD-CD
SD-WP
SD6-VSS
SD3-VSS
MS8-SCLK
MS4-DATA0
MS3-DATA1
MS5-DATA2
MS7-DATA3
MS6-INS
MS2-BS
MS1-VSS
MS10-VSS

XD_D0_SD_CLK_MS_D2
XD_D1_SD_D5_MS_D0
XD_D2_SD_CMD
XD_D3_SD_D4_MS_D4
XD_D4_SD_D3_MS_D1
XD_D5_SD_D2_MS_D5
XD_D6_MS_BS
XD_D7
XD_WE#_SD_CD#
XD_WP_SD_D6_MS_D6
XD_ALE_SD_D7_MS_D3
XD_CD#
XD_RDY_SD_WP_MS_CLK
XD_RE#_MS_INS#
XD_CE#_SD_D1
XD_CLE_SD_D0_MS_D7

T-SOL_144-1300302600_NR
CONN@

RR10 @ 100K_0402_5%

CR11 0.1U_0402_16V4Z

Close to JCR1

CR8 0.1U_0402_16V4Z

CR7 0.1U_0402_16V4Z

EMI reserved Close to JCR1

XD_D0_SD_CLK_MS_D2_R
XD_RDY_SD_WP_MS_CLK_R

RR8 @ 10_0402_5%

RR9 @ 10_0402_5%

CR9 @ 10P_0402_50V8J

CR10 @ 10P_0402_50V8J

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Card Reader/7-IN-1 Socket

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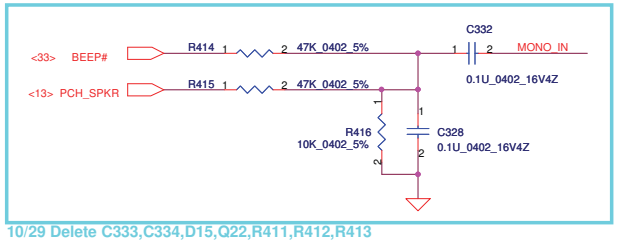
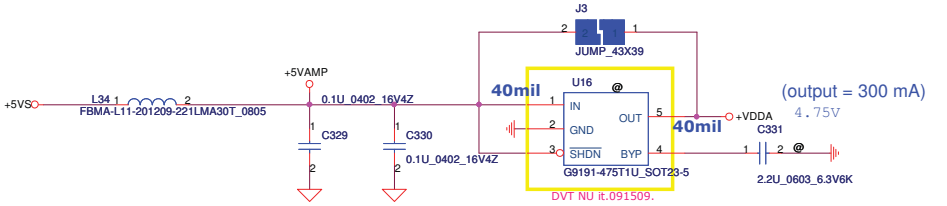
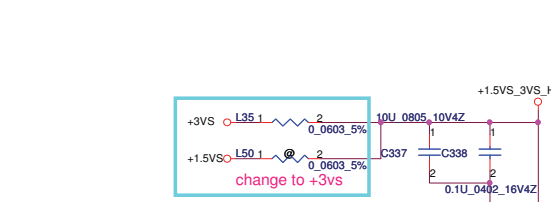
10/29 Follow NTUC0

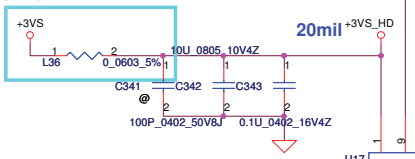


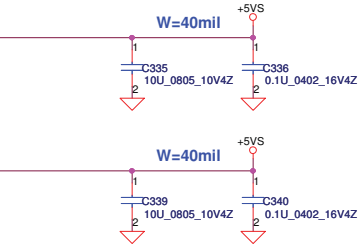
10/29 Delete C333,C334,D15,Q22,R411,R412,R413
Change R414,R415 from 560ohm to 47kohm
Change C332,C328 from 1uF to 0.1uF

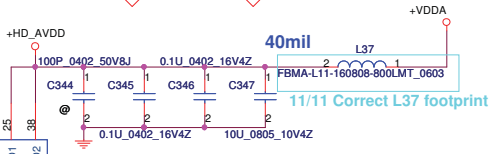




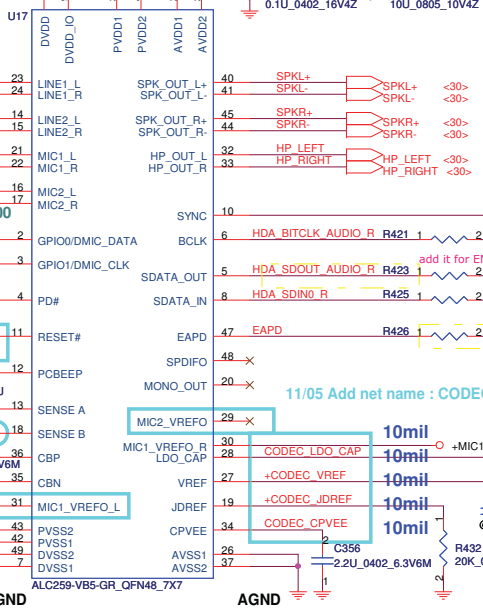
11/09 Change L35,L36,L50 from SM010015410 to SD013000080







11/11 Correct L37 footprint



11/10 Change R465,R466 from SE053475Z80 to SE107475M80 (Realtek Recommend)

02/26 Change R422 from SD028000080 to SM01000CY00

01/07 Change C351.2 from R422.2 to R422.1

01/07 Add R648(@) to +HD_AVDD (Realtek Recommend)

add it.070709

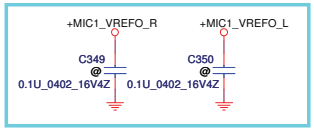
10/30 Change C352 GND from AGND to GND

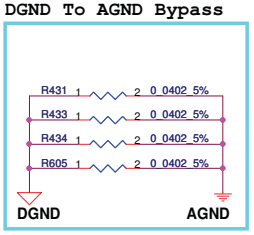
change pin31 and pin28

10/21 Change U17 to SA00003QR00 Symbol

03/04 Change U17 from SA00003QR00 to SA00003QR10

11/05 Add net name : CODEC_LDO_CAP,+CODEC_VREF,+CODEC_JDREF,CODEC_CPVEE





11/02 Change R429,R430,R431,R433,R434,R605 from 0_0603 to 0_0402 (Layout Spacing)
11/17 Delete R429,R430

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: HDA Codec ALC259Q-GR

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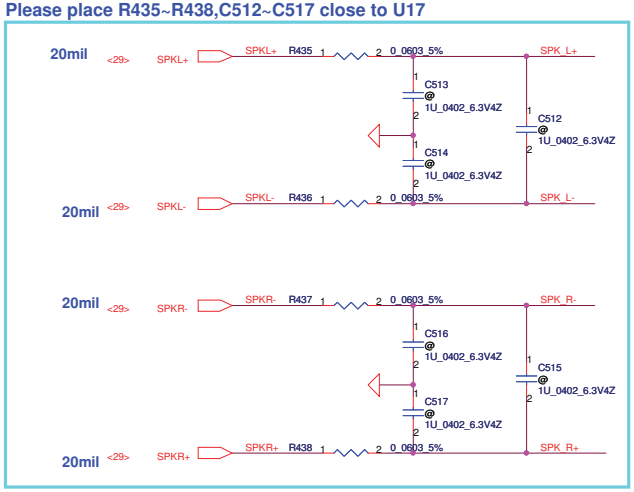
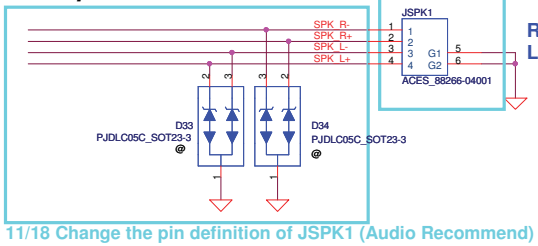
11/11 Change R435~R438 from SM010012010 to SD013000080
11/10 Add C512~C517(@) for EMI (Follow Realtek CRB)
Please place R435~R438,C512~C517 close to U17



Int. Speaker Conn.

Copy KTV00

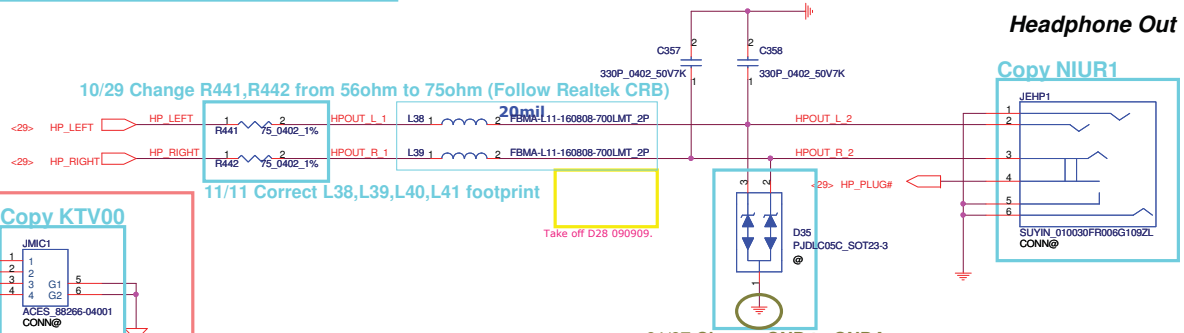


11/18 Change the pin definition of JSPK1 (Audio Recommend)
11/18 Swap D33

Headphone Out

Copy NIUR1

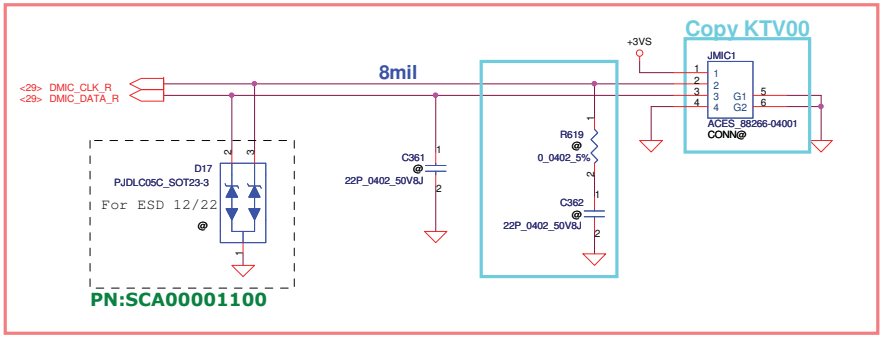
10/29 Change R441,R442 from 56ohm to 75ohm (Follow Realtek CRB)



11/11 Correct L38,L39,L40,L41 footprint
Take off D28 090909.

01/07 Change GND to GNDA

Copy KTV00

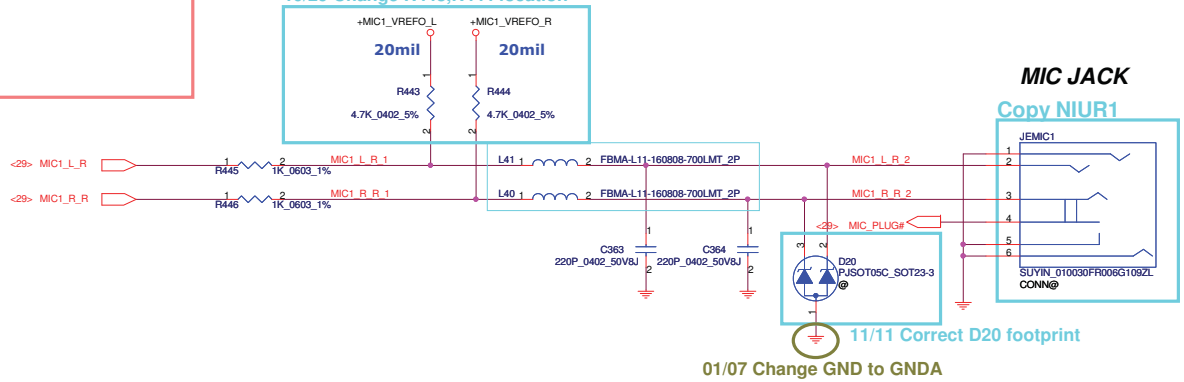


PN:SCA00001100

10/29 Short D18,D19 (Follow Realtek CRB)
10/29 Change R443,R444 location

MIC JACK

Copy NIUR1



11/11 Correct D20 footprint

01/07 Change GND to GNDA

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Audio Jack/MIC Conn/SPK Conn

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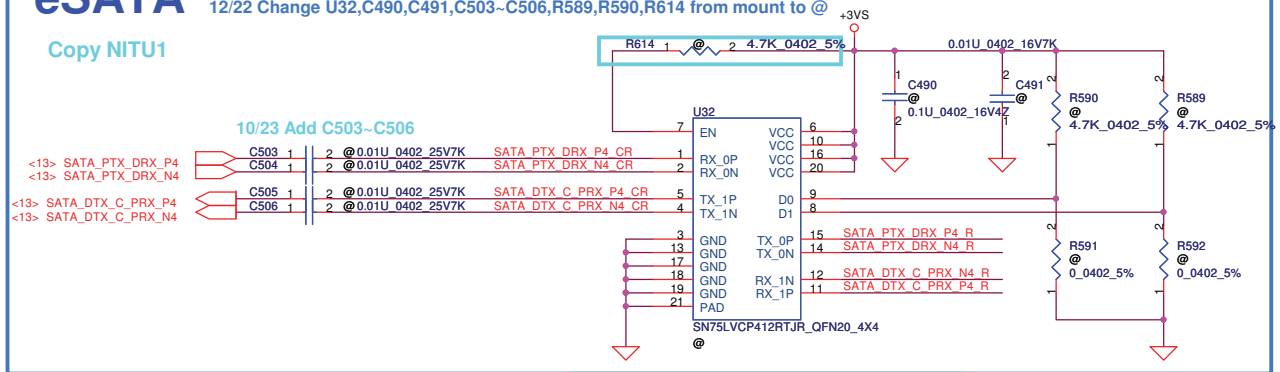
eSATA

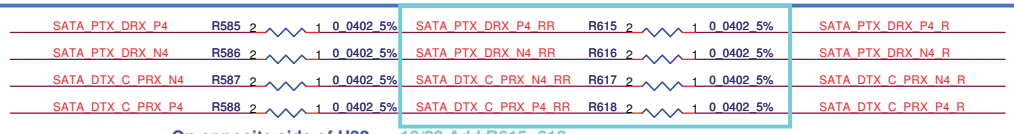
10/22 Add R614, change R590,R589 from 0ohm to 4.7kohm (Vendor Recommend)

12/22 Change U32,C490,C491,C503~C506,R589,R590,R614 from mount to @

Copy NITU1

10/23 Add C503~C506





On opposite side of U32

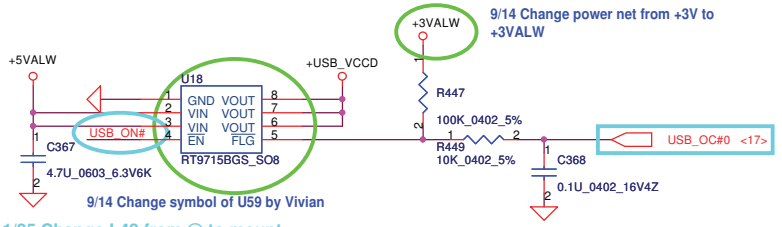
10/23 Add R615~618

12/22 Change R585~R588,R615~R618 from @ to mount

TI:D0 D1					SN75LVCP412		
EN	BA	BB			CHANNEL 0	CHANNEL 1	
0	X	X			Low-power	Low-power	
1	0	0			0dB	0dB	(Default)
1	1	0			2.5dB pre-emphasis	0dB	
1	0	1			0dB	2.5dB pre-emphasis	
1	1	1			2.5dB pre-emphasis	2.5dB pre-emphasis	

9/14 Change power net from +3V to +3VALW

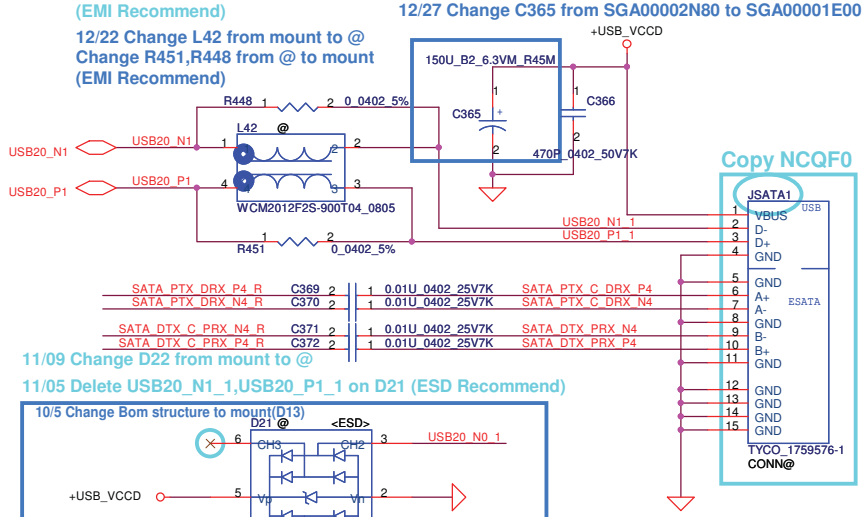
9/14 Change symbol of U59 by Vivian



11/25 Change L42 from @ to mount
Change R451,R448 from mount to @
(EMI Recommend)

12/22 Change L42 from mount to @
Change R451,R448 from @ to mount
(EMI Recommend)

12/27 Change C365 from SGA00002N80 to SGA00001E00

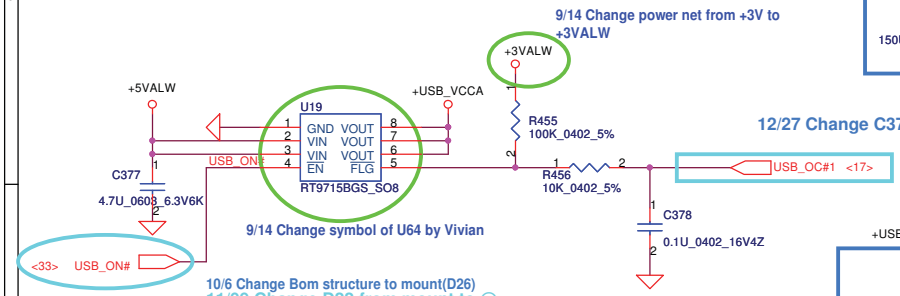


11/09 Change D22 from mount to @

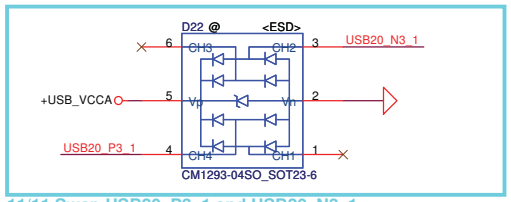
11/05 Delete USB20_N1_1,USB20_P1_1 on D21 (ESD Recommend)

10/5 Change Bom structure to mount(D13)

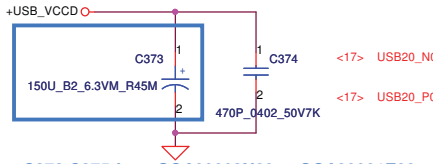
USB Port



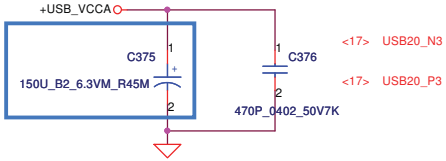
10/6 Change Bom structure to mount(D26)
11/09 Change D22 from mount to @

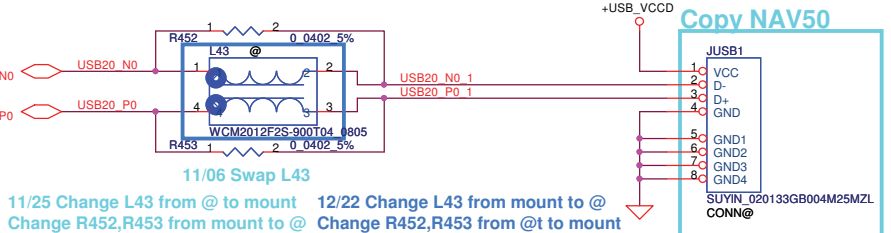


11/11 Swap USB20_P3_1 and USB20_N3_1



12/27 Change C373,C375 from SGA00002N80 to SGA00001E00

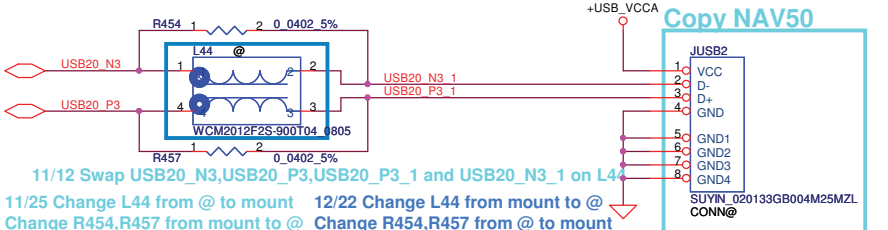




11/06 Swap L43

11/25 Change L43 from @ to mount
Change R452,R453 from mount to @
(EMI Recommend)

12/22 Change L43 from mount to @
Change R452,R453 from @t to mount
(EMI Recommend)



11/12 Swap USB20_N3,USB20_P3,USB20_P3_1 and USB20_N3_1 on L44

11/25 Change L44 from @ to mount
Change R454,R457 from mount to @
(EMI Recommend)

12/22 Change L44 from mount to @
Change R454,R457 from @ to mount
(EMI Recommend)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.			
Title	USB / BT / eSATA		
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WLAN

10/22 Add Net : BT_ACTIVE and R613, Delete T13
11/10 Add R631(@)

Copy NTUC0

JWLAN1

FOX_AS0B226-S40N-7F

11/14 Add +1.5VS

+3VS_WLAN R458 0_0603_5% +3VS
R459 0_0603_5% +3VALW

R460 0_0402_5%
<15,26,37> PCH_PCIE_WAKE# → PCH_PCIE_WAKE# 1 @ 2
R631 @ 0_0402_5% BT_ACTIVE_R
R613 @ 0_0402_5% BT_ACTIVE_R
<35> BT_ACTIVE
<14> MINI1_CLKREQ# → MINI1_CLKREQ#

<14> CLK_PCIE_MINI1# → CLK_PCIE_MINI1#
<14> CLK_PCIE_MINI1 → CLK_PCIE_MINI1

<14> PCIE_DTX_C_PRX_N2 → PCIE_DTX_C_PRX_N2
<14> PCIE_DTX_C_PRX_P2 → PCIE_DTX_C_PRX_P2

<14> PCIE_PTX_C_DRX_N2 → PCIE_PTX_C_DRX_N2
<14> PCIE_PTX_C_DRX_P2 → PCIE_PTX_C_DRX_P2

+3VS_WLAN

<33> EC_TX_P80_DATA → EC_TX_P80_DATA
<33> EC_RX_P80_CLK → EC_RX_P80_CLK
R634 100K_0402_5%

11/10 Change net : EC_TX_P80_DATA from JWLAN1.17 to JWLAN1.49
Add R634

+3VS_WLAN

WL_OFF# → WL_OFF# <33>
PLT_RST_BUF# → PLT_RST_BUF# <17,26,37>
R632 0_0402_5% +3VS_WLAN
R633 @ 0_0402_5% +3VALW

11/10 Add R632,R633(@)

PCH_SMBCLK → PCH_SMBCLK <12,14,37>
PCH_SMBDATA → PCH_SMBDATA <12,14,37>

11/17 Add GND on JWLAN1.40

USB20_N8 → USB20_N8 <17>
USB20_P8 → USB20_P8 <17>

WWAN_LED# R646 @ 0_0402_5%
WLAN_LED# R647 0_0402_5%
WLAN_LED# <35>

12/16 Add R646(@),R647

10/22 Reserve pull-up resister R611(@) for WLAN_LED#
01/21 Change R611 from @ to mount
Change R461 from mount to @

+5VS (9~16mA) +3VS
R461 @ 10K_0402_5%
R611 10K_0402_5%
WLAN_LED#

+3VS_WLAN
0.1U_0402_16V4Z
C379 4.7U_0805_10V4Z
C380 0.1U_0402_16V4Z
C381

10/5 Add C13/C15/C16 by Vivian

WWAN

+3VS_WWAN R462 0_0603_5% +3VS

12/15 Reserve R642(@)
12/16 Add R643(@)

Copy NTUC0

JWWAN1

FOX_AS0B226-S40N-7F

<15,26,37> PCH_PCIE_WAKE# → R643 @ 0_0402_5% PCH_PCIE_WAKE#_3G

11/17 Swap SATA port5 signals

+3VS R642 @ 10K_0402_5%

<13> SATA_PTX_DRX_P5 → C489 0.01U_0402_16V7K SATA_PTX_C_DRX_P5
<13> SATA_PTX_DRX_N5 → C488 0.01U_0402_16V7K SATA_PTX_C_DRX_N5
<13> SATA_DTX_C_PRX_N5 → C487 0.01U_0402_16V7K SATA_DTX_PRX_N5
<13> SATA_DTX_C_PRX_P5 → C486 0.01U_0402_16V7K SATA_DTX_PRX_P5
<13> SATA_DTX_C_PRX_P1 → C382 0.01U_0402_16V7K SATA_DTX_PRX_P1
<13> SATA_DTX_C_PRX_N1 → C384 0.01U_0402_16V7K SATA_DTX_PRX_N1
<13> SATA_PTX_DRX_N1 → C385 0.01U_0402_16V7K SATA_PTX_C_DRX_N1
<13> SATA_PTX_DRX_P1 → C386 0.01U_0402_16V7K SATA_PTX_C_DRX_P1

+3VS_WWAN

11/17 Change SSD_DET# from JWWAN1.47 to JWWAN1.51

<33> SSD_DET#
+3VALW R469 @ 100K_0402_5%
+3VS R545 @ 100K_0402_5%

+3VS_WWAN
+1.5VS

+UIM_PWR
UIM_DATA
UIM_CLK
UIM_RST
UIM_VPP

12/15 Add PLT_RST_BUF# on JWWAN.22
12/16 Add R644(@),R645(@)

R463 0_0402_5%
PLT_RST_BUF# → WWAN_OFF# <33>
PLT_RST_BUF# <17,26,37>
R464 0_0402_5% +3VS_WWAN
R465 @ 0_0402_5% +3VALW

R644 @ 0_0402_5%
R645 @ 0_0402_5%
PCH_SMBCLK <12,14,37>
PCH_SMBDATA <12,14,37>

USB20_N13 → USB20_N13 <17>
USB20_P13 → USB20_P13 <17>

WWAN_LED# → WWAN_LED# <35>
R467 @ 100K_0402_5% +5VS
R468 100K_0402_5% +3VS

10/28 Change Net from USB20_N9,USB20_P9 to USB20_N13,USB20_P13

01/22 Change R468 from @ to mount
Change R467 from mount to @

Copy NTUC0

SIM Card Conn.

JSIM1

UIM_VPP
UIM_DATA
R466 @ 10K_0402_5%
+UIM_PWR

GND VPP I/O DET
VCC RST CLK
GND GND

+UIM_PWR
UIM_RST
UIM_CLK
C383 1U_0603_10V4Z

TAITW_PMPAT6-06GLBS7N14N0 CONN@

Reserve for SIM card does not meet rise time and pull-up is needed.

+3VS_WWAN
0.1U_0402_16V4Z
C552 4.7U_0805_10V4Z
C553
C554 0.1U_0402_16V4Z

01/19 Add C552,C553,C554 for +3VS_WWAN

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.
Title: WLAN/WWAN
Size: Custom
Document Number: NAU00 M/B LA-6101P Schematics
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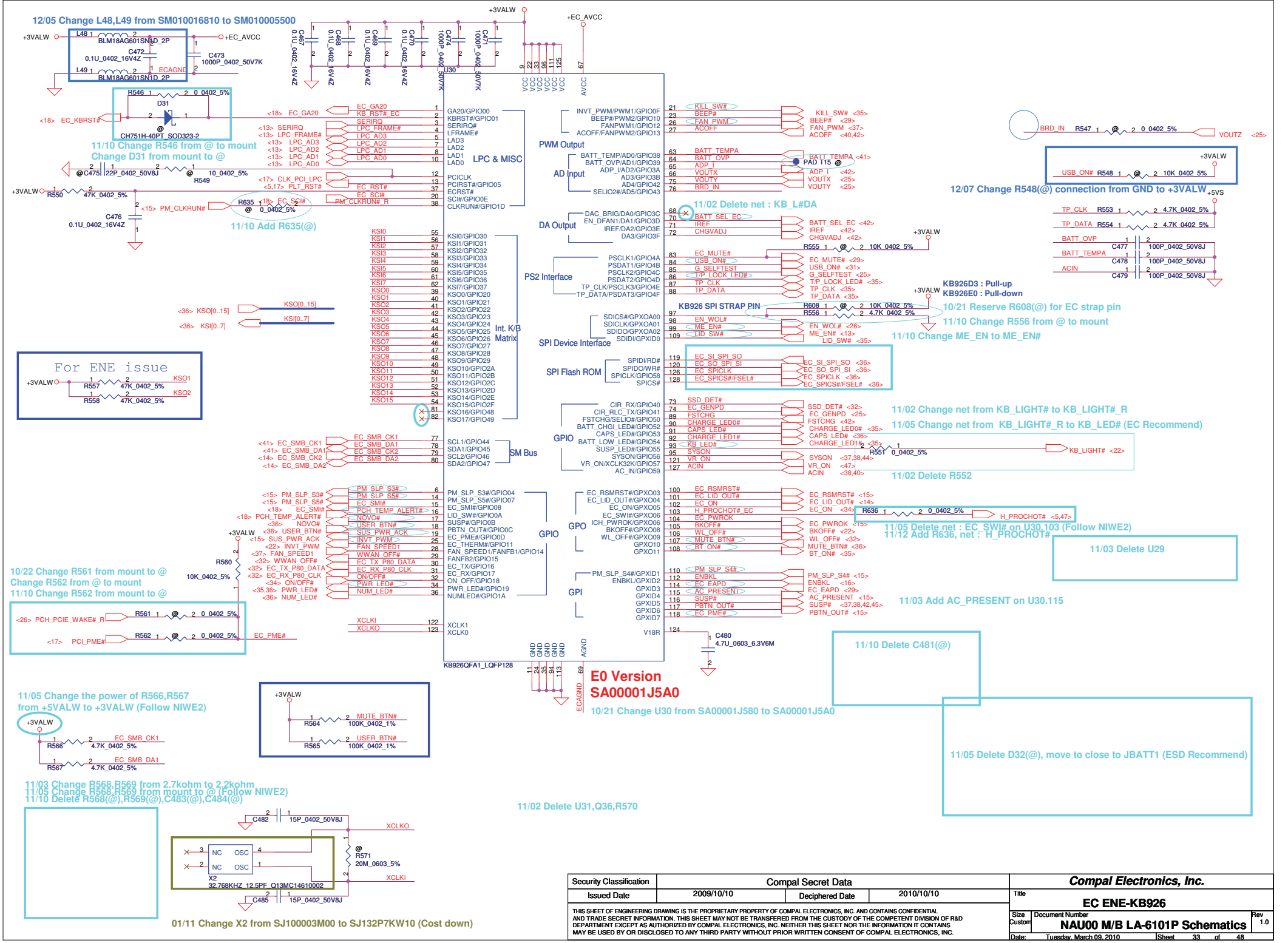
12/05 Change L48,L49 from SM010016810 to SM010005500
11/10 Change R546 from @ to mount
Change D31 from mount to @
11/10 Add R635(@)
11/02 Delete net : KB_L#DA
12/07 Change R548(@) connection from GND to +3VALW
KB926D3 : Pull-up
KB926E0 : Pull-down
KB926 SPI STRAP PIN
10/21 Reserve R608(@) for EC strap pin
11/10 Change R556 from @ to mount
11/10 Change ME_EN to ME_EN#
For ENE issue
11/02 Change net from KB_LIGHT# to KB_LIGHT#_R
11/05 Change net from KB_LIGHT#_R to KB_LED# (EC Recommend)
11/02 Delete R552
11/05 Delete net : EC_SWI# on U30.103 (Follow NIWE2)
11/12 Add R636, net : H_PROCHOT#
11/03 Delete U29
11/03 Add AC_PRESENT on U30.115
11/10 Delete C481(@)
10/22 Change R561 from mount to @
Change R562 from @ to mount
11/10 Change R562 from mount to @
11/05 Change the power of R566,R567
from +5VALW to +3VALW (Follow NIWE2)
11/03 Change R568,R569 from 2.7kohm to 2.2kohm
11/05 Change R568,R569 from mount to @ (Follow NIWE2)
11/10 Delete R568(@),R569(@),C483(@),C484(@)
11/02 Delete U31,Q36,R570
11/05 Delete D32(@), move to close to JBATT1 (ESD Recommend)
01/11 Change X2 from SJ100003M00 to SJ132P7KW10 (Cost down)
E0 Version
SA00001J5A0
10/21 Change U30 from SA00001J580 to SA00001J5A0
KB926QFA1_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
Security Classification
Compal Secret Data
Issued Date
2009/10/10
Deciphered Date
2010/10/10
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Custom
Document Number
NAU00 M/B LA-6101P Schematics
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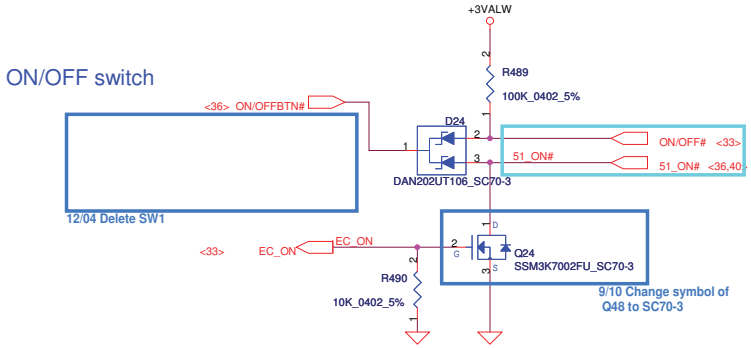
Power Button



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Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Power OK/PBN/TP Lock/LED

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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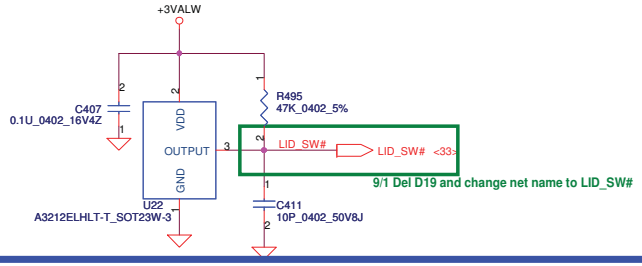
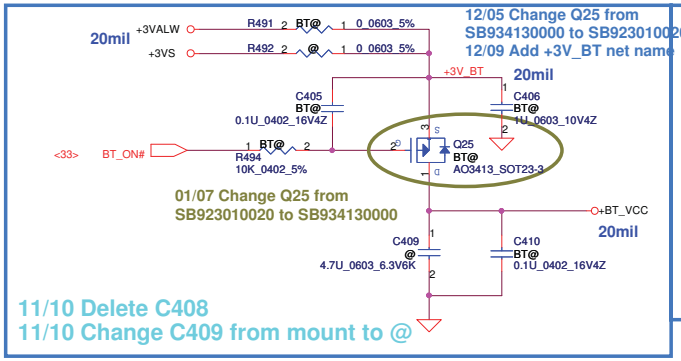
Lid Switch

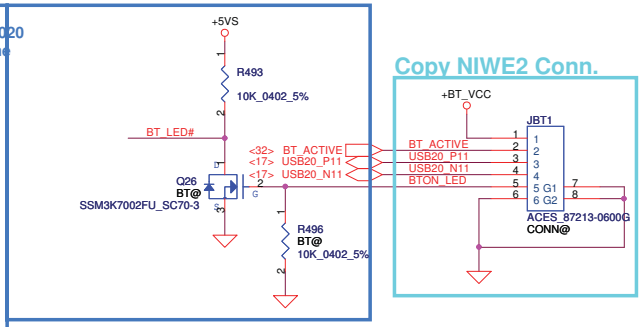
(Hall Effect Switch)



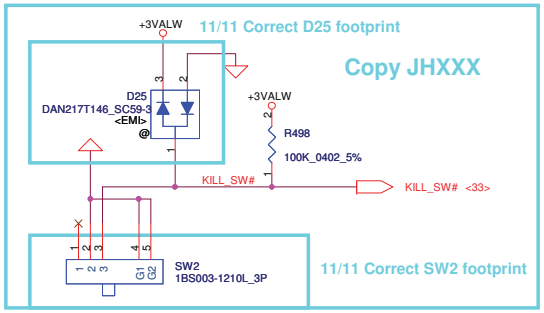
BT

12/17 Change R491,C405,R494,C406,Q25,C410,Q26,R496 from mount to BT@



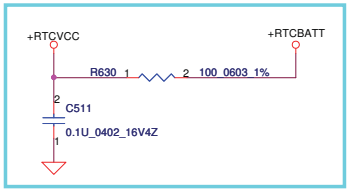


KILL Switch



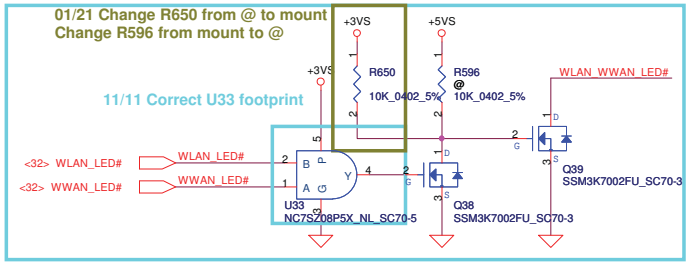
RTC

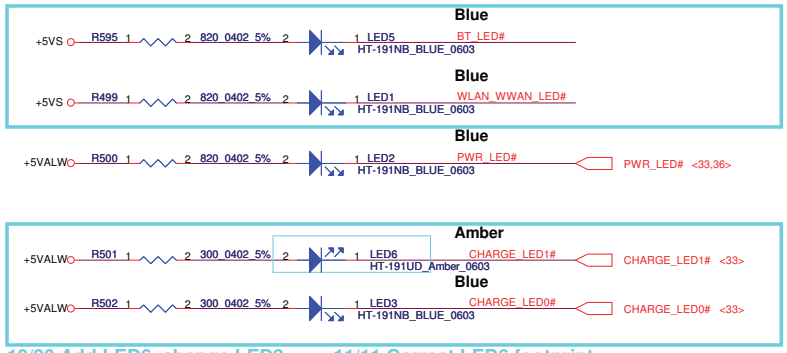
11/10 Delete D26,C412,R497, Add R630,C511 (Follow NIWE2)



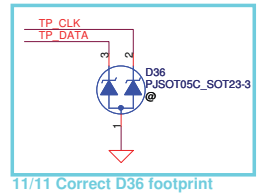
LED

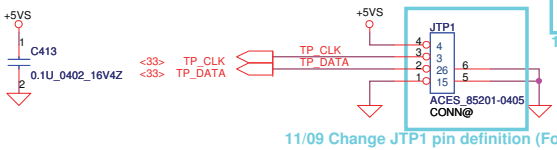
01/20 Add R650(@)

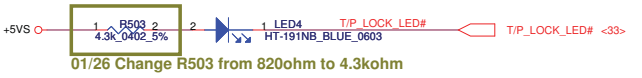




Touch Pad







Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LID/RTC/BT/TP/KILL SW/LED

Size	Document Number	Rev
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INT_KBD Conn.

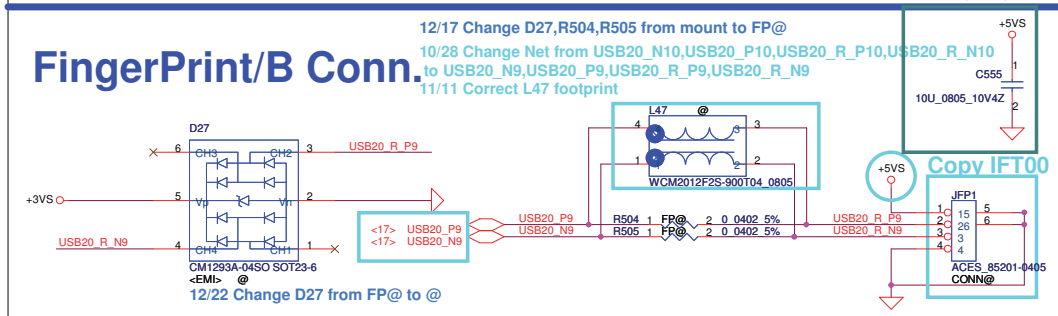
03/02 Add C555 (10uF) for FP power

FingerPrint/B Conn.

12/17 Change D27,R504,R505 from mount to FP@

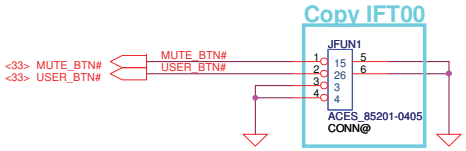
10/28 Change Net from USB20_N10,USB20_P10,USB20_R_P10,USB20_R_N10 to USB20_N9,USB20_P9,USB20_R_P9,USB20_R_N9

11/11 Correct L47 footprint

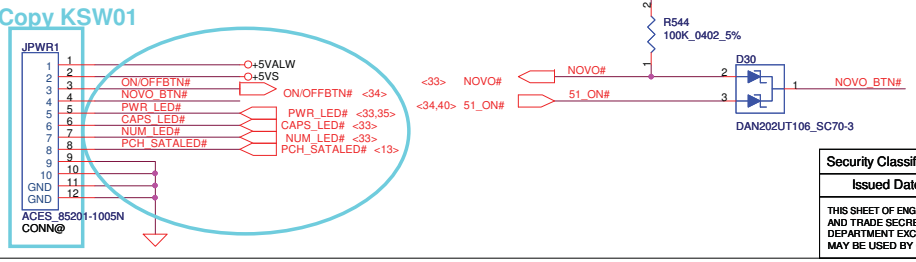


12/22 Change D27 from FP@ to @

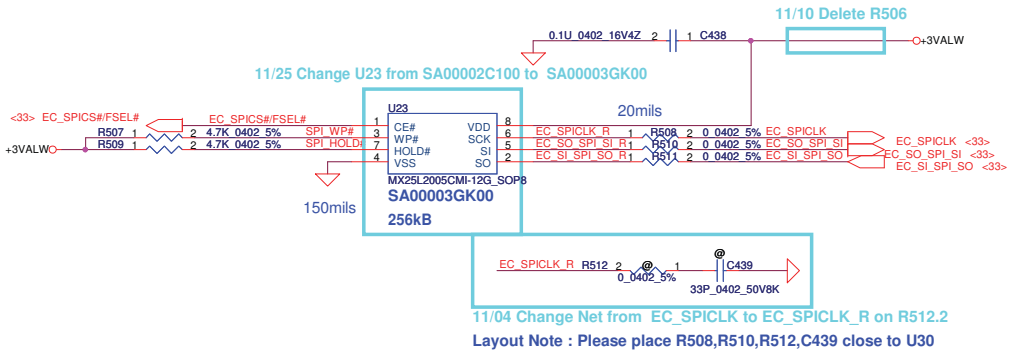
Function/B Conn.



Power/B Conn.



EC SPI ROM



11/04 Change Net from EC_SPICLK to EC_SPICLK_R on R512.2

Layout Note : Please place R508,R510,R512,C439 close to U30

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.	
Title	BIOS/KBD/Fun_B/PWR_B/FP_B
Size B	Document Number: NAU00 M/B LA-6101P Schematics
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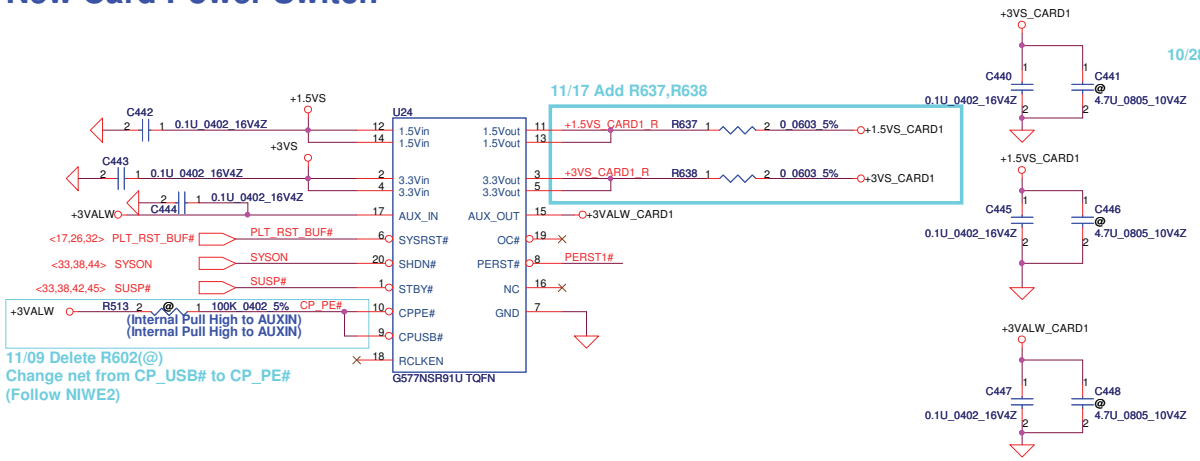
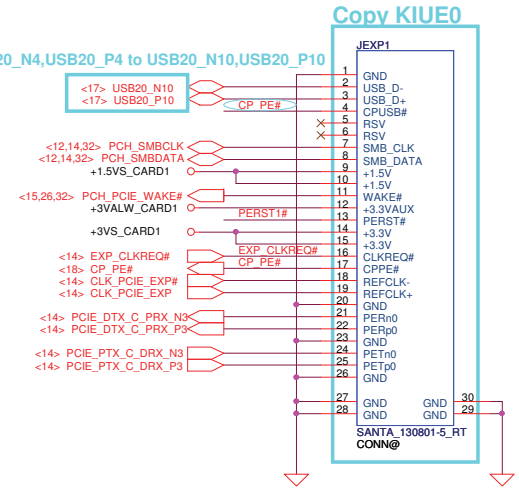
Date: Tuesday, March 09, 2010	Sheet 36 of 48

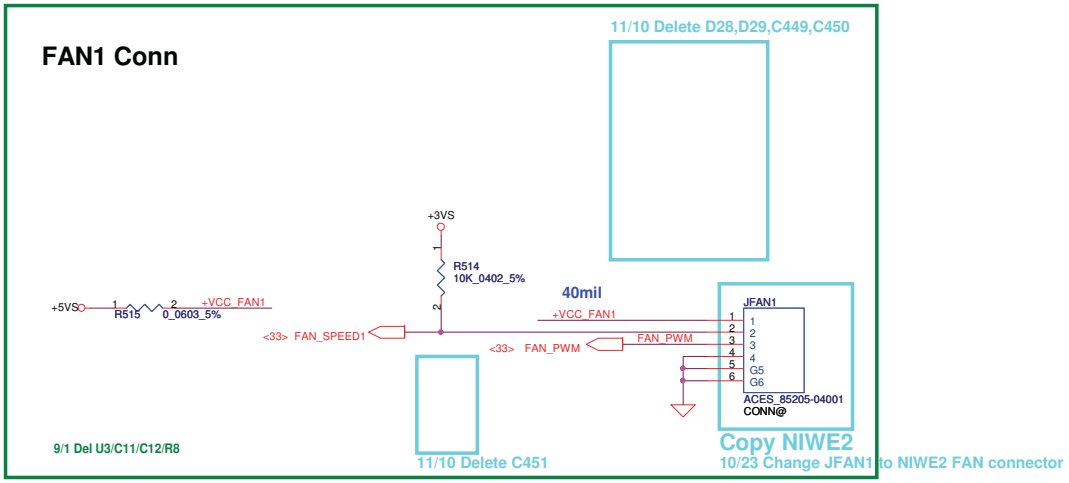
New Card Power Switch

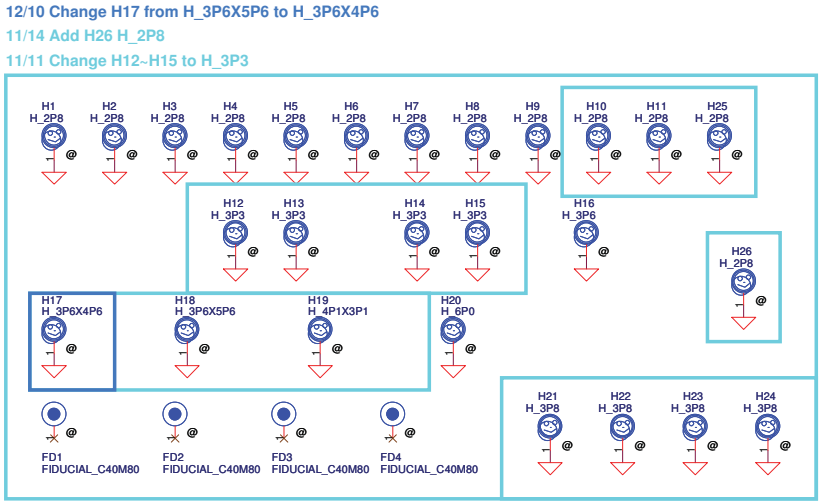


New Card Socket



FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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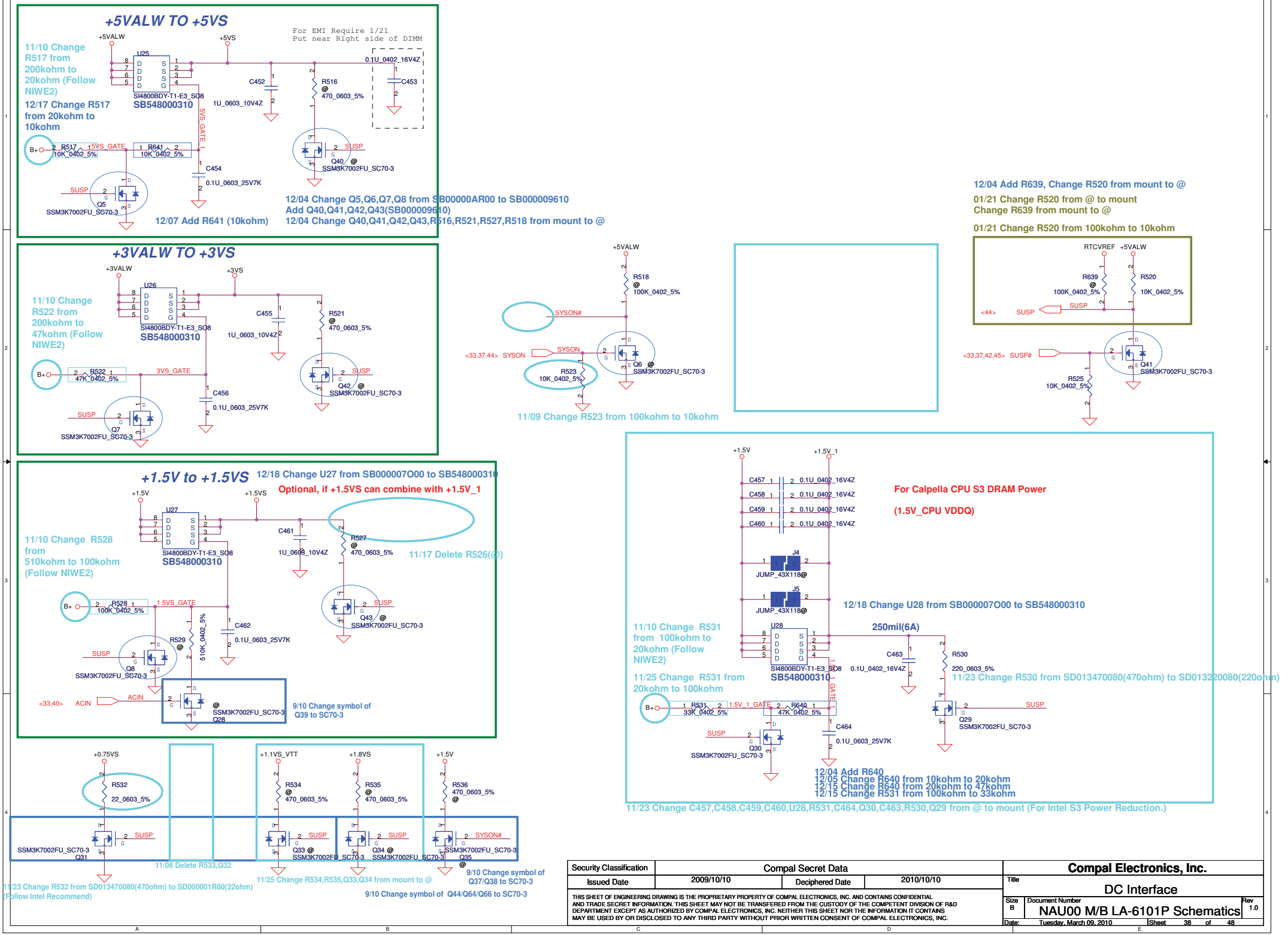


Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

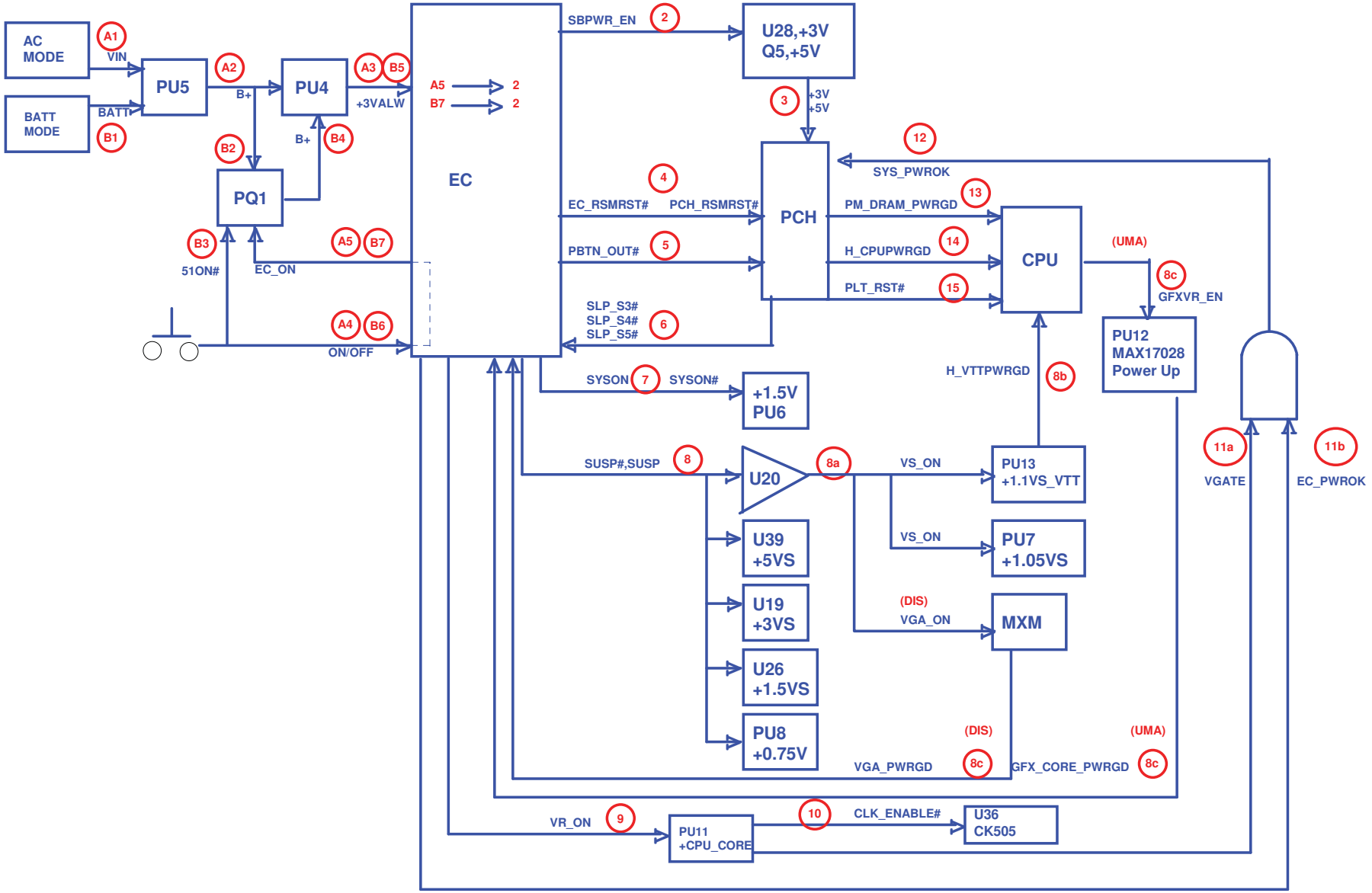
Title: DC Interface

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 38 of 48

COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



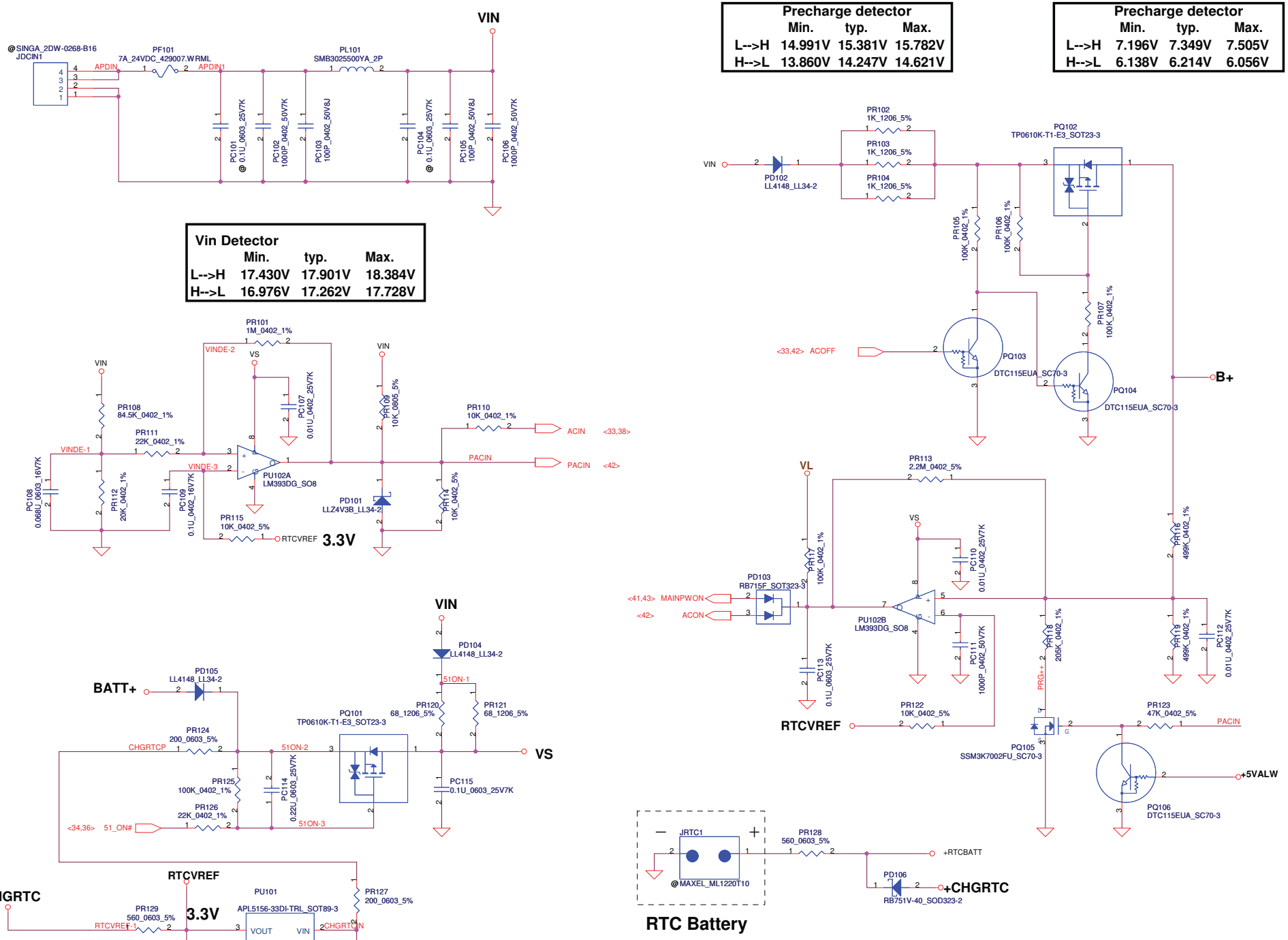
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 39 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

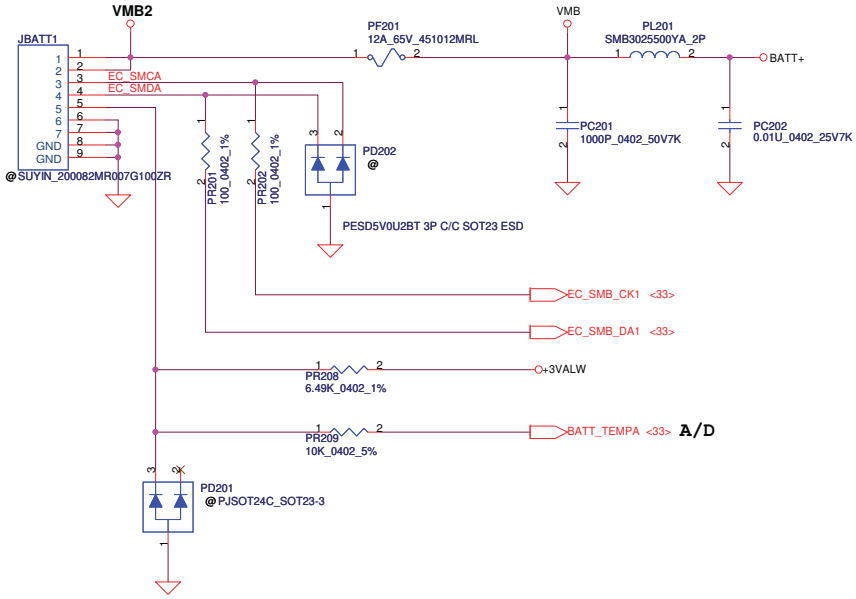
Compal Electronics, Inc.

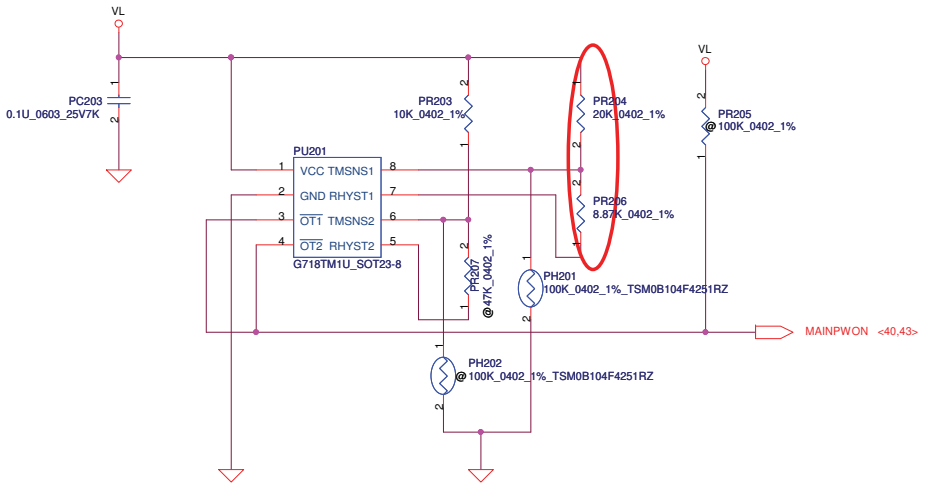
Title: DCIN & DETECTOR

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, March 09, 2010 | Sheet 40 of 48

PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

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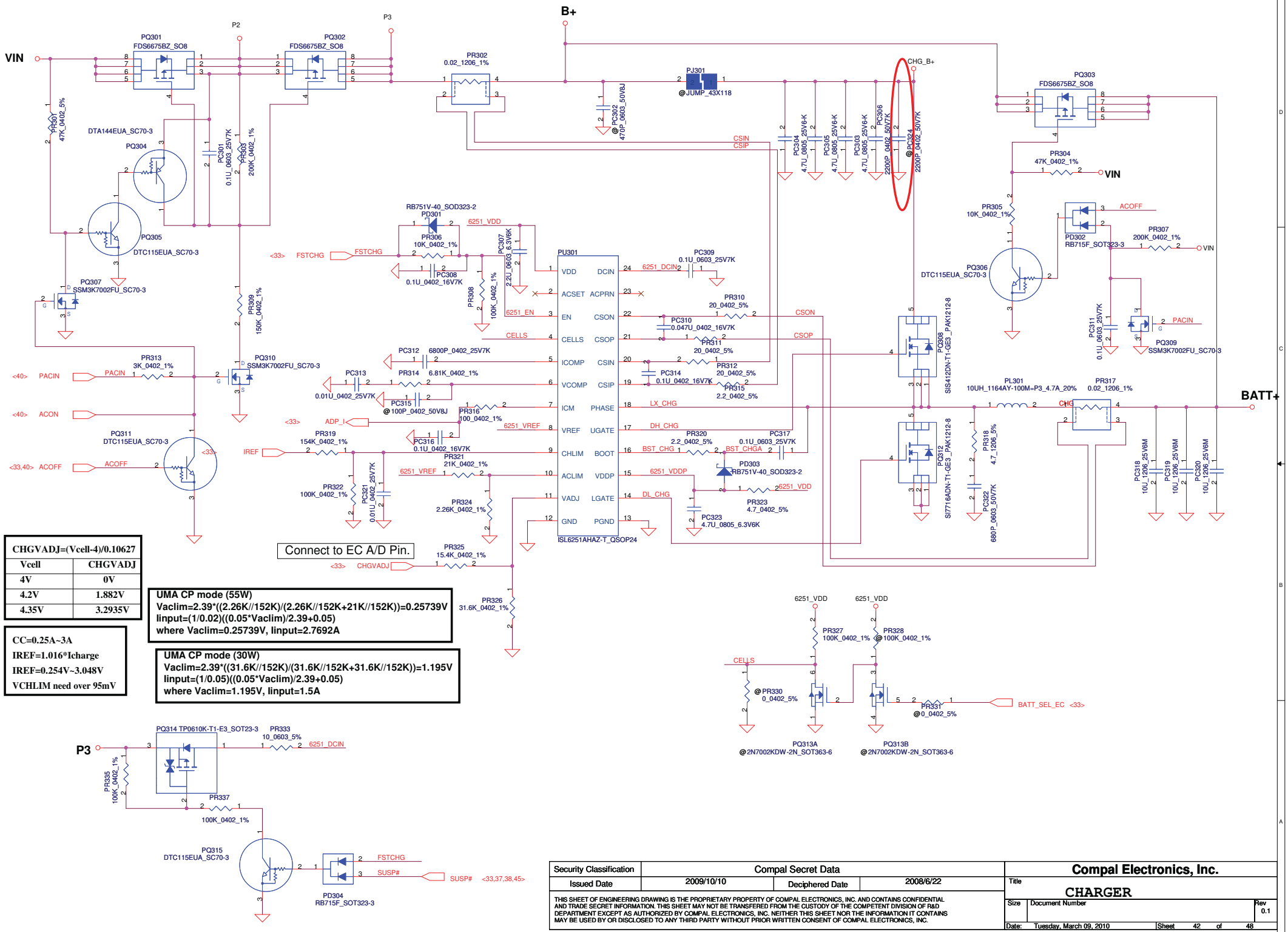


CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

UMA CP mode (55W)
Vaclim=2.39*((2.26K//152K)/(2.26K//152K+21K//152K))=0.25739V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.25739V, Iinput=2.7692A

UMA CP mode (30W)
Vaclim=2.39*((31.6K//152K)/(31.6K//152K+31.6K//152K))=1.195V
Iinput=(1/0.05)((0.05*Vaclim)/2.39+0.05)
where Vaclim=1.195V, Iinput=1.5A

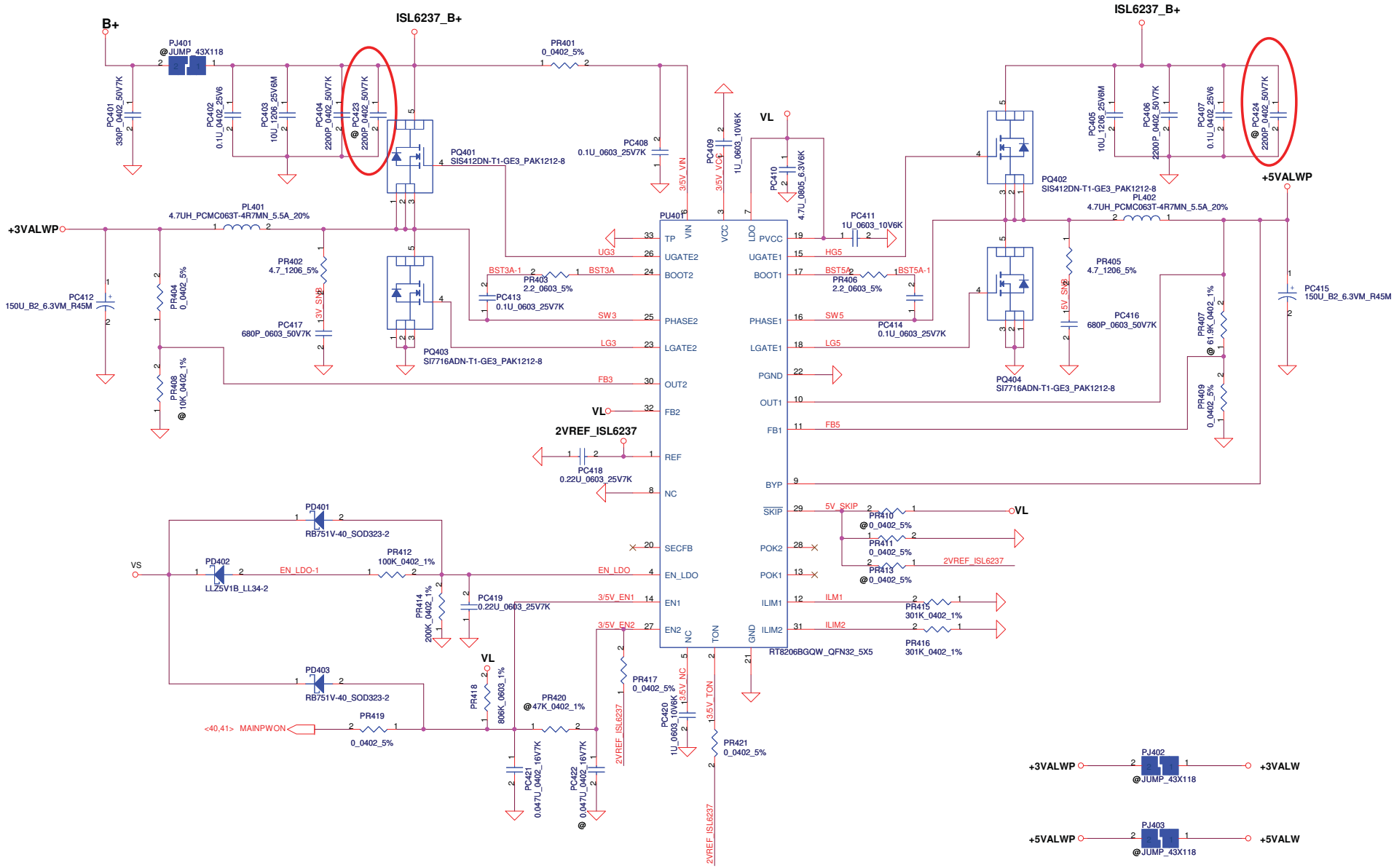
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.1

Date: Tuesday, March 09, 2010 | Sheet 42 of 48



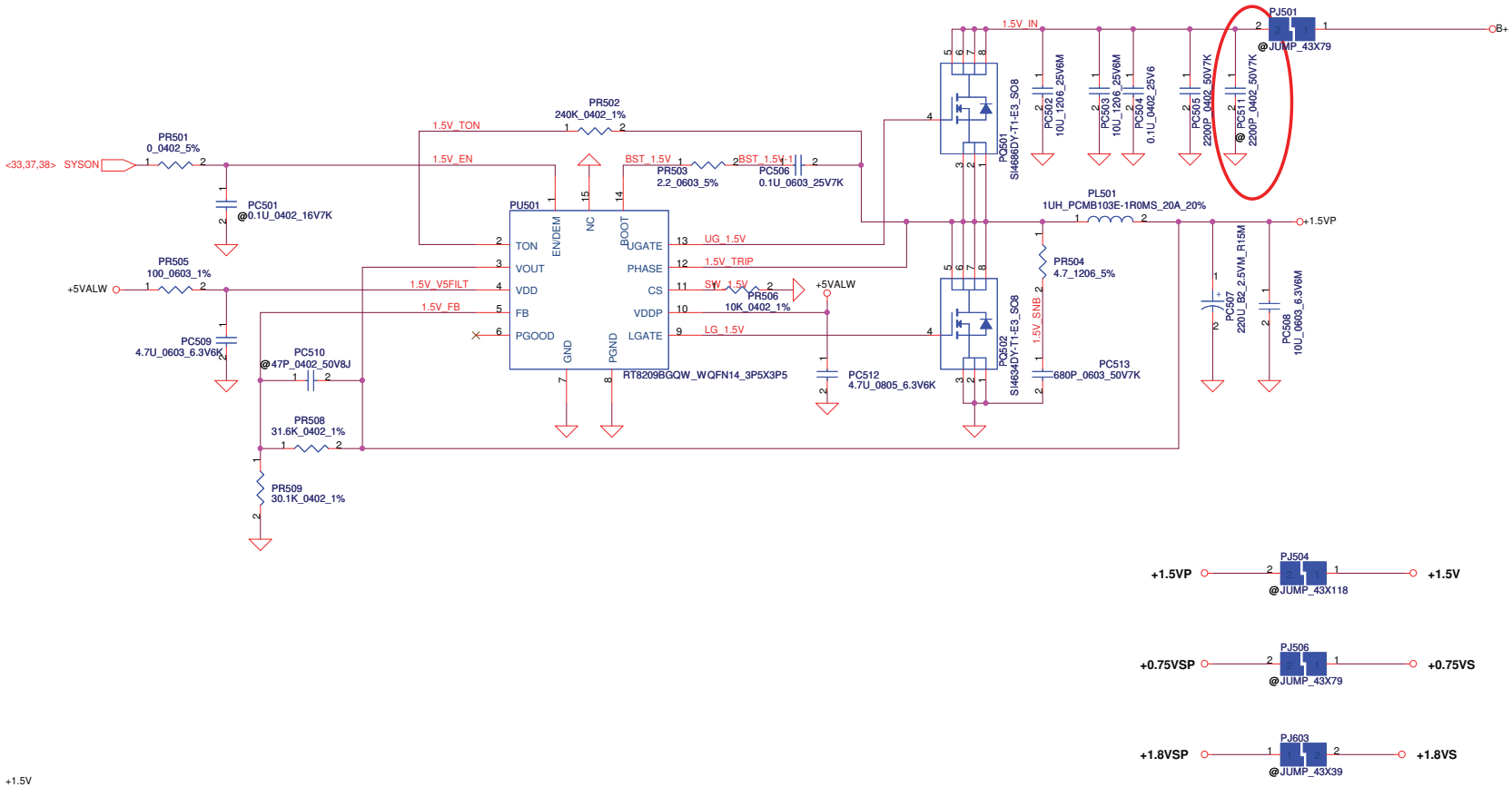
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, March 09, 2010 | Sheet 43 of 48



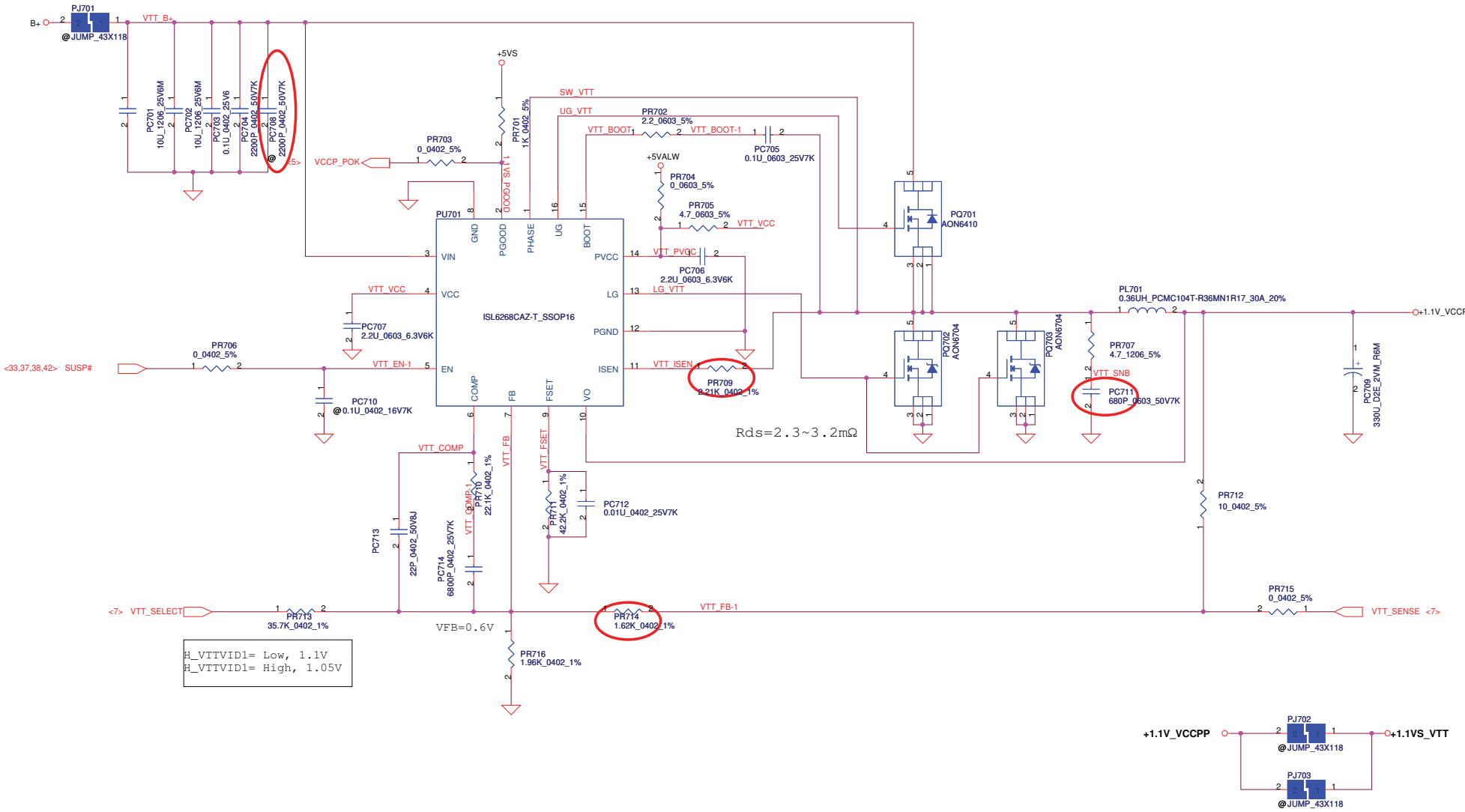
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/0.75V/1.8V

Size	Document Number	Rev
		0.1

Date: Tuesday, March 09, 2010 | Sheet 44 of 48



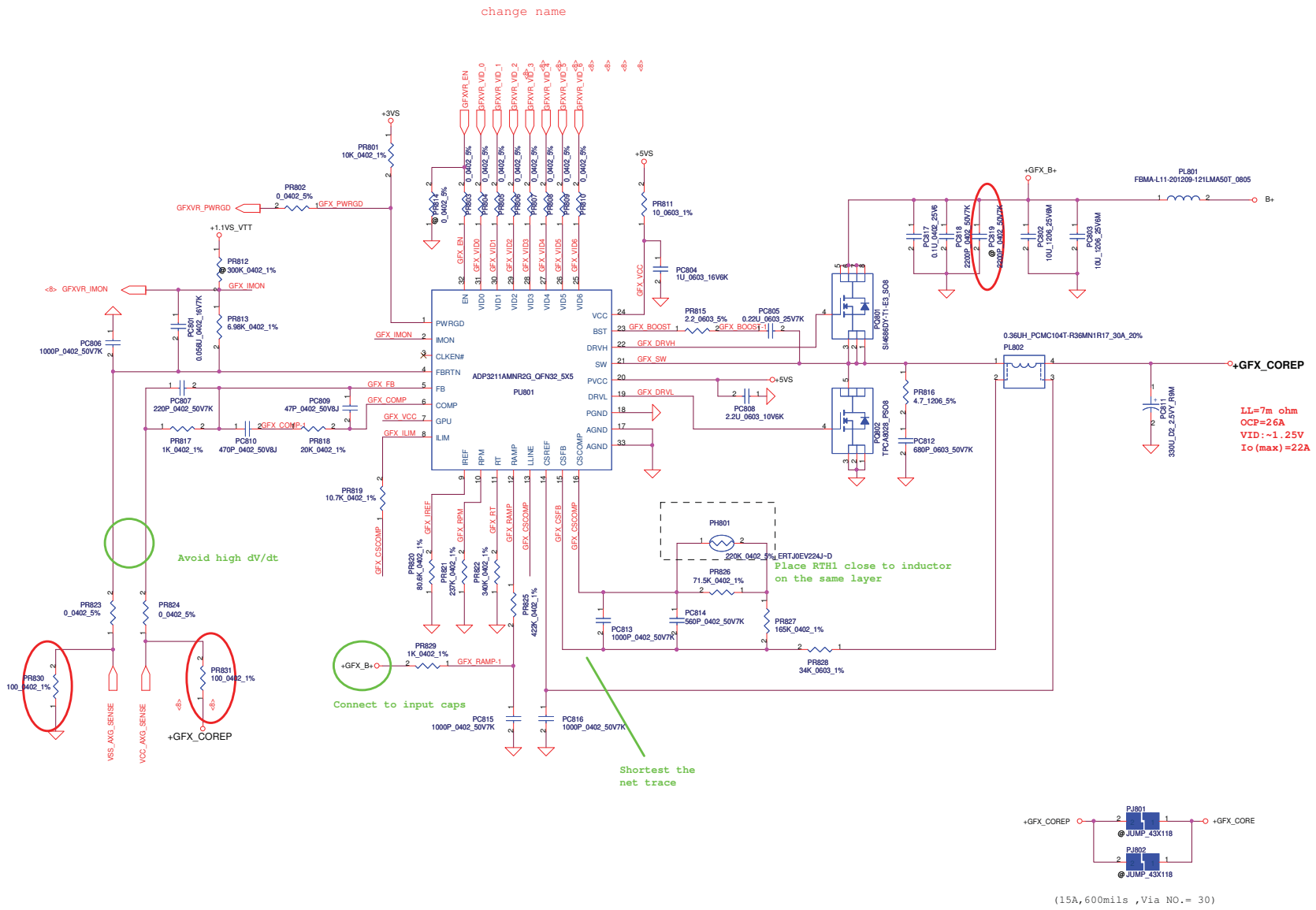
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +1.1VS_VTT

Size	Document Number	Rev
Custom		0.1

Date: Tuesday, March 09, 2010 | Sheet 45 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

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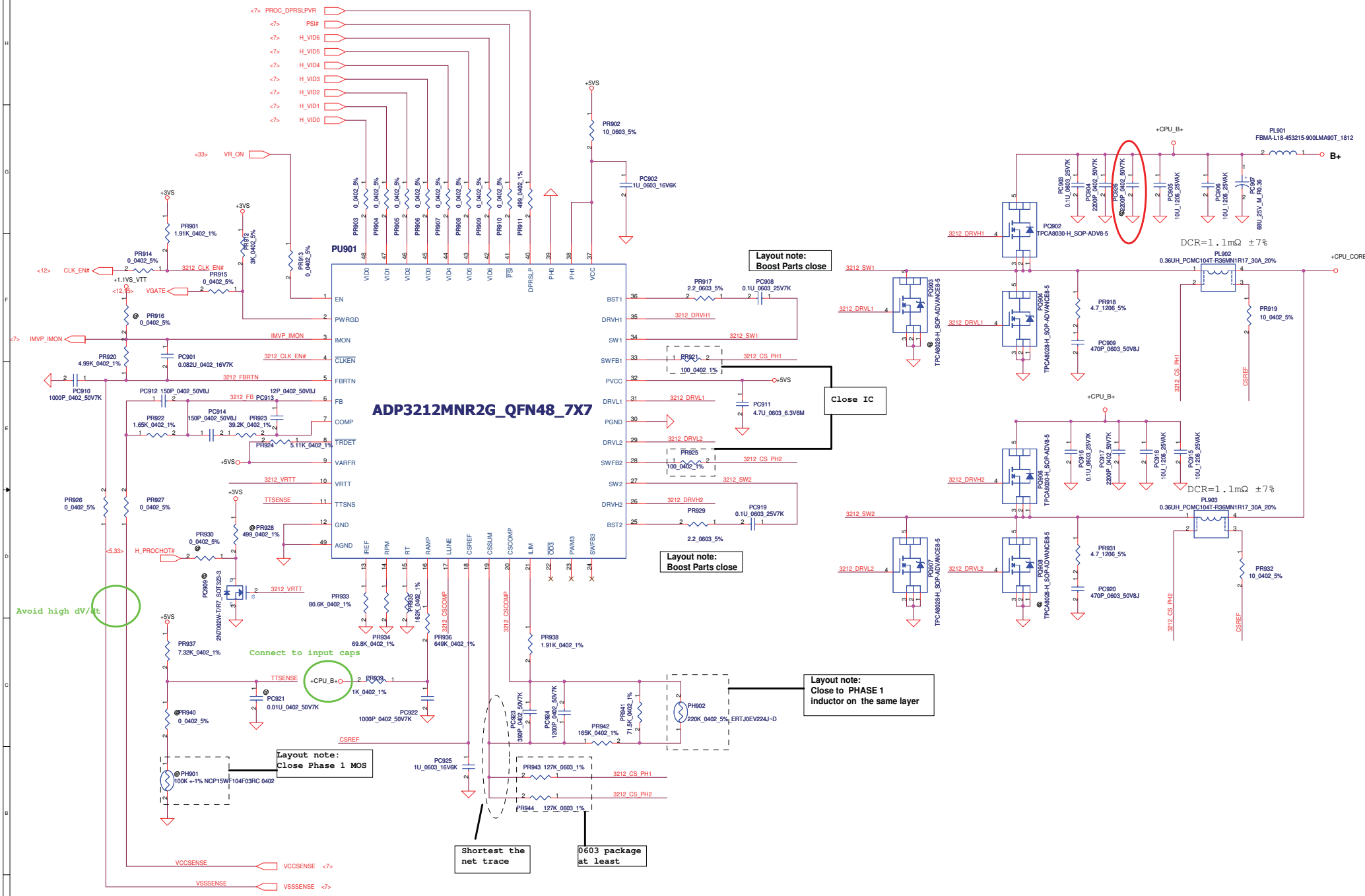
Compal Electronics, Inc.

Title: **GFX_CORE**

Size	Document Number	Rev
		0.1

Date: Tuesday, March 09, 2010 Sheet 46 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

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Compal Electronics, Inc.

Title: CPU_CORE

Size | Document Number | Rev 0.1

Date: Tuesday, March 09, 2010 | Sheet 47 of 48

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For ESD	P41	Add PD202	2009.11.5	EVT
2	For HW request remove +1.05V's JUMP	P41	Remove +1.05V's JUMP	2009.11.6	EVT
3	Because limited high is not enough.	P47	Change PC907 from 220uF to 68uF	2009.11.6	EVT
4	Add PR830,PR831 for GFX_CORE sence.	P46	Add PR830,PR831 for GFX_CORE sence.	2009.11.17	EVT
5	Change Battery connent footprint.	P41	Change Battery connent footprint.	2009.11.17	EVT
6	Change PR521 from 0ohm to 150Kohm. Add PC528 on BOM.	P44	HW request	2009.11.25	EVT
7	Add PD501.	P44	HW request	2009.12.16	DVT
8	Reserve Cap. on B+ for RF.		RF request	2010.1.15	PVT
9	Change PR204 from 21.5Kohm to 20Kohm. Change PR206 from 9.76Kohm to 8.87Kohm.	P41	Thermal team request to change OTP temp. change from 92 degree to 95 degree.	2010.1.22	PVT
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 0.1

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